HP 3000 SERIES II
COMPUTER SYSTEM
MANUAL OF STAND-ALONE DIAGNOSTICS

STAND-ALONE HP 30050A/51A UNIVERSAL IF AND HP 30219A CARD READER PUNCH IF DIAGNOSTIC

Diagnostic No. D435A

30050-90012
Printed in U.S.A.

2/76

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1.0 INTRODUCTION

This manual explains the test program for the PCA (Printed Circuit Assembly) in: the HP 30050A Universal Interface (TTL), or the HP 30051A Universal Interface (Differential), or the HP 30219A Card Reader Punch Interface. The test procedure is the same for the three PCA's unless stated otherwise in this manual.

Most stand-alone diagnostics, including this one, are controlled through either of two switch registers: the Internal Switch Register which is a 16-bit word stored within the program, or the System Switch Register.

2.0 MINI OPERATING INSTRUCTIONS

Install Diagnostic Hardware PCA (HP 30049C).

Cold Load Diagnostic Tape

D100 UNIV. INTERFACE TEST (HP D435A.ØØ.Ø)

Q110 DEVICE NUMBER? (DRT# (DECIMAL))

Q112 INTERRUPT MASK (ENABLED)

Q113 NEGATIVE TRUE? Yes or No

Q114 CHANGE INTERNAL SWITCH REGISTER?

Bit 9 of Internal Switch Register is preset to suppress non-error messages.

Halts to allow switch register setting.

0	Use External Switch Register.
1	Change Section Flag Register.
7	Line Printer.
9	Suppress Non-Error Messages.
10	Suppress Error Message.
11	Loop on Step.
12	Halt After Error.
13	Halt After Step.
14	Halt At End of Section
15	Halt At End of Pass.

Q115 SECTION LIST? Enter Sections to be tested. (1 thru 10)

Q116 READER-PUNCH INTERFACE? Yes or No.

2.1 Section 1 tests the Diagnostic Hardware (HP 30049C).

2.2 Section 2 through 10 will run and cycle without operator intervention.

3.0 REQUIREMENTS

3.1 Hardware Environment

Stand-alone diagnostics are run on a minimum HP 3000 Series II Computer System hardware configuration: the CPU (Central Processor Unit), a magnetic tape unit, and an operator's console (keyboard terminal). A line printer can be included to print data and error messages from the diagnostic.

This diagnostic also requires three other devices: an HP 30049C Diagnostic Hardware assembly, a logic level indicator such as an oscilloscope or a logic probe, and a voltmeter of 2% or better accuracy for use only on the HP 30051A PCA. (The later two devices are used when section 1 is exercised.)

The HP 30049C Diagnostic Hardware is used to simulate a peripheral device connected to the Interface PCA, and is also tested by this diagnostic program. To test one of these PCAs with an actual peripheral device, a diagnostic program for the device must be used instead of this diagnostic.

3.2 Software Environment

Stand-alone diagnostic programs are prepared for loading through SDUP (the Stand-Alone Diagnostic Utility Program). SDUP operates under MPE/3000 (the HP 3000 Multiprogramming Executive Operating System) to produce two magnetic tapes: one that contains a set of cold-loadable CPU diagnostics, and one that contains a cold-loadable relocating loader with an input/output communications module and a set of unit (non-CPU) diagnostics in relocatable form. This diagnostic is a unit diagnostic that is written onto the tape in relocatable form.

4.0 DETAILED OPERATING INSTRUCTIONS

Operation of the diagnostic includes loading and running.

NOTE

When the diagnostic is preconfigured using SDUP, the preconfigured information is placed in the following DB locations.

DB + 0 = Internal Switch Register
+ 1 = DRT # of Interface PCA
+ 2 = Interrupt mask setting
+ 3 = Negative or positive true
+ 4 = Select Sections

4.1 Loading

Before this diagnostic can be loaded from a tape of unit diagnostics in relocatable form, the MPE/3000 system must be shutdown. Further, an HP 30049C Diagnostic Hardware assembly must be installed in place of the peripheral device cable(s) normally connected to the PCA for the Universal Interface to be tested.

4.1.1 Use the SHUTDOWN instructions given in the manual *HP 3000 Multiprogramming Executive Operator's Guide.* Do NOT turn off system power.

4.1.2 Remove the cable(s) for the peripheral device from the PCA to be tested and remove the 2-pin jumper plug from the HP 30049C Diagnostic Hardware.

4.1.3. Install the HP 30049C Diagnostic Hardware component side up in place of the cable(s) for the peripheral device.

4.1.4 Install the 2-pin jumper plug into the two matching holes between connectors J2 and J3 on the PCA to be tested. The lamp labelled +5VDC or POWER ON should light.

4.1.5 Perform this step only if the PCA to be tested is that of an HP 30051A Universal Interface (Differential); otherwise, skip to 4.2.6. Measure the voltages at test points A and B on the HP 30049B Diagnostic Hardware with respect to ground. Each must be in the range +1.0 through +1.2 VDC.

4.1.6 Set the TIMERS switch on the HP 30354A Maintenance Panel to ENABLE if connected.

4.1.7 Mount the tape written by SDUP on the tape device to be used, usually that for DRT Entry Number 6, unit 0.

4.1.8 Set the tape to the LOAD point then set the tape device to ON LINE and to unit 0.

4.1.9 Enter %003006 on the SYSTEM SWITCH REGISTER to cold load the tape. Press together the ENABLE and LOAD switches on the System Control Panel.

4.1.10 Press the RUN-HALT switch; the Computer HALTs with %030361 in CIR (Current Instruction Register).

4.1.11 Set the file number of the diagnostic to be run on the SYSTEM SWITCH REGISTER. Then press RUN-HALT again; the Computer HALTs with %030362 in the CIR. The diagnostic is loaded by the relocating loader, the tape is rewound, and control is passed to the diagnostic. Proceed to "RUNNING," in this text.

4.2 Running

After this diagnostic is loaded by the relocating loader, from a tape written by SDUP, execution is started by three actions:

4.2.1 Press RETURN
The program identification message D1ØØ (see Table 3) is printed.

4.2.2 The Section Ø Configuration Questions below occur only if:

Section Ø of this diagnostic was selected to change the internal switch register.

If the above occurred, action 4.2.3 occurs.

4.2.1 Section Ø Configuration Questions From Terminal

For each question from Section Ø, give a new answer as described here, or strike RETURN (or equivalent) key to use the previous answer or the current entry from preconfiguration (see "PREPARING ON TAPE").

a. To answer Q11Ø DEVICE NUMBER? see the list of input/output devices for the HP 3000 system in use or check the positions of the Device Number Jumpers on the PCA to be tested. Then type the DRT Entry Number for that PCA, in decimal or octal (e.g., in decimal, type 15; in octal, type %17).

b. To answer Q111 TIMER DEVICE NUMBER?? Type the DRT Entry Number for the Timer PCA in the same format as Q11Ø.

c. To answer Q112 INTERRUPT MASK? check the position of the Group Interrupt Mask Jumper on the PCA to be tested, then type the letter or number (D, E, or 0 through 15) of that position.

d. To answer Q113 NEGATIVE TRUE? type NO for Universal Interface PCA 30050-60003. Type YES for Universal Interface PCA 30050-60001 or 30050-60008.

e. To answer Q114 CHANGE INTERNAL SWITCH REGISTER? see Table 1, Switch Register Options, set the SYSTEM SWITCH REGISTER accordingly then press RUN-HALT.

f. To answer Q115 SECTION LIST? see Table 2, Section Number Table, and "PROGRAM ORGANIZATION." Type the numbers of the diagnostic Sections to be run, using these rules:

1. Type only one line of numbers.
2. Type numbers in any order, the numeric order is used.
3. Follow each number except the last with a comma.
4. Duplicate numbers are ignored.
5. Do not enter 1 unless the test equipment specified in 3.1 is available.

g. To answer Q116 READER-PUNCH INTERFACE? type YES if U.I. PCA is used as an interface for Reader Punch. Otherwise type NO.

h. The diagnostic prints D1Ø2 END SECTION Ø and the identification message D1ØØ, UNIV. INTER to signal the end of Configuration Questions.

4.2.3 The diagnostic performs its functions and tests according to the diagnostic Sections and Switch Register Options selected during the preparation or running steps. Further instructions are taken from messages and halt codes generated by the diagnostic and described on the following pages.

5.0 DETAILED DESCRIPTION OF TEST

This program is separated into Sections that perform tests or preparations for tests. Each Section uses primary steps that, in turn, use secondary steps. This text lists each secondary step in numerical order, then each primary step in order of execution, in each Section. The formats of Control Words and Status Words referenced in these lists are shown in Tables 5 and 6 at the end of this text.

5.1 Secondary Steps

Number	Description
ØØ1	Check for Condition Code CCL after a CIO instruction.
ØØ2	" " " " " " " TIO "
ØØ3	" " " " " " " SIN "
ØØ4	" " " " " " " SMSK "
ØØ5	" " " " " " " RIO "
ØØ6	" " " " CCG " " RIO "
ØØ7	" " " " CCL " " WIO "
Ø1Ø	" " " " CCG " " WIO "
Ø11	" " " " CCL " " SIO "
Ø12	" " " " CCG " " SIO "
Ø13	Perform TIO and check the status word.
Ø14	Issue CIO, then TIO, then check the status word.
Ø15	Issue a Control Word to connect all jumpers J2W1 through 10, then issue a series of Control Words to disconnect all but the required jumpers.
Ø16	Issue Selective Interrupt Clear (Control Word bits 2-4) in various combinations, and, for each combination, perform two checks of the status: a. that the bit being tested remains set while other combinations of bits 2-4 are issued; b. that the bit being tested clears when the proper code is issued.
Ø17	Write, then read, a data word by using WIO and RIO instructions, to check for accurate transmittal.

Secondary Steps (cont.)

Number	Description
Ø2Ø	Check data in the buffer after an SIO read operation.
Ø21	Check contents of an SIO program after an SIO operation.
Ø22	Check the status obtained immediately after interrupt through a TIO instruction.

(End of secondary steps.)

5.2 Primary Steps By Test Section

Number	Description
5.2.1 Control Section (unnumbered)	
1ØØ through 1Ø3	Print messages D1ØØ, P1Ø1, D1Ø2, and D1Ø3, of Table 3.
1Ø4 through 1Ø6	Print messages Q1Ø4 through Q1Ø6, of Table 3, and accept user's responses.
5.2.2 Section Ø, Configuration	
11Ø through 114	Print messages Q11Ø through Q112, Q113, and Q114, of Table 3, and accept user's responses.
5.2.3 Section 1, HP 30049C Diagnostic Hardware User Checks	
12Ø	Turn on lamps CONT6 through CONT1Ø in sequence, for user check.
121	Set jumper flip-flops J2W1 through J2W1Ø in sequence, for user checks by a logic probe or an oscilloscope.
122	Set the DEV. END signal for user check by a logic probe or an oscilloscope.
124	Set pins BIT 0 through 15 in sequence, for user checks by a logic probe or an oscilloscope, as described in Table 3 message P124.

(cont.)

Primary Steps (cont.)

Number	Description
5.2.4	Section 2, HP 30049C Diagnostic Hardware Program Tests
13Ø	Issue a Master Clear (Control Word bit 0 set), reset all jumper flip-flops, then check initial status.
131	Test logic paths from Control Word bits 6, 7, and 8 to Device Status Interrupt bits 8, 9, and 10.
132	Test logic paths of Master Clear (Control Word bit 0), PON (Power On) signal, and Power Fail signal to Device Status bits 8, 9, and 10.
133	Test logic path of Control Word bit 6 to Device Flag (Device Status bit 5), and check Sequence Counter states 00 through 10 to 11 through 00 (Device Status bits 3 and 4).
134	Test logic path of Clear Interface signal to Device Status Interrupt bit 12.
135	Test logic path of Transfer Error signal to Device Status Interrupt bit 14.
136	Test Data Out word to Data In word, bit by bit, using WIO and RIO instructions.
137	Test Data Out word bits 11 through 15 to Device Status bits 11 through 15, one bit at a time, using WIO and TIO instructions.
14Ø	Send a Data Out word set to %177777, issue a Master Clear, then check that the Data In word is clear.
5.2.5	Section 3, Data Transfer and Device Status Byte Tests
15Ø	Compare inputs to outputs by using WIO to output data word patterns and using RIO to input them.
151	Similar to step 15Ø, but with Byte Transfer (Control Word bit 13) set.
152	Test Initiate Data Transfer (Control Word bit 5).
153	Test that J2W7 allows byte packing to be verified.
154	Test Control Word bits 6, 7, and 8, in all combinations, to Device Status bits 8, 9, and 10.
155	Test Data Out word bits 11 through 15, in all combinations, to Device Status bits 11 through 15, using WIO, RIO, and TIO instructions.

(cont.)

Primary Steps (cont.)

Number	Description
5.2.6	Section 4, Device Status Interrupt Bit Tests
16Ø	Initialize the Interface Card for the subsequent steps, by enabling jumpers J2W4, 8, and 9, issuing a Master Clear, and selecting Device Status.
161	Set, then clear, Device Status bit 8; check that Status bit 2 (Interrupt Pending) is set on the leading edge of bit 8; check that Device Status Interrupt bit 8 is set.
162	Check that Device Status Interrupt bit 8 remains asserted while Selective Interrupt Clear codes (Control Word bits 2 through 4) are issued for all other Device Status Interrupt bits. Then issue the selective Interrupt Clear code for bit 8 and check that it clears.
163	Disable jumper J2W4, then set, and clear, Device Status bit 8; to check that the Interrupt Pending bit and the Device Status Interrupt bit 8 remain cleared.
16Ø	Repeated.
164	Similar to step 161, but for bit 9 instead of bit 8.
165	Similar to step 162, but for bit 9 instead of bit 8.
166	Similar to step 163, but for jumper J2W8 and bit 9 instead of bit 8.
16Ø	Repeated.
167	Similar to step 161, but for bit 10 instead of bit 8.
17Ø	Similar to step 162, but for bit 10 instead of bit 8.
171	Similar to step 163, but for jumper J2W9 and bit 10 instead of bit 8.
16Ø	Repeated.
172	Set, then clear, together, Device Status bits 8, 9, and 10; check that Device Status Interrupt bits 8, 9, and 10 are set.
173	Issue a Master Clear then check that Device Status Interrupt bits 8, 9, and 10 are clear.
16Ø	Repeated.
172	Repeated.
174	Issue Clear All Interrupts (Control Word bit 1 set) then check that Device Status Interrupt bits 8, 9, and 10 are clear.

(cont.)

Primary Steps (cont.)

Number	Description
5.2.7	Section 5, Interface Interrupt Status Bit Tests
200	Performs data transfer with Data Transfer Interrupt disabled; test status for Interrupt Pending (bit 2) and Data Transfer Interrupt (bit 11) cleared.
201	Similar to step 200, but with Data Transfer Interrupt enabled; test that status bits 2 and 11 are set.
202	Similar to step 162 (in Section 4), but for bit 11 instead of bit 8.
134	(in Section 2) Repeated.
203	Similar to step 162 (in Section 4), but for bit 12 instead of bit 8.
204	Issue an SIN instruction then check status for I/O System Interrupt (bit 13) set.
205	Similar to step 162 (in Section 4), but for bit 13 instead of bit 8.
135	(in Section 2) Repeated.
206	Similar to step 162 (in Section 4), but for bit 14 instead of bit 8.
207	Issue Start Transfer Timer (Control Word bit 15); check Interrupt Status Time Out (bit 15) that it doesn't set within four seconds.
210	Issue Start Transfer Timer again; check that Interrupt Status Time Out does set within seven seconds; then issue a Selective Interrupt Clear code and check that the Time Out bit cleared.
211	Set Interface Interrupt Status bits 11 through 15, issue Clear All Interrupts (Control Word bit 1), and check that those Status bits cleared.
5.2.8	Section 6, Interrupt Tests
220	Issue a Master Clear then issue Control Word bit 14 (Enable Interrupt Request), then perform an SIN instruction; expect an interrupt and test for Status bits 2 and 13 set.
221	Issue an SIN instruction again, but do not expect an interrupt; EXIT after the previous interrupt should have caused a RESET INT signal. Issue a Master Clear then check that Status bits 2 and 13 are clear.
222	Issue Disable Interrupt Request (Control Word bit 14 clear), then perform an SIN instruction; expect no interrupt and test for Status bits 2 and 13 set.
223	Perform this step only if the Group Interrupt Mask Jumper is not in the D (DISABLE) position; issue an SMSK instruction with the appropriate mask bit set (or all bits clear if the GIM Jumper is in the E (ENABLE) position). Then issue an SIN and expect an interrupt; check that Status bits 2 and 13 set.

(cont.)

Primary Steps (cont.)

Number	Description
5.2.8	Section 6, Interrupt Tests (cont.)
224	Perform this step only if the Group Interrupt Mask Jumper is not in the E (ENABLE) position; issue an SMSK instruction with all except the appropriate mask bit set (or all bits set if the GIM Jumper is in the D (DISABLE) position). Then issue an SIN and expect no interrupt; check that Status bits 2 and 13 set.
5.2.9	Section 7, SIO Tests
23Ø	Run an elementary SIO program that performs SENSE orders while setting and clearing interrupt request; check SIO program locations.
231	Run a write-read SIO program, check SIO program status and residue locations and check the read buffer for proper data.
232	Run a write-read SIO program that does repeated long blocks; check Status and the first read buffer.
233	Check the second read buffer from step 232.
234	Abort a write SIO program by using a Clear Interface signal; check that the SIO program did not complete; check Status. (This step not performed for the card reader punch interface.)
5.2.10	Section 8, SIO Device End Tests
24Ø	Run an SIO program to read five words, once to transfer the words then check status and the data, then four more times but assert the Device End signal one word less each time; check each time that the correct number of words were transferred.
241	In the manner of step 24Ø, write five words then check status and the residue.
242	Run an SIO program to read 10 bytes, once to transfer the bytes then check status and the data, then nine more times but assert the Device End signal one byte less each time; check each time that the correct number of bytes were transmitted.
243	In the manner of step 242, write 10 bytes then check status and the residue.
244	Run an SIO program to read with data chaining; after the first word is transferred, assert the Device End signal to end the chain without reading further; the program should continue to do a non-chained five word read. Check the data in the chained buffers for only one word read.
245	Check the data in the unchained buffer used in step 244.

(cont.)

Primary Steps (cont.)

Number	Description
5.2.11	Section 9, Jumper Option Tests
25Ø	Test the Device Flag versus the Device Command signal with Jumpers J2W2, 6, and 10 disconnected and in the Response Mode (Jumper J2W3 disconnected).
251	Same as step 25Ø, but with Jumper J2W6 connected.
252	Same as step 25Ø, but with Jumper J2W2 connected.
253	Same as step 25Ø, but with Jumpers J2W2 and 6 connected.
254	Same as step 25Ø, but with Jumper J2W10 connected.
255	Same as step 25Ø, but with Jumpers J2W6 and 10 connected.
256	Same as step 25Ø, but with Jumpers J2W2 and 10 connected.
257	Same as step 25Ø, but with Jumpers J2W2, 6, and 10 connected.
26Ø	Test the Device Flag versus the Device Command signal with Jumpers J2W2, 6, and 10 disconnected and in the Pulse Mode (Jumper J2W3 connected).
261	Same as step 26Ø, but with Jumper J2W6 connected.
262	Same as step 26Ø, but with Jumper J2W2 connected.
263	Same as step 26Ø, but with Jumpers J2W2 and 6 connected.
264	Same as step 26Ø, but with Jumper J2W10 connected.
265	Same as step 26Ø, but with Jumpers J2W6 and 10 connected.
266	Same as step 26Ø, but with Jumpers J2W2 and 10 connected.
267	Same as step 26Ø, but with Jumpers J2W2, 6, and 10 connected.
27Ø	Test that Jumper J2W1 connected allows Device Status bit 11 to control progress of an SIO program (i.e., controls Service Requests to a Multiplexor Channel).
271	Check that status bit 14 (Transfer Error) was not set when Device End signal and Device Status bit 11 are asserted (i.e., that a spurious Service Request while not in an SIO program did not set a Transfer Error).

(cont.)

Primary Steps (cont.)

Number	Description

5.2.12 Section 10, Basic Functions

3ØØ	Issue a Master Clear (Control Word bit 0 set).
3Ø1	Set up a Sense-End SIO program, then issue an SIO instruction.

5.2.13 Section 12, Device End Functions

32Ø	Set up an SIO program to write five words, then issue a Device End signal after the number of words specified by the user (in Switch Register bits 1, 2, and 3 — see Table 1) have been transferred.
321	Same as step 32Ø, but to read.

5.2.14 Section 13, (none,spare)

5.2.15 Section 15, Halt at a Specific Step

(none)	Delete this Section number 15 from the list of Section numbers to be run (see Switch Register Option 5 and message Q1Ø4), then perform step 1Ø6 in the CONTROL SECTION.

APPENDIX A

Messages and Halt Codes

Messages from the program are of four classes signalled by a prefix letter D, E, P, or Q:

Class	Description
D	Data message, for information only. These messages can be directed to a line printer (if configured for the input/output communications module; see the SDUP manual) or to the user's console (keyboard terminal).
E	Error message, to identify a test failure. These messages can be directed to a line printer or to the user's console.
P	Pause message, to request an action from the user. The diagnostic HALTs, the user performs the action then presses RUN-HALT to resume the program. These messages are always printed on the user's console.
Q	Question message, to request a user's response on the user's console.

Each message is numbered to signal the diagnostic step for which it appears. See Table 3, Program Messages, and "PROGRAM ORGANIZATION."

Halt codes identify errors found in the Cold Loader, the stand-alone relocating loader, or sections and steps in this diagnostic. See Table 4, Halt Codes, and "PROGRAM ORGANIZATION."

APPENDIX B

TABLES

Table 1. Switch Register Options

Bit(s)	Function When Set
0	Used only in the System Switch Register, to override the Internal Switch Register settings made when the program was prepared or started.
1	Change Section Flag register.
4	
5	
6	
7	Use the line printer.
8	
9	Suppress non-error messages.
10	Suppress error messages.
11	Loop one repeat to current step.
12	HALT on error.
13	HALT after step.
14	HALT at end of section.
15	HALT at the end of pass.

Table 2. Section Number Table

Section Number*	Name	Steps
(none)	None, these are secondary steps* that can be part of primary steps* in the following sections or part of other secondary steps.	1 through 22
(none)	Control.	100 through 106
0	Configuration.	110 through 114
1	HP 30049C Diagnostic Hardware User Checks.	120 through 122,124
2	HP 30049C Diagnostic Hardware Program Tests.	130 through 140
3	Data Transfer and Device Status Byte Tests.	150 through 155
4	Device Status Interrupt Bit Tests.	160 through 174
5	Interface Interrupt Status Bit Tests.	200 through 211
6	Interrupt Tests.	220 through 224
7	SIO Tests.	230 through 233**
8	SIO-Device End Tests.	240 through 245
9	Jumper Option Tests.	250 through 271
10	Basic Functions.	300 and 301

*See "PROGRAM ORGANIZATION."

**For the card reader punch interface, these are steps 230 through 233.

Table 3. Program Messages

NOTE: See "Remarks" at the end of this table.

Full Message
Short Message
Comments (where needed)

```
E001  CCL AFTER CIO IN STEP sss IN ppp
  E001  sss sss ppp

E002  CCL AFTER TIO IN STEP sss IN ppp
  E002  sss sss ppp

E003  CCL AFTER SIN IN STEP sss IN ppp
  E003  sss sss ppp

E004  CCL AFTER SMSK IN STEP sss IN ppp
  E004  sss sss ppp

E005  CCL AFTER RIO IN STEP sss IN ppp
  E005  sss sss ppp

E006  CCG AFTER RIO, STATUS = cccccc IN  STEP sss IN ppp
  E006  cccccc sss ppp

E007  CCL AFTER WIO IN STEP sss IN ppp
  E007  sss sss ppp

E010  CCG AFTER WIO, STATUS = cccccc IN  STEP sss IN ppp
  E010  cccccc sss ppp

E011  CCL AFTER SIO IN STEP sss IN ppp
  E011  sss sss ppp

E012  CCG AFTER SIO, STATUS = cccccc IN  STEP sss IN ppp
  E012  cccccc sss ppp

E013  TIO STATUS:  EXPECT e eee eee eee eee eee
                   ACTUAL a aaa aaa aaa aaa aaa IN STEP ppp
  E013  e eee eee eee eee eee eee
        a aaa aaa aaa aaa aaa aaa ppp
```

(cont.)

Table 3. Program Messages (cont.)

```
Full Message
  Short Message
    Comments (where needed)

E014  ISSUED CIO     t ttt ttt ttt ttt ttt
      STATUS: EXPECT e eee eee eee eee eee
              ACTUAL a aaa aaa aaa aaa aaa IN STEP ppp
  E014  t ttt ttt ttt ttt ttt
        e eee eee eee eee eee
        a aaa aaa aaa aaa aaa ppp

E017  WROTE wwwwww
      READ  rrrrrr IN STEP ppp
  E017  wwwwww
        rrrrrr ppp
```

For the word transfer mode.

- or -

```
E017  WROTE www www
      READ  rrr rrr IN STEP ppp
  E017  www www
        rrr rrr ppp
```

For the byte transfer mode.

```
E020  DATA DISCREPANCY IN STEP ppp
      WORD #    yyy    yyy  .  .     yyy
      EXPECT eeeeee eeeeee  .  .  eeeeee
      ACTUAL aaaaaa aaaaaa  .  .  aaaaaa
  E020  ppp
           yyy    yyy  .  .     yyy
        eeeeee eeeeee  .  .  eeeeee
        aaaaaa aaaaaa  .  .  aaaaaa
```

For the word transfer mode: on the user's console, one line of up to five errors is printed; on a line printer, all errors are printed.

- or -

```
E020  DATA DISCREPANCY IN STEP ppp
      BYTE # bbb bbb bbb bbb  .  .  bbb bbb
      EXPECT eee eee eee eee  .  .  eee eee
      ACTUAL aaa aaa aaa aaa  .  .  aaa aaa
  E020  ppp
        bbb bbb bbb bbb  .  .  bbb bbb
        eee eee eee eee  .  .  eee eee
        aaa aaa aaa aaa  .  .  aaa aaa
```

For the byte transfer mode: on the user's console, one line of up to ten errors is printed; on a line printer, all errors are printed.

(cont.)

Table 3. Program Messages (cont.)

```
Full Message
  Short Message
    Comments (where needed)

E021  SIO PROGRAM    EXPECT
      xxxxxx         zzzzzz
      iiiiii         mmmmmm

      xxxxxx         zzzzzz
      iiiiii         mmmmmm

        .              .

        .              .

      xxxxxx         zzzzzz
      iiiiii         mmmmmm
      DRT POINTER INDEXED nn INTO PROGRAM, IN STEP ppp
  E021  xxxxxx zzzzzz
        iiiiii mmmmmm

          .      .

          .      .

        xxxxxx zzzzzz
        iiiiii mmmmmm
        nn ppp

E022  INT STATUS:  EXPECT e eee eee eee eee eee
                   ACTUAL a aaa aaa aaa aaa aaa
   E022  e eee eee eee eee eee
         a aaa aaa aaa aaa aaa

D100  UNIV. INTERFACE TEST     (D335A.nn.n)
  D100 ddd




P101  END STEP ppp
  P101  ppp
    After this message is printed, the program clears the number saved by message
    Q106 below then HALTs.

D102  END SECTION uu
  D102  uu
```

(cont.)

Table 3. Program Messages (cont.)

Full Message
Short Message
Comments (where needed)

D103 PASS vv
D103 vv

Q106 PAUSE AT STEP?
Q106 ?

Q110 DEVICE NUMBER?
Q110 ?
See "RUNNING," in this text.

Q112 INTERRUPT MASK?
Q112
See "RUNNING," in this text.

Q113 NEGATIVE TRUE?
Q113 ?
See "RUNNING," in this text. For the card reader punch interface, type YES.

Q114 CHANGE INTERNAL SWITCH REGISTER
Q114
See "RUNNING," in this text.

(cont.)

Table 3. Program Messages (cont.)

Full Message
  Short Message
    Comments (where needed)

Q114 SECTION LIST?
  Q114 ?
    See "RUNNING," in this text.

P120 CONToo ON, REST OFF
  P120 oo
    Observe lamp CONToo (oo = 06 through 10) on the HP 30049B Diagnostic Hardware. Press RUN-HALT to resume the program.

P121 JUMPER J2Wj LOW, REST HIGH
  P121 j
    Check the logic level of pins J2W1 through J2W1Ø at the left edge of the HP 30049B Diagnostic Hardware, using either a logic probe or an oscilloscope. Press RUN-HALT to resume the program.

P122 DEVICE END ASSERTED
  P122
    Check the DEV. END signal on the HP 30049B Diagnostic Hardware, using a logic probe or an oscilloscope. Press RUN-HALT to resume the program.

P123 PRESS I/O RESET (CONT6-7 GO OFF), RUN
  P123
    Press I/O RESET, check that lamps CONT6 and CONT7 on the HP 30049B Diagnostic Hardware turn off, then press RUN-HALT. The program checks the logic path to device Status bit 8 (and reports an error in a Class E message.)

P124 BIT qq HIGH, REST LOW
  P124 qq
    Check the logic levels of pins BIT 0 through BIT 15 at the right side of the HP 30049B Diagnostic Hardware, using a logic probe or an oscilloscope. Press RUN-HALT to resume the program.

    Note: If the PCA to be tested is an HP 30050A (TTL) specifically wired for negative-true logic, the full message is P124 BIT qq LOW, REST HIGH.

E207 TRANSFER TIMER DELAY <4 SEC
  E207

(cont.)

Table 3. Program Messages (cont.)

Full Message
  Short Message
    Comments (where needed)

E210 TRANSFER TIMER DELAY >7 SEC
  E210

E220 NO INTERRUPT
  E220

E221 ILLEGAL INTERRUPT
  E221

E222 ILLEGAL INTERRUPT
  E222

E223 NO INTERRUPT
  E223

E224 ILLEGAL INTERRUPT
  E224

Remarks:

1. All *sss* numbers identify secondary steps and all *ppp* numbers identify primary steps (see "PROGRAM ORGANIZATION").

2. All message numbers identify the program steps for which the message is printed (see "PROGRAM ORGANIZATION").

3. For all messages without comments in this Table 3, if the program HALTs, perform any desired action(s) — change Switch Register Options, etc. — then press RUN-HALT to resume the program.

Table 4. Halt Codes

HALT Number	$0303xx_8$ (in CIR)	Segment Number[1]	Definition
n/a	n/a	06	Cold Loader is finished; press RUN-HALT.
00	60	20	An unexpected external interrupt has occurred; irrecoverable error.
01	61	22	Stand-alone relocating loader requests a program number; see "LOADING".
02	62	22	Stand-alone relocating loader request the program origin; see "LOADING".
04	64	20	A system clock error has occurred; irrecoverable error.
05	65	n/a	(Spare)
06	66	20	Set the Internal Switch Register as stated in step d of "RUNNING".
07	67	20	Observe lamps on the HP 30049C Diagnostic Hardware (as stated in Table 3 message P12Ø and shown in RB Register).
10	70	20	Check jumpers on the HP 30049C Diagnostic Hardware (as stated in Table 3 message P121 and shown in RB Register).
11	71	20	Check DEV. END on the HP 30049C Diagnostic Hardware (see Table 3 message P122).
12	72	20	Press I/O RESET, check that lamps CONT6 and 7 on the HP 30049C Diagnostic Hardware turn off, then press RUN-HALT (see Table 3 message P123).
13	73	20	Check pins on the HP 30049C Diagnostic Hardware (as stated in Table 3 message P124 and shown in RB Register).
14[2]	74	20	Section *uu* has finished; see *uu* or a related step number in the RA Register; also see the RB, RC, and RD Registers as defined below[2]. Change Switch Register Options, etc., then press RUN-HALT.
13 (cont.)	75	20	Step *sss* or *ppp* has finished; see the RA Register, bits 1 through 6 for the secondary step number *sss,* and bits 8 through 15 for the primary step number *ppp;* also see the RB, RC, and RD Registers as defined below[2]. Change Switch Register Options, etc., then press RUN-HALT.

[1] The segment number can be seen in the Computer's Status Register bits 8 through 15.

[2] At HALTs 14, 15, and 16 these Registers contain data:

RB – Interface/Interrupt Status Word (see the Maintenance Manual for the Card being tested).
RC – The data word read, where applicable.
RD – The data word written, where applicable.

Table 4. Halt Codes (cont.)

HALT Number	0303xx_8 (in CIR)	Segment Number[1]	Definition
12	76	20	This program has found an error; the RA, RB, RC, and RD Registers are as defined above for HALT 15. Change Switch Register Options, etc., then press RUN-HALT.
15	77	20	This program has completed a pass. To run it again, decide whether or not to change Switch Register Options (see Table 1), then press RUN-HALT.

[1] The segment number can be seen in the Computer's Status Register bits 8 through 15.

[2] At HALTs 14, 15, and 16 these Registers contain data:

RB – Interface/Interrupt Status Word (see the Maintenance Manual for the Card being tested).

RC – The data word read, where applicable.

RD – The data word written, where applicable.

Table 5. Control Word Format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Bit(s)	Function(s), When Set (or as otherwise stated)
0	Master Clear. Initializes the Interface Card; similar to a user pressing the I/O RESET switch on the Computer.
1	Clear All Interrupts. Clears all processes on the Card that could initiate an interrupt request.
2, 3, 4	Selective Interrupt Clear. Programmed in octal code, to clear each of eight processes that can initiate an interrupt request: **Bits 2 3 4** — **Process (Interrupt Status Bits) Cleared** 0 0 0 — None, inactive state. 0 0 1 — Transfer Timer and Transfer Error (15 and 14). 0 1 0 — I/O System (13). 0 1 1 — Clear Interface (12). 1 0 0 — Data Transfer (11). 1 0 1 — (8). 1 1 0 — (9). 1 1 1 — (10).
5	Initiate Data Transfer. Must be set by a CIO instruction before every RIO instruction, to signal the Card to accept another data word from a peripheral device.
6 through 10	Device Control. Available to control a peripheral device, through output or differential line drivers.
11	Data Transfer Interrupt. Issues an interrupt request at the end of each data transfer sequence.
12	Interrupt/Device Status. Selects the function of status word bits 8 through 15: when set, those bits show peripheral device status; when clear, those bits show interrupt status.
13	Enable Byte Transfer. Enables byte transfers, for packing during read and unpacking during write.
14	Enable Interrupt Request. Enables the Card to request an interrupt.
15	Enable Transfer Timer. Starts the transfer timer.

Table 6. Status Word Formats[1]

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Bit(s)	Function(s), When Set (or as otherwise stated)
0	SIO OK. Signals that an SIO instruction can be executed.
1	RIO, WIO OK. Signals that an RIO or a WIO instruction can be executed.
2	Interrupt Pending. Signals that at least one of eight Interface Card operations possible is requesting interrupt.
3 and 4	Sequence Counter. Indicates a position in the data transfer sequence, for trouble-shooting: **Bits 3 4** — **Position** 0 0 — COUNT 0, no action has occurred. 1 0 — COUNT 1, operation request to device issued. 1 1 — COUNT 2, device operation started. 0 1 — COUNT 3, operation request to device to begin transfer of second byte issued.
5	Device Flag. Signals the start of an I/O operation by the device.
6	Interrupt/Device Status: When clear, signals the Interrupt Status definitions of bits 8 through 15 of the status word are used; when set, signals the Device Status definitions are used.
7	None, permanently clear.
8, 9, 10	Interrupt Status bits. Device Status Interrupts, set through jumper wires (when installed in connector J2) J2W4, J2W8, and J2W9, respectively, by the leading edge of Device Status bits (signals) 8 and 9, and the trailing edge of Device Status bit (signal) 10, respectively; and cleared by Control Word bits (signals) 2, 3, and 4, described in Table 5. Device Status bits. Signal status of the device and set Interrupt Status bits 8, 9, and 10, as described above.
11	Interrupt Status bit. Data Transfer Interrupt, enabled when Control Word bit 11 is set, requests an interrupt when data transfer is complete. Device Status bit. Use is determined by the device.
12	Interrupt Status bit. Clear Interface Interrupt, valid only during an I/O program when a multiplexer channel is controlling the Card; the device can completely abort the I/O program and enable this interrupt by sending a clear interface signal to the Card. Device Status bit. Use is determined by the device.
(cont.)	

[1]Three fields are included: bits 0 through 5 are always Interface Status, bits 8 through 15 are determined by bit 6 as defined above.

Table 6. Status Word Formats[1] (cont.)

Bit(s)	Function(s), When Set (or as otherwise stated)
13	Interrupt Status bit. I/O System Interrupt, signals a direct SIN instruction or an I/O program INTERRUPT order was executed and an interrupt was requested. Device Status bit. Use is determined by the device.
14	Interrupt Status bit. Transfer Error Interrupt, signals one of three errors in transfer of data between the Card and the computer: a. An illegal address, or b. A memory parity error, or c. A parity error on transfer to or from memory. This bit must be cleared before another data transfer can occur. Device Status bit. Use is determined by the device.
15	Interrupt Status bit. Time Out Interrupt, set if the transfer timer delay expires (is not cleared by Control Word bit 4 five seconds after it is set by Control Word bit 15); an interrupt is requested. Device Status bit. Use is determined by the device.

[1]See bit 6, on the previous page.