HEWLETT PACKARD

General Purpose Register Diagnostic

Reference Manual

For HP 12551B/12554A/12566B/C 12589A/12597A/12602B/12849A/ 12875B/12930A Interfaces and HP 1000 Series Computers.

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PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, Update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past Updates, however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all Updates.

To determine what software manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

First Edition	Aug 1978	
Update 1	Apr 1982	Adds 12566C strapping
Reprint	Apr 1982	Update 1 incorporated

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ILLUSTRATIONS

TABLES

SECTION I
INTRODUCTION

1-1. GENERAL

This diagnostic tests several types of interface boards used with the HP 1000 M/E/F-Series Computers.* A list of the interfaces that can be tested by this diagnostic, the tests executed and the required test connectors are listed in table 1-1.

1-2. REQUIRED HARDWARE

The following hardware is required:

a. An HP 1000 M/E/F/Series Computer with at least 4K of memory.

b. One of the interface cards listed in Table 1-1. Each of the interfaces that may be tested by this diagnostic has circuit jumpers that can be installed in different positions, according to the specific application of the card. The normal installation positions for those jumpers are described in the *Operating and Service Manual* for the particular card. However, when this diagnostic program is used to test a given card, some of the normal jumper installations may have to be changed temporarily while the tests are run or between the execution of some tests. At the end of the diagnostic they must be returned to the position required by the specific application. The various jumper installations allowed for the diagnostic tests are listed in appendix A of this manual.

c. The appropriate test connector must be installed on all cards that are to be tested with this diagnostic (see Note for exceptions). Table 1-1 lists the required test connector for each of the interface cards.

d. A disgnostic input device used only for loading the configurator and the diagnostic.

e. A console device with interface for message reporting (recommended but not required).

f. When running diagnostics on an HP 12930A Universal Interface board, an HP 12777A, Priority Jumper board is required.

*Except where otherwise noted, when the HP 1000 M/E/F-Series is mentioned in this manual, it includes the 21MX, 21MX M-Series, 21MX E-Series, HP 1000 M-Series, HP 1000 F-Series Computers and also applies to the 2100 A/S Computer. It does not include or apply to the HP 1000 A/L Series Computer.

Table 1-1. Interface Board, Test Execution and Test Connector

INTERFACE BOARD		TEST EXECUTION		TEST CONNECTOR
NO.	NAME	STANDARD TEST RUN	SPECIALLY SELECTABLE TEST	
HP 12551B HP 12551B-001	Relay Register Relay Register with Storage Read-back	TST 00 01	TST 02 TST 12	Both boards should be tested with a special test and display connector which is not supplied with either one of the two boards. This special connector can be built by the user. The electrical lay-out is shown in Appendix B figure B-3. The connector is required to run TST 02.(See Note)
HP 12554A HP 12554A-001	16 Bit Duplex Register Positive Logic 16 Bit Duplex Register Negative Logic	TST 00 03	TST 12	Part no. 1251-0332 (supplied with board).
HP 12566B/C HP 12566B/C-001 HP 12566B/C-002 HP 12653A HP 12875B	Microcircuit Interface Ground True Microcircuit Interface Ground True, Party Line Microcircuit Interface Positive True Microcircuit Interface Special 2767A Line Printer Interface Processor Interconnect Kit	TST 00 03	TST 12	Part no. 1251-0332 (supplied with board). The user has to modify that test connector by connecting pin Z/22 to pin AA/23 via a solder joint as shown in Appendix B figure B-1. (See Note)
HP 12597A HP 12597A-001[1]	8 Bit Duplex Register Positive Logic 8 Bit Duplex Register Negative Logic	TST 00 03	TST 12	Part no. 1251-0332 (supplied with board).
HP 12602B	Optical Mark Reader Interface	TST 00 03	TST 12	Part no. 1251-0332 (supplied with board).
HP 12849A HP 12849A-001	Controller Microcircuit Interface, Ground True Controller Microcircuit Interface, Positive True	TST 00 03 04	TST 12	Requires two different test connectors as follows: Test connector HP 12849-60003 which is supplied with the board as shown in Appendix B figure B-1 is used for TST 03. Test connector HP 12849-60004 which is supplied with the board as shown in Appendix B figure B-2 is used for TST 04.

[1]The HP 12597A-002, -003, and -005 Interface diagnostics are described in the Tape Reader/Punch subsystems diagnostic manual (part number 12597-90031), although this diagnostic may be used to check just the interface cards.

Table 1-1. Interface Board, Test Execution and Test Connector (Continued)

INTERFACE BOARD		TEST EXECUTION		TEST CONNECTOR
NO.	NAME	STANDARD TEST RUN	SPECIALLY SELECTABLE TEST	
HP 12589A	Automatic Dialer Interface	TST 00 05 06 07	TST 12	ACU — test connector part no. 12589-6005 (supplied with the board).
HP 12930A	Universal Interface Bit Differential Driver	TST 00[3] 03 08	TST 12	Part no. 12930-60013[2] (supplied with standard board 12930A).
HP 12930A-001 and -003	Universal Interface Bit Ground True Driver	09 10 11		Part no. 12930-60014[2] (supplied with ground true board 12930A-001 and -003).
HP 12930A-002	Universal Interface Kit Positive True Driver			Part no. 12930-60015[2] (supplied with positive true board 12930A-002).

[2] With this diagnostic release the test connectors for the three universal interface boards were modified. 12930-60013 replaces 12930-60006, 12930-60014 replaces 12930-60008 and 12930-60015 replaces 12930-60009. This diagnostic will fail in TST 11 if the old test connectors are used. The old connectors can easily be converted by the user to conform to the new ones as shown in Appendix B, figures B-4, B-5 and B-6.

[3] TST 00 is executed twice, once on the data channel SC, once on the command channel SC of the 12930 UI board.

NOTE

The following 2 boards can be tested without a test connector provided the user is willing to accept certain short comings or inconveniences.

1. Relay Register Board HP 12551B and HP 12551B-01: The standard pattern test, TST 01 can be exercised without the special test connector (see paragraph 4-3). However the non-standard command test, TST 02 requires the special test connector (see paragraph 4-4).

2. Processor Interconnect Kit HP 12875B can be tested like a 12566B/C interface board in which case a test connector is required (part no. 1251-0332) or it can be tested as a processor interconnect kit with a central processor, two interconnect boards and an I/O processor (see paragraph 4-15).

1-3. REQUIRED SOFTWARE

The following software is required:

a. The Diagnostic Configurator (part numbers listed below) is used for equipment configuration and as a console device driver.

Binary	object tape	Part No. 24296-60001
Manual		Part No. 02100-90157

b. General Purpose Register Diagnostic binary object tape Part No. 24391-16001.

The Diagnostic Serial Number (DSN) for this diagnostic resides in memory location 126 (octal). The DSN is 143300 (octal).

NOTE

S-REG and Switch Register, P-REG and P-register, etc., used in this manual are synonymous.

PROGRAM ORGANIZATION

SECTION II

2-1. ORGANIZATION

This diagnostic program consists of an Initialization and Control section, 12 tests, and a Pseudo Operator Design section (Opdesign). The Initialization and Control section accepts the select code, board type, and options required by the tests. The tests are named as follows:

Basic I/O (Flag and Interrupt logic) — (TST00)

Pattern Test (Relay Register Interface only) — (TST01)

Command Test (Relay Register Interface only) — (TST02)

Data Buffer Test (all interfaces except Relay Register) — (TST03)

Control Signals Test (HP 12849A Interface only) — (TST04)

Input/Output Test (Automatic Dialer only) — (TST05)

Multi-line Operation Test (Automatic Dialer only) — (TST06)

Dialer Turn-on, Wait, Turn-off Test (Automatic Dialer only) — (TST07)

Command/Status and Data Test without STC (Universal Interface board only) — (TST08)

Command/Status and Data Test with STC (Universal Interface board only) — (TST09)

Command Channel Test (Universal Interface board only) — (TST10)

Data Channel and Power On Circuit Test (Universal Interface board only — (TST11)

Pseudo Operator Design (Opdesign) — (TST12)

2-2. TEST CONTROL AND EXECUTION

The diagnostic outputs a title message to the console device and then executes the tests according to the options selected on the Switch Register. The diagnostic control section primarily checks Switch Register bits 15, 13, and 12.

The diagnostic also keeps count of the number of passes that have been completed and will output the pass count at the completion of each pass (if Switch Register bit 10 is clear). The count will be reset only if the diagnostic is restarted.

Test sections are executed one after the other in each diagnostic pass. User selection or default will determine which test sections will be executed. Switch Register bit 9 is used to indicate that test selection is desired. (Refer to paragraph 3-3.)

By setting Switch Register bit 8 the Preset test in BI-O is suppressed. When Switch Register bit 12 is set the tests that are selected will be repeated and the Preset test is skipped.

Table 2-1 shows the approximate execution time of each test on an HP 1000 M-Series Computer. The execution time will be less on a 2100A/S, HP 1000 E/F-Series Computer.

Table 2-1. Approximate Execution Time of Each Test on an M-Series Computer

TEST NO.	EXECUTION TIME IN SEC
00	Depends on operator response
01	Depends on operator response
02	Depends on operator response
03	10 sec
04	Depends on operator response
05	<1 sec
06	Depends on operator response
07	Depends on operator response
08	12 sec
09	> 20 sec. Depends on operator response
10	> 7 sec. Depends on operator response
11	> 10 sec. Depends on operator response
12	Depends on operator response

2-3. MESSAGE REPORTING

There are two types of messages output for this diagnostic: error and information. Error messages are used to inform the operator when the interface fails to respond to a given control or sequence. Information messages are used to inform the operator of the progress of the diagnostic or to instruct the operator to perform an operation related to a function of the interface. In the latter case, an associated halt will occur to allow the operator time to perform the function. The operator must then press RUN. If a console device is used, the printed message will be preceded by the letter E (error) or the letter H (information) and a number (in octal). The number is also related to the halt code when a console device is not available. Examples of error and information messages are as follows: (Specific meanings are listed in section IV.)

Example — Error with halt

Message: E026 INT EXECUTION ERROR
Halt Code: 102026 (octal) (T-register or Memory Data Register)

Example — Information with halt

Message: H024 PRESS PRESET (EXT & INT), RUN
Halt Code: 102024 (octal)

Example — Information only

Message: H025 BASIC I/O COMPLETED
Halt Code: None

Error messages can be suppressed by setting Switch Register bit 11 and error halts can be suppressed by setting Switch Register bit 14. This is useful when looping on a single section that has several errors.

Information messages are suppressed by setting Switch Register bit 10.

2-4. DIAGNOSTIC LIMITATIONS

Interface capability for receiving, passing, and denying priority (priority string logic) is not completely checked by this diagnostic. If the interface does not receive priority (i.e., PRH from the next lower select code) an error E014 NO INT will occur. To check this, remove an interface of a lower select code and run the Basic I/O test. the above mentioned error should occur. Checking the interface ability to pass or deny priority is beyond the scope of this diagnostic.

Direct Memory Access (DMA) in the 2100A/S or Dual Channel Port Controller (DCPC) in the HP 1000 M/E/F-Series Computers, portion of the interface under test is checked by its own diagnostic.

The diagnostic does not check the gating functions of jumpers W9 through W12 on the HP part number 12554-60023 (HP 12554A) and 12554-60024 (HP 12554A-001) cards, or jumpers W6 through W8 on HP part number 12566-60024 (HP 12566B/C-001) and 12566-60025 (HP 12566B/C-002) cards.

Also, the diagnostic does not check the Device Command flip-flop reset signal carried (when CLC or CRS signals occur) by jumper W13 on the HP part number 12554-60023 (HP 12554A) and 12554-60024 (HP 12554A-001) cards, or jumper W9 on the HP part number 12566-60024 (HP 12566B/C-001) and 12566-60025 (HP 12566B/C-002) cards.

For the HP 12849A Interface, the diagnostic does not check the gating functions of jumpers W6 through W8, the Device Command flip-flop reset signal carried by W9 when CLC or CRS* signals occur, the false condition of buffered control signals PON* and CTL*, nor the buffered POPIO signal.

The diagnostic does not check the Device Encode or Device Flag circuitry on cards HP part number 12551-6001 (HP 12551B) or 12551-6002 (HP 12551B-01) if the display connector is not used (see table 1-1).

*CRS=Control Reset, PON=Power On Normal, CTL=Control Flip Flop.

OPERATING PROCEDURE

SECTION III

3-1. OPERATING PROCEDURES

Remove the interface board to be diagnosed and set the jumpers or switches on the interface board (if applicable) as specified in appendix A. Install the appropriate test connector per table 1-1. Install the interface board to be diagnosed into the desired I/O channel. If a HP 12930 Universal Interface Board is tested the next higher I/O channel (lower priority channel) must be loaded with a 12777A Priority Jumper card because the 12930 UI board occupies two select codes.

If an HP 12930 Universal Interface Board is tested, set power fail/auto restart switch as follows:

For 2100A/S computers — On top of I/O Control Card A7, set ARS/$\overline{\text{ARS}}$ switch S1 to ARS (auto restart position).

For 21MX and HP 1000 computers — At rear of CPU PCA A1, set ARS/$\overline{\text{ARS}}$ switch A1S2 (right-hand switch when viewed from rear of PCA) to ARS (right-hand position). This is the auto restart position.

NOTE

When testing an HP 12930, it is advantageous to put the board on an extender board so that the switches (see table A-7) can be easily accessed.

A flowchart of the operating procedures for loading the Diagnostic Configurator and this diagnostic is provided in figure 3-1.

Table 3-1 is used in conjunction with the flow chart to configure the diagnostic program for the interface to be tested.

The default case (bits 7 through 15 cleared) is for the HP 12554A, HP 12566B/C, HP 12602B or the HP 12875B interface.

Table 3-2 is used during execution of the diagnostic to allow the operator to control the sequence of execution and to set up the desired diagnostic options.

Table 3-3 summarizes test selection via the A-REG and is discussed further in paragraph 3-3.

For Pseudo Opdesign instructions refer to paragraph 4-14.

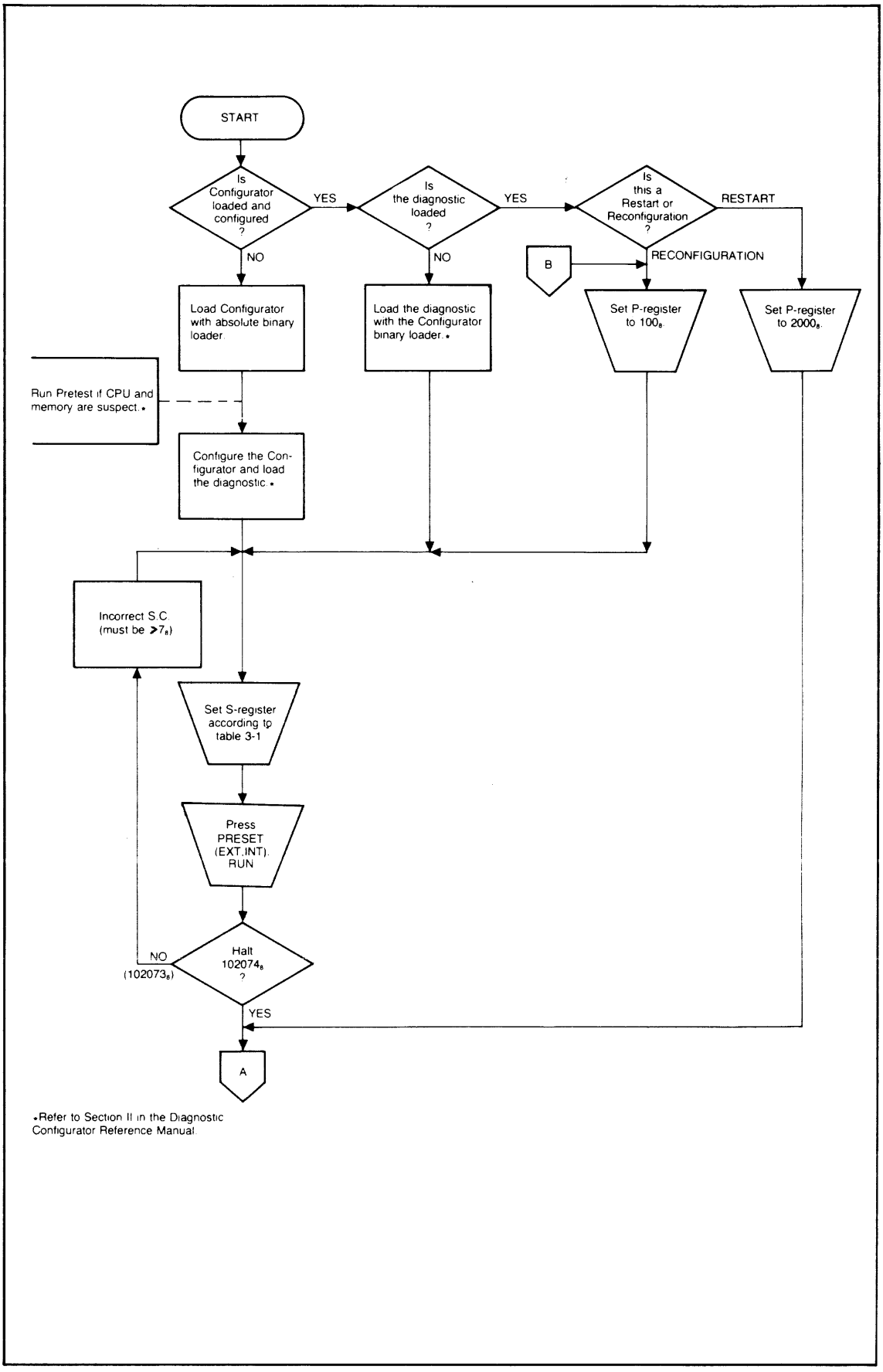

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Figure 3-1. Operating Procedure Flowchart (Sheet 1 of 2)

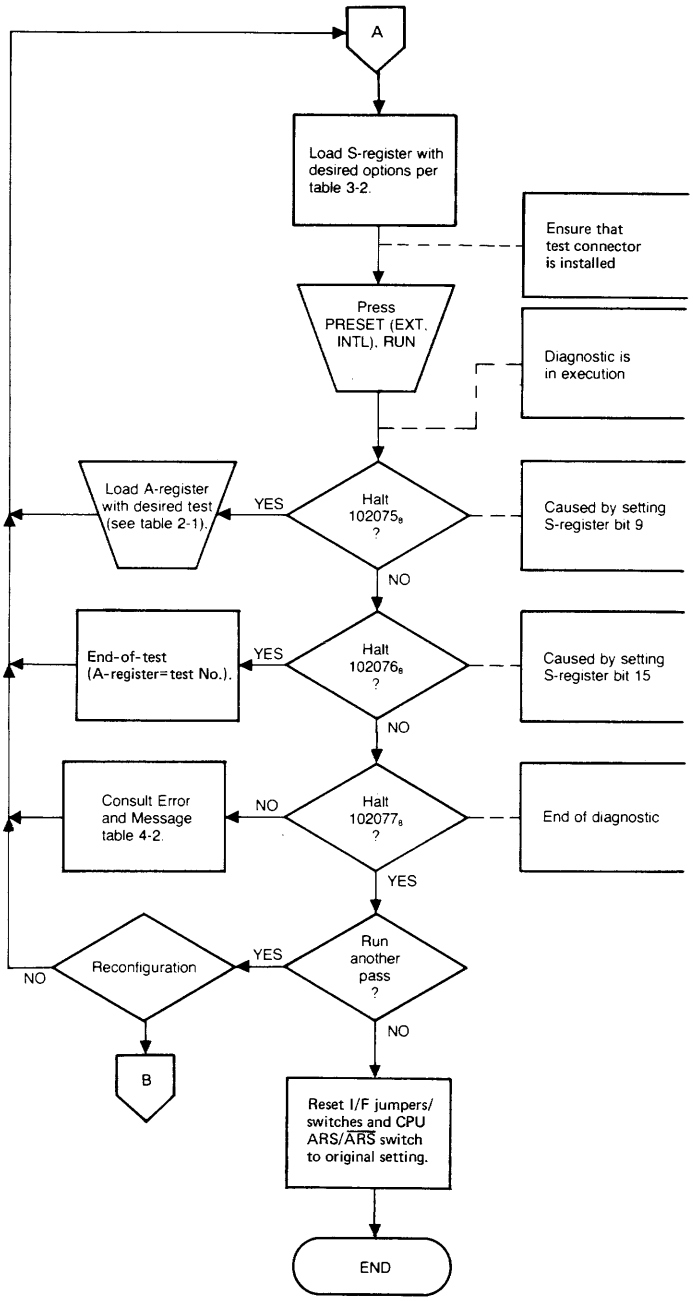

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Figure 3-1. Operating Procedure Flowchart (Sheet 2 of 2)

Table 3-1. Select Code and Interface Type Entered via S-Register

BIT		MEANING IF SET
0-5	S.C.	Set to select code of interface under test.
6		Reserved.
7	HP 12930A	Universal interface kit is under test.
8	HP 12589A	Automatic Dialer interface kit is under test.
9	HP 12551B	Relay Register has data read-back capabilities (12551B-01).
10		Relay Register is under test (12551B or 12551B-01).
11	HP 12597A	8-bit duplex register interface bit is under test (12597A ground true/ positive, 12597A-001 negative true/ground, or 12597A-002, -003 or -005).
12	HP 12849A	Set if W5 of 12849A is removed (W4 must be in positive B), cleared if W5 is installed (W4 may be in positive A or B).
13		Set if 12849A-001, positive true, cleared if 12849A, ground true.
14		Set if W10 on 12849A is in positive B (PON ground true), cleared if W10 on 12849A is in positive A (PON positive true).
15		Controller Microcircuit interface kit 12849A or 12849A-001 is under test.

The default case (bits 7 through 15 cleared) is for the HP 12554A, HP 12566B/C, HP 12602B or the HP 12875B interface.

3-2. RUNNING THE DIAGNOSTIC

At the completion of each pass of the diagnostic, the pass count is output to the console, If Switch Register bit 12 was not set, the computer will halt with 102077 in the Memory Data Register (T-register). At this point the A-register contains the pass count. The operator can press RUN to execute another pass.

If bit 12 is set it causes the diagnostic to loop on the selected tests. Bit 13, when set, is used to loop on a given test that is running at the time, as specified in paragraph 3-3 and table 3-2. Bit 15, if set, will halt the computer at the completion of a test.

If a trap cell halt occurs (106077) the operator must determine the cause of either the interrupt or the transfer of control to the location shown in the M-REG. The program may need to be reloaded to continue.

When a halt occurs and/or a message is printed on the console device, the operator must refer to table 4-2 for the meaning of the halt.

The execution time of the diagnostic is dependent upon the computer used, the card under test, the test selection and operator response time. Table 2-1 lists the approximate execution time for each test minus the time required by the operator.

Table 3-2. Switch Register Options

BIT	MEANING IF SET
0 1 2 3 4 5 6	Pseudo Operator Design, refer to paragraph 4-14.
7	Reserved.
8	Suppress tests requiring operator intervention.
9	Abort current diagnostic execution and halt (102075); the user may specify a new group of tests in the A-register (see table 3-3) and press RUN. This may also be used after error halt 102034 or 102042, 102054, 102055, 102056, 102057, 102060, 102061.
10	Suppress non-error messages.
11	Suppress error messages.
12	Repeat all selected tests which do not require operator intervention after diagnostic run has completed without halting. Message "PASS XXXXXX" will be output before looping unless bit 10 is set or a console device is not present. Also, the Preset test (in BI-O) will be suppressed. All other selected tests will be executed. However H062 will not be skipped in case of exercising TST 09-11.
13	Repeat last test executed (loop on test). H062 will be skipped in case of exercising TST 09, 10, or 11.
14	Suppress error halts.
15	Halt (102076) at the end of each test; the A-register will contain the test number in octal.

Table 3-3. Test Selection Summary via A-Register

A-REG BIT	IF SET WILL EXECUTE	TEST NO.	TEST IS EXECUTED ON
0	Basic I/O test (flag and interrupt logic).	00	Every I/O board
1	Pattern test.	01	Relay Register.
2*	Command test.	02	Interface board only.
3	Data buffer test.	03	All interfaces except Relay Register and Automatic Dialer.
4	Control signal test.	04	Controller Microcircuit Interface only.
5	Input/output test.	05	Automatic Dialer interface only.
6	Multiline operation test.	06	
7	Dialer turn on, wait, turn off test.	07	
8	Command/Status and Data test without STC.	08	Universal Interface only.
9	Command/Status and Data test with STC.	09	
10	Command Channel test.	10	
11	Data Channel and power on circuit test.	11	
12*	Pseudo Operator Design.	12	

* If the A-Register is cleared the default case will be selected. The control section will then select all applicable tests excluding TST 02 and 12. After turning control over to a discreet test, the first routine inside the test checks the original interface type entered via the S-Register (see table 3-1) and either exits the test if the test is not executed on the specified board or else continues with the test.

3-3. TEST SELECTION

The Control portion of the program provides the operator with a method to select a single test or sequence of tests to be run. The operator sets Switch Register bit 9 to indicate that a selection is desired. If the computer is halted press RUN. The computer will come to a halt 102075 (octal) to indicate ready for selection (see table 3-3). If the diagnostic is running, the test in progress will be completed, then the program will halt. After the halt, the operator may load the A-register with the test selections. Bit 0 of the A-register represents Test 00, bit 1 represents Test 01, and so on through bit 12, which represents Test 12 (decimal). After pressing RUN, the operator-selected test(s) will be executed. If the operator clears all bits of the A-register, all applicable tests defined in table 3-3 will be executed except Test 12, Pseudo Opdesign.

3-4. RESTARTING

The diagnostic may be restarted by setting the P-REG to 2000, loading the S-REG with the desired diagnostic options per table 3-2, then pressing PRESET (EXTERNAL and INTERNAL) and RUN.

The diagnostic may be reconfigured by setting the P-REG to 100, loading the S-REG according to table 3-1, pressing PRESET (INTERNAL and EXTERNAL) and RUN.

DIAGNOSTIC PERFORMANCE

SECTION IV

4-1. TEST DESCRIPTION

Tests 00 through 12 (decimal) are described below. Refer to table 4-2 (comments on halt codes) for additional details on the content of each test.

4-2. BASIC I/O TEST, TST00

Subtest 1 — Checks the ability to clear, set, and test the interrupt system. The following instruction combinations are tested:

```
CLF 0 - SFC 0
CLF 0 - SFS 0
STF 0 - SFC 0
STF 0 - SFS 0
```

Errors in the above sequences produce error messages E000 through E003 as shown in table 4-2.

Subtest 2 — Checks the ability to clear, set and test the interface flag. The following instruction combinations are tested:

```
CLF SC - SFC SC
CLF SC - SFS SC
STF SC - SFC SC
STF SC - SFS SC
```

Errors in the above sequences produce error messages E005 through E010 as shown in table 4-2.

Subtest 3 — Checks that the test select code does not cause an interrupt with the flag and control set on the interface and the interrupt system off. The sequence of instructions is shown below:

```
STF 0
STF SC
STC SC
CLF 0
```

The CLF 0 instruction should inhibit an interrupt from occurring from the interface. Error message E004 occurs if CLF 0 fails.

Subtest 4 — Checks that the flag of the interface under test is not set when all other select code flags are set. Error message E011 occurs if a flag is set incorrectly.

Subtest 5 — Checks the ability of the interface to interrupt. With the flag and control set and the interrupt system on, the interface should interrupt. If the interrupt is missing error message E014 occurs.

Checks that the interrupt occurred where expected. The interrupt should not occur before a string of priority-affecting instructions are executed. The following instructions are used to check the hold-off operation:

```
STC 1
STF 1
CLC 1
CLF 1
JMP *+1,I
DEF *+1
JSB *+1,I
DEF *+1
NOP
```

Error messages E012 and/or E015 will occur if the hold-off failed. If a second interrupt is encountered after the interrupt system has been turned back on error message E013 will occur.

Checks that no instruction was missed during the interrupt (E026 INT EXECUTION ERROR).

Subtest 6 — Checks that with the interrupt system on, and the SC control and flag set, there is no interrupt following a CLC SC instruction. The following sequence of instructions is used:

```
STC SC
STF SC
STF 0
CLC SC
```

If the CLC SC fails to inhibit an interrupt, error message E016 will occur.

Subtest 7 — Checks that the CLC 0 instruction inhibits interrupts when the SC control and flag are set. The following sequence of instructions is used:

```
CLF SC
STC SC
STF SC
STF 0
CLC 0
```

If the CLC 0 fails to inhibit an interrupt, error message E017 will occur.

Subtest 8 — Checks that the PRESET (EXTERNAL and INTERNAL as applicable) switch(es) on the operator panel performs the following actions: (Error messages E020 through E023 can occur.)

Sets the interface flag (EXTERNAL).
Clears interface control (EXTERNAL).
Turns off the interrupt system (INTERNAL).
Clears the I/O data lines (EXTERNAL).
Clears the data register in the interface (INTERNAL).

4-3. PATTERN TEST, TST01

This test is for the HP 12551B Relay Register Interface only. The test outputs a set of four patterns, halting after each pattern to allow the operator to observe the relay closures and openings. If the read-back option card (HP 12551B-01) is being used, the read-back option is checked. Error message E034 will occur if the data read back is incorrect.

NOTE

One method that may be used to check relay outputs would be to apply an ohmmeter across the relay contacts. When an output bit is a "1", the corresponding relay is closed.

If available, the 16-Bit Display Hood can be used for a visual display of the relay outputs (refer to display connector figure B-3 in appendix B of this manual). This connector is not part of the interface kit but can be built by the operator.

The above mentioned methods do not check rise/fall time or bounce of the relay contacts. These parameters will depend upon the relay and the loading of special resistor-capacitor combinations on the card.

4-4. COMMAND TEST, TST02

This test is not part of the standard test run. It has to be explicitly selected by the operator. The test is only for the HP 12551B Relay Register Interface. It checks that the command output signals are functioning correctly. The test requires the special connector shown in appendix B figure B-3. Error messages E030 and E040 can occur, (i.e., flag should set when the response signal is received), and information messages H035 and H037 will occur (if a console is present and Switch Register bit 10 is not set).

4-5. DATA BUFFER TEST, TST03

This test is applicable to all cards except the Relay Register. The test checks the input and output buffers by comparing inputs and outputs for all possible combinations of the data bits. At the end of the test a CRS signal is generated to ensure that the data buffer is cleared. Error message E034 or E042 may occur.

4-6. CONTROL SIGNALS TEST, TST04

This test is for the HP 12849A Controller Microcircuit Interface only and test connector part no. 12849-60004 as shown in appendix B figure B-2 must be connected for the test. A halt has been provided to allow the operator to accomplish this. The test ensures that the buffered control signals CRS, PON, FLG*, and CTL are functioning. The test also checks the ability to set the DIR* flip-flop with an input command, and to clear it with an RDIR* signal. The test checks the ability to set the ORL* flip-flop with an output command, and to clear it with an RORL* signal. For this test, error messages E042 and E044 through E053 can occur. Information message H043 will occur.

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*FLG=Flag, DIR=Data Input Received, RDIR=Reset Data Input Received, ORL=Output Register Loaded, RORL=Reset Output Register Loaded.

4-7. INPUT/OUTPUT TEST, TST05

This test is exclusively for the HP 12589A Automatic Dialer Interface Kit. Test connector 12589-6005 must be connected to exercise the test. It checks the Dial Register and the Call Register FF by outputting a program data word which is read back via the test connector as a device status word. The same input is also verified through the status register flag buffer and flag FF. Error messages E101 through E116 may occur.

4-8. MULTI-LINE OPERATION TEST, TST06

This test is exclusively for the HP 12589A Automatic Dialer Interface Kit. The test connector 12589-6005 must be connected to exercise the test. It verifies the proper operation of the call request register and the line selector relays K1 through K4. The test connector interconnects these relay outputs serially to the DS2 light. The information message "H100 Multi-line operation, use SWR bits 1-4 to operate DS2" is output to the console (if present). The user then can check if each relay operates by turning on bits 1 through 4 of the S-register which should turn on DS2. By turning off any one of the 4 bits DS2 should go off accordingly. The condition of DS1 has no significance. To exit the test, set, then clear bit 7 on the S-register. No error messages occur with this test.

4-9. DIALER TURN ON, WAIT, TURN OFF TEST, TST07

This test is exclusively for the HP 12589A Automatic Dialer Interface Kit. The test connector 12589-6005 must be connected to exercise the test. It checks the Call request, the Digit present buffer and Digit present FF's via the DS1 light on the test connector. The test consists strictly of a visual check of DS1 and has no error messages. During this test DS1 should cycle on and off every 2 seconds until requested to exit by setting, then clearing S-Register bit 7.

4-10. COMMAND/STATUS AND DATA TEST WITHOUT STC, TST08

This test is exclusively for the HP 12930A Universal Interface Board. The appropriate test connector for each of the three boards as shown in table 1-1 is required to run this test. The test checks the command and status register, interference between command/status register and the data register and checks the data register transfer at full speed without STC between data output and input. The oneshot for the CRS-stretched signal is also tested. The switches of the interface board have to be set as specified in table A-7, column "TST0-8".

4-11. COMMAND/STATUS AND DATA TEST WITH STC, TST09

This test requires the same test connector as outlined in paragraph 4-10. It performs the same tests as outlined above except that the data register transfer is accomplished with a STC instruction and CRS-stretched is not tested. The switch setting U106S2 has to be set to the new position "5" as specified in table A-7, column "TST09."

4-12. COMMAND CHANNEL TEST, TST10

This test is exclusively for the HP 12930A Universal Interface Board. This test requires the same test connector as outlined in paragraph 4-10. It checks the Command Channel Control FF and the Command Channel Command FF. The setting of switches U85S2 to position 5 and U85S3 to position 9 as outlined in table A-7, column "TST10" is required.

4-13. DATA CHANNEL AND POWER ON CIRCUIT TEST, TST11

This test is exclusively for the HP 12930A Universal Interface board. It requires the same test connector as outlined in paragraph 4-10. The test will not pass if the old test connectors 12930-60006, -60008 or -60009 are employed (see table 1-1, footnote [2]). The setting of six switches have to be changed as outlined in table A-7, column TST11. The test checks the data channel control FF with the data- and command channel device flag signals connected through the inverting one shots U117A and U116B. The power on circuit through the specially coupled isolators is also tested.

4-14. PSEUDO OPERATOR DESIGN TEST, TST12

Test 12 is not part of the standard sequence of tests for this diagnostic and must be specifically selected to execute. The test is primarily used for troubleshooting. Refer to paragraph 3-3 for test selection instructions. When executed it allows the operator to select a given set of operations.

When first entered, information message H065 is output instructing the operator to select functions on the Switch Register, followed by a Halt 102065. The operator should then:

a. Set the A-register to the desired pattern. This is the pattern that will be output to the interface (except bits eliminated by the B-REG).

b. Set the B-register to the bit mask (1=eliminate bit during any output, input, or compare, 0=retain bit).

c. Set S-REG to the desired options as outlined below.

S-REG BIT	FUNCTION IF SET
0	Increment test pattern by one
1	Output test pattern to interface (OTA SC)
2	Encode test pattern (STC SC,C)
3	Wait for flag (SFS SC) (E042-possible)
4	Input pattern from interface (LIA SC)
5	Compare input with output test pattern (E034-possible)
6	Loop on Opdesign selection
7-15	Refer to table 3-2

d. Press RUN.

If Switch Register bit 6 is not set the program will halt 102065 after executing the selection. Message H065 will not print again. If another pass is desired, make selections and press RUN. To exit the section clear bits 0 through 6 of the Switch Register and press RUN.

4-15. PROCESSOR INTERCONNECT KIT

The following procedure describes a method of testing the HP 12875B Processor Interconnect Kit using this diagnostic. Only one channel can be checked at a time with this method. The assumption is made that the diagnostic has been loaded and the tests for the individual cards in the central processor have been executed. The procedure follows:

a. Ensure that all cables are correctly installed.

b. Load the following into I/O processor memory:

ADDRESS	CONTENT	PROGRAM
2	107700	CLC 0,C
3	1023SC*	SFS SC
4	024003	JMP *−1
5	1025SC*	LIA SC
6	1026SC*	OTA SC
7	1037SC*	STC SC,C
10	024003	JMP *−5

This program will loop the data and flag back to the central processor in a manner similar to that of the test connector.

c. On the I/O processor, set the P-register to 2 (octal) and press PRESET (INTERNAL and EXTERNAL) and RUN.

d. Execute the diagnostic in the central processor as if the test connector is being used.

e. To check the opposite channel perform the above procedures using the opposite channel select code.

This procedure does not accomplish the Basic I/O test on the interfaces in the I/O processor. It does check enough of the hardware so that the diagnostic can be cross loaded. The interfaces in the I/O processor may then be thoroughly tested.

*SC = The select code of the interface in the I/O processor that corresponds to the interface in the central processor that is under test.

4-16. ERROR INFORMATION MESSAGES/HALT CODES

A halt code summary appears in table 4-1. Complete explanations of individual error information messages and halt codes appear in table 4-2.

Table 4-1. Halt Code Summary

HALT	MEANING
TEST 00 (OCTAL) THROUGH 05 (OCTAL)	
102000 thru 102070 and 106000 thru 106017	Error (E) or information (H) messages 00 thru 117 (octal).
CONTROL	
102073	Select code input error.
102074	End of Configuration (select code valid).
102075	User selection request.
102076	End of Test (A-register contains test number).
102077	End of diagnostic run.
106077	Trap cell halt in locations 2 thru 77 (octal).
Note: For any other halts refer to the *Diagnostic Configurator Reference Manual.*	

Table 4-2. Error and Information Messages and Halt Codes

HALT** CODE	PROGRAM SECTION	MESSAGE	COMMENTS
None	Test Control	GENERAL PURPOSE REGISTER DIAGNOSTIC, DSN XXXXXX	Introductory message with current DSN.
None	Test Control	TEST XX	Information message before error message (XX equals test number). Message occurs only once within a test and is suppressed for any subsequent messages within the same test.
102000	Test 0	E000 CLF 0-SFC 0 ERROR	CLF/SFC 0 combination failed. CLF did not clear flag or SFC caused no skip with flag clear.
102001	Test 0	E001 CLF 0-SFS 0 ERROR	CLF/SFS 0 combination failed. CLF did not clear flag or SFS caused skip with flag clear.
102002	Test 0	E002 STF 0-SFC 0 ERROR	STF/SFC 0 combination failed. STF did not set flag or SFC caused skip with flag set.
102003	Test 0	E003 STF 0-SFS 0 ERROR	STF/SFS 0 combination failed. STF did not set flag or SFS caused no skip with flag set.
102004	Test 0	E004 CLF 0 DID NOT INHIBIT INT	With card flag and control set, CLF 0 did not turn off interrupt system.
102005	Test 0	E005 CLF SC-SFC SC ERROR	CLF/SFC SC combination failed. CLF did not clear flag or SFC caused no skip with flag clear. If this halt occurs while testing a 12930 UI board after the message "H025 basic I/O completed on data channel" verify that the jumper U97S1 is in position 1.
102006	Test 0	E006 CLF SC-SFS SC ERROR	CLF/SFS SC combination failed. CLF did not clear flag or SFS caused skip with flag clear.
102007	Test 0	E007 STF SC-SFC SC ERROR	STF/SFC SC combination failed. STF did not set flag or SFC caused skip with flag set.
102010	Test 0	E010 STF SC-SFS SC ERROR	STF/SFS SC combination failed. STF did not set flag or SFS caused no skip with flag set.
102011	Test 0	E011 STF XX SET CARD FLAG	Select code screen test failed. A-register contains XX (octal) where XX equals select code that caused card flag to set.
102012	Test 0	E012 INT DURING HOLD OFF INSTR	Interrupt occurred during an I/O instruction or a JMP/JSB indirect instruction.
102013	Test 0	E013 SECOND INT OCCURRED	Card interrupted a second time after initial interrupt was processed.

**Error halt codes are in octal, test numbers are in decimal.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT** CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102014	Test 0	E014 NO INT	No interrupt occurred with card flag and control set and the interrupt system on.
102015	Test 0	E015 INT RTN ADDR ERROR	Interrupt did not occur at the correct location in memory.
102016	Test 0	E016 CLC SC ERROR	CLC SC did not clear card control with the interrupt system on.
102017	Test 0	E017 CLC 0 ERROR	CLC 0 did not clear card control with the interrupt system on.
102020	Test 0	E020 PRESET (EXT) DID NOT SET FLAG	PRESET (EXT) did not set the card flag.
102021	Test 0	E021 PRESET (INT) DID NOT DISABLE INTS	PRESET (INT) did not disable the interrupt system.
102022	Test 0	E022 PRESET (EXT) DID NOT CLEAR CONTROL	PRESET (EXT) did not clear control.
102023	Test 0	E023 PRESET (EXT) DID NOT CLEAR I/O LINES	PRESET (EXT) did not clear I/O data lines.
102024	Test 0	H024 PRESS PRESET (EXT & INT), RUN	Press PRESET (EXTERNAL/ INTERNAL then RUN.
None	Test 0	H025 BASIC I/O COMPLETE (ON DATA/ CONTROL CHANNEL)	Basic I/O tests completed. (In case of a 12930 UI board this message should occur twice, once for the data, once for the control channel.)
102026	Test 0	E026 INT EXECUTION ERROR	Interrupt was not processed correctly.
102030	Test 1	H030 OBSERVE ALL ZEROS	Operator should check that all relay outputs are open. A-register equals the test pattern.
102031	Test 1	H031 OBSERVE ALL ONES	Operator should check that all relay outputs are closed. A-register equals test pattern.
102032	Test 1	H032 OBSERVE PATTERN 125252	Operator should check that relay outputs are properly set. A-register equals test pattern.
102033	Test 1	H033 OBSERVE PATTERN 052525	Operator should check that the relay outputs are properly set. A-register equals test pattern.
102034	Tests 1,3,5	E034 DATA NON-COMPARE EXPECTED XXXXXX ACTUAL XXXXXX	Read-back indicates failure of card between input to buffer register and feed-back to computer. A-register equals expected read-back, B-register equals actual.

**Error halt codes are in octal, test numbers are in decimal.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT** CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102035	Test 2	H035 OBSERVE COMMAND OUTPUT FOLLOWED BY APPLYING EXTERNAL RESPONSE SIGNAL. PUSH RUN.	Check that Command flip-flop was set (pin W at logical level 0 and pins U and 17 are connected). Apply response signal to card. (12 VDC to pins V and 18.) Remove response signal. Push RUN.
102036	Test 2	E036 APPLICATION OF RESPONSE SIGNAL CAUSED FLAG TO SET.	Flag was set by application of external response signal to card.
102037	Test 2	H037 OBSERVE COMMAND OUTPUT FOLLOWED BY APPLYING EXTERNAL RESPONSE SIGNAL. PUSH RUN.	Check that Command flip-flop was cleared (pin W at logic level 1 and pins U and 17 are not connected). Apply response signal to card (12 VDC to pins V and 18). Remove response signal. Press RUN.
102040	Test 2	E040 APPLICATION OF RESPONSE SIGNAL DID NOT SET FLAG.	Flag was not set by application of response signal.
102041	Test 3	H041 USE TEST CONN. 12849-60003.	Use test connector A for data test. This message output only for HP 12849A.
102042	Tests 3,4 & 12	E042 FLAG DID NOT SET.	Test Device Command and ability of Device Flag Command to set flag. (Check if proper test connector is installed.)
102043	Test 4	H043 USE TEST CONN. 12849-60004.	Use test connector B for Control Signals test.
102044	Test 4	E044 NO CRS OR RDIR DOES NOT CLEAR DIR-FF.	Test CRS and ability to clear DIR-FF with RDIR.
102045	Test 4	E045 DIR FALSE AFTER IOI	Test DIR and ability of IOI to set DIR-FF.
102046	Test 4	E046 ORL TRUE AFTER RORL	Test ORL and ability to clear ORL-FF with RORL.
102047	Test 4	E047 ORL FALSE AFTER IOO	Test ORL and ability of IOO to set ORL-FF.
102050	Test 4	E050 PON FALSE	PON should be true when computer is on.
102051	Test 4	E051 FLG TRUE AFTER CLF	Test buffered flag output (FLG pin U of the 48-pin connector).
102052	Test 4	E052 FLG FALSE AFTER STF	Test buffered flag output (FLG pin U of the 48-pin connector).
102053	Test 4	E053 CTL FALSE AFTER STC	Test buffered control output (CTL pin X of the 48-pin connector).
102054	Test 8/9	E054 INCORRECT STATUS WORD EXPECTED XXXXXX ACTUAL YYYYYY	If this error occurs in test 08 and the expected word is 000200 check first that the next higher SC is occupied by a jumper board. A control word was output and the read-back status word did not compare with the expected (see Note 1).

**Error halt codes are in octal, test numbers are in decimal.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT** CODE	PROGRAM SECT ON	MESSAGE	COMMENTS
102055	Test 8/9	E055 DATA WORD MODIFIED BY COMMAND/ STATUS EXPECTED XXXXXX ACTUAL YYYYYY	The outputted data word was modified by the command word output or the status word input. If this error occurs in TST 08 with expected = actual = 000000 check jumper setting U106S2 (see note 1).
102056	Test 8	E056 CRS STRETCHED IS < 5 μs	The one-shot U75B stayed in the set position for less than 5 μs. (Only a rough time comparison is employed.)
102057	Test 8	E057 CRS STRETCHED is >5 μs	The one-shot U75B stayed in the set position for more than 5 μs. (Only a rough time comparison is employed.)
102060	Test 8/9	E060 FULL SPEED DATA TRANSFER FAILURE EXPECTED XXXXXX ACTUAL YYYYYY	The outputted data word at maximum transfer speed was modified. (See note 1.)
102061	Test 8/9	E061 COMMAND OR STATUS MODIFIED BY DATA WORD EXPECTED XXXXXX ACTUAL YYYYYYY	The outputted command word or the read-back status word was modified by a long transfer of data words. (See note 1.)
102062	Test 9/10/11	H062 TURN CPU POWER OFF (STANDBY), CHANGE SWITCHES ON UI BOARD PER APPENDIX A, AND TURN POWER ON.	This information message is preceeded by a line "TEST nn". Turn the CPU power off, go to Appendix A, table A-7 and set all 15 switches as specified in the column headed by the test number preceeding the message H062. Then turn power back on. The CPU will go automatically into the run mode and exercise the test. When looping on one test the message and the halt will not be reached.
102063	Test 10/11	H063 DATA WORD WAS MODIFIED EXPECTED XXXXXX ACTUAL YYYYYY.	A data word transferred to and read back from the interface board was modified (see note 1).
102064	Test 10/11	H064 INCORRECT STATUS WORD EXPECTED XXXXXX ACTUAL YYYYYY.	The status word read in was not as expected (see note 1).
102065	Test 10/11	H065 DATA CH FLAG FF NOT SET	Data channel flag FF was not set after data transfer.
102066	Test 10/11	H066 COMMAND CH FLAG FF NOT SET	Command channel flag FF was not set after control word was transmitted
102070	Test 12	H070 SET SWITCH REG FOR PSEUDO OP DESIGN	Make Switch Register selection as described in paragraph 4-14.

**Error halt codes are in octal, test numbers are in decimal.

Note 1: When reading the error halts 102054, 55, 60, 61, 63 or 64 the A-reg. displays the expected, the B-reg. the actual value.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT** CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102073	Config-uration	None	I/O select code entered at config-uration is invalid. Must be greater than 7 (octal). Reenter a valid select code and press RUN.
102074	Config-uration	None	Select code entered during config-uration is valid. Enter Switch Regis-ter options (see table 3-2) and press RUN.
102075	Test Control	None	Test selection request resulting from Switch Register bit 9 being set. Enter the desired tests to be exe-cuted in the A-REG, then press RUN.
102076	Test Control	None	End-of-test halt resulting from Switch Register bit 15 being set (A-register equals test number). To continue, press RUN.
102077	Test Control	PASS XXXXXX	Diagnostic run complete. (A-register value equals pass count.) Switch Register options may be changed. To continue, press RUN.
106000	Test 6	H100 MULTI LINE OPERATION USE SWR BITS 1-4 TO OPERATE DS2.	Set S-reg bit 1 through 4. DS2 should turn on. By clearing any one of the 4 bits DS2 should go off. To exit, set, then clear bit 7. (See para-graph 4-8.)
106001	Test 5	E101 IOBO=100017, FLAG@ 1, IOBI=XXXXXX	Flag should be cleared but was found set.*
106002	Test 5	E102 IOBO=100017, FLAG= 1, IOBI@XXXXXX	IOBI should be 000000.*
106003	Test 5	E103 IOBO=100000, FLAG@ 1, IOBI=XXXXXX	Flag should be cleared but was found set.*
106004	Test 5	E104 IOBO=100000, FLAG= 1, IOBI@XXXXXX	IOBI should be 000000.*
106005	Test 5	E105 IOBO=040017, FLAG@ 1, IOBI=XXXXXX	Flag should be cleared but was found set.*
106006	Test 5	E106 IOBO=040017, FLAG= 1, IOBI@XXXXXX	IOBI should be 000000.*
106007	Test 5	E107 IOBO=040016, FLAG@ 0, IOBI=XXXXXX	Flag should be set but was found cleared.*
106010	Test 5	E110 IOBO=040016, FLAG= 0, IOBI@XXXXXX	IOBI should be 100000.*
106011	Test 5	E111 IOBO=040015, FLAG@ 0, IOBI=XXXXXX	Flag should be set but was found cleared.*
106012	Test 5	E112 IOBO=040015, FLAG= 0, IOBI@XXXXXX	IOBI should be 040000.*

**Error halt codes are in octal, test numbers are in decimal.

* In error halts 106001 through 106016 the pattern outputted to the I/O bus is shown as "IOBO=YYYYYY". Either the flag FF (FLAG) or the input bus (IOBI) was tested and the value tested was not as expected. The value with the "@" symbol indicates the signal which was tested and failed. The one with the "=" symbol is for references only. The A-reg will equal the IOBI-bus.

Table 4-2. Error and Information Messages and Halt Codes (Continued)

HALT** CODE	PROGRAM SECTION	MESSAGE	COMMENTS
106013	Test 5	E113 IOBO=040013, FLAG@ 1, IOBI=XXXXXX	Flag should be clear but was found set.*
106014	Test 5	E114 IOBO=040013, FLAG= 1, IOBI@XXXXXX	IOBI should be 020000.*
106015	Test 5	E115 IOBO=040007, FLAG@ 0, IOBI=XXXXXX	Flag should be set but was found cleared.*
106016	Test 5	E116 IOBO=040007, FLAG= 0, IOBI@XXXXXX	IOBI should be 010000.*
106017	Test 7	H117 OBSERVE DS2.	DS2 should turn on and off at the rate of approximately 2 sec. To exit, set, then clear bit 7 (see paragraph 4-9).
106077	Test Control	None	Halt stored in locations 2 through 77 (octal) to trap interrupts which may occur unexpectedly because of hardware malfunctions. M-register contains the I/O slot number of interrupt. Diagnostic may be partially destroyed if halt occurs. The program may have to be reloaded; the problem should be corrected before proceeding.

**Error halt codes are in octal, test numbers are in decimal.

* In error halts 106001 through 106016 the pattern outputted to the I/O bus is shown as "IOBO=YYYYYY". Either the flag FF (FLAG) or the input bus (IOBI) was tested and the value tested was not as expected. The value with the "@" symbol indicates the signal which was tested and failed. The one with the "=" symbol is for references only. The A-reg will equal the IOBI-bus.

REQUIRED JUMPER INSTALLATIONS

APPENDIX A

Each of the interface cards that can be tested by the General Purpose Register Diagnostic program must have, during execution of the diagnostic, a certain combination of circuit jumper positions installed. (The HP 12930A Universal Interface Kit requires a different jumper setting for the execution of test 9, 10, and 11.) The combinations allowed are listed below in tables A-1 through A-7, according to the type of interface card to be tested.

A-1. HP 12554A 16-BIT DUPLEX REGISTER (POSITIVE LOGIC)

Any one of the following combinations is allowed:

Table A-1.

		Positions under Combination Number				
		1	2	3	4	5
Jumper Number	W4	B	B	A/B	A	A
	W5	B	A	A/B	A	B
	W6	A/B	A	C	A/B	A
	W7	A	A	A/B	B	B

NOTE

Jumpers not listed may be installed in any position described in the Operating and Service Manual for this card.

A-2. HP 12554A-001 16-BIT DUPLEX REGISTER (NEGATIVE LOGIC)

Any one of the following combinations is allowed:

Table A-2.

		Positions under Combination Number				
		1	2	3	4	5
Jumper Number	W4	A/B	A	A/B	A/B	B
	W5	A	A	A/B	B	A
	W6	B	A	C	B	A
	W7	B	B	A/B	A	A

NOTE

Jumpers not listed may be installed in any position described in the Operating and Service Manual for this card.

A-3. HP 12566B/C, HP 12566B/C-001, HP 12566B/C-002, HP 12566B/C-003 MICROCIRCUIT INTERFACE

Any one of the following combinations is allowed:

Table A-3.

	12566B	12566C
W1	C	C
W2	B	B
W3	B	B
W4	B	B
W5	IN	OUT
W6	IN	OUT
W7	IN	OUT
W8	IN	OUT
W9	A	A
W10	NA	B
W11	NA	IN
W12	NA	OUT
W13	NA	OUT

NOTE

Jumpers not listed may be installed in any position described in the Operating and Service Manual for this card.

A-4. HP 12597A 8-BIT DUPLEX REGISTER (POSITIVE OR NEGATIVE LOGIC)

Any one of the two following combinations is allowed:

Table A-4.

	1	2
W1	A	B
W2	A/B	A/B
W3	Connected	Removed
W4	Connected	Connected
W8	Removed	Connected
W9	Removed	Removed

NOTE

All other jumpers must remain in the factory installed position (they set the polarity of the interface).

A-5. HP 12602B OPTICAL MARK CARD READER INTERFACE

Only one combination is allowed:

Table A-5.

W1	Connected	W8	Connected
W2	Connected	W9	Connected, then removed*
W3	Connected	W10	Connected
W4	B	W11	Connected
W5	B	W12	Connected
W6	B	W13	A
W7	A	W14	B

*Jumper W9 on the HP 12602B card is connected ONLY during execution of the diagnostic. When the card is returned to normal use, W9 MUST be removed.

A-6. HP 12849A, 12849A-001 CONTROLLER MICRO-CIRCUIT INTERFACE

Any one of the following combinations is allowed:

Table A-6.

		Positions under Combination Number			
		1	2	3	4
Jumper Number	W1	B	A	A	B
	W2	A	B	C	C
	W3	A	B	B	A
	W4	B	B	A/B	A/B
	W5	If W4 is in position A, W5 through W8 must be present (installed). If W4 is in position B, any one or more of W5 through W8 may be absent.			
	W6				
	W7				
	W8				
	W9	A/B (for all combinations).			
	W10				

A-7. HP 12875B PROCESSOR INTERFACE KIT

Any one of the following combinations is allowed:

Table A-7.

		Positions under Combination Number					
		1	2	3	4	5	6
Jumper Number	W1	B	A	A	A	B	B
	W2	A	B	C	C	C	C
	W3	A	B	B	A	A	B
	W4	B	B	A/B	B	A/B	B

A-7. HP 12930A UNIVERSAL INTERFACE KIT

The universal interface board requires a different jumper switch setting for each of the special UI tests (TST 08-11). At the beginning of TST 09, 10 and 11 the CPU will halt and inform the operator to change the jumpers as specified in the columns headed by the appropriate test number. The switch settings circled indicate any changes from the switch setting of the previous test.

Table A-7.

SWITCH	SWITCH POSITION DURING TEST NR			
	TEST 00-08	TEST 09	TEST 10	TEST 11
U 8 5 S 1	1	1	1	1
S 2	6	6	(5)	5
S 3	10	10	(9)	(8)
U 8 7 S 1	1	1	1	1
S 2	5	5	5	5
S 3	8	8	8	8
U 9 7 S 1	1	1	1	1
S 2	5	5	5	(4)
S 3	10	10	10	(9)
U 1 0 2 S 1	2	2	2	2
S 2	7	7	7	(6)
S 3	10	10	10	10
U 1 0 6 S 1	1	1	1	(2)
S 2	6	(5)	5	5
S 3	9	9	9	(10)

TEST CONNECTIONS

APPENDIX B

Figure B-1 shows the modification required to the test connector part no. 1251-0332 to test the 12566B/C or 12653A microcircuit interface board which is equal to the unmodified test connector part no. 12849-60003 supplied with the 12849A controller microcircuit interface board. In case of the 12849A board this test connector is used during the data buffer test TST 03.

PINS		SIGNAL
FROM	TO	
A	1	Bit 0 to Bit 0
B	2	Bit 1 to Bit 1
C	3	Bit 2 to Bit 2
D	4	Bit 3 to Bit 3
E	5	Bit 4 to Bit 4
F	6	Bit 5 to Bit 5
H	7	Bit 6 to Bit 6
J	8	Bit 7 to Bit 7
K	9	Bit 8 to Bit 8
L	10	Bit 9 to Bit 9
M	11	Bit 10 to Bit 10
N	12	Bit 11 to Bit 11
P	13	Bit 12 to Bit 12
R	14	Bit 13 to Bit 13
S	15	Bit 14 to Bit 14
T	16	Bit 15 to Bit 15
Z	23	Device Command to Device Flag
BB,24		N/C (GROUND)

Figure B-1. Modified Test Connector No. 1251-0332 Equal 12849-60003

Figure B-2 shows the special test connector (part no. 12849-60004) connections which must be used for the control signals test TST 04 for the HP 12849A Controller Microcircuit Interface):

PINS		SIGNAL
FROM	TO	
17	1	ORL to Input Bit 1
18	2	DIR to Input Bit 1
U	3	FLG to Input Bit 2
W	4	PON to Input Bit 3
X	5	CTL to Input Bit 4
V	A	RORL to Output Bit 0
Y	20	CRS to RDIR
Z	23	Device Command to Device Flag
BB,24		N/C (GROUND)

Figure B-2. Test Connector 12849-60004

The special test and display connector for the HP 12551B and HP 12551B-01 Relay Register Board can be used to display the contact closures of the read relays in Test 01 and is required for Test 02. Figure B-3 shows the electrical layout of the test and display connector.

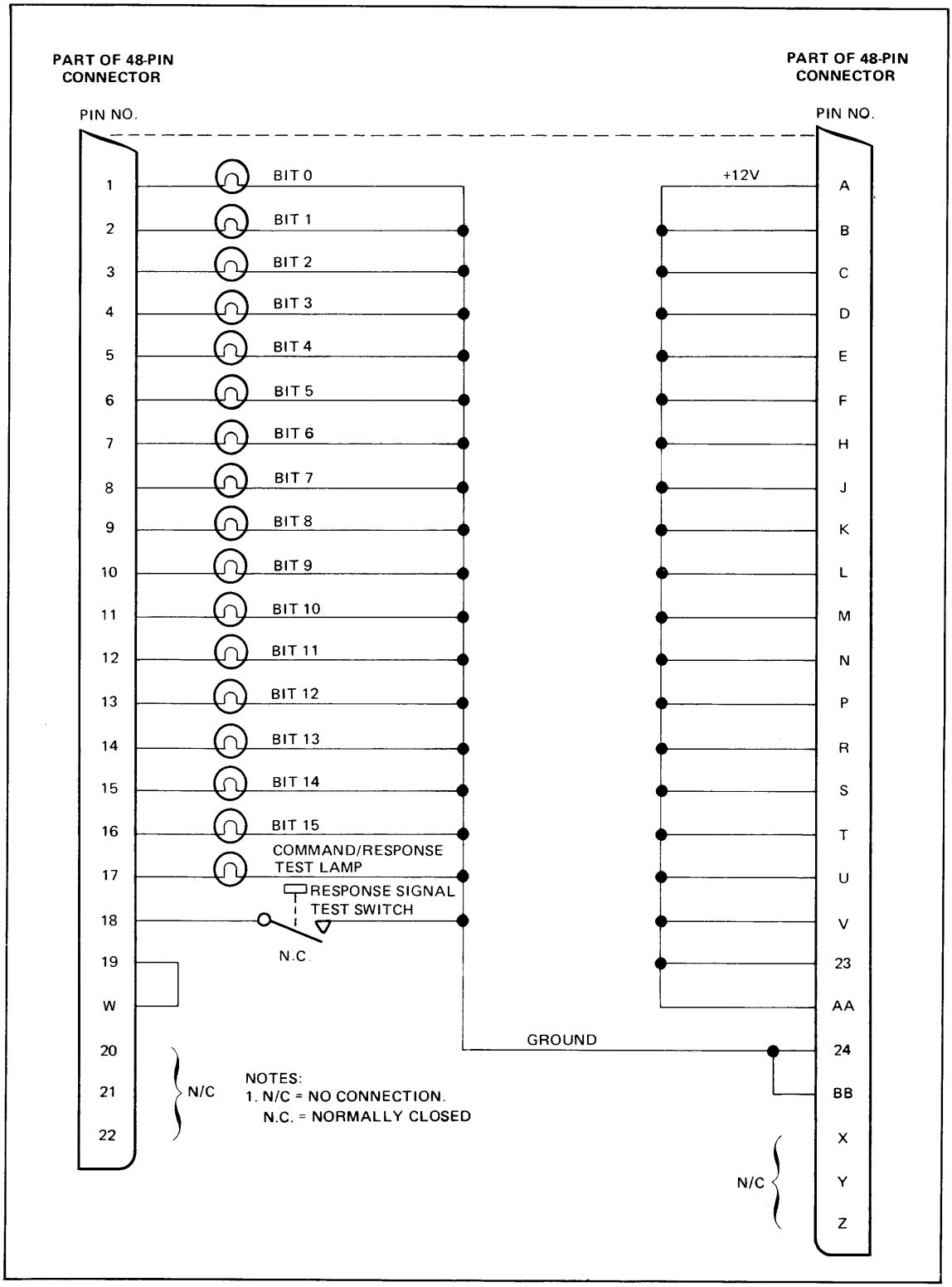

Figure B-3. Test and Display Connector Layout for 12551B Boards

Figure B-4 shows the pin connections to convert a 12930-60006 to a 12930-60013 test connector required to exercise test 11 on the HP 12930 UI board.

FROM PIN	TO PIN	FROM PIN	TO PIN
A1	A26	B1	B26
A2	A27	B2	B27
A3	A28	B3	B28
A4	A29	B4	B29
A5	A30	B5	B30
A6	A31	B6	B31
A7	A32	B7	B32
A8	A33	B8	B33
A9	A34	B9	B34
A10	A35	B10	B35
A11	A36	B11	B36
A12	A37	B12	B37
A13	A38	B13	B38
A14	A39	B14	B39
A15	A40	B15	B40
A16	A41	B16	B41
A17	A42 & B25	B17	B42 & A25
A18	A43	B18	B43
A19	A44	B19	B44
A20	A45	B20	B45
A21	A46	B21	B46
A22	A47	B22	B47
A23	A48	B23	B48
A24	A49	B24	B49

Figure B-4. Diagnostic Test Connector (12930-60013) Wire List

Figure B-5 shows the pin connections to convert a 12930-60008 to a 12930-60014 test connector required to exercise test 11 on the HP 12930A-001 and -003 UI board (ground true).

Figure B-6 shows the pin connections to convert a 12930-60009 to a 12930-60015 test connector required to exercise test 11 on the HP 12930A-002 UI board (positive true).

FROM PIN	TO PIN	FROM PIN	TO PIN
B1	B26	B14	B39
B2	B27	B15	B40
B3	B28	B16	B41
B4	B29	B17	B42 & A25
B5	B30	B18	B43
B3	B31	B19	B44
B7	B32	B20	B45
B8	B33	B21	B46
B9	B34	B22	B47
B10	B35	B23	B48
B11	B36	B24	B49
B12	B37	B25	A17
B13	B38		

Figure B-5. Diagnostic Test Connector (12930-60014) Wire List

FROM PIN	TO PIN	FROM PIN	TO PIN
A1	A26	A14	A39
A2	A27	A15	A40
A3	A28	A16	A41
A4	A29	A17	A42 & B25
A5	A30	A18	A43
A6	A31	A19	A44
A7	A32	A20	A45
A8	A33	A21	A46
A9	A34	A22	A47
A10	A35	A23	A48
A11	A36	A24	A49
A12	A37	A25	B17
A13	A38		

Figure B-6. Diagnostic Test Connector (12930-60015) Wire List

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