HEWLETT-PACKARD

PURCHASE SPECIFICATION

for

HP 2116B COMPUTER

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HP 2116B COMPUTER PURCHASE SPECIFICATION

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PURCHASE SPECIFICATION -- HP 2116B DIGITAL COMPUTER

1.0 SCOPE OF REQUIREMENTS

This specification establishes minimum requirements for a general purpose digital computer, for computer manuals, and for software packages ranging from Compilers to computer self-test programs.

The required computer should have a mainframe memory capacity of 8192 (or 16,384) 16-bit words, and a memory cycle time of 1.6 microseconds or less.

Memory should be field expandable up to 32,768 16-bit words, and Input/Output should be field expandable up to 48 multilevel priority interrupting Input/Output Channels.

Hardware/software interface should be available for Teletype, photoreader, paper tape punch, seven and nine channel magnetic tape transports, disc memory, line printer, integrating digital voltmeters, scanners, scanning (sample and hold) ADC's, counters, and frequency synthesizers. Peripherals should be field installable by means of plug-in interface cards and software modules which fit into the FORTRAN Input/Output structure.

Processor options should include Hardware Arithmetic and Direct Memory Access for high speed word and byte transfer. The Extended Arithmetic Package should perform hardware multiply and divide on positive and negative integers; Direct Memory Access should be software assignable to any two Input/Output Channels, and should allow simultaneous use of each channel at 300 kHz word rate.

2.0 HARDWARE REQUIREMENTS

The computer shall be constructed of replaceable plug-in circuit cards incorporating monolithic integrated circuits where applicable; identical circuit cards shall be used whenever possible.

Physical layout shall allow front accessibility to all circuit cards; accessibility shall not be impaired by mounting the computer in a standard 19" equipment enclosure.

2.1 Central Processor

The central processor must perform parallel operations on 16-bit computer words, making use of 16-bit instructions and two 16-bit arithmetic registers.

2.1.1 Instruction Set

A powerful yet conventional instruction set should be oriented towards the development of software systems and input-output flexibility.

Memory reference and jump instructions should allow unlimited multilevel indirect addressing and suppress interrupt during indirect jumps where interrupt could cause loss of the program counter.

2.1.1.1 Single Cycle Instructions

Within a single cycle machine instruction, it shall be possible to:

one's complement, two's complement, or increment either arithmetic register by one

set either arithmetic register to plus one, minus one, or zero

skip if a given arithmetic register is positive, negative, zero, non-zero, even, or odd

read or write either arithmetic register onto any I/O channel, or read the switch register image into either arithmetic register

enable or disable the interrupt system

exchange the high and low order 8-bits of either arithmetic register

jump to any location on base page (1024 words) or current page

load either arithmetic register with the address of the last channel to cause an interrupt

2.1.1.2 Indirect Jumps

Unlimited multilevel indirect addressing should be provided, and interrupt should be inhibited during indirect jumps.

Jump to any location in memory from any location in memory should require a maximum of two machine cycles, and a maximum of one level of indirect addressing.

A "Jump to Subroutine" instruction must:

allow transfer of 32 bits of data in working registers to facilitate floating point operations

allow indirect transfer to any location in memory from any location in memory within three machine cycles

establish return linkage by depositing the return address in the destination address, and initiate subroutine execution at the destination address plus one.

2.1.1.3 Memory Reference Instructions

Within three machine cycles, it shall be possible to ADD or COMPARE the contents of any memory location to either arithmetic register, or to LOAD the contents of any memory locations into either arithmetic register, or to STORE the contents of either arithmetic register in any memory location.

Within three machine cycles, it shall be possible to find the logical "and", "inclusive or", or "exclusive or" of one arithmetic register and a memory location or the other arithmetic register.

All the above instructions shall require only two machine cycles if the reference memory location is on the same page as the instruction, or on base page.

2.1.1.4 Register Display and Front Panel Controls

The front panel of the computer shall provide simultaneous display of all working registers and provide facilities for:

entering 16-bit numbers into memory,

displaying locations in memory,

displaying machine cycle status,

displaying overflow status,

displaying and altering arithmetic registers and the program counter,

use of single cycle steps.

The front panel shall have 16-latching switches which may be used to load 16-bit binary numbers into the working registers, the program counter, and memory locations. A single cycle instruction should read the switch pattern into either arithmetic register.

2.1.2 Central Processor Plug-In Options

Maximum utility can be made of the computer system if plug-in options allow expansion of system capabilities as need and budget warrant. The following plug-in options shall be available for field expansion of central processor capabilities:

2.1.2.1 Extended Arithmetic Unit

The extended arithmetic unit shall provide in a single hardware instruction:

Hardware Integer Multiply/Divide

Hardware Integer Multiply/Divide instructions should provide two's complement multiplication and division of positive and negative integers within 20 microseconds.

Hardware multiplication should yield a 32-bit signed product; hardware division should divide a 32-bit signed dividend by a signed 16-bit divisor and product a signed 16-bit quotient and a signed 16-bit remainder. Hardware divide shall provide overflow indication if the quotient exceeds 16-bits.

High Speed Double Load and Store

To facilitate floating point operations, the hardware arithmetic unit should permit loading and storing of 32-bit floating point numbers to and from the working registers indirectly to any location in memory within 10 microseconds, without changing the contents of the indirect address memory location.

Bi-Directional Dual Register Long Shifts and Rotates

For long shifts and rotates, the two 16-bit arithmetic registers shall be considered as one 32-bit register. Arithmetic shifts, logical shifts, and rotates in either direction shall be performed within 10 microseconds.

2.1.2.2 Direct Memory Access

Direct Memory Access should allow high speed data I/O, and should be assignable to any two Input/Output devices under program control. Word or byte transfer rate should be at least 300 kHz per channel, with no reduction in data rate if both channels are operating simultaneously.

To provide high speed buffer transfer to and from 9-channel magnetic tape and similar 8-level devices, DMA should pack or unpack 8-bit bytes during transfer if specified.

Upon termination of transmission, on either channel, DMA should optionally interrupt the computer.

2.1.2.3 Direct Memory Increment

To accept data from high speed Nuclear ADC's, or other devices where "slot counts" are generated, provision should be available for external increment of individual memory addresses at a 500 kHz rate.

Under program control, the limits of the externally accessible memory block should be set. The central processor should accept logic level address codes, and increment the selected memory location by one.

The computer should be interrupted if a memory location overflows or if an address appears which is outside the allowed block.

Only one channel of DMA may be used when DMI is installed in the computer.

2.2 Computer Memory

Memory should be a wide-temperature range, magnetic-core stack with a 1.6 microsecond read/write cycle time.

2.2.1 Memory Size

Minimum memory size required is 8192 (or 16,384) 16-bit words. Plug-in or cable-on modules shall allow straight-forward field expansion up to 32,768 words.

2.2.2 Loader/Loader Protection

Provision for protection of a bootstrap loader resident in core must be provided, preferably with a front panel switch.

2.2.3 Memory Protection Against Power Failure

Whenever the primary power to the computer drops below levels which the computer may operate at, the computer should be interrupted with adequate time to execute up to 100 machine instructions for shutdown purposes. It is assumed that within these 100 instructions, the working registers will be stored in memory and a HALT will be executed. Thus, when power does go down, no memory locations will be lost, and the working registers will be saved in memory.

2.2.4 Power Failure Memory Protection with Automatic Restart

A technique for saving memory and the working registers in the event of a power failure, and automatic restart upon restoration of power, should be available as a plug-in option.

Power failure should cause transfer of control to a specified memory location so that shutdown software can be implemented. Power supply capacitors should be sufficient to maintain power for execution of at least 200 instructions before shutdown.

Restart upon restoration of power should transfer control to a specified memory location so that software routines for getting back on the air can be implemented.

2.2.5 Memory Parity Check

Memory parity check should be available as a plug-in option. The parity check option should provide parity error and parity bit lamp indications for diagnostic purposes, and should optionally produce either a halt or an interrupt when an error is detected.

2.2.6 Memory Protect

A technique for converting a segment of computer memory into protected memory should be available as a plug-in option. The length of protected memory should be set with a machine instruction, and should be variable from one word to almost all of memory, in single word increments.

Any attempt to violate protected memory should be flagged with a computer interrupt, and memory protect should make available the address of the instruction which attempted to violate protected memory.

Memory protect should be designed for systems programming, and as such, it should inhibit HALT instructions and all Input/Output instructions. Thus, if memory protect were slaved to a system executive, all sub-programs would be forced to do Input/Output with the cognizance of the system executive, and no sub-program could halt the computer or violate the protected executive system.

2.3 Input/Output System

Central Processor Input/Output capability shall include sixteen channels of multilevel priority interrupt, such that any higher priority channel can interrupt the processing of any lower priority channel.

Each Input/Output channel shall accept vendor-supplied plug-in interface circuit cards which provide electrical interface to peripherals. Interface circuit cards shall be accessible from the front of the unit, and accessibility shall not be hampered by mounting in a standard 19" equipment enclosure.

2.3.1 Interrupt Linkage

Within three machine cycles after an interrupt, transfer shall have been made to an interrupt processing subroutine, and the return linkage stored in memory. The location of interrupt processing subroutines shall not be restricted to base page.

2.3.2 Expandability

Expandability shall be to 48 Input/Output channels, with a corresponding 48-levels of priority interrupt. Expansion to 48 Input/Output channels shall not hamper front accessiblity of plug-in interface circuit cards.

2.4 Physical and Electrical Requirements

The computer shall operate and meet specifications in a hostile environment, and shall be tolerant of humidity, temperature, and power fluctuations as specified below.

2.4.1 Primary Power

The computer shall turn on and meet specifications for line voltages between 103.5 and 126.5 volts, and between 207 and 253 volts, for line frequencies between 47.5 and 70 Hz.

(400-Hz operation is available on special order.)

2.4.2 Weight and Size

The mainframe central processor, including up to 16,384 words of 16-bit memory, shall weigh no more than 250 pounds, and shall mount in a standard 19" equipment enclosure.

2.4.3 Environmental Tolerance

The computer must be mechanically and electrically rugged, durable, and free of loose or fragile parts which may cause failure under severe service conditions.

2.4.3.1 Temperature, Operating and Non-Operating

The computer shall withstand a NON-OPERATING temperature of -40°C to +75°C, and an OPERATING temperature of 0°C to 55°C ambient. The computer must turn on and become operational at low line voltage (see 2.4.1) and at 0°C.

2.4.3.2 Humidity

The computer must remain operational and meet specifications anywhere within the temperature range of 25°C to 40°C in a relative humidity of 50% to 95%.

2.4.3.3 Mechanical Ruggedness

The computer shall be able to withstand a shock equivalent to righting itself from a tilt where any edge is raised 4" from the surface plane.

2.4.3.4 RFI Susceptability

The computer must remain operational and meet specifications when tested per MIL-I-6181D:

1) RF radiated (to 10 GHz) 0.1 volt open circuit on 41" rod, tuned dipole, or non-directive antenna; 400 to 1000 Hz, modulated 30%.
2) RF conducted - 0.15 MHz to 10 GHz at 0.1 volt level into 50 ohm sources. The RF signal shall be 400 or 1000 Hz, modulated 30%.
3) AF conducted - 3V rms from 30 Hz to 150 KHz through line isolation transformer.

2.5 Internal Power Supplies

The computer shall contain an integral power supply which is electronically protected against short circuit or overload. Upon short circuit or overload, the power supply shall turn itself off and remain so until the computer is turned on again.

A standard SCR Crowbar circuit shall be used to protect the central processor and memory circuits against power supply overvoltages. The "crowbar" shall clamp

the power supply to ground immediately upon detection of over voltages, such that logic circuits can not be damaged upon failure of power supply regulation.

3.0 SOFTWARE REQUIREMENTS

A fully documented and comprehensive software package is a necessary part of the required computer system. Software provided shall include a FORTRAN Compiler (and an ALGOL Compiler), and sufficient backup software to implement the computational and logging capabilities of FORTRAN/ALGOL.

Vendor supplied software shall be sufficient to allow top-level FORTRAN/ ALGOL statements to provide Input/Output data transfer to all peripherals.

Relocatability, and automatic page-free linking up to 16K memory, is required of all FORTRAN/ALGOL and assembler generated code.

On-line debugging and computer self-test routines are required.

3.1 Internal Data Representation

Sixteen bit fixed point and thirty-two bit floating point numeric data representation shall be used. Software routines shall be provided to implement the fixed and floating point operations addition, subtraction, multiplication, and division, as well as the floating point operations sine, cosine, tangent, square root, arctangent, hyperbolic tangent, natural log, and natural exponentiation.

3.1.1 Fixed Point Data Word Format

Fixed point numbers should be represented in two's complement form, fifteen bits plus sign. Thus, the range of fixed point numbers should be -32,768 to +32,767.

3.1.2 Floating Point Data Word Format

Floating point numbers should be represented in mantissa and exponent form. The mantissa should be normalized, and encompass 23 bits plus sign, thus yielding about seven decimal digits precision. The exponent should encompass seven bits plus sign, thus yielding a range of ±38.

3.2 Symbolic Assembler Program

A symbolic assembler program should be provided which will operate in a minimum configuration (8192 word, Teletype only) system, and which will generate absolute or page-independent relocatable machine code.

In order to perform floating point operations in assembly language programs, relocatable assembly language programs should have access to the FORTRAN/ALGOL floating point package including routine for floating addition, subtraction, multiplication, division, and the SIN, COS, TAN, ATAN, EXP, and SQRT functions.

In order to read and write numeric and alphanumeric information under Format Control, relocatable assembly language programs should have access to the FORTRAN/ALGOL Input/Output Package, such that ASCII buffers can be read in or written under interrupt control, and generated or broken down in memory under Format Control.

In order to initialize constants and ASCII string, assembler pseudo instructions should convert integers, floating point numbers, and ASCII strings into appropriate machine code.

A cross-reference table generator routine should provide an alphabetical list of all assembly language labels, and line numbers of the assembly language statements which reference each label.

3.3 FORTRAN Compiler

The FORTRAN Compiler should operate in a minimum configuration system and produce page-independent relocatable machine code from source programs written in American Standards Association Basic FORTRAN.

In order to allow ease of data entry, the FORTRAN Formatter Package shall provide free-field input capability, which will allow numeric data to be entered without regard for column spacing or decimal points, the Formatter should also provide "A", "E", "F", "H", "I", "O", "X", and QUOTE FORMAT capability.

In order to provide maximum use of computer time, output generated by FORTRAN "WRITE" statements shall be automatically dynamically stored in free core, such that buffers can stack up and wait for device availability without slowing down computation.

Subroutines, Functions, and Statement Functions shall link as required to FORTRAN and relocatable Assembly Language programs anywhere in memory.

The compiler shall optionally produce a source listing and an object listing showing the assembly code generated, and an object tape suitable for relocatable loading.

3.4 Input/Output Package

A modular software Input/Output Package which can be configured to the Input/Output channel locations of the peripherals should be provided. The I/O package should provide logical to physical unit number translation, to allow device independent programming.

The Input/Output Package should implement simultaneous I/O of ASCII or binary buffers on all peripherals under interrupt control.

3.5 Math Subroutine Library

The math subroutine library should contain all of the math routines necessary to implement FORTRAN as described in Section 3.3. Speed of these routines without the Extended Arithmetic Unit should be sufficient to run the following FORTRAN routine in 100 milliseconds:

```
X = ALOG (Y*Z)
X = ATAN (Y*Z)
X = COS (Y*Z)
X = EXP (Y*Z)
X = SIN (Y*Z)
X = SQRT (Y*Z)
X = TAN (Y*Z)
X = Y + Z
X = Y - Z
X = Y*Z
X = Y/Z
X = ABS (Z)
X = FLOAT (I)
```

3.6 Relocating, Linking Loader

A software loader capable of loading and linking together relocatable programs and subroutine shall be provided. The loader shall insert indirect base page linkages as necessary, so that any program in memory can link to any subroutine in memory.

In a "library load" mode, the loader shall read the Math Subroutine Library described in Section 3.5, and load only those routines required by the programs and subroutines previously loaded.

A technique for using the core memory required by the loader shall be provided such that relocatable programs may overlay the loader.

3.7 On Line Debugging Program

A relocatable "debugging" program which interpretively executes other relocatable programs in "debug" mode shall be provided. The "debugging" pro-

gram shall allow "trace" of program segments and should not interfere with normal Input/Output functions. The "debugging" program should provide core dumps of specified areas in memory, and allow initiation of execution at any point in memory.

3.8 ALGOL Compiler

The ALGOL Compiler should operate in a minimum configuration system and produce page-independent relocatable machine code from programs written in an implementation of ALGOL 60.

In order to allow ease of data entry, the ALGOL Formatter Package should provide free-field input capability, which will allow numeric data to be entered without regard for column spacing or decimal points. The Formatter should also provide "A", "E", "F", "H", "I", "O", "X", and QUOTE FORMAT capability.

In order to provide maximum use of computer time, output generated by ALGOL "WRITE" statements shall be automatically dynamically stored in free memory, such that buffers can stack up and wait for device availability without slowing down computation.

The ALGOL Compiler should allow initialization of variables or arrays within type declarations, or allow values to be assigned to variables during compilation with EQUATE statements.

ALGOL should contain character manipulation operations, and allow ASCII as well as decimal and integer and octal constants.

3.9 Data Acquisition Executive Program

A data acquisition Executive Program should allow manual execution of data acquisition subroutines, automatic queuing of subroutines based upon interval times entered on the Teletype, and ability to look at and change computing constants, high and low limits, channel numbers, etc., which are contained in arrays within data acquisition subroutines.

Subroutines for giving real time based upon a hardware time base generator, and for operating a digital voltmeter and scanner under interrupt shall be provided.

FORTRAN subroutine calls should return the time of day and initiate a block or random data channel scans which operate under interrupt. In conjunction with the FORTRAN buffered output package, it should be possible to take data, compute on previous data, and output on all devices simultaneously under interrupt.

3.10 BASIC Compiler

A Basic Compiler should operate in a minimum configuration system, and should accept programs entered from the teleprinter in a language similar to GE-BASIC.

Operationally, BASIC should make use of a high speed paper tape reader and high speed paper tape punch, if these are included in the system.

The BASIC Compiler should accept BASIC Language statements, and provide syntax diagnostics during entry. The Compiler should have provisions for listing the program as entered, editing the program, interpretively executing the program, and punching the program onto paper tape.

System functions should include SIN, COS, TAN, ATN, EXP, LOG, ABS, and SQR. Using the GOSUB statement, it should be possible to execute user subroutines.

BASIC Matrix operations should include:

setting a matrix to all zeros,

setting a matrix to all ones,

setting one matrix equal to another,

adding, subtracting, multiplying, inverting and transposing matrixes,

multiplying all elements of a matrix by an expression.

Technique should be available to link assembly language subroutines into the BASIC environment.

3.11 Time Shared BASIC

A Time Shared version of the BASIC Compiler should allow up to 16 teleprinters simultaneous access to the computer, and may require 16K of memory and a disc.

Time Shared BASIC should contain a library system, which will allow a library of programs to be stored on the disc, and be retrieved and executed by user stations.

An accounting scheme should be built into the system, which will keep track of the time used by each of the consoles.

3.12 Real-Time Executive

A Real-Time Executive program should allow execution of a large number of programs on a priority basis, with program storage in disc memory, and automatic swapping as required.

Such an executive system should encompass real-time priority programs, and background programs which would generally be of lower priority. Background operations could include FORTRAN Compilation, loading, and debugging, while foreground operations could include data taking and logging programs, as well as high priority response programs which could be executed in response to an abnormal system condition.

The Real-Time Executive program should handle all scheduling and all disc swapping; and it should provide extra disc storage space to programs requiring additional storage space for temporary or long term records.

The Executive should respond to a system keyboard, which may be used to change program priority, initiate or terminate program operation, and to select background programs.

3.13 Magnetic Tape System

When a high speed 7-track magnetic tape transport is supplied, additional software should be provided for loading the compiler, assembler, and other standard software selectively from magnetic tape.

Magnetic tape assisted compilation and assembly should effectively require only one pass: the computer should accept the source tape and produce the final binary tape without requiring any intervention on the part of the operator.

Magnetic Tape assisted relocatable loading should provide facilities for the relocating loader, the input/output package, and the system library to be loaded directly from magnetic tape, so that the operator need only load the relocatable binary tapes which comprise his software programs.

(Note: Magnetic Tape System requires photoreader.)

3.14 Computer Self-Test Routines

Standard software shall include diagnostic routines which will test all computer instructions and every location in memory. These tests should be done in a cascading fashion, such that instructions used in the test are tested before they are used as part of the test program. Documentation of these tests is required.

3.15 Peripheral Diagnostics

Standard software shall include diagnostic routines which will test each peripheral. These routines shall isolate any peripheral faults which may be detected under computer control. Documentation of these tests is required.

4.0 DOCUMENTATION

Well illustrated, clearly written, hardware and software manuals shall be included with the system at the time of delivery. These manuals shall cover operating instructions, dimensions, weight, power, installation, programming, theory of operation, logic equations, replaceable parts, diagnostic programs, complete schematics, and cable data for interconnections to peripherals.

4.1 Hardware Manuals

Hardware manuals shall be provided for the central processor and all peripherals. The manuals shall cover the theory of operation, schematics of all circuits, parts lists, and, for the central processor, backplane wiring lists.

4.1.1 Installation

Installation instructions shall cover initial inspection, environmental limits and requirements, power requirements, and conversion to and from rack mount configuration.

4.1.2 Operation

Operation instructions shall describe the use and function of each button, switch, etc., locations and functions of each control indicator, and input/output connections.

4.1.3 Principles of Operation

An insight should be provided as to how the computer functions on a block diagram level. Detailed explanation should be provided where it is required for computer maintenance, trouble-shooting, or testing.

4.1.4 Maintenance

Hardware manuals shall outline preventive maintenance procedures, and recommended readjustment or recalibration times where appropriate.

Component location and test points should be fully described, and pertinent waveforms and voltages should be documented; complete schematics must be provided.

4.1.5 Replaceable Parts

Spare parts should be available from the vendor. A table of spare parts by schematic reference designation should be provided which references the schematic reference designation to vendor part number.

A cross-reference between vendor part numbers and commercial part numbers is desirable.

The vendor shall provide the following parts lists for the computer and for each peripheral:

1) Component List
2) Circuit Board List
3) One year's recommended spares
4) One year's isolated spares

4.2 Software Manuals

Clearly written, indexed, and bound software manuals shall be provided for every programming system (FORTRAN, ALGOL, BASIC, Assembler, Library, Input/Output Package, etc.). Programmer's reference manuals shall be shipped with or before the system, and shall cover every detail of the software systems that would reflect the external specifications of those systems.

Listings of all supplied software shall be available from the vendor, as well as source files on paper tape.

Updates to the software manuals shall be provided when software systems are updated.

4.2.1 FORTRAN/ALGOL

The FORTRAN Manual shall cover arithmetic expressions and assignment statements, specification statements, control statements, argument characteristics of subroutines and functions, Input/Output Data Lists and FORMAT Control, use of the compiler, sample programs, and digest of compiler generated error messages.

4.2.2 Assembler

The Assembler Manual shall cover assembly language instructions and pseudo instructions, use of the assembler package, use of the FORTRAN/ALGOL Formatter package from assembly language, use of the Input/Output package from assembly language, sample programs, and a digest of assembler generated error messages.

4.2.3 Library Routines

The Library Manual shall cover the calling sequences to the math library and service subroutines, from FORTRAN and from Assembly language programs. The Library Manual should also describe the length, accuracy, and speed of the Library subroutines.

4.2.4 Input/Output Configuration

The I/O Software Manual shall cover the process of configuration of the I/O package to the peripheral channel locations. A description of the calling sequence to the I/O package should be provided, along with sample programs.

4.2.5 Diagnostic Routines

Diagnostic Software should be supplied for every peripheral and for the central processor. Peripheral diagnostic programs should test the capabilities of the peripheral under interrupt where applicable.

Documentation of Diagnostic Software should contain step-by-step operating instructions, a narrative description of the test being performed, and a listing of the source program for the diagnostic.

5.0 MAINTAINABILITY

All internal control and adjustments shall be located so as to be readily accessible. All central processor circuitry and memory circuitry should be accessible from the front of the computer. Accessibility shall not be hampered by mounting in a standard 19" equipment enclosure.

5.1 Service Accessories

One set of all accessories required to operate and maintain the computer shall be provided and shall include but not be limited by the following:

5.1.1 Special Tools

All special tools (not normally found in an electronic technician's tool box) required to wire, connect, disconnect, assemble, and disassemble the unit of its components for maintenance and operation shall be provided.

5.1.2 Extenders

Card extenders shall be provided such that all connections on any circuit board in the central processor, memory, and Input/Output circuitry may be easily reached with a normal oscilloscope probe while the circuit card operates in the unit.

5.2 Test Points

All test points should be accessible from the front of the computer. Power supply voltages should be brought out to pin or jack connectors easily accessible from the front of the unit.

6.0 INSTALLATION

The vendor shall install the computer and demonstrate successful operation of the computer self-test routines specified in Section 3.14.

Standard software packages shall be demonstrated to show compliance with this specification.

7.0 WARRANTY

The computer shall be covered with a one year parts and service warranty. If defects in material or workmanship are found during the warranty period, the unit shall be repaired or replaced by the vendor.

8.0 TRAINING

The vendor shall provide hardware and software training courses. Training aids including films, slides, and student material used in the courses shall be available from the vendor so that the training courses may be given at customer sites.

8.1 Software Course

Prior to purchase of the computer system, the vendor should provide a comprehensive software training course sufficient to train inexperienced personnel in FORTRAN and Assembly language programming.

8.2 Hardware Course

Subsequent to purchase of the computer, the vendor shall provide a comprehensive computer maintenance course sufficient to train personnel, experienced in the field of electronic maintenance, to maintain the central processor. Additional training on peripheral maintenance shall be available.