A700 User Control Store
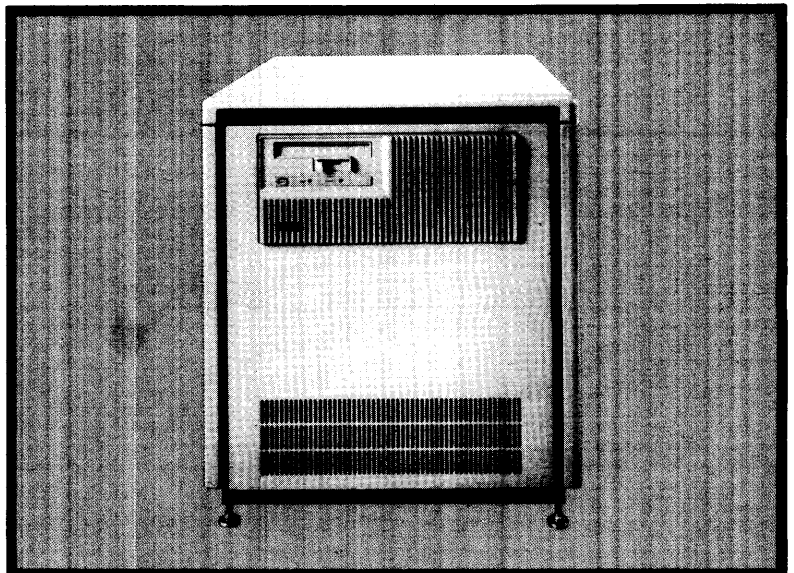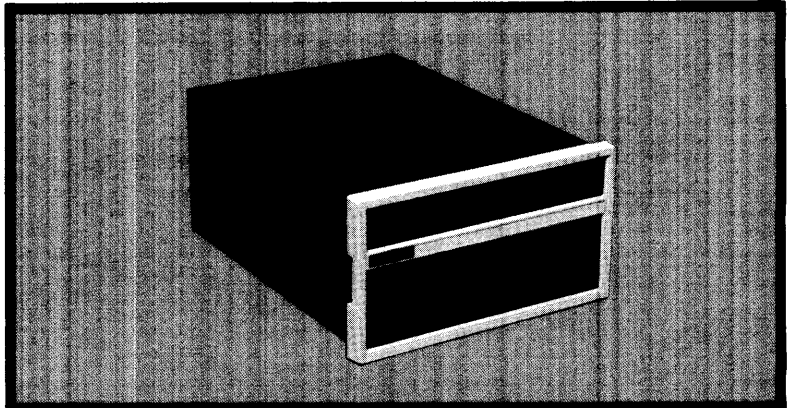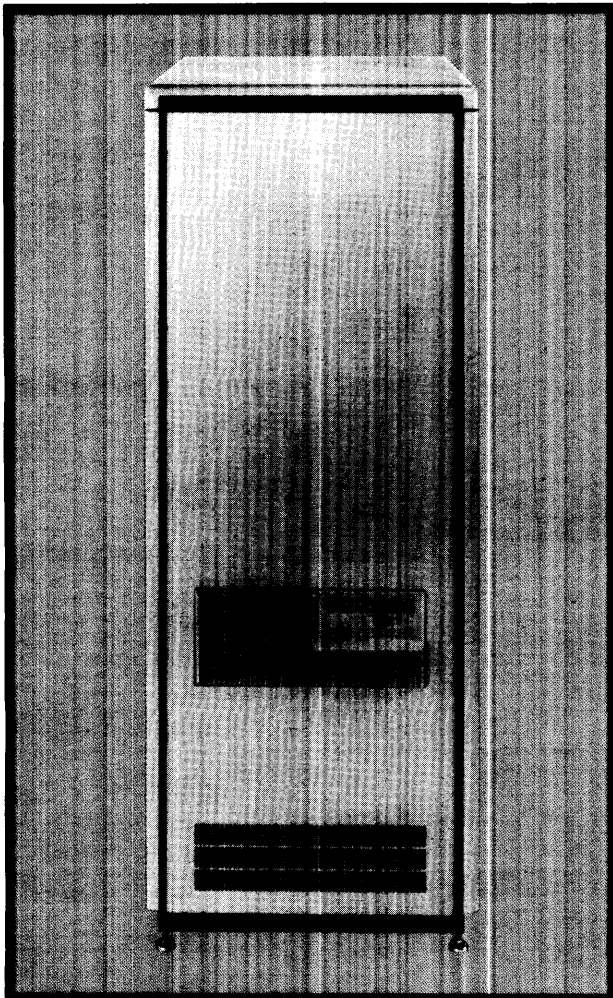
Installation and Reference Manual

HP1000
A-Series

A700 User Control Store

Installation and Reference Manual

PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, Update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past Updates, however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all Updates.

To determine what software manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

First Edition .... Mar 1982
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Reprint .... Jul 1982   Update 1 incorporated.

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ILLUSTRATIONS

TABLES

GENERAL INFORMATION

1-1. INTRODUCTION

This manual provides general information, installation procedures, and programming information for the HP 12153A Writable Control Store (WCS) and HP 12155A PROM Control Store (PCS) cards for the HP 1000 A700 Computer.

1-2. DESCRIPTION

The WCS and PCS cards provide the computer system with the internal computer hardware required to develop, store, and execute user-designed microprograms, and operate as an extension of the computer base set. With the WCS card installed, microprograms can be loaded into the WCS via the computer I/O system, and executed by the computer processor during the microprogram development phase. Completed microprograms can then be permanently stored in PROMs on the PCS card, and executed whenever addressed by macrocode instructions in the computer processor.

The PCS and WCS cards install in unassigned card slots in the computer card cage. Up to four separate control store function cards (including the floating point processor card) can be installed in the computer card cage.

1-3. UNPACKING

If ordered separately from the computer system, inspect the WCS/PCS shipping carton contents upon arrival for possible damage during shipment. If any kit items are damaged, contact the shipping agent immediately for claims adjustment procedures, and the nearest Hewlett-Packard Sales and Service Office for replacement of the damaged items.

1-4. CARD IDENTIFICATION

The WCS and PCS card part number is located in the lower right corner, on the component side of the card. Reference this part number in all correspondence concerning the WCS and PCS card.

1-5. RESHIPMENT

Prior to returning the WCS or PCS card to Hewlett-Packard for repair, attach a tag to the card identifying the owner and indicating the service to be performed.

NOTE

Remove all PROM chips from the PCS card before reshipment,
for reinstallation when the card is returned or replaced.

1-6. ADDITIONAL INFORMATION

For additional information on programming and use of the WCS and PCS cards, refer to the following:

- HP 1000 A700 Computer Reference Manual, Part No. 02137-90001

- HP 1000 A700 Computer Installation and Service Manual, Part No. 02137-90002

- HP 92045A Microprogramming Package Reference Manual, Part No. 92045-90001.

2-1. INTRODUCTION

This chapter provides general information, installation procedures, and programming information for the HP 12153A Writable Control Store option.

2-2. DESCRIPTION

The HP 12153A Writable Control Store (WCS) card (Figure 2-1) provides temporary addressable storage of up to 4096 (4k) 32-bit microprogram instructions that operate as an extension of the computer base set instructions.

Microprograms developed by the user are loaded into the WCS card via the computer I/O system, and enabled to the computer processor frontplane for execution, all under I/O program control.

Whenever the WCS card is loaded with microinstructions, the 4k of RAM storage on that card is programmatically mapped into the overall computer control store 16k address scheme of 16 separate 1k logical modules.

The WCS card mounts in the computer card cage just to the left of the Lower Processor card (see Figure 2-2). Card cage backplane interconnect for the WCS provides I/O system interface and required power, while the flexible control store cable provides address, data, and control interface to the processor frontplane. Operation of the WCS card is under program control, with both programmed I/O and direct memory access (DMA) capability.
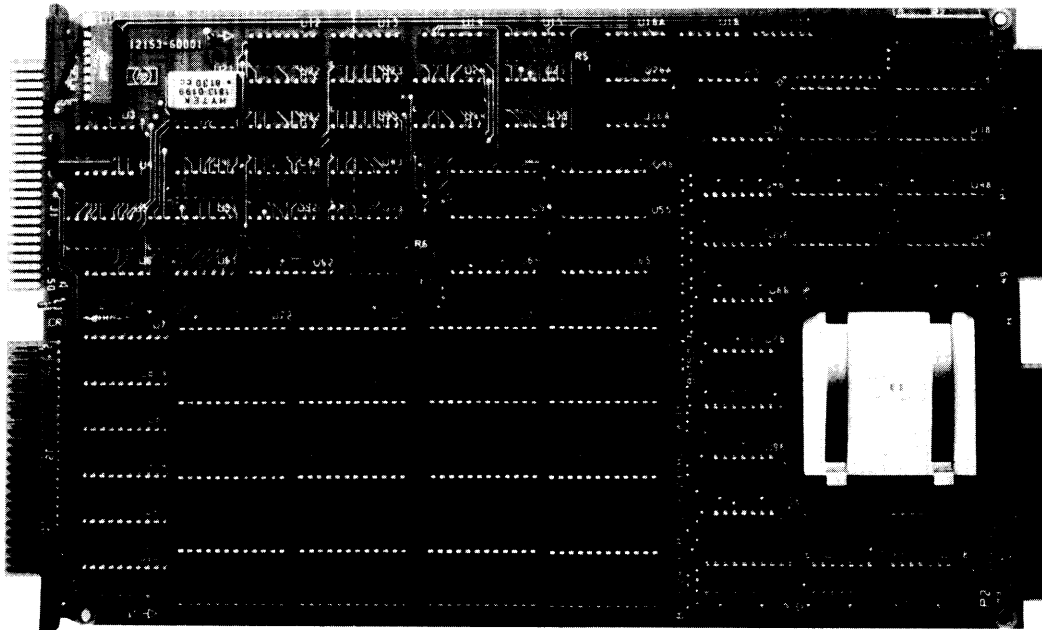
Figure 2-1. HP 12153A Writable Control Store Card

2-3.   EQUIPMENT SUPPLIED

The following provides a list of equipment supplied with the WCS option:

- HP 12153-60001 Writable Control Store Card

- Control Store Flexible Frontplane Connector, Part No. 5061-3480

- HP 1000 A700 User Control Store Installation and Reference Manual, Part No. 02137-90003.

2-4.   SPECIFICATIONS

Table 2-1 provides the specifications for the WCS card.

Table 2-1. HP 12153A Writable Control Store Card Specifications

ELECTRICAL CHARACTERISTICS
Required Power: 21.19 Watts Maximum at +5V
0.73 Watts Maximum at +12V
Required Current: 5.42 Amps Maximum
OPERATING TEMPERATURE
0 to +55 Degrees Celsius
(32 to 131 Degrees Fahrenheit)
PHYSICAL DIMENSIONS
Length: 28.91 cm (11.38 in)
Width: 17.15 cm (6.75 in)
CONTROL STORE CAPACITY
32-bit by 4k words (4 logical modules)
DMA TRANSFER RATE
Word Mode: Input − 711k words/sec
Output − 592k words/sec
Byte Mode: Input − 507k words/sec
Output − 444k words/sec

2-5.   SELECT CODE ASSIGNMENT

Before installing the WCS card, ensure that the I/O select code eight-element DIP switch (near the left front card edge) has been set to the proper select code for the card. Switch elements are numbered 1 through 8, left-to-right, with elements 3 through 8 set to the card octal select code (element 1 must be OPEN; element 2 is not used).

An open switch represents a logic 1; a closed switch a logic 0, with element 3 as the most significant bit (MSB).

2-6. INSTALLATION

$$\boxed{\textbf{CAUTION}}$$

Static sensitive devices. Use antistatic procedures when
handling printed circuit assemblies.

To install the WCS card, complete the following steps:

a. Ensure that computer power is OFF, open the computer card cage access panel, and
    remove the processor card frontplane board.

b. Insert the WCS card (component side to the right) just to the left of the Lower Processor
    card, and in desired proximity to existing control store cards as determined by front plane
    priority (see Figure 2-2).

NOTE

As shown in Figure 2-2, there can be no empty card slots
between the Lower Processor card, control store cards, and any
I/O cards. This is required in order to maintain computer
backplane I/O interrupt daisy-chain integrity.

CONTROL STORE OPTION

CONTROL STORE OPTION

CONTROL STORE OPTION

I/O CARD

I/O CARD

I/O CARD

LOWER PROCESSOR

FLOATING POINT OPTION

UPPER PROCESSOR

MEMORY CONTROLLER

MEMORY ARRAY(S)
(1 THRU 4 CARDS)

FRONTPLANE PRIORITY
(CONTROL STORE)   *1   2   3   5   4

BACKPLANE PRIORITY   6   5   4   3   2   *1

(CARD ACCESS VIEW)

*1 = HIGHEST PRIORITY

8200-1
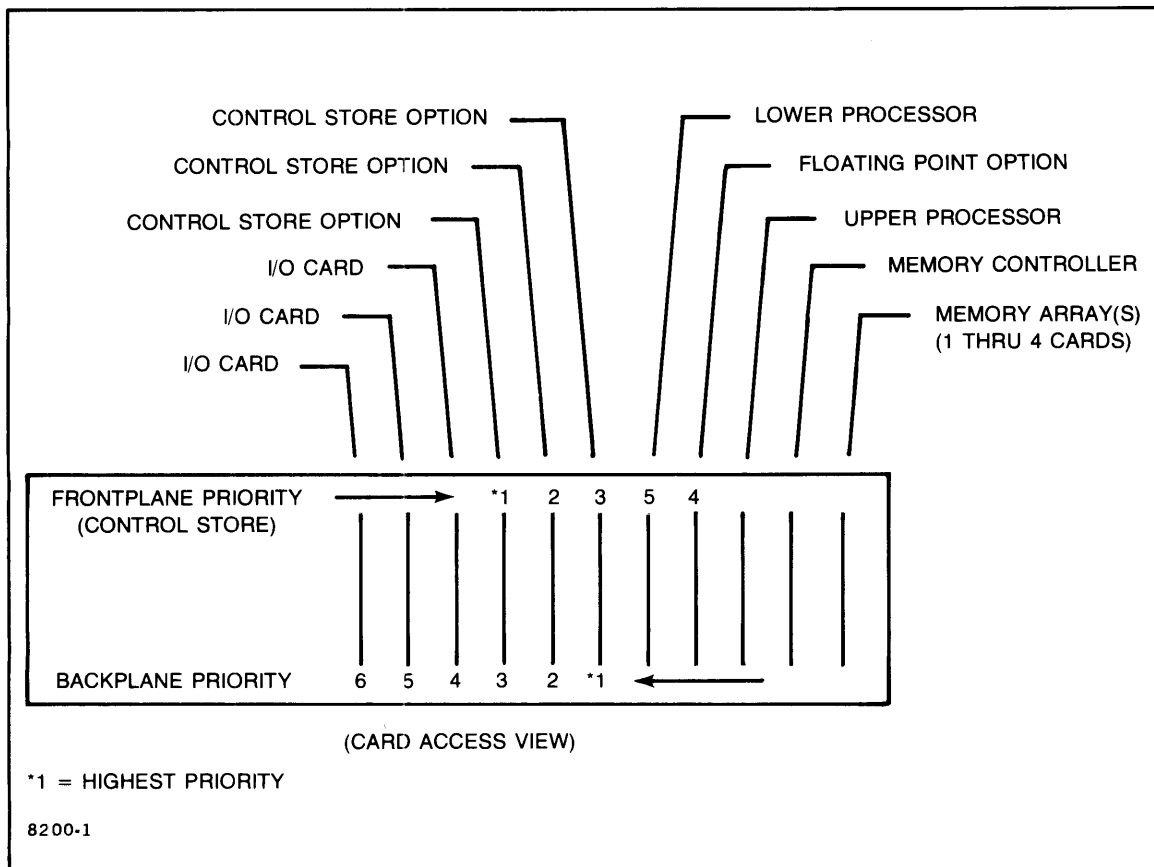
Figure 2-2. Card Cage Loading Diagram

c. Using a pair of sharp scissors, cut the control store flexible cable as close as possible to the far side of the selected connector, as shown in Figure 2-3, as required to fit the new control store card configuration. Cut the self-adhering foam strip to cover the exposed pins of the remaining control store connectors on the flexible cable (Figure 2-3, A thru D). Attach the foam strip to the flexible cable, covering the sharp exposed pins, as a push-pad when attaching the control store flexible cable.

CAUTION

To prevent shorting any signal traces to the grounding mesh in the flexible cable, cut the cable as closely as possible to the far side of the selected card connector, and within the small open space in the grounding mesh.
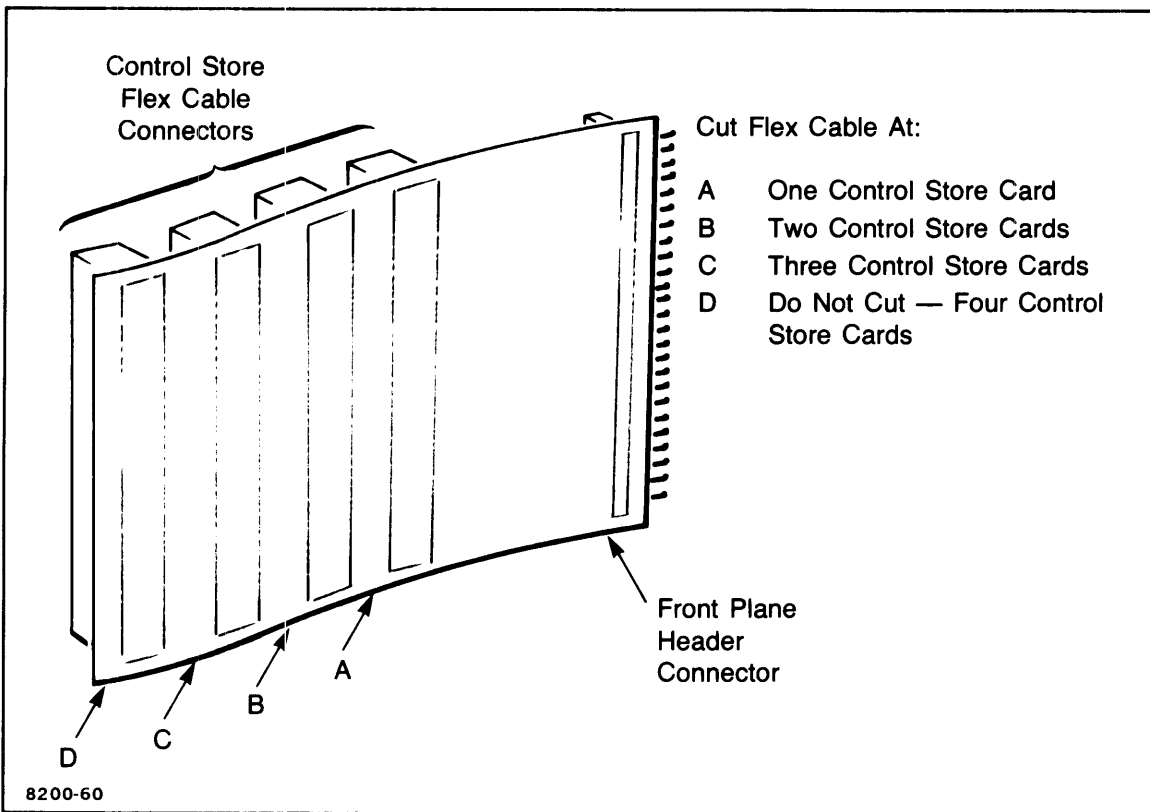
Figure 2-3. Flexible Cable Configuration

d. Connect the flexible cable header connector to the frontplane board control store connector, and reinstall the frontplane board (see Figure 2-4). Attach the flexible cable control store connectors to all installed control store cards, and complete the operational checkout procedures referenced in paragraph 2-7.

8200-61
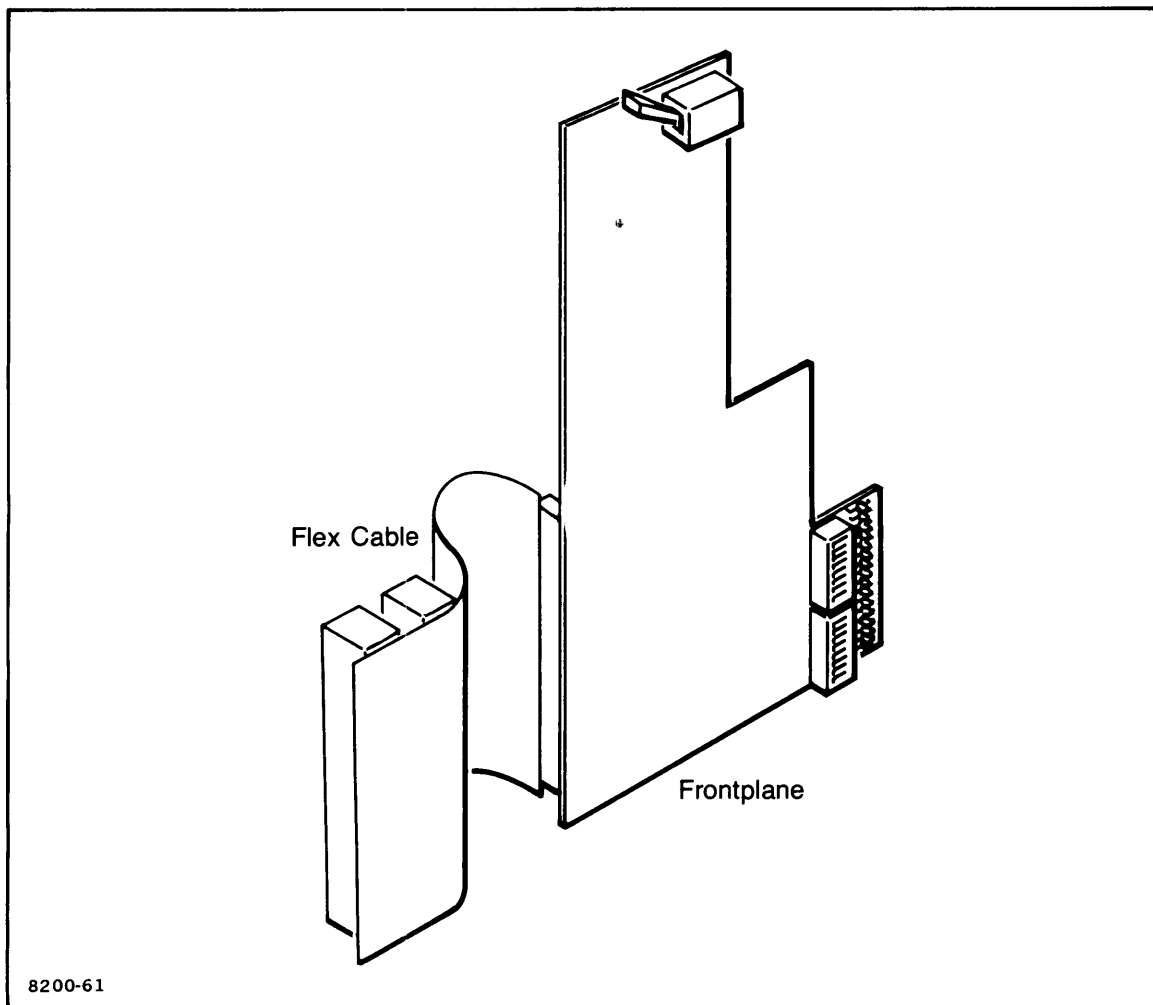
Figure 2-4. Flex Cable Interconnect

2-7. OPERATIONAL CHECKOUT

Load and run the WCS diagnostic test to ensure proper WCS operation (refer to the HP 1000 A-Series Computer Kernel Diagnostic Reference Manual, Part No. 24612-90003).

2-8. PROGRAMMING CONSIDERATIONS

This subsection provides general programming considerations for the WCS card, including frontplane interface, backplane interface, address mapping, direct memory access (DMA) operation, programmed I/O interface, word format, and programming examples.

2-9. FRONTPLANE INTERFACE

The WCS flexible cable provides address, data, and control signal interconnect between the WCS card and the Lower Processor. Access to the frontplane for the WCS card is under program control, and is enabled only when the WCS card is in the ON state. A green LED located on the front of the WCS card illuminates whenever the card is in the ON state.

With the proper select code stored in the Global Register, frontplane access for the WCS card is enabled and disabled by the following backplane I/O instructions (refer to paragraph 2-10):

OTA 32 (Sign bit of A = 1)
            Turns WCS card ON, and enables card access to the frontplane

OTA 32 (Sign bit of A = 0)
            Turns WCS card OFF, and disables card access to frontplane bus.

When in the ON state, and when the microinstruction being addressed is located on the WCS card, the WCS card disables the base set instruction firmware and all other installed control store cards of a lower frontplane priority.

2-10. BACKPLANE INTERFACE

Backplane interface for the WCS card is provided through standard I/O Master logic, and is under program control (refer to the HP 1000 Computer L-Series Computer I/O Interfacing Guide, Part No. 02103-90005). Backplane access to the card I/O Master logic and card contents require that the WCS card be in the OFF state (frontplane access disabled) and, with the exception of the CLC 0 instruction, that the Global Register be loaded with the card select code and enabled.

The following is a summary of I/O instructions executed on the WCS card via the computer backplane.

OTA/B 30   Writes into data RAMs or map RAM
LIA/B 30   Reads data RAMs or map RAM

OTA/B 31   Writes WCS address of data transfer
LIA/B 31   Reads WCS address of data transfer

OTA/B 32   Turns WCS ON or OFF (to frontplane access)
LIA/B 32   Reads WCS ON or OFF status

STC 30   Controls address increment in programmed I/O
CLC 30   Clears Flag 30

2-11. ADDRESS MAPPING

The 4k by 32-bit control store RAM area on each WCS card is arranged into four physical banks of 1k each. Each of these banks must be address mapped as one of the 16 1k logical modules of the overall computer control store address space. Address mapping of each RAM bank is determined by the programmer, and is accomplished when the card is loaded via the backplane I/O interface.

To provide WCS address mapping, an on-board map RAM provides sixteen (16) 4-bit map words, each word representing the address of a 1k logical module within the computer control store address scheme. When the WCS card is loaded with microinstructions under programmed I/O or DMA control, the WCS map RAM must be loaded with a control store logical module address for each of the four 1k RAM banks on the WCS card.

The four map RAM words that assign logical module addresses to the WCS RAM banks must contain the following bit pattern, as shown in the example in Table 2-2:

- Bit 3 (MSB) – 1
- Bit 2   – Not used (don't care)
- Bit 1   – Bits 1 and 0; one's complement RAM Bank address
- Bit 0 (LSB) – (0 thru 3) of logical modules on the WCS card.

If total WCS address space is exceeded (program counter greater than 4095) while loading the data RAMs, the DMA loading operation will cause an I/O interrupt of the loading operation. Refer to the HP 1000 L-Series Computer I/O Interfacing Guide, Part No. 02103-90005 for information on DMA interrupts caused by address overflow.

Table 2-2. Map RAM Bit Pattern Example

LOGICAL MODULE	RAM BANK ADDRESS*			
	3	2	1	0
0	0	X	0	0
1	0	X	0	0
2	0	X	0	0
3	0	X	0	0
4	0	X	0	0
5	1	X	0	0*
6	0	X	0	0
7	1	X	1	1*
8	0	X	0	0
9	0	X	0	0
10	0	X	0	0
11	1	X	1	0*
12	0	X	0	0
13	1	X	0	1*
14	0	X	0	0
15	0	X	0	0

X = Don't Care Bit Value
* = One's Complement Bit Pattern

NOTE

Logical Module 5 Mapped to Physical Bank 3
Logical Module 7 Mapped to Physical Bank 0
Logical Module 11 Mapped to Physical Bank 1
Logical Module 13 Mapped to Physical Bank 2

2-12. DIRECT MEMORY ACCESS (DMA) OPERATION

Direct memory access (DMA) operations transfer data to and from the WCS card via the standard I/O system, and operate with the following restrictions on DMA Control Word 1 (refer to the HP 1000 A700 Computer Reference Manual, Part No. 02137-90001).

- Bit 14 – DVCMD; must be set
- Bit 13 – BYTE; clear for data RAM, set for map RAM
- Bit 8 – AUTO; must be clear for input, set for output transfer

2-13. PROGRAMMED I/O INTERFACE

User interface to the WCS card is provided by the backplane I/O system and software. Backplane access to the WCS card is enabled only when the card is in the OFF state (paragraph 2-9), the Global Register contains the card select code, and the Global Register is enabled.

The following provides a list of I/O applications with corresponding I/O instructions and required bit patterns:

Turns WCS ON
> OTA 32   – sign bit of A contains 1

Turns WCS OFF
> OTA 32   – sign bit of A contains 0

Reads status of WCS card
> LIA 32   – sign bit of A is 1 = WCS ON; 0 = WCS OFF

Address data RAMs
> OTA/B 31 – A/B must contain data RAM address in bits 0-11, 0 in bit 12
> 0 in bit 12
> 0/1 in bit 13 (don't care)
> 0 in bit 14 to select data RAMs
> 0 in bit 15 = lower half word; 1 = upper half

Address map RAM
> OTA/B 31 – A/B must contain map RAM address in bits 0-3
> 1 in bits 4-11
> 0 in bit 12
> 0/1 in bit 13 (don't care)
> 1 in bit 14 to select map RAM
> 0 in bit 15

Writes data to data RAMs
> OTA/B 30 – A/B contains half microword (16 bits)
>
> In DMA, address is automatically incremented; half microinstruction output each transfer. Data should start with lower half word (sign bit of address = 0).
>
> In programmed I/O, new address must be loaded each transfer, or STC 30 issued after each OTA/B 30, to increment address counter.

Reads data from data RAMS
> LIA/B 30 – Half microword returned in A/B. Lower half when address sign bit = 0; upper half when 1.
> Address increment same as writing to data RAMs.

Writes to map RAM
   OTA/B 30 – Data in bits 0-3 of A/B.

> Address counter must increment twice between each data transfer to or from map RAM.
>
> In DMA, BYTE bit must be set in Control Word 1 to increment the address counter twice.
>
> In programmed I/O, new address must be loaded for each transfer, or STC 30 issued twice, for proper address increment.

Reads map RAM
   LIA/B 30 – One's complement of map RAM data returned in A/B bits 0-3. Address increment same as writing to map RAM.

2-14. WORD FORMAT

The following provides a list of WCS card I/O word formats:

   X = Any Bit Value
   A = Address Word Bit
   D = Data Bit
   M = Microword Bit

Data RAM Address

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1/0	0	X	0	A	A	A	A	A	A	A	A	A	A	A	A

Map RAM Address

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	X	0	1	1	1	1	1	1	1	1	A	A	A	A

Read Data RAM Data (32 Bits)

Lower half-word, sign bit of address = 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Upper half-word, sign bit of address = 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Write Map RAM Data (One's Complement)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	D	X	D	D
											0	1	X	1	1
											1	1	X	1	0
											2	1	X	0	1
											3	1	X	0	0
											0	X	0	0

Read Map RAM Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	D	X	D	D
											0	0	X	0	0
											1	0	X	0	1
											2	0	X	1	0
											3	0	X	1	1
												1	X	1	1

Inserts for above

Physical Bank   —
Physical Bank   —
Physical Bank   —
Physical Bank   —
No Physical Bank   —

Physical Bank   —
Physical Bank   —
Physical Bank   —
Physical Bank   —
No Physical Bank   —

2-15. PROGRAMMING EXAMPLES

In the programming examples below, operand definitions are as follows:

SELCD — Select Code of WCS Card
COUNT — Complement of Number of Words to be Transferred
AAAAA — Address Bits
XXXXX — Can be Any Value, User Defined
CCCCC — COUNT Value
( ) — Binary Number Enclosed in Parentheses
MDATA — Complement of Map Data in Bits 0-3, Bits 4-15 Any Value
RDATA — RAM Data

Control Store Operation

Turn ON WCS

LDA	SELCD	Load and enable Global Register
OTA	2,C	
.		
.		
.		
LDA	1XXXXXB	Turn board ON
OTA	32B	

Turn OFF WCS

LDA	SELCD	Load and enable Global Register
OTA	2,C	
.		
.		
.		
LDA	0XXXXXB	Turn board OFF
OTA	32B	

Read Status of WCS

LDA	SELCD	Load and enable Global Register
OTA	2,C	
.		
.		
.		
LIA	32B	Status in sign bit of A

Programmed I/O Operation (WCS Card Turned OFF)

Load Map RAM

```
            LDA   SELCD           Load and enable Global Register
            OTA   2,C
            .
            .
            .
            LDA   0677(11A)AB      Map RAM address in A
            OTA   31B             Load address counter
MLOOP       LDA   MDATA           Map RAM data in A
            OTA   30B             Output data
            STC   30B,C           Increment address
            STC   30B,C
            ISZ   COUNT
            JMP   MLOOP
            CLC   30,C
```

Read Map RAM

```
            LDA   SELCD           Load and enable Global Register
            OTA   2,C
            .
            .
            .
            LDA   0677(11A)AB      Map RAM address in A
            OTA   31B             Output address
MWLP        LIA   30B             Read map data
            STA   MEM             Store in memory
            STC   30B,C           Increment address
            STC   30B,C
            ISZ   COUNT
            JMP   MWLP            (one's complement of map data is read)
            CLC   30,C
```

Load and Enable RAMs

```
            LDA   SELCD           Load and enable Global Register
            OTA   2,C
            .
            .
            .
            LDA   00AAAAB         RAM address in A
            OTA   31B             Output address
LOOP        LDA   RDATA           RAM data in A
            OTA   30B             Output data
            STC   30B             Increment address
            ISZ   COUNT
            JMP   LOOP
            CLC   30,C            Clear Flag 30
```

Read Data RAMs

```
           LDA  SELCD          Load and enable Global Register
           OTA  2,C
            .
            .
            .
           LDA  00AAAAB        RAM address in A
           OTA  31B            Output address
    LOOP   LIA  30B            Read RAM data
           STA  RMEM           Store in memory
           STC  30B,C          Increment address
           ISZ  COUNT
           JMP  LOOP
           CLC  30B,C          Clear flag 30
```

DMA Operation (WCS Card Turned OFF)

Load Map RAM

```
           LDA  SELCD          Load and enable Global Register
           OTA  2,C
            .
            .
            .
           LDA  BUFMW
           OTA  20B            Set up self-configuration
           STC  20B,C
           SFS  21B
           JMP  *-1
            .
            .
            .
    BUFMW  DEF  *+1
           OCT  0614XX         Control Word 1
           OCT  0677(11A)A     Map RAM address
           DEF  MEMAD          Address of map data
    COUNT  DEC  -31            Two times words -1
```

Read map RAM

```
           LDA  SELCD          Load and enable Global Register
           OTA  2,C
            .
            .
            .
           LDA  BUFMR
           OTA  20B            Set up self-configuration
           STC  20B
           SFS  21B
           JMP  *-1
```

```
                    CLC   30B,C
                     .
                     .
                     .
BUFMR               DEF   *+1
                    OCT   0612XX          Control Word 1
                    OCT   0677(11A)A      Map RAM address
                    DEF   MEMAD           Address to store data
COUNT               OCT   CCCC            Twice number of words to transfer
```

Load Data RAMs

```
                    LDA   SELCD           Load and enable Global Register
                    OTA
                     .
                     .
                     .
                    LDA   BUFDW           Set up DMA self-configuragion
                    OTA   20B
                    STC   20B,C
                    SFS   21B
                    JMP   *-1
                    CLC   30B,C
                     .
                     .
                     .
BUFDW               DEF   *+1
                    OCT   0414XX          Control Word 1
                    OCT   00AAAA          Address in RAM
                    DEF   MEMAD           Memory address of data
COUNT               OCT   CCCC            Multiple of two words
                            X
```

Read Data RAMs

```
                    LDA   SELCD           Load and enable Global Register
                    OTA   2,C
                     .
                     .
                     .
                    LDA   BUFDR
                    OTA   20B             Set up self-configuration
                    STC   20B
                    SFS   21B
                    JMP   *-1
```

```
            CLC   30B,C
             .
             .
             .
BUFDR       DEF   *+1
            OCT   0412XX              Control Word 1
            OCT   00AAAA              Data RAM address
            DEF   MEMAD               Address to store data
COUNT       OCT   CCCCC               Multiple of two words
```

Load Map RAM and Data RAMs Consecutively

```
            LDA   SELCD               Load and enable Global Register
            OTA   2,C
             .
             .
             .
            LDA   BUFF
            OTA   20B                 Set up self-configuration
            STC   20B
            SFS   21B
            JMP   *-1
            CLC   30B,C
             .
             .
             .
BUFF        DEF   *+1
            OCT   1614XX              Cont. Word 1, CONT bit set
            OCT   0477AA              Map RAM address
            DEF   MEMAD               Memory address of map data
COUNT       DEC   -31                 Twice words -1
            OCT   0414XX              Control Word 1
            OCT   00AAAA              Data RAM address
            DEF   DATAD               Memory address of RAM data
COUNT       OCT   CCCCC               Multiples of two words
```

NOTE

Bit 6 of Control Word 1 is user definable for WCS operations
(can be any value)

As illustrated in the above examples, a subroutine can be written to perform DMA self-configuration for all WCS access operations, with parameters passed in order to determine read/write, map RAM/data RAM, and other variables.

3-1. INTRODUCTION

This chapter provides general information, installation procedures, and programming reference information for the HP 12155A PROM Control Store option.

3-2. DESCRIPTION

The HP 12155A PROM Control Store (PCS) card (Figure 3-1) provides non-volatile memory storage for up to 8192 (8k) 32-bit microinstructions, and operates as an extension of the computer base set. Microprogrammed PROM chips are provided by the user, and install on the card in eight addressable banks of 1k each.

The PCS card installs in the computer card cage to the left of the lower processor, with both frontplane and backplane interconnect. The computer backplane interconnect provides only power and backplane I/O interrupt daisy-chain continuity, as the PCS card is not part of the computer I/O system. The PCS frontplane interconnect provides address, data, and control signal interface to the Lower Processor card.

Each 1k PROM bank on the PCS card is manually address-mapped as one logical module in the overall computer control store address scheme of 16 1k logical modules. These eight logical modules are then enabled to the Lower Processor via the frontplane interface for execution, when addressed.
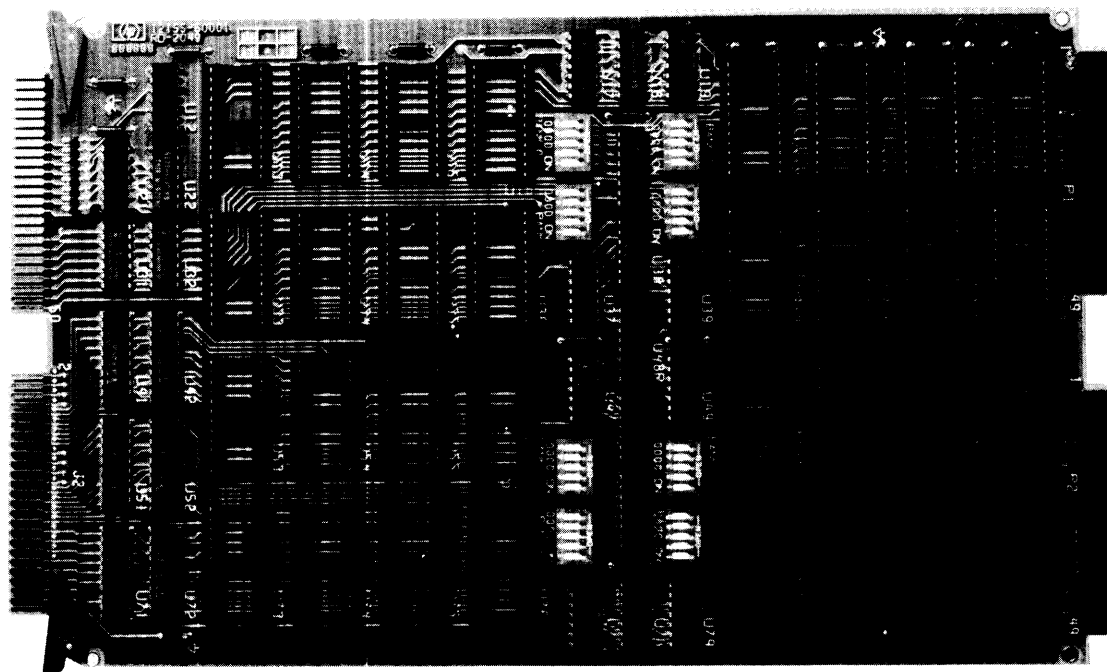

Figure 3-1. HP 12155A PROM Control Store Card

3-3.   EQUIPMENT SUPPLIED

The PCS card is shipped from the factory without PROM chips, which must be supplied by the user, and includes the following equipment.

- HP 12155A PROM Control Store Card, Part No. 12155-60001

- Control Store Flexible Frontplane Connector, Part No. 5061-3480

- User Control Store Installation and Reference Manual, Part No. 02137-90003

3-4.   SPECIFICATIONS

Table 3-1 provides the specifications of the HP 12155A PROM Control Store Card.

Table 3-1. HP 12155A PROM Control Store Card Specifications

RECOMMENDED PROM DEVICES

Signetics 82S181, Harris HM 7681-5, or any equivalent 1k by 8-bit PROM having an access time (taa) no greater than 70 nsec, chip enable access time (tea,tce) no greater than 40 nsec, and power supply current requirement no greater than 175 mA.

REQUIRED POWER

1.14 Amps RMS; card random logic only
5.42 Amps RMS; maximum loading of specified PROMs

OPERATING TEMPERATURE

0 to 55 Degrees Celsius
32 to 131 Degrees Fahrenheit

PHYSICAL DIMENSIONS

Length: 28.91 cm (11.38 in.)
Width: 17.15 cm (6.75 in.)

CONTROL STORE CAPACITY

32-bit by 8k words (8 logical modules)

3-5. PROGRAMMING REFERENCES

The PCS card is shipped from the factory without PROMs, and must be configured by the user for any particular application.

For information on microprogram development, refer to the following documents:

- HP 1000 A700 Computer Reference Manual, Part No. 02137-20001

- HP 92045A Microprogramming Package Reference Manual, Part No. 92045-90001

3-6. PROM INSTALLATION AND ADDRESS MAPPING

The PCS card can be physically configured for 1k through 8k of PROM storage, installed in addressable banks of 1k each. At installation, each 1k bank must be address-mapped as a 1k logical module within the computer control store address scheme, using the eight PROM bank address switches located on the PCS card.

When installing programmed PROMs in PROM bank sockets on the card, ensure that the alignment notch at one end of each chip package matches-up with the alignment notch on the chip socket.

CAUTION

PROM chips can be burned-out if installed backwards in PROM receptacles. Ensure that all PROMs are aligned correctly before applying power to the PCS card.

Table 3-2 provides a computer control store logical module address map, showing corresponding bit patterns required to address-map any 1k PROM bank on the PCS card to any control store logical module within the address scheme.

NOTE

Control store logical modules 0 and 1 are allocated to the 2k base set, but can be mapped-over by the PCS card if desired. Note that this will replace the microinstruction base set until logical modules 0 and 1 are released by manually address-mapping the PCS card PROM banks to other logical modules within the scheme, or disabling modules 0 and 1 with switch element 5.

Select logical modules for each bank of installed PROM, and set the bank address map switches as shown in Table 3-2. Note that all empty PROM banks must have switch element 5 in the OFF position (Table 3-2), which disables that bank. A loaded PROM bank can also be disabled by placing switch element 5 in the OFF position.

Table 3-2. Address-Mapping Switch Settings

LOGICAL MODULE NUMBER	LOGICAL MODULE ADDRESS BLOCKS			PROM BANK MAP SWITCH*				
	DECIMAL	OCTAL	HEX	5	4	3	2	1
0	0-1023	0-1777	0-3FF	ON	0	0	0	0
1	1024-2047	2000-3777	400-7FF	ON	0	0	0	1
2	2048-3071	4000-5777	800-BFF	ON	0	0	1	0
3	3072-4095	6000-7777	C00-FFF	ON	0	0	1	1
4	4096-5119	10000-11777	1000-13FF	ON	0	1	0	0
5	5120-6143	12000-13777	1400-17FF	ON	0	1	0	1
6	6144-7167	14000-15777	1800-1BFF	ON	0	1	1	0
7	7168-8191	16000-17777	1C00-1FFF	ON	0	1	1	1
8	8192-9215	20000-21777	2000-23FF	ON	1	0	0	0
9	9216-10239	22000-23777	2400-27FF	ON	1	0	0	1
10	10240-11263	24000-25777	2800-2BFF	ON	1	0	1	0
11	11264-12287	26000-27777	2C00-2FFF	ON	1	0	1	1
12	12288-13311	30000-31777	3000-33FF	ON	1	1	0	0
13	13312-14335	32000-33777	3400-37FF	ON	1	1	0	1
14	14336-15359	34000-35777	3800-3BFF	ON	1	1	1	0
15	15360-16383	36000-37777	3C00-3FFF	ON	1	1	1	1

```
    OFF=1=OPEN
*   ON=0=CLOSED
```

NOTE

PROM bank switch element 5 must be
in the OFF position when PROMs are
not installed in that bank.

3-7. INSTALLATION

Before installing the PCS card, ensure that all required PROM banks are loaded with pro-grammed PROMs, and that all map switches are properly set (refer to Table 3-2).

To install the PCS card, complete steps a through d of paragraph 2-6, with the exception of the checkout procedures referenced in step d. There are no specific checkout procedures for the PCS card.