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1 INTRODUCTION

1.1 Scope

This Engineering Product Specification (EPS) defines the Enhanced Small Device Interface Controller (ESDIC) which is a Megabus Controller (the data bus is 16 bits wide and the address bus is 24 bits wide) Printed Circuit Assembly (PWA) with logic providing control over the ESDI (serial mode only) and radially connected, maximum of two, Winchester Disk Drives (WDD's). In addition the ESDIC can connect to other devices (minidiskette or streamer tape) through unique adapters.

The ESDIC consists of one Printed Circuit Assembly (PWA) which can reside in the low priority Megabus I/O positions only as defined by the 1975 EPS # 60126298 and is also intended to be used on MRX systems on selectable basis.

1.2 Objective

To provide a subassembly enabling communication between a Megabus and ESDI devices. The subsystem consists of five parts:

- ESDI Controller motherboard assembly
- Winchester Disk Drives with radial interface cables
- Interface for two ESDI disk drives
- Minidiskette and/or Streamer Tape adapters
- Interface cables for the above
- DC power cables to the system Power

The ESDIC with the serial mode only is described in this EPS; reference other documents describing the remaining components.

1.3 Documentation

1.3.1 Related documents

60126298, EPS, Level 6 Bus (Megabus)
60149832, EPS, MRX Megabus
60149782, EPS, High Speed Disk Controller
60149612, EPS, L6 Quarter Daughter Board Subsystem
60149781, EPS, Streamer Adapter

77738019, MPI, Rev.B, Product Specification for Wren II Disk Drive Model 94156.
77738212, MPI, Rev.A, Product Specification for Wren III Disk Drive Model 94166.
77738076, MPI, Rev.D, Enhanced Small Device Interface Specification

1.3.2 Reference documents

Q4.1, PWA/PWB Testability Design Rules
MG1, Component Availability
MTG2, PWA Test Documentation Requirements
MTG4, PWA Test Monitor/Test Box Design
MTG5, PWA Quality Logic Test Creation
MTG6, PWA Test and Verification Program Creation
MTG7, PWA IC Socket Utilization
MTG8, Design for Producibility, Installability, Maintainability and Replaceability
MPDG1, PWA/PWB Producibility Guidelines
58035052, Worldwide Maintainance Requirements

1.3.3 Standards

1.3.3.1 General Design, Honeywell Standards:

B01.08, Environment, Operating
B01.09, Equipment Safety
B01.10, Environment, Transportation, Storage & Installation
B01.48, Primary Power-Utility Supplied

B03.07, Reliability - Standard Failure Rate Data Base
B03.08, Reliability Failure Rate & MTBF Predictions

B04.06, System Grounding

1.3.3.2 Product Maintainability, Honeywell Standards:

B07.11, Logic Nomenclature
B07.12, Location Reference Designation
B07.13, Identification Nomenclature for IC's, Printed Cards and Card Cages
B07.38, Logic Symbology
B07.39, Logic Block Diagrams

G02.01, FE Tools and Test Equipment Catalog
G02.05, FE Product Tools & Test Equipment

G07.01, Field Product Maintenance Documentation
G07.02, Product Manual Content Guide
G07.03, Product Style Guide for Manuals
G07.08, Major and Intermediate Block Diagrams
G07.09, Repair Documentation, Draft

1.3.3.3 **Manufacturing Testability Guidelines:**

D.002.01, PWA/PWB Testability Design Rules
MTG1, PWA Test Equipment Connection Requirements
MTG3, PWA Microdiagnostic Creation
60129949, Application Rules for Minicomputer & Terminal Products

1.4 Definitions

CRC	Cyclic Redundancy Check
CPU	Central Processor Unit
DMA	Direct Memory Access
EDAC	Error Detection and Correction
ESDI	Enhanced Small Disk Interface
HDA	Head Assembly (Disk)
HSDC	High Speed Disk Controller
LSA	Larkette Streamer Adapter
MBZ	Must be Zero
ORU	Optimum Replaceable Unit
PWA	Printed Wire Assembly
QDM	Quarter Daughter Board Diskette Adapter
QLT	Quick Logic Test
SPM	Scratch Pad Memory
RFU	Reserved for Future Use
TCD	Tape Cartridge Device
T&V	Test and Verification
WDD	Winchester Disk Drive

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2 ARCHITECTURE

2.1 Overview

The Enhanced Small Device Interface Controller (ESDIC), Figure 2.1, provides the Megabus systems with facility to store and retrieve data from mass storage media mounted on a disk drive. Up to two Winchester Disk Drives (WDD's) can be cabled to one ESDIC which can process one data transfer and several motion commands simultaneously. The ESDIC interfaces with other devices through adapters mountable on the ESDIC motherboard; all devices can function independently and interface asynchronously with the Megabus.

2.2 Major components

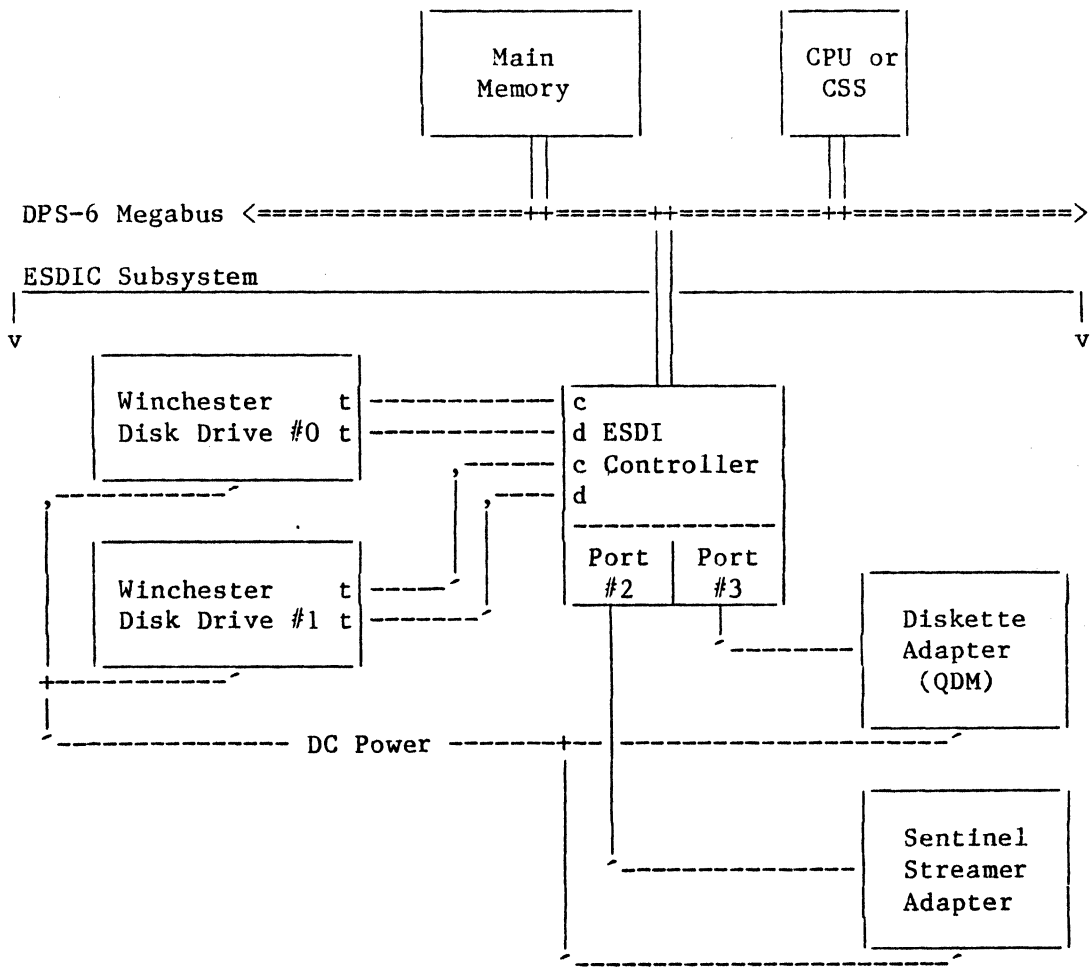
2.2.1 Disk Controller - ESDI

The ESDIC is a microprogrammed peripheral control unit which can interface up to two WDD's cabled radially via connectors mounted on the edge of the printed circuit board (PWB). The ESDIC firmware is generalized to facilitate its application as a control element for other devices interfaced through adapters. The ESDIC performs the following functions:

- Execution of Megabus I/O command sequences such as ACK, NAK, WAIT, etc...; status and control register storage in dedicated, per channel, random access memory accessible by both the ESDIC and the CPU.
- Direct Memory Access (DMA) data transfer control with data buffer for intermediate storage.
- Multi-sector data transfers overlapping track and cylinder boundries.
- ESDI, serial mode sector mark format, control dialog with serial to parallel and parallel to serial data conversion and associated error detection and correction.
- Self-diagnostic, QLT, functions with an LED go/no-go indicator.
- Media defect handling using the prerecorded error logs on each surface sector zero of the maximum cylinder (maximum cylinder minus eight redundant error log is ignored) and a new error log recorded on the surface zero sector one of the maximum cylinder; this cylinder is also used for reallocated error sectors starting with surface zero, sector two, then

proceeding to other surfaces in a normal sequential manner skipping over sector zero on each surface.

o Adapter Interface for up to two additional channels.



d = Data Cables
c = Control Cables
t = Terminators

Figure 2-1 ESDIC Subsystem

2.2.2 Wren II Disk Drive

The Wren II is a small, random access, rotating 5 1/4" disk, mass memory device with rigid disk media storage and serial mode standard Enhanced Small Device Interface. Components of the Wren II are: a base casting, direct coupled DC brushless spindle drive motor with digital speed control, brake, the Head/Disk Assembly (HDA) with thin film heads,logic package with read/write (phase locked data separation and NRZ to MFM code conversion), fault detection, transmitter/receiver and microprocessor controlled servo electronics. The HDA is an environmentally sealed unit containing the disks, heads, actuator, DC motor and a non-replaceable absolute air filter. A dedicated head landing zone at the innermost radius of the media is used to eliminate the possibility of destroying or degrading data. An automatic shipping lock prevents transit damage to the actuator; it releases when power is applied to the device.

Wren II configurations:

- o Model number 94156-48, serial mode ESDI operation, is 37,824,540 Bytes formatted (48,285,000 Bytes unformatted) and 5 MHz data rate.
  - 3 disks per drive; 5 data surfaces plus 1 servo surface
- o Model number 94156-86, serial mode ESDI operation, is 68,198,400 Bytes formatted (86,913,000 Bytes unformatted) and 5 MHz data rate.
  - 5 disks per drive; 9 data surfaces plus 1 servo surface

Each Wren II interfaces with the ESDIC via two cables: one radial to each drive B (data) and one daisy-chainable A (command) cable arranged on the PWA as a radial cable to each device; external termination is required on both devices; terminator is supplied with each device.

Power Requirements.

Each Wren II drive requires +5v. dc. and +12v. dc. power, reference section 6.3.

2.2.3 Wren III Disk Drive

The Wren III is a small, random access, rotating 5 1/4" disk, mass memory device with rigid disk media storage and serial mode standard Enhanced Small Device Interface. Components of the Wren III are: a base casting, direct coupled DC brushless spindle drive motor with digital speed control, brake, the Head/Disk Assembly (HDA) with thin film heads,logic package with read/write (phase locked data separation and NRZ to 2,7 code conversion), fault detection, transmitter/receiver and microprocessor controlled servo electronics. The HDA is an environmentally sealed unit containing the disks, heads, actuator, DC motor and a non-replaceable absolute air filter. A dedicated head landing zone at the innermost radius of the media is used to eliminate the possibility of destroying or degrading data. An automatic shipping lock prevents transit damage to the actuator; it releases when power is applied to the device.

Wren III configuration:

- o Model number 94166-182, serial mode ESDI operation, is 142,589,952 Bytes formatted (182,094,480 Bytes unformatted) and 10 MHz data rate.

  - 5 disks per drive; 9 data surfaces plus 1 servo surface

Each Wren III interfaces with the ESDIC via two cables: one radial to each drive B (data) and one daisy-chainable A (command) cable arranged on the PWA as a radial cable to each device; external termination is required on both devices; terminator is supplied with each device.

Power Requirements.

Each Wren III drive requires +5v. dc. and +12v. dc. power, reference section 6.3.

2.2.4 Diskette Adapter, QDM

The Quarter Daughter Board Diskette Adapter (QDM), reference EPS #60149612, provides an interface to the 5 1/4 inch minidiskette. The ESDIC emulates the MDC III (BDC8) firmware in controlling one minidiskette device attached to the QDM. Adapter functions are as follows:

- o Performs device interface dialog control.
- o Data recovery and transmission.
- o Address Mark generation and detection.
- o Control of Seek and Seek overlap; multi-sector data transfers overlapping track and cylinder boundries.
- o CRC generation and verification.
- o Device status monitoring.

Minidiskette Power.

Minidiskette device requires +5v. dc. and +12v. dc. power.

2.2.5 Larkette Streamer Adapter.

The Larkette Streamer Adapter (LSA) quarter-sized daughter board is a microprogrammed peripheral control unit that can interface with one Tape Cartridge Device (TCD) cabled via a connector mounted on the LSA printed circuit board (Reference EPS #60149781). On one side, the LSA, provides an interface to the common MDC-4 internal bus and on the other it controls access to the TCD. The LSA contains the following functionality:

- o Device interface dialog control

- Device read/write data buffers control; one 16 K byte buffer on the adapter and one 32 byte FIFO buffer on the ESDIC.

- LSA to ESDIC and MDC-4 interface control

TCD Power.

The TCD requires DC power from the system power supply. Frame ground and signal grounds are isolated in the TCD and are brought out separately to an external, system level, tie point. The TCD requires +5v. dc., +12v. dc. and -12v. dc. power.

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3 FUNCTIONAL REQUIREMENTS

3.1 Configuration and Simultaneity

Devices attached to the ESDIC are software addressable via channel numbers. Each individual device has two channel numbers assigned, differing from each other only in the low order bit value (the direction bit). When an IOLD instruction is issued to the ESDIC, the direction bit of the output address channel number specifies whether it is going to be an input or an output data transfer; for all other commands, the direction bit is ignored. Bits 8 through 13 (reference figure 3-1) are assigned at system installation and must conform to constraints defined in the Megabus EPS. Software visibility of the devices attached to the ESDIC is such that the devices are independent of each other; except that initiation of a command sequence addressed to one device may be stalled while the ESDIC is busy servicing another device.

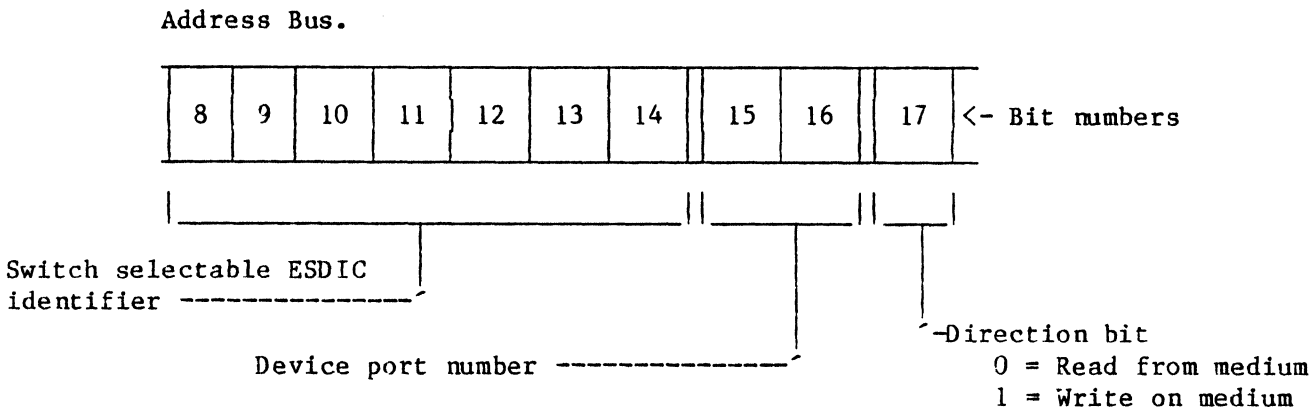
The ESDIC provides a single level of simultaneity (only one data transfer can be active in the subsystem) and supports the following:

- A not busy channel must accept instructions directed to it over the Megabus even though a data transfer may be active over another channel. An instruction may be "waited" for a period not exceeding 12 microseconds; longer delays can affect performance.
- Any seek orders received during a data transfer must be initiated prior to the start of any another data transfer.
- Channels are serviced on an alternating priority basis so that no channel can dominate controller usage.
- Controller accepts a data read/write command to channel B while channel A is in the process of moving data but does not initiate a data transfer on B until A's data transfer is complete. If the ESDIC is configured with less then four devices, it responds to channel numbers associated with the installed devices only.

3.2 Megabus Control

3.2.1 Command Transfer

The ESDIC recognizes a command transfer request on the Megabus when a valid channel number is decoded in bits 8 through 17 of the address bus. If the addressed channel is not busy, the contents of the data and address buses are stored in the



Device assignments:

ESDI #0	= Channel	n
ESDI #1	= "	n + 080
Streamer Tape	= "	n + 100
Diskette Adapter	= "	n + 180

Figure 3-1 Channel Numbers.

ESDIC interface hardware and the ESDIC issues an ACK to the CPU to complete the bus cycle; now the ESDIC can process the information contained in the registers. If the addressed channel is busy executing a previously received command, the ESDIC completes the bus cycle by issuing a NAK (except for the Output Control Word command; reference section 5.). If, however, the ESDIC is temporarily busy, processing a not interruptible function, it completes the bus cycle with a WAIT response which must be followed by either an ACK or a NAK response when the function in process terminates. WAIT response must be as short as possible ($\leq$ 12us.) to avoid performance degradation and if too long system hardware or software timeout may occur (1ms on 6/9X CPU's).

3.2.2 Data Transfer

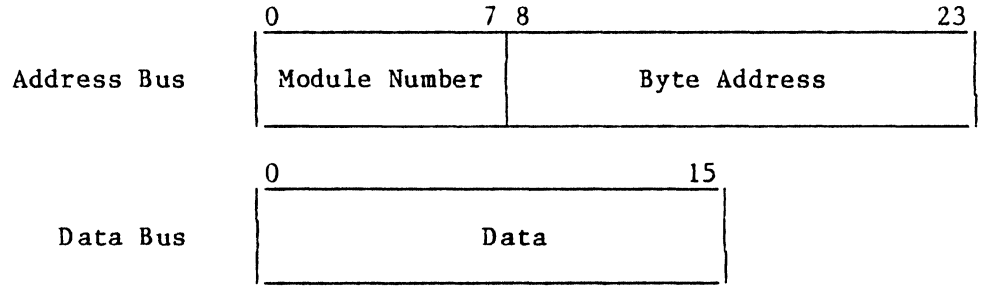
All data transfers associated with the ESDIC are executed in Direct Memory Access (DMA) mode; transfers are normally word wide but byte wide operation may occur on the first and/or last memory cycle of a particular data transfer if the memory buffer begins or ends on an odd byte boundary.

If, during memory read/write request cycle on the Megabus, a NAK response is received at the ESDIC, data transfer continues to its normal termination with a nonexistent resource error posted in Status Word 1 (reference section 5.). A WAIT response to a memory read/write request cycle results in the ESDIC retry of the Megabus request cycle; retries continue until an ACK or a NAK response is received. While either this Megabus cycle or the second half read cycle is pending in the ESDIC interface it is not accessible to the CPU including the Output Control Word command. Once the ESDIC is conditioned to do a memory access all other Megabus cycles addressed to the ESDIC are completed with either a NAK or a WAIT until the memory reference is terminated.

Memory read and write data accesses are illustrated in figure 3-2. During the memory read request cycles, bits 10 through 15 of the data bus may contain an address of a register in the ESDIC into which the returned memory data is delivered. Memory responds in the second half of the read cycle by placing on the address bus, bits 8 through 23, the contents of the entire data bus as received, by the memory, during the request cycle.

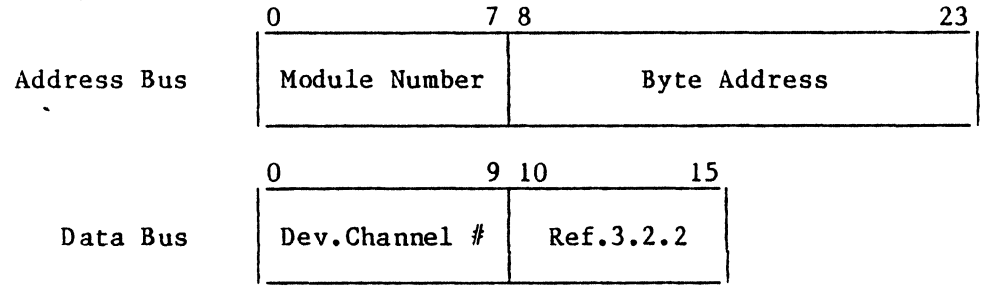
ESDIC Memory Write Request.

Request Cycle.



ESDIC Memory Read Request.

Request Cycle.



Response Cycle.

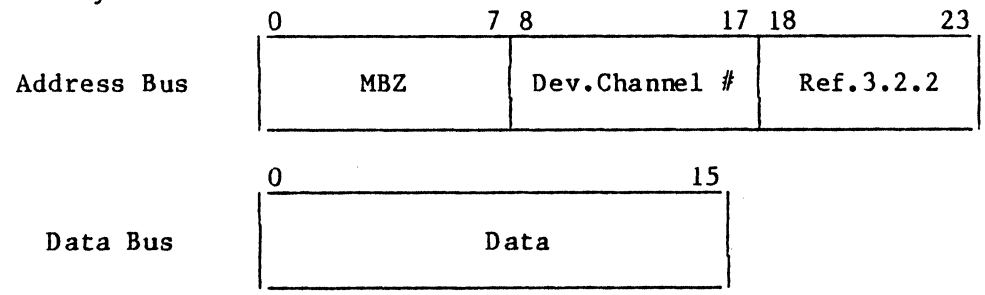


Figure 3-2 Address and Data Bus Configuration for Read and Write Memory Access

3.2.3 Interrupts

Whenever the channel interrupt level is not zero, either an operation initiated by an Output Task Word or an Output Control Word command is completed or the attention bit in the Status Word 1 is set, an interrupt on the Megabus is attempted. If a NAK response is received to an interrupt request, the ESDIC saves the interrupt status until it detects the BSRINT pulse on the Megabus; interrupt is then retried. When an interrupt is saved the channel with the pending interrupt is busy and does not accept commands (except Output Control Word), however, other channels on the ESDIC are free to function normally.

Channel zero interrupt level (initialized or set to zero) inhibits Megabus interrupts for that channel. If a condition or an event occurs which would normally cause an interrupt, the appropriate bits in a status word are set but no interrupt is attempted on the Megabus nor is the interrupt request saved; specifically, interrupts that would be generated as a result of either Output Control Word Initialize or Master Clear.

Address and data bus configuration for interrupt sequences is illustrated in Figure 3-3. The channel number supplied on the data bus during an interrupt is the one used in the most recent Output Address instruction to the ESDIC; if the instruction has not been received the low order bit of the channel number is zero.

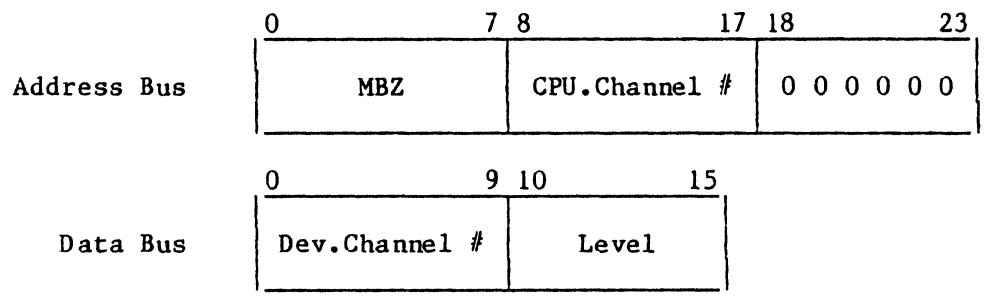


Figure 3-3 Address and Data Bus Configuration for Interrupt Sequences

3.3 Overview of ESDIC Access

Associated with each channel is a set of registers which are loaded by software and specify parameters required for attached device operation. In addition to the range and the address registers, used for DMA operation, there are configuration registers which contain record location and identification information and a task register for command codes. To perform a specific operation software first loads the address, range and configuration registers. The task register is loaded last with a command to be performed which also triggers the ESDIC channel operation. Commands addressed to a not busy channel are always accepted, but execution may be delayed because another channel is in the process of data transfer. All commands addressed

to a busy channel are rejected (NAK response) except Output Control Word, reference section 5.

3.4 Memory Addressability

The Megabus interface is 16 bits wide for the data path and 24 bits wide for the address path with provision for the third rail and its impedance matching components. Memory burst mode of operation is not included in the ESDIC design.

3.5 Scatter/Gather

The Scatter/Gather DMA data transfer is not supported by the ESDIC in either hardware or firmware.

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4 INTERFACES

4.1 User Interface

No specific user action is required to load or initialize the ESDIC other than during subsystem installation and subsystem configuration identification. Actions required to load/unload removable media devices (minidiskette or tape cartridge) are described in an appropriate EPS; see references in 1.3.1.

4.2 External Interfaces

4.2.1 ESDIC to Megabus Interface

The ESDIC attaches to the Megabus as a standard DPS-6 (see Megabus EPS) controller with provision for the third rail impedance matching.

4.2.2 Device Level Interface (DLI)

Refer to the Winchester Disk Device (WDD) specification for information more detailed than that presented in this section which is concerned with the physical interface only. The WDD specification (see references in 1.3.1) also represents the governing document for the device functionality.

The (WDD) requires two cables for attachment to the ESDIC. The daisy chain "A" cable is arranged on the PWA to provide radial connection to each of the two WDD´s) together with the radial "B" cable. Figure 4-1 shows signals present on each cable.

NOTE

For more detailed general ESDI information reference the CDC specification #77738076 Rev. D.

4.2.2.1 Drive Select

Three Drive Select lines are used to send information to all connected drives on the "A" cable; only the selected drive responds to the encoded information with Drive Selected true; decode 000 is a no select. All input control lines are decoded with the Drive Select lines at an appropriate active channel. This implementation of the ESDIC design requires that drive select jumpers 1 thru 7 be configured for drive 1 only.

ESDIC	CONTROL - "A" CABLE	DRIVE SIG	DRIVE GND
	-- Head Select 2^3 * ---------->	2	1
	-- Head Select 2^2 * ---------->	4	3
	-- Write Gate * ---------->	6	5
	<- Configuration/Status Data ----------	8	7
	<- Transfer ACKnowledge ----------	10	9
	<- Attention ----------	12	11
	-- Head Select 2^0 (LSB) * ---------->	14	13
	<- Sector/Byte Clock/Add. Mark Found --	16	15
	-- Head Select 2^1 * ---------->	18	17
	<- Index ----------	20	19
	<- Ready ----------	22	21
	-- Transfer REQuest * ---------->	24	23
	-- Drive Select 1 ---------->	26	25
	-- Drive Select 2 ---------->	28	27
	-- Drive Select 3 ---------->	30	29
	-- Read Gate * ---------->	32	31
A CONNECTOR	-- Command Data * ---------->	34	33
		CONNECTOR	

DATA - "B" CABLE

		SIG	GND
	<- Drive Selected ----------	1	
	<- Sector/Byte Clock/Add. Mark Found --	2	
	<- Command Complete ----------	3	
	-- Address Mark Enable ---------->	4	
	<- Reserved for Step Mode ** ----------	5	
	------- Ground ----------		6
	-- + Write Clock ---------->	7	
	-- - Write Clock---------->	8	
	<- Reserved for Step Mode ** ----------	9	
	<- + Read/Reference Clock ----------	10	
	<- - Read/Reference Clock ----------	11	
	------- Ground ----------		12
	-- + NRZ Write Data ---------->	13	
	-- - NRZ Write Data ---------->	14	
	------- Ground ----------		15
	------- Ground ----------		16
	<- + NRZ Read Data ----------	17	
	<- - NRZ Read Data ----------	18	
	------- Ground ----------		19
B CONNECTOR	<- Index ----------	20	
		CONNECTOR	

* Gated by decoded Drive Select
** Must be at logical zero level

Note: 1. All unmarked signals are negative true.
2. Termination resistors are located in both drives.

Figure 4-1 "A" & "B" Interface Cables

4.2.2.2 Head Select 2^0, 2^1, 2^2 and 2^3

The four lines allow selection of each individual read or write head in a binary coded sequence with Head Select 2^0 being the least significant bit line. Heads are numbered 0 through 15; when all Head Select lines are high (not true) head 0 is selected. More than 16 heads can be addressed by using the Select Head Group command (0100, not implemented). Addressing more heads than contained in the drive results in a write fault when attempting to perform a write operation.

4.2.2.3 Write Gate

This line , when true, enables Write Data to be written on the disk. When formatting, the line should be deactivated for a minimum of 2 bit times between the address area and the data area to identify to the drive the beginning of the PLO synchronization field.

4.2.2.4 Read Gate

This line, when true, enables the Read Date to be read from the disk. The line should become active only during a PLO synchronization field and at least the number of bytes defined by the drive prior to the ID or Data Sync. Bytes. The PLO synchronization field length is determined by the response to the Request PLO Sync. Field Length command. Read Gate must be false when passing over a write splice area.

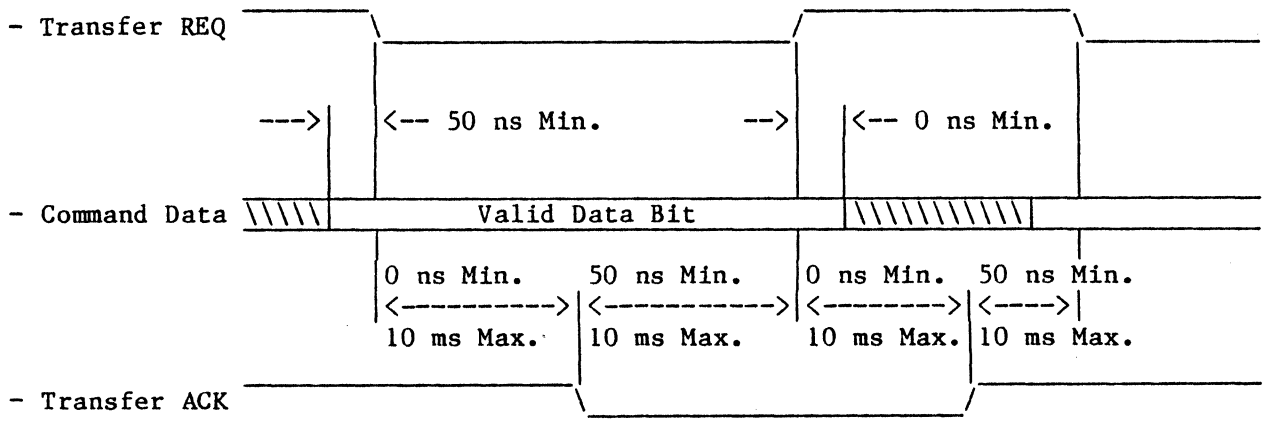


Figure 4-2 Command Data - Bit Timing

4.2.2.5 Command Data

When presenting a command two words of 16 bits of serial data, plus odd parity, are sent on this line controlled by the handshake protocol (reference Figure 4-2) with Transfer REQ and Transfer ACK signals. Data is transmitted most significant bit first and on receipt of the last command word the drive performs the required task as specified in Table 4-1. No other tasks should be attempted unless the Command Complete line is true.

Most Significant Bit															Least Significant Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	P
CMD Function				CMD Modifier				All Zeros								P
CMD Function				Command (CMD) Parameter												P

Odd parity bit = P

Command (CMD) Function Bit 15 14 13 12	Command Function Definition	Command Modifier Bits 11-8	Command Parameter Bits 11-0	Data to ESDIC
0 0 0 0	Seek	No	Yes	No
0 0 0 1	Recalibrate	No	No	No
0 0 1 0	Request Status	Yes	No	Yes
0 0 1 1	Request Configuration	Yes	No	Yes
0 1 0 0	RFU			
0 1 0 1	Control	Yes	No	No
0 1 1 0	Data Strobe Offset	Yes	No	No
0 1 1 1	Track Offset	Yes	No	No
1 0 0 0	Initiate Diagnostics	No	No	No
1 0 0 1	Set Bytes Per Sector	No	Yes	No
1 0 1 0	RFU			
Through	RFU			
1 1 1 1	RFU			

Notes: 1. All unused bits must be zero.
2. All RFU commands are invalid.
3. Simultaneous Data Strobe and Track Offset are allowed by multiple commands.

Table 4-1 Command Data Definition

4.2.2.5.1 Seek (0000)

This Command causes the drive to seek to the cylinder specified in bits 11 through 0. The Seek command restores Data Strobe and Track Offset to zero.

4.2.2.5.2 Recalibrate (0001)

When this command is true, the actuator is returned to cylinder 0000 in 500 milliseconds maximum; Data Strobe and Track Offset are returned to zero.

4.2.2.5.3 Request Status (0010)

This command causes the drive to send 16 bits of standard or vendor unique status information to the ESDI Controller as determined by the command modifier bits. The ESDIC need only request standard status in response to the Attention line set true.

When the Command Modifier bits 11-8 are 0000 the drive responds with 16 bits of the Standard Status; bits 15-12 are state bits which do not cause the Attention line to be set and bits 11-0 are state change bits which cause the Attention line to be set each time one is set.

When the command modifier bits are 0001 through 1111 and bit 2 of the Standard Status is set the drive makes available 15 Vendor unique status words addressed one word at a time. This status is intended for detailed device analysis to be used by repair personnel only. These Vendor unique status words should be read and printed out after at least three sequences of attempting to send the original command and reset Standard Status Control command; if all attempts fail the device is then inoperative.

Standard Status bits are defined as:

15	----------	RFU, set to 0.
14	----------	RFU, set to 1.
13	through 10	RFU, set to 0.
9	----------	Spindle motor stopped
8	----------	Power On reset conditions exist
7	----------	Command data parity error
6	----------	Interface fault
5	----------	Invalid or not implemented command fault
4	----------	Seek fault
3	----------	Write Gate with Track Offset fault
2	----------	Vendor unique status available
1	----------	Write fault
0	----------	RFU, set to 0.

- **Bit 9 - Spindle motor stopped**

  This bit is activated when the spindle motor is stopped.

- **Bit 8 - Power On reset condition exists**

  This bit is activated after a Power On Reset occurs or when an internal drive fault condition exists which would cause a Power On Reset to occur; the drive must be reinitialized by the ESDIC to a desired state.

- **Bit 7 - Command data parity fault**

  This bit is set when a parity error is detected on the serial Command Data line from the ESDIC; the command is not executed. The ESDIC then sends the reset Standard Status control command and if not successful should retry the sequence at least three times of attempting to send the original command and reset Standard Status Control command; if all attempts fail the device is then inoperative.

- **Bit 6 - Interface fault**

  This bit is activated when the interface protocol is violated; e.g. when the drive detects 10 ms. timeout.

- **Bit 5 - Invalid or not implemented command fault**

  This bit is set when one of the following conditions is detected by the drive:

  - An RFU or invalid command function is received.
  - A command function plus an RFU or invalid command modifier is received.
  - A valid but not implemented by the drive, command is received.
  - A valid command function with an invalid parameter is received.

- **Bit 4 - Seek fault**

  This bit is activated when the drive detects a problem with its actuator electronics or mechanism. It is also set when the drive is unable to maintain the Read/Write heads within the recording zone of the medium.

  If the seek fault bit is set the ESDIC should attempt to reset the Standard Status, send the Recalibrate command and reissue the Seek command a minimum of three times prior to defining the drive as inoperable.

- **Bit 3 - Write Gate with Track Offset fault**

  This bit is set when the drive actuator is offset from the normal On Cylinder location and the ESDIC activates the Write Gate signal. Writing to the drive medium is inhibited. When this bit is active the ESDIC should return the actuator to zero offset, reset the Standard Status and then reattempt the write function again.

- **Bit 2 - Vendor unique status available**

  This bit indicates that additional status is available in the Vendor Unique Status words.

o **Bit 1 - Write Fault**

This bit, when set, indicates that a write fault condition has occurred in the drive and that further writing is inhibited until the fault is cleared. On detecting a fault the drive immediately activates the Attention line notifying the ESDIC to stop writing and to enable the drive to identify the fault sector. The ESDIC should attempt to reset the write fault condition at least three times prior to defining a drive as inoperative. The following conditions set the write fault:

- Write current in a head without the Write Gate active or no write current with the Write Gate active Drive Selected.
- Write Gate active and multiple heads are selected, no heads selected or heads improperly selected.
- Write Gate active and the head is not On Cylinder.
- Write Gate and Read Gate are both active.

Command Modifier Bits 11 10 9 8	Configuration Response
0 0 0 0	General Configuration of drive and format, Table 4-3
0 0 0 1	Number of cylinders, fixed
0 0 1 0	Number of cylinders, removable (zero if fixed only)
0 0 1 1	Number of heads Bits 15-8: Removable drive heads Bits 7-0: Fixed heads
0 1 0 0	Minimum unformatted bytes per track
0 1 0 1	Unformatted bytes per sector (hard sector only)
0 1 1 0	Sectors per track (hard sector only) Bits 15-8: Spare Bits 7-0: Sectors per track
0 1 1 1	Minimum bytes in ISG field (without speed tolerance Bits 15-8: ISG bytes after index, (12) Bits 7-0: Bytes per ISG, (16)
1 0 0 0	Minimum bytes per PLO sync. field Bits 15-8: Spare Bits 7-0: Bytes per PLO sync. field, (11)
1 0 0 1	Number of words of vendor unique status available Bits 15-8: Spare Bits 7-0: Number of vendor unique status words
1 0 1 0 1 0 1 1 1 1 0 0	Reserved for use by the Wren III and must not be used by the ESDIC
1 1 0 1 1 1 1 0 1 1 1 1	These codes are reserved but if requested no configuration data will be sent with the Attention line and the Invalid Command Standard Status bit active.

Table 4-2 Request Configuration Modifier Bits and Response

4.2.2.5.4 Request Configuration (0011)

This command causes the drive to send 16 bits of configuration data to the ESDIC. The specific configuration requested is defined by the command modifier bits as shown in Table 4-2 with the general configuration of a drive specified in Table 4-3.

Bit Position	Function	Wren II or III
15	Tape Drive	0
14	Format speed tolerance gap required	0
13	Track offset option available	1
12	Data strobe offset option available	1
11	Rotational speed tolerance is > 0.5%	1
10	Transfer rate > 10 MHz	0
9	Transfer rate > 5 MHz ≤ 10 MHz	0 or 1
8	Transfer rate ≤ 5 MHz	1 or 0
7	Removable cartridge drive	0
6	Fixed drive	1
5	Motor control option implemented	0 *
4	Head switch time > 15 us	0
3	RLL encoded (not MFM)	0 or 1
2	Controller soft sectored (ADR mark)	0 *
1	Drive hard sectored (sector pulses)	1 *
0	Controller hard sectored (byte clock)	0 *

* Configuration switch selectable on Wren II

Table 4-3 General Configuration Response Bits

4.2.2.5.5 Control (0101)

This command causes the control operations specified by the command modifier bits 11-8 to be performed as shown below:

- Command modifier bits = 0000

  This command must be sent to reset the interface Attention line and the standard status bits 11-0. This command should not be sent until the ESDIC has read the standard status word to determine what caused the Attention line to be asserted.

- Command modifier bits = 0011.

  This command must be sent by the ESDIC to turn On the spindle motor when the "Motor Control Option Implemented" General Configuration Bit is active; conversely if the option is not present the command is invalid.

- Remaining command modifier codes are RFU and invalid.

4.2.2.5.6 Data strobe offset (0110)

The drive accepts all of the data strobe offset commands (command modifier codes 0000 through 1XXX) but offsets only by a single amount. Reference Table 4-4 and note on the next page (See Note on the next page).

Command Modifier Bits 11	10	9	8	Function
0	0	0	0	Restore offset to 0
0	0	0	1	Restore offset to 0
0	0	1	0	Early offset 1
0	0	1	1	Late offset 1
0	1	0	0	Early offset 2
0	1	0	1	Late offset 2
0	1	1	0	Early offset 3
0	1	1	1	Late offset 3
1	X	X	X	RFU

Table 4-4 Data Strobe Command Modifier Bits

4.2.2.5.7 Track offset (0111)

The drive accepts all of the track offset commands (command modifier codes 0000 through 1XXX) but offsets only by a single amount from nominal. This command may require up to 3 milliseconds for execution (See Note on the next page). Reference Table 4-5.

Command Modifier Bits 11	10	9	8	Function
0	0	0	0	Restore offset to 0
0	0	0	1	Restore offset to 0
0	0	1	0	Positive offset 1
0	0	1	1	Negative offset 1
0	1	0	0	Positive offset 2
0	1	0	1	Negative offset 2
0	1	1	0	Positive offset 3
0	1	1	1	Negative offset 3
1	X	X	X	RFU

Table 4-5 Track Offset Command Modifier Bits

NOTE

Seek or Recalibrate commands restore both of the above offsets to zero. Simultaneous Data Strobe and Track offsets are allowed by use of multiple commands.

4.2.2.5.8 Initiate diagnostics (1000)

This command causes the drive to perform extensive internal diagnostics; Command Complete when true again indicates successful completion of diagnostics. Attention with Command Complete true indicates that a fault has been detected and status should be requested to determine the proper course of action.

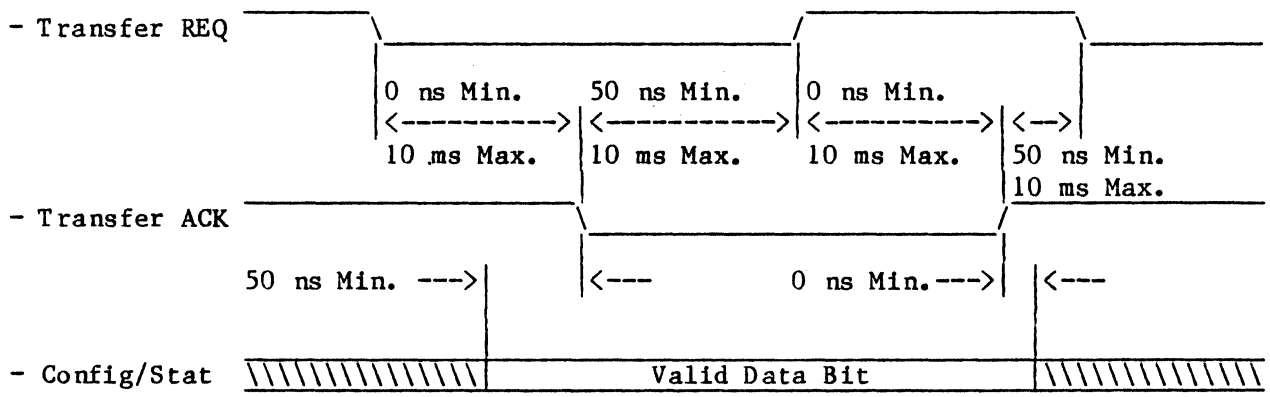


Figure 4-3 Configuration/Status From Drive - Bit Timing

4.2.2.5.9 Set Unformatted bytes per sector (1001)

This command causes the drive to set the number of unformatted bytes per sector specified by bits 11-0. The Maximum value is 4,095 (decimal) with a minimum value of 41 (decimal). This command is valid only if the drive is configured to be in the drive hard sectored mode.

4.2.2.6 Transfer REQuest

This line acts as a handshake signal in conjunction with the Transfer ACKnowledge line during command and configuration/ststus transfers; reference Figures 4-2 and Figure 4-3.

4.2.2.7 Address Mark Enable

This signal line is not used with the hard sectored Wren II drive to write or search for Address Marks. The trailing edge of the Address Mark line with Write Gate true initiates the writing of the header PLO sync. field.

4.2.2.8 Drive Selected

This signal goes active when the drive is selected as described in 4.2.2.1.

4.2.2.9 Ready

This signal indicates that the drive spindle is up to speed and together with Command Complete true is ready to read, write or seek. When this line is false due to a Write Fault or the Attention line is true, the drive is inhibited from all writing and seeking.

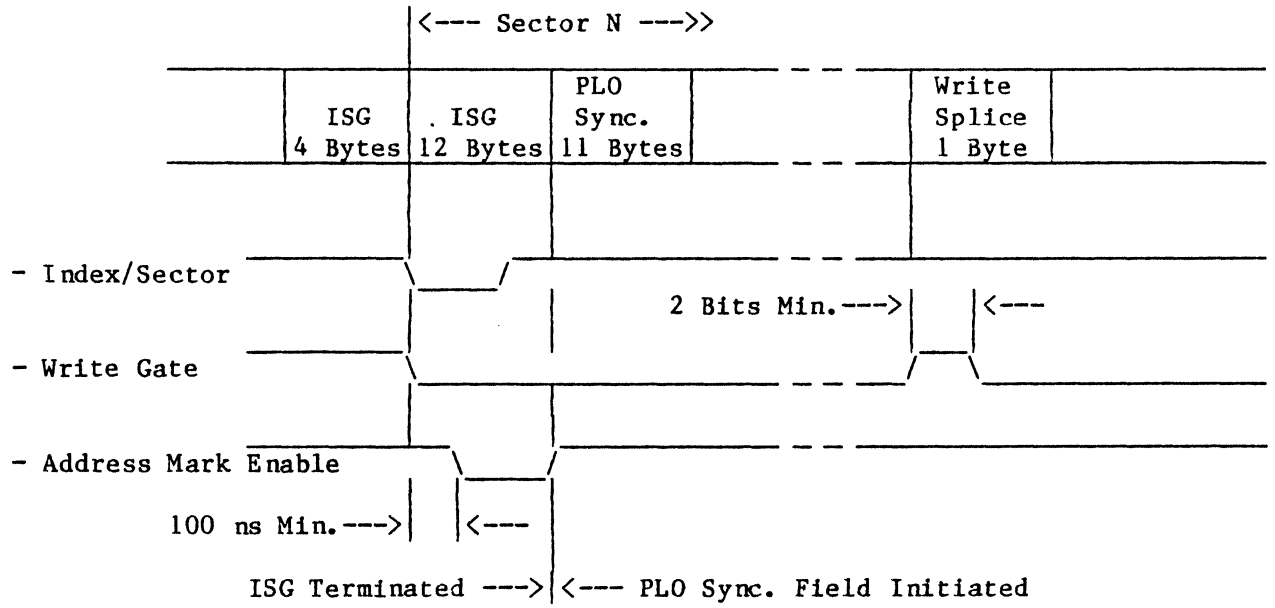


Figure 4-4 Fixed Sector Address Mark, Write Gate & PLO Sync Format Timing

4.2.2.10 Transfer ACKnowledge

This line acts as a handshake signal in conjunction with the Transfer REQuest line during command and configuration/ststus transfers; reference Figure 4-2 and Figure 4-3.

4.2.2.11 Attention

This line is asserted when the drive wants the ESDIC to request its standard status as a result of a fault condition or a change of state of one of the standard status bits 11-0. Writing or seeking is inhibited. Attention is deactivated by the Reset Interface Attention command.

4.2.2.12 Index

This pulse (1.596 us $\pm$ 1%, 8 * the reference clock on Wren II and 1.596 us $\pm$ 1%, 16 * the reference clock on Wren III) is provided by the drive each revolution to indicate the beginning of a track. Only the negative leading edge transition of the pulse is accurately controlled. This signal is available on the command cable (gated) and on the data cable (not gated).

4.2.2.13 Sector/Byte Clock/Address Mark Found

These three signals are mutually exclusive and share this line. Selection is determined by switch settings at the back of the unit (SW5 and SW6 must be in Off positions on the Wren II and SW4 in the Off position on the Wren III to provide sector pulse input. This signal is available on the command cable (gated) and on the data cable (not gated) and has the same timing conditions as the Index pulse.

The Byte Clock signal, on Wren II only, occurs every eight Reference Clock periods and is used by the ESDIC to count the desired number of bytes to determine the sector size and the beginning of a sector location. This signal is continuously transmitted as long as the spindle is up to speed and the heads are positioned over the recording zone of the medium. This clock does not have a fixed phase relationship to the recorded data.

4.2.2.14 Command Complete

This signal is an ungated output from the drive which allows the ESDIC to monitor the drive's Command Complete status, during overlapped commands, without selecting the drive. This signal is deactivated in the following cases:

- o A recalibrate sequence is initiated (by drive logic) at power on, if the R/W heads are not over track zero.
- o Upon receipt of the first Command Data bit. The Command Complete stays false during the entire command sequence.
- o Within 15 us. from the head select change if head selection line is >15 us as indicated in Configuration Data.

4.2.2.15 NRZ Write Data

This is a differential pair that defines the data to be written on a track and clocked by the Write Clock signal. For timing relationships reference Figure 4-5 and for sector format reference Figure 4-5.

4.2.2.16 NRZ Read Data

This is a differential pair that defines the data recovered from the medium by reading previously written information; the read data is clocked by the Read Clock signal. These lines are held at zero level until PLO sync. has been established and data is valid. For timing relationships reference Figure 4-5.

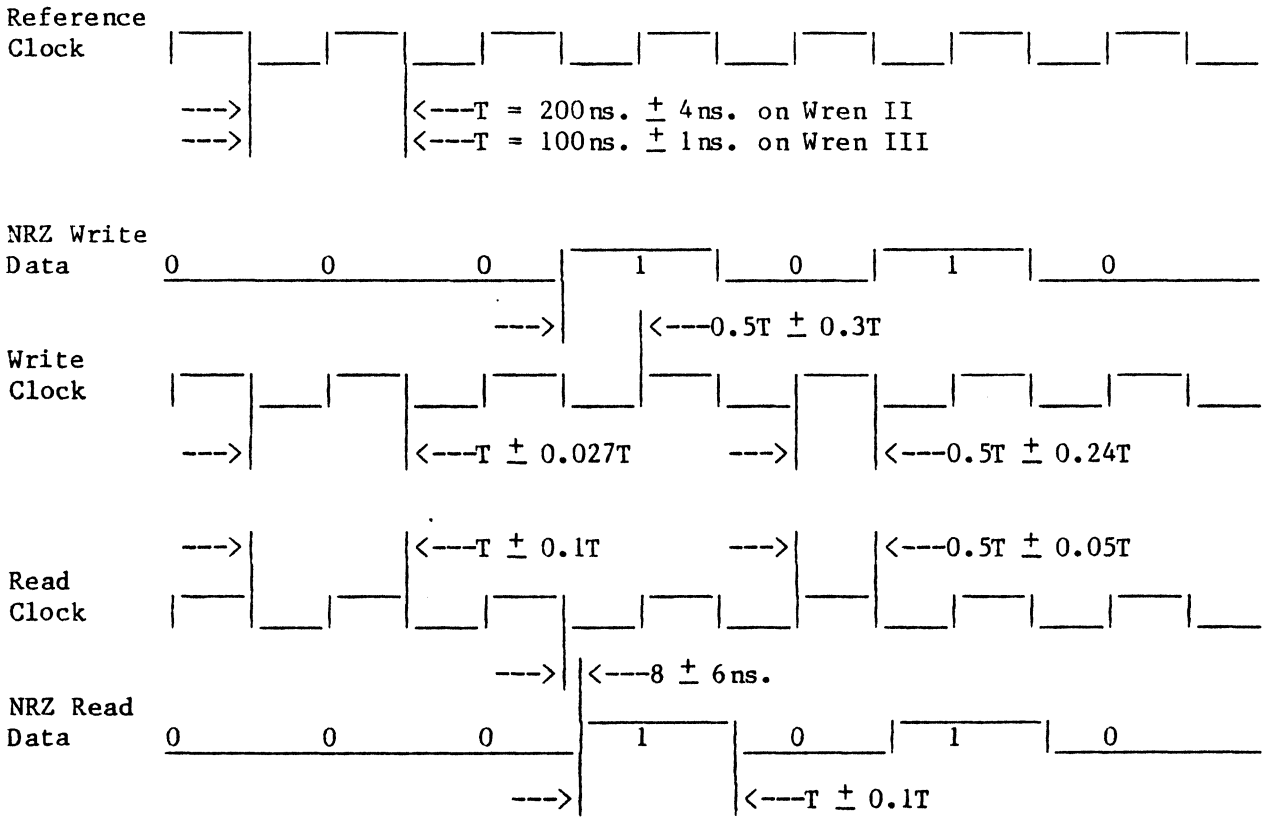


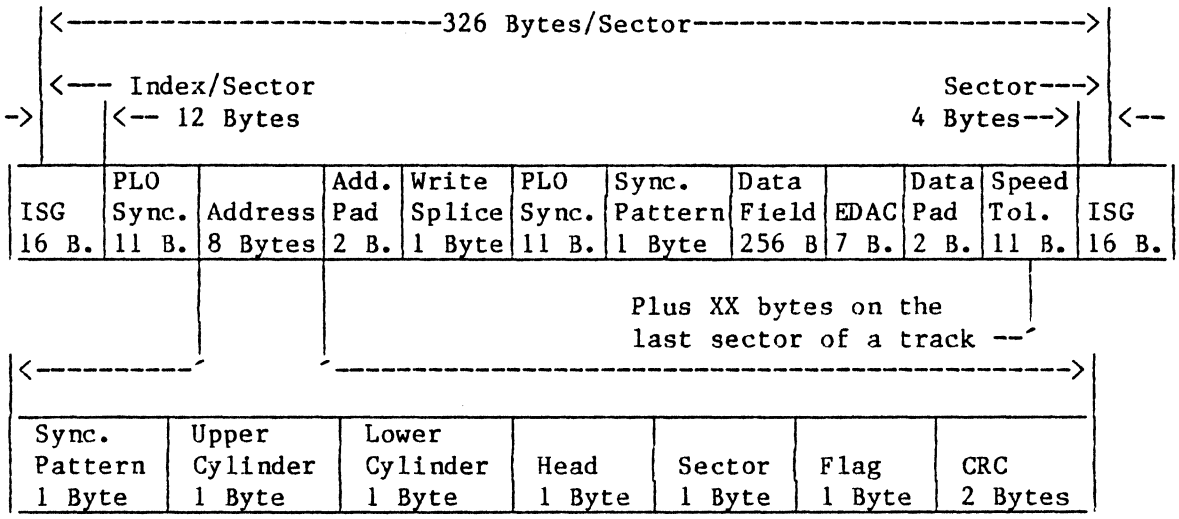
Figure 4-5 NRZ Read/Write Data Timing

4.2.2.17 Read/Reference Clock

The timing diagram in Figure 4-5 illustrates the necessary sequence of events and associated timing restrictions for proper read/write operation of a drive. The Reference Clock signal from a drive determines the read data transfer rate. Transitions from Reference Clock to Read Clock are performed without glitches at a nominal rate of 5 MHz ±1.5% on Wren II and 10 MHz ±1.0% on Wren III.

4.2.2.18 Write Clock

Write Clock is provided by the ESDIC at the bit data rate obtained from the Read/Reference Clock during a write operation. This signal need not be continuously supplied by the ESDIC but must be available before the beginning and last for the duration of a write operation.



	Wren II	Wren III
Bytes per track	10,440	20,880
Bytes per sector	256	256
Sectors per track	32	64
XX in bytes	8	16

Efficiency $\frac{256 * 32(*2)}{10,440(*2)} = 78.5\%$

Synchronization Pattern = #FE

Figure 4-6 Wren II & III Fixed Sector Format.

4.2.2.19 Summary of Critical Write/Function Parameters

ESDIC timing variations in the record-update function are allowed if the following drive dependent write (and interrelated read) timing parameters are met:

- **Read to write recovery time**

  Assuming that head selection is stabilized, the time lapse from deactivating Read Gate to activating Write Gate shall be five Reference Clock periods minimum.

- **Write Clock to Write Gate timing**

  Write Clocks must precede Write Gate by a minimum of two and a half Reference Clock periods.

- **Write-driver plus data-encoder turn-on from Write Gate**

  The write-driver plus data-encoder turn-on time (write splice width) is between 3 and 7 Reference Clock periods.

- **Write-driver turn-off from Read Gate**

  To account for data encoding delays, Write Gate must be held On for at least two byte times after the last bit of the information to be recorded.

- **Write to read recovery time**

  The time lapse before Read Gate or Address Mark Enable can be activated after deactivating the Write gate is 10 us.

- **Head switching time**

  Write Gate must be deactivated at least 1 us before a head change; conversely, Write Gate may not be activated until 15 us after after a head change or a Command Complete is true.

- **Reference Clocks valid time**

  The Read/Reference Clock line contains valid Reference Clocks within two Reference Clock periods after deactivation of the Read Gate. Pulse widths are not shortened during the transition time but clock transitions may not occur for up to two Reference Clock periods.

- **Read Clocks valid times**

  The Read/Reference Clock line contains valid Read Clocks within two clock periods after PLO sync. is established. Pulse widths are not shortened during the Reference Clock to Read Clock transition time but missing clocks may occur for up to two clock periods.

- **Write propagation delay**

  Write gate received at the device connector are delayed by the Write Data Encoder by up to eight bit times maximum prior to being recorded on a medium.

4.2.2.20 Drive Configuration Switches

The Wren II is configured by turning on/off switches in SW1 through SW6 on Servo PWA. This implementation of the ESDIC design requires that all of the configuration switches be in the OFF position. Switch position interpretation is shown below:

Wren II only:

Switch #	ON	OFF
SW1-1	Factory Test	Normal.
SW1-2	Motor control implemented *	Motor control not implemented.
SW1-7	Serial Mode	Step Mode

Sectors/Track	Switch # SW1-3	SW1-4
17	On	On
16	Off	On
34	On	Off
32	Off	Off

Format Mode	SW1-5	SW1-6
Address Mark	On	On
Byte Clock	Off	On
Sector Pulse	On	Off
Sector Pulse	Off	Off

Wren III only:

Switch #	ON	OFF
SW1-1	Motor control implemented *	Motor control not implemented.

Sectors/Track	Switch # SW1-2	SW1-3
35	On	On
32	Off	On
70	On	Off
64	Off	Off

Format Mode	SW1-4
Sector Pulse	Off

* If the SW1-2(II)/SW1-1(III) switch is On, a Start Motor command is required from the ESDIC to start the spindle motor after Power On. The drive generates an Attention signal and activates Standard Status bits 8 and 9 signifying "Power On Reset Condition Exists" and "Spindle Motor Stopped". The ESDIC then responds with a command to Reset the Attention line and also the Start Motor command. This procedure is required anytime that the "Power On Reset Condition Exists" status bit is received by the ESDIC if the SW1-2(II)/SW1-1(III) is On.

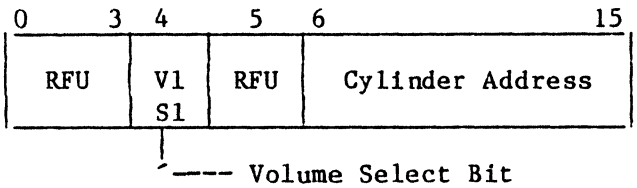
5 INSTRUCTIONS

5.1 General

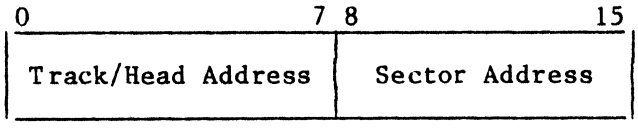
Two configuration words are required to define data access on a disk device. Configuration Words A and B contain the image of the ID field of the sector on which a particular operation is initiated. Data access is defined via four hierarchical elements split between the two Configuration Words. In order to provide for the potential growth of WDD disk type devices, the following guidelines are established for the distribution of the four elements in the two Configuration Words.

- Bits 0 through 5 of Configuration Word A are reserved for use as a magazine address. Magazine selection applies to a device which has more than one physically identifiable media. For example, a cartridge disk device may have a fixed media and a removable media. These bits may also be used to indicate track condition and/or sector size.
- Bits 6 through 15 of Configuration Word A are reserved for use as a cylinder address.
- Bits 0 through 7 of Configuration Word B are reserved for use as a track/head address.
- Bits 8 through 15 of Configuration Word B are reserved for use as a sector address.

Configuration Word A.



Configuration Word B.



In multiple sector data transfer operations (Read or Write), the controller enables an automatic track and cylinder switching function. Track switching occurs whenever the last logical sector on the track has been completed and the range has not expired. Note that track switching is not associated with Index Mark but with equality with the last sector number. When the last track of the cylinder has been completed and track switching is attempted, the ESDIC initiates a seek to the next consecutive cylinder number, selects track number zero, and initiates a search for sector number zero. Note that activities on another channels (including data transfer) may occur during the seek latency period.

Additional considerations are:

- Data transfer continues until the range expires, an error is encountered, an unsuccessful search occurs or the end of the last cylinder is detected (setting bit 5 of the status word).

- Automatic track switching does not occur for any format operation or any unsuccessful search (detection of two Index Marks without a successful compare on both the addressed track and the Error Log cylinder).

- When track completion is detected without an error, the Configuration Words are modified to reflect the next consecutive track and sector zero. In addition, if cylinder completion is also detected, the Configuration Words are modified to reflect the next consecutive cylinder, track and sector zero. Note that this update occurs only if the range is nonzero at the end of the last sector of the previous track.

- An attempt to automatically switch off the last track of the last cylinder results in status bit 5 being set (except in the case where the range has been decremented to Zero).

- Both track and cylinder switching occur within the fixed disk selected by the Configuration Words. A multiple sector operation takes place only within the selected media and does not link to another drive media.

The functionality described above enables software to access records in sequential order without having to reload the sector ID argument for every operation on a particular track. Extended reads or writes operate on sequential records and can therefore be used to advantage on files that are formatted with interleaved sectors.

5.2 Instructions

The DPS-6 instructions supported by the ESDIC are listed in Table 5-1 with detailed instruction description following.

5.2.1 IOLD

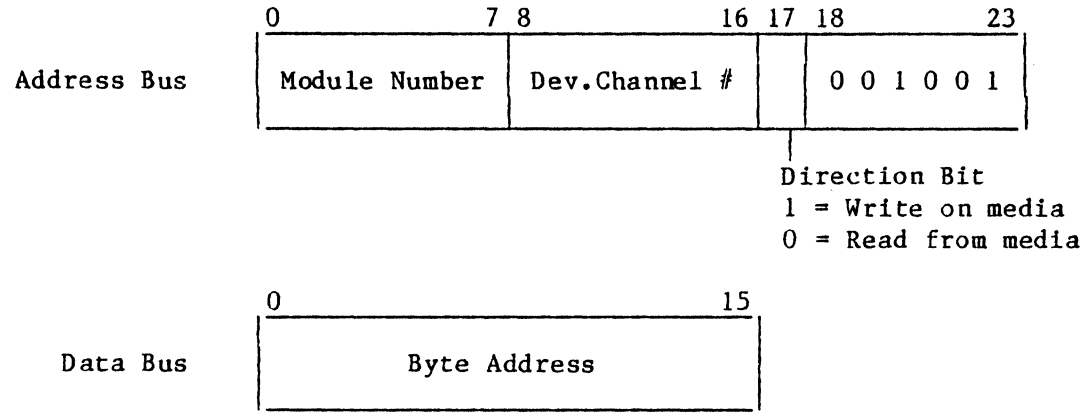
The I/O Load (IOLD) instruction is transformed by the CPU into the Output Address and Output Range instructions on the Megabus. Each IOLD instruction results in an Output Address instruction followed by an Output Range instruction.

Type	Function Code Hex.	Instruction	Ref. Section
	*		
Output		IOLD:	5.2.1
	09	Address	5.2.1.1
	0D	Range	5.2.1.2
	0F	Offset Range (not used)	5.2.2
	11	Configuration Word A	5.2.3
	13	Configuration Word B	5.2.4
	15	Configuration Word C	5.2.5
	03	Interrupt Control	5.2.6
	07	Task Word	5.2.7
	01	Control Word	5.2.8
Input	00	Initial Controller ID	5.2.9
	08	Memory Byte Address	5.2.10
	0A	Memory Module Address/QLTI	5.2.11/20
	0C	Range	5.2.12
	0E	Offset Range (not used)	5.2.13
	10	Configuration Word A	5.2.14
	12	Configuration Word B	5.2.14
	14	Configuration Word C	5.2.14
	02	Interrupt Control	5.2.15
	26	Identification Code	5.2.16
	06	Task Word	5.2.17
	18	Status Word 1	5.2.18
	1A	Status Word 2	5.2.19
	3C	Firmware Revision	5.2.21
	20	Retry Counter	5.2.22
Diag-nostic	Any Even Code	Read ESDIC Registers	5.2.23
	Any Odd Code	Write ESDIC Registers	5.2.23

* All other Function Codes are RFU.

Table 5-1 Instructions

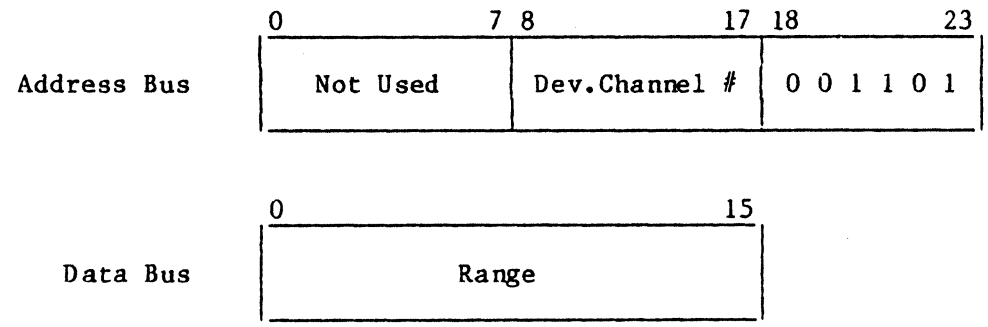
5.2.1.1 Output Address



This instruction loads a 24 bit address into the address register associated with the referenced channel (device). The address refers to the starting (byte) location in the main memory where the ESDIC commences input or output data transfers. Bits 0 through 7 of the address bus (module number) are the most significant bits. Data transfers to or from memory are normally on a word basis, but byte mode transfers can occur associated with the first and/or last memory cycle of a particular data transfer if the main memory buffer (identified by this instruction) begins or ends on an odd byte boundary.

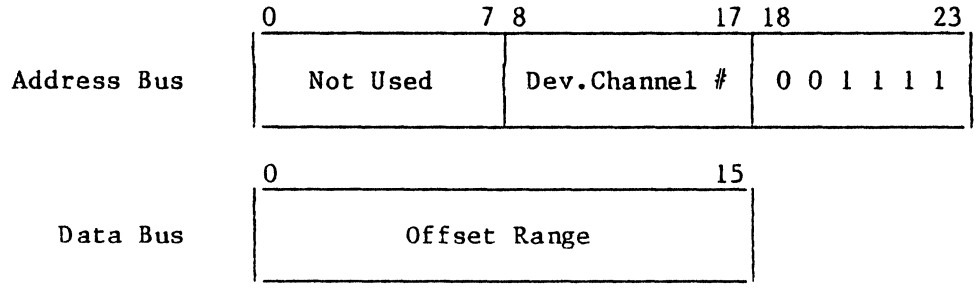
Bit 17 of the address bus (direction bit of the channel number) determines the direction of any subsequent data transfer operation. A logical One specifies an output operation (writing on media) while a logical Zero specifies an input operation (reading from media).

5.2.1.2 Output Range



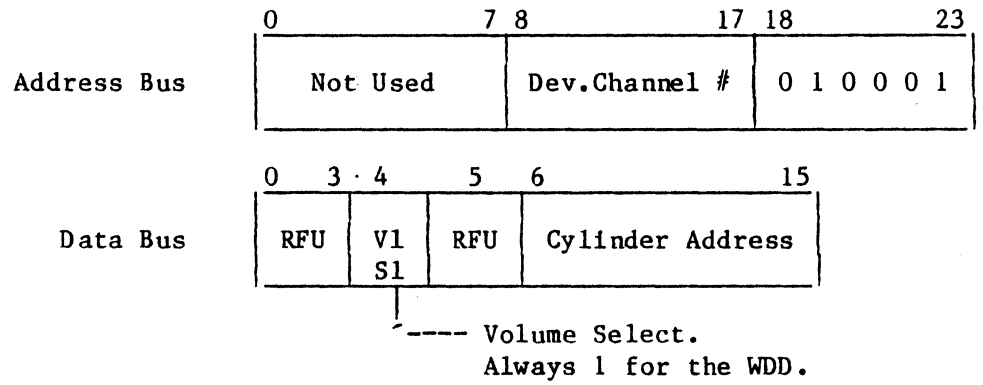
This instruction loads the range register associated with the referenced channel. The (16 bit) quantity loaded (data bus) is the number of bytes to be transferred during the data transfer that is being set up. The number is a positive binary quantity and is decremented by the ESDIC after each memory transfer. A range of zero results in a premature End-of-Operation termination for any Read or Write command that may be subsequently issued (refer to subsections 5.2.7.3 through 5.2.7.9). Any range register residue is applied to the next command unless reset by another IOLD instruction.

5.2.2 Output Offset Range



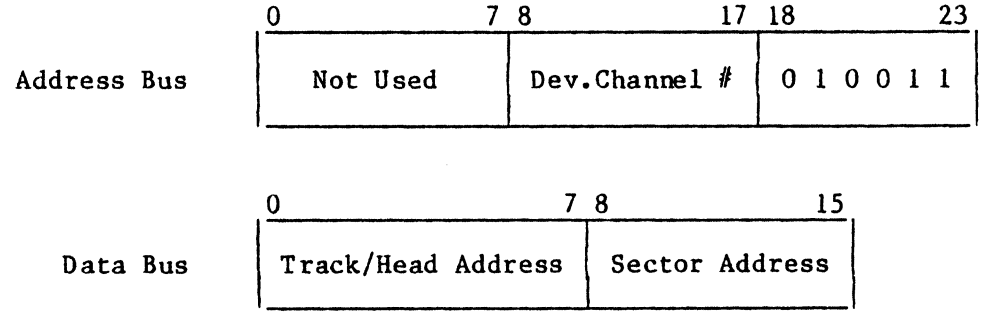
This instruction, implemented partially for compatibility reasons, loads the Offset Range register associated with the referenced channel and no other action takes place, except the normal instruction termination.

5.2.3 Output Configuration Word A



This instruction loads Configuration Word A for the device corresponding to the referenced channel. The cylinder address (bits 6 through 15) is used as the seek argument during Seek operations. The complete word is used as the two high order bytes of a sector ID field to be searched for during a data field Read or Write operation. Bits 0 through 3, and bit 5 are reserved for future use (RFU). The maximum cylinder address permissible is 724 for the WDD. Bit 4, the volume select bit, is defined as: 0 = removable volume, 1 = fixed volume.

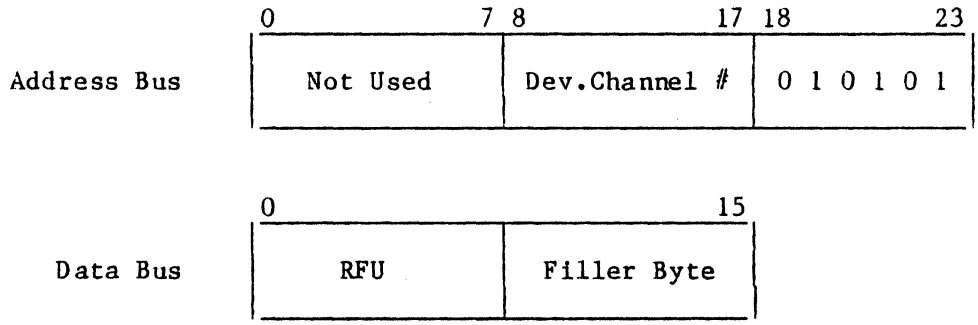
5.2.4 Output Configuration Word B



This instruction loads Configuration Word B for the device corresponding to the referenced channel. This word is used as the low order two bytes of a sector ID field to be searched for during a data field Read or Write operation. Bits 0 through 7 provide the track address for any Read or Write operations: even = upper surface address, odd = lower surface address.

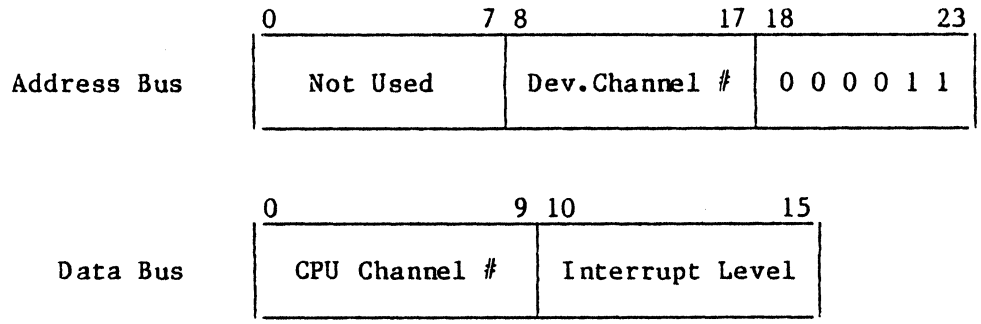
The subsystem treats bits 8 through 15 of Configuration Word B as a sector number. This number is incremented after operating on a data field during a data field Read or Write operation (see subsection 5.2.7).

5.2.5 Output Configuration Word C



This instruction loads Configuration Word C to the referenced channel. The low order byte of Configuration Word C is used for filling the data field during the execution of a Format Write instruction. The filler byte is initialized to 6D.

5.2.6 Output Interrupt Control



This instruction loads, for the referenced channel, the interrupt level and the channel number of the CPU. The interrupt level number is a 6 bit quantity and is positioned on the data bus as illustrated above. Bits 0 through 9 of the data bus contain the CPU channel number to which subsequent interrupts are to be directed.

If an interrupt level of Zero is loaded, the subsystem does not generate or save interrupts for any events that occur while the interrupt level is Zero. The interrupt level is set to Zero whenever the subsystem is initialized.

5.2.7 Output Task Word

	0 — 7	8 — 17	18 — 23
Address Bus	Not Used	Dev.Channel #	0 0 0 1 1 1

Data Bus	0 — 7 Command Code	8	9 — 13	14	15	
	0 0 0 0 0 0 0 0	0	MBZ	0	0	Recalibrate
	0 0 0 0 0 0 0 1	0	"	0	0	Seek
	1 0 A R R 0 0 0	0	"	0	0	Format Write
	1 0 A R R 0 0 1	0	"	C	0	Read/Write Data
	1 0 A R R 0 1 0	0	"	0	0	Diagnostic Format Read/Write
	1 0 A R R 0 1 1	0	"	0	0	Diagnostic Read/Write Data
	1 0 A R R 1 0 0	B	"	0	0	Format Read/Write ID
	1 1 0 0 0 0 0 0	0	"	0	0	Wraparound Read/Write
	1 1 0 0 0 0 1 0	0	"	0	0	Diagnostic Error Log Buffer Read/Write
	1 1 0 1 0 0 0 0	0	"	VUS		Device Status

where:

A = Automatic Seek Bit
B & C = Specific meaning for the command
R = Reserved for Future Use (RFU). These must be "don't care" bits when not implemented.
VUS = Vendor Unique Status bits (bits 12 through 15)
MBZ = Must Be Zero

This instruction outputs a Task Word to the referenced channel. The coding of bits 0 through 7, illustrated above, represents operations that are to be performed (modified by bits defined in 8 through 15). When this instruction is accepted, the channel enters the "busy" state and the indicated task is initiated or stacked. All address, range, and configuration information must be loaded prior to execution of this instruction. The direction of data transfer is indicated in the low order bit of the most recent output address instruction (refer to subsection 5.2.1.1). For example, if the data field encoding of the Task Word is received when a read channel number is indicated, than a Read Data command is executed. Note that track selection is performed for each media data transfer command prior to initiation of the data transfer and is based on the current contents of the Configuration Word B.

Bits 2 through 4 of the command code have specific meaning for all media data transfers as follows:

- Bit 2 - Automatic Seek

  If this bit is logical Zero, the data transfer is initiated based on the current cylinder position of the drive.

  If this bit is a logical One, a Seek Cylinder operation, based on the current contents of Configuration Word A, is initiation to the drive. Another channel may be serviced by the ESDIC during the Seek latency period. At Seek completion, no Seek complete interrupt is generated to the bus channel and the specified data transfer operation is initiated.

- Bits 3 & 4 - Reserved for future use and must be don't care bits in the ESDIC.

5.2.7.1 Recalibrate

The Recalibrate command causes the channel to move the device's positioner to cylinder Zero, select track Zero, and send a Reset Interface Attention and Standard Status bits command to the WDD. This instruction is intended as an Initialization command to guarantee that the position location information in the ESDIC is correct and that all device faults are cleared. Completion of the Return To Zero operation by the device results in an On Cylinder status and Seek End.

5.2.7.2 Seek

The Seek command in the Task Word causes the channel to move the device's positioner to the cylinder indicated in Configuration Word A. If the cylinder specified is greater than the innermost cylinder or an error occurs during positioner movement, than an error bit is set in the Status Word (refer to subsection 5.2.20 or 5.2.21). Completion of a positioning operation (whether or not any physical movement occurred) by the device results in the generation of an interrupt. Note that Seek completion as a result of an automatic Seek (see subsection 5.2.7) does not result in an interrupt.

5.2.7.3 Format Read

This command is redundant and is not implemented. Refer to subsection 5.2.7.4.

5.2.7.4 Format Read ID

The Format Read ID command causes the channel to read all Identifiers (IDs) on a track beginning with the first user sector after index and in the order in which they are recorded. IDs are transferred to memory beginning at the memory location specified in the subsystem's memory address register. This address is the address loaded by the most recent Output Address (IOLD) instruction if no data transfer has occurred since that instruction was executed. If one or more data transfer operations have been executed since the last Output Address IOLD instruction, then the starting memory address used for this operation is the byte address immediately following the end of the most recent data transfer executed for this device (either read or write).

If Bit 8 (B) of the Command code is a One, then the CRC bytes of any sector identifier read are ignored. If bit 8 of the Command code is a Zero, then the CRC bytes of any sector identifier read are checked.

Data is transferred until an uncorrectable read error occurs (except as noted for bit 8), the range is satisfied, or the entire track is read (index is detected).

Normal range for this command, to read one complete track is (R = 4 x 32) 128 bytes for the Wren II and (R = 4 x 64) 256 bytes for the Wren III.

Where: 4 = number of bytes in any ID
32 = number of user sectors per track for the Wren II
64 = number of user sectors per track for the Wren III

If this command is terminated due to end of track before the range is satisfied, the residual range is available via the Input Range command (refer to subsection 5.2.12). An uncorrectable read error in any field (except as previously noted for bit 8 of the Command code = 1) causes the operation to be terminated with the read error bit set in the status word (bit 4). The field in error can be determined through examination of the residual range. If a read error is detected in an ID field the range is decremented for the ID field only.

If the required transfer rate, 625 K Bytes/sec, is not maintained on the Megabus, the operation is terminated and the overrun/underrun bit 2 in Status Word 1 is set.

If the range register is zero when this command is received, the task is immediately terminated. No data is read or transferred. Track selection of the operation is based on the current contents of the track address of Configuration Word B.

5.2.7.5 Format Write

The Format Write command causes the channel to format the track which is positioned under the read/write head specified by Configuration Words A and B when this command is received. 32 equal length sectors(except the 32nd sector which is 8 bytes longer) are written starting at index. The sector ID fields are read from memory, beginning with the memory location specified in the subsystem's memory address register. Bit 8 is Zero for this command.

The data fields are filled by the ESDIC with the 6D filler byte from Configuration Word C.

NOTES

1. Format Write ID and Format Write codes have the same functionality.

2. Read errors can occur on reallocated sectors which were found to contain uncorrectable errors.

3. Error sector reallocation is performed at this time. Identified error sector ID field CRC bytes are written incorrectly, ie, complemented CRC (see subsection 5.3.3.3).

If the required transfer rate, 625 K Bytes/sec, is not maintained on the Megabus, the operation is terminated and the overrun/underrun bit 2 in Status Word 1 is set.

If a range other than 128 is specified, Program Error Bit 5 is set to One in Status Word 1. Innermost cylinder Format Write is described in subsection 5.3.4. If the range register is zero when this command is received, the task is immediately terminated (End-of-Operation) and no data is written.

5.2.7.6 Read Data

The Read Data command causes the channel to locate the sector defined by the sector ID image loaded in Configuration Words A and B and to begin transfer of the data field of (at least) that sector to buffer memory. Data is transferred to the main memory from the ESDIC buffer memory beginning with the memory location specified in the subsystem's memory address register.

When the transfer of the first specified sector data field is completed without error, the sector number field of Configuration Word B is incremented. If the initial range was greater than 256, then the sector on that track represented by the updated contents of Configuration Words A and B is located and data transfer continues with the new sector's data field. This operation continues until either the range is satisfied, an uncorrectable read error occurs, or the record specified by Configuration Words A and B cannot be located on the track or the reallocated track as indicated by the detection of two Index Marks without a successful compare (Reference section 5.3.4). If the specified record cannot be located, an unsuccessful search is posted in the Status Word 1, bit 7. Note that track and cylinder switching may occur as described in subsection 5.1.

Track selection for the operation is based on the current contents of the track address of Configuration Word B. If an uncorrectable read error (Reference section 5.3.2) is found in a data field, the operation is terminated and the read error bit in the Status Word 1, bit 4, is set. The sector number field of Configuration Word B contains the address of the record in error. If a read error is encountered in an ID field (Reference section 5.3.4), a miscompare result is assumed and the search continues. In this case the read error bit is posted in the status word so that, if the desired record is never located, the operation is terminated with both the unsuccessful search bit and read error bit posted in the Status Word 1, indicating that the reason for the miscompare could be a read error in the sector ID. If the search is eventually successful, the read error bit in the status word is reset.

If this command is terminated before the range is satisfied, the residual range is available via the Input Range command (refer to subsection 5.2.12). If the range register is zero when this command is received, the task is immediately terminated (End-of-Operation). No data is read or transferred. If the required transfer rate, 625 K Bytes/sec, is not maintained on the Megabus, the operation is terminated and the overrun/underrun bit 2 in Status Word 1 is set.

NOTE

Bit C (bit 14 of the Task Word), when set, inhibits read retries; conversely, retries are enabled when reset. This bit is intended to be used by diagnostics only for identification of bad spots on the media.

5.2.7.7 Write Data

The Write Data command causes the channel to locate the sector defined by the sector ID image loaded in Configuration Words A and B and to rewrite the data field of at least that sector. The data is read from main memory, beginning with the memory location specified in the subsystem's memory address register into the ESDIC's buffer memory and then the data is written on the disk one sector at a time. Rewritten data fields are preceded by PLO synchronization bytes and data field synchronization byte (see Figure 4-6). When the transfer of a sector is completed, the sector number field of Configuration Word B is incremented.

If the range is less than 256, the remainder of the data field is zero filled. If the range is greater than 256, the sector represented by the updated contents of Configuration Words A and B is located and the data field rewritten. This operation continues until either the range is satisfied or the record specified by Configuration Words A and B cannot be located on the track or the reallocated track, as indicated by the detection of two index marks without a successful ID field compare (Reference section 5.3.4). If the latter event occurs, the unsuccessful search bit is posted in the Status Word 1, bit 7. Note that track and cylinder switching may occur as described in subsection 5.1.

If a read error is encountered in an ID field (Reference section 5.3.4), the ID contents are ignored and the search continues. In this case the read error bit is posted in the Status Word 1 so that, if the desired record is not located, the operation is terminated with both the unsuccessful search bit and the read error bit posted in the Status Word 1, indicating that the reason for the miscompare is a read error in the sector ID. If the search is eventually successful, the read error bit in the status word is reset. If this command is terminated before the range is satisfied, the residual range is available via the Input Range command (refer to subsection 5.2.12). If the range register is zero when this command is received, the task is immediately terminated (End-of-Operation) and no data is written.

If the required transfer rate, 625 K Bytes/sec, is not maintained on the Megabus, the operation is terminated and the overrun/underrun bit 2 in Status Word 1 is set.

5.2.7.8 Diagnostic Write Data

The Diagnostic Write Data command causes the channel to perform as if the Write Data command is specified, except that EDAC characters are written at the end of the data field updated as read from memory (not hardware generated). Only one sector can be updated by this command so that the range must equal 263 (256 + 7) bytes.

Track selection for the operation is based on the current contents of the track address of Configuration Words A and B.

5.2.7.9 Diagnostic Read Data

The Diagnostic Read Data command causes the channel to perform as if the Read Data command is specified, except that the seven byte EDAC field attached to the data field is also transferred to memory (error detection or correction of the data field is not performed). Only one sector can be read by this command so that the range must equal 263 (256 + 7) bytes. Track selection for the operation is based on the current contents of the track address of Configuration Words A and B.

5.2.7.10 Diagnostic Format Write

The Diagnostic Format Write command causes the channel to perform as if the Format Write command is specified, except that invalid CRC characters (true CRC one's complemented) are written at the end of each ID field. Note that the data written in the data field is a pattern of bytes derived from the filler byte of Configuration Word C.

5.2.7.11 Diagnostic Format Read

The Diagnostic Format Read command is not implemented but the same functionality can be obtained by the Format Read ID with bit 8 set (Section 5.2.7.4).

5.2.7.12 Wraparound Read/Write

During the Wraparound Write command, the channel reads 1 to 8 words from memory at the address specified by the subsystems memory address register and transfers these bytes to the ESDIC FIFO buffer.

When a Wraparound Read command is received (immediately following a Wraparound Write), the bytes previously loaded into the specified buffer by the previous Wraparound Write command are returned to the main memory at the address specified in the subsystem's memory address register. The bytes returned during this operation are the same as the bytes supplied by software in the preceding Wraparound Write command. The range supplied for the Wraparound Write must be the same as the range supplied for the Wraparound Read or the results are unpredictable.

A range smaller than or equal to a 16 bytes should be specified for these commands. If a range of zero is specified, the command is immediately terminated (without being executed nor with any status indications). If a range greater than a buffer size is specified, the results are uncertain and the Program Error bit (bit 5) of the Status Word 1 is set and the command is terminated immediately. In any case, the Wraparound Write and its associated Wraparound Read must start and end from the same memory boundary (byte or word).

Execution of a Task instruction on another channel during a Wraparound sequence is unpredictable.

5.2.7.13 Diagnostic Error Log Buffer Read/Write

On initialization, this buffer is filled with error sectors ID's read from the Error Log and New Error Log on the maximum number cylinder sectors 00 (all surfaces) and 01 (surface 0 only) respectively. This Error Log Buffer is used during the Format Write routine in reallocating bad sectors to the maximum number cylinder starting on surface 0 sector 02 and continuing through the rest of the cylinder but skipping over sector 00 on each surface. This diagnostic procedure allows the addition of a temporary error log to the Error Log Buffer without affecting the source of error logs on the maximum cylinder; which results in:

- the temporary sector being reformatted

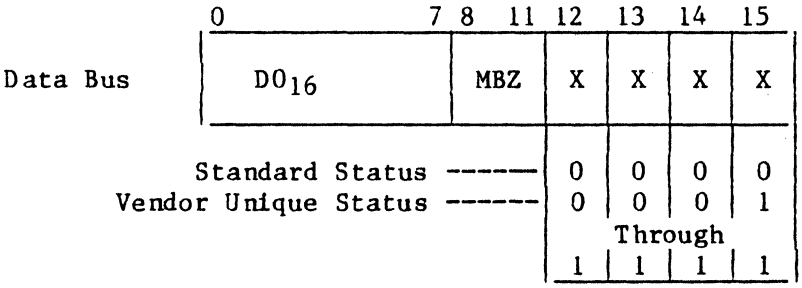
  addition of a complemented CRC to the error sector ID field

o verification that the ID field now contains an error

After the diagnostic procedure is completed, the ESDIC must be returned to its original state by removing all temporary Error Log Buffer entries.

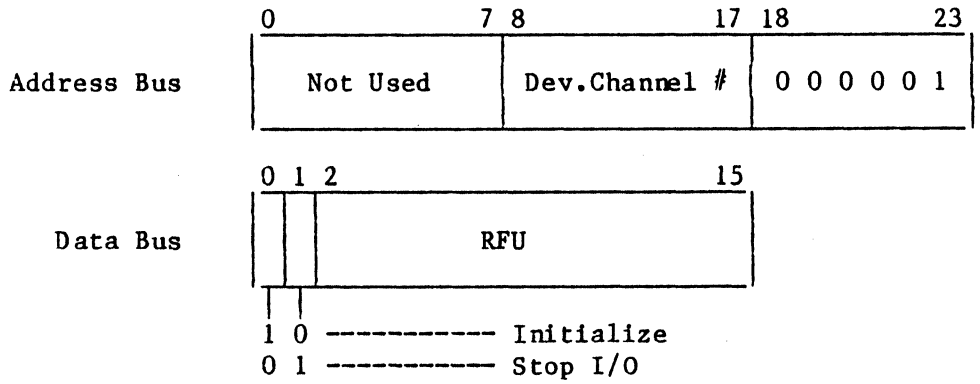
5.2.7.14 Read Device Status

This command provides the capability of inputting the Standard Status and all the Vendor Unique Status words described in section 4.2.2.5.3.. When inputting a status the status word selected by bits 12 through 15 of the data bus in the Task Word is stored in memory location indicated by the last IOLD.



When the command modifier bits are 0001 through 1111 (bits 12 through 15 above) and bit 2 (bit 13 above) of the Standard Status is set the drive makes available 15 Vendor unique status words addressed one word at a time. This status is intended for detailed device analysis to be used by repair personnel only.

5.2.8 Output Control Word



This instruction loads a Control Word into the referenced channel. This command is unconditionally accepted by the channel regardless of its busy status, except as noted in subsection 3.1.2.

5.2.8.1 Initialize.

This command causes the ESDIC to reset to the same state that it enters after power-up. When an Initialize command is received by the ESDIC, all of its channels are initialized (regardless of which channel the command is received over). A Recalibrate is executed on all connected WDD's.

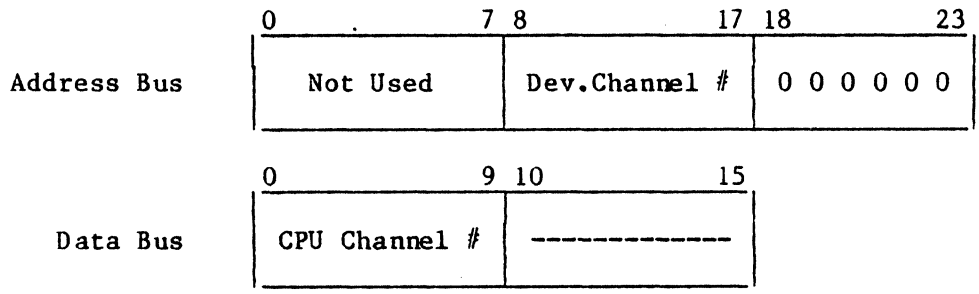
Operations that are in progress in the ESDIC at the time of the initialization are abruptly terminated and all software addressable registers are initialized. No information about the terminated operations are retained and no interrupts for the operation are generated. The interrupt level for all channels is set to zero (interrupts blocked). Note that execution of this command may result in either invalid data on the media (if a Write command is in progress) or a device fault (if a Seek is in progress at a drive).

5.2.8.2 Stop I/O

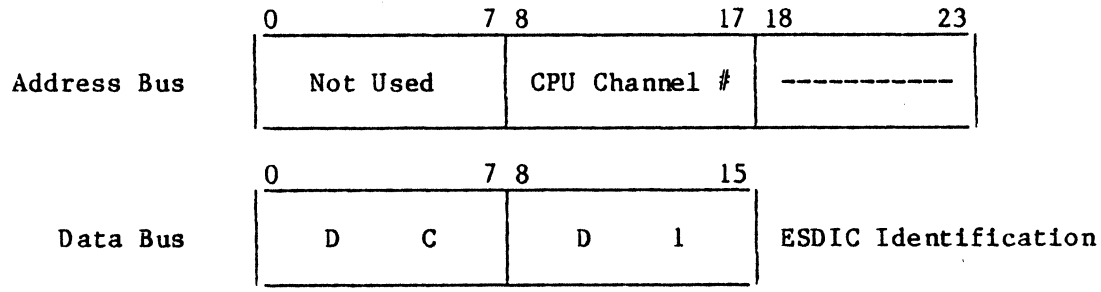
This command causes any operation currently active on the specified channel to be abruptly terminated. If a data transfer operation is in progress, it is not completed and no error checking is done. An interrupt is generated for the operation terminated by this command as if the operation comes to a normal ending point. Status, address and range information, present in the ESDIC when this command is received, is retained. Note that execution of this command may result in invalid data on the media (if a Write operation is in progress) or a device fault (if a Seek operation is initiated and not completed prior to a subsequent operation).

5.2.9 Input Initial Controller ID

Request Cycle



Response Cycle



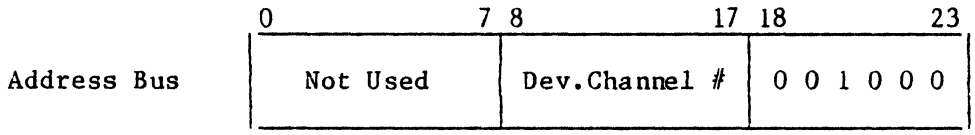
This instruction causes the current contents of the referenced channel's Initial Controller ID to be transferred to the requesting CPU channel.

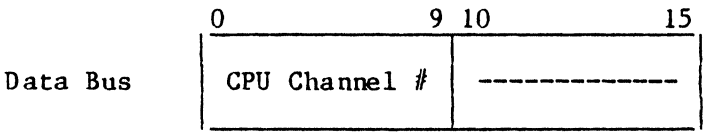
During the response cycle (second half read), the ESDIC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle. The data bus contains the unique numeric (HEX) identifier which is only true after the initialize command or after power-up

procedure; i.e. after QLT's are run. This command is intended to be used by diagnostics for controller or adapter identification.

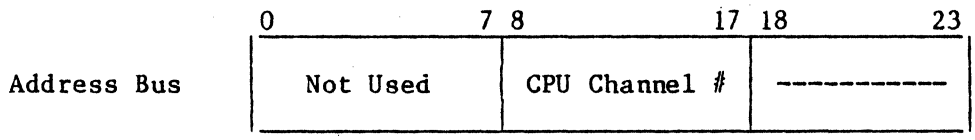
5.2.10 Input Memory Byte Address

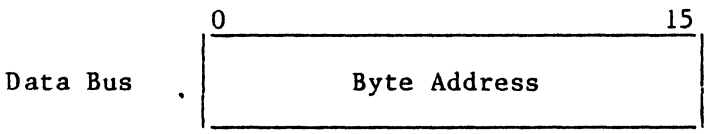
Request Cycle





Response Cycle



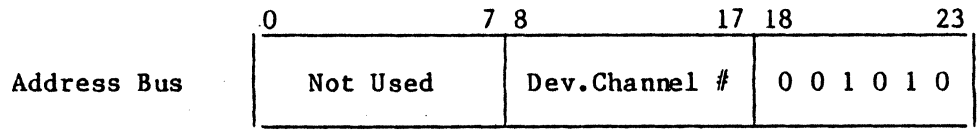


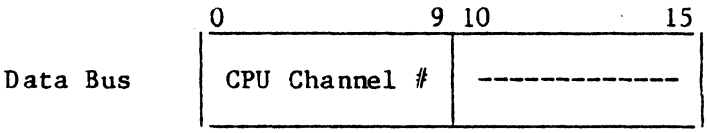
This instruction causes the current contents of the referenced channel's memory byte address to be transferred to the requesting CPU channel. During the response cycle (second half read), the ESDIC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle. The data bus contains the low order 16 bits of the Memory Byte address currently stored for the specified channel in the ESDIC. Note that if a Write command ended at a byte boundary (high order 8 bits of word), the memory address reflects the next word (not the low order 8 bits of the previous word). This command is used for diagnostic purposes only.

5.2.11 Input Memory Module Address

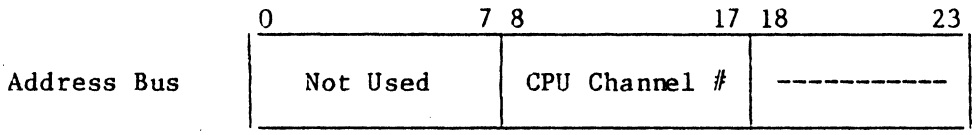
This instruction causes the current contents of the referenced channel's memory module address to be transferred to the requesting CPU channel.

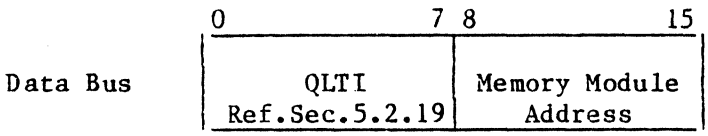
Request Cycle





Response Cycle

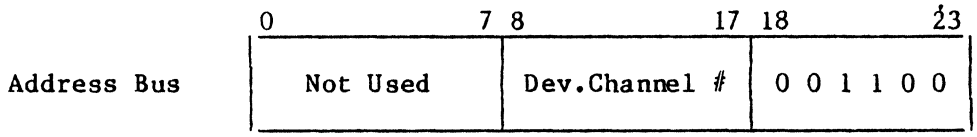


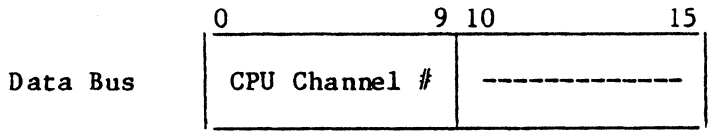


During the response cycle (second half read), the ESDIC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle. The data bus contains the high order 8 bits of the memory word address currently stored for the specified channel in the ESDIC. This command is used for diagnostic purposes only.

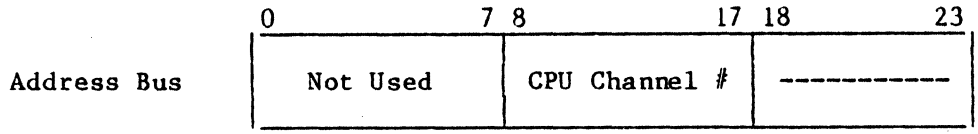
5.2.12 Input Range

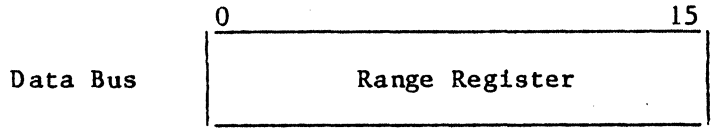
Request Cycle





Response Cycle



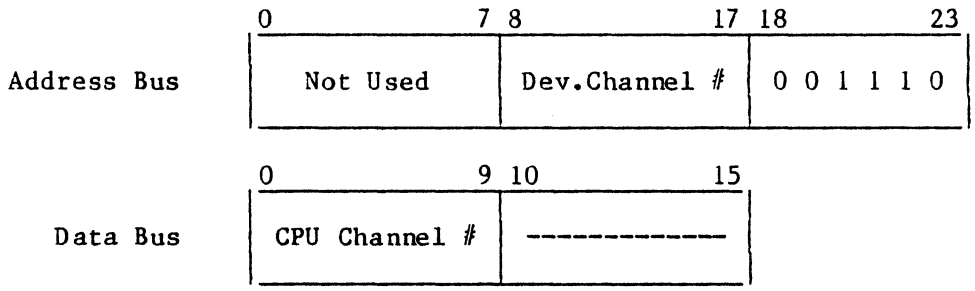


This instruction causes the current contents of the referenced channel's range register to be transferred to the requesting CPU channel.

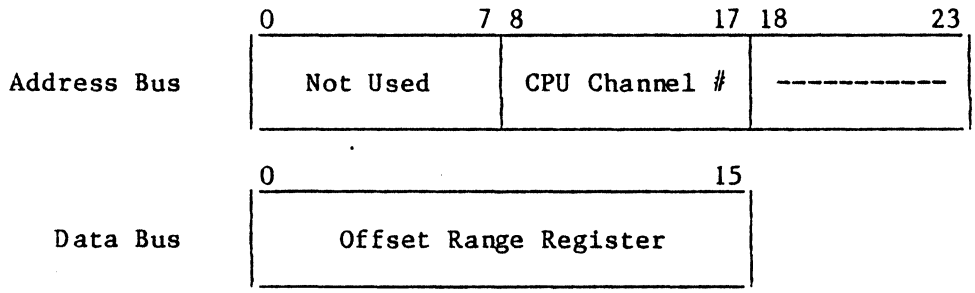
During the response cycle (second half read), the ESDIC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

5.2.13 Input Offset Range

Request Cycle



Response Cycle

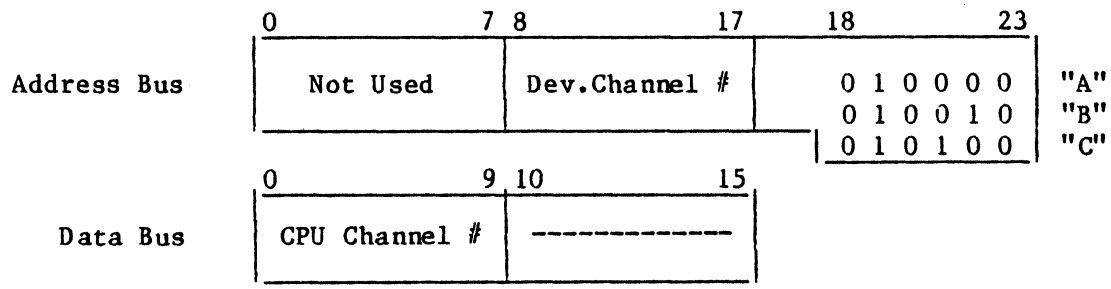


This instruction causes the current contents of the referenced channel's offset range register to be transferred to the requesting CPU channel.

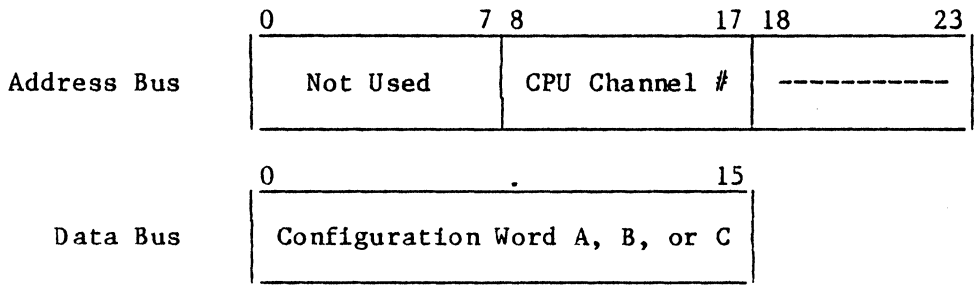
During the response cycle (second half read), the ESDIC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle. This instruction, implemented partially for compatibility reasons, reads the contents of the offset range register which was previously loaded by the Output Offset Range command and no other action takes place except the normal instruction termination.

5.2.14 Input Configuration Word A, B or C

Request Cycle



Response Cycle

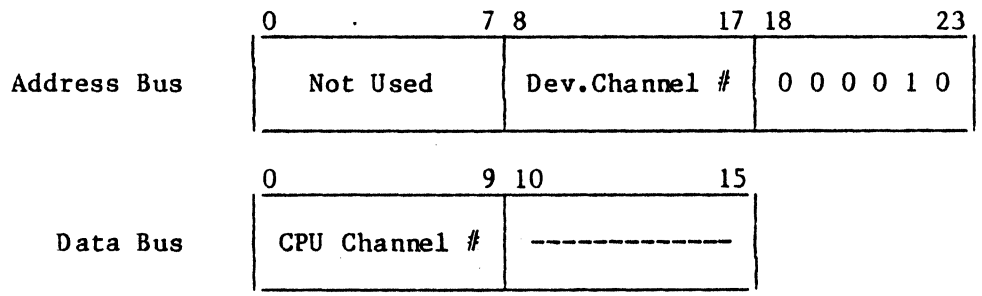


This instruction causes the current contents of the channel's Configuration Word A, B or C to be transferred to the requesting CPU channel.

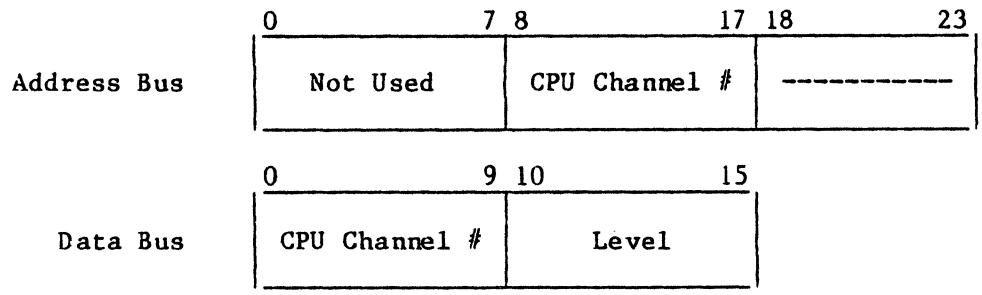
During the response cycle (second half read), the ESDIC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

5.2.15 Input Interrupt Control

Request Cycle



Response Cycle

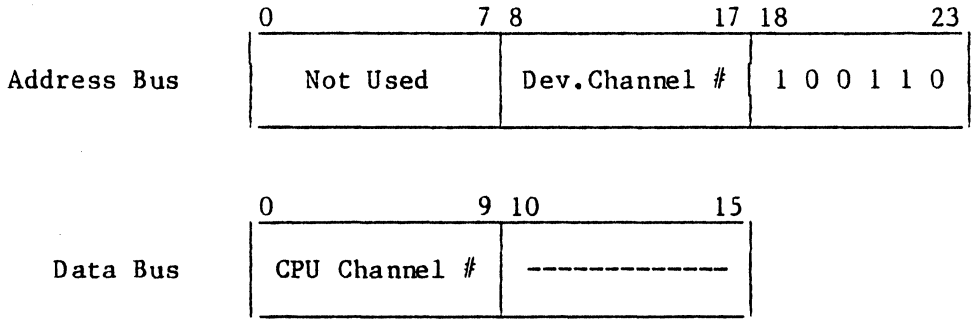


This instruction causes the channel's interrupt level to be transferred to the requesting channel. The level value is placed on data bus bits 10 through 15 (see above) with bit 15 as the least significant bit. This quantity is the value previously received in an Output Interrupt Control instruction, or a default value of 00. The default value is the interrupt level assumed by the channel when initialized. Note that the channel number returned in bits 0 through 9 of the data bus might be different than the channel number of the CPU executing this instruction if more than one CPU is attached to the Megabus.

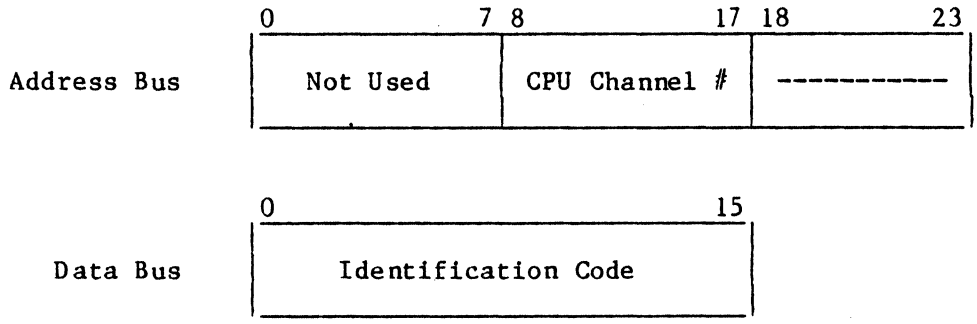
During the response cycle (second half read), the ESDIC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

5.2.16 Input Identification Code

Request Cycle



Response Cycle



This instruction causes the referenced channel to transfer its Identification Code to the requesting CPU channel. Depending on the device accessed, one of the following codes is returned:

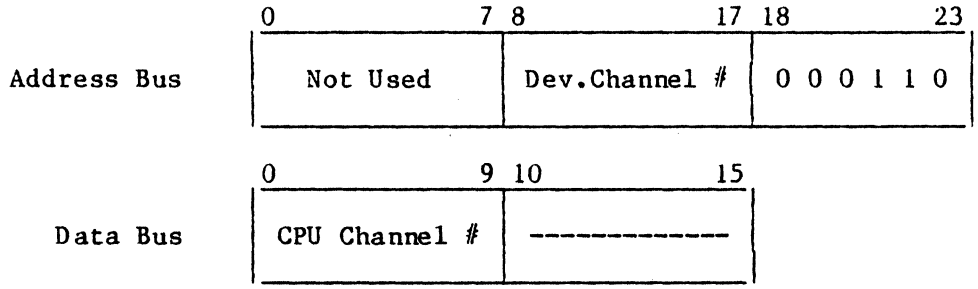
Code (Hex.)	Model
333A	Wren III, 142.6 MB
333C	Wren II, 37.8 MB
333D	Wren II, 68 MB
333F	See description below
207E	65 MB Sentinel Streamer
207F	Sentinel not Accessible
2017	5 1/4" Diskette
201F	Diskette not Accessible

The 333F code represents the ID code received when an WDD is physically attached but is not accessible to the system because the mainframe has been powered-up but the drive on the channel is not. The ESDIC generates the correct ID code when the device becomes available (i.e., when the drive is cycled up). It should be noted that this updated ID code becomes visible to software via the issuance of another Input Identification Code instruction.

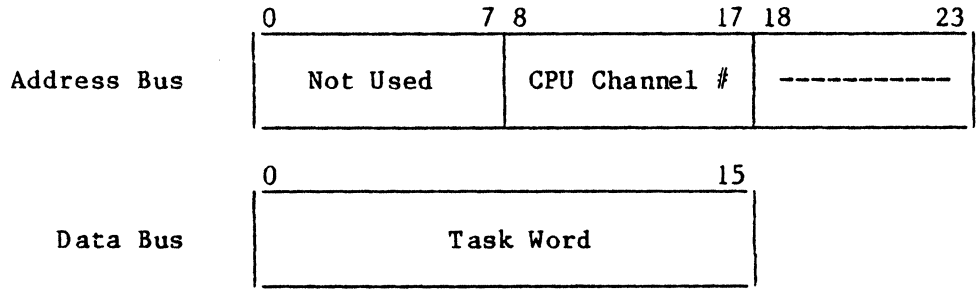
During the response cycle (second half read) the ESDIC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

5.2.17 Input Task Word

Request Cycle



Response Cycle

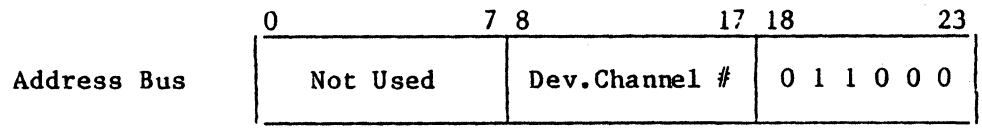


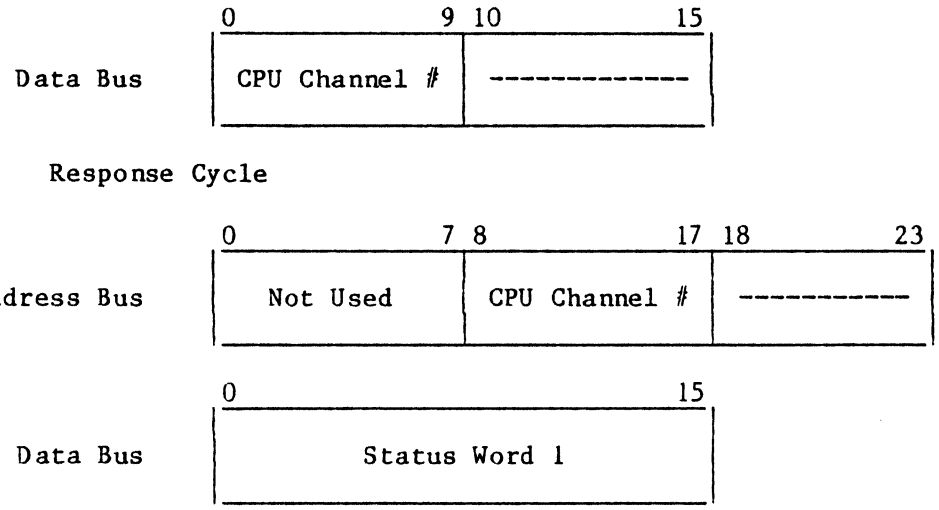
This instruction causes the Task Word of the referenced channel to be transferred to the requesting CPU channel. The Task Word transferred contains the code for the last operation executed by the channel (unless an initialize has occurred).

During the response cycle (second half read), the ESDIC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

5.2.18 Input Status Word 1

Request Cycle





This instruction causes the Status Word 1 of the referenced channel to be transferred to the requesting CPU channel.

During the response cycle (second half read), the ESDIC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

Data Bit		Description
0	----------	Device Ready
1	----------	Attention
2	----------	Overrun/Underrun
3	----------	Device Fault
4	----------	Read Error
5	----------	Program Error
6	----------	QLT Fault
7	----------	Unsuccessful Search/Format Error
8	----------	Error Log Overflow
9	----------	Successful Recovery
10	----------	ESDI Timeout
11	----------	RFU - MBZ
12	----------	Corrected Memory Error
13	----------	Nonexistent Resource
14	----------	Bus Parity Error
15	----------	Uncorrected Memory Error

5.2.18.1 Device Ready (Bit 0)

This bit indicates that the device is on line with the medium loaded and that no further manual intervention is required to place it under program control. Note that a change of state of this bit causes the attention bit (bit 1) to be set, resulting in an interrupt (if the interrupt level is nonzero). This bit reflects the current condition of the device. When the device is cycled down, spindle motor off, the Ready Status indication becomes not true.

5.2.18.2 Attention (Bit 1)

This indicator is set whenever the device ready bit (Bit 0 of the Status Word 1) changes state. Any change of operational status of the device is indicated to software in this way.

Whenever the attention bit is set, an interrupt is attempted (if the interrupt level is nonzero). If a previously initiated operation is in progress when a device status change is sensed, the resultant interrupt (with the attention bit set) serves as notification of both the end of the operation and the device state change.

This bit is reset by an Initialize command, an Output Task Word command, an Input Status Word command or Master Clear on the Megabus.

5.2.18.3 Overrun/Underrun (Bit 2)

This bit is set during a read or a write operation when the data transfer to or from main memory cannot be maintained at a high enough rate, 625 K Bytes/sec. Either data was lost on input because of failure to keep up with the device demands or data was not transferred from the FIFO into main memory fast enough.

This bit is reset by an Initialize command, an Output Task Word command, an Input Status Word command or Master Clear on the Megabus.

5.2.18.4 Device Fault (Bit 3)

This bit is set if the ESDIC status bit 0 is set indicating a device fault; bits 08 through 15 of Status Word 2 reflect more specific faults.

This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus. Note that operator intervention is required to reset the write protect condition of the device. Also note that this bit is reset if the condition causing it to set is removed by the WDD.

5.2.18.5 Read Error (Bit 4)

This bit is set during any Read operation if either the EDAC word at the end of a field indicates that an uncorrectable data error has occurred within the field or the CRC Error bit appears within the ID field provided it is a new error not logged in the New Error Log on the highest number cylinder. This bit is also set when during the Read After Write and Compare command a miscompare error is detected.

This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.18.6 Program Error (Bit 5)

This bit is set if any of the available Megabus commands are executed erroneously, e.g.:

- Seek to a nonexistent cylinder,

- o Format Write range is not = 128 bytes
- o Wraparound buffer range is incorrect
- o Attempt to select a nonexistent head

This bit is reset by an Initialize command, an Output Task Word command, or a Master Clear on the Megabus.

5.2.18.7 QLT Fault (Bit 6)

This bit indicates that the controller or an adapter QLT has failed and that the QLT status buffer contains the fault identification. The Device Ready bit is also reset in Status Word 1.

This bit is reset by an Initialize command or a Master Clear on the Megabus.

5.2.18.8 Unsuccessful Search/Format Error (Bit 7)

This bit is set during other than format Read or Write operation for which the sector ID specified in Configuration Words A and B cannot be located on the track or on the maximum cylinder. It is also set if Index Mark is detected during a format Write operation; in this case, memory address and range registers are invalid.

This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.18.9 Error Log Overflow (Bit 8)

This bit is set whenever the ESDIC detects that the New Error Log (on the innermost cylinder sectors 1 through 4) on the WDD, has exceeded 63 error sectors count. If reformatting does not reduce the error count, the media or the device needs further attention.

5.2.18.10 Successful Recovery (Bit 9)

This bit is set when an error condition was successfully recovered during previous operation; Status Word 2 specifies the error condition which has occurred.

This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.18.11 ESDI Timeout (Bit 10)

If the device decides to terminate a dialog sequence by not responding to Transmit REQuest signal with Transmit ACKnowledge, the ESDIC waits for approximately 500 milliseconds and then closes the dialog.

This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.18.12 RFU - MBZ (Bit 11)

This bit is reserved for future use and must be zero.

5.2.18.13 Corrected Memory Error (Bit 12)

This bit indicates that, during the previous Disk Write operation, main memory detected and corrected a memory read error. The data that was delivered to the ESDIC was assumed to be correct.

This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.18.14 Nonexistent Resource (Bit 13)

This bit is set whenever the ESDIC attempts any bus cycle (except interrupt) and receives a NAK response from memory.

This bit is reset by an Initialize command, an Output Task Word command, an Input Status Word 1 command, or Master Clear on the Megabus.

5.2.18.15 Bus Parity Error (Bit 14)

This bit is set whenever the ESDIC detects a parity error on either byte of the data bus during any bus cycle, or when a parity error is detected in bits 0 through 7 of the address bus.

This bit is reset by an Input Status Word command or an Initialize (via Master Clear or an Output Control Word command).

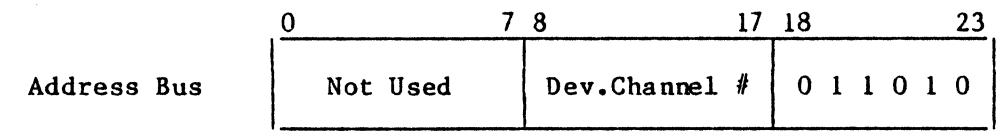
5.2.18.16 Uncorrectable Memory Error (Bit 15)

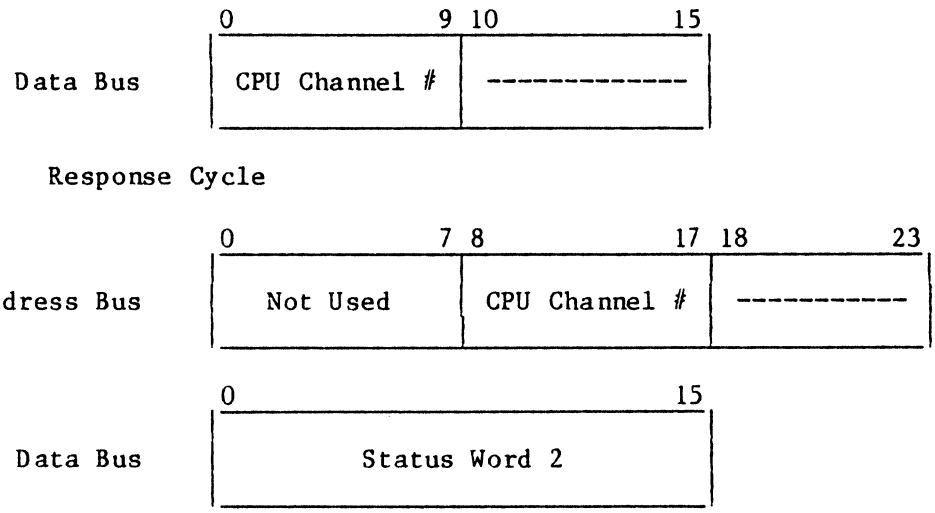
This bit indicates that, during the previous Disk Write operation, main memory detected a memory read error which the EDAC algorithm could not correct. The data that was delivered to the ESDIC may have been incorrect. Occurrence of this condition does not cause termination of the operation in progress but may result in bad data on the medium.

This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.19 Input Status Word 2

Request Cycle





This instruction causes the referenced channel's Status Word 2 to be transferred to the requesting CPU channel.

During the response cycle (second half read), the ESDIC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

Data Bus bit assignments:

Data Bit	Description
0	Corrected Read Error
1	Successful Retry
2	Overrun/Underrun Recovery
3 thru 5	RFU-MBZ
6	Error Log Overflow
7 thru 12	RFU-MBZ
13	Hardware Fault
14	Seek Error
15	RFU-MBZ

NOTE

If either bit 13 or 14, is set, bit 3 of the Status Word 1 is also set.

5.2.19.1 Corrected Read Error (Bit 0)

This bit is set when a correctable read error occurred during the previous Read operation. Correction was performed by the ESDIC in main memory. When this bit is set, it causes bit 9 of Status Word 1 to be set. See subsection 5.3.1 for EDAC functionality.

This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.19.2 Successful Retry (Bit 1)

This bit is set when a data read error has been successfully retried during the previous operation. Data stored in main memory is correct. When this bit is set, it causes bit 9 of Status Word 1 to be set. See subsection 5.3.2 for retry algorithm.

This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.19.3 Overrun/Underrun Recovery (bit 2)

This bit is set when an underrun or overrun error has been successfully retried during the previous operation. Data stored in main memory is correct. When this bit is set it also sets bit 9 of Status Word 1. See subsection 5.3.3 for the recovery algorithm.

This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.19.4 RFU - MBZ (Bits 3 through 12)

These bits are reserved for future use and must be zero.

5.2.19.5 Hardware Fault (Bit 13)

When this bit is set a device fault has occurred as listed in the interface specification, reference section 4.2.2.5.

5.2.19.6 Seek Error (Bit 14)

When this bit is set a seek error has occurred. This signal indicates that the device is unable to complete the actuator move or that it has moved to a position outside the recording area or that the address greater than the maximum number of tracks availabie has been selected. Read error is also set in Status Word 1 bit 4.

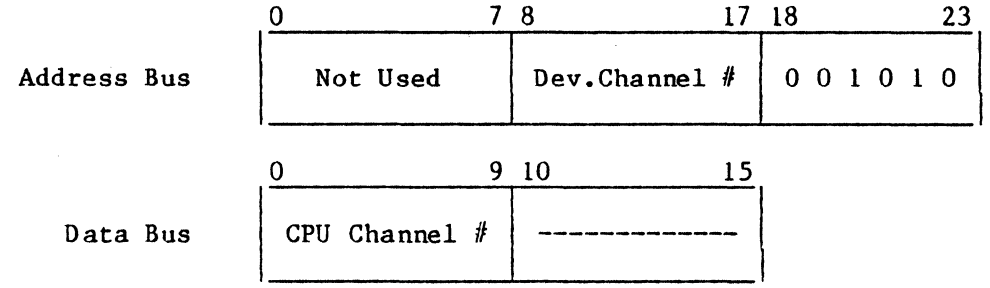
The Return To Zero command is required to clear this error and return the heads to track zero.

5.2.19.7 RFU - MBZ (Bit 15)

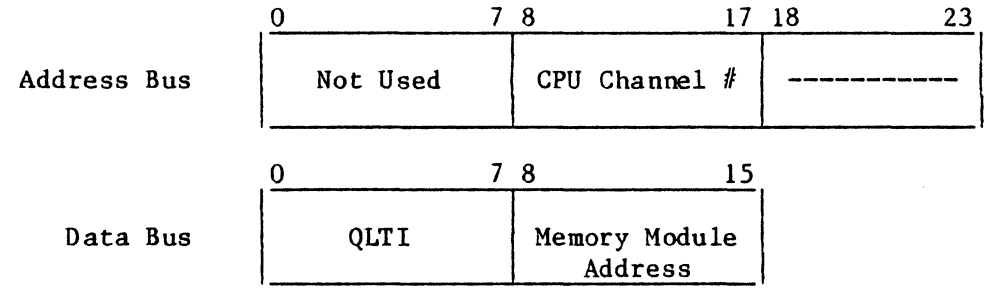
This bit is reserved for future use and must be zero.

5.2.20 Input Quick Logic Test Indicators (QLTI's)

Request Cycle



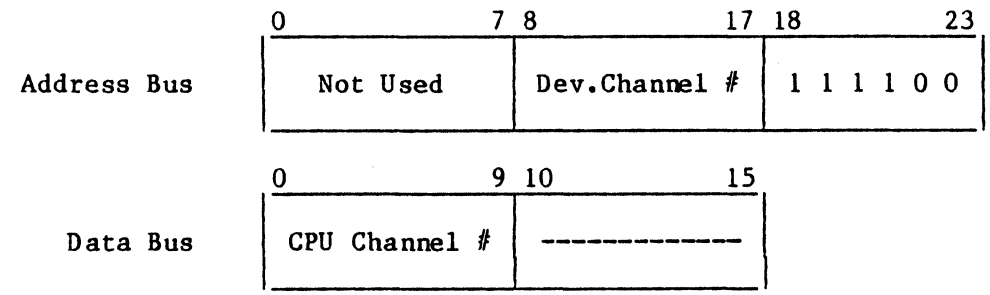
Response Cycle



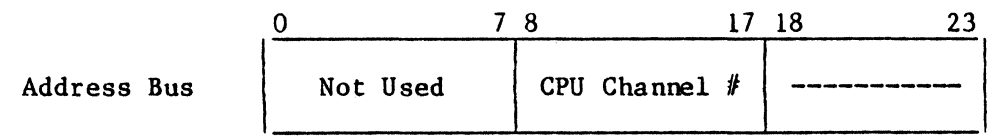
The QLTI's are stored in the Scratch Pad Memory (SPM) buffer during the QLT. If the edge indicator remains lit, the QLTI buffer contains the code of a test which had failed on either the ESDIC or on an adapter. (Reference subsection 8.3.2).

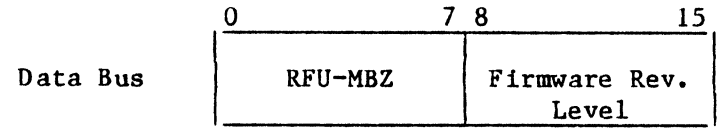
5.2.21 Input Firmware Revision

Request Cycle



Response Cycle

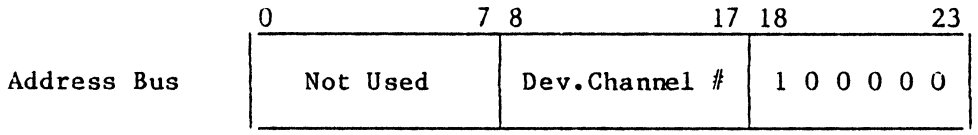


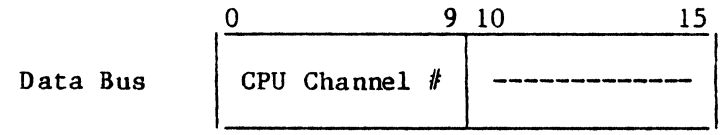


The firmware revision level is represented by a hex number, e.g., 23, which is the sequential control number.

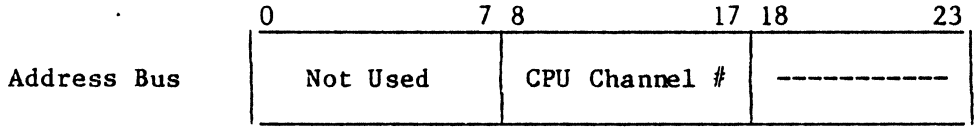
5.2.22 Input Retry Counter

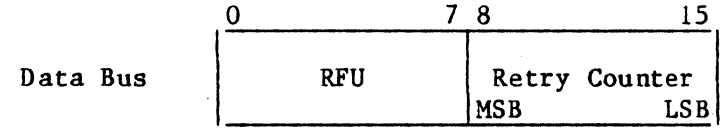
Request Cycle





Response Cycle





This instruction causes the referenced channel's Retry Counter to be transferred to the requesting CPU channel.

The Retry Counter contains the count of the number of times Read Error Retries were performed; reference subsection 5.3.2. This count is provided for error logging purposes.

The Retry Counter is reset by an Output Task Word, Initialize or a Master Clear on the Megabus.

5.2.23 Read/Write ESDIC Registers

The ESDIC maintains 32 registers (16 bits per register) for each channel. The address of each of the various registers in the ESDIC is a combination of 2 bits of the Channel Number and the high order five bits of the Function Code used to write into or read from a particular register (see Table 5-1). For example, Configuration Word A for ESDIC channel 2 is ESDIC register 48 (hex):

- Function code for configuration word A = 01000X (X = read/write bit)
- Channel number = 010Z (Z = direction bit)
- Register number = 0100, 1000 = 48 (hex)

Complete software visibility to the ESDIC registers is provided for diagnostic purposes. An output bus sequence addressed to one of the devices causes the information on the data bus (16 bits) to be loaded into the device specific register specified by the device port number and the high order 5 bits of the function code. (Reference Figure 5-1). The Output Address command is a special case. When an Output Address command is executed (on port 0, for example) the ESDIC register 04 (hex) is loaded with the low order 16 bits of the address. The high order 8 bits of the ESDIC register 05 are loaded with the high order 8 bits of the address.

Any input bus sequence addressed to a device causes the register specified by the Port Number and the high order 5 bits of the Function Code to be returned via the data bus (during the second half read cycle). A detailed register map for each device type is available in the ESDIC manual.

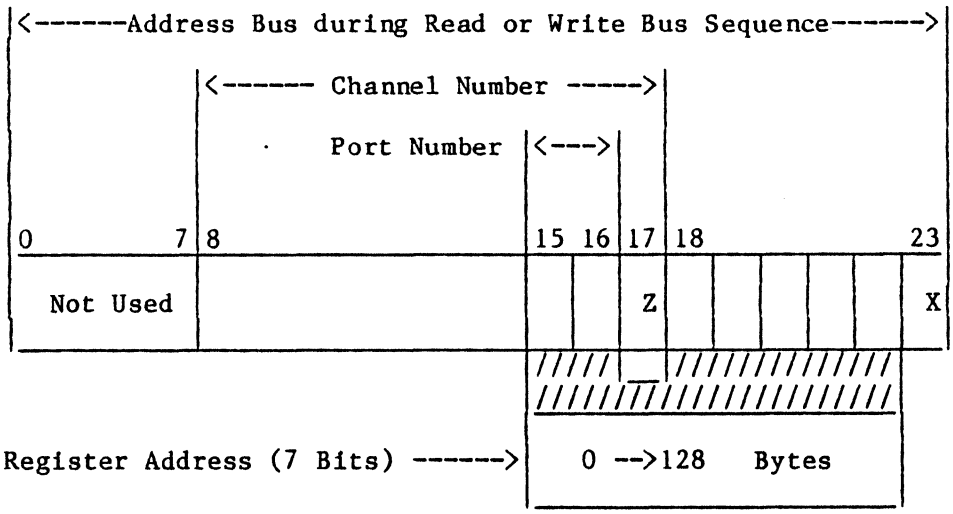


Figure 5-1 ESDIC Device Specific Registers and Addressing

5.3 Defect Management

5.3.1 EDAC Functionality

The seven byte EDAC field appended to the data field provides the correction of error bursts of up to 11 bits and detection of an error burst of up to 22 bits. Any bit errors separated by more than 10 bits are not correctable. The write polynomial generator used for the creation of a seven byte EDAC field is as follows:

$$\text{Write Polynomial} = 1 + x^i$$

where: i = 1, 5, 9, 11, 12, 15, 16, 17, 19, 22, 31, 36, 37, 38, 39, 41, 45, 49, 55 and 56.

During Update Read and Write operations, the detection of any read error in an ID field causes bit 4 of the Status Word 1 to be set. The search (update read or write) continues. If a successful search is not made prior to detection of two Index Marks, the operation is terminated with bit 4 set. If a successful search is made prior to detection of two Index Marks, bit 4 is reset and the operation continues normally. In either case, no error correction is performed on the ID field.

If a read error is detected following the transfer of a sector data field to main memory, one of two situations is possible:

- The ESDIC automatically performs the required correction in main memory, if a read error is correctable by EDAC after all retries, then sets bit 9 of Status Word 1 and bit 0 of Status Word 2, and continues the data transfer operation. Note that a loss of a number of revolutions of the media occurs during the retry period.

- If the error is not correctable EDAC is attempted only once after the retry procedure is unsuccessful in removing an error.

5.3.2 Read Error Retry

If a read error is detected following transfer of a sector data field to the main memory, the following retry procedure is invoked automatically by the ESDIC:

1. Three retries.
2. Three retries with data strobe offset early.
3. Three retries with data strobe offset late.

4. Three retries with track offset negative, data strobe offset early.
5. Three retries with track offset positive, data strobe offset late.
6. Three retries with track offset positive, data strobe offset early.

7. Three retries with track offset negative, data strobe offset late.
8. Three retries with track offset positive.
9. Three retries with track offset negative.

- The read error retry is applied to data field errors only during Read Data commands (does not apply to format or diagnostic commands - bit 4 of Status Word 1 is set in these cases as applicable).

- A latency period is entered between retries, i.e., no other channel on the ESDIC can be serviced.

- A loss of at least one revolution occurs for each retry.

- Any data strobe offset change or any track offset condition is automatically restored after retry (successful or unsuccessful).

The read error retry has one of two results:

- If the error is not recoverable, bit 4 of Status Word 1 is set and the operation is terminated.

- If the error is recoverable, bit 9 of Status Word 1 and bit 1 of Status Word 2 are set and the data transfer operation is continued.

5.3.3 Overrun/Underrun Retry

If an overrun or underrun condition is detected during Read or Write data procedures, the data field affected is automatically retransmitted by the ESDIC until the transfer is successful. Note that:

- o A latency period is entered between retries, i.e. another channel on the ESDIC can be serviced.
- o A loss of at least one revolution occurs for each retry.
- o An occurrence of an overrun or underrun retry results in the setting of Status Word 1 bit 9 and Status Word 2 bit 2.
- o Format and diagnostic commands are not retried if an overrun or underrun condition is detected. This results in Status Word 1 bit 2 being set.

5.3.4 Media Defect Handling

Definitions:

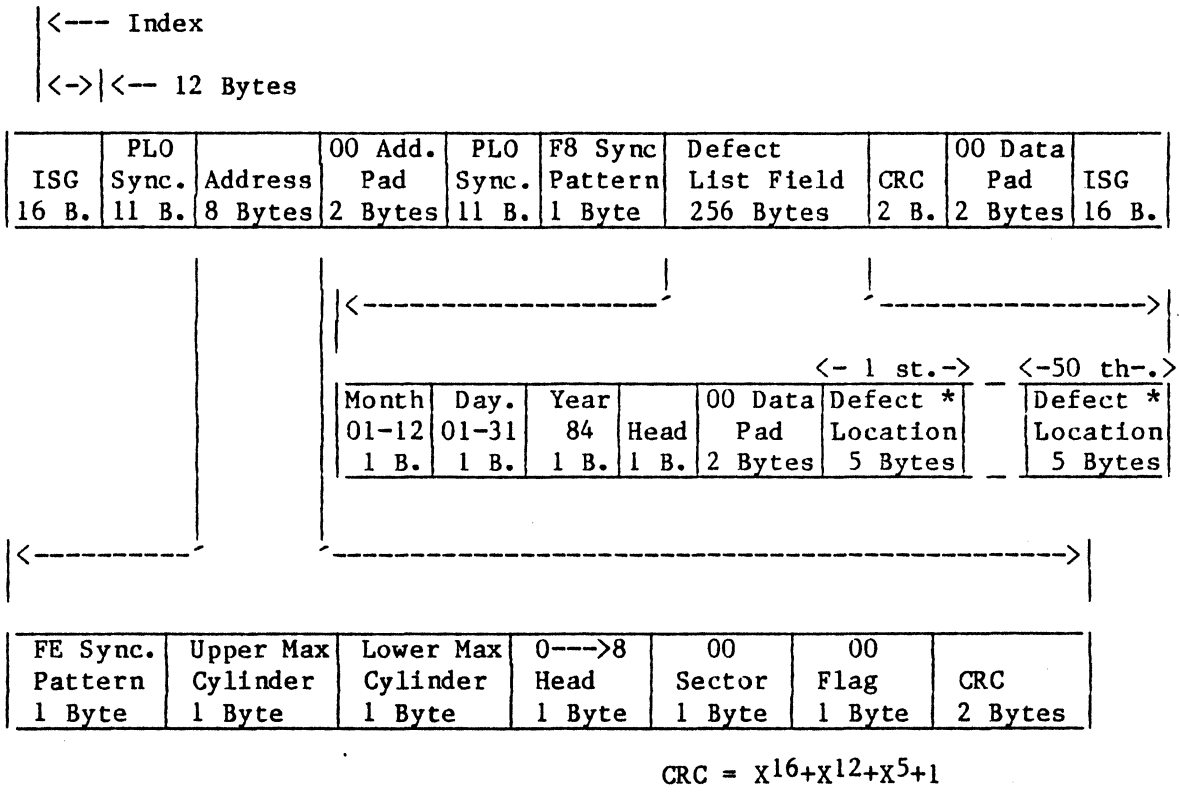
- o An error burst of 11 bits or less is a correctable error.
- o An uncorrectable error is one greater than 11 bits in length.
- o Acceptable criteria (CDC specification 77738019, Wren II, and 77738212, Wren III,, section 8.0 through 9.0) for the Wren fixed media:
  - a Have no media defects on track 0 on each surface, i.e. cylinder 0 is error free.
  - b Have no more than 15 defects per surface for the Wren II and 30 defects per surface for the Wren III.
  - c Accumulative defects not to exceed 1 per one megabyte based on total available drive capacity.

5.3.4.1 Vendor Error Log

Each track is analyzed, during media certification by the device vendor, for correctable and uncorrectable error conditions. If either defects exist, they are logged on sector 0 of the corresponding surface, on all surfaces of the maximum cylinder. The same, redundant, error log is provided on a second cylinder, maximum cylinder minus eight; ESDIC ignores this second error log because the error sector (both vendor identified and new) replacement algorithm allows for errors on the maximum cylinder. A list of all the media defects is also available with each device.

5.3.4.2 New Error Log

The New Error Log is constructed during Create Volume (CV) procedure when a new volume is formatted for the first time or when a volume is reformatted and the error

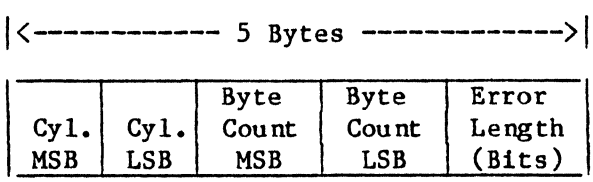


$CRC = X^{16}+X^{12}+X^{5}+1$

- Format and defect list is duplicated at maximum cylinder minus eight.

- End of Defect Location listing is 1's filled to end of data field (5 bytes of 1's minimum to terminate) or end of sector.

* Defect Location:



- Byte count from index to define start of defect; resolution is within 7 bits.

Figure 5-2 Vendor Error Log Format

log is recreated. The New Error Log resides on the maximum cylinder, head 0, sector 1; it can contain identities of up to 63 new defective sectors for the entire volume. The remainder of the Error Log cylinder is used, by the ESDIC firmware, for reallocation of error sectors identified by both the Vendor Error Log and the New Error Log.

Additionally, if during the life of the medium a new error should develop, software identifies the erroneous sector and appends its parameters to the New Error Log. This triggers the firmware in the ESDIC to reallocate that new error sector.

5.3.4.3 Error Log Management

On initialization it is necessary to ascertain that a device has been previously formatted and contains Error Logs, it is necessary to attempt to read the Error Log cylinder first:

- New or unformatted media.

  If, initially, an attempt to read sector 0 on all surfaces results in either a CRC error or an unsuccessful search or both, the Error Log cylinder must be formatted because the Vendor Error Log does not exist.

- Formatted media.

  However, if the Vendor Error Log does exist, all correctly read Vendor Error Log error sector parameters are translated into Honeywell sector ID format and are saved in local memory. The maximum cylinder must be formatted.

  If the Error Log cylinder has been formatted before, reading head 0,sector 0 produces an ID of maximum cylinder # + head 0 + sector 0. The New Error Log sector ID's are maximum cylinder # + head 0 + sector 1; remaining sector ID and data spaces on that track are FF filled . Remaining tracks on the Error Log cylinder are formatted with true sector ID for the zero sector and all other sector ID's and data fields are FF filled. It is optional to format this cylinder when part or the entire volume is reformatted. All vendor identified bad sectors on the Error Log cylinder are identified by an ID of BADD and an incorrect CRC; when reallocating error sectors, firmware skips over these sectors.

  The Format Write Task to the Error Log cylinder, head 0, is interpreted by the HSDC firmware as a command to format that cylinder, all heads; data fields of all sectors (and all ID fields except ID fields of all sector zero's and the New Error Log) are FF filled. The New Error Log parameters, if present, and reallocated sectors are lost in this process.

5.3.4.3.1 Vendor and New Error Logs

The Format Write Task to any other track (not the Error Log cylinder) results in the following:

- On Initialization the ESDIC reads the Vendor Error Log and translates its parameters into standard Honeywell, four byte, sector ID format and together with the parameters from the New Error Log stores them in the local memory. Each error sector entry consists of:

- High Cylinder Address byte with the volume bit (bit 4) set to 1.
- Low Cylinder Address byte.
- Head/Track Number byte.
- Sector Number byte.

o All the identified bad sectors have bad CRC's written in the ID fields when the track is formatted.

o The ESDIC firmware then searches for the error sectors' ID's on the Error Log cylinder beginning on surface 0 ,sector 2. The search continues until that sector ID is found or an ID of FF's is encountered on this or following surfaces.

If error sector ID is found data field is written with 6D pattern, sectors have been already reallocated and no further action is required.

If an ID of FF's is found sectors have not been reallocated. This error sector ID is then written, beginning on this surface, with replacement of the first ID of FF's.

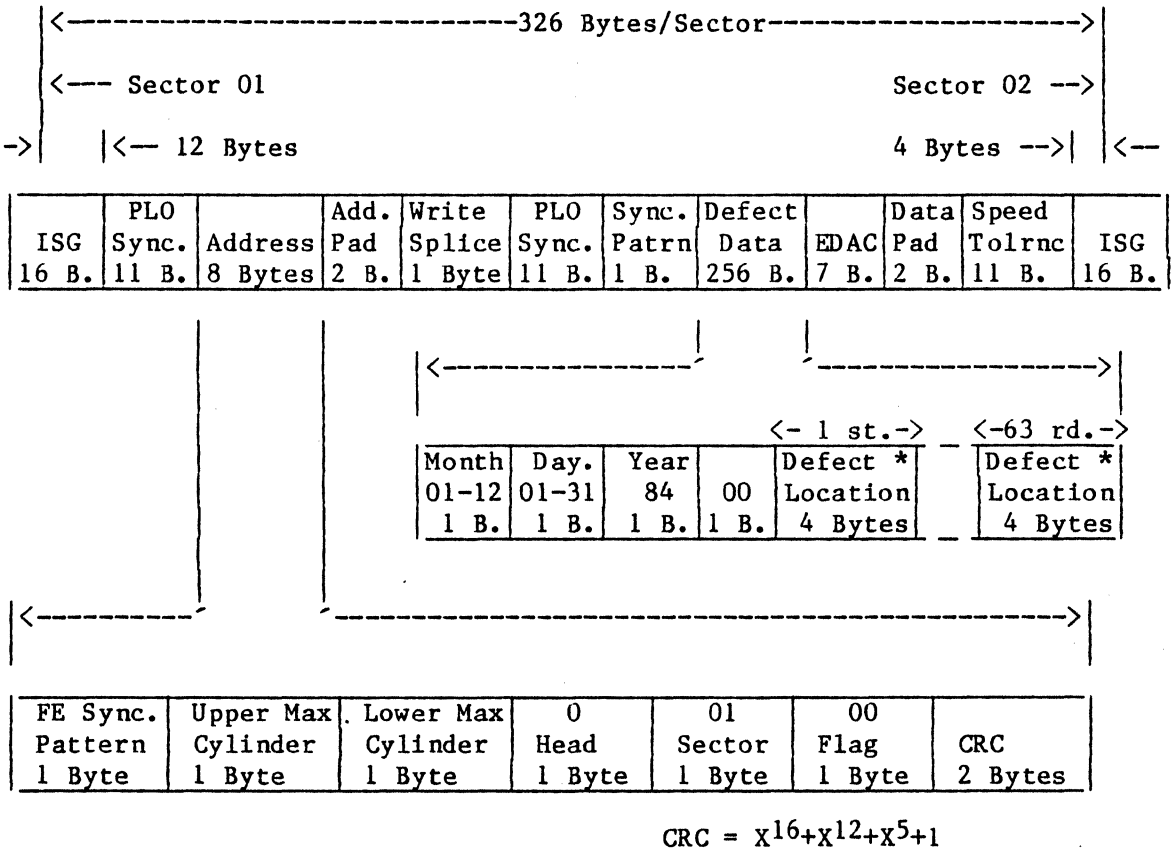
o If the New Error Log exists on the Error Log cylinder (head 0, sector 1) it is read into the main memory, by software, where it remains until a command other than a Format Write is in process. Subsequent Format Write commands to other tracks need only to refer to the New Error Log saved in the main memory to identify associated error sectors. The above is necessary to identify error sectors already recorded in the New Error Log for the track being formatted. Bad CRC's are written in ID fields of sectors identified as in error on the formatted track.

5.3.4.3.2 New Error Log Management

After formatting part or the entire volume the Format Write operation has to be verified by reading, not more than a track at a time, the formatted section of the volume. If a new error sector is found it is reallocated as described in the "New Error Procedure" below after which verification of the remaining sectors on that track resumes.

New Error Procedure:

- o If a new error is found the ESDIC stops the disk data transfer on the error sector and sends an interrupt to the CPU.
- o Software responds to the interrupt then reads Status Word 1 and both Configuration Words A and B to determine which sector on the track is in error.
- o The New Error Log is then read, by software, and the error sector parameters are appended (in place of the first four bytes of FF's in the data field) to the log.
- o The New Error Log is written back on the Error Log cylinder which triggers the ESDIC firmware to reallocate the last error log entry.



o End of Defect Location listing is 1's filled to end of data field (4 bytes of 1's minimum to terminate) or end of sector.

* Defect Location:

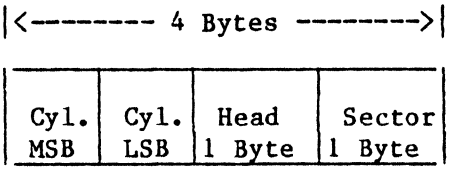


Figure 5-3 New Error Log Format.

- The firmware records bad CRC in the ID field of the error sector and then reallocates that sectors' ID to the Error Log cylinder searching to replace the first ID field (from Index Mark) of FF's starting on surface 0, sector 2 then continue for the rest of the maximum cylinder (skip over all 0 sectors); search continues sequentially to other surfaces until an ID field of FF's is found. If not found Status Word 1 bit 8, Error Log Overflow, is set and search terminates.

5.3.4.3.3 New Error Management

If, during the life of media, a new error develops the sector in error is reallocated in the same way as described in section 5.3.3.3.2 "New Error Procedure".

5.3.4.4 New Error Log Format

The New Error Log is 256 bytes long, residing on the maximum cylinder, head 0, sector 1. The one sector of the log is initialized, by firmware, to all FF's when the Format Write Task is issued, by software, to the Error Log cylinder. The first four bytes of the log are reserved for software use and the rest of the log is used for new error sector parameters. Each error sector log consists of four bytes corresponding to the error sector ID; thus 63 [(256-4)/4] new error sectors can be accommodated in the New Error Log.

6 PHYSICAL STRUCTURE

6.1 General

The Enhanced Small Device Interface Controller subsystem consists of an ESDIC and from one to two WDD's which are connected to the controller board via radial cables. The controller, a mother (M) board, is etched and has four connectors and electrical attachments to WDD's; two control "A" cable connectors and two data "B" cable connectors.

The ESDIC mother board has provision for connecting two adapters; one to interface to the Minidiskette (QDM) and one to interface to the Streamer Adapter (SA).

6.1.1 Physical Specifications

6.1.1.1 Mechanical

- Dimensions: 15 in. (38.1 cm) wide by 16 in. (40.64 cm) long by 0.062 in. (0.157 cm) thick
- Weight: Approximately 28 oz. (0.794 kg)
- Cabling: Four connectors connect between the M-board and the WDD's. There are two control "A" cables and two data "B" cables between the M-board, and from one to two disk drives connected. The maximum cable length from the controller to the device shall not exceed 10 feet (3.0 m). Device connectors have 34 pins on cable "A" and 20 pins on cable "B".
- Cooling: Forced, unfiltered air at 125°F (51.7°C) maximum ambient at 110 CFM (51.9 liters per second).

6.1.1.2 Environmental

- Meets HIS standards, B01.08 - Class II (contamination requirements are waived).
- Meet all U/L requirements, CSA approval.

6.1.1.3 **Electrical**

- o Primary power - B01.48, Group I, II, III and VI
- o Power module to share a common chassis with the printed circuit boards.
- o Further definition given in NML Power Spec (60126325).

6.1.2 **Physical Specifications, Winchester Disk Drive.**

6.1.2.1 **Mechanical**

- o Dimensions: 5.75 in. (14.6 cm) width, 3.25 in. (8.26 cm) height (including the front face panel), 8.0 in. (20.3 cm) depth.
- o Weight: 6.7 lb. (3.1 kg), Wren II; 7.3 lb. (3.4 kg), Wren III
- o Rear panel: Location of cable connectors
- o Cabling: Cabling connecting the ESDIC with the WDD device in a radial fashion should not exceed 10 feet (3.0 m.). Cable connectors at rear of each device accept cables.
- o Cooling: Forced air cooling to satisfy operational temperature requirements.
- o Mounting positions: Horizontal; Ready light on the lower left side.
  Vertical; Ready light on the bottom.

6.1.2.2 **Environmental**

The disk device withstands the following environmental extremes without adverse effects and meets HIS standards B01.08 and B01.10, Class II except as noted (*).

Wren II:

- o Operating temperature, dry bulb: 50°F (10.0°C) to 114.8°F (46°C) with linear derating to 95°F (35°C) from above 983 feet (300 m) to 9,840 feet (3000 m); ie @ 1.8°F/1640 ft. (1°C/500m.).
- o Operating temperature gradient: 18°F (10°C)/hour maximum
- o * Operating humidity: 20% to 80% RH (noncondensing); HIS specification: 10% to 90% RH.
- o Humidity gradient: 10% per hour maximum.
- o Wet bulb temperature: 82°F (28°C) maximum, reference 58.7°F (14.8°C).
- o Storage temperature: 14°F ((-10°C) to 122°C (50°C).
- o * Storage temperature gradient: 27°F (15.0°C)/hour maximum; HIS specification: 25°C/hour.
- o * Storage humidity: 10% to 90% RH for 90 days maximum; HIS specification: 95% RH.

- o Transit temperature: -40°F (-40°C) to 158°F (70.0°C)
- o * Transit temperature gradient: 36°F (20°C)/hour maximum; HIS specification: 25°C/hour.
- o Transit humidity: 5% to 95% RH.

- o Effective Altitude (Operating & Storage): - 983 to + 9,830 feet (- 300 m. to +3000 m.) with sea level reference with
- o Transit Altitude - 983 to 40,000 feet (- 300 to 12,210 m.).

Wren III:

- o Operating temperature, dry bulb: 50°F (10.0°C) to 122°F (50°C) with linear derating to 112°F from above 1,000 feet (305 m) to 10,000 feet (3048 m); ie @ 1.8°F/1640 ft. (1°C/500m.).
- o Operating temperature gradient: 18°F (10°C)/hour maximum

- o * Operating humidity: 5% to 85% RH (noncondensing); HIS specification: 10% to 90% RH.
- o Humidity gradient: 10% per hour maximum.
- o Wet bulb temperature: 82°F (28°C) maximum, reference 58.7°F (14.8°C).

- o Storage temperature: 6°F ((-14°C) to 130°C (54°C).
- o * Storage temperature gradient: 27°F (15.0°C)/hour maximum; HIS specification: 25°C/hour.
- o Storage humidity:· 5% to 95% RH for 90 days maximum.

- o Transit temperature: -40°F (-40°C) to 158°F (70.0°C)
- o * Transit temperature gradient: 36°F (20°C)/hour maximum; HIS specification: 25°C/hour.
- o Transit humidity: 5% to 95% RH.

- o Effective Altitude (Operating & Storage): - 1,000 to + 10,000 feet (- 305 m. to +3048 m.) with sea level reference with
- o Transit Altitude - 1,000 to 40,000 feet (- 305 to 12,210 m.).

- o Meet all UL requirements.

6.1.2.3 Shock and Vibration

Wren II and Wren III:

- o Operating shock, normal: 2 G's maximum of 10 ms., half sinewave.
- o Operating shock, degraded: 6 G's maximum of 10 ms., half sinewave.
- o Non-operating shock: 32 G's maximum of 10 ms., half sinewave.

- o Transit shock, MPI package: 48" (1.22 m.) drop.

- o Operating vibration, normal: 5 - 22 Hz @ 0.010" displacement
  22 - 500 Hz @ 0.25 G
- o Operating vibration, degraded: 5 - 22 Hz @ 0.010" displacement
  22 - 500 Hz @ 0.35 G of 15 minutes duration.

- Non-operating vibration: 5 - 10 Hz @ 0.020" displacement
  10 - 500 Hz @ 1.00 G

6.1.2.4 Electrical

Wren II Power Requirements

Voltage	+ 5 V dc.	+ 12 V dc.
Regulation	± 5%	± 5% *
Ripple	50 mV.	100 mV.
Current		
Maximum operating Current	0.9 A.	2.4 A.
Typical operating Current	0.75 A.	2.0 A.
Maximum (peak) starting Current	1.3 A	4.5 A.
Power		
Maximum power requirement	31.5 Watts (116 BTUs/hour)	
Average power requirement	≤ 28 Watts (96 BTUs/hour)	

Wren III Power Requirements

Voltage	+ 5 V dc.	+ 12 V dc.
Regulation	± 5%	± 5% *
Ripple	100 mV.	100 mV.
Current		
Maximum operating Current	1.0 A.	2.3 A.
Typical operating Current	0.7 A.	1.6 A.
Maximum (peak) starting Current	1.4 A	4.5 A.
Power		
Maximum power requirement	28 Watts (96 BTUs/hour)	
Average power requirement	≤ 23 Watts (79 BTUs/hour)	

* ± 10% tolerance is permissible during power up to Unit Ready interval.

There is isolation of dc ground and frame ground in the disk device. The two grounds are brought out separately for external connection at a system level tie point.

6.1.2.5 World Standards/Safety

UL 478, 5th Edition.
CSA 22.2, 154 - 1983.
IEC 345
IEC 380
VDE 0804/3.77
VDE 0806
VDE 0871
FCC, Part 15, Class A

7 PERFORMANCE

7.1 General

The ESDIC accommodates a maximum data throughput of 14.52 MHz bits per second from a device; Wren II data rate is 5.0 MHz and Wren III data rate is 10.0 MHz with an average Megabus data rate of 625 K bytes per second. The controller provides a 32 byte FIFO memory buffer.

The ESDIC has only one level of simultaneity. Only one data transfer can be active at any time but control functions, like seek, are processed simultaneously. One data transfer and any number of control functions can be processed at the same time. All error retries cause at least one revolution (16.7 ms) delay and all reallocated error sectors cause at least two revolutions delay plus two average seek times.

Device Model #	Wren II 94156-48/86	Wren III 94166-182
Positioning times in ms.:		
maximum	85	50
maximum single track	8	6
average	35	23
Latency, in ms.:		
maximum	16.83	16.74
average	8.33	8.33
Spindle timing, in sec.:		
start time	< 35	< 35
stop time	< 30	< 30
Head timing, in us.:		
select time	5	5
settling time (with PLO lock)	19	19
Write to Read recovery, us:	11	11
Read to Write recovery, us:	0.3	0.3
Return To Zero (RTZ), sec.:	< 0.5	< 0.5

Table 7-1 WDD Performance Characteristics.

7.2 WDD Performance Characteristics

Performance characteristics of the WDD are summarized in Tables 7-1 and 7-2 .

Device Model #	Wren II 94156-48	Wren II 94156-86	Wren III 94166-182
Capacity (Unformatted):			
Bytes per track	10,440	10,440	20,880
Bytes per cylinder	52,200	93,960	187,920
Bytes per Spindle	48,285,000	86,913,000	182,094,480
Capacity (Formatted):*			
Bytes per track *	8,196	8,196	16,384
Bytes per cylinder *	40,980	73,728	147,456
Bytes per spindle *	37,824,540	68,050,944	142,589,952
Sectors per track	32	32	64
Bytes per sector	256	256	256
Number of user cylinders **	923	923	967
Number of heads (data)	5	9	9
Number of user tracks	4,615	8,307	8,703
Recording mode	MFM	MFM	2,7
Density, in bits per inch: inner track	9,600	9,600	19,058
Tracks per inch	960	960	960
Spindle speed, $\pm$ 0.5%	3,600	3,600	3,600
Data rate, MHz. $\pm$ 1%	5.0	5.0	10.0
Weight, lbs.	6.7	6.7	7.3

* Calculations are based on the number of user cylinders.

** In addition, two cylinders are reserved: one for T. & V. use and one for Error Logs & reallocated error sectors.

Table 7-2 WDD Device Characteristics.

8 AVAILABILITY

8.1 Integrity

Data integrity is checked in the subsystem by the Error Detection and Correction code described in subsection 5.3.1. All data written on the media has a seven byte code (EDAC) appended such that when the data is subsequently read, the accuracy of the recovered data is guaranteed within limits. Parity is checked from the Megabus through the internal bus structure including buffer memory and SPM. Whenever the subsystem is initialized, QLTs are executed by the ESDIC to provide a basic level of confidence that the microprocessor is fault free (see subsection 8.3). All subsystem detected errors are reported or displayed (refer to subsections 5.3 and 8.4).

8.2 Security

Write protect option is not available on this device.

8.3 Maintainability

8.3.1 Maintainability Requirements

The following design goals, measured in hours, are specified as a minimum to be achieved during the first year after initial shipment or the 100th unit shipped, whichever comes first. References to "repair" normally imply ORU replacement.

8.3.1.1 Mean Time to Repair (MTTR)

MTTR represents the average repair time for a service engineer to diagnose, isolate, repair or replace, and verify the fix using the maintainance procedure described in 8.3.2. MTTR does not include response time, travel time, or idle time at the site waiting for the system or needed spare parts. These MTTR times are given for each unit that comprises the ESDIC subsystem.

UNIT	AFTER FIRST YEAR
ESDIC	0.9 hour
WDD	0.9 hour

8.3.1.2 Mean Time Between Preventive Maintenance (MTBPM)

This goal, the period of operational time between required or recommended preventive maintenance (PM), is given for each unit.

UNIT	MTBPM
ESDIC	no PM
WDD	no PM

8.3.1.3 Diagnostic Facility Localization Effectiveness (DFLE)

This represents the probability that a hard failure can be localized to a unit. The DFLE given takes into consideration the comprehensiveness, the resolution, and the accuracy of the diagnostic facility provided. Requirements below relate to the SCPO designed components of the subsystem, not to the WDD, when complete set of maintainability tools, subsection 8.3.2, are used to detect and isolate the fault.

DFLE	First Ship
Comprehensiveness	95%
Isolation to an ORU	85%

- Comprehensiveness is the ratio, in percent, of the number of faults detected to the total number of faults that can occur.
- Isolation to an ORU is the ratio of the number of faults correctly resolved to the ORU, to the total number of faults that can occur.

8.3.2 Maintenance Strategy

The maintenance strategy for the ESDIC subsystem is in accordance with the governing EPS on the DPS-6 System. The subsystem is partitioned into ORU's which can be effectively diagnosed for a faulty condition via a combination of firmware controlled tests, software tests, and visual indicators. Available diagnostic aids to be provided are to be executable by the customer as well as a service engineer. Simple repairs such as the replacement of a defective ORU with an operational one should be able to be carried out by trained customer personnel or service engineers. Faulty ORU's are not serviced on the customer site.

8.3.2.1 Maintainability Features

The ORU's for the ESDIC Subsystem are:

- ESDIC
- ESDIC adapters either minidiskette and/or streamer tape.
- ESDIC to WDD cables
- WDD

Isolation of a failure to an ORU is achieved via a three step Trouble Shooting and Repair Procedure (T. & R.P.):

The first step:

The Quality Logic Test (QLT) supplies a go/no-go visual identification of a ESDIC hardware failure. The QLT is invoked by one of the following: Power On sequence, Master Clear or Output Control Word initialize command on any of the ESDIC channels. QLT LED's conform to the following rules:

QLT "ON" the ESDIC = ESDIC failure
QLT "ON" an Adapter = Adapter failure
QLT "ON" the ESDIC and an Adapter = Don't know which

The QLT verifies operation of each of the ESDIC ORU's. In addition, if a failure is detected during any of the tests, a QLT indicator register is loaded associating tests performed with deviations from expected results for the ESDIC; the results are made available for interrogation at the end of the QLT in the QLTI register. QLTI contains the failing firmware routine code; firmware listing must be consulted for further clarification.

The QLT should conform to the following:

- The QLT provides a means of isolating a fault to a ORU when combined with an appropriate T&V software routine.
- No test must be allowed to stop the clock; i.e., no halt condition can exist in the firmware unless, if permitted to run, the controller would affect the Megabus operation.
- The controller must issue NAK, not WAIT, during the QLT.
- Cables can be tested by substitution or by a continuity meter only.

Major QLT functions:

- Read/Write a data pattern into all local memory locations and verify; verify EPROM/ROM integrity.
- Wraparound data with bad parity on the Megabus to test the data paths of the controller and check the parity error detection logic.
- Run extensive tests on the ESDIC and connected adapter logic.

The second step:

Software T&Vs are provided to verify, operational aspects of the ESDIC, and to isolate failures to an ORU. Operator interface with these routines is via a CSS control panel or a TTY compatible console. The routines are run stand alone. Diagnostic functionality has been included, last but one cylinder on a WDD, in the subsystem to support software diagnostic routines.

The third step:

Each WDD is equipped with a self diagnostics which can be invoked by a command; results, if not successful, are available through Standard and Vendor Unique Status for further analysis.

A test procedure for execution by nontechnical trained customer personnel, field engineering personnel, or by others isolating faults to an ORU, is supplied to support the QLT and the appropriate device ORU isolation test routines. The designated ORU's are easily removable and replaceable. The only tool required is a screwdriver. System power must be off to remove or replace an ORU.

0	1	2	3	4	5	6	7	QLTI Byte
0	0	0	0	0	0	0	0	All good
1	0	0	0	0	0	0	0	Device #1, fault
1	0	0	0	0	0	0	1	Device #2, fault
1	0	0	0	0	0	1	1	Device #4, fault
1	0	0	1	0	0	0	0	Channel #1, fault
1	0	0	1	0	0	0	1	Channel #2, fault
1	0	0	1	0	0	1	1	Channel #4, fault
1	1	0	1	0	0	0	0	ESDIC fault
1	1	1	0	0	0	0	0	ESDIC to Megabus fault

Figure 8-1 QLT Indicator Register Codes.

8.3.2.2 Installation

All ESDIC equipment installations or expansions to a basic system are Field Engineering responsibility. Replacement of faulty units is also CSD's responsibility for the initial shipments; subsequent maintenance can be performed by customer personnel, except for the ESDIC which resides in the main cabinet assembly.

8.4 Reliability

8.4.1 Product Life

Product life is defined as the period of time within which the equipment performs within established reliability goals.

ESDIC	10 years
WDD	5 years (30,000 hours)

The above estimates are made assuming 100% duty factor.

8.4.2 Mean Time Between Failures (MTBF)

MTBF is expressed in "power on" hours of the component or ORU and is concerned only with hardware failures. It is a minimum to be achieved after First Customer Ship (FCS).

	100^{th} UNIT
ESDIC	65,000 hours
Wren II	15,000 hours
Wren III	20,000 hours

8.4.3 Mean Time Between Calls (MTBC)

MTBC is expressed in usage hours of the component or ORU between unscheduled or scheduled demand or emergency calls caused by hardware, operator, or media malfunctions which cannot be corrected by the operator (this includes installation of required FCOs). A "call" is a visit to the customer site by a field engineer. MTBC does not include calls for preventive maintenance.

	100^{th} UNIT
ESDIC	55,000
WDD	5,000

8.4.4 Transient Error Rate - 1 in 10^9.

The transient error rate is the total number of errors encountered as a function of the number of bits read before any recovery techniques are attempted.

8.4.5 Recoverable Error Rate - 1 in 10^{10}.

The recoverable error rate is the number of errors encountered which are recovered within 27 subsystem retries as a function of the number of bits read.

8.4.6 Unrecoverable Error Rate -1 in 10^{12}.

The unrecoverable error rate is the number of errors encountered which cannot be recovered within 27 subsystem retries as a function of the number of bits read.

8.4.7 Recoverable Seek Error Rate -1 in 10^6.

A recoverable seek error is one in which the Seek operation fails to position the device read/write head on the proper cylinder. However, upon the issuance of a Recalibrate command followed by a Seek command to the same cylinder, the Seek is executed correctly.

Blank

Reviewed by: _____ Date: _____
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Director, Peripheral Hardware Development.

Approved by: T Hatch Date: 11/18/85
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