CAUTION

DON'T DO ANYTHING BEFORE YOU READ THIS DOCUMENT!

```
/A4.        --
100
0100=0000  1D5
0101=0000  200
0102=0000  620
0103=0000  10FF
0104=0000  73FE
0105=0000  18BF
0106=0000  9900
0107=0000  72E
0108=0000  73F8
```

how to use your GA-16/220

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RECORD OF REVISIONS

Title: How To Use Your GA-16/220

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Oct 79	Original Issue

FOREWORD

The following documents, pertinent to the operation and configuration of the GA-16/220, may be referenced for additional information.

Document Number	Title
88A00508A	GA-16/110/220 System Reference Manual
88A00509A	GA-16/110/220 Maintenance Manual
94A01519A	Reference Manual for Peripheral T&Vs on GA Series
94A01531A	GA-16/220/330 Stand-Alone Utilities Manual
94A01555A	System Generation and Operator Interface for RTOS, RTX or DBOS on a GA-16/220
94A01563A	System Generation and Operator Interface for FSOS on a GA-16/220

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introduction 1

The purpose of this document is to briefly describe the configuration and operation of the GA-16/220 Computer System to the new user.

This document presents the information required to install and bring the GA-16/220 to a fully-operational state. The user should also read the applicable reference manuals and documentation for the individual system.

To avoid delays and possible damage to the hardware, the installation and start-up procedure presented herein must be followed.

system configuration 2

2.1 HARDWARE OVERVIEW

Current production models of the GA-16/110/220 may use either the Jumbo or Compact chassis. (Refer to Appendix A for early configuration system drawings.) Figures 2-1 through 2-4 show the Jumbo and Compact Chassis and identify circuit board slots and major assemblies.

2.1.1 CPU-1 MODULE

The CPU-1 Module (Figures 2-5, 2-6 and 2-7), the heart of the GA-16/220, is a high-speed, microprogrammed LSI microprocessor. The CPU-1 module contains a CROM/RALU chip set that provides the arithmetic and logical operation capabilities of the processor and the microcode instructions.

2.1.2 CPU-2 MODULE

The CPU-2 Module (Figures 2-8 and 2-9) contains the Direct Memory Access (DMA) port, a Serial I/O Controller for a CRT/TTY, the one millisecond (1ms) Real-Time Clock, the console interrupt logic, and mini-rocker type manual data entry switches.

2.1.3 MEMORY BOARDS

The GA-16/220 computer may be equipped with several types of memory modules (circuit boards). The standard memory module is a dynamic random-access (RAM) memory of 4K, 8K or 16K capacity (see Figures 2-10 and 2-11). The 4K, 8K and 16K modules are identical in size and have a similar switch and indicator configuration; Figure 2-11 shows the address switch configuration. Memory modules are available in the conventional 16-bit word length or in an 18-bit word length for parity error detection (usually used in conjunction with a Memory Parity Protect Module). A Parity Override switch is provided to disable parity error detection, if desired.

NOTE

> If parity override is not enabled, a parity
> error will result in a stall condition on
> data fetches or a repeated attempt to execute
> instruction with instruction fetches. Indicator
> lights DERR and IERR are provided to indicate
> these conditions and are operative if Memory
> Parity Protect (MPP) is not installed.

In addition to the standard memory, PROM/RAM boards are available as piggyback-mounted options on the CPU-1 Module (see Figure 2-6). The standard piggyback is a 2K static RAM that is set for a start address of 0 or 8K by strapping on the piggyback assembly. (The dynamic RAM requires a periodic refresh write cycle or memory contents are lost; the static RAM does not require the refresh.)

Because RAM memories are solid-state, they require continuous power in order to hold their contents. To ensure that power is maintained, a battery back-up power supply consisting of a rechargeable battery pack and a battery charger may be installed; and an external battery may be connected across the battery pack. If no battery back-up supply is installed, a memory service module (MSM) must be installed in the J-21 connector (Compact Chassis) or the J-28 Connector (Jumbo Chassis) at the rear of the Master Interconnect Board (MIB).

Slide switches on the memory board front edge (refer ahead to Figures 3-2 and 3-3) must be set to provide contiguous address boundaries for the memory boards. The 4K module can be set to beginning addresses on any 4K boundary up to 60K, the 8K module can be set on 8K boundaries up to 56K, and the 16K module can be set on boundaries to 48K.

Figure 2-11 contains a core map that shows how the slide switches are used to set address boundaries.

NOTE

The conventions shown in Figure 2-11 are
typical of core map representations
throughout this manual. Low addresses
are shown at the bottom and high addresses
at the top. Unless otherwise specified,
locations on core map are in hexadecimal
numbering system. Hexadecimal locations
in text will always be represented as
X'nnnn' which corresponds to the CAP-16
assembler convention for defining a hexa-
decimal number.

The jumbo chassis in Figure 3-3 is shown with four 16K memory boards. The
address switches, ㉜ and ㉝ , are shown set for contiguous boundaries, as
follows:

START
ADDR

Board in J13 = 00 to 16K
          J14 = 16K to 32K
          J15 = 32K to 48K
          J16 = 48K to 64K

In general, memory must be contiguous from zero and addresses must be provided
from X'0040' through X'007F' for the vectored interrupt system to work
properly. All address assignments are completely independent of the physical
location of the memory module within the CPU chassis.

Contiguous memory space cannot be achieved with an odd number of 4K memory
modules unless these modules are paired to make 8K blocks with the odd module
assigned to the highest address block in the system.

In like manner, the user of the 2K piggyback memory module cannot provide
contiguous memory when combined with a single 4K module or when placed in a
system with more than 8K of memory (other than piggyback). This situation is
due to the fact that the piggyback memory is limited to starting addresss of
either zero or 8K.

Other types of memories that may be installed in a GA-16/220 system include
preprogrammed read-only-memories; or a combination of ROM and RAM configured to
a user's requirements. In addition to the 2K static RAM, a 64-word IPL ROM
(refer to Figure 2-6) may also be installed on the piggyback module; however,
the 64-word IPL ROM is not used when the SCI is installed on the CPU-2 module
(refer to Figure 2-9).

2.1.4 MEMORY PARITY PROTECT (MPP) MODULE

The MPP module is an option which may be installed in a GA-16/220 system. The MPP provides the system programmer with the capability of protecting selected areas of memory from being changed by a CPU write operation (program protect) or by direct memory write from a DMA or MHSDC controller (DMA protect). The MPP module contains the indicators necessary for identifying memory protect violations, parity errors, and multiple errors. Parity error detection requires the violations, parity errors, and multiple errors. Parity error detection requires the installation of 18-bit memory modules. The MPP module also contains the logic necessary for initiating either a CPU stall condition or a program interrupt via vector X'42' when parity errors occur. The STALL switch is preset before the module is installed to select which action will occur.

For a detailed explanation of the MPP module, refer to the GA-16/110/220 System Reference Manual, Section 5.

2.1.5 CROM MODULE

A CROM module, 31D03005A can be used with the GA-16/220 to enhance the 220 operation when using GA-16/440 software. The CROM module is mounted on CPU-1 board, 31D02573A31, in a piggyback fashion, in the same manner as the RAM memory module (Figure 2-7). CPU-1 board, 31D02573A31 is available as a production item, or a 31D02573A01 CPU-1 board can be converted to the -31 version by installing an ECO (field modification is feasible). Early production models of the CPU-1 board were not assigned the 2573 number, and these boards can not be upgraded to accept the CROM module.

Installation of the CROM piggyback prevents use of the 2K RAM piggyback memory module but poses no other constraints. An installed CROM module is ready to operate, there are no switch settings (unless different capacity memory boards are used) and no software preparation. Although the basic 220 operates successfully with 440 software, using extended instruction software simulation, overhead penalties reduce system efficiency. The new CROM ensures optimum performance.

2-4

2.1.6 SYSTEM CONSOLE INTERFACE (SCI) MODULE *7C00* ~~~ *FC00* ~~~

The system console interface module (Figure 2-9), is an optional module which is plugged into the CPU-2 module. It contains a 256-word, random-access-memory (RAM) and a 512-word, read-only-memory (ROM) that provides an interactive utility program. This program, called the console ROM or SCI program, uses the teletype/CRT capabilities of the CPU-2 module. Using the SCI program, an operator at a TTY/CRT may perform a wide range of utility operations, including the following:

1. Display and change registers.

2. Display and change memory locations.

3. Reset I/O.

4. Step through a program in memory.

5. Start a program in memory.

6. Load or punch a binary program tape.

7. Set program traps.

8. Set program bias.

A detailed description of the SCI operator commands and system response is contained in the GA-16/110/220 System Reference Manual, Section 3.6. The controls and indicators on the SCI module are described in Table 3-3. The SCI module may also contain an Initial Program Load (IPL) ROM which is described in the following section.

2.1.7 IPL ROMS

GA offers, as normal options, the following Initial Program Load (IPL) ROMs:

1. Single-device IPL - This IPL runs on a dedicated GA-16/110 and mounts on a 2K piggyback memory. It is a complete, 64-word, mini PGS loader requiring no preamble on the media being loaded. It is an absolute, load-and-go binary loader with checksum.

     Version 1 - TTY

     Version 2 - High-speed, paper tape reader

2. Multi-device IPL - This IPL ROM is mounted on the GA-16/220 System Console Interface Module. It consists of a 256-word program which provides bootstrap loaders for the TTY, high-speed paper tape reader, card reader, floppy disk, moving arm disk (both fixed and removable platter), and head-per-track disk (refer to Table 3-4 for device select list). Each of these bootstrap loaders accesses its designated peripheral to bring a PGS loader into RAM. (The PGS loader must be in the zero sector of a disk or in the preamble of tapes and card decks.) The PGS loader then automatically loads the program and data which must be in the PGS format; i.e., relocatable with checksum and designated start address as described in Section 3.5.1 of the GA-16/110/220 System Reference Manual.

2.1.8 POWER SUPPLIES

Three types of power supply may be used with a GA-16/220 system.

1. A built-in supply, for use with self-contained systems, is installed in the compact chassis (Figure 2-3). This supply requires 115V, 47-63Hz input at 230 watts maximum. Its outputs are +5V at 8A (convection cooled) or 18A (fan cooled), +15V at 2A, and 15V at 1A.

2. An external supply, which is used for larger GA-16/220 systems, is installed with the jumbo chassis (Figure 2-2). (An external supply may also be used with a compact chassis, if desired.) The external supply input is 115V or 230V, 47-63Hz at 500 watts maximum. Outputs are +5V at 30A, +15V at 5A, and -15V at 5A.

3. Battery back-up power supply is used to supply ±5V and +12V to the memory modules (including the 2K piggyback memory), and to switch to batteries (to preserve the contents of memory) when the AC input power stops. A provision is available which permits using an external battery for a greater back-up life span. A manual cutoff switch (④⓪ in Figures 3-1 and 3-2) permits an operator to deliberately disconnect the battery supply; but only when AC power is off.

An indicator ㉟ monitors memory power. When battery back-up is not installed, a circuit board, designated the memory service module (MSM), must be

inserted in the J-21 or J-28 connector at the rear of the MIB chassis (Figures 2-2, 2-4, 3-1, and 3-2).

BATTERY BACK-UP   BATTERY BACK-UP   I/O EXPANSION
POWER SUPPLY   REGULATOR BOARD   MEMORY OR   CPU-1   CPU-2   I/O CONTROLLER   CABLE INTERFACE
                                               MPP   MODULE   MODULE   LOCATIONS   DRIVER (CID)
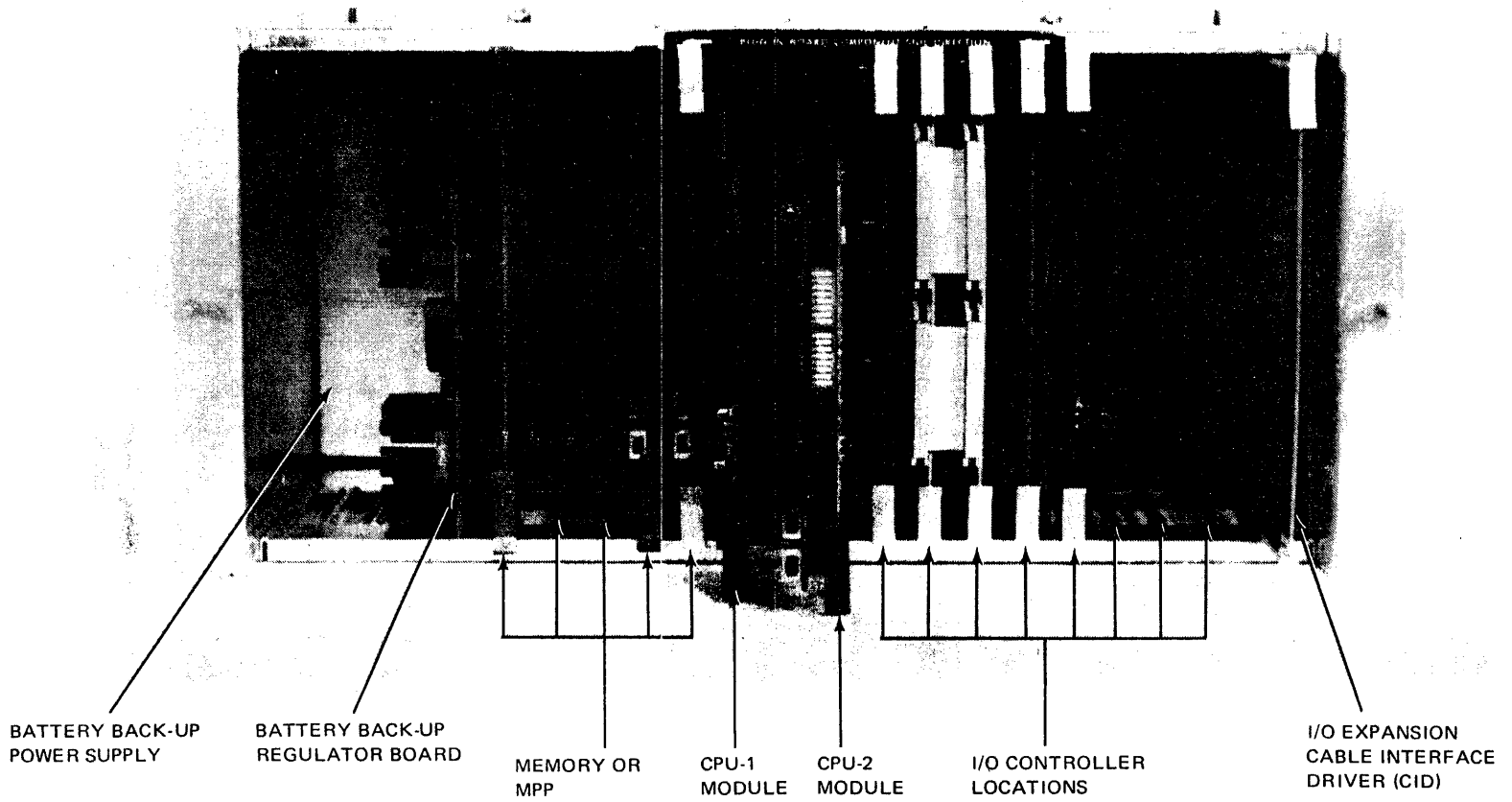
Figure 2-1.   Jumbo Chassis (Front View)
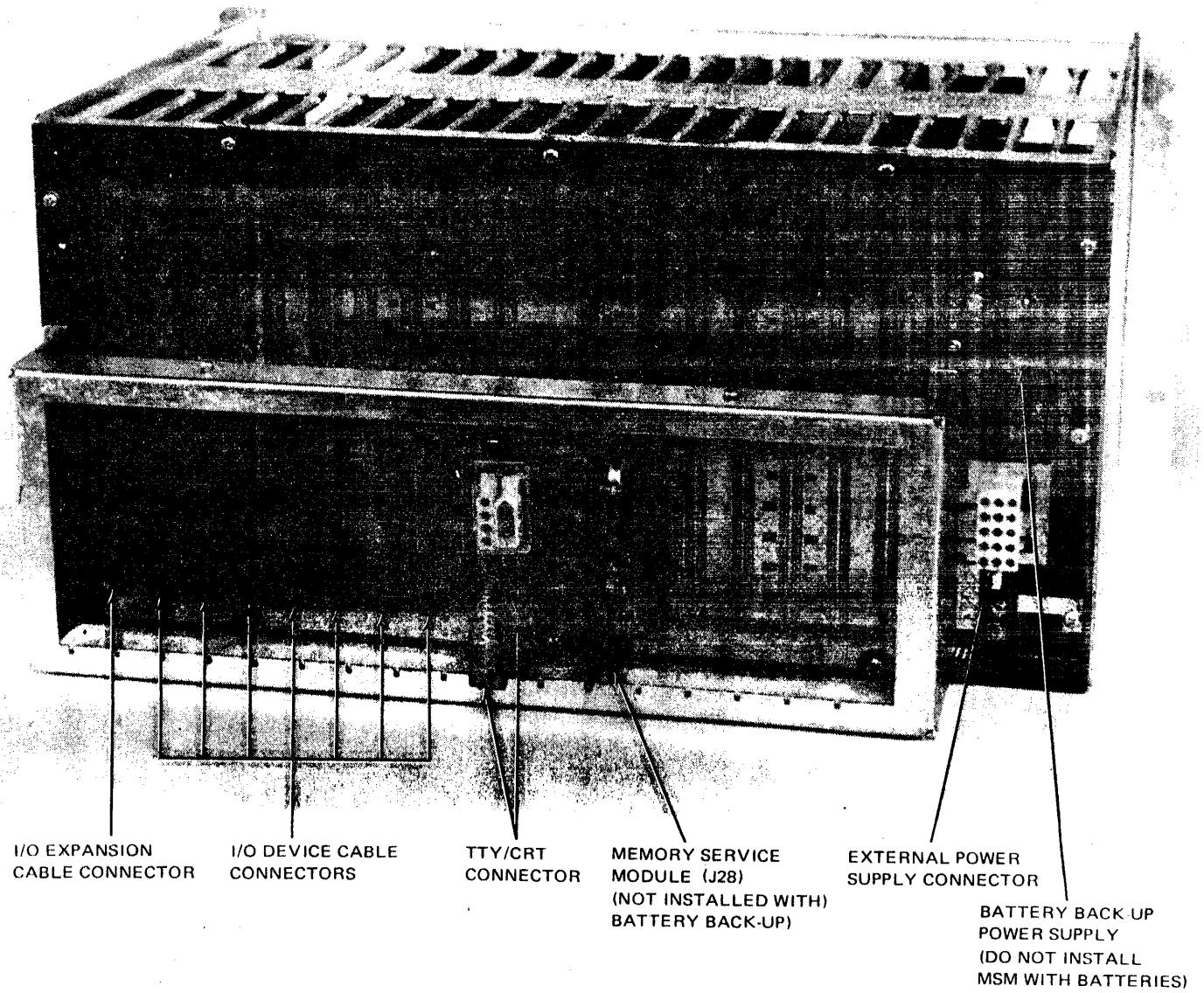
Figure 2-2. Jumbo Chassis (Rear View)

I/O EXPANSION
CABLE CONNECTOR

I/O DEVICE CABLE
CONNECTORS

TTY/CRT
CONNECTOR

MEMORY SERVICE
MODULE (J28)
(NOT INSTALLED WITH)
BATTERY BACK-UP)

EXTERNAL POWER
SUPPLY CONNECTOR

BATTERY BACK-UP
POWER SUPPLY
(DO NOT INSTALL
MSM WITH BATTERIES)

88A00525A-B
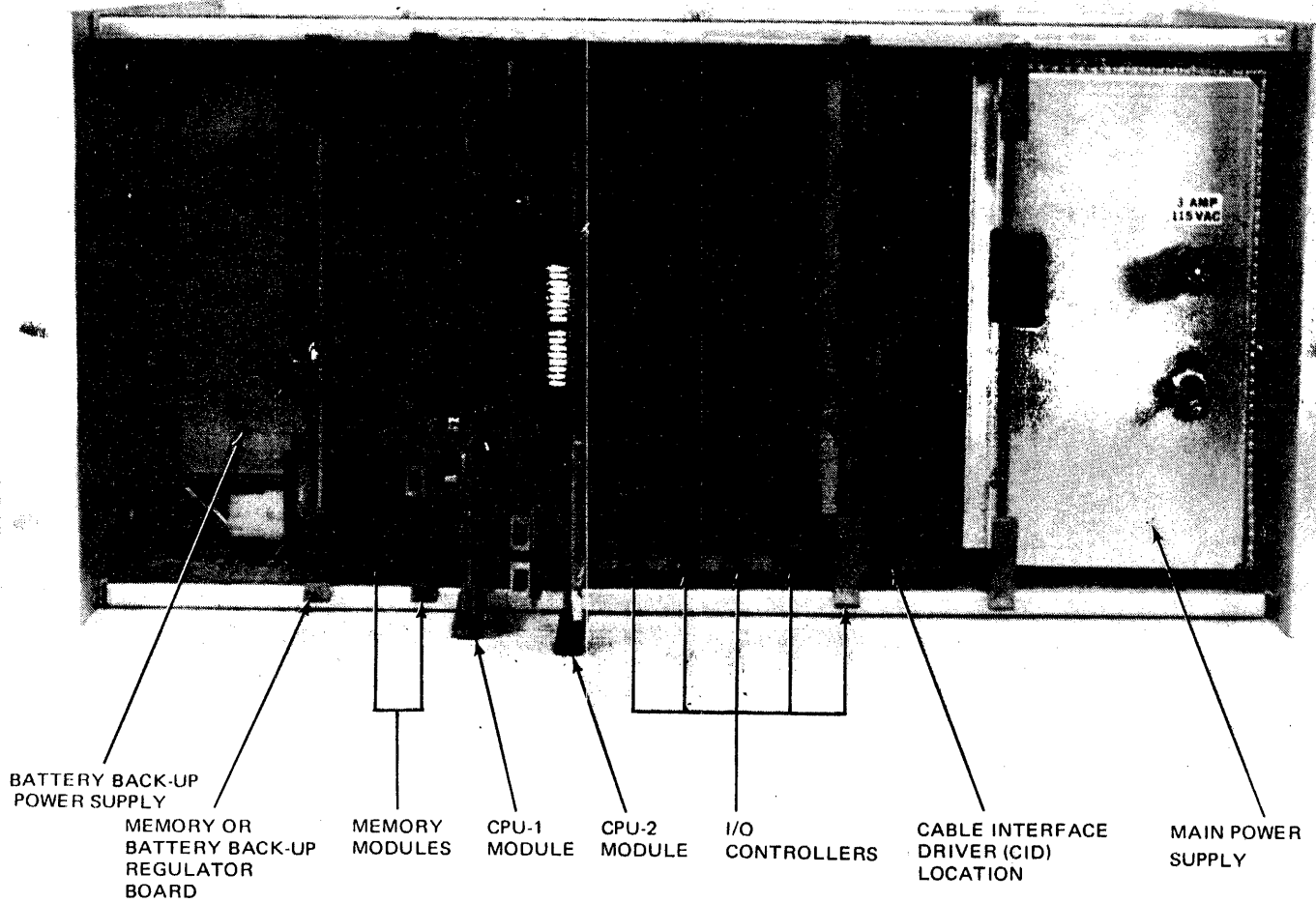
Figure 2-3. Compact Chassis (Front View)

2-10

A/C LINE   EXTERNAL POWER   I/O EXPANSION   TTY/CRT   AC LINE
CORD   SUPPLY CONNECTOR   CABLE CONNECTOR   CONNECTOR   CORD

     MAIN POWER   I/O DEVICE   BATTERY BACK-UP
     SUPPLY   CABLE CONNECTORS   POWER SUPPLY
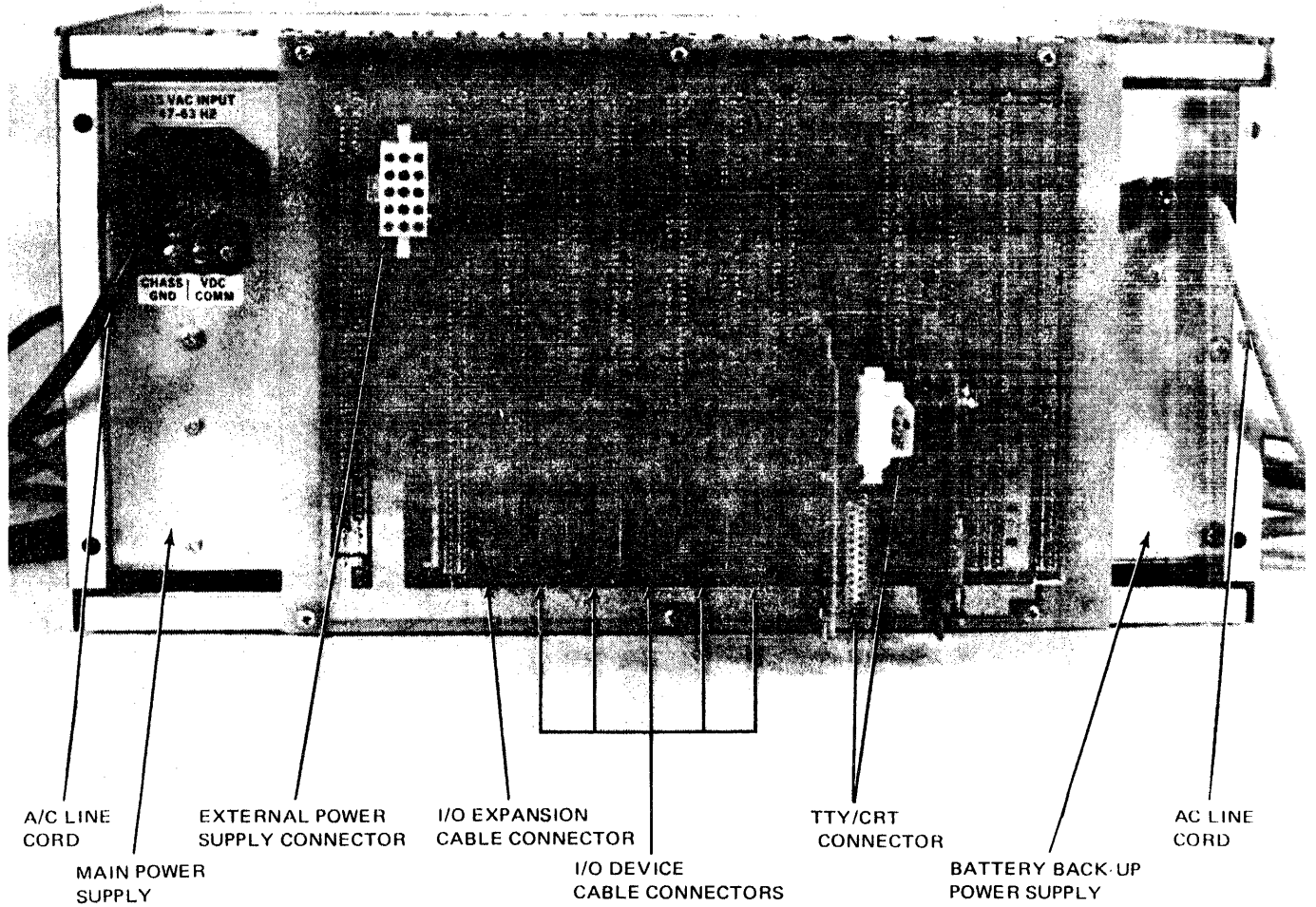
Figure 2-4. Compact Chassis (Rear View)
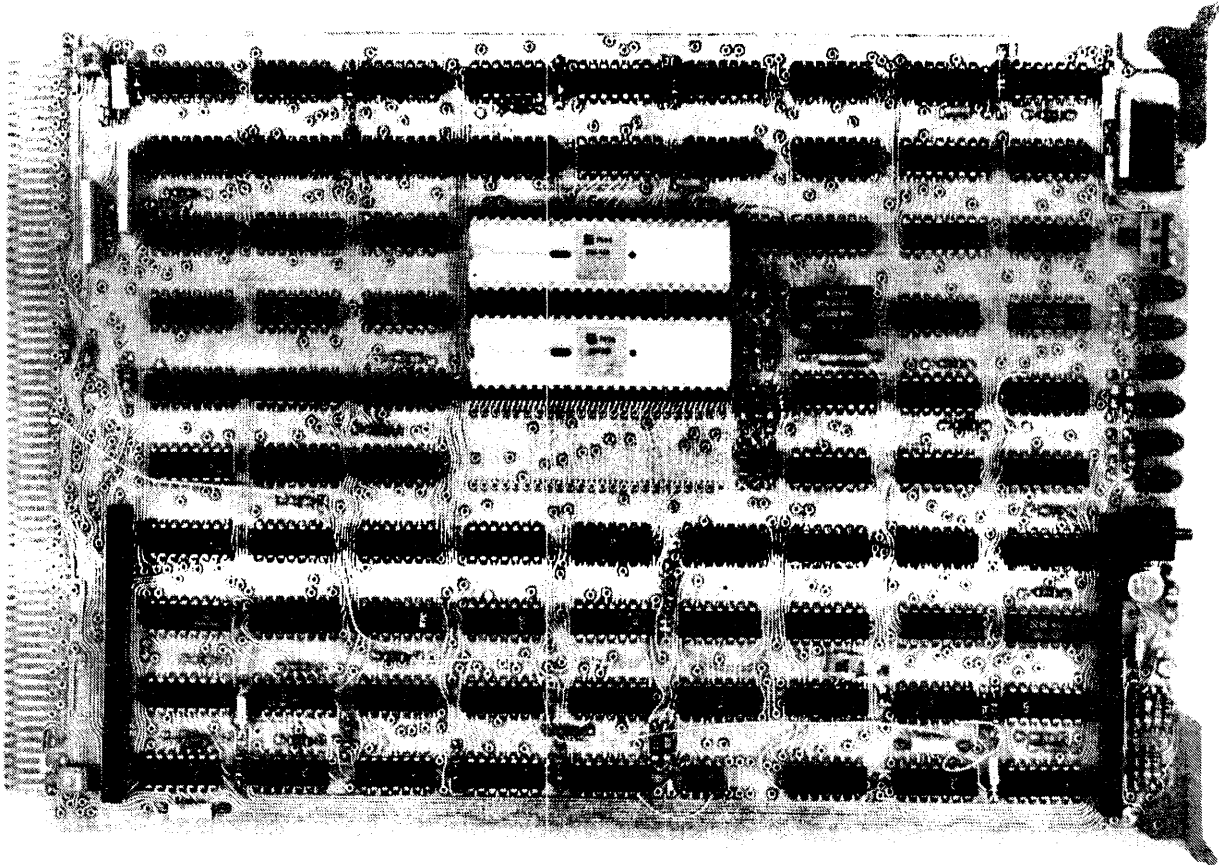
Figure 2-5. CPU-1 Module (Without Piggyback Module)
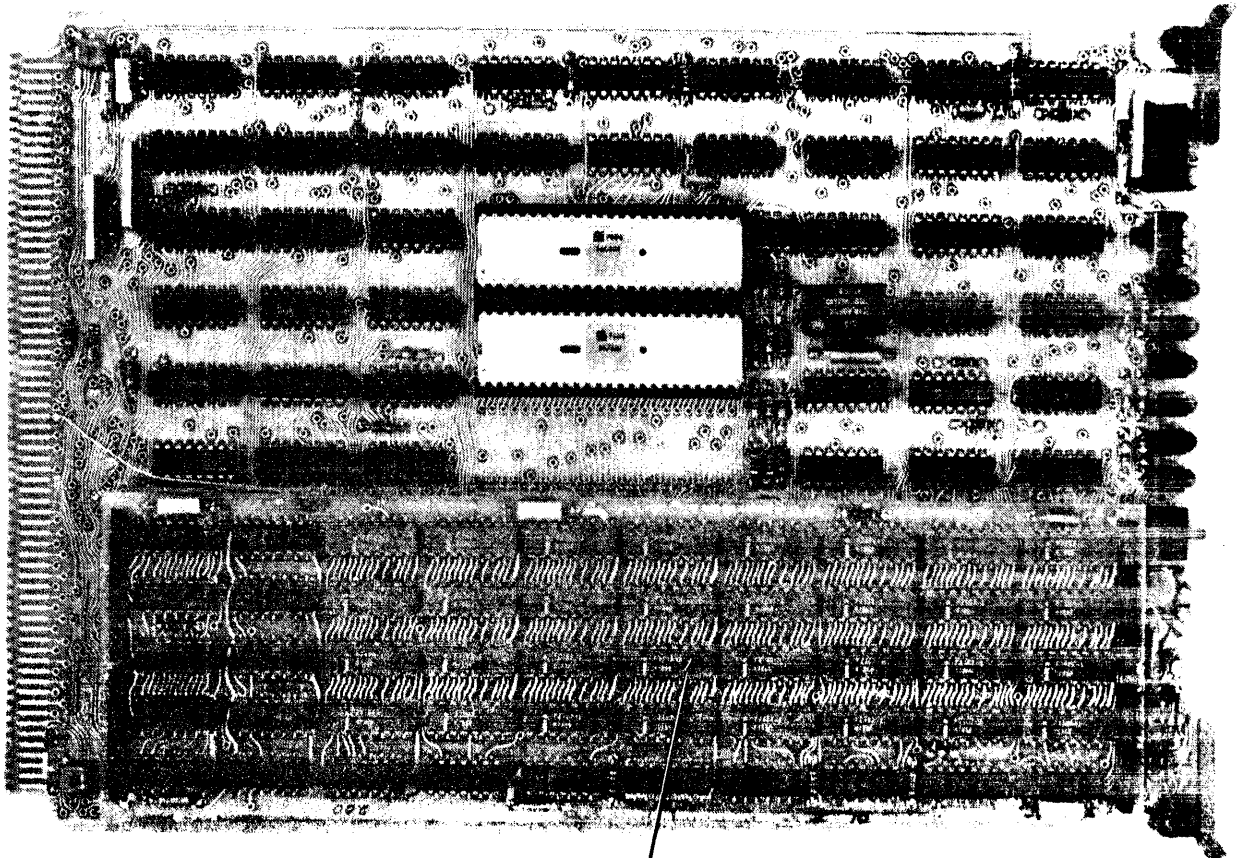
2K PIGGYBACK MEMORY

Figure 2-6. CPU-1 Module (With Piggyback Memory)
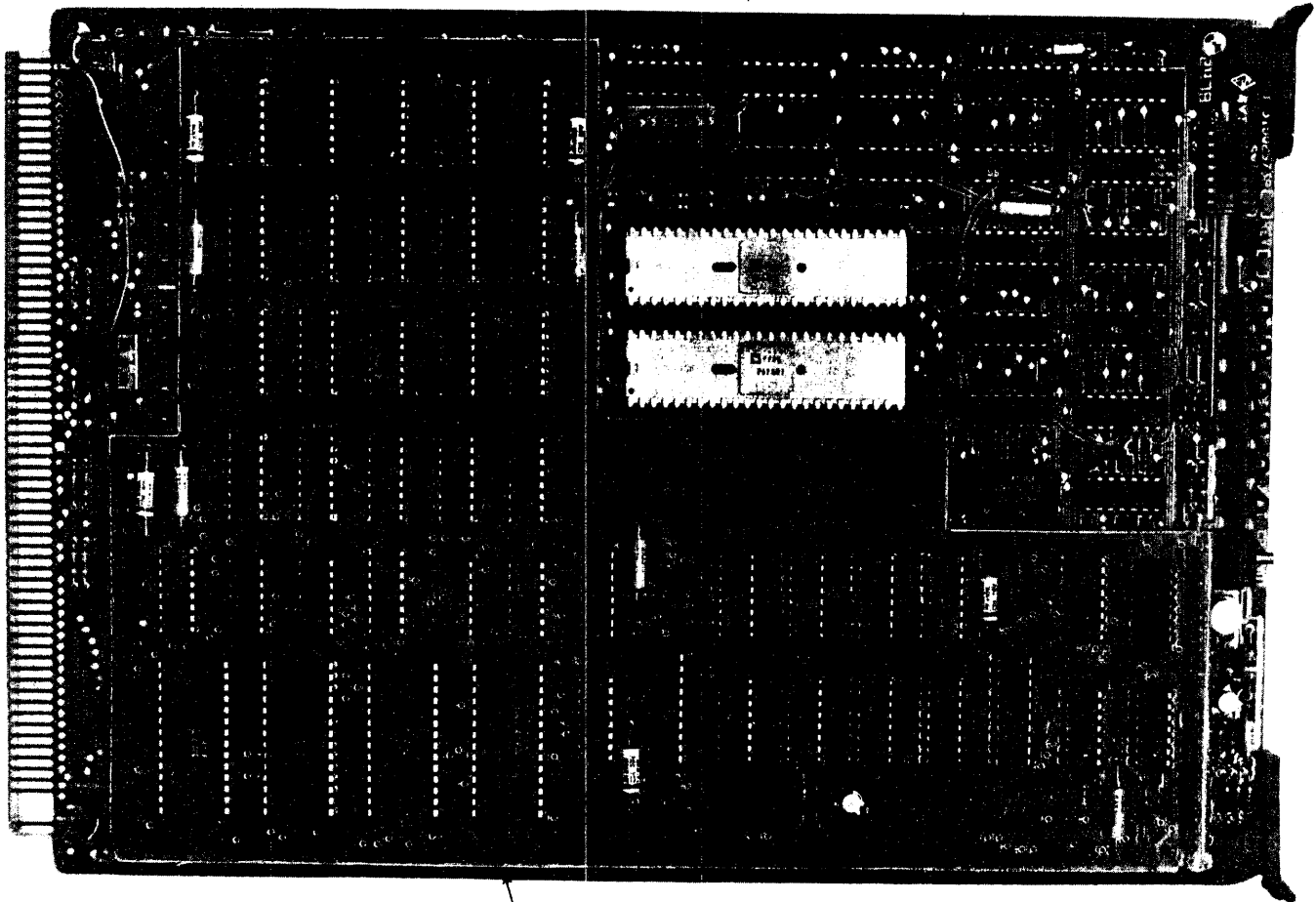
PIGGYBACK CROM MODULE

Figure 2-7.   CPU-1 Module 31D02573A31 (With Piggyback CROM)
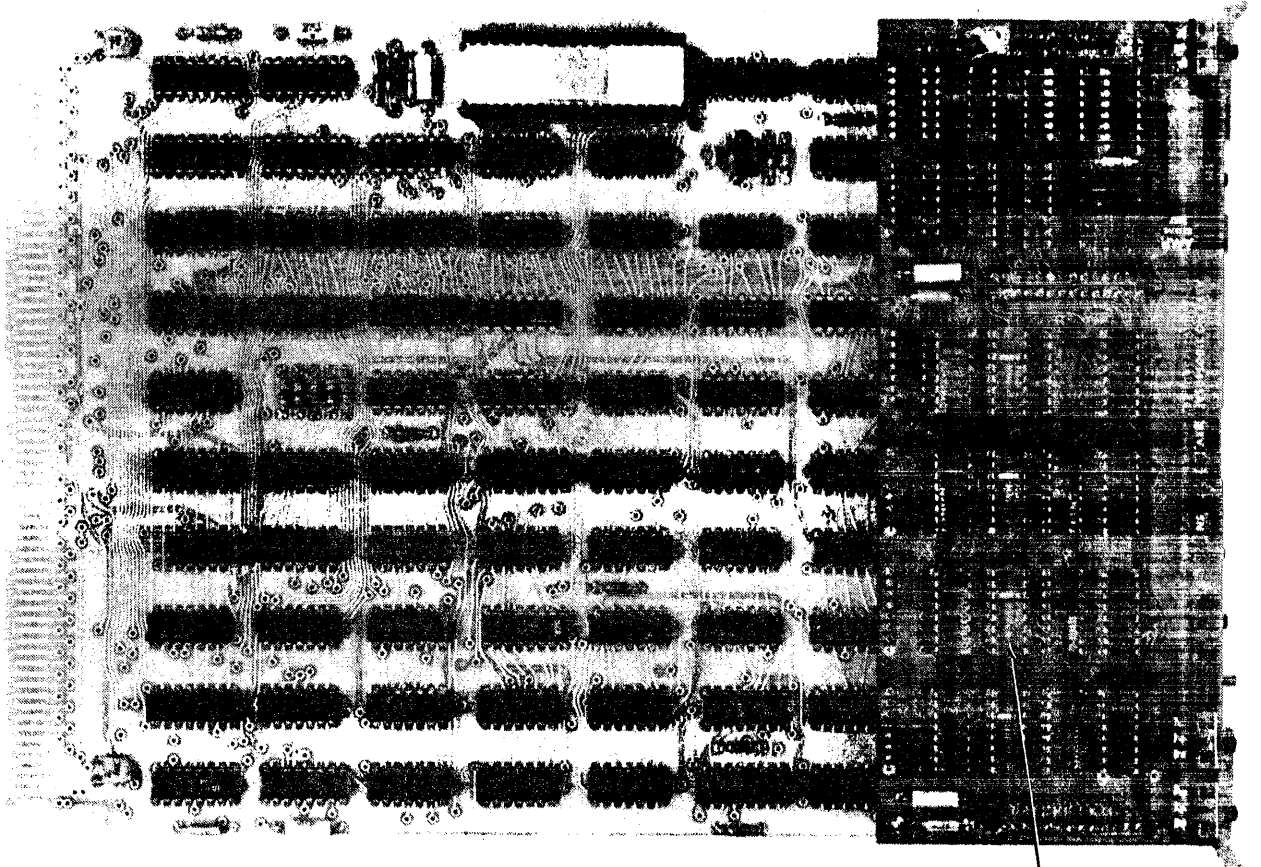
SYSTEMS CONSOLE INTERFACE (SCI)
WITH IPL

Figure 2-8. CPU-2 Module (Without SCI)
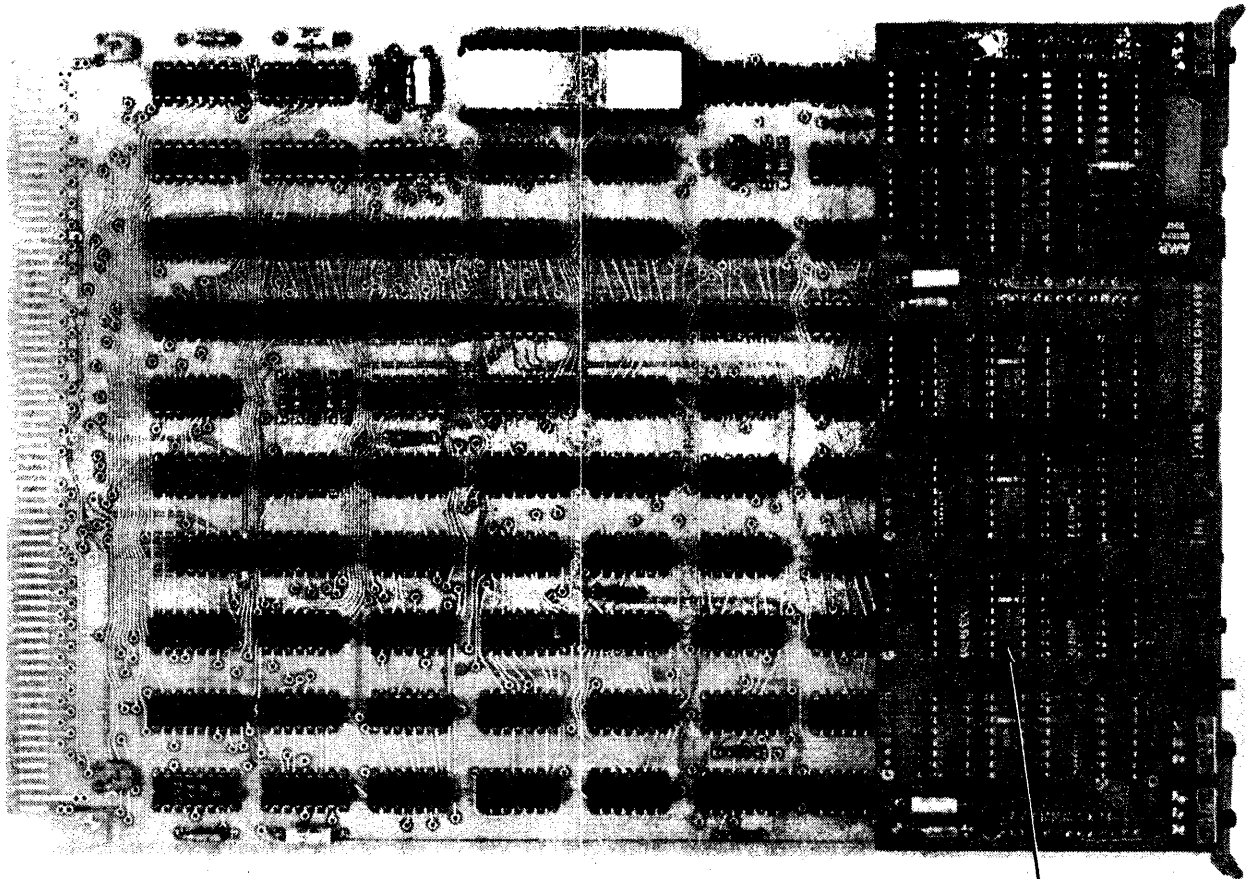
SYSTEMS CONSOLE INTERFACE (SCI)
WITH IPL

Figure 2-9. CPU-2 Module (With SCI)
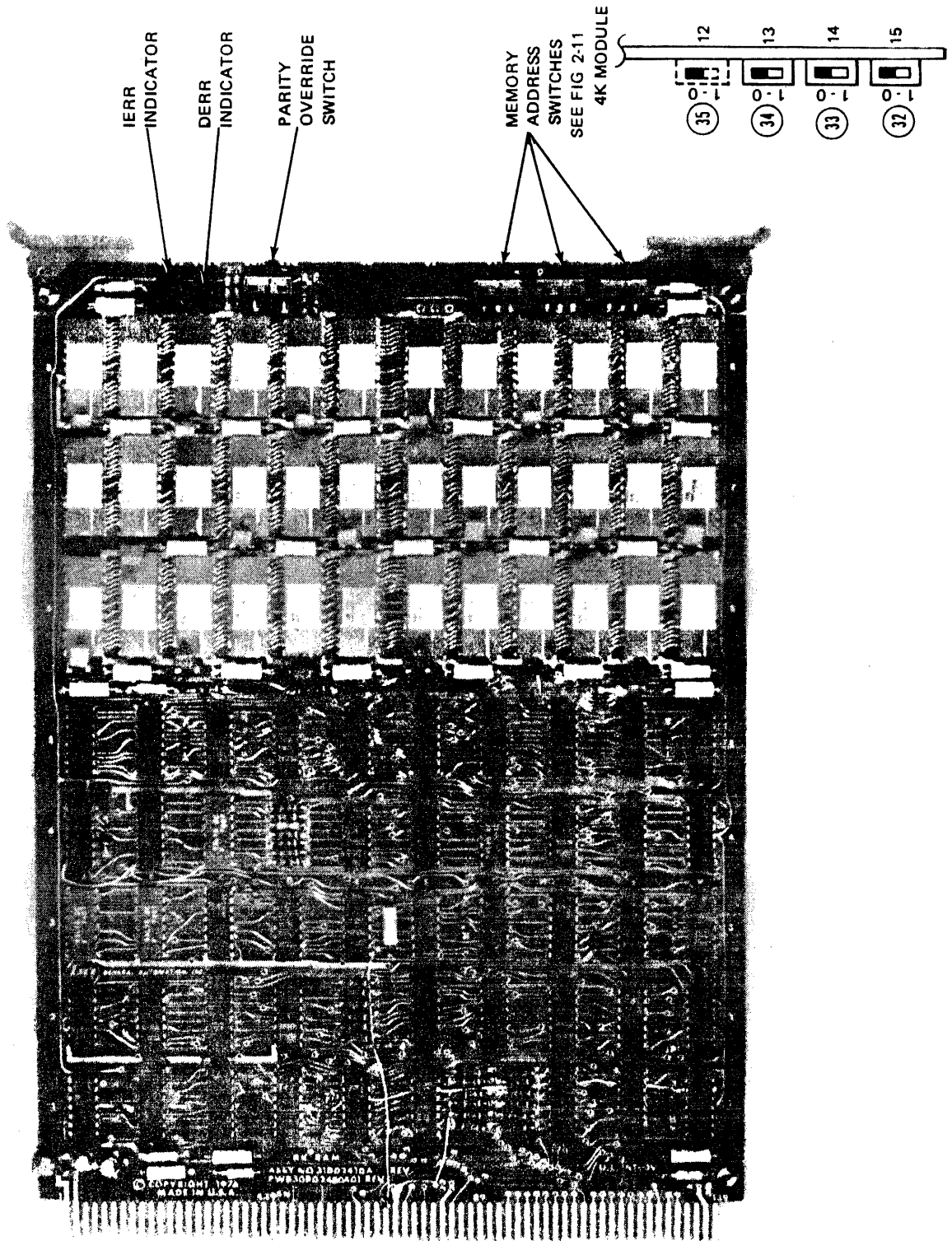
Figure 2-10.   8K Memory Board

	4K MEMORY SWITCHES	8K MEMORY SWITCHES	16K MEMORY SWITCHES
	35 12	34 13	
	34 13	33 14	
	33 14	32 15	33 14
	32 15		32 15

HEXADECIMAL ADDRESS

DECIMAL ADDRESS

HEX	DECIMAL	4K	8K	16K	
FFFF	65,535 (64K)	1	—	—	
		1			
		1			
F000	61,440	1			
EFFF	(60K)	0	1		
		1	1		
E000	57,344	1	1		
DFFF	57,343 (56K)	1			
		0			
D000	53,248	1			
CFFF	53,247 (52K)	0	0		12
		0	1	1	13
		1	1	1	14
C000	49,152	1			15
BFFF	49,151 (48K)	1			
		0			
B000	45,056	1			
AFFF	45,055 (44K)	0	1		
		1	0		
A000	40,960	0	1		
9FFF	40,959 (40K)	1			
		0			
		0			
9000	36,864	1			
8FFF	36,863 (36K)	0	0	0	12
		0	0	0	13
		1	1	1	14 15
8000	32,768	1			
7FFF	32,767 (32K)	1			
		1			
7000	28,672	0			
6FFF	28,671 (28K)	0	1		
		1	1		
6000	24,576	0	0		
5FFF	24,575 (24K)	1			
		0			
5000	20,480	0			
4FFF	20,479 (20K)	0	0	1	12 13 14
		1	1		15
4000	16,384	0	0	0	
3FFF	16,383 (16K)	1			
		1			
		0			
3000		0			
2FFF	(12K)	0	1		
		1	0		
2000	8192	0			
1FFF	8191 (8K)	1			
		0			
1000	4096	0			
0FFF	4095 (4K)	0	0	0	12 13 14
0400		0	0	0	
0000	1024	0	0	0	15

Figure 2-11. Memory Address Map (Sheet 1 of 2)

NOTES:

1   Each small division represents 400 hexadecimal (X'400') or 1024 decimal (in common terminology, 1K) words of memory.

2   4K boundaries are represented by dashed lines.

3   8K boundaries are represented by solid lines.

4   Hexadecimal and decimal addresses shown specify both lower and upper addresses of each 4K block of memory.

5   The decimal number in parenthesis represents the commonly used terminology for defining memory capacity (i.e., a 16K system actually has 16,384 words, or an addressing range from 0 through 16,383 words, decimal; or X'0' through X'3FFF' when expressed in hexadecimal).

6   Memory switch settings are shown in the order they appear on the memory module, top to bottom. As shown in Figures 3-2 and 3-3) The up position of the switch is 1.

7   Memory addresses X'00' through X'C1' are dedicated to the interrupt vector locations or are reserved for Series 16 operating systems which may be used.

8   On a GA-16/220, the upper 1K of each memory mode, locations X'7C00' through X'7FFF' when in 32K mode or locations X'FC00' through X'FFFF' when in 64Kmode, is reserved for the SCI Console ROM and IPL ROM. These locations are independent of the amount of memory implemented by memory modules; however, if a memory module is set to include the reserved locations , those locations are not usable by that memory module.

9   A 2K static RAM and a 64-word IPL ROM may be installed on the CPU-1 board. This memory, also referred to as the "piggyback" memory, physically occupies the first 2K of memory +64 words or 2K of memory beginning at the 8K boundary (set by jumpers). The static RAM memory module may not be set to a boundary which includes the locations of the piggyback memory.

Figure 2-11. Memory Address Map (Sheet 2 of 2)
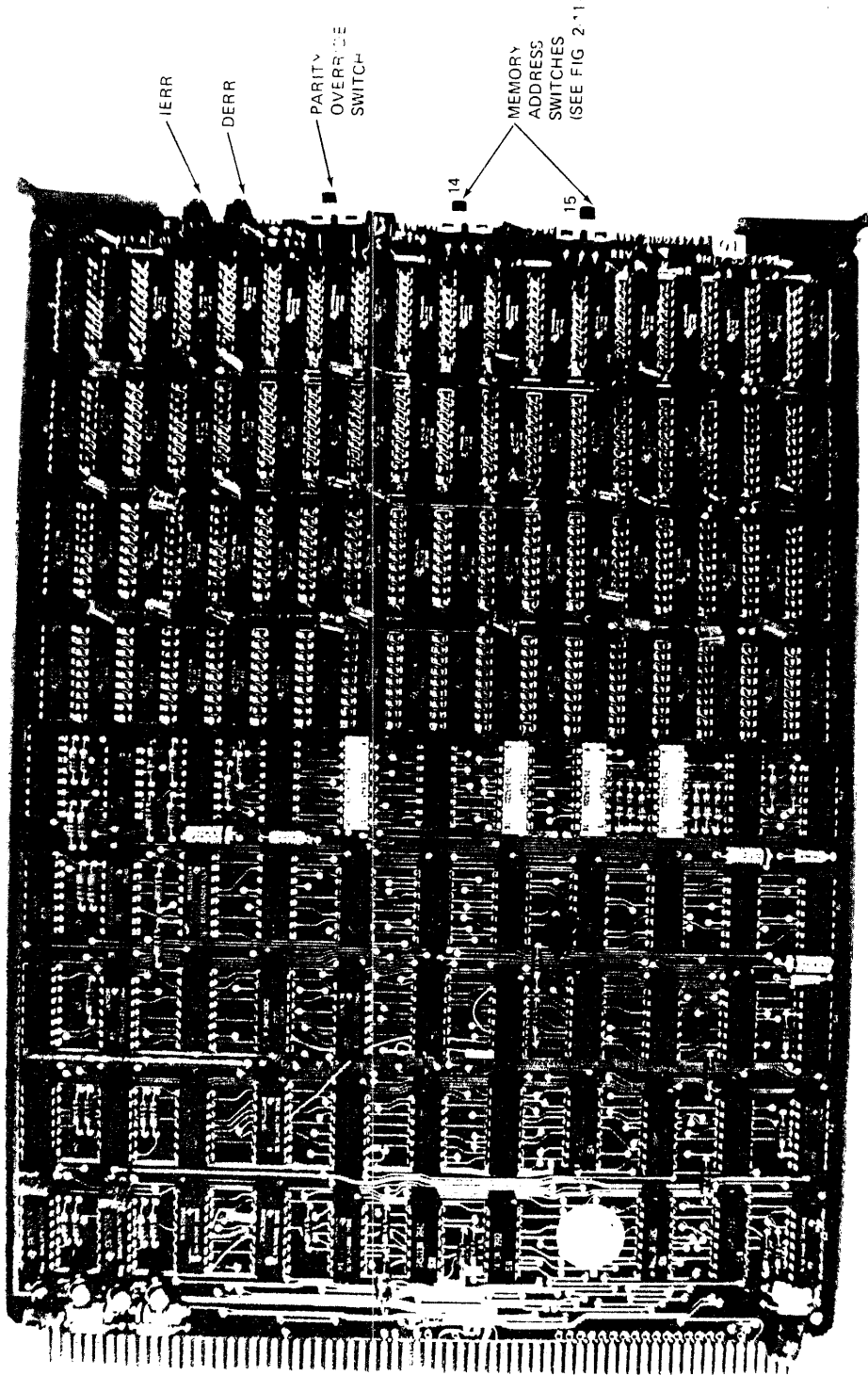
Figure 2-12.   16K Memory Board

start-up procedure 3

This start-up procedure applies to a GA-16/220 system having a System Console Interface (SCI) module, a minimum of 8K of memory, and a TTY or CRT operator input/output device. For operating procedures for systems having configurations other than stated here, refer to the special documentation supplied with the individual system.

NOTE

To load the CPU Test and Verify (T&V) program (referenced later in this document) a TTY, with a paper tape reader, or a high-speed paper tape reader must be installed in the system.

CAUTION

DO NOT APPLY PRIMARY POWER UNTIL INSTALLATION OF COMPONENT PARTS IS VERIFIED AS CORRECT.

3.1 MODULE (BOARD) INSTALLATION

Prior to applying primary power to the GA-16/220, verify that all the individual boards (CPU, memory, I/O controllers, etc.), are correctly installed in the chassis as shown in Figures 3-1 or 3-2 (or Appendix A). A correctly seated board will be completely vertical (no skew) and solid in its connector on the Master Interconnect Board (MIB).

All modules must have the COMPONENT SIDE TO THE LEFT (when viewed from the front) to avoid possible damage to the board.

3.2 SWITCH SETTINGS

Table 3-3 contains descriptions of the controls and indicators for the GA-16/220 system. Th user must gain familiarity with a few "key" controls and indicators to make the system operational (i.e., execute the CPU T&V). These key switch settings are described in Section 3.2.2. For more sophisticated operation, or maintenance, the user should be familiar with all controls and indicators.

3.2.1 SWITCH AND INDICATOR CONFIGURATION

The switches and indicators are shown on Figures 3-1, 3-2 and 3-3. Switch and indicator configuration on the CPU-1 and CPU-2 boards will depend upon the type of CPU boards that are installed. There is a difference between the early model CPU-1 and CPU-2 boards and the later model boards. The late model CPU-1 and CPU-2 boards, 31D02573A and 31D02574A, embody the following changes:

● CPU-1 (31D02573A) - The Battery Backup Power Supply Switch ㉓ faces the rear of the board and is located between board coordinates D1 and E1. On the 31D02573A CPU-1 board, the backup power supply position on this switch is UP. This switch must be set in the backup power supply position if a battery backup supply is installed. If a battery backup power supply is not installed, this switch must be set in the DOWN position. (It is important that the user distinquish between the late model 31D02573A CPU-1 board and the early model boards having numbers 31D02274A and 31D02422A.) In the early model CPU-1 boards, the backup power supply switch must be in the UP position if a backup supply is not installed and in the DOWN position if it is installed.

CAUTION

If AC power is off with the backup power supply in the main power supply position and a battery backup supply is installed, the battery will drive the main +5V CPU circuit. The result: a rapidly discharged battery and possible damage to the backplane etch.

● CPU-2 (31D02574A) - a. A rotary hex-position switch ⚠2 selects 1 of 15 available baud rates for serial I/O devices.
   b. A STOP BIT select switch ⚠1 selects a one- or a two-bit "STOP BIT" for serial I/O. Unless otherwise specified, the STOP BIT switch should be in the DOWN position to select a two-bit "STOP BIT".
   c. The TTY BAUD, 9600, and 110 (⑧, ⑨, and ⑩) baud rate controls described for the early model CPU-2 board are not present on the late model 31D02574A board.

Figures 3-2 and 3-3 show the complete switch and indicator configuration for a GA-16/220 with early model CPU boards. Figure 3-1 shows the switch and indicator configuration for the late model CPU-1 and CPU-2 boards.

Figures 3-2 and 3-3 show 8K memory boards; each 8K board has three address boundary switches. The number of address boundary switches on a memory board depends upon the board capacity. This is demonstrated in Figure 2-11.

POWER-ON OR RESET BUTTON GOES TO CNSL ROM

(15) RESET SELECTOR

POWER-ON OR RESET BUTTON INTERRUPTS TO X'41', OR IF COLD START GROUNDED

BAUD RATE SELECT OR (2)

1 BIT
STOP BIT   TYPICALLY IN DOWN POSITION
2 BIT   (1)

(23)

ALSO REFER TO SEC 3.2.2

BACK-UP PS SWITCH (REAR OF BOARD)

BACK-UP PS

MAIN PS

IPL SELECTOR (14)

(22) WAIT

(21) RUN

(20) FOREGROUND/ BACKGROUND MODE

(19) STALL/PMA

(18) INTERRUPT STATUS

(17) INTERRUPT ACKNOWLEDGE

(16) RESET

DMA (7)

DATA SWITCHES (6) (5)

CONSOLE INTERRUPT TO X'47'

PROGRAMMED

32K/64K MODE

32K

BREAK RESETS CPU (NOT I/O) AND GOES TO CNSL ROM

(12) BREAK MODE SELECTOR

BREAK INTERRUPTS TO X'46'

IPL (AUTOLOAD) (13)

ENABLE

TTY/CRT BREAK DISABLE (11)

DISABLE

110 BOARD (CPU-1)

220 BOARD (CPU-2)

SYSTEM CONSOLE INTERFACE

(2) BAUD SELECT SETTINGS

SWITCH SETTING	BAUD RATE	SWITCH SETTING	BAUD RATE
0	NOT USED	9	1200
1	50	A	1800
2	75	B	2400
3	110	C	3600
4	134.5	D	4800
5	150	E	7200
6	300	F	9600
7	600		
8	900		

(1) PLACE IN DOWN POSITION TO SELECT 2-BIT STOP BIT WHEN USING A TTY OR MOST OTHER SERIAL I/O DEVICES.

Figure 3-1.   Late Model CPU Boards, 31D02573A and 31D02574A

Figure 3-2. GA-16/220 System in Compact Chassis (No NPP)

3-4

88A00525A-B

TERMINALS FOR
EXTERNAL 12
VOLT BATTERY
(ON REAR)

MEMORY SERVICE
MODULE (IF
BACKUP POWER
SUPPLY NOT USED)

TO SERIAL I/O
AND REMOTE
CONTROL
LINES

TO FLOPPY
DISK UNIT

TO CABLE
INTERFACE
TRANSLATOR
(CIT) IN I/O
EXPANSION
CHASSIS
(IF USED)

AC CABLE TO
BACKUP POWER
SUPPLY

CONNECTOR FOR OPTIONAL
EXTERNAL POWER SUPPLY

AC CABLE TO MAIN
POWER SUPPLY

J21   J20 J19   J18   J17 J16   J15   J14   J13

J12   J11   J10   J9   J8   J7   J6   J5   J4   J3   J2   J1

BATTERY
PACK

MAIN POWER SUPPLY

SYSTEM GROUND
TERMINALS
(ON REAR)

FUSE

CPU SECTION   I/O SECTION

SEE APPENDIX G FOR CPU2 BOARD 31D02574A

SWITCHES AND INDICATORS ON
CPU-1 AND CPU-2 ARE FOR EARLY
MODEL BOARDS. FIGURE 3-1
SHOWS LATE MODEL CPU-1
(31D02573A)
AND CPU-2 (31D02574A) BOARDS.

Table 3-1. Connector Assignments for Compact Chassis Computer System

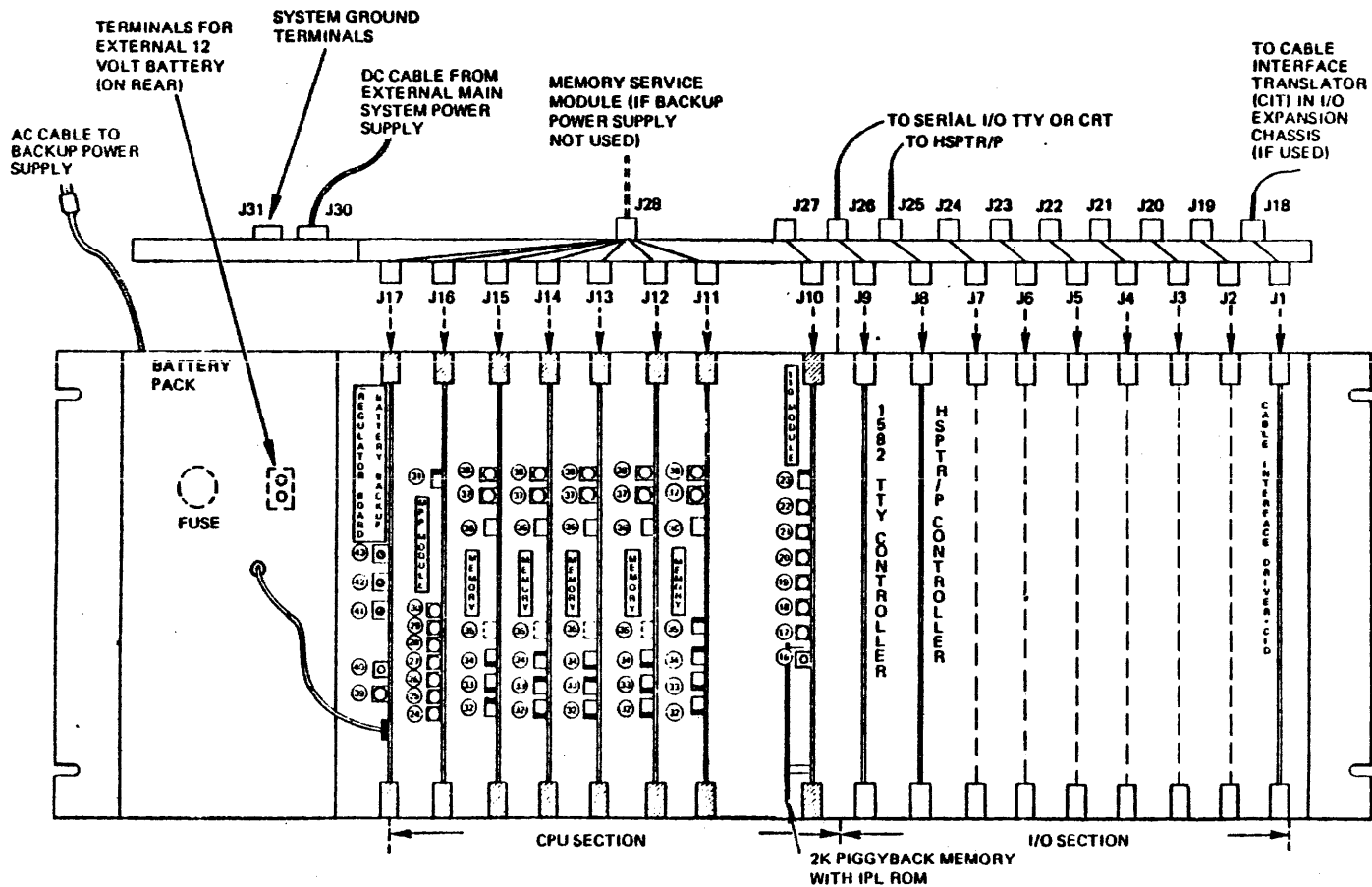| Front/Module (220)		Rear/Interface (220)	
J1	Main power supply	–	AC input connector and system grounding terminals on power supply.
J2	Cable Interface Driver (CID)		
J3, J4	I/O controllers or shorting boards.	J13	Connector for optional external power supply cable.
J5, J6	Shorting boards are used in empty slots between controllers or CID to maintain interrupt chain continuity.	J14	Cable to I/O expansion chassis (6-foot maximum).
J7	MHSDC controller, if used, should go into J7.	J15, J16, J17, J18, J19	Paddleboards and cables interfacing controllers (in J3 through J7) to peripheral devices.
J8	CPU-2 module with optional System Console Interface.	J20	Serial I/O paddleboard with connector to TTY or CRT also provides access to cold-start (CLDS-) jumpers and remote control lines (IPLSW-, PFD-, RSET-, RUN-).
J9	CPU-1 module with optional piggyback memory.		
J10, J12	Memory module, DMT controller, or Memory Parity Protect module. J12 also used for battery backup regulator board.	J21	Memory Service Module if battery backup power supply is not used. J21 also may be used as interface for external DMT controller.
–	Backup power supply battery pack (use regulator board in J12).	–	AC cord for backup power supply.
		–	Terminals for external 12-volt battery on rear of battery pack.

Figure 3-3. GA-16/220 System in Jumbo Chasis (With MPP)

3-6

88A00525A-B

TERMINALS FOR
EXTERNAL 12
VOLT BATTERY
(ON REAR)

SYSTEM GROUND
TERMINALS

DC CABLE FROM
EXTERNAL MAIN
SYSTEM POWER
SUPPLY

MEMORY SERVICE
MODULE (IF BACKUP
POWER SUPPLY
NOT USED)

TO SERIAL I/O TTY OR CRT
TO HSPTR/P

TO CABLE
INTERFACE
TRANSLATOR
(CIT) IN I/O
EXPANSION
CHASSIS
(IF USED)

AC CABLE TO
BACKUP POWER
SUPPLY

J31   J30   J28   J27 J26 J25 J24 J23 J22 J21 J20 J19 J18

J17 J16 J15 J14 J13 J12 J11   J10 J9 J8 J7 J6 J5 J4 J3 J2 J1

BATTERY
PACK

FUSE

REGULATOR BOARD
BATTERY BACKUP

1/O MODULE

1582 TTY CONTROLLER

HSPTR/P CONTROLLER

CABLE INTERFACE DRIVER (CID)

CPU SECTION   I/O SECTION

2K PIGGYBACK MEMORY
WITH IPL ROM

SWITCHES AND INDICATORS ON
CPU-1 AND CPU-2 ARE FOR EARLY
MODEL BOARDS. FIGURE 3-1
SHOWS LATE MODEL CPU-1 (31D02673A)
AND CPU-2 (31D02574A) BOARDS

Table 3-2. Connector Assignments for Jumbo Chassis Computer System

Front/Module (220)		Rear/Interface (220)	
J1	Cable Interface Driver (CID).	J18	Cable to I/O expansion chassis (6-foot maximum).
J2 J3	I/O controllers or shorting boards.	J19 J20 J21 J22 J23 J24 J25 J26	Paddleboards and cables interfacing I/O controllers (in J2 thru J9) to peripheral devices.
J4 J5 J6 J7	Shorting boards are used in empty slots between controllers or CID to maintain interrupt chain continuity.		
J8 J9	MHSDC controller, if used, should go into J9.		
		J27	Serial I/O paddleboard with connector for TTY or CRT. Also provides access to cold-start (CLDS-) jumper, and remote control lines (IPLSW-, PFD-, RSET-, RUN-).
J10	CPU-2 module with optional System Console Interface.		
J11	CPU-1 module with optional piggy-back memory.		
J12 J13	Memory module, DMT controller or Memory Parity Protect module.	J28	Memory Service Module if battery backup power supply is not used. J28 also may be used as interface for external DMT controller.
J14 J15 J16 J17	J17 also used for battery backup regulator board.		
		J30	Power cable from external power supply.
-	Backup power supply battery pack (use regulator board in J17).	J31	System grounding terminals.
		-	AC cord for backup power supply.
		-	Terminals for external 12-volt battery on rear of battery pack.

Table 3-3. GA-16/220 Controls and Indicators (Sheet 1 of 7)

Key	Label	Description and Function
△1	STOP BIT Figure 3-1 Only	Selects one- or two-bit "STOP BIT" for serial I/O. A two-bit "STOP BIT" (switch in DOWN position) must be selected for TTY and most other serial I/O devices.
△2	BAUD RATE SELECTOR Figure 3-1 Only	Selects 1 of 16 available baud rates for serial I/O. Refer to Figure 3-1. 110 baud should be selected for the TTY.
①(PS)	ON OFF	The main power switch causes power to be applied to CPU and I/O controllers. Power is also applied to memory modules, memory service module is installed.
②(PS)	FUSE	The fuse holder allows replacement of main power supply fuse.
③(CPU-2)	32K PGM	The 2-position switch selects memory addressing mode. When in the 32K position, program addressing limit is 32K words. When in the PROGRAM position, either 32K or 64K mode is selected by a program which sets the memory mode mask word.
④(CPU-2)	CNSL INT	Console interrupt pushbutton, when pressed, causes a program interrupt through vector X'47' if, 1) the console interrupt bit in the internal mask word is set and, 2) the interrupt system is enabled.
⑤(CPU-2)	15→8	These miniature binary switches are called the console switches.
⑥(CPU-2)	7→0	The console switches may be read by an RCSM or RCSR instruction in a program. This capability permits writing programs which allow data entry and control via these switches. When switch is in position labeled OPEN, bit is set to 0.
⑦(CPU-2)	DMA ACK	This indicator may blink periodically when direct memory access cycle stealing is occurring. It may illuminate continuously if very high DMA activity is in progress or if there is a malfunction. In a GA-16/220 system, DMA activity is controlled by the multiple high-speed data channel (MHSDC) controller.

Table 3-3. GA-16/220 Controls and Indicators (Sheet 2 of 7)

Key	Label	Description and Function
⑧ (CPU-2)	TTY BAUD Figures 3-2 & 3-3 Only	Does not apply to late model CPU-2 board (31D02474A). The 2-position switch changes the baud rate of the built-in serial I/O controller to accommodate either a teletype (Model 33 automatic send receive, ASR, or equivalent) at 110 baud or a CRT terminal at 110 or 9600 baud.
⑨ (CPU-2)	9600 Figures 3-2 & 3-3 Only	Does not apply to late model CPU-2 board (31D02574A). This screw adjustment permits fine adjustment of the 9600 baud transmission rate. It is adjusted only when the BAUD switch ⑧ is in the 110 position.
⑩ (CPU-2)	110 Figures 3-2 & 3-3 Only	Does not apply to late model CPU-2 board (31D002574A). This screw adjustment permits fine adjustment of the 110 baud transmission rate. It is adjusted only when the BAUD switch ⑧ is in the 110 position.
⑪ (SCI)	BKDS*	Break Disable Switch - The 2-position switch enables or disables the TTY break capability. When switch is in the break-disable (BKDS) position, TTY breaks are ignored. When in the other position, TTY break is enabled so when a TTY operator presses the BREAK key on a teletype or CRT (provided unit is equipped with this key) either a processor (CPU) reset or an interrupt occurs, depending on the setting of the BKINT switch ⑫.
⑫ (SCI)	BKINT*	Break Mode Switch - The 2-position switch sets the break mode for TTY or CRT, provided BKDS switch ⑪ is set so that break mode is enabled. When BKINT switch is set to break-interrupt position (BKINT), a TTY break causes a non-inhibitable interrupt, via vector location X'46' (provided CPU is not operating under the SCI Console ROM program or the IPL ROM). Registers and status are saved in locations in the SCI program RAM. When switch is not in the BKINT position, a TTY break initiates a break reset, which causes control to be transferred to the Console ROM and registers and status are not saved. I/O controllers are not reset.

*Label refers to switch position. See description for function PL name.

Table 3-3. GA-16/220 Controls and Indicators (Sheet 3 of 7)

Key	Label	Description and Function
⑬ (SCI)	IPL	Pushbutton initiates initial program load (IPL). When pressed, control is passed to the IPL ROM installed on the SCI module, and program loading occurs from a peripheral device. Selection of the peripheral device is accomplished by setting the IPL SEL switch ⑭ to the appropriate position for the IPL device installed with the system. This function may be remotely controlled, via IPLSW line, or at auto-restart with cold start line at ground.
⑭ (SCI)	IPL SEL	The IPL selector switch is a 16-position rotary switch. The switch is used to preselect which I/O device will be the source of an IPL when the IPL switch ⑬ is pressed. Load-and-go operation is selectable for all devices; while load-and-stop operation may be selected for teletype, high-speed paper tape reader, or card reader. Table 3-4 specifies the device selections.
⑮ (SCI)	CNSL*	(Reset Selector). The 2-position switch determines both the function of the CPU RESET button ⑯ and an auto-restart operation, when power is applied. When in the console position (CNSL), the CPU and I/O are reset and control is transferred to the Console ROM. If in the other position the status of the cold-start line, (CLDS) determines the operations as described for RESET push button on the CPU-1 module ⑯ .
⑯ (CPU-1)	RESET	Pushbutton resets the CPU and the I/O system, and causes control to be transferred in accordance with the Reset Selector Switch (Console Mode) as follows: Reset-Selector Switch Console Mode: Control is transferred to the Console ROM program. Non-Console Mode: Control is transferred via auto-restart vector (Location X'41') to the contents of X'41'. (Provided CLDS- line is not grounded.)
⑰ (CPU-1)	IACK	Interrupt acknowledge indicator blinks when control has passed to a routine, via an interrupt vector. It normally blinks so rapidly as to be barely visible. If continuously illuminated, it indicates that the control has not returned from the interrupt processing routine, a "hung up" condition.

*Label refers to switch position. See description for function PL name.

Table 3-3. GA-16/220 Controls and Indicators (Sheet 4 of 7)

Key	Label	Description and Function
(18) (CPU-1)	ISE	Interrupt system enabled indicator is illuminated when the ISE flip-flop is set; which means that the inhibitable interrupt system is enabled.
(19) (CPU-1)	OMA	This indicator (also referred to as the OMA stall indicator) is illuminated when the operator's monitor alarm (OMA) has timed out. The OMA must have been initially turned on by a PMA instruction. When the OMA indicator illuminated, the RUN indicator (21) is extinguished and the CPU is in an idle state. To recover from an OMA, the operator must press an idle state. To recover from an OMA, the operator must press the RESET button (16).
(20) (CPU-1)	FGND	Foreground indicator is illuminated when the foreground registers are used, and extinguished when background registers are used. Refer to instructions BMS and FMS.
(21) (CPU-1)	RUN	The RUN indicator is illuminated when the CPU is in the run mode. If the WAIT indicator (22) is also illuminated, the CPU is in a wait condition as a result of executing a WAIT instruction. If MPP indicators (27) through (30) are illuminated, memory parity error has caused the stall. In order for an MPP stall to occur, the STALL switch (31) must be in the stall position. To recover, the user must RESET the system. If the run indicator is extinguished, the system is in idle. NOTE: If 18-bit memories are installed without installation of MPP module, a stall condition may occur if the parity override switch (36) is not set. Refer to description of (36), (37), and (38) in this table.
(22) (CPU-1)	WAIT	Wait indicator illuminates when a WAIT instruction has been executed.

Table 3-3.   GA-16/220 Controls and Indicators (Sheet 5 of 7)

Key	Label	Description and Function
㉓ (CPU-1)	-	In the 31D02573A board, this unlabeled 2-position battery backup switch faces to the rear of CPU-1 module; it is located between coordinate D1 and E1. In the backup power supply position (UP), +5VB refresh power for the memories (including the piggyback RAM) originates in the backup power supply or from batteries (when AC power is disconnected). When switch is not in backup position, the refresh power is obtained from the main power supply. When backup power supply is not installed, a memory service module must be installed in the J18 or J21 rear connector (Figures 3-1 and 3-2) to obtain power from the main power supply for the RAM memories. On CPU-1 boards other than 31D02573A (early models) the battery backup switch is on the board front edge; and the backup power supply position is DOWN.
㉔ (MPP)	DPT	The DMA write protect indicator, when illuminated, indicates that an attempt has been made by DMA or DMT port 1 to write into a memory area (via the high-speed data channel) which has been DMA-protected.
㉕ (MPP)	ME	Multiple error indicator illuminates when a second error occurs before software can process a previous error. Other indicators also may be illuminated.
㉖ (MPP)	PPT	Program write protector indicator, illuminates when a program has attempted to write data in a memory area which has been program-protected.
㉗ (MPP)	LPB	Lower parity bit indicator shows the contents of parity bit for the lower byte of a memory word (illuminated = 1). Content of bit must be compared with the lower byte to determine if error has occurred; even parity is error.
㉘ (MPP)	UPB	Upper parity bit indicator shows contents of the parity bit for the upper byte of a memory word (illuminated = 1). Content of bit must be compared with the upper byte to determine if error has occurred; even parity is error.
㉙ (MPP)	DPY	DMA parity indicator illuminates when a parity error is detected during a DMA transfer.

Table 3-3. GA-16/220 Controls and Indicators (Sheet 6 of 7)

Key	Label	Description and Function
㉚ (MPP)	PPY	Program parity indicator illuminates when a parity error is detected when a program reads a memory location (data or instruction fetch). NOTE: Indicators ㉔ through ㉚ remain illuminated until MPP status is reset under software control.
㉛ (MPP)	STALL	The 2-position switch faces to the rear of the MPP module and is preset prior to operation. This switch determines CPU action when a DMT, DMA or CPU parity error occurs. When switch is in STALL position, the memory bus is forced to a busy state, thereby, halting the CPU. When not in the STALL position, control is passed to a routine, via non-inhibitable interrupt vector X'42'. (All non-parity errors pass control, via X'42', regardless of the setting of STALL switch. The routine must determine type of error.)
㉜ ㉝ ㉞ ㉟	15 14 13 12	2-position switches on the memory modules set the memory module address boundaries as described in Section 2.1.3 and Figure 2-11. The number of switches present depend on the memory module capacity (8K boards are shown in Figures 3-2 and 3-3).
㊱ (MEM)	PAR OVRD	The 2-position switch is installed only on 18-bit memories. This switch is effective only if MPP module is not installed; it enables parity override, which disables parity error detection, when in DOWN position. When in UP position, parity error detection occurs. Action upon a parity error depends on whether or not an MPP module is installed. 1. When MPP module is not installed and switch is in the UP position, a parity error will cause a CPU STALL condition on data fetches. The DERR and IERR indicators will identify the error. 2. When an MPP module is installed, switch may be in either position and parity errors will be identified by the LPB, UPB, DPY, and PPY indicators ㉗ through ㉚ on the MPP module. Detection is enabled by a programmed I/O instruction to the MPP module. Action taken upon parity error detection then is determined by the setting of the stall switch ㉛ on the MPP module.

Table 3-3. GA-16/220 Controls and Indicators (Sheet 7 of 7)

Key	Label	Description and Function
�37 (MEM)	DERR	The data error indicator illuminates (in 18-bit memories) when a parity error occurs on a data fetch. The data comes out as X'0000'. This condition is cleared by a system re-set or by a break reset (see description of ㉗ and ㉑).
�38	IERR	This instruction error indicator (in 18-bit memories) illu-minates when a parity error occurs on an instruction fetch. The instruction comes out as X'0000' (WAIT). This condi-tion is cleared by a system reset or by a break reset. NOTE: If the Memory Parity Protect (MPP) option is includ-ed in a system, neither the IERR nor DERR indicators will illuminate unless there is a high failure rate, assuming the MPP is managing the memory under pro-gram control.
�39 (BAT)	-	Unlabeled indicator illuminates when power (either from AC line or from batteries) is applied to the memory modules. Light is extinguished when manual cut-off button �38 is pressed, (or if batteries are exhausted), provided AC pow-er is disconnected from the auxiliary power supply.
�40 (BAT)	-	Unlabeled pushbutton provides manual cut-off of battery power to memory modules. Pressing this button will have no effect unless AC power is disconnected from auxiliary power supply. If AC power is disconnected, pressing this button will cut off power to memories. Power will not be restored to memories until AC power is reconnected. NOTE: Application of power to auxiliary power supply is independent of built-in main power supply switch ① , or other means of controlling power to external main power supply.
�41 (BAT)	BAT CHG* ADJ	This control is used to adjust the charge voltage to the battery pack to maintain a 0.4 ampere rate (maximum).
�42 (BAT)	5VB	This control is used to adjust the +5 volt regulator. (Specification 82S00629A.)
�43 (BAT)	VDD	This control is used to adjust the +12 volt regulator. (Specification 82S00629A).

*Refer to Specification 82S00629A for adjustment procedure.

Table 3-4. IPL Selector Switch on SCI Module (GA-16/220)

Position	Device
0	Teletype (Load and Go)
1	High-Speed Paper Tape Reader (Load and Go)
2	Card Reader (Load and Go)
3	3347 Disk (Load and Go)
4	3346 Removable Disk (Load and Go)
5	3349 Floppy Disk (Load and Go)
6	3343 Disk (Load and Go)
7	3346 Fixed Disk (Load and Go)
8	3342 Disk (Load and Go)
9	3341 Disk (Load and Go)
A	Teletype (Load and Stop)
B	High-Speed Paper Tape Reader (Load and Stop)
C	Card Reader (Load and Stop)
D	Option
E	Option
F	Option

NOTE: Refer to description of IPL SEL switch ⑭ in Table 3-3.

3.2.2 INITIAL SWITCH SETTINGS

1. BAUD RATE SELECTOR $\triangle 2$: This switch should be set to the 110 baud position for a TTY, or to the baud rate required for a CRT or alternate serial I/O device.

2. Memory Address Switches (32), (33), (34), (35): Set these switches to provide contiguous memory addressing as explained in Section 2.1.3.

3. PAR OVRD (36): Set this switch in the UP position. A parity error will stall the machine if no MPP is installed, otherwise, the resulting action is a function of the MPP board. (Refer to explanation of PAR OVRD switch in Table 3-3.)

4. Unlabeled (23): This switch has two positions: backup power supply and main power supply. The switch MUST be set in the backup power supply position if a battery backup power supply is installed. If a battery backup unit is not installed, this switch must be in the main power supply position.

On the 31D02573A CPU-1 board, the backup power supply position is UP. On other, early model CPU-1 boards, the backup power supply position is DOWN. Refer to item (23) in Table 3-3.

CAUTION

If AC power is off with this switch in the main power supply position (non-backup) and the battery backup unit is installed, the battery will attempt to drive the main +5V CPU circuit, and will, therefore, discharge rapidly. The +5V battery output is not capable of driving the +5V logic for both CPU and memories, since it is only intended for memory backup power. In addition to a discharged battery, this situation may also result in damage to the backplane etch.

3.3 INITIAL POWER-UP

1. If a battery backup unit is installed in the system, AC primary power should be applied to it first. The unlabeled indicator ㉟, will light indicating the backup unit is functioning.

2. Apply primary AC power to the system supply. If the Reset Selector ⑮, Break Disable ⑪ and Break Mode ⑫ switches are set as:

    RESET SELECTOR ⑮: Console Position ("UP")

    BREAK DISABLE ⑪: Enable Position ("UP")

    BREAK MODE   ⑫: Interrupt Position ("DOWN")

    The TTY or CRT should output a CR/LF when power is applied. The "FGND" ⑳ and "RUN" ㉑ indicators should be lit at this time.

3. Pushing "RESET" ⑯ will cause the TTY or CRT to output a CR/LF. The same will occur if the AC power is switched off and then back on again.

3.4 EXECUTING THE CPU T&V

The user should now refer to the CPU T&V listing (Model 5T10A) for loading and executing procedures for the GA Series-16 processor T&V. The T&V listing contains all the remaining necessary information to load and execute the CPU T&V.

additional documentation 4

4.1 ADDITIONAL T&VS AND UTILITY PROGRAMS

4.1.1 CPU RELATED T&VS

The following CPU related T&Vs may also be loaded and executed in a similar manner to the CPU T&V if desired:

- MPP T&V   5T110A
- TTY T&V   5T100A
- Memory T&V   5T14A

4.1.2 PERIPHERAL T&V

The standard SPC-16 peripheral T&Vs have been updated to be applicable to GA-Series computers. To facilitate loading and operating these programs a peripheral T&V Reference Manual (94A01519A) is provided. This manual should be used in conjunction with the particular peripheral T&V manual and listing for full understanding of the operation.

A list of the applicable peripheral T&Vs is provided in Appendix B.

4.2 STAND-ALONE UTILITIES

A description of the GA-16/220/330 Stand-Alone Utility programs is provided in Document Number 94A01531A, GA-16/220/330 Stand-Alone Utilities Manual.

4.3 BECOMING AN EXPERIENCED 220 USER

After successfully loading and executing the CPU T&V (Section 3), the user should now become intimately familiar with the System Reference Manual, GA Document Number 88A00508A. Once this is achieved, the user may then become familiar with the additional documentation pertinent to the particular system.

early GA-16/220 configuration A

Figure A-1 shows the configuration of the compact chassis, built prior to November, 1976. The major changes, made in currently shipped units, provide additional space between CPU-1 and CPU-2 modules to accommodate a redesigned SCI module. (See Section 3, Figure 3-2, System Reference Manual.) Table A-1 shows connector assignments for early compact chassis.

Figure A-2 shows the configuration of jumbo chassis built prior to October, 1976. To provide more space between CPU-1 and CPU-2 modules to accommodate redesigned SCI module (see Section 3, Figure 3-4, System Reference Manual), an I/O slot has been eliminated in currently shipped units. Table A-2 shows connector assignments for early jumbo chassis.

The circled numbers are keyed to Table 3-3, Section 3, for descriptions of controls and indicators.

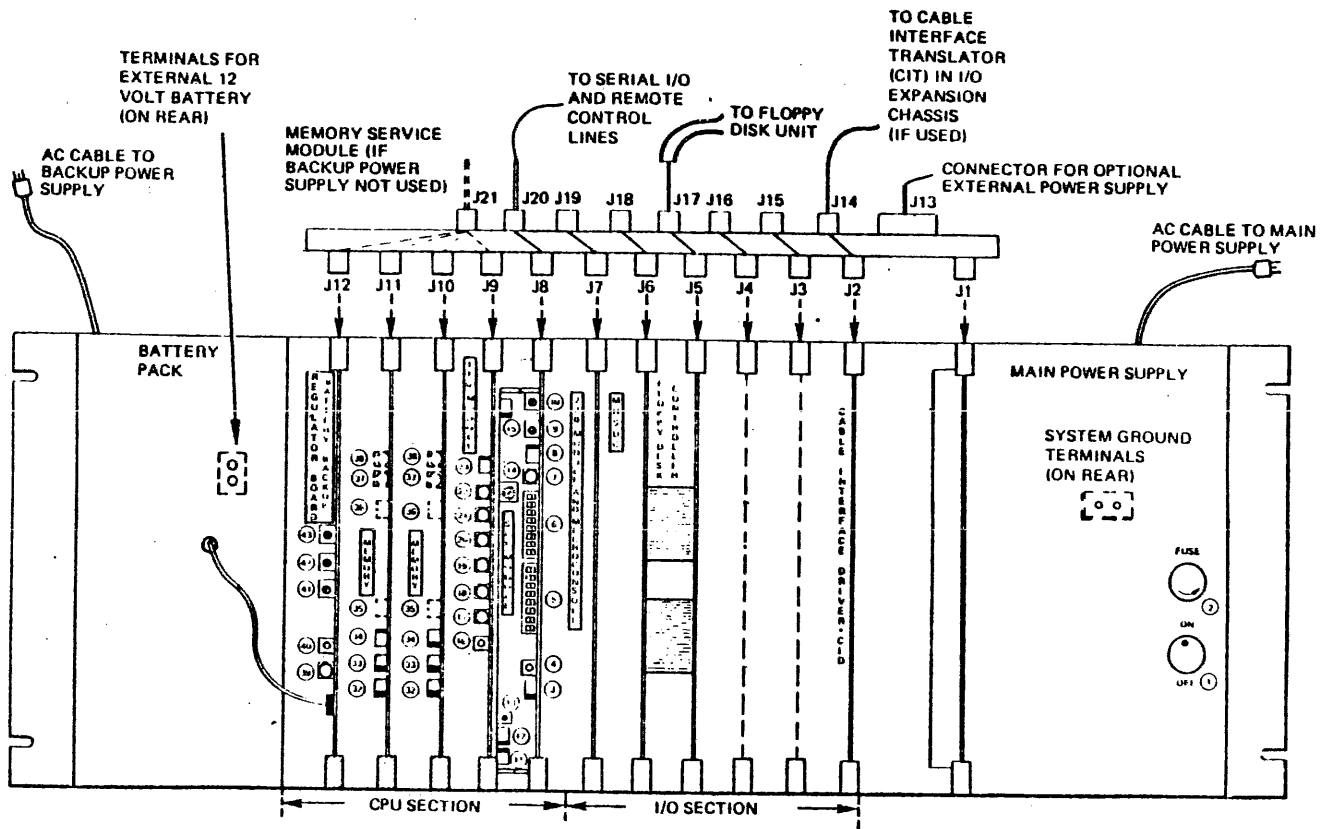Figure A-3 shows the priority interrupt chain wiring for early compact and jumbo chassis.

Figure A-1. GA-16/220 System in Compact Chassis (No MPP)

A-2

88A0525A-B

Table A-2. Connector Assignments for Jumbo Chassis,
GA-16/220 Computer System

Front/Module (220)		Rear/Interface (220)	
J1	Channel Interface Driver (CID).	J19	Cable to I/O expansion chassis (6 foot maximum).
J2 J3 J4	I/O controllers or shorting boards.	J20 J21 J22 J23 J24 J25 J26 J27 J28	Paddleboards and cables interfacing I/O controllers (in J2 through J10) to peripheral devices.
J5 J6 J7 J8	Shorting boards are used in empty slots between controllers or CID to maintain interrupt chain continuity.		
J9 J10	MHSDC controller, if used, should go into J10.	J29	Serial I/O paddleboard with connector for TTY or CRT. Also provides access to cold-start (CLDS-) jumper, and remote control lines (IPLSW-, PFD-, RSET-, RUN-).
J11	220 module with optional System Console Interface.		
J12	110 module with optional piggyback memory.	J30	Memory Service Module if battery backup power supply is not used. J30 also may be used as interface for external DMT controller.
J13 J14 J15 J16 J17 J18	Memory module, DMT controller, or memory parity protect module. J18 also used for battery backup control module.		
		J32	Power cable from external power supply.
–	Auxiliary power supply and battery pack (use control module in J18).	J33	System grounding terminals.
		–	AC cord and terminals for external 12-volt battery on rear of auxiliary power supply.

Model No.	Revision No.	Title
4TC02	1	1575/1579 Synch Data Link Comm. Controller
4TC03	1	1578 Synch Data Link Comm. Controller T&V
4TC05	1	1574-0001 Synchronous Comm. Controller T&V
5T000	1	GA-16 System Exerciser T&V
5T010	1	GA-16 Signed MPY/DIV T&V
5T100	1	GA-16 Series TTY T&V
5T110	2	GA-16 Series Memory Parity Protect T&V
5T14A	1	GA-16 Semiconductor Memory T&V
5T18M	2	GA-16 Floating Point Processor T&V (Section 1)
5T200	1	GA-16 Series High-Speed Paper Tape T&V
5T20A	1	GA-16 CalComp 936 (3374) Plotter T&V
5T30A	1	GA-16 H-P 7210 (3375) Plotter T&V
5T35A	1	GA-16 CalComp 3371/3372 Plotter T&V
5T40A	1	GA-16 CalComp 926 (3374) DMA T&V
5T600	1	GA-16 Card Reader T&V
5T610	1	GA-16 Card Punch 3314 T&V
5T700	1	GA-16 Series Line Printer T&V
5T70A	1	GA-16 3345 DMA Disk T&V
5T80A	1	GA-16 CCIF T&V
5T850	1	GA-16 Series 3346/3347 Disk T&V
5T870	1	GA-16 Series 3349 Floppy Disk T&V
5T880	1	GA-16 3341/43 Disk w/Sector Bits In Label T&V
5T890	1	GA-16 3346/3347 Double Density Disk T&V
5T900	1	GA-16 3342 Drum T&V
5T950	1	GA-16 ADDS Console 980 CRT T&V
5TA00	1	GA-16 Series 3331 Mag Tape T&V
5TE00	1	GA-16 801 Auto Calling Unit T&V
5TE05	1	GA-16 Hazeltine 2000 CRT T&V
5TE45	1	GA-16 ADC/DAC T&V
5TE55	1	GA-16 Digital Process I/O T&V
5TE75	1	GA-16 GAARD T&V

Command Mnemonic	Function	Format, Example and Comments
BREAK	Interrupt CPU and gain access to Console ROM[1]	Press BREAK key on TTY or CRT
R	Display all registers	R (CR) (You cannot change any registers)
R	1. Display specified register	rR (CR) 3R (CR) Display Z register. Then b, display next register.
	2. Change register	Simply type new hex value after desired register display. Then b enters it and displays next register or (CR) enters it and terminates.
CR	1. Display memory location	a (CR) 3FC0 (CR) Both the address and its contents appear on CRT.
	2. Change memory location	Simply type new hex value after the desired location. Then, b enters it and displays next location - or (CR) enters it and terminates.
M	Display block of memory	b/eM (CR) 10/22M (CR) Display memory from hex 0010 to 0022. (You cannot modify memory.)
Z	Store a pattern in a block of memory	b/e/nZ (CR) 23AB/24AB/1111Z (CR) Store all "1s" from 23AB to 24AB.
S	Single step	aS (CR) 60AS (CR) Execute instruction at 060A and return to Console ROM; and print address of next instruction.

[1] Requires CPU-2 switches preset as follows:
   BKDS switch not in BKDS position (Break enabled)
   BKINT switch not in BKINT position (Break interrupt enabled)

Command Mnemonic	Function	Format, Example and Comments
S	Single Step (Cont'd)	2. S (CR) Execute instruction following last single step or at last Trap, whichever occurred last.
T	Set TRAP	1. aT (CR) 1000T (CR) Set Trap at hex 1000. Up to four traps can be set.
		2. T (CR) Remove Trap.
G	Go to specified address and	1. aG (CR) 100G (CR) Start execution at hex 0100.
		2. G (CR) Start execution at hex 0100, last single step.
Y	Set bias for relative addressing	aY (CR) 3000Y (CR) Bias to be used in relative addressing is 3000.
	Address modes used if a bias has been set for relative addressing	
A	Absolute	100S,A (CR) Single step at absolute address 0100; ignore the bias.
B	Relative	100S,B (CR) Single step at relative address 0100 plus bias.

Listed below are the 3 other console functions which permit resetting I/O and loading binary tapes (such as a bootstrap loader or punching binary tape).

L	Load absolute binary tape	aL (CR) Load from TTY starting at specified address.
I	Punch absolute binary tape	b/eI (CR) Output to TTY the specified block of memory.
!	I/O reset	! (CR) Initialize all perhipheral controllers.