LS256-1 LSI-11 MEMORY

INSTALLATION

Installation of the LS256-1 is straightforward. There are two links on the board, LINK 1 and LINK 2 (refer to the figure on the facing page). LINK 1 is inserted to select the 22 bit addressing mode and removed for the 18 bit addressing mode. The position of LINK 2 selects the parity mode. Connect pins 2 and 3 to disable parity and connect pins 1 and 2 to enable parity generation and checking.

The switch S1 must be set to determine the address range to which the LS256-1 will respond. The simplest case occurs when the LS256-1 is the only memory in the system - then it is suggested that LINK 1 be inserted to select 22 bit addressing and switches 1 to 8 be all set ON.

Where the LS256-1 is the only memory, you can also select 18 bit addressing by removing LINK 1 and setting S1 as in Table 2. (Useful if you lose the link!) For configurations which are not likely to change, replacing the links with wire wrapped connections may provide a higher degree of permanency and prevent the settings being changed by accident.

With multiple LS256-1s, insert LINK 1 and select an appropriate starting address for each board from table 1. Most operating systems will require the addresses to be set so that the boards occupy contiguous blocks of addresses, i.e. there must be no gaps.

If you have ROM present or multiple memory boards in the lowest 256 Kbytes of addresses, then it is possible to set the LS256-1's starting and ending addresses on any 16 Kbyte boundary: remove LINK 1 and select the desired range using settings for S1 derived from Table 3. The starting address is set in switches 1 to 4 and the ending address in switches 5 to 8. Thus if the address range sought is 32 kb (100000 octal) to one less than 240 kb (737777 octal), then switches 1 to 4 are set to on-on-off-on and switches 5 to 8 are set to off-on-on-on.

NOTE: When the CPU selects addresses in the IO page (124K-128K words for an 11/23 and 28K-32K words for an 11/2), the LS256-1 is automatically disabled by the assertion of the BBS7 (Bank 7 Select) signal. Thus it is not necessary to worry about whether the selected address range overlaps the IO page.

NOTE: Selecting memory address limits that fall within the range of another memory can cause unpredictable system behaviour.

TABLE 1: 22 bit addressing (link 1 closed) 0 - 2048 Kw

Starting address		sw1	sw2	sw3	sw4	sw5	sw6	sw7	sw8	Octal (bytes)
0kw	0kb	on	on	on	on	on	on	on	on	00000000
128kw	256kb	on	on	on	--	on	on	on	--	01000000
256kw	512kb	on	on	--	on	on	on	--	on	02000000
384kw	768kb	on	on	--	--	on	on	--	--	03000000
512kw	1024kb	on	--	on	on	on	--	on	on	04000000
640kw	1280kb	on	--	on	--	on	--	on	--	05000000
768kw	1536kb	on	--	--	on	on	--	--	on	06000000
896kw	1792kb	on	--	--	--	on	--	--	--	07000000
1024kw	2048kb	--	on	on	on	--	on	on	on	10000000
1152kw	2304kb	--	on	on	--	--	on	on	--	11000000
1280kw	2560kb	--	on	--	on	--	on	--	on	12000000
1408kw	2816kb	--	on	--	--	--	on	--	--	13000000
1536kw	3072kb	--	--	on	on	--	--	on	on	14000000
1664kw	3328kb	--	--	on	--	--	--	on	--	15000000
1792kw	3584kb	--	--	--	on	--	--	--	on	16000000
1920kw	3840kb	--	--	--	--	--	--	--	--	17000000

TABLE 2: 18 bit addressing (link 1 out) 0 - 128 Kw

Starting address	sw1	sw2	sw3	sw4	sw5	sw6	sw7	sw8
0	on	on	on	on	--	--	--	--

TABLE 3: 18 bit addressing (link 1 open)

Address		Start				End				Octal (bytes)
		sw1	sw2	sw3	sw4	sw5	sw6	sw7	sw8	
0kw	0kb	on	on	on	on					000000
						on	on	on	on	037777
8kw	16kb	on	on	on	--					040000
						on	on	on	--	077777
16kw	32kb	on	on	--	on					100000
						on	on	--	on	137777
24kw	48kb	on	on	--	--					140000
						on	on	--	--	177777
32kw	64kb	on	--	on	on					200000
						on	--	on	on	237777
40kw	80kb	on	--	on	--					240000
						on	--	on	--	277777
48kw	96kb	on	--	--	on					300000
						on	--	--	on	337777
56kw	112kb	on	--	--	--					340000
						on	--	--	--	377777
64kw	128kb	--	on	on	on					400000
						--	on	on	on	437777
72kw	144kb	--	on	on	--					440000
						--	on	on	--	477777
80kw	160kb	--	on	--	on					500000
						--	on	--	on	537777
88kw	176kb	--	on	--	--					540000
						--	on	--	--	577777
96kw	192kb	--	--	on	on					600000
						--	--	on	on	637777
104kw	208kb	--	--	on	--					640000
						--	--	on	--	677777
112kw	224kb	--	--	--	on					700000
						--	--	--	on	737777
120kw	240kb	--	--	--	--					740000
						--	--	--	--	777777

THEORY OF OPERATION

The LS256-1 uses industry standard 64K x 1 dynamic RAM memory devices. Refresh circuitry is provided on the board so that replacements are available from many sources. Pin 1 of the memory chips is held high (used as a refresh control on some DRAMS).

The 36 chip dynamic RAM array is organised as two banks, each storing 64K words of data and two parity bits. Bank 0 consists of chips U41-U49 and U59-U67, with bank 1 made up of U50-U58 and U68-U76.

Switch S1 is used to select the range of addresses to which the LS256-1 board will respond. Depending on the position of Link 1, comparators U12 and U13 compare the switch setting with address lines A14 to A17 (18 bit backplane) or A18 to A21 (22 bit backplane). If the board is selected when the Q-BUS signal SYNCH goes high, the MREQH signal (U1(P2)) will be high. The SYNC signal is also used to latch address bits A1-A16 into the memory row and column address drivers U17 and U18.

MEMORY CYCLE

With the MREQH signal high, a memory cycle commences when the Q-BUS signals DIN or DOUT is asserted. Cycle timing is controlled by the shift register U19 with control states ST1H through ST8H being enabled on successive pulses of the 20MHz system clock.

On ST1H the RAS signal to the appropriate bank of memory chips is enabled, latching the row addresses.

On ST2H, MROWL (U22/P8) changes from low to high and MCASL changes from high to low. Thus the row address is disabled (U17) and the column address is enabled (U18) to the memory chips.

On ST3H the CAS signal is enabled to both memory banks latching the column address.

On ST4H the MRPLYH U31(P8) is enabled activating the Q-BUS RPLY signal.

On ST5H the RAS signal is released to the memory chips and they enter their precharge phase.

On ST8H the shift register is cleared when the DIN or DOUT signal is released.

Memory cycle timing is equivalent for both a DIN or DOUT cycle. However, during a DOUT cycle, the write line to the memory chips (WEL) is enabled by the combination of U23 and U33. Data is written into the low byte

(WELBL U33/P8 active), the high byte (WEHBL, U33(P11), active) or both in low and high bytes depending on the state of the Q-BUS signals WTBTH and DAL00. A parity bit is generated for each byte by U26 and U27 and is stored together with the data.

During a DIN cycle, the bus transcievers U5, U6, U7, U8, U9 enable data onto the Q-BUS when BENL signal U21 (P11) is active. The parity of each byte in the word is checked by U24 and U25. If an error is detected, the PE16 signal, U21(P3) goes high enabling the Q-BUS signal DAL16 if link 2 is so configured.

REFRESH TIMING

Refresh cycles are initiated every 16us by the refresh clock U10(P2). The refresh address is incremented each cycle by the counter U15 and enabled to the memory chips, when the REFL signal U28(6) is active, by U16. Timing is controlled by the shift register U19 in the following manner:

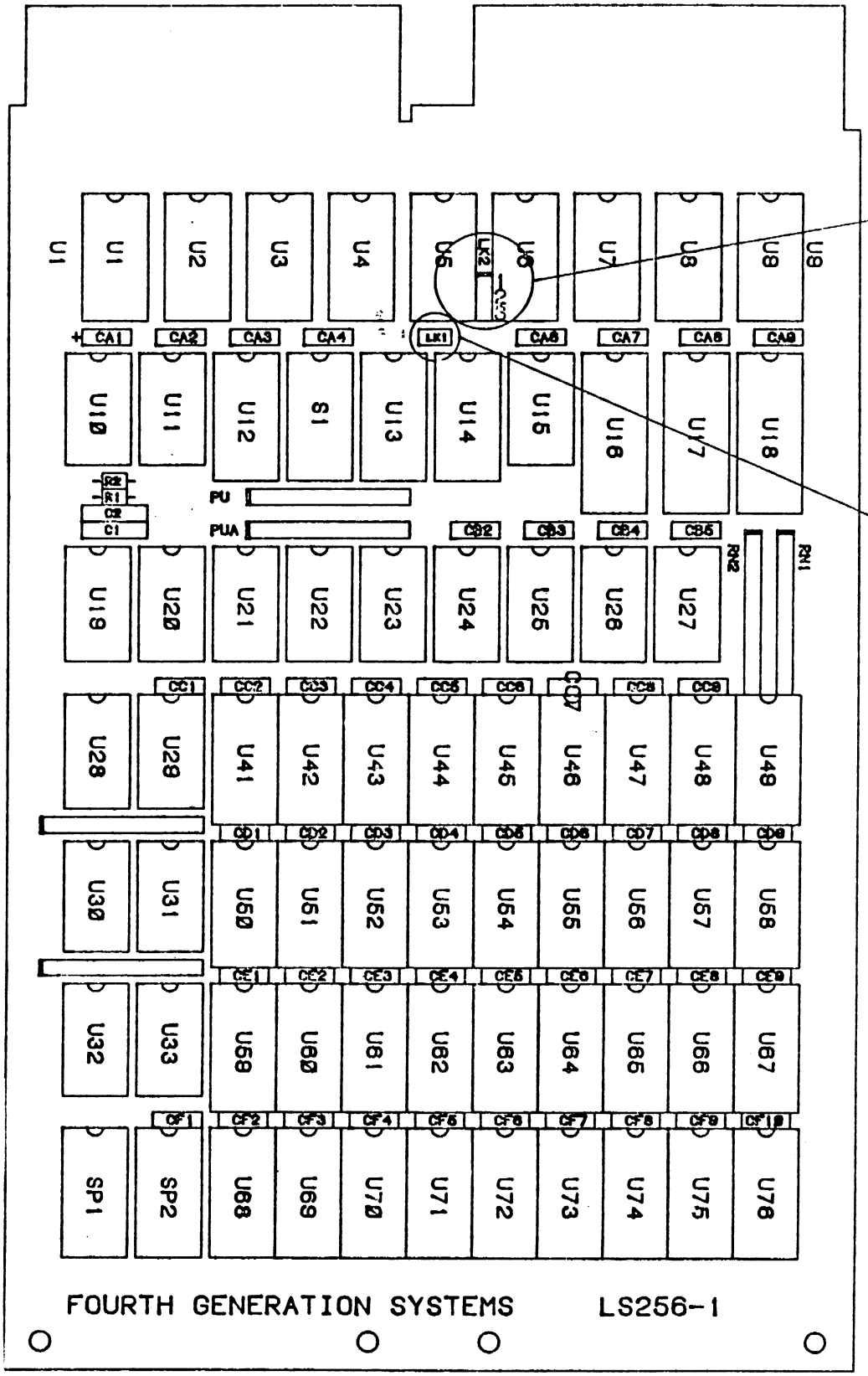
On ST1H the RAS signal to both memory banks is enabled (as the DREFL signal U30P(P6) is low), latching the refresh address.

On ST5H the RAS signal is released and the memory chips enter the precharge phase. Note that the CAS signal remains high during the entire cycle.

On ST8H the cycle is terminated and the shift register cleared.

REFRESH ARBITRATION

Conflicts between a pending memory cycle or refresh cycle are arbitrated in the following manner: if a refresh request occurs during a memory cycle, the refresh cycle is held off by U31 until the SYNCH signal goes low and clears the MREQH signal. Similarly, a memory cycle is held off until a current refresh cycle is complete.


LINK 2
Parity selection
1-2 : enabled
2-3 : disabled
LINK 1
Address mode
In - 22 bit
Out - 18 bit
FOURTH GENERATION SYSTEMS
LS256-1