I'M INTERESTED IN DETAILED INFORMATION

☐ for a current application in

_____

☐ for a potential application in

_____

My system is based around the:

☐ PDP-11/____ ☐ RDS 500____
☐ Interdata ____ ☐ NOVA ____
☐ SEL 32 ____ ☐ TI 980____

☐ Other _____

Please do the following:

☐ Send User's Manual, Hardware.
☐ Send User's Manual, Software.
☐ Phone me, to discuss my application.
☐ Add me to your mailing list.

Name _____

Title _____

Company _____

Street _____

City _____

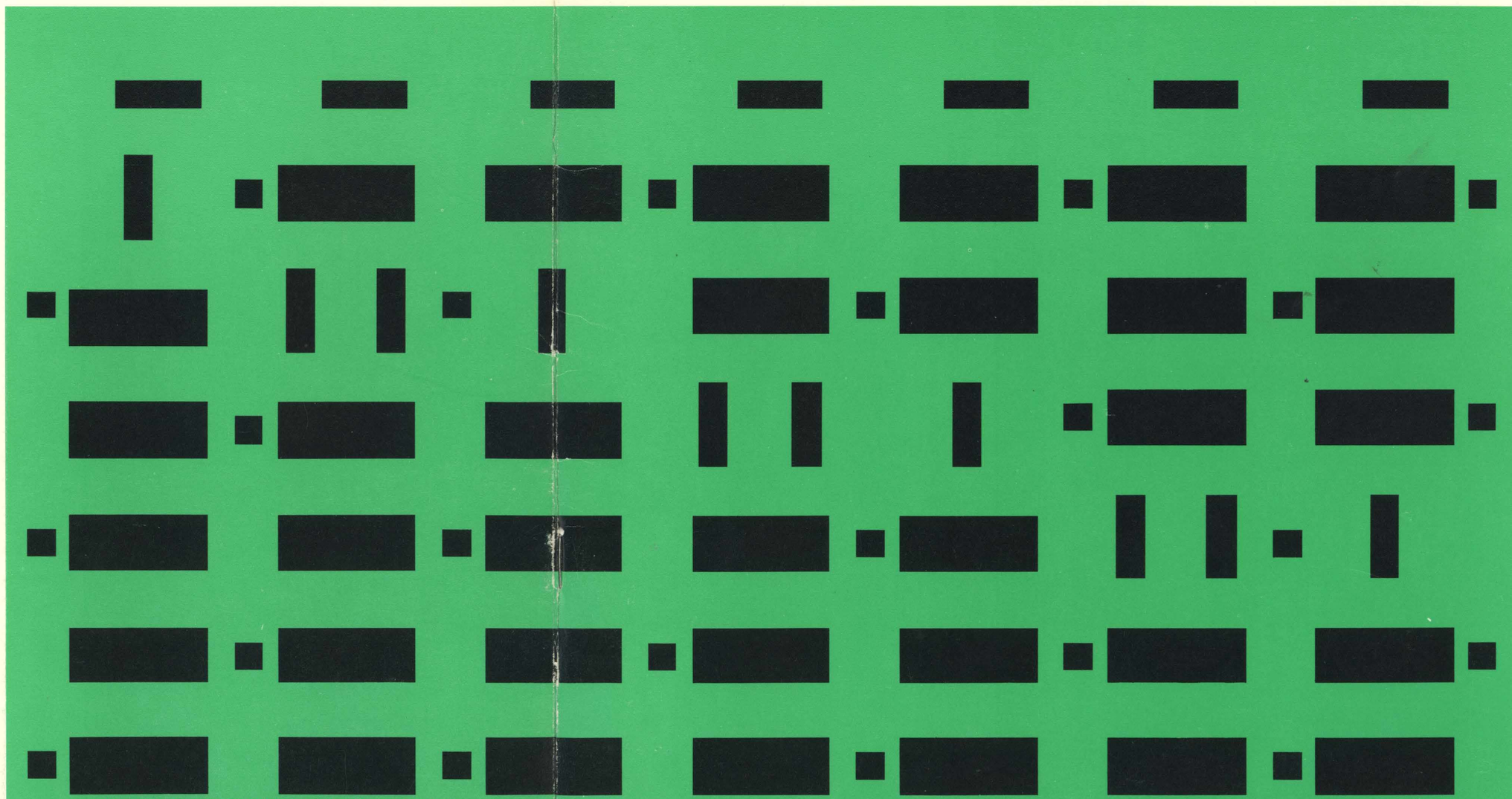
State _____ Zip ____

Telephone _____

Floating Point Systems, Inc.

AP-120B

ARRAY TRANSFORM PROCESSOR



FLOATING POINT SYSTEMS INCORPORATED
10520 S.W. CASCADE BLVD. PORTLAND, OREGON 97223

POWER YOU CAN HANDLE

Introducing the AP-120B, the unique peripheral floating-point array transform processor.

You'll look at the specifications and see the computational speed and accuracy of a mega-dollar mainframe.

Then you'll look at the cost, size, weight and ease of programmability, and realize what a breakthrough the AP-120B really is.

The unique culmination of years of floating-point and array processing expertise, the AP-120B offers a completely new source of convenient *dedicated* computational power.

THE HARDWARE: UNIQUELY FAST AND ACCURATE

The AP-120B has advanced hardware features that speed arithmetic through-put, while maintaining an extra cushion of computational accuracy.

BIG-JOB SPEED.

In the AP-120B, the processor instruction cycle is an order of magnitude faster than most computers — 167 nanoseconds. Up there with processors costing 20 times as much. The pipelined floating-point multiplier — 167 nanoseconds. The pipelined floating-point adder — 167 nanoseconds. That's 12 million floating-point computations per second.

BIG-JOB FLEXIBILITY

The AP-120B allows the paralleling of internal functions, such as arithmetic operations and address calculations, as well as allowing the merger of inputting/processing/outputting.

BIG-JOB PROCESSING.

The AP-120B offers up to a megaword of data memory, 167- or 333-nanosecond cycle. 16 index registers. 64 accumulators. Up to 32 kilobytes of program memory.

BIG-JOB ACCURACY.

The AP-120B advances computational precision with its full 38-bit arithmetic — normalized and convergently rounded. That's eight decimal digits, *not* just *six,* over ±153 decades.

BIG-JOB ARCHITECTURE.

The AP-120B is built for simultaneous operation of all processor elements. Its synchronous design provides extraordinary freedom from data glitches, requires no internal timing adjustments, provides a deterministic system capable of easy single-step operation, debugging, and unambiguous verification of correct operation. A system-specific, hardware format-converter mates with your mainframe to handle a variety of floating-point and integer word formats, easing on-line applications.

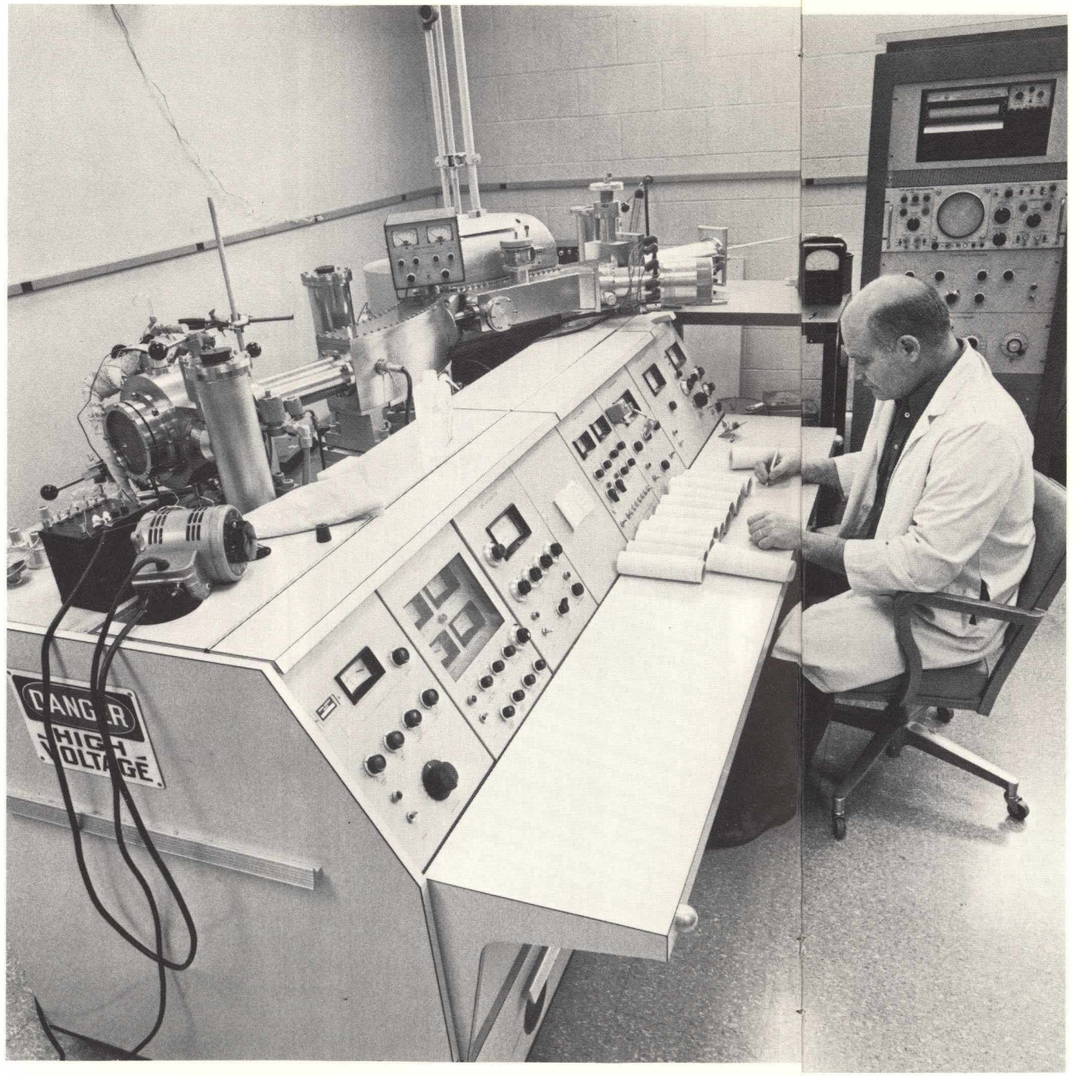
BIG-JOB RELIABILITY.

The AP-120B offers advanced Schottky-TTL microcircuitry for long life, and is backed by a full 90-day warranty, plus standard and on-call maintenance contracts.

It's a new type of processor, ready **now** to work for you.

APPLICATIONS: THE HARDER, THE BETTER

If you've been troubled by computational bottlenecks, by projects that outgrew your CPU budget, by complex simulations that boggled your mini — consider a cost-effective advance to the AP-120B.



You can save on DP charges, man-hours, and hardware investment, while gaining an accurate, secure, convenient, and powerful processor. Consider the possibilities:

Mechanical designers are optimizing the design and control features of the mechanical arms of the NASA Space Shuttle, using myriad algorithms without tying up their CPU.

Nuclear researchers are incorporating an AP-120B in their simulation projects, for rapid-fire solutions of differential equations in such areas as neutron flux densities, plasma behavior, laser-induced fusion — areas previously tackled only by heavy mainframe systems.

Oil exploration firms are adding the AP-120B to central and on-site systems, for effective analysis of the voluminous seismic records from their expensive exploration projects.

Weather prediction leaps a notch in both capability and economy with the introduction of the AP-120B for implementing complex hydrodynamic models.

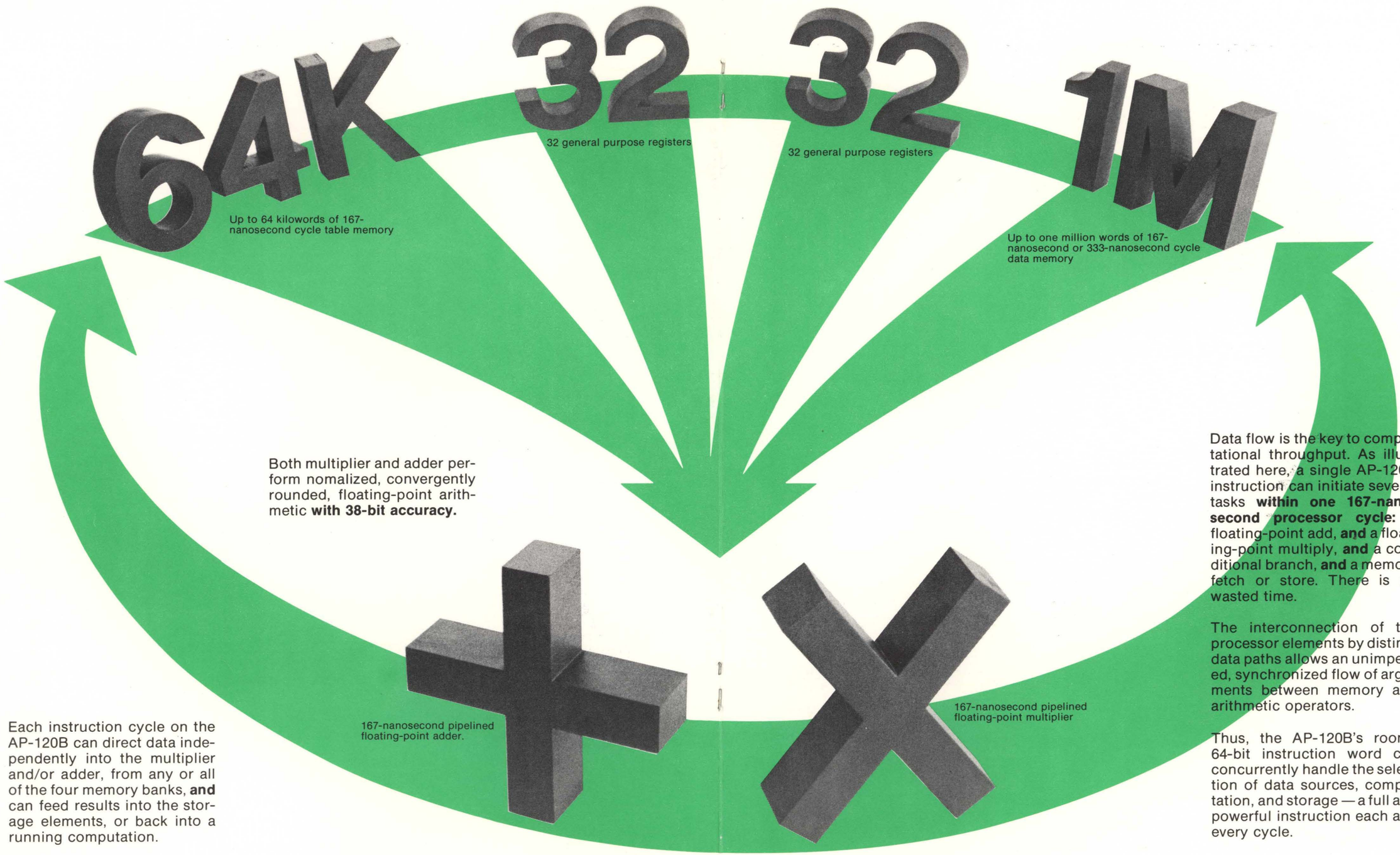
Heavy statistics users are planting the AP-120B's numerical power in the fields of statistical mechanics and actuarial modeling.

Speech researchers are beginning to rely on the AP-120B, to perform FFT's, convolutions, and other signal processing; and to implement algorithms in compressed-speech transmission and voice recognition experiments.

Physical chemists specify the AP-120B's 38-bit accuracy to compute the force equations that describe particle interaction and molecular bonding.

Plus simulation, image enhancement, graphic display, elastic modeling . . . . In short, the AP-120B is ready to handle the most demanding applications.

THE FULL CYCLE



Each instruction cycle on the AP-120B can direct data independently into the multiplier and/or adder, from any or all of the four memory banks, **and** can feed results into the storage elements, or back into a running computation.

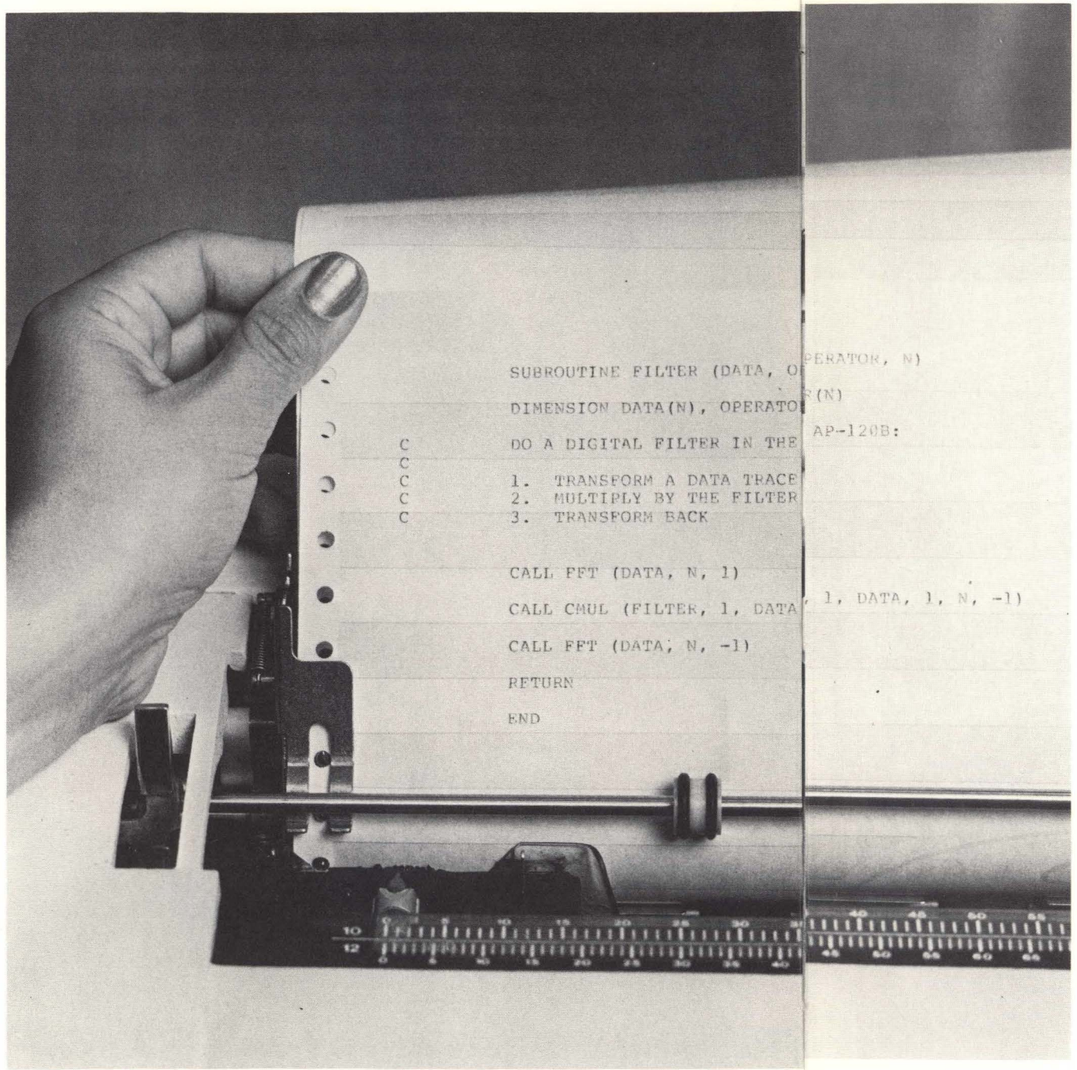
Data flow is the key to computational throughput. As illustrated here, a single AP-120B instruction can initiate several tasks **within one 167-nanosecond processor cycle:** a floating-point add, **and** a floating-point multiply, **and** a conditional branch, **and** a memory fetch or store. There is no wasted time.

The interconnection of the processor elements by distinct data paths allows an unimpeded, synchronized flow of arguments between memory and arithmetic operators.

Thus, the AP-120B's roomy 64-bit instruction word can concurrently handle the selection of data sources, computation, and storage — a full and powerful instruction each and every cycle.

SOFTWARE: "CALL" AND GET IT.

The AP-120B comes with a complete software package that integrates the processor's power into your operating system. You can initiate AP programs using your own FORTRAN code.



Four levels of software function independently and compatibly.

EXECUTIVE.

APEX (AP executive) decodes subroutine calls from your host system's FORTRAN or machine language, enabling you to initiate AP-120B execution with a familiar FORTRAN "CALL".

APPLICATION SUBROUTINES.

There are over 80 standard FORTRAN-callable algorithms written in AP-120B assembly code. They handle the arithmetic, trigonometric, and logarithmic functions; vector and matrix array operations; and signal processing operations.

PROGRAM DEVELOPMENT.

Four FORTRAN packages, compiled on the host operating system during installation, help you develop AP-120B programs: APAL (AP Assembly Language) assembles programs from machine code. APLINK (AP Program Linker) combines APAL modules into a load module for execution. APDBUG (AP Debugger) lets you interactively test new programs. Single-step capability is conveniently available due to the synchronous design.

APSIM (AP Simulator) simulates all aspects of the AP-120B on an off-line system, enabling you to develop programs and get execution times without interrupting AP-120B jobs. These four packages add up to a powerful repertoire of program development aids.

MAINTENANCE.

APTEST (AP tester) will completely test and verify proper operation of data paths, arithmetic elements, memory units, and the central processor, yielding diagnostic pointers.

You should expect a minimal transition time to full use of the AP-120B, with software support you can CALL on.

A MESSAGE

The importance of providing fast floating-point hardware for the mini-computer user was the impetus for the incorporation of Floating Point Systems, Inc., in 1970. Each year since, we have introduced faster and more compact floating-point processors, spurred on by customers who in turn took our hardware into increasingly sophisticated applications — and tougher hardware environments.

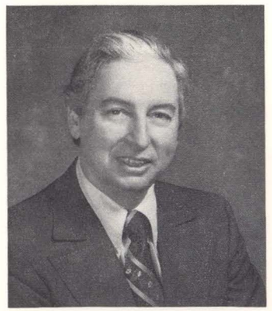
Early recognition of these new requirements led us to consider a revolutionary processor. What users needed was the very heart of a maxi- computer — high-speed arithmetic power — but in a small package, and at a small price.

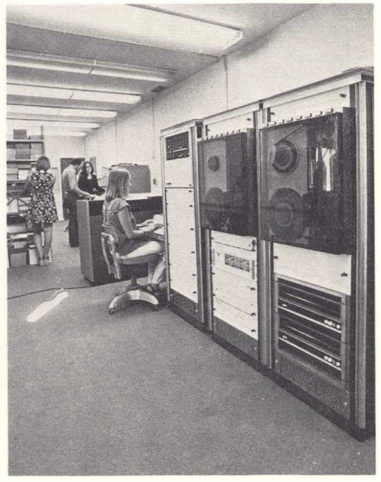
Thus we have designed a processor with general-purpose computing properties, aimed directly at high-speed algorithm execution, and made it easy to program for these tasks.

The AP-120B is a uniquely advanced balance of precision, speed, and economy. It provides an opportunity to upgrade computational capacity while lowering investment and usage costs.

We invite all those with complex computational tasks to undertake a detailed appraisal of the AP-120B Array Transform Processor. With years of deliveries of floating-point processors behind us, it is gratifying to approach the first anniversary of deliveries of the AP-120B. With customers world-wide, acceptance has been uniformly overwhelming. The AP-120B is field proven, reliable (MTBF 3900 hours), convenient to use, and most importantly, easily meets specifications.

C.N. Winningstad
President,
Floating Point Systems, Inc.





NOTES:

First Class
Permit No. 9645
Portland,
Oregon

BUSINESS REPLY
No postage stamp necessary if mailed in the United States

Postage will be paid by:

FLOATING POINT SYSTEMS
10520 S.W. Cascade Blvd.
Portland, Oregon 97223

Phone: (503) 620-1980
TELEX 360470 FloatPoint Ptl

Floating Point Systems, Inc.

AP-120B

PART NUMBER	DESCRIPTION	PRICES
AP-120B	**FLOATING-POINT ARRAY PROCESSOR** Includes: 256 words of RAM Program Source Memory. 512 words of ROM Table Memory for storage of transcendental constants APAL Cross Assembler Program APEX Executive Program APLINK Linking Loader Program APSIM Simulator Program APDEBUG Debugging Program APTEST Diagnostic and Test Programs Algorithm Library	$29,500.00
*AP-xx-1**	**TYPICAL INTERFACE TO HOST PROCESSOR.** Includes formatting hardward.	3,000.00**
AP-120-DM	**MAIN DATA MEMORY.** 8192 words of 38-bit MOS semiconductor RAM memory. 333ns interleaved effective cycle time.	6,550.00
AP-120-DMF 8	**FAST MAIN DATA MEMORY.** 8192 words of 38-bit MOS semiconductor RAM memory. 167ns interleaved effective cycle time.	10,700.00
AP-120-DMF 4	**FAST MAIN DATA MEMORY.** 4096 words of 38-bit MOS RAM. 167ns interleaved effective cycle time.	6,700.00
AP-PAR	**PARITY OPTION.** Implementation of 3 parity bits for checking data coming from and going to Main Data Memory.	
	Basic option and first 8K Main Data Memory. For each additional 8K Main Data Memory module, add	3,100.00 475.00
AP-120-TM	**TABLE MEMORY.** 512 words of 38-bit bipolar ROM. Used to store such constants as the roots of unity for FFT. Obtain n words of table memory to accomplish a 4n point real or complex FFT. One 512 word module is included in the AP-120B for transcendentals.	645.00
AP-120-TMR	**RAM TABLE MEMORY.** 1024 words of 38-bit bipolar RAM.	1,750.00
AP-120-PS	**PROGRAM SOURCE MEMORY.** 256 words of 64-bit bipolar RAM, used to hold microprograms. One 256 word module is included in the basic AP-120B.	1,595.00
APSDP	**AP SOFTWARE DEVELOPMENT PACKAGE.** Includes: APAL, APLINK, APSIM, APDEBUG, Algorithm Library, etc. All software necessary to allow the user to write and debug programs for the AP. Operates off line from the AP.	3,248.00
	If software installation is required it will be at the rate of $350.00 per day plus round trip air fare from Portland, Oregon. Installation typically requires two days.	
	NOTE: The full price of APSDP may be credited against the purchase of the AP-120B.	

* "xx" refers to the interface identification for the specific host processor.

** Price for majority of host processor interfaces.

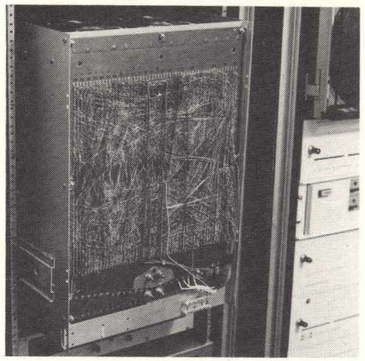
Floating Point Systems, Inc.

AP-120B

ARRAY TRANSFORM PROCESSOR

FEATURES

- **Fast Floating-point arithmetic — 167ns**
- **Enhanced computing accuracy**
- **Powerful 64-bit instructions**
- **Multiple high-speed memories**
- **Numerous hardware registers**
- **Multiple data paths**
- **Overlap input/processing/output**
- **Efficient data widths**
- **Intelligent interface**
- **Flexible format conversion**
- **DMA to Peripherals**
- **Reliable synchronous design**
- **Extensive software support**
- **High accuracy & range**



DESCRIPTION

The AP-120B floating-point array processor gives a unique combination of computational capability to mini- and maxi-computer systems. The high-speed, high-accuracy floating-point operations and programmability greatly increase system flexibility and throughput. Formatting hardware and interface logic provide full control processor and host interaction; an internal 38-bit floating-point format gives extra precision. Multiple accumulators, registers and data paths give ready access to data. Separate internal memories avoid accessing conflicts. A variety of mathematical functions and software packages allow the user to upgrade his existing computer system to handle heavy computational loads.

ARITHMETIC

The AP-120B performs floating-point arithmetic at maxi-computer speeds. Separate multiplier and adder units operate concurrently. The two-cycle pipelined adder completes a normalized, convergently rounded floating-point add (or subtract, fix, float, absolute value, logical And, Or, Equivalence) every 167ns. The three-cycle pipelined multiplier completes a normalized, convergently rounded floating-point multiply every 167ns.

Each unit detects overflow and underflow error conditions, forcing the result to the proper signed maximum value or zero, and setting the appropriate error flag.

ACCURACY

The floating-point adder and multiplier both contain special hardware to provide an extra cushion of accuracy for each computational step.

The adder has three extra bits (equal to 28 extra bits for normalized arguments) to preserve information shifted right during exponent alignment for use later during normalization and convergent rounding. The binary floating-point format further minimizes loss of resolution.

The multiplier computes the entire 56-bit fractional product, and then normalizes and convergently rounds to 28-bits.

Convergent rounding hardware in both arithmetic units rounds the normalized result up only when the remainder is greater than one half of the least significant bit. This causes the cumulative rounding error bias to converge toward zero.

INSTRUCTIONS

A single AP-120B instruction handles operations that would require several successive instructions on most computers. Each 64-bit instruction is divided into 10 powerful command fields, allowing a single instruction to perform a variety of tasks:

Floating-point add
Floating-point multiply
Fetch or store from Data memory
Read and store accumulators (two reads and two writes)
Conditional branching
Fetch from Table memory
Index register arithmetic

All transfers, computations, and memory accesses occur synchronously. No special programmed testing is needed to insure proper execution.

The AP-120B has three separate high-speed memories, each with dedicated controller logic. Multiple memories eliminate accessing conflicts, allow an optimal word length and cycle speed for each, and provide flexibility in configuring for specific applications.

Program Memory: 64-bit word size; 50ns cycle bipolar memory in 256-word increments. Addressable to 4K words.

Data Memory: 38-bits word size; either 167ns interleaved cycle MOS memory in 4K word increments, or 333ns interleaved cycle MOS memory in 8K word increments. Two parity bits are optional. Addressable to 1 Megawords.

Table Memory: 38-bit word size, 167ns cycle bipolar ROM in 512 word increments. Addressable to 64K words. Optional 167ns RAM table memory available in 1024 word increments up to 64K.

ACCUMULATORS AND REGISTERS

The AP-120B has 64 floating-point accumulators. Four accumulators are available during any instruction cycle; two as argument sources and two as result destinations.

The 16 integer index registers permit address calculations and loop overhead to occur concurrently with floating-point arithmetic. Data arrays may be indexed in either true or bit-reversed order.

DATA PATHS

Four separate 38-bit wide data paths into the floating-point adder and multiplier allow an uninterrupted flow of arguments for computation. Three additional data paths concurrently channel results back into accumulators or memory. This combination of multiple data paths allows sustained computational throughput, and avoids intermediate data moves. DMA cycle stealing allows overlapped data input, arithmetic processing, and data output.

DATA WIDTHS

Three distinct data widths are used to fit each particular data type: instructions, floating-point numbers and integers.

The 64-bit instruction word permits up to 10 different instructions to be programmed concurrently in a single 167ns processor cycle.

The 38-bit floating-point data word gives both extra computing accuracy and increased dynamic range over traditional 32-bit word lengths (8.1 vs 6.0 decimal digits, with a dynamic range of over $10^{\pm 153}$).

The 16-bit integer word allows direct memory addressing to 65,536 words; and to 1 million words with memory bank selection.

INTERFACE

An intelligent interface coordinates interaction between the AP-120B processor and the host computer.

The AP-120B electronic front panel gives the host computer access inside the AP-120B. The internal memories and registers may be examined and modified. A hardware break-point can be set to stop AP-120B execution at a selected program location or data address.

Programs may be single stepped for debugging purposes, with execution identical to free-running programs.

The interface provides four data transfer combinations between the two processors: host DMA to AP-120B DMA; Host DMA to AP-120B programmed 1/0; host programmed 1/0 to AP-120B DMA; and host programmed 1/0 to AP-120B programmed 1/0. Either the AP-120B or the host computer can control data transfers.

Floating Point Systems, Inc.

AP-120B

WARRANTY, INSTALLATION AND SERVICE INFORMATION

Warranty: The AP-120B is warranted for 90 days to end users, 60 days to OEM customers. This includes both parts and labor. Repair is to performed at the nearest regional Floating Point Systems, Inc. repair facility.

Installation: Installation on the customers site is at the rate of $350.00 per day plus round trip coach air fare from Portland, Oregon. Installation typically requires 3 to 5 days.

Service:

1. An annual service agreement is available for a charge of 6% of the list price of the system, plus, for each call, round trip coach air fare from the nearest FPS repair facility.
2. On call service is available for on site repair at a rate of $350.00 per day plus parts plus round trip coach air fare from the nearest regional FPS repair facility.
3. Faulty circuit boards may be sent to the nearest regional FPS facility for repair or exchange at the then prevailing price. See "AP-120B Spare Parts Information" Data Sheet, Form 7295.

FORMAT CONVERSION

The formatting hardware in the AP-120B interface converts data "on-the-fly" during transfers between the AP-120B and host or peripherals. Four standard formats are automatically handled and many options are available.

Host Computer Format to AP-120B Format

16-bit integers	– 38-bit unnormalized floating point
32-bit integers	– 32-bit integers
IBM 360 floating point	– 38-bit normalized floating point
Host floating point	– 38-bit normalized floating point

On return of results to the host, any floating-point numbers that would be out of range for the target format are detected and forced to the proper signed maximum or zero, and indicator bits set.

PERIPHERALS

A separate programmed 1/0 and direct memory access bus is provided for peripheral devices (A/D converters, disks, tape drives, etc.) to be interfaced directly to the AP-120B. Up to 256 1/0 device addresses can be accommodated.

RELIABILITY

A single master clock synchronizes processor actions in the AP-120B. There is no uncertainty caused by inter-element "hand-shaking", not variable phasing delays.

Timing allowances are designed to worst case temperature and voltage operating specifications — a full 50% safety margin in every cycle.

Units are tested as a functioning system at extremes of heat and supply voltage: a minimum of eight successful hours at high temperature, high voltage and again at low temperature, low voltage.

The high-speed Schottky MSI and LSI TTL logic is pre conditioned and parametrically tested to eliminate "infant mortality".

COMPACT PACKAGING

The AP-120B is arithmetic power in a compact package. The chassis mounts in standard 19' rack and occupies 24½" of space, including a high-efficiency switching regulated power supply. Rugged mechanical design and moderate card size (10" x 15") maximize system integrity in the field.

SOFTWARE SUPPORT

An extensive package of library functions, vector and matrix subroutines, and signal processing algorithms is supplied with the AP-120B; all callable from the host computer's FOR-TRAN programs. A cross assembler, program linker, on-line debugger (using the electronic front panel) and software simulator aid in new program development.

ALGORITHM EXECUTION TIMES*

Multiply-add: 167ns
Complex multiply: 667ns

Algorithm	167ns memory	333ns memory
1024 pt real FFT	2.9 ms	4.1 ms
1024 pt complex FFT	5.5 ms	6.9 ms
8192 pt real FFT	28.4 ms	37.7 ms
1024 pt vector elem. by elem. mult.	0.52 ms	1.05 ms
1024 x 32 pt convolution	6.0 ms	6.5 ms
512 x 512 real 2 DIM FFT	1.55 sec	2.2 sec
1000 element vector square root	1.85 ms	1.85 ms

*Established by benchmarks at user installations.

SPECIFICATIONS

ARITHMETIC

Floating-point width: 38-bits
Floating-point adds: every 167ns, 333ns for completion
Floating-point multiples: every 167ns, 500ns for completion
Integer width: 16-bits
Integer arithmetic: 167ns

MEMORY

Cycle: Program Memory, (bipolar RAM); Data Memory, 167ns interleaved or 333ns interleaved (MOS); Table Memory, 167ns (bipolar ROM).

Sizes: Program Memory, increments of 256 words to 4K words; Data Memory, increments of 2K words (167ns) or 8K words (333ns) to 1 million words; Table Memory, increments of 512 words to 64K words.

Word Sizes: Program Memory, 64 bits,
Data Memory, 38-bits, plus two optional parity bits
Table Memory, 38 bits.

REGISTERS

Floating-point Accumulators: 64
Index registers: 16
Subroutine return stack: 16

INPUT/OUTPUT

Direct memory access rate: Up to 3 million 38-bit words per second, depending upon the host computer.

Input/Output System, 38-bit word length, 256 devices addressable. An ancillary DMA port allows the AP-120B to communicate with other peripherals, such as disc memory A/D and D/A converters etc.

ELECTRICAL

Power service: 105/125 at 20 amps or 188/228 Vac, or 210/250 Vac at 10 amps. 50/60 Hz. 50/400 Hz optional.
Power Dissipation with 512 words of Program Memory, 16K Data Memory, and 2K Table Memory; less than 1200 watts.

ENVIRONMENTAL

Temperature Range: 10 to 40°C operating

Relative humidity range: 0-90%
Ventilation: 8 push-pull fans.

PHYSICAL

Dimensions: 24½" H, 19" W, 20"-25" D
Weight: 88 pounds including power supplies

Phone: (503) 620-1980 TELEX 360470 FLOATPOINT PTL

FLOATING POINT SYSTEMS, INCORPORATED
10520 S.W. CASCADE BLVD. PORTLAND, OREGON 97223

floating point systems incorporated

10520 S.W. Cascade Blvd.
Portland, Oregon 97223
Phone: (503) 620-1980
TLX 360470 FLOATPOINT PTL

July 1, 1976

Following is a list of the price and delivery on AP-120B interfaces presently available for various host computers. Interfaces not cited below will be quoted upon request.

DGC NOVA/ECLIPSE	$3,000	60-90 days
DEC PDP-11	3,000	60-90 days
TI-980	3,000	90 days
VARIAN 620 and 70 series	3,000	90 days
RAYTHEON RDS 500/R704	3,000	60 days
HARRIS (and DATACRAFT series)	4,600	90 days
HP2100 or 3000 series	3,500	120 days
CDC 1700 series or System 17	3,800	120-150 days
SEL 32 HSD Interface	5,600	120 days
Note: Customer must purchase HSD from SEL		
INTERDATA 8/32, 7/32 & 80	4,700	120-150 days
Note: (I/O cards provided by FPS)		
MODCOMP II to IV	4,700	90-120 days
Note: Customer must purchase board 4805 from Modcomp and drop ship to FPS		
SIGMA series	7,000	150 days
UNIVAC 1100 series	12,000	180 days
G.P. Interface (IOP 16) for A/D, etc.	3,000	90 days

Jon A. Salquist
Vice President
Marketing

Floating Point Systems, Inc.

AP-120B
TRAINING PROGRAMS

COURSE	DURATION	CHARGE PER STUDENT
AP-120B Maintenance I Prepares the graduate to trouble-shoot to the card level, and to work efficiently with the FPS RTM (Real Time Maintenance) program.	2 days	2 TC or $130
AP-120B Maintenance II Pre-requisite is Maintenance I, a solid working knowledge of floating-point notation, and experience in digital computer technology. Prepares the graduate to trouble-shoot to the component level.	4 days	4 TC or $260
AP-120B Programming Pre-requisite is experience in Assembly Level Programming, and a solid working knowledge of floating-point notation. Prepares the graduate to write programs for the implementation of algorithms for the AP-120B.	4 days	4 TC or $260
Floating Point Notation A survey of floating-point notation including the several popular floating-point formats and conversion between formats.	1 day	1 TC or $65

For courses given on-site, add instructor round-trip air fare and $250 per day on-site charge to the above charges. The minimum on-site course attendance required is three students.

Assignment of Training Credits (TC) is determined by equipment purchased.

2 Training Credits are issued for each AP-120B system purchased by an end user.

2 Training Credits are issued for the first OEM AP-120B purchased and 1 Training Credit is issued per unit thereafter.

COMPLEX FFTS ON THE AP-120B

TRANSFORM SIZE	BUFFER SIZE	TIME IN MILLISECONDS (INCLUDES BIT-REVERSE) FAST MEMORY	STANDARD MEMORY
64.	256.	0.20	0.28
64.	128.	0.28	0.40
128.	512.	0.47	0.72
128.	256.	0.62	0.95
256.	1024.	0.97	1.41
256.	512.	1.28	1.86
512.	2048.	2.26	3.48
512.	1024.	2.86	4.38
1024.	4096.	4.75	6.93
1024.	2048.	5.95	8.73
2048.	8192.	10.83	16.60
2048.	4096.	13.23	20.19
4096.	16384.	22.66	33.16
4096.	8192.	27.44	40.33
8192.	32768.	50.76	77.31
8192.	16384.	60.33	91.66
16384.	65536.	105.58	154.59
16384.	32768.	124.70	183.27
32768.	131072.	233.08	353.29
32768.	65536.	271.32	410.64

REAL FFTS ON THE AP-120

TRANSFORM SIZE	BUFFER SIZE	TIME IN MILLISECONDS (INCLUDES BIT-REVERSE) FAST MEMORY	STANDARD MEMORY
64.	128.	0.14	0.20
64.	64.	0.18	0.27
128.	256.	0.27	0.38
128.	128.	0.35	0.50
256.	512.	0.58	0.90
256.	256.	0.74	1.13
512.	1024.	1.20	1.76
512.	512.	1.50	2.22
1024.	2048.	2.70	4.18
1024.	1024.	3.30	5.08
2048.	4096.	5.61	8.32
2048.	2048.	6.81	10.12
4096.	8192.	12.56.	19.37
4096.	4096.	14.95	22.96
8192.	16384.	26.89	38.69
8192.	8192.	30.88	45.86
16384.	32768.	57.63	88.36
16384.	16384.	67.19	102.70
32768.	65536.	119.30	176.68
32768.	32768.	138.42	205.35

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AP-120B FLOATING POINT ARRAY PROCESSOR
FFT Times in milliseconds

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FAST AP-120B MEMORY (167 NS CYCLE)

	POINTS	BIT-REVERSE	FFT TIME	TOTAL TIME (MEMORY SIZE) N	TOTAL TIME (MEMORY SIZE) 2N	BENCHMARK PROBLEM TIME	BENCHMARK PROBLEM THRUPUT (KHZ)
REAL	64.	0.04	0.14	0.18	0.14	0.33	195.60
	128.	0.08	0.27	0.35	0.27	0.63	204.29
	256.	0.16	0.58	0.74	0.58	1.36	188.06
	512.	0.30	1.20	1.50	1.20	2.78	184.45
	1024.	0.60	2.70	3.30	2.70	6.17	165.93
	2048.	1.20	5.61	6.81	5.61	12.75	160.59
	4096.	2.40	12.56	14.95	12.56	28.20	145.25
	8192.	4.78	26.09	30.88	26.09	58.28	140.57
	16384.	9.56	57.63	67.19	57.63	127.56	128.44
	32768.	19.12	119.30	138.42	119.30	262.92	124.63
COMPLEX	64.	0.08	0.20	0.28	0.20	0.50	128.14
	128.	0.16	0.47	0.62	0.47	1.13	113.57
	256.	0.30	0.97	1.28	0.97	2.33	110.00
	512.	0.60	2.26	2.86	2.26	5.29	96.71
	1024.	1.20	4.75	5.95	4.75	11.02	92.93
	2048.	2.40	10.83	13.23	10.83	24.75	82.74
	4096.	4.78	22.66	27.44	22.66	51.40	79.69
	8192.	9.56	50.76	60.33	50.76	113.83	71.97
	16384.	19.12	105.58	124.70	105.58	235.48	69.58
	32768.	38.24	233.88	271.32	233.88	515.24	63.60

STANDARD AP-120B MEMORY (333 NS CYCLE)

	POINTS	BIT-REVERSE	FFT TIME	TOTAL TIME (MEMORY SIZE) N	TOTAL TIME (MEMORY SIZE) 2N	BENCHMARK PROBLEM TIME	BENCHMARK PROBLEM THRUPUT (KHZ)
REAL	64.	0.06	0.20	0.27	0.20	0.52	124.24
	128.	0.12	0.38	0.50	0.38	0.97	131.66
	256.	0.23	0.90	1.13	0.90	2.22	115.11
	512.	0.45	1.76	2.22	1.76	4.38	116.90
	1024.	0.90	4.18	5.08	4.18	10.07	101.73
	2048.	1.80	8.32	10.12	8.32	20.05	102.13
	4096.	3.59	19.37	22.96	19.37	45.54	89.93
	8192.	7.17	38.69	45.86	38.69	91.00	90.02
	16384.	14.34	88.36	102.70	88.36	204.00	80.31
	32768.	28.68	176.68	205.35	176.68	407.91	80.33
COMPLEX	64.	0.12	0.28	0.40	0.28	0.78	82.00
	128.	0.23	0.72	0.95	0.72	1.86	68.85
	256.	0.45	1.41	1.86	1.41	3.67	69.76
	512.	0.90	3.48	4.38	3.48	8.67	59.08
	1024.	1.80	6.93	8.73	6.93	17.27	59.28
	2048.	3.59	16.60	20.19	16.60	40.01	51.19
	4096.	7.17	33.16	40.33	33.16	79.94	51.24
	8192.	14.34	77.31	91.66	77.31	181.90	45.03
	16384.	28.68	154.59	183.27	154.59	363.73	45.04
	32768.	57.35	353.29	410.64	353.29	815.74	40.17

NOTE 1 : BY DOUBLING MEMORY SIZE, BIT-REVERSE IS HIDDEN IN FFT PROCESSING TIME.
NOTE 2 : BENCHMARK PROBLEM CONSISTS OF FFT, COMPLEX VECTOR MULTIPLY (FILTER), INVERSE FFT, PLUS I/O TIME. TIMES EFFECTIVE AS OF JUNE 1,1976.

FPS-7314
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