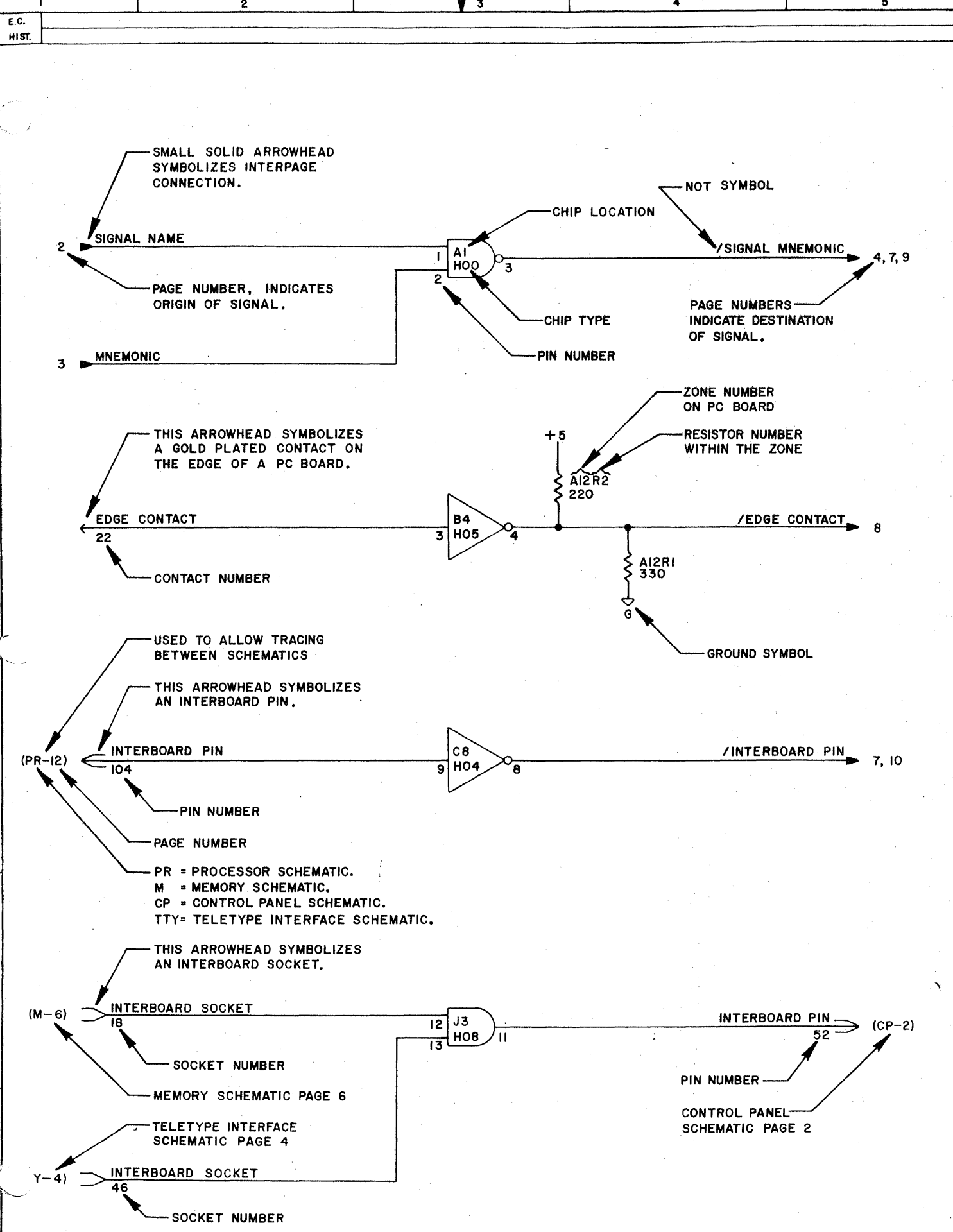


**SECTION III
REFERENCE DOCUMENTS**

INDEX OF SCHEMATIC DIAGRAMS

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138-002020	Processor Electronics Board	1-43
138-002019	Memory Electronics Board	1-38
138-002018	Communications Interface - ASR33	1-15
138-002031	TTY Modification	1-5



EC
HIST

2

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1 PIN DEFINITION:

—> INDICATES SOCKET FOR CONNECTION TO PROCESSOR BOARD.

REVISION STATUS OF SHEETS				
		1	2	3

		DATE
DRAWN	CHEUNG	12-30-73
CHECKED	POON	1-7-74
APPROVED	<i>W.H. Ferguson</i>	3-12-74

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COMPUTER SYSTEMS

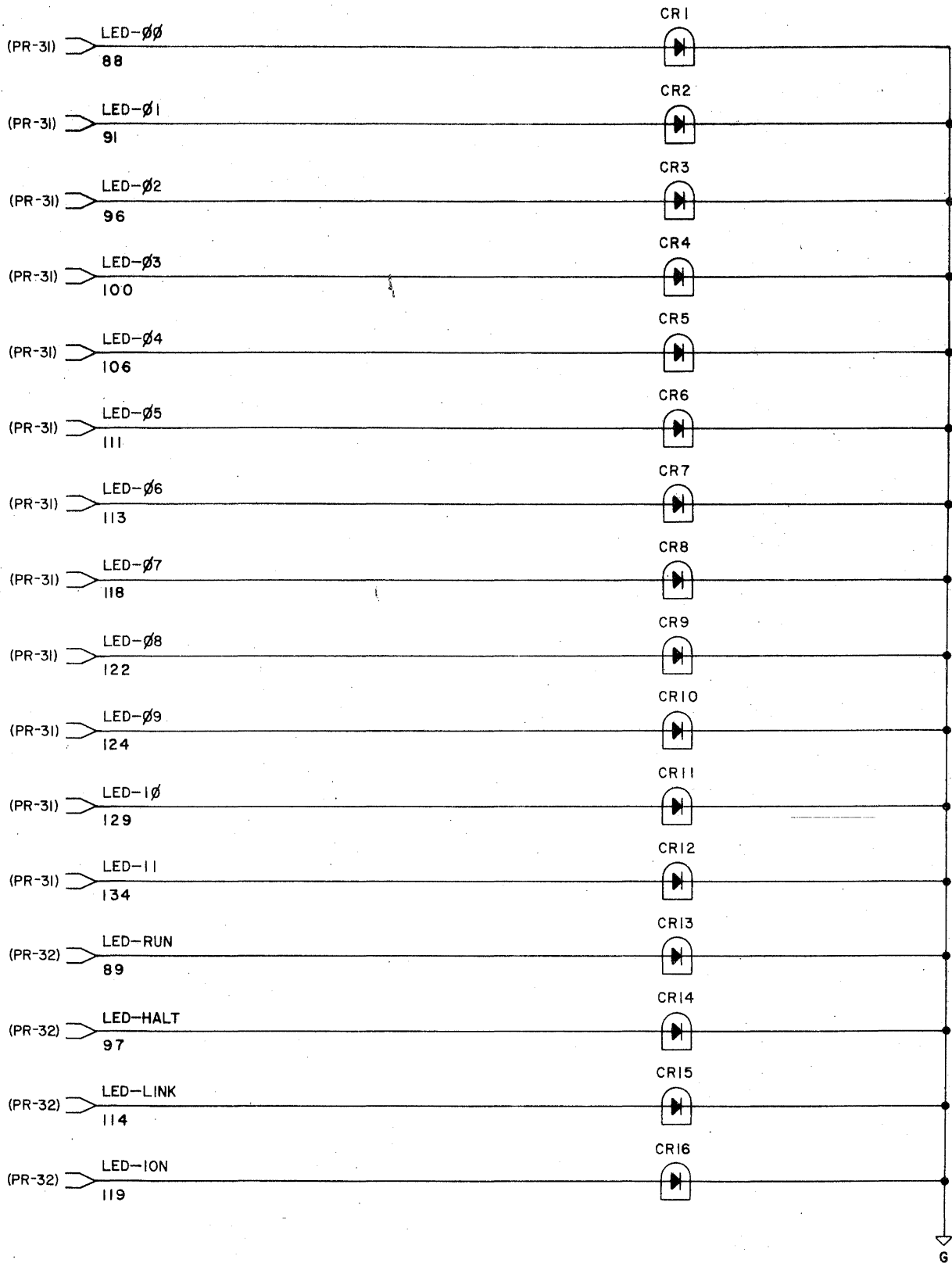
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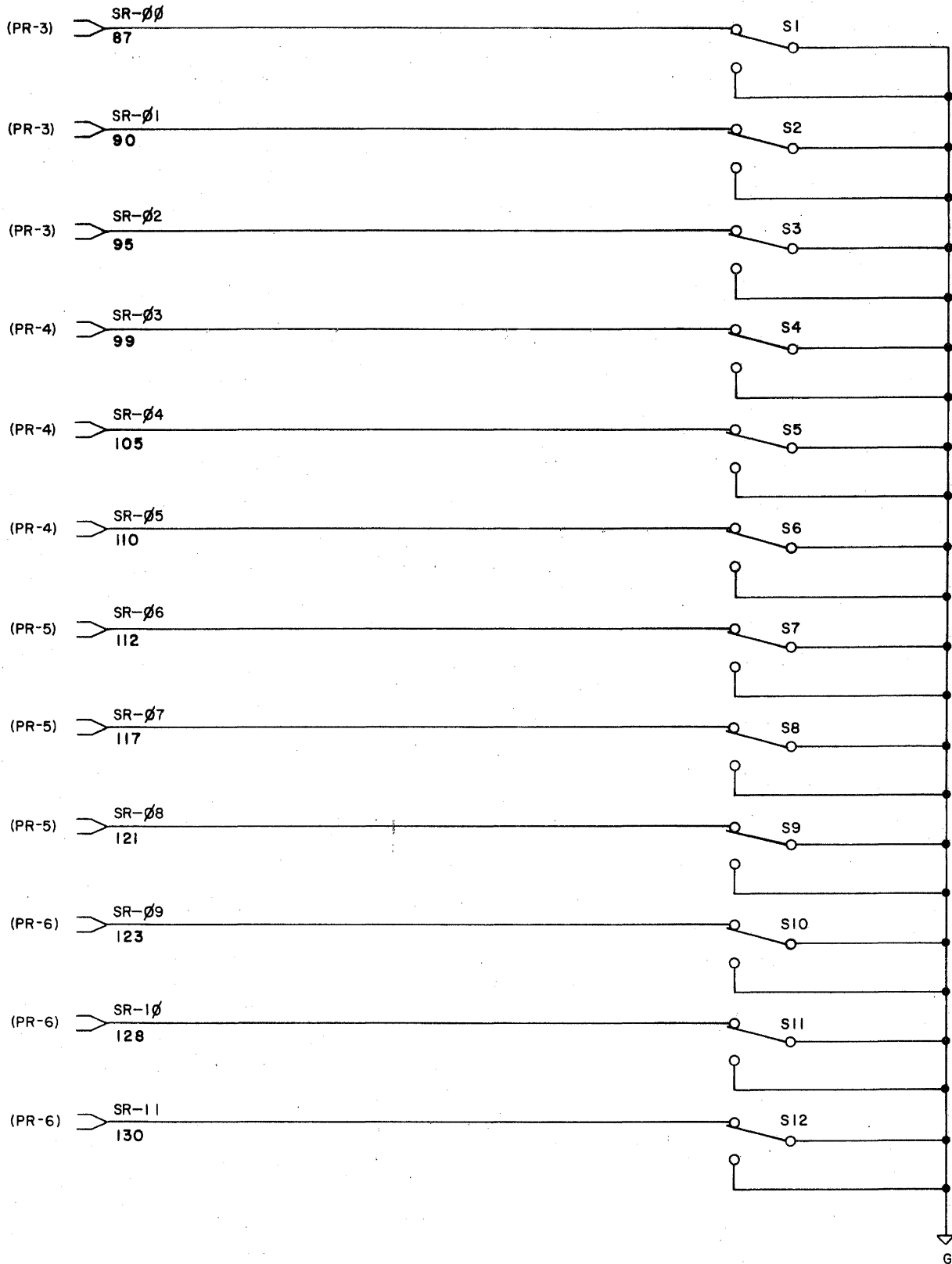
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VERS 190-1664-00

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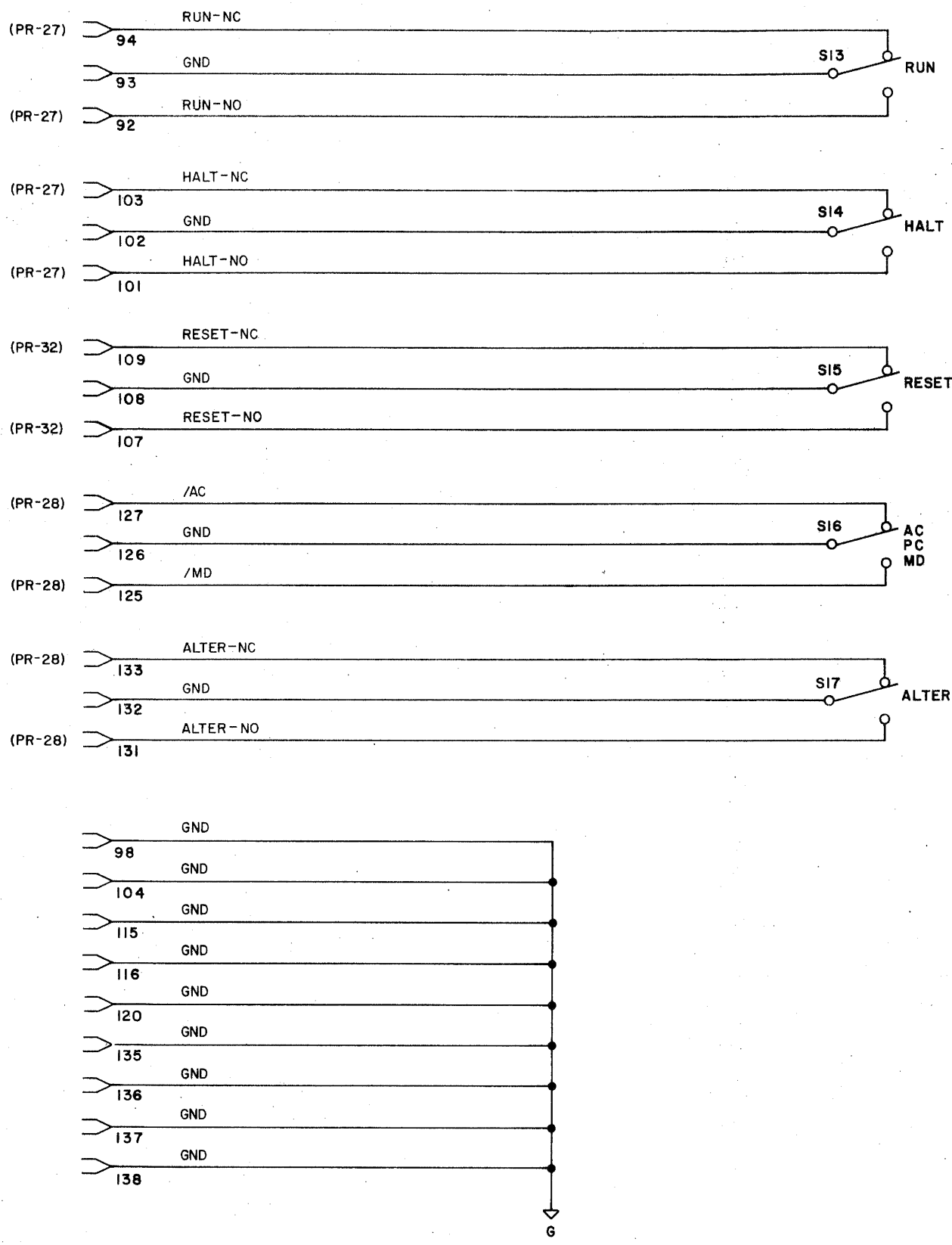
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1 2 3 4 5

T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19
83.3NS

12MHZ CLOCK

Q1

Q2

Q3

Q4

Q5

Q6

Q7

Q8

Q9

/SYNC

PA

TA

PB

TB

/READ 1

/READ 2

/WRITE 1

/WRITE 2

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TITLE SCHEMATIC, PROCESSOR ELECTRONICS BD

DWG. NO. C 138-0020-20

MODEL

VERB.

PAGE

I-A

MODULE CODE TABLE

CODE	VENDOR	VENDORS P/N	DESCRIPTION			TOTAL NO OF PINS
				+5V	GND	
H00	TI	SN74H00	QUAD 2-INPUT NAND	14	7	14
H04	TI	SN74H04	HEX INVERTER	14	7	14
H08	SP	US74H08A	QUAD 2-INPUT AND	14	7	14
H10	TI	SN74H10	TRIPLE 3-INPUT NAND	14	7	14
H11	TI	SN74H11	TRIPLE 3-INPUT AND	14	7	14
H20	TI	SN74H20	DUAL 4-INPUT NAND	14	7	14
H21	TI	SN74H21	DUAL 4-INPUT AND	14	7	14
H30	TI	SN74H30	8-INPUT NAND	14	7	14
H37	SP	US74H37A	QUAD 2-INPUT NAND BUFF	14	7	14
H38	SP	US74H38A	QUAD 2-INPUT NAND BUFF OC	14	7	14
H54	TI	SN74H54	EXP 2-2-2-3 INPUT AOI	14	7	14
74	TI	SN7474	DUAL D-TYPE FLIP FLOP	14	7	14
86	TI	SN7486	QUAD 2-INPUT EXCLUSIVE OR	14	7	14
175	TI	SN74175	QUAD D-TYPE FLIP FLOP	16	8	16
283	TI	SN74283	4 BIT BINARY ADD W/CARRY	16	8	16
17	TI	SN7413	DUAL SCHMITT TRIGGER	14	7	14

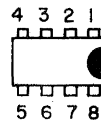
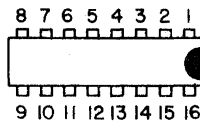
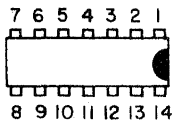


TABLE OF GND PINS TO CONTROL PANEL

93	98	102	104	108	115	116
120	126	132	135	136	137	138

TABLE OF GND PINS TO MEMORY

1	14	15	28	29	41	42	49
50	51	52	53	54	55	56	

TABLE OF GND PINS TO COMMUNICATIONS INTERFACE

66	67	68	69	70	71	76
----	----	----	----	----	----	----

TABLE OF 5 VOLT PINS TO MEMORY

43	44	45	46	47	48
----	----	----	----	----	----

TABLE OF 5 VOLT PINS TO COMMUNICATIONS INTERFACE

84	85	86
----	----	----

TABLE OF GND CONTACTS ON EDGE CONNECTOR

9	11	13	15	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47	49	51	53	
55	57	59	61	63	65	67	69	71	73	75	77	79	81	83	85	87	89	91	93	95	97	99	

TABLE OF 5 VOLT CONTACTS ON EDGE CONNECTOR

1	2	3	4	5	6	7	8
---	---	---	---	---	---	---	---

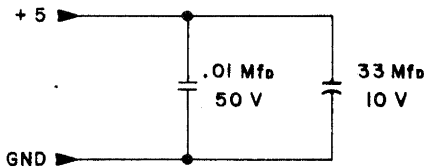
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		COLUMN										
		A	B	C	D	E	F	G	H	J	K	L
ROW	1						C1		C1		C1	
	2	C1	C1		C1		C1		C1		C1	
	3	C2	C1		C1		C2		C1		C1	
	4	C1	C1		C1		C1		C1		C1	
	5	C1	C1		C1		C1		C1		C1	
	6	C1	C2		C1		C1		C1		C1	
	7	C1	C1		C1		C1		C1		C1	
	8	C1	C1		C1		C1		C1		C1	
	9	C1	C1		C1		C2		C1		C1	
	10	C1	C1		C1		C1		C1			
	11	C1	C1		C1		C1		C1		C1-C2	
	12		C1		C1		C1		C1		C1	

COLUMN AND ROW DESIGNATION FOR LOCATION OF .01 Mfd 50 V DECOUPLING CAPACITORS.

		COLUMN										
		A	B	C	D	E	F	G	H	J	K	L
ROW	1	C1	C1									
	2											
	3						C1				C2	
	4											
	5											
	6		C1									
	7											
	8											
	9						C1					C1
	10											
	11											
	12											
	13		C1				C1				C1	

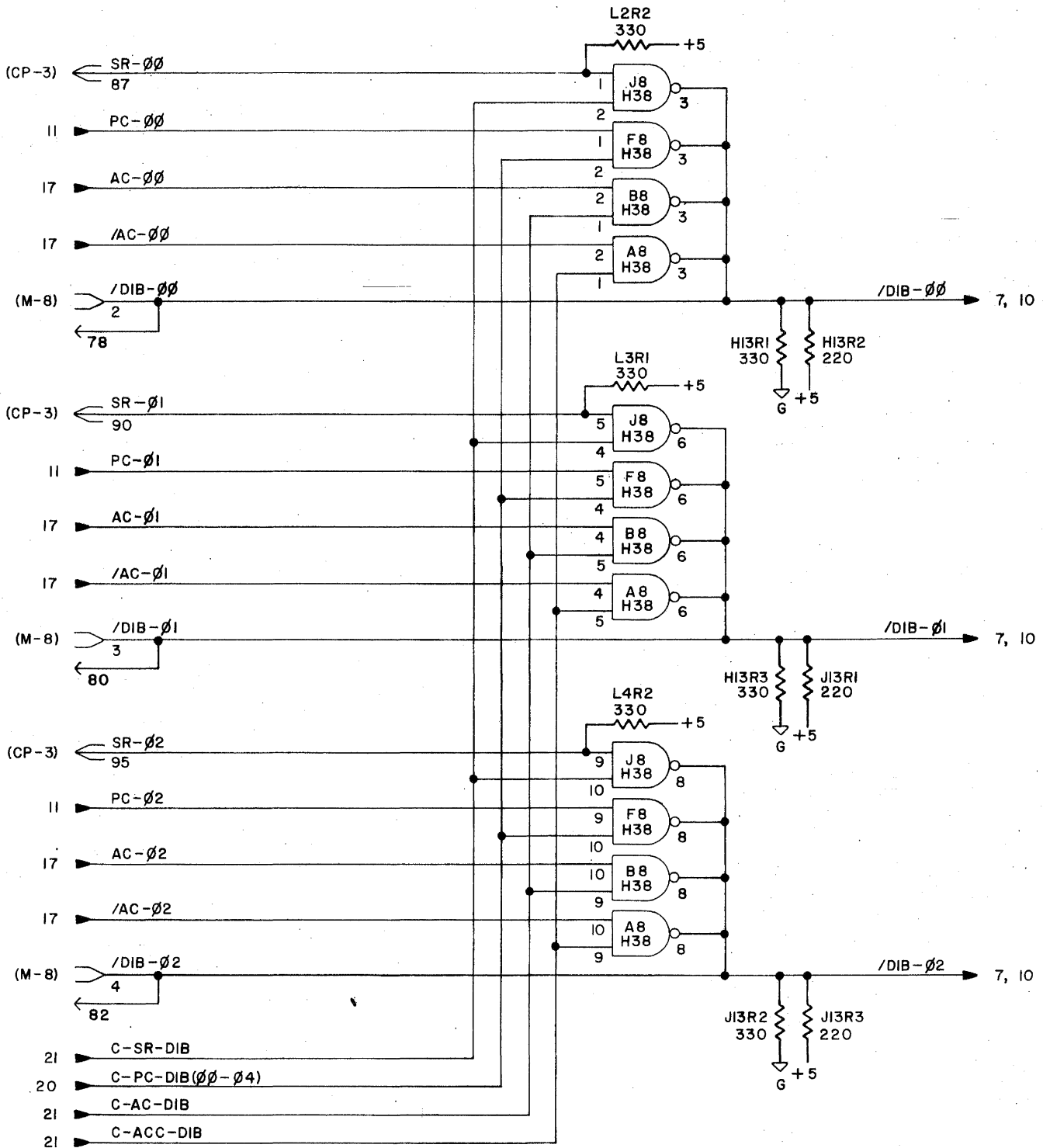
COLUMN AND ROW DESIGNATION FOR LOCATION OF 33 Mfd 10 V DECOUPLING CAPACITORS.



TYPICAL DECOUPLING CAPACITOR CONNECTION

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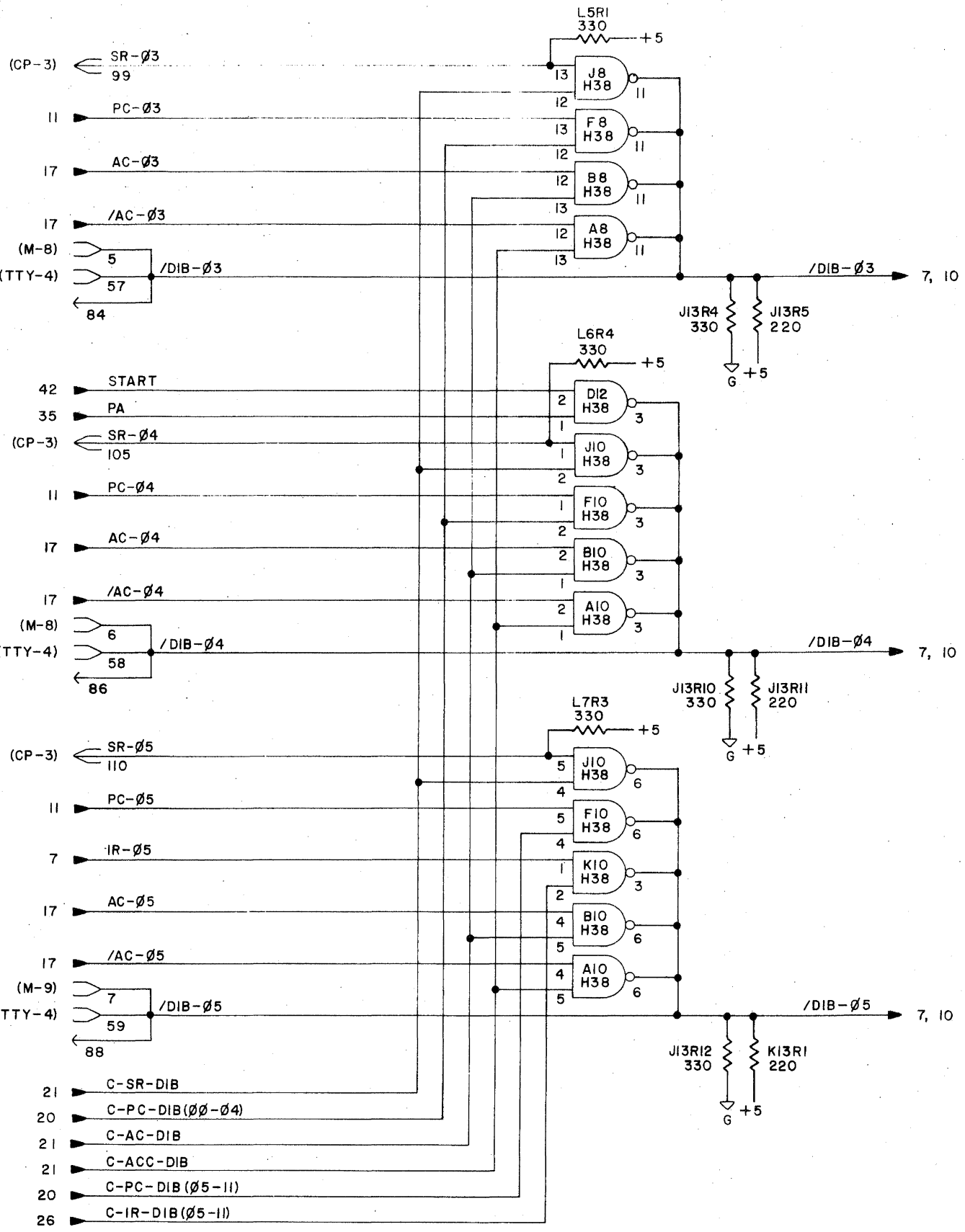
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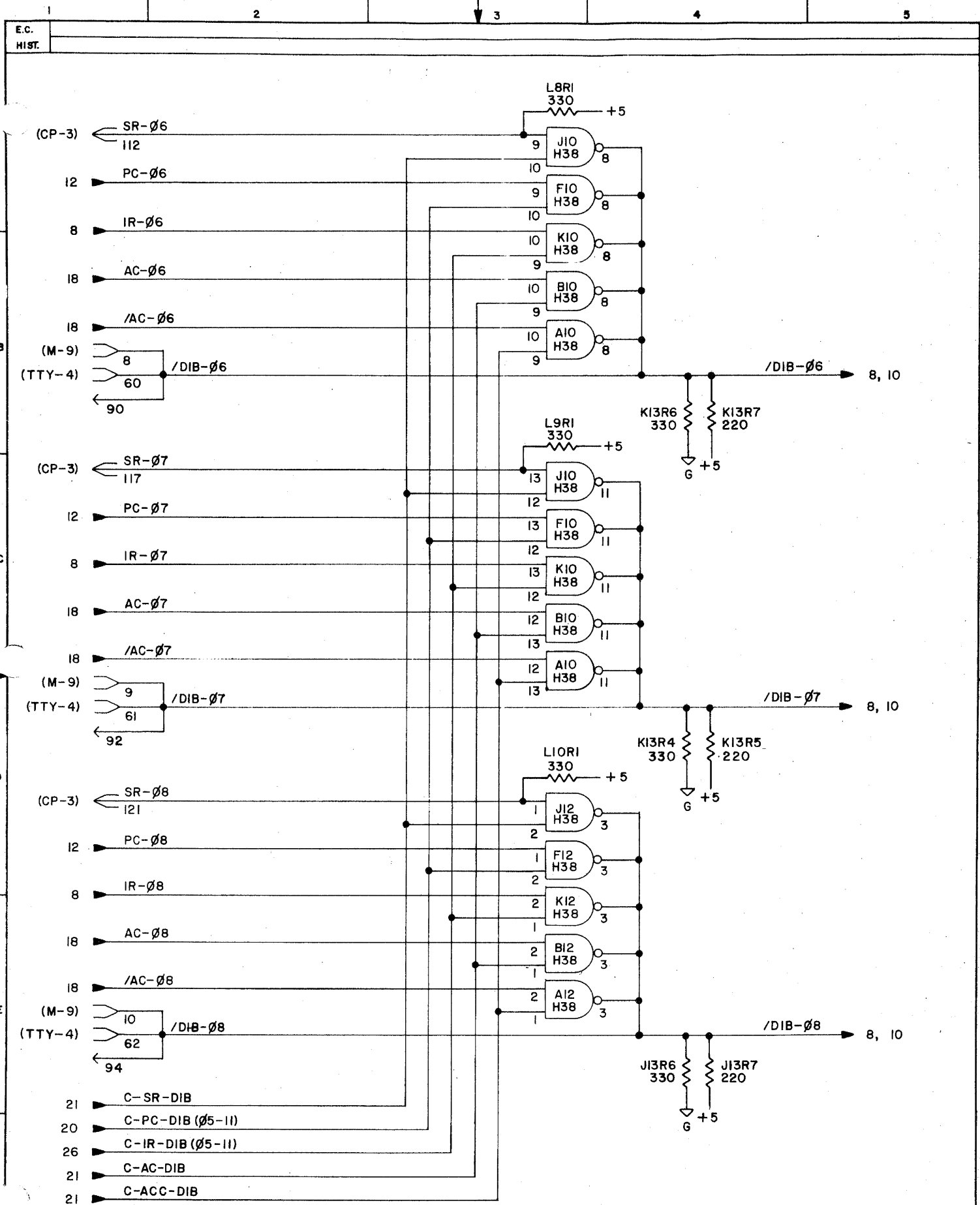
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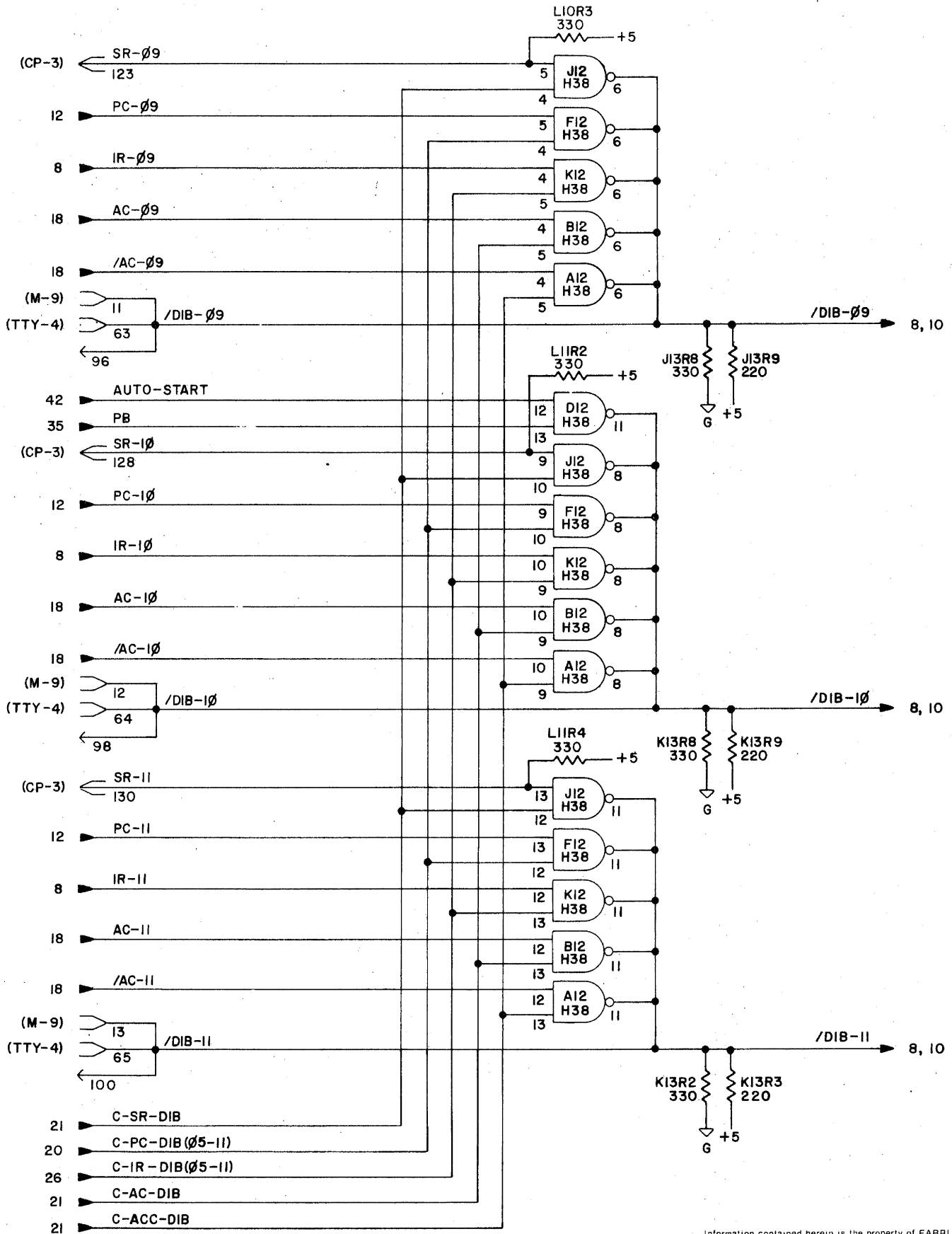
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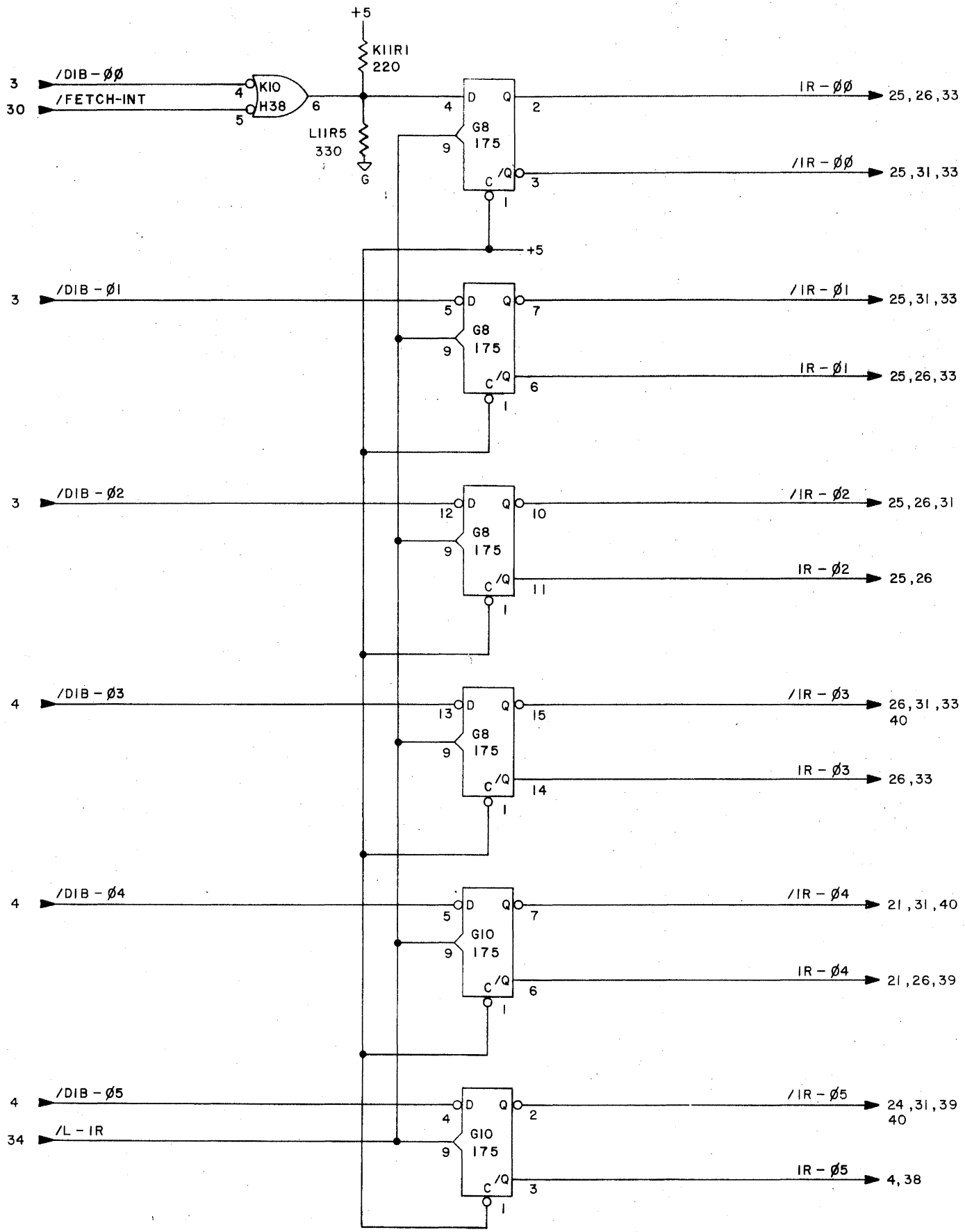


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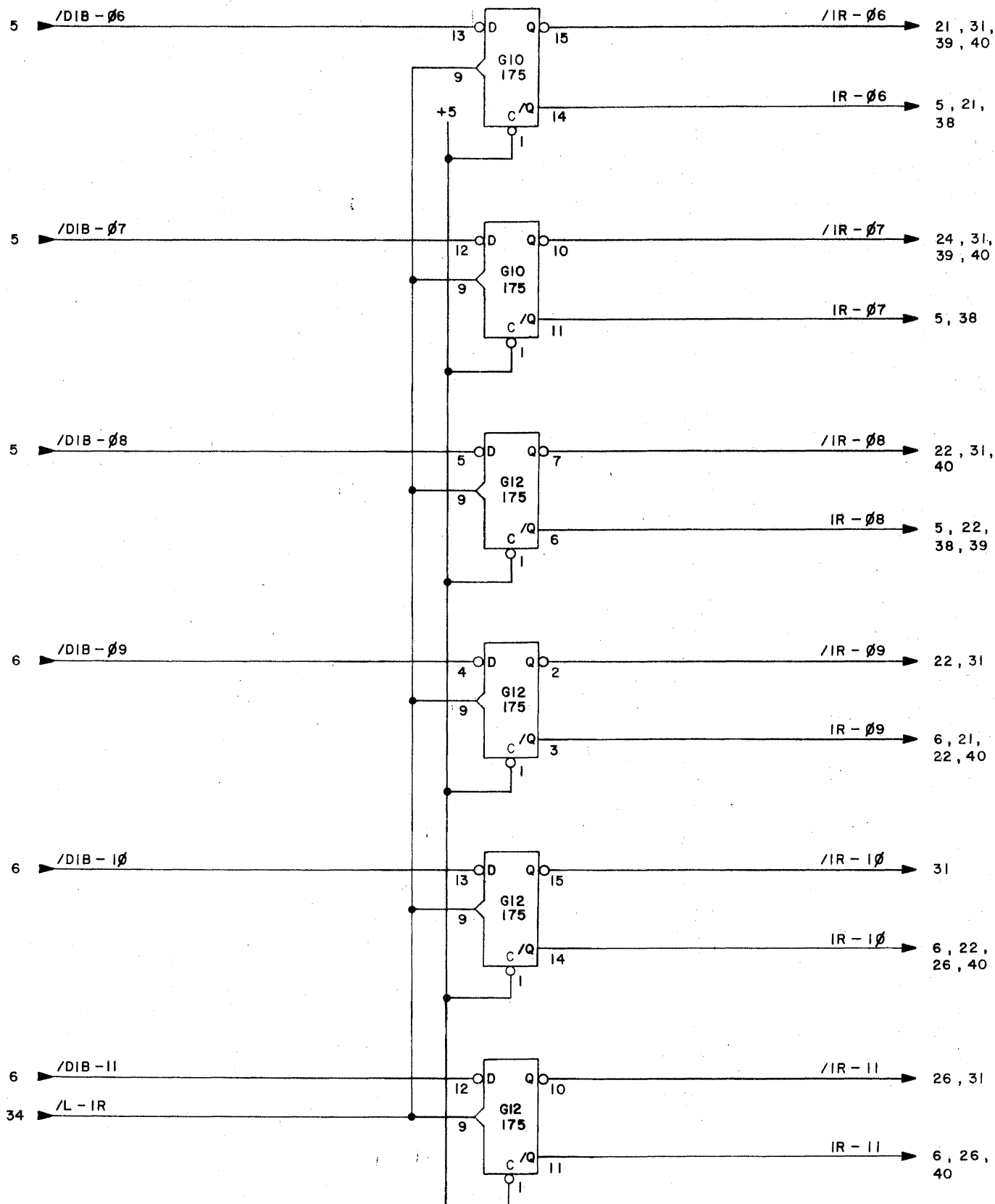


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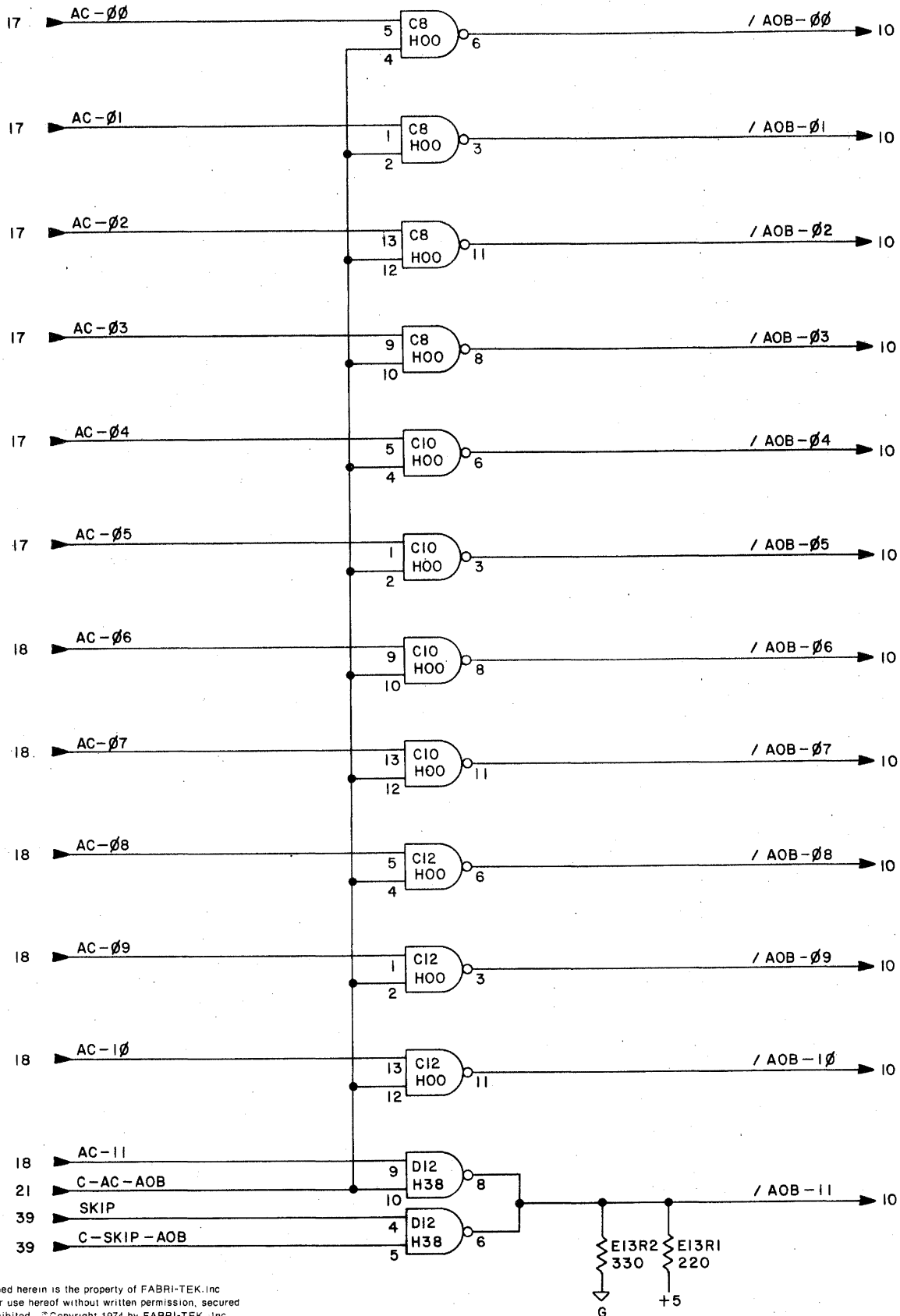


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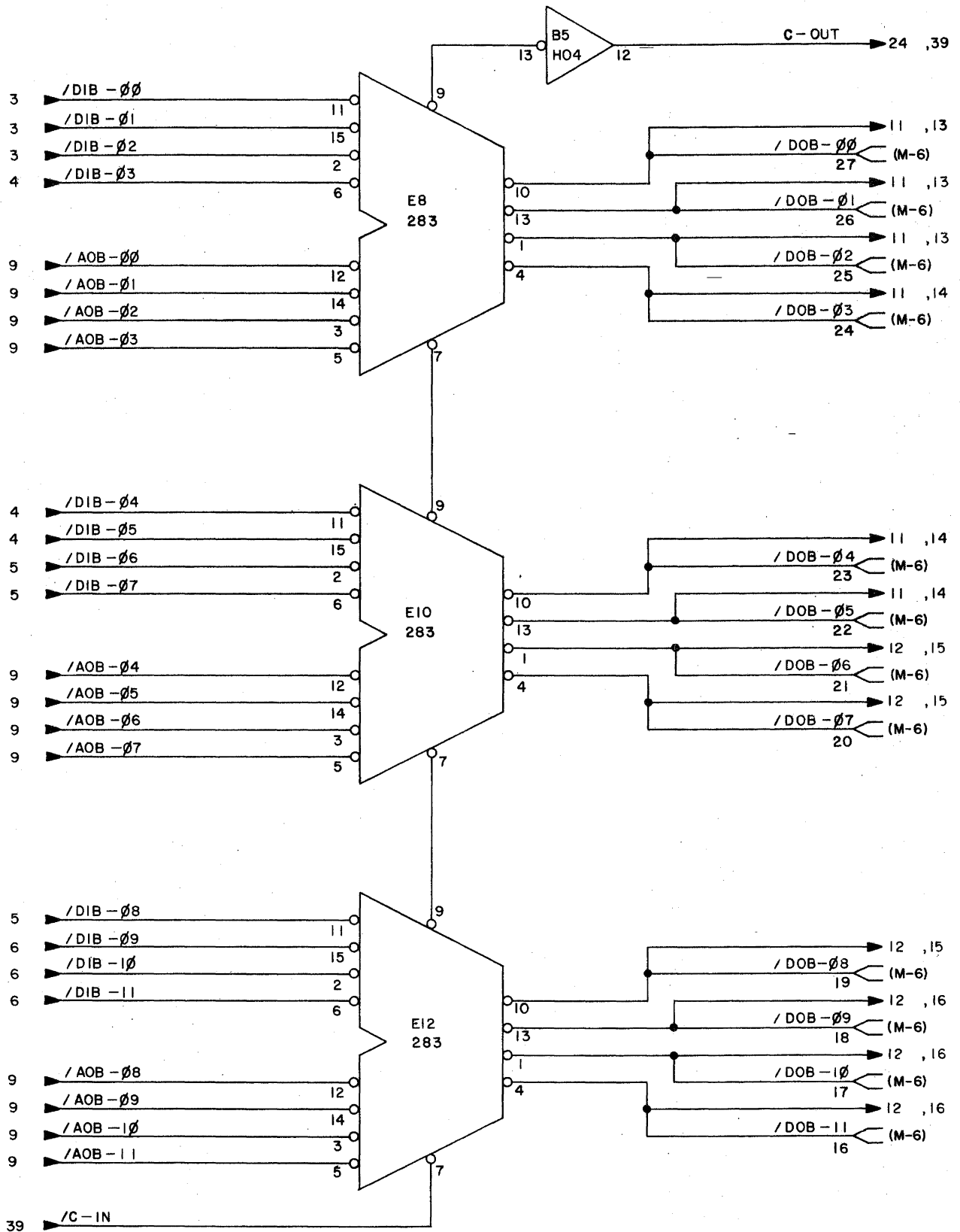
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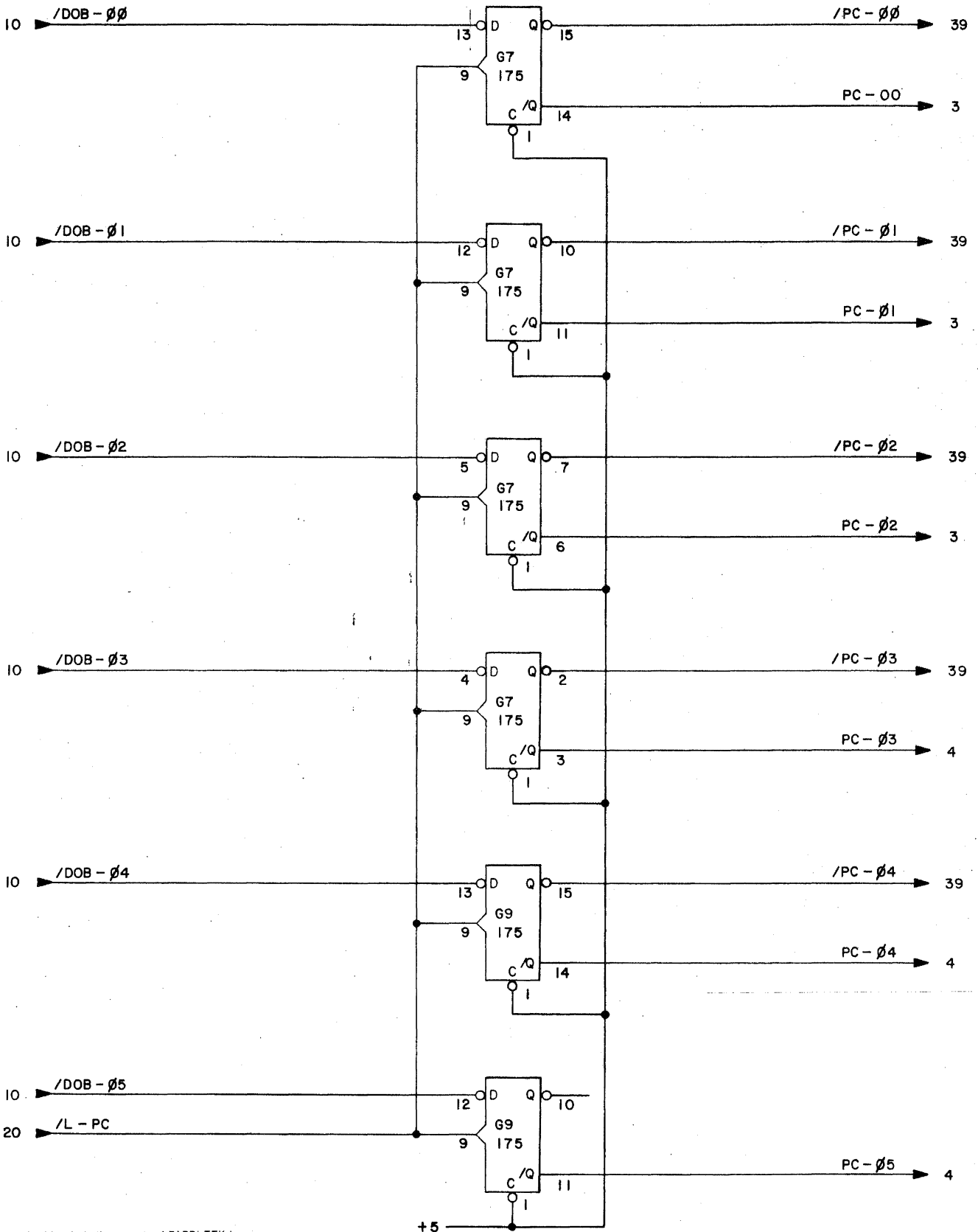
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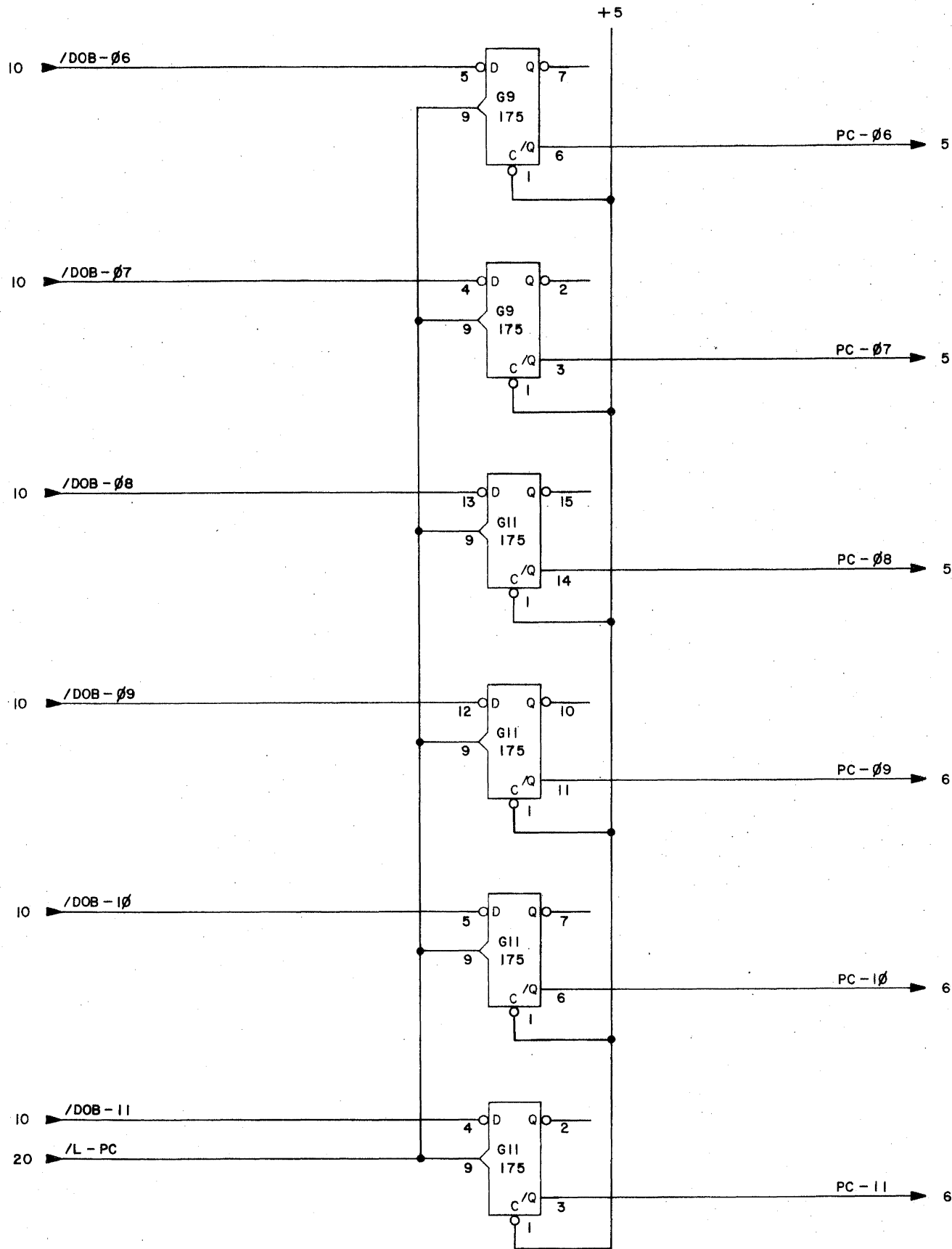
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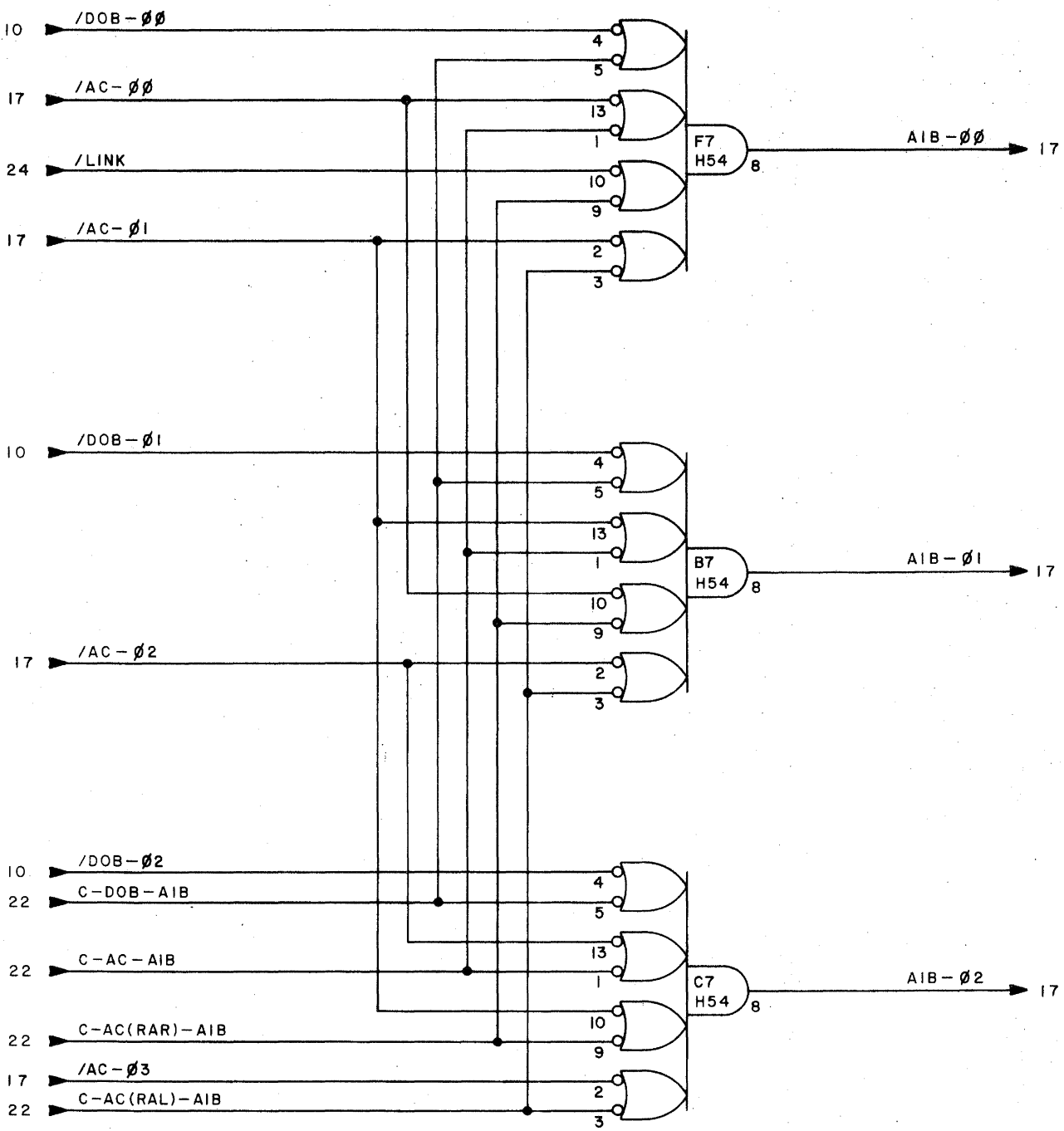
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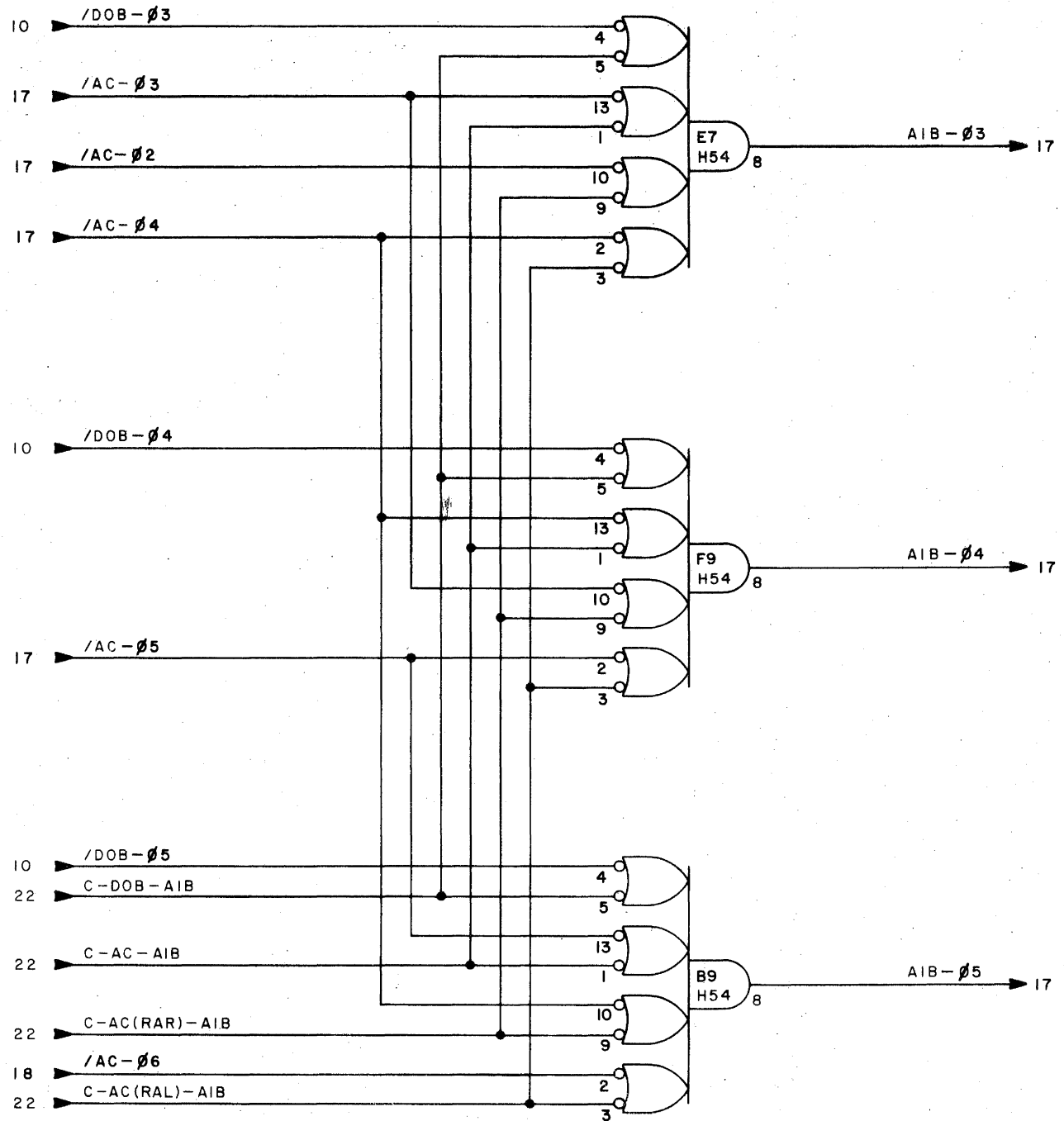


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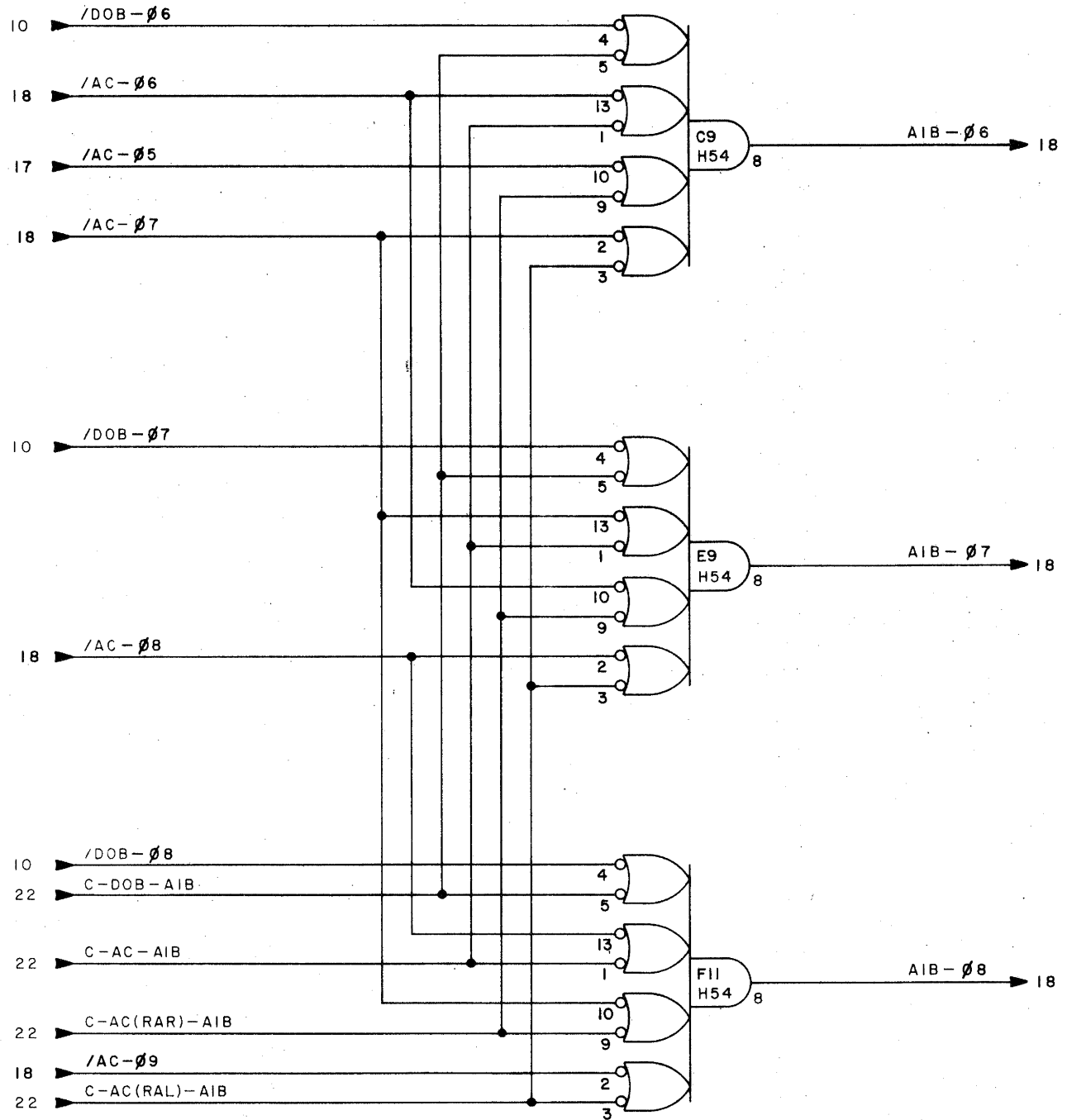
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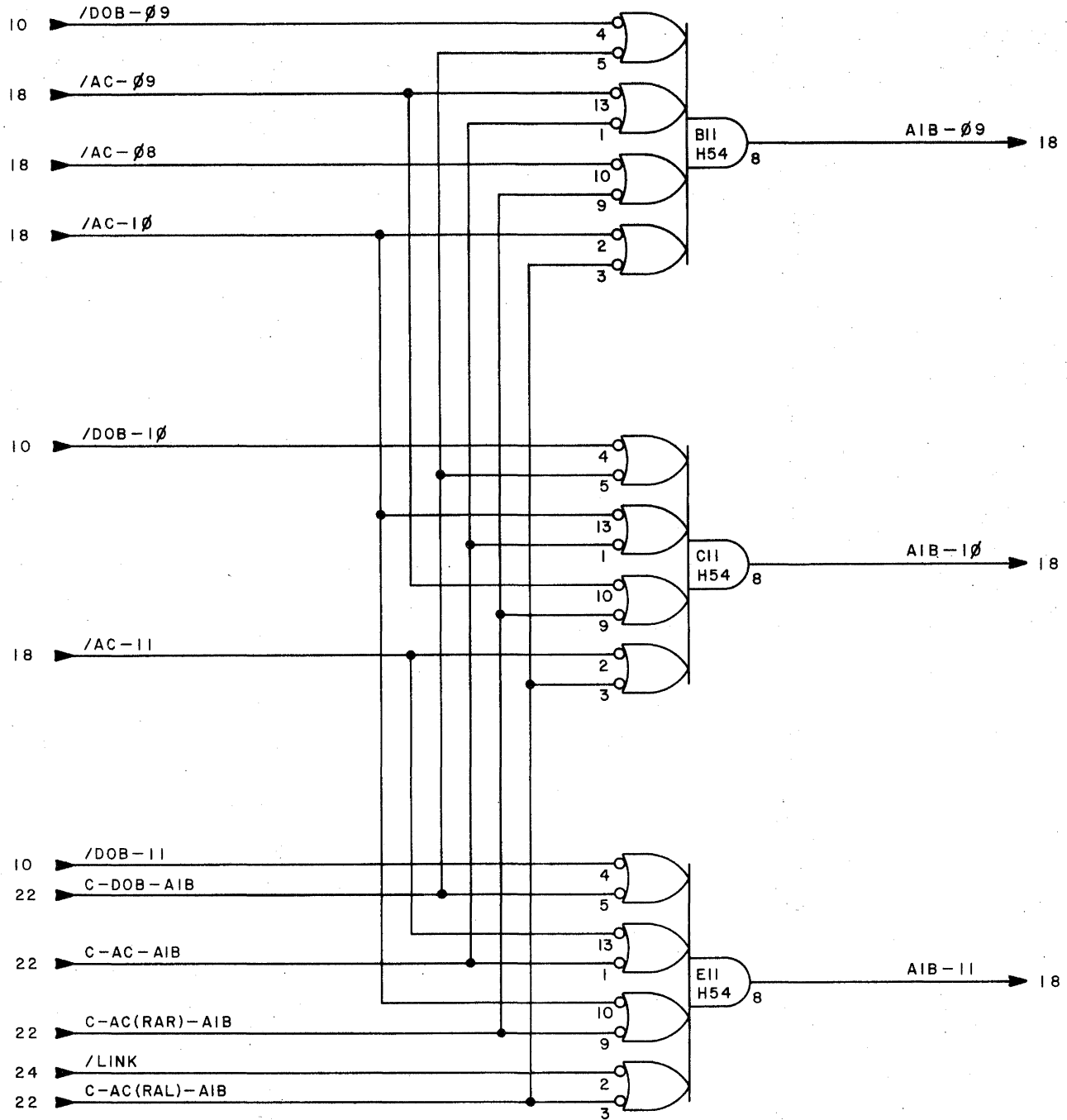
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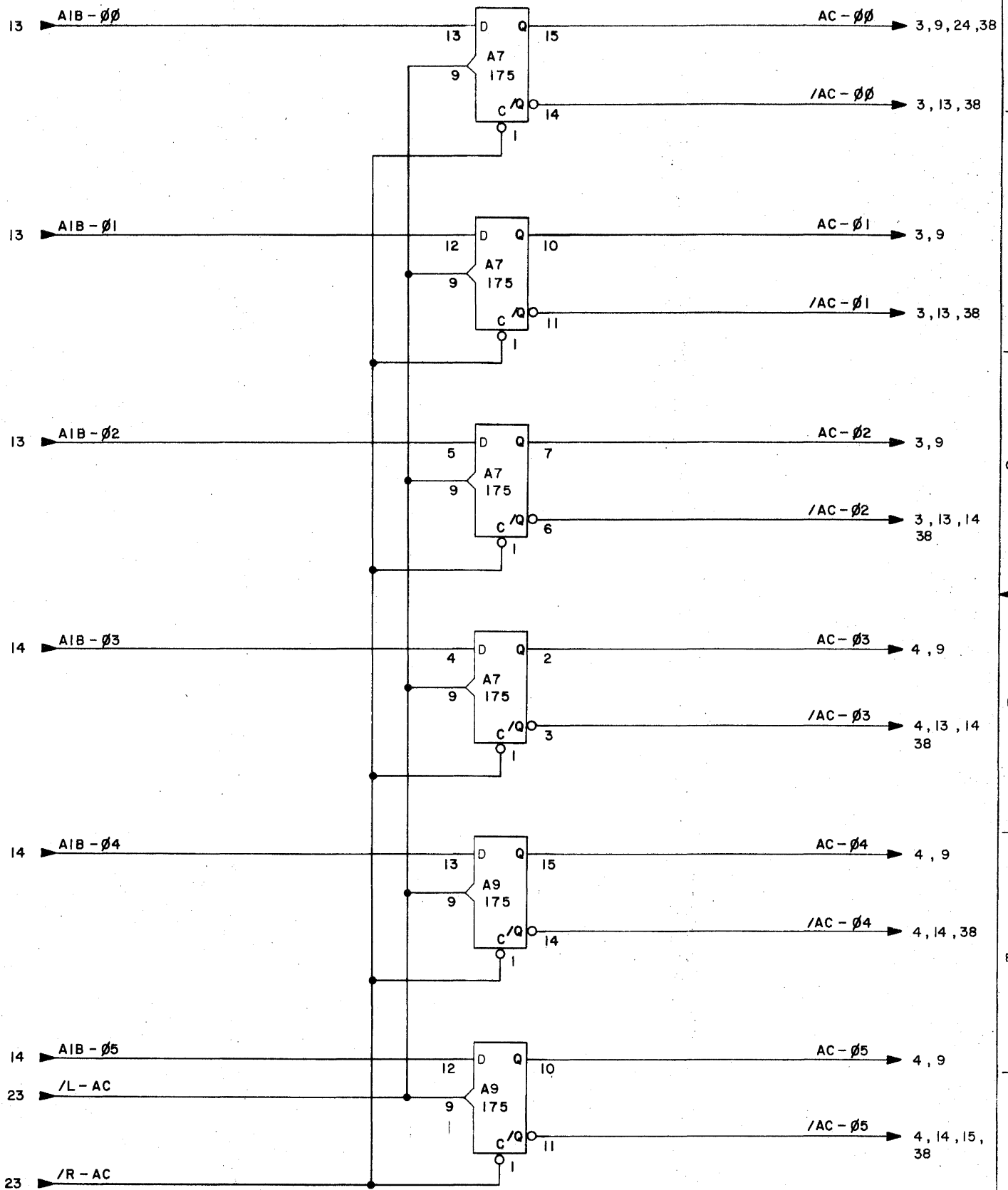
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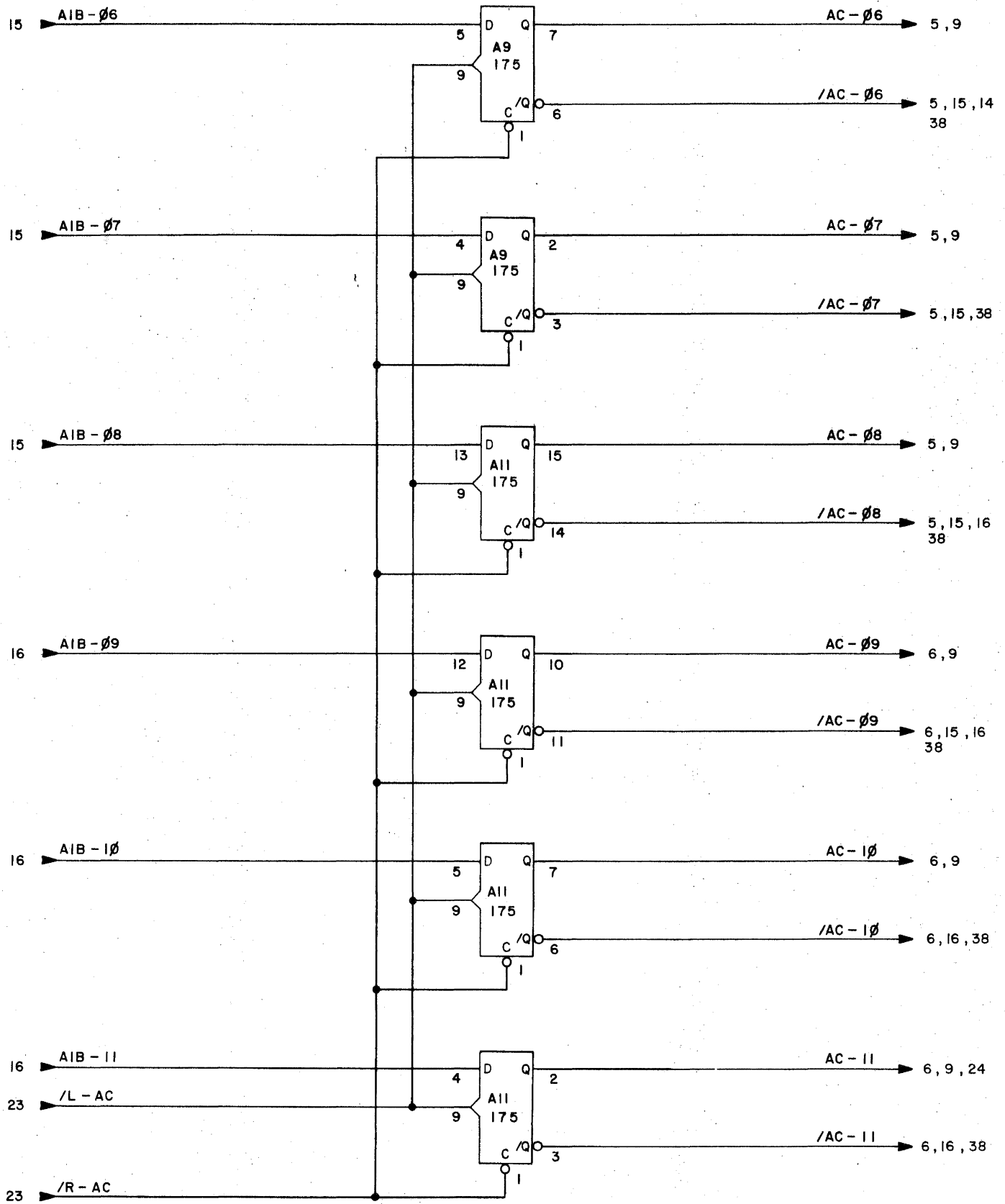


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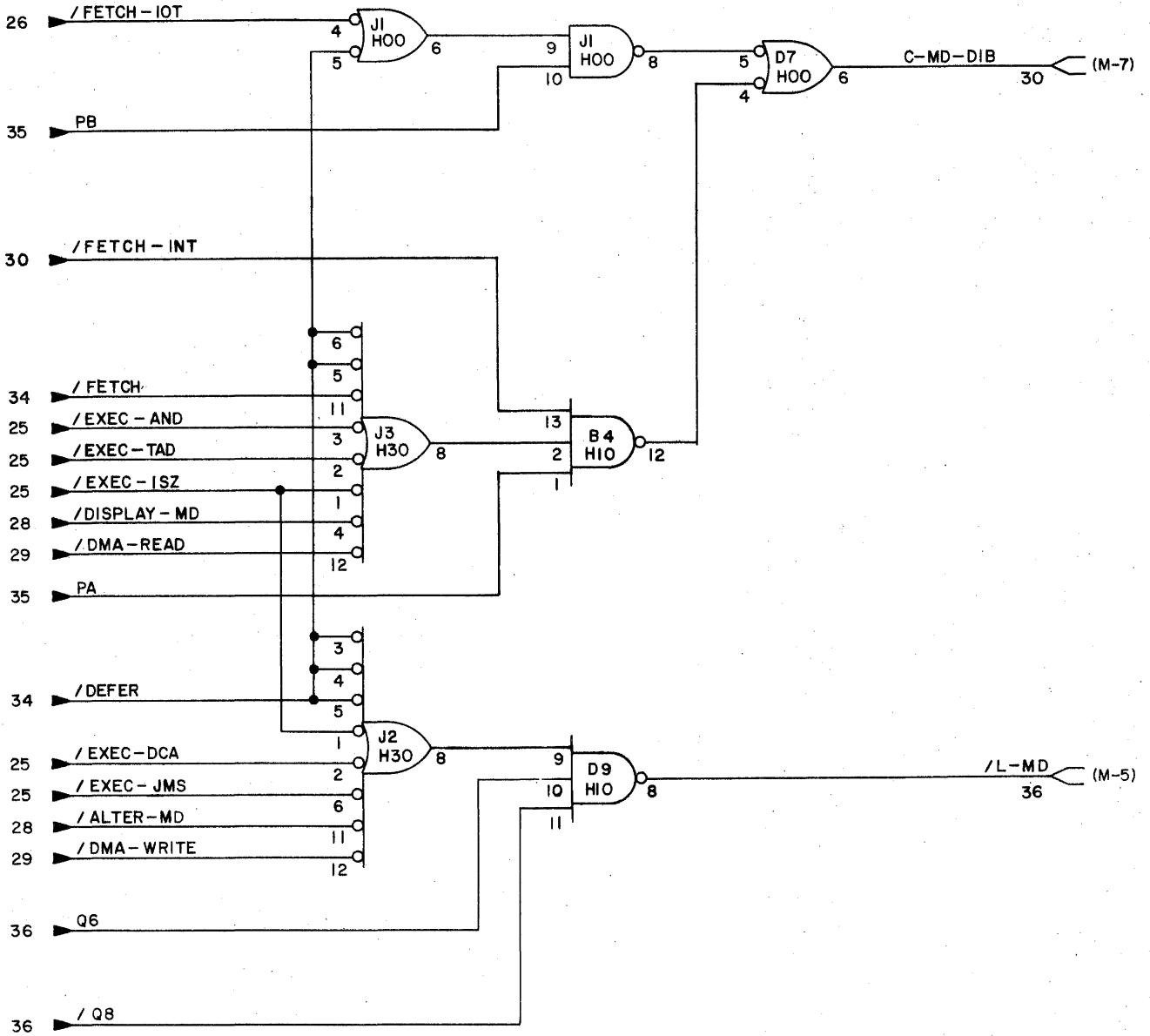


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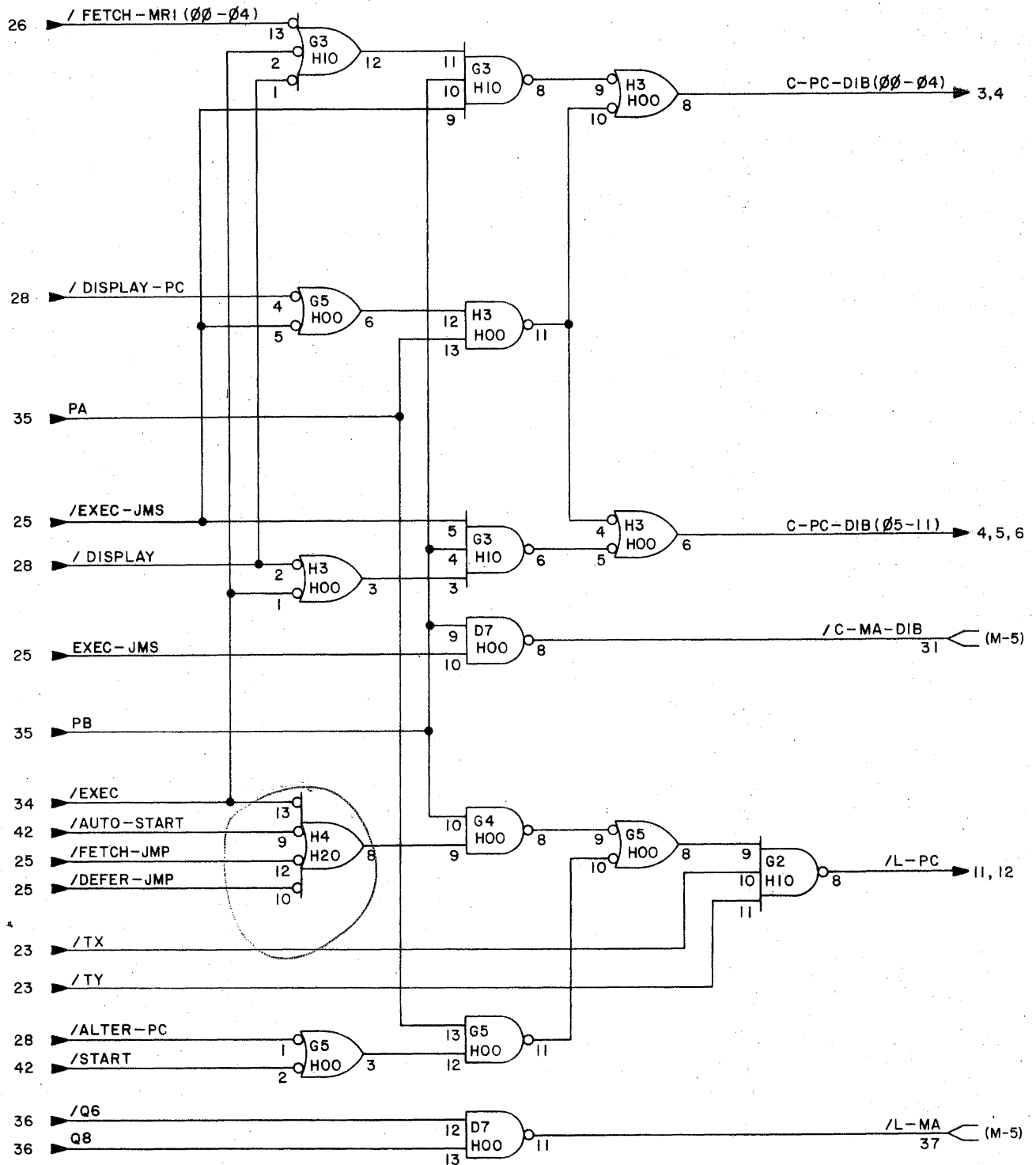
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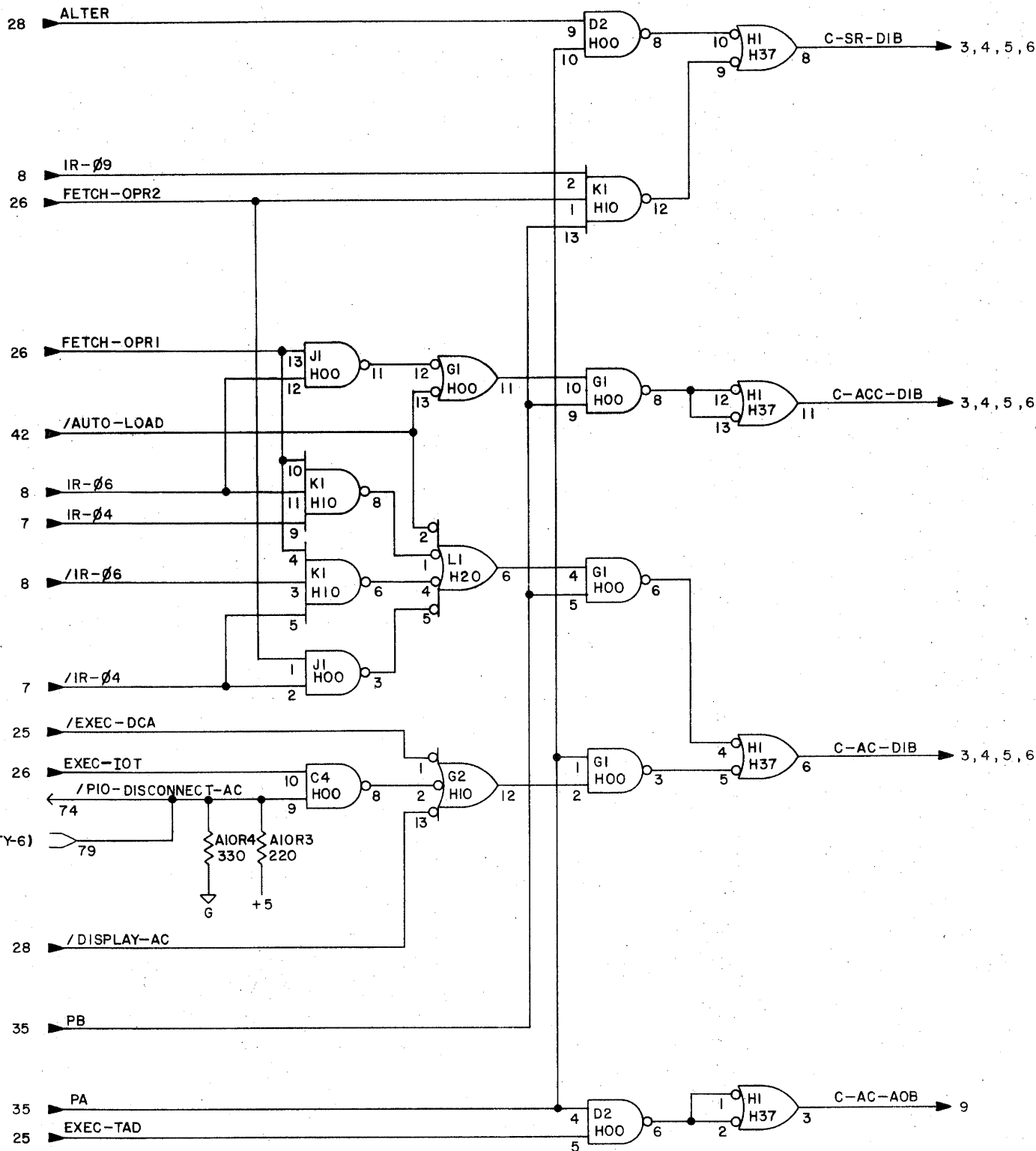


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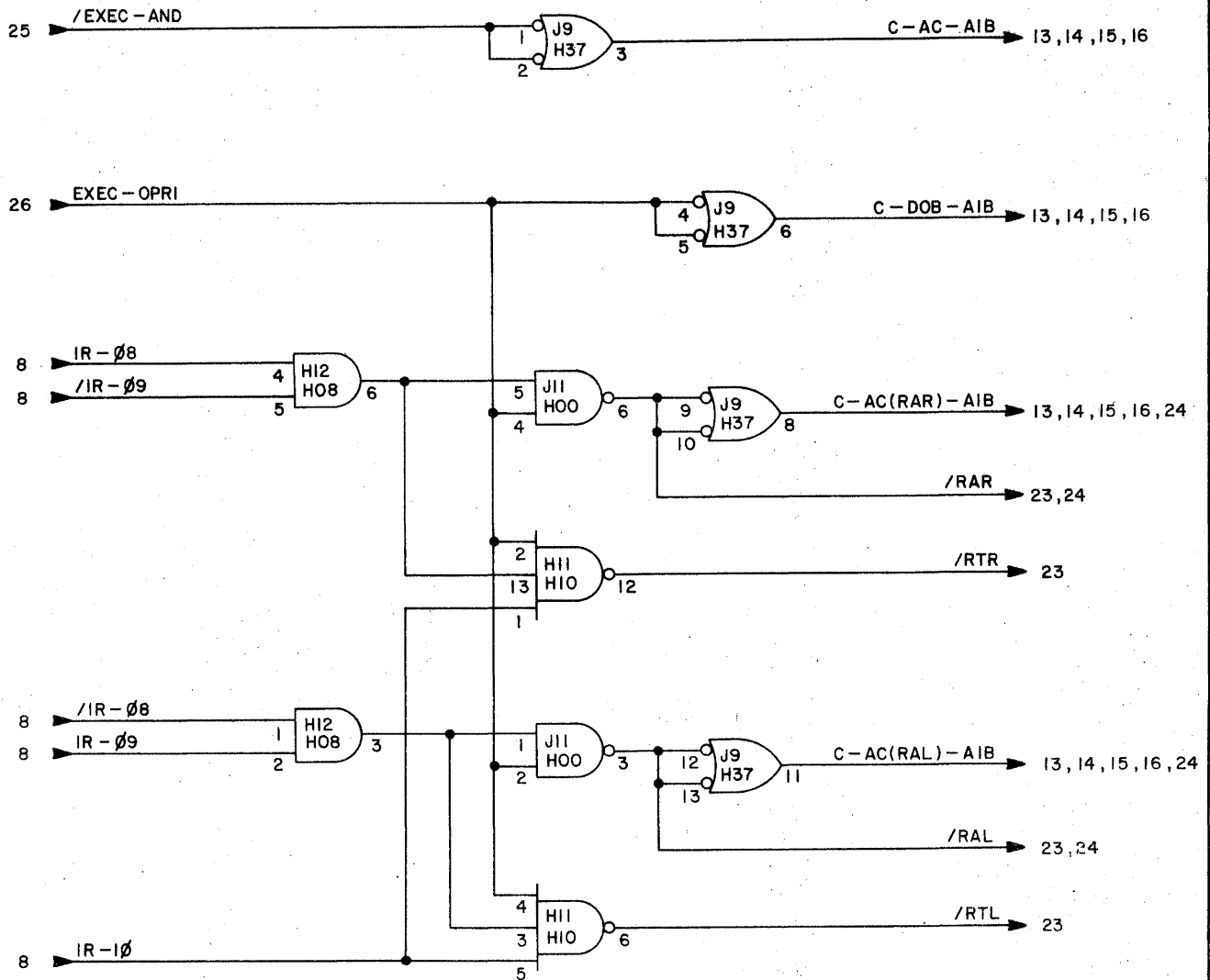
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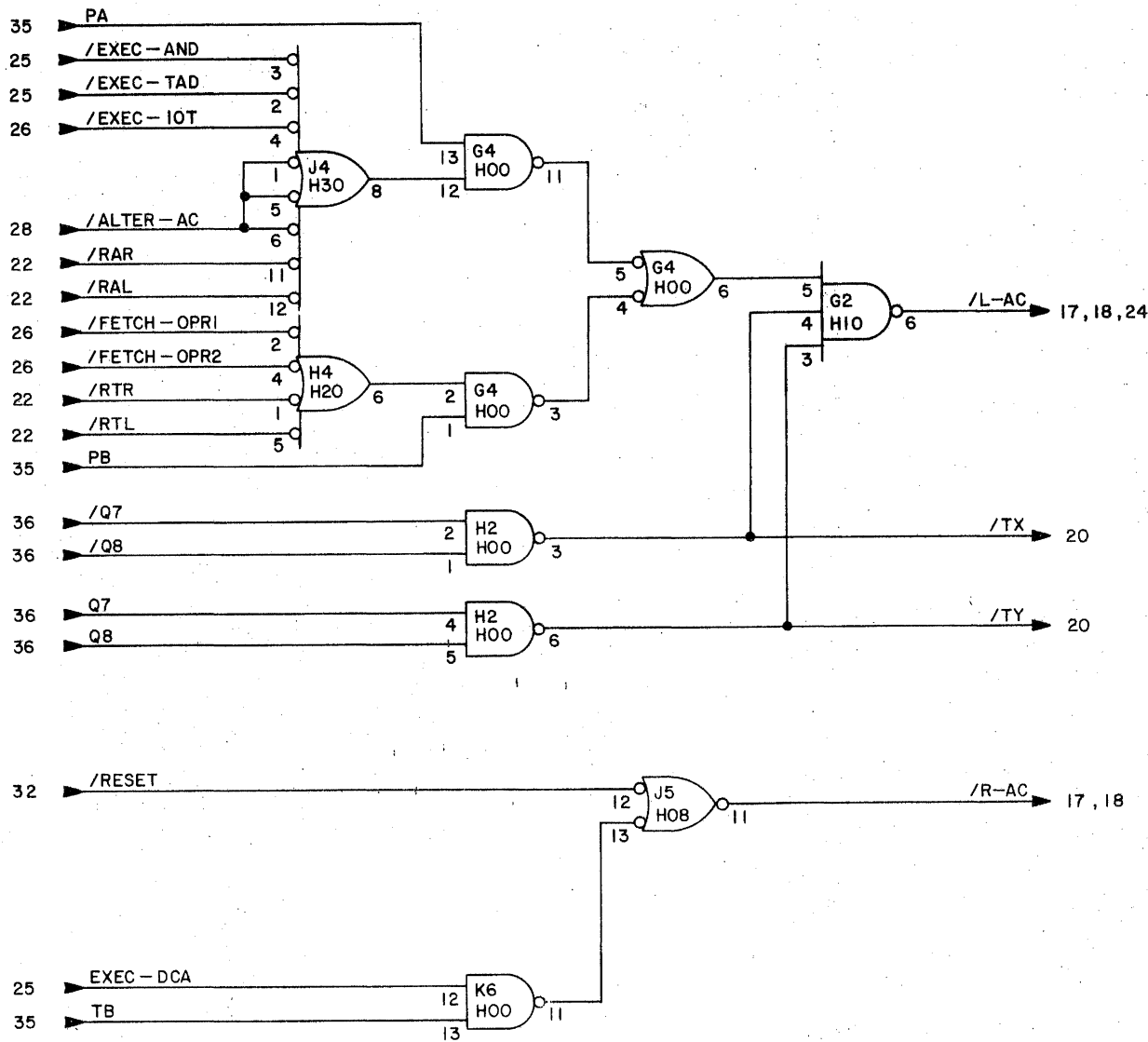
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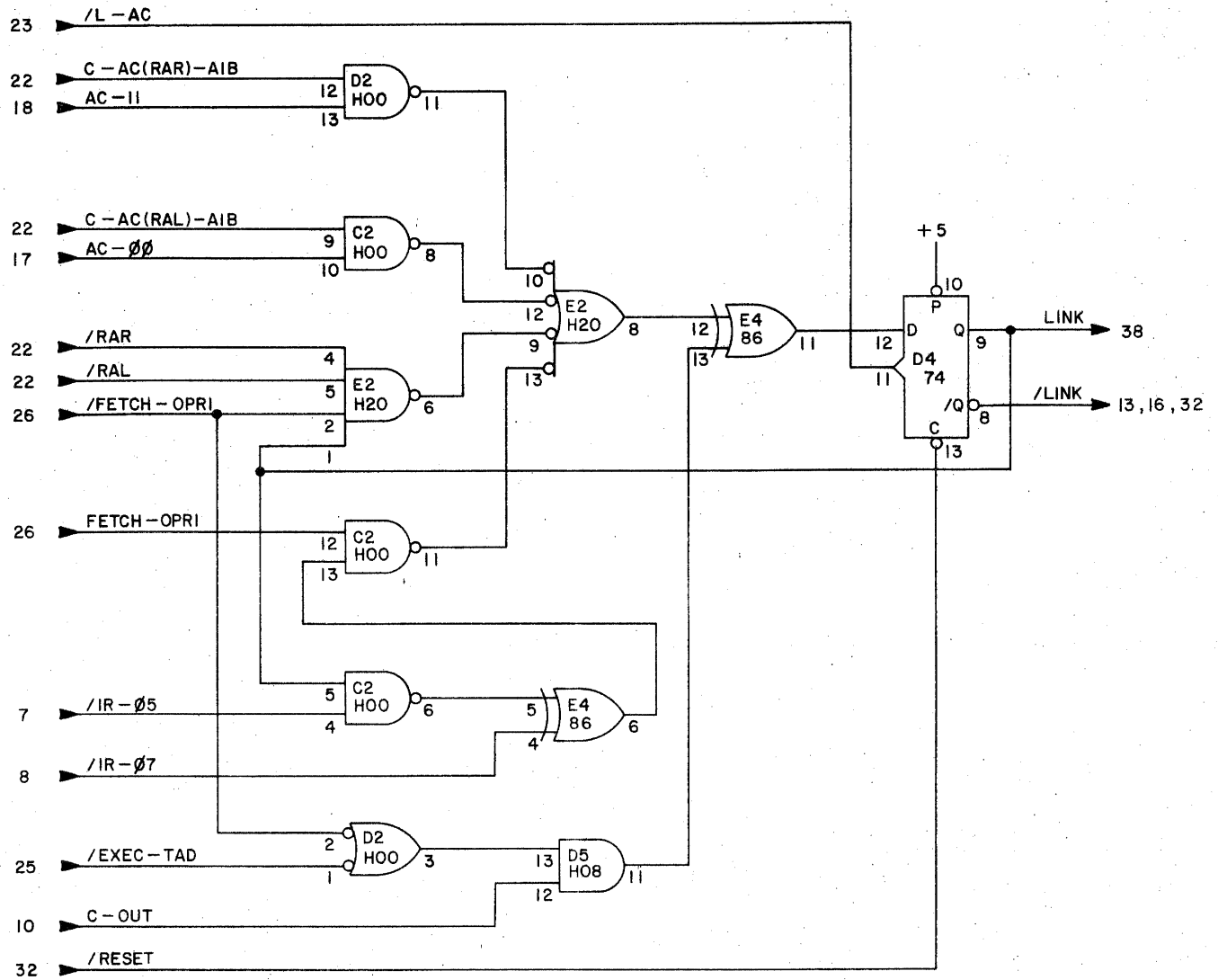
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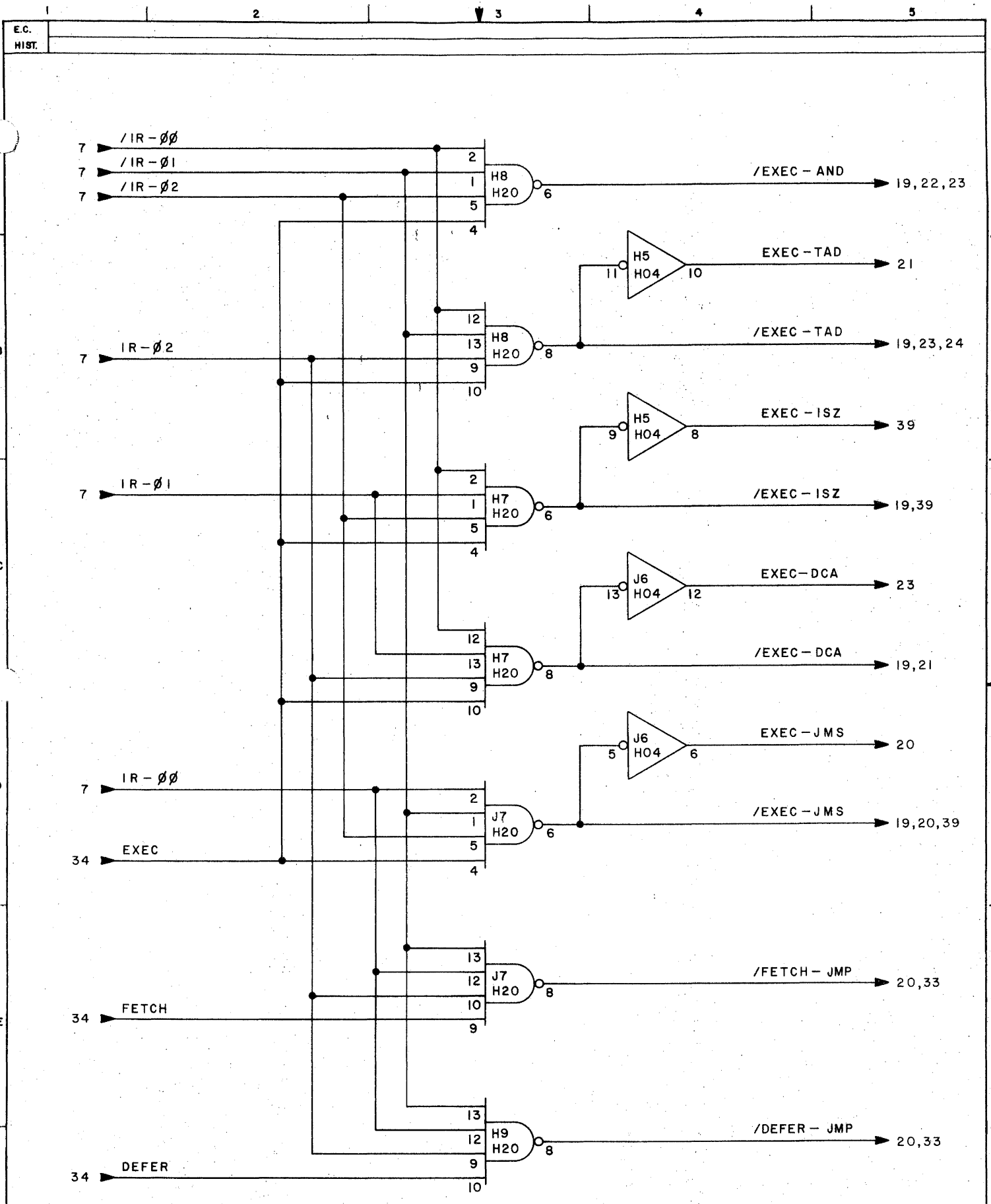
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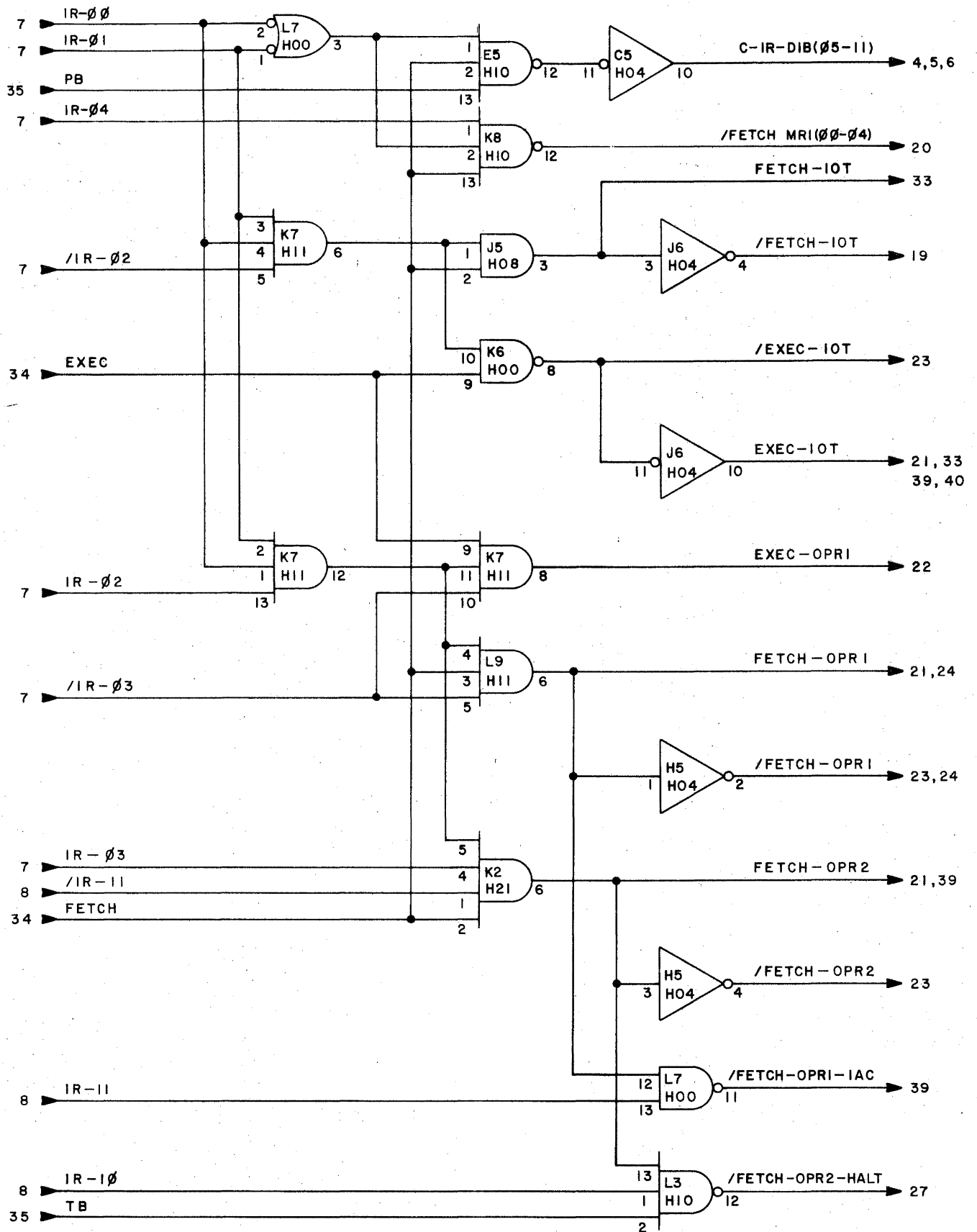


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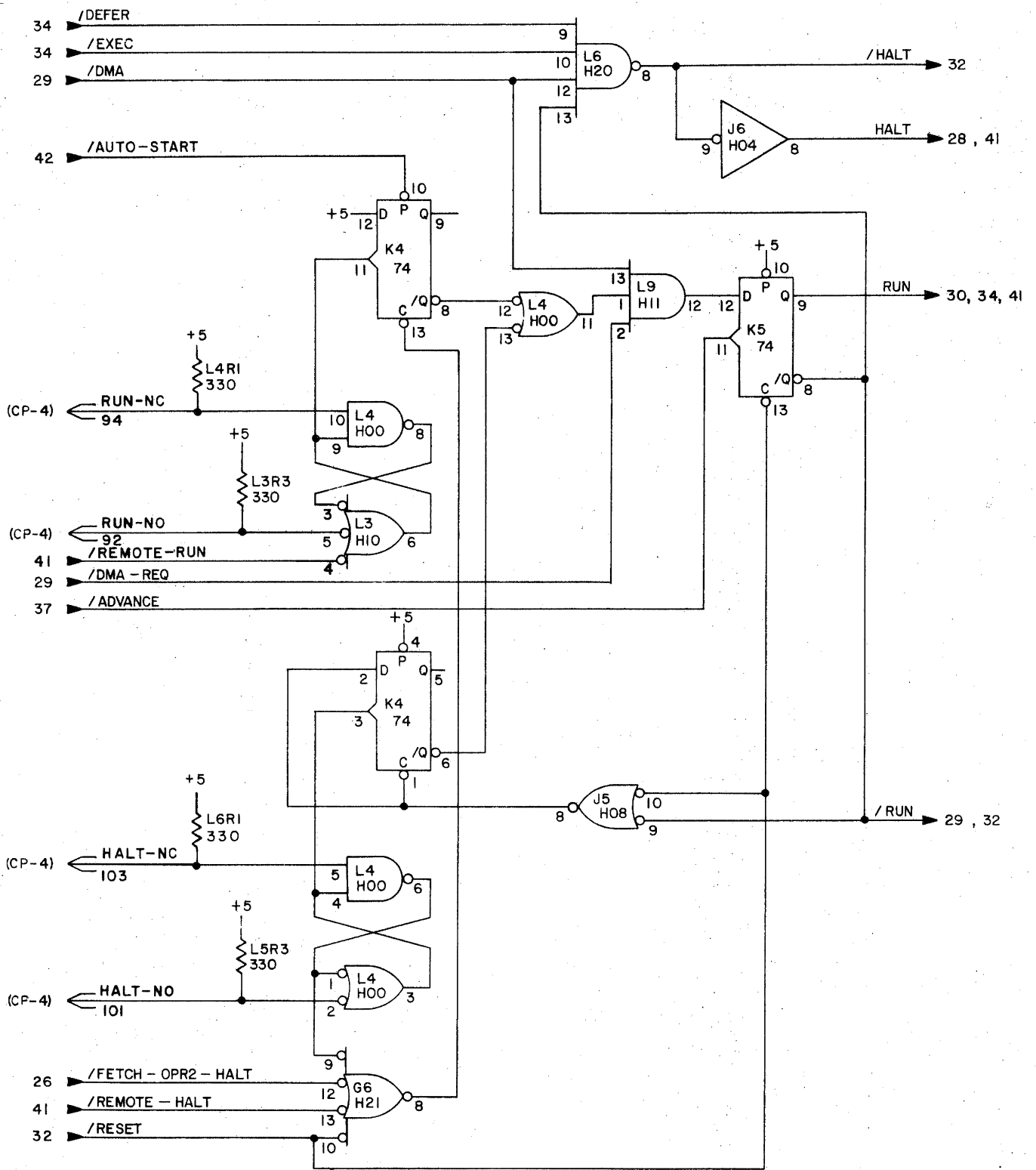


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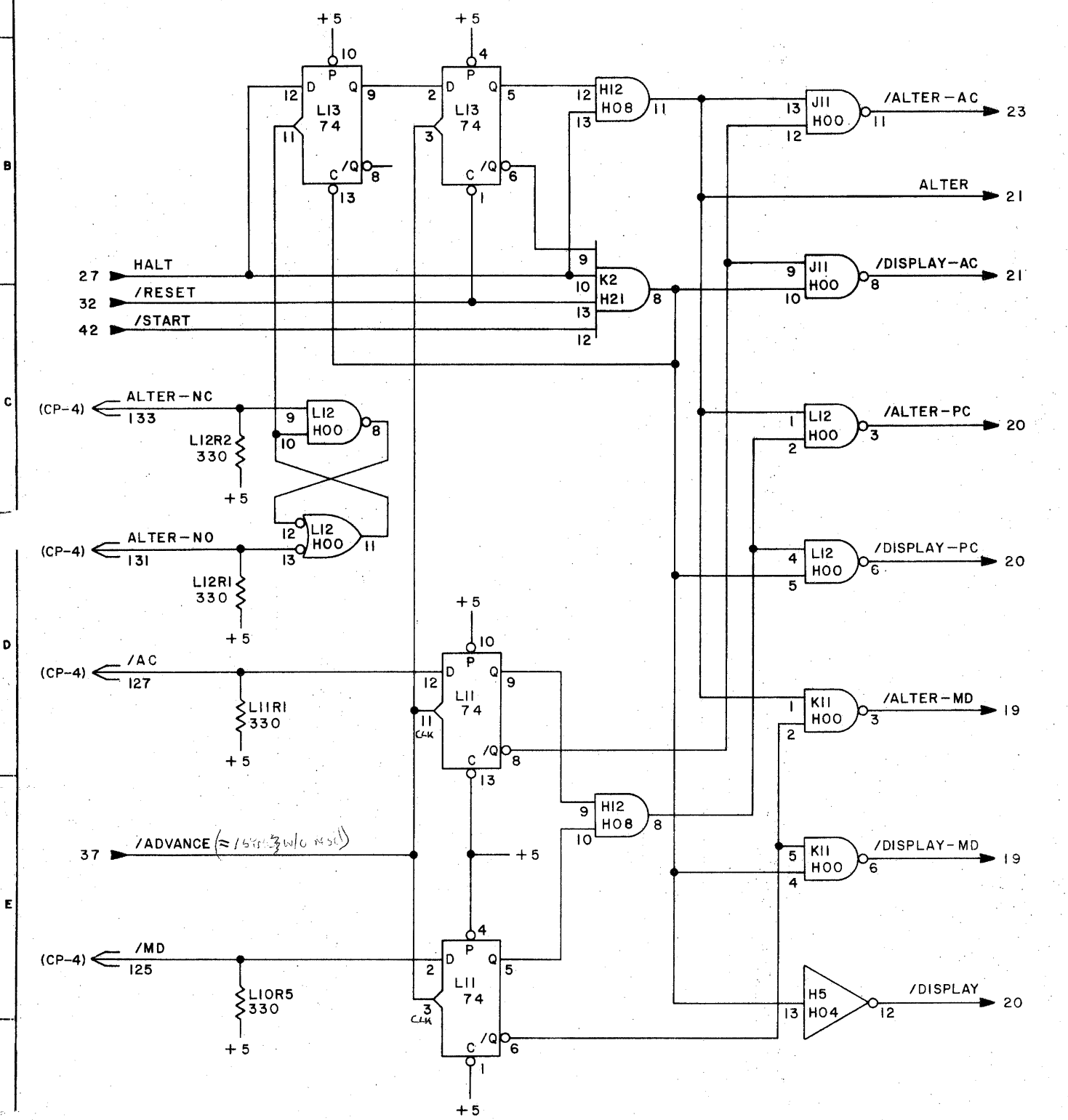
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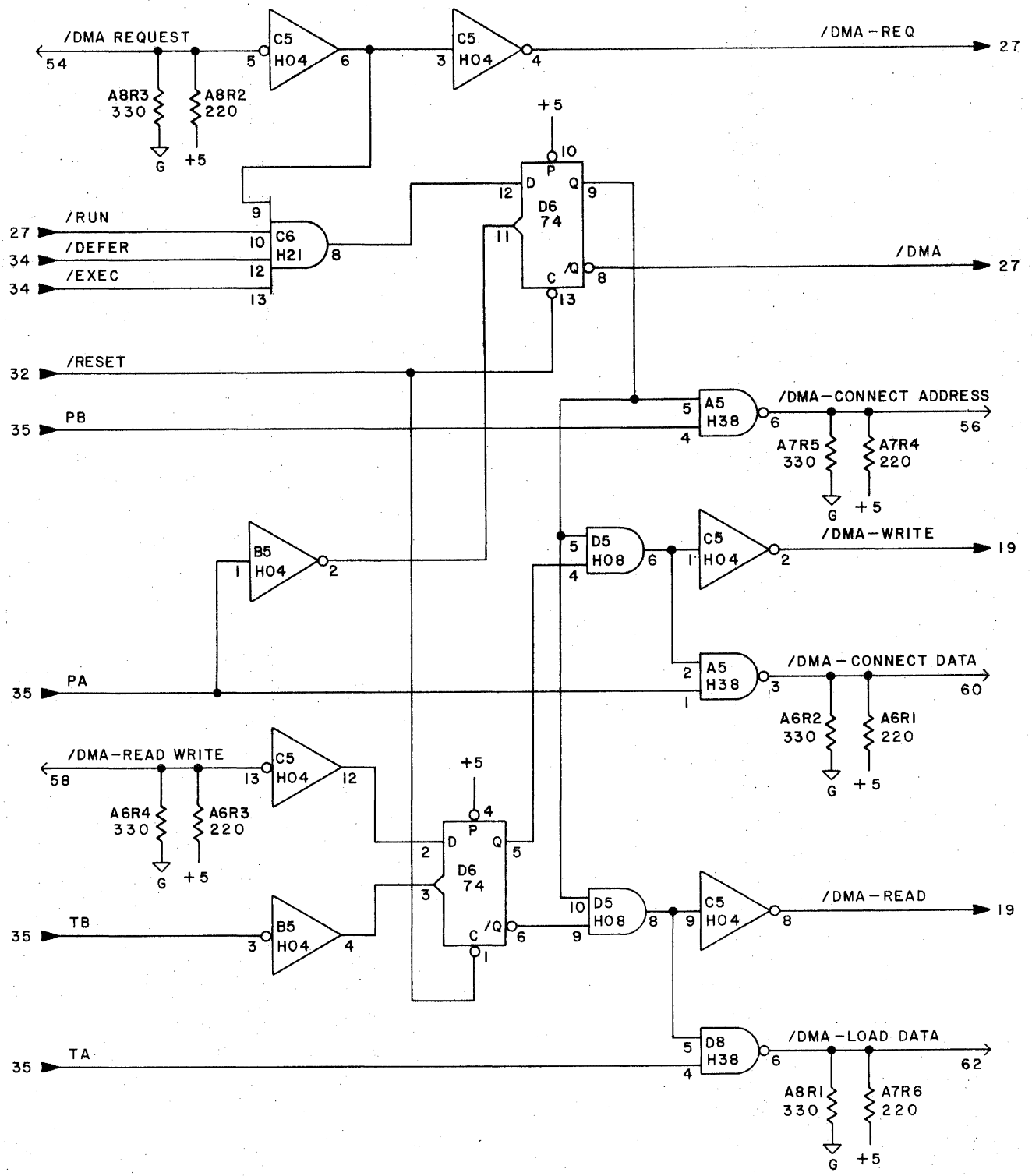
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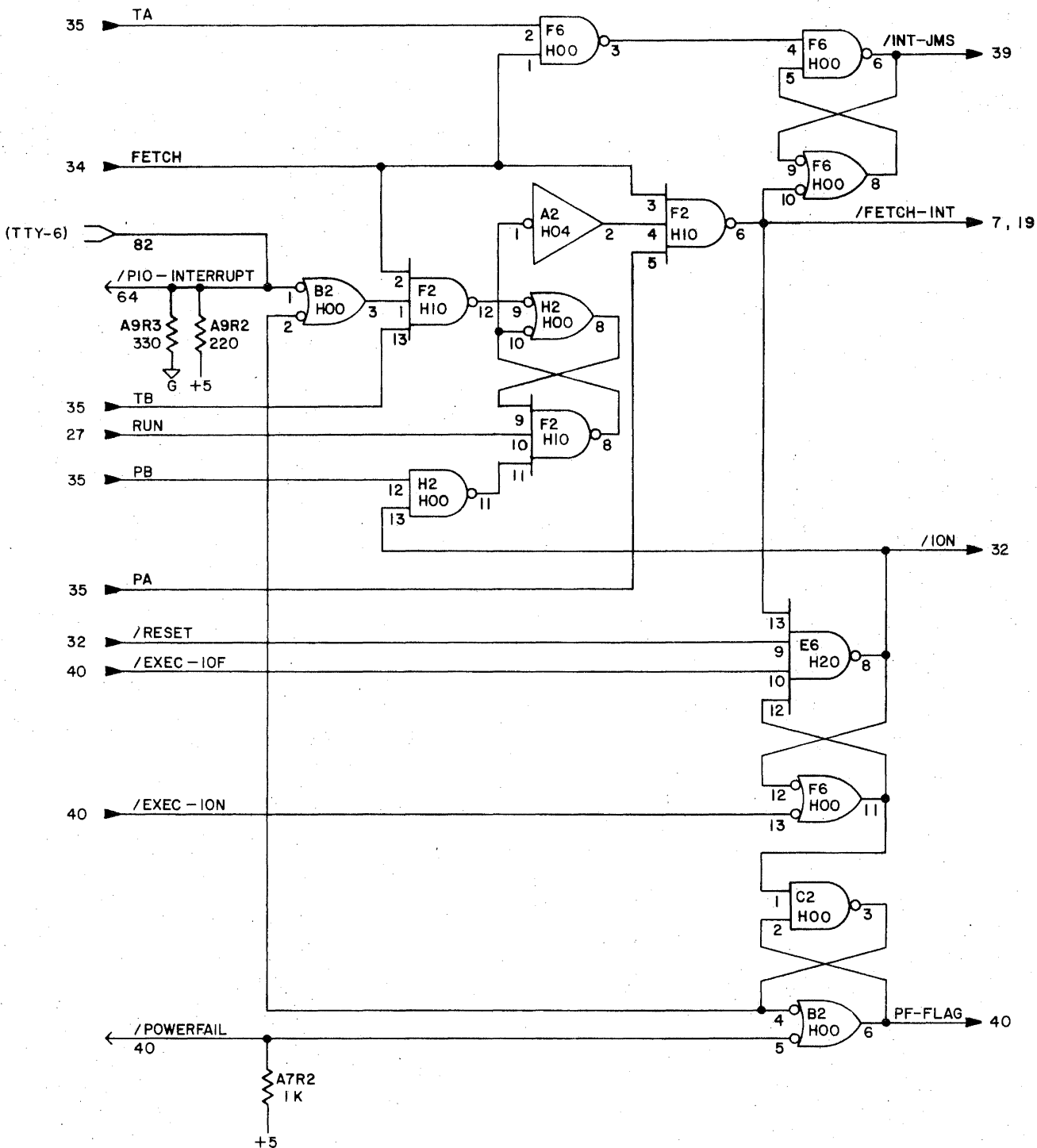
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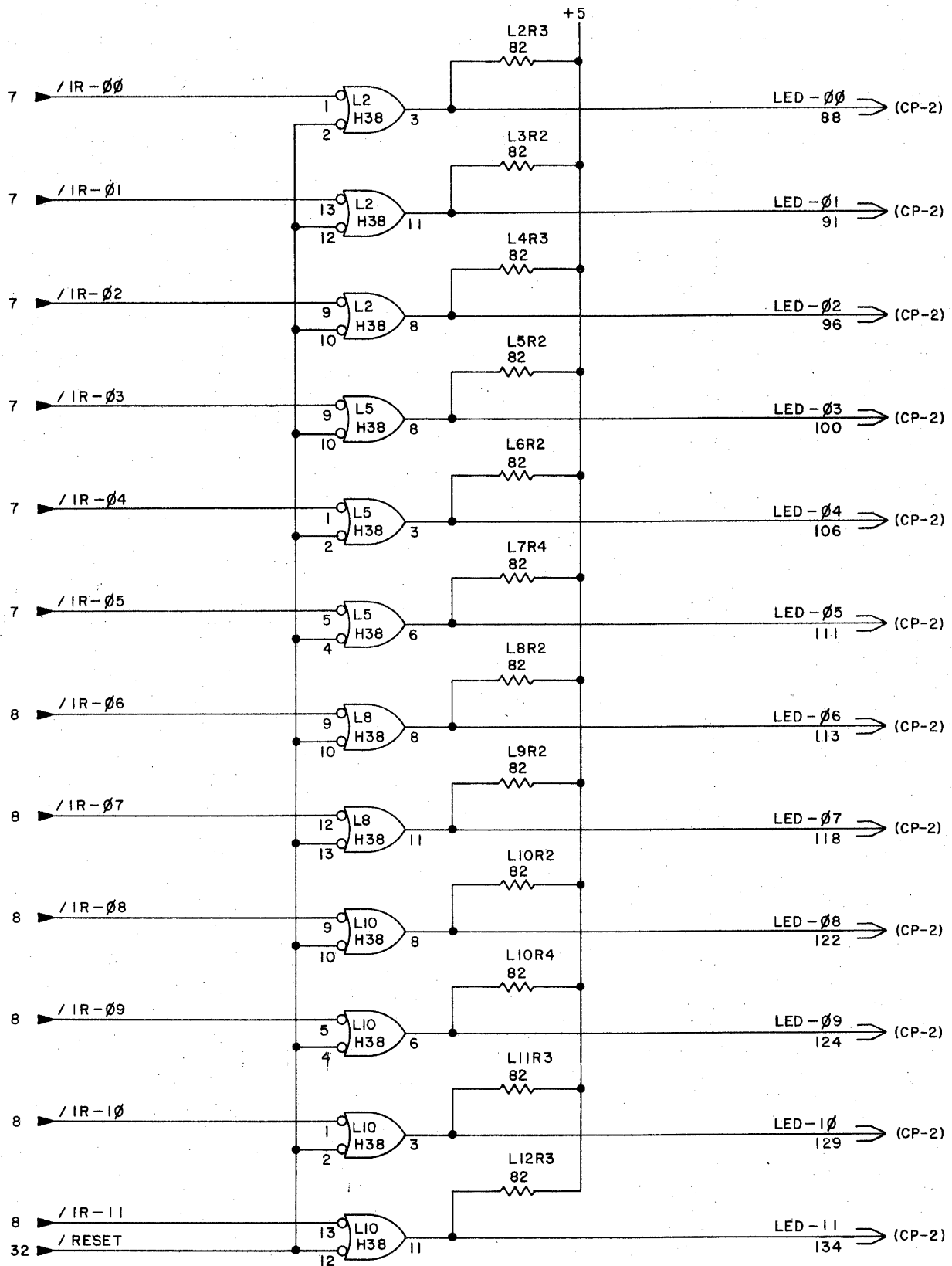
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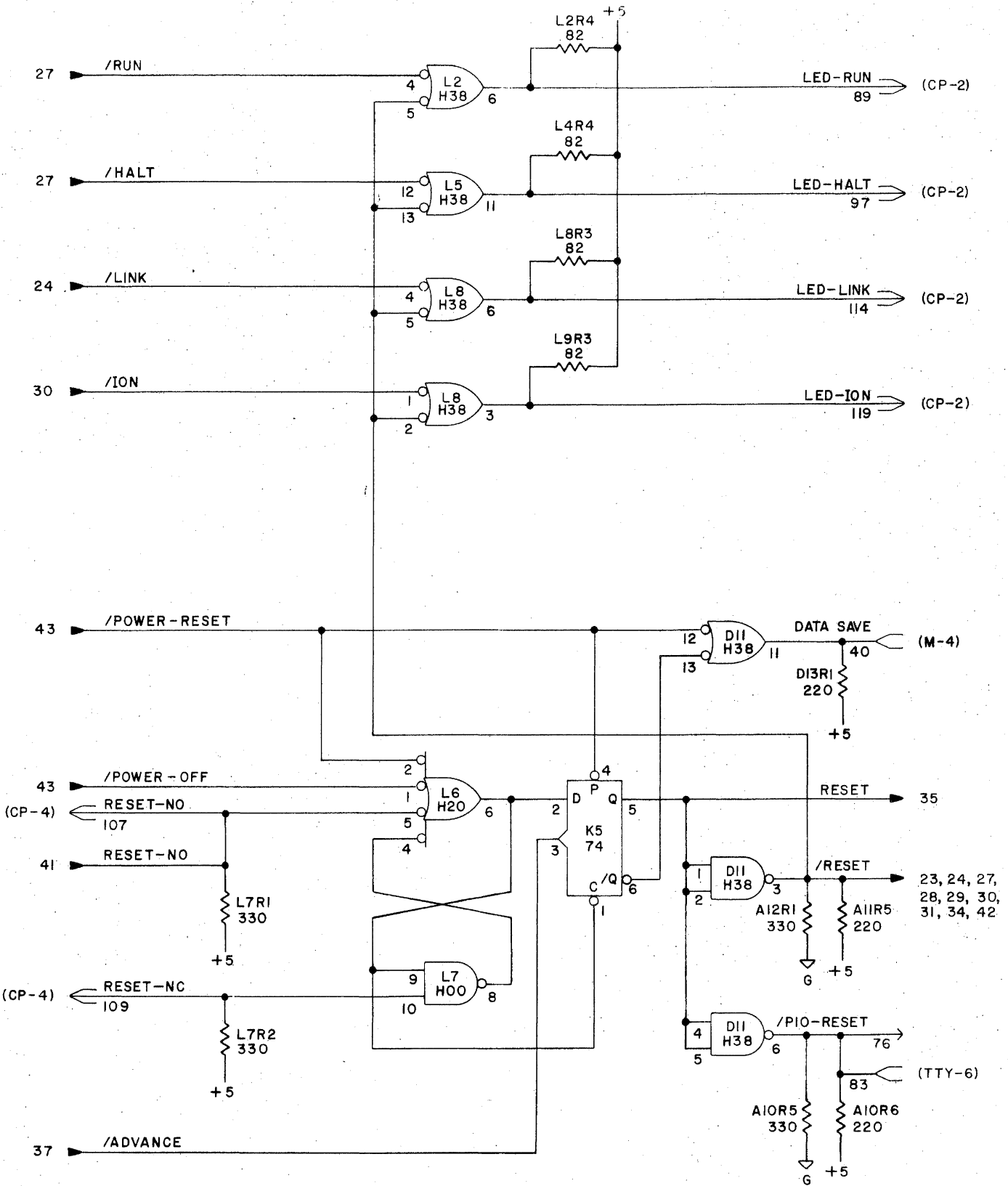
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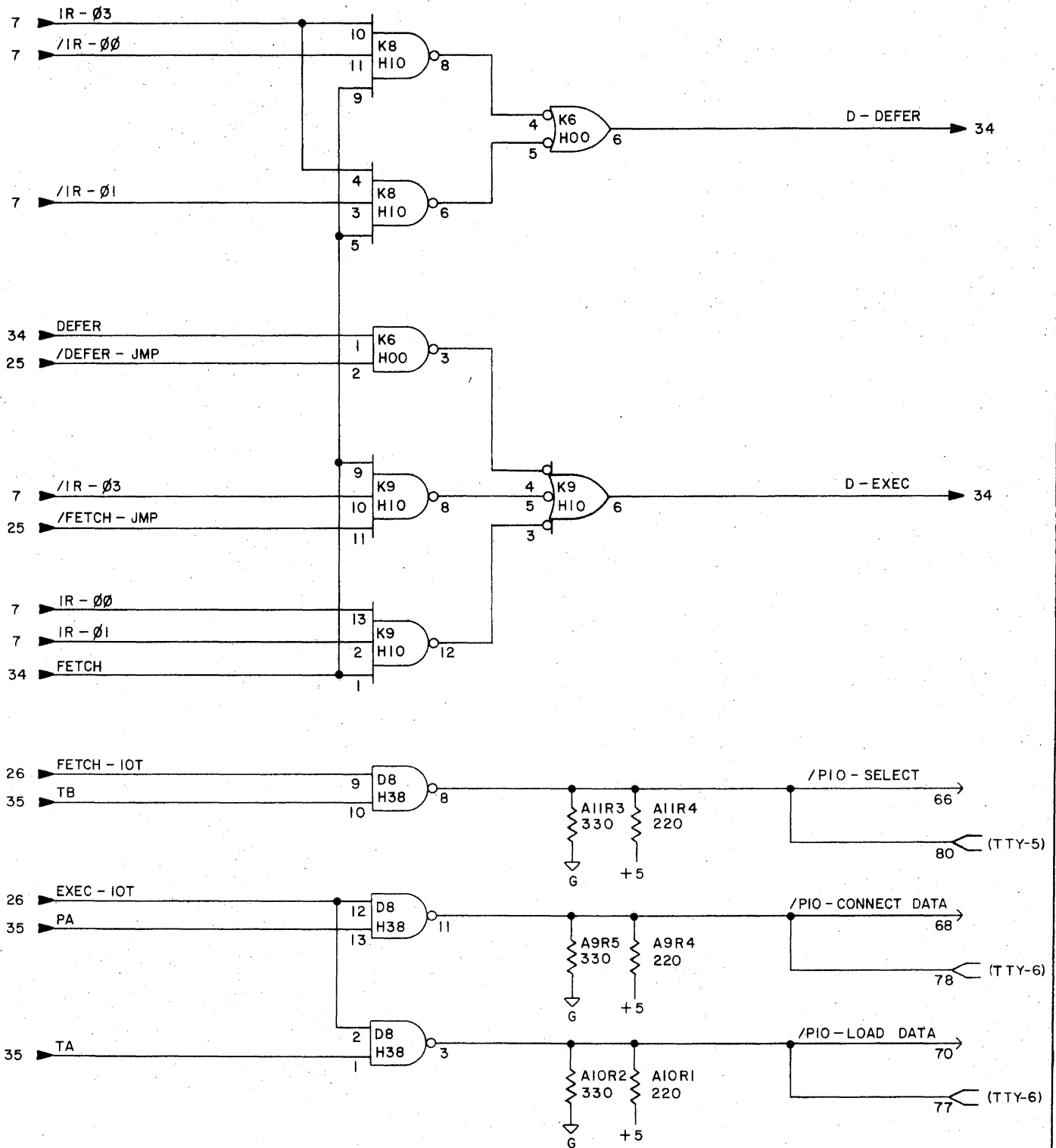
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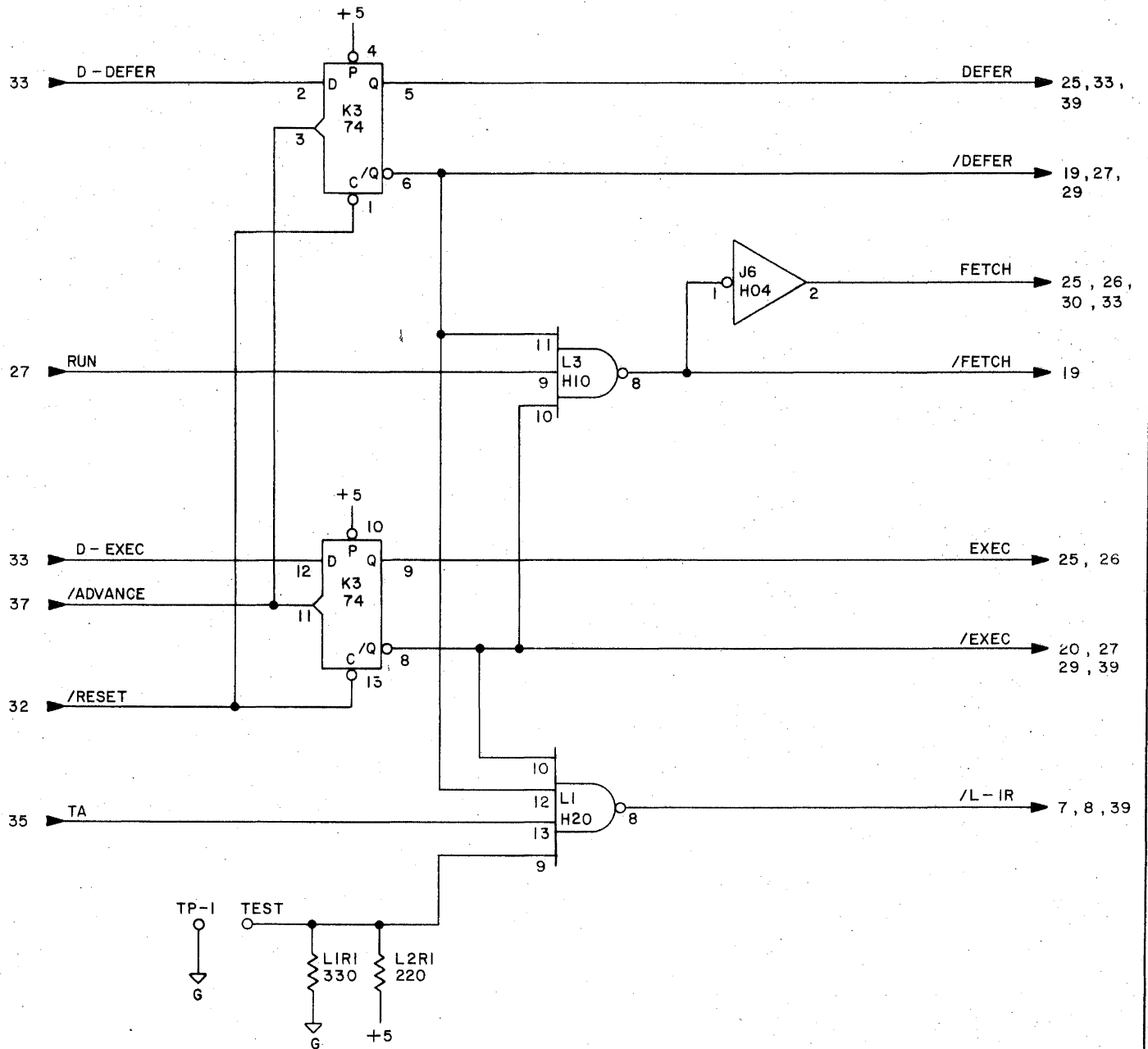


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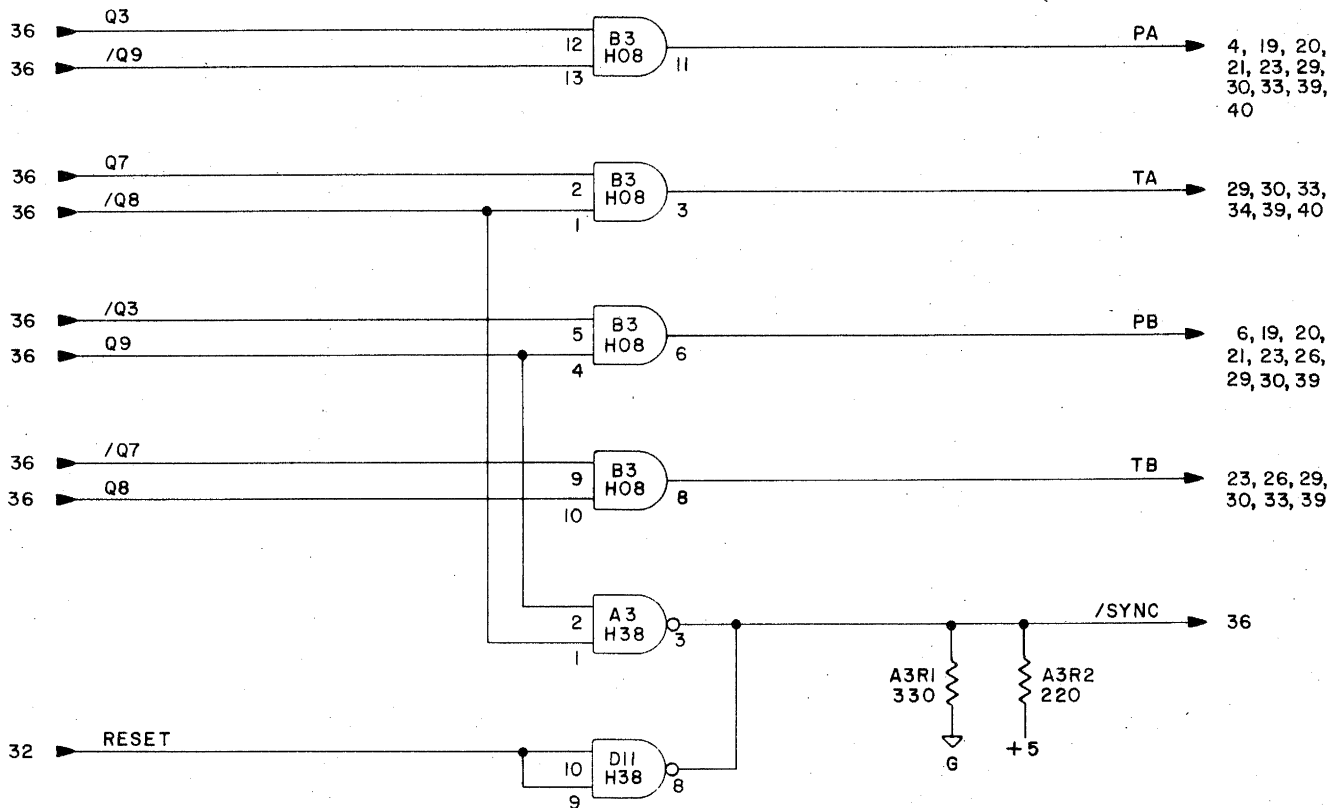
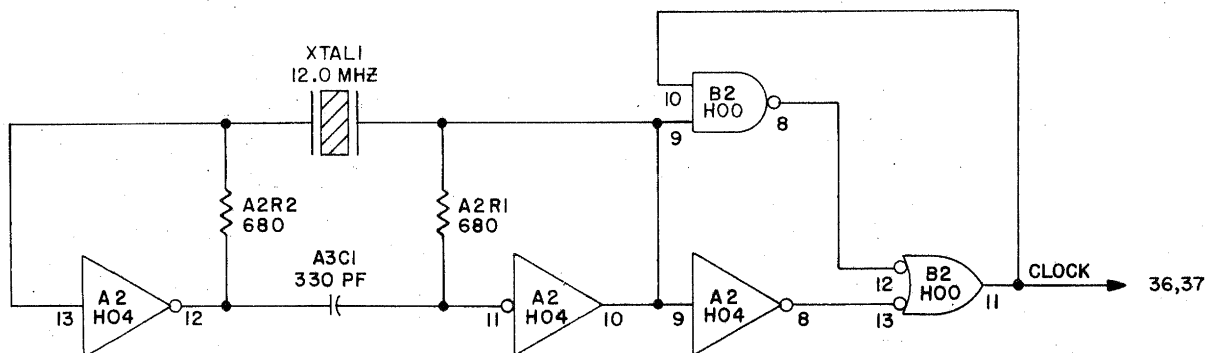
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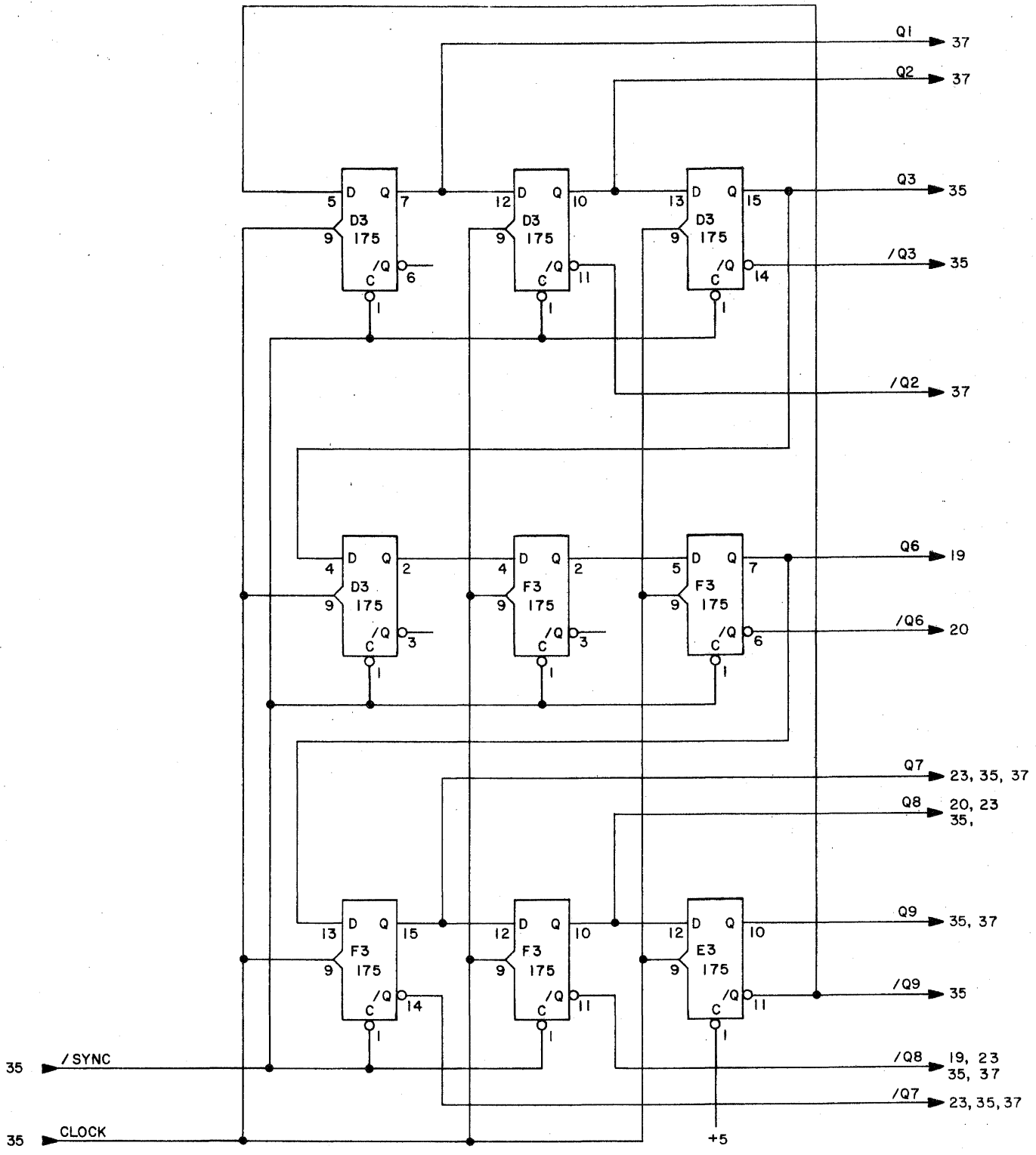
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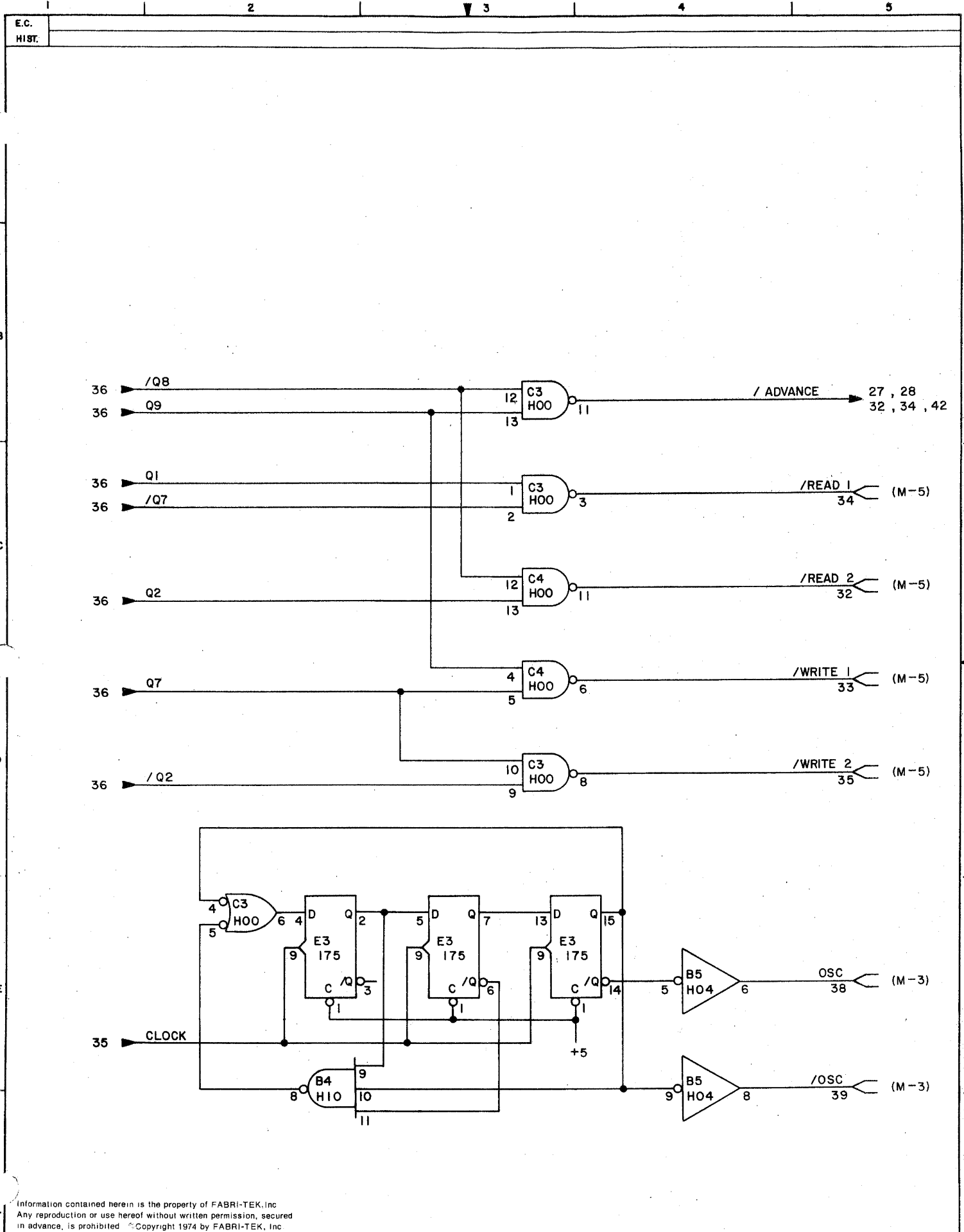


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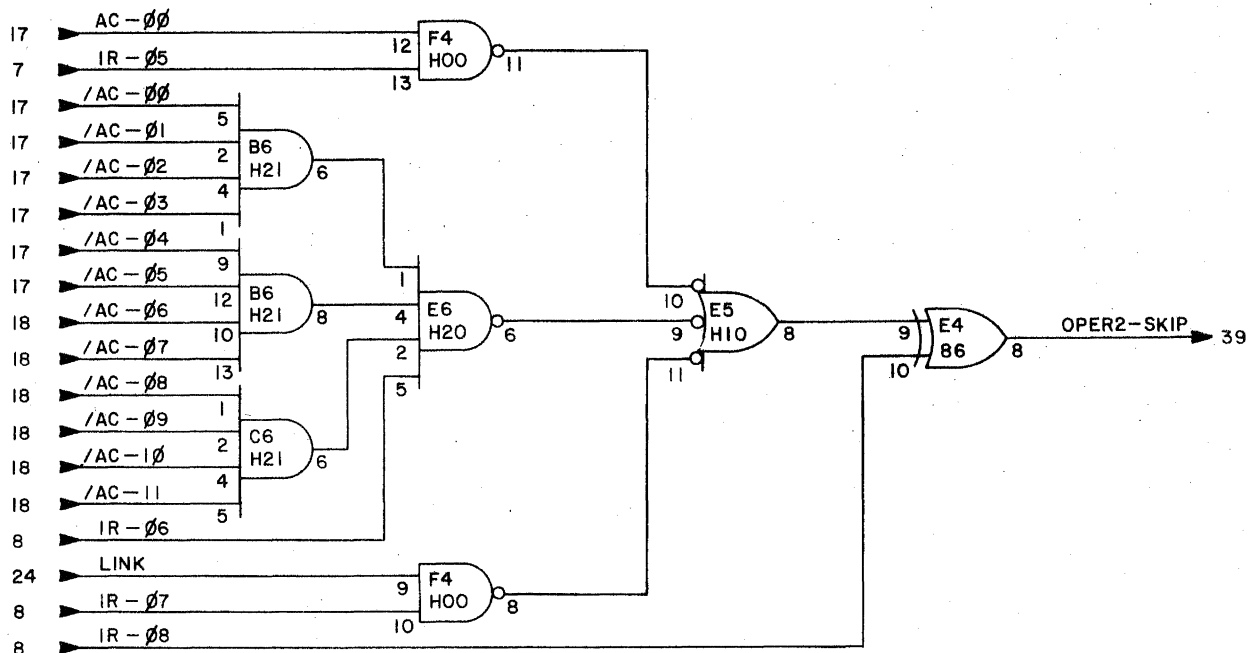
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HIST.

2

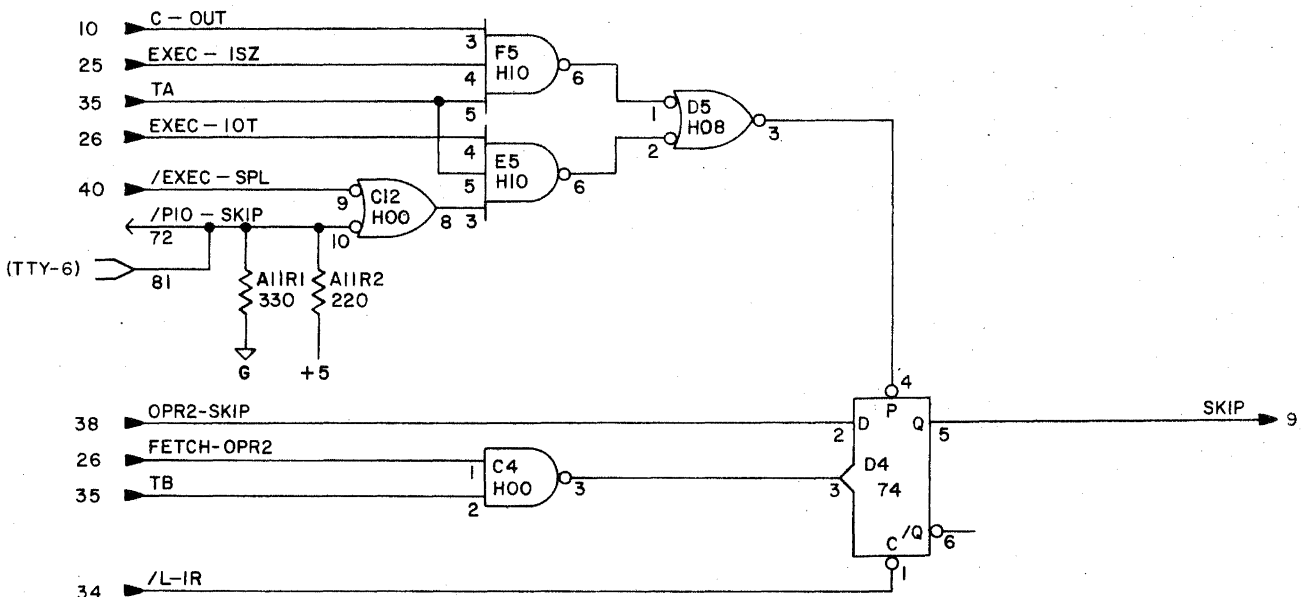
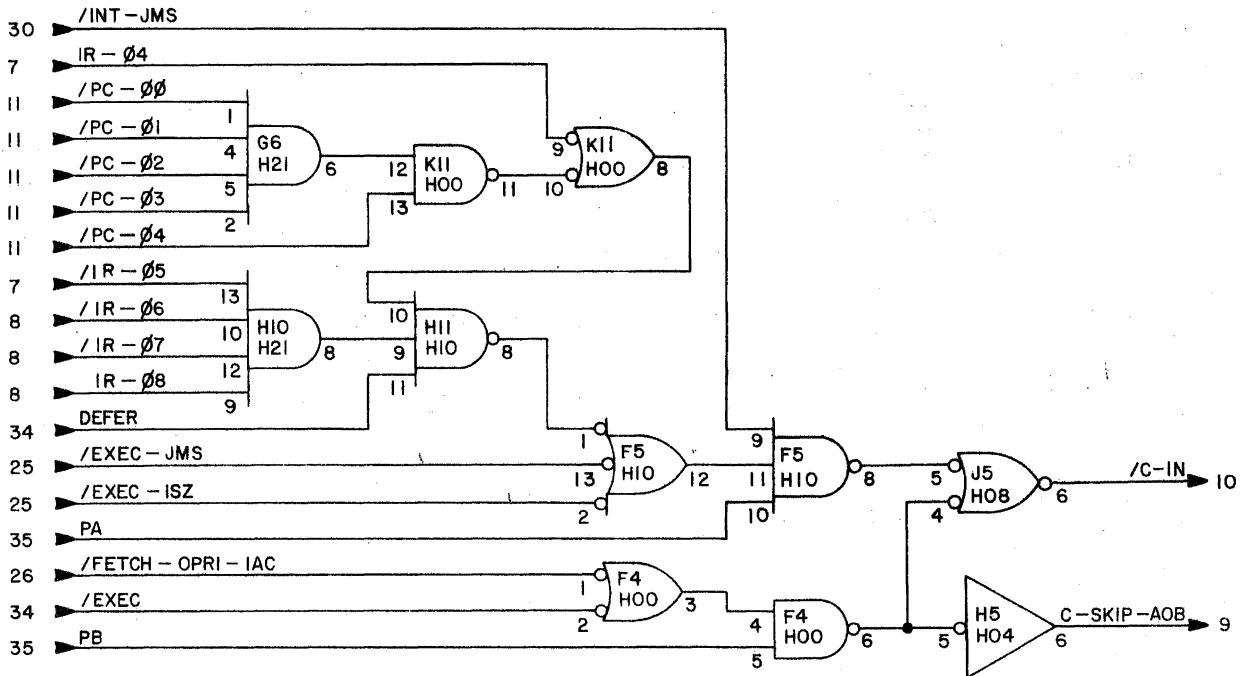
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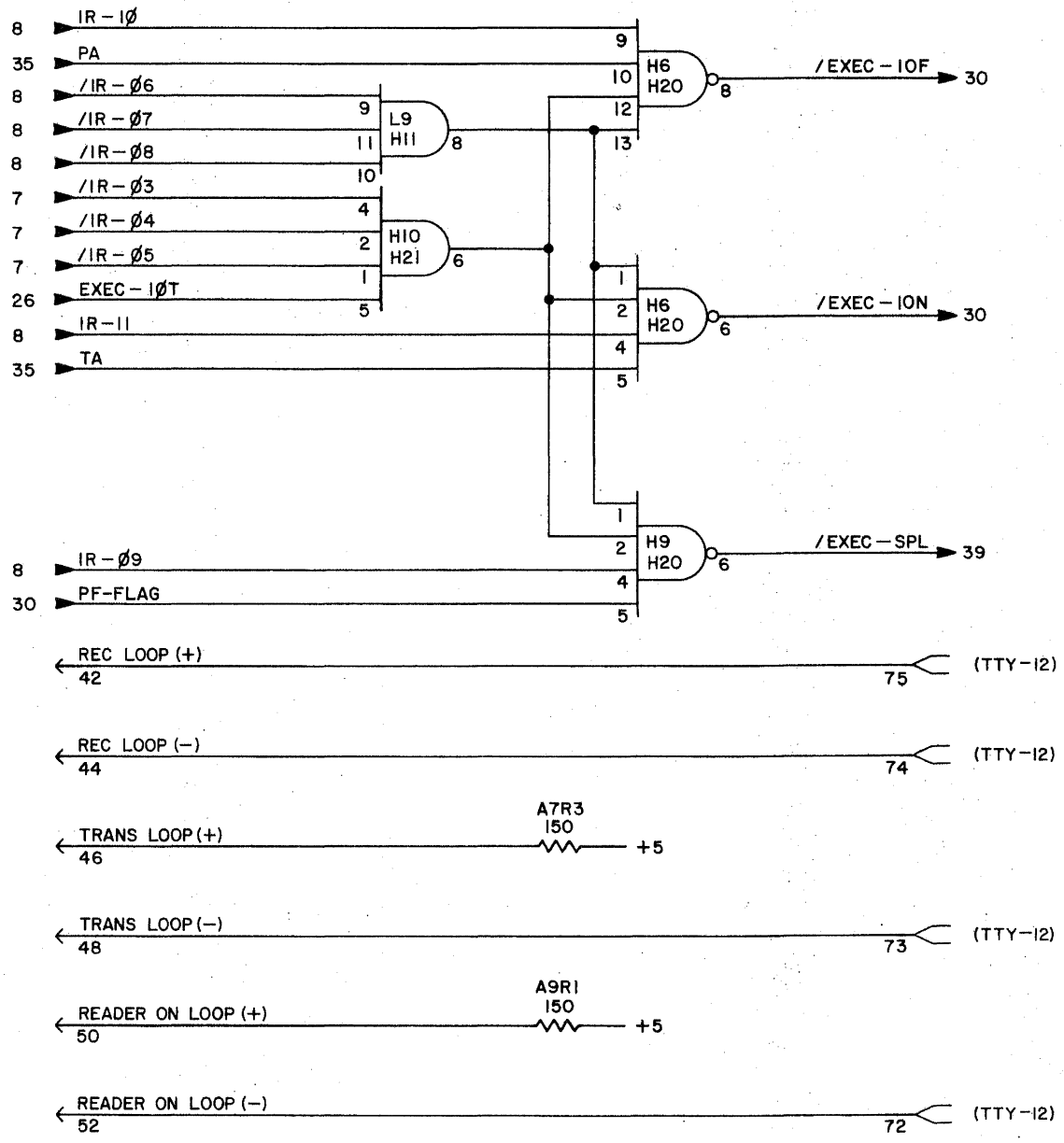
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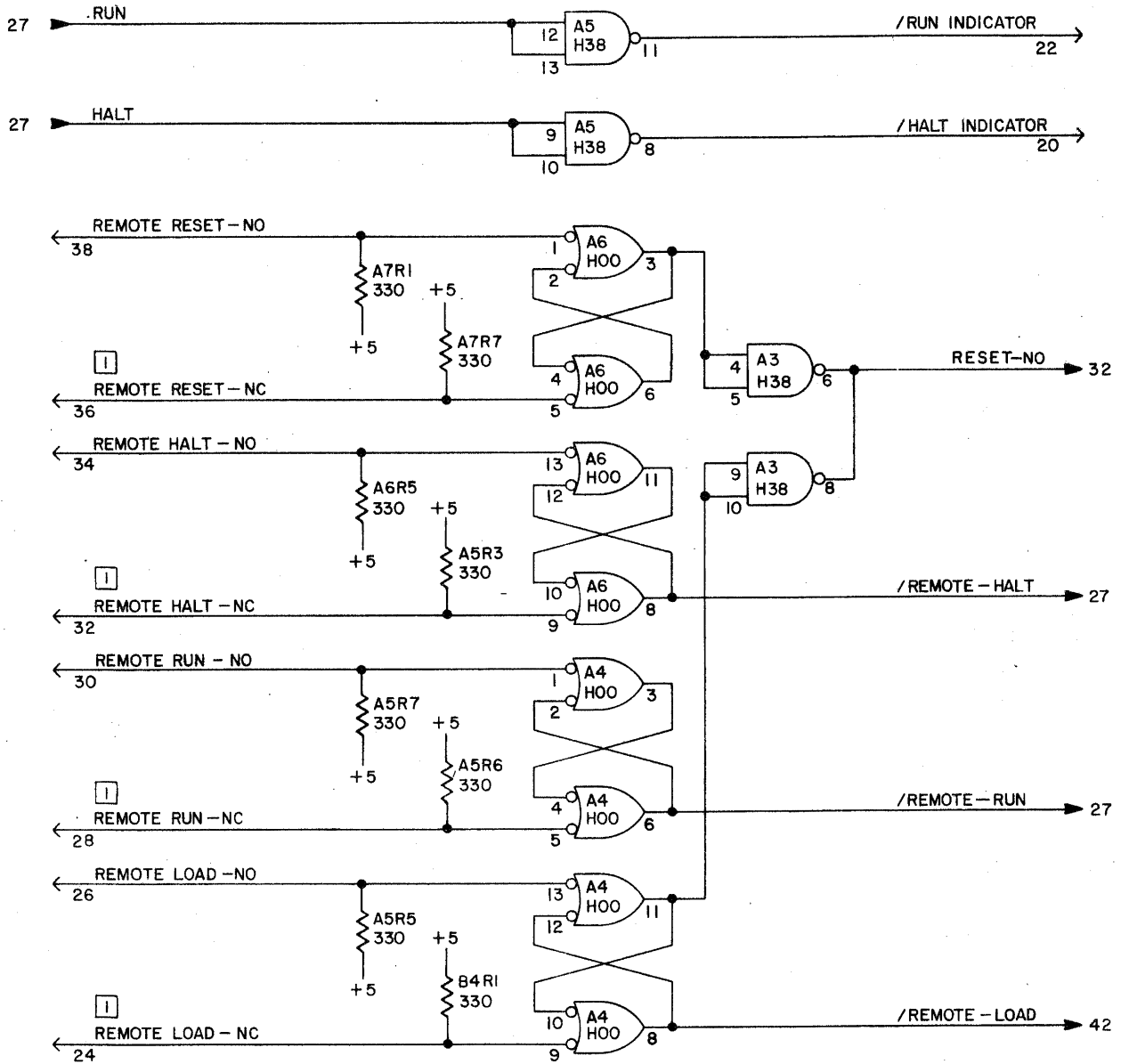
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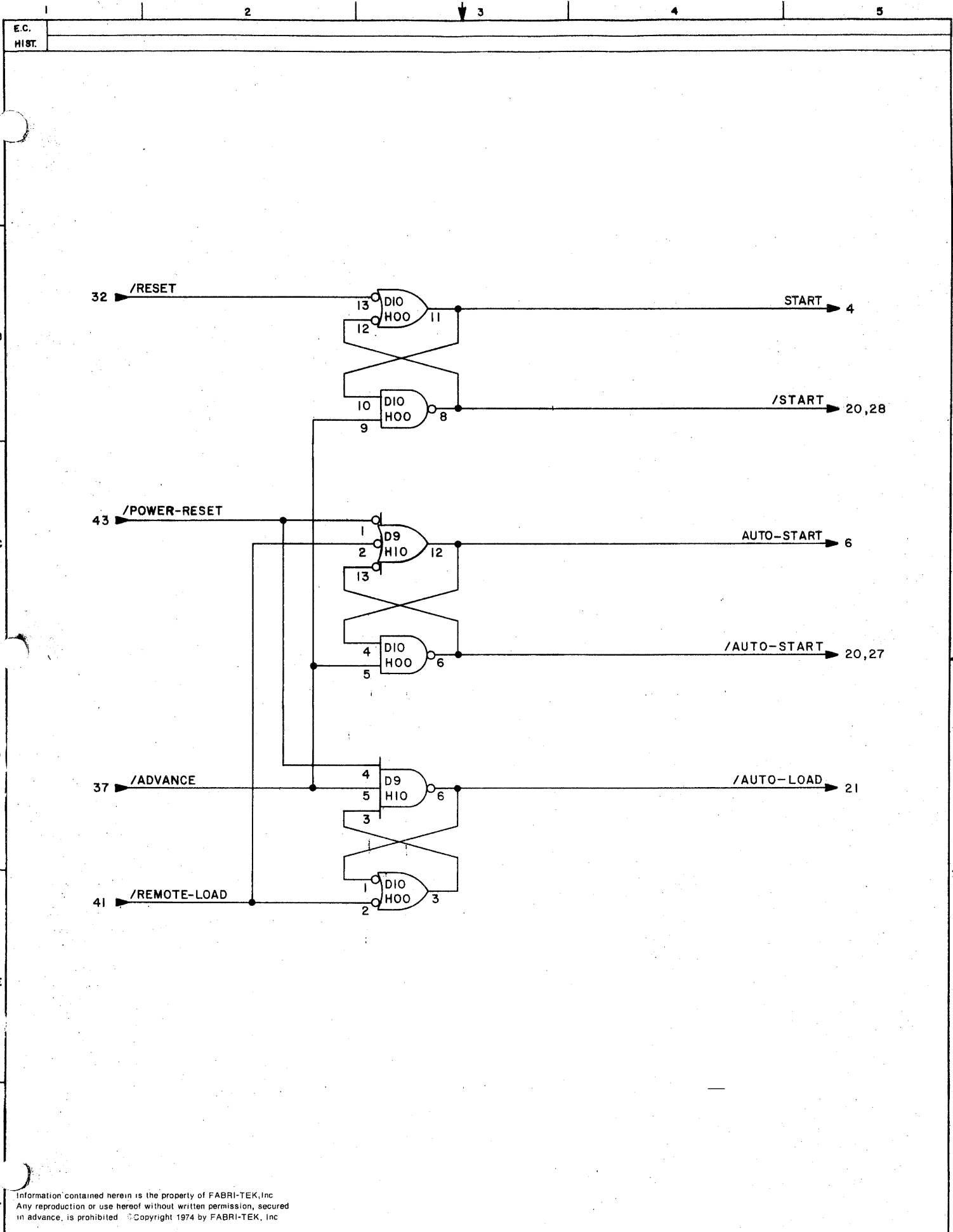
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[1] IF REMOTE CONTROL INPUTS ARE NOT USED, THE FOLLOWING MUST BE DONE.

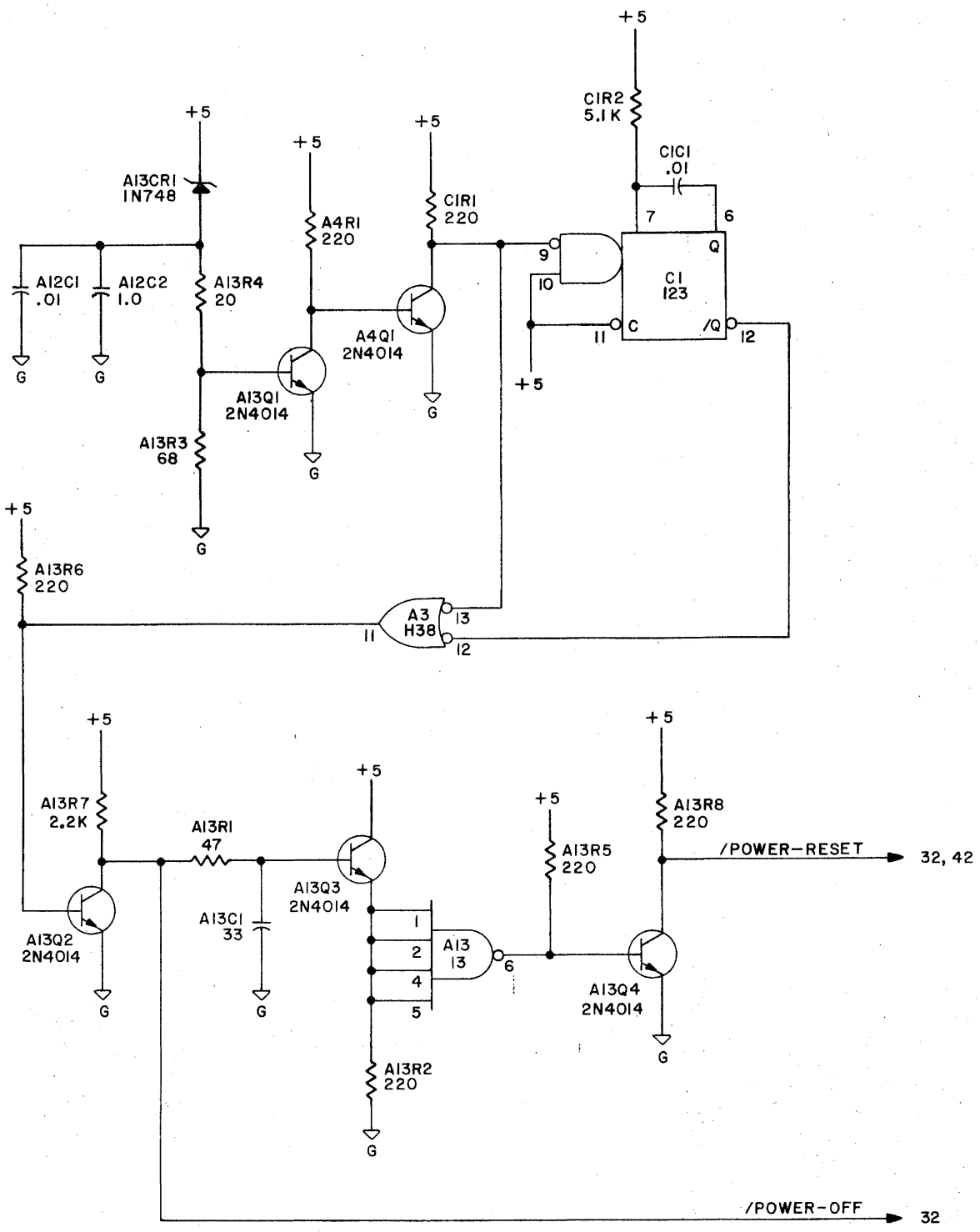
- CONNECT PIN 23 TO PIN 24
- CONNECT PIN 27 TO PIN 28
- CONNECT PIN 31 TO PIN 28
- CONNECT PIN 35 TO PIN 36

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TITLE SCHEMATIC, PROCESSOR ELECTRONICS BD.

DWG. NO. C 138-0020-20

TYPE

VERS.

PAGE

43

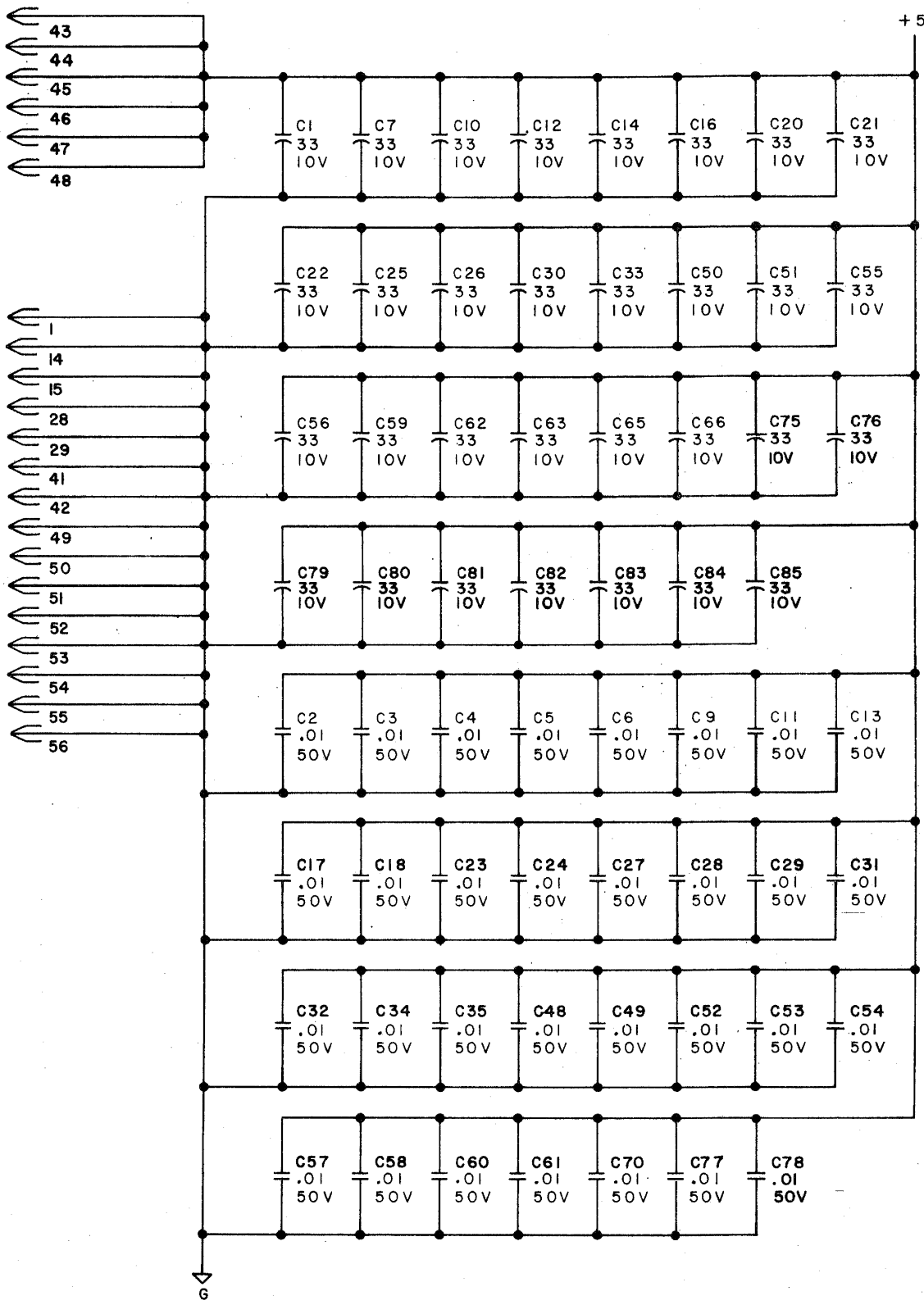
E.C.
HIST.

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TITLE SCHEMATIC, MEMORY ELECTRONICS BOARD

DWG. NO. C 138-0020-19

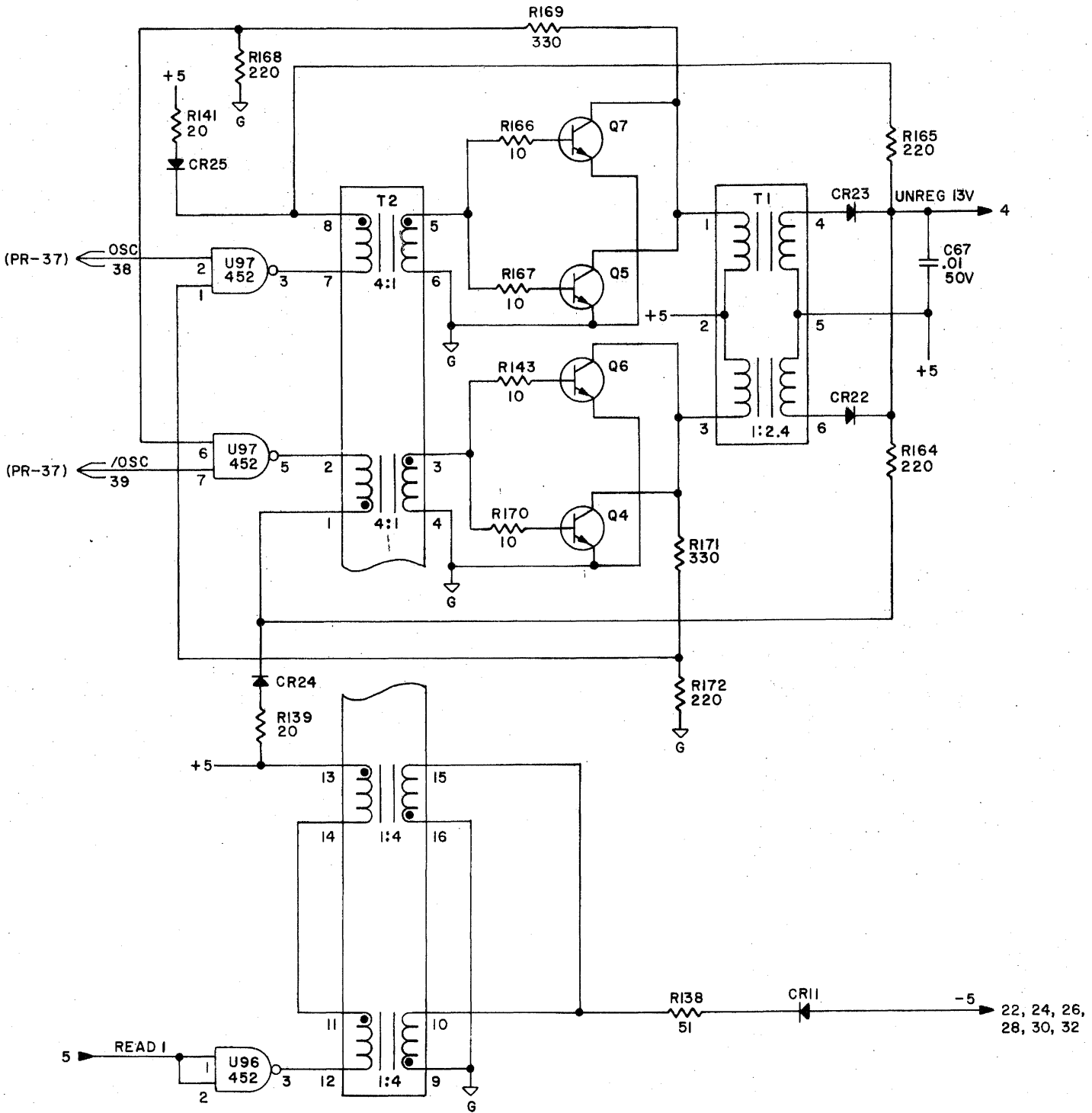
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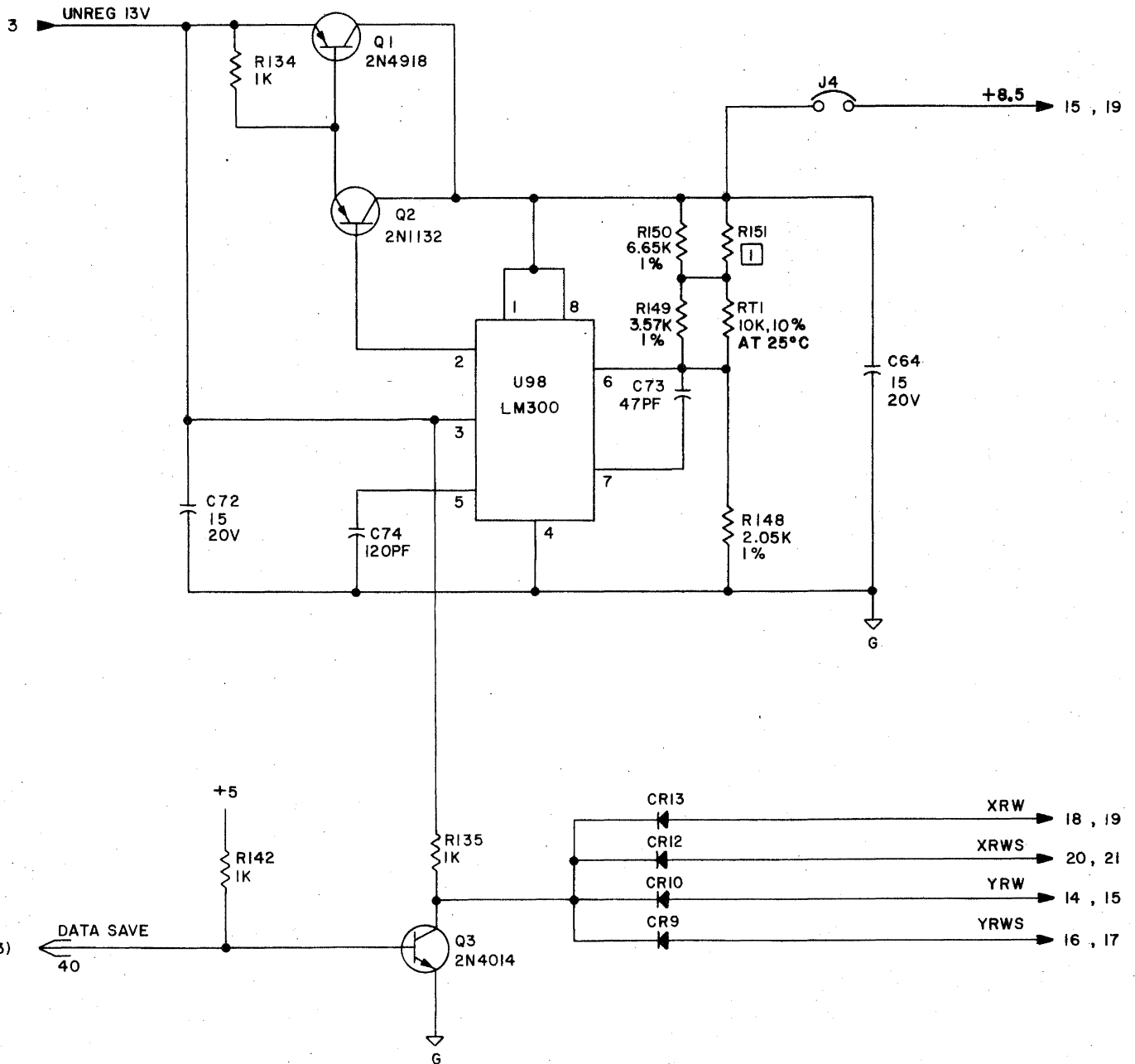
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2

E.C.
HIST.

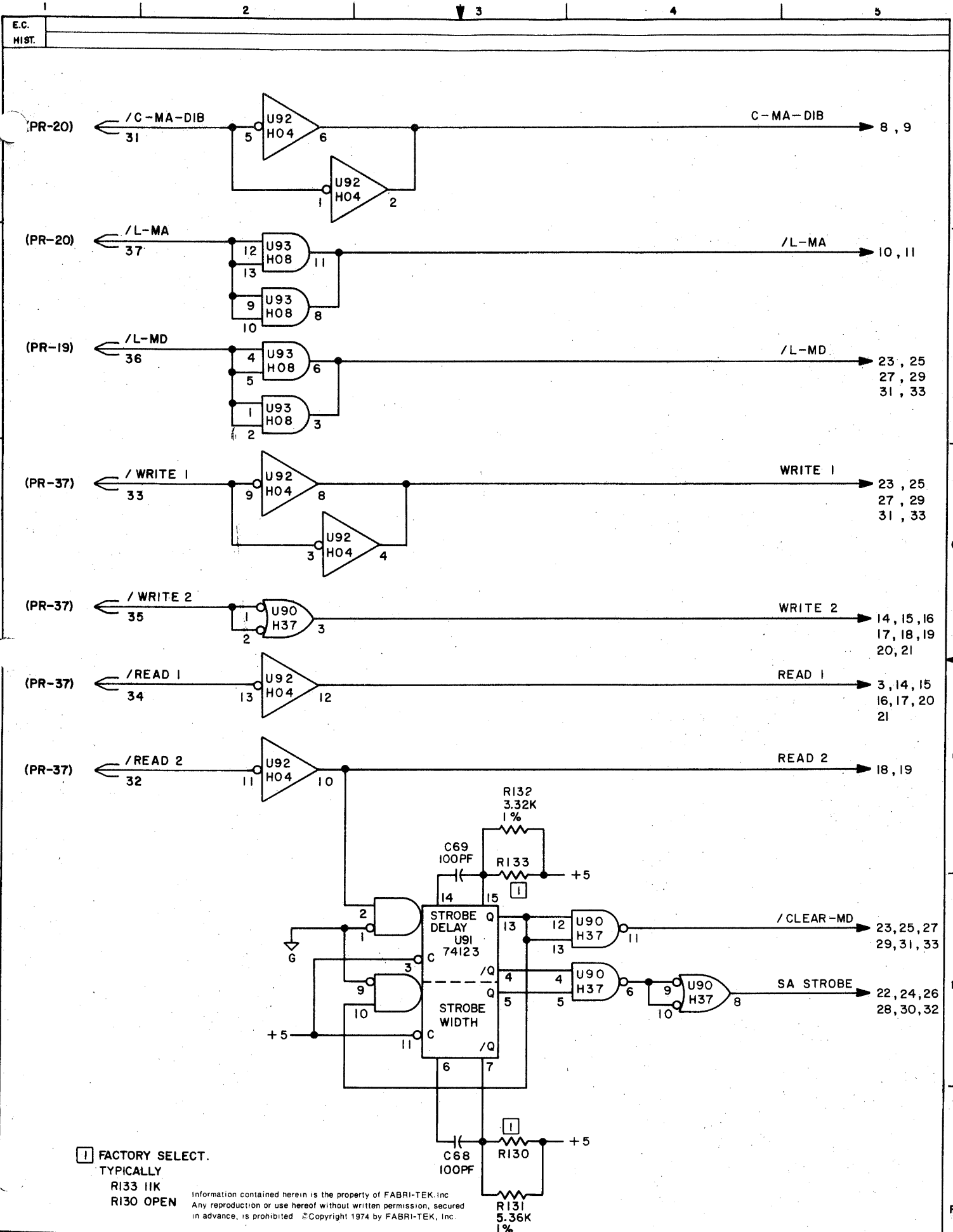


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FACTORY SELECT.
TYPICALLY 40K.

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FACTORY SELECT.
 TYPICALLY
 R133 11K
 R130 OPEN

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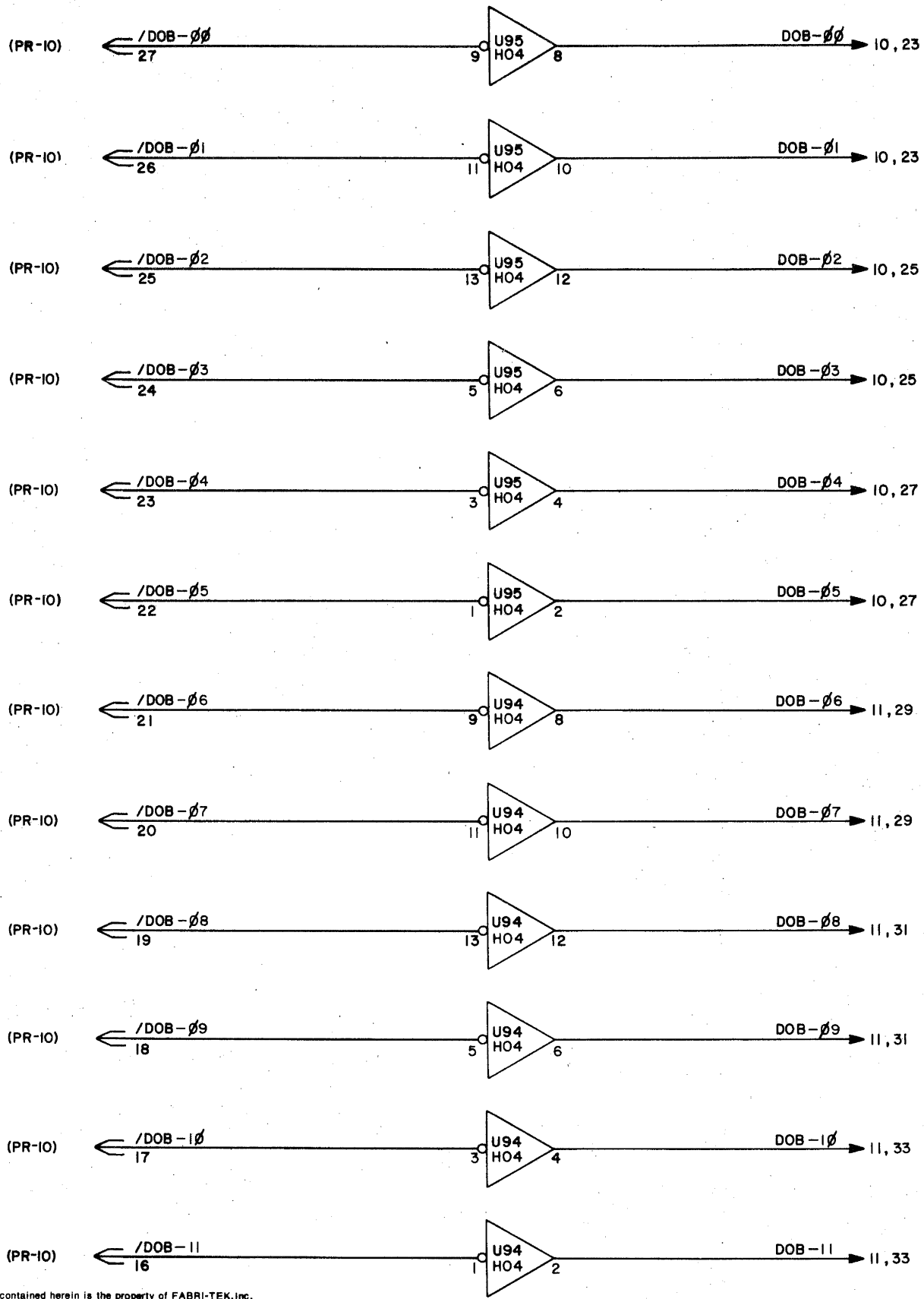
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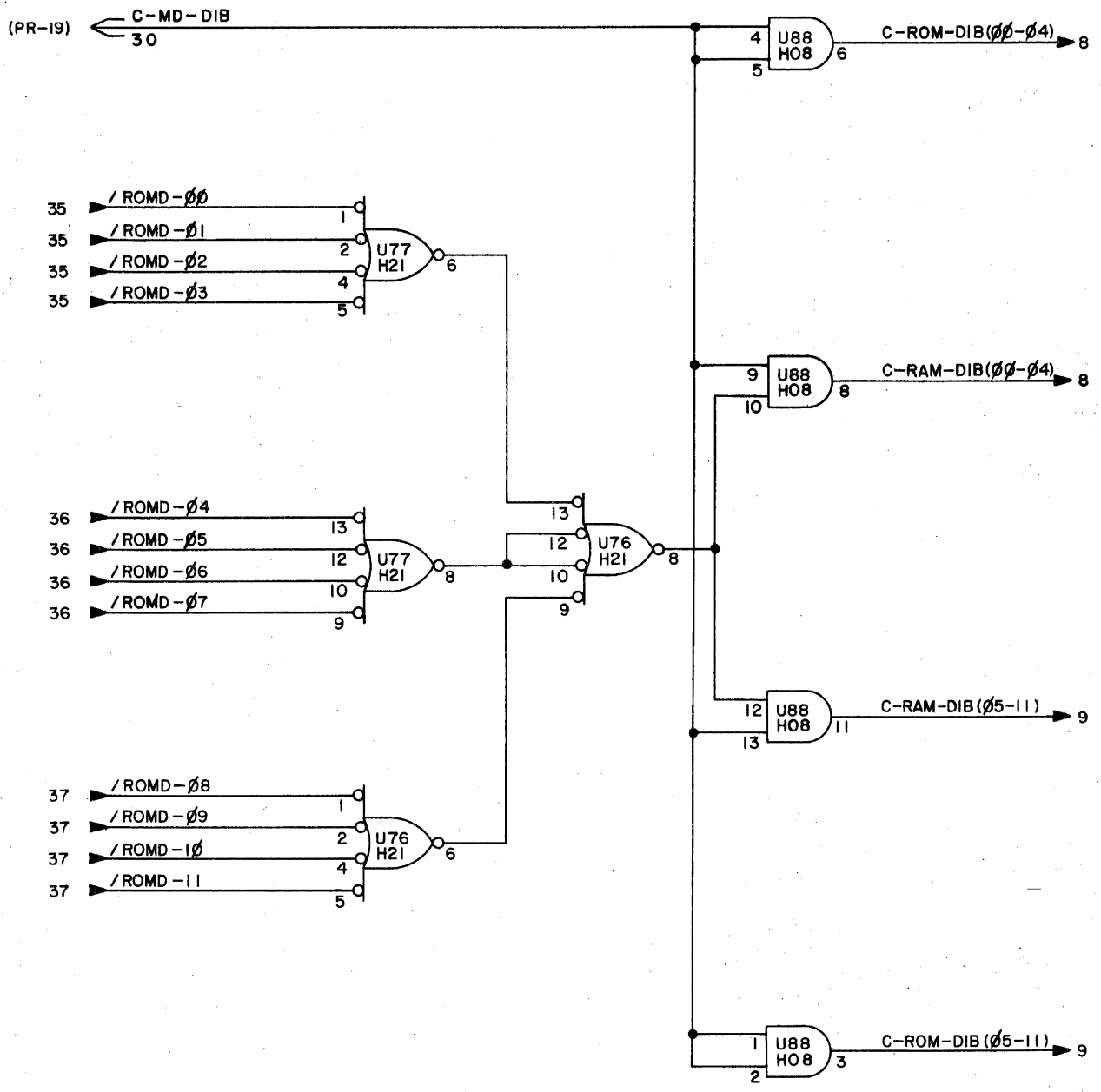
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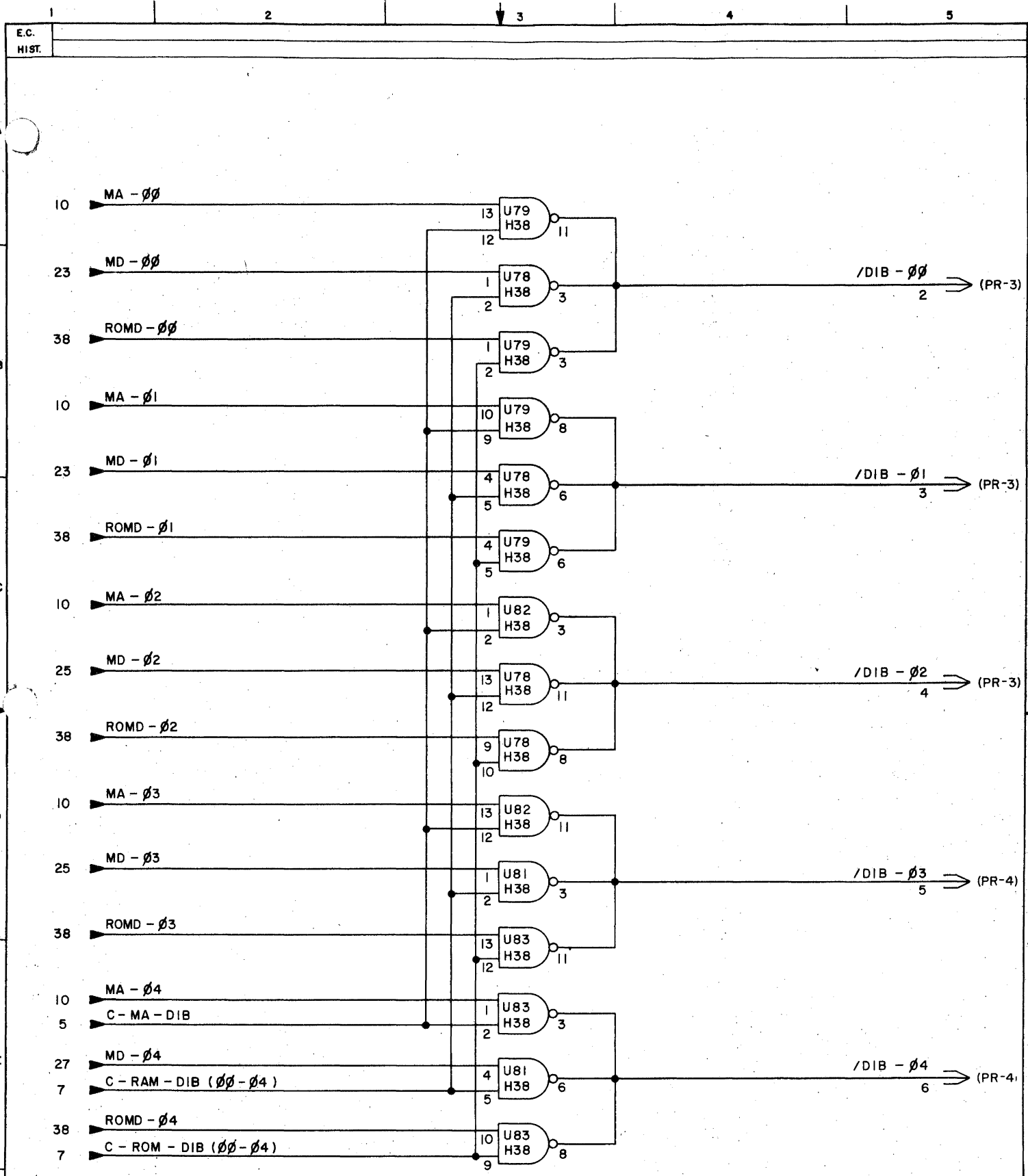
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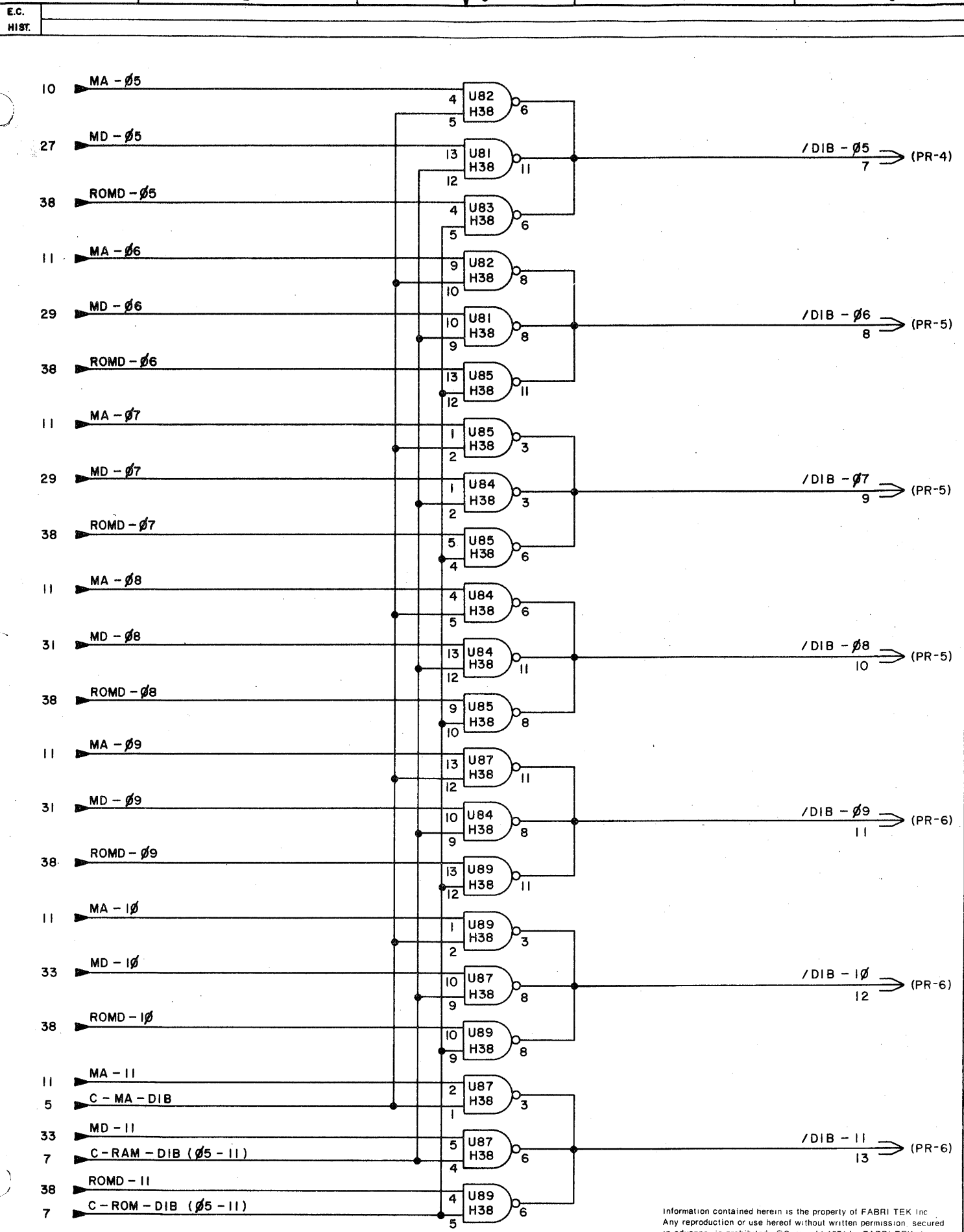
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TITLE		SCHEMATIC, MEMORY ELECTRONICS BOARD		
DWG. NO.	C 138-0020-19	TYPE	VERS.	PAGE
				7

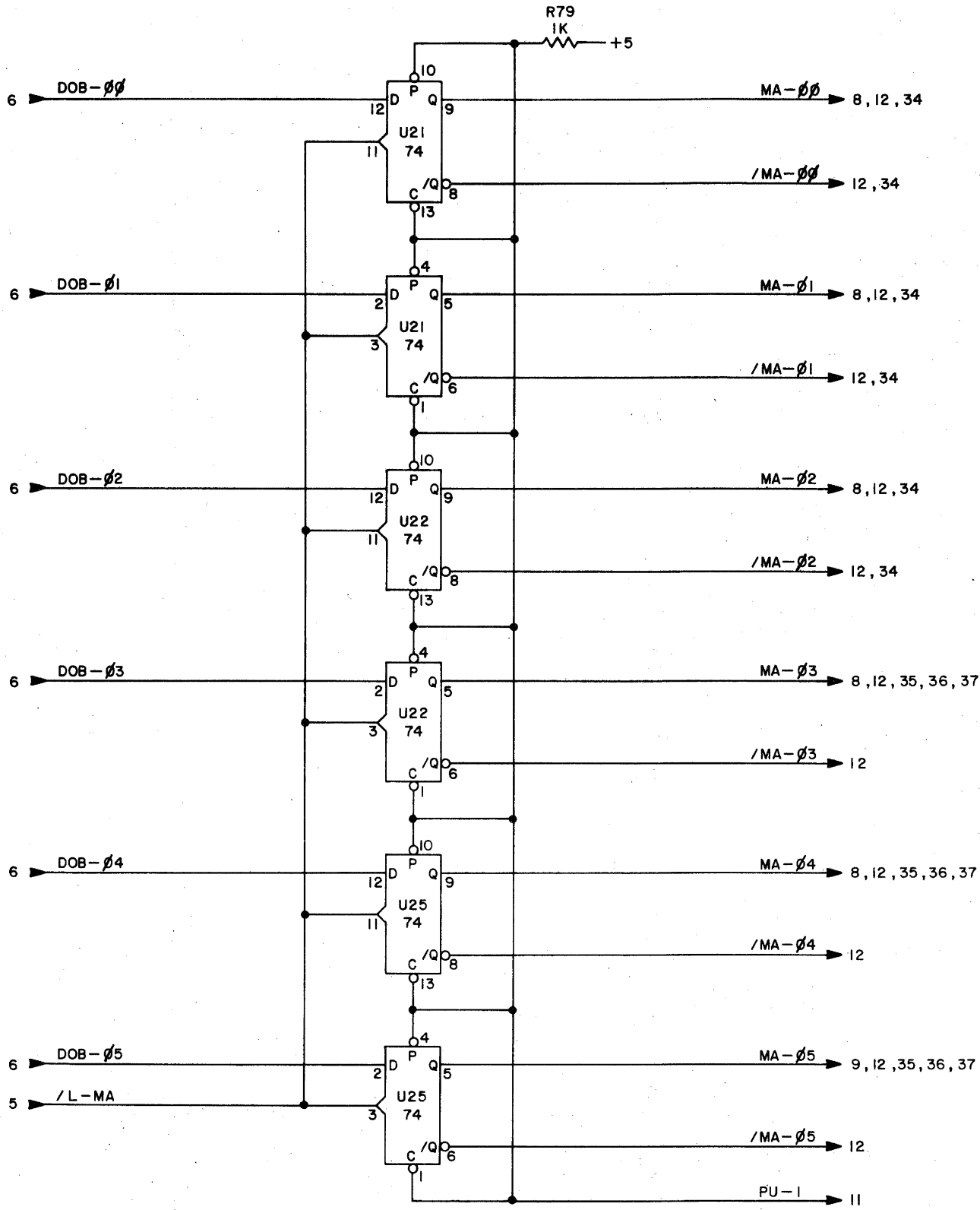


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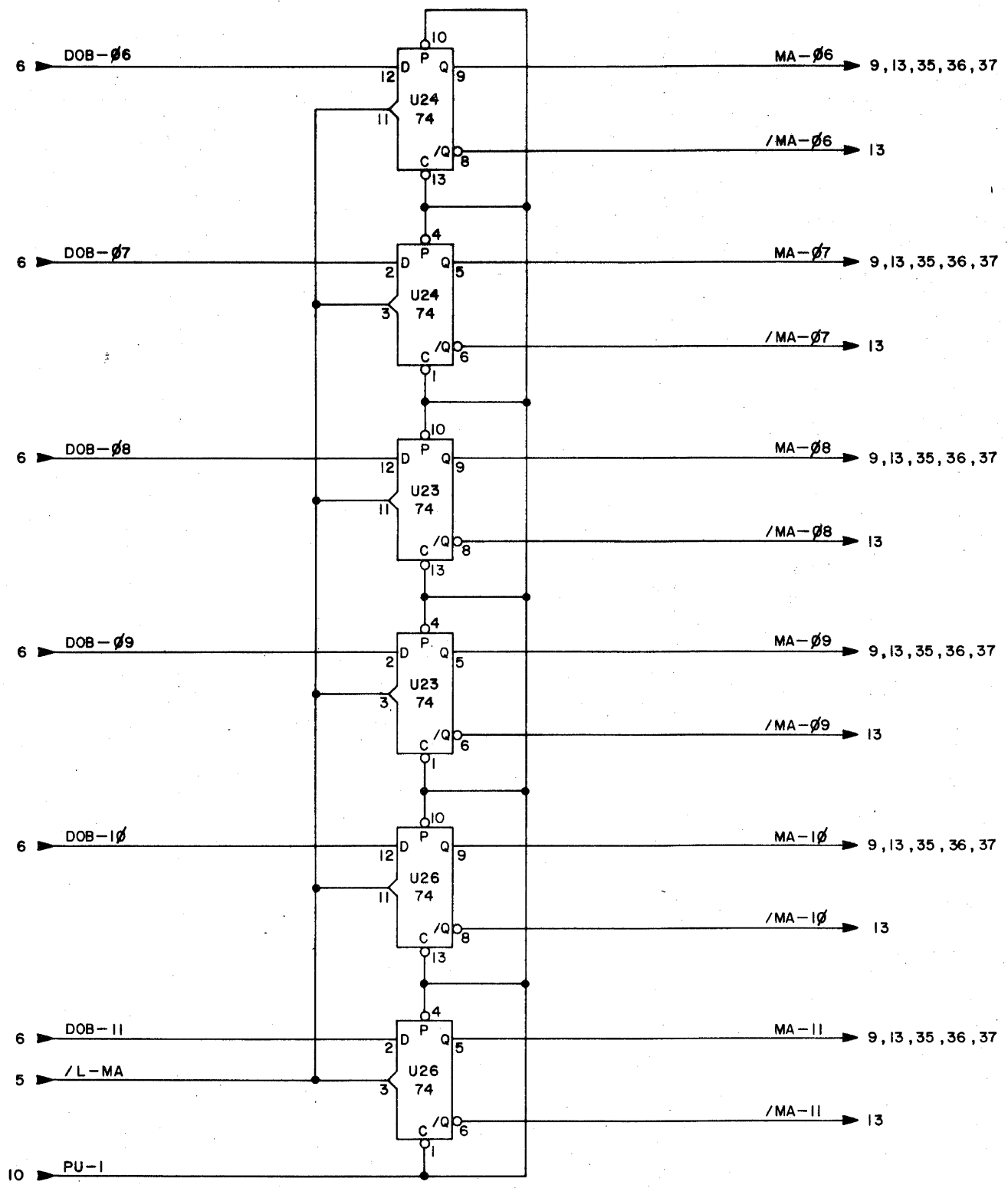
TITLE SCHEMATIC, MEMORY ELECTRONICS BOARD

DWG. NO. C 138-0020-19

TYPE

VERS.

PAGE 10



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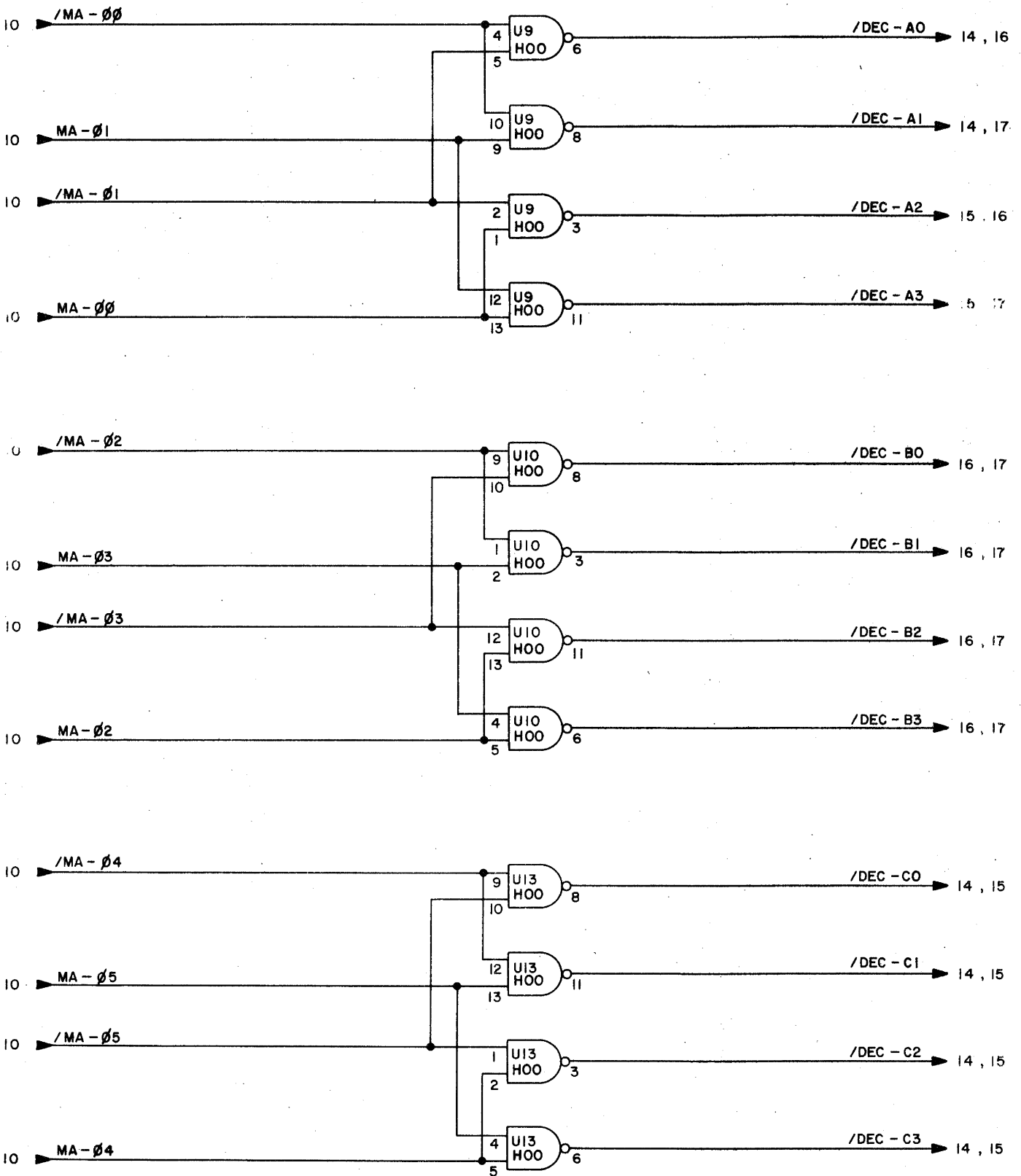
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HIST.

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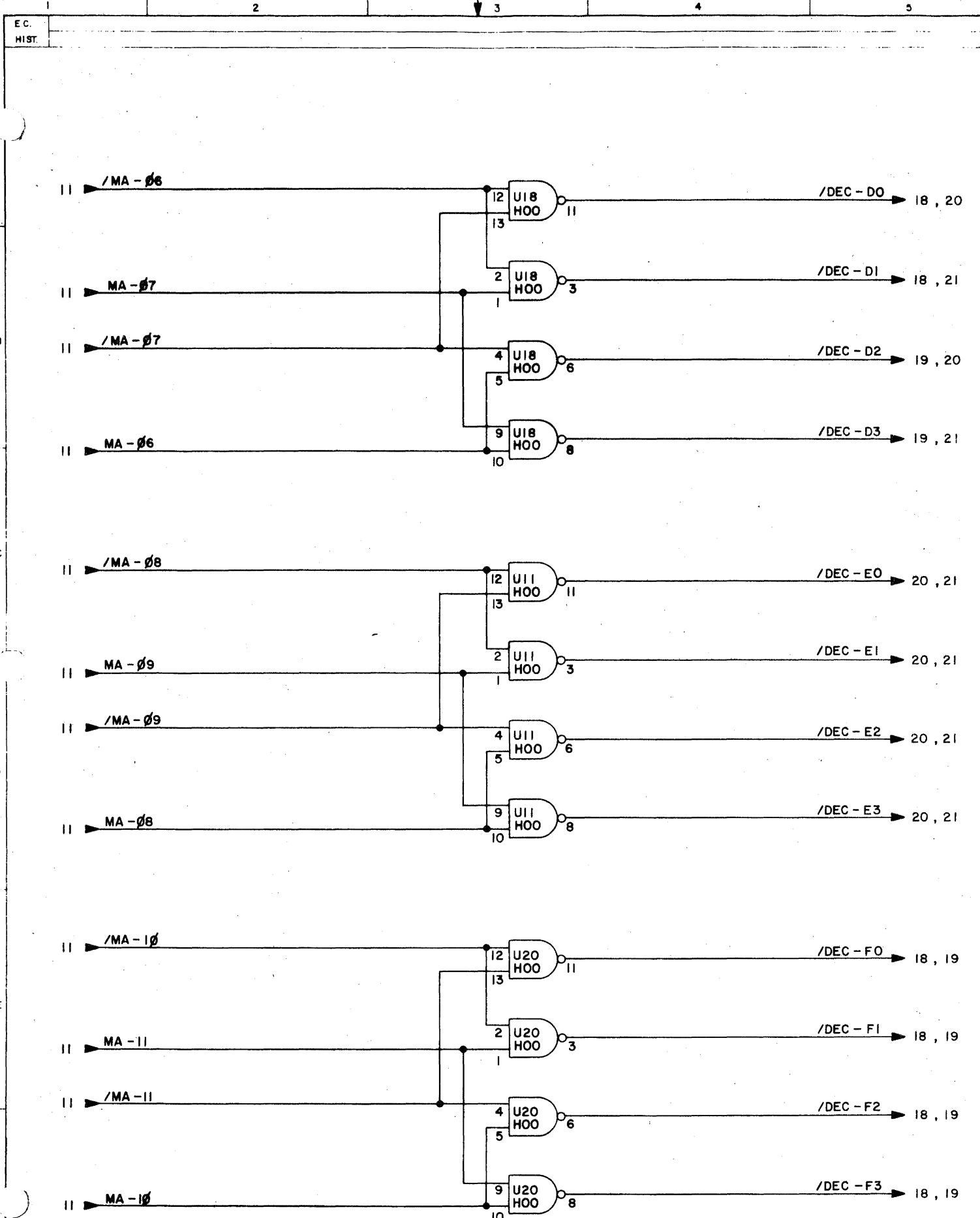
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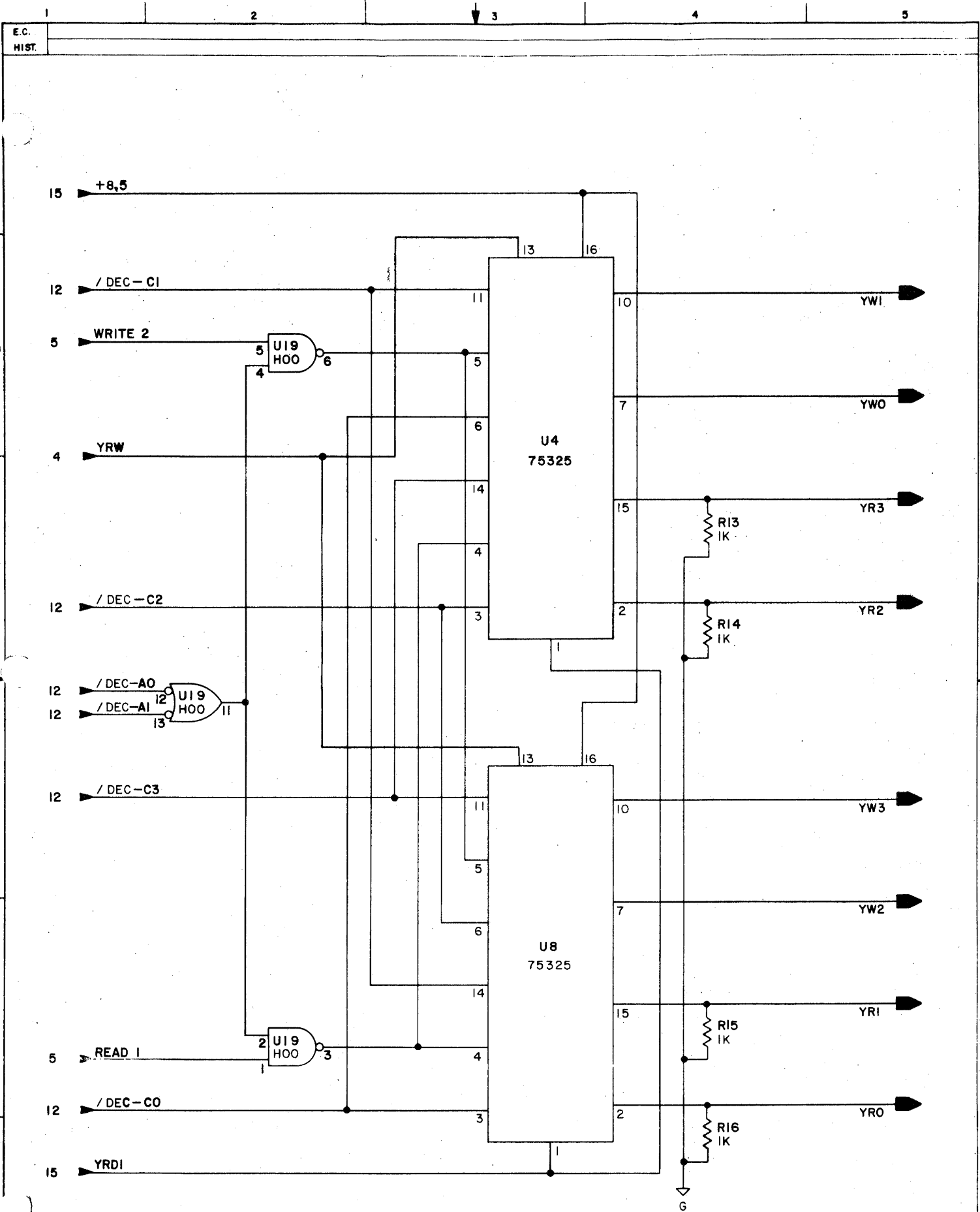
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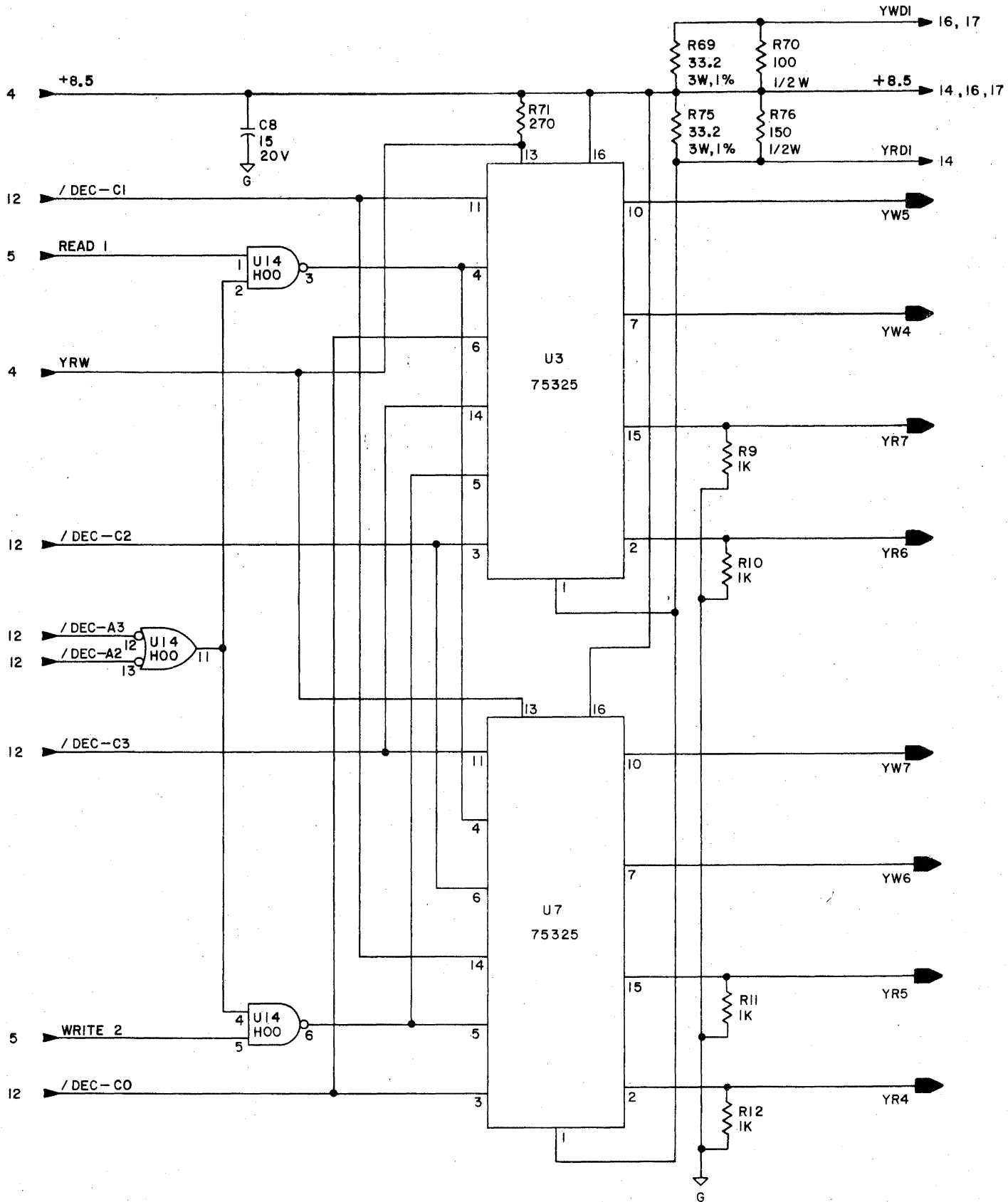
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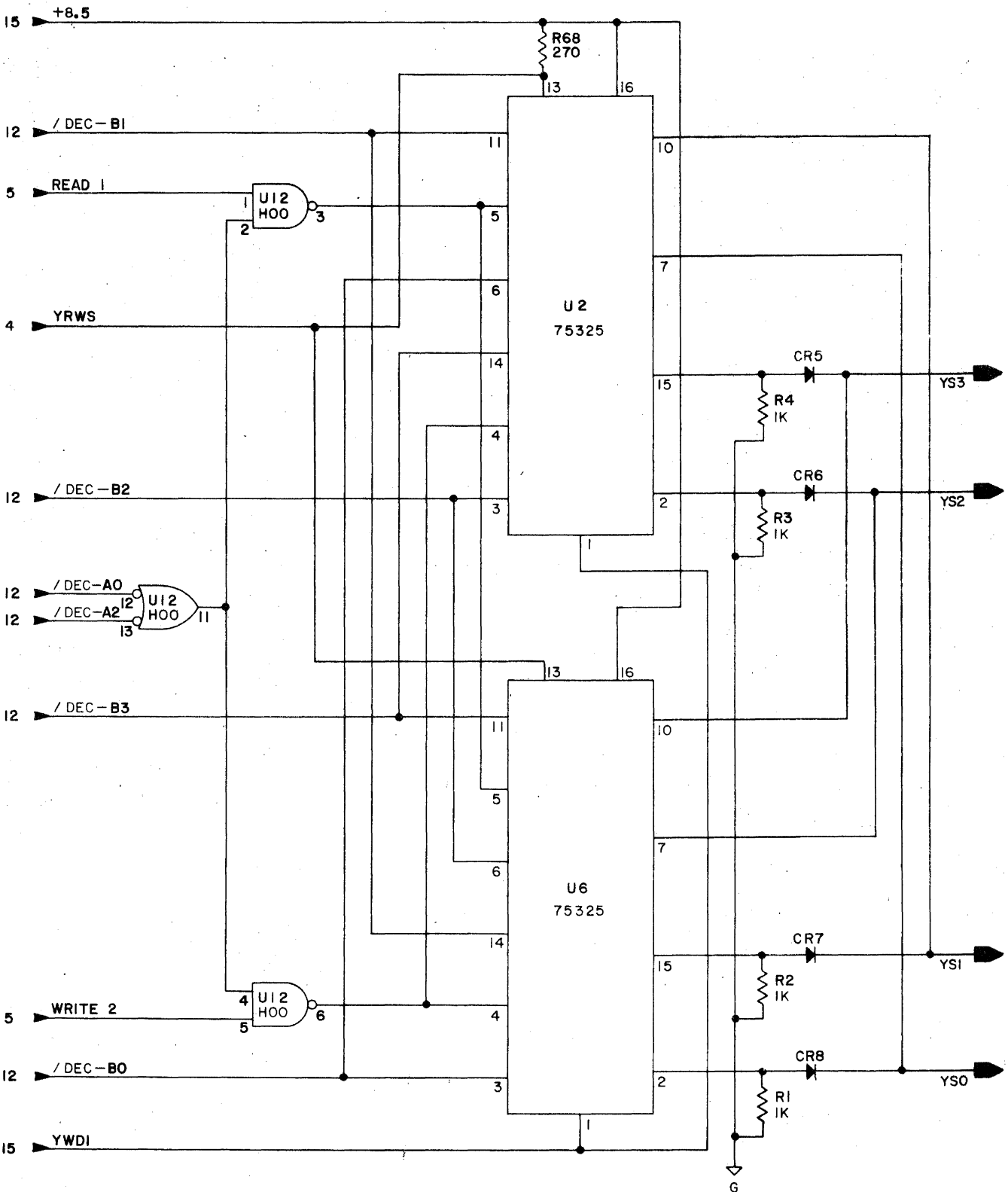
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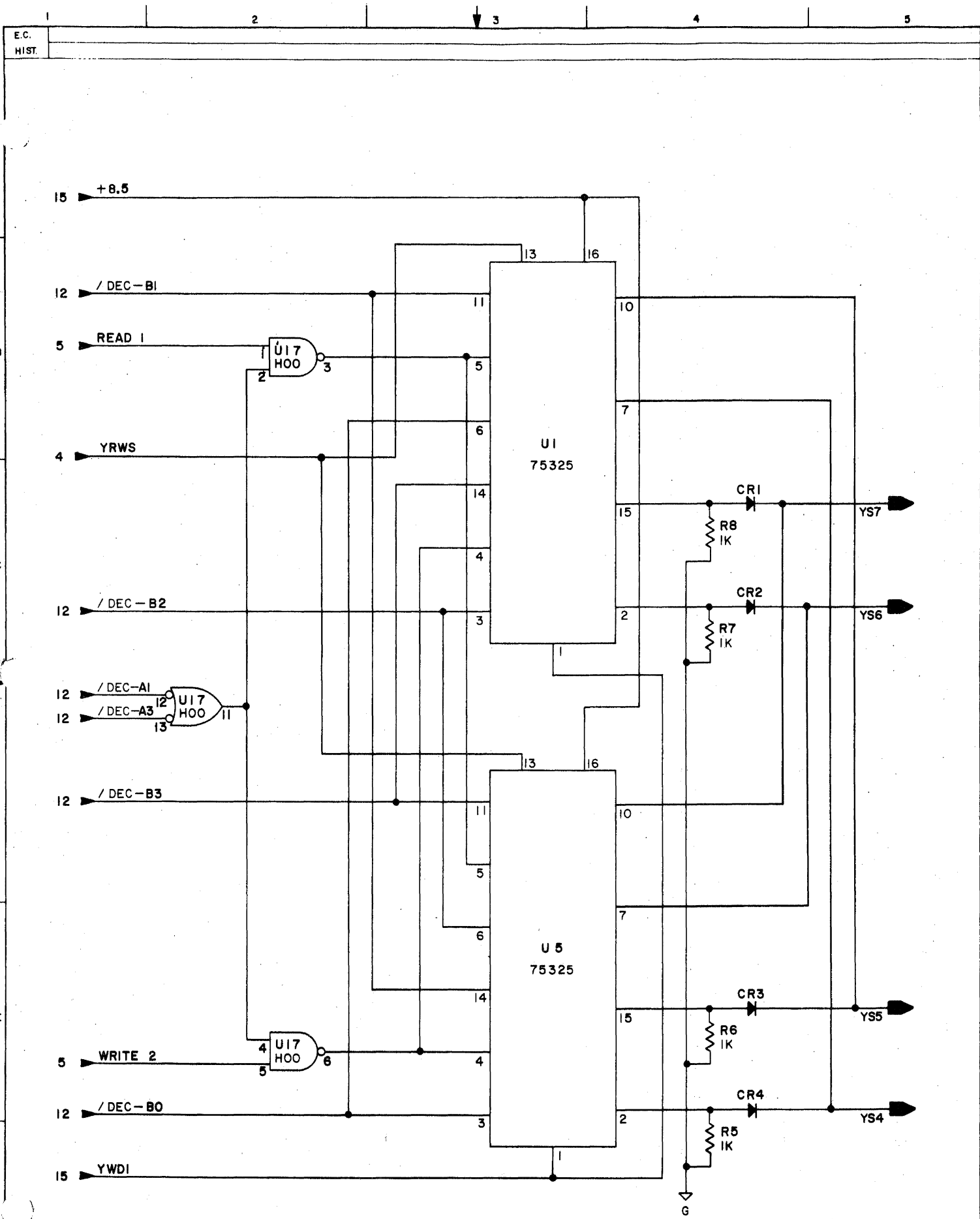
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E.C.
HIST.

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A

A

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B

C

C

D

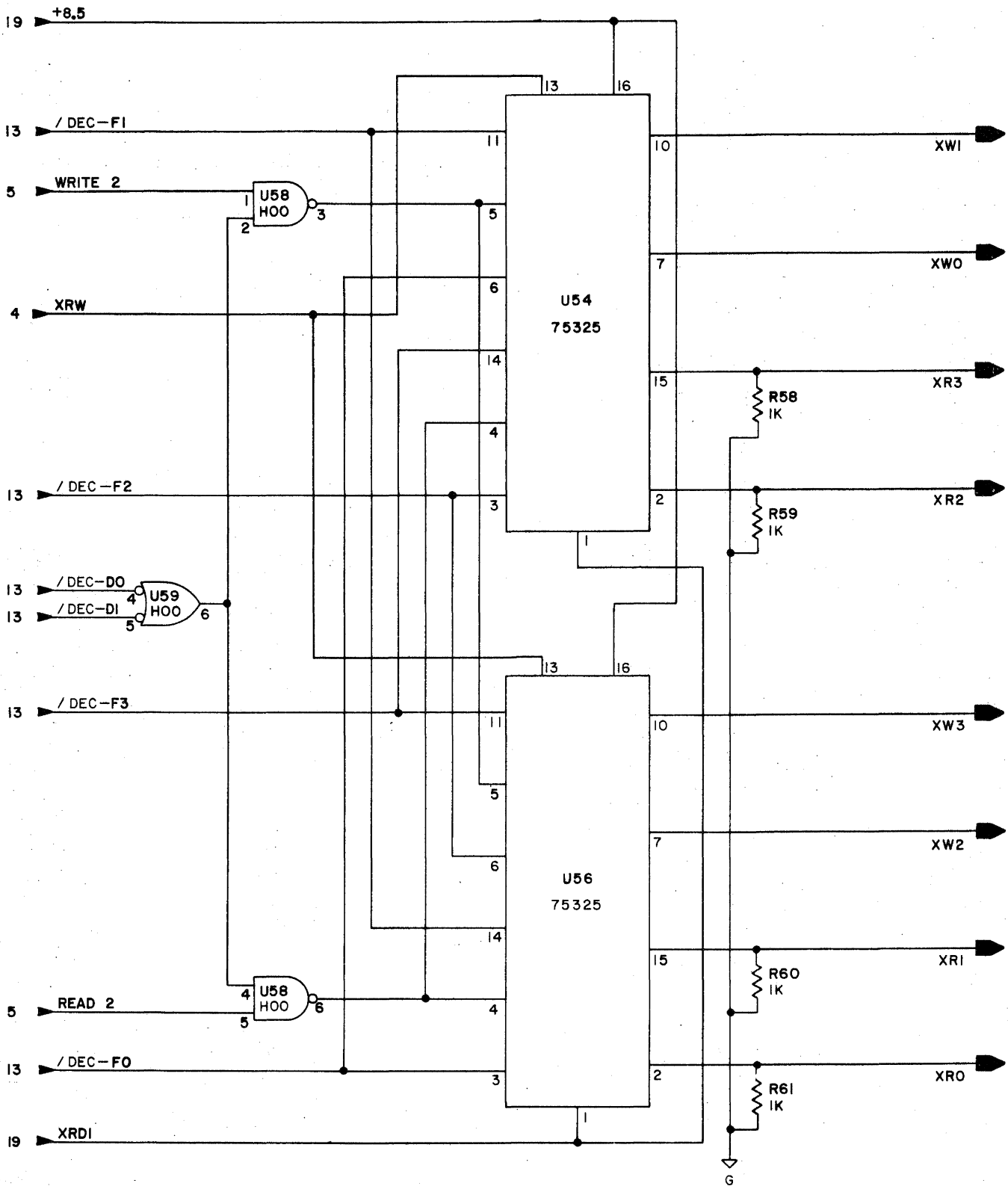
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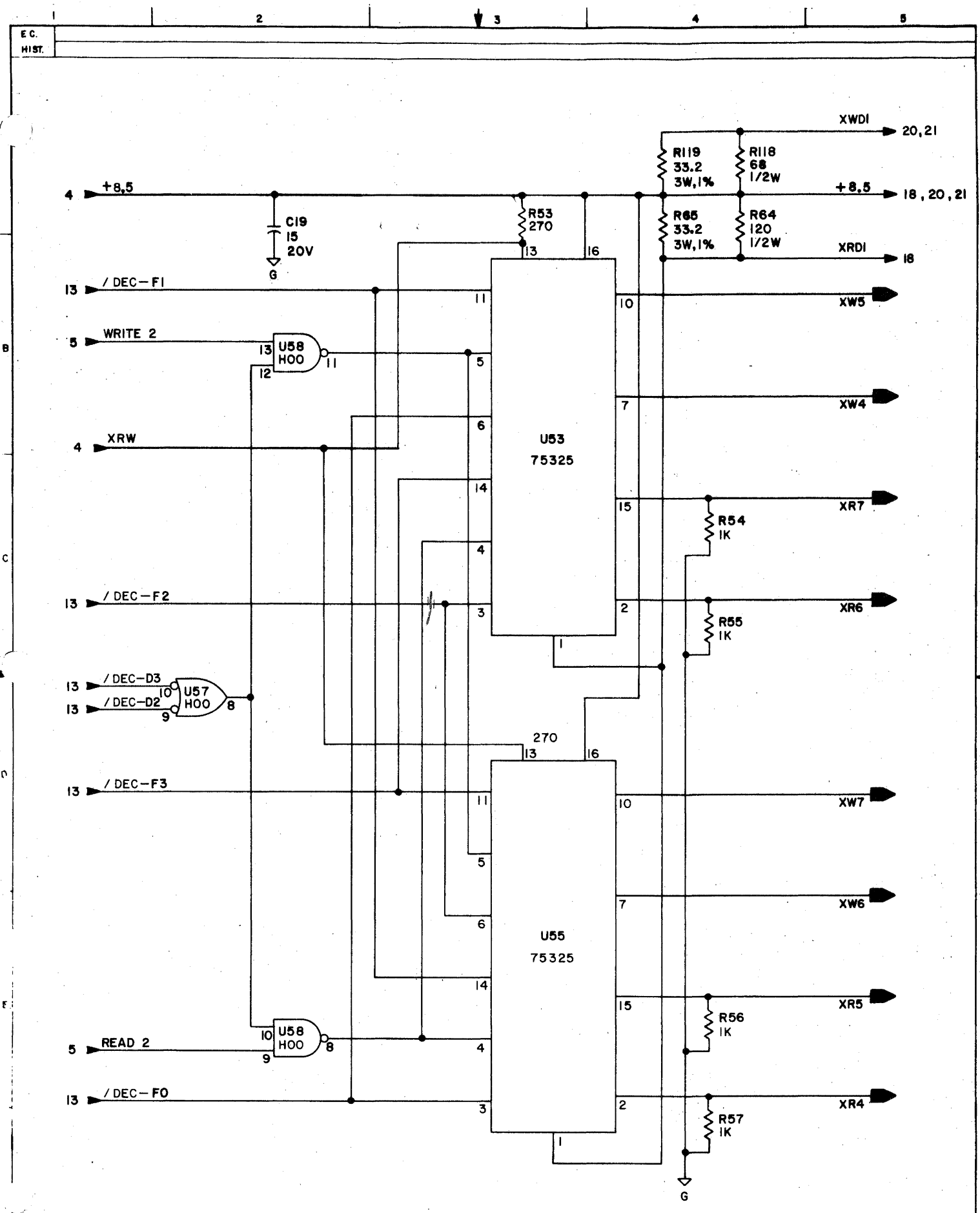
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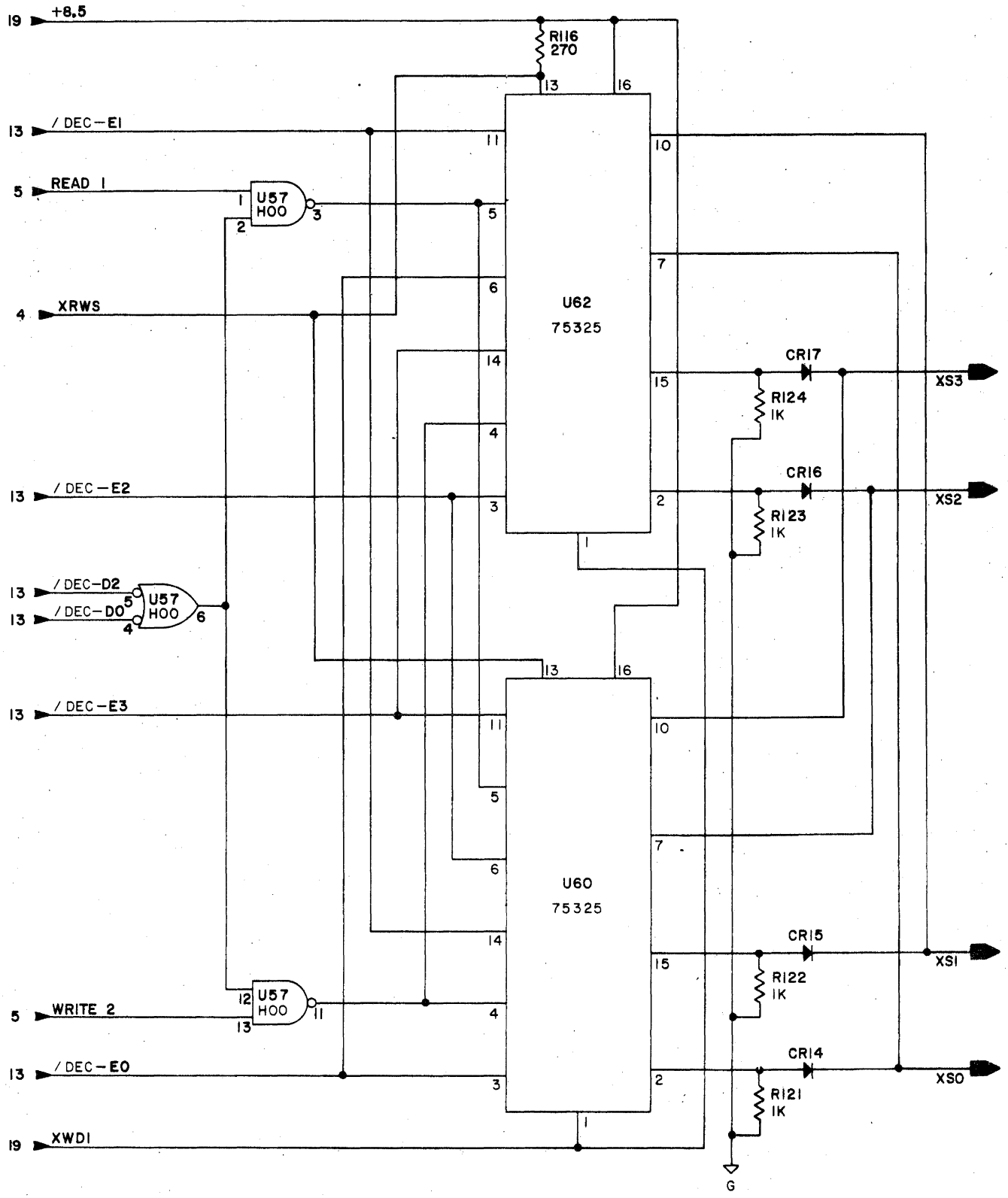
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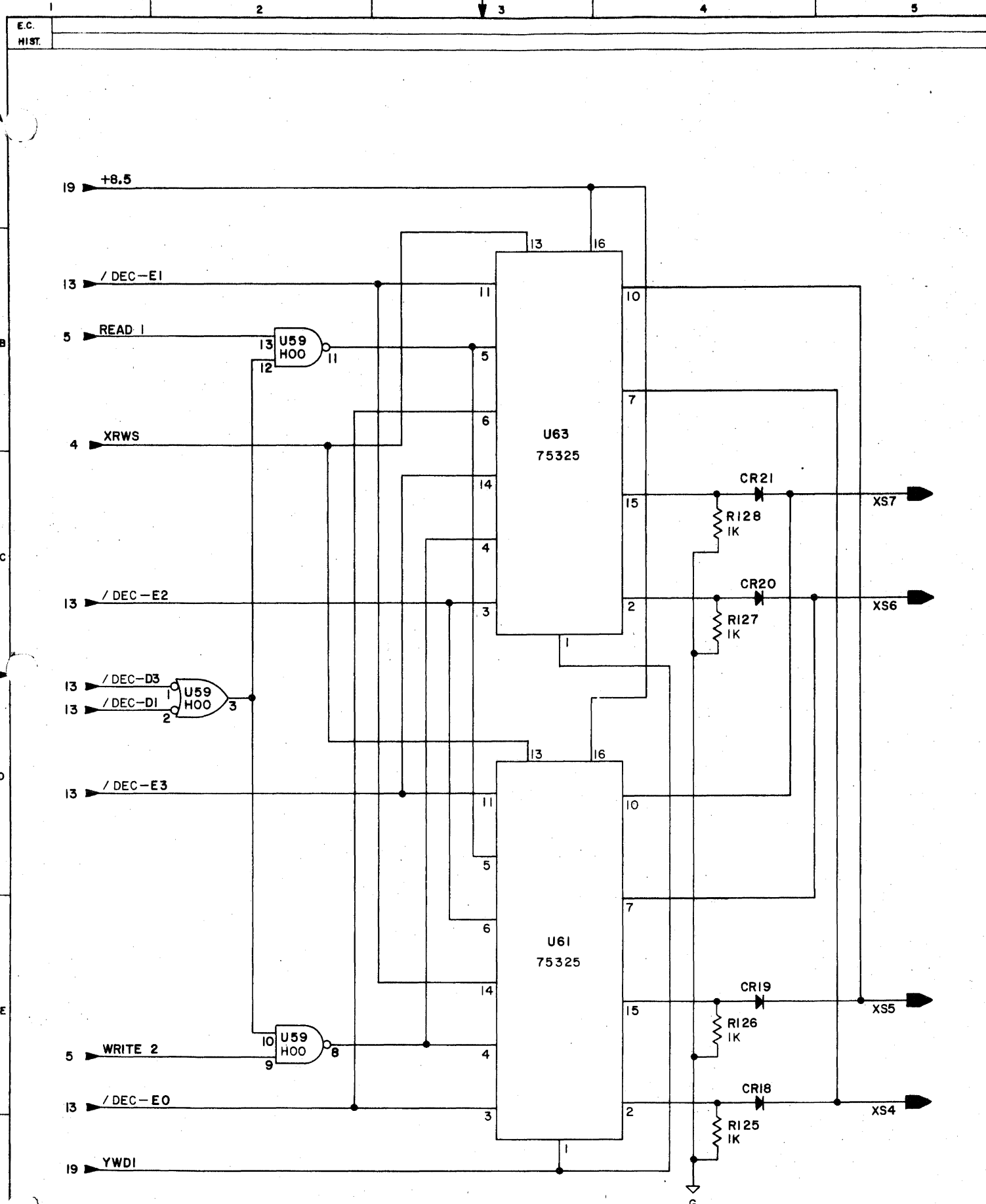
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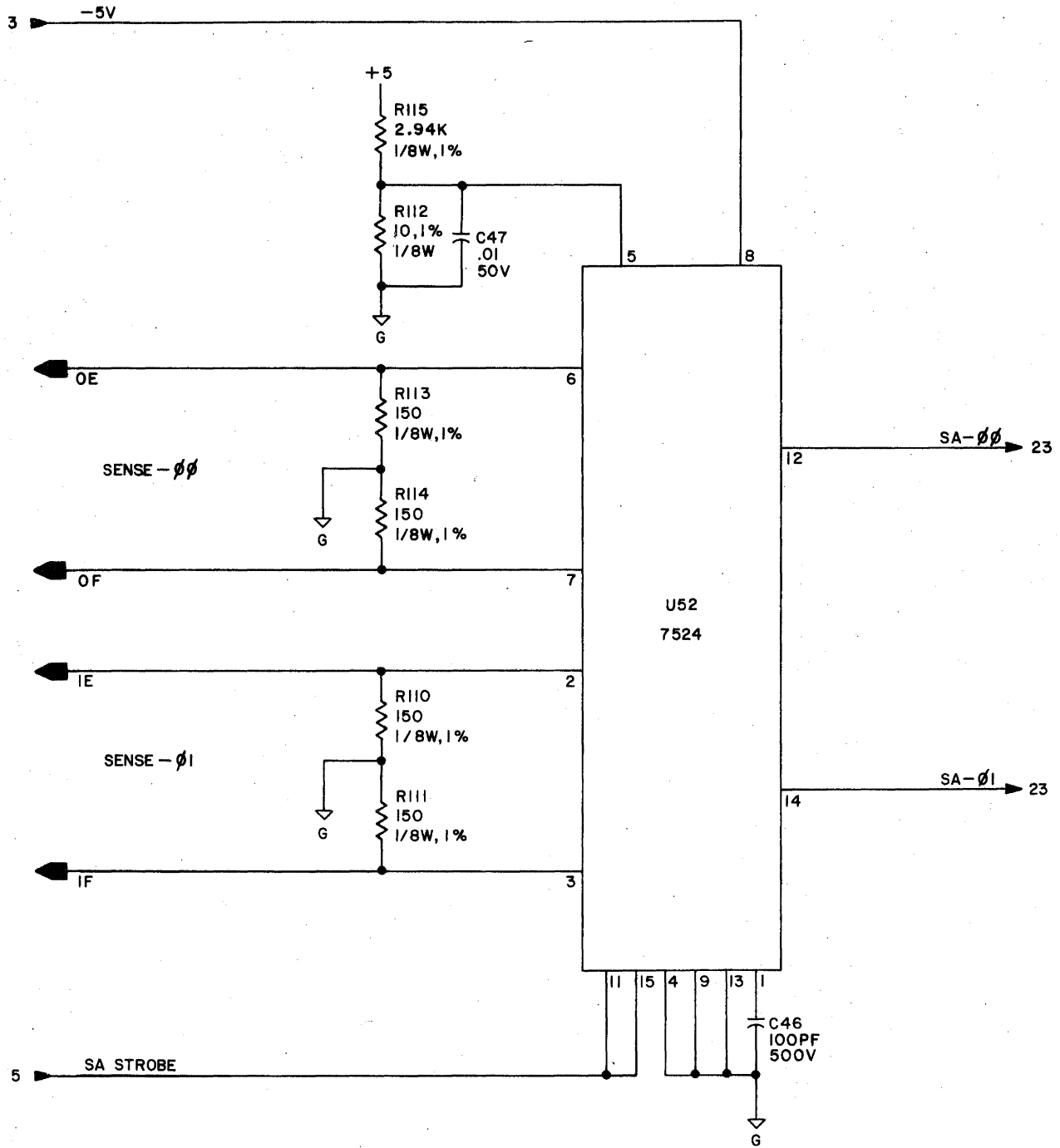


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FABRI-TEK INC.
COMPUTER SYSTEMS

TITLE SCHEMATIC, MEMORY ELECTRONICS BOARD

DWG. NO. C 138-0020-19

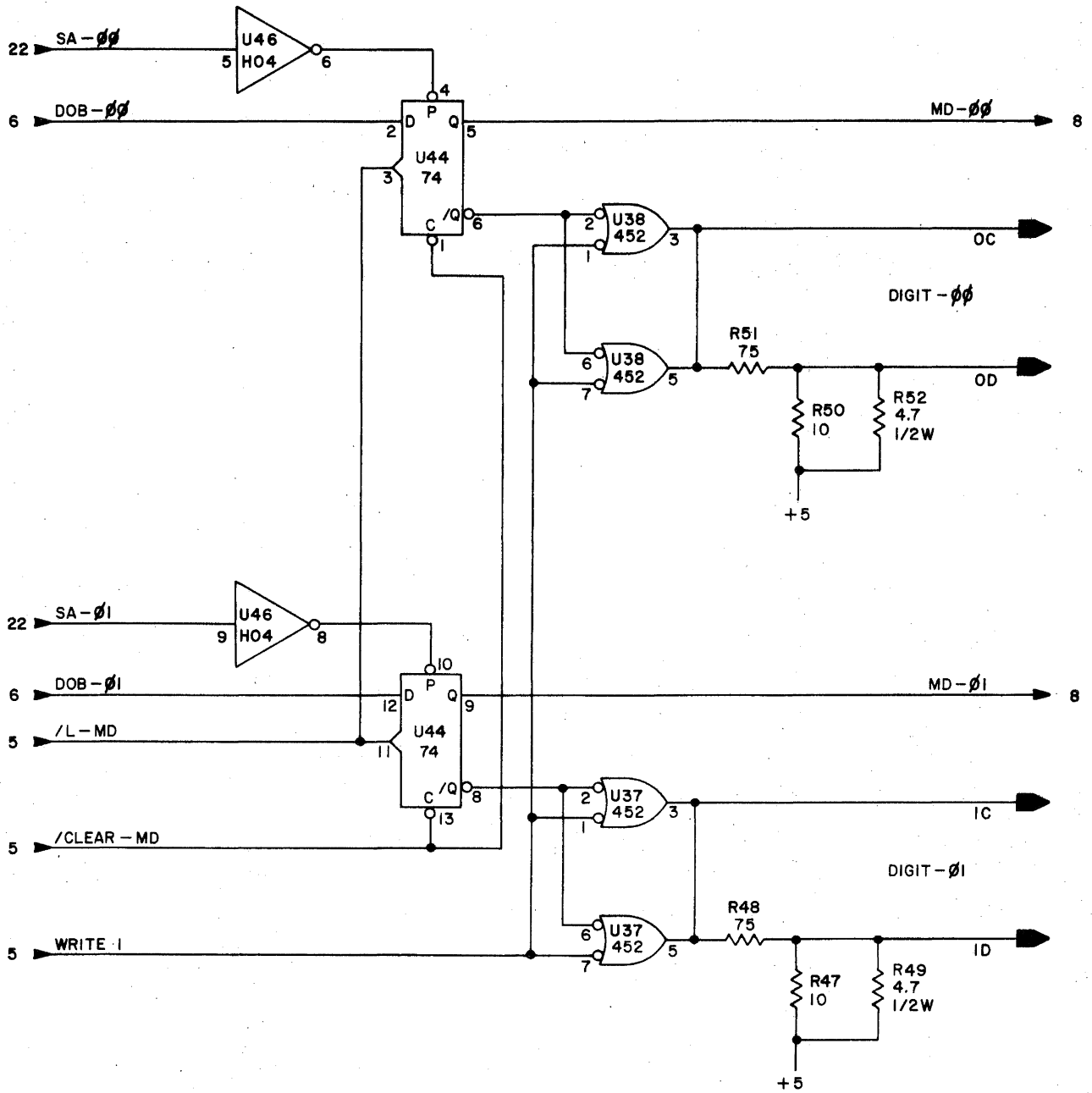
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VERS.

PAGE

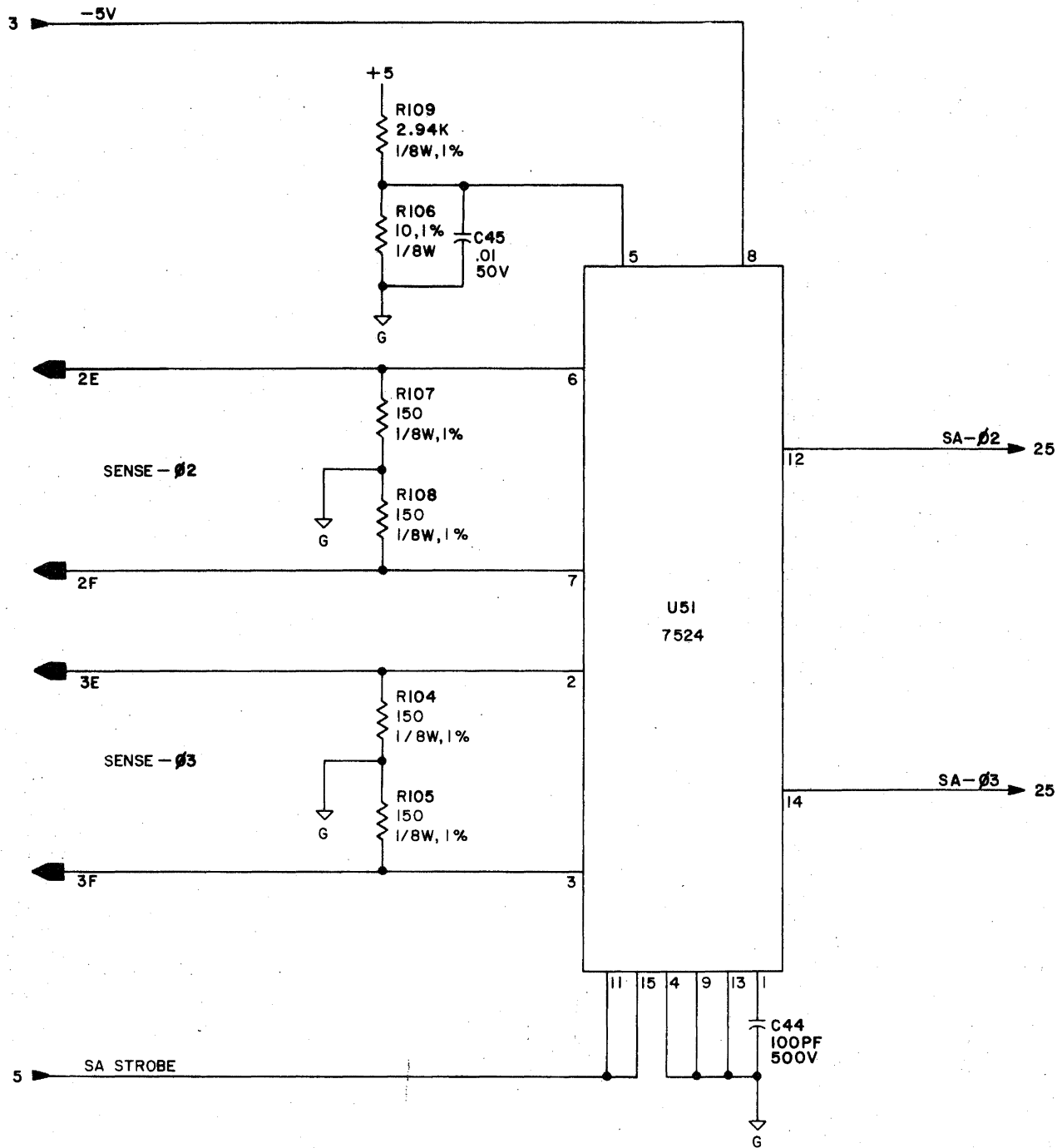
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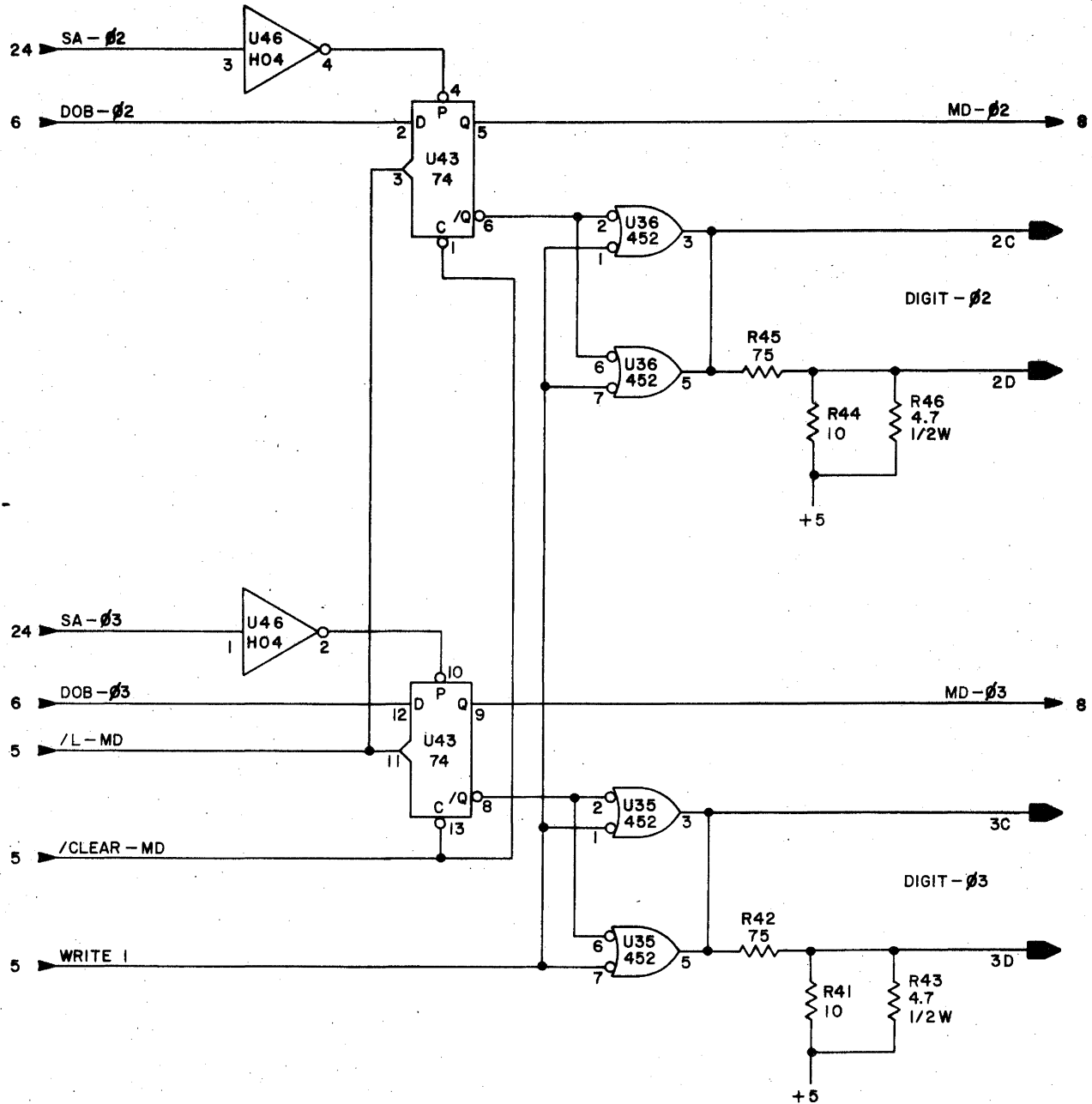
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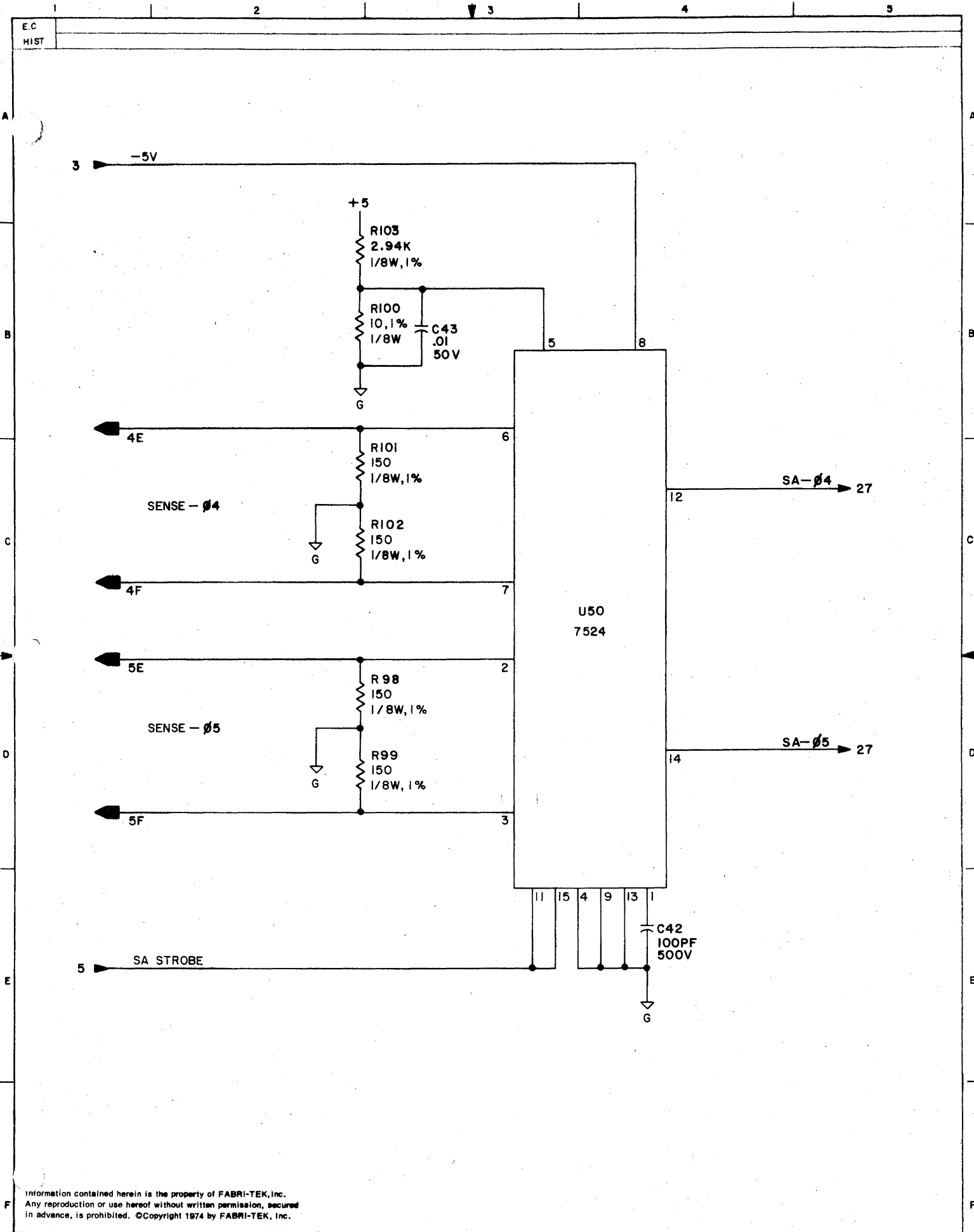


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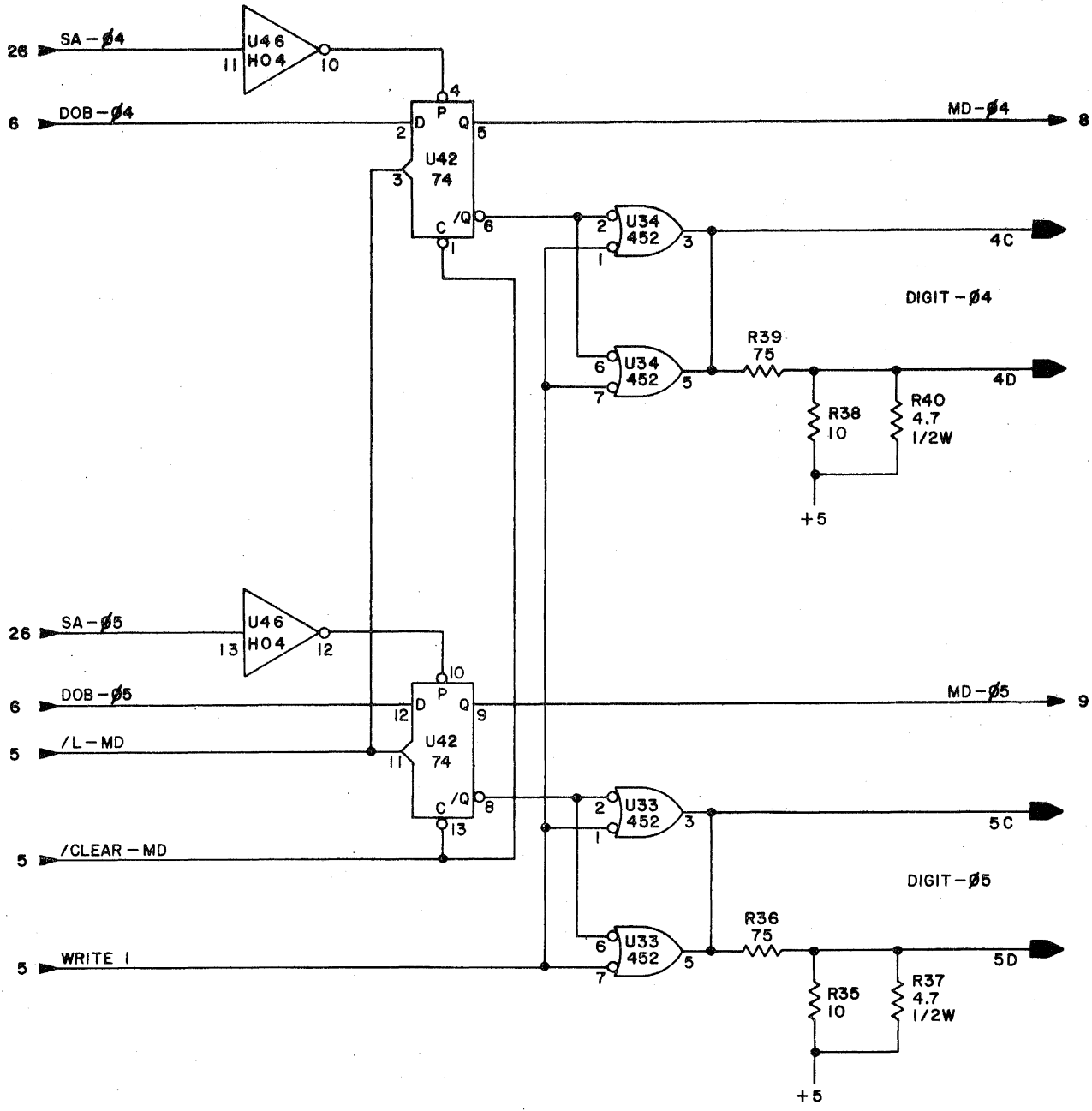
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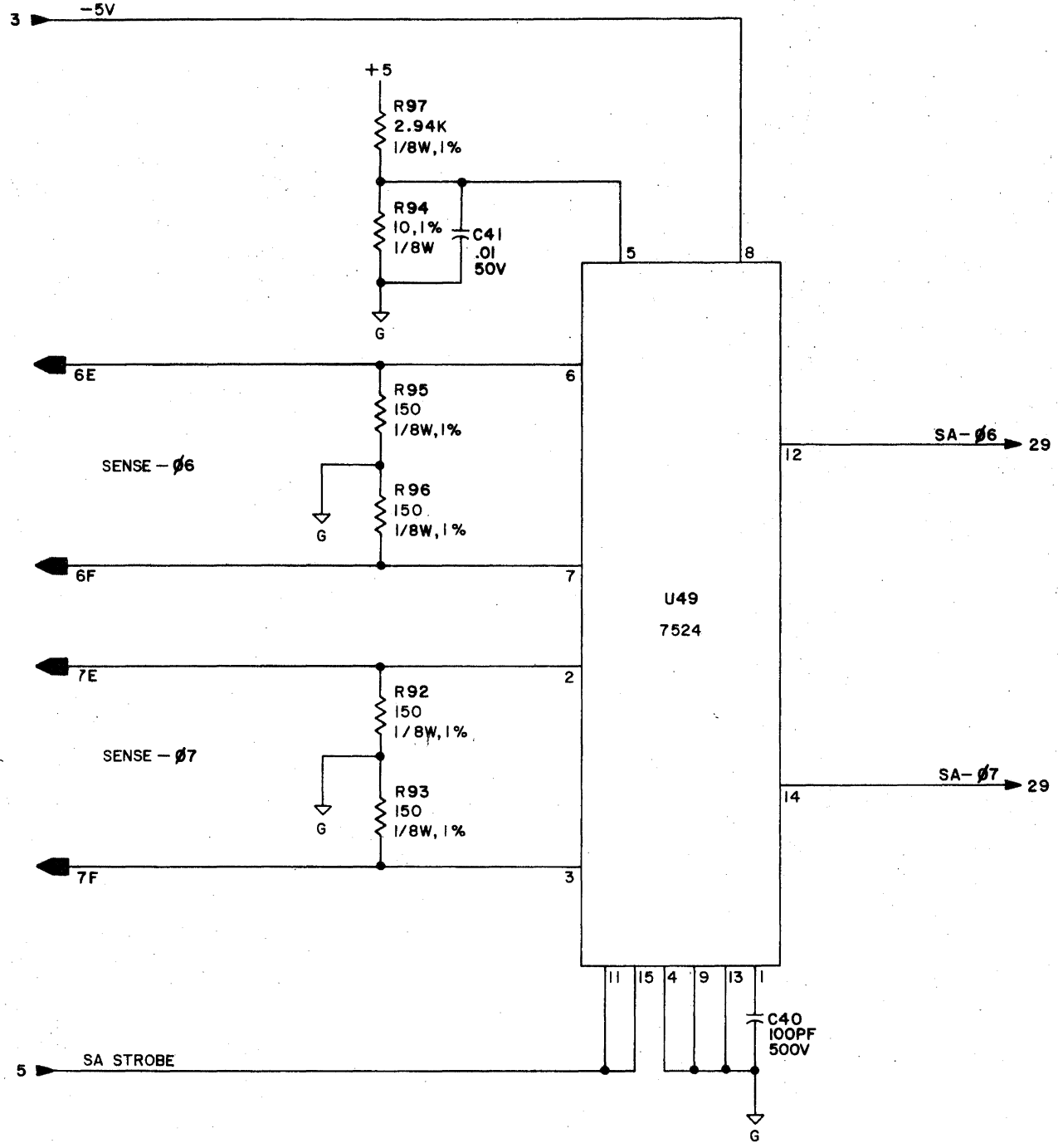


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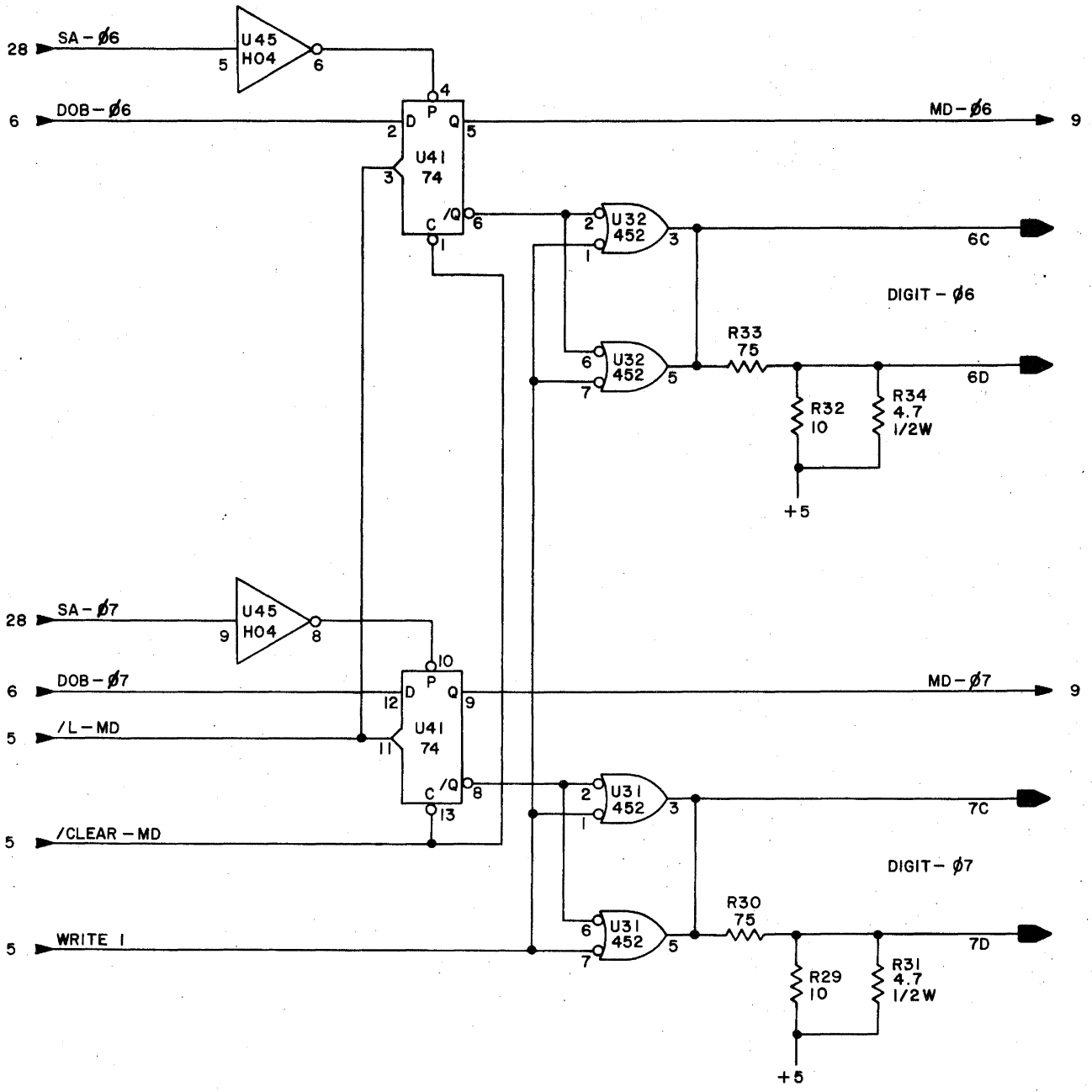
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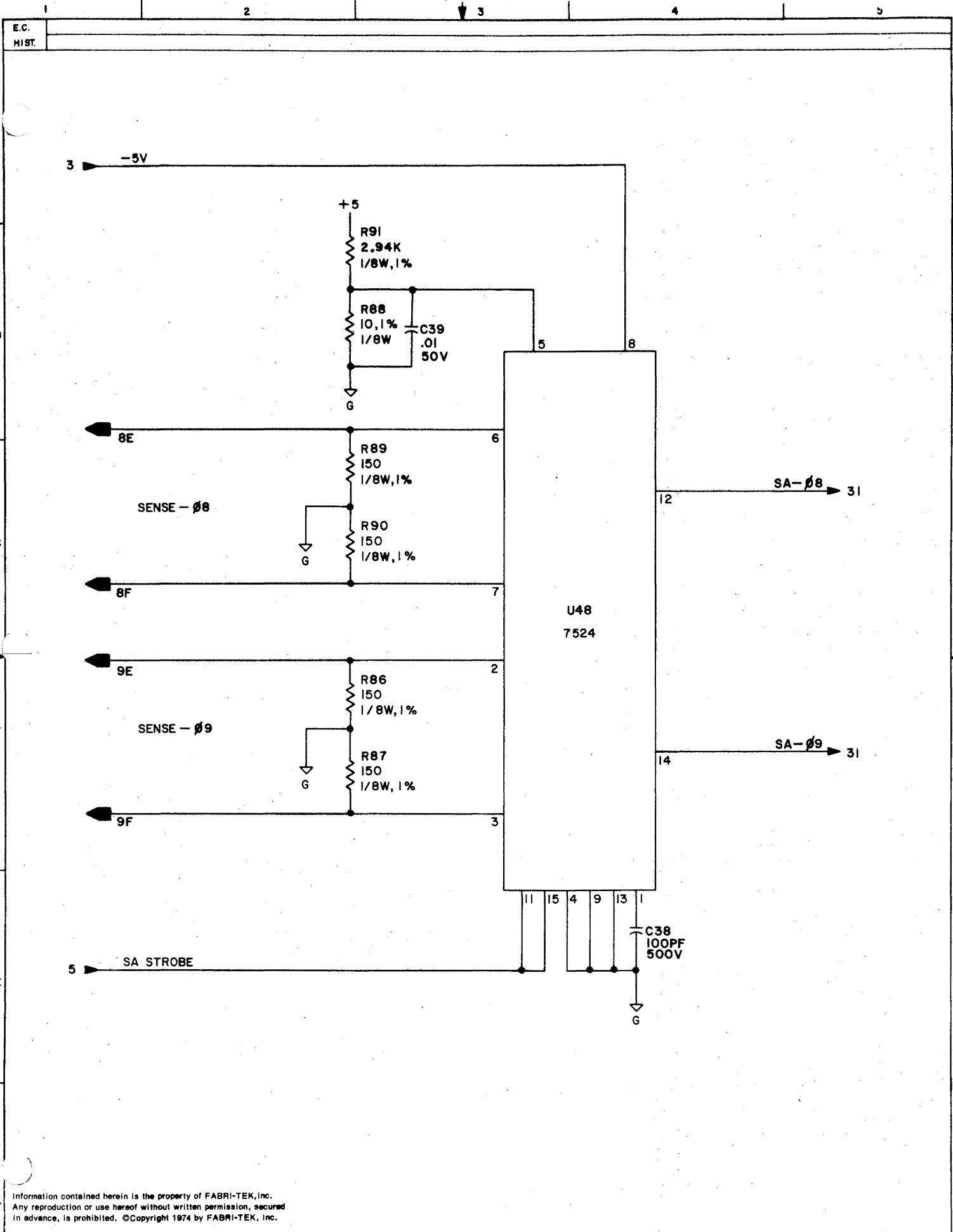


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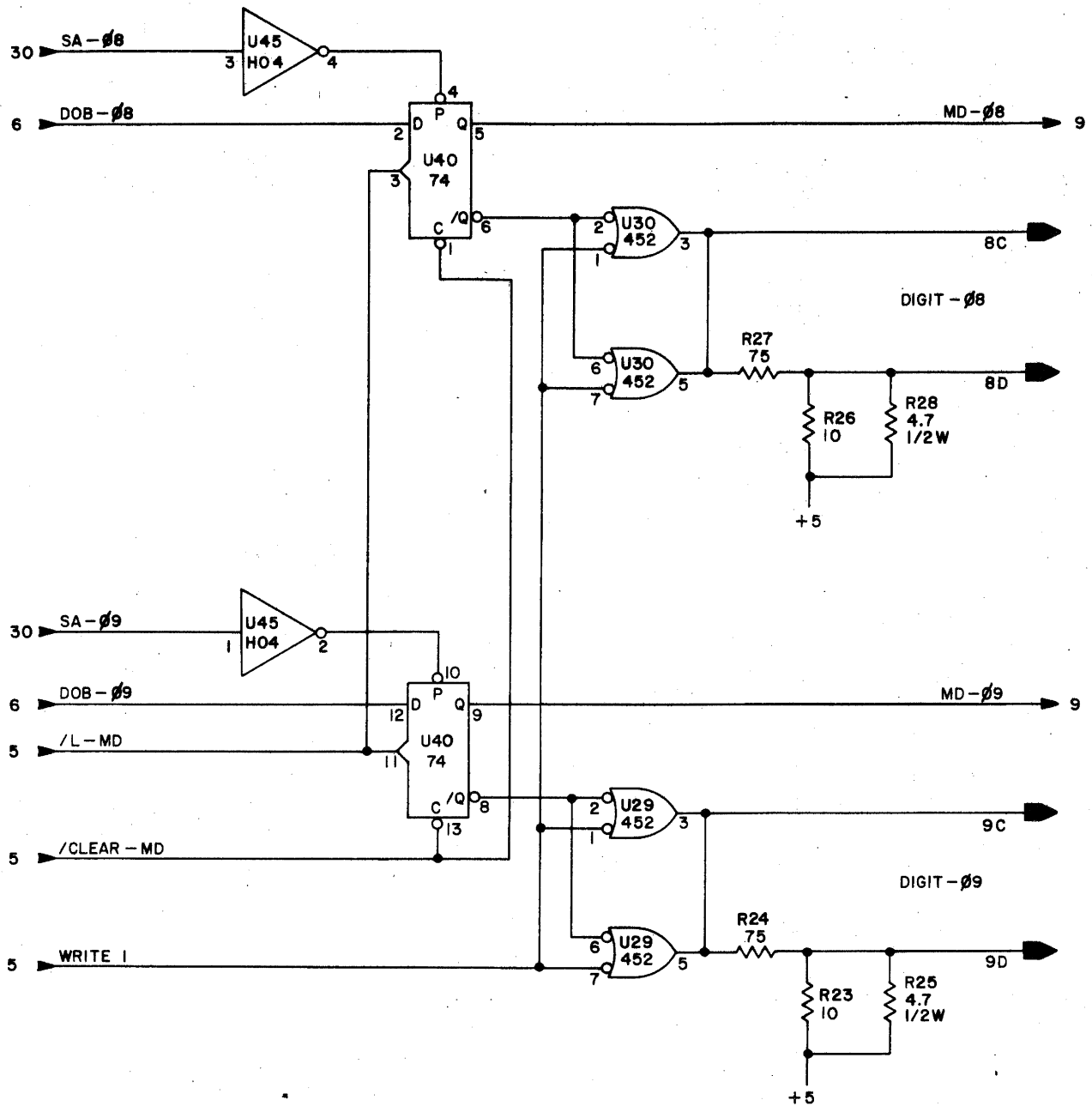


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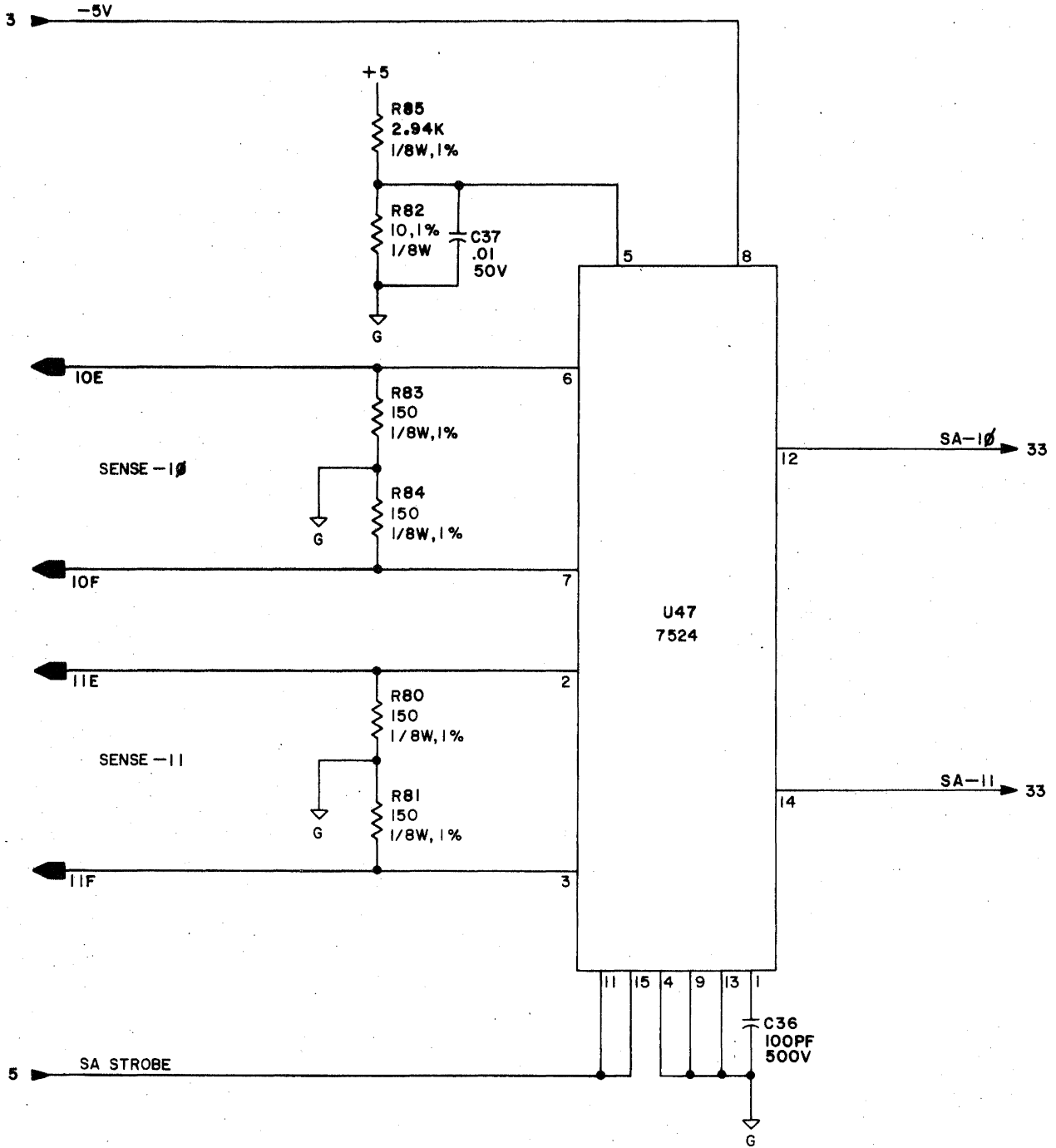
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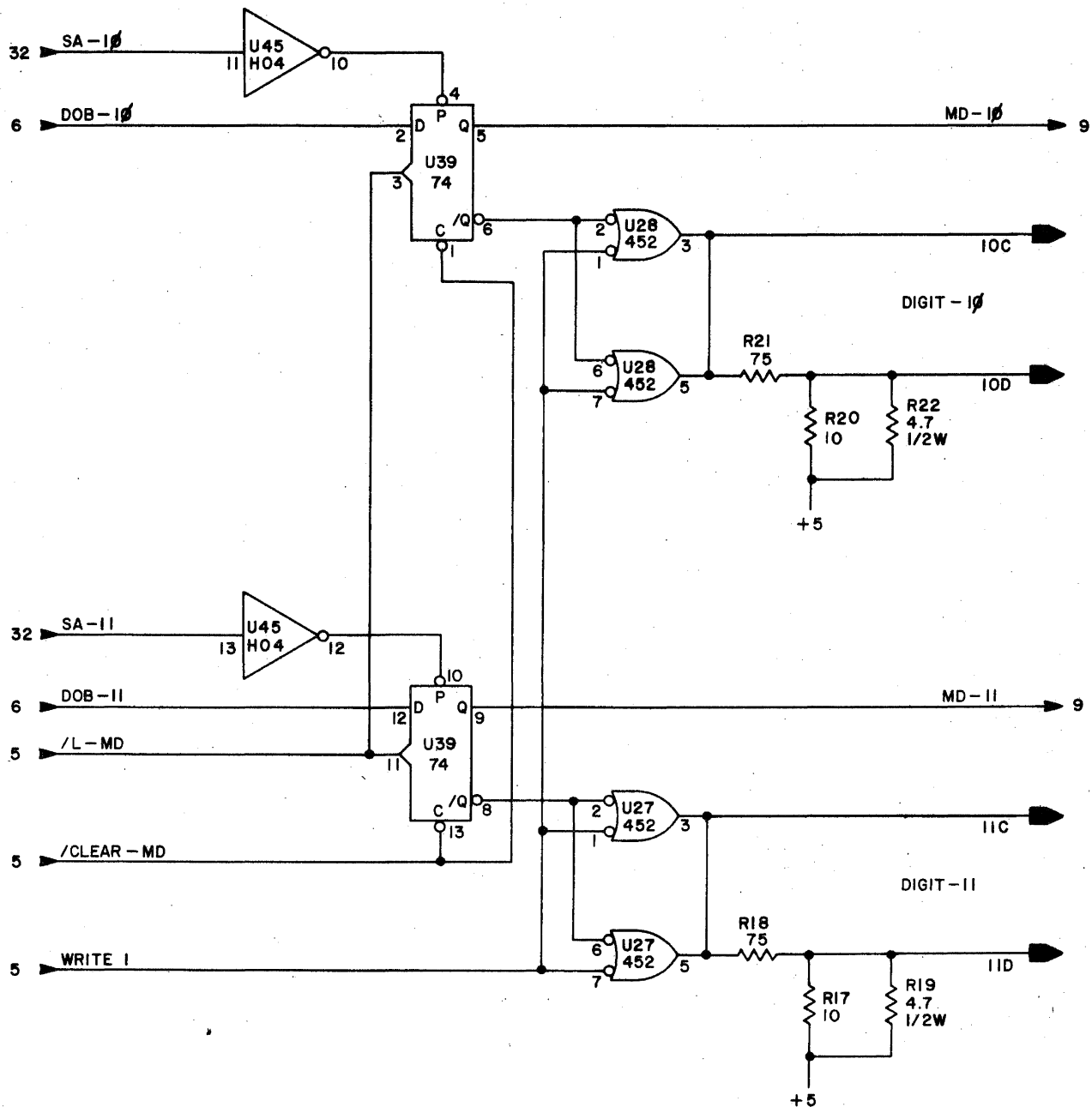
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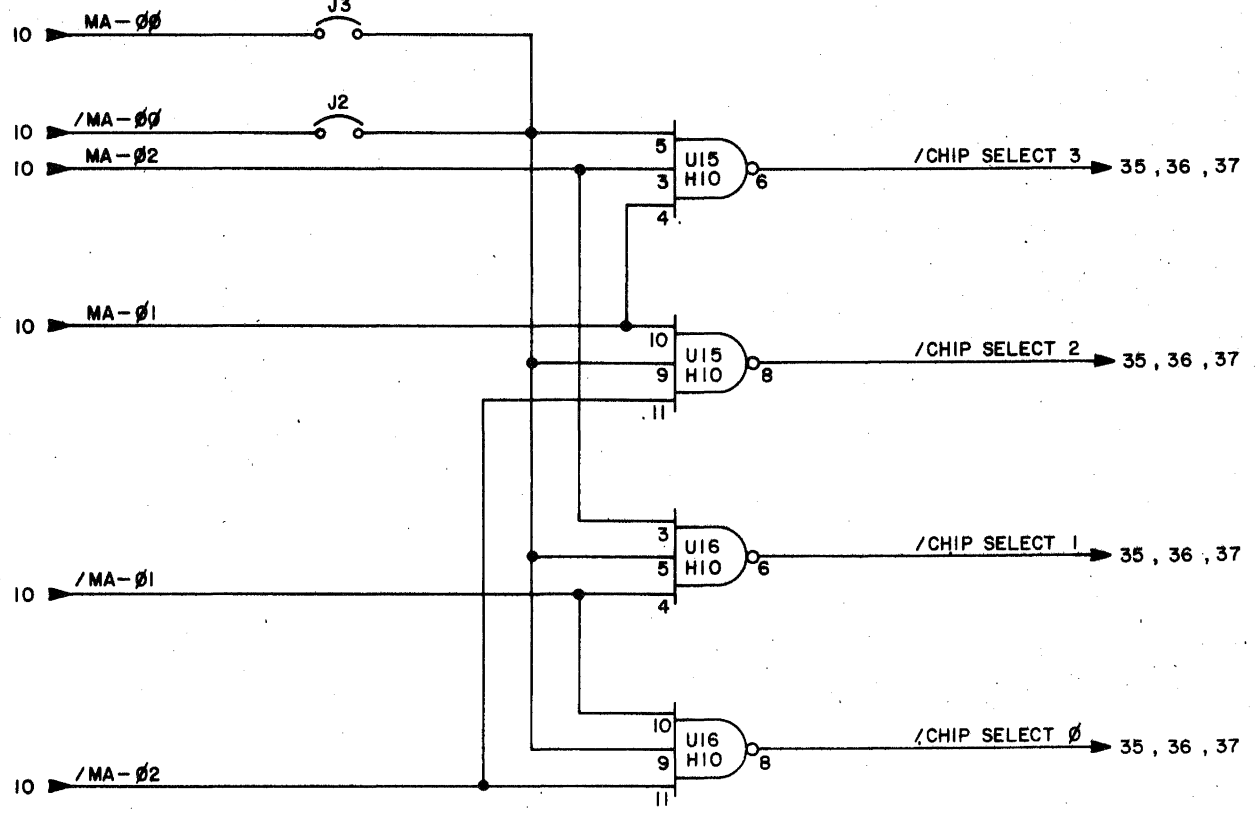
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FOR INSTALLATION OF
JUMPER REFER TO
TABLE I BELOW

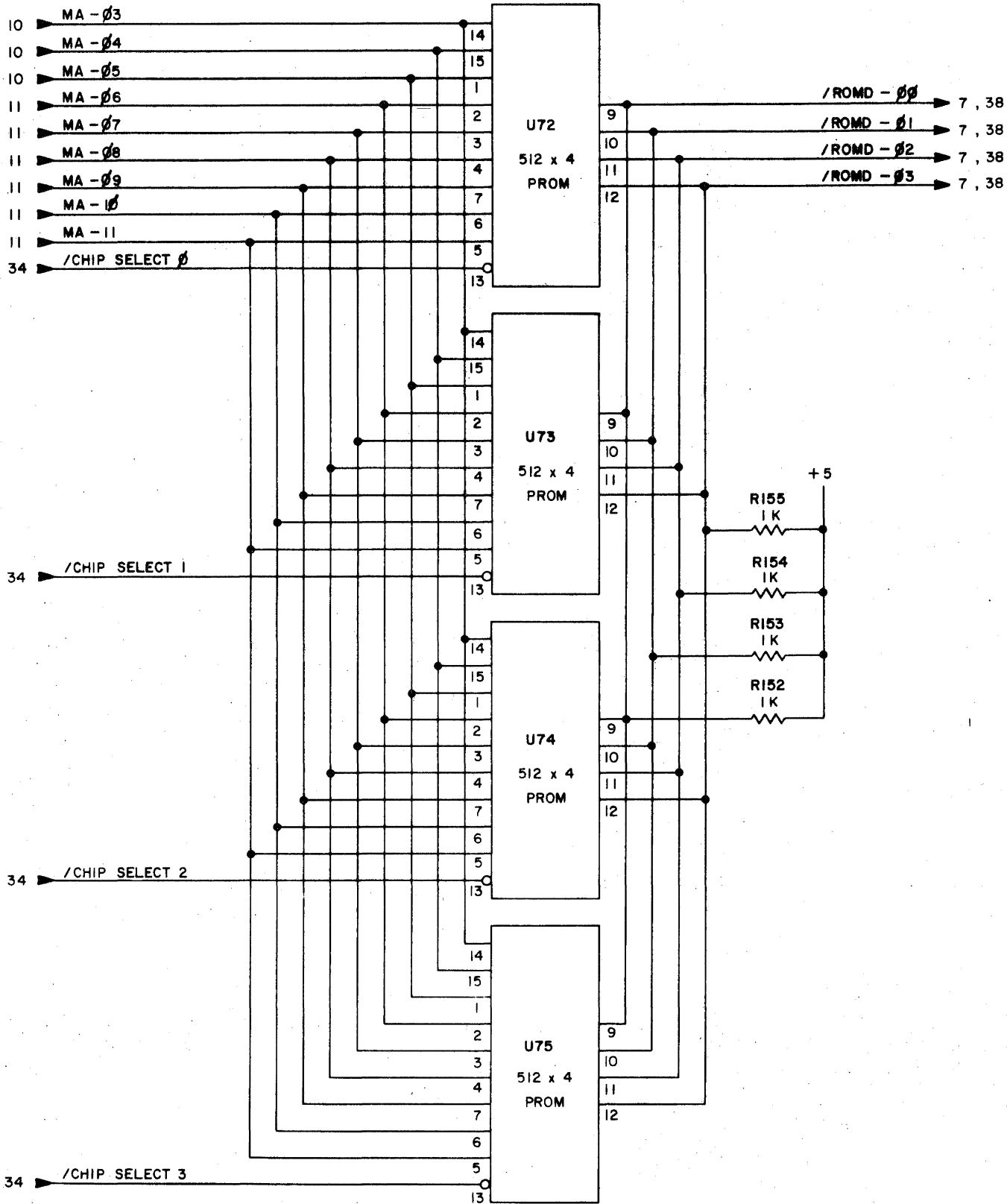


CHIP SELECT	MEMORY ADDRESS		MD-BIT			JUMPER INSTALLED
	CHIP ADDR	777 000	00-03	04-07	08-11	
3	7	777 000	U75	U71	U67	J3
	7	777 000				
	6	777 000	U74	U70	U66	
	6	777 000				
2	5	777 000	U73	U69	U65	J2
	5	777 000				
	4	777 000	U72	U68	U64	
	4	777 000				
0	3	777 000	U75	U71	U67	J2
	3	777 000				
	2	777 000	U74	U70	U66	
	2	777 000				
1	1	777 000	U73	U69	U65	J2
	1	777 000				
	0	777 000	U72	U68	U64	
	0	777 000				

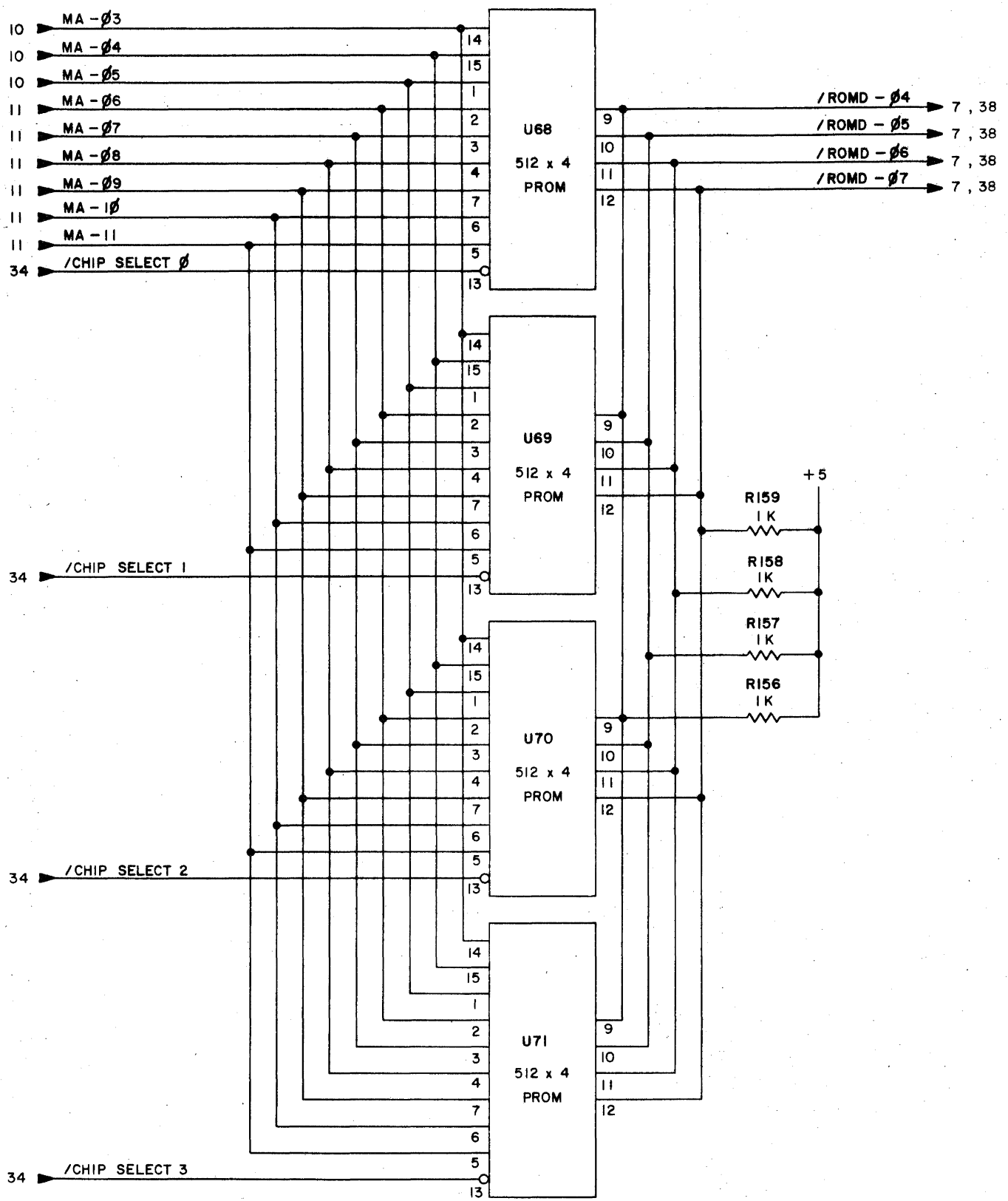
PROM LOCATION
TABLE I

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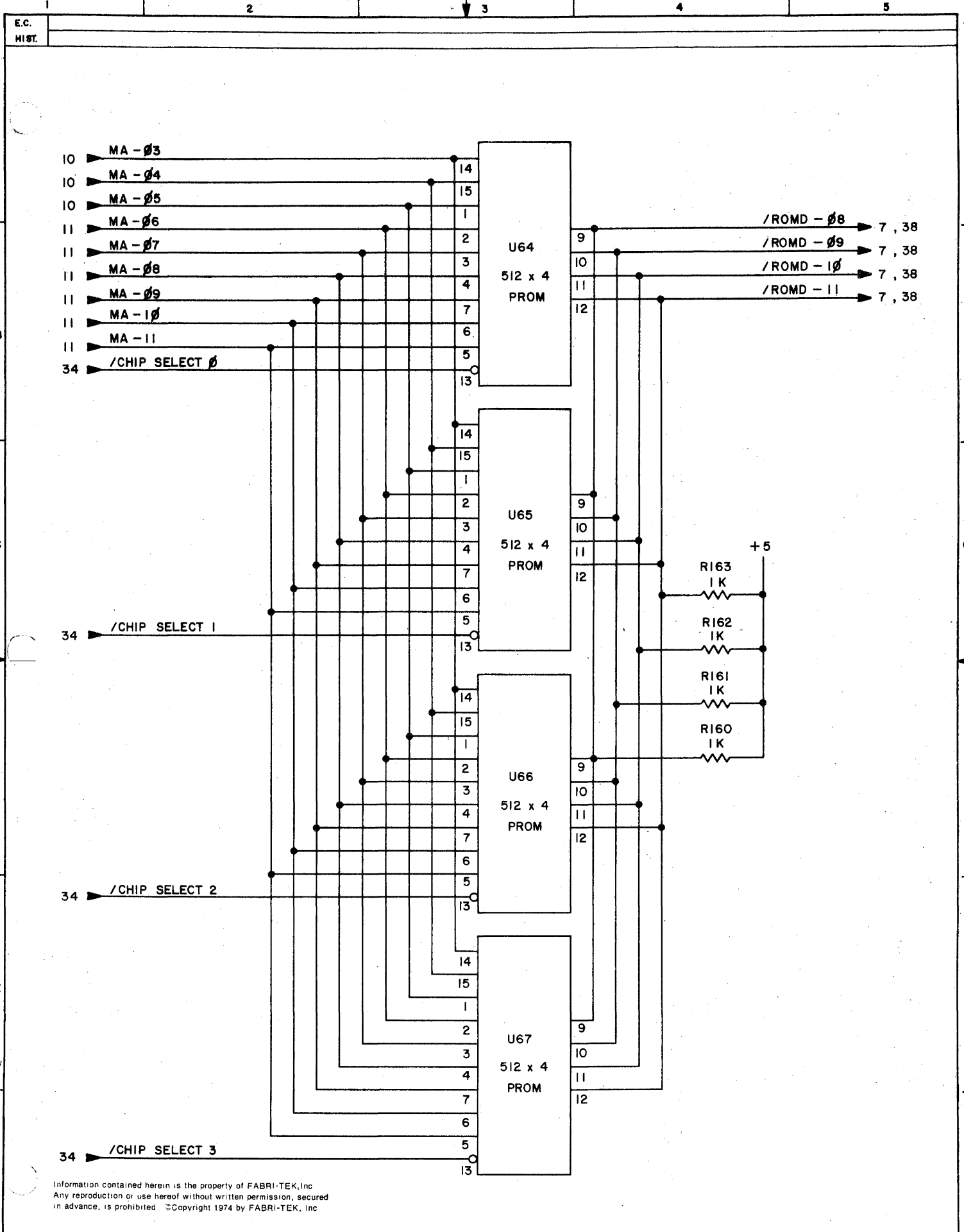
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HIST



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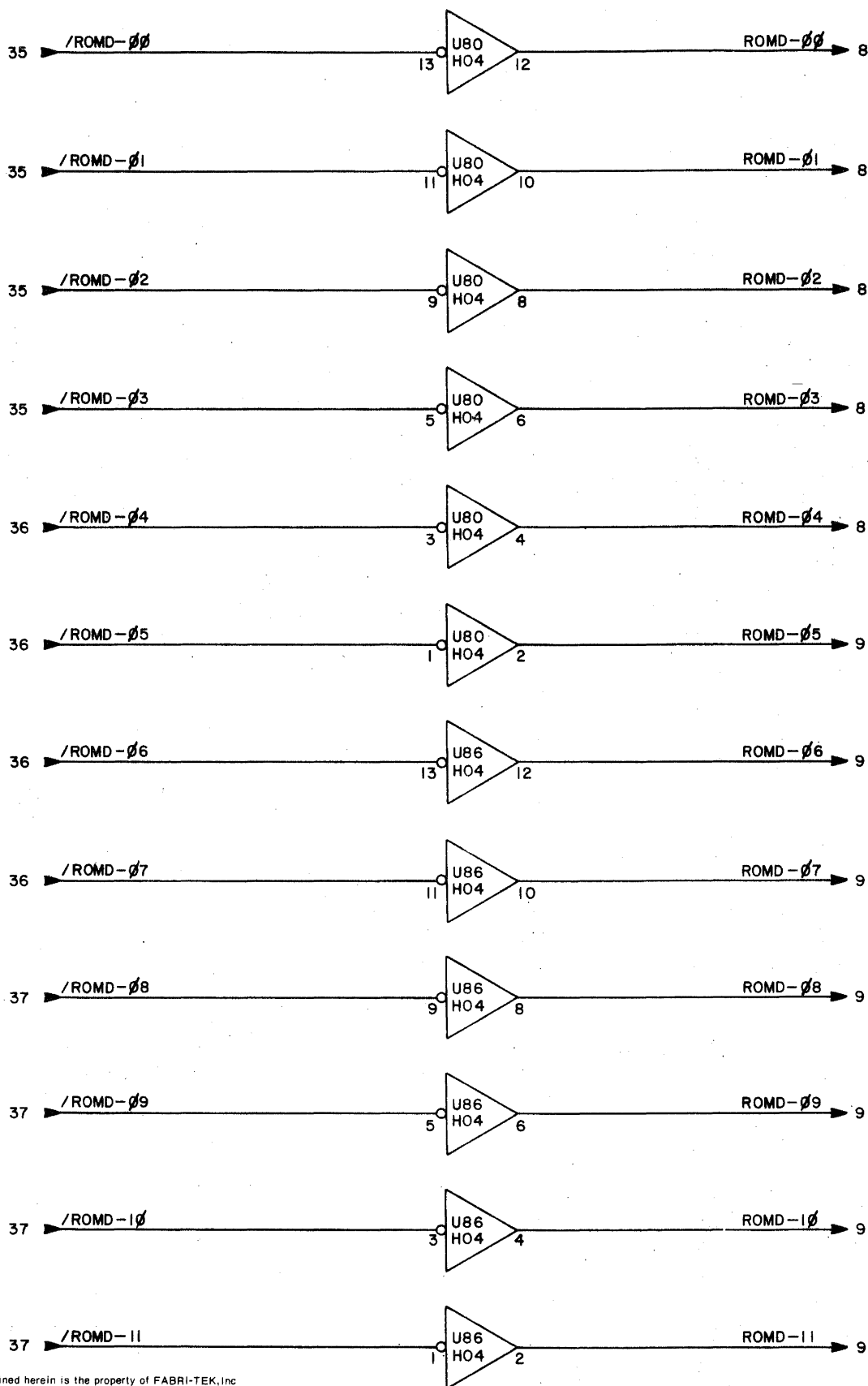
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NOTES: APPLICABLE THROUGHOUT THIS SCHEMATIC.

1. UNLESS OTHERWISE STATED:

- A. RESISTANCE VALUES ARE IN OHMS. RESISTORS ARE 5% TOLERANCE, 1/4 WATT.
- B. CAPACITANCE VALUES ARE IN MICROFARADS.

2. JEDEC OR MANUFACTURER'S PART NUMBERS ARE FOR REFERENCE ONLY. FOR EXPLICIT DESCRIPTION OF THE DEVICE CHARACTERISTICS, REFER TO THE FABRI-TEK SPECIFICATION FOR THE FABRI-TEK PART NUMBER.

3. ← INDICATES PIN FOR CONNECTION TO PROCESSOR BOARD.

REVISION STATUS OF SHEETS															

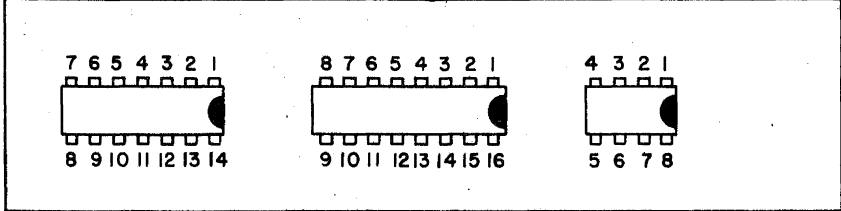
		DATE
DRAWN	LAI	1/5/74
CHECKED	POON	1/7/74
APPROVED	<i>[Signature]</i>	3/12/74

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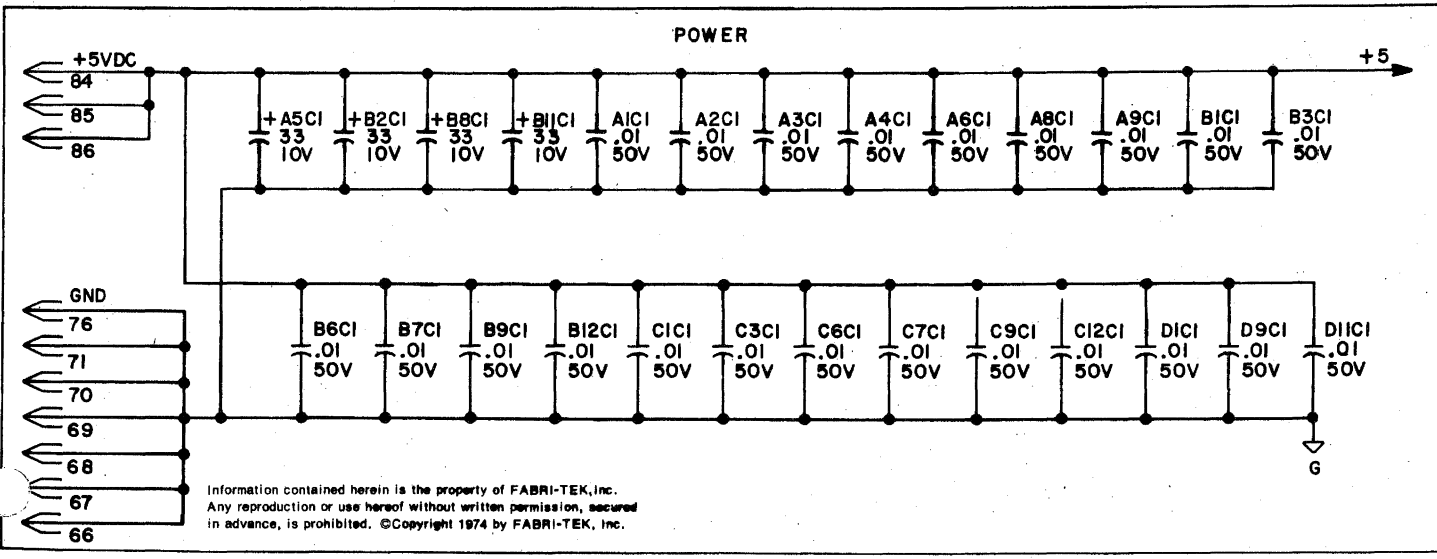
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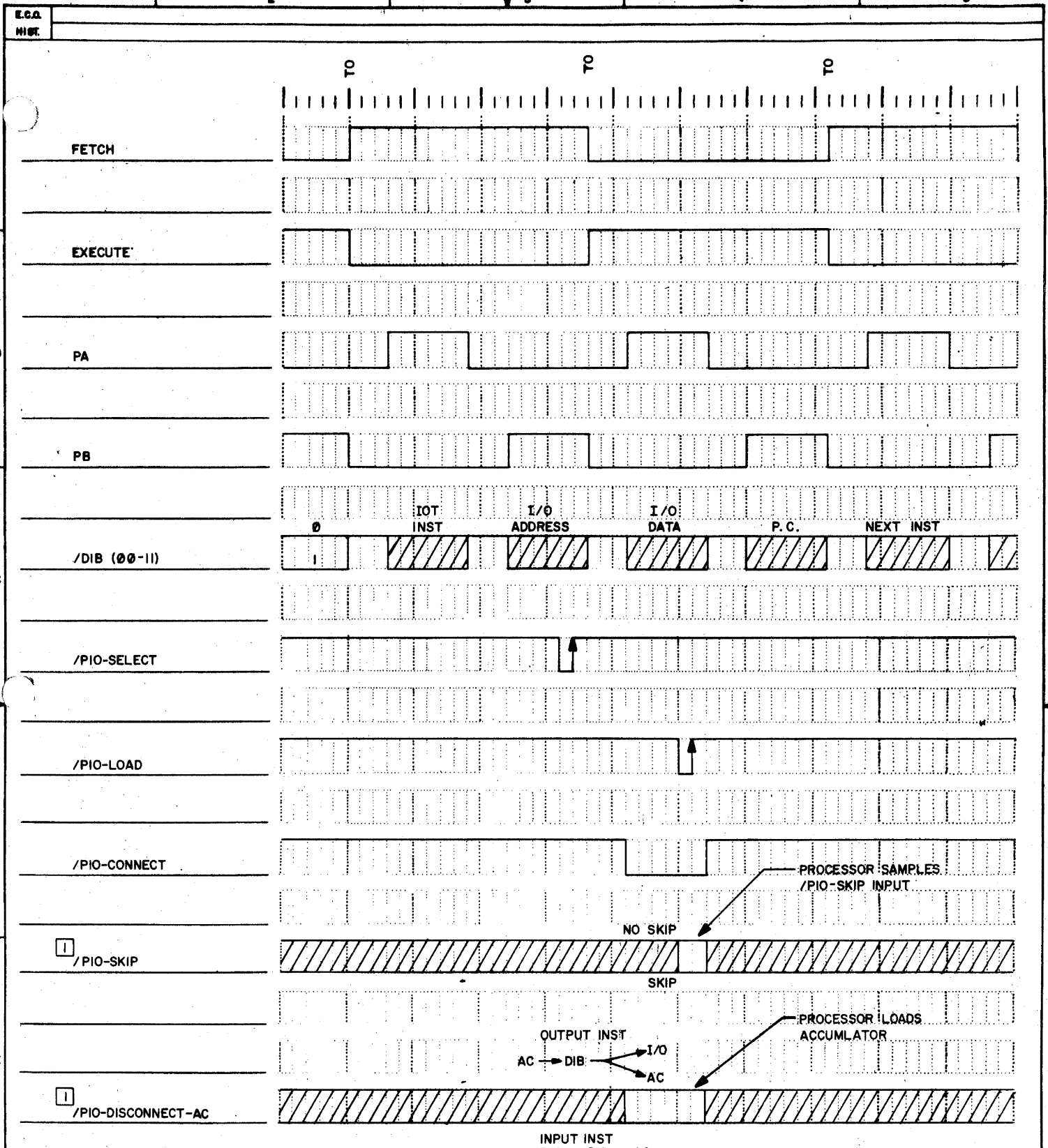
MODULE CODE TABLE

CODE	VENDOR	VENDORS P/N	DESCRIPTION			TOTAL NO OF PINS
				+5V	GND	
H00	T. I.	SN74H00	QUAD 2-INPUT NAND	14	7	14
H04	T. I.	SN74H04	HEX INVERTER	14	7	14
H08	SP	US74H08A	QUAD 2-INPUT AND	14	7	14
H10	T. I.	SN74H10	TRIPLE 3-INPUT NAND	14	7	14
H11	T. I.	SN74H11	TRIPLE 3-INPUT AND	14	7	14
H20	T. I.	SN74H20	DUAL 4-INPUT NAND	14	7	14
H21	T. I.	SN74H21	DUAL 4-INPUT AND	14	7	14
H38	SP	US74H38A	QUAD 2-INPUT NAND BUFF OC	14	7	14
74	T. I.	SN7474	DUAL D-TYPE FLIP FLOP	14	7	14
123	T. I.	SN74123	DUAL MONO MV W/CLEAR	16	8	16



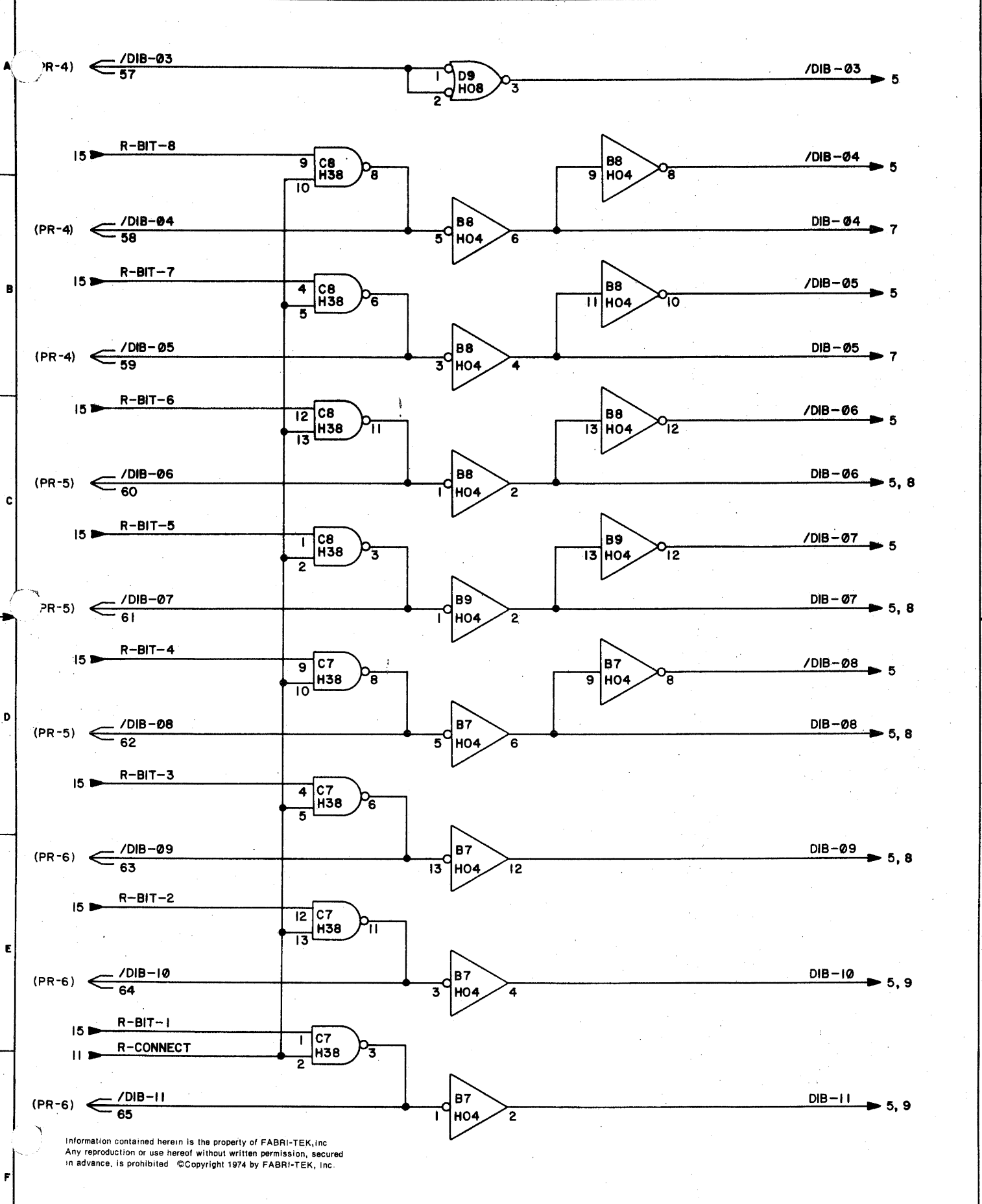
POWER



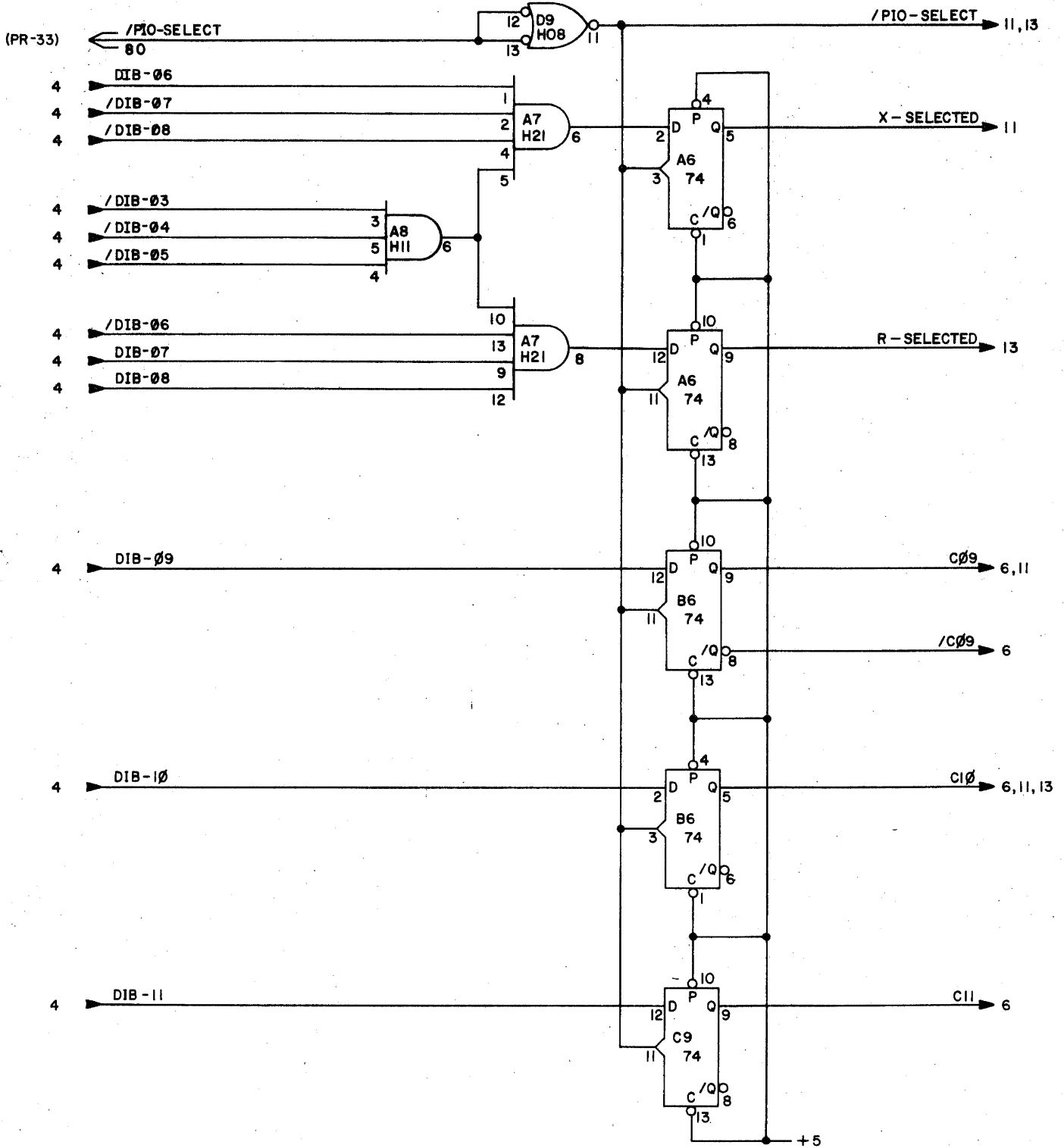


NOTE:
 1. SIGNALS GENERATED BY PIO DEVICE CONTROLLER.
 2. EACH DIVISION REPRESENTS 83 NS.

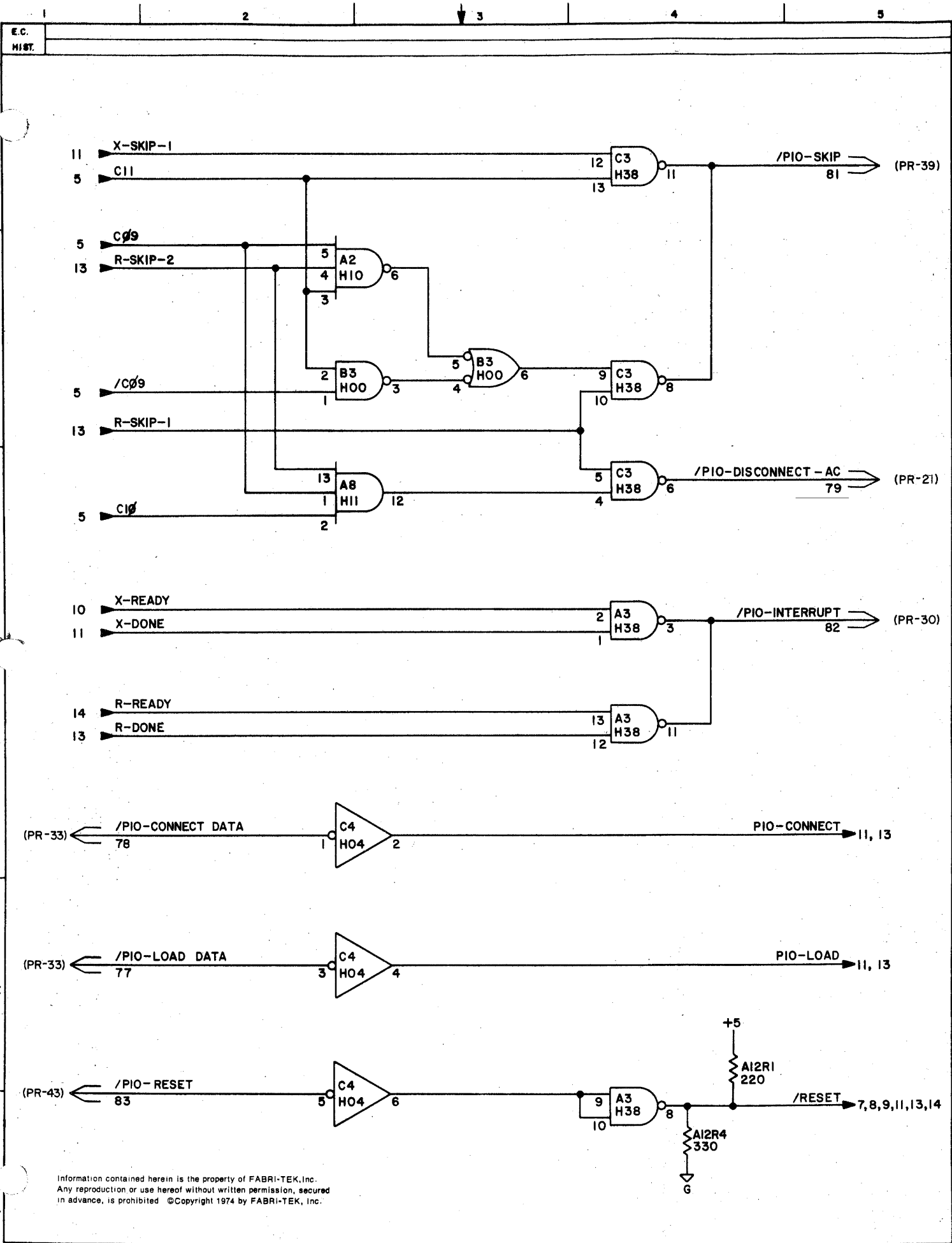
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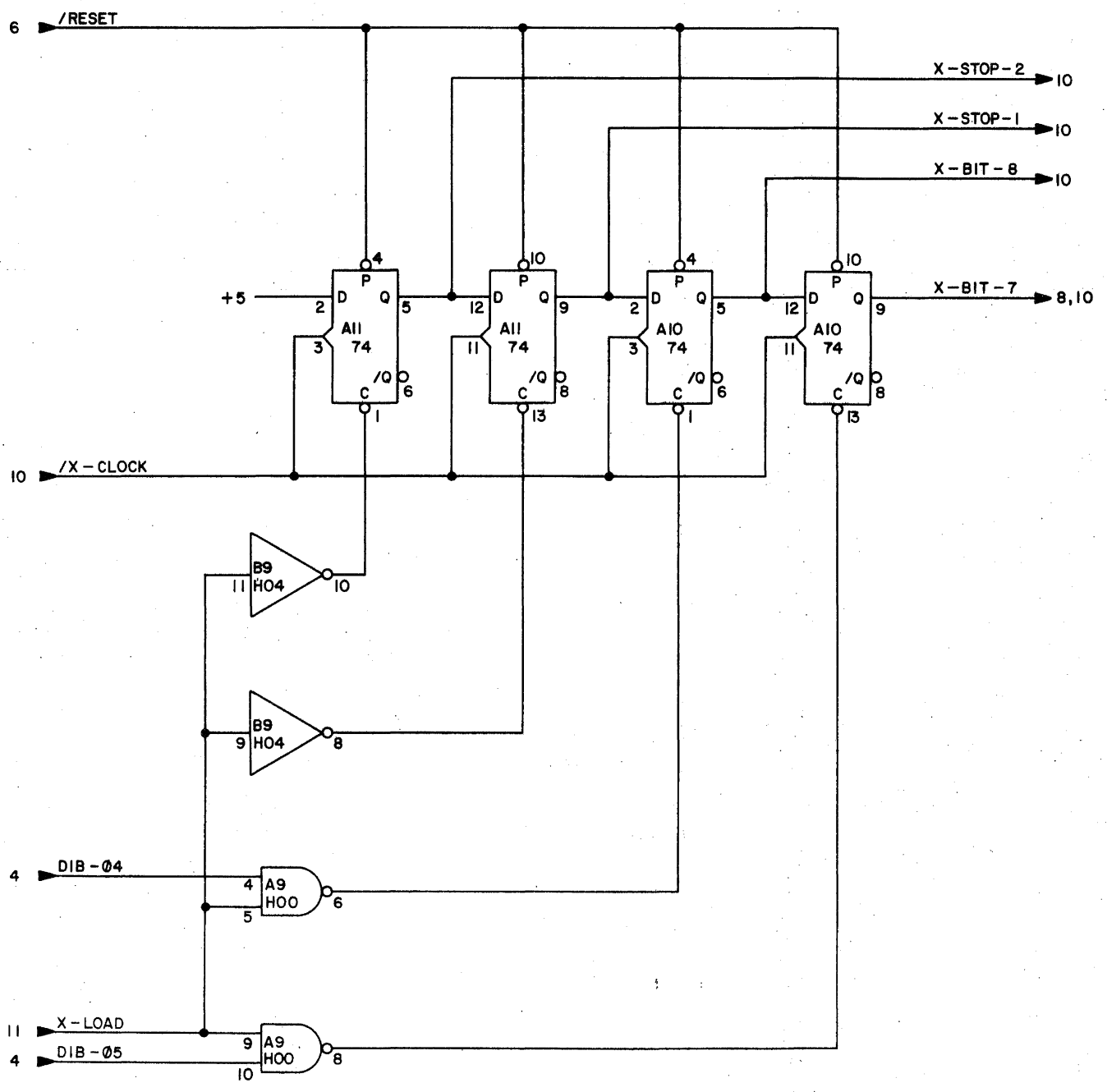


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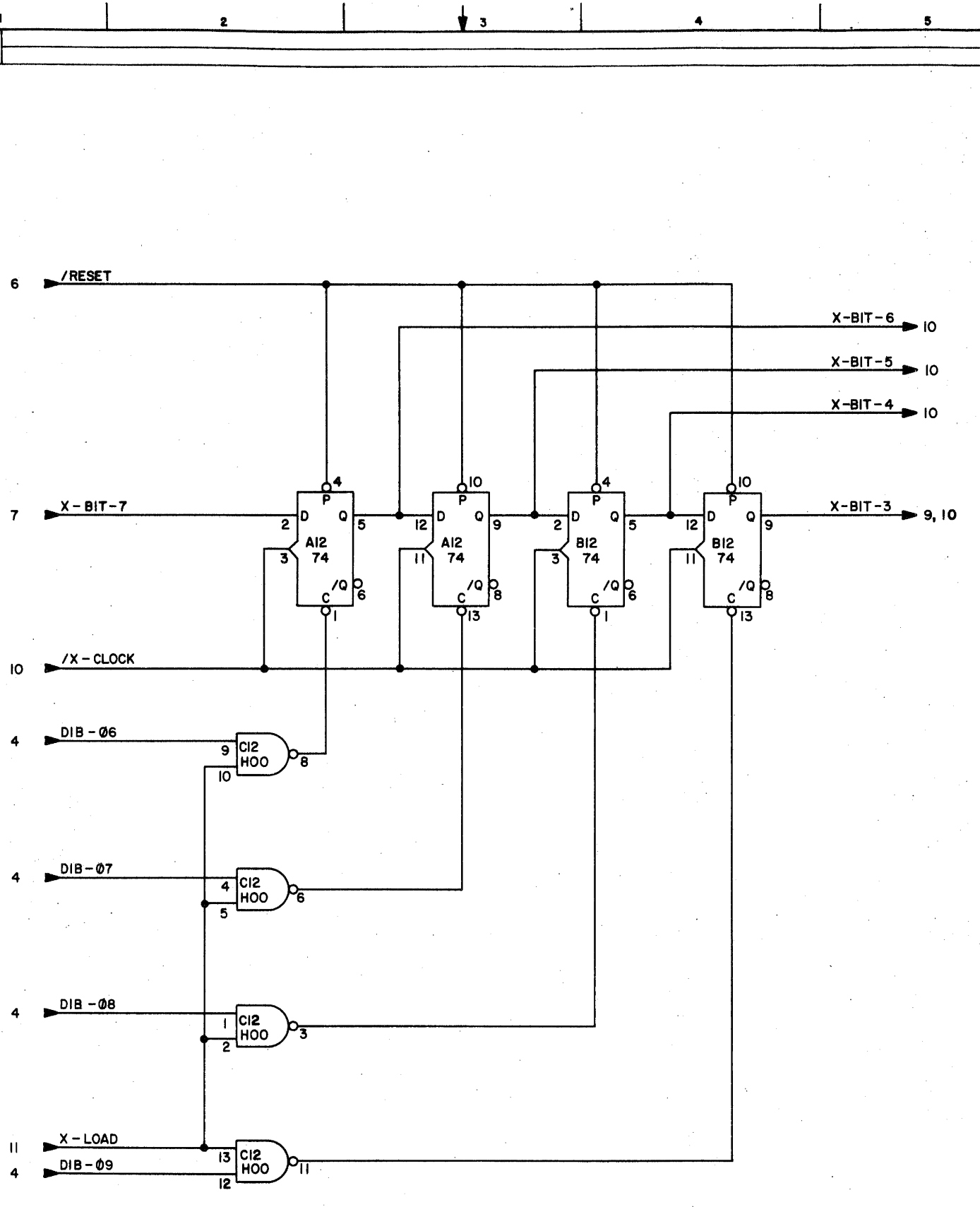
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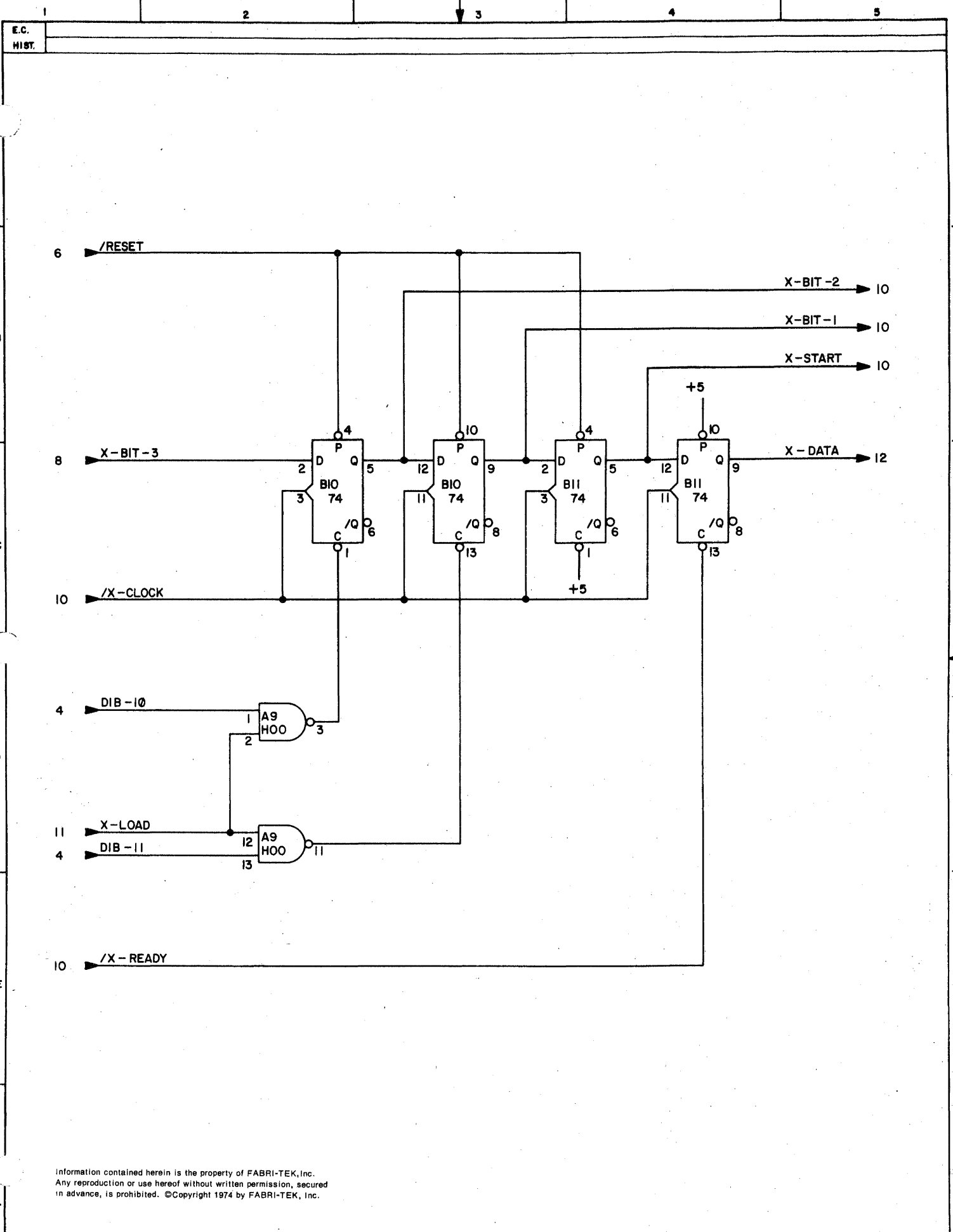
TITLE SCHEMATIC , COMMUNICATIONS INTERFACE-ASR 33

DWG. NO. C 138-0020-18

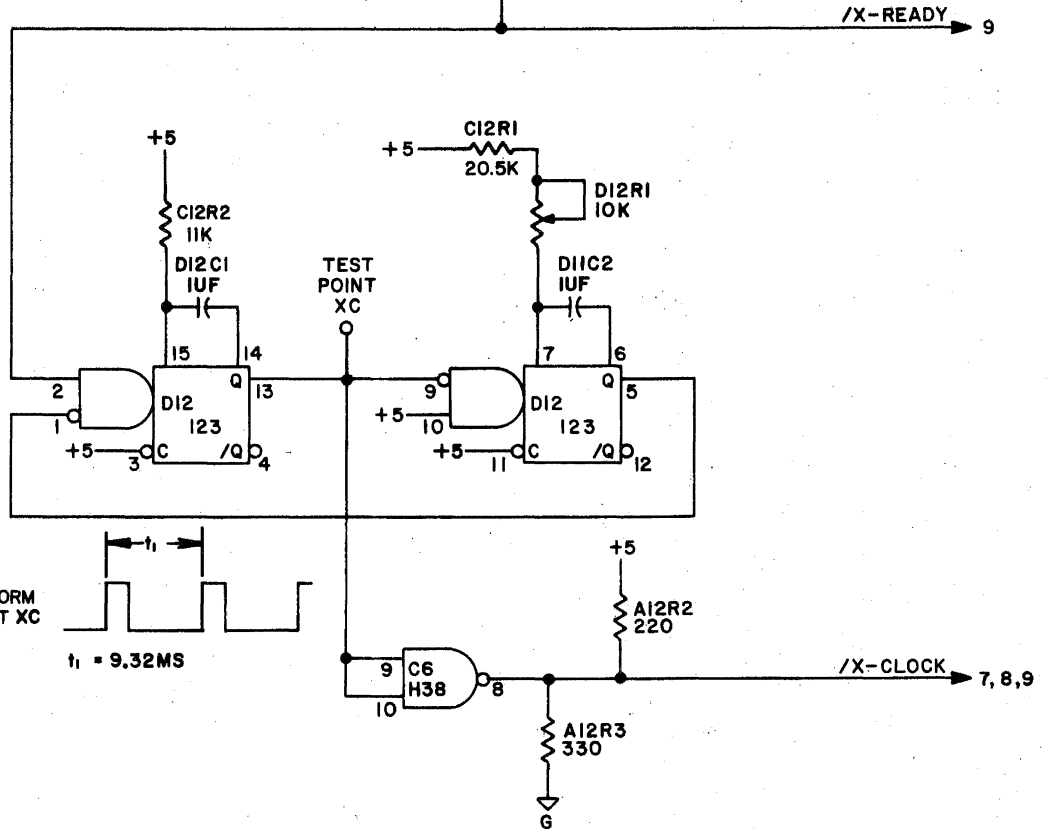
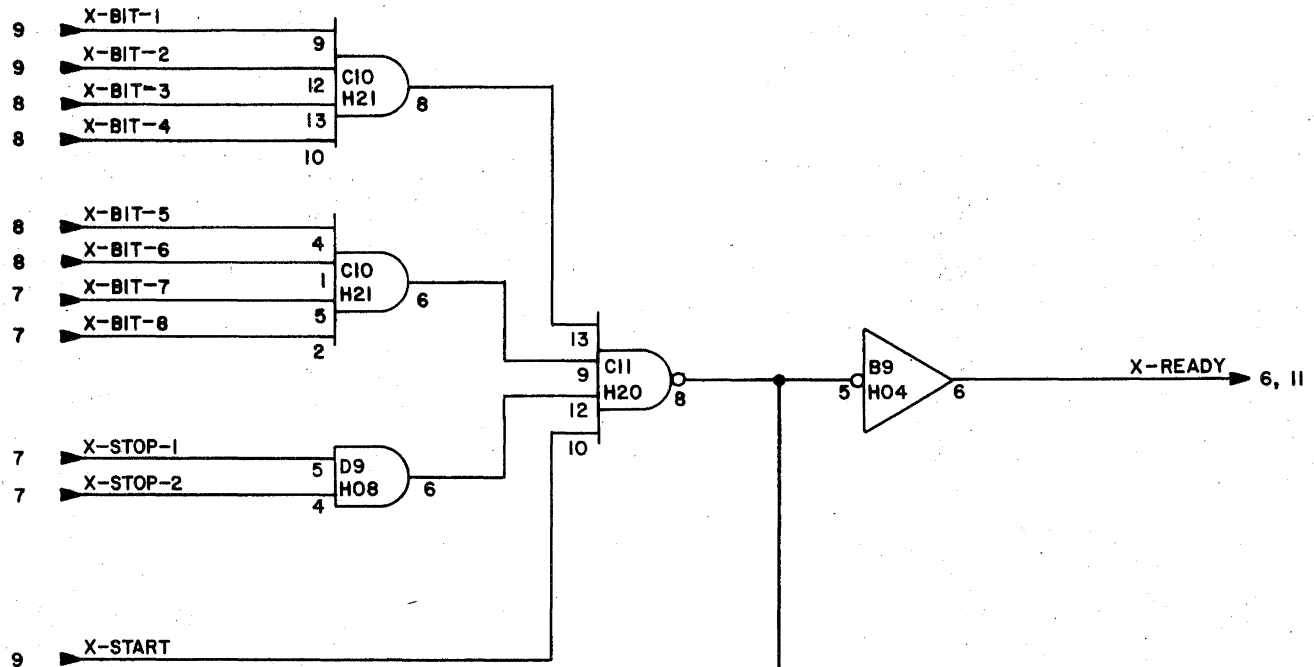
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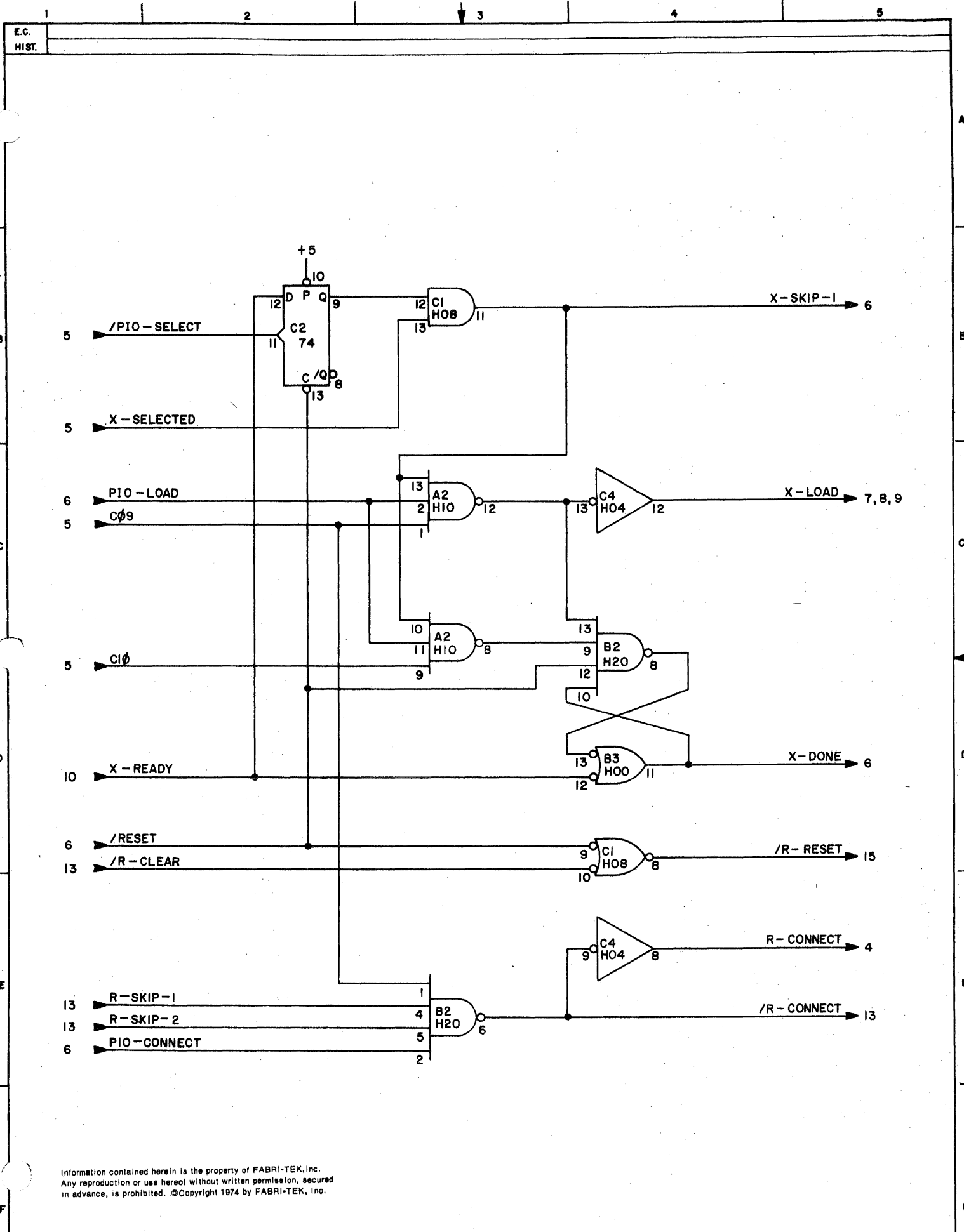
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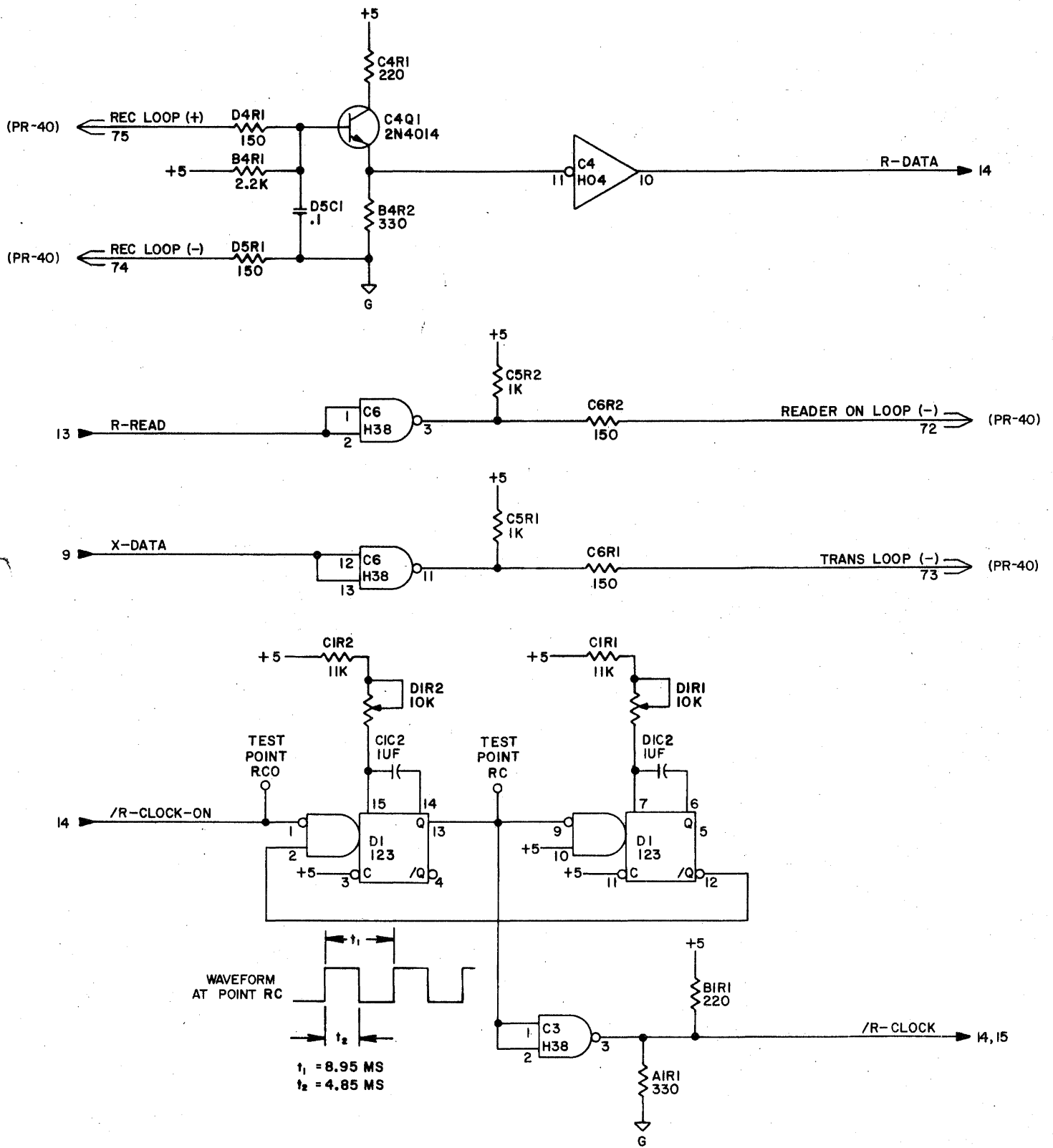
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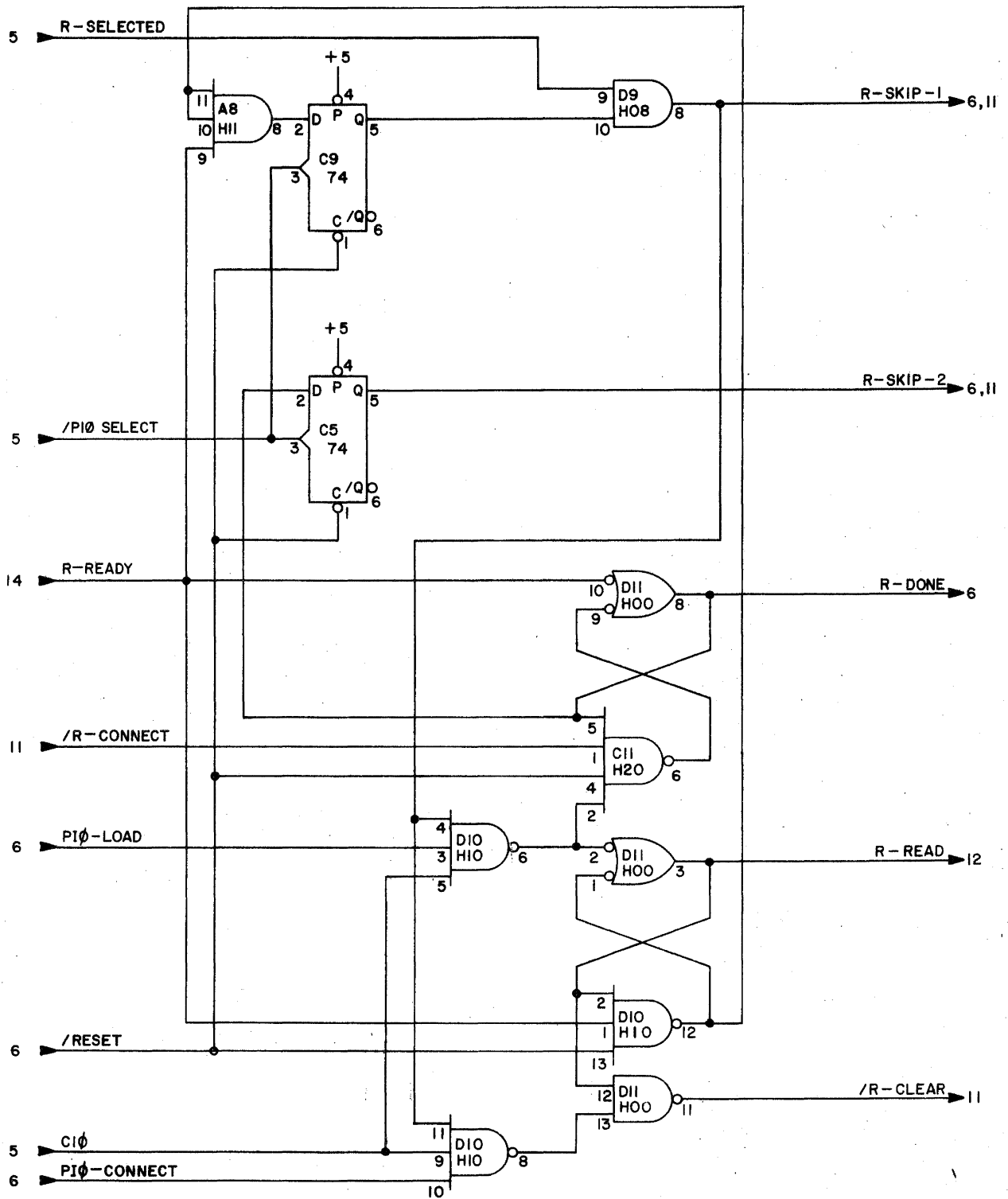
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 COMPUTER SYSTEMS

TITLE SCHEMATIC, COMMUNICATIONS INTERFACE — ASR 33

DWG. NO. C 138-0020-18 TYPE VERS. PAGE 11

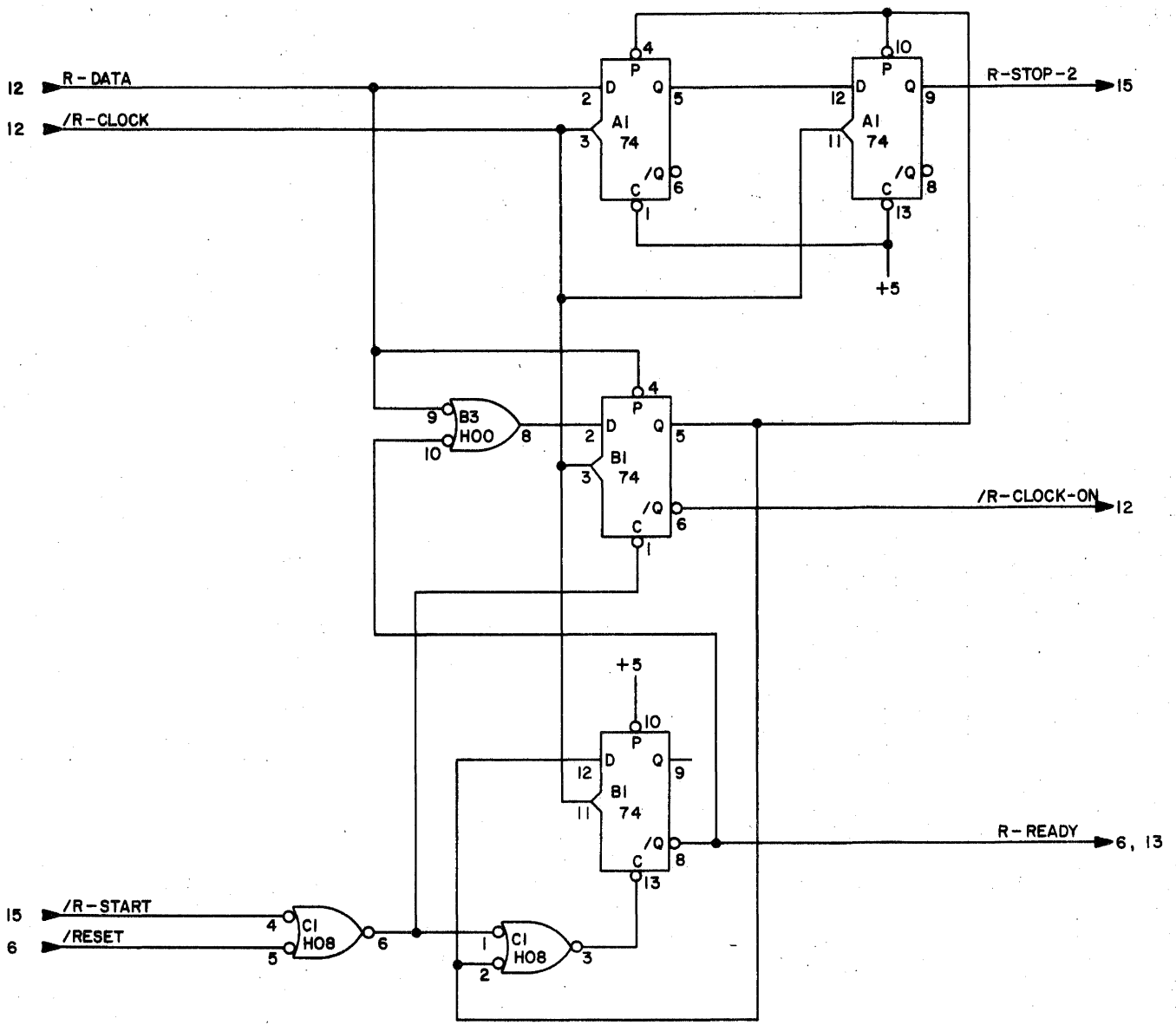


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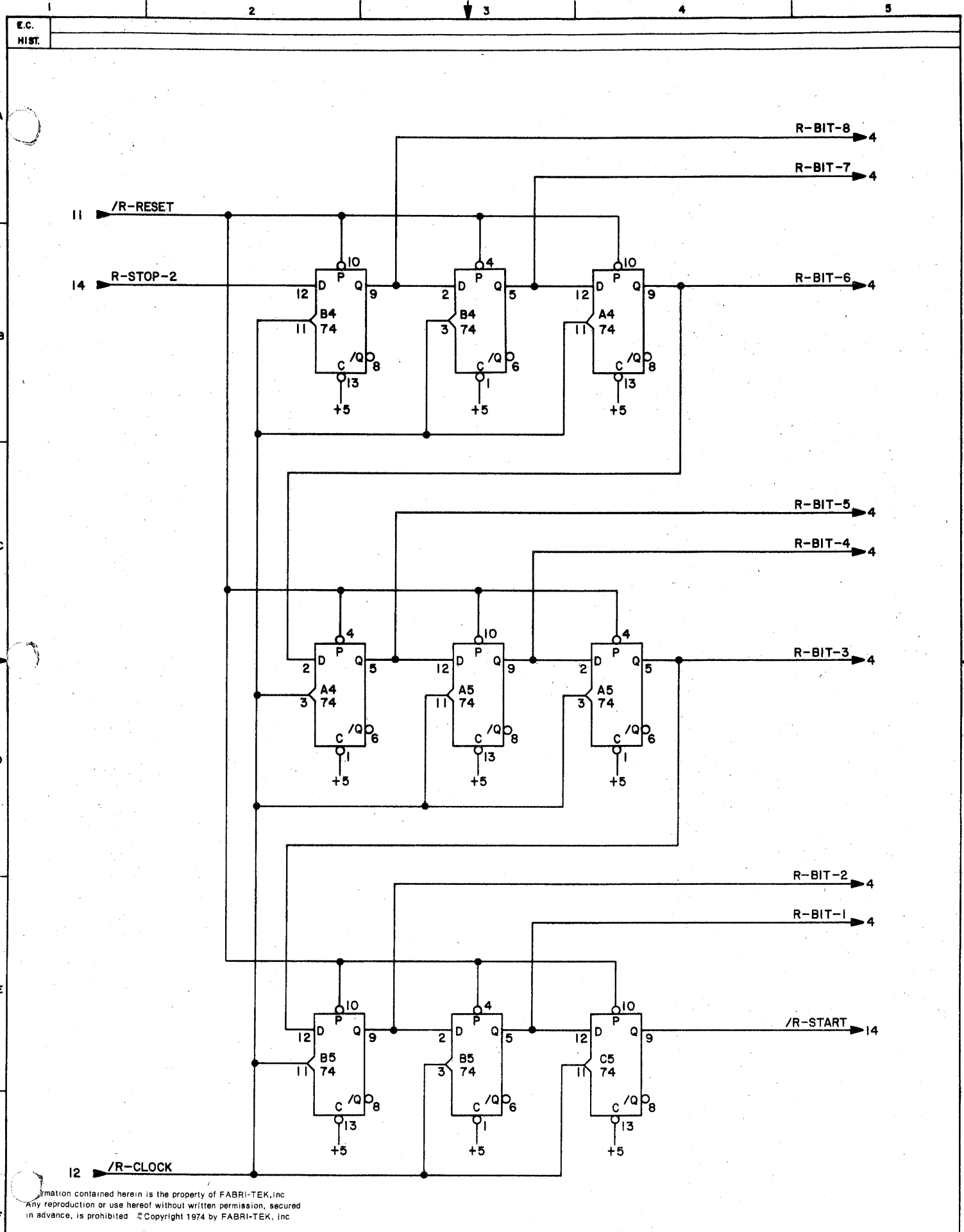


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NOTES: APPLICABLE THROUGHOUT THIS SCHEMATIC.

1. UNLESS OTHERWISE STATED:

- A. RESISTANCE VALUES ARE IN OHMS. RESISTORS ARE 5% TOLERANCE, 1/4 WATT.
- B. CAPACITANCE VALUES ARE IN MICROFARADS.

2. JEDEC OR MANUFACTURER'S PART NUMBERS ARE FOR REFERENCE ONLY. FOR EXPLICIT DESCRIPTION OF THE DEVICE CHARACTERISTICS, REFER TO THE FABRI-TEK SPECIFICATION FOR THE FABRI-TEK PART NUMBER.

3. ALL DIODES ARE FTI-022-0163-00 UNLESS OTHERWISE NOTED.

4. PIN DEFINITION:

- ↳ DENOTES INPUT CONNECTION TO ASSEMBLY.
- DENOTES OUTPUT CONNECTION FROM ASSEMBLY.
- DENOTES SCHEMATIC INTERPAGE CONNECTION.

REVISION STATUS OF SHEETS					
	1	2	3	4	5

	DATE
DRAWN C. CZAR	6-3-74
CHECKED <i>[Signature]</i>	7-4-74
APPROVED <i>[Signature]</i>	7-4-74

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TITLE SCHEMATIC, TTY MODIFICATION			
DWG. NO. C	138-0020-31	TYPE 117-0320-00	VERS
			PAGE 1 OF 5

190-1723-00
PIN NO.

DESTINATION

SCHEMATIC
MNEMONIC

FUNCTION

1	MODE SWITCH TERM L2	AAL2	115V AC
2	TERMINAL BLOCK BL(X) PIN 1	BL(X)-1	115V AC COM.
3	J3-8	RL1	READER RELAY
4	J3-7	RL2	READER RELAY
5	J2-3	48VAC	FOR CUSTOMER
6	J2-4	48V RTN	USE
7	J2-6	RTN	DISTRIBUTOR RTN
8	J2-7	RTN	SMD RTN
9	J2-8	SMD	SEL. MAG. DRIVE
10	J2-5	SEND	DISTRIBUTOR
11	C23	RDR ON +	READER
12	C24	RDR ON -	ON
13	C21	TRANS +	DATA FROM
14	C22	TRANS -	CPU
15	C19	REC +	DATA TO
16	C20	REC -	CPU
17	C25	CHGND	CHASSIS GND
18	C50	CHGND	CHASSIS GND
19	C50	CHGND	CHASSIS GND

INTERFACE MNEMONIC TABLE

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TITLE

SCHEMATIC, TTY MODIFICATION

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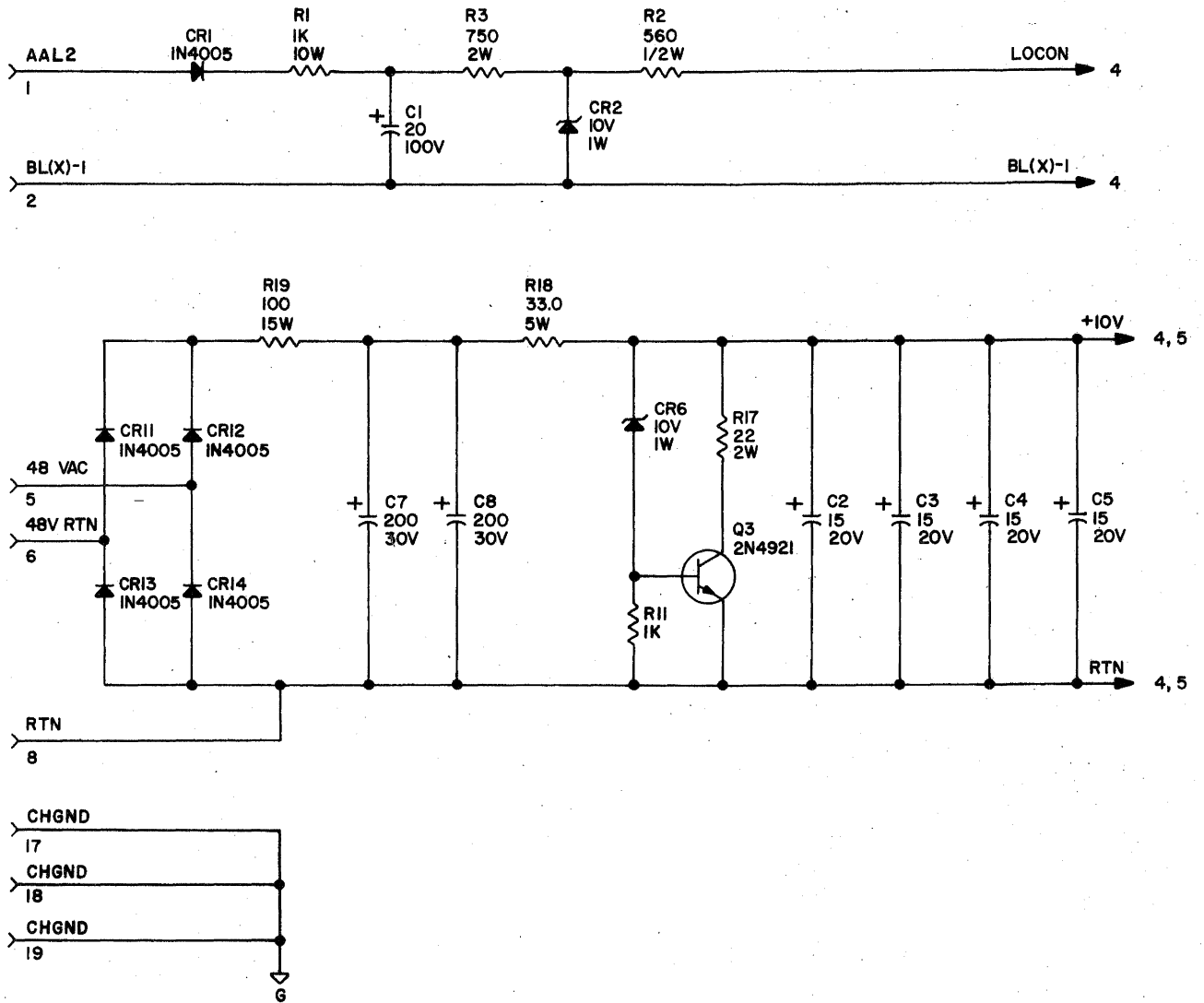
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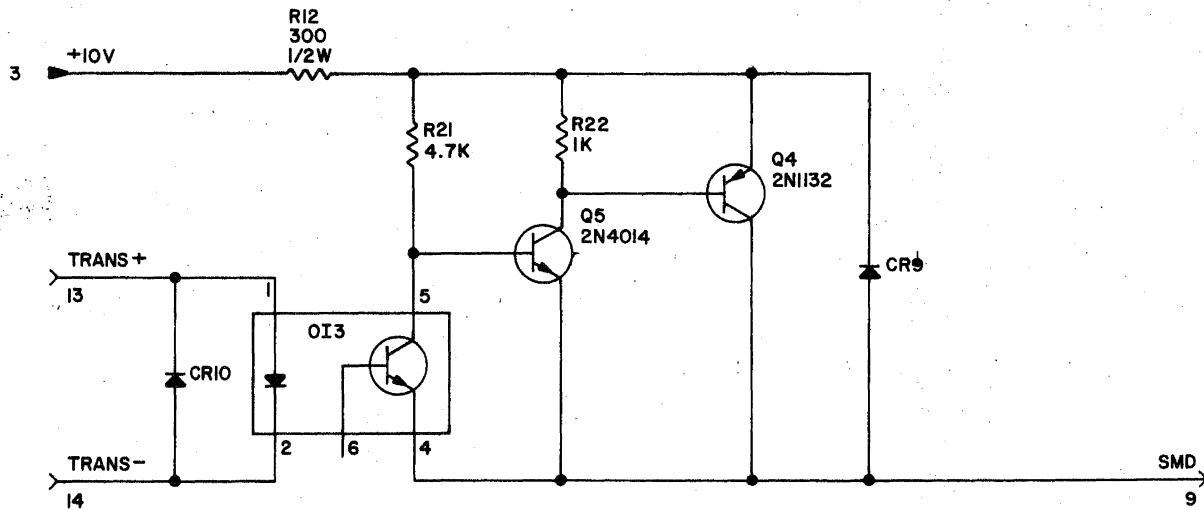
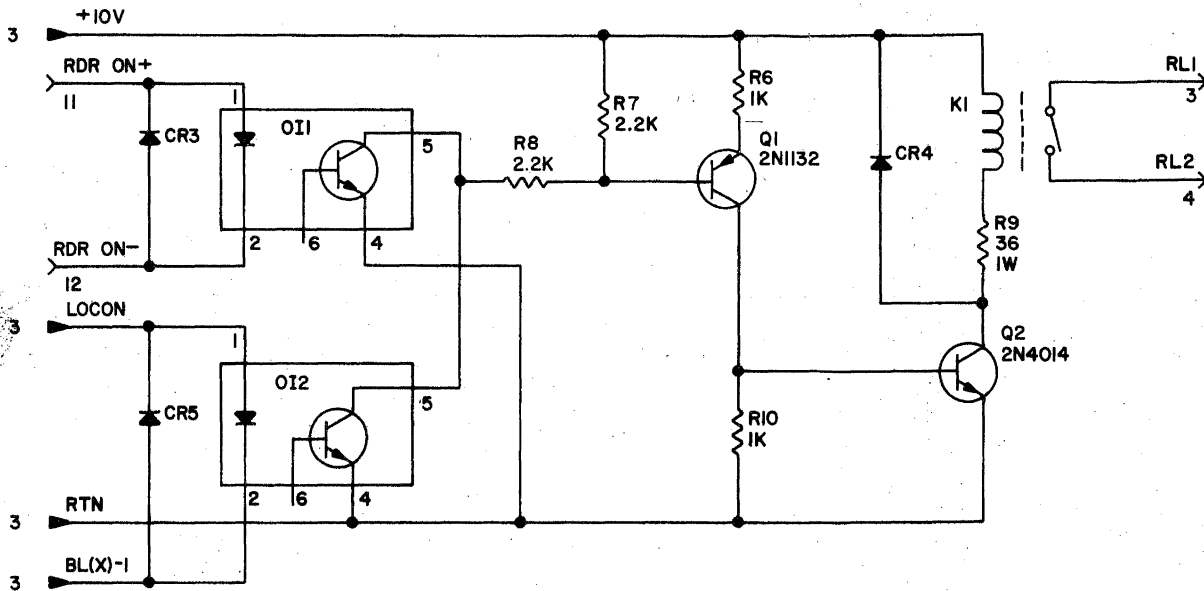
TITLE SCHEMATIC, TTY MODIFICATION

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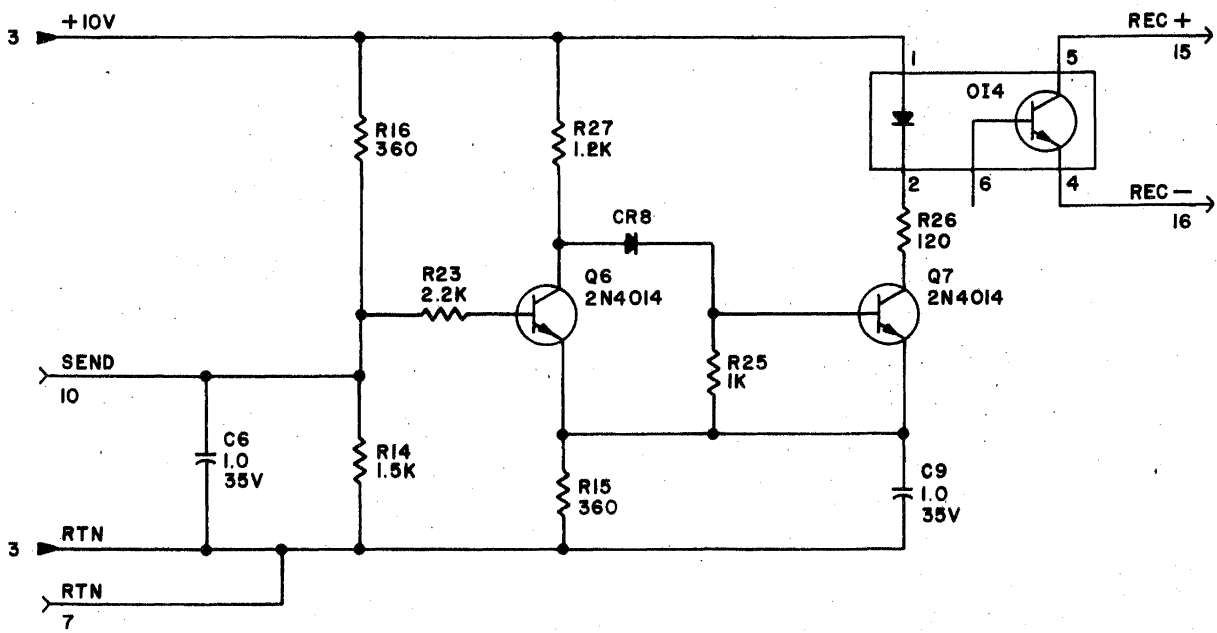
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