EMULEX MICRO DEVICES

FAST/WIDE SINGLE-CHIP SCSI CONTROLLER

FAS256

FEATURES

- ❑ Conformity with ANSI X3T9.2 SCSI-2 standard
- ❑ Sustained SCSI data transfer rates of up to
  - — 7MHz asynchronous
  - — 10MHz synchronous (8-bit)
  - — 20MHz wide synchronous (16-bit)
- ❑ 16-bit wide SCSI data handling
- ❑ 16-bit arbitration
- ❑ On-chip, single-ended SCSI transceivers (48mA drivers)
- ❑ Initiator or Target mode
- ❑ Hot pluggability
- ❑ Pipelined command structure
- ❑ 16-byte data FIFO between the DMA and SCSI channels
- ❑ SCSI P-Cable configuration
- ❑ Direct connection to differential transceivers
- ❑ Direct DIFFSENS support
- ❑ SCSI sequences implemented without microprocessor intervention
- ❑ Parity pass-through on SCSI data
- ❑ 3-byte ID message checking

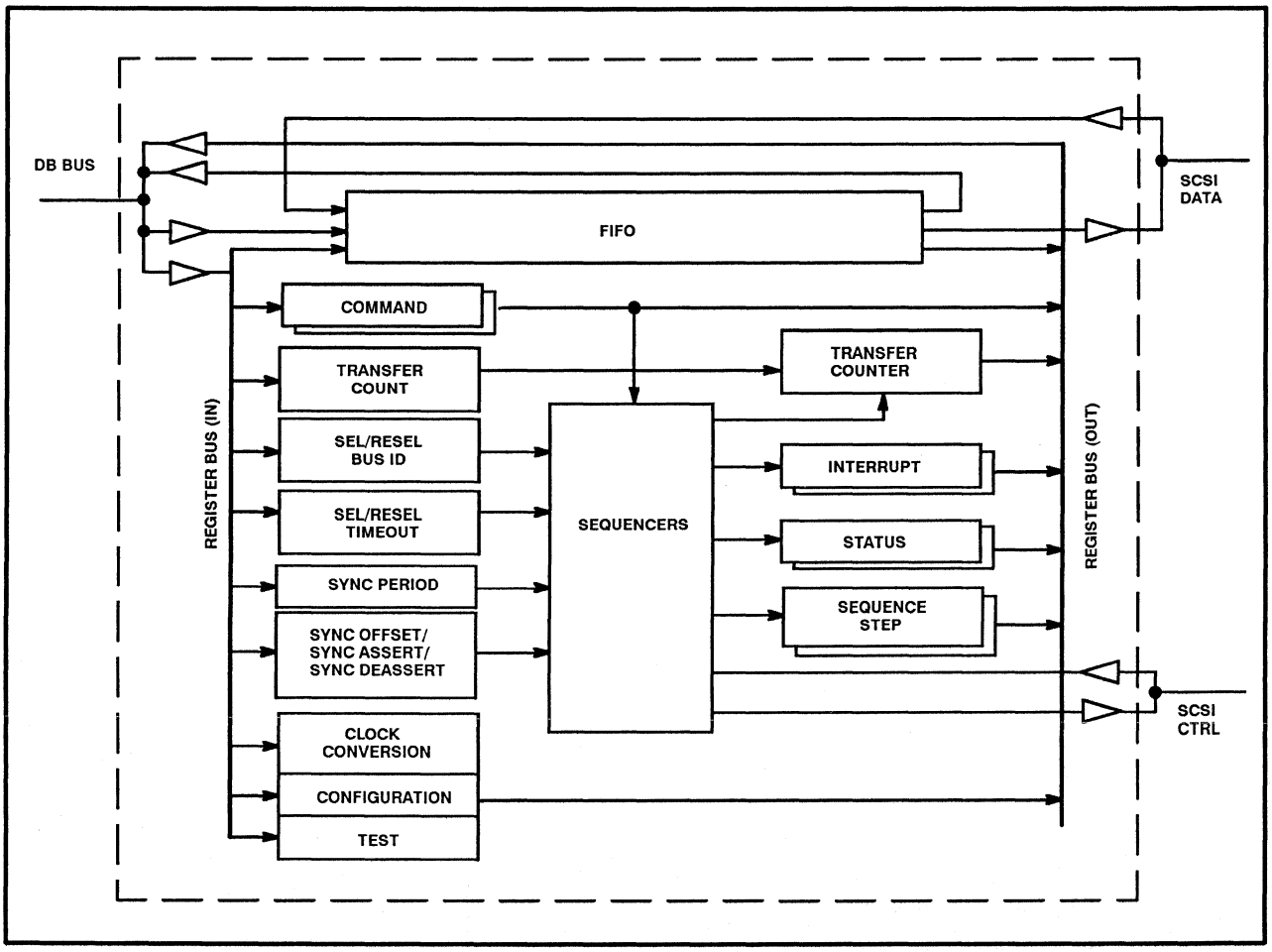


Figure 1. FAS256 Block Diagram

PRODUCT DESCRIPTION

The FAS256 is an addition to the Emulex Fast Architecture SCSI Processor (FAS) chip family with features designed to facilitate SCSI-2 support. Major new features of the FAS256 chip are 16-bit wide SCSI data handling and fast SCSI.

The FAS256 supports both single-ended and differential mode SCSI operations. The FAS256 operates in Initiator and Target roles; it can be used in both host adapter and device (peripheral) applications. The chip performs such functions as bus arbitration, selection of a Target, or reselection of an Initiator. It handles message, command, status, and data transfer between the SCSI Bus and its internal FIFO and an external buffer memory. These are largely internal processes that the FAS256 automates without microprocessor intervention.

The FAS256 can replace all existing SCSI interface circuitry which typically consists of discrete devices, external drivers, and a low-performance SCSI interface chip. It contains an accelerated DMA interface, a 16-byte FIFO, and accelerated asynchronous and synchronous data interfaces to the SCSI Bus. It has special high-current SCSI Bus drivers with controlled electrical and impedance characteristics.

The chip maximizes protocol efficiency by utilizing a first-in, first-out command pipeline structure and combination commands to minimize host intervention. The FAS256 offers typical maximum transfer capability through sustained asynchronous data rates up to 7MHz and synchronous data rates up to 20MHz in fast SCSI mode.

The FAS256 has been optimized for interaction with a DMA controller and the controlling processor. Common SCSI Bus sequences that typically require significant amounts of processing time and microprocessor interaction have been reduced to single commands. These commands are listed in Table 1.

SYSTEM APPLICATIONS

The FAS256 is a versatile yet powerful SCSI controller. The application diagrams in figures 2 and 3 show typical chip design usage for both Initiator and Target modes. The FAS256 accommodates single bus system architecture. If simultaneous execution of instructions and DMA data transfer is required, an external means of bus isolation is necessary.

Table 1. Single SCSI Commands

Command	Description
Selection	Arbitration, target selection, transmission of an optional 1- or 3-byte message followed by a multiple-byte command.
Reselection	Arbitration, Initiator reselection, and transmission of a 1- or 3-byte message.
Bus-Initiated Selection	Transmission of the selection bus ID, a 1-byte Identify or null message, a 2-byte Queue Tag message (if SCSI-2 mode enabled), and a multiple-byte command.
Bus-Initiated Reselection	Transmission of the reselection bus ID followed by a 1-byte Identify message.
Target Command Complete	Transmission of a status byte and a 1-byte message.
Target Disconnect Sequence	Transmission of two 1-byte messages followed by disconnection from the SCSI Bus.
Initiator Command Complete	Transmission of a status byte and a 1-byte message.
Reselect3 Sequence	Transmission of a 1-byte Identify message and a 2-byte Queue Tag message.

INTERFACES

The FAS256 provides a 16-bit SCSI interface along with support signals for differential SCSI. The microprocessor interface consists of a chip select signal, four address lines, and a read and write strobe. The active low chip select signal (CSN) indicates that a FAS256 register is being accessed. The four address lines (A3-0) select internal registers to be accessed. Data written to or read from the FAS256 internal registers is transferred on DB07-00. The memory controller resolves bus contention between register data transfers and DMA data transfers. The DMA request and acknowledge control signals (DREQ and DACKN) provide timing for DMA transfers. DMA memory data transfers are 16 bits wide with optional byte parity. The read and write strobes (RDN and WRN) indicate the direction of data flow for register or DMA transfers. All interfaces are shown in Figure 4.

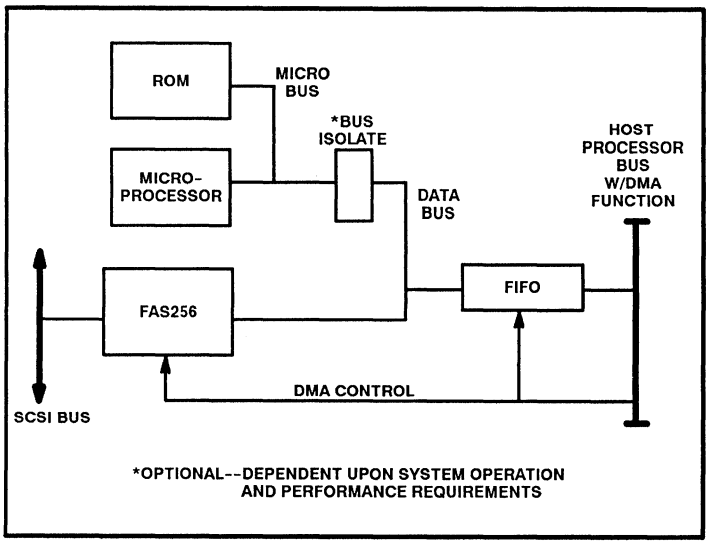


Figure 2. SCSI Host Adapter Application

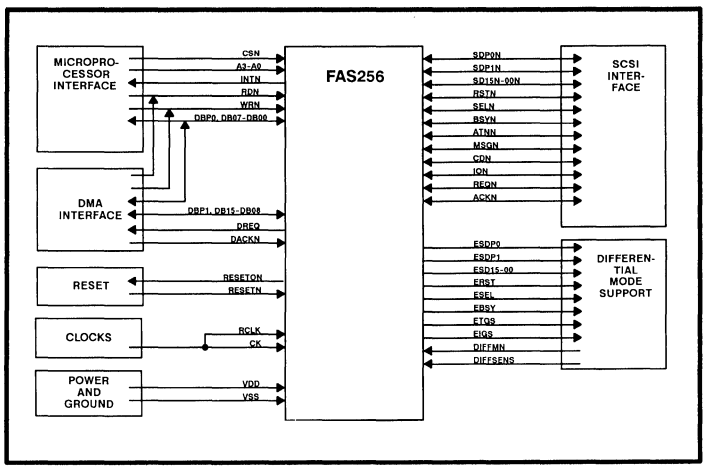


Figure 4. FAS256 Functional Signal Grouping

PACKAGING

The FAS256 is available in a 160–pin plastic quad flat pack (PQFP). The pin diagram for this package is illustrated in Figure 5.

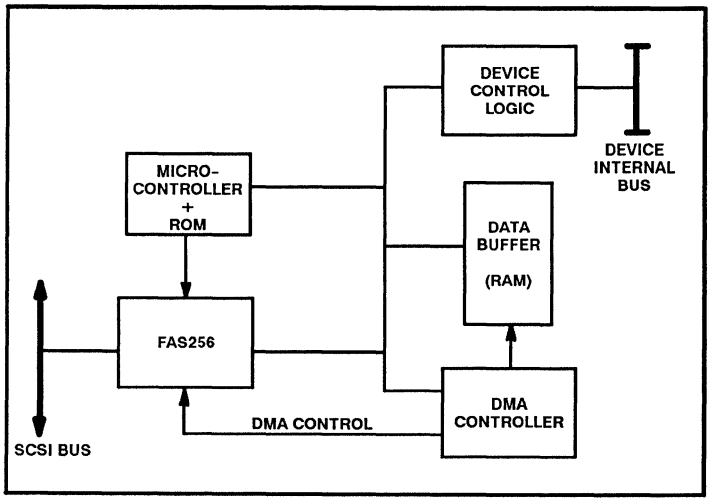


Figure 3. SCSI Target Device Embedded Controller Application

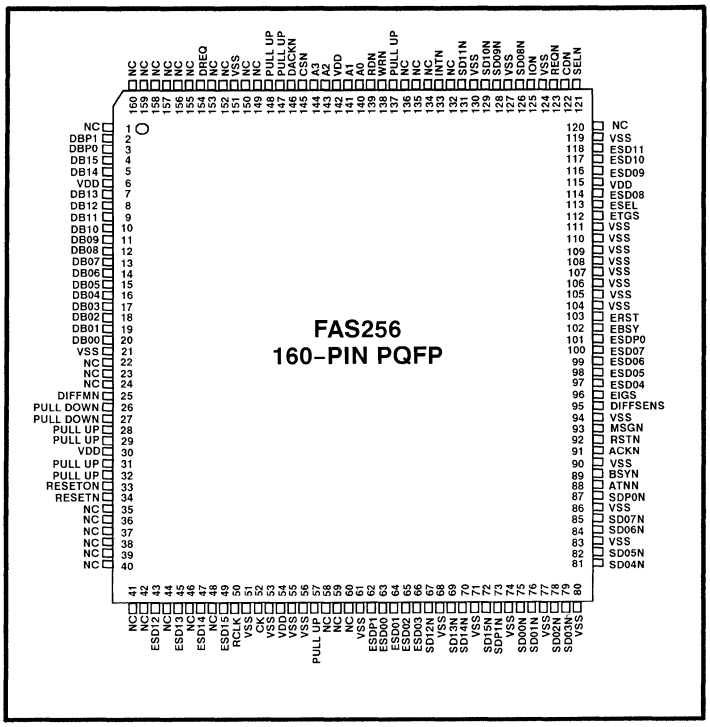


Figure 5. FAS256 Pin Diagram

REGISTERS

The FAS256 registers are used by the microprocessor to configure, command, and monitor the SCSI Bus, and to pass data through the chip to the SCSI Bus. The FAS256 registers are summarized in Figure 6.

TRANSFER COUNTER LOW (00 R)
TRANSFER COUNTER HIGH (01 R)

TRANSFER COUNT LOW (00 W)
TRANSFER COUNT HIGH (01 W)

7	6	5	4	3	2	1	0

RESET: x

THE TRANSFER COUNTER REGISTER COUNTS THE NUMBER OF BYTES TRANSFERRED IN A DMA COMMAND OR RECEIVED IN A COMMAND SEQUENCE IN TARGET MODE. THE TRANSFER COUNT NEED ONLY BE LOADED ONCE FOR SUCCESSIVE DMA COMMANDS USING THE SAME COUNT. ZERO SPECIFIES THE MAXIMUM COUNT.

FIFO (02 R/W)

7	6	5	4	3	2	1	0

RESET: 0

15	14	13	12	11	10	9	8

0

THE FIFO IS A 16-BYTE, WORD DEEP BUFFER BETWEEN THE SCSI BUS AND THE BUFFER MEMORY. THE FIFO IS FLUSHED DURING A HARD RESET.

COMMAND (03 R/W)

7	6	5	4	3	2	1	0

RESET

COMMAND	x
INITIATOR MODE	x
TARGET MODE	x
DISCONNECTED MODE	x
ENABLE DMA	x

STATUS #1 (04 R)

7	6	5	4	3	2	1	0

RESET

SCSI BUS PHASE	x
PHASE TRANSFER COMPLETE	0
TRANSFER COUNTER ZERO	0
PARITY ERROR	0
GROSS ERROR	0
INTERRUPT PENDING	0

SELECT/RESELECT BUS ID (04 W)

7	6	5	4	3	2	1	0

RESET

BUS ID	x
RESERVED	0

INTERRUPT (05 R)

7	6	5	4	3	2	1	0

RESET

SELECTED	0
SELECTED WITH ATN	0
RESELECTED	0
FUNCTION COMPLETE	0
BUS SERVICE	0
DISCONNECT	0
ILLEGAL COMMAND	0
SCSI RESET DETECTED	0

SELECT/RESELECT TIMEOUT (05 W)

7	6	5	4	3	2	1	0

RESET

TIMOUT VALUE	0

SEQUENCE STEP (06 R)

7	6	5	4	3	2	1	0

RESET

SEQUENCE STEP	0
RESERVED	0

SYNCHRONOUS TRANSFER PERIOD (06 W)

7	6	5	4	3	2	1	0

RESET

SYNCHRONOUS TRANSFER PERIOD	1
SYNCHRONOUS TRANSFER PERIOD	0
SYNCHRONOUS TRANSFER PERIOD	1
SYNCHRONOUS TRANSFER PERIOD	0
RESERVED	0

FIFO FLAGS (07 R)

7	6	5	4	3	2	1	0

RESET

FIFO COUNT	0
SEQUENCE STEP BIT 0	0
SEQUENCE STEP BIT 1	0
SEQUENCE STEP BIT 2	0

SYNCHRONOUS OFFSET (07 W)

7	6	5	4	3	2	1	0

RESET

SYNCHRONOUS OFFSET	0
REQ/ACK ASSERT	0
REQ/ACK DEASSERT	0

CONFIGURATION #1 (08 R/W)

7	6	5	4	3	2	1	0

RESET

BUS ID	0
CHIP TEST MODE	0
SCSI PARITY ENABLE	0
PARITY TEST MODE	0
SCSI RESET INTERRUPT DISABLE	0
SLOW CABLE MODE	0

CLOCK CONVERSION FACTOR (09 W)

7	6	5	4	3	2	1	0

RESET

CLOCK CONVERSION FACTOR	0
CLOCK CONVERSION FACTOR	1
CLOCK CONVERSION FACTOR	0
RESERVED	0

STATUS #2 (09 R)

7	6	5	4	3	2	1	0

RESET

RESERVED	0
SCSI WIDE TRANSFER	0
INPUT SHUTTLE	0
OUTPUT SHUTTLE	0
FIFO EMPTY	1

TEST (0A W)

7	6	5	4	3	2	1	0

RESET

TARGET TEST MODE	0
INITIATOR TEST MODE	0
TRISTATE TEST MODE	0
FAS256 ENABLE	0
RESERVED	0

CONFIGURATION #2 (0B R/W)

7	6	5	4	3	2	1	0

RESET

DMA PARITY ENABLE	0
REGISTER PARITY ENABLE	0
TARGET BAD PARITY ABORT	0
SCSI-2 MODE	0
FEATURES ENABLE	0
RESERVED	0

CONFIGURATION #3 (0C R/W)

7	6	5	4	3	2	1	0

RESET

FASTCLK	0
FASTSCSI	0
CDB10	0
QUENB	0
IDRESCHK	0
IDBIT3	0
WIDESCSI	0
RESERVED	0

RECOMMAND COUNTER LOW (0E R/W)

7	6	5	4	3	2	1	0

RESET

RCMD CNT LOW	BEh

RECOMMAND COUNTER HIGH (0F R/W)

7	6	5	4	3	2	1	0

RESET

RCMD CNT HIGH	0

Figure 6. FAS256 Register Set

ELECTRICAL CHARACTERISTICS

Table 2. Absolute Maximum Stress Ratings

Symbol	Description	Min	Max	Unit
T_{STG}	Storage Temperature	-55	150	°C
V_{DD}	Supply Voltage	-0.5	7	V
V_{IN}	Input Voltage	V_{SS} - 0.5	V_{DD} + 0.5	V
I_{LP}[1]	Latch-Up Current	-100	100	mA
ESD[2]	Electrostatic Discharge (All except SCSI pins)	TBD	TBD	V
ESD[2]	Electrostatic Discharge (SCSI pins)	TBD	TBD	V

[1]Test conditions of $-2V < V_{PIN} < +8V$

[2]ESD values will be provided by Emulex Engineering when characterization of the chip is completed.

Table 3. Operating Conditions

Symbol	Description	Minimum	Maximum	Unit
V_{DD}	Supply Voltage	4.5	5.5	V
I_{DD}[1]	Supply Current (Static I_{DD})		1	mA
I_{DD}[2]	Supply Current (Dynamic I_{DD})		TBD	mA
T_A	Ambient Temperature	0	70	°C

[1]Static I_{DD} refers to all inputs at V_{DD}, all outputs open circuit, and all bidirectional pins configured as inputs.

[2]Dynamic I_{DD} is dependent on the application.

DC CHARACTERISTICS

Table 4. Single-Ended Mode SCSI Signals

Symbol	Description	Minimum	Maximum	Unit	Test Condition
SD15N—SD00N, SDP1N, SDP0N, ACKN, ATTN, MSGN, CDN, ION, BSYN, REQN, RSTN, SELN					
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	
I_{IH}	Input High Leakage Current	-10	10	µA	$0 < V_{DD} < 5.5$ $V_{IN} = 3.1$
I_{IL}	Input Low Leakage Current	-10	10	µA	$V_{IN} = 0$
V_{OL}	Output Low Voltage		0.5	V	$I_{OL} = 48mA$
I_{OZ}	Tristate Leakage Current	-10	10	µA	$0 < V_{OUT} < V_{DD}$
S_{FT}	Signal Fall Time	6		ns	SCSI Termination
H_{ST}	Hysteresis	200		mV	

NOTE: Pins ATNN, MSGN, CDN, ION, BSYN, RSTN, and SELN have the same DC characteristics in both single-ended and differential modes.

Table 5. Differential Mode SCSI Signals

Symbol	Description	Minimum	Maximum	Unit	Test Condition
SD15N–SD00N, SDP1N, SDP0N, ACKN, REQN					
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	
I_{IN}	Input Current	-10	10	µA	$0 < V_{IN} < V_{DD}$
V_{OH}	Output High Voltage	2.4			I_{OH} = -2mA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4mA

Table 6. Schmitt Input SCSI Signals

Symbol	Description	Minimum	Maximum	Unit	Test Condition
DIFFSENS					
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	
I_{IN}	Input Current	-10	10	µA	$0 < V_{IN} < V_{DD}$
H_{ST}	Hysteresis	200		mV	

Table 7. TTL Schmitt Inputs

Symbol	Description	Minimum	Maximum	Unit	Test Condition
CSN, WRN, RDN, RESETN, A3–A0					
V_{IH}	Input High Voltage	2.2	V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	
I_{IN}	Input Current	-10	10	µA	$0 < V_{IN} < V_{DD}$
H_{ST}	Hysteresis	300		mV	

Table 8. CMOS Inputs

Symbol	Description	Minimum	Maximum	Unit	Test Condition
CK, RCLK					
V_{IH}	Input High Voltage	3.85	V_{DD} + 0.5	V	V_{DD} = 5.5
V_{IH}	Input High Voltage	3.15	V_{DD} + 0.5	V	V_{DD} = 4.5
V_{IL}	Input Low Voltage	V_{SS} - 0.5	1.65	V	
I_{IN}	Input Current	-10	10	µA	$0 < V_{IN} < V_{DD}$

Table 9. 4mA Tristatable Outputs

Symbol	Description	Minimum	Maximum	Unit	Test Condition
ETGS, RESETON					
V_{OH}	Output High Voltage	2.4			I_{OH} = -2mA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4mA
I_{OZ}	Tristate Leakage Current	-10	10	µA	$0 < V_{IN} < V_{DD}$

Table 10. 2mA Tristatable Outputs

Symbol	Description	Minimum	Maximum	Unit	Test Condition
INTN, ESDP1, ESDP0, ESD15—ESD00, EIGS, ERST, EBSY, ESEL					
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -1mA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2mA
I_{OZ}	Tristate Leakage Current	-10	10	µA	$V_{SS} \leq V_{OUT} \leq V_{DD}$

Table 11. Bidirectional Signals with TTL Inputs

Symbol	Description	Minimum	Maximum	Unit	Test Condition
DBP1, DBP0, DB15—DB00					
V_{IH}	Input High Voltage	2	V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	V_{SS} - 0.5	0.8	V	
V_{OH}	Output High Voltage	2.4			I_{OH} = -2mA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4mA
I_{LL}	Input Low Leakage Current	-660	-200	µA	V_{IN} = 0
I_{IH}	Input High Leakage Current	-10	10	µA	V_{IN} = 5.5

AC TIMING

The following figures and table values are illustrative of the FAS256 chip timing characteristics. For more information, refer to the Emulex *FAS256 SCSI Processor Technical Manual*, VLSI51013-00 Rev A.

SYSTEM INTERFACE TIMING

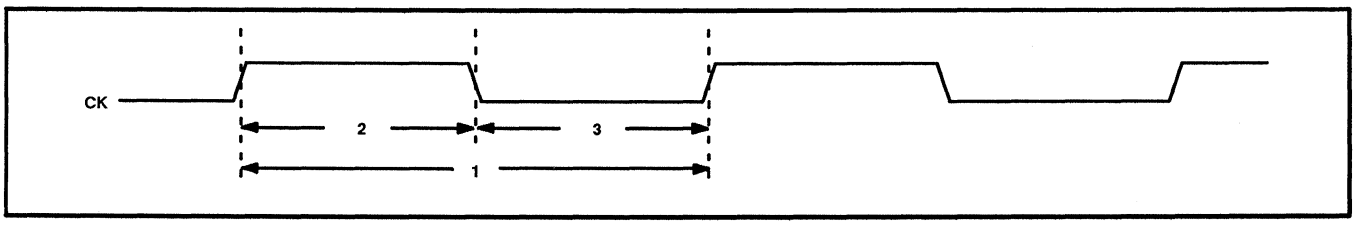
CK input, reset input/output, and interrupt output timing is listed below and illustrated in Figure 7.

CK INPUT[1]						
#	Symbol	Description	Min	Max	Unit	Note
1	T_{CP}	Clock Period (1 ÷ Freq)			ns	
	T_{CS}	Synchronization Latency	T_{CL}	T_{CL} + T_{CP}	ns	
With FASTCLK Bit Reset						
	F_{CPA}	Clock Frequency, Async	12	25	MHz	
	F_{CPS}	Clock Frequency, Sync	20	25	MHz	
2	T_{CH}	Clock High	14.58	0.65 • T_{CP}	ns	2
3	T_{CL}	Clock Low	14.58	0.65 • T_{CP}	ns	2
With FASTCLK Bit Set						
	F_{CPA}	Clock Frequency, Async	20	40	MHz	
	F_{CPS}	Clock Frequency, Sync	38	40	MHz	
2	T_{CH}	Clock High	0.40 • T_{CP}	0.60 • T_{CP}	ns	
3	T_{CL}	Clock Low	0.40 • T_{CP}	0.60 • T_{CP}	ns	

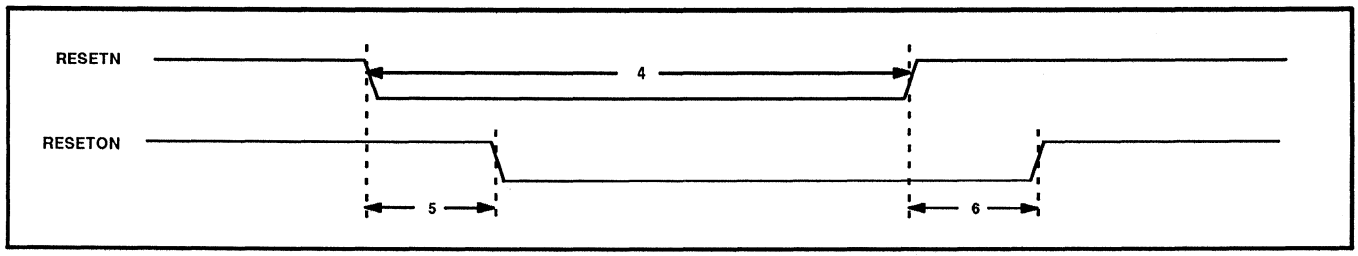
#	Symbol	Description	Min	Max	Unit	Note
		RESET INPUT				
4	T_{RST}	RESETN Pulse Width	200		ns	
		RESET OUTPUT				
5	T_{RH}	RESETN High to RESETON High		50	ns	
6	T_{RL}	RESETN Low to RESETON Low		50	ns	
		INTERRUPT OUTPUT				
7	T_{RI}	RDN Low to INTN High		75	ns	
8	T_{ICY}	RDN High to INTN Low	T_{CS}		ns	

NOTES

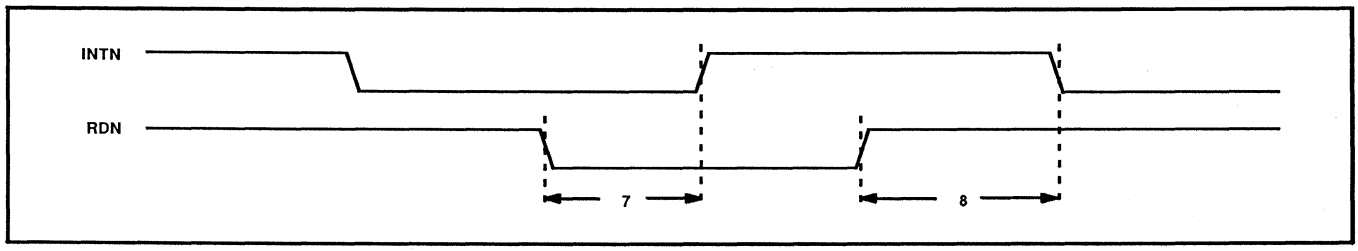
1. CK and RCLK must be tied together.
2. For synchronous SCSI transfers and FASTCLK disabled, the clock must also meet the following requirements: $(2 \bullet T_{CP} + T_{CL} \geq 97.92$ ns) and $(2 \bullet T_{CP} + T_{CH} \geq 97.92$ ns).



CK INPUT



RESET INPUT/OUTPUT



INTERRUPT OUTPUT

Figure 7. CK Input, Reset Input/Output and Interrupt Output

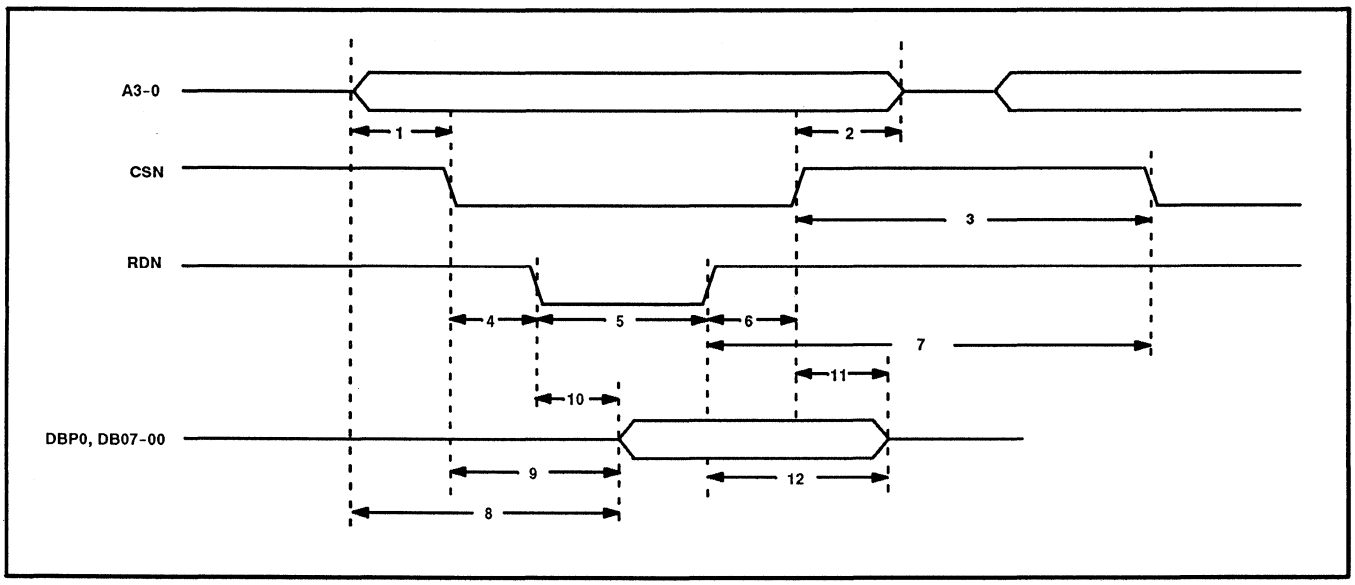
REGISTER INTERFACE TIMING

Register interface timing is listed below and illustrated in Figure 8.

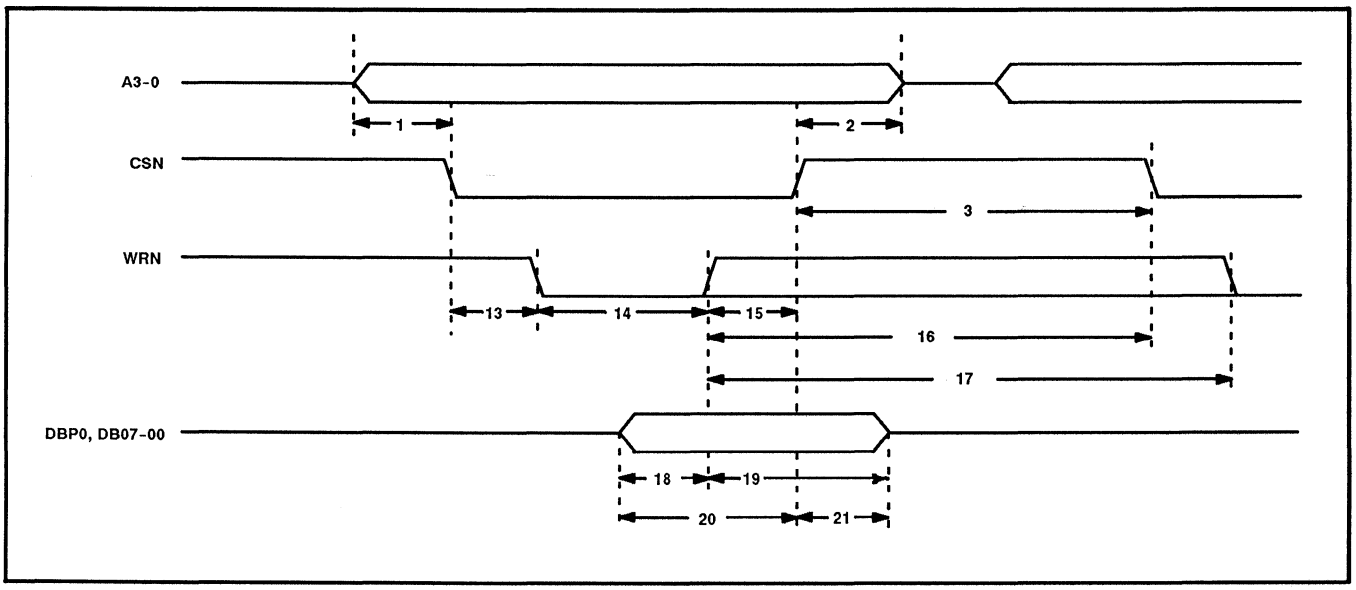
#	Symbol	Description	Min	Max	Unit	Note
1	T_{RASC}	Address Setup to CSN Low	0		ns	
2	T_{RAHC}	Address Hold from CSN High	40		ns	
3	T_{RCCY}	CSN High to CSN Low	40		ns	
		READ CYCLE				
4	T_{RSCR}	CSN Low to RDN Low	0		ns	
5	T_{RRD}	RDN Pulse Width	T_{RDR}		ns	
6	T_{RCHR1}	RDN High to CSN High	0		ns	
7	T_{RCHR2}	RDN High to CSN Low	40		ns	
8	T_{RDA}	Address Setup to Data		48	ns	1
9	T_{RDC}	CSN Low to Data		40	ns	1
10	T_{RDR}	RDN Low to Data		40	ns	1
11	T_{RDHC}	CSN High to Data Release	2	30	ns	2
12	T_{RDHR}	RDN High to Data Release	2	30	ns	2
		WRITE CYCLE				
13	T_{RCSW}	CSN Low to WRN Low	0		ns	3
14	T_{RWR}	WRN Pulse Width	50		ns	
15	T_{RCHW}	WRN High to CSN High	0		ns	3
16	T_{RWH}	WRN High to CSN Low	50		ns	
17	T_{RWCY}	WRN High to WRN Low	50		ns	
18	T_{RDW}	Data Setup to WRN High	0		ns	4
19	T_{RDHW}	Data Hold from WRN High	35		ns	5
20	T_{RDWC}	Data Setup to CSN High	0		ns	4
21	T_{RDHWC}	Data Hold from CSN High	35		ns	5

NOTES

1. T_{RDA}, T_{RDC}, and T_{RDR} specifications must be met.
2. RDN edges may precede or follow CSN edges.
3. WRN edges may precede or follow CSN edges.
4. Either T_{RDW} or T_{RDWC} specification must be met.
5. Either T_{RDHW} or T_{RDHWC} specification must be met.



REGISTER READ



REGISTER WRITE

Figure 8. Register Interface Timing

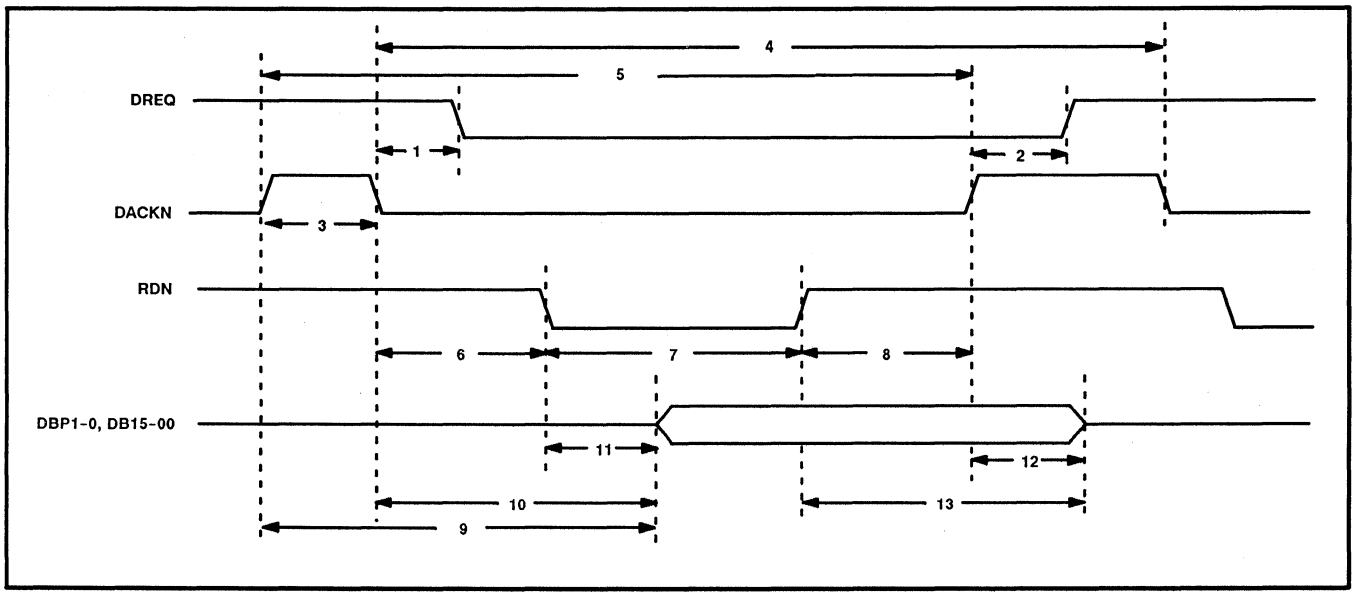
DMA INTERFACE TIMING

DMA interface timing is listed below and illustrated in Figure 9.

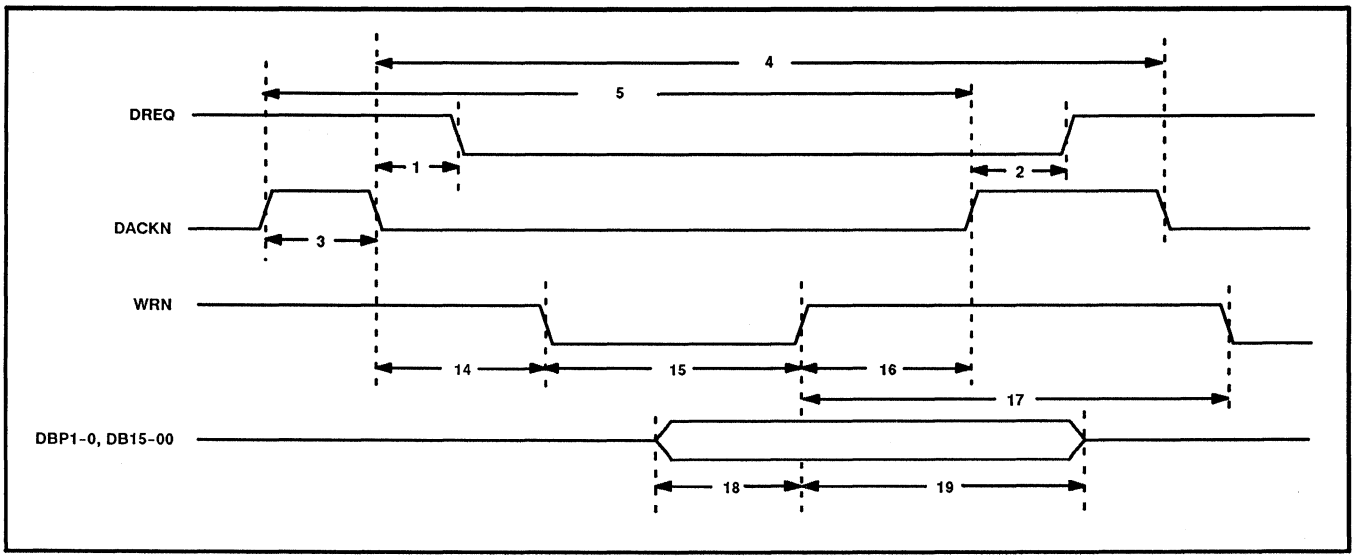
#	Symbol	Description	Min	Max	Unit	Note
1	T_{DARL}	DACKN Low to DREQ Low		40	ns	1
2	T_{DRH}	DACKN High to DREQ High		40	ns	2
3	T_{DACY}	DACKN High to DACKN Low	17		ns	3
4	T_{ACP0}	DACKN Low to DACKN Low	75		ns	
5	T_{ACP1}	DACKN High to DACKN High	$T_{CS}+30$ $-T_{DACY}$ and $2T_{CP}$		ns	3, 4
5	T_{ACP1}	DACKN High to DACKN High	$2T_{CP}+35$ $-T_{DACY}$ and $3T_{CP}$		ns	3, 5
		READ CYCLE				
6	T_{DAR}	DACKN Low to RDN Low	0		ns	
7	T_{DRD}	RDN Pulse Width	T_{DDRL}		ns	
8	T_{DRA}	RDN High to DACKN High	0		ns	6
9	T_{DDAH}	DACKN High to Data		30	ns	7
10	T_{DDAL}	DACKN Low to Data		30	ns	7
11	T_{DDRL}	RDN Low to Data		35	ns	7
12	T_{DADR}	DACKN High to Data Release	2	25	ns	
13	T_{DRDR}	RDN High to Data Release	2	30	ns	
		WRITE CYCLE				
14	T_{DAW}	DACKN Low to WRN Low	0		ns	
15	T_{DWR}	WRN Pulse Width	37		ns	
16	T_{DWA}	WRN High to DACKN High	0		ns	
17	T_{DWCY}	WRN High to WRN Low	30		ns	
18	T_{DDW}	Data Setup to WRN High	0		ns	
19	T_{DHW}	Data Hold from WRN High	10		ns	

NOTES

1. Negation pending.
2. Assertion pending.
3. Synchronous transfers only.
4. FASTCLK disabled.
5. FASTCLK enabled.
6. RDN high may follow DACKN high.
7. Both T_{DDAH} and T_{DDAL} specifications must be met.



DMA READ



DMA WRITE

Figure 9. DMA Interface Timing

SCSI ASYNCHRONOUS TIMING

SCSI asynchronous timing is listed below and illustrated in figures 10 and 11.

#	Symbol	Description	Min	Max	Unit	Note
1	T_{AAROH}	ACKN (IN) Low to REQN (Out) High		50 30	ns ns	1 2
2	T_{AAROL}	ACKN (In) High to REQN (Out) Low		50 30	ns ns	1, 3, 6 2, 3, 6
3	T_{ARAOH}	REQN (In) High to ACKN (Out) High		50 30	ns ns	1 2
4	T_{ARAOL}	REQN (In) Low to ACKN (Out) Low		50 30	ns ns	1, 4, 6 2, 4, 6
		OUTPUT				
5	T_{ARDSO}	Data Setup to REQN (Out) Low	60 70		ns ns	1 2
5	T_{AADSO}	Data Setup to ACKN (Out) Low	60 70		ns ns	1 2
6	T_{ARHDO}	Data Hold from REQN (In) High	20 30		ns ns	1, 5 2, 5
6	T_{AAHDO}	Data Hold from ACKN (In) Low	30 35		ns ns	1, 5 2, 5
		INPUT				
7	T_{ARDSI}	Data Setup to REQN (In) Low	0		ns	
7	T_{AADSI}	Data Setup to ACKN (In) Low	0		ns	
8	T_{ARHDI}	Data Hold from REQN (In) Low		15	ns	
8	T_{AAHDI}	Data Hold from ACKN (In) Low		15	ns	

NOTES

1. Single-ended mode, 200pF loading.
2. Differential mode.
3. T_{ARDSO} specification must also be met (output cycle only).
4. T_{AADSO} specification must also be met (output cycle only).
5. FIFO is not empty.
6. FIFO is not full (input cycle only).

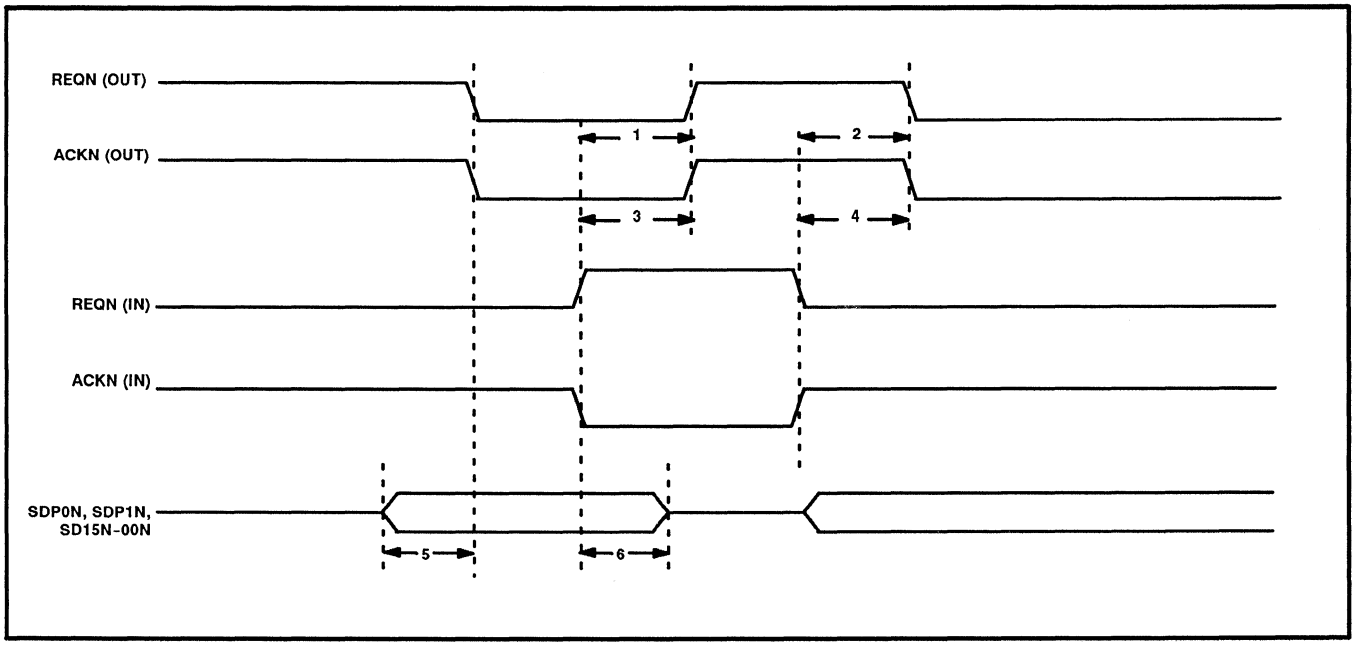


Figure 10. SCSI Asynchronous Output

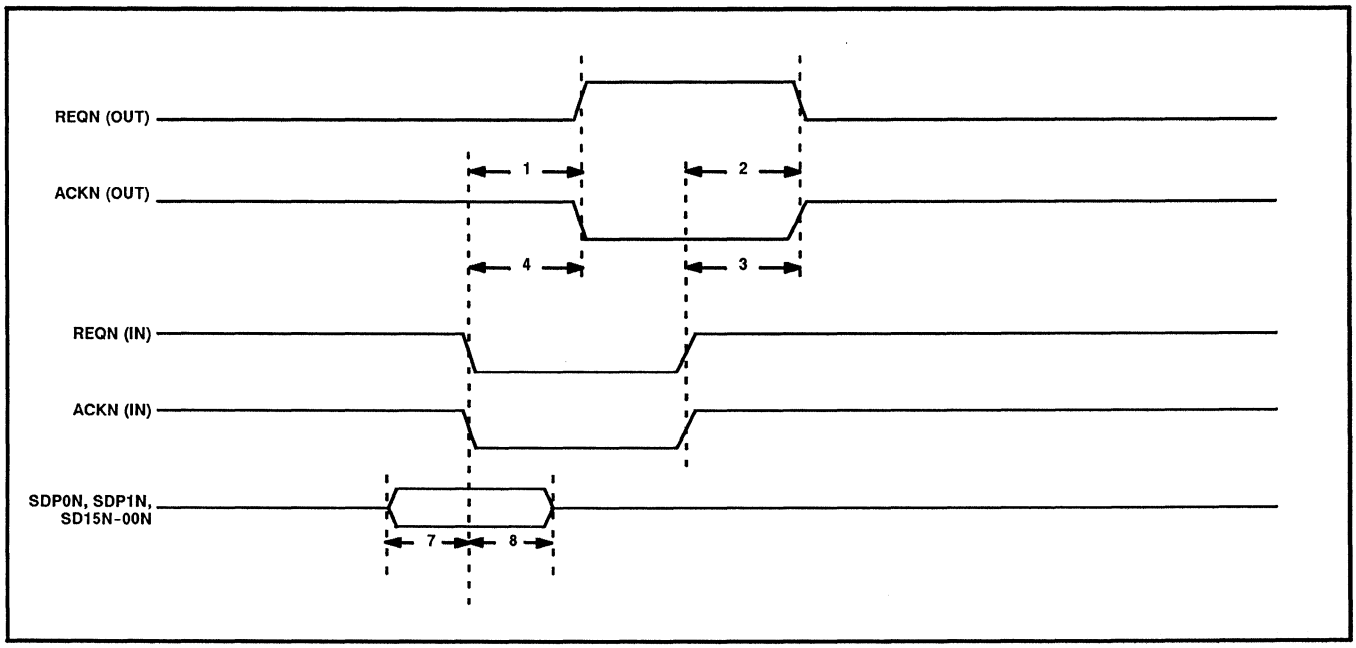


Figure 11. SCSI Asynchronous Input

SCSI SYNCHRONOUS TIMING

SCSI synchronous timing is listed below and illustrated in figures 12 and 13.

#	Symbol	Description	Min	Max	Unit	Note
		OUTPUT				
1	T_{SASTO}	REQN (Out) or ACKN (Out) Assertion Period	90		ns	1
			100		ns	2
			30		ns	3
			40		ns	4
2	T_{SNEGO}	REQN (Out) or ACKN (Out) Negation Period	90		ns	1
			100		ns	2
			30		ns	3
			40		ns	4
3	T_{SDSO}	Data Setup to REQN (Out) Low or ACKN (Out)	55		ns	1
			65		ns	2
			25		ns	3
			35		ns	4
4	T_{SHDO}	Data Hold from REQN (Out) Low or ACKN (Out)	110		ns	1
			110		ns	2
			45		ns	3
			45		ns	4
		INPUT				
5	T_{SRASTI}	REQN (In) Assertion Period	25		ns	5
6	T_{SRNEGI}	REQN (In) Negation Period	20		ns	5
7	T_{SAASTI}	ACKN (In) Assertion Period	20		ns	5
8	T_{SANEGI}	ACKN (In) Negation Period	20		ns	5
9	T_{SDSI}	Data Setup to REQN (In) or ACKN (In) Low	5		ns	
10	T_{SHDI}	Data Hold from REQN (In) or ACKN (In) Low	15		ns	

NOTES

1. Normal SCSI (5MHz), single-ended mode.
2. Normal SCSI (5MHz), differential mode.
3. Fast SCSI (10MHz), single-ended mode.
4. Fast SCSI (10MHz), differential mode.
5. Input specification for input cycle and output cycle.

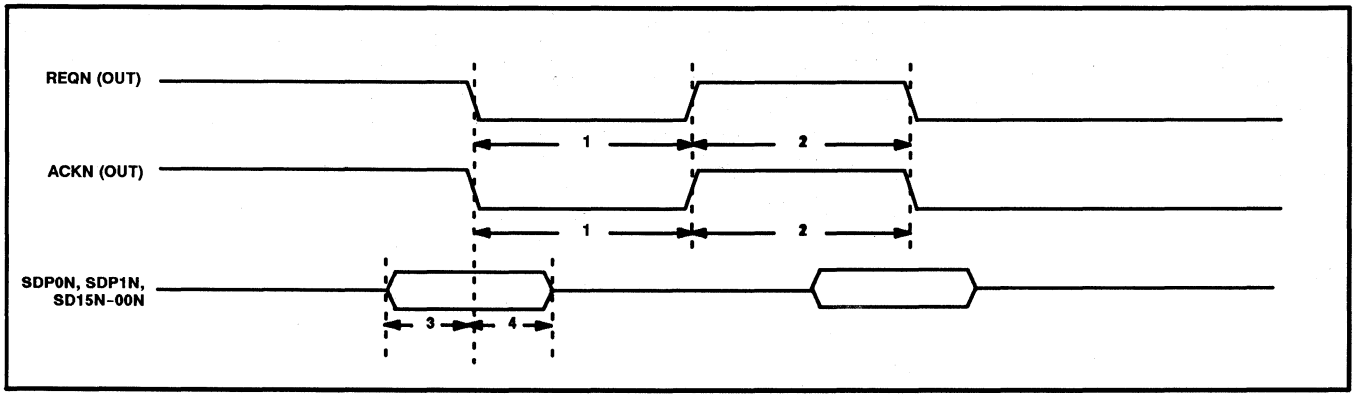


Figure 12. SCSI Synchronous Output

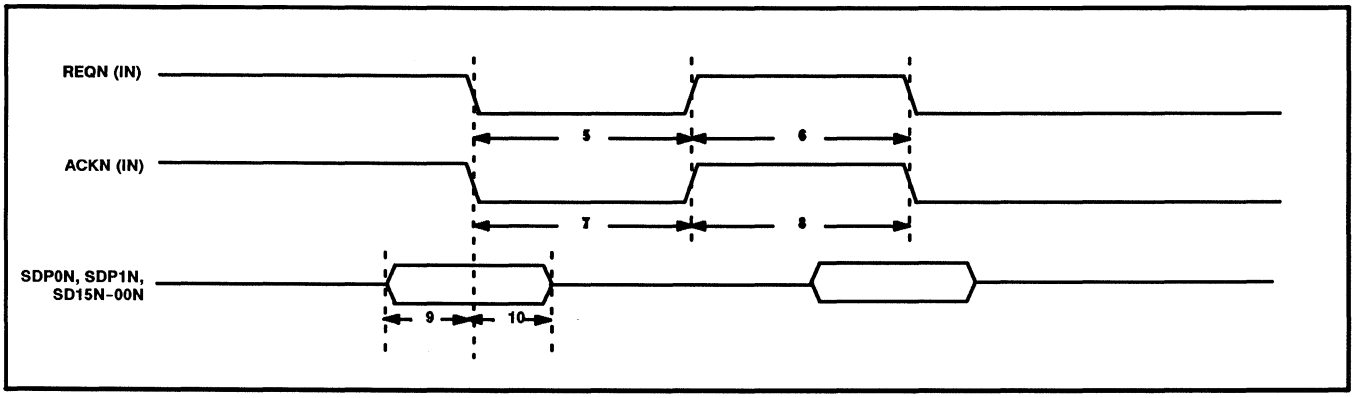


Figure 13. SCSI Synchronous Input

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