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ELECTRONIC ASSOCIATES, INC. *Long Branch, New Jersey*

TR-48 ANALOG COMPUTER

OPERATORS MANUAL

Reprinted October 1963

TR-48 COMPUTER

CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

CONTENTS (Cont)

ILLUSTRATIONS

SECTION I

INTRODUCTION

Many problems encountered in scientific or engineering work involve mathematical equations or sets of equations whose solution in most cases is difficult or practically impossible to obtain by the classical approach to equation solution. The TR-48 Analog Computer provides the technical worker with a general purpose computer which permits the rapid solution of linear or non-linear equations.

Although the analog machine is correctly termed a computer, it does not perform its computations by serial calculations as does the desk calculator or digital computer. Instead it performs the required mathematical operations in a parallel manner on continuous variables. In the TR-48, as in most modern analog computers, the continuous variables are direct current voltages. The electronic analog computer makes it possible to build an electrical model of a physical system where the voltages on the computer represent the dependent variables of the physical system. Except for a constant of proportionality, or scale factor, each voltage will behave with time in a manner similar to the physical system variable. Thus, if the vertical position of the center of gravity of an automobile oscillates with time during a disturbance, then the voltage representing the height of the center of gravity above the road surface will also oscillate; if the temperature of the coolant at the exhaust port of a condenser rises exponentially to a steady value, then so will the voltage representing it on the computer.

It can be said that the actual system and the electrical model are analogous in that the variables which demonstrate their characteristics are described by relations which are mathematically equivalent. The actual system has thus been simulated because of the similarity of operation of the electrical model and the physical system. This capability of the analog computer is of great value in performing scientific research or engineering design calculations because it permits an insight into the relationship between the mathematical equations and the response of the physical system. Once the electrical model is completed, well-controlled experiments can be performed quickly, inexpensively, and with great flexibility to predict the behavior of the primary physical system.

Although the analog computer utilizes electronic components in its operation, it is not essential that the user have an extensive knowledge of electrical circuits. The TR-48 is basically a set of mathematical building blocks, each able to perform specific mathematical operations on direct voltages and capable of being easily interconnected. By appropriately interconnecting these building blocks, an electrical model is produced in which the voltages at the outputs of the blocks obey the relations given in the mathematical description of a physical problem.

Since our interest is frequently in the dynamic behavior of physical systems, the mathematical equations are usually differential equations having time as the independent variable. In order to solve such equations, the standard components of the computer must perform the following operations: inversion, algebraic summation, integration with respect to time, multiplication and division, and function generation.

The sequence of steps for constructing a dynamic model on an analog computer requires first a mathematical description of the physical system, usually in equation form. From this description the operator derives the information necessary to set up a computer program for interconnecting the computing components and determines the required initial conditions and forcing functions. The computing components are interconnected with wires called patch cords. The input and output terminations of the computing components are brought out to a patch bay which is fitted with a removable patch panel into which the patch cords are inserted. The problem patching may, therefore, be done in advance, away from the computer. The problem is placed on the computer by inserting the patch panel and adjusting the problem parameters to the value of the first case to be investigated. Selected voltages are applied to various components in the form of inputs or initial conditions. These voltages are derived from a precise reference voltage.

Once the computing elements have been patched, adjusted, and energized, the computer is switched into the operate mode. The voltages on the computer change with time in accordance with the equations that govern the physical system variables. The behavior of the computer model is viewed through an output device such as an X-Y plotter, oscilloscope, strip-chart recorder, or digital voltmeter.

The intention of this manual is to provide the scientist or engineer, using an analog computer for the first time, with an introduction to its functions, programming, and operation so that he is able to achieve usable experimental results. The reader ought to gain from the early sections sufficient knowledge of the computer operation to enable him to interconnect computing components and to operate the computer without difficulty. Later sections provide an understanding of simple programming procedures and computing techniques so that he is able to construct a computer program for any straightforward investigation. Needless to say, the full story cannot be told in a short manual and in many cases the literature cited in the bibliography provides a more comprehensive treatment. However, the ideas and facts presented here should set the reader well along the best path towards dynamic problem investigation by effective use of the modern general purpose analog computer.

SECTION II

THE TR-48 COMPUTER

1. GENERAL DESCRIPTION OF THE TR-48

The PACE® TR-48 (Figure 2.1-1) is a fully transistorized, general purpose analog computer. Consisting entirely of solid-state circuit elements, the TR-48 is compact in size and is suitable for desk top mounting. The computer is able to operate stably and accurately in normal office ambient conditions; there is no need for large primary power systems or special cooling duct installations since the power requirements are small. Reliable, with simplicity in functional design, the TR-48 is easy to use and can be a powerful aid to the individual engineer in the rapid solution of scientific and engineering problems.

The TR-48 utilizes a building block concept, in which individual computing components may be easily interconnected to solve the required equations by forming electrical models analogous to the system under study. Each building block, either individually or in combination with others, is capable of performing one or more of the following operations on variable DC voltages: multiplication by a constant, algebraic summation, integration with respect to time, multiplication of two variables, and generation of known functions of a variable. Each component has input and output terminations which are readily accessible at the computer Pre-Patch Panel for interconnection by bottle plugs (jumpers) and patch cords.

The Pre-Patch Panel is arranged in a series of twelve similar modules, with each module terminating a complete set of computing components. (Figure 2.1-2.) The modular design tends to eliminate patch-panel clutter caused by long across-the-panel patching. In addition, problem patching, checking, and trouble-shooting are more readily accomplished, and patching errors are less likely. The five patching areas within each module are color coded in vivid contrasting colors with large, clear lettering to help in faster and surer patching. The Pre-Patch Panel is removable to permit problem storage and also problem patching without committing operating time.

To the left of the Pre-Patch Panel is the monitoring and control panel. This area contains the control switches, and metering circuits which permit turning the computer on and off, engaging and dis-engaging the removable Pre-Patch Panel, and controlling the computer mode. Monitoring facilities consist of a digital voltmeter and a multi-range voltmeter. The digital voltmeter permits setting problem parameters to two-decimal accuracy and observing or measuring all computational and operating potentials.

To the right of the Pre-Patch Panel is the coefficient-setting potentiometer and function switch panel. This panel provides space for a maximum of sixty potentiometers and five function switches. Four of every five potentiometers have one

end grounded while the fifth potentiometer is ungrounded. The potentiometers and function switch connections are terminated in the appropriate areas as indicated on the Pre-Patch Panel.

2. OPERATING CONSIDERATIONS

The TR-48 is shipped complete with all components in place. The unit is completely calibrated and adjusted at the time of manufacture. After performing the simple installation checkout procedure outlined in the maintenance manual, and connecting the unit to a suitable power source, the computer is ready for operation.

The use of low level reference supplies (+10 and -10 volts) with their associated current-limiting circuits eliminates shock hazards when patching with the Pre-Patch Panel in place in the computer. The current-limiting circuits also protect the reference supplies from damage due to shorting to ground, or to each other. Thus an errant patching connection (shorting the plus reference to the minus reference for example) will not adversely effect the supplies (output current drops to zero) nor will the reference supply fuses blow. In addition, the metal portions of the Pre-Patch Panel (except the handles) have a scratch-resistant, non-conductive paint coating which, in conjunction with the plastic patching blocks, practically eliminates shorting-out hanging patch cords. Not so.

a. Preliminary Operating Considerations

The following steps are recommended prior to operating the TR-48 to prevent possible false trouble indications.

(1) Ascertain that all operational amplifiers have four-connector bottle-plugs properly placed and seated as shown in Figure 2.2-1. This provides the amplifiers with feedback and prevents them from overloading during the problem solution. The procedure for inserting and removing the Pre-Patch Panel is described in Sub-Paragraph b.

(2) Patch the Digital Voltmeter (DVM) and multi-range voltmeter (VM) to the selector readout system. (See Figure 2.3-2 and Paragraph 3a. of this section for a description of the selector system operation.)

(3) Apply power to the computer and depress the PS (potset) button. Initially the overload lamps of the operational amplifiers will light; after a few seconds all of the lamps should extinguish.

(4) Check the various supply voltages of the TR-48. All power supply outputs are connected directly to the voltmeter FUNCTION switch (through appropriate scaling resistors); thus, the check may be accomplished simply and rapidly. (See Paragraph 3c. of this section.)

(5) Check the plus and minus reference supplied for readout on the DVM by selecting A49 and A50. (See Paragraph 3a.)

A48

TR48
45

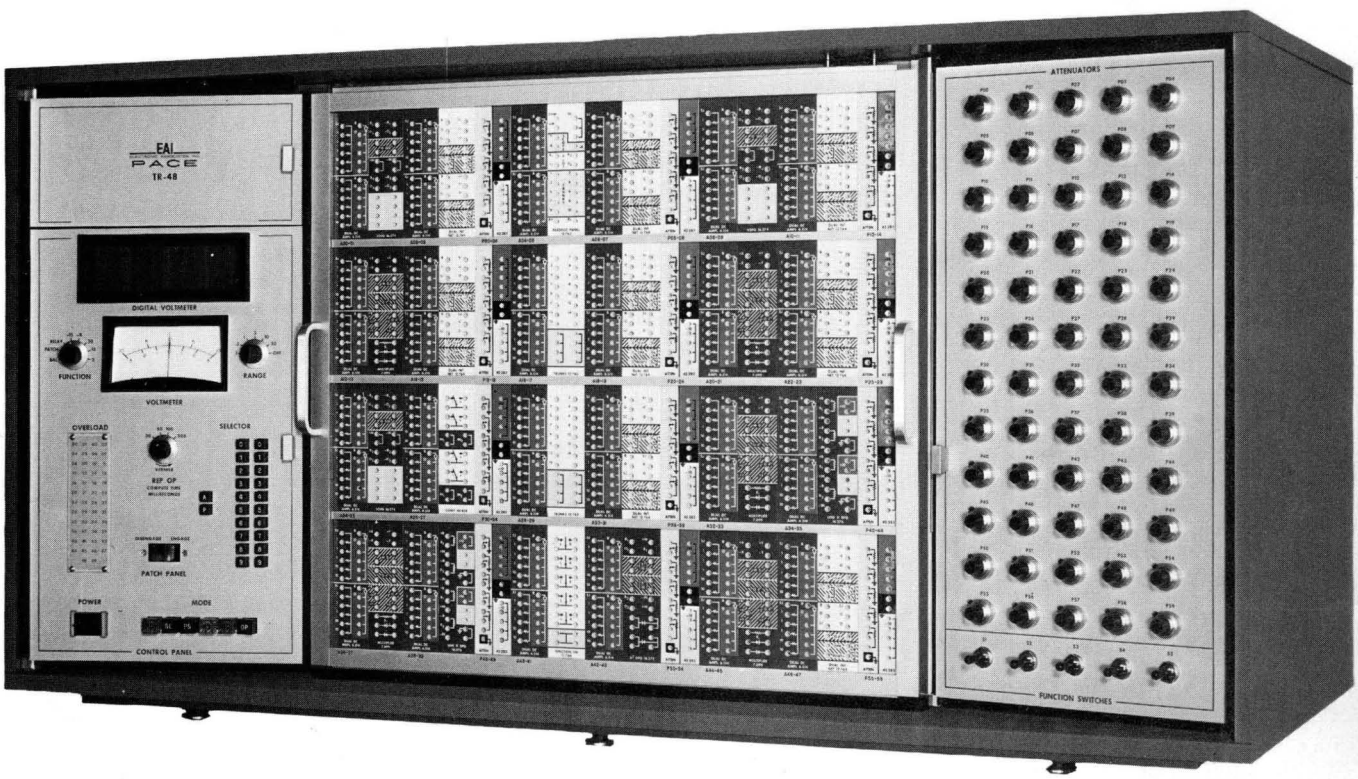


FIGURE 2.1-1 TYPICAL TR-48, FRONT VIEW

TR-48
69

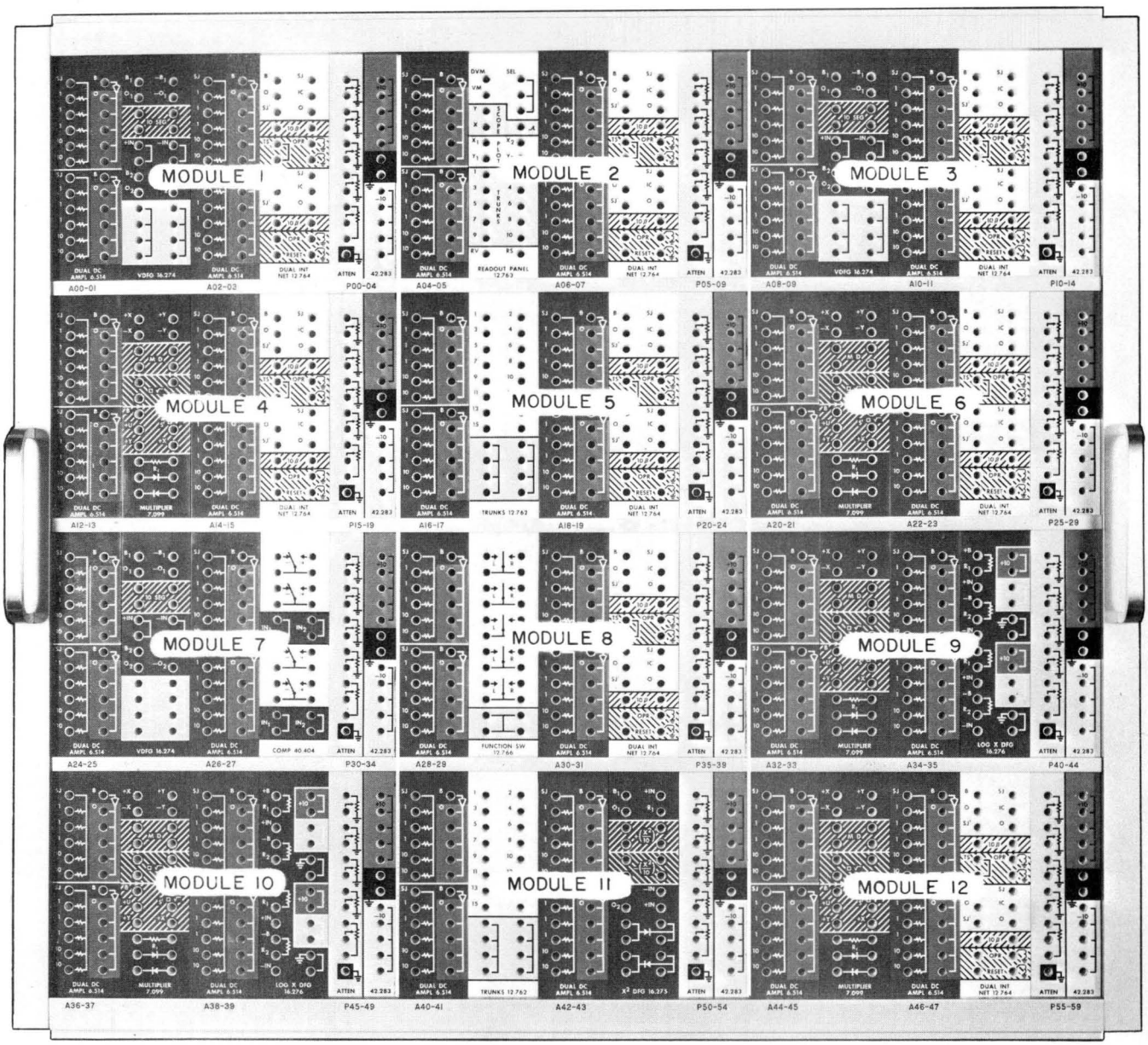


FIGURE 2.1-2 PRE-PATCH PANEL MODULAR LAYOUT

TR48
47,38

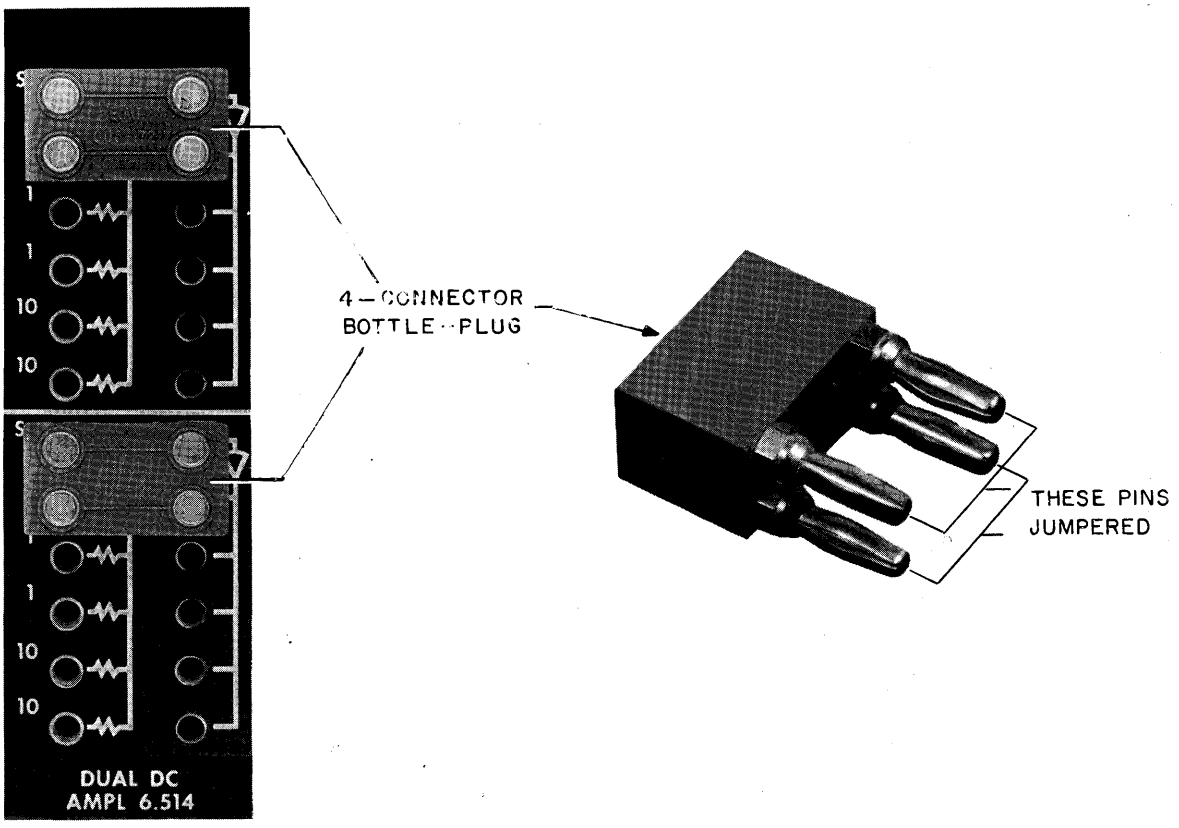


FIGURE 2.2-1 AMPLIFIER WITH FOUR-CONNECTOR BOTTLE-PLUG PROVIDING FEEDBACK

CAUTION

If the VM FUNCTION switch is in the PATCH position the selected voltages are also applied to the VM. Be sure the RANGE switch is set to a high enough range selection to handle these inputs.

(6) Allow a few minutes warm-up time; this assures that the computing components, (including the DVM) are up to normal operating temperature. Ground the DVM input termination (designated DVM on the 12.763 READOUT PANEL) and adjust the DVM zero control on the back of the Control Panel door (Figure 2.2-2) for a 00.00 reading. Should the polarity relay begin to chatter, turn the zero control slightly clockwise until the chatter stops and the indicators retain the 00.00 display. The DVM zero adjustment should be checked daily; initially, due to aging of the precision components, this adjustment may be required more frequently.

(7) In the pot-set mode of the computer (PS button on the Control Panel depressed), closed relay contacts provide a feedback circuit for the operational amplifier. (See Paragraph 4 of this section for a more detailed description.) This feature permits the removal of the Pre-Patch Panel to balance the operational amplifier. However, when the computer is switched from pot-set to any other mode, the relay contacts open and the circuit as patched on the Pre-Patch Panel provides the feedback loop. Momentary amplifier overload may result during the relay operating time; thus to eliminate possible error in the computer solution, the operator should always switch the computer to re-set (depress the RS button) before switching to the operate mode. This permits the pot set relays to open and the amplifier summing junctions to settle before starting the problem solution. There is no actual waiting period required; that is, the operator may depress the RS button and then immediately depress the button for the desired mode. This sequence of operation will prevent the possible momentary overloads from effecting the problem solution.

b. Pre-Patch Panel Insertion and Removal

To insert the Pre-Patch Panel, set the lip on the lower edge of the panel in the guide groove (Figure 2.2-3). Push the top of the panel in so the panel is vertical. (A micro-switch will not permit the Pre-Patch Panel motor to function unless the panel is properly seated.) Applying a slight hand pressure to the center of the panel (to maintain the panel in the vertical position) depress and hold the ENGAGE button on the Control Panel. (The computer must be in the pot-set mode.) This button properly seats and firmly holds the Pre-Patch Panel in position. Note that the ENGAGE and DISENGAGE positions of the switch are spring loaded; therefore, the switch must be depressed and held until the limit switches stop the motor operation. This feature eliminates the possibility of accidentally engaging or disengaging the Pre-Patch Panel.

The removal of the Pre-Patch Panel is essentially the opposite of inserting the panel. When disengaging the panel (depress and hold the DISENGAGE button) a light

hand pressure should again be placed on the panel to eliminate the possibility of the panel falling forward when disengaged.

c. Amplifier Balance

The d-c operational amplifiers are chopper stabilized to prevent drift and resultant errors in the computer results. Drift in an amplifier results in an output voltage (or offset) with a zero input. To eliminate offset, the amplifiers of the TR-48 are balanced, i.e., with a zero input, a bias current is applied to the amplifier summing junction equal and opposite to any current due to drift thus placing the summing junction at virtual ground. Once balanced, drift in the amplifiers is eliminated automatically by the stabilizer circuit.

The d-c amplifiers of the TR-48 are extremely stable and normally do not require balancing for periods up to several months. To assure accuracy and confidence in the computer results, it may be desirable to check the amplifier balance daily; this check can be made rapidly and simply since the selector system and voltmeter are used. The following is a step by step procedure for checking amplifier balance.

(1) Place the voltmeter FUNCTION switch in the BAL position and depress the PS push-button of the MODE switch.

(2) Using the selector system, select each amplifier A00 through A49 (A48 and A49 are the plus reference and minus reference amplifiers respectively). The voltmeter should register a zero deflection for each amplifier.

(3) Should an amplifier cause a deflection to either side of the center zero on the voltmeter, adjust the corresponding balance control. The balance controls for amplifiers A00 through A47 (the operational amplifiers) are located directly behind the Pre-Patch Panel (Figure 2.2-4a). The balance controls for A48 and A49 (reference amplifiers) are located on the Reference Regulator 43.104 behind the Potentiometer Panel (Figure 2.2-4b). Adjust these controls for a zero reading on the meter.

d. Changing Computational Components

In the solution of some problems it may be necessary to add a specific type of computational component to the existing complement. Since many of the module positions are designed to handle more than one type of computing component, a component not required in the problem investigation may be removed and another unit placed in that cradle. Figure 2.2-5 illustrates the various positions of the computing components in the TR-48 module area. This diagram illustrates which type of computing component is compatible with each cradle or module position. The procedure for replacing a computer component and changing the Pre-Patch Panel patching block is described in the following Sub-Paragraphs (1) and (2).

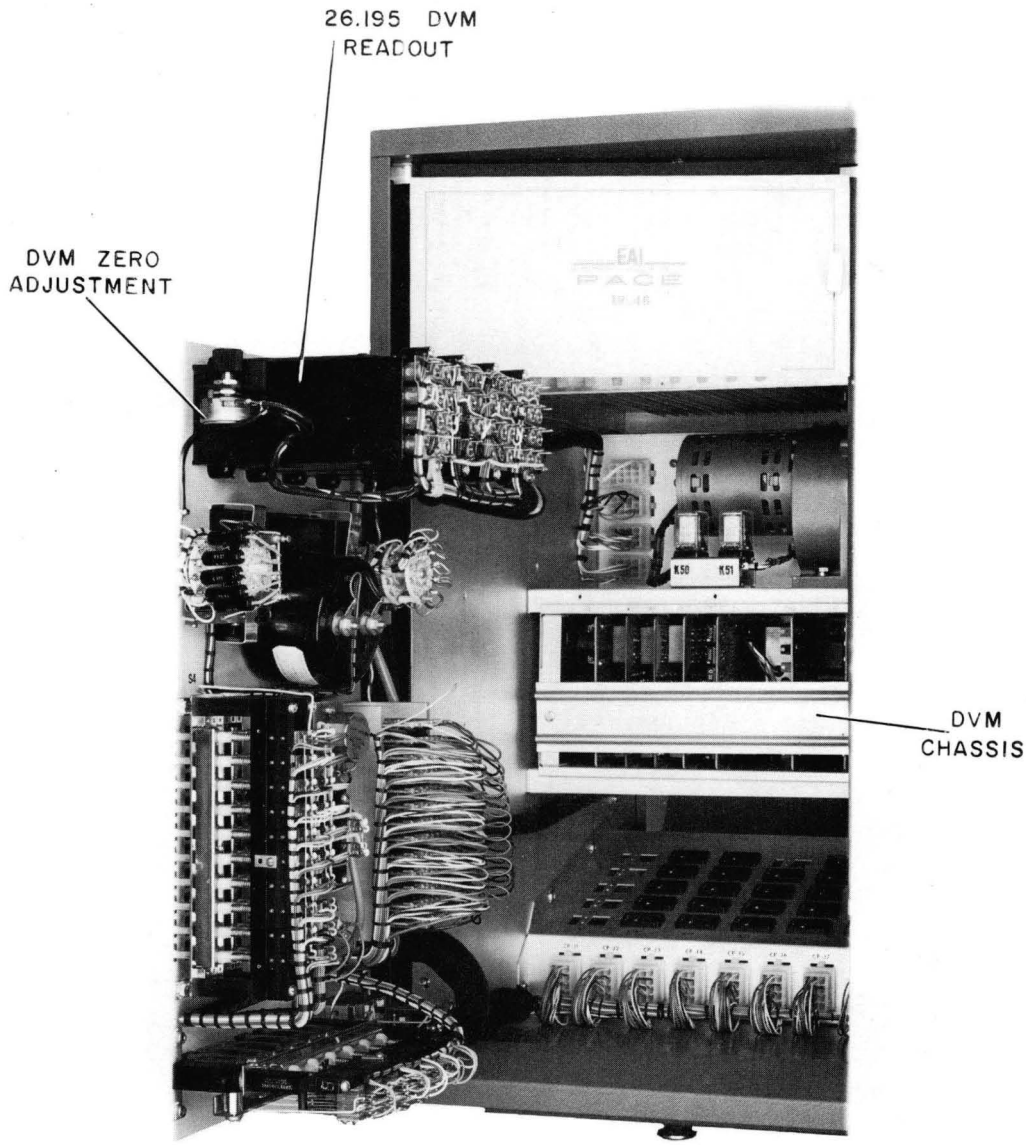
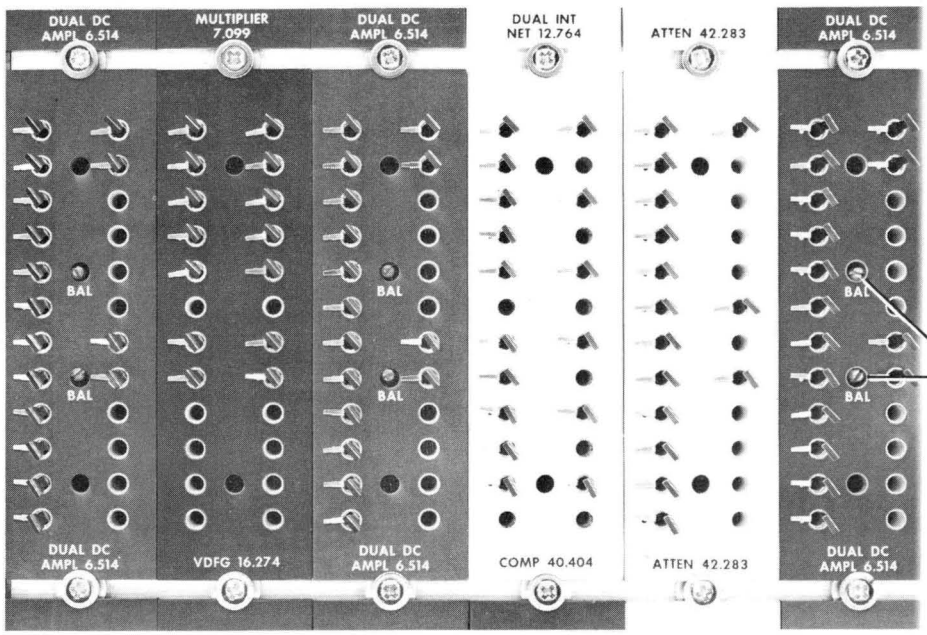


FIGURE 2.2-2. DVM ZERO ADJUSTMENT LOCATION

A4628

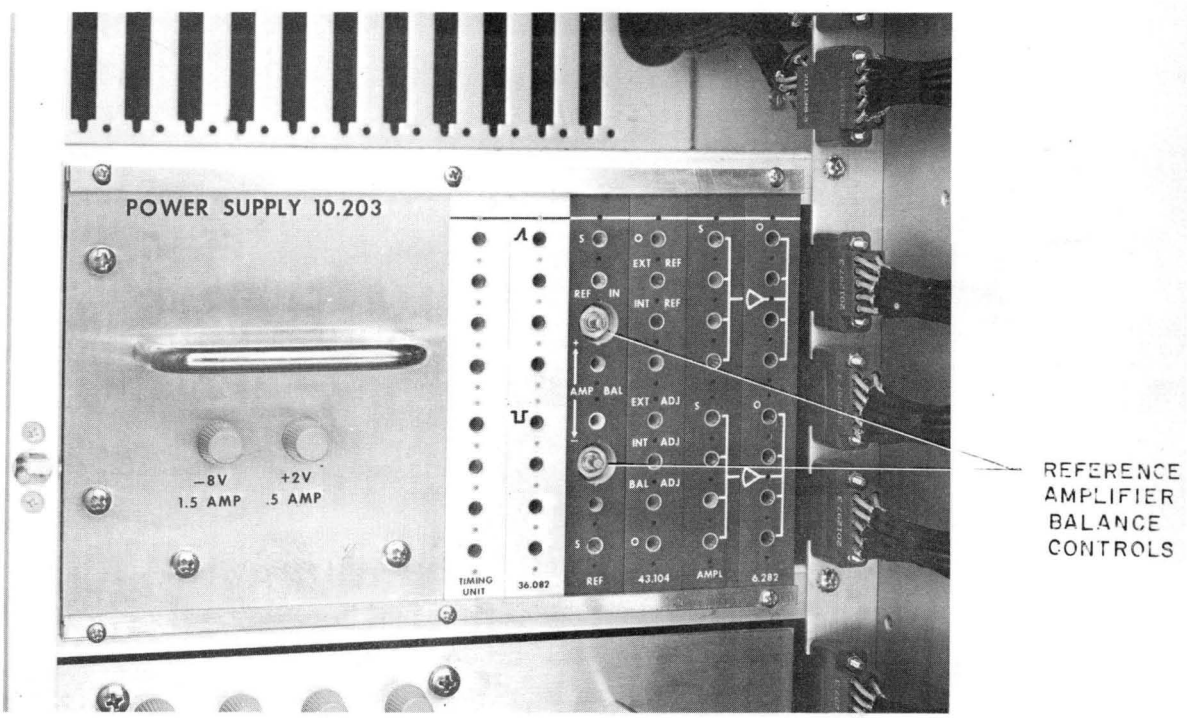
TR48
#22

FIGURE 2.2-3 PRE-PATCH PANEL INSERTION



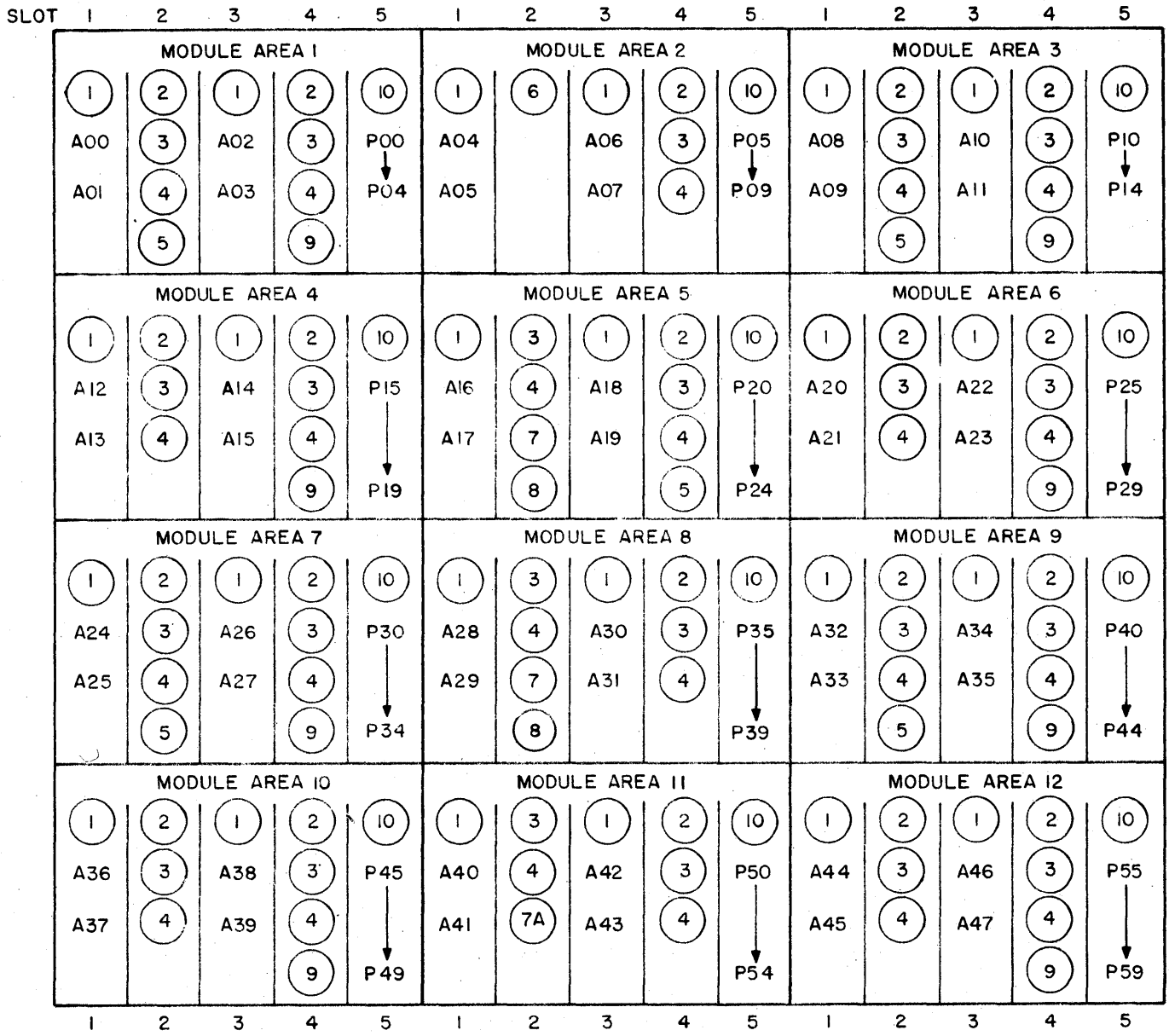
TR-48
#66,67

a.



b.

FIGURE 2.2-4. AMPLIFIER BALANCE CONTROL LOCATION



SYMBOL KEY

1. DUAL DC AMPLIFIER
2. DUAL INTEGRATOR
3. QUARTER-SQUARE MULTIPLIER
4. FIXED DIODE FUNCTION GENERATOR (X^2, LOG X, $\frac{1}{2}$ LOG X)
5. VARIABLE DIODE FUNCTION GENERATOR
6. READOUT PANEL
7. TRUNKS
7A. IN TRUNKS
8. FUNCTION SWITCHES
9. COMPARATOR
10. POTENTIOMETERS & REFERENCE

FIGURE 2.2-5 COMPUTER COMPONENT MODULE ASSIGNMENT AREAS

NOTE

Failure to change the Pre-Patch Panel patching block may prevent proper use of a computer component due to the arrangement of jumpers on the rear of the patching block.

(1) Computing Module Replacement

(a) Remove the Pre-Patch Panel to expose the component modules. Remove the two phillips-head retaining screws from the top and bottom of the module to be removed (Figure 2.2 -6).

(b) Insert the special module removal handle in the holes provided in the central area of the module (Figure 2.2-6). Pull the module forward removing it from the TR-48.

(c) Place the new component in place; be sure the guide pins are properly seated in the guide-pin holes before mating the connectors at the rear of the module.

(d) Check that the module is properly installed (connector firmly mated, etc.) and replace the two retaining screws.

(2) Patching Block Replacement

(a) The Patching blocks of the computing components are held securely in place by the retaining strips on the front of the Pre-Patch Panel (Figure 2.2-7a).

(b) The retaining strip above or below the patching block may be removed to change blocks. The retaining strip is released by removing the four screws directly behind the strip on the rear of the Pre-Patch Panel (Figure 2.2-7b).

(c) Once the retaining strip is free, remove the original patching block and replace it with the new block (Figure 2.2-7). Secure the retaining strip with the four screws. The Pre-Patch Panel is now ready for problem patching.

NOTE

If blocks on two adjacent horizontal rows are to be replaced it is only necessary to remove the retaining strip between the two rows. Patching blocks may then be removed from the row above and below the strip.

3. MONITORING AND CONTROL

The control panel of the TR-48 is designed to allow simple control and monitoring of the computer components (Figure 2.3-1). The following sub-paragraph describes the function and operation of the various switches and controls mounted on this panel.

a. Signal Selector

The signal selector consists of three vertical rows of pushbuttons: The first row contains two buttons designated A and P, and the second (tens) and third (units) rows contain buttons designated 0 through 9. Depressing the A button permits the operator to select the outputs of the 48 operational amplifiers (A00 through A47), the two reference supply amplifiers A48 and A49 (plus and minus reference respectively), and 15 of the IN trunk lines (selected as A50 through A64). Depressing the P button permits the operator to select the individual wiper outputs of the sixty potentiometers (P00 through P59).

Depressing the tens button (assuming the A button is depressed) sets the selector system for amplifiers in a given tens group, i.e., if the 2 button in the tens row is depressed, amplifiers A20 through A29 are set up for selection. The units button determines which of these ten amplifiers is actually selected. The selector system button numbering corresponds with the amplifier and potentiometer designations as marked on the Pre-Patch Panel and Potentiometer Panel respectively.

Once the letter and tens selector buttons are depressed, say P1 (addressing P10 through P19), the individual potentiometers of this group may be selected by merely changing the units designation button, i.e., if P10 is selected, P11 may be selected by depressing the units 1 button only.

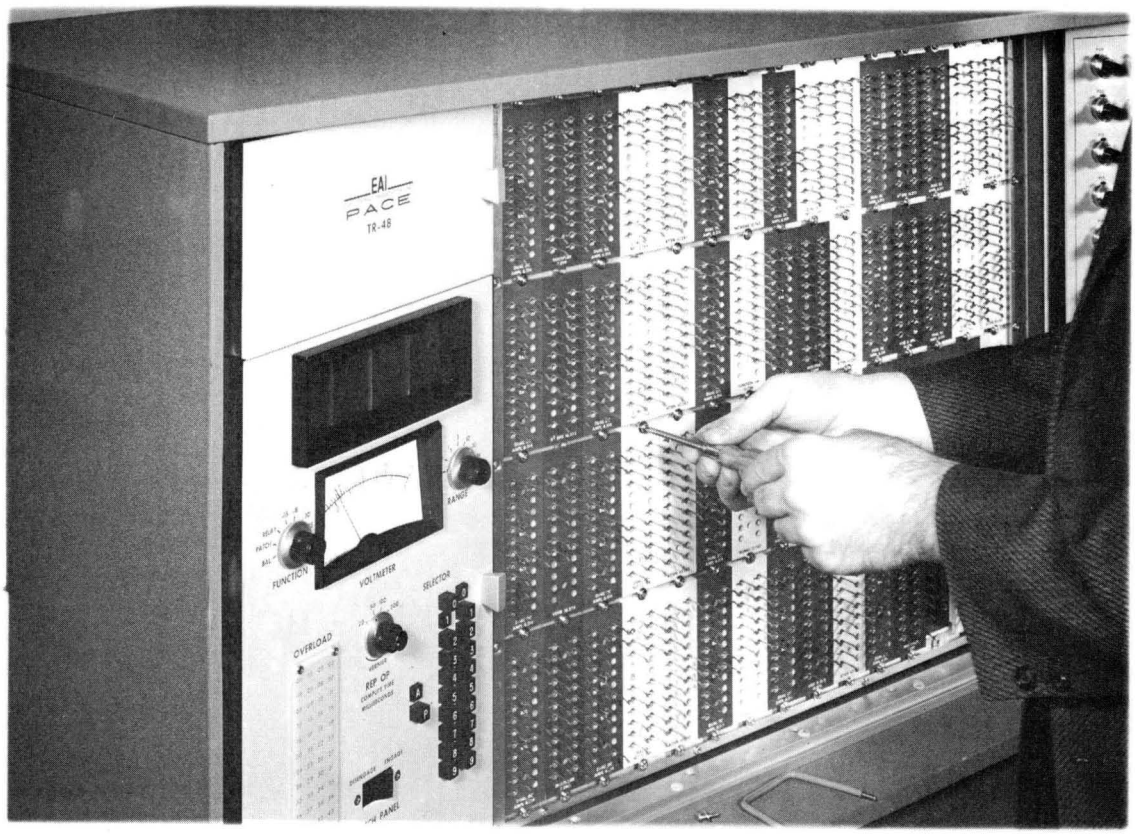
The selector system output is connected to the three terminations marked SEL in the upper white portion of the 12.763 Readout Panel (Figure 2.3-2a).

In order to read out a selected signal on the DVM, the upper bottle plug shown in Figure 2.3-2b must be in place. The multi-range voltmeter (VM) may also be connected to the selector line by installing the lower bottle plug shown in the illustration (the VM FUNCTION switch must be in the PATCH position). It should be noted, however, that the VM circuit will load the output of the selected component with a relatively low impedance and should not be used if the monitored circuits cannot tolerate this load. (Set the FUNCTION switch to a position other than PATCH to disconnect the VM from the SEL terminations.) The VM should not be used when setting attenuators. To prevent this possibility from accidently occurring, a relay circuit disconnects the VM from the selector system when the computer is placed in the pot-set mode.

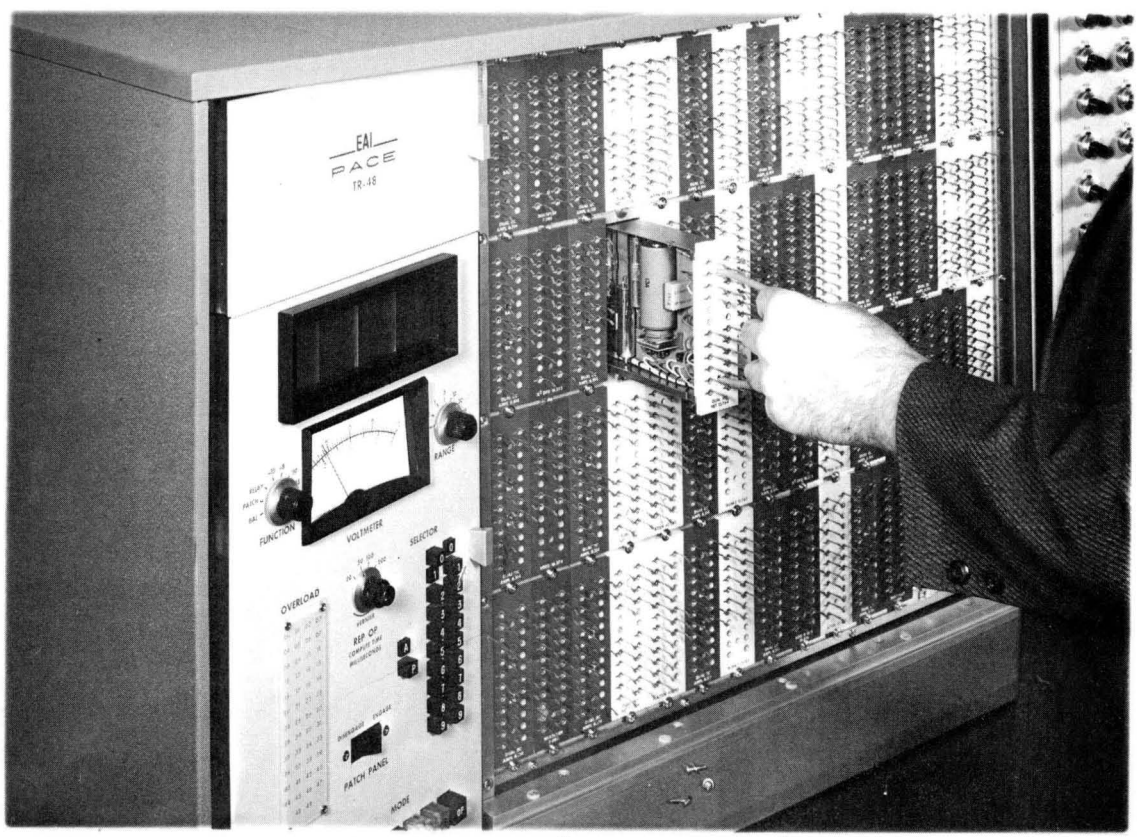
b. Digital Voltmeter

The Transistorized Digital Voltmeter 26.183 is terminated in the 12.763 Readout Panel area (Figure 2.3-2a) and is designated DVM. As previously mentioned the

TR 48
#26
#29

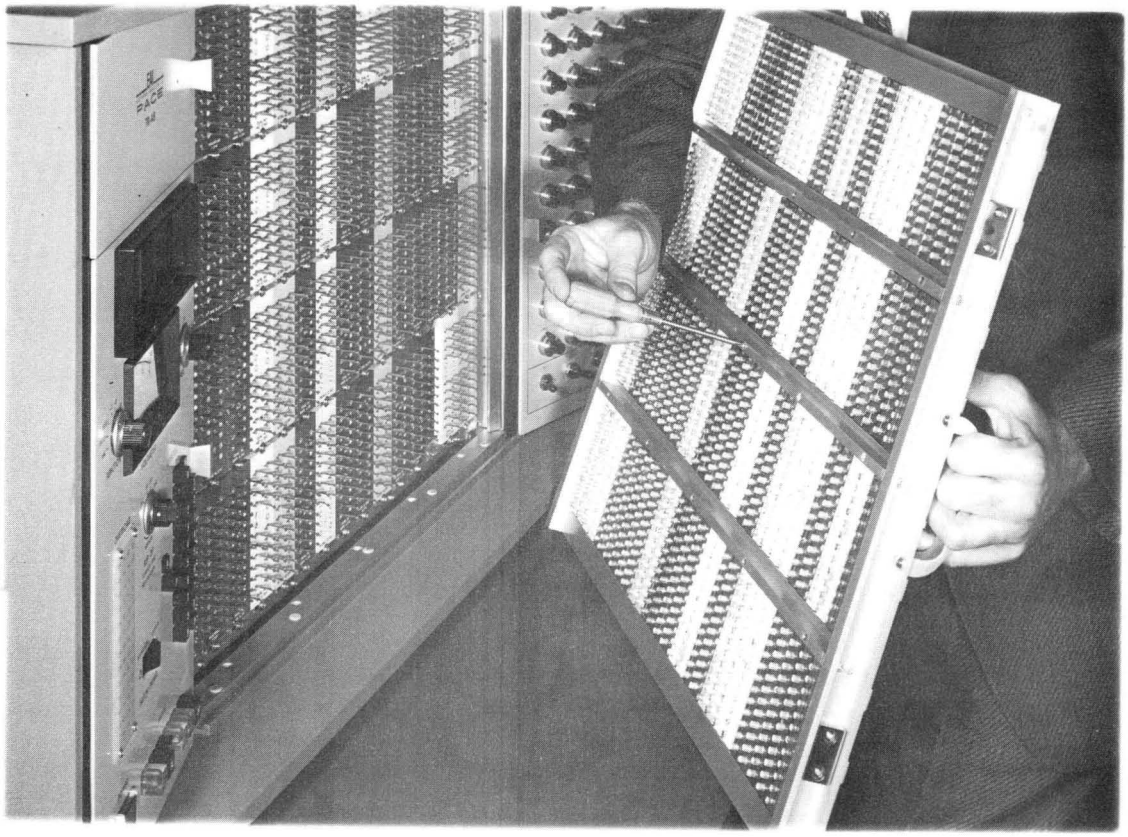


a



b

FIGURE 2.2-6 REMOVAL OF COMPUTING MODULE



a

TR48
23
24

b

FIGURE 2.2-7 PATCHING BLOCK REPLACEMENT

TR48
48

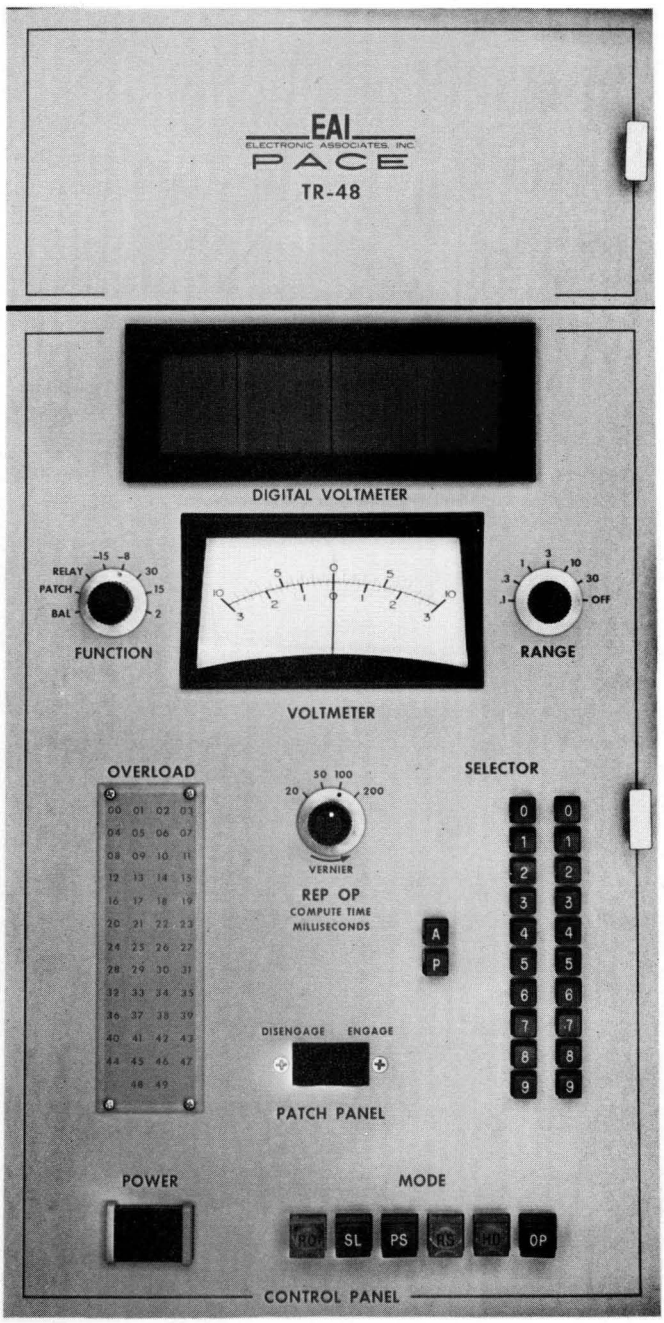


FIGURE 2.3-1 TR-48 CONTROL PANEL

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#60
#61

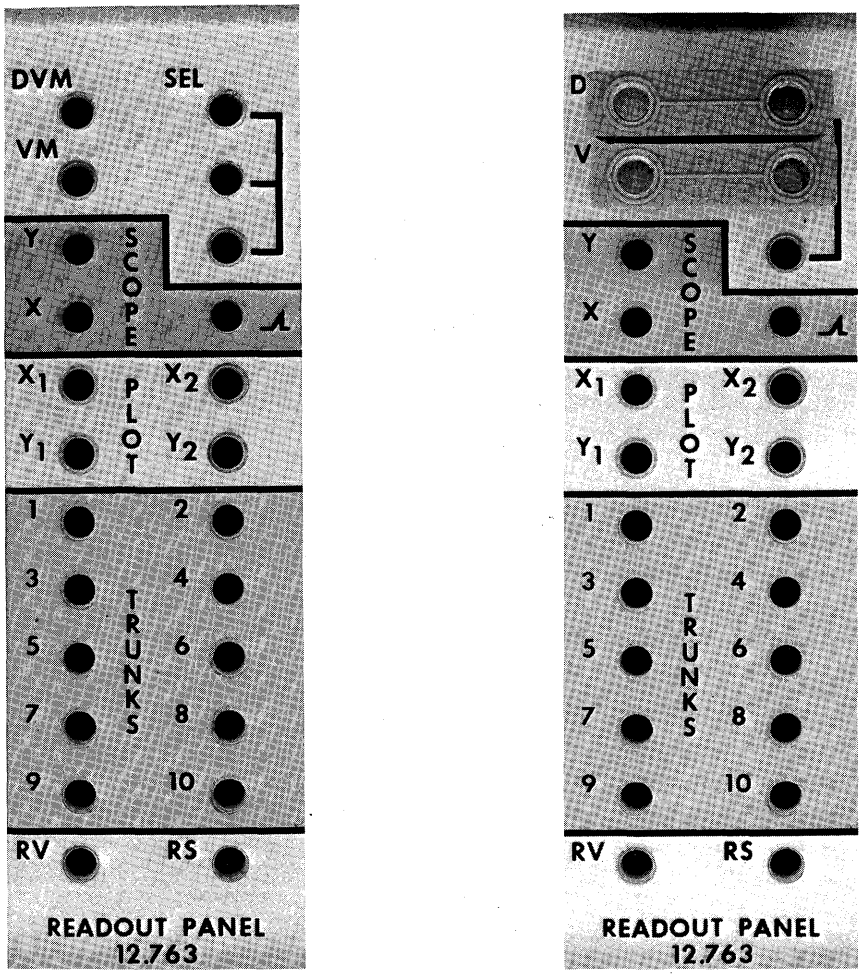

FIGURE 2.3-2 READOUT PANEL 12.763 AREA AND DVM/VM TO SEL PATCHING

DVM may be bottled to the SEL termination to monitor the selector system voltages, or with a patch cord the DVM may be used to monitor signal levels at practically any termination in the Pre-Patch Panel. The DVM has a 10 megohm (minimum) full-time input impedance.

The only operational setting required for the DVM is periodic adjustment of the zero control. (See Paragraph 2a., Operating Considerations.)

c. Multi-Range Voltmeter

The Multi-Range Voltmeter is permanently wired into various circuits of the TR-48 to facilitate rapid readout of certain voltages by selection with the meter FUNCTION switch. The voltmeter also has a RANGE switch, thus permitting close to full scale readouts for maximum accuracy. The ranges are 0.1, 0.3, 1, 3, 10, and 30 volts, (in addition to an off position). The RANGE switch functions only when the function switch is in the PATCH position. The PATCH position connects the voltmeter to the Pre-Patch Panel VM termination (Figure 2.3-2) permitting this point to be bottle-plugged to the SEL output or, as in the case of the DVM, monitoring voltages at most Pre-Patch Panel terminations via a patch cord.

Following is a list of the voltmeter FUNCTION switch positions with a brief description of the function of each position.

POSITION	DESCRIPTION
BAL	Connects the stabilizer output of the amplifier addressed by the selector system to the meter to facilitate checking and/or adjusting the amplifier balance.
PATCH	Connects the meter, via the RANGE switch, to the VM Pre-Patch Panel termination.
RELAY	Connects meter to the relay power supply (-20 volts).
-15, -8, 30, 15, and 2	Connects voltmeter to output of corresponding power supply. and automatically selects meter scale.

d. Computer MODE

The operating mode of the computer is controlled by the six-pushbutton selector just to the right of the POWER button (Figure 2.3-1). Following is a list of the pushbutton and brief description of their functions.

MODE BUTTON	DESCRIPTION
OP (Operate)	When this pushbutton is depressed, all integrators are simultaneously released to respond to

MODE BUTTON	DESCRIPTION
OP (Operate) (Continued)	input signal voltages. The integrator outputs change in potential as dictated by the inputs; a time varying behavior is produced. This generates the voltage solution of the programmed problem.
HD (Hold)	Depressing the HD pushbutton permits the problem solution to be stopped and all voltages held at the potential attained up to the instant of depressing the button. The problem may be continued from this point by depressing the OP button or re-set to the starting point by depressing the RS button.
RS (Reset)	In the RESET mode all circuits except the integrators function normally. The integrator outputs are held at their respective initial conditions (IC) as dictated by the IC input voltage. (The integrator output is zero if no IC voltage is applied.)
PS (Pot Set)	Amplifier input resistor summing junction grounded; permits setting potentiometers under actual load. Also provides amplifiers with relay-contact feedback so Patch Panel may be removed to balance amplifiers.
SL (Slave)	When a TR-48 Computer is to be slaved to another TR-48 (master) this button is depressed. The slaved computer then responds to the selected modes of the master computer pushbuttons.
RO (Rep-Op)	The RO button switches the computer into the repetitive operation mode. The computer switches automatically between operate and reset at a predetermined rate. (See Paragraph 8 of this section.)

e. Overload Indicators

The overload indicators (Figure 2.3-1) provide a visual alarm when an overload occurs in any of the operational amplifiers, i.e., when the summing junction is not at virtual ground. An overload may be due to improper scaling, improper patching or loading.

When the computer is initially turned on, all the indicator lamps may light; however, in a few seconds, as the amplifiers settle, all the lamps should go out. Should a lamp remain lit it could be caused by a patching error such as the failure to provide un-used amplifiers with feedback (via the four connector bottle plugs). Prolonged overloads will not damage an amplifier.

f. Trunks

The trunks (terminating at the Trunk 12.762 area) provide point-to-point connections to the connectors at the left-rear of the computer (Figure 2.3-3). These connectors may be used as outputs to accessory equipment, or the trunk terminations may be cabled to a second TR-48 as signal carrying lines for the interconnection of the problems patched on the separate Pre-Patch Panels of slaved computers.

g. Readout Devices

The problem solution obtained from the TR-48 may be permanently recorded or temporarily displayed on various types of readout devices. A few of the more common readout devices are described in this paragraph.

Either the DVM or voltmeter may be used to read out the problem solution. These devices, however, do not record the solution and thus a permanent record is not made. When in REP-OP the computer solution is continuously displayed on an oscilloscope; in this case a permanent record may be obtained by photographing the scope trace. X-Y plotters (such as the EAI 1110 VARIPLOTTER®) or strip-chart recorders may be used for a permanent record of TR-48 problem solutions. These units, however, do not have the frequency response necessary to accurately record the solution when the computer is placed in the high-speed REP-OP mode of operation. The Readout Panel scope and plotter terminations are wired to connector plugs at the rear of the TR-48. See Figure 2.3-3.

4. ATTENUATORS

One of the simplest and most useful operations performed on an analog computer is the multiplication of a variable voltage by a positive constant less than unity; i.e., attenuation of a signal. The TR-48 has a basic complement of 10 attenuators (or potentiometers) and may be expanded to a full complement of 60 potentiometers.

Each Attenuator Group 42.283 provides five potentiometers for setting problem coefficients, initial conditions, and problem inputs. The potentiometers are mounted in up to 12 horizontal rows of five potentiometers per row. Each row is terminated at an individual patching area of the Pre-Patch Panel; space is provided for one potentiometer patching area per module of the Pre-Patch Panel. Four of the five potentiometers have one end grounded while the fifth has both ends ungrounded. (See Figure 2.4-1.)

The standard potentiometers in the TR-48 are 10 turn, wirewound, 5000 ohms, individually fused units with calibrated dials and a locking mechanism.

The potentiometer may be used in conjunction with reference to obtain a fixed accurate voltage less than reference, or to multiply a problem variable by any constant less than unity. Figure 2.4-2 is a schematic of a potentiometer with +10

volts applied to the high end*; the output at the wiper is k times +10, where k is:

$$k = \frac{R_1}{R_T} \qquad \text{(EQ. 2.4-1)}$$

The potentiometer shown in Figure 2.4-2 is unloaded, and the mechanical ratio of $R_1:R_T$ equals the electrical ratio $e_o:e_{in}$; thus, the potentiometer may be set to the exact ratio by means of the calibrated dial attached to the wiper shaft. However, the two ratios will not be equal when the potentiometer is loaded as is the case when it is used as a computer problem element. Normally, the pot is loaded by either a 100,000 (100K) or 10,000 (10K) ohms resistor since a potentiometer generally feeds an amplifier and these values are the most common amplifier input resistors. Figure 2.4-3 illustrates the effect on the $e_{in}:e_o$ and $R_1:R_T$ ratios when the potentiometer wiper feeds a 10K load.

In order to eliminate the effects of loading, it is more convenient to set the potentiometers under actual load and monitor the wiper voltage (the potentiometer output), than to calculate a corrected mechanical ratio ($R_1:R_T$).

Figure 2.4-4a and b illustrate the TR-48 circuitry provided to permit setting the potentiometers under actual load. Relay K1 is energized when the computer is placed in the pot set mode (depress PS button) and applies +10 volts reference to the Hi ends of all the grounded potentiometers. Note that the wiper remains connected to the Pre-Patch Panel termination; thus, the wiper "sees" the impedance of the actual load it is patched to in the problem. Even when the potentiometer is selected for monitoring via the readout system and K2 is energized, the wiper remains connected to its actual load. The readout system connects the wiper to a high impedance DVM (10 megohms minimum) or, in the absence of the DVM, a null pot circuit. The operator may then set the wiper for the attenuation factor required in the problem.

The method of setting the ungrounded potentiometers is similar except the +10 volt reference is not automatically applied to the potentiometer high end (relay K1 is eliminated on ungrounded attenuators). The operator must patch inputs to the potentiometer; this arrangement prevents possible erroneous settings depending on the configuration in which the potentiometer is used.

NOTE

Figure 2.4-5 shows schematics and symbols for the two types of potentiometer configurations. The TR-48 potentiometer designation (i.e., number) is given within the circular symbol and the setting is written in close proximity to the symbol. In addition, the Hi and Lo ends of the ungrounded potentiometer(s) are also designated to indicate clearly both input signal sources.

---

*The high (or hi) end of a potentiometer refers to the termination physically located at the top of the schematic designation of the Pre-Patch Panel. The low (or lo) end is the bottom termination, normally grounded except in the case of the ungrounded potentiometer.

TR48
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FIGURE 2.3-3 PLUG PLATE, REAR TR-48

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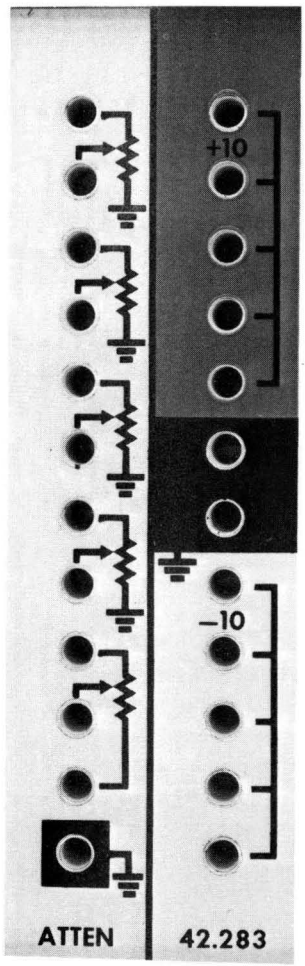
≠37



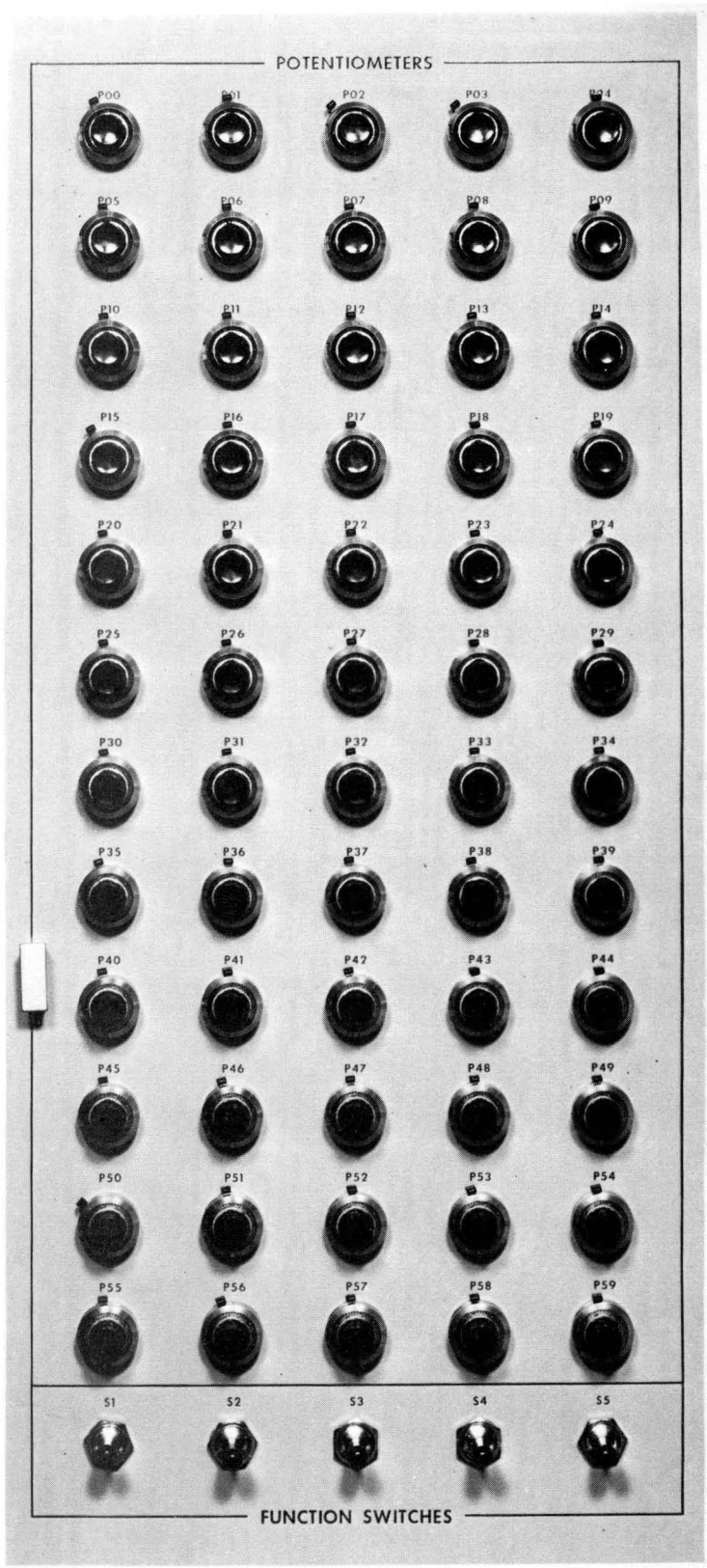


FIGURE 2.4-1 ATTENUATOR GROUP 42.283
PATCHING AREA AND POTENTIOMETER PANEL

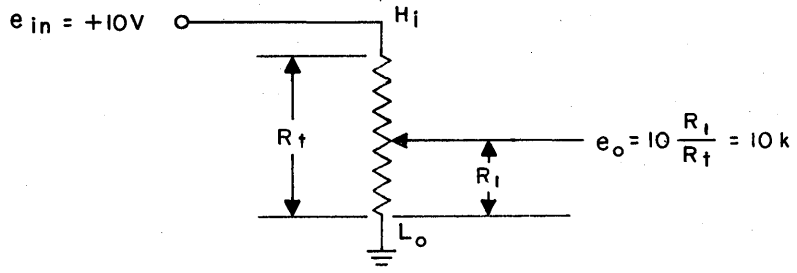
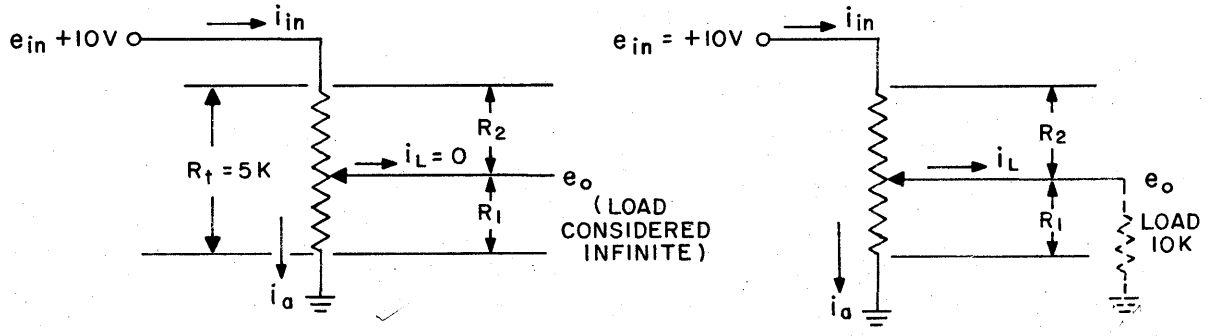


FIGURE 2.4-2. POTENTIOMETER SCHEMATIC SHOWING e_{in} TO e_o RELATIONSHIP FOR e_{in} = + 10 VOLTS.



(a) INFINITE LOAD: DIAL SET AT 0.800

$\therefore R_1 = 4K \quad R_2 = 1K$

$e_o = 10 - i_{in} R_2$

$i_{in} = i_L + i_a$

$i_{in} = i_a = 2$ ma. $\quad i_L = 0$

$\therefore e_o = 10 - 2\,(1) = 8$ VOLTS

$\frac{R_1}{R_t} = 0.800$ (AS SET BY DIAL)

$\frac{e_o}{e_{in}} = \frac{8}{10} = 0.8$

$\therefore \frac{R_1}{R_t} = \frac{e_o}{e_{in}}$

(b) 10K LOAD: DIAL SET AT 0.800

$\therefore R_1 = 4K \quad R_2 = 1K$

$e_o = 10 - i_{in} R_2$

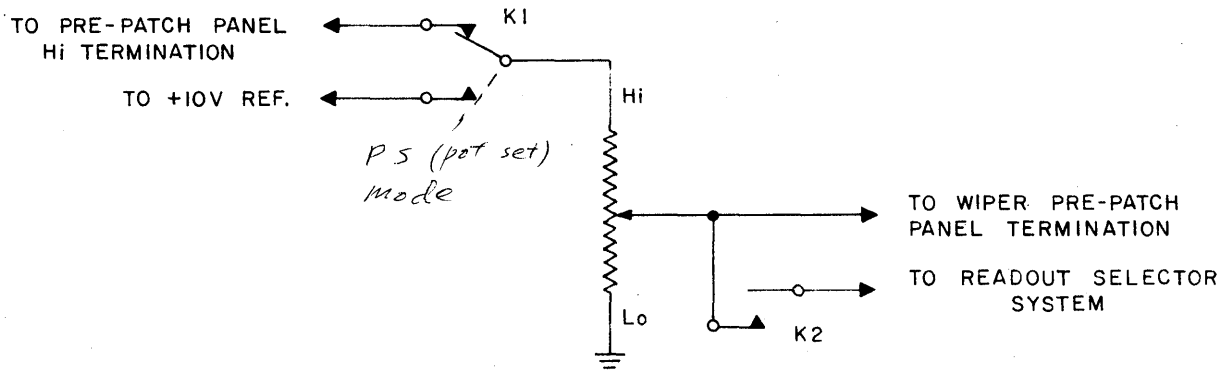
$i_{in} = i_L + i_a$

WITH 10K LOAD $i_{in} = 2.58$ ma.

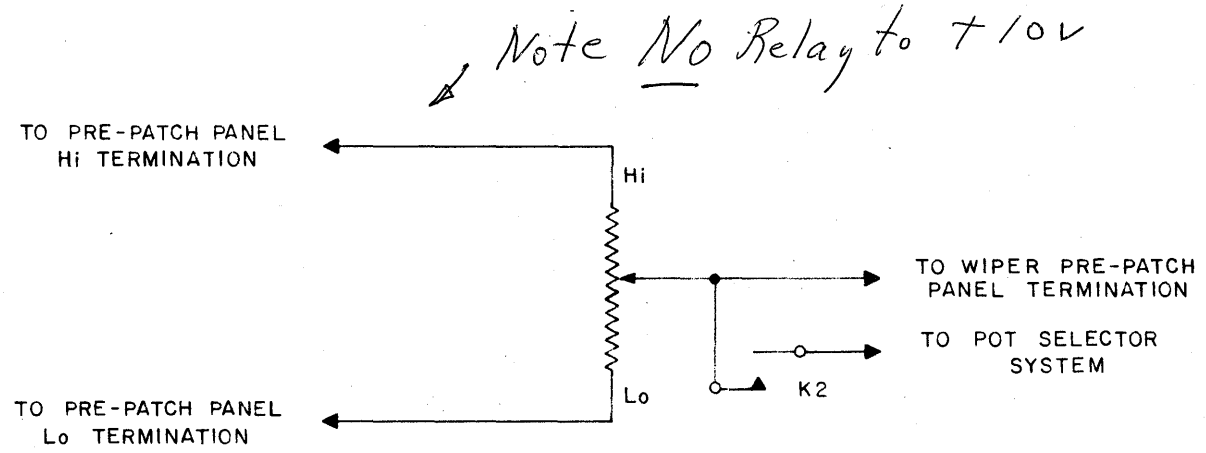
$\therefore e_o = 10 - 2.58\,(1) = 7.42$ VOLTS

$\frac{R_1}{R_t} \neq \frac{e_o}{e_{in}}$

FIGURE 2.4-3. POTENTIOMETER LOADING.

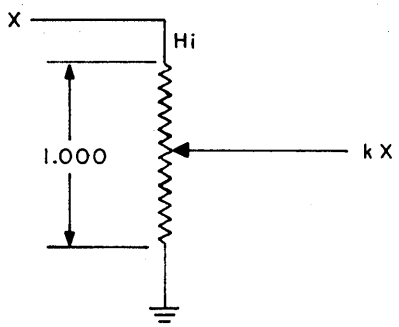


a. GROUNDED POTENTIOMETER CIRCUIT

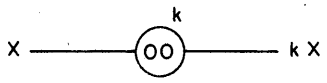


b. UNGROUNDED POTENTIOMETER CIRCUIT

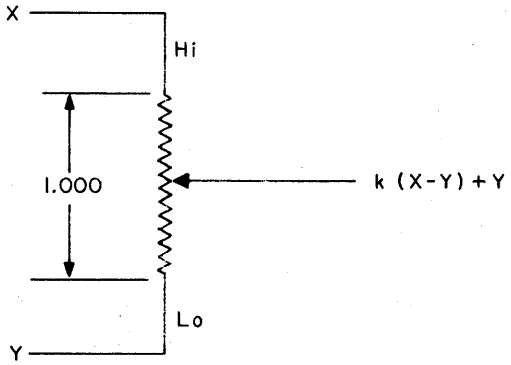
FIGURE 2.4-4. TR-48 POTENTIOMETER CIRCUITS, SIMPLIFIED SCHEMATIC



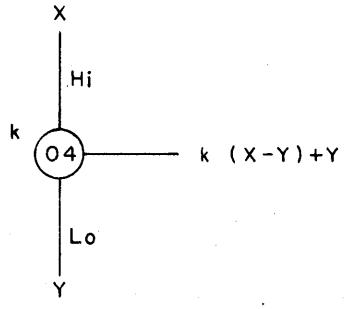
a. GROUNDED POT SCHEMATIC



b. GROUNDED POT COMPUTER DIAGRAM SYMBOL



c. UNGROUNDED POT SCHEMATIC



d. UNGROUNDED POT COMPUTER DIAGRAM SYMBOL

NOTE $k = \frac{e_o}{e_{in}}$

FIGURE 2.4-5. POTENTIOMETER SCHEMATIC AND COMPUTER DIAGRAM SYMBOLS

5. OPERATIONAL AMPLIFIER

a. General Considerations

When a high-gain d-c amplifier is used in conjunction with input and feedback networks to perform methematical operations, the resulting system is generally referred to as an operational amplifier. The operational amplifier is the basic and most versatile unit in the analog computer. It can be used for inversion, summation, multiplication by a constant, integration, and used in conjunction with special networks for squaring, extracting square root, generating logarithmic functions, etc.

To understand the basic concept of the operational amplifier, consider the simplified block diagram of Figure 2.5-1 where a high-gain amplifier (gain of -A) has a feedback impedance Z_f and an input impedance Z_{in}. The amplifier is designed so that it has three basic and essential characteristics.

(1) The amplifier output (e_o) is related to the summing junction voltage (e_b) by the gain of the amplifier: $\underline{e_o = -Ae_b}$

(2) The input stage of the amplifier draws negligible current: $\underline{i_b \approx 0}$

(3) The open loop gain of the amplifier is extremely high: $\underline{A \gg 1}$ (on the order of 3×10^7 at d-c).

Using Kirchhoff's laws, the nodal current equation at the summing junction (SJ) is:

$$i_{in} = i_f + i_b$$

or

$$\frac{e_{in} - e_b}{Z_{in}} = \frac{e_b - e_o}{Z_f} + i_b \qquad \text{(EQ. 2.5-1)}$$

since $e_b = -e_o/A$, and since $i_b \approx 0$, Equation 2.5-1 can be rewritten to obtain:

$$\frac{e_{in}}{Z_{in}} + \frac{e_o}{AZ_{in}} = -\frac{e_o}{AZ_f} - \frac{e_o}{Z_f}$$

Solving for e_o:

$$e_o = \frac{-\frac{Z_f}{Z_{in}}\, e_{in}}{1 + \frac{1}{A}\left[\frac{Z_f}{Z_{in}} + 1\right]} \qquad \text{(EQ. 2.5-2)}$$

In most applications the ratio of Z_f to Z_{in} is less than 30 and since 1/A approaches zero Equation 2.5-2 becomes:

$$e_o = -\left(\frac{Z_f}{Z_{in}}\right) e_{in} \qquad \text{(EQ. 2.5-3)}$$

Equation 2.5-3 illustrates one of the most important considerations of the operational amplifier: The input-output relationship of the operational amplifier is solely dependent on the ratio of the feedback to the input impedance.

Using Equation 2.5-3 as the basis of discussion, the following sub-paragraphs describe the various uses of the operational amplifier.

(1) Inversion. When the same value resistor is used for both the feedback and the input impedance, the amplifier output voltage has the same amplitude as the input voltage but is opposite in polarity.

$$e_o = -\frac{R_f}{R_{in}} e_{in}$$

In the TR-48 the value of R_f and R_{in} used for the inverter is normally 100,000 ohms, (100K) therefore:

$$e_o = -\frac{100K}{100K} e_{in} = -e_{in}$$

Thus a +10 volt input results in a -10 volt output, and the amplifier is said to have a gain of minus one. The accuracy of the output to input ratio depends solely on the accuracy of the ratio R_f/R_{in}.

(2) Multiplication by a Constant. A change in the ratio of the resistors results in multiplication by a constant. With R_f equal to 100K and R_{in} equal to 10K, for example, the amplifier output is:

$$e_o = -\frac{100K}{10K} e_{in} = -10e_{in}$$

An input of plus one volt results in an output of minus ten volts. This operational amplifier has a gain of ten. The multiplying constant can be made smaller than one by using a 10K feedback resistor with a 100K input resistor.

$$e_o = -\frac{10K}{100K} e_{in} = -0.1e_{in}$$

An input of minus ten volts produces an output of plus one volt.

(3) Summation. When multiple input resistors are used with a feedback resistor R_f, the basic relationship is extended to:

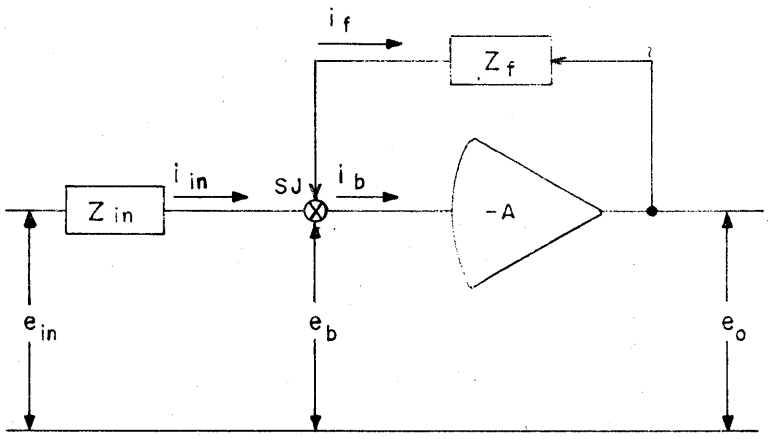
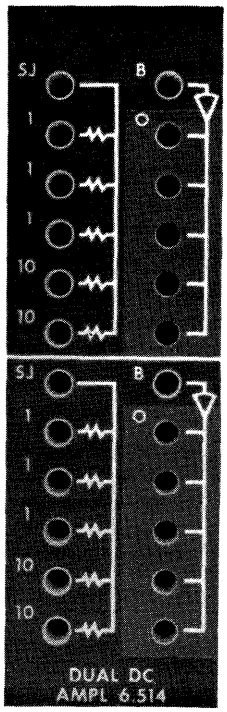
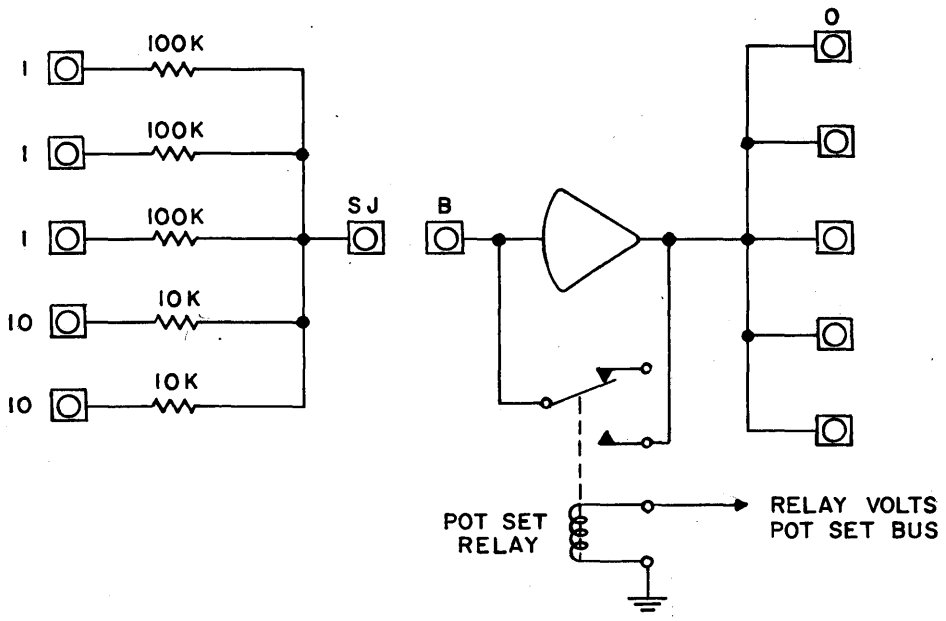


FIGURE 2.5-1. OPERATIONAL AMPLIFIER, SIMPLIFIED BLOCK DIAGRAM



b. PATCHING BLOCK



a. SIMPLIFIED SCHEMATIC OF 1/2 OF THE DUAL DC AMPLIFIER

FIGURE 2.5-2. TR-48 OPERATIONAL AMPLIFIER, SIMPLIFIED SCHEMATIC AND PATCHING BLOCK LAYOUT

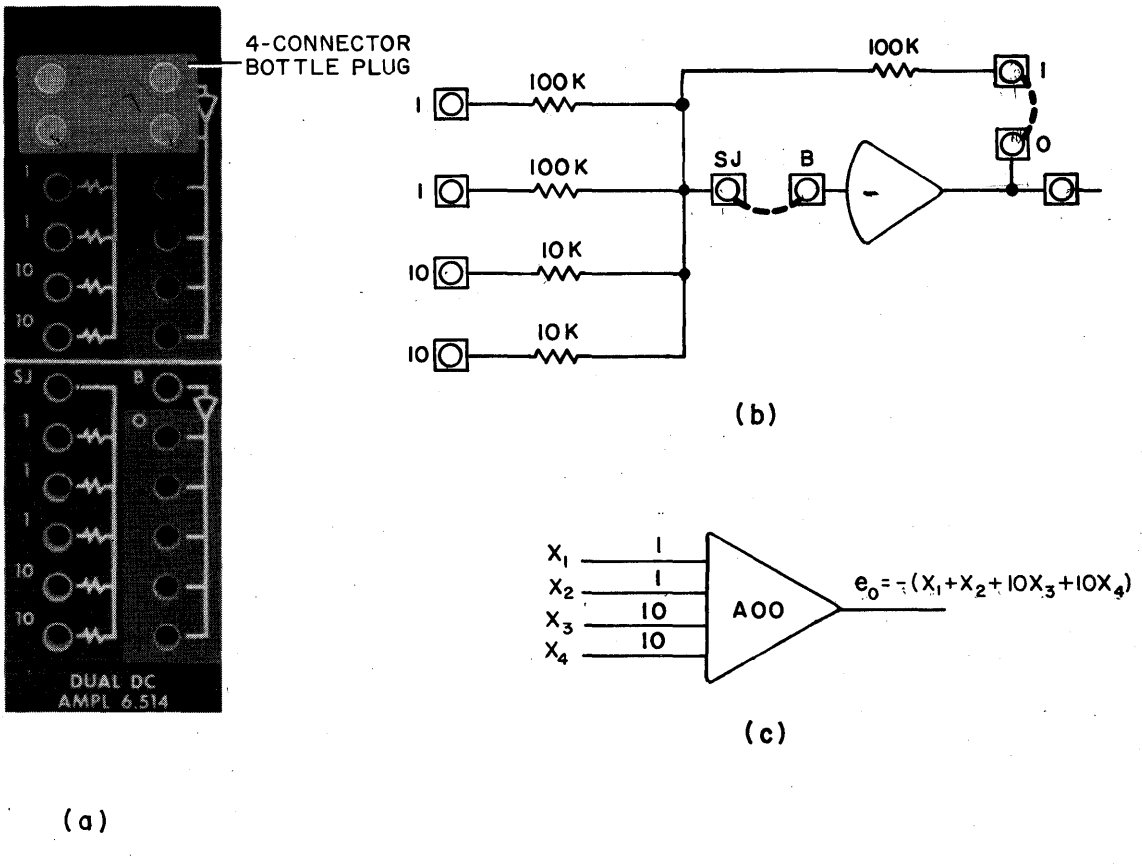


FIGURE 2.5-3. SUMMER AMPLIFIER PATCHING

$$e_o = -\left(\frac{R_f}{R_1} e_1 + \frac{R_f}{R_2} e_2 + \ldots + \frac{R_f}{R_n} e_n\right)$$

The circuit can be used to algebraically sum an indefinite number of inputs; furthermore, each input may be multiplied by an arbitrary constant.

(4) Integration With Respect to Time. When the feedback element Z_f is a capacitor rather than a resistor, the summing junction current equation is:

$$\frac{e_1}{R_1} + \frac{e_2}{R_2} + \ldots + \frac{e_n}{R_n} = -C\frac{de_o}{dt}$$

Integrating this equation and assuming an initial charge on the feedback capacitor of V_o:

$$e_o = -\frac{1}{C}\int_o^t \left(\frac{e_1}{R_1} + \frac{e_2}{R_2} + \ldots + \frac{e_n}{R_n}\right) dt + V_o$$

Looking at this another way, if Z_f is a capacitor having an operational impedance $1/pC$ and Z_{in} is a resistor, the basic operational amplifier relationship, Equation 2.5-3, becomes:

$$e_o = -\frac{E_{in}}{pRC} = -\frac{1}{RC}\int_o^t e_{in}\, dt$$

With this arrangement, the operational amplifier will integrate (with respect to time) any input voltage. In addition to integrating, the amplifier also inverts the input voltage. An indefinite number of inputs may be applied to produce the time-integral of the sum of the input voltages.

(5) Other Mathematical Operations. As previously indicated the operational amplifier has uses other than those indicated in sub-paragraph a through d. Complicated transfer functions can be simulated by using series and parallel RC networks for the feedback and input impedances. The circuit performance is still governed by the basic relationship of Equation 2.5-2. For the general case where three-terminal networks are used, the short-circuit transfer impedance of Z_f and Z_{in} must be used. (The short circuit transfer impedance of a network is the ratio of input voltage to short-circuit output current.) The input and feedback elements need not be linear; therefore, almost any non-linear characteristic can be approximated. The amplifier can also be used in conjunction with diodes and resistors to simulate the non-linear operations of limiting, dead-zone generation, X^2, Log X, etc.

b. TR-48 Operational Amplifier 6.514

Figure 2.5-2 shows the operational amplifier patching terminations and a simplified schematic of the high gain d-c amplifier and summing resistor network. By placing a four-connector bottle plug in the patching block as shown in Figure 2.5-3a, the high-gain amplifier is connected to the summing resistor network as shown in Figure 2.5-3b. The resultant operational amplifier can be used for inversion, multiplication by a constant, and summation. The computer diagram symbol is shown in Figure 2.5-3c. On the computer diagram it is customary to show only those inputs that are used; the amplifier number is written inside the triangular symbol.

Figure 2.5-4a shows the patching to provide an operational amplifier that is capable of integrating with respect to time. Figure 2.5-4b illustrates a simplified schematic for an amplifier patched as an integrator. The computer symbol for an integrator is shown in Figure 2.5-4c.

Figure 2.5-5 is an expanded schematic of the integrator amplifier. In addition to the terminations interconnected by the Tee-shaped bottle plug, certain circuits are brought out to the patching block for additional control of the integrators. These include the Operate and Reset relay coils and the operate and reset buses. Normally these terminations are connected as shown in Figure 2.5-4; however, by cross patching (operate bus to reset relay, etc.) the integrator can be used as a track and hold unit.

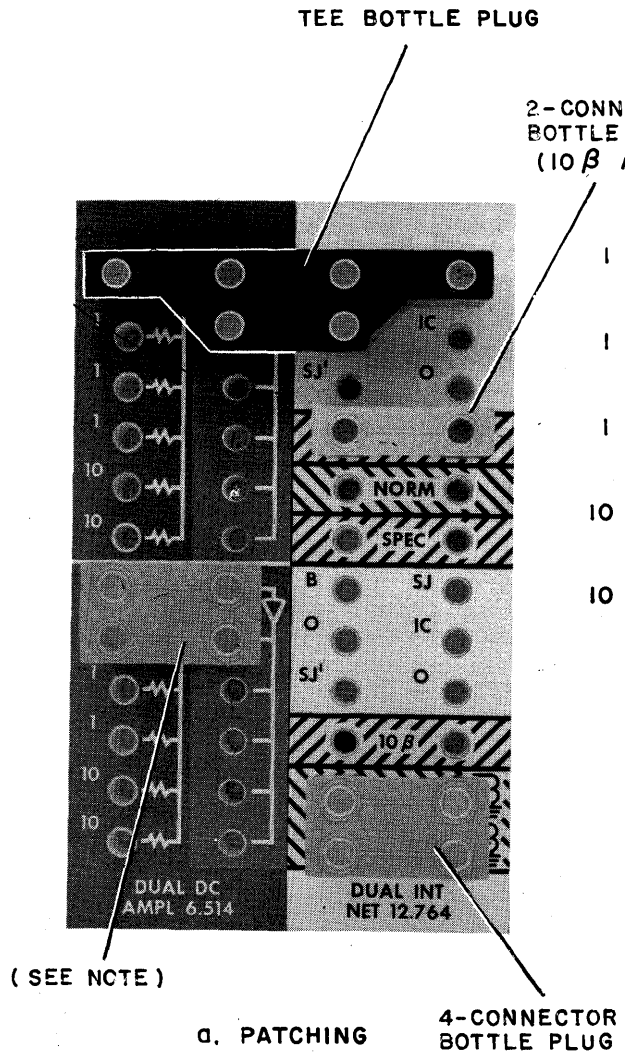
An additional feature is the 10β terminations; for normal operation these two terminations are jumpered by a two-connector bottle plug (Figure 2.5-4). This bottle plug parallels a 9 microfarad with a 1 microfarad capacitor (Figure 2.5-5) to produce an integrating rate of 10 volts/second for the gain-of-ten inputs and 1 volt/second for the gain-of-one inputs. By removing the 10β bottle plug the integrating rate can be increased by a factor of ten.

6. QUARTER-SQUARE MULTIPLIER

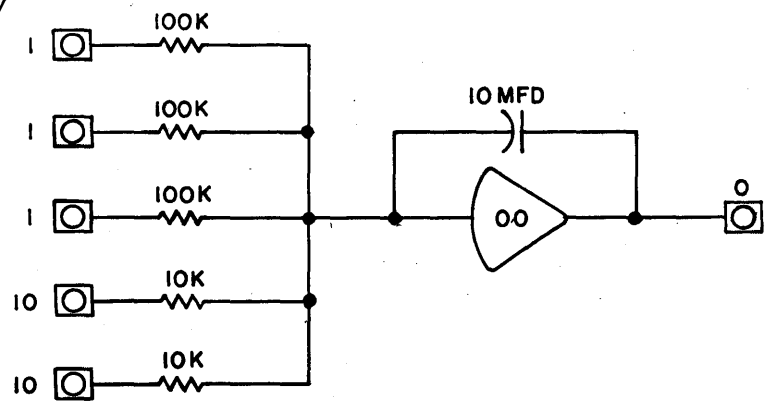
Multiplication of two variables is one of the non-linear operations necessary in a general purpose computer. The TR-48 Multiplier utilizes the quarter-square multiplication technique to produce a product of two variables (X and Y) as illustrated by the following equation:

$$XY = \frac{1}{4}\left[(X + Y)^2 - (X - Y)^2\right] \qquad \text{(EQ. 2.6-1)}$$

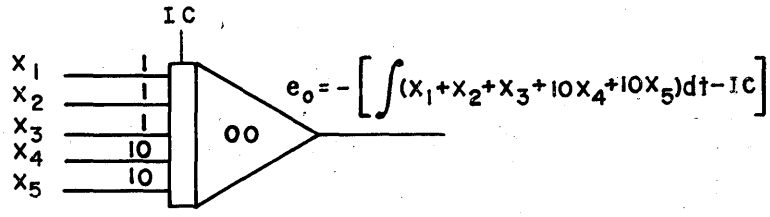
The TR-48 Quarter-Square Multiplier is basically a gated-resistor circuit application of the quarter-square technique. When the quarter-square multiplier is used as the input impedance Z_{in} for a high-gain d-c amplifier, the resultant circuit is capable of multiplication or squaring of input variables. When used as the feedback impedance, the multiplier-amplifier combination is capable of division or extracting the square root of the input variables. The quarter-square multiplier



a. PATCHING



b. INTEGRATOR SIMPLIFIED SCHEMATIC



c. COMPUTER DIAGRAM SYMBOLS

NOTE:
IF AMPLIFIER IS NOT USED, BOTTLE PLUG REQUIRED TO PROVIDE FEEDBACK.

FIGURE 2. 5-4. INTEGRATOR PATCHING AND DIAGRAMS

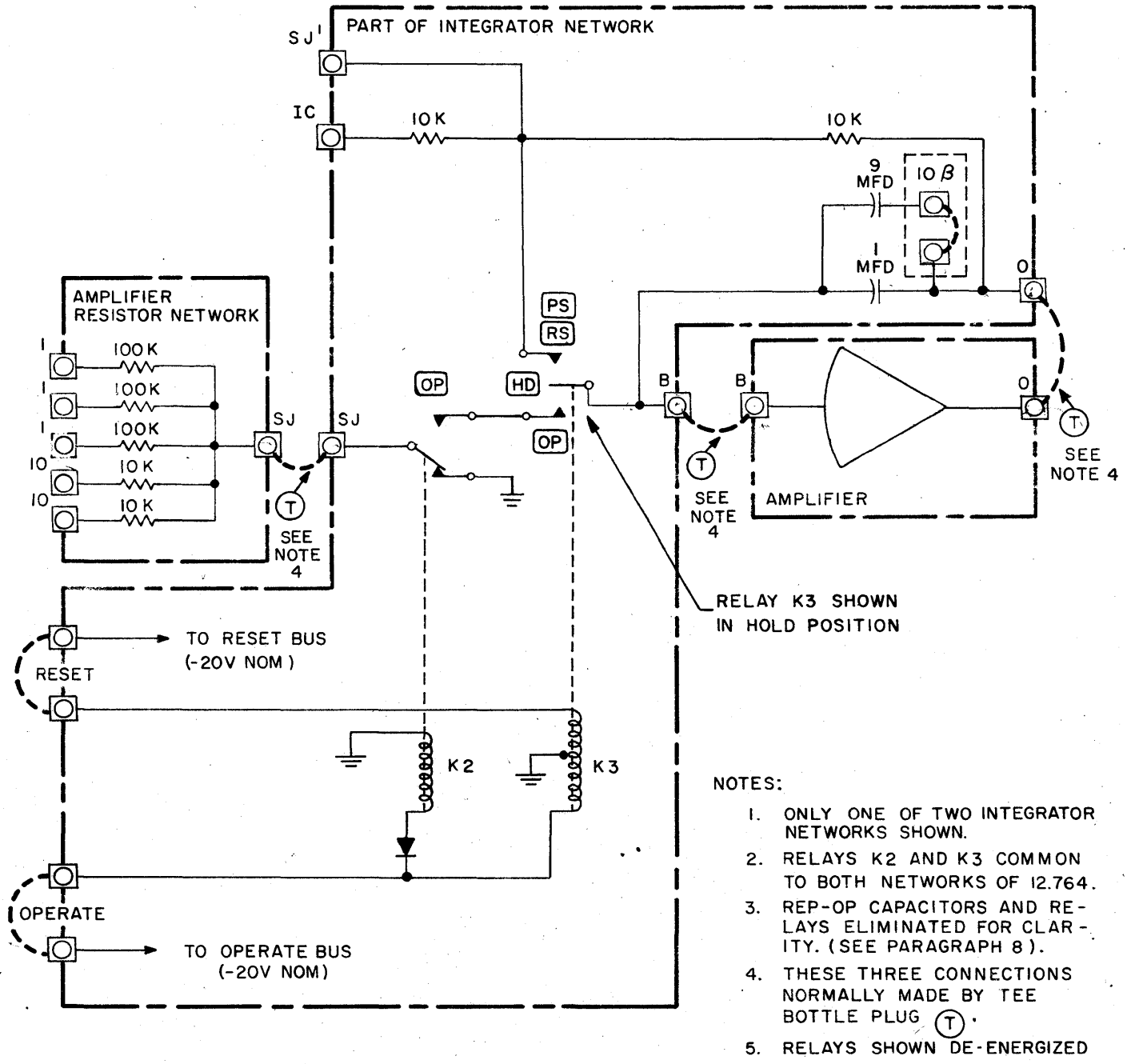
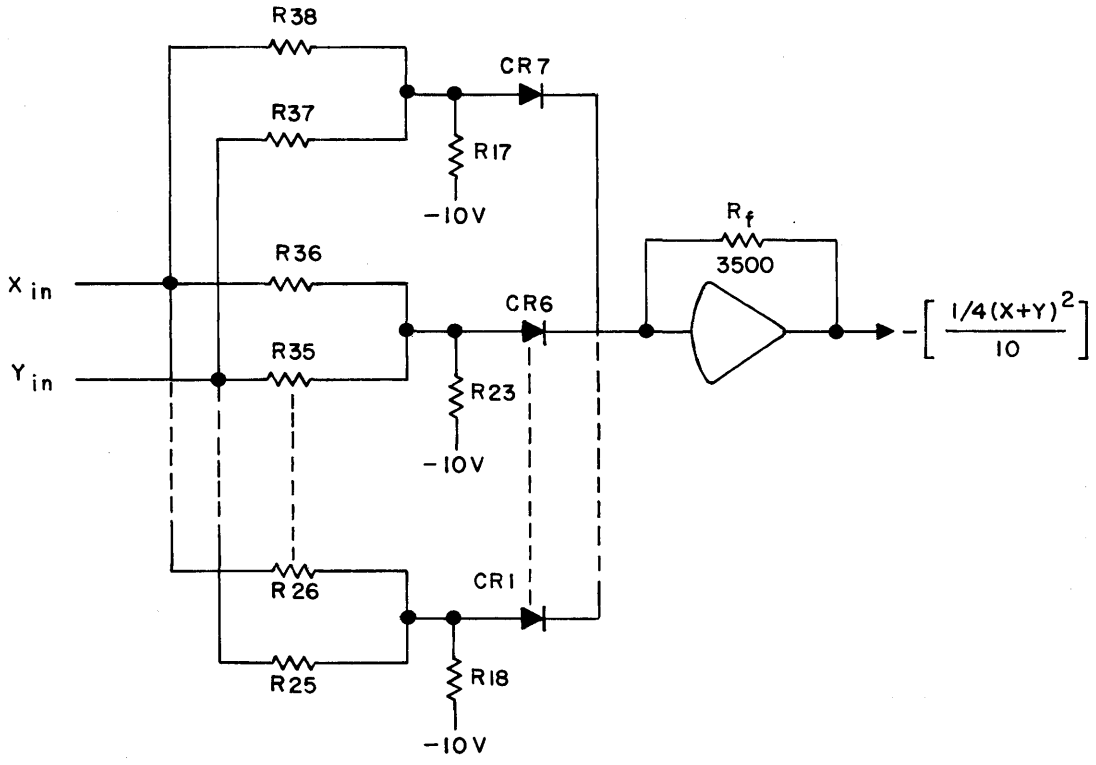


FIGURE 2.5-5 INTEGRATOR AMPLIFIER AND SIMPLIFIED SCHEMATIC



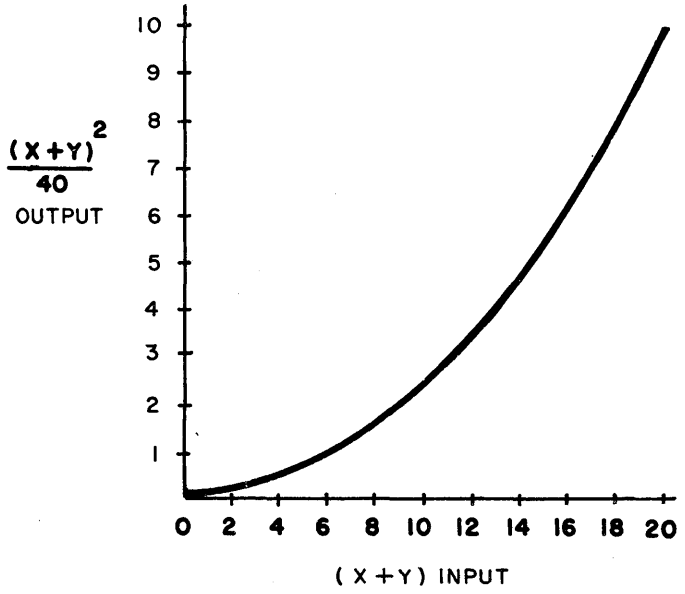


FIGURE 2.6-1. $(X+Y)^2$ SIMPLIFIED SCHEMATIC

employs four squaring circuits which utilize solid-state diodes and precision resistors to produce the square of a given input. Figure 2.6-1 is a simplified schematic typical of one of the four squaring circuits of the quarter-square multiplier. Each diode is reverse-biased (cut off) by the negative reference source at a potential dependent on the series resistance (R17, R23, etc.) in the reference source leg. To cause a given diode to conduct, the sum of the X and Y inputs (applied via weighted resistors) must attain a potential opposite in polarity and larger than the bias of the reference leg. By means of appropriate input resistors (R38 and R37, R36 and R35, etc.) and bias resistors (R17, R23, etc.) the diodes may be made to conduct at different predetermined values of (X + Y). (The potential at which a given diode conducts is known as the diode breakpoint.) As the input (X + Y) reaches the breakpoint of each diode, the input resistors are essentially paralled. The gain of the operational amplifier changes as each diode conducts; therefore, by proper selection of components, the network of Figure 2.6-1a can simulate a curve of $(X + Y)^2$ with straight-line segments, Figure 2.6-1b. The number of segments used determines the accuracy of the approximation.

In order to accomplish four quadrant multiplication, four squaring circuits are required.

Figure 2.6-2 is a simplified schematic of the quarter-square multiplier showing the patching terminations and the patching block area of the Pre-Patch Panel. For multiplication or division, a four-connector bottle plug is placed in the cross-hatched $\square\sqrt{}$ area; for squaring or extracting square root the four-connector bottle plug is moved up to the MD area. Note in each case the symbols left exposed indicate the functions that may be performed. On the simplified schematic the +Y inputs are designated $+Y_T$ and $+Y_B$ since they are common only when patched accordingly; these designations correspond to the +Y input in the upper field of the patching block and the +Y input in the lower cross-hatched area respectively. Resistor R_f is a 3550 ohm precision resistor available for use as an input resistor to the amplifier used in the multiplier circuit. This input may be used, for example, to produce $Z \pm XY/10$.

a. Multiplication

Figure 2.6-3 illustrates the patching procedure for multiplication of two variables, X and Y. All four input (+X, -X, +Y, and -Y) are necessary even though the inputs do not change sign during a problem run. Note that the output voltage from the associated amplifier is -XY/10 (due to the inversion of the amplifier). The +X and -X or +Y and -Y inputs can be interchanged to produce +XY/10.

b. Division

A variable (U) may be divided by a second variable (X) by using the quarter-square multiplier as the feedback element of a high-gain amplifier. Figure 2.6-4 illustrates the patching together with the simplified schematic for division with the quarter-square multiplier.

An important point to note with this circuit is that inputs to +X must be positive in polarity (negative input to -X) ie., the problem variable X, must be positive for division. If X is negative the +X and -X inputs should be interchanged.

Both +10 U/X and -10 U/X are available as outputs.

The following restrictions must be observed when using the quarter-square multiplier for division.

1. The absolute value of the divisor X must always be greater than or equal to the absolute value of the dividend U; i.e., $U/X \leq 1.0$.

2. The divisor X must be positive.

3. The divisor X must never equal zero.

The quarter-square multiplier may also be used to generate various other functions such as X^2 and $\sqrt{X}$. The patching and associated computer diagrams for various multiplier operations are given in Appendix 3.

7. DIODE FUNCTION GENERATORS

Four diode function generators (DFG's) are available for the TR-48. Three are of the fixed function type (X^2, Log X, and 1/2 Log X), and the fourth, a variable function type (VDFG), may be set to represent a single-valued function. All of the DFG's operate on a principle similar to the quarter-square multiplier; i.e., diode gates are reverse biased such that the input voltage must attain certain levels to cause succeeding diodes to conduct. As each diode conducts the Z_f/Z_{in} ratio of the operational amplifier is changed.

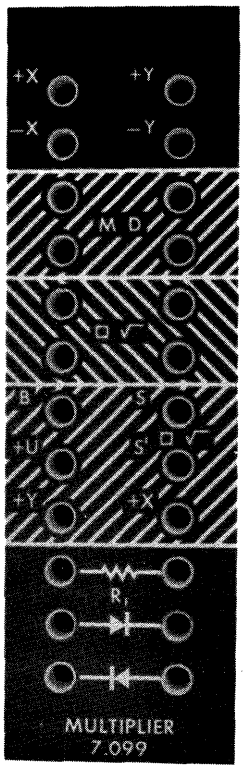
a. X^2 Diode Function Generator

The TR-48 X^2 DFG accepts both positive and negative input voltages and generates either a $+X^2$ or a $-X^2$ output. Figure 2.7-1 is a simplified schematic of the X^2 generator circuit showing the high-gain amplifiers as normally patched into the circuit. To generate a $+X^2$ function a four-connector bottle plug must be placed as shown in Figure 2.7-2a; this jumpers the four terminations associated with the $-X^2/10$ area of Figure 2.7-1; i.e., the two upper terminations are connected together as are the two lower terminations. For $-X^2$ the bottle plug is moved up as shown in Figure 2.7-2b. Note in each case the output function is designated by the exposed printing on the patching block. This feature enables the operator to determine the DFG output by glancing at the Pre-Patch Panel.

An additional feature, shown on Figure 2.7-2, is the R_1 input termination which provides an input with a gain-of-one via the amplifier connected between B_2 and O_2. The output; shown by Equation 2.7-1 is available when an input Y is applied to R_1.

$$\pm \frac{X^2}{10} \pm Y \qquad \text{(EQ. 2.7-1)}$$

TR48
57



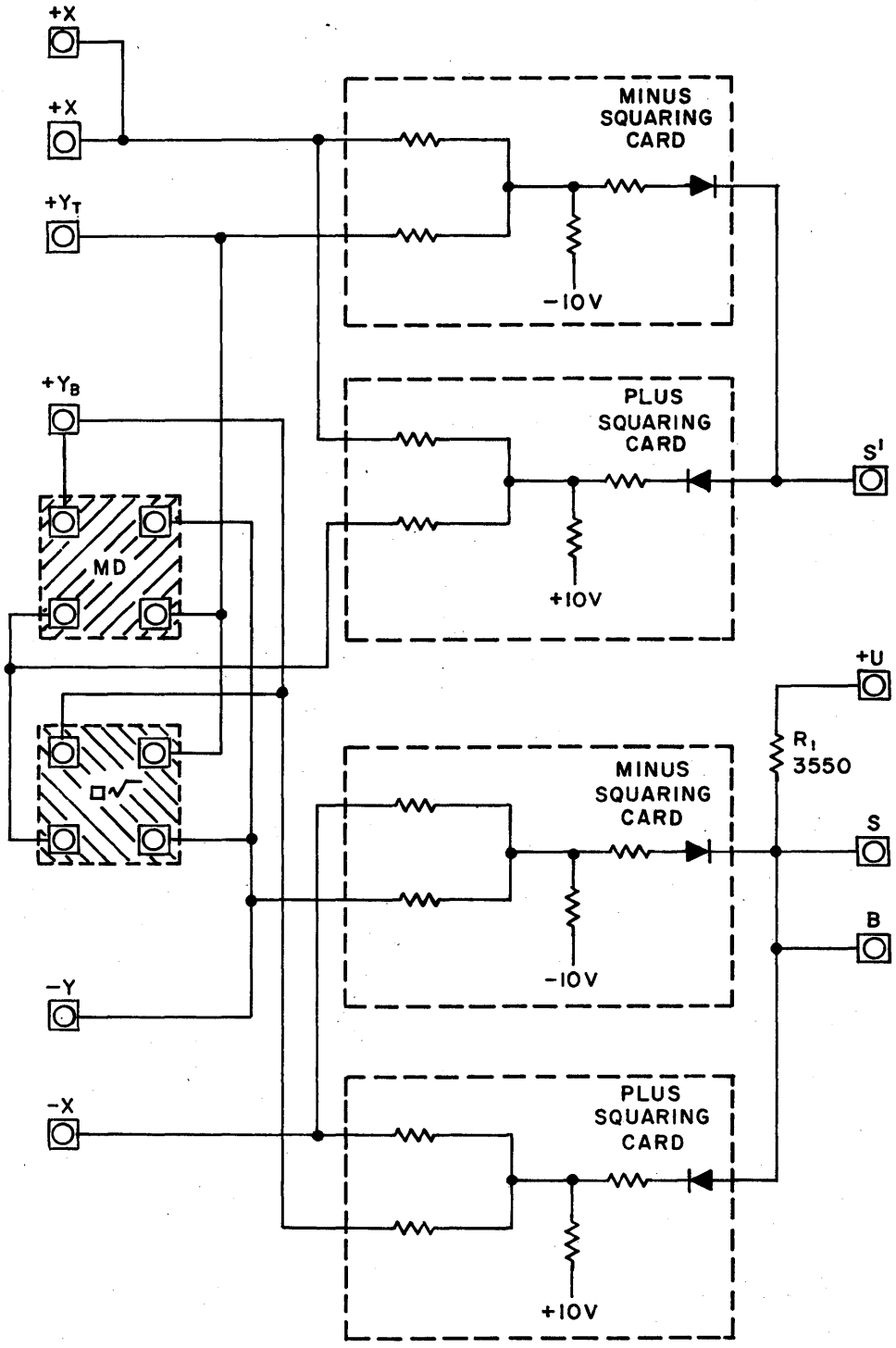


FIGURE 2.6-2. QUARTER-SQUARE MULTIPLIER, SIMPLIFIED SCHEMATIC AND PATCHING BLOCK

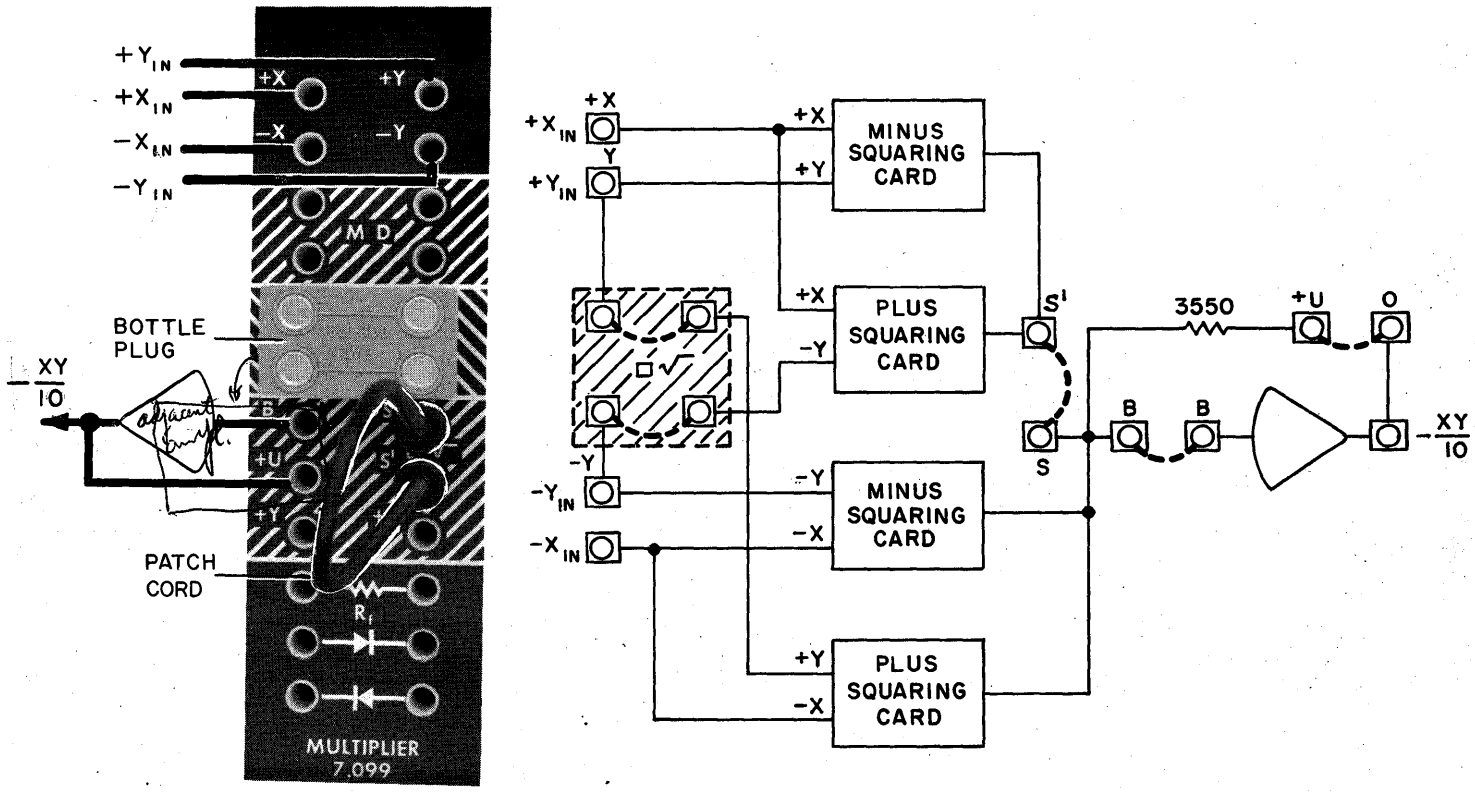
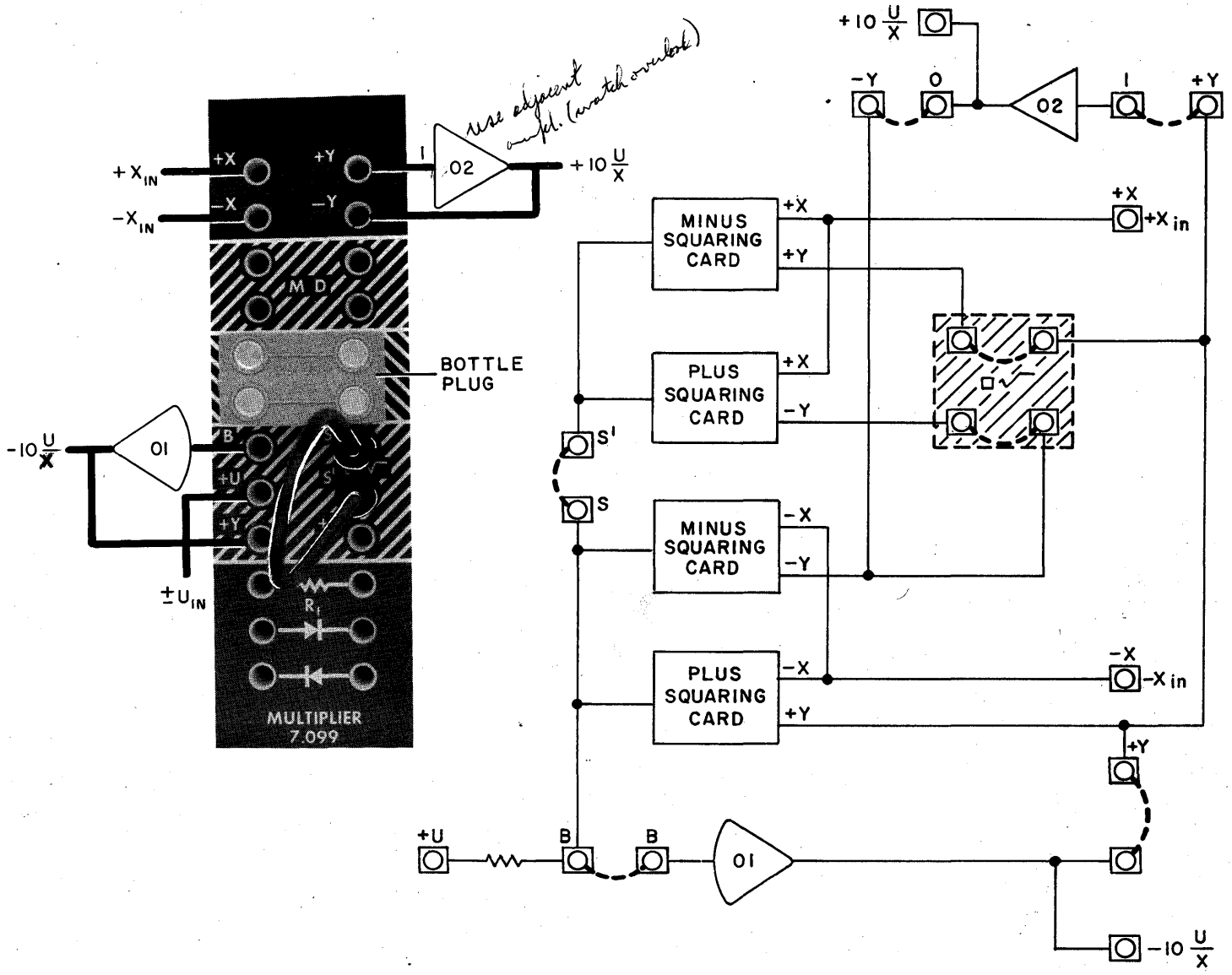


FIGURE 2.6-3. MULTIPLICATION PATCHING AND SIMPLIFIED SCHEMATIC



NOTES:

1. $X \geq U$
2. $X \neq 0$
3. X MUST BE POSITIVE (IF X IS NEGATIVE, INTERCHANGE THE +X AND −X CONNECTIONS; THE OUTPUTS OF AMPLIFIERS 02 AND 03 BECOME $-10\frac{U}{X}$ AND $+10\frac{U}{X}$ RESPECTIVELY)

FIGURE 2.6−4. DIVISION PATCHING AND SIMPLIFIED SCHEMATIC

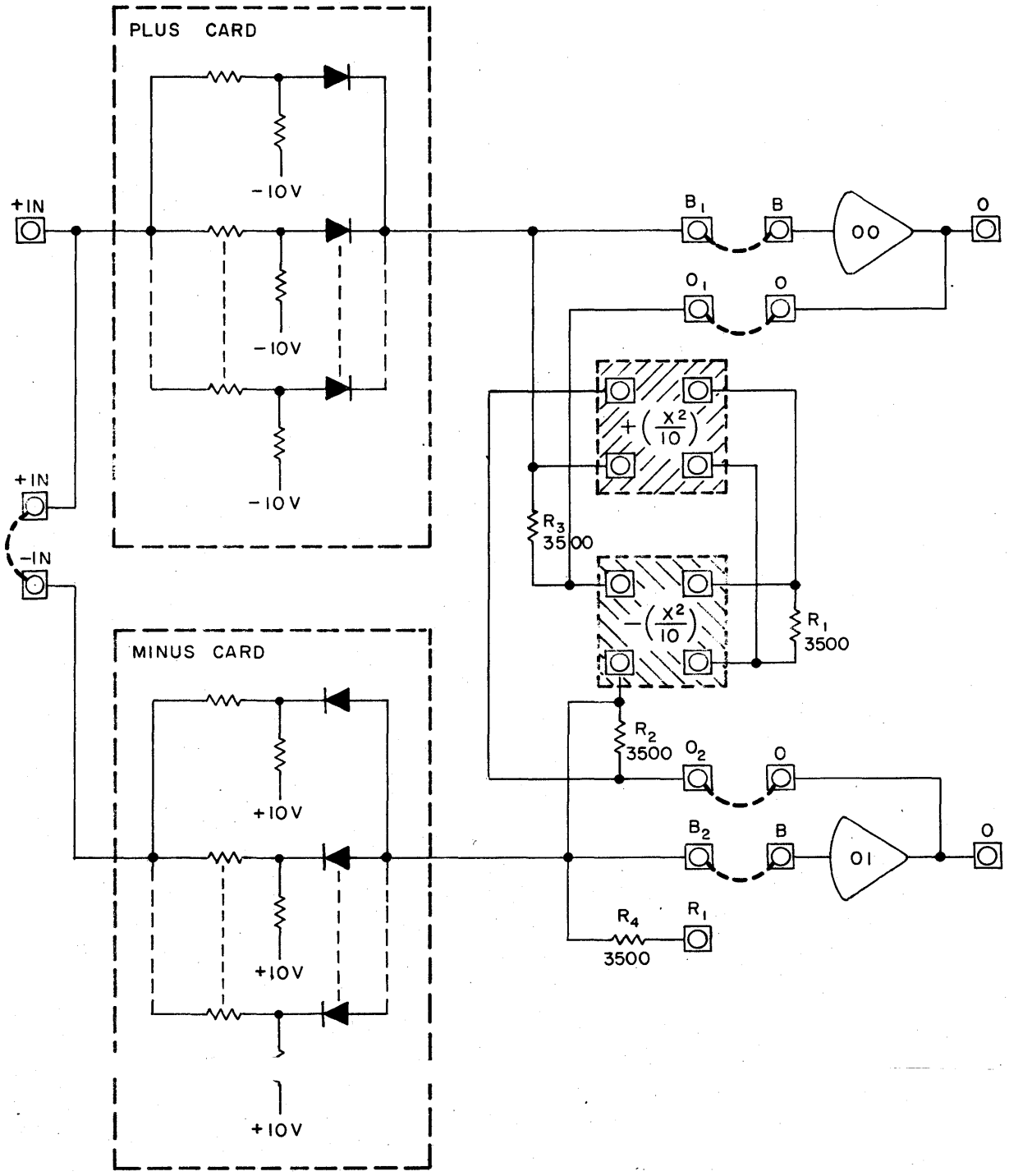
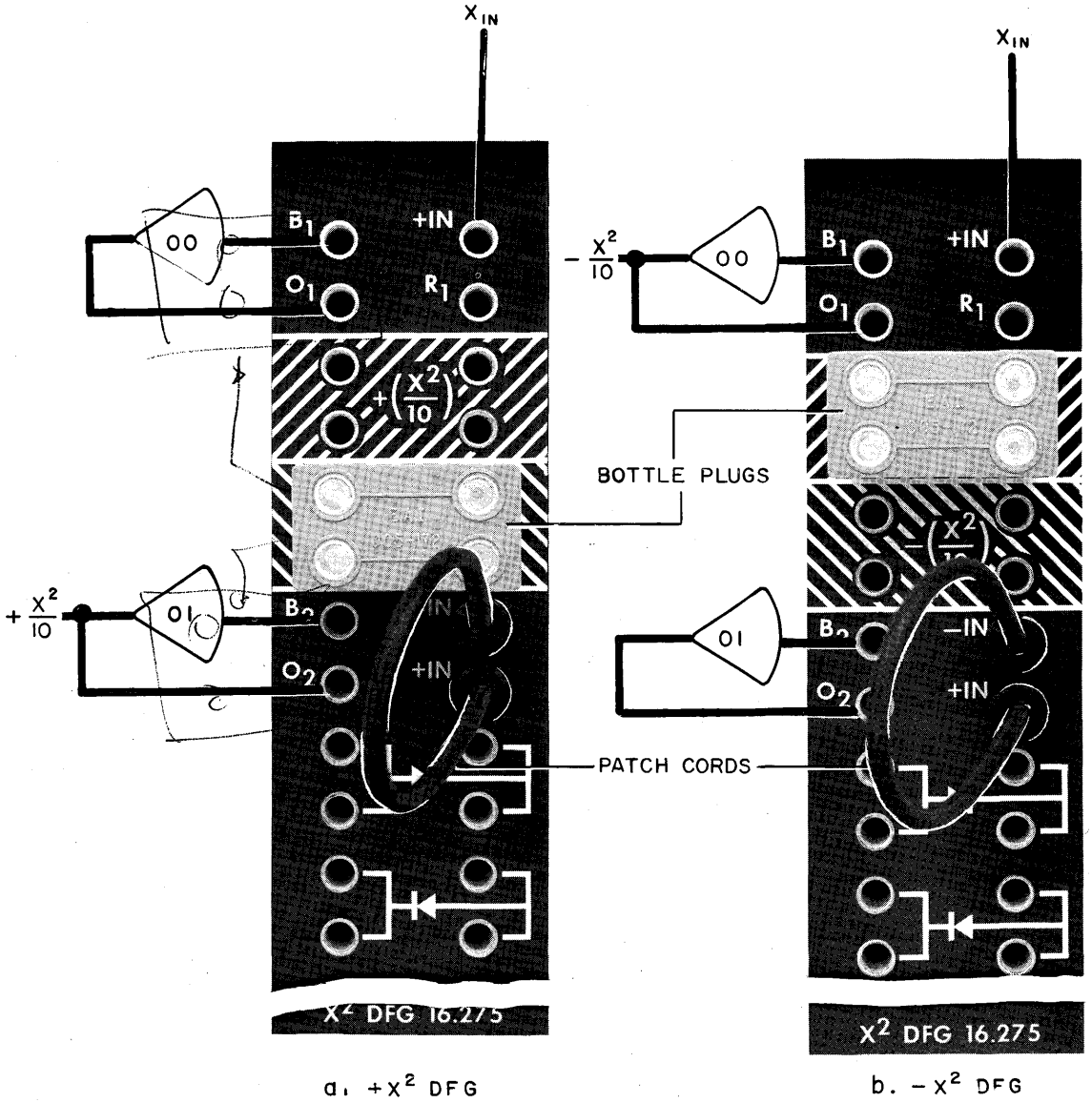


FIGURE 2.7-1. X^2 DFG SIMPLIFIED SCHEMATIC

TR48
#63,64



a. $+X^2$ DFG

b. $-X^2$ DFG

FIGURE 2.7-2. X^2 DFG PATCHING

This entire quantity must be appropriately scaled to prevent amplifier overload.

Additional functions (such as $\sqrt{X}$ or $X^2/10$ for limited inputs) are also obtainable with the X^2 DFG. The patching and computer diagrams are given in Appendix 4.

b. Log X Diode Function Generator

The TR-48 Log X DFG contains four individual log function generators all of which are terminated at the Pre-Patch Panel. Two of the generators accept only positive voltage inputs and two accept only negative voltage inputs. The output of the generators is the scaled logarithm to the base 10 (i.e., $5 \log_{10} [10|X|]$).

Figure 2.7-3 illustrates the patching for both positive and negative voltage input log X generators. Additional patching and DFG uses (such as obtaining the antilog of a log input, multiplication, division, or raising an input to an unusual power) are given in Appendix V.

c. 1/2 Log X Diode Function Generator

The 1/2 Log X DFG is similar in theory of operation, patching, and function generation to the Log X DFG. The difference lies in the output function: the 1/2 Log X DFG generates the log of the $\sqrt{X}$ (i.e., $2.5 \log_{10} [10|X|]$).

d. Variable Diode Function Generator

Frequently in a problem, the dependence of one variable quantity (Y) on another quantity (X) is known only in the form of experimentally obtained data. The variable Diode Function Generator (VDFG) provides a means, with a single component of approximating and generating functions of this type.

The TR-48 VDFG utilizes the same technique as the Log X, 1/2 Log X, and X^2 DFG's; i.e., the VDFG is used to vary the Z_f to Z_{in} relationship of the operational amplifier as a function of the input voltage to approximate a curve with straight line-segments. With the VDFG the operator can control only the line-segment slopes since the breakpoints (i.e., the beginning of each straight line segment) are fixed at 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9 volts.

The TR-48 VDFG consists of two VDFG's: a negative generator that responds to in-

zero to +10 volts. The positive and negative VDFG's can be used separately or combined to form a ±VDFG for both positive and negative voltage inputs.

(1) Patching and Simplified Schematics. Figure 2.7-4 shows the VDFG patching area and the simplified schematic of the overall unit; the plus and minus VDFG portions show only a single diode-gated resistor circuit for clarity. Figure 2.7-5 shows the patching for using the plus and minus VDFG's separately; this figure also contains a simplified schematic of the plus VDFG. The minus VDFG is similar except that the diodes are orientated in the opposite sense and are biased by plus reference.

Figure 2.7-6 shows the VDFG patching to combine the plus and minus VDFG's for bi-polar inputs. Note that a four-connector bottle plug covers the 10 SEG area of the patching block; one of the +IN terminations is jumpered to a -IN termination to combine the input leads.

(2) Set Up Procedure. The VDFG units are located behind the Control Panel as shown in Figure 2.7-7. They are individually mounted on sliding shelves thus facilitating access to the slope potentiometer controls.

Each VDFG unit has eleven adjustments; one is a parallax control and the other ten are slope potentiometers to adjust the output curve slope between unitary incremental inputs of X. When used in the ±VDFG combined mode the parallax pots of the -VDFG and +VDFG are interdependent.

The parallax potentiometer permits the operator to set the value of Y (at X = 0) within the range of +10 to -10 volts. The +1 slope adjustment permits the operator to set the initial line segment slope between 0 and 1 volt so that with 1 volt into the DFG, the Y output can be set to a voltage between ±2 volts above or below the X = 0 point (i.e., a slope of 2 volts/volt). The remaining slope potentiometers (2 to 10) permit the operator the change the slope of each preceding segment by a voltage slope of one volt per volt.

Figure 2.7-8 is a sample output curve of a plus VDFG. This curve is used as the basis for the typical VDFG set-up procedure.

The following procedure is for the set-up of a +VDFG patched as shown on Figure 2.7-5. The set-up adjustments of the +VDFG must be started at X = 0 and continued in sequence to X = +10. The procedure for the -VDFG is accomplished in a similar manner, again starting at X = 0 and in sequence to X = -10.

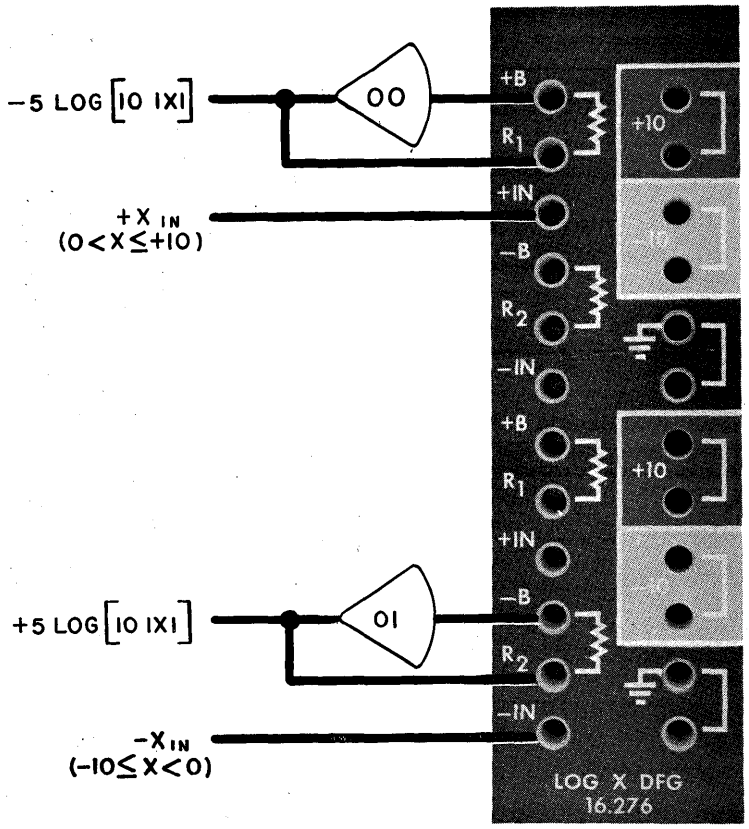
When setting up a VDFG for combined plus and minus inputs the operator again starts at X = 0. Once the X = 0 point is set (parallax potentiometer) the operator must proceed in sequence to either +10 or -10 on one VDFG, then starting again at zero, proceed in sequence to the limit of the remaining VDFG.

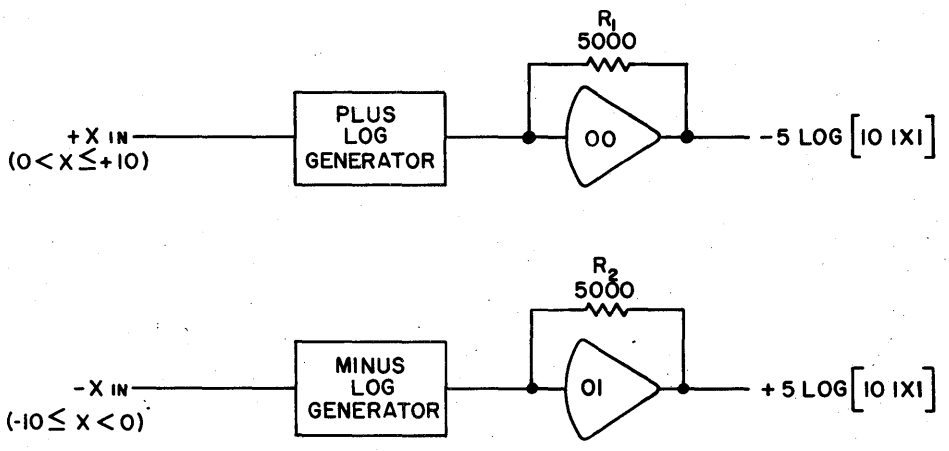
(3) Typical VDFG Set-Up Procedure

(a) Release the quarter-turn locking device and slide the desired +VDFG forward exposing the set-up controls.

(b) Select the Y = f(X) amplifier output (designated 01 on Figure 2.7-5) for readout on the DVM (or multi-range voltmeter if the DVM is not available).

(c) Ground the +IN termination of the VDFG. Using a small-blade screw driver set the PARALLAX control for a DVM readout of -2 volts.



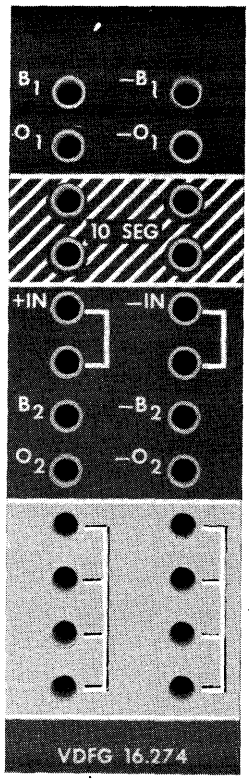


NOTES

1. R_1 AND R_2 5000 OHMS IN ALL CASES.
2. OUTPUTS ARE LOG TO BASE 10

FIGURE 2.7-3 LOG_{10} X DFG PATCHING AND SIMPLIFIED SCHEMATICS

TR-48
50



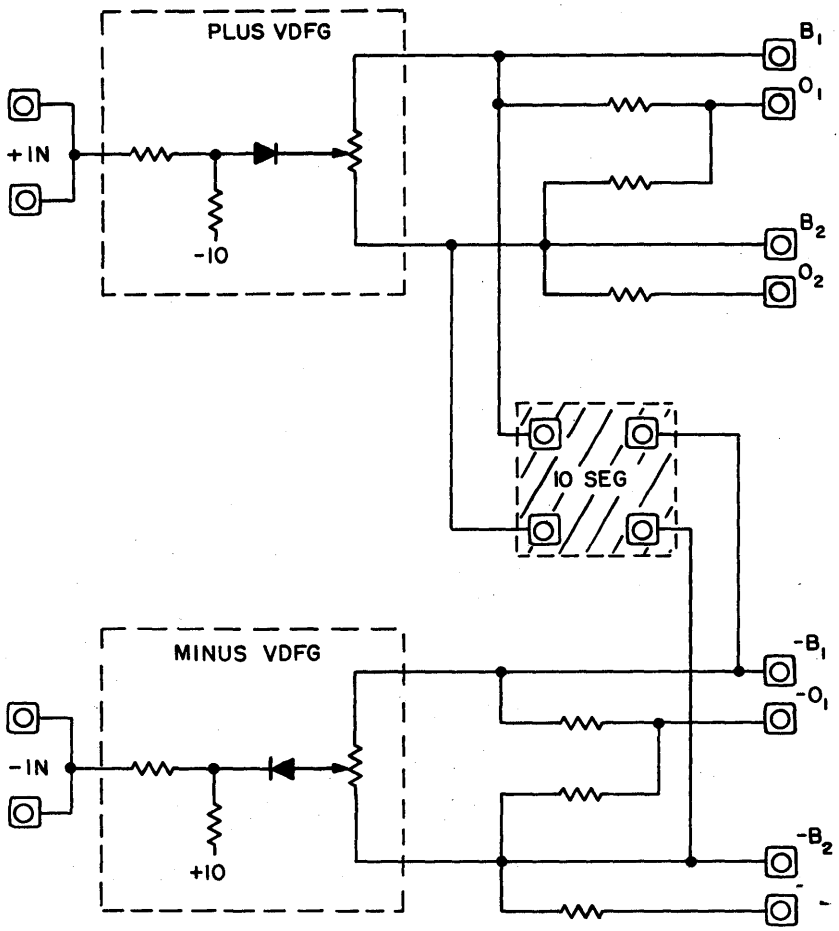
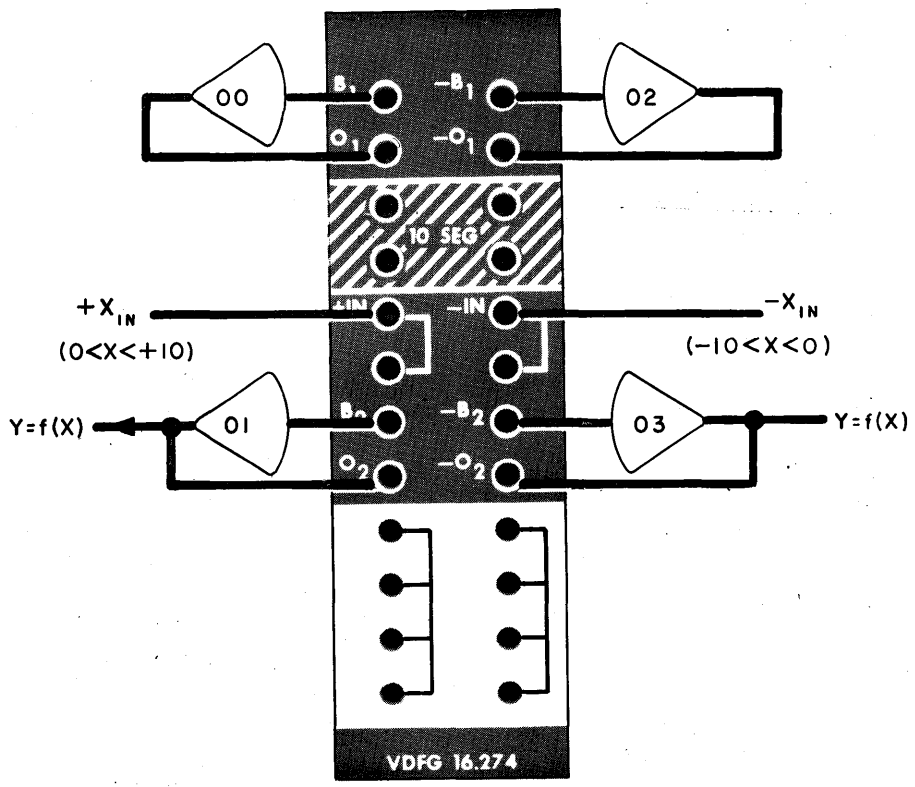
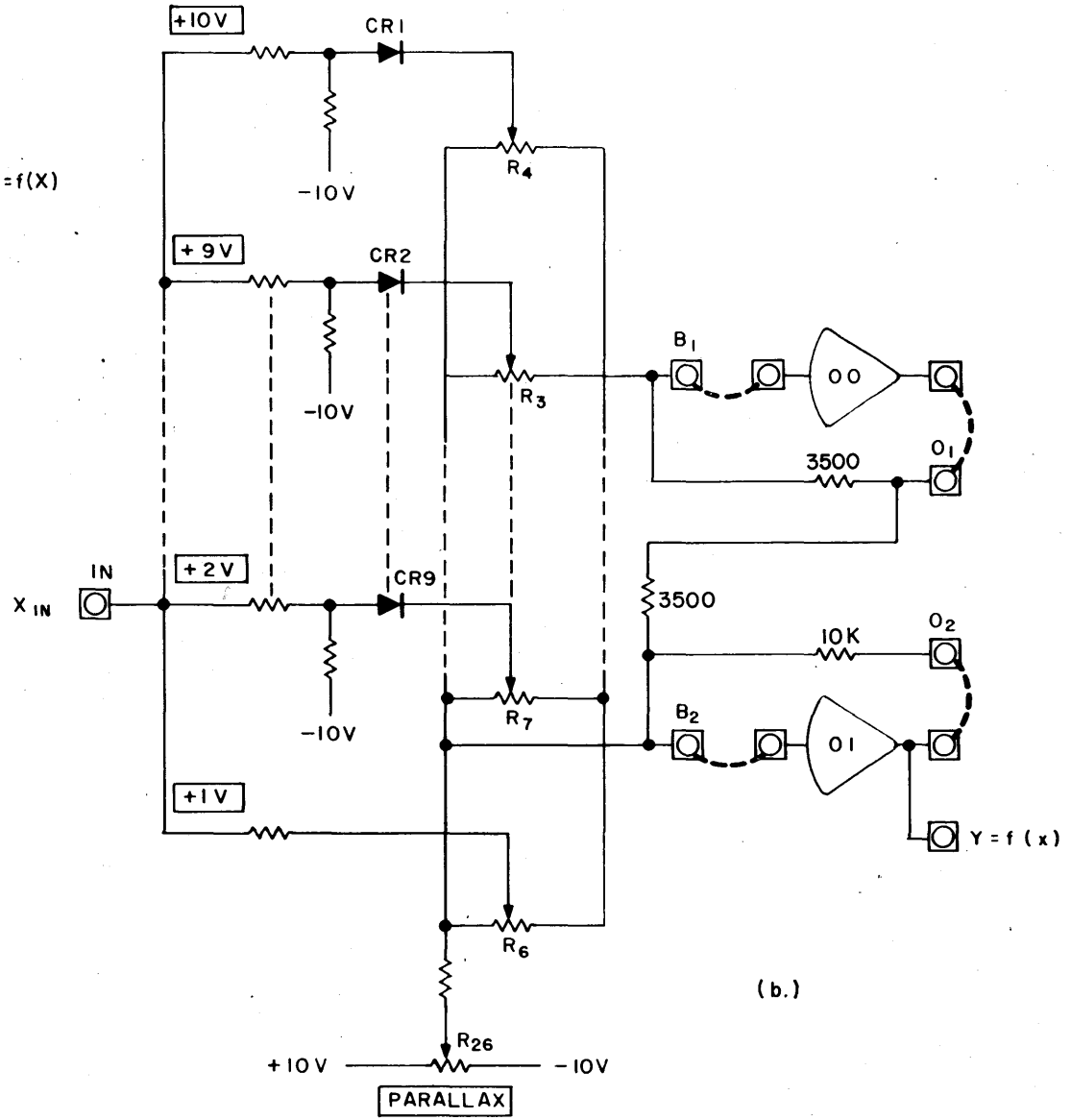


FIGURE 2.7-4 VDFG PATCHING BLOCK AND SIMPLIFIED SCHEMATIC



(a.)



(b.)

FIGURE 2.7-5. +VDFG AND -VDFG PATCHING AND +VDFG SIMPLIFIED SCHEMATIC

TR48
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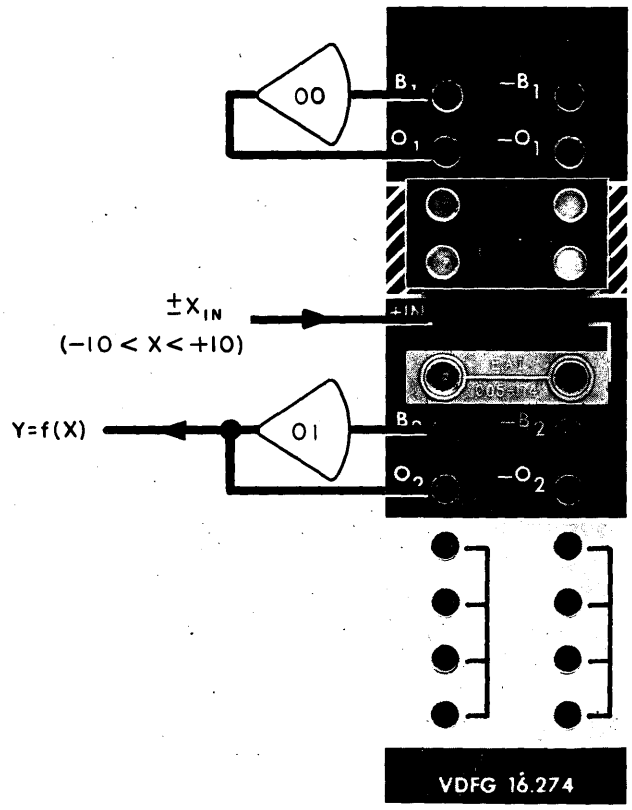
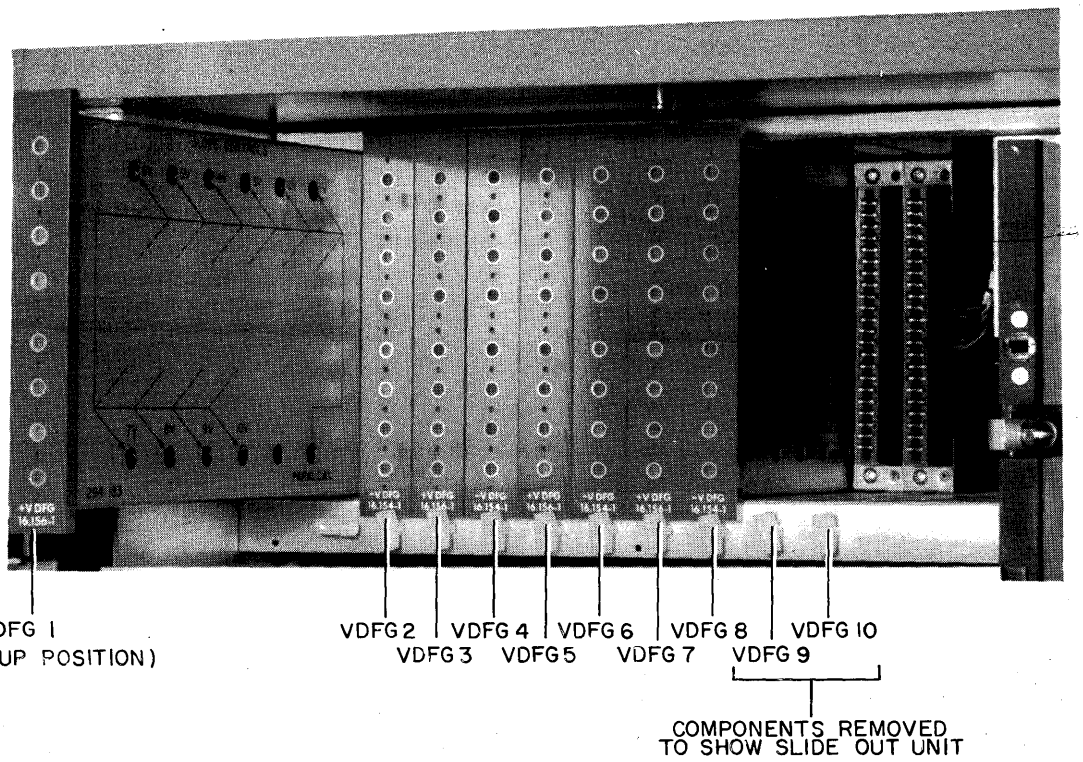
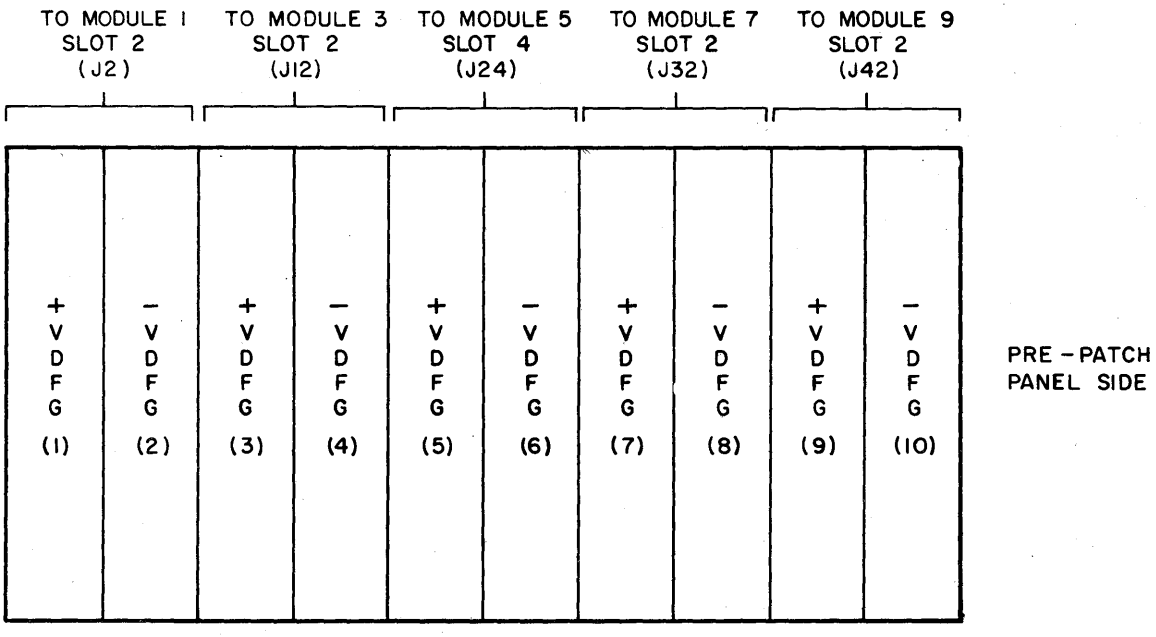


FIGURE 2.7-6. $\pm$ VDFG PATCHING

TR 48
82

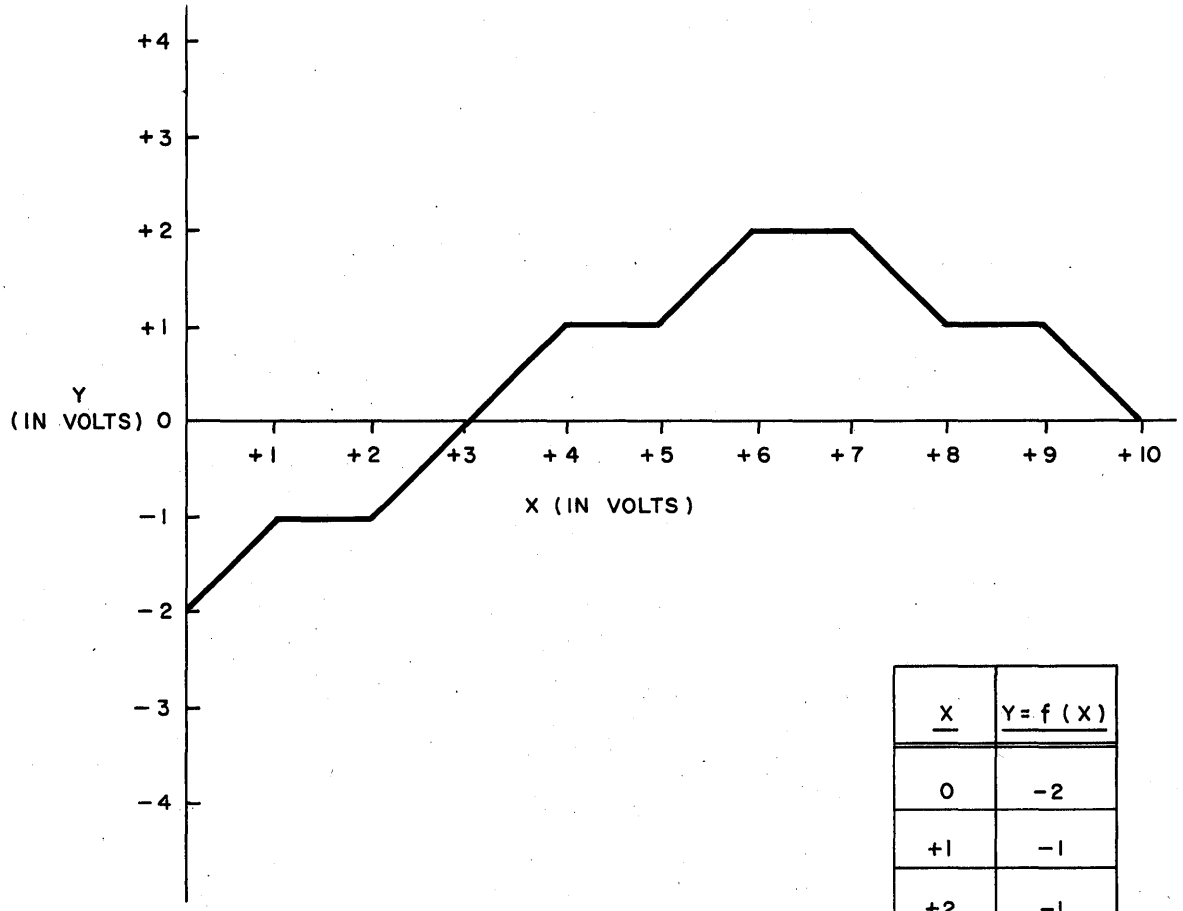


a. VDFG UNIT LOCATION



b. VFDG LOCATIONS AND ASSOCIATED PRE-PATCH PANEL AREAS

FIGURE 2.7-7 ± VDFG UNIT LOCATION SHOWING CHASSIS IN SETUP POSITION



X	Y = f (X)
0	-2
+1	-1
+2	-1
+3	0
+4	+1
+5	+1
+6	+2
+7	+2
+8	+1
+9	+1
+10	+0

FIGURE 2.7-8. SAMPLE +VDFG OUTPUT CURVE

(d) Apply +1 volt to the +IN termination and adjust the +1 control for a DVM readout of -1.

(e) Apply +2 volts to +IN. Adjust the +2 control for -1.

(f) Continue the procedure applying X = +3, +4, etc., and adjusting the corresponding control for the proper DVM readout as listed in the table.

(g) For optimum accuracy repeat the set-up procedure, starting with Step (c), and making any necessary touch up adjustments.

8. REPETITIVE OPERATION (REP-OP)

The addition of the high-speed repetitive operation feature to the TR-48 provides a means of rapidly switching the computer integrators between the initial condition (or reset) and operate modes at controlable rates up to 50 cycles per second. The computer can be switched from manual to repetitive operation without requiring changes to the computer program.

Figure 2.8-1 is a simplified schematic of an integrator showing the Rep-Op capacitors and the Time Scale relay. Energizing the Time Scale relay K1, the feedback capacitor is changed from 10 microfarads to 0.02 microfarads, thus changing the integrator time scaling by a factor of 500. By terminating the time scale bus and relay K1 at the Pre-Patch Panel, the operator can use iterative techniques in problem solution by operating desired integrators at "real time" rates even though the computer is in the Rep-Op mode.

Essentially, the Rep-Op mode, with the time scaling and rapid switching between the integrator reset and the operate modes, a problem is solved, reset, and then solved again; this process continues repetitively at the pre-set rate. The Rep-Op circuits also provide a saw-tooth sweep voltage at the selected Rep-Op rate, suitable for driving an external oscilloscope. Thus, the problem solution may be displayed on an oscilloscope that is synchronized with the Rep-Op cycling rate. The sweep voltage is terminated in the yellow scope area of Readout Panel 12.763 of the Pre-Patch Panel. (See Figure 2.3-2a.) By connecting a bottle plug between the sweep termination (⏜) and the scope X termination of the 12.763 area, the sweep voltage is applied to the scope connector plug on the rear of the TR-48 (Figure 2.3-3).

To place the computer in the Rep-Op mode the operator sets the desired rate on the REP-OP COMPUTER TIME control located on the control panel. This is a dual control; the outside portion is a four position switch for selecting operate times of 20, 50, 100, or 200 milliseconds per cycle. The inside control (VERNIER) permits the expansion of these four settings up to 2.5 times. The control is calibrated so the 20, 50, 100, and 200 settings are accurately obtained when the VERNIER is turned fully counter-clockwise.

After setting the desired repetition rate, the computer is switched into the Rep-Op mode by depressing the RO button on the control panel. Only those integrators

with a jumper between the TS bus and relay K1 respond to the Rep-Op drive signals.

9. COMPUTATIONAL ACCESSORIES

In addition to the standard computing elements, certain devices are found useful in programming a problem on the computer. These items are used as required by the programmer to expand the computer capabilities.

a. Signal Comparator 40.404

The signal comparator is an automatic switching device that consists of a comparator amplifier and a double-pole, double-throw relay. The amplifier compares two input voltages and energizes or de-energizes the relay, depending on whether the sum of the input voltages is greater than zero (positive) or less than zero (negative). There are two separate comparator units terminated at a Dual Comparator 40.404 Pre-Patch Panel area.

Figure 2.9-1 shows the comparator patching area and a simplified schematic of one of the comparators. (The second comparator is identical.) The relay termination indicated by the negative sign is the position of the relay when the sum of the IN_1 and IN_2 inputs is negative, this is the de-energized position of the relay. When the sum of the IN_1 and IN_2 inputs is positive, the relay energizes and the wiper swings to the positive contact.

(1) Comparator Switching Data

Relay Switching Time

Typical	7 milliseconds
Maximum allowable	10 milliseconds

Sensitivity

Typical	2 millivolts
Minimum	3 millivolts

(2) Set Up Procedure. The problem variable that is to control the comparator switching should always be applied to the IN_1 termination and the reference or bias voltage should be applied to the IN_2 termination. The following is the set-up procedure for the comparator.

(a) Apply an input to the IN_1 termination equal in magnitude and polarity to the desired switching level (Figure 2.9-1).

(b) Connect the wiper of a potentiometer to the IN_2 termination; apply reference, opposite in polarity to the IN_1 input, to the potentiometer hi end.

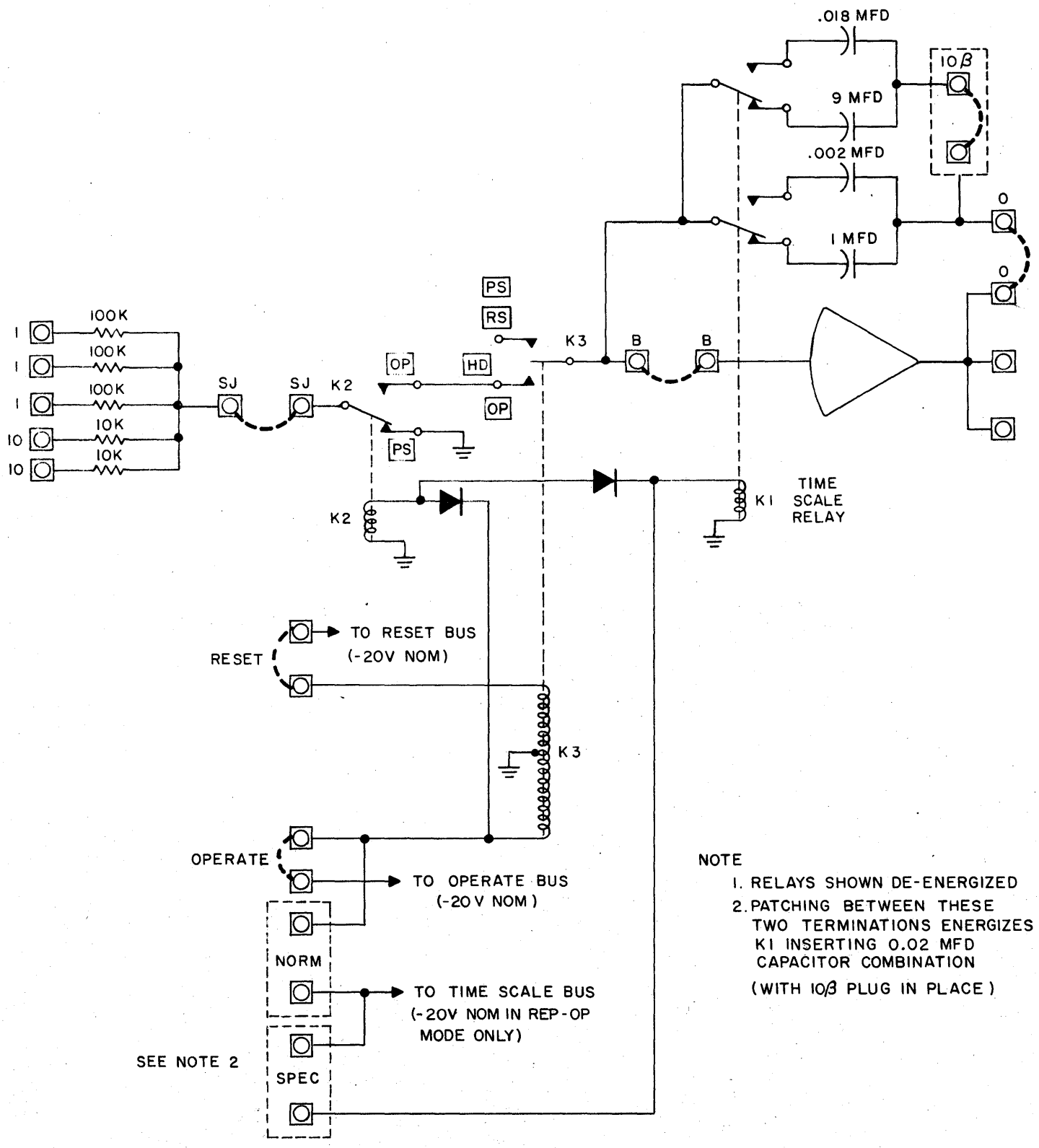


FIGURE 2.8-1. SIMPLIFIED INTEGRATOR SCHEMATIC SHOWING TIME SCALE CIRCUIT

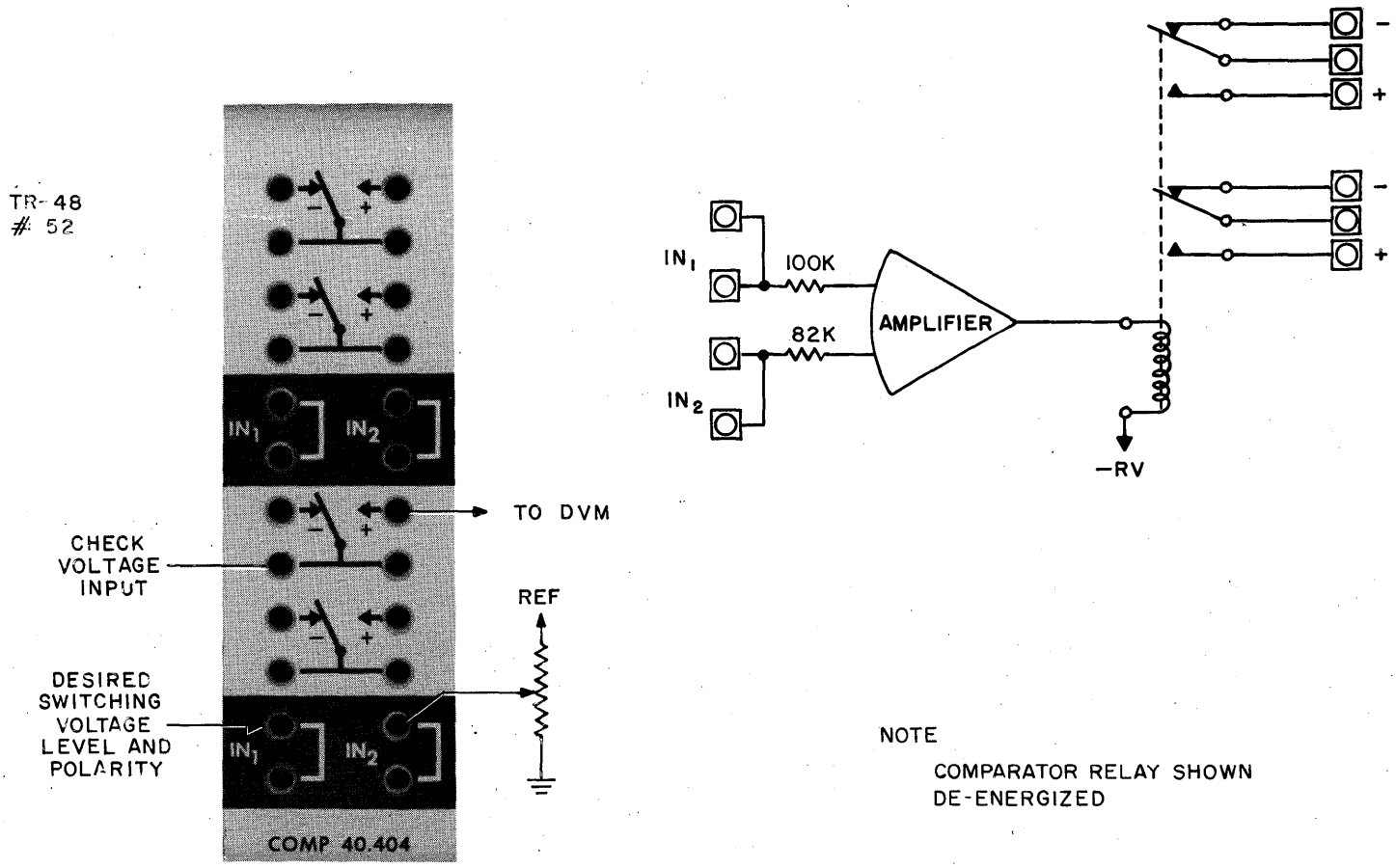


FIGURE 2.9-1. COMPARATOR PATCHING AREA AND SIMPLIFIED SCHEMATIC

(c) Adjust the input to IN_2 so the comparator relay is actuated as required when IN_1 reaches the switching level.

NOTE

By applying a voltage (designated check voltage on Figure 2.9-1) to one wiper and connecting the DVM to the contact that makes when the relay is actuated, visual indication of the relay switching may be obtained for set up.

(d) The comparator is now set for use in the problem and should be patched to the appropriate signal sources.

b. Function Switches

The Function Switch Group 12.766 provides five, 3-position single-pole switches mounted on the potentiometer panel (Figure 2.4-5) and terminated at the Pre-Patch Panel area shown in Figure 2.9-2. With these switches the operator may manually switch computer problem circuit functions. The center position may be considered the off position.

TR 48
62

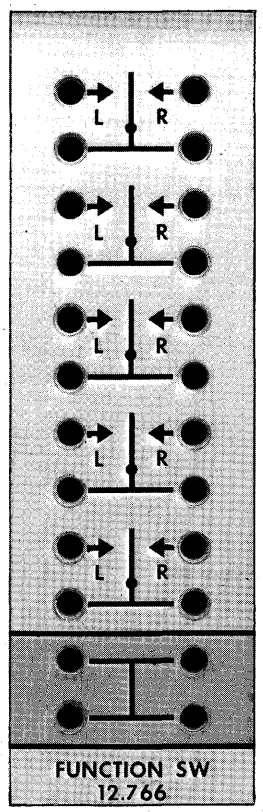


FIGURE 2.9-2. FUNCTION SWITCH PATCHING AREA

SECTION III

BASIC PROGRAMMING

The previous sections of this manual outlined the operation of the basic computing elements of the TR-48. An organized approach to programming a problem for the analog computer will now be discussed. The sample problems that follow will serve to illustrate the particular points in the programming procedure.

1. SYSTEM EQUATIONS

Starting from the physical system a mathematical description can be derived using well known physical laws, experimental results, and any reasonable simplifications that might appear desirable. The description will include a set of equations, coefficient values, initial conditions, and possibly some experimental data relating variables in the study. Next, it is necessary to consider the computing equipment available for the study, and what equation modifications, if any, are desirable (for instance, linearizing wherever possible to reduce the complexity of the study, using finite difference approximations to reduce partial differential equations to sets of ordinary differential equations, etc.). At the same time the operator should make any changes of variables or problem modifications that facilitate programming. Remember that the equations most conveniently solved on the computer are ordinary differential equations.

2. THE BOOTSTRAP METHOD

Consider the equation

$$a\dot{x} + bx = c \qquad \text{(EQ. 3.2-1)}$$

where a, b, and c are positive constants.

In order to solve this constant coefficient, linear, differential equation on the analog computer, three devices are needed: integrators, summers and potentiometers.

Earlier it was shown that summation and integration with respect to time could be accomplished by means of operational amplifiers, and that coefficients could be set on attenuators. To avoid differentiation on the computer (this operation has inherent noise problems), the differential equation usually can be manipulated so that only integration is required. This is accomplished by rewriting the equation so that the highest order derivative of the dependent variable under consideration appears alone on the left-hand side of the equation. The rewritten equation is

$$\dot{x} = \frac{c}{a} - \frac{b}{a}x \qquad \text{(EQ. 3.2-2)}$$

Note that Equation 3.2-2 indicates that if c/a and -bx/a are represented by voltages

and summed in an amplifier (Figure 3.2-1a), the resultant output is proportional to $-\dot{x}$ (the minus sign is a result of the inversion performed by the amplifier).

If the voltage proportional to $-\dot{x}$ is used as the input to an integrator (Figure 3.2-1b) the output of the integrator will vary as x.

The resulting output, x, may then be scaled by the coefficient b/a, multiplied by -1, and used as an input to the first summing amplifier (Figure 3.2-1c).

A voltage to represent c/a is generated by multiplying reference voltage by c/10a and used as the second input to the summer (Figure 3.2-1d). Thus, Figure 3.2-1d is a computer circuit which, in effect, is an electronic model of the equation $ax + bx = c$.

The steps followed in the bootstrap procedure to obtain the model are:

(1) Rewrite the equation to place the highest order derivative of the dependent variable by itself on the left side of the equation.

(2) Assume that a voltage proportional to this variable can be formed; consider it as the starting point in the diagram.

(3) Integrate this voltage as many times as necessary to generate the variables on the right side of the equation.

(4) Make use of the generated variables by scaling them and summing them to form the highest derivative that was originally assumed to exist.

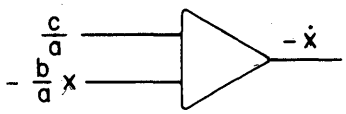
(5) Provide any required forcing function and initial condition.

Simultaneous equations may be mechanized in a similar manner as illustrated by the mechanization of the following set of equations (Figure 3.2-2):

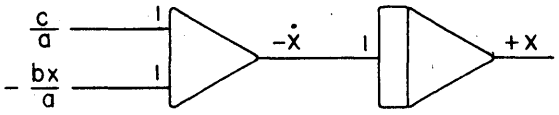
$$\dot{y} + a_1 y + a_2 z + a_3 \dot{z} = c$$
$$\ddot{z} + b_1 \dot{z} + b_2 z - b_3 y = 0 \qquad \text{(EQ. 3.2-3)}$$

No initial condition inputs are shown to any of the integrators, so the assumption must be that all I.C.'s are zero. If a non-zero I.C. is needed, it can be applied to the proper integrator as shown in Figure 3.2-3. Note that a sign inversion is present.

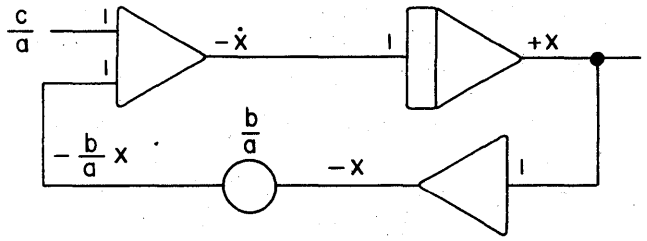
One point which has not yet been mentioned is economy of equipment. In Figure 3.2-2 the output $-\dot{y}$ from summer-1 serves no purpose other than to provide an input for the following integrator. This summation might be performed by the integrating amplifier, thereby saving two amplifiers (Figure 3.2-4). This combining of summation and integration may be done whenever the highest derivative does not appear anywhere else in the system of equations as an input and when it is not required as an output for recording.



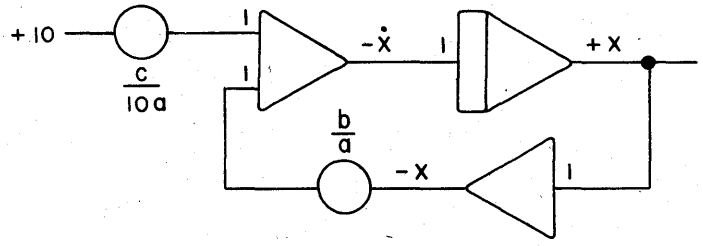
a.



b.



c.



d.

FIGURE 3.2-1 EVOLUTION OF COMPUTER DIAGRAM VIA BOOTSTRAP METHOD

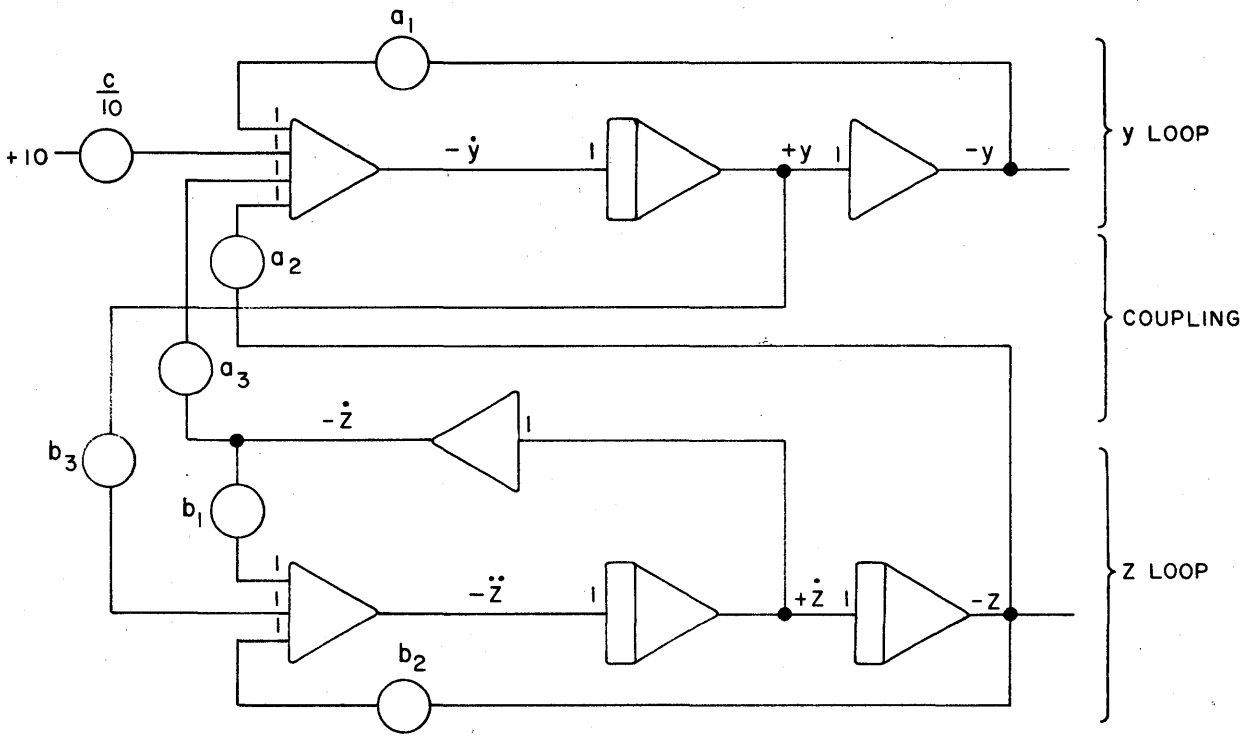


FIGURE 3.2-2 ANALOG COMPUTER MECHANIZATION OF EQUATION 3.2-3

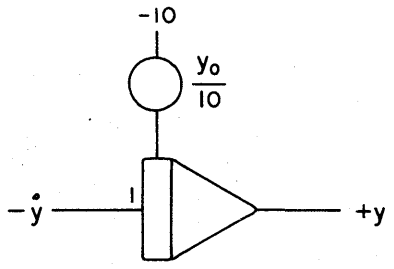


FIGURE 3.2-3. OBTAINING INITIAL CONDITION OF $y = +y_0$ AT $t = 0$

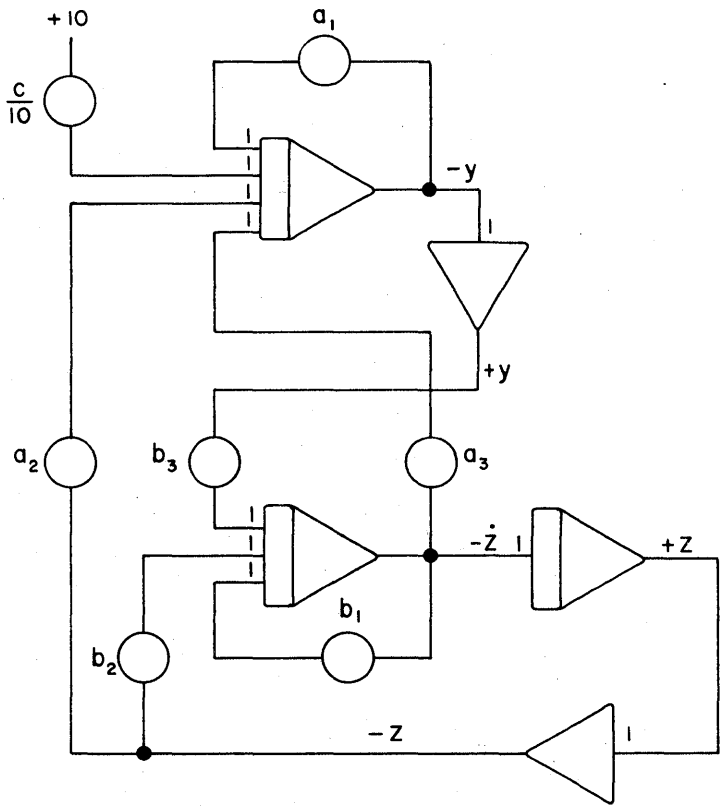


FIGURE 3.2-4 MODIFICATION OF CIRCUIT SHOWN IN FIGURE 3.2-2 USING FEWER AMPLIFIERS

3. SCALING

The independent variable of the equations is represented on the computer by time; the dependent variables and their derivatives with respect to time are represented on the computer by voltages. These signal voltages should never exceed the maximum allowable value of ±10 volts, nor should any voltage change rapidly enough to exceed the frequency limitations of the computing or recording equipment. On the other hand, the voltages should not be so small that they are of the same order as possible errors in a problem solution; also, the problem solution time should not be so long as to result in inefficient use of the computer. Between these extremes there is a reasonable value for the voltage variables and the speed of solution. The process of scaling determines these values; amplitude scaling to control the maximum value of the voltage variables, time scaling to control the speed of solution.

The maximum values which quantities can assume in a particular physical system can usually be estimated from:

(1) A knowledge of the physical system under study.

(2) An investigation of the system equations. Steady state relations and characteristic frequencies may be employed to evaluate the ranges of the dependent variables.

a. Amplitude Scaling

For maximum accuracy, the signal voltages representing the dependent variables and their derivatives should be as large as possible without causing the equipment to overload. The equipment is designed to operate within the range of ±10 volts. This implies that the maximum expected absolute value of the problem variable must correspond to 10 volts on the computer. An amplitude scale factor relating volts on the computer to the physical units of the problem variable can then be introduced. This scale factor has the dimensions of volts per physical unit and is determined by dividing the computer reference voltage (10 volts) by the maximum expected absolute value of the problem variable. For ease of calculation, the maximum expected absolute value is usually increased to the nearest convenient integer before calculating the scale factor. The table, Figure 3.3-1, shows typical scale factor calculations using the relationship:

$$\text{amplitude scale factor} = \frac{10}{\text{estimated maximum of variable}}$$

When a range is known for a variable (for example the variable T in Figure 3.3-1) a new variable can be defined to give better resolution. By defining $\Delta T = T-650$, optimum scaling for the physical quantity is obtained.

Having determined the amplitude scale factors, the problem variables in the mathematical equations are replaced by the equivalent voltages, adjustments being made to the coefficients throughout the equations in order to maintain equality. For

Problem Variable	Max. Expected Value or Max. Expected Range (Physical Units)	Scale Factor (Volts per Physical Unit)	Computer Variable (Volts)
Linear Distance, x	0.001 inches	$\frac{10}{.001} = 10^4$ volts/inch	$[10^4 x]$
Linear Distance, s	1,000 feet	$\frac{10}{1,000} = \frac{1}{100}$ volts/foot	$[\frac{s}{100}]$
Angular Acceleration, $\ddot{\theta}$	2 rad/sec^2	$\frac{10}{2} = 5$ volts/rad/sec^2	$[5\ \ddot{\theta}]$
Pressure, P	70 psi	$\frac{10}{70} > \frac{10}{100} = \frac{1}{10}$ volts/psi	$[\frac{P}{10}]$
Temperature, T Let $\Delta T = T-650$	650-700°F 50°F	$\frac{10}{50} = 0.2$ volts/°F	$[0.2\Delta T]$

Figure 3.3-1. Calculation of Amplitude Scale Factors, and Computer Variables. (Computer Variable=Scale Factor times Problem Variable)

example, s and θ would be replaced in the appropriate equations by $[s/100]$ and $[5\ \ddot{\theta}]$ respectively. The related coefficients would have to be multiplied by 100 and 1/5 to retain the validity of the equation. The equations are thus changed into voltage equations from which a computer circuit diagram can be drawn. Summarizing the rules for amplitude scaling:

(1) Determine the expected maximum absolute values and/or working ranges of all variables, including any derivatives which appear in the equations.

(2) Increase these maximum values to the nearest power of ten times, 1, 2, or 5 so that the scale factors can be manipulated conveniently.

(3) Determine the scale factors by dividing 10 by the values obtained in (2).

(4) Associate each variable with its scale factor and write the scaled voltage equations from the original problem equations.

(5) Prepare a computer diagram from the scaled voltage equations, and label it at appropriate points with the computer variables.

b. Time Scaling

The independent variable of the computer is time and the problem solution time may be increased or decreased with respect to time in the physical system. Time scaling is carried out by defining a time scale factor β, where:

$$\tau = \beta t \qquad \text{(EQ. 3.3-1)}$$

where

t = Time required for a solution in the physical problem.

τ = Time required for the same solution on the computer.

β = Dimensionless time scale factor.

If β is less than one, the computer solution is achieved in less time than would be required in the physical system. If β is greater than one, the computer solution takes longer than the physical problem solution. When β is equal to one, the computer solution is said to be a real time solution.

The time required for a phenomenon to occur can be changed by increasing or decreasing the rate at which the phenomenon takes place. This can be accomplished on the computer by changing the time constants in <u>all</u> circuits by the same amount. Usually this requirement is met by changing the time constants of <u>all</u> the integrators in the problem. (If any other network associated with the problem has a time constant, it too must be changed to effect a change in time scale.) Changing the time constant of an integrator amounts to simply changing the "gain" of the integrator; increasing the input gain to decrease the time of solution, and decreasing the gain to increase the time of solution.

If the independent variable of the computer is taken as τ, the integrator performs the operation

$$e_o(\tau) = -\frac{1}{RC}\int e_{in}(\tau)\, d\tau \qquad \text{(EQ. 3.3-2)}$$

Since $\tau = \beta t$ and $d\tau = \beta dt$:

$$e_o(\beta t) = -\frac{1}{RC}\int e_{in}(\beta t)\,\beta dt = -\frac{1}{\frac{RC}{\beta}}\int e_{in}(\beta t)\, dt \qquad \text{(EQ. 3.3-3)}$$

The integrator thus integrates with respect to time, t, but has a time constant of RC/β. The computer variable at the output of the integrator is a function of βt (or τ).

As an example of time scaling, consider a second order system described by

$$\ddot{x} + 2\zeta\omega_n\dot{x} + \omega_n^2 x = 0 \qquad \text{(EQ. 3.3-4)}$$

and $\dot{x} = 0,\ x = x_o,$ at $t = 0$

The general analytic solution to this equation is

$$x(t) = Ae^{-\zeta\omega_n t} \sin\left(\omega_n\sqrt{1-\zeta^2}\, t + \Phi\right) \qquad \text{(EQ. 3.3-5)}$$

A computer circuit to represent Equation 3.3-4 is shown in Figure 3.3-2. For the case where $\omega_n = 1000$ and $\zeta = 0.1$, potentiometers 00, 01, 02 and the associated amplifiers must provide gains of 200, 1000 and 1000 respectively. These high gains are not compatible with maximum computer accuracy. If the circuit is properly amplitude scaled the large gains indicate that time scaling is required since the rate inputs to the integrators must be reduced.

The independent variable of Equation 3.3-4 can be changed by defining

$$\tau = \beta t$$

$$\frac{dx}{d\tau} = \frac{1}{\beta}\frac{dx}{dt}$$

$$\frac{d^2x}{d\tau^2} = \frac{1}{\beta^2}\frac{d^2x}{dt^2}$$

Equation 3.3-4 becomes

$$\frac{d^2x}{d\tau^2} + \frac{2\zeta\omega_n}{\beta}\frac{dx}{d\tau} + \frac{\omega_n^2}{\beta^2}x = 0 \qquad \text{(EQ. 3.3-6)}$$

whose solution is

$$x(\tau) = Ae^{\frac{-\zeta\omega_n\tau}{\beta}} \sin\left(\frac{\omega_n}{\beta}\sqrt{1-\zeta^2}\,\tau + \Phi\right) \qquad \text{(EQ. 3.3-7)}$$

It is clear that the solution for $x(\tau)$ is simply a time scaled version of the original solution for $x(t)$ with the natural frequency (ω_n) and decay time ($\zeta\omega_n$) reduced by a factor β. The amplitudes and initial conditions are not affected.

An appropriate time scale factor for this example is 100 which results in a com-

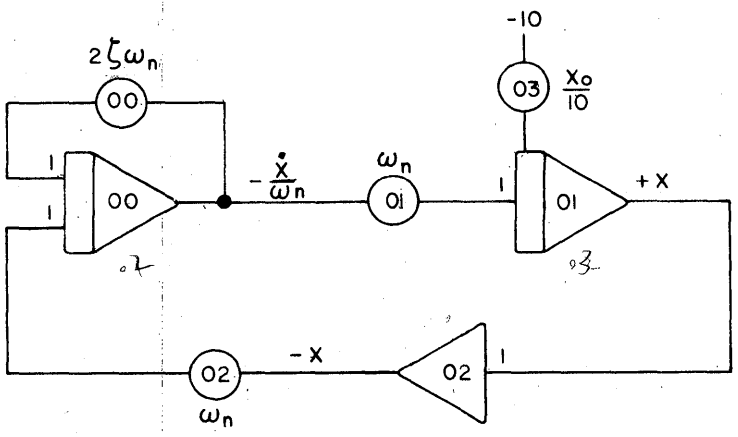


FIGURE 3.3-2 COMPUTER DIAGRAM FOR EQUATION 3.3-4

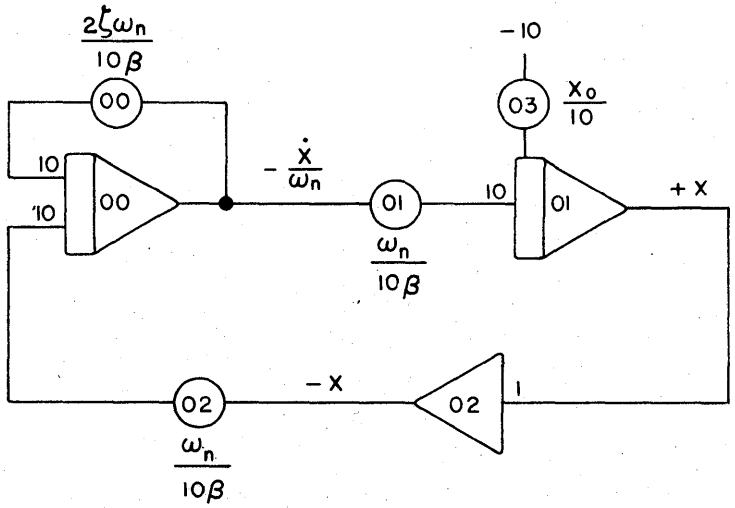
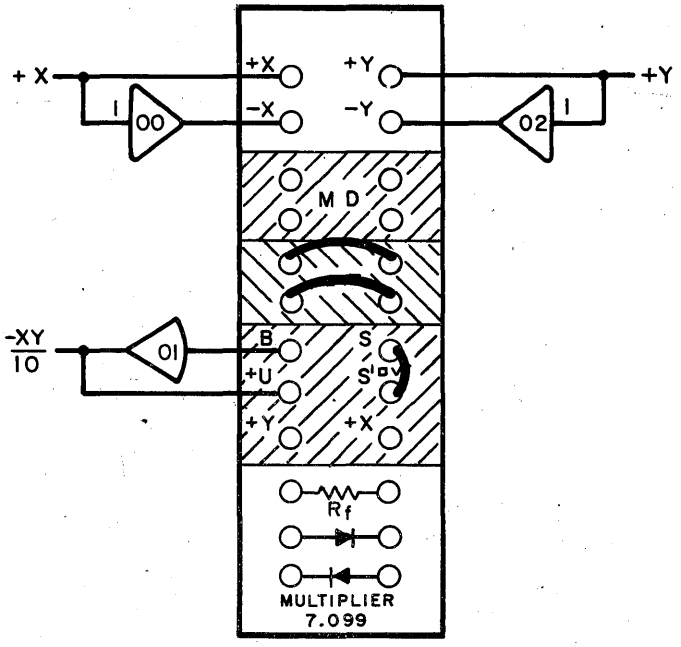


FIGURE 3.3-3. TIME SCALED DIAGRAM FOR EQUATION 3.3-4.

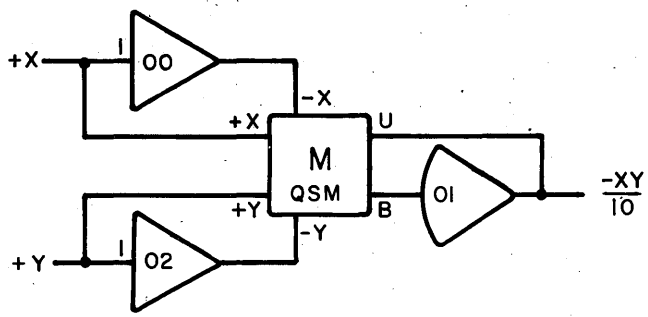
APPENDIX 3

QUARTER-SQUARE MULTIPLIER CIRCUITS

1. MULTIPLICATION



PATCHING DIAGRAM



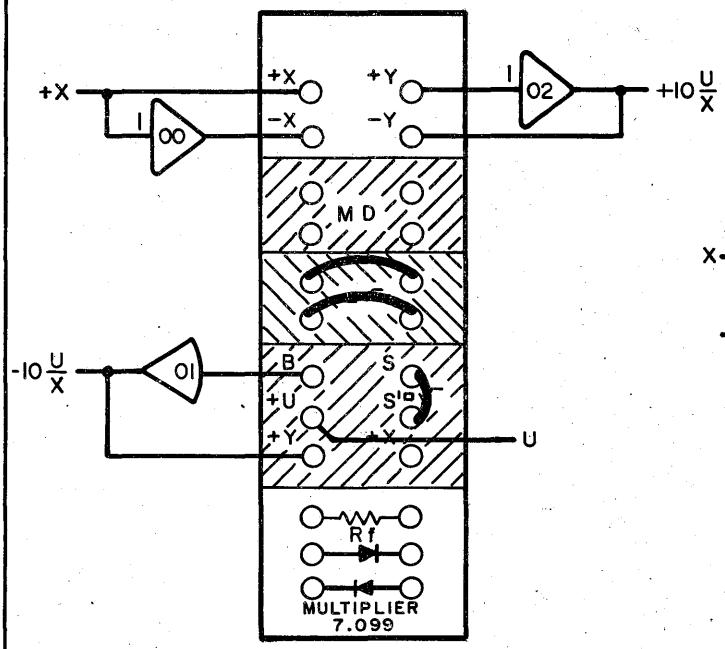
COMPUTER DIAGRAM

$-10 \leq X \leq +10$

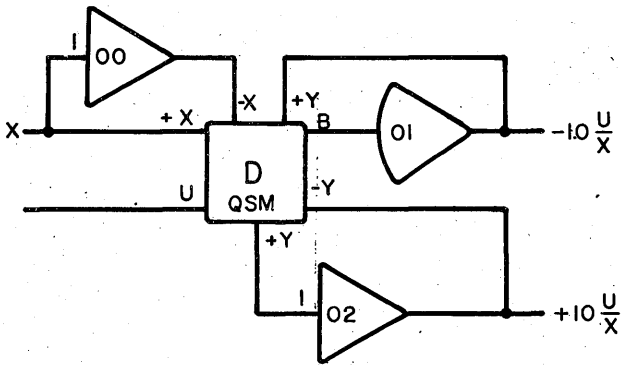
$-10 \leq Y \leq +10$

$-10 \leq \frac{XY}{10} \leq +10$

2. DIVISION



PATCHING DIAGRAM



COMPUTER DIAGRAM

$-10 \leq X < 0$ OR $0 < X \leq +10$

$-10 \leq U \leq +10$ BUT $|U| \leq |X|$

DIVISION CIRCUIT RESTRICTIONS

1. $\frac{U}{X} \leq 1.0$
2. X MUST BE POSITIVE, (IF X IS NEGATIVE, CONNECTIONS TO +X AND −X SHOULD INTERCHANGED)
3. $X \neq 0$

puter frequency of (ω_n/β) of 10 rad/sec and a damping time constant $(\zeta\omega_n/\beta)$ of one second. This change in time scale is obtained as shown in Figure 3.3-3 by dividing all inputs to the integrators by β. Note, in addition, that potentiometer settings less than or equal to one are obtained by using gains of ten on the integrators.

Let us check through the circuit of Figure 3.3-3.

The input to amplifier 01 is

$$e_{i1} = \frac{\dot{x}(\tau)}{10\beta}$$

The output of amplifier 01 is

$$e_{o1} = -10 \int \left[\frac{-\dot{x}(\tau)}{10\beta}\right] d\tau = \int \dot{x}dt = x(\tau)$$

The input to amplifier 00 is

$$e_{i0} = \frac{-2\zeta\omega_n}{10\beta}\frac{\dot{x}(\tau)}{\omega_n} - \frac{\omega_n}{10\beta}x(\tau)$$

The output of amplifier 00 is therefore

$$e_{o0} = \int \left[\frac{2\zeta}{\beta}\dot{x}(\tau) + \frac{\omega_n}{\beta}x(\tau)\right] d\tau = \int \left(-\frac{\ddot{x}(\tau)}{\omega_n}\right) dt = -\frac{\dot{x}(\tau)}{\omega_n}$$

Thus with $\beta = 100$, the rates to the integrators are decreased by 100, the computer solution is slowed down by 100, and the time scale is effectively 100 times its previous value.

Since the amplitudes present in the computer solution are not changed by time scaling, it is reasonable to use the same notation for the variables in the time scaled circuit as is used in circuits without it. It is important, however, to remember that all computing components, including output equipment such as strip chart recorders and oscilloscopes, are operating in machine time (or τ) and the time axis of all recordings must eventually be labeled in terms of t in order to interpret the output data. If for example, a particular point in the time scaled computer solution is labeled as ten seconds (in τ), then the same point is labeled as $10/\beta$ seconds in t.

The procedure for time scaling may be summarized as follows:

(1) Consider in the early stages of the problem whether or not a time scale change is indicated. If possible, determine the natural frequencies and exponential time constants of the physical system.

(2) Perform amplitude scaling and write the scaled voltage equations as described earlier without regard to time scaling.

(3) If the input gains to the integrators are very high, or very low, include in all the integrator inputs an attenuator factor of $1/\beta$.

(4) Choose an appropriate value of β from steps 1 or 3, and calculate the necessary potentiometer settings. If possible, select β so that standard amplifier gains and reasonable potentiometer settings (>.01) are used.

(5) Determine the recorder speed settings or scale factors for output devices so that time axes read appropriately.

4. COMPUTER CIRCUIT DIAGRAM

A computer circuit diagram can be produced directly from the scaled voltage equations. It will follow the general data flow of a mathematical block diagram but will include detailed information about the computer components such as, component assignment number, amplifier and integrator gains, potentiometer settings (in terms of the system parameters) and function switch terminations, etc. The outputs of major components should be labeled with the computer variable appearing at that point in the diagram. Standard symbols should be used in preparing the diagram such as the recommended set given in Appendix 1. The diagram should be drawn so that it can be easily reproduced.

Each computing component on the diagram is assigned a number corresponding to the location of the component in the computer. The assigned numbers appear on the amplifier assignment sheets and the potentiometer and function switch assignment sheets. The amplifier assignment sheet should include problem identification, amplifier number, function of the amplifier (summer, inverter, high gain, or integrator), the variable represented by the output of the amplifier, calculated values for the static check voltages and provision for recording the measured check voltages and any comments or notes. The potentiometer assignment sheet should include problem identification, potentiometer number, parameter description, potentiometer settings for both static check and the problem runs. Function switch assignment sheets are prepared in essentially the same form as potentiometer assignment sheets.

5. PROBLEM CHECK PROCEDURES

When the programming and scaling operations are completed and the computer circuit diagram is drawn, the methods to be used in checking the computer program and subsequent patching should be considered.

Amplifier and potentiometer assignment sheets are prepared and a detailed sequence of steps to be followed after insertion of the patch panel should be drawn up.

The first phase of a problem check procedure is the static check. The static check consists of two parts. Part one, the program check is a pencil and paper check to determine if the scaled computer program (circuit diagram) truly represents the original equations. This part should be completed before patching

the problem. Part two, the patching check, is the actual measurement of computer input and output voltage levels to ascertain that the interconnections (made by patching) of computer components are correct, and to check the static operation of inverters, summers, high gain amplifiers, potentiometers, multipliers, X^2 DFG's, etc. The static check does not test the operation of the integrators.

To perform the first part of the static check, assume convenient values for the variables, their n-1 derivatives, and all parameters. The variables and their derivatives are represented by scaled initial condition voltages at each integrator and need not have physical significance. The values selected for these initial conditions should be chosen to produce reasonable outputs (one to ten volts) from all computing components. The selected scaled voltages are then written down on the computer diagram next to the outputs of the appropriate integrators. These voltages are then used as a starting point for computing the voltage levels of all input and output terminations of the computing components on the circuit diagram. These computations are made by performing the various operations of multiplication by a constant, sign inversion, summations, etc., at the computing components on the diagram until the input to an integrator is reached. At the input to an integrator the calculation stops since the integrator is not operational in the I.C. mode. This procedure is repeated for all variables until the complete set of voltage levels has been calculated.

The assumed check values are then substituted into the <u>original</u> unscaled mathematical equations and the value of the highest derivative is computed. This computed value for the highest (nth) derivative, properly scaled, (includes both the voltage scale factor and the time scale factor β) should check the voltage level calculated for that point on the diagram. In order to check the inputs to the other integrators, a calculation is made on the basis that the input to the integrator should be <u>minus</u> the derivative of the output (divided by β, the time scale factor). Example: If the output of an integrator was $[-1000\ \dot{x}]$ the input should be $+1000\ddot{x}/\beta$. If the assumed value of $\ddot{x} = 0.05$ ft/sec^2 and $\beta = 10$ this results in an input voltage of $+1000(.05)/10$ or +5 volts. The +5 volts should check the calculated input voltage level on the diagram. In some cases the assumed values for the variables, n-1 derivatives and parameters produce low voltage levels or zero outputs. In these cases it is necessary to change some of the assumed values and repeat the calculations. In the case of coupled equations a static check should be made of the entire system with one set of assumed values. When this portion of the static check is complete, the computer program should be patched.

Patching is best accomplished by two people, one person calling off from the computer diagram, the connections to be made, and the second person making the connections on the patch panel. A colored line is then drawn through the corresponding line on a copy of the computer diagram indicating that a connection has been made. After patching is complete the two persons should exchange places, and the patched program read off from the patch panel by one person and checked against the diagram by the other. A systematic procedure that is recommended is to check out all of the patched inputs to computing components against a copy of the computer diagram.

The second part of the static check is to set the potentiometers and initial conditions on the computer to the static check values. Since all computing components except integrators are operational in the I.C. mode, their outputs can be read out and checked against the calculated values. In order to check inputs to integrators it is necessary to use an uncommitted amplifier. The inputs to the integrators are temporarily patched into this amplifier to allow read-out of the effective input voltage to the integrator. Since the input to an integrator can exceed ten volts it is often necessary to use a check amplifier with a gain of -1/10. The use of a check amplifier is described in the example problems.

Once the static check is completed one or more dynamic checks are made depending on the information available. In linear systems a simplified form of the equation can be checked by reducing the damping to zero and checking undamped natural frequencies. Many times the response of the system to a step input can be calculated and the computer program modified to accept a step input as a check. In non-linear systems, a linear approximation can often be implemented by adjustment of the parameters and a check obtained using results from a precalculated linear analysis. Numerical checks from digital computer results can also be used. If experimental data for the model is available, a check can be made by direct comparison.

6. PROGRAMMING A LINEAR PROBLEM

To demonstrate programming, amplitude scaling, and time scaling, a computer program will be developed to investigate the effect of shock-absorber damping coefficient upon the transient motion of an automobile chassis.

a. Problem Description

A simplified representation of one wheel of an automobile suspension system together with one-fourth the vehicle chassis, is shown in Figure 3.6-1.

The differential equations of motion are derived by equating the forces acting upon the masses to zero to establish dynamic equilibrium.

Thus for M_1:

$$M_1 \frac{d^2x_1}{dt^2} + D\left(\frac{dx_1}{dt} - \frac{dx_2}{dt}\right) + K_1 (x_1 - x_2) = 0 \qquad \text{(EQ. 3.6-1)}$$

And for M_2:

$$M_2 \frac{d^2x_2}{dt^2} + D\left(\frac{dx_2}{dt} - \frac{dx_1}{dt}\right) + K_1(x_2 - x_1) + K_2(x_2 - x_3) = 0 \qquad \text{(EQ. 3.6-2)}$$

Where

$$M_1 = \frac{W_1}{g} = 25 \text{ slugs} \qquad K_1 = 1000 \text{ lb/ft}$$

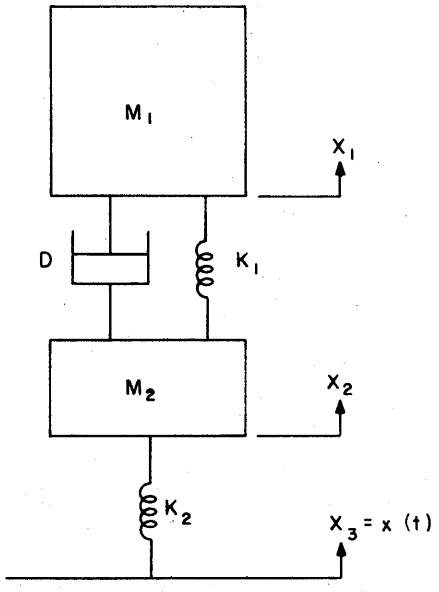


FIGURE 3.6-1 SIMPLIFIED REPRESENTATION OF A SINGLE AUTOMOBILE-WHEEL SUSPENSION SYSTEM

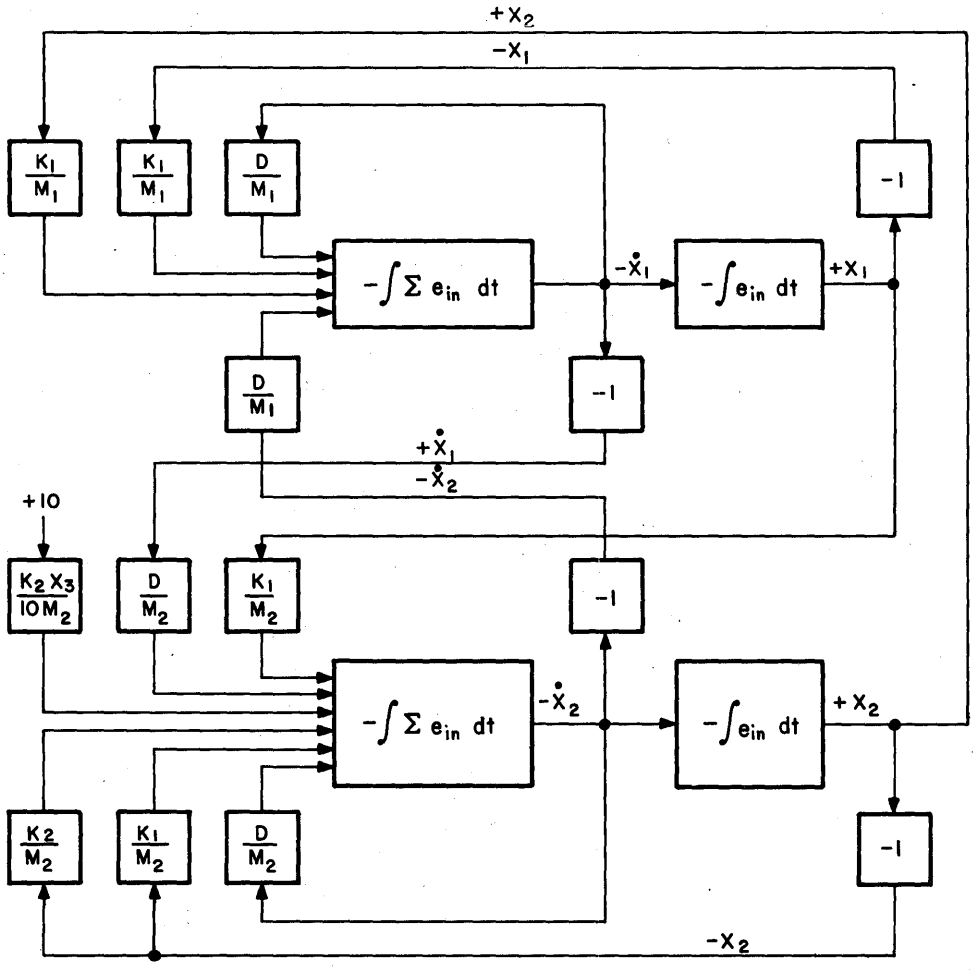


FIGURE 3.6-2 MATHEMATICAL BLOCK DIAGRAM FOR EQUATIONS 3.7-3 AND 3.7-4

$$M_2 = \frac{W_2}{g} = 2 \text{ slugs} \qquad K_2 = 5000 \text{ lb/ft}$$

$x_3 = x(t)$ = step input; 5 inches in amplitude (car riding up on curb)

D = variable damping coefficient; 20, 50, and 100 lb-sec/ft

For scaling we shall assume that the displacements x_1 and x_2 will not exceed twice the input function and that the velocities $\dot{x}_1$ and $\dot{x}_2$ will not exceed 5 feet per second and 50 feet per second respectively.

b. Preliminary Considerations

The mathematical block diagram is the first step in programming. It is a translation of the system equations and shows the basic approach to the whole problem. From this diagram one can determine approximate equipment requirements; it also serves as a guide to the final form of the scaled equations, the method of generating the various functions required and the layout of the final circuit diagram.

The block diagram shown in Figure 3.6-2 was obtained from Equations 3.6-3 and 3.6-4 using the bootstrap method. The initial equipment requirements are four integrators, four inverters and 10 potentiometers (exclusive of IC potentiometers).

$$\ddot{x}_1 = -\frac{D}{M_1}\dot{x}_1 + \frac{D}{M_1}\dot{x}_2 - \frac{K_1}{M_1}x_1 + \frac{K_1}{M_1}x_2 \qquad \text{(EQ. 3.6-3)}$$

$$\ddot{x}_2 = -\frac{D}{M_2}\dot{x}_2 + \frac{D}{M_2}\dot{x}_1 - \frac{K_1}{M_2}x_2 + \frac{K_1}{M_2}x_1 - \frac{K_2}{M_2}x_2 + \frac{K_2}{M_2}x_3 \qquad \text{(EQ. 3.6-4)}$$

An examination of the natural frequencies and damping time constants of the uncoupled Equations, 3.6-5 and 3.6-6, will give a good indication as to whether time scaling will be required.

$$\ddot{x}_1 + \frac{D\dot{x}_1}{M_1} + \frac{K_1 x_1}{M_1} = 0 \qquad \text{(EQ. 3.6-5)}$$

$$\ddot{x}_2 + \frac{D\dot{x}_2}{M_2} + \left(\frac{K_1+K_2}{M_2}\right)x_2 = 0 \qquad \text{(EQ. 3.6-6)}$$

Where the undamped natural frequencies are:

$$\omega_{n_1} = \sqrt{\frac{K_1}{M_1}} = \sqrt{40} = 6.325 \text{ rad/sec} \cong 1 \text{ cps}$$

$$\omega_{n_2} = \sqrt{\frac{K_1+K_2}{M_2}} = \sqrt{3000} = 54.77 \text{ rad/sec} \tilde{=} 9 \text{ cps}$$

Using the maximum value of D, the damping time constants are:

$$\frac{2M_1}{D} = 0.50 \text{ secs} \qquad \frac{2M_2}{D} = 0.04 \text{ secs}$$

Therefore, for the uncoupled systems, the frequencies involved will be of the order 1-9 cps, and the time required for the solution to reach a steady state will be in the order of 5 time constants or 0.2 to 2.5 seconds. Frequencies in the order of 0.1 to 1 cycle/second are more desirable, therefore, a time scale change with $10<\beta<100$ is indicated.

c. Scaling

The amplitude scale factors are obtained by dividing 10 volts by the maximum absolute value of the problem variables. The computer variables are obtained by multiplying the problem variables by their scale factors. In this example the maximum values are given, and the computer variables are calculated in the table, Figure 3.6-3. Since the accelerations, $\dddot{x}_1$ and $\dddot{x}_2$ are not explicitly required in this study, these terms can be formed at the inputs to integrators and can be scaled at the level of $\dot{x}_1$ and $\dot{x}_2$ respectively.

Problem Variable	Maximum Value	Scale Factor	Computer Variable
x_1	10/12 feet	120/10> 10 volts/ft	$[10x_1]$
x_2	10/12 feet	120/10> 10 volts/ft	$[10x_2]$
$\dot{x}_1$	5 ft/sec	10/5> 2 volts/ft/sec	$[2\dot{x}_1]$
$\dot{x}_2$	50 ft/sec	10/50> 0.2 volts/ft/sec	$[0.2\dot{x}_2]$
$\ddot{x}_1$	Use same S.F. as for $\dot{x}_1$	2 volts/ft/sec^2	$[2\ddot{x}_1]$
$\ddot{x}_2$	Use same S.F. as for $\dot{x}_2$	0.2 volts/ft/sec^2	$[0.2\ddot{x}_2]$
x_3	constant		

Figure 3.6-3. Calculating Scale Factors

Solving the original equations for the highest derivatives and introducing the scaled variables yields the scaled voltage equations.

$$[2\ddot{x}_1] = -2\frac{D}{M_1}\frac{1}{2}[2\dot{x}_1] + 2\frac{D}{M_1}\frac{1}{0.2}[0.2\dot{x}_2] - 2\frac{K_1}{M_1}\frac{1}{10}[10x_1] + 2\frac{K_1}{M_1}\frac{1}{10}[10x_2] \quad \text{(EQ. 3.6-7)}$$

$$[0.2\ddot{x}_2] = -0.2\frac{D}{M_2}\frac{1}{0.2}[0.2\dot{x}_2] + 0.2\frac{D}{M_2}\frac{1}{2}[2\dot{x}_1] - 0.2\frac{K_1}{M_2}\frac{1}{10}[10x_2] + 0.2\frac{K_1}{M_2}\frac{1}{10}[10x_1]$$

$$-0.2\frac{K_2}{M_2}\frac{1}{10}[10x_2] + 0.2\frac{K_2x_3}{M_2}\frac{1}{10}[10] \quad \text{(EQ. 3.6-8)}$$

Note that square brackets are placed around the computer variables. The computer variables are voltages which have been scaled to be as large as possible but less than 10 volts. These equations contain constant coefficients which will appear in the computer circuit as attenuator settings (that cannot be greater than one) and amplifier gains. The maximum value of these gains can be determined after first simplifying Equations 3.6-7 and 3.6-8.

$$[2\ddot{x}_1] = -\frac{D}{M_1}[2\dot{x}_1] + 10\frac{D}{M_1}[0.2\dot{x}_2] - \frac{K_1}{5M_1}[10x_1] + \frac{K_1}{5M_1}[10x_2] \quad \text{(EQ. 3.6-9)}$$

Maximum gains $= 4$ $= 40$ $= 8$ $= 8$

$$[0.2\ddot{x}_2] = -\frac{D}{M_2}[0.2\dot{x}_2] + \frac{D}{10M_2}[2\dot{x}_1] - \frac{K_1}{50M_2}[10x_2] + \frac{K_1}{50M_2}[10x_1] - \frac{K_2}{50M_2}[10x_2] + \frac{K_2x_3}{50M_2}[10]$$

Maximum gains $= 50$ $= 5$ $= 10$ $= 10$ $= 50$ $= 20.83$

(EQ. 3.6-10)

These gains must be obtained by a combination of potentiometer settings and amplifier gains.

The circuit to generate $[2\ddot{x}_1]$ is shown in Figure 3.6-4a where standard gains of one and ten are used where possible and the attenuator settings are less than one. The nigh input gains required suggests that the input rate is high; it is an indication that time scaling is required. The rate can be decreased by a factor of 10 to slow the problem down. The circuit with $\beta = 10$ is shown in Figure 3.6-4b.

Including β, the final scaled equations are:

$$\left[\frac{2\dot{x}_1}{\beta}\right] = -1\left(\frac{D}{M_1\beta}\right)[2\dot{x}_1] + 10\left(\frac{D}{M_1\beta}\right)[0.2\dot{x}_2] - 1\left(\frac{K_1}{5M_1\beta}\right)[10x_1] + 1\left(\frac{K_1}{5M_1\beta}\right)[10x_2] \quad \text{(EQ. 3.6-11)}$$

$$\left[\frac{0.2\dot{x}_2}{\beta}\right] = -10\left(\frac{D}{10M_2\beta}\right)[0.2\dot{x}_2] + 1\left(\frac{D}{10M_2\beta}\right)[2\dot{x}_1] - 1\left(\frac{K_1}{50M_2\beta}\right)[10x_2] + 1\left(\frac{K_1}{50M_2\beta}\right)[10x_1]$$

$$-10\left(\frac{K_2}{500M_2\beta}\right)[10x_2] + 10\left(\frac{K_2x_3}{500M_2\beta}\right)[10] \quad \text{(EQ. 3.6-12)}$$

In Equations 3.6-11 and 3.6-12, the terms in square brackets represent computer variables; the terms in curved brackets represent attenuator settings; the unbracketed coefficients represent amplifier gains. From these equations the computer circuit diagram can be drawn directly.

d. Computer Circuit Diagram

Taking Equation 3.6-11 as an example:

(1) Integrate the highest derivative to obtain the lower derivatives and the variable itself; Figure 3.6-5.

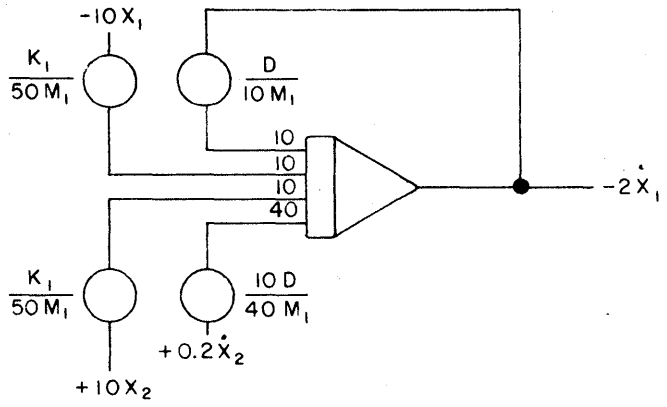
(2) Similarly generate $-0.2\dot{x}_2$ and $10x_2$.

(3) Use the scaled equations to provide the inputs to the first integrator, e.g., the first term in Equation 3.6-11 says to take $-2\dot{x}_1$ through an attenuator set at $D/M_1\beta$ into a gain of 1 on the integrator; the second term says to take $+0.2\dot{x}_2$ through an attenuator set at $D/M_1\beta$ into a gain 10 on the same integrator. The other terms in the $\ddot{x}_1$ equation are supplied in a similar manner. The complete computer diagram is shown in Figure 3.6-6. Note that integrator 06 is generating $+[0.2\dot{x}_2]$, rather than $-[0.2\dot{x}_2]$. This circuit arrangement uses two less amplifiers than the circuit that would follow directly from the mathematical block diagram. Also note that numbers have been assigned to all components and all amplifier outputs are labeled with the appropriate computer variable.

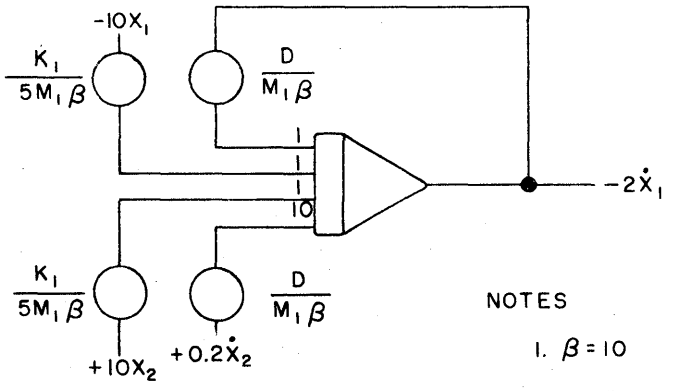
e. Check Procedures and Set Up Sheets

Once the scaled computer diagram is completed, a static check is calculated and the equipment assignment sheets are prepared. A definite sequence of steps must be followed in preparing a static check so that the operator can check his work up to this point.

(1) Calculate all potentiometer settings, using convenient values for the parameters, say those which will be used in the first run. For this example,



a. DIRECT MECHANIZATION OF EQUATION

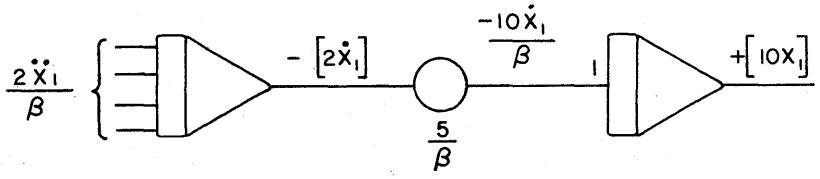


NOTES

1. $\beta = 10$
2. INTEGRATOR INPUT $= \frac{2\ddot{X}_1}{\beta} = \frac{d(2\dot{X}_1)}{d\tau}$

b. TIME SCALED CIRCUIT

FIGURE 3.6-4 DIRECT AND TIME SCALED MECHANIZATION OF EQUATION 3.6-9



NOTE

A GAIN OF 5 IS REQUIRED THROUGH THE INTEGRATOR TO OBTAIN $10X_1$ FROM $2\dot{X}_1$ AND THE FACTOR OF β MUST BE INCLUDED TO TIME SCALE

FIGURE 3.6-5 GENERATION OF $10X_1$ FROM $2\dot{X}_1$

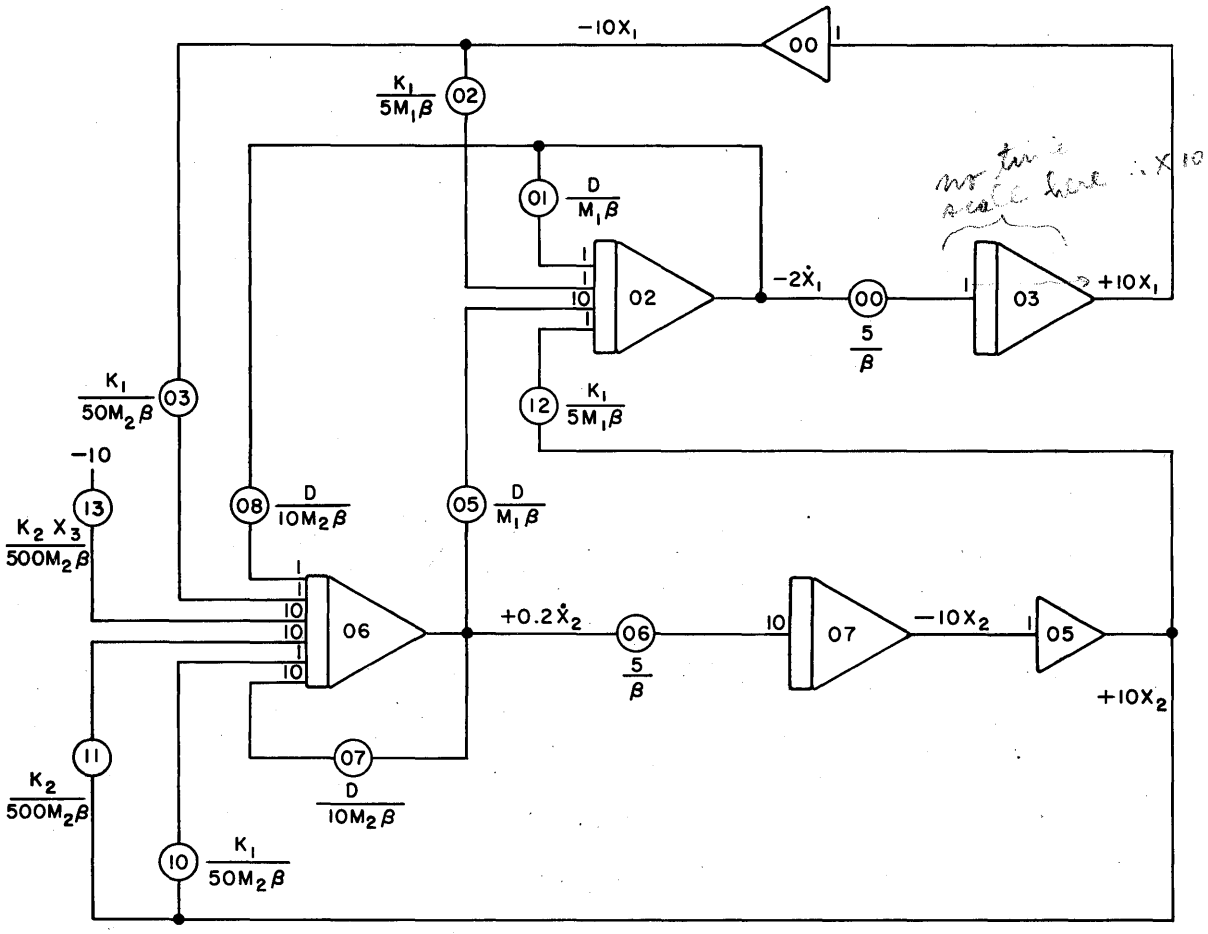


FIGURE 3.6-6 SCALED COMPUTER DIAGRAM FOR THE AUTOMOBILE SUSPENSION SYSTEM

choose the parameters as given and D = 100 lbs-sec/ft. List the parameter and static check setting of each potentiometer on a potentiometer set up sheet as shown in Figure 3.6-7.

(2) Assume convenient values for the inputs and initial conditions. These values need not have physical significance. For this example choose:

$x_1 = +1$ ft $\qquad \dot{x}_1 = +5$ ft/sec $\qquad x_3 = 3$ inches

$x_2 = -1$ ft $\qquad \dot{x}_2 = -10$ ft/sec

On a copy of the computer diagram, "establish" these values as initial conditions or inputs, see Figure 3.6-8. If additional potentiometers are necessary, list them on the potentiometer set up sheet.

Note that integrators that normally have a zero initial condition for problem runs are now supplied with initial condition inputs. <u>These inputs must be removed when the static check is completed</u>. The reference voltage to potentiometer 15 and to the initial condition inputs of amplifiers 02, 03, and 07 will be supplied by the reference terminations next to potentiometers P15-19. The minus reference from this source will be designated -ST; the positive reference, +ST. When the static test is completed, all leads to this reference block will be removed.

(3) On the basis of the initial conditions and inputs established, determine the voltage at the output of each computing component as shown in Figure 3.6-8. The output of A03 is +10 volts, the output of A00 is -10 volts, the output of P02 is -8 volts, and so on. This checks that reasonable outputs are being obtained from all components for the values chosen. <u>If an overload or zero voltage results from any component, choose different initial conditions</u>. Also list the output voltages of all the amplifiers on the amplifier set up sheet as shown in Figure 3.6-9.

From the diagram, determine the voltages representing the highest derivatives, e.g., in Figure 3.6-8, the voltage representing $\ddot{x}_2$ is

$$\frac{-0.2\ddot{x}_2}{\beta} = -5(1) -10(1) -1.25(10) -5(10) -10(1) -1(10) = -97.5 \text{ volts}$$

In a similar fashion:

$$\frac{+2\ddot{x}_1}{\beta} = -28 \text{ volts (integrator 02)}$$

$$\frac{-10\dot{x}_1}{\beta} = -5 \text{ volts (integrator 03)}$$

$$\frac{+10\dot{x}_2}{\beta} = -10 \text{ volts (integrator 07)}$$

These voltages will appear at the inputs to the integrators and can be measured by making use of a check amplifier as explained later. List these voltages next to the appropriate integrator under the calculated check point column on the amplifier set up sheet.

(4) Substitute the assumed initial condition values of the variables into the original system equations, calculate the value of the highest derivatives and then the scaled computer voltages to represent these derivatives. These voltages should check with the voltages determined in step three. Substituting into Equations 3.6-3 and 3.6-4:

$$\ddot{x}_1 = \frac{100}{25}(5) + \frac{100}{25}(-10) - \frac{1000}{25}(1) + \frac{1000}{25}(-1) = -140 \text{ ft/sec}^2$$

$$\ddot{x}_2 = 4875 \text{ ft/sec}^2$$

Therefore the input to integrator 02 should be

$$\frac{+2\ddot{x}_1}{\beta} = \frac{2(-140)}{10} = -28 \text{ volts}$$

the input to integrator 06 must be:

$$\frac{-0.2\ddot{x}_2}{\beta} = \frac{-0.2(4875)}{10} = -97.5 \text{ volts}$$

This check verifies that the final program is a model of the original equations.

(5) The final step in the static check is to actually measure the voltage outputs of the computing components. Any discrepancy between calculated and measured outputs must be due to incorrect potentiometer settings, faulty patching, or to a component malfunction.

After the problem is patched from the computer diagram, the static test inputs are introduced. The computer is placed in the Pot Set mode and the potentiometers are set to the coefficients listed for the static test (ST) case on the potentiometer set up sheet. The computer is placed in the RS mode and the voltage output of each amplifier is measured and recorded on the amplifier set up sheet. These measured values should check with the values calculated in step three.

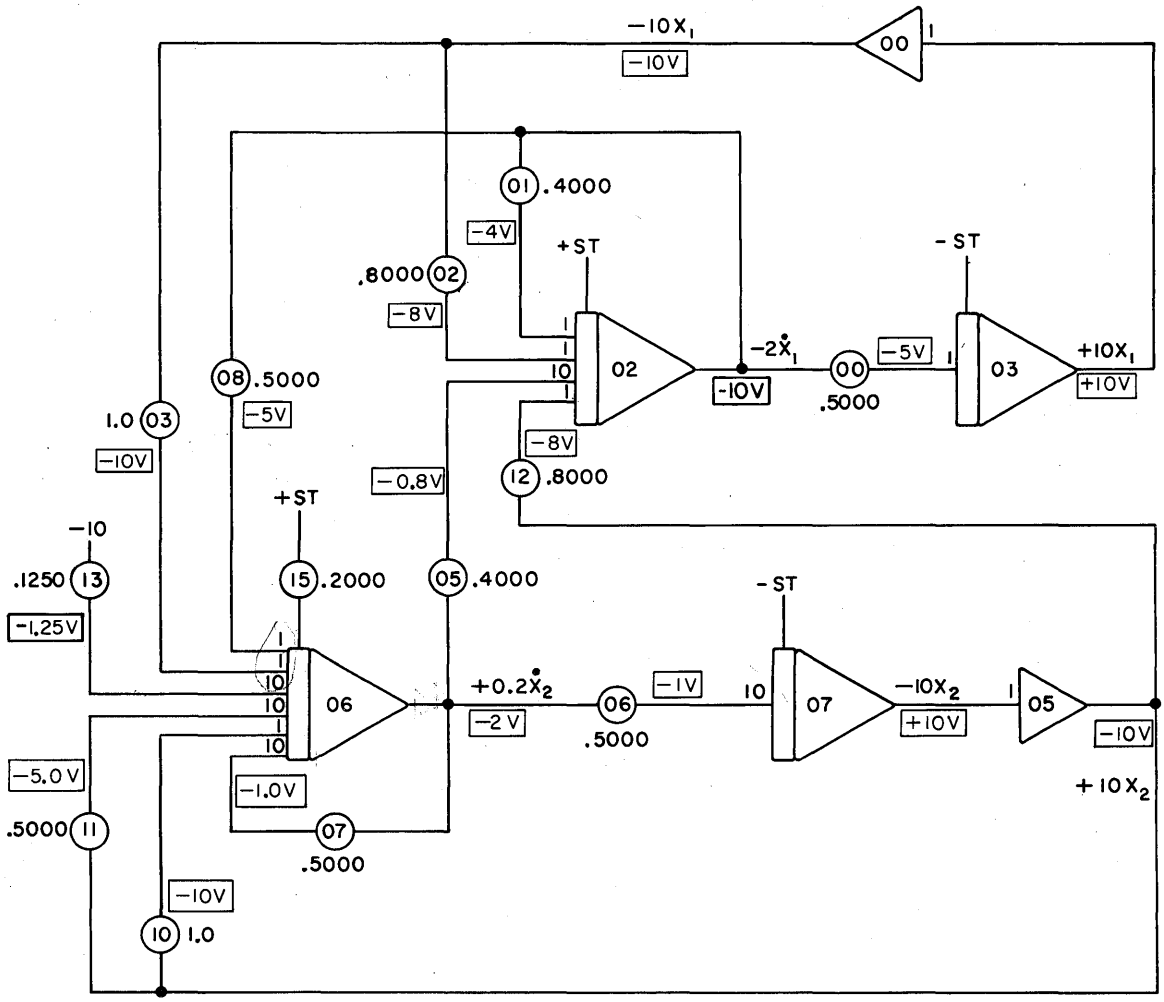
A4715

TR-48 POTENTIOMETER ASSIGNMENT SHEET

DATE _____ PROBLEM _____

POT NO.	PARAMETER DESCRIPTION	SETTING STATIC CHECK	SETTING RUN NO.1	SETTING RUN NO.	SETTING RUN NO.	NOTES	POT NO.
00	$5/\beta$	.5000	.5000				00
01	$D/M_1\beta$	.4000	.4000				01
02	$K_1/5M_1\beta$	.8000	.8000				02
03	$K_1/50M_2\beta$	1.000	1.000				03
04							04
05	$D/M_1\beta$	.4000	.4000				05
06	$5/\beta$	.5000	.5000				06
07	$D/10M_2\beta$	.5000	.5000				07
08	$D/10M_2\beta$	.5000	.5000				08
09							09
10	$K_1/50M_2\beta$	1.000	1.000				10
11	$K_2/500M_2\beta$	.5000	.5000				11
12	$K_1/5M_1\beta$	.8000	.8000				12
13	$K_2X_3/500M_2\beta$	.1250	.2083			$X_3 = 3"$ FOR ST	13
14							14
15	$0.2\dot{X}_{20}/10$	.2000	REMOVE			STATIC TEST I.C.	15
16							16
17							17
18							18
19							19
20							20
21							21
22							22
23							23
24							24
25							25
26							26
27							27
28							28
29							29

FIGURE 3.6-7 TR-48 POTENTIOMETER ASSIGNMENT SHEET



NOTES:

1. ALL PATCH CORDS TO ST REFERENCE ARE REMOVED WHEN CHECK IS COMPLETED.
2. VOLTAGES IN RECTANGLES ARE STATIC CHECK VOLTAGES.

FIGURE 3.6-8 STATIC CHECK PROGRAM

A4720

TR-48 AMPLIFIER ASSIGNMENT SHEET

DATE _____ PROBLEM _____

AMP NO.	FB	FUNCTION, AND/OR VARIABLE	STATIC CHECK				NOTES
			CALCULATED		MEASURED		
			CHECK PT.	OUTPUT	CHECK PT.	OUTPUT	
00	S	$-10X_1$		-10		-10	
01	10K	CHECK AMPL. (-1/10)					
02	INT	$-2\dot{X}_1$	-28	-10	+2.8*	-10	* CHECK AMPLIFIER GAIN -1/10
03	INT	$+10X_1$	-5	+10	+5	+10	
04							
05	S	$+10X_2$		-10		-10	
06	INT	$+0.2\dot{X}_2$	-37.5	-2	+3.75*	-2	"
07	INT	$-10X_2$	-10	+10	+10	+10	
08							
09							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							

FIGURE 3.6-9. TR-48 AMPLIFIER SETUP SHEET

The check points of the integrator can be quickly checked by making use of a "check amplifier". For example, remove the SJ to SJ connection for integrator 02 and connect the summing junction of the four input resistors to the base of amplifier 01 (which, in this case, is not being used in the problem). Since amplifier 01 has a 10K feedback resistor, its gain is -1/10 and its output should measure +2.8 volts. The circuit is shown in Figure 3.6-10.

If all the voltages on the patched computer program check against the calculated values, then the patching, pot settings, and amplifier gains are verified.

If the check point voltage of an integrator is less than ten volts, the gain of the check amplifier is increased to -1. The measured check point values and the gain of the check amplifier are listed on the amplifier set-up sheet.

7. A NON-LINEAR PROBLEM

The next example is supplied through the courtesy of the Engineering Department of E.I. DuPont de Nemours and Company, Wilmington, Delaware. Again the primary concern is to get the problem onto the computer.

a. Problem Description

A surge tank must accommodate fluctuations in flow of effluent from a plant. The outlet line from the tank is terminated by a weir, and the flow goes to a river. The system can be represented as shown in Figure 3.7-1.

The tank is in service and operates satisfactorily with two pumps feeding into the tank. Expansion of the process calls for the addition of another pump. A steady state calculation shows that the tank will not overflow with all three pumps operating. The question is raised whether the tank might overflow before the mass of water in the outlet line could accelerate to the final discharge rate. If this occurs, additional outflow or tank capacity must be provided. Operating considerations indicate that all pumps have the same capacity and that the third pump will not start until well after the first two have started.

The system is described by three equations:

Material Balance in Tank: (ft^3/sec) $$\frac{dH_T}{dt} = \frac{1}{A_T}(NQ_A - Q_L) \qquad \text{(EQ. 3.7-1)}$$

Force Balance: (lb) $$(H_T - H_p)\rho A_L = \left(\frac{A_L L \rho}{g}\right)\left(\frac{d}{dt}\frac{Q_L}{A_L}\right) \qquad \text{(EQ. 3.7-2)}$$

Empirical Formula: (ft) For Head Loss Due to Pipe Friction $$H_p = 0.0185\, Q_L + 0.000036\, Q_L^2 \qquad \text{(EQ. 3.7-3)}$$

N = number of pumps operating

Q_A = flow from one pump, ft^3/sec

Q_L = outflow from line, ft^3/sec

H_T = height of liquid in tank, above weir, ft

H_p = friction head loss in pipe, ft

t = time, sec

A_T = cross sectional area of tank, ft^2

A_L = cross sectional area of line, ft^2

L = length of line, ft

ρ = density of effluent, lb/ft^3

g = gravitational constant, ft/sec^2

The system, parameters are:

$A_T = 470\ ft^2$ $\qquad$ $Q_A = 90\ ft^3/sec$

$A_L = 12.6\ ft^2$ $\qquad$ $N = 1, 2, 3$

$L = 665$ ft $\qquad$ $H_T < 9$ ft, to avoid overflow

$g = 32.2\ ft/sec^2$

Design a computer program to study this system, switch in the pumps with function switches. Does the present tank have sufficient capacity? If not, how high must the tank be? Are there any other possible solutions aside from increasing the height of the tank?

b. Preliminary Considerations

The three system equations can be reduced to two by substituting Equation 3.7-3 into Equation 3.7-2. Rewriting the resulting equations so that the highest derivative appears alone on the left-hand side:

$$\dot{H}_T = \frac{1}{A_T}(NQ_A - Q_L) \qquad \text{(EQ. 3.7-4)}$$

$$\dot{Q}_L = \frac{gA_L}{L}(H_T - 0.0185\ Q_L - 0.000036\ Q_L^2) \qquad \text{(EQ. 3.7-5)}$$

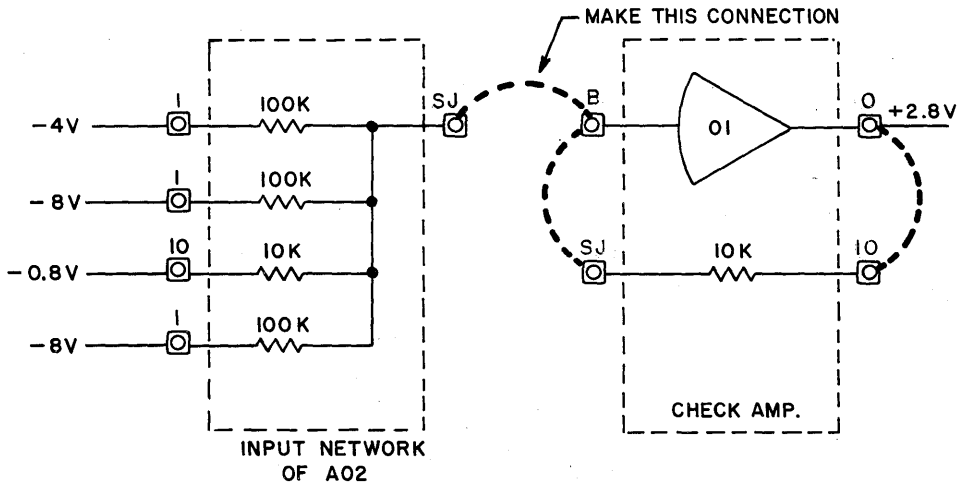


FIGURE 3.6-10 CHECK AMPLIFIER PATCHING TO MONITOR INTEGRATOR OR CHECK POINT, TYPICAL

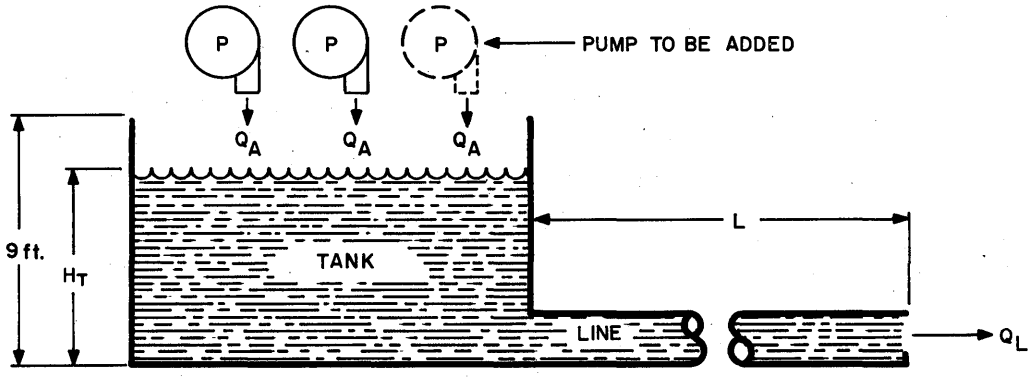


FIGURE 3.7-1. SURGE TANK, SIMPLIFIED SYSTEM DIAGRAM.

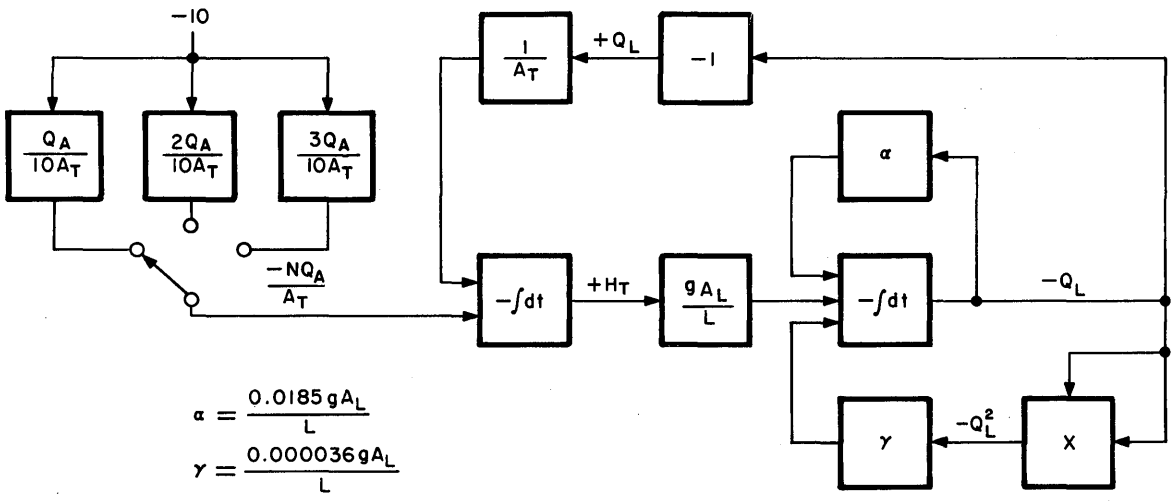


FIGURE 3.7-2 MATHEMATICAL BLOCK DIAGRAM

The mathematical block diagram is shown in Figure 3.7-2. One possible arrangement for switching the pumps is shown. Note that Q_A is a constant and need not be scaled.

Equation 3.7-5 can be used to determine the steady state level of the head ($NQ_A = Q_L$) with the following results:

$$N = 1 \quad H_T = 1.96 \text{ ft}$$

$$N = 2 \quad H_T = 4.5 \text{ ft}$$

$$N = 3 \quad H_T = 7.62 \text{ ft}$$

The computer results should confirm these steady state levels.

c. Scaling

The maximum value of the inflow is given as 270 ft^3/sec (3 pumps on). The maximum value of Q_L is not known; it may be greater than the inflow due to surges in the tank. The maximum value of Q_L will be estimated at about twice that of the maximum inflow, say 500 ft^3/sec. This value may be changed later if the amplifier voltage representing Q_L is extremely high or low.

The maximum allowable value of H_T, before tank overflow, is 9 feet. If H_T is scaled at this level and the tank overflows due to surges, the amplifier producing H_T will overload. It would then be impossible to determine the amount of additional tank capacity required. In order to avoid this difficulty, assume that extra capacity already exists, i.e., the tank is about twice as high, say 20 feet. Estimates of $\dot{H}_T$ and $\dot{Q}_L$ are not required since these variables are of no interest and will appear only as inputs to integrators; they may be therefore, scaled at the same level as H_T and Q_L. The amplitude scale factors and the computer variables are shown in Figure 3.7-3.

The scaled equations are obtained by substituting the computer variables into Equations 3.7-4 and 3.7-5.

Variable	Est. Max. Value	Scale Factor	Computer Variable
Q_L	500 ft^3/sec	$\frac{10}{500}$	$[0.02\ Q_L]$
H_T	20 ft	$\frac{10}{20}$	$[0.5\ H_T]$
$\dot{Q}_L$	Scale to Level	of Q_L	$[0.02\ \dot{Q}_L]$
$\dot{H}_T$	Scale to Level	of $\dot{H}_T$	$[0.5\ \dot{H}_T]$

Figure 3.7-3. Scale Factors

$$[0.5\dot{H}_T] = \frac{0.5}{A_T} NQ_A - \frac{0.5}{0.02A_T}[0.02Q_L] = \frac{NQ_A}{20A_T}\left\{10\right\} - \frac{25}{A_T}[0.02Q_L] \qquad \text{(EQ. 3.7-6)}$$

(Where the ten in braces refers to reference voltage which is used to generate the constant term NQ_A/A_T.)

$$[0.02\dot{Q}_L] = \frac{0.02gA_L}{0.5L}[0.5H_T] - \frac{0.02(0.0185)gA_L}{0.02L}[0.02Q_L] - \frac{0.02(0.000036)gA_L}{(0.02)\ (0.02)L}[0.02Q_L]^2$$

$$[0.02\dot{Q}_L] = \frac{0.04gA_L}{L}[0.5H_T] - \frac{0.0185gA_L}{L}[0.02Q_L] - \frac{0.018gA_L}{L}\frac{[0.02Q_L][0.02Q_L]}{10}$$

(EQ. 3.7-7)

(The square term for Q_L is arranged so that the scale factor of 1/10 inherent in multiplication is considered.)

The low value of the coefficients in Equations 3.7-6 and 3.7-7 indicates a long solution time, therefore, time scaling is desirable. Each of the terms on the right-hand side of these equations appears as an input to an integrator. Time scaling is accomplished by dividing all integrator inputs by an appropriate factor β, where β is selected to give reasonable pot settings. In this case let $\beta = 0.1$.

d. Computer Diagram

The computer diagram is shown in Figure 3.7-4. The function switches make it possible to switch in the pumps, one at a time, in case a particular timing sequence will give a more satisfactory response. Four gains of one are needed for integrator 02. This can be accomplished by borrowing a resistor from an unused amplifier and connecting it to the summing junction of the integrator. Since Q_2 can never be negative, only one squaring card of the X^2 DFG is used. Integrator 15 is used to provide a time-base for plotting H_T as a function of time on an X-Y plotter.

e. Checking the Computer Program

Following the steps used in the previous example:

(1) Calculate all potentiometer settings and list them on the potentiometer set-up sheet.

(2) Assume convenient values for the variables.

$H_T = 20$ ft

$Q_L = 500$ ft^3/sec

$Q_A = 90$ ft^3/sec (one pump on)

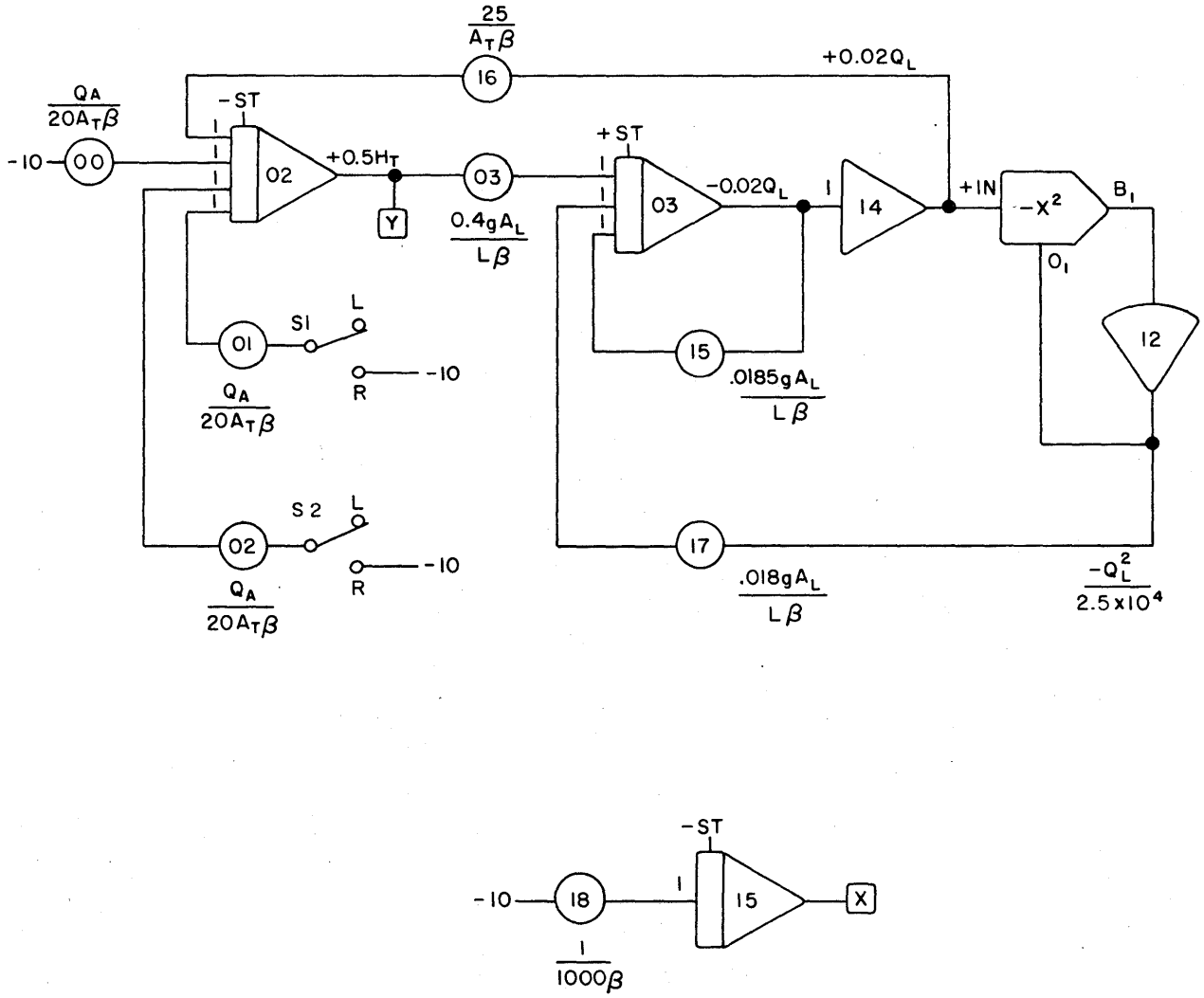


FIGURE 3.7-4 COMPUTER DIAGRAM; SURGE TANK

Establish these values on a copy of the computer diagram. On the basis of the inputs and initial conditions established, determine the voltage at the output of each computing component, and the voltages representing the higher derivative. The voltages representing $\dot{H}_T$ and $\dot{Q}_L$ at the input to integrator 02 and 03 respectively are:

$$\frac{-0.5\dot{H}_T}{\beta} = -10(.096)(1) + 10(.532)(1) = +4.36 \text{ volts}$$

$$\frac{+0.02\dot{Q}_L}{\beta} = +2.44(1) - 1.13(1) - 1.10(1) = +0.21 \text{ volts}$$

(3) Substitute the assumed values of the variables into Equations 3.7-4 and 3.7-5, calculate the values of the highest derivatives.

$$\dot{H}_T = \frac{1}{470}(90 - 500) = -0.8723 \text{ ft/sec}$$

$$\dot{Q}_L = \frac{(32.2)(12.6)}{665}[20 - 0.0185(500) - 0.000036(500)^2] = 1.067 \text{ ft}^3/\text{sec}^2$$

therefore

$$\frac{-0.5\dot{H}_T}{\beta} = \frac{-0.5(-0.8723)}{0.1} = +4.362 \text{ volts}$$

$$\frac{+0.02\dot{Q}_L}{\beta} = \frac{+0.02(1.067)}{0.1} = +0.213 \text{ volts}$$

which checks the computer diagram.

(4) Check that the outputs of the amplifiers are labeled correctly by substituting the assumed initial values into the expression for the amplifier output. Prepare amplifier set-up sheets.

(5) Place the computer in the RS mode and verify that the calculated and measured outputs agree. This checks the patching, pot settings, etc.

(6) Remove all static test reference leads, check that the integrators are reconnected properly and prepare for run one.

The steady state values of H_T for N = 1, 2, 3 were determined earlier; the computer should confirm these levels. Several other check cases can also be deter-

mined. For example, assume the system is in equilibrium with one pump operating; then pump two is switched on. What would be the instantaneous rate of change of the head (ft/sec) in the tank?

Consider the following possible solutions; increase the height of the tank, increase the tank diameter, increase the pipeline diameter, drive the third pump with a two-speed motor, etc. (The addition of a third pump identical to the first two may be due to plant standardization and the pump capacity may be arbitrary.) Find the largest capacity that can be added and still prevent overflow.

A4721

TR-48 AMPLIFIER ASSIGNMENT SHEET

DATE _____ PROBLEM _____

AMP NO.	FB	FUNCTION, AND/OR VARIABLE	STATIC CHECK				NOTES
			CALCULATED		MEASURED		
			CHECK PT.	OUTPUT	CHECK PT.	OUTPUT	
00							
01							
02	INT	$+0.5\,H_T$	-4.36^*	+10.00			*WITH CHECK AMPLIFIER GAIN = −1
03	INT	$-0.02\,Q_L$	-0.21^*	−10.00			"
04							
05							
06							
07							
08							
09							
10							
11							
12	HG	$-Q_L^2/2.5 \times 10^4$		-10.00			
13							
14	S	$+0.02\,Q_L$		+10.00			
15	INT	TIME BASE	$+0.10^*$	+10.00			"
16							
17							
18							
19							
20							
21							
22							
23							

FIGURE 3.7-5. AMPLIFIER ASSIGNMENT SHEET; SURGE TANK

A4716

TR-48 POTENTIOMETER ASSIGNMENT SHEET

DATE _____ PROBLEM _____

POT NO.	PARAMETER DESCRIPTION	SETTING STATIC CHECK	SETTING RUN NO.1	SETTING RUN NO.	SETTING RUN NO.	NOTES $\beta = 0.1$	POT NO.
00	$Q_A/20A_T\beta$	.096 →			→		00
01	$Q_A/20A_T\beta$	.096 →			→		01
02	$Q_A/20A_T\beta$	.096 →			→		02
03	$0.4g\,A_L/L\beta$	.244 →			→		03
04							04
05							05
06							06
07							07
08							08
09							09
10							10
11							11
12							12
13							13
14							14
15	$0.0185g\,A_L/L\beta$	.113 →			→		15
16	$25/A_T\beta$	.532 →			→		16
17	$0.018g\,A_L/L\beta$	.110 →			→		17
18	$1/1000\beta$	.010 →			→		18
19							19
20							20
21							21
22							22
23							23
24							24
25							25
26							26
27							27
28							28
29							29

FIGURE 3.7-6. POTENTIOMETER ASSIGNMENT SHEET; SURGE TANK

SECTION IV

ADVANCED TECHNIQUES

1. FUNCTION GENERATION

It is often necessary to generate functions of the independent variable (time) or of a dependent variable (voltage). The following techniques are frequently useful.

a. Analytic Functions

If a function is given by an analytic expression, such as e^{kx}, sin kx, etc., a differential equation can often be found whose solution is the desired function. Mechanizing the differential equation will then generate the function.

(1) Generation of Ae^{-kt}

Let $y = Ae^{-kt}$

then $\dot{y} = -kAe^{-kt} = -ky$ (EQ. 4.1-1)

The computer circuit is shown in Figure 4.1-1. The function $y = Ae^{+kt}$ is generated by including an inverter in the loop. Since this is an expanding exponential function, the amplifiers will eventually overload. The function must be scaled carefully so that the overload does not occur before the maximum running time, which is selected in advance.

(2) Generation of A sinωt or A cosωt

Let $y = A \sin\omega t$ and $z = A \cos\omega t$

then $\dot{y} = \omega z$ and $\dot{z} = -\omega y$ (EQ. 4.1-2)

The computer circuit shown in Figure 4.1-2 arises from the coupled equations above or as a solution of the second-order equation $\ddot{y} = -\omega^2 y$.

(3) Generation of $y = e^{kx}$ where x is a problem variable. The desired equation is similar to Section (1) above except that x is a voltage. Since x is a function of time:

$$\dot{y} = ke^{kx}\dot{x} = k\dot{x}y \qquad \text{(EQ. 4.1-3)}$$

The computer circuit is shown in Figure 4.1-3. Note that the input is $\dot{x}$ not x. This rate input is typical of such systems. In most cases, $\dot{x}$ is available from the circuit that is generating x.

(4) Generation of A sin kx where x is a dependent problem variable

$$\text{Let } y = A \sin kx \qquad \text{and} \qquad z = A \cos kx$$

$$\dot{y} = (k\ A \cos kx)\ \dot{x} \qquad \dot{z} = (-K\ A \sin kx)\ \dot{x}$$

$$\dot{y} = kz\dot{x} \qquad \dot{z} = -ky\dot{x} \qquad \text{(EQ. 4.1-4)}$$

The computer circuit is shown in Figure 4.1-4.

b. Techniques Involved in Using the DFG

If an analytic expression cannot be found for the function to be generated, then use of a DFG is indicated. Since the DFG provides a straight-line segment approxmation to a curve, a certain error is inevitable, and careful programming is necessary to minimize this error. Often it is not a good idea to generate the desired function directly on a DFG. Instead the function should be approximated by a simple analytic expression and the DFG used to generate the error or correction term. The following examples illustrate the technique.

Assume the function f(x) in Figure 4.1-5 is to be generated. Since $0 \leq x \leq 10$ and $0 \leq f(x) \leq 75$, scale factors of 1 and 1/10 could be used resulting in [x] and [1/10 f(x)] as computer variables.

A DFG could be set up to generate [1/10 f(x)] directly. However, better accuracy may be obtained by observing that f(x) has an average value of approximately 70. Considering deviations from this mean value,

$$\text{Let } f_1(x) = f(x) - 70 \qquad \text{(EQ. 4.1-5)}$$

Then $-5 \leq f_1(x) \leq +5$, and f_1 may be scaled as $[2f_1(x)]$. Generate $[2f_1(x)]$ on the DFG, and then obtain f(x) by solving Equation 4.1-5 for f(x).

$$f(x) = f_1(x) + 70 \qquad \text{(EQ. 4.1-6)}$$

Equation 4.1-6 must be scaled, just like any other equation. For computer variables [1/10 f(x)] and $[2\ f_1(x)]$ the scaled equation is:

$$\left[\frac{1}{10}\ f(x)\right] = \frac{1}{20}\ [2F_1(x)] + 7 \qquad \text{(EQ. 4.1-7)}$$

Figure 4.1-6 gives the circuit diagram. Note that any drift or noise occurring in generating $f_1(x)$ on the DFG is attenuated, along with $f_1(x)$ itself by a factor of 20.

c. Curve Follower and BIVAR

A curve follower is available to enable the X-Y Plotter to be used as a function generator. The curve to be generated is set up by using a fine wire (#18) taped

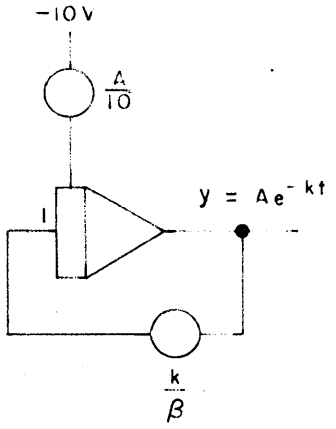


FIGURE 4.1-1. GENERATING THE FUNCTION Ae^{-kt}

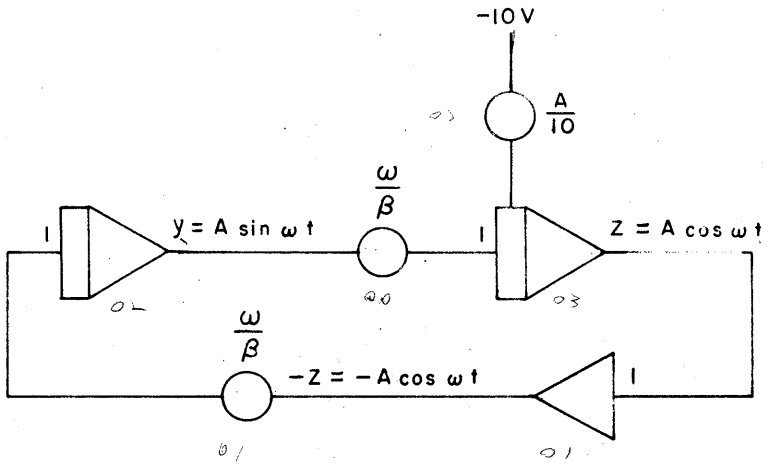


FIGURE 4.1-2. GENERATING THE FUNCTION A sin ωt

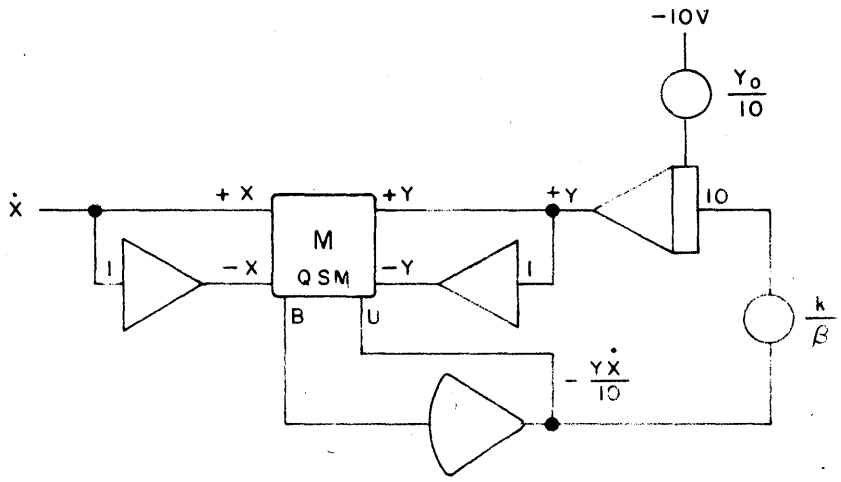


FIGURE 4.1-3. GENERATING THE FUNCTION $Y = e^{k\dot{x}}$

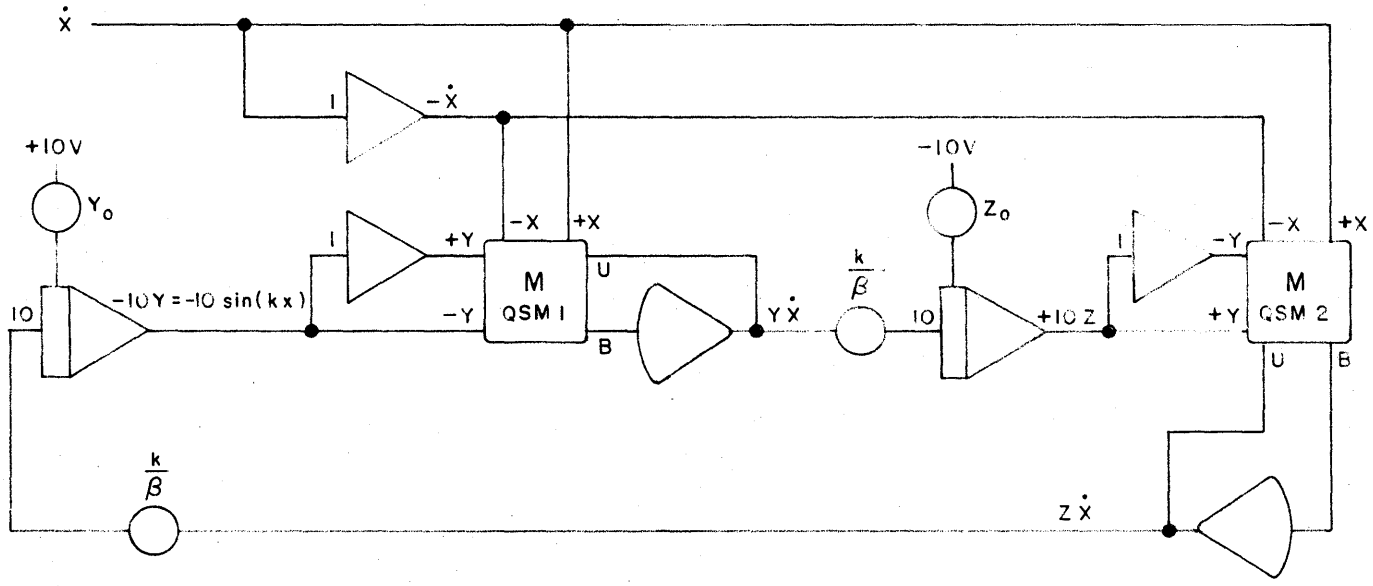


FIGURE 4.1-4. CONTINUOUS RESOLUTION CIRCUIT; EQUATION 4.1-4.

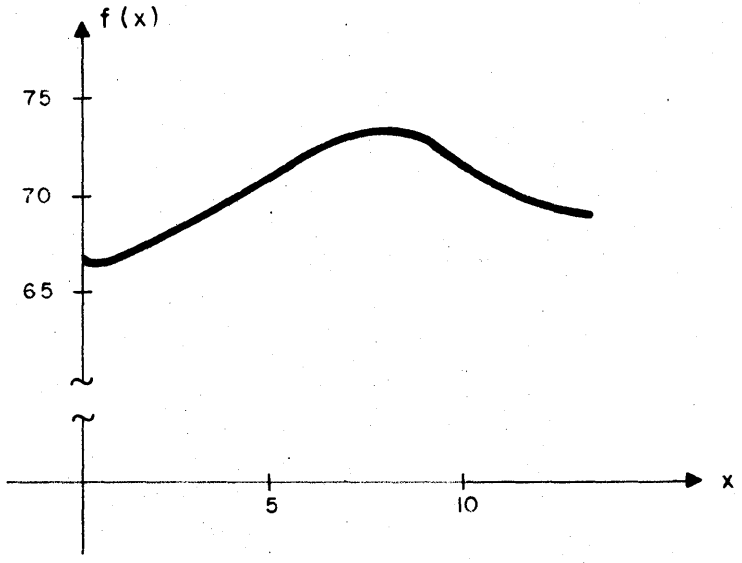


FIGURE 4.1-5. SAMPLE FUNCTION CURVE

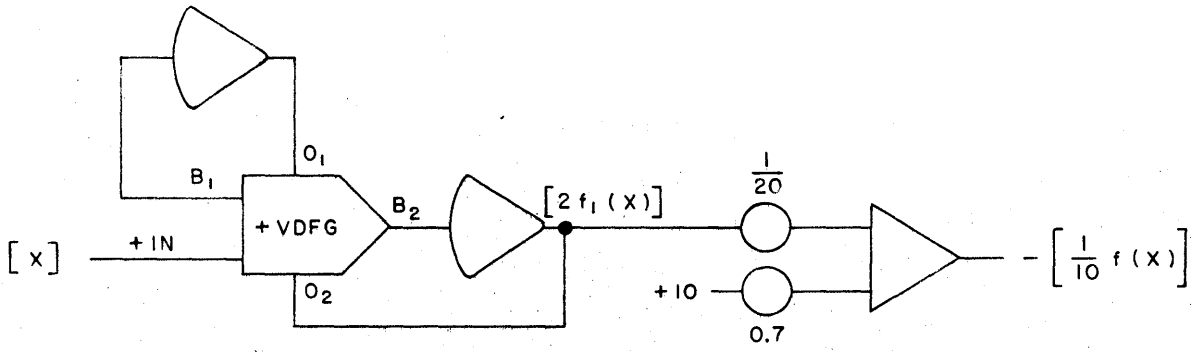


FIGURE 4.1-6. COMPUTER DIAGRAM; EQUATION 4.1-7.

over the desired curve drawn on the plotting surface or by drawing the curve initially with conducting ink. The wire or conducting ink curve is energized with a high-frequency signal; the pen is replaced by a sensing unit which tracks the curve. As the arm is moved back and forth in response to the variable x, the sensing unit remains above the curve so that its displacement is f(x). The pen potentiometer is energized with reference voltage, thus the sensing unit output is proportional to f(x). If a variable y is used to energize the pen potentiometer instead of reference, the output is proportional to y·f(x), enabling the curve follower to perform multiplication and function generation in one step.

A BIVAR (Bi-Variant Function Generator) is also available to generate functions of two variables.

2. TRANSFER FUNCTION SIMULATION

Many engineering problems dealing with linear time-invariant systems are conveniently described in terms of transfer functions. If the transfer functions of a system are available, one may readily simulate the system on the TR-48. Two general methods are available; first, the transfer function may be treated as a differential equation and programmed directly using standard amplifiers and potentiometers; second, passive element networks, containing resistors and capacitors, may be used as input and feedback impedances for amplifiers to produce desired transfer functions. The first method, in general, uses more amplifiers than the second but is more convenient to use, especially with unfactored transfer functions. The intermediate derivatives are readily available and the introduction of initial conditions does not cause complications as it does in the second case. On the other hand, the use of RC networks affords a saving in the number of amplifiers used. Both methods are illustrated here. (The reader should refer to the literature cited in the Bibliography for a more comprehensive discussion of transfer function simulation.)

a. Transfer Function Simulation Using Standard Amplifiers and Potentiometers

If a transfer function is treated as a differential equation, it can be programmed directly. As an example, consider the transfer function in Equation 4.2-1.

$$G(p) = \frac{E_o(p)}{E_1(p)} = \frac{1}{1+\tau p} \qquad \text{(EQ. 4.2-1)}$$

Solving for the highest derivative:

$$pE_o = \frac{E_1}{\tau} - \frac{E_o}{\tau} \qquad \text{(EQ. 4.2-2)}$$

Assuming that the highest derivative exists at the input to an integrator, the computer circuit shown in Figure 4.2-1 is obtained.

Occasionally a system is represented by an unfactored transfer function, such as:

$$G(p) = \frac{E_o(p)}{E_1(p)} = \frac{Ap^2+Bp+C}{p^3+Dp^2+Ep+F} \qquad \text{(EQ. 4.2-3)}$$

The following approach is recommended for programming a transfer function of this type resulting in the minimum number of components. First, expand the equation into differential equation form, giving:

$$p^3E_o+Dp^2E_o+EpE_o+FE_o = Ap^2E_1+BpE_1+CE_1 \qquad \text{(EQ. 4.2-4)}$$

Next, divide the equation by p^{n-1}, where n equals the highest power of p. (Here the divisor is p^2.)

$$pE_o+DE_o+\frac{EE_o}{p}+\frac{FE_o}{p^2} = AE_1+\frac{BE_1}{p}+\frac{CE_1}{p^2} \qquad \text{(EQ. 4.2-5)}$$

Solving the equation for the highest derivative and grouping terms according to powers of p:

$$pE_o = AE_1 -DE_o + \frac{1}{p}(BE_1 -EE_o) + \frac{1}{p^2}(CE_1 -FE_o) \qquad \text{(EQ. 4.2-6)}$$

Keeping in mind that the notation 1/p represents an integration, the equation can then be programmed to yield the computer circuit shown in Figure 4.2-2.

b. Transfer Function Simulation Using RC Networks

The transfer function of the operational amplifier is:

$$\frac{E_o}{E_i} = -\frac{Z_f}{Z_{in}} \qquad \text{(EQ. 4.2-7)}$$

where Z_f and Z_{in} are the short-circuit transfer impedances of the feedback and input networks. (The short-circuit transfer impedance of a network is defined as the input voltage-output current ratio when the output terminals of the network are short-circuited.) Therefore, the relationship expressed in Equation 4.2-7 can be used to generate transfer functions of the form

$$G(p) = \frac{M(p)}{N(p)}$$

where M(p) and N(p) are the short-circuit transfer impedances of Z_f and Z_{in} respectively. A table of short-circuit admittances of some standard networks is included in Appendix 7 and is used in the illustrative example which follows.

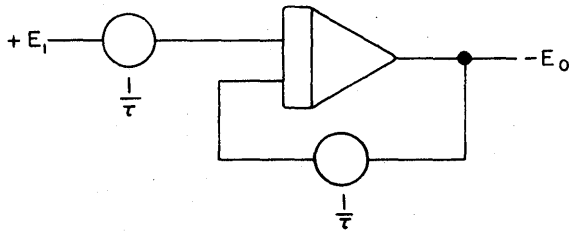


FIGURE 4.2-1 COMPUTER DIAGRAM; EQUATION 4.2-2

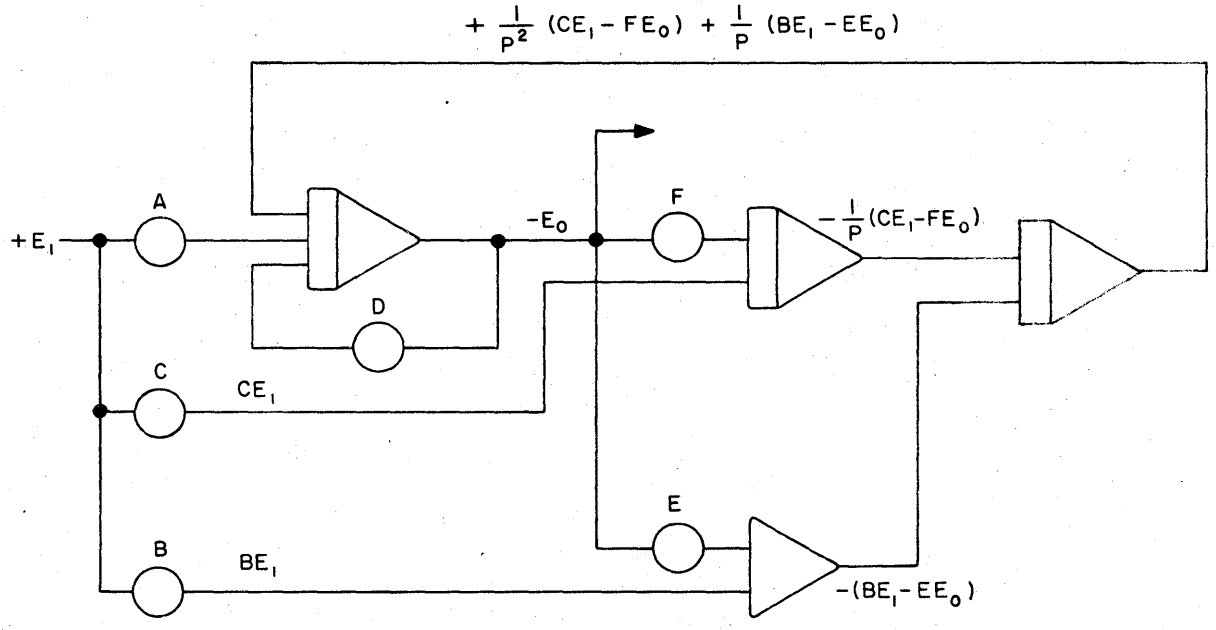


FIGURE 4.2-2 COMPUTER DIAGRAM; EQUATION 4.2-6

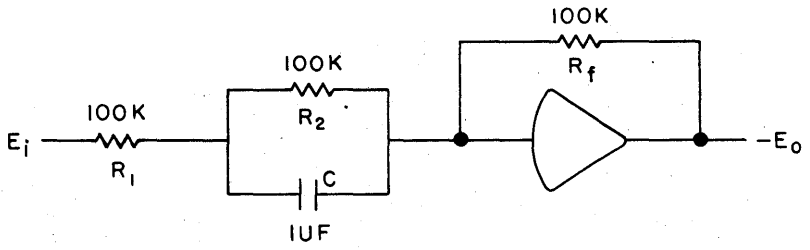


FIGURE 4.2-3 SIMULATION OF TRANSFER FUNCTION; $G(p) = \frac{(1+0.1p)}{2(1+0.05p)}$

Example:

Simulate the transfer function

$$G(p) = \frac{(1+0.1p)}{2(1+0.05p)}$$

The short-circuit admittance of network four is given as

$$Y_{ss} = \frac{1}{Z_{ss}} = \frac{1(1+pT)}{A(1+p\theta T)} \qquad \theta < 1$$

where $A = R_1 + R_2$, $T = R_2C$, $\theta = \frac{R_1}{R_1 + R_2}$

Using this network as an input network to an amplifier that has R_f as a feedback network produces the required transfer function. (See Figure 4.2-3.)

$$\frac{E_o}{E_i} = -\frac{Z_f}{Z_{in}} = -\frac{R_f}{A}\frac{(1+pT)}{(1+p\theta T)}$$

$$\frac{R_f}{R_1+R_2} = \frac{100K}{100K+100K} = \frac{1}{2}$$

$$T = R_2C = (100\times10^{3})\ (1\times10^{-6}) = 0.1$$

$$\theta T = \frac{R_1}{R_1+R_2}(R_2C) = \frac{0.1}{2} = 0.05$$

3. REPRESENTATION OF DISCONTINUITIES

Frequently, non-linear effects do not require multipliers and function generators for adequate representation on the computer. These effects can be described graphically by discontinuous straight line input-output relationships. Some of the most common discontinuities occurring in physical systems are simple limiting, coulomb friction, hysteresis, and gear backlash. All can be represented reasonably well on the computer by standard circuits containing diodes and/or comparators. Dry friction and hysteresis are discussed as typical applications; several other useful circuits are shown in the Appendix 8.

Figure 4.3-1 shows both a diode circuit and a comparator circuit for simulating

coulomb friction. In equation form, coulomb friction can be represented as:

$$f = +c \qquad \frac{dx}{dt} < 0$$

$$f = -c \qquad \frac{dx}{dt} > 0 \qquad \text{(EQ. 4.3-1)}$$

The diode circuit (Figure 4.3-1b) to produce this characteristic is a high-gain limited amplifier. Since the gain of the amplifier is very high with no limiting, the output will very rapidly swing in one direction or the other, depending upon the input, until one of the diodes conducts. The diode conduction effectively introduces a low resistance in the feedback path of the amplifier, reducing its gain very sharply to a very small value. However, the flat parts of the static friction characteristic will have a slight rise since the gain of the limited amplifier is not exactly zero during the diode conduction because of the finite resistance of the potentiometer in the feedback circuit. If this rise in the output characteristic is considered objectionable, a low value of K (possibly 1) should be used.

The simulation of static friction using comparators may be accomplished as shown in Figure 4.3-1c. If V_1 is positive, $V_o = -c$. If V_1 is negative, $V_o = +c$. The only error present in the system is in the vicinity of $V_1 = 0$; here V_o will be 0 over only a small range, however, this does not usually interfere with satisfactory operation in the overall circuit.

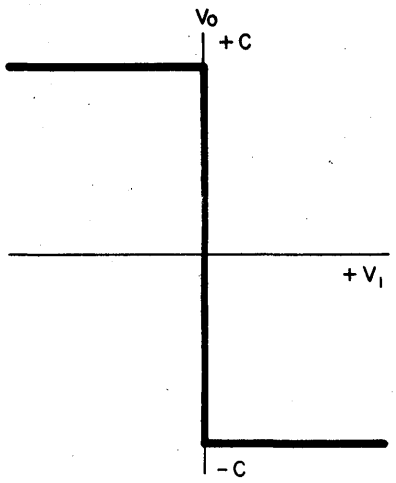
Figure 4.3-2 shows a diode circuit which can be used to represent hysteresis, or back-lash.

This circuit will generate a hysteresis characteristic, but with certain high frequency limitations. If the input V_1 increases from zero, the output V_o will remain at zero until the difference between V_1 and V_o is a. When this occurs the upper diode will conduct and the integrator will integrate at a rate of

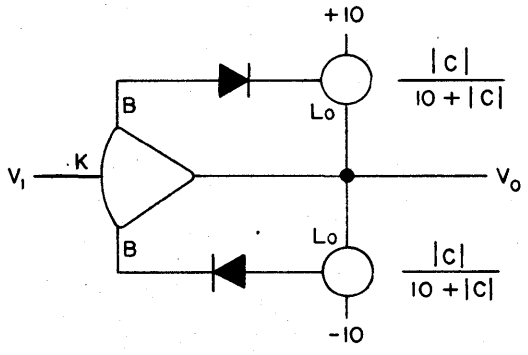
$$\frac{V_1 - V_o - a}{[R_p + KR_a]C} \text{ volts per second,}$$

where R_p is the forward resistance of the diode,
R_a is the total resistance of the attenuator,
K is the setting of the attenuator,
C is the value of integrating capacitor used.

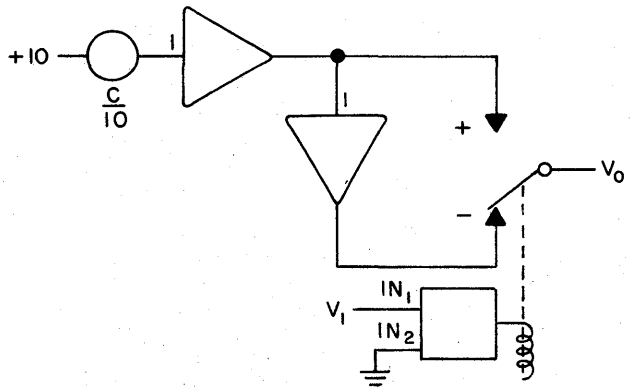
The circuit in this phase behaves exactly like a simple first-order time lag with a time constant $[R_p + KR_a]$ C. However, since $[R_p + KR_a]$ will normally be very low ($< 10K\ \Omega$) and C may also be made small, the time constant is very small and can usually be considered insignificant. When V_1 starts decreasing, the upper diode will cut off and V_o will remain constant until an error of -a is developed between V_1 and V_o. The lower diode will then conduct causing V_o to decrease. The initial value of V_o can be set as an initial condition on the integrator. The integrator feedback capacitor should be selected so that the resulting time constant is small.



a. SATURATION OR COULOMB FRICTION



b. FEEDBACK LIMITER



c. RELAY LIMITER

FIGURE 4.3-1 COMPUTER MECHANIZATION OF SATURATION, OR COULOMB FRICTION

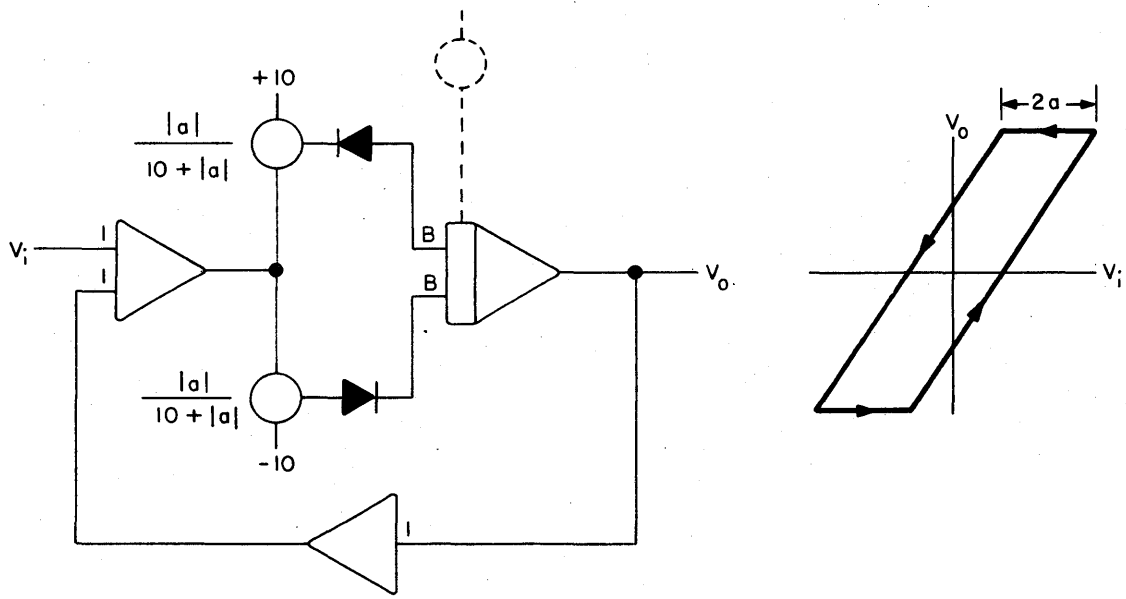


FIGURE 4.3-2 COMPUTER MECHANIZATION OF HYSTERESIS OR BACKLASH

4. PARTIAL DIFFERENTIAL EQUATIONS

Partial differential equations can be successfully solved on the analog computer. However, a mathematical manipulation of the equation is necessary since the analog computer will integrate with respect to only one variable, i.e., time. By using finite-difference approximations for the derivatives with respect to all but one variable, a set of ordinary differential equations may be written.

This technique can be illustrated by using it to solve the equation

$$\frac{\partial^2 y}{\partial x^2} = \frac{\rho}{T}\frac{\partial^2 y}{\partial t^2} \qquad \text{(EQ. 4.4-1)}$$

Equation 4.4-1 describes the motion of an elastic string, where ρ is the mass per unit length of the string, T is the string tension, and y(x,t) is the transverse displacement of the string at time t and at a distance x from one end. For such an equation, the values of y and $\partial y/\partial t$ must be specified for all x at t = 0, and the value of y at both ends of the string must be specified for all t. These are the initial conditions and boundary values of the problem respectively.

Assuming that the initial conditions and boundary values are given, the problem can be approached by considering the independent variable x at discrete points $x_0, x_1, \ldots, x_n$, and writing $y_i(t)$ for $y(x_i,t)$. An ordinary differential equation can be written for each $y_i(t)$ by replacing the space derivatives (derivatives with respect to x) by finite-difference approximations. The resulting system of ordinary differential equations can be solved on an analog computer.

To obtain finite-difference expressions for space derivatives, consider the ratio

$$\frac{y(x+\Delta x,t) - y(x,t)}{\Delta x}$$

This is the slope of the secant line in Figure 4.4-1, and represents the average rate of increase of y over the interval from x to x + Δx, for a fixed t. If Δx is small, this is an approximation to $\partial y/\partial x$ at $(x + \Delta x/2, t)$, since $x + \Delta x/2$ is the midpoint of this interval. A similar approximation holds for the interval from x - Δx to x, whose midpoint is $x - \Delta x/2$. Hence the following approximations are obtained:

$$\left.\frac{\partial y}{\partial x}\right|_{(x + \frac{\Delta x}{2},t)} \cong \frac{y(x + \Delta x,t)-y(x,t)}{\Delta x} \qquad \text{(EQ. 4.4-2)}$$

$$\left.\frac{\partial y}{\partial x}\right|_{(x- \frac{\Delta x}{2},t)} \cong \frac{y(x,t) - y(x -\Delta x,t)}{\Delta x} \qquad \text{(EQ. 4.4-3)}$$

The accuracy of these approximations depends on the size of Δx. For maximum accuracy, Δx should be as small as possible.

Similarly, $\partial^2 y/\partial x^2$ can be approximated by applying a finite-difference to $\partial y/\partial x$. Since x is midway between $x - \Delta x/2$ and $x + \Delta x/2$:

$$\frac{\partial^2 y}{\partial x^2}(x,t) \approx \frac{\frac{\partial y}{\partial x}(x + \frac{\Delta x}{2},t) - \frac{\partial y}{\partial x}(x - \frac{\Delta x}{2},t)}{\Delta x} \qquad \text{(EQ. 4.4-4)}$$

Replacing the first derivatives by their approximate values given in Equation 4.4-2 and Equation 4.4-3, results in:

$$\frac{\partial^2 y}{\partial x^2}(x,t) \approx \frac{y(x + \Delta,t) - 2y(x,t) + y(x - \Delta x,t)}{(\Delta x)^2} \qquad \text{(EQ. 4.4-5)}$$

This is the desired equation. It expresses the second partial derivative that appears in Equation 4.4-1 in terms of the values of y(x,t) at discrete points, spaced Δx apart.

Next consider the n + 1 points $x_0, x_1, \ldots, x_n$, equally spaced so that $\Delta x = \ell/n$, where ℓ is the length of the string. Equation 4.4-5 then yields:

$$\frac{\partial^2 y_i(t)}{\partial x^2} \approx \frac{y_{i+1} - 2y_i + y_{i-1}}{(\Delta x)^2} \qquad \text{(EQ. 4.4-6)}$$

and combining this with Equation 4.4-1, results in:

$$\ddot{y}_i = \frac{T}{\rho(\Delta x)^2}(y_{i+1} - 2y_i + y_{i-1}) \qquad \text{(EQ. 4.4-7)}$$

Since y_0 and y_n are given as boundary values no equations are needed for them. Suppose the string is stretched taut between two fixed points. Then $y_0 = y_n = 0$ for all t. These boundary values, together with the system of Equation 4.4-7, determines the y_i for all t.

Take n = 5. Then $\Delta x = \ell/5$. The equations become:

$$\ddot{y}_1 = \frac{25\,T}{\rho\ell^2}(y_2 - 2y_1) \qquad \text{(EQ. 4.4-8)}$$

$$\ddot{y}_2 + \frac{25\,T}{\rho\ell^2}(y_3 - 2y_2 + y_1) \qquad \text{(EQ. 4.4-9)}$$

$$\ddot{y}_3 = \frac{25\,T}{\rho\ell^2}(y_4 - 2y_3 + y_2) \qquad \text{(EQ. 4.4-10)}$$

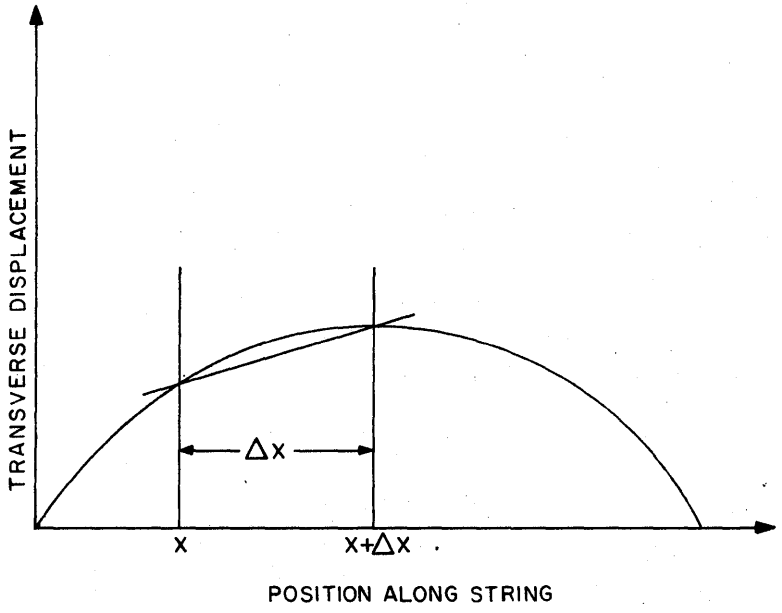


FIGURE 4.4-1 STRING DISPLACEMENT AT A FIXED INSTANT OF TIME

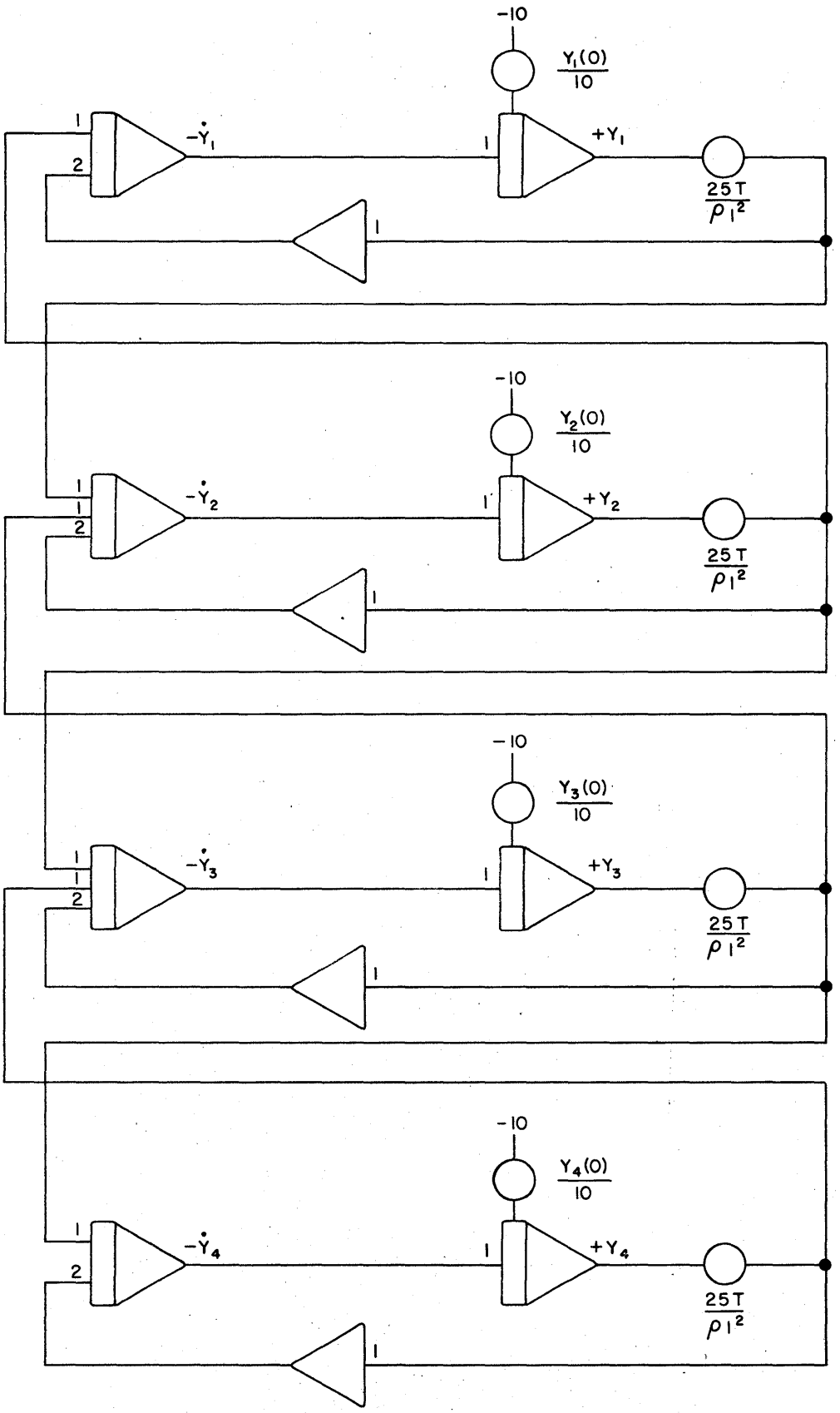


FIGURE 4.4-2 COMPUTER DIAGRAM (UNSCALED); EQUATIONS 4.4-8 THROUGH 4.4-11

$$\ddot{y}_4 = \frac{25\,T}{\rho \ell^2}\,(-2y_4 + y_3) \qquad \text{(EQ. 4.4-11)}$$

Thus by considering the string displacement at discrete points, a system of 4 ordinary differential equations is obtained which can be easily solved on the computer. The appropriate (unscaled) computer diagram is given in Figure 4.4-2.

The above method for solving partial differential equations on the analog computer is the one most frequently used. More information about this technique and others may be found in the following Bibliography.

1. Rogers, A.E. and T.W. Connolly: "Analog Computation in Engineering Design", McGraw-Hill Book Company, Inc., New York 1960

2. Karplus, W.J.: "Analog Simulation", McGraw-Hill Book Company, Inc., New York 1958

3. Jackson, A.S.: "Analog Computation", McGraw-Hill Book Company, Inc., New York 1960

5. THE METHOD OF STEEPEST DESCENTS

The analog computer is basically a device for solving differential equations, which makes it especially valuable for the study of dynamic systems. However, certain essentially static problems, such as the solution of simultaneous algebraic equations (linear or non-linear), transcendental equations, linear and non-linear programming, and curve fitting can also be handled on the analog computer by a number of techniques. One such technique, the method of steepest descents, is finding increasing application. Although the method will be illustrated by solving a trivial algebraic system, its scope of application is much more general.

Consider the set of algebraic equations

$$a_{11}\,x_1 + a_{12}\,x_2 = b_1 \qquad \text{(EQ. 4.5-1)}$$

$$a_{21}\,x_1 + a_{22}\,x_2 = b_2 \qquad \text{(EQ. 4.5-2)}$$

where a_{11} and a_{22} are both positive. Attempting a solution by means of the bootstrap method used for differential equations results in:

$$x_1 = \frac{b_1}{a_{11}} - \frac{a_{12}}{a_{11}}\,x_2 \qquad \text{(EQ. 4.5-3)}$$

$$x_2 = \frac{b_2}{a_{22}} - \frac{a_{21}}{a_{22}}\,x_1 \qquad \text{(EQ. 4.5-4)}$$

A computer circuit for this system is shown in Figure 4.5-1. If a_{12} and a_{21} have the same sign, there will be an even number of amplifiers in the loop. A condition of positive, rather than negative, feedback will then exist, and the circuit will be unstable unless the total loop gain is less than one, that is, unless

$$K = \frac{a_{12}\, a_{21}}{a_{11}\, a_{22}} < 1 \qquad \text{(EQ. 4.5-5)}$$

This requirement is necessary for stability in any loop with an even number of summers and no integrators. If it is violated, an overload will quickly arise, and no solution will be obtained. Loops containing an odd number of summing amplifiers appear to be free of this difficulty. However, this is not necessarily true. When no integrator is present in a loop, the phase shift unavoidably present in the amplifiers will produce high-frequency oscillations if the loop gain is too high, again preventing the circuit from reaching a stable condition. Thus, no matter how many amplifiers are present, one must be very careful to keep the loop gain small if a solution is to be obtained.

For these reasons a naive approach to the solution of algebraic equations is not guaranteed of success. A better approach is to program a set of <u>differential</u> equations whose steady-state solution satisfies the original algebraic equations. In the example given, one can write the differential equations:

$$a_{11}\, x_1 + a_{12}\, x_2 - b_1 + \frac{dx_1}{dt} = 0 \qquad \text{(EQ. 4.5-6)}$$

$$a_{21}\, x_1 + a_{22}\, x_2 - b_2 + \frac{dx_2}{dt} = 0 \qquad \text{(EQ. 4.5-7)}$$

The circuit for these equations may be obtained from Figure 4.5-1 by substituting integrators for the high-gain amplifiers.

A steady state solution, if one exists, may be found by setting dx_1/dt and dx_2/dt equal to zero, and such a solution will clearly satisfy Equations 4.5-1 and 4.5-2. However, if a_{12} and a_{21} have the same sign, the loop will contain an even number of amplifiers, and positive feedback still exists. Again Equation 4.5-5 must be satisfied for stability, as may be seen by analytically solving Equations 4.5-6 and 4.5-7.

The method of steepest descents is also based on the idea of writing a differential equation whose steady-state solution satisfies the algebraic equation. However, this method guarantees stability, and the correct solution is obtained as a steady-state solution with no restrictions on the coefficients.

Consider a system of n equations in m unknowns:

$$f_i\,(x_1, \ldots, x_m)\; b_i \quad i = 1, 2, \ldots, n \qquad \text{(EQ. 4.5-8)}$$

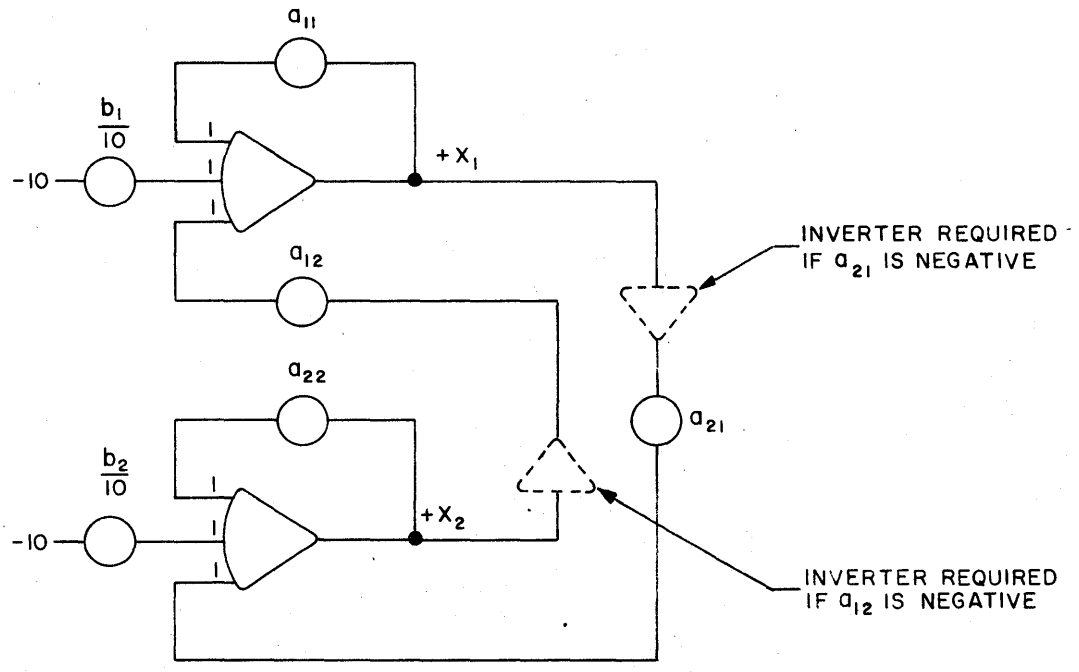


FIGURE 4.5-1 COMPUTER DIAGRAM; EQUATIONS 4.5-3 AND 4.5-4

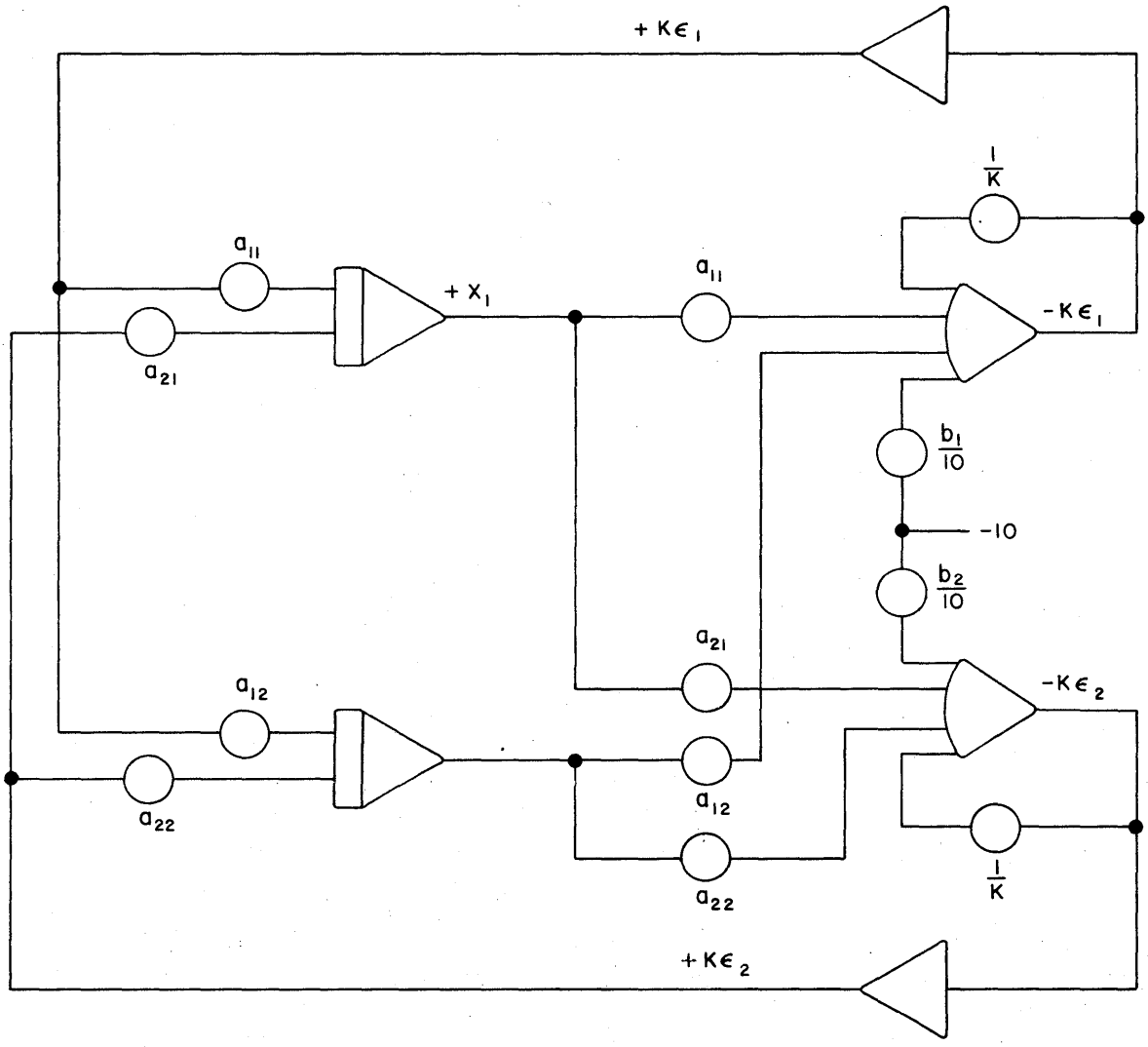


FIGURE 4.5-2 COMPUTER DIAGRAM; EQUATIONS 4.5-17 THROUGH 4.5-20

It is not necessary to assume that the f_i are linear, nor that m = n. By definition,

$$\varepsilon_i (x_1 \ldots x_m) = f_i (x_1 \ldots x_m) - b_i \qquad \text{(EQ. 4.5-9)}$$

$$S (x_1 \ldots x_m) = \sum_{i=1}^{n} \varepsilon_i^2 \qquad \text{(EQ. 4.5-10)}$$

Note that $S(x_1 \ldots x_m) = 0$ if and only if the values $x_1, \ldots, x_m$ satisfy Equation 4.5-8. We want to make the x_j's vary with time in such a way that lim $S \rightarrow 0$ as $t \rightarrow \infty$. Since $S \geqslant 0$, S must decrease, which means that dS/dt should be negative. From Equation 4.5-10:

$$\frac{dS}{dt} = 2 \sum_{i=1}^{n} \varepsilon_i \frac{d\varepsilon_i}{dt} \qquad \text{(EQ. 4.5-11)}$$

Since the ε_i are functions of $x_1, \ldots, x_m$:

$$\frac{d\varepsilon_i}{dt} = \sum_{j=1}^{m} \frac{\partial \varepsilon_i}{\partial x_j} \frac{dx_j}{dt} \qquad \text{(EQ. 4.5-12)}$$

Combining Equations 4.5-11 and 4.5-12:

$$\frac{dS}{dt} = 2 \sum_{i=1}^{n} \varepsilon_i \sum_{j=1}^{m} \frac{\partial \varepsilon_i}{\partial x_j} \frac{dx_j}{dt} \qquad \text{(EQ. 4.5-13)}$$

Upon interchanging the order of summation, Equation 4.5-13 becomes:

$$\frac{dS}{dt} = 2 \sum_{j=1}^{m} \frac{dx_j}{dt} \sum_{i=1}^{n} \varepsilon_i \frac{\partial \varepsilon_i}{\partial x_j} \qquad \text{(EQ. 4.5-14)}$$

The functions $\varepsilon_i (x_1, \ldots x_m)$ and $\partial \varepsilon_i / \partial x_j$ are known, and a set of differential equations for the derivatives dx_j/dt is desired which will guarantee that dS/dt is negative. One way to do this is to write:

$$\frac{dx_j}{dt} = -K \sum_{i=1}^{n} \varepsilon_i \frac{\partial \varepsilon_i}{\partial x_j} \qquad \text{(EQ. 4.5-15)}$$

as the basic set of differential equations, where K is a positive constant. Substituting 4.5-15 in 4.5-14 yields:

$$\frac{dS}{dt} = \frac{-2}{K} \sum_{j=1}^{m} \left(\frac{dx_j}{dt}\right)^2 \qquad \text{(EQ. 4.5-16)}$$

which clearly implies that dS/dt is always negative. Since S is positive and decreasing, it will approach a limit, (positive or zero) which will be a minimum.

The method may be summarized as follows: S is an error term (the familiar sum of the errors squared) and the vector $(x_1 \ldots x_m)$ moves around in m-dimensional coordinate space looking for a minimum S. In the language of vector analysis, Equation 4.5-15 says that the point $(x_1 \ldots x_m)$ moves in the negative direction along the gradient of S, so that S decreases as rapidly as possible. Hence, the name "steepest descents". The factor K determines the speed with which the vector $(x_1 \ldots x_m)$ moves.

If a solution to Equation 4.5-8 exists, then the minimum value of S is clearly zero and the x_j will converge to a solution.

If no solution exists, a best approximation is found(best in the least-square sense). If several solutions (or several minima) exist, they will be obtained by starting with different initial conditions. There are no problems of instability such as appeared with the other methods.

Applying this method to the original problem, rewrite Equations 4.5-1 and 4.5-2 in terms of the errors:

$$a_{11} x_1 + a_{12} x_2 - b_1 = \varepsilon_1 \qquad \text{(EQ. 4.5-17)}$$

$$a_{21} x_1 + a_{22} x_2 - b_2 = \varepsilon_2 \qquad \text{(EQ. 4.5-18)}$$

The partial derivatives $\partial\varepsilon_i/\partial x_j$ appearing in Equation 4.5-15 are simply the coefficients a_{ij}, and Equation 4.5-15 becomes:

$$\frac{dx_1}{dt} = -K \left[\varepsilon_1 a_{11} + \varepsilon_2 a_{21}\right] \qquad \text{(EQ. 4.5-19)}$$

$$\frac{dx_2}{dt} = -K \left[\varepsilon_1 a_{12} + \varepsilon_2 a_{22}\right] \qquad \text{(EQ. 4.5-20)}$$

Equations 4.5-17 through 4.5-20 can now be programmed on the computer. The resulting diagram appears in Figure 4.5-2.

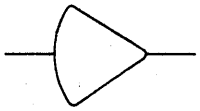
As pointed out above, the range of applications of this method is much wider than the simple example used as an illustration. Since it is essentially an optimization procedure, it is equally applicable to systems with more equations than unknowns. Such systems usually have no solution, in which case a "solution" is found which minimizes the error term S. The following references and those in Appendix 9 contain more detailed descriptions of the application of this method to least squares curve fitting, linear and nonlinear programming, and similar optimization problems.

1. Rogers, A.E. and T.W. Connolly: "Analog Computation in Engineering Design", McGraw-Hill Book Company, Inc., New York 1960

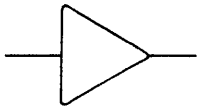
2. Fifer, S: "Analog Computation", McGraw-Hill Book Company, Inc. New York 1961

APPENDIX I

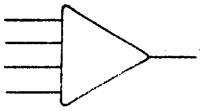
COMPUTER SYMBOLS



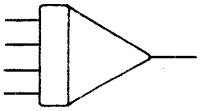
HIGH GAIN AMPLIFIER



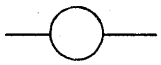
INVERTING AMPLIFIER



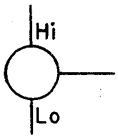
SUMMING AMPLIFIER



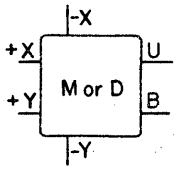
INTEGRATING AMPLIFIER



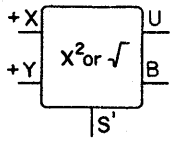
HAND-SET POTENTIOMETER, GROUNDED



HAND-SET POTENTIOMETER, UNGROUNDED

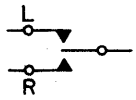


QUARTER-SQUARE MULTIPLIER, MULTIPLICATION AND DIVISION MODE



QUARTER-SQUARE MULTIPLIER, SQUARE AND SQUARE-ROOT MODE

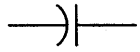
DIODE FUNCTION GENERATOR, FIXED AND VARIABLE



FUNCTION SWITCH

SOLID-STATE DIODE

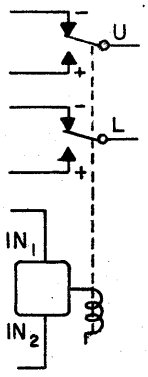
FIXED RESISTOR



CAPACITOR

Y INPUT OF XY PLOTTER

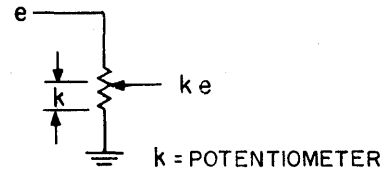
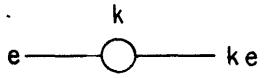
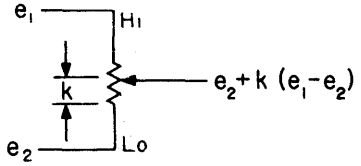
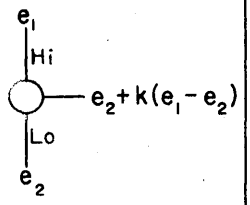
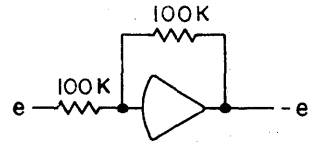
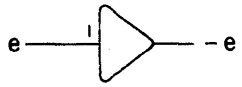
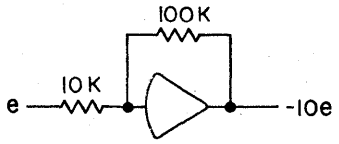
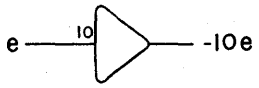
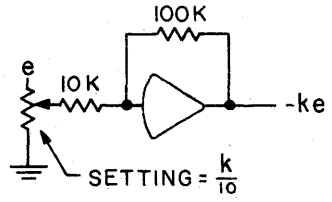
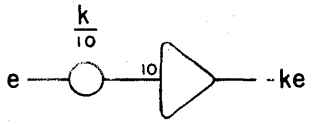
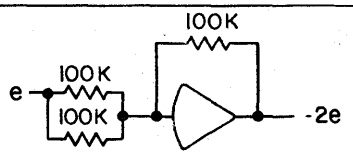
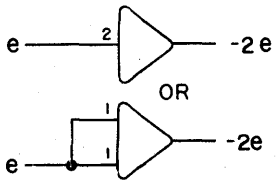
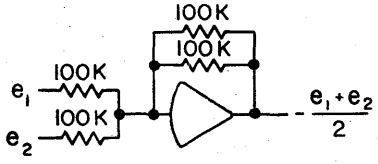
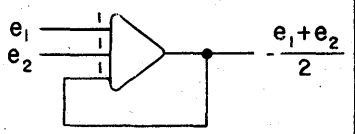
X INPUT OF XY PLOTTER



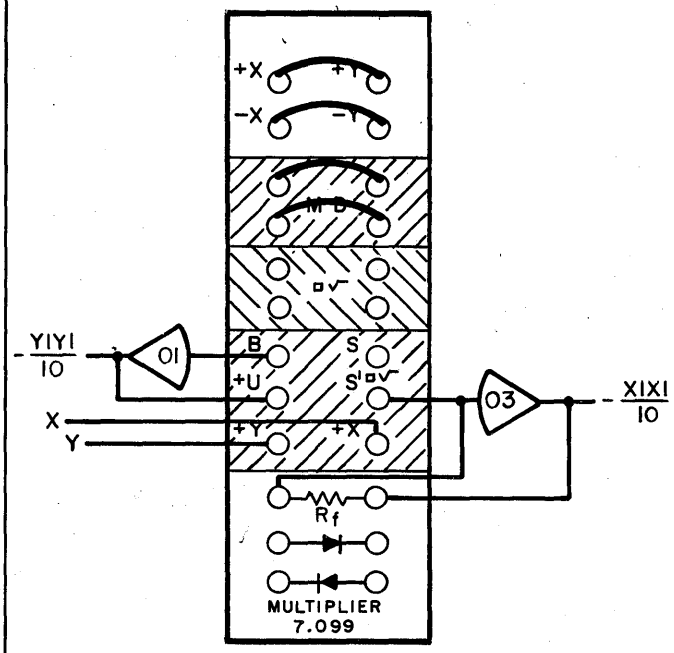
RELAY COMPARATOR

APPENDIX 2

SIMPLE CIRCUITS USING AMPLIFIERS AND POTENTIOMETERS

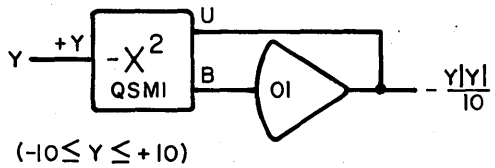
CIRCUIT DESCRIPTION	CIRCUIT	COMPUTER SYMBOL
1. GROUNDED POTENTIOMETER		
2. UNGROUNDED POTENTIOMETER		
3. INVERTER		
4. MULTIPLICATION BY -10		
5. MULTIPLICATION BY -k for $1 \leq k \leq 10$ (for $k < 1$ use circuit 1 feeding circuit 3)		
6. MULTIPLICATION BY 2		
7. MULTIPLICATION BY $\frac{1}{2}$		

3. X|X| AND Y|Y|



PATCHING DIAGRAM

IF ONLY ONE ABSOLUTE VALUE CIRCUIT IS REQUIRED, ELIMINATE AMPLIFIER 03 ~~AND X TO Y JUMPER~~

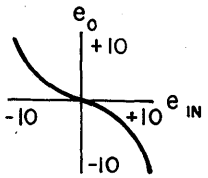


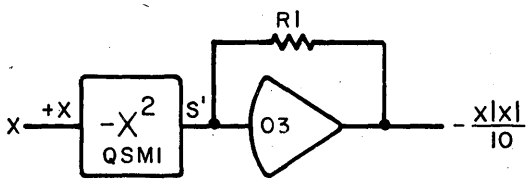
$(-10 \leq Y \leq +10)$

NOTE

$-\frac{Y|Y|}{10} = -\frac{Y^2}{10}$ WHEN $Y \geq 0$

$-\frac{Y|Y|}{10} = +\frac{Y^2}{10}$ WHEN $Y \leq 0$





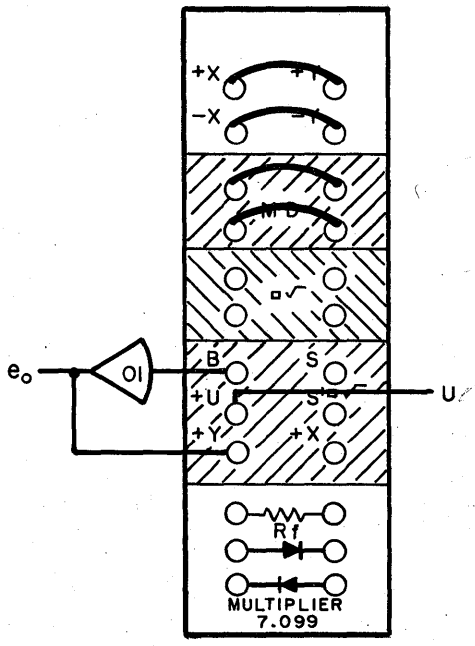
$(-10 \leq X \leq +10)$

NOTE

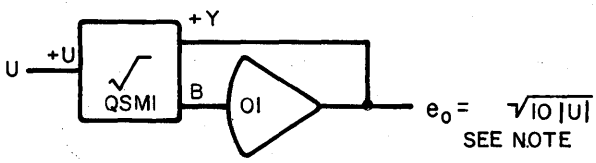
$-\frac{X|X|}{10} = -\frac{X^2}{10}$ WHEN $X \geq 0$

$-\frac{X|X|}{10} = +\frac{X^2}{10}$ WHEN $X \leq 0$

4. SQUARE ROOT



PATCHING DIAGRAM

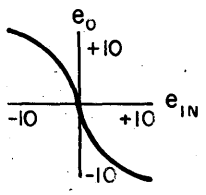


$(-10 \leq U \leq +10)$

NOTE

WHEN U IS POSITIVE $e_o = -\sqrt{10|U|}$

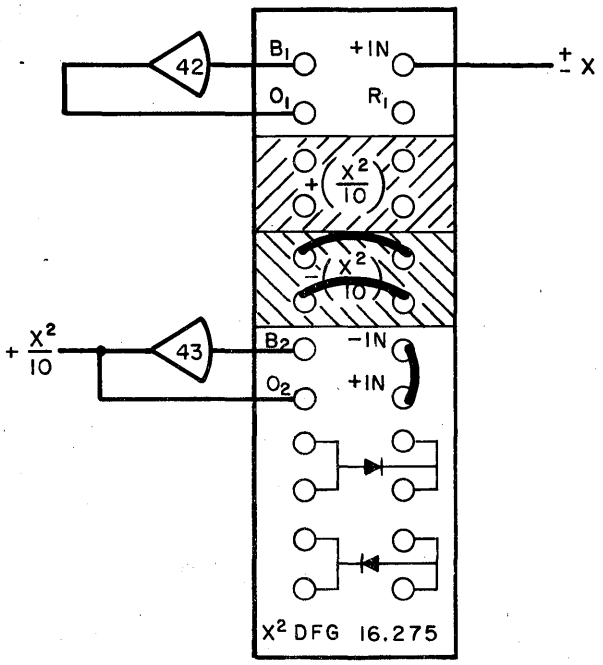
WHEN U IS NEGATIVE $e_o = +\sqrt{10|U|}$



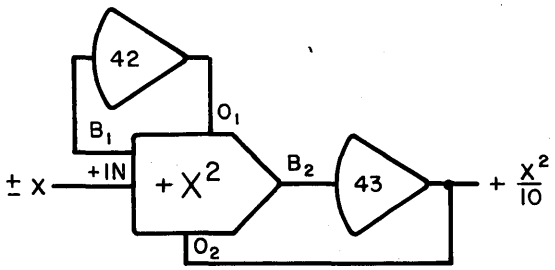
APPENDIX 4

X^2 DFG CIRCUITS

1. $\frac{X^2}{10}$

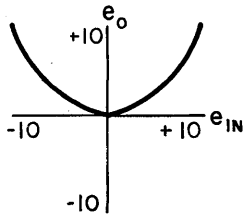


PATCHING DIAGRAM

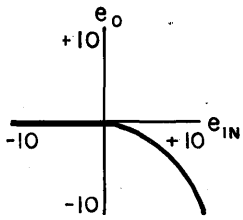


COMPUTER DIAGRAM

$-10 \leq X \leq +10$

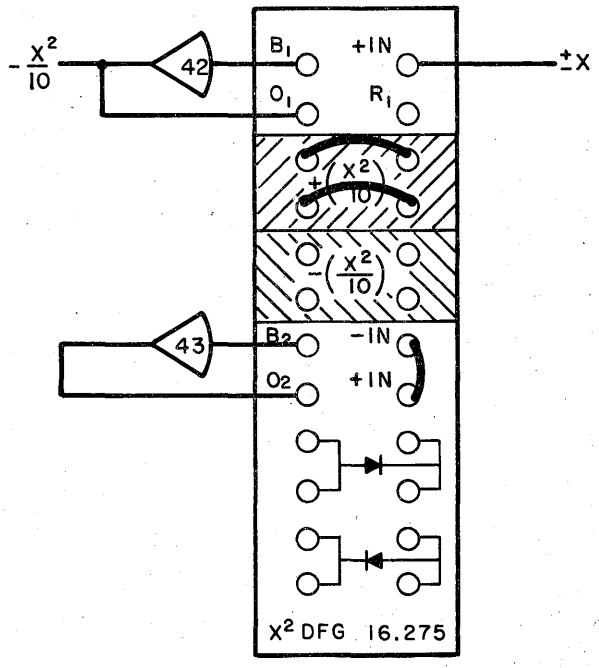


e_o AMPLIFIER 43

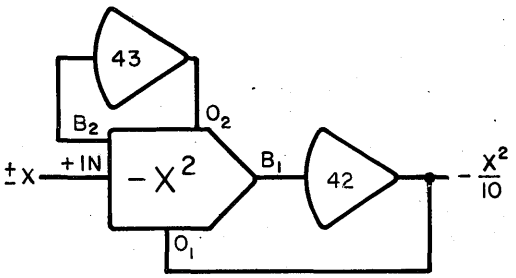


e_o AMPLIFIER 42

2. $-\frac{X^2}{10}$

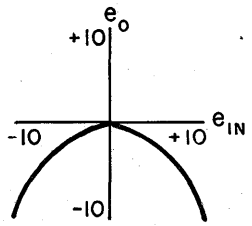


PATCHING DIAGRAM

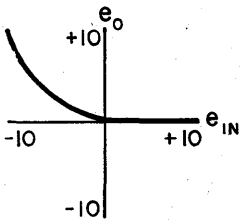


COMPUTER DIAGRAM

$-10 \leq X \leq +10$

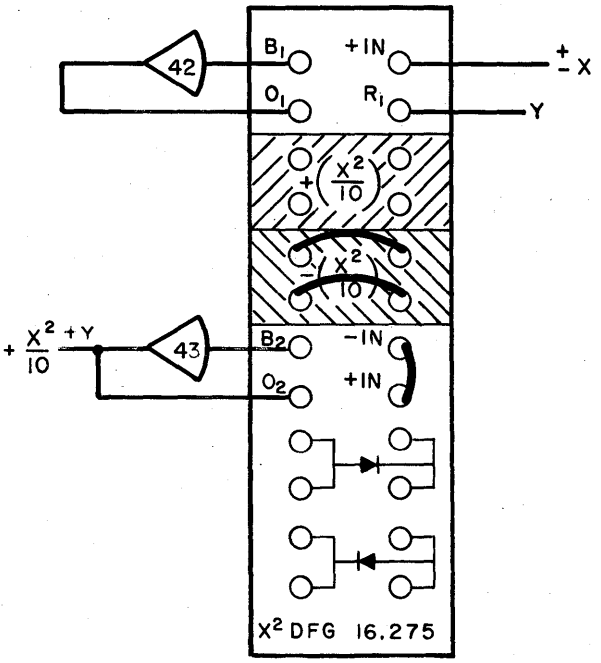


e_o AMPLIFIER 42

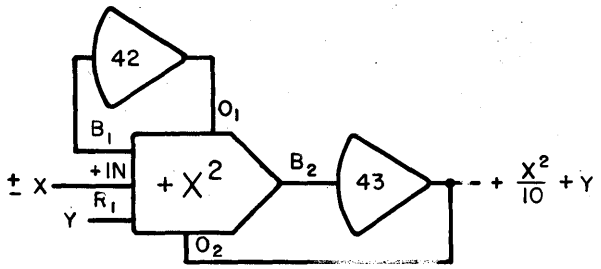


e_o AMPLIFIER 43

3. $+\frac{X^2}{10}+Y$

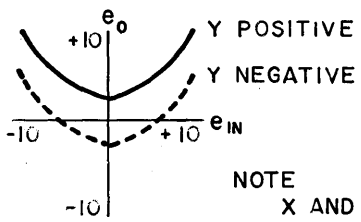


PATCHING DIAGRAM



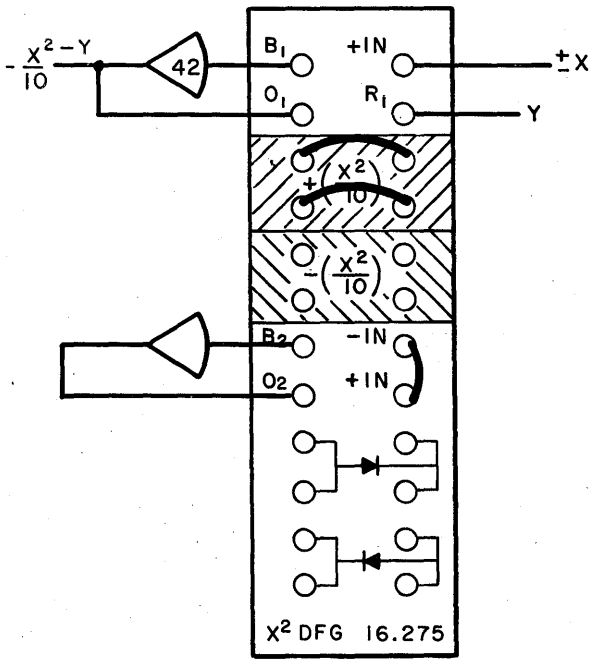
COMPUTER DIAGRAM

$-10 \leq X \leq +10$

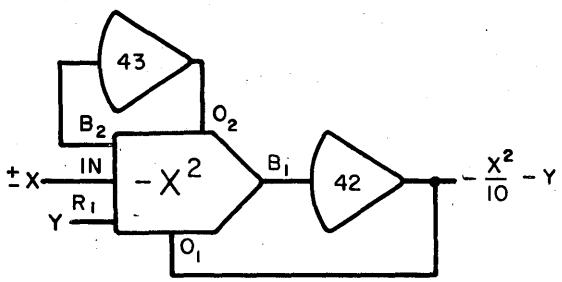


NOTE
X AND Y MUST BE SCALED TO PREVENT AMPLIFIER OVERLOAD

4. $-\frac{X^2}{10}-Y$



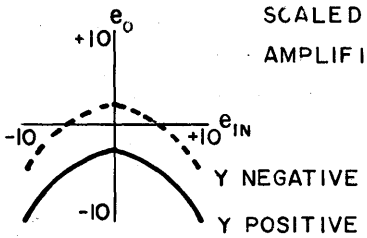
PATCHING DIAGRAM



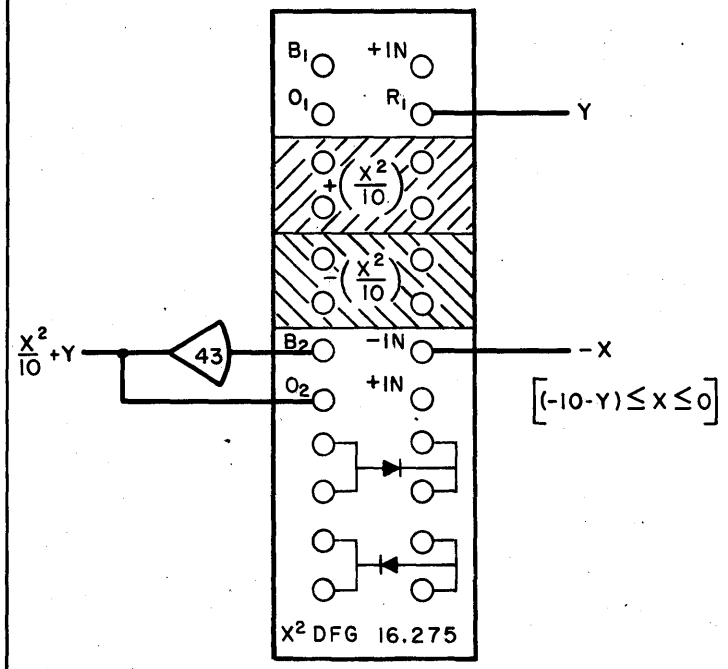
COMPUTER DIAGRAM

$-10 \leq X \leq +10$

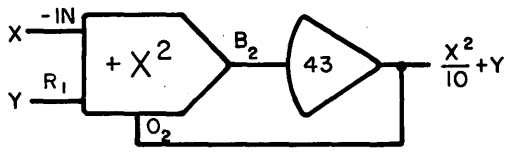
NOTE
X AND Y MUST BE SCALED TO PREVENT AMPLIFIER OVERLOAD



5. $(\frac{X^2}{10} + Y)$ FOR $X \leq 0$



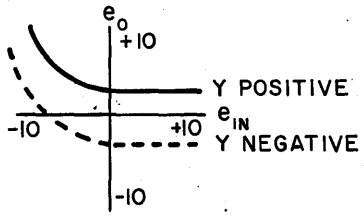
$[(-10-Y) \leq X \leq 0]$



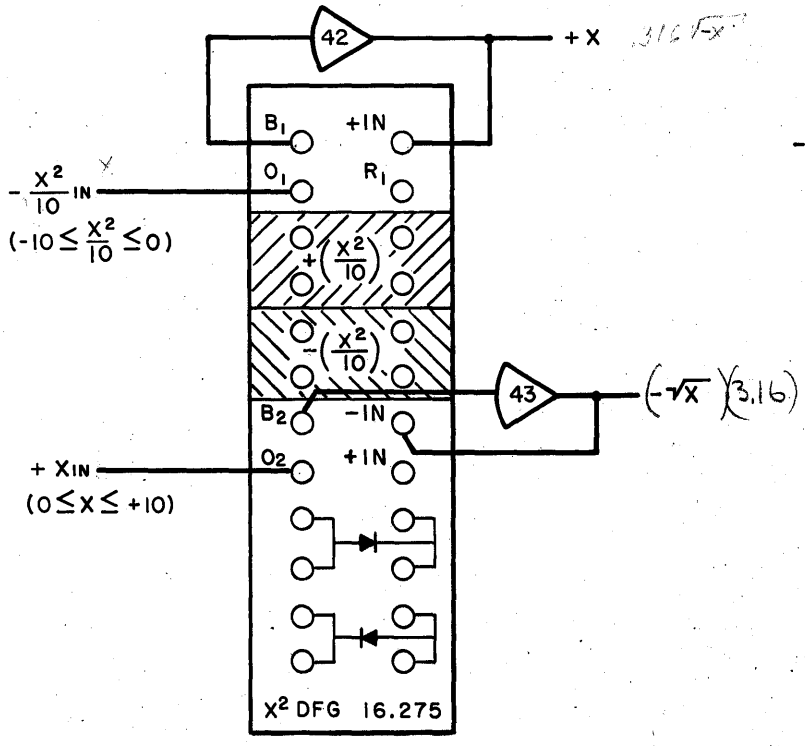
NOTE

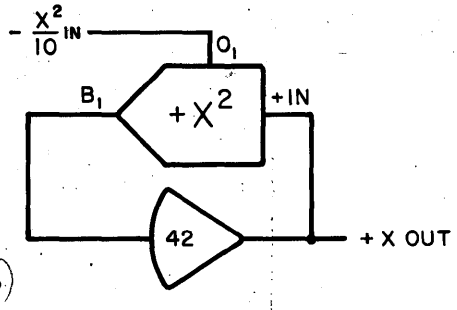
X AND Y MUST BE SCALED TO PREVENT AMPLIFIER OVERLOAD

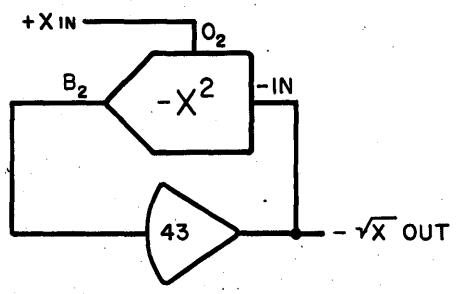
$[(-X-Y) \leq -10]$



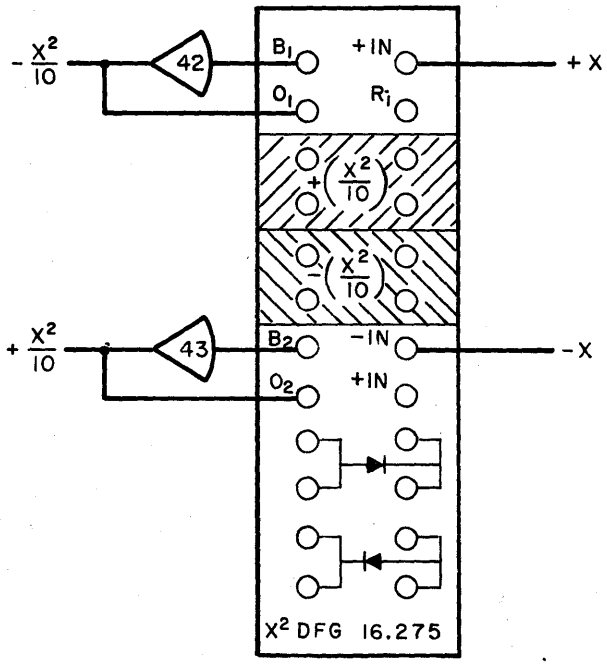
6. $\sqrt{X}$

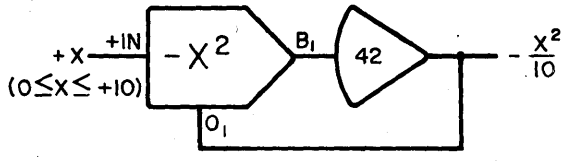


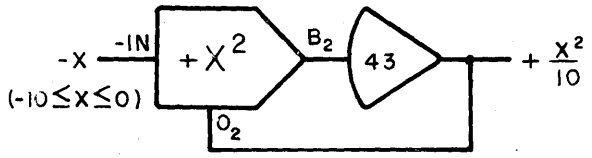


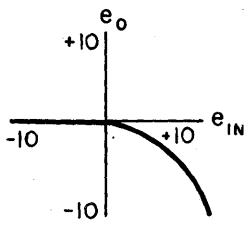


7. $+\frac{X^2}{10}$ FOR $X \leq 0$ AND $-\frac{X^2}{10}$ FOR $X \leq 0$

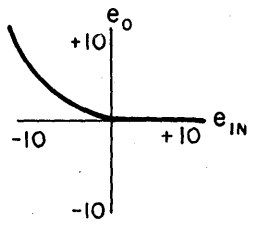








e_o AMPLIFIER 42



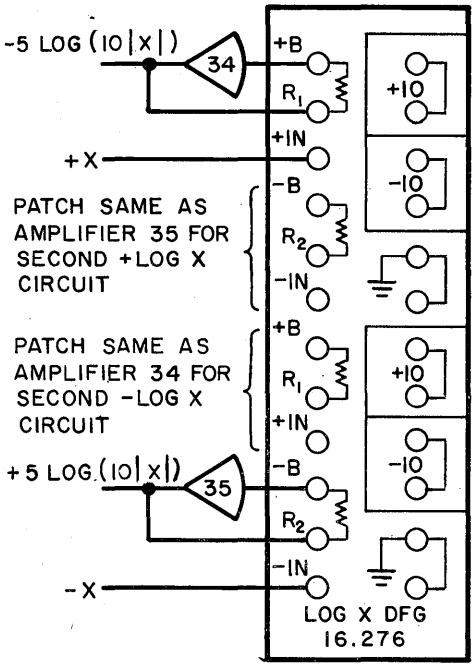
e_o AMPLIFIER 43

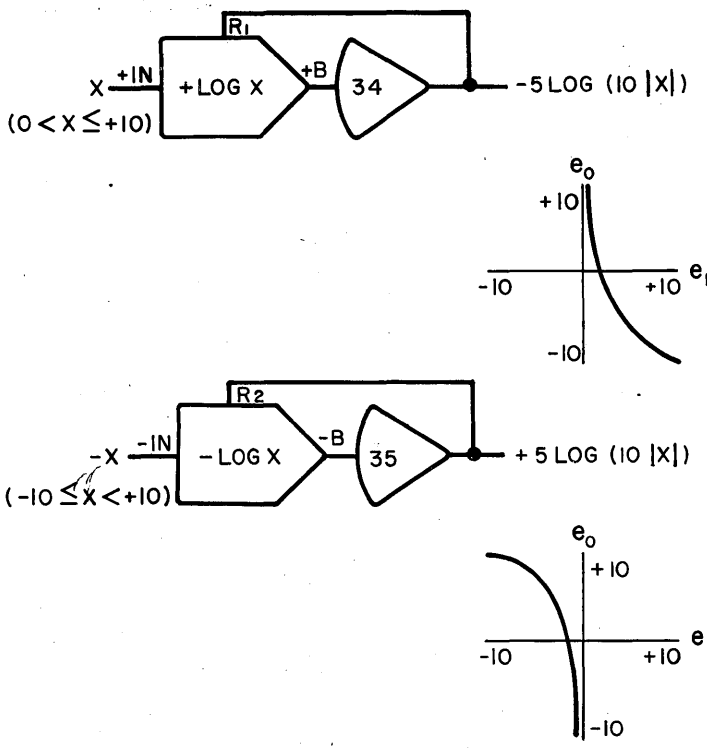
APPENDIX 5

LOG X AND $\frac{1}{2}$ LOG X DFG CIRCUITS

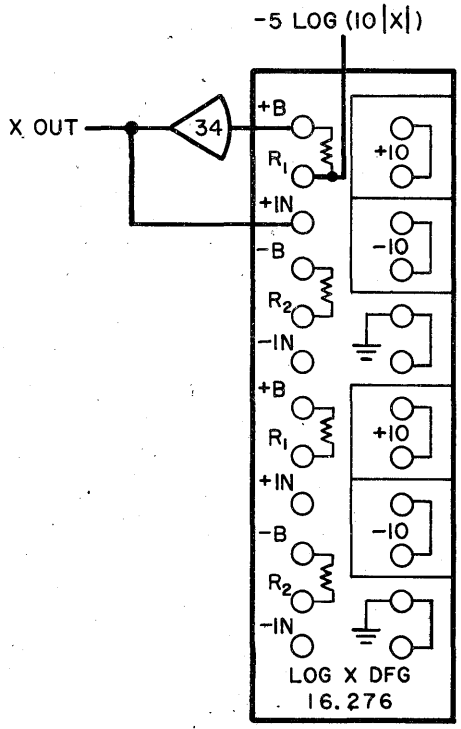
a. LOG X DFG CIRCUITS

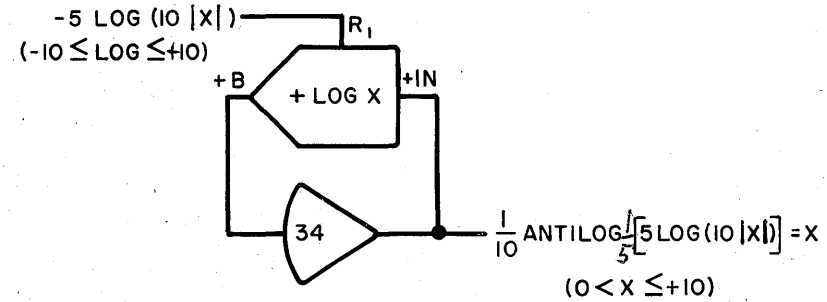
1. $-\text{LOG}_{10}$ X FOR +X INPUT AND $+\text{LOG}_{10}$ X FOR -X INPUT



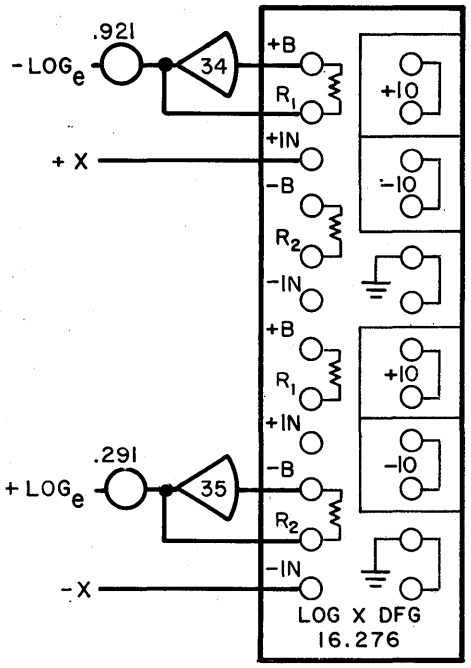


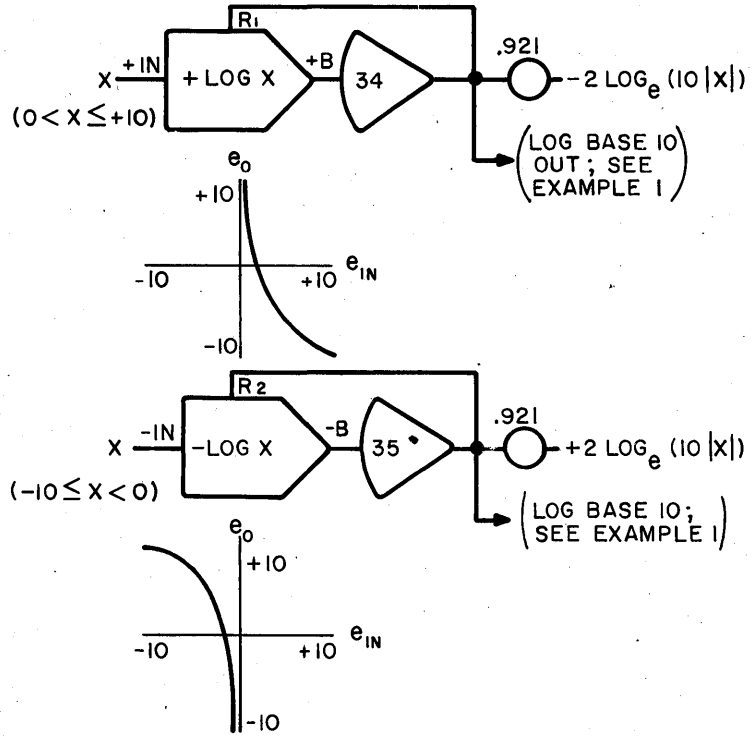
2. ANTILOG, BASE 10



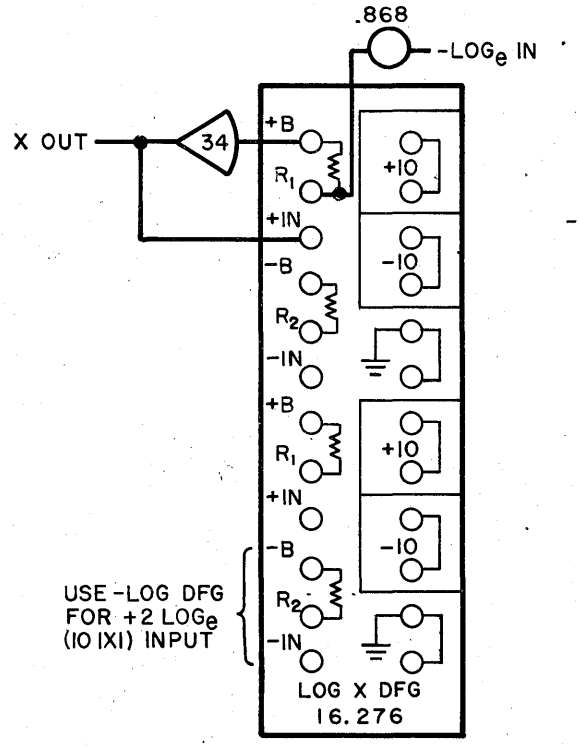


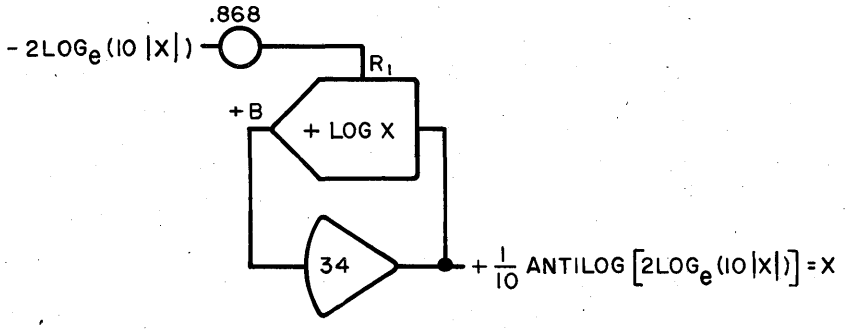
3. LOG BASE e



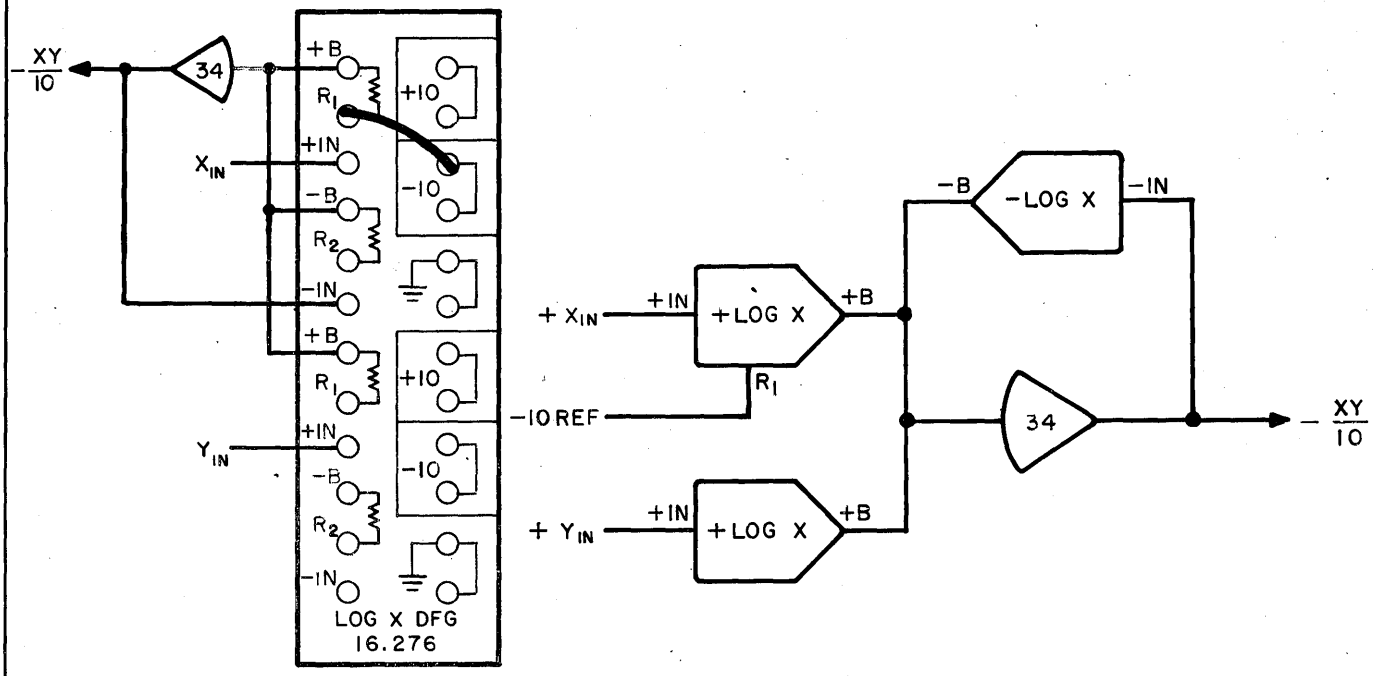


4. ANTILOG, BASE e

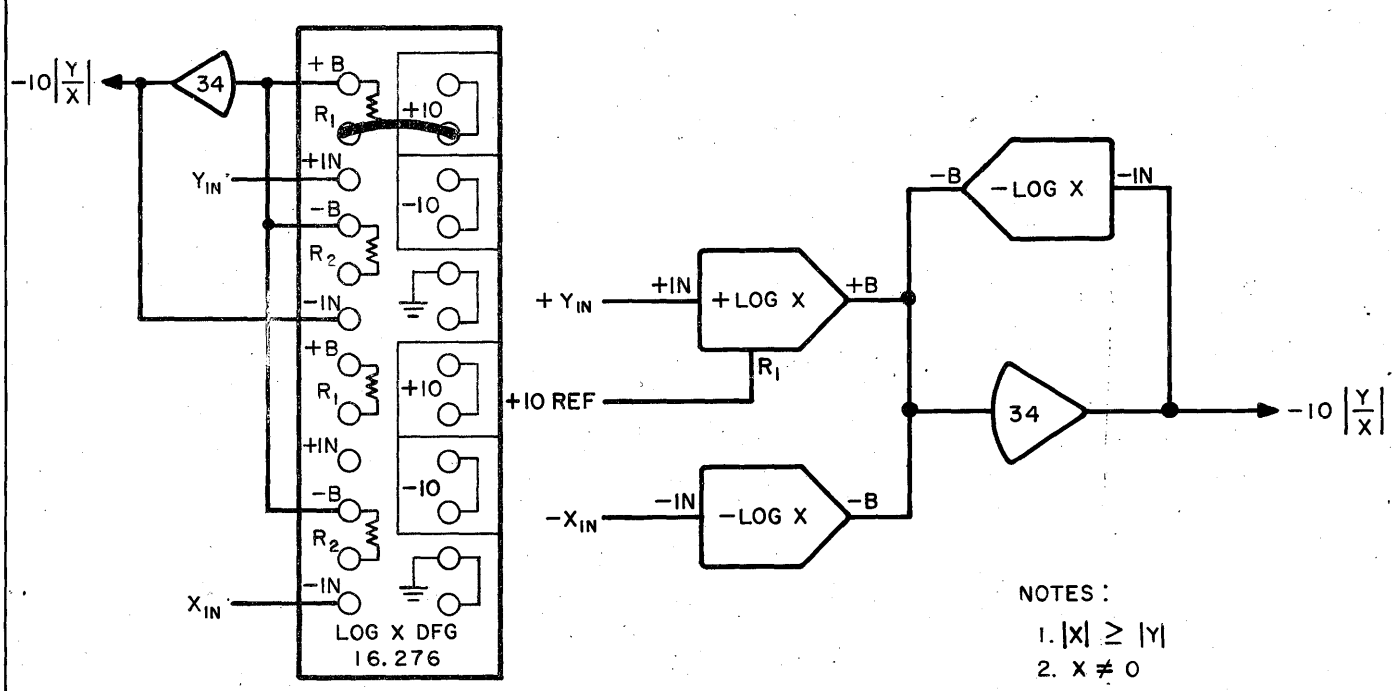




5. MULTIPLICATION (TWO VARIABLES)



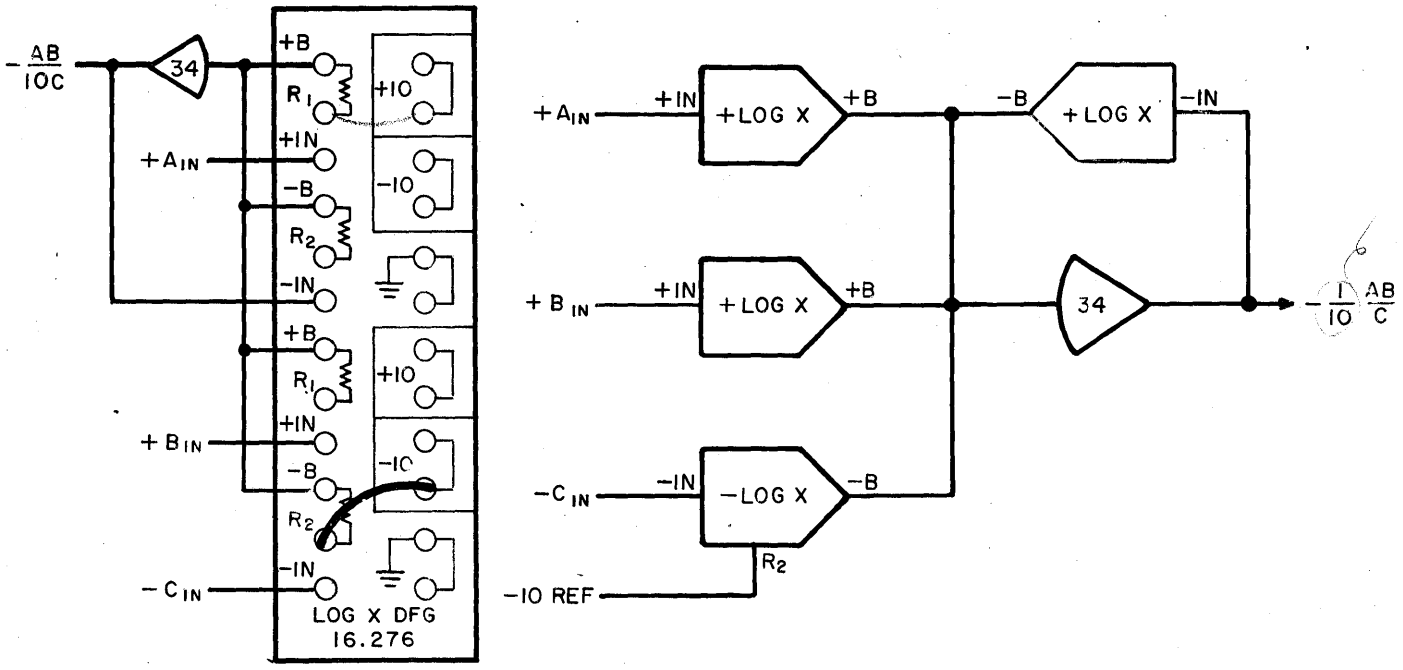
6. DIVISION (TWO VARIABLES)



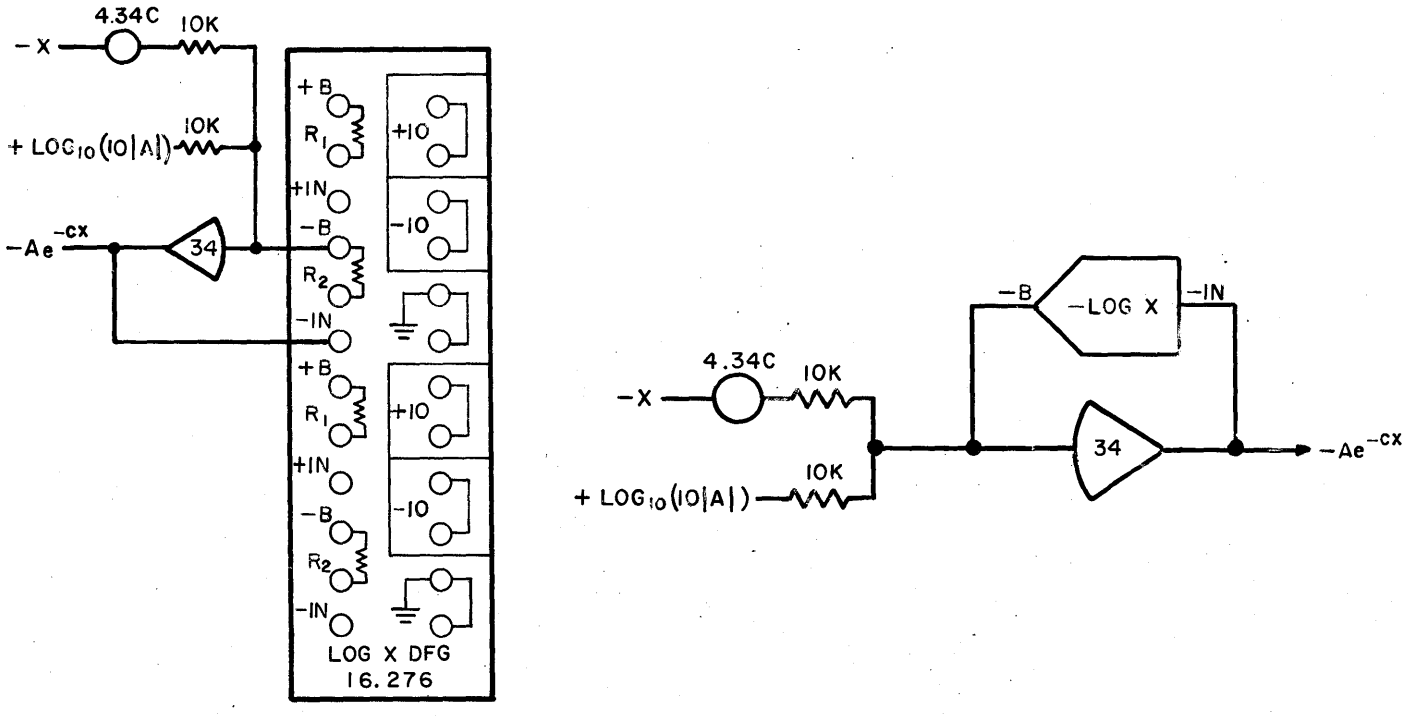
NOTES:

1. $|X| \geq |Y|$
2. $X \neq 0$

7. MULTIPLICATION AND DIVISION (MORE THAN TWO VARIABLES)

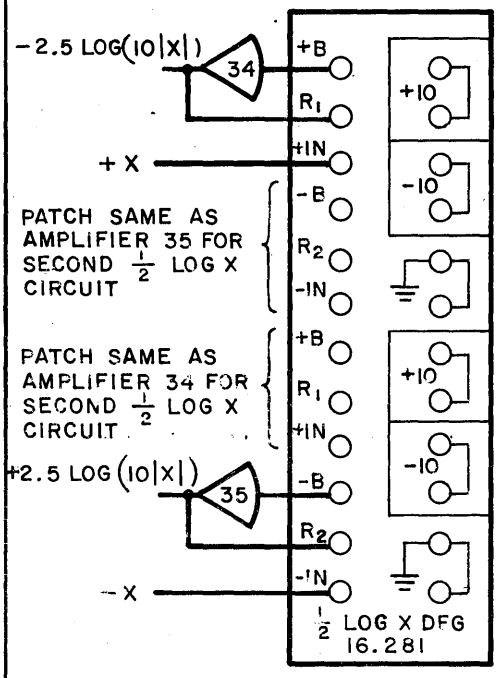


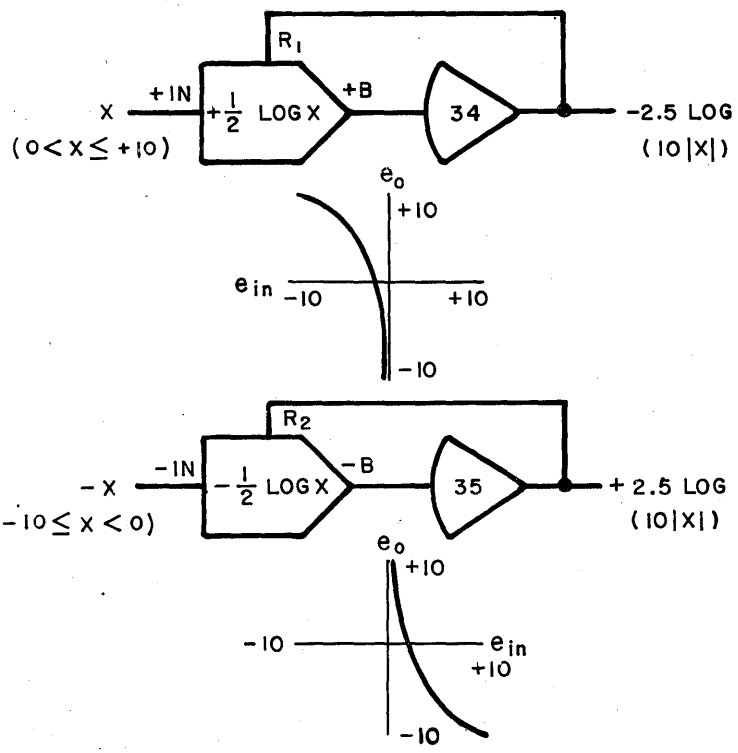
8. EXPONENTIAL



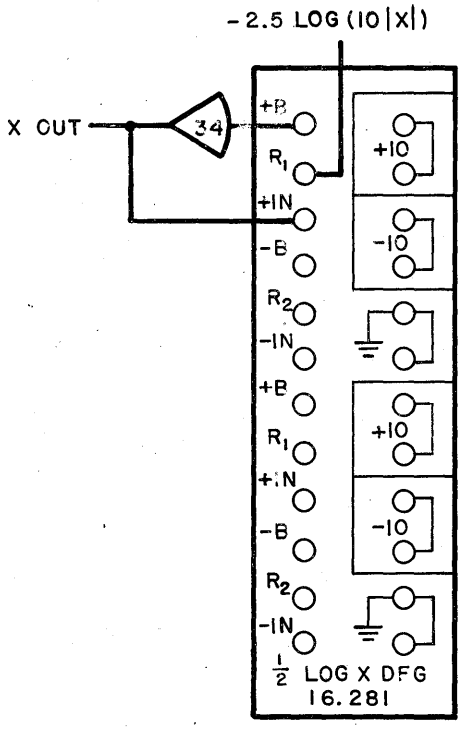
b. $\frac{1}{2}$ LOG X DFG CIRCUITS

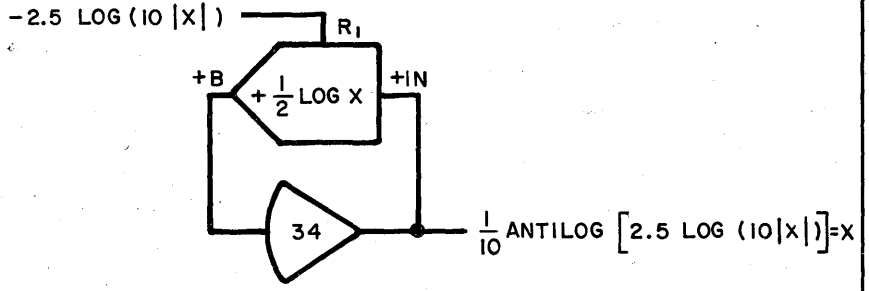
1. LOG BASE 10 OF $\sqrt{X}$



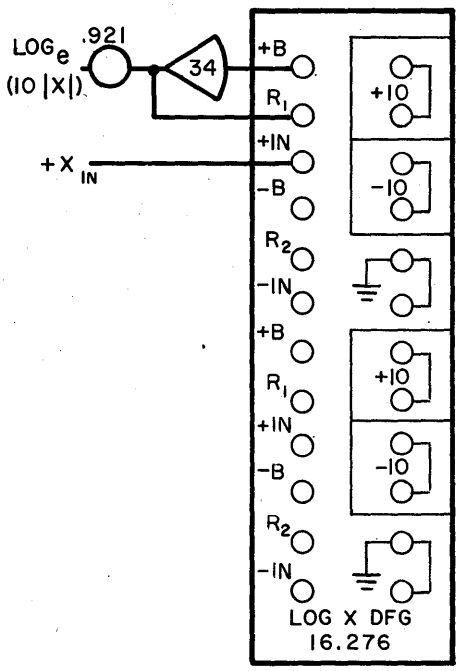


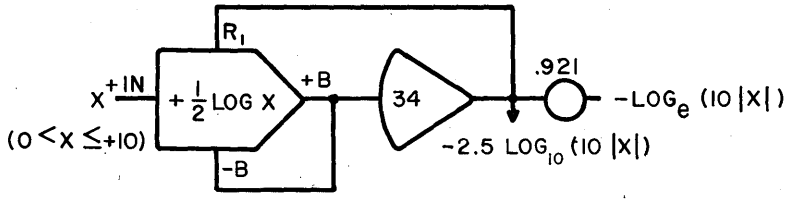
2. ANTILOG, BASE 10



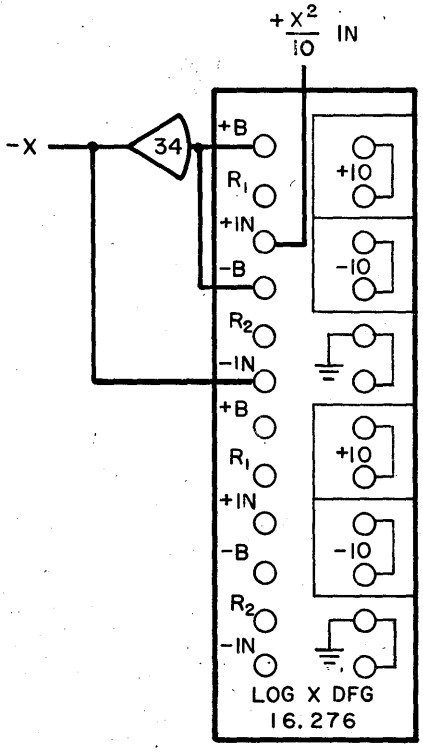


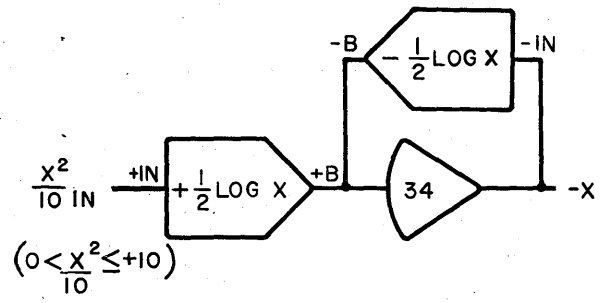
3. LOG BASE $_e$ OF X





4. SQUARE ROOT

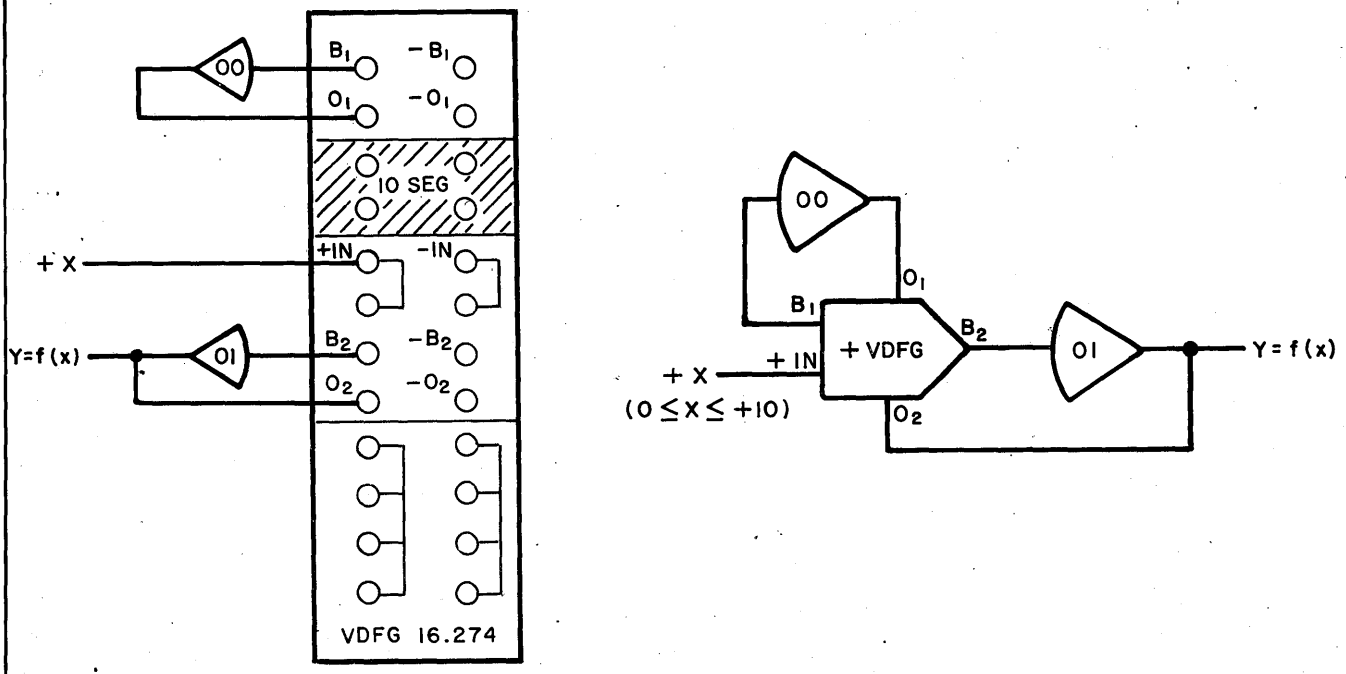




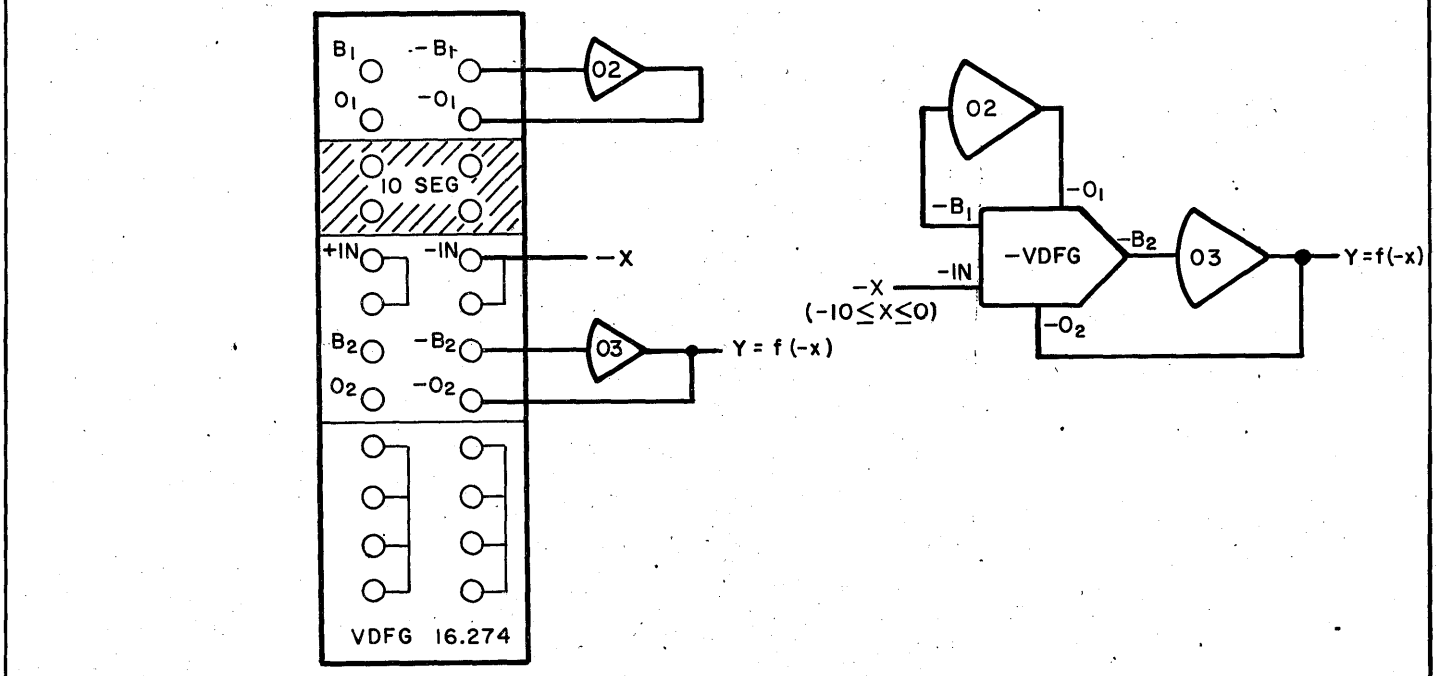
APPENDIX 6

VDFG CIRCUITS

1. + VDFG



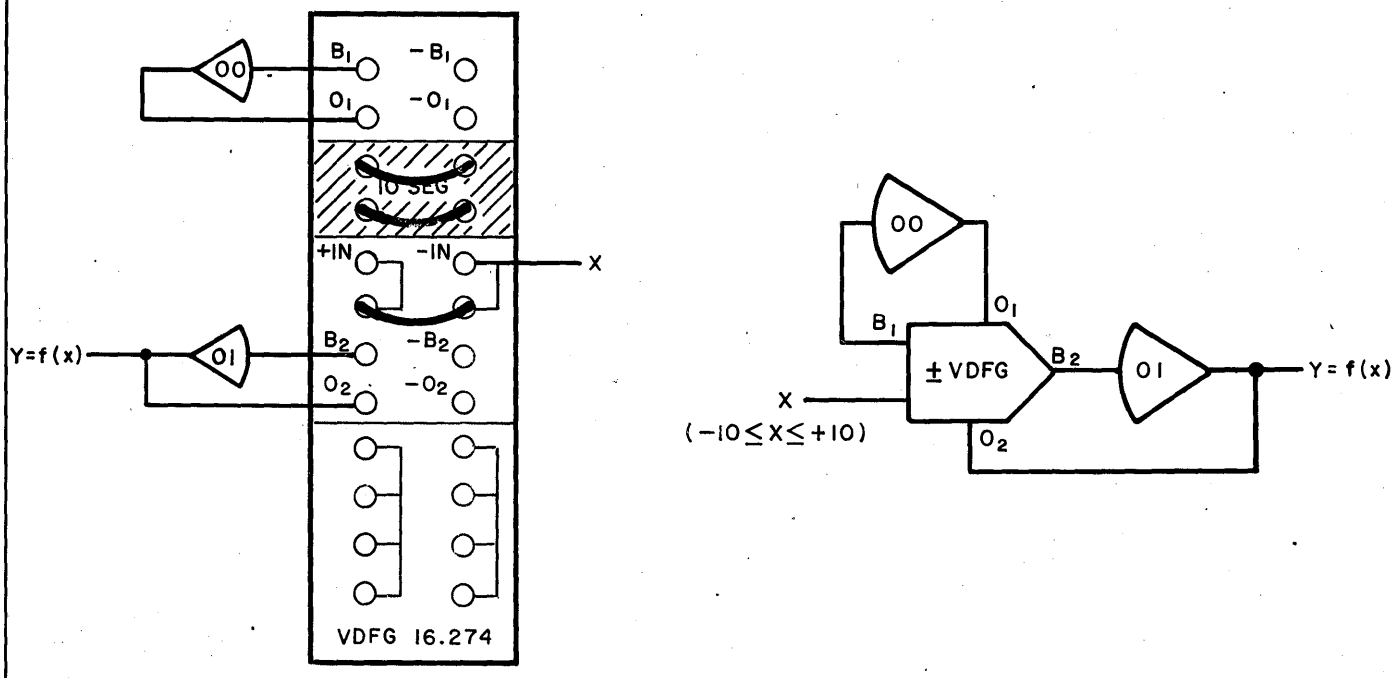
2. −VDFG



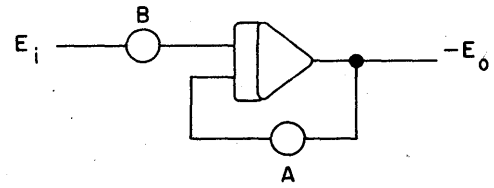
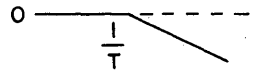
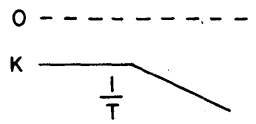
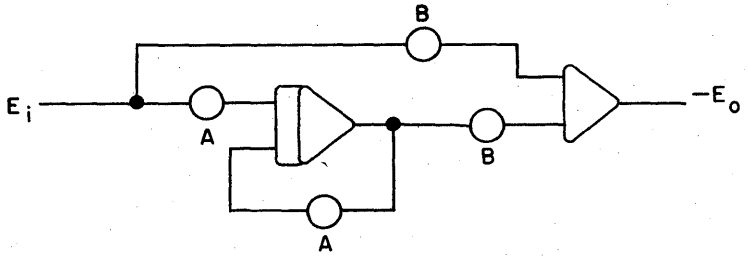
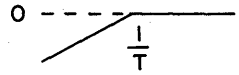
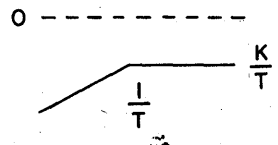
APPENDIX 6

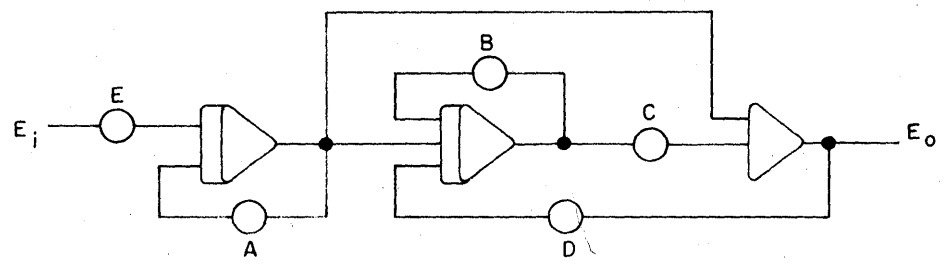
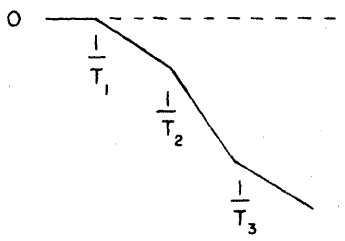
VDFG CIRCUITS

3. ± VDFG

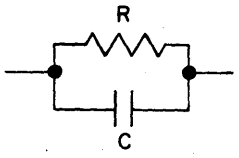
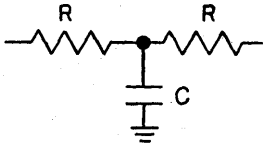


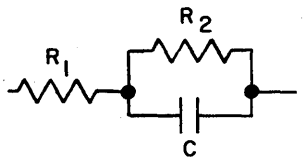
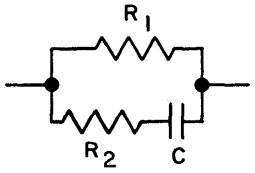
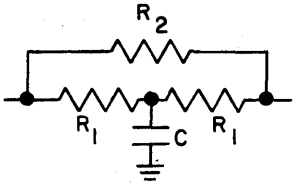
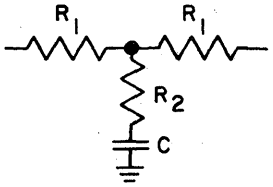
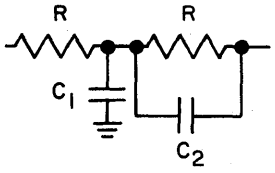
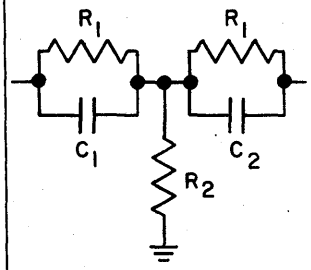
(a) The following Table contains examples of amplifier circuits for simulating transfer functions. A more complete listing may be found in Jackson, A.S.: "Analog Computation", McGraw-Hill Book Company, Inc., New York, 1960.

NO.	BODE PLOT	TRANSFER FUNCTION	TIME CONSTANTS	GAINS
				
1		$\frac{1}{1+Tp}$	$T = \frac{1}{A}$	$A = B = \frac{1}{T}$
2		$\frac{K}{1+Tp}$	$T = \frac{1}{A}$ $K = \frac{B}{A}$	$A = \frac{1}{T}$ $B = AK$
				
3		$\frac{Tp}{1+Tp}$	$T = \frac{1}{A}$	$A = \frac{1}{T}$ $B = 1$
4		$\frac{Kp}{1+Tp}$	$T = \frac{1}{A}$ $K = BT$	$A = \frac{1}{T}$ $B = AK$

NO.	BODE PLOT	TRANSFER FUNCTION	TIME CONSTANTS	GAINS
				
5		$\frac{1+T_3p}{(1+T_1p)(1+T_2p)}$	$T_1 = \frac{1}{A}$ $T_2 = \frac{1}{B-CD}$ $T_3 = \frac{1}{B-C}$	$A = \frac{1}{T_1}$ $B = C + \frac{1}{T_3}$ $D = \frac{1}{C}\left(\frac{1}{T_3} - \frac{1}{T_2}\right)+1$ $E = \frac{T_3}{T_1T_2}$

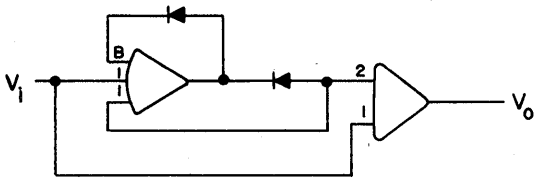
(b) The following table contains the short-circuit admittance and component values for some useful networks for simulating transfer functions. A more extensive listing may be found in Jackson, A.S.: "Analog Computation", and Fifer, S.: "Analog Computation". (See Bibliography.)

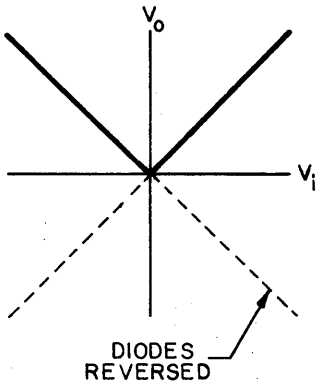
NO.	Yss SHORT-CKT. ADMITTANCE	NETWORK	
1.	$\frac{1}{A}$		A = R
2.	$\frac{1 + pT}{A}$		A = R T = RC
3.	$\frac{1}{A(1 + pT)}$		A = 2R $T = \frac{RC}{2}$

NO.	Yss SHORT-CKT. ADMITTANCE	NETWORK	
4.	$\frac{1}{A}\left(\frac{1+pT}{1+p\Theta T}\right)$ $\Theta < 1$		$A = R_1 + R_2$ $T = R_2 C$ $\Theta = \frac{R_1}{R_1 + R_2}$
5.	$\frac{1}{A}\left(\frac{1+pT}{1+p\Theta T}\right)$ $\Theta < 1$		$A = R_1$ $T = (R_1 + R_2)\, C$ $\Theta = \frac{R_2}{R_1 + R_2}$
6.	$\frac{1}{A}\frac{1+p\Theta T}{1+pT}$ $\Theta < 1$		$A = \frac{2R_1 R_2}{R_1 + R_2}$ $T = \frac{R_1 C}{2}$ $\Theta = \frac{2R_1}{2R_1 + R_2}$
7.	$\frac{1}{A}\frac{1+p\Theta T}{1+pT}$ $\Theta < 1$		$A = 2R_1$ $T = \left(R_2 + \frac{R_1}{2}\right) C$ $\Theta = \frac{2R_2}{2R_2 + R_1}$
8.	$\frac{1}{A}\frac{1+p\Theta T}{1+pT}$ $\Theta < 1$		$A = 2R$ $T = \frac{R}{2}(C_1 + C_2)$ $\Theta = \frac{2C_2}{C_1 + C_2}$
9.	$\frac{1}{A}\left(\frac{(1+pT_1)(1+pT_3)}{(1+pT_2)}\right)$ $T_2 \leqslant T_1 \leqslant T_3$		$A = 2R_1 + \frac{R_1^2}{R_2}$ $T_1 = R_1 C_1$ $T_2 = \left[\frac{R_1 R_2}{R_1 + 2R_2}\right](C_1 + C_2)$

APPENDIX 8
REPRESENTATION OF DISCONTINUTIES

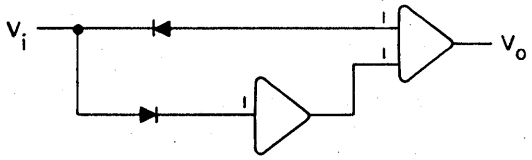
1.

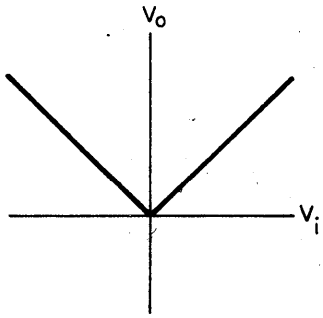




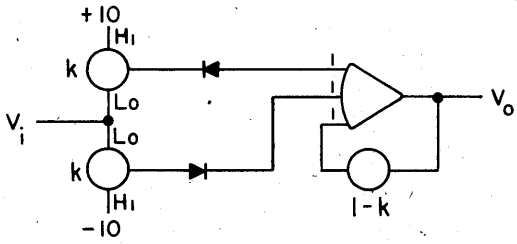
ABSOLUTE VALUE CIRCUITS

2.

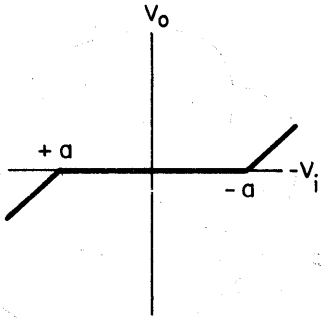




3.

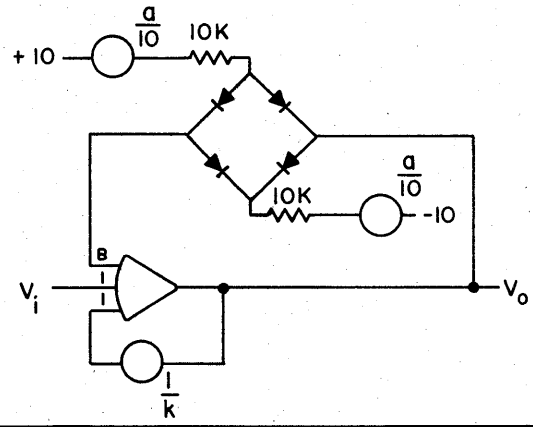


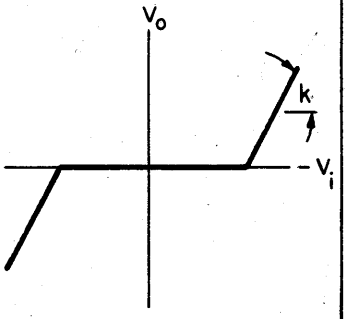
$$k = \frac{|a|}{10 + |a|}$$



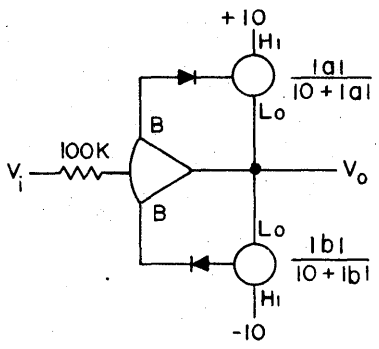
DEAD SPACE SIMULATION

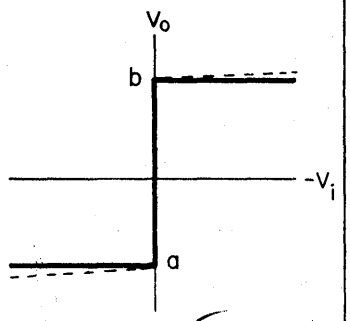
4.





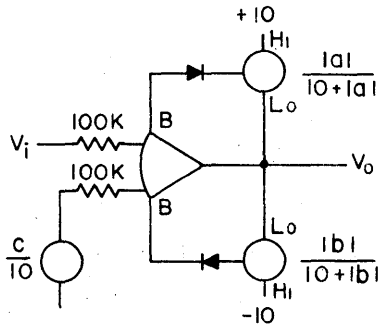
5.

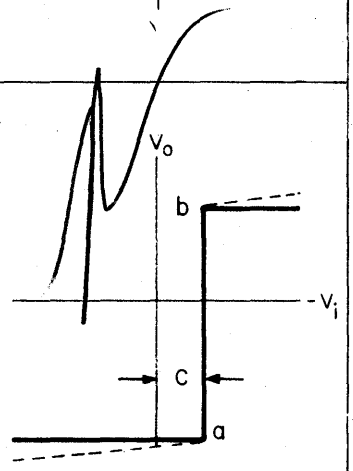




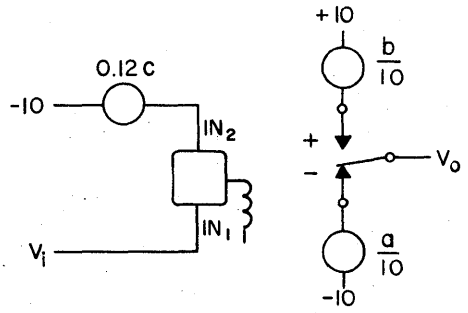
6.

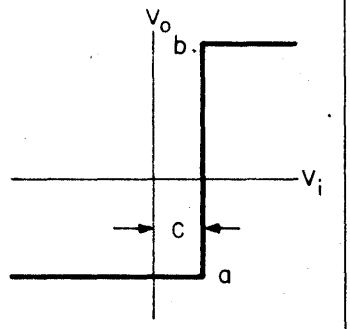
BANG-BANG CIRCUITS





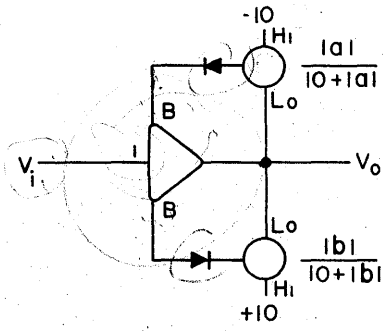
7.

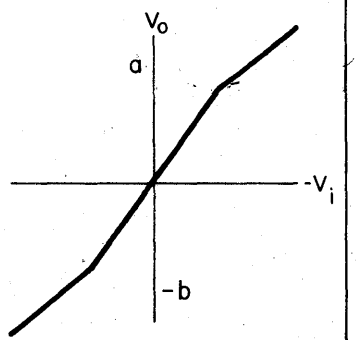




8.

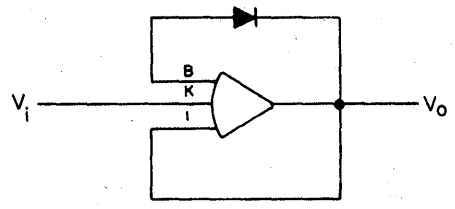
SOFT LIMITER

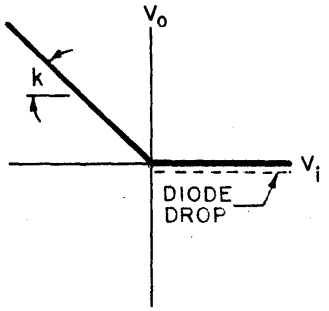




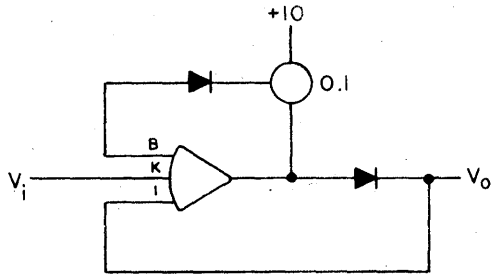
9.

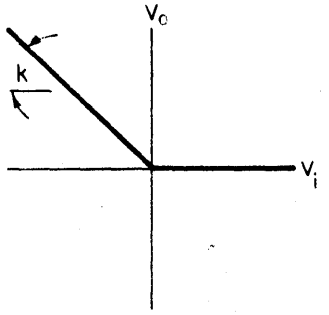
ZERO LIMIT HALF-WAVE RECTIFIER





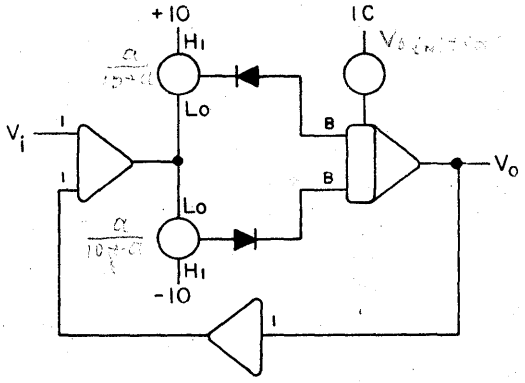
10.

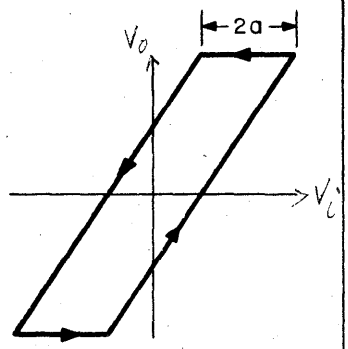




11.

HYSTERESIS





APPENDIX 9

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MANUFACTURING PLANTS

ELECTRONIC ASSOCIATES, INC.
Manufacturing Division
Long Branch, New Jersey

ELECTRONIC ASSOCIATES, LTD.
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COMPUTATION CENTERS

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