Firefox Workstation Backplane

Revision 3.0

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Revision History

Date	Version	Content/Changes
10 Dec 87	3.0	Add Power and Fan connector signal list; change External connector pinout
26 May 87	2.1	Add module numbers, slot IDs, and physical characteristics; change VI-bus pinout
01 May 87	2.0	L-series connector changes
07 Feb 87	1.0	First external release

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12. Firefox Backplane

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The Firefox backplane module is an 11.9-inch x 16-inch assembly that uses press-pin connector blocks to implement a 12-slot, quad-height backplane. The printed circuit board is a four-layer board: two signal layers, one +5-volt power plane, and one ground plane. A 64-ohm, controlled-impedance circuit board is used to enhance signal integrity on the high-speed Firefox backplane. A new etch is used to implement the Firefox system M-bus and local subsystem interconnects for the Q-bus and graphics VI-bus.

The part numbers for the backplane are as follow:

- 50-17254-01 (etch)
- 54-17255-01 (assembled module)

The Q-bus section of the backplane will support a maximum of **TBD** equivalent AC loads (the backplane itself presents **TBD** AC loads) and **TBD** DC loads from all the Q-bus modules inserted in the backplane.

The backplane is bounded and cannot be expanded.

The mechanical placement is shown in Figure 12-1. Slot 1 is located on the right side of the backplane (J1 and J2) and slot 12 on the left (J23 and J24).

The backplane has two power connectors; each is a dual, 28-pin (56 pins total), card-edge connector. The connector near slot 1 (J50) is called the Primary Power Supply connector and distributes +5 volts and +12 volts to slots 1-6. The connector near slot 12 (J51) is called the Expansion connector and distributes +5 volts and +12 volts to slots 7-12. Ground is common throughout the backplane.

To minimize system clock skews, the M-bus clock circuit is implemented on the backplane module. The logic for the clock circuit is located near the Primary Power Supply connector (J50).

12.1. Clock Circuit

The **TBD** ns oscillator goes through a J-K circuit that performs a divide-by-6 function and outputs a **TBD** ns clock. This clock is distributed through 74F244 drivers and routed (matched impedance) to each of the M-bus slots (slots 3-9).

There are two jumpers in the circuit: W9, which is normally in place, and W10, which is normally not present. By changing this to W9 out and W10 in, an external clock can be injected at J25, a coaxial connector. This feature is for test purposes and will not be used in a customer environment.

H-3000

Figure 12-1: Mechanical Connector Placement

12.2. Physical Characteristics

The backplane has the following physical characteristics:

- 11.9" × 16.0" × .125" in size
- 4 layers (power and ground are inner layers)
- Inner layers are 2-ounce copper
- Outer layers are 1-ounce copper
- Dielectric is 8 mil thick
- Etch is 8/8 technology
- 64-ohm matched impedance (10 percent tolerance)
- No buried signals

12.3. Backplane Segmentation

The backplane has two types of connectors: regular Q-bus connectors and L-series connectors. Slots 1-9 use the L-series connectors, an example of which appears in Figure 12-2.

Each of slots 1-9 has two L-series connectors, and each connector has 94 pins. The pins on the top connector (J1, for example) are named A1-A94. The pins on the bottom connector (J2, for example) are named B1-B94. Each of slots 1-9 has 188 pins available for signals, power, and ground.

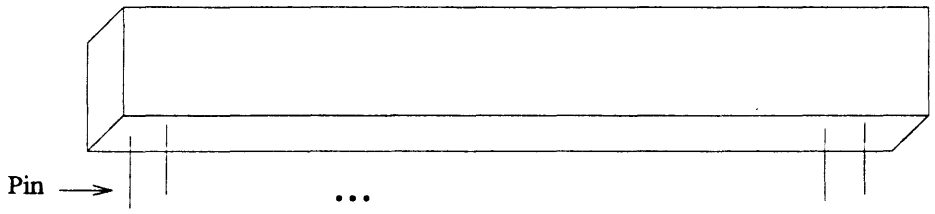

Figure 12-2: The L-series connector has one set of two rows of 47 pins (a total of 94 pins)

Slots 10-12 use the Q-bus connectors, an example of which appears in Figure 12-3.

Each of slots 10-12 has two Q-bus connectors, and each connector has 72 pins. The pins on the top and bottom connectors are named AA-AV and BA-BV. Note that each pin will occur twice in each slot. For example, J23 pin AA and J24 pin AA are both in slot 12. To specify a particular pin, the connector must also be named. Each of slots 10-12 has 144 pins available for signals, power, and ground.

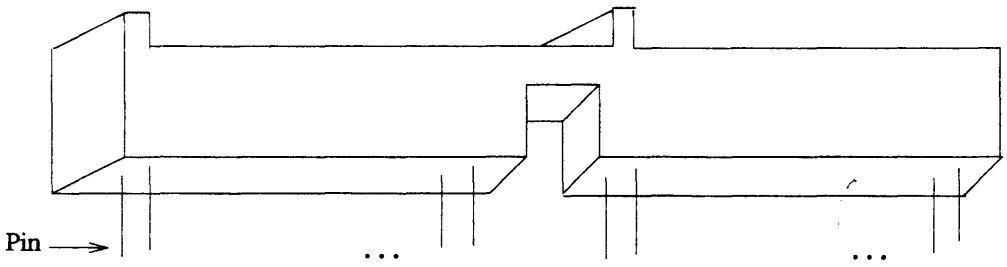

Figure 12-3: The Q-bus connector has two sets of two rows of 18 pins (a total of 72 pins)

The busses for slots 1-9 are assigned as shown in Table 12-1.

Table 12-1: Busses for Slots 1-9

Slot	Busses on Pins A1-A94	Busses on Pins B1-B94
1	J1 VI-bus	J2 VI-bus
2	J3 VI-bus	J4 VI-bus
3	J5 VI-bus	J6 M-bus
4	J7 (reserved)	J8 M-bus
5	J9 (reserved)	J10 M-bus
6	J11 (reserved)	J12 M-bus
7	J13 (reserved)	J14 M-bus
8	J15 (reserved)	J16 M-bus
9	J17 Q-bus	J18 M-bus

On the reserved pins above, there are power and ground connections and a small number of signals (see Tables 12-3 through 12-17 for more specific information concerning signal assignments).

The busses for slots 10-12 are assigned as shown in Table 12-2.

Table 12-2: Busses for Slots 10-12

Slot	Busses on J19, J21, J23	Busses on J20, J22, J24
10	Q22-bus	Q22-bus
11	Q22-bus	Q22-bus
12	Q22-bus	Q22-bus

Note that the Q22-bus is present only if the Q-bus adapter module is in slot 9. Six dual Q-bus modules can be supported, but there may be mechanical restrictions.

12.4. Signal Assignments

The −12-volt signal, although implemented across the slots, is not connected to −12 volts of power on the Firefox backplane because it is not supported by the Firefox power supply (H7868).

12.4.1. M-Bus Backplane Signal Assignments

The MID signals (MID2, MID1, MID0) are used to assign a module ID to the modules in the M-bus slots. The module IDs are assigned to the slots as shown in Table 12-3. The LEGSS (Low-End Graphics Subsystem) base module will always be in the slot with module ID 7.

Table 12-3: Module IDs

Slot	MID2, MID1, MID0
1	Not applicable
2	Not applicable
3	111 (7)
4	101 (5)
5	100 (4)
6	011 (3)
7	010 (2)
8	001 (1)
9	000 (0)
10	Not applicable
11	Not applicable
12	Not applicable

Tables 12-4 through 12-7 show the pin assignment for each of the M-bus signals on the backplane.

Table 12-4: M-Bus Backplane Signal Assignment for Slots 3-9 on Connector B

Pin	Signal	Pin	Signal
B1	GND	B2	BATTERY5V
B3	MCLKA	B4	GND
B5	GND	B6	+5V
B7	MCLKB	B8	GND
B9	GND	B10	+12V
B11	+12V	B12	+12V
B13	MBRQ L	B14	GND
B15	MBRM0 L	B16	MBRM1 L
B17	+5V	B18	MBRM2 L
B19	MBRM3 L	B20	MBRM4 L
B21	MBRM5 L	B22	GND
B23	MBRM6 L	B24	MSPAR
B25	GND	B26	MSTAT0
B27	MSTAT1	B28	MIRQ0 L
B29	MIRQ1 L	B30	+5V
B31	MIRQ2 L	B32	MIRQ3 L
B33	GND	B34	MCPAR
B35	MCMD0	B36	MCMD1
B37	MCMD2	B38	GND
B39	MCMD3	B40	MRSVB40
B41	+5V	B42	MSLOT
B43	MDPAR	B44	MID0
B45	MID1	B46	GND
B47	MID2	B48	MCLKI
B49	GND	B50	GND
B51	MDAL00	B52	MDAL01
B53	MDAL02	B54	+5V
B55	MDAL03	B56	MDAL04
B57	GND	B58	MDAL05
B59	MDAL06	B60	MDAL07
B61	MRESET L	B62	GND
B63	MDAL08	B64	MDAL09
B65	+5V	B66	MDAL10
B67	MDAL11	B68	MDAL12
B69	MDAL13	B70	GND
B71	MDAL14	B72	MDAL15
B73	GND	B74	MDAL16
B75	MDAL17	B76	MDAL18
B77	MDAL19	B78	+5V
B79	MDAL20	B80	MDAL21
B81	GND	B82	MDAL22
B83	MDAL23	B84	MDAL24
B85	MDAL25	B86	GND
B87	MDAL26	B88	MDAL27
B89	+5V	B90	MDAL28
B91	MDAL29	B92	MDAL30
B93	MDAL31	B94	GND

Table 12-5: M-Bus Backplane Signal Assignments for Slots 4-8 on Connector A

Pin	Signal	Pin	Signal
A1	GND	A2	Not used
A3	Not used	A4	Not used
A5	Not used	A6	+5V
A7	Not used	A8	Not used
A9	GND	A10	Not used
A11	Not used	A12	Not used
A13	Not used	A14	GND
A15	Not used	A16	Not used
A17	+5V	A18	Not used
A19	Not used	A20	Not used
A21	Not used	A22	GND
A23	Not used	A24	Not used
A25	GND	A26	Not used
A27	Not used	A28	Not used
A29	Not used	A30	+5V
A31	Not used	A32	Not used
A33	GND	A34	Not used
A35	Not used	A36	Not used
A37	Not used	A38	GND
A39	Not used	A40	Not used
A41	+5V	A42	Not used
A43	Not used	A44	Not used
A45	Not used	A46	GND
A47	Not used	A48	Not used
A49	GND	A50	Not used
A51	Not used	A52	Not used
A53	Not used	A54	+5V
A55	Not used	A56	Not used
A57	GND	A58	Not used
A59	Not used	A60	Not used
A61	Not used	A62	GND
A63	Not used	A64	Not used
A65	+5V	A66	Not used
A67	Not used	A68	Not used
A69	Not used	A70	GND
A71	Not used	A72	Not used
A73	GND	A74	Not used
A75	Not used	A76	Not used
A77	Not used	A78	+5V
A79	−12V	A80	−12V
A81	GND	A82	MRUN L
A83	MRSVA83	A84	MRSVA84
A85	MDATINV L	A86	GND
A87	MBUSY L	A88	MSHARED L
A89	+5V	A90	MABORT L
A91	BHALT L	A92	BDCOK
A93	BPOK	A94	GND

The following are open collector signals that have backplane termination:

MDATINV L	MRESET L
MBUSY L	MCLKI
MSHARED L	MIRQ<3:0> L
MABORT L	

The following signals have weak pull-ups:

MDAL<31:0>	MBRM<6:0> L
MCMD<3:0>	MDPAR
MSTAT<1:0>	MSPAR
MBRQ L	MCPAR

The signals on the A block labeled MBRM<0:6> are the bus-request signals from the other slots. Table 12-6 lists the connections for the MBRQ signal from each of the slots to the other six slots.

Table 12-6: M-Bus MBRQ Connections per Slot

MBRQ	Slot9 M-bus 0	Slot8 M-bus 1	Slot7 M-bus 2	Slot6 M-bus 3	Slot5 M-bus 4	Slot4 M-bus 5	M-bus 6	Slot3 M-bus 7
MBRQ0*	B13	B15	B15	B15	B15	B15	B15	B15
MBRQ1**	B15	B13	B16	B16	B16	B16	B16	B16
MBRQ2	B16	B16	B13	B18	B18	B18	B18	B18
MBRQ3	B18	B18	B18	B13	B19	B19	B19	B19
MBRQ4	B19	B19	B19	B19	B13	B20	B20	B20
MBRQ5	B20	B20	B20	B20	B20	B13	B21	B21
MBRQ6	B21	B21	B21	B21	B21	B21	B13	B23
MBRQ7	B23	B23	B23	B23	B23	B23	B23	B13

Note: In the Firefox backplane, M-bus 6 does not exist as a physical slot.

* MBRQ0 is the MBRQ output from slot 0 (B13 from slot 0).
** MBRQ1 is the MBRQ output from slot 1 (B13 from slot 1).

The information from the previous table is restated in Table 12-7.

Table 12-7: MBRQ Wiring to MBRM per Slot

Slot	MBRM0 B15	MBRM1 B16	MBRM2 B18	MBRM3 B19	MBRM4 B20	MBRM5 B21	MBRM6 B23
M-bus 0	MBRQ1	MBRQ2	MBRQ3	MBRQ4	MBRQ5	MBRQ6	MBRQ7
M-bus 1	MBRQ0	MBRQ2	MBRQ3	MBRQ4	MBRQ5	MBRQ6	MBRQ7
M-bus 2	MBRQ0	MBRQ1	MBRQ3	MBRQ4	MBRQ5	MBRQ6	MBRQ7
M-bus 3	MBRQ0	MBRQ1	MBRQ2	MBRQ4	MBRQ5	MBRQ6	MBRQ7
M-bus 4	MBRQ0	MBRQ1	MBRQ2	MBRQ3	MBRQ5	MBRQ6	MBRQ7
M-bus 5	MBRQ0	MBRQ1	MBRQ2	MBRQ3	MBRQ4	MBRQ6	MBRQ7
M-bus 7	MBRQ0	MBRQ1	MBRQ2	MBRQ3	MBRQ4	MBRQ5	MBRQ6

MCLKA and MCLKB are radially distributed to each slot from the M-bus clock subsystem. The M-bus clock-generator components are located on the M-bus backplane.

Although the unspecified signals in the A connector block are reserved and must not be connected to any internal logic of the M-bus modules, the modules must still connect to the assigned power pins because they are part of the DC-power-distribution network.

The maximum stub length for the MCMD, MSTATUS, MDAL, and MPARITY signals is 1.5 inches, where stub length is the amount of etch between the top of the edge finger and the IC pin. Stub length of all other M-bus signals should not exceed 3.0 inches.

12.4.2. Q-Bus Backplane Signal Assignments

When the Q-bus adapter module is installed, slots 10-12 function as Q-bus slots. The Q-bus slots are implemented as A/B, A/B (no C/D interconnect). A Q-bus slot can hold one quad or two dual Q-bus modules. Because the Q-bus DMA grant and interrupt-acknowledge signals are daisy-chained, there is an order in which the Q-bus modules must be inserted to avoid the use of grant cards: the highest priority slots must be filled before the lower.

Table 12-8: Q-Bus Slot Order of Priority

Priority	Slot
Highest	10 (J19)
.	11 (J21)
.	12 (J23)
.	12 (J24)
	11 (J22)
Lowest	10 (J20)

Table 12-9: Q-Bus Backplane Signal Assignments for Slots 10-12

Connector A			Connector B		
Column 1	**Row**	**Column 2**	**Column 1**	**Row**	**Column 2**
BIRQ5	AA	+5V	BDCOK	BA	+5V
BIRQ6	AB	Not used	BPOK	BB	Not used
BDAL16	AC	GND	BDAL18	BC	GND
BDAL17	AD	+12V	BDAL19	BD	+12V
SSPARE1	AE	BDOUT	BDAL20	BE	BDAL02
SSPARE2	AF	BRPLY	BDAL21	BF	BDAL03
SSPARE3	AH	BDIN	SSPARE8	BH	BDAL04
GND	AJ	BSYNC	GND	BJ	BDAL05
MSPAREA	AK	BWTBT	MSPAREB	BK	BDAL06
MSPAREA	AL	BIRQ4	MSPAREB	BL	BDAL07
GND	AM	BIAKI	GND	BM	BDAL08
BDMR	AN	BIAKO	BSACK	BN	BDAL09
BHALT	AP	BBS7	BIRQ7	BP	BDAL10
BREF	AR	BDMGI	BEVENT	BR	BDAL11
Not used	AS	BDMGO	Not used	BS	BDAL12
GND	AT	BINIT	GND	BT	BDAL13
PSPARE1	AU	BDAL00	PSPARE2	BU	BDAL14
Not used	AV	BDAL01	+5V	BV	BDAL15

Note that the MSPARE, SSPARE, and PSPARE signals are not bussed from slot to slot.

Table 12-10: Q-Bus Backplane Signal Assignments on for Slot 9 Connector A

Pin	Signal	Pin	Signal
A1	GND	A2	BIRQ5
A3	Not used	A4	BIRQ6
A5	Not used	A6	+5V
A7	BDAL16	A8	Not used
A9	GND	A10	BDAL17
A11	Not used	A12	BDOUT
A13	Not used	A14	GND
A15	BRPLY	A16	Not used
A17	+5V	A18	BDIN
A19	Not used	A20	BSYNC
A21	Not used	A22	GND
A23	BWTBT	A24	Not used
A25	GND	A26	BIRQ4
A27	Not used	A28	BIAK01
A29	BDMR	A30	+5V
A31	BBS7	A32	BREF
A33	GND	A34	BDMGO1
A35	BINIT	A36	BDAL00
A37	BDAL01	A38	GND
A39	Not used	A40	Not used
A41	+5V	A42	BDAL18
A43	BDAL19	A44	BDAL20
A45	BDAL02	A46	GND
A47	BDAL21	A48	BDAL03
A49	GND	A50	BDAL04
A51	BDAL05	A52	Not used
A53	BDAL06	A54	+5V
A55	BDAL07	A56	Not used
A57	GND	A58	BDAL08
A59	BSACK	A60	BDAL09
A61	Not used	A62	GND
A63	BIRQ7	A64	Not used
A65	+5V	A66	BDAL10
A67	BEVENT	A68	BDAL11
A69	Not used	A70	GND
A71	BDAL12	A72	BDAL13
A73	GND	A74	BDAL14
A75	Not used	A76	BDAL15
A77	Not used	A78	+5V
A79	–12V	A80	–12V
A81	GND	A82	MRUN L
A83	MRSVA83	A84	MRSVA84
A85	MDATINV L	A86	GND
A87	MBUSY L	A88	MSHARED L
A89	+5V	A90	MABORT L
A91	BHALT L	A92	BDCOK
A93	BPOK	A94	GND

12.4.3. Graphics VI-Bus Backplane Signal Assignments

Table 12-11: VI-Bus Backplane Signal Assignments for Slot 3 on Connector A

Pin	Signal	Pin	Signal
A1	GND	A2	BUFVI31 H
A3	BUFVI30 H	A4	BUFVI29 H
A5	BUFVI28 H	A6	+5VA
A7	BUFVI27 H	A8	BUFVI26 H
A9	GND	A10	BUFVI25 H
A11	BUFVI24 H	A12	BUFVI23 H
A13	BUFVI22 H	A14	GND
A15	BUFVI21 H	A16	BUFVI20 H
A17	+5VA	A18	BUFVI19 H
A19	BUFVI18 H	A20	BUFVI17 H
A21	BUFVI16 H	A22	GND
A23	BUFVI15 H	A24	BUFVI14 H
A25	GND	A26	BUFVI13 H
A27	BUFVI12 H	A28	BUFVI11 H
A29	BUFVI10 H	A30	+5VA
A31	BUFVI09 H	A32	BUFVI08 H
A33	GND	A34	BUFVI07 H
A35	BUFVI06 H	A36	BUFVI05 H
A37	BUFVI04 H	A38	GND
A39	BUFVI03 H	A40	BUFVI02 H
A41	+5VA	A42	BUFVI01 H
A43	BUFVI00 H	A44	BUFBM3 L
A45	BUFBM2 L	A46	GND
A47	BUFBM1 L	A48	BUFBM0 L
A49	GND	A50	BUFWR L
A51	DATAS L	A52	BUFDS L
A53	GRSVA53 H	A54	+5VA
A55	GRSVA55 H	A56	GRSVA56 H
A57	GND	A58	GRSVA58 H
A59	GRSVA59 H	A60	GRSVA60 H
A61	GRSVA61 H	A62	GND
A63	GRSVA63 H	A64	INIT L
A65	+5VA	A66	GRSVA66 H
A67	GRSVA67 H	A68	GRSVA68 H
A69	GRSVA69 H	A70	GND
A71	Not used	A72	Not used
A73	GND	A74	Not used
A75	GRSVA75 H	A76	Not used
A77	Not used	A78	+5VA
A79	–12V	A80	–12V
A81	GND	A82	MRUN L
A83	MRSVA83 H	A84	MRSVA84 H
A85	MDATINV L	A86	GND
A87	MBUSY L	A88	MSHARED L
A89	+5VA	A90	MABORT L
A91	BHALT L	A92	BDCOK H
A93	BPOK H	A94	GND

Table 12-12: VI-Bus Backplane Signal Assignments for Slots 1 and 2 on Connector A

Pin	Signal	Pin	Signal
A1	GND	A2	BUFVI31 H
A3	BUFVI30 H	A4	BUFVI29 H
A5	BUFVI28 H	A6	+5VA
A7	BUFVI27 H	A8	BUFVI26 H
A9	GND	A10	BUFVI25 H
A11	BUFVI24 H	A12	BUFVI23 H
A13	BUFVI22 H	A14	GND
A15	BUFVI21 H	A16	BUFVI20 H
A17	+5VA	A18	BUFVI19 H
A19	BUFVI18 H	A20	BUFVI17 H
A21	BUFVI16 H	A22	GND
A23	BUFVI15 H	A24	BUFVI14 H
A25	GND	A26	BUFVI13 H
A27	BUFVI12 H	A28	BUFVI11 H
A29	BUFVI10 H	A30	+5VA
A31	BUFVI09 H	A32	BUFVI08 H
A33	GND	A34	BUFVI07 H
A35	BUFVI06 H	A36	BUFVI05 H
A37	BUFVI04 H	A38	GND
A39	BUFVI03 H	A40	BUFVI02 H
A41	+5VA	A42	BUFVI01 H
A43	BUFVI00 H	A44	BUFBM3 L
A45	BUFBM2 L	A46	GND
A47	BUFBM1 L	A48	BUFBM0 L
A49	GND	A50	BUFWR L
A51	DATAS L	A52	BUFDS L
A53	GRSVA53 H	A54	+5VA
A55	GRSVA55 H	A56	GRSVA56 H
A57	GND	A58	GRSVA58 H
A59	GRSVA59 H	A60	GRSVA60 H
A61	GRSVA61 H	A62	GND
A63	GRSVA63 H	A64	INIT L
A65	+5VA	A66	GRSVA66 H
A67	GRSVA67 H	A68	GRSVA68 H
A69	GRSVA69 H	A70	GND
A71	MX23B3 H	A72	MX23B2 H
A73	GND	A74	MX23B1 H
A75	GRSVA75 H	A76	MX23B0 H
A77	NIBCLK H	A78	+5VA
A79	−12V	A80	−12V
A81	GND	A82	MX22B3 H
A83	MX22B2 H	A84	MX22B1 H
A85	CMP5 H	A86	GND
A87	CMP4 H	A88	CMP3 H
A89	+5VA	A90	CMP2 H
A91	CMP1 H	A92	CMP0 H
A93	BPOK H	A94	GND

Table 12-13: VI-Bus Backplane Signal Assignment for Slots 1 and 2 on Connector B

Pin	Signal	Pin	Signal
B1	GND	B2	not used
B3	MX22B0 H	B4	GND
B5	GND	B6	+5VA
B7	MX21B3 H	B8	GND
B9	GND	B10	+12VA
B11	+12VA	B12	+12VA
B13	MX21B2 H	B14	GND
B15	MX21B1 H	B16	MX21B0 H
B17	+5VA	B18	MX20B3 H
B19	MX20B2 H	B20	MX20B1 H
B21	MX20B0 H	B22	GND
B23	MX19B3 H	B24	MX19B2 H
B25	GND	B26	MX19B1 H
B27	MX19B0 H	B28	MX18B3 H
B29	MX18B2 H	B30	+5VA
B31	MX18B1 H	B32	MX18B0 H
B33	GND	B34	MX17B3 H
B35	MX17B2 H	B36	MX17B1 H
B37	MX17B0 H	B38	GND
B39	MX16B3 H	B40	MX16B2 H
B41	+5VA	B42	VISLOT H
B43	MX16B1 H	B44	MID0
B45	MID1	B46	GND
B47	MID2	B48	MX16B0 H
B49	GND	B50	GND
B51	MX15B3 H	B52	MX15B2 H
B53	MX15B1 H	B54	+5VA
B55	MX15B0 H	B56	MX14B3 H
B57	GND	B58	MX14B2 H
B59	MX14B1 H	B60	MX14B0 H
B61	GND	B62	GND
B63	MX13B3 H	B64	MX13B2 H
B65	+5VA	B66	MX13B1 H
B67	MX13B0 H	B68	MX12B3 H
B69	MX12B2 H	B70	GND
B71	MX12B1 H	B72	MX12B0 H
B73	GND	B74	MX11B3 H
B75	MX11B2 H	B76	MX11B1 H
B77	MX11B0 H	B78	+5VA
B79	MX10B3 H	B80	MX10B2 H
B81	GND	B82	MX10B1 H
B83	MX10B0 H	B84	MX09B3 H
B85	MX09B2 H	B86	GND
B87	MX09B1 H	B88	MX09B0 H
B89	+5VA	B90	MX08B3 H
B91	MX08B2 H	B92	MX08B1 H
B93	MX08B0 H	B94	GND

12.4.4. Primary-Power-Supply Connector Signal Assignment

The primary-power-supply connector (J50) located near slot 1 distributes +5 volts, +12 volts, and power to the fans. Power connector signal assignments on connector J50 appear in Table 12-14.

Table 12-14: Power Connector Signal Assignment on Connector J50

Pin	Signal	Pin	Signal
1	FANAPLUS	2	FANAMINUS
3	FANBPLUS	4	FANBMINUS
5	+5VA	6	+5VA
7	+5VA	8	+5VA
9	+5VA	10	+5VA
11	+5VA	12	+5VA
13	+5VA	14	+5VA
15	+5VA	16	+5VA
17	+5VA	18	+5VA
19	+5VA	20	+5VA
21	+5VA	22	GND
23	GND	24	GND
25	GND	26	GND
27	GND	28	GND
29	GND	30	GND
31	GND	32	GND
33	GND	34	GND
35	GND	36	GND
37	GND	38	GND
39	GND	40	GND
41	GND	42	GND
43	GND	44	GND
45	GND	46	GND
47	GND	48	GND
49	+12VA	50	+12VA
51	+12VA	52	+12VA
53	+12VA	54	BDCOK
55	BEVENT L	56	BPOK

12.4.5. Expansion-power-supply connector Signal Assignment

The Expansion-power-supply connector (J51) located near slot 12 distributes +5 volts and +12 volts to slots 7-12.

Table 12-15: Power Connector Signal Assignment on Connector J51

Pin	Signal	Pin	Signal
1	Not used	2	Not used
3	Not used	4	Not used
5	+5VB	6	+5VB
7	+5VB	8	+5VB
9	+5VB	10	+5VB
11	+5VB	12	+5VB
13	+5VB	14	+5VB
15	+5VB	16	+5VB
17	+5VB	18	+5VB
19	+5VB	20	+5VB
21	+5VB	22	GND
23	GND	24	GND
25	GND	26	GND
27	GND	28	GND
29	GND	30	GND
31	GND	32	GND
33	GND	34	GND
35	GND	36	GND
37	GND	38	GND
39	GND	40	GND
41	GND	42	GND
43	GND	44	GND
45	GND	46	GND
47	GND	48	GND
49	+12VB	50	+12VB
51	+12VB	52	+12VB
53	+12VB	54	BDCOK
55	+12VB	56	BPOK

12.4.6. Fan Connector Signal Assignments

The primary-power-supply distributes power to fans A and B through the Fan connector J52 located near slot 1.

Table 12-16: Fan Connector J52 Signal Assignment

Pin	Signal
1	FANAPLUS
2	No signal (used for keying)
3	FANAMINUS
4	FANBPLUS
5	FANBMINUS

12.4.7. External Connector Signal Assignments

The External Connector (J53) sends signals to the RF distribution panel. J53 signal assignments appear in Table 12-17.

Table 12-17: External Connector Signal Assignments on Connector J53

Pin	Signal	Pin	Signal
1	+5VA	2	+5VA
3	BHALT L	4	GND
5	GND	6	GND
7	BPOK	8	Not used
9	BDCOK	10	MRUN L