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PC11
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reader/punch and
control manual

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FOREWORD

This manual provides the user with the theory of operation and block diagrams necessary to understand and maintain the PC11 High-Speed Paper-Tape Reader/Punch and Control. This manual is directed at the reader who is familiar with basic digital computer theory. Consequently, this manual contains both general and detailed descriptions of the PC11 Reader/Punch and Control.

Control signals and data are transferred between the PC11 Reader/Punch Control and the Unibus(TM) ; however, this manual does not cover the operation of the Unibus. A detailed description of the Unibus is presented in the PDP-11 Peripheral Handbook.

The PC11 Reader/Punch Control is basically an interface between the bus and the PC05 High-Speed Paper-Tape Reader/Punch; however this manual does not discuss operation of thePC05 unit. For a detailed discussion of the operation and maintenance of the PC05 High-Speed Paper-Tape Reader/Punch consult the *PC04/PC05 Paper-Tape Reader/Punch Maintenance Manual* (DEC-00-HPCAA-C-D).

A complete set of reduced engineering drawings and module circuit schematics is provided in a companion volume to this manual which is entitled *PC11 High-Speed Paper-Tape Reader/Punch, Engineering Drawings.*

This manual is divided into five chapters:

a. introduction
b. installation
c. operation and programming
d. detailed description
e. maintenance

The following publications provide additional information about the PDP-11 System and the PC05 Reader/Punch:

Document Title	Number	Information
Applicable PDP-11 System Manual		A description of the overall system and of the instruction set.
H720 Power Supply and Mounting Box Manual	EK-H720-TM-003	This manual depicts the physical construction and locations of parts, and a description of the power supply.
PDP-11 Paper-Tape Software Programming Handbook	DEC-11-XPTSA-A-D	This manual describes the use of devices in the operating environment, and programming instructions.

(continued on next page)

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Document Title	Number	Information
PC04/PC05 Paper-Tape Reader/Punch Maintenance Manual	DEC-00-HPCAA-C-D	A description of the operating controls, physical construction, and logic of both the PC04 and PC05 units.
PDP-11 Processor Handbook	DEC, 1972	Discusses PDP-11 processor and software including system architecture, addressing modes, instruction set, and programming techniques.
PDP-11 Peripherals Handbook		Discusses various peripherals (including the PC11). Also covers Unibus and external device logic including examples of typical interfaces.

CHAPTER 1
INTRODUCTION

The PC11 Reader/Punch and Control comprises a PC05 High-Speed Paper-Tape Reader/Punch, a PC11 Control, and two connecting cables.

The PC05 High-Speed Paper-Tape Reader/Punch can be controlled by any PDP-11 System through a PC11 Reader/Punch Control. The PC05 serves as an input device (from eight-channel perforated paper tape) and an output device (to the same medium) for the sytem.

The PC11 Reader/Punch Control directs the operation of the PC05 Reader/Punch, which can be operated for single data transfers or for continuous data transfer. The PC11 controls the parallel transfer of an eight-bit byte between the Unibus and the PC05.

A PC11 Reader/Punch Control consists of a single quad module mounted on one-fourth of a system unit (DD11-A Peripheral Mounting Panel or any system unit slot wired as a DD11-A equivalent, such as slots 13 and 14 in the KA11 Processor). Thus, four PC11 Reader/Punch Controls can be mounted in the space of a single system unit.

Two variations of the PC11 device are available from Digital Equipment Corporation (DEC). The PC11-A is designed for operation at 50 Hz power. The PR11 is a reader without a punch; it uses equipment identical to the reader portion of the PC11. When a 240V power supply provides power to any of these devices, an H722 Step-Down Transformer must be connected to the PC05 power supply.

1.1 FUNCTIONAL DESCRIPTION

The PC11 Control operates one PC05 High-Speed Paper-Tape Reader/Punch. The PC05 combines a photoelectric paper-tape reader and an electromechanical paper-tape punch in a 10-1/2 in. high frame that mounts in a standard 19-in. rack.

The paper-tape reader comprises: *a)* a light source, *b)* a set of photodiodes to translate the presence or absence of holes (in the tape) to logic levels representing 1s and 0s, *c)* a tape transport mechanism to move and position the paper tape between the light source and the read head, and *d)* bins to hold and collect the tape that passes through the reader. In addition to transferring an eight-bit byte from the paper tape to the PC11 Control, the reader can inform the PC11 Control of the reader's status. The specific indications of reader status are presented in Paragraph 3.1.

The paper-tape punch comprises: *a)* a punch drive motor, *b)* a punch mechanism that translates logic levels representing 1s and 0s to the presence or absence of holes in the tape, and *c)* a mechanism to advance the tape and position it under the punch mechanism. A supply of fan-folded paper tape is loaded into the PC05, and the tape, which is output by the punch, is collected in a bin accessible from the front of the PC05. The punch also provides signals to the PC11 Control to indicate its status; these signals are described in Paragraph 3.1.

Any information read or punched by the PC05 Reader/Punch is parallel transferred through the PC11 Control. One data path is used for input from the reader, and one path is used for output to the punch. The PC11 Reader/Punch Control enables the processor to determine the status of the PC05 device, to initiate device operations, and to control the use of the bus interrupt logic by the PC11.

When an address is placed on the Unibus, the PC11 Control decodes the address and determines if the reader or punch has been selected. If one of the four device register addresses assigned to the PC11 is selected, the PC11 Control determines whether an input or an output operation should be performed.

The PC11 Reader/Punch Control consists of four functional parts (Figure 1-1): the address selection logic, the interrupt control, the punch control, and the reader control (four device register addresses that are divided into the two controls). The device register addresses are determined by the location of jumpers in the address selection logic. These addresses are four sequential word addresses, assigned in ascending order to the device registers. The names, mnemonics, functions, and normally assigned addresses for the four registers are shown in Table 1-1.

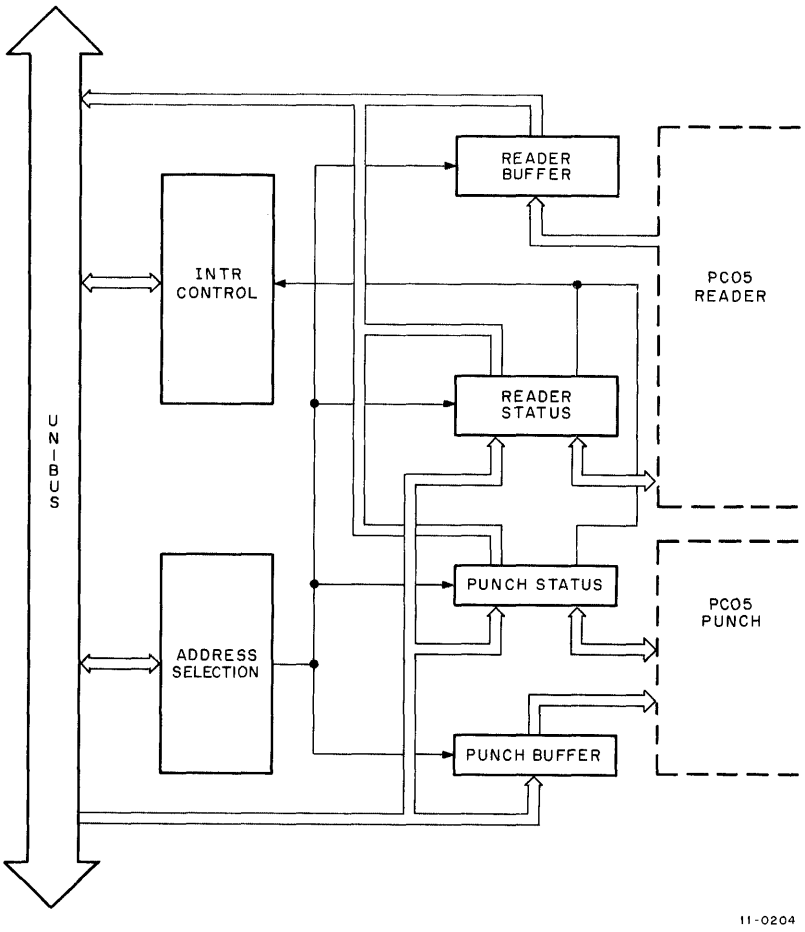

Figure 1-1 Simplified Block Diagram

Table 1-1
PC11 Device Registers

Name	Address	Mnemonic	Function
Paper-Tape Reader Status Register	777550	PRS	Provides indications of reader status, controls interrupts by the reader, and initiates reading.
Paper-Tape Reader Buffer Register	777552	PRB	Read-only register that gates data from the reader. Information is in low byte.
Paper-Tape Punch Status Register	777554	PPS	Provides indications of the punch device status and controls interrupts by the punch.
Paper-Tape Punch Buffer Register	777556	PPB	Write-only gating to the punch. Punching begins when the buffer in the punch is loaded.

An input operation from the reader is initiated when the processor transmits a command to the Paper-Tape Reader Status (PRS) register. The reader encodes and transmits one byte of data from a frame on the paper tape and then advances the tape. If the tape is in motion, the reader waits until the next frame of tape is in position over the read head, reads that frame, and advances the tape. In the reader, the transmitted word is stored in a buffer that can be read through the Paper-Tape Reader Buffer (PRB) register. A flag is then set, signifying that a byte of data is available. The processor may test the PRS to determine if this flag is set, or may enable interrupts from the reader. When the new data is available in the PRB, the processor executes an instruction that moves the contents of the PRB to another bus location. The PRB is not cleared until the processor initiates another read operation.

An output operation is initiated when the processor transfers a byte to the Paper-Tape Punch Buffer (PPB) register. The punch mechanism waits until the punch rotor is synchronized with the punch head; it then punches the character and begins moving the tape forward to position it for the next punch operation. The processor can test the Paper-Tape Punch Status (PPS) register to determine if the current punch operation has been completed, or an interrupt service routine can be used.

1.2 SPECIFICATIONS

The physical structure, environmental specifications, and power supply requirements of the PC11 are presented in the following paragraphs. Corresponding specifications for the PC05 High-Speed Paper-Tape Reader/Punch are located in the *PD04/PC05 Paper-Tape Reader/Punch Maintenance Manual* (DEC-00-HPCAA-C-D).

1.2.1 Physical Description

The PC11 Reader/Punch and Control is a small peripheral control device for the PDP-11. The PC11 consists of a single quad module that occupies four module slots in one row of the KA11 Processor (row 13 or row 14), or any one row of a DD11-A Peripheral Mounting Panel, or appropriate slots in other PDP-11 family processors. Two BC08J cables connect the M7810 quad module to the PC05 Reader/Punch (only one cable is needed for a PR11).

1.2.2 Specifications

Specifications for the PC11 are listed in Table 1-2.

Table 1-2
PC04/PC05 Specifications

Specification	Description
Physical dimensions	Height: 10.5 in. Width: 19 in. Depth: 15 in.
Tape characteristics	Reader: Gray, unoiled, fan-folded* Punch: Oiled or unoiled, fan-folded
Tape tension (in punch)	6 oz, maximum
Power requirements	115 Vac ± 10%, 50 or 60 Hz
Power supplies (internal)	Regulated, -15V ± 1V Regulated, +5V ± 0.25V Unregulated, -36V ± 4V
Logic levels	Logic 1 (H): +2.0V, input +2.4V, output Logic 0 (L): +0.8V, input +0.4V, output
Temperature (Operating)	Reader: 55° to 110°F Punch: 55° to 110°F
Temperature (Nonoperating)	Reader: 10° to 150°F Punch: 10° to 150°F
Humidity** (Operating)	Reader: 20 to 95% (w/o condensation) Punch: 20 to 95% (w/o condensation)
Humidity (Nonoperating)	Reader: 5 to 95% (w/o condensation) Punch: 5 to 95% (w/o condensation)

* Tape of up to 12% transmittance may be used. Consult DEC for operation of reader with more transparent tape.

** The humidity specifications are for the reader/punch mechanism. Paper-tape manufacturers' recommendations for operating environment should be followed. Suppliers of paper tape include Digital Equipment Corporation and Carter Rice Storrs and Bement.

1.2.3 Power Requirements

The PC11 Control logic draws all necessary power from the power supply*, located in the mounting box. The power required is approximately 1.5A at +5V.

*The PDP-11/20 System uses an H720 Power Supply.

CHAPTER 2
INSTALLATION

This chapter contains the procedures necessary for installing the PC11 Control. The installation procedure is a function of the system configuration and the address and priority assignments, which dictate the presence or absence of jumpers. When a configuration has been selected, the user must assign and implement addresses, interrupt vectors, and priorities. After the hardware modifications required for the selected values have been completed and the physical components of the system have been connected, the installation can be verified by testing the new hardware and the system.

2.1 CONFIGURATIONS

The PC11 Control is available in one standard configuration that includes a PC05C Reader/Punch. The PR11 Reader Control is a similar configuration to the PC11; however, it requires only one BC08J cable. This configuration is used to control a PC05R Paper-Tape Reader.

2.2 CABLING AND TERMINATIONS

The PC11 module fits into slots in a system unit. These slots, in turn, are connected to the Unibus signal paths by back-panel wiring. Signals are transmitted from the PC11 to the PC05 through two BC08J cables that plug into two connectors on one side of the M7810 Reader/Punch Control Module. The BC08J cable is tied to an M953 Connector Module that plugs into the PC05 and a Berg Connector that plugs into the M7810 module. These connectors are labeled READER and PUNCH on the M7810 board. The READER cable plugs into slot B09 in the PC05 and the PUNCH cable plugs into slot B10 in the PC05.

2.3 ADDRESS AND PRIORITY ASSIGNMENTS

Each PC11 uses four device register addresses, two interrupt vector address pairs, and a bus priority level assignment. There are certain constraints, however: *a)* the device register addresses must be four contiguous word addresses with least significant digits ranging from 0 to 7; *b)* the two interrupt vector pairs must be directed to contiguous vector addresses differing only in the least significant digit; *c)* the interrupt priority levels must be on the same major priority level for the punch and for the reader. Consequently, only three hardware assignments are required.

The device register addresses are assigned by the address selection logic. This logic, as supplied with the PC11, is preset by jumpers to respond to addresses between 777550 and 777557. A different series of addresses can be selected by changing the jumper arrangement, but care must be taken to use addresses not assigned to other devices in the system. Any change from DEC-assigned addresses requires program changes before the DEC-supplied system programs and diagnostic programs will operate with the system. The order in which addresses are assigned to the device registers is presented in Paragraph 3.1.

The two interrupt vectors are: the reader interrupt vector, and the punch interrupt vector. The reader interrupt vector is normally assigned the value of 70 by jumpers on the interrupt control logic. The punch interrupt vector, which differs only in address bit 2, has the value 74. These values can be changed by modifying the jumper arrangement. The same cautions listed for the device register addresses must be adhered to for the interrupt vector addresses.

The bus major priority level is determined by a request and grant jumper plug that mounts into a receptacle on the module. The M7810 module is normally supplied with a jumper plug that provides a BR4 priority level. However, this jumper plug can be replaced with one that selects a higher priority level if desired. The reader has a higher priority level than the punch if both request service simultaneously, because the bus grant signal must pass through the reader interrupt logic before reaching the punch interrupt logic.

2.4 POWER CONNECTIONS

The PC11 Control draws all electrical power from the system unit in which it is mounted. Power is supplied to the system by a power supply located in the mounting box. The PC05 Reader/Punch includes an integral power supply that is connected to the system power supply; status signals from the PC05 to the PC11 include signals that indicate whether the power supply is connected to the main voltage.

2.5 INSTALLATION VERIFICATION

When all system components have been connected and adjusted, the installation can be verified by running the PC11 High-Speed Reader and Punch Diagnostic Test (MainDEC-11-D2BB-D).

NOTE

The DEC-supplied test will operate only with the standard address and interrupt vector assignments, but can be modified (consult the document) to operate with non-standard address and interrupt vectors.

CHAPTER 3
OPERATION AND PROGRAMMING

This chapter describes the operation and programming of the PC11 Reader/Punch and Control. The PC11 Control responds to processor commands through operations that are initiated and controlled by bits in the device registers. The device registers are presented in Paragraph 3.1. Technical details in the application of these registers are described in Paragraphs 3.2 through 3.4. Paragraph 3.5 provides examples for programming the device, and Paragraph 3.6 describes the program modifications required if the system has been assigned non-standard addresses and vectors.

The PC05 Reader/Punch has manual power controls and manual feed switches, located on the front panel, for operation of the tape advance feature of both the reader and punch. All other operations of the PC05 are program-controlled.

3.1 DEVICE REGISTERS

The PC11 comprises four device registers (the PR11 uses only the first two device registers, which are assigned to the read function). These registers are described in order of ascending addresses. The descriptions that follow include: *a)* the normally assigned address; *b)* the mnemonic suggested for use with the PAL-11 assembly program to address the register; *c)* a bit assignment map illustrating the use of each register; *d)* INIT, the initialization signal issued by the processor during power up or power down, by the START switch, or during a RESET instruction; and *e)* loading "unused" or "read-only" bits has no effect on the bit position.

Name: Paper-Tape Reader Status Register (Figure 3-1)
Mnemonic: PRS
Address: 777550

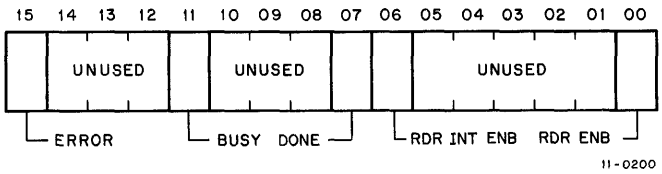

Figure 3-1 Reader Status Register Bit Assignments

Bit	Name	Function
00	Reader Enable (RDR ENB)	Write-Only. Always reads as a 0. If a 1 is loaded into this bit, a read cycle is started, BUSY is set, DONE is cleared, and the PRB is cleared.
06	Reader Interrupt Enable (RDR INTR ENB)	Read/Write. Cleared by INIT. When this bit is set, DONE or ERROR becoming set starts an interrupt sequence.
07	DONE	Read-Only. This bit is set when a new data byte is available and cleared when RDR ENB is set, or the PRB is read, or an INIT signal occurs. If RDR INTR ENB is also set, an interrupt sequence is started.
11	BUSY	Read-Only. This bit indicates that the reader is completing an operation. BUSY is set when RDR ENB is set, and cleared when the present operation is complete (DONE is set).
15	ERROR	Read-Only. This bit is set to indicate that one of the following conditions has occurred: *a)* reader out of tape, *b)* reader off-line, *c)* no power to reader. This bit starts an interrupt sequence if RDR INTR ENB is set. If the error condition has not been cleared manually, and an attempt to set RDR ENB is made, an immediate interrupt occurs, and no operation is initiated.

Name: Paper-Tape Reader Buffer Register (Figure 3-2)
Mnemonic: PRB
Address: 777552

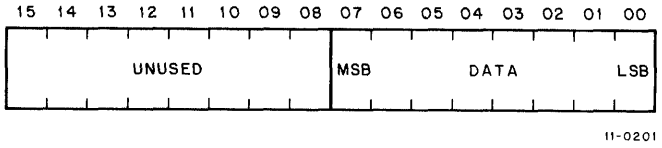

Figure 3-2 Reader Buffer Register Bit Assignments

Bit	Name	Function
07-00	Data (07:00)	This register transfers eight bits of data from the PC05 reader to the Unibus. The register is read-only; it responds to DATO operations, but the contents of the register are unchanged. The most significant bit of register is bit 07, and the least significant bit is bit 00. (For more information on the bit assignments in the PC05, PC11, and PDP-11 Systems, refer to Appendix A.)

Name: Paper-Tape Punch Status Register (Figure 3-3)
Mnemonic: PPS
Address: 777554

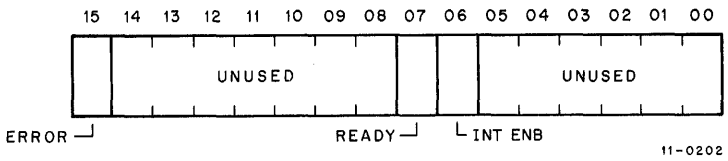

Figure 3-3 Punch Status Register Bit Assignments

Bit	Name	Function
06	Punch Interrupt Enable (PUN INTR ENB)	Read/Write. Cleared by INIT. When this bit is set, either READY or ERROR can start an interrupt sequence.
07	READY	Read-Only. This bit signifies that the punch can accept a byte for transfer to the paper tape. This bit is set when the current operation is completed, or by INIT, and cleared when the PPB is loaded. This bit starts an interrupt sequence if PUN INTR ENB is set.
15	ERROR	Read-Only. This bit indicates that one of the following conditions has occurred: *a)* punch out of tape, *b)* no power to punch. If PUN INTR ENB is set, this bit causes an interrupt. If an attempt to punch a character is made before the error condition has been manually corrected, an immediate interrupt can occur.

Name: Paper-Tape Punch Buffer Register (Figure 3-4)
Mnemonic: PPB
Address: 777556

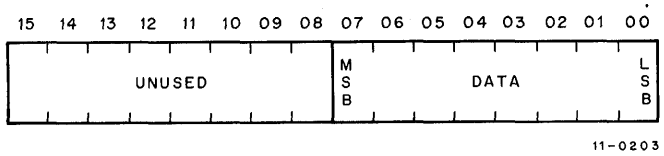

Figure 3-4 Punch Buffer Register Bit Assignments

Bit	Name	Function
07-00	Data (07:00)	Write-Only. Loading a byte into the PPB register clears READY in the PPS register and begins a new cycle of punch operation. The contents of the PPB register cannot be read to the bus. Refer to Appendix A for information on the bit assignments in the PC05, PC11, and PDP-11.

3.2 ADDRESSES

The standard addresses for the PC11 device registers are listed in Paragraphs 1.1 and 3.1. The address assigned to these registers must be four contiguous word addresses, with bits 17–13 all 1s and bits 12–3 identical for all four addresses. Consequently, the addresses must be in the form n, n+2, n+4, and n+6, where n is divisible by eight and is in the range 760000 to 777770.

The address selected must not be assigned to any other device on the Unibus. Certain addresses in this range are assigned to internal storage within the processor; these addresses, which must not be assigned to any device, are listed in both the *PDP-11 Processor Handbook and the PDP-11 Peripherals Handbook.*

The address assignments for the PC11 must maintain the device register sequence of the standard assignments. This sequence is shown in Table 3-1.

Table 3-1
Sequence of Standard Assignments

Device Register Mnemonic	Relative Address
PRS	N
PRB	N+2
PPS	N+4
PPB	N+6

3.3 TIMING CONSIDERATIONS

The timing of PC11 Control operations is dictated by a cycle of operations in the PC05, which is dependent on the direction of the data transfers. For each data transfer, the PC05 Reader/Punch executes a cycle of operations that includes positioning the paper tape, conducting an internal data transfer, and participating in a data transfer with the Unibus (through the PC11 Control).

3.3.1 Reader Timing

When the RDR ENB bit of the PRS register is set for a previously inactive reader (BUSY=0), the PC11 clears the DONE bit of the PRS register and sets the BUSY bit. The frame of the paper tape currently over the read head is transmitted to a buffer register in the PC05, and the PC05 begins moving the paper tape to position the next frame over the read head. When the buffer is loaded, the DONE bit of the PRS register is set, signifying that a byte is ready to transfer. The BUSY bit is cleared. When the PRB is read (addressed), the DONE bit is cleared.

The processor can transfer the contents of the PRB register as soon as the DONE bit becomes set. If the processor sets the RDR ENB bit again, the DONE bit is cleared again, and the PC11 Control is ready to begin another reader cycle as soon as the paper tape is repositioned. The programmer does not have to test the BUSY bit or wait until it is clear before beginning another cycle, provided he is testing the DONE bit.

When the reader is started from idle, the first character is read immediately, and the tape is advanced. This tape advance is controlled by the reader clock in the PC05. The reader clock produces pulses that: *a)* control the stepping motor that advances the tape, *b)* strobe the data into the reader buffer, *c)* set the reader flag when new data is available, and *d)* determine when to stop the movement of the paper tape. During continuous operation, the clock maintains a character rate of 300 characters/second by running on a 3.33 ms cycle. This speed is

maintained as long as the PC11 receives another read command within 1/2 cycle (1.67 ms) after the DONE bit of the PRS is set. If no further read operations are requested, the reader stops the tape.

A late read command is not executed until the reader comes to a stop, then the tape motion is started again. The starting motion is slower than the continuous motion because it must accelerate the tape from a standstill. The reader clock is controlled by an acceleration circuit that extends the first few clock periods while the tape is reaching proper operating speed. Therefore, when the tape is moved in a start-stop fashion (because the read commands are not frequent enough to maintain continuous motion), the reader operates at a slower rate. The maximum speed for single-character operation (which occurs whenever the read commands are more than 1.67 ms apart) is approximately 25 characters/second.

The PC11 operating speed will affect the total time necessary to complete a data transfer program; however, it does not change the instruction sequence. The programming necessary to control a PC11 is independent of the operating speed.

3.3.2 Punch Timing

The PC05 Punch operates at a fixed cycle time of 20 ms, resulting in a punching rate of 50 characters/second. If the punch is idle, and a punch command is received (the PPB is loaded): *a)* the punch motor is turned on, *b)* the punch mechanism accelerates up to speed while a 1-sec timer delays punching, *c)* the punch unit punches the data into the tape and advances the tape one frame, and *d)* the PC05 signals that it is ready to begin another operation.

A second timer keeps the punch running for 3 sec after the last command is executed (the timer restarts after each punch command). When the punch motor is running, any punch command received within 10 ms after the READY bit of the PPS is set is executed during the next punch cycle. Punch commands that are delayed more than 10 ms after READY is set are delayed until the following punch cycle (an extra delay of 20 ms).

The timing considerations for the punch affect only the throughput of the PC11, not the programming. The instructions required to operate the PC11 Reader/Punch and Control are independent of the effective speed of operation.

3.4 DATA FORMATS

The paper tape processed by the PC11 Reader/Punch and Control is 1-in. wide, eight-channel tape. Each byte of data is punched into one frame that consists of eight data positions arranged in a line perpendicular to the length of the tape. A hole punched in a data position represents a 1; a 0 is represented by the absence of a hole.

The data positions are numbered from 0 to 7, with 0 the least significant bit and 7 the most significant bit. The feed hole, which is punched for every frame, is positioned between channels two and three (a channel is composed of one data position in successive frames of tape, i.e., a row of holes and unpunched positions extending the length of the tape). Figure 3-5 illustrates the tape format.

3.5 PROGRAMMING EXAMPLES

The PC11 Control enables the PDP-11 System to control the reading or punching of paper tape in a flexible manner. The reader can be operated independently of the punch, and either device can be under direct program control or can operate without direct supervision through the use of interrupts, to maintain continuous operation.

The examples provided in this section illustrate four types of programs that can be used with the PC11. These programs include: *a)* direct control of the reader, *b)* interrupt control of the reader, *c)* direct control of the punch, and *d)* interrupt control of the punch.

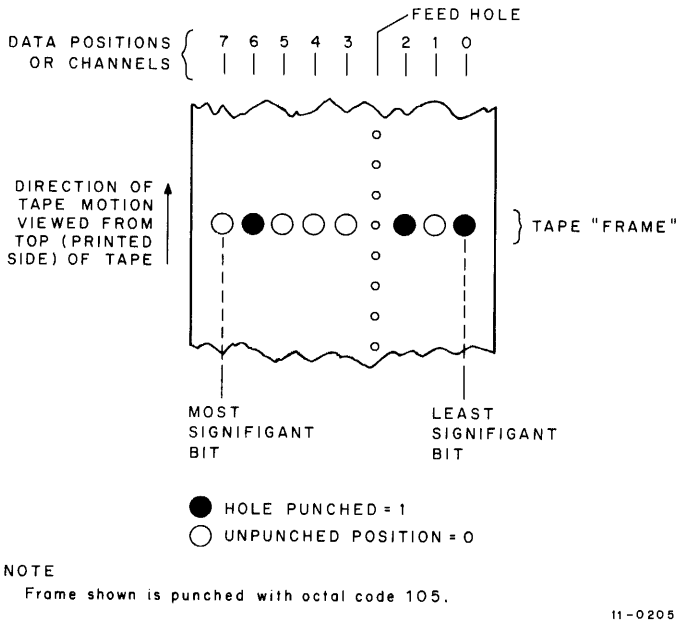

Figure 3-5 Paper-Tape Format

3.5.1 Program Control of the Reader

The sequence of instructions that follows reads one byte from the paper tape and deposits it in general register 0. If a reader error is sensed, the program branches to an error routine, which may type out a message and then wait for operator intervention.

```
READ:   INC   PRS        ;SET RDR ENB
LOOP:   TST   PRS        ;LOOK FOR ERROR
        BMI   ERR        ;BRANCH ON ERROR=1
        TSTB  PRS        ;LOOK FOR DONE
        BPL   LOOP       ;WAIT IF DONE=0
        MOV   PRB, R0    ;READ CHARACTER
```

A shorter form of the test loop is possible, as shown below:

```
READ:   INC   PRS
LOOP:   BIT   #100200, PRS  ;TEST BITS 15 and 7
        BEQ   LOOP          ;WAIT IF NO BITS SET
        BMI   ERR           ;ERROR IF BIT 15 SET
        MOV   PRB, R0       ;IF BIT THAT IS SET IS
                            ;NOT BIT 15, MUST BE
                            ;BIT 7
```

3.5.2 Reader Interrupt Service

The PDP-11 System can combine PC11 operations with other processing by using the interrupt mode of device operation. When a device operation has been initiated, the PC11 continues without supervision until the operation is complete (or an error occurs); the remainder of the PDP-11 System is free to perform other operations. When the PC11 Control requires further service, the processor is notified by an interrupt.

Each device that is operated in an interrupt mode must be initialized by commands from the processor. An interrupt service routine and an interrupt vector (at the address corresponding to the vector address selected by the jumpers on the interrupt control logic) must be provided.

The program that follows can be used to read a block of 128 characters from the paper tape to a buffer.

```
START:    MOV     #-200, R0          ;INITIALIZE COUNTER
          MOV     #101, PRS          ;SET INTR ENB AND RDR ENB
HANG:     BR      HANG               ;HANG UP HERE UNTIL BLOCK
                                     ;IS READ
                  .
                  .
70:       RDRINT                     ;VECTOR TO INTERRUPT ROUTINE
72:       200     .                  ;SETS STATUS TO PRIORITY 4
                  .
RDRINT:   TST     PRS                ;TEST FOR ERROR
          BMI     ERR                ;TYPE OUT MESSAGE IF ERROR
          MOVB,   PRB, BUFEND(R0)    ;FILL BUFFER STARTING AT
                                     ;BUFEND-200 (OCTAL)
          INC     R0                 ;COUNT ONE BYTE AND MOVE POINTER
          BEQ     OUT                ;WHEN COUNT IS ZERO, EXIT LOOP
          INC     PRS                ;ENABLE READER AGAIN
          RTI                        ;RETURN FROM INTERRUPT
OUT:      ADD     #4, SP             ;UNSTACK INTERRUPT PC AND PS
          CLR     PRS                ;INHIBIT FURTHER INTERRUPTS
          JMP     HANG+2             ;CONTINUE MAIN PROGRAM
```

NOTE

The position of the buffer used by this program is specified by the end of the buffer, not the beginning. The indexed address uses the negative counter values to access bytes at decreasing distances from this base address.

Two operations performed by this program require caution. When a program accesses the same or contiguous locations, the program operating speed increases if the locations are addressed through a register. If this is done, either no other use can be made of this register or: *a)* the interrupt service routine must stack the former contents of the register, *b)* the counter must be moved from a temporary storage location to the register, *c)* the register must be used, and *d)* the storage operations reversed. In this example, where the processor does not do any other processing, no conflicts with the use of the register occur.

A second caution refers to the terminating exit from the service routine. When the exit does not occur through an RTI instruction, the main program PC *(Program Counter)* and PS *(Processor Status)* words that are stacked by the interrupt must be removed from the stack. The ADD instruction at OUT performs this operation. If this operation is not performed, the values stacked by other operations previous to the interrupt are not properly accessible.

3.5.3 Punch Programmed Service

The sequence of instructions that follows transfers one byte from register 0 to the paper tape. When controlling the punch, the READY bit of the PPS register is checked before the transfer; when controlling the reader, the DONE bit of the PRS register is checked after a command.

```
                .
                .
PUNCH:    BIT   #100200, PPS     ;CHECK PUNCH STATUS
          BEQ   PUNCH            ;IF NOT READY OR ERROR, WAIT
          BMI   ERROR            ;PROCESSOR ERROR IF ANY
          MOV   R0, PPB          ;OUTPUT CHARACTER
                .
                .
```

3.5.4 Punch Interrupt Service

This interrupt service routine outputs 8-bit codes to the paper tape, unless they are ASCII representations of the formatting characters Line Feed, Rubout, or Form Feed. Line Feeds and Rubouts are ignored (not punched), and the program stops punching when the character read from the buffer is a Form Feed. The Form Feed is not punched. The program transfers the contents of a buffer: *a)* starting at a preselected address to paper tape, *b)* stopping automatically when it reads an end-of-buffer character, and *c)* performing simple character editing.

The interrupt service routine is called into operation when the following sequence of instructions is encountered in the main program:

```
                .
                .
                .
R0 = %0                                ;REGISTER ZERO
SP = %6                                ;REGISTER SIX
PC = %7                                ;REGISTER SEVEN
PS = 177776                            ;PROCESSOR STATUS WORD
CLR       PUNDON                       ;CLEAR SOFTWARE FLAG
MOV       #BUFFER, POINTER             ;SET UP BUFFER POINTER
MOV       #100, PPS                    ;SET PUNCH INTR ENB
                .
                .
                .
```

This instruction sequence sets up the system by initializing the service routine and enabling interrupts from the punch.

If the punch is idle, an interrupt occurs immediately; otherwise, the first interrupt is delayed until the current operation is completed. The software flag is used by the main program to provide a check on the progress of the output. This occurs in the following manner: The main program continues with other processing until the use of the punch is required, or further processing is dependent on completion of the output. At this point the sequence of instructions shown below is executed:

```
LOOP:     TST   PUNDON           ;CHECK SOFTWARE FLAG
          BPL   LOOP
```

If the interrupt service routine has not set the flag, the processor stays in this wait loop, allowing interrupts for further output operations, until the routine signals that it is finished.

In this example, the interrupt routine to service the punch requires the following sequence of instructions:

```
                                                .
                                                .
                                                .
74:     PCHINT                                  ;VECTOR TO ROUTINE
76:     200                                     ;NEW STATUS WORD SET TO PROCESSOR
                                                ;PRIORITY LEVEL 4
                                                .
PCHINT: MOV     R0      -(SP)                   ;SAVE REGISTER ZERO
        MOV     POINTER, R0                     ;SETUP REGISTER
        TST     PPS                             ;CHECK NO ERRORS
        BMI     ERROR                           ;IF ERROR, EXIT WITH LAST
                                                ;BUFFER POSITION IN R0
RETEST: CMPB    (R0),   #212                    ;LINE FEED?
        BNE     TEST2                           ;NO, CONTINUE
        INC     R0                              ;YES, IGNORE CHARACTER,
        BR      RETEST                          ;AND TEST NEXT CHAR.
TEST2:  CMPB    (R0),   #377                    ;RUBOUT?
        BNE     TEST3                           ;NO, CONTINUE
        INC     R0                              ;YES, IGNORE
        BR      RETEST
TEST3:  CMPB    (R0),   #214                    ;FORM FEED?
        BEQ     OUT                             ;YES, EXIT
        MOVB    (R0)+,  PPB                     ;NO, OUTPUT CHARACTER
        MOV     R0,     POINTER                 ;SAVE REGISTER
        MOV     (SP)+,  R0                      ;UNSTACK PREVIOUS CONTENTS
        RTI                                     ;NORMAL RETURN
OUT:    MOV     (SP)+,  R0                      ;RESTORE TO PREVIOUS STATUS
        COM     PUNDON                          ;SET SOFTWARE FLAG
        RTI
POINTER: 0
PUNDON: 0
```

3.6 RESTRUCTURING THE SYSTEM

When a PC11 device changes address, or multiple PC11 devices are included in a system, the system software must be changed to reflect the changes in the device. Similar changes are required whenever the interrupt vector address or the priority level of a PC11 device changes.

Many of the system's programs, provided for use with the PC11, address the device registers indirectly through pointer locations. These locations can be changed to represent the new values of the device register addresses. Where the program addresses the device registers directly (through symbolic names that have been assigned the values of the addresses), the program can be reassembled with new values assigned to the symbolic names.

When the interrupt vectors are changed, the new addresses can be easily patched into the program, because only four bytes are affected.

NOTE

Be certain not to assign the interrupt vectors to any locations that may be required for other devices.

Any changes in the bus priority level are reflected by changes in the processor priority level stored in the second word of the interrupt vector. Normally, this processor priority is the same as the bus priority assigned to the PC11. (Hardware changes involved in reconfiguring a PC11 System are described in Paragraph 2.3.)

CHAPTER 4
DETAILED DESCRIPTION

The PC11 Control logic can be divided into three functional sections: selection logic, interrupt logic, and data transfer logic. Each of these sections is covered separately in subsequent paragraphs. The purpose of each of these functional sections is as follows:

Selection Logic	Determines if the PC11 has been selected for use, which register is to participate in the data transfer, and whether an input or output transfer is to be performed.
Interrupt Logic	Permits the PC11 to gain bus control and perform a program interrupt. Priority level of bus request (BR) line may be changed by user. Consists of interrupt control logic and the interrupt enable bits in the reader and punch status registers.
Data Transfer Logic	Controls data transfer functions when data is sent to the punch or when data is transmitted from the reader.

Figure 4-1 is a detailed block diagram of the logic in the PC11 Control. The print set contains the circuit schematics for this logic.

Earlier versions of the PC11 Control consisted of three separate logic modules. This new version consists of a single quad-type module.

4.1 ADDRESS SELECTION

The address selection logic (drawing PC-4) decodes the address information from the bus and provides four select line and two gating signals that determine which register has been selected and whether it is to perform an input or output function. Jumpers are arranged on the logic so that the module responds only to standard device register addresses 777550, 777552, 777554, and 777556 (jumpers in bit positions 4 and 7). Although these addresses have been selected by DEC as the standard assignments for the PC11 Control, the user may change the jumpers to any address desired. However, any MainDEC program (or other software) that references the PC11 standard address assignments must be modified if other than the standard assignments are used.

The first five octal digits of the address (77755) indicate that the PC11 Control has been selected as the device to be used. The final octal digit, consisting of address lines A02, A01, and A00, determines which register has been selected and whether a word or byte operation is to be performed. The two mode control lines, C00 and C01, determine whether the selected register is to perform an input or output operation.

Address lines A02 and A01 are decoded to produce one of four select line signals (Table 4-1) which select the register to be used. The two mode control lines produce IN and OUT signals (Table 4-1) which determine whether the bus cycle is a DATI or DATO. Note that an IN gating signal is not produced for the punch buffer

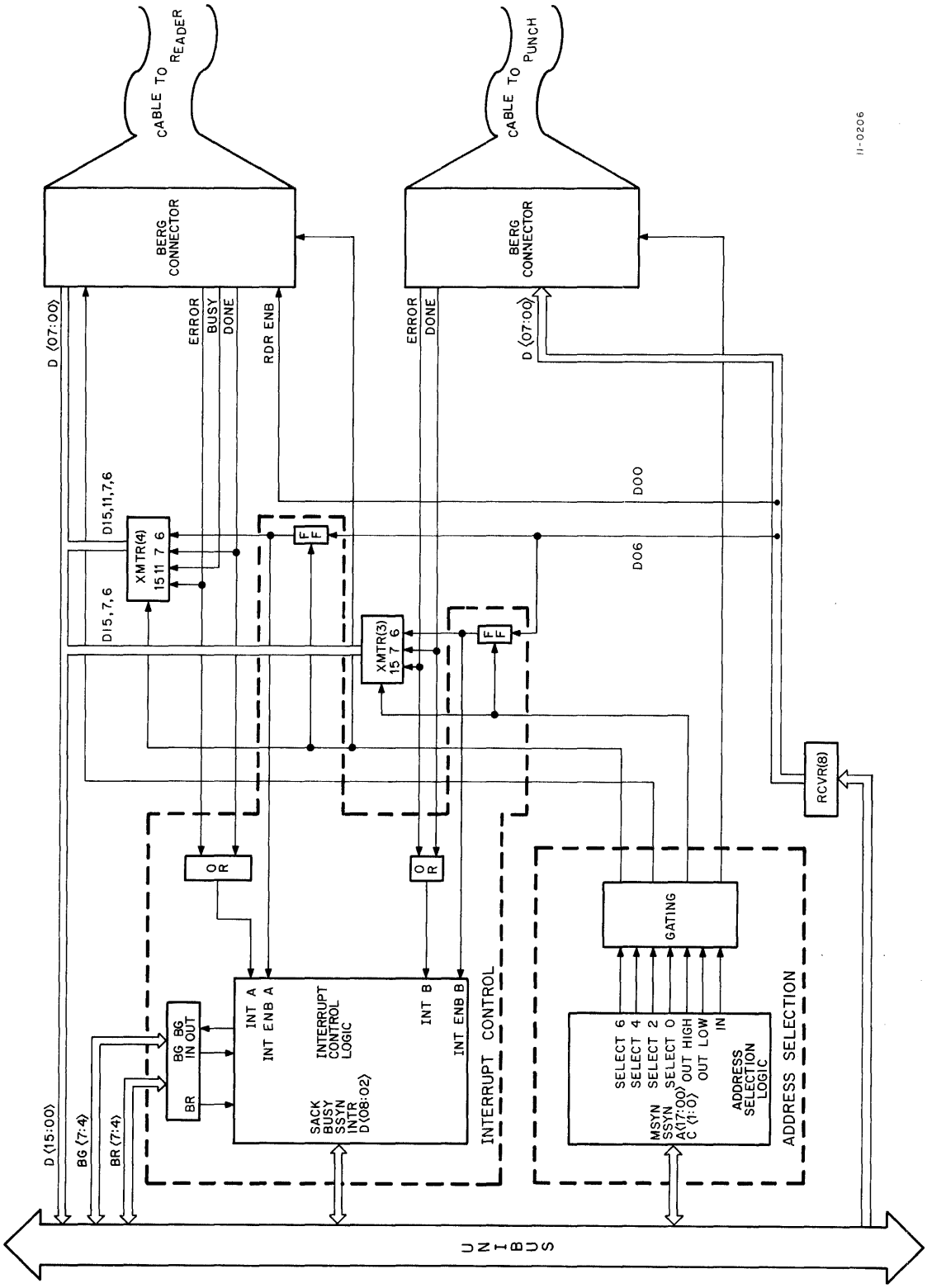

Figure 4-1 Detailed Block Diagram

because it cannot be read from the bus. An OUT gating signal is not produced for the reader buffer because it cannot be loaded from the bus.

Table 4-1
Data Transfer Functions for
Gating Signals

Gating Structure	Function
SELECT 0 · IN	Gates PRS to bus.
SELECT 0 · OUT LOW	Gates bus to PRS (loads RDR INT ENB and RDR ENB).
SELECT 2 · IN	Gates PRB to bus.
SELECT 4 · IN	Gates PPS to bus.
SELECT 4 · OUT LOW	Gates bus to PPS (loads PUN INT ENB).
SELECT 6 · OUT LOW	Gates bus to PPB (produces IOP4 that loads punch buffer).

4.1.1 Inputs

A simplified block diagram of the address selection logic is shown in Figure 4-2. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the PC11 Control is used, an OUT transfer is a transfer of data out of the master (the processor) and into the device. Likewise, an IN transfer is the operation of the controller furnishing data to the processor.

The address selection logic input signals consist of 18 address lines, A ⟨17:00⟩; 2 bus control lines, C ⟨1:0⟩; and a master synchronization (MSYN) line. The address selection logic decodes the incoming address as described below. This address format is shown in Figure 4-3. Note that all input gates are standard bus receivers.

a. Line A00 is used for byte control.

b. Lines A01 and A02 are decoded to select one of the four addressable device registers.

c. Decoding of lines A ⟨12:03⟩ is determined by jumpers. When a given line contains a jumper, the address logic searches for a 0 on that line; if there is no jumper, the logic searches for a 1.

NOTE
Connection of jumpers on the quad module is identical to the method used on earlier versions of this device which employed an M105 Address Selector Module.

d. Address lines A ⟨17:13⟩ must be all 1s. This specifies an address within the top 8K byte address bounds for device registers.

NOTE
Pin EA1 (EXT GND) must be grounded by the user to ensure proper operation of the address selection logic.

Tables 4-2 and 4-3 indicate the input signals that select the control output line states.

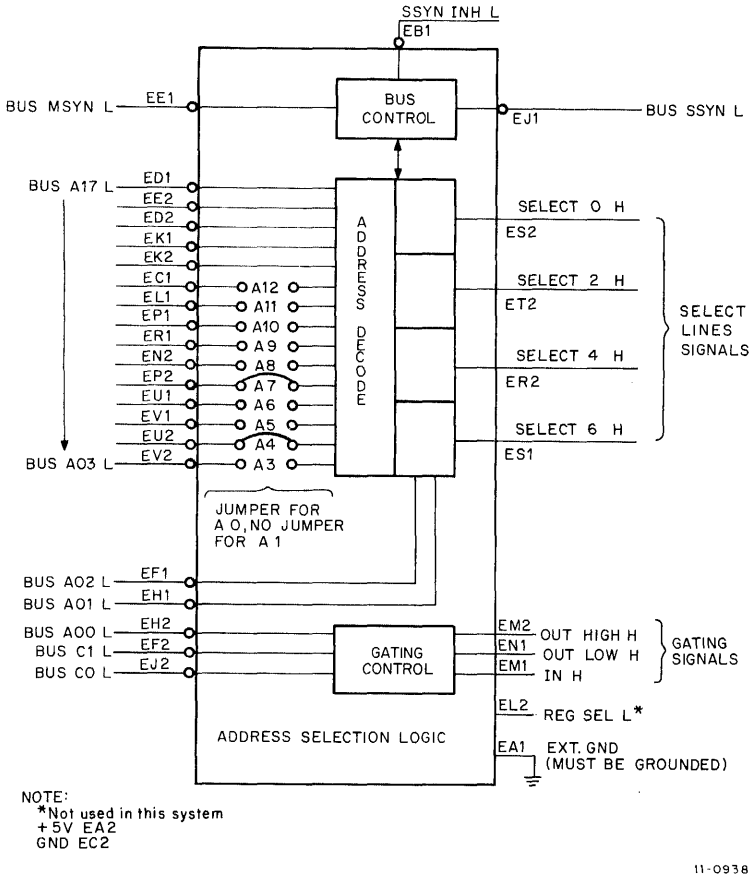

Figure 4-2 Address Selection Logic, Simplified Diagram

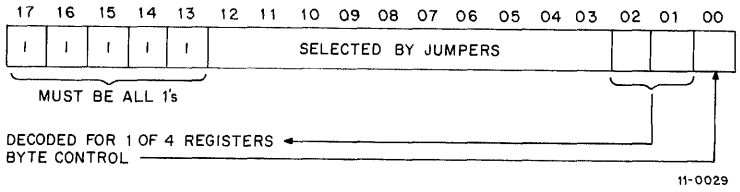

Figure 4-3 PC11 Control Select Address Format

Table 4-2
Select Lines

Input Lines A ⟨02:01⟩	Select Lines True (+3V)
00	0
01	2
10	4
11	6

NOTES
1. Lines A ⟨17:13⟩ must be all 1s (0V on Unibus).
2. Lines A ⟨12:03⟩ are selected by jumpers.

Table 4-3
Gating Control Signals

Mode Control C⟨1:0⟩	Byte Control A00	Gating Control Signals True (+3V)	Bus Sequence
00	0	IN	DATI
00	1	IN	DATI
01	0	IN	DATIP
01	1	IN	DATIP
10	0	OUT LOW OUT HIGH	DATO
10	1	OUT LOW OUT HIGH	DATO
11	0	OUT LOW	DATOB
11	1	OUT HIGH	DATOB

NOTE
Gating control signals may become true although select lines are not.

4.1.2 Slave Sync (SSYN)

Although the select line and gating signals normally determine the data transfer that is to take place, in some instances no action occurs other than the transmission of SSYN by the address selection logic. A DATO to the PRB register or a DATI to the PPB register has no effect on the logic and no data transfers take place between the PC11 Control and the Unibus. When SSYN INH is grounded, it inhibits the acknowledgment signal (SSYN) normally generated by the address selection logic.

4.2 INTERRUPT CONTROL

The interrupt control logic (drawing PC-4) permits the PC11 Control to gain control of the bus (become bus master) and perform an interrupt operation. The jumpers on this logic are arranged so that the logic has a normal vector address of 70 for the reader and 74 for the punch (jumpers in bit positions 3, 4, and 5). Although this is the recommended vector address, the user may change the jumpers to correspond to any address desired, but MainDEC programs and other software referencing the standard vector address assignments must be changed to reflect the new assignments.

NOTE
Connection of jumpers on the M7810 quad module is the *reverse* of the method used on M782 and M7820 Interrupt Control modules and the same as the M7821 module. On the quad module, a jumper represents a 1, no jumper represents a 0.

The interrupt control logic consists of a dual-input request and grant acknowledge circuit for establishing bus control. The "A" input is connected to the reader control logic and provides a vector address of 70; the "B" input is connected to the punch control logic and provides a vector address of 74.

Before the "A" input interrupt logic can generate an interrupt request, two input signals must be high: INT A and INT ENB A. The logic that generates these two signals is shown on drawing PC-3. When a 1 is loaded into bit 06 of the reader status register (PRS), it sets the INT ENB flip-flop to produce INT ENB A H. This signal is applied to the interrupt control logic as an enabling signal.

The second signal that must be present to generate an interrupt is INT A H. Whenever an ERROR condition (RDR OUTAPE H true) or DONE condition (I/O BUS INT L true) occurs in the reader, a series of gates is qualified to produce INT A H.

The "A" input section of the interrupt logic (Figure 4-4) is used to gain control of the bus. When both the INT A and INT ENB A requesting inputs are asserted, a bus request is made on the BR level corresponding to the level of the priority plug in the logic. The standard level for the PC11 Control is BR4 but this may be changed on the priority plug, if desired. When the priority arbitration logic in the processor recognizes the request and issues a bus grant signal, the master control circuit acknowledges with a SACK signal. When the PC11 Control has fulfilled all requirements to become bus master (BBSY false, SSYN false, and BG false) the master control section asserts BBSY.

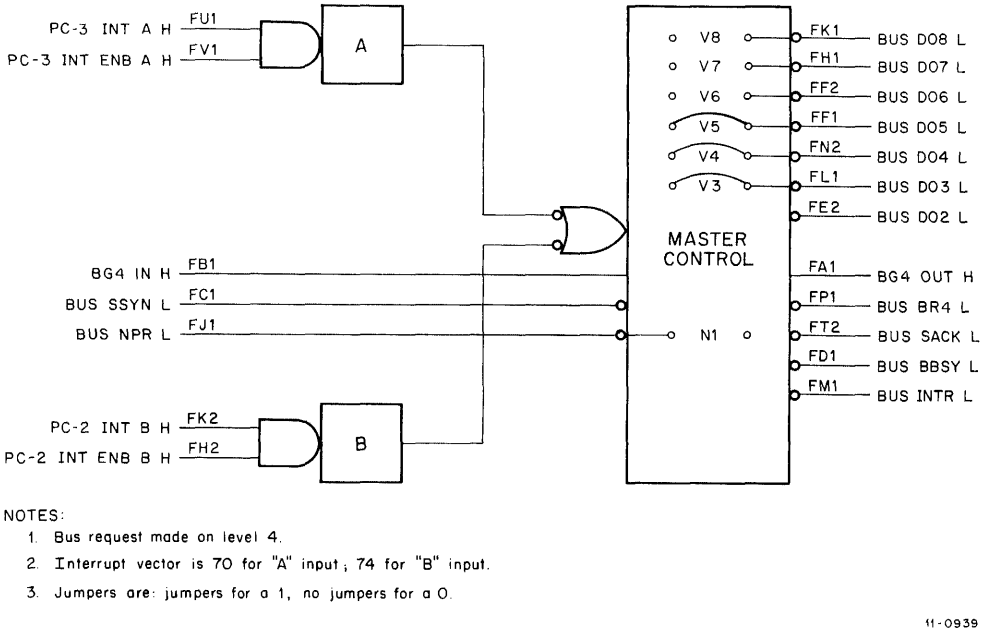

Figure 4-4 Interrupt Control Logic, Simplified Block Diagram

The "B" input interrupt logic operates in a similar manner to that of the "A" input logic. In this case, the two input signals that must be high are: INT B and INT ENB B. The logic for these two signals is shown on drawing PC-2. When a 1 is loaded into bit 06 of the punch status register (PPS), it sets the interrupt flip-flop to produce INT ENB B, which is applied to the interrupt logic as an enabling signal.

The second signal that must be present is INT B H. Whenever an ERROR condition (PUN OUTAPE L true) or READY condition (PUN ACTIVE L goes high) occurs in the punch, a series of gates is qualified to produce INT B H.

The "B" input interrupt logic functions in an identical manner to the "A" input logic except that it generates a different vector address. Although both the reader and the punch are at a BR4 level, the reader has a slightly higher priority.

Once the PC11 Control has gained bus control by means of a BR request, an interrupt is generated. The interrupt vector address is selected by jumpers on the logic as shown on Figure 4-4. Because the vector is a 2-word (4-byte) block, it is not necessary to assert the state of bits 0 and 1.

The six selectable (jumpered) lines determine the two most significant octal digits of the vector address. The least significant octal digit is controlled by bit 02, so that all vector addresses end in either 0 or 4. The input to bit 02 is tied to the V2 flip-flop logic. Whenever an interrupt occurs on the "A" input logic, bus line D02 is *not* asserted, and the interrupt causes a vector at location 070. When an interrupt occurs on the "B" input logic, bus line D02 is asserted, and the interrupt causes a vector at location 074. Note that the first two digits can be changed by jumpers but the last digit is always 0 or 4.

The BG IN signal is allowed to pass through the logic to BUS BG OUT when the controller is not issuing a request. To request bus use, the AND condition of INT and INT ENB must be satisfied. These levels must be true until the interrupt service routine clears INT or INT ENB. Once bus control has been attained, it is released when the processor has strobed in the interrupt vector. After releasing bus control, the logic inhibits further bus requests from that particular input ("A" or "B") even if INT and INT ENB remain asserted. In order to make another bus request, INT or INT ENB must be dropped and then reasserted to cause the logic to reassert the request line. This prevents multiple interrupts when the logic is used to generate interrupts. The interrupt control logic used in the PC11 Control is not capable of issuing NPR requests.

In order to improve NPR latency, the NPR line is sampled and prevents an interrupt request until all NPRs have been honored. The sampling of the NPR line is controlled by a jumper (N1) on the PC11 Control Module.

CAUTION

Only certain PDP-11 processors can work with the special circuit described above. The jumper (N1) on the module, when cut, prevents the special circuit from working.

4.3 OUTPUT LOGIC

The PC05 Reader/Punch contains internal data buffering and provides complete control of one timing cycle. The only output logic required of the PC11 Control is the gating logic between the Unibus and the punch and reader connectors. This gating logic controls when a byte of data is sent to the punch, when a start signal is sent to the punch, or when a start signal is sent to the reader.

4.4 INPUT LOGIC

The input logic is involved in transfers that transmit data to the Unibus. The M7810 module provides gating that controls the transmission of: *a)* a byte of data from the reader, or *b)* status information from one of two status and control registers onto the Unibus.

The M7810 module has one set of eight bus receivers that connect the inputs of the four device registers to Unibus lines D ⟨07:00⟩. Each register is gated separately. The PRS and PPS registers each include one flip-flop that can be loaded from line D06 to store the Interrupt Enable for the corresponding device. The PRS register also requires a gate to transmit RDR ENB from line D00 to the reader. All other bits of these registers are read-only and do not receive information from the bus.

The PRB register is also read-only and does not accept information from the bus. The PPB register, however, is write-only; information from the bus is gated to a buffer in the punch, along with a signal to start a punch operation.

Each register that can supply data to the Unibus has a separate transmission system. The PRS and PPS registers each have bus drivers that transmit the status bits for the two devices; only bit 0 of the PRS is not transmitted to the bus. The PRB register requires eight bus drivers to gate a byte of data from the buffer register in the reader to the bus. The PPB register does not transmit data to the bus.

CHAPTER 5
MAINTENANCE

This chapter covers the equipments and techniques necessary to maintain the PC11 High-Speed Paper-Tape Reader/Punch and Control. The *PC05 Maintenance Manual* and the *PC04/PC05 Paper-Tape Reader/Punch Manual* provide information on the maintenance of the PC05 Reader/Punch. This chapter also lists the equipments and programs useful in determining the operating status of the system and describes some basic techniques for isolating and repairing faults in the PC11 hardware.

5.1 TEST EQUIPMENT AND PROGRAMS

Table 5-1 lists a variety of tools useful in testing and repairing the PC11 Control. The PC11 Control consists of only one module; consequently, it is possible to correct faulty operation by swapping modules, and no tools are actually necessary to repair the control. Fault isolation and checking for marginal conditions is much easier in the PC11 because of this design.

Table 5-1
Test Equipment and Tools

Equipment	Item	Type
Test Equipment	Oscilloscope	Tektronix Model 453 (or equivalent)
	Volt-Ohmmeter	Triplett Model 630 (or equivalent)
Devices	Extender Board	Two W984A double-extender boards
		Four single-extender boards (a W984 board divided in half)
	Maintenance Module Set	One W130 One W131
	IC Test Clip	
	Pin probe tip	Two Tektronix #30
	Pointed-tip solder iron	Rated at less than 40W
	Package of solder wick	Used for removal of solder on printed circuit boards.
Tools	Screw drivers Allen wrench set Needle-nose pliers Wire strippers	
	Paper-Tape Gauge	DEC Part No. 18-09211

The maintenance philosophy for the PC11 Reader/Punch and Control is based on system checkout using test programs. The diagnostic program, supplied by DEC, can be used to verify correct operation of the equipment or to indicate possible sources of malfunction. This maintenance program is as follows:

MainDEC-11-D2BB-D	PC11 High-Speed Reader and Punch Test Listing
MainDEC-11-D2BB-PB	PC11 High-Speed Reader and Punch Test Program

5.2 PREVENTIVE MAINTENANCE

Improper operation of the PC11 Reader/Punch can be caused by a dirty reader or by an unlubricated punch. The reader photocells should be examined for dirt each time a tape is loaded into the reader and should be cleaned with a nonabrasive cleaning agent at regular intervals. The paper-tape punch should be lubricated regularly, and the paper-tape output should be compared to the standard (as represented by the paper-tape gauge, Part Number 18-09211, available from DEC) for hole spacing. Make certain that the holes are properly shaped; poorly shaped holes may indicate a worn punch block that needs replacement.

In addition to these maintenance procedures, the system should be fully checked at regular intervals by running the MainDEC programs to verify correct operation and to identify marginal conditions. Many apparent operating errors are caused by incorrect or improperly operating programs; these errors can be identified by using the diagnostic programs to determine that the errors are not caused by the hardware.

5.3 CORRECTIVE MAINTENANCE

When it has been verified that the PC11 Reader/Punch and Control is not operating correctly, the fault must be isolated and corrected. Often the nature of the errors encountered when running the diagnostic programs indicate the type of fault, or the possible locations of faulty components. However, further testing may be required to determine the exact problem.

APPENDIX A
SIGNAL CORRELATIONS

The following tables provide signal correlations between the PC11 and PC05 devices.

Table A-1
Reader Data Signals

Comment	PC05	PC11	Unibus
Least significant bit (LSB), nearest back of reader	RD1	I/O BUS IN 11	BUS D00
	RD2	I/O BUS IN 10	BUS D01
	RD3	I/O BUS IN 09	BUS D02
	RD4	I/O BUS IN 08	BUS D03
	RD5	I/O BUS IN 07	BUS D04
	RD6	I/O BUS IN 06	BUS D05
	RD7	I/O BUS IN 05	BUS D06
Most significant bit (MSB), at front of reader	RD8	I/O BUS IN 04	BUS D07

Table A-2
Punch Data Signals

Comment	Unibus	PC11	PC05	Punch
LSB, right-side of reader; tape is upside down	BUS D00	BD00	(AC11 (1))	PB 7
	BUS D01	BD01	(AC10 (1))	PB 6
	BUS D02	BD02	(AC09 (1))	PB 5
	BUS D03	BD03	(AC08 (1))	PB 4
	BUS D04	BD04	(AC07 (1))	PB 3
	BUS D05	BD05	(AC06 (1))	PB 2
	BUS D06	BD06	(AC05 (1))	PB 1
MSB, left-side of reader	BUS D07	BD07	(AC04 (1))	PB 0

Table A-3
Reader Control Signals

PC05 Name	PC11 Name	Function
IOP 1 (1)	Not used	Not used
IOP 2 (1)	SELECT 2 * IN	PRB selected
IOP 4 (1)	SELECT 0 * OUT LOW * BD 00	Read command
I/O BUS SKIP	Not used	Not used
I/O BUS INT	RDR DONE	Done
RDR RUN (0)	RDR BUSY	Busy
RDR OUTAPE	RDR ERR	Error
QUALIFY		Always set
RDR INITIALIZE	BINIT	Initialization

Table A-4
Punch Control Signals

PC05 Name	PC11 Name	Function
IOP 1 (1)	Not used	Not used
IOP 2 (1)	Not used	Not used
IOP 4 (1)	SELECT 6 * OUT	PPB selected
PUN ACTIVE	PUN READY	BUS D07 (done)
PUN OUTAPE	PUN ERROR	BUS D15 (error)
PUN QUALIFY		Always set
I/O BUS SKIP	Not used	Not used
I/O BUS INTR	Not used	Not used
PUN INITIALIZE	BINIT	Initialization

APPENDIX B
ENGINEERING DRAWINGS

ENGINEERING DRAWINGS

A complete set of engineering drawings and module circuit schematics is provided with each PC11 System in a companion volume entitled, *PC11 High-Speed Paper-Tape Reader/Punch, Engineering Drawings.* Each manual in the basic PDP-11 series also has a companion volume containing a complete set of reduced engineering drawings of the component described in the manual. The general logic symbols used on these drawings are described in the *DEC Logic Handbook,* 1971. Specific symbols as well as special ICs and circuits are discussed in the *KA11 Processor Manual,* EK-KA11-TM-002.

Reader's Comments

PDP-11 PC11 HIGH-SPEED
READER/PUNCH AND CONTROL
EK-PC11-TM-003

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