Roy Hugenberger
13 February 1979

IMP11-B ARPANET INTERFACE

GENERAL DESCRIPTION:

The IMP11-B is a microprocessor controlled interface which
provides a full duplex serial connection between a PDP11 Computer
System and the Interface Message Processor (IMP) of the Advanced
Research Project Agency Network (ARPANET). The IMP is the
communications processor that interfaces the Host Computer to the
ARPANET. The IMP11-B ARPANET INTERFACE allows the PDP11 user,
with the addition of appropriate software, to communicate with
other Host machines on the ARPANET. The IMP11-B will support
both the local ($\leq$ 30 ft.) distant ($\leq$ 2000 ft.) host operation of
ARPANET IMP interface.

FEATURES:

* Compact design - 2-Hex size SPC modules plus a rack mounted
  indicator and cable connection panel.

* Microprocessor based (KMC11).

* Full duplex operation.

* 16 bit UNIBUS NPR transfers.

* Indicator Panel.

* Switch selectable for either the IMP's local or distant
  interface.

* Static and dynamic diagnostic software and ARPANET test
  program.

OPERATION:

The IMP11-B logic consists of two modules, a KMC11-A
microprocessor module and a line termination module. To
initialize the IMP11-B, the PDP11 operating software loads the
Digital supplied firmware code into the KMC11. Once this
firmware is loaded and started, the IMP11-B is operational.

A user program issues a command to the IMP11-B by loading the
command in the pertinent KMC11 Control and Status registers
(CSR's). The firmware in the KMC11 then interprets the command
and performs the specified action. Similarly, the IMP11-B issues
a status to the user program by setting the status bits in the
pertinent CSR's and interrupting the user program.

Message data buffers which the KMC11 fetches are setup thru the
use of input and output buffer descriptor lists residing in PDP11
memory. The IMP11-B then proceeds to fill or empty the data
buffers with data.

The IMP11-B transmits and receives full duplex serial data from
the IMP processor according to the "Report Number 1822" Four Way
Handshake. Serial bit data is assembled into 8 bit bytes in the
line termination module, and bytes are packed into 16 bit words
for transfer to and from PDP11 memory. An important feature is
the IMP11-B's ability to handle non-octet sized data buffers, and
then passed as a 16 bit word from the KMC11 to the PDP11.

SPECIFICATIONS:

Mechanical:

Logic Mounting Space: 2 adjacent Hex SPC slots in a
                             DD11-B,C,or D. When mounting in a
                             DD11-B or C, the Line Unit module
                             can reside in slot 1,2,3,or 4. The
                             KMC11 module must be mounted in slots 2
                             or 3 only.

Panel Mounting Space: Cabinet Space 5 1/4" high x 19" wide.
                             Cable access clearance must be made
                             available to the rear of the panel.

Electrical:

Input Power: +5 VDC @ 6 Amps
(Both Modules)   -15 VDC @ .2 Amp
                             +15 VCD @ .1 Amp

Cabling: A 10 foot cable between logic and the
                             indicator/cable termination panel is
                             supplied as well as all internal
                             cables. The local and distance IMP
                             Host Cable connectors for the IMP11-B
                             cable end are supplied. The Customer
                             shall provide connectors for the
                             Arpanet IMP side and assemble the
                             desired length cable.

Environmental:

Operating Temperature: +10 to 40 degrees celsius

Humidity: 10 to 90%

Operational:

Transfer Mode: Full duplex NPR (DMA)

Unibus Load: 1 Bus load

Signaling: Bit asynchronous complies with
                                specification in the Bolt, Beranek, and
                                Newman "Report Number 1822", Four Way
                                Handshake, local or distant interface.

Data Rate: 330K bits/sec nominal, full duplex with
                                25 foot cable. Rate decreases as longer
                                cable distance between IMP11-B and IMP
                                are implemented.

WHO CAN JOIN ARPANET?

ARPANET is a network of computer systems administered by the Advanced Researc
Government Department of Defense.

U.S. government agencies may request membership in ARPANET by
applying to: Director, Defense Communications Agency, 8th and S.
Courthouse road, Arlington, VA 22204. Non-US government
activites may also apply provided they are sponsored by a U.S.
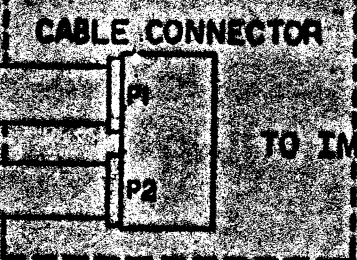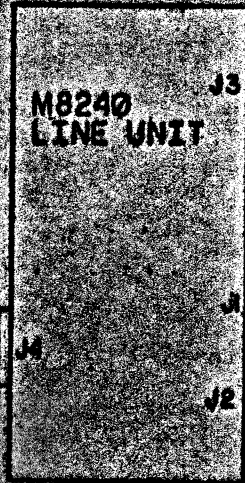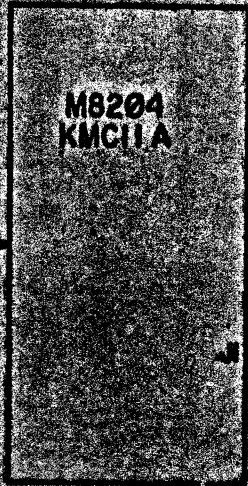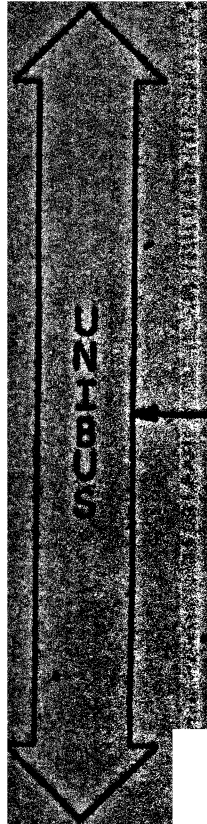government activity.

INFORMATION AVAILABILITY:

Further information may be obtained from your nearest Digital
Sales Office.

/sk
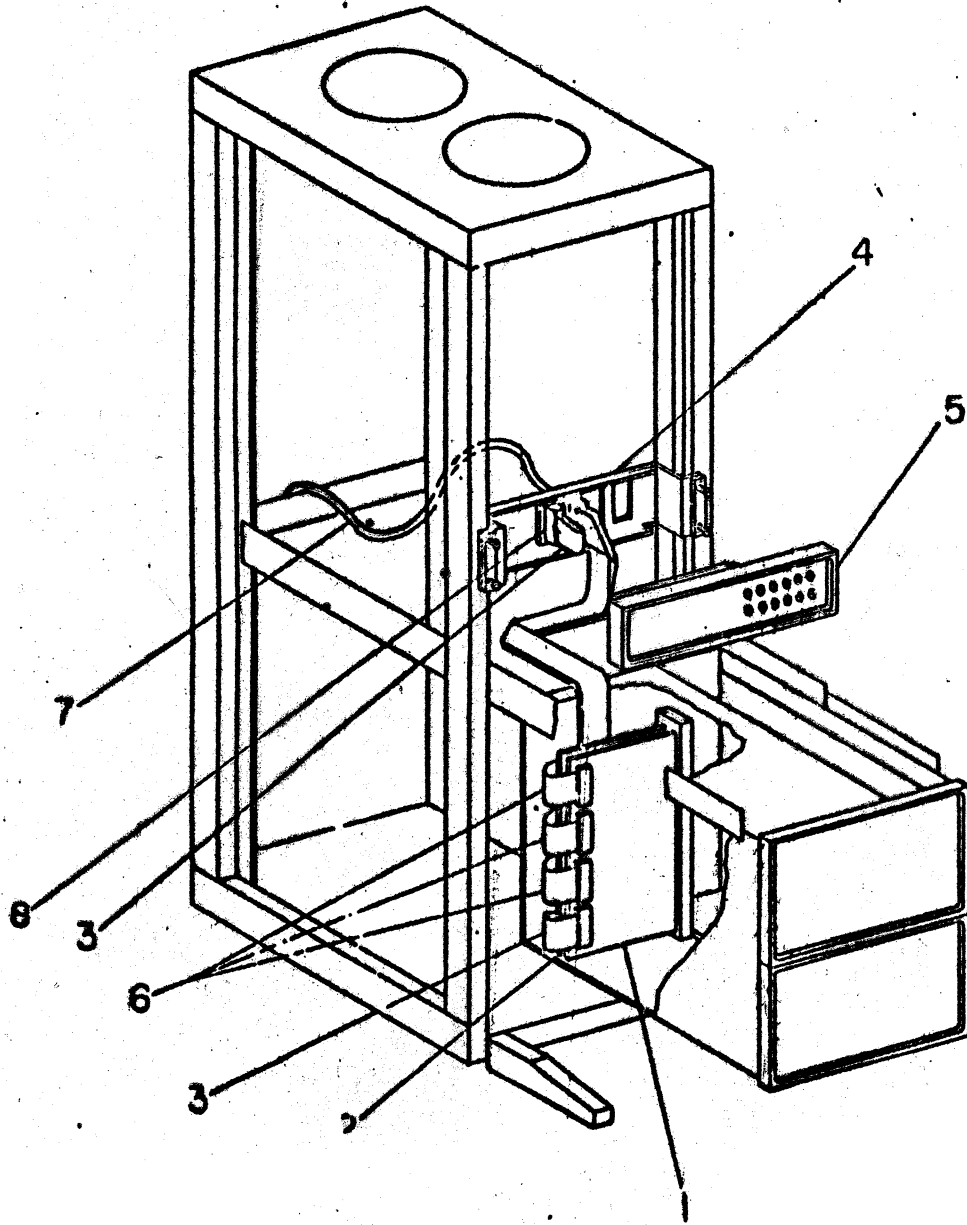
DESCRIPTION	PART NO. REF.
1. M8204 μP	M8204
2. M8240 LINE UNIT	M8240
3. BC08R CABLE	BC08R-01
4. PANEL	7412379-00
5. PANEL BEZEL	2ME111A
6. DISTRIBUTION CABLE	BC06R-10
7. DEVICE CABLE (CUSTOMER SUPPLIED)	
8. MAINTENANCE PLUG	2ME067A

UNIBUS

M8204
KMC11 A

J4 BC08R J4

M8240
LINE UNIT

J3 BC06R INDICATOR PANEL J1

J1 BC06R P1 CABLE CONNECTOR

J2 BC06R P2 TO IMP CABLE

INDICATOR CABLE
PANEL ASSEMBLY

DWG DAD YYE757-0-0

SS PART 2ME067A

1

P1

2

3

TO P1

P2

2

2
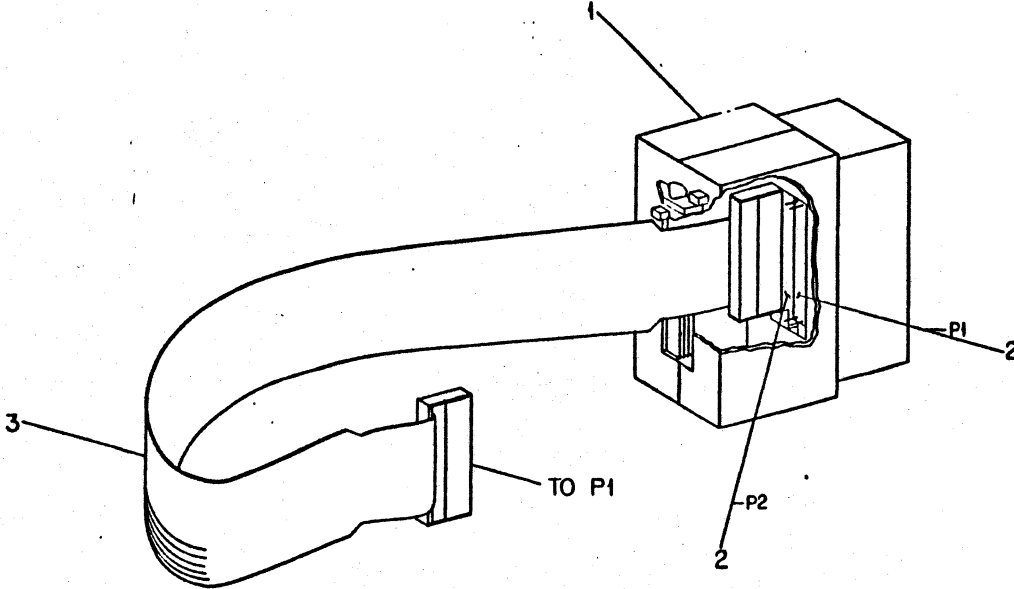
1	CABLE, BC 85 I/O	BC085-01	3
2	PLUG TERMINATOR	1211591-21	2
1	PLUG KIT, FLAT CABLE	1211591-40	1
	DESCRIPTION	DWG PART NO	ITEM NO

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

FIRST USED ON

TITLE

MAINTENANCE PLUG

digital

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL

QUANTITY & VARIATION

SIZE CODE   NUMBER   REV.
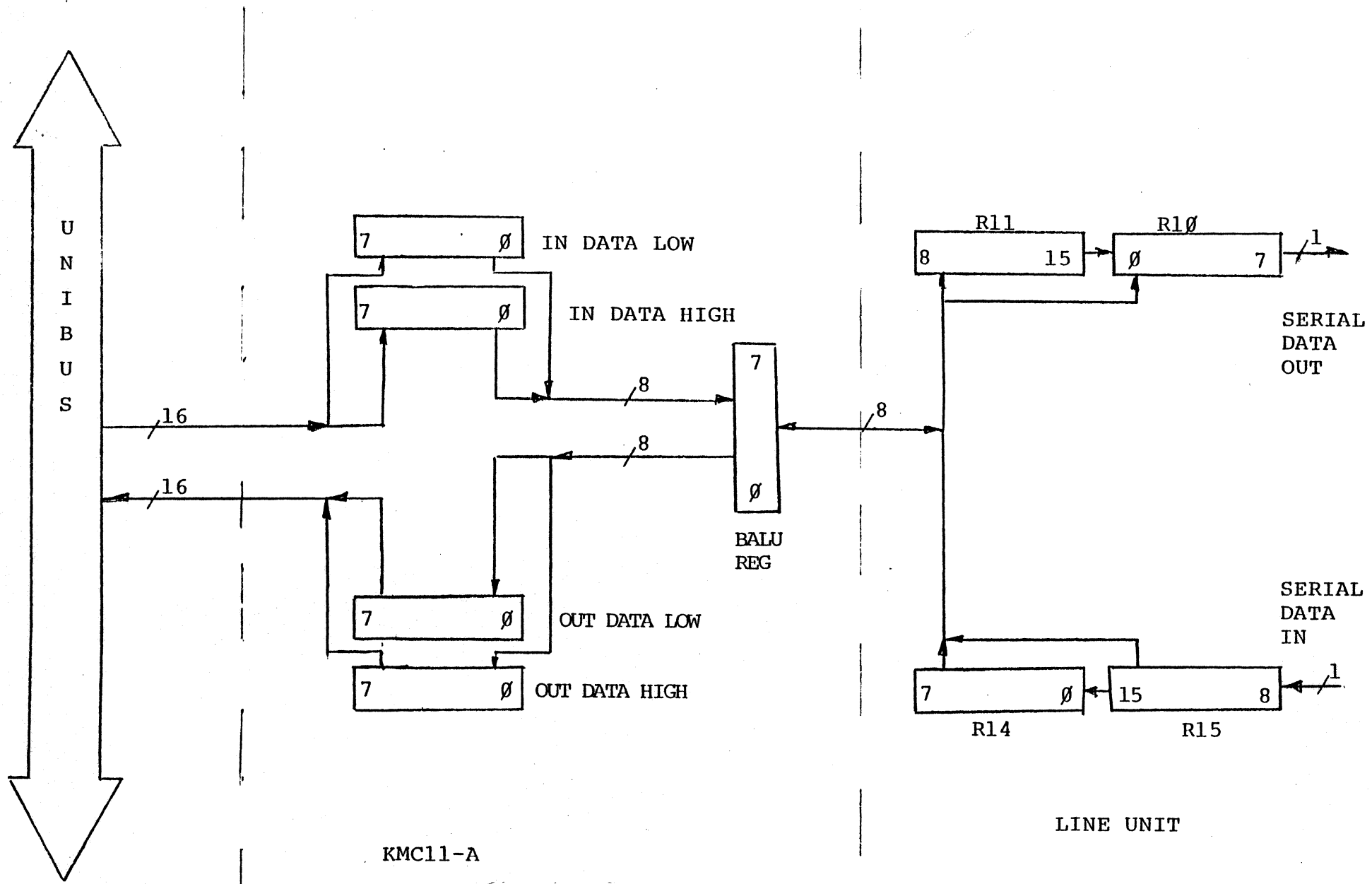
IMP DATA FORMAT

1	(1 - 32)	32

IMP11-B BYTES (8 BITS)

7	Ø	15	8	7	Ø	15	8
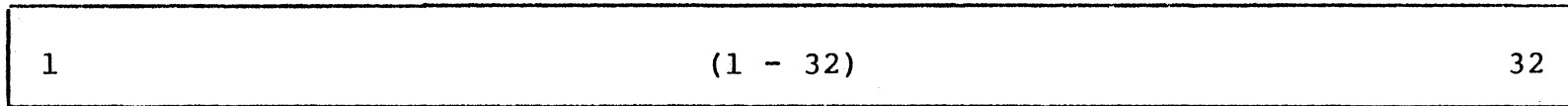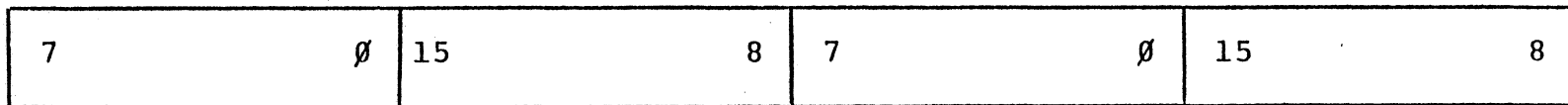
BYTE 1	BYTE 2	BYTE 3	BYTE 4
PDP11 WORD 1		PDP11 WORD 2	

STARTING BIT   LAST BIT

IMP11-B/IMP DATA BIT MAP

7	6	5	4	3	2	1	0	
TX BUF 0								R10
TX BUF 1								R11
			ENA LAST BIT			TX ERR CLR	TX CLR STATUS	R12
								R13
								R14
								R15
						HOST RDY.	RX CLR STATUS	R16
							GET IMP WORD	R17

LINE UNIT DATA IN REGISTER

7	6	5	4	3	2	1	0	
								R10
								R11
			ENA LAST BIT			TX ERR CLR	TX CLR STATUS	R12
			IMP NOT RDY			RFN IMP11 BIT	BUFFER EMPTY	R13
RX BUF 0								R14
RX BUF 1								R15
						HOST RDY.	RX CLR STATUS	R16
			IMP LINE ERROR			END OF MSG.	DATA AVAIL.	R17

BDL #1   PDP 11 MEMORY

BUFFER ADR #1	
(BF1) EXT ADR 17,16	
WC1	
∅	STATUS
BUFFER ADR #2	
(BF2) EXT ADR 17,16	
WC2	
∅	STATUS
TERM -1 (odd Adr)	

} BUFFER 1

} BUFFER 2

BDL
TERMINATION
WD

∅

BD1 ADR:	BDL #1
BD2 ADR:	BDL #2

BF1:
BUFFER #1
WC1

BF2:
BUFFER #2
WC2

MAINT	UP INPUT CONTL	SEL 0
	UP OUTPUT CONTL	SEL 2
		SEL 4
		SEL 6
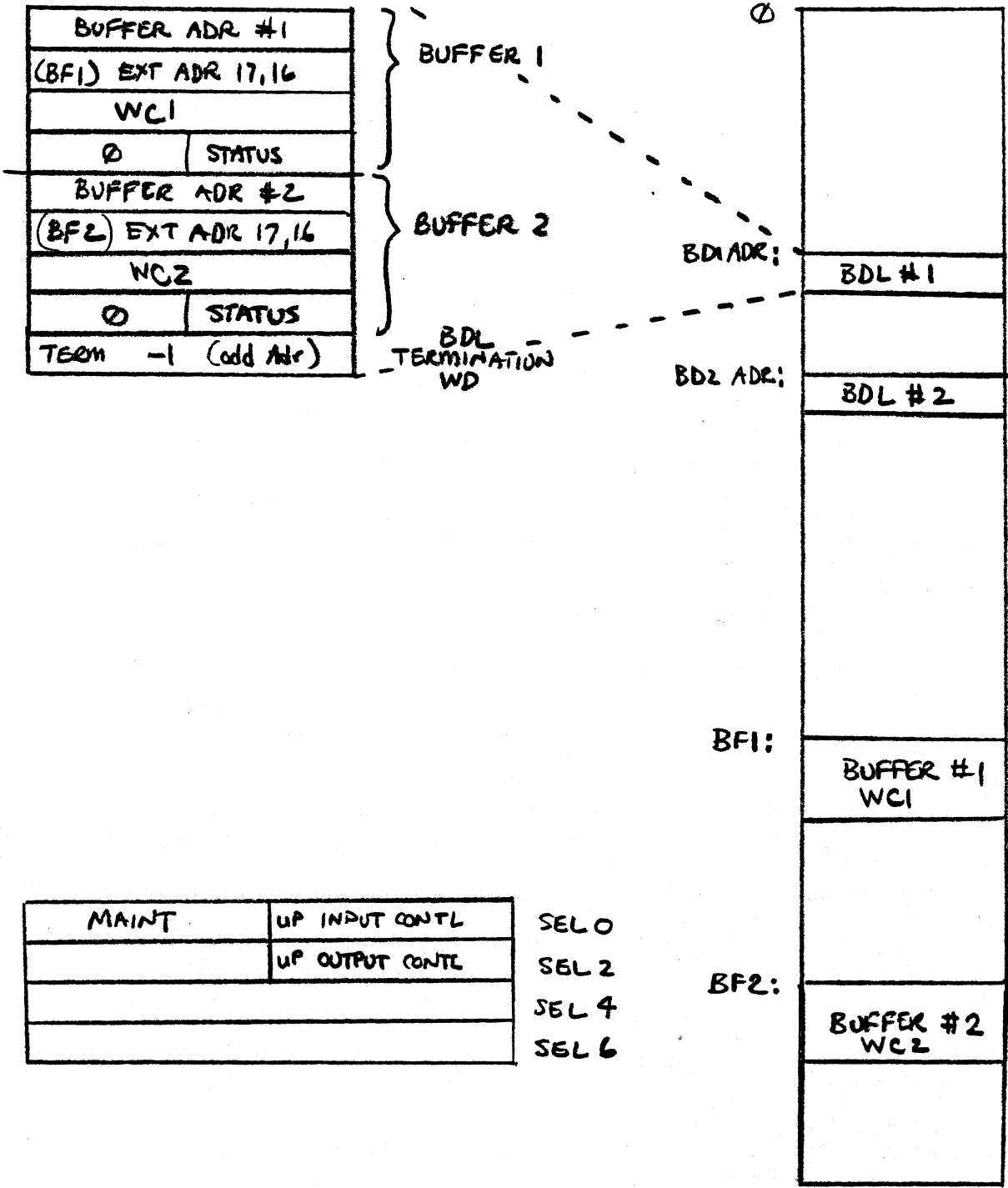
BDL (BUFFER DESCRIPTOR LIST)
OVERVIEW

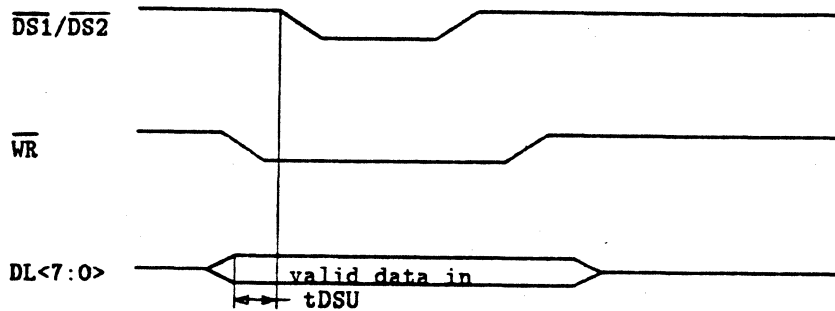Product: DC349-AA   Number: 4   Date: 04-OCT-1984

Author: Dave Stanley

Description: This bulletin pertains only to designs incorporating the Data Set Change Register. Disregard if not using the Data Set Change Register.

1. Change in AC Specification Section

Set-up of valid DL<7:0> to the falling (leading) edge of DS1 and DS2.

tDSU (min)   = 0ns

All other AC parameters remain unaffected.

2. Addition to Data Set Change Summary Register description

   To insure proper operation of the Data Set Change Summary Register, it is specified in the data sheet that programs should read and save a copy of its contents. The copy should then be written back to clear the bits that were set. What the data sheet does not specify is that the write-back should follow the read without intervening reads or writes to other registers in the chip. It is recommended that system interrupts be disabled before reading and writing the Data Set Change Summary Register so that the write-back can be guaranteed to follow the read without being interrupted.

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IMP11-B

PDP11 ARPANET INTERFACE

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Computer Special Systems

NOTEBOOK SECTION

OPTION NUMBER

2M-C078A-00

DRAWING SET NUMBER

PROGRAM NUMBER

YM-Z078A   STATIC
YM-Z078B   DYNAMIC

DOCUMENT NUMBER   REVISION

YM-C078C-00

DATE

SEPTEMBER 1978

IMP11-B

PDP11 ARPANET INTERFACE

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Computer Special Systems

NASHUA

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1   GENERAL DESCRIPTION

The IMP11-B Interface, a second generation IMP11-A interface, provides a direct serial connection between a PDP11 computer system and the Interface Message Processor (IMP) used to connect Host computers to the Advanced Research Projects Agency (ARPA) network. This UNIBUS option allows the user (with addition of appropriate software) to communicate via the ARPA network with other Host systems. The option has provisions for connecting to the IMP's Local or Distant Host Interface.

The IMP11-B is a microprocessor (KMC11-A) based serial line unit interface comprised of two hex modules (M8204 and M8240). The two modules can be mounted in any two adjacent hex SPC slots (example: middle two slots in a four slot DD11-B) and are connected by a short flat cable. The M8240 is a line termination unit module which contains the driver/receivers and shift registers that connect to the IMP Host Interface. The M8204 is a KMC11-A microprocessor which controls the M8240 and UNIBUS DMA transfers. See Figure 1-1.
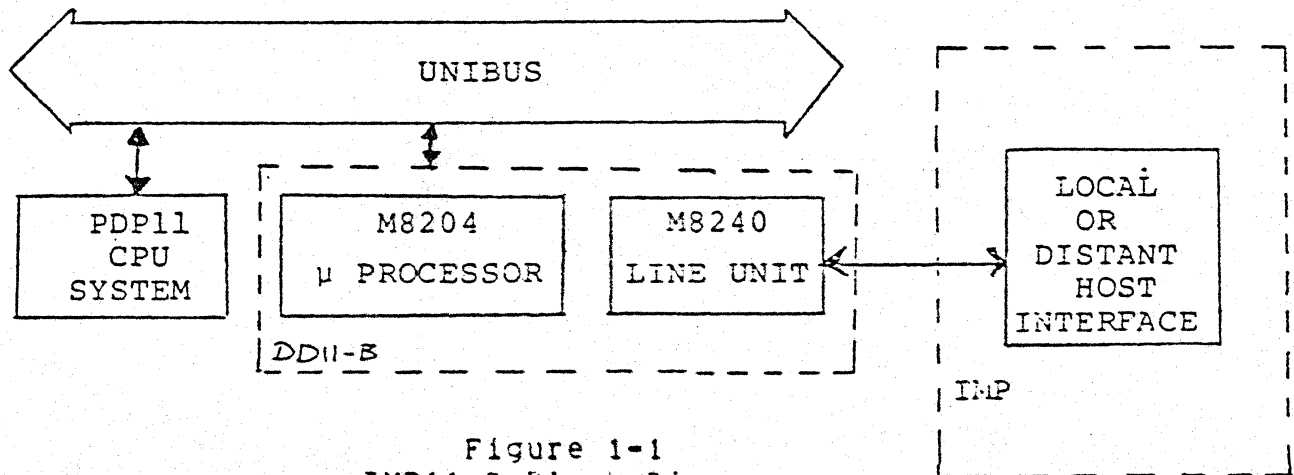
Figure 1-1
IMP11-B Block Diagram

1.2 OPERATION

The IMP11-B is controlled by a KMC11-A microprocessor. To initialize the unit, the PDP11 operating software must load the KMC11-A with a set of supplied firmware (microcode). Once this firmware is loaded and started, the KMC11-A/M8240 line unit is operational.

The KMC11-A microprocessor executes from a 1K writeable control store (firmware store) and 1K byte data store. It controls both full duplex DMA UNIBUS transfers and a full duplex 8 bit data port to the M8240 line unit. The KMC11-A moves data between the M8240 line unit and PDP11 memory according to the word count (14 bits) and bus address (18 bits - 128K range) set up by the 4 user accessible KMC11-A UNIBUS registers. Error handling and command information is also passed thru these registers. DMA block transfers can be 16K (16 bit words) long, however, it is recommended that block transfers be limited to the maximum IMP message length (8096 bits). These blocks may be chained; up to 8 transmit and 8 receive buffer addresses may be stored by the KMC11-A.

The M8240 line unit drives and receives full duplex data from the Host Interface. Data is received serially from the IMP processor according to the 1822 Report Four Way Handshake and assembled into a 16 bit register. The 16 bit data word is presented to the KMC11-A data port as two eight bit bytes. Line status from the Host Interface is also passed to the KMC11-A via this data port. Data transmitted to the Host Interface is passed as two eight bit bytes to the M8240. The two bytes are serialized one at a time and transmitted to the Host Interface according to the 1822 Report Defined Four Way Handshake.

1.3 SPECIFICATIONS*

a. Mechanical

Mounting Space Prerequisite	Two adjacent hex SPC slots in an H960-DH expander box or BA11-K box
Dimensions M8204	8.5 x 17.0 inches (HEX)
M8240	8.5 x 17.0 inches (HEX)
Weight	10 lbs. (Approx.)

b. Electrical

Input Power	+5VDC±5%	4.0 Amp
	-15VDC±5%	0.1 Amp
	+15VDC±5%	0.1 Amp

* Specifications are subject to change without notice.

                    M8240   +5VDC5%   4.0 Amp
                             -15VDC5%   0.1 Amp
                             +15VDC±5%   0.1 Amp

Power supplied by regulated system unit power supplies.

Logic   TTL levels, ±6VDC levels

c. Operational

      Transfer Mode   Full Duplex, NPR (DMA)

      UNIBUS Load   One (KMC11-A-ONE, M8240-None)

      Data Rate**   360,000 bits/sec nominal, full
                           duplex (Dependent on IMP Host
                           Interface)

      Signaling   Bit asynchronous - 1822
                           Report Four Way Handshake

      Cabling   Cable terminator supplied Customer
                           must supply - IMP Host Cable.

1.4   PHYSICAL DESCRIPTION

The IMP-B hardware as supplied consists of the following:

        1.   M8204 (KMC11-A microprocessor)

        2.   M8240 (IMP Line Terminator Unit)

        3.   BC08R-01 (M8204 to M8240 Cable)

        4.   Inticator/Connector Cable

        5.   IMP - Host Cable Terminator

        6.   Interconnect Cable (M8240 to panel Cable)

The IMP11-B software as supplied will consists of the following:

        1.   M8204 Firmware

        2.   IMP11-B Diagnostic

        3.   IMP11-B (Host to IMP) Test Software

**Data rate is based on local interface (25 foot cable). Data
rates will decrease over longer cables when using distant
interface because of cable delays.

CHAPTER 2

INSTALLATION

2.1 SITE CONSIDERATIONS

The IMP11-B consists of two hex height modules, an indicator/cable panel, and four interconnecting cables. The PDP11 system must supply the following:

1. Mounting space for two hex height modules with UNIBUS access for the KMC11-A module.

2. Mounting space for a 5 1/4 inch by 19 inch panel. Provision must be made to allow access to the rear of the panel for cable insertion.

3. Power for the modules.

4. Adequate cooling for the modules.

5. NDR jumper must be removed from the slot that the KMC11-A resides. (Remove CA1 to CB1)

6. Adequate Bus loading.

2.1.1 Module Mounting Space

The two modules KMC11-A (M8204) and the Line Unit (M8240) module may be mounted in a DD11-B system unit or DD11-DF system unit. The KMC11-A must be mounted in one of the hex SPC (small peripheral control) mounting slots. The Line Unit module should be mounted in the next adjacent slot.

2.1.2 Panel Module Space

The indicator/cable panel is a 5 1/4 by 19 inch unit and can be mounted to the rails of the standard H960 cabinet. It should be mounted in the same cabinet as the hex modules and close enough to them so that the 8 foot BC06R-08 cables can connect the panel to the Line Unit module (M8240). Also, keep in mind that the indicators should be easily viewed by the operator. Adequate space should be provided behind the panel to allow the connect of the Line Unit cables and the IMP cable.

2.1.3 Power For The Modules (See Section 1.3)

KMC11-A

The KMC11-A (M8204) derives its power from the SPC slot (+5, -15, and ground).

LINE UNIT

The Line Unit (M8204) derives its power from the SPC slot (DD11-B, DD11-DF, or equivalent). It requires +5V, -15, and ground. The +5V is taken from pin A2 of each slot (A, B, C, D, E, F) and the ground is brought on to the module from pin C2 of each slot (A, B, C, D, E, F). The -15V is brought in only on pin B2 in slot C. If there is no -15V on pin CB2, then -15V must be jumpered to this pin. Generally pin CB2 is reserved for -15V. The -15V is used to provide power to the Line Unit's distant logic.

NOTE

Make sure that CB2 is not used before jumping -15V to it.
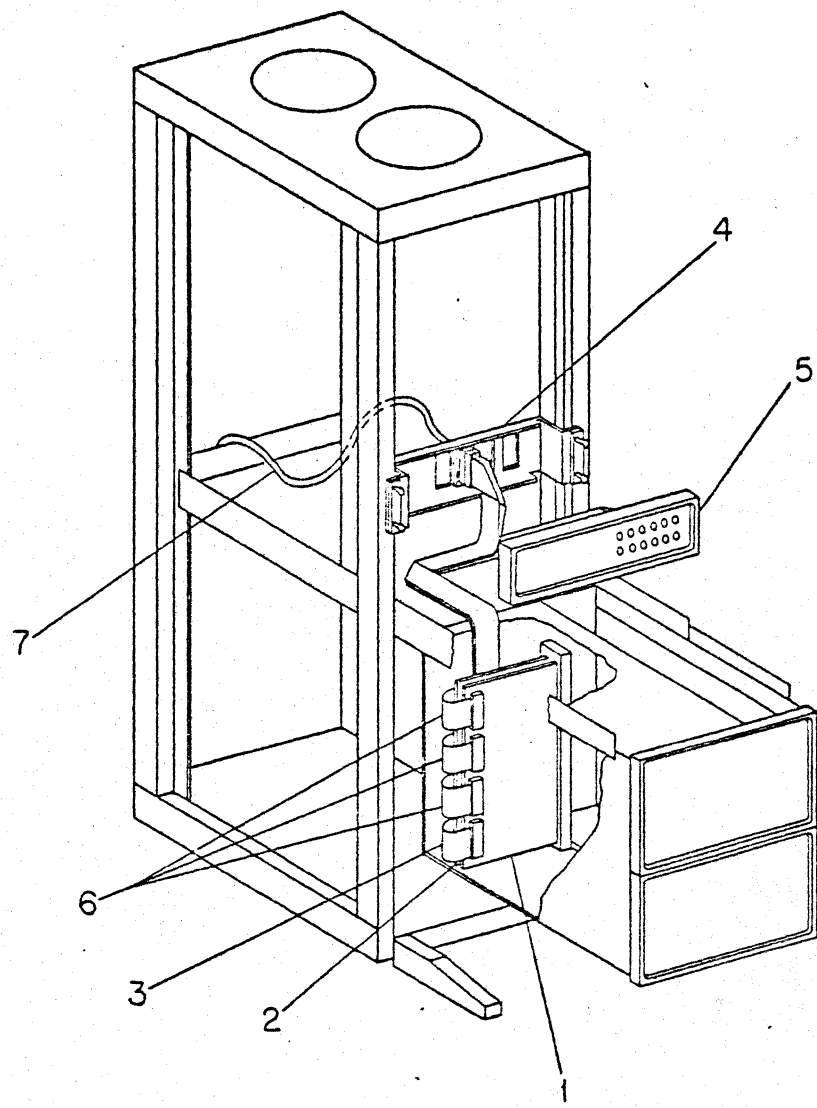
1. M8204 uP
2. M8240 LINE UNIT
3. BCO8R CABLE
4. PANEL
5. PANEL BEZEL
6. DIST CABLE
7. DEVICE CABLE (TERM. SUP. ONLY)

Figure 2-1

2.1.4 Adequate Cooling

Generally adequate cooling is provided in a PDP11 CPU box or in
an expander box. Ensure that there is nothing blocking the flow
of air across the two modules. Consult you PDP11 installation
manual.

2.1.5 NPR Jumpter

The NPR Non Processor Request jumper (CA1 to CB1) must be removed
when the KMC11-A is installed.   The KMC11-A has logic that
arbitrates the NPR's on the UNIBUS.

2.1.6 Adequate Bus Loading

There must be room to add two UNIBUS loads onto the UNIBUS.

2.2   INTERCONNECTIONS

2.2.1 M8204 To M8240

The KMC11-A (M8204) is connected to the Line Unit (M8240) with a
1 foot BC08S-01, 40 pin flat cable. J4 of the M8240, located
next to the handle approximately 3 1/2 inches from the bottom of
the module, is connected to J1 of the M8204 module, which has the
same placement. The BC08S-01 should be folded over from one
module to the other. See Figure 2-2. This cable is used to line
the KMC11-A to the Line Unit.
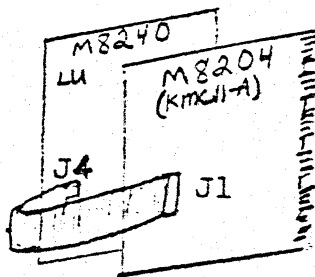
Figure 2-2

2.2.2   M8240 To Indicator/cable Panel

There are three cables used to connect the M8240 Line Unit module
to the indicator/cable panel. Two of the cables, BC06R-08's, are
used to connect the IMP output connector to the driver/receivers
on the M8240 Line Unit Module. The third flat cable is used to
connect the M8240 indicator drivers to the indicator panel. This
cable also supplies the power to the panel.

2.2.3   Initial Power Up Check

Make sure there are no direct shorts of the power pins to ground.
If there are, remove the modules M8204 and isolate and remove the
shorting condition.

2.2.4   IMP To IMP11-B Connection

The IMP (Information Message Processor) is connected to the
IMP11-B's indicator/cable panel with a customer supplied cable.
There are two different cables; one supports the IMP's local
interface (30 ft. max) and the other supports the IMP's distant
interface (2000 ft. max.).   Both cables plug into the same
connector on the IMP11-B although different pins are used. See
Table 2-1 for cable pin out.

NOTE

Do not connect the IMP cable to the
IMP11-B until the IMP11-B has been
checked out with its maintenance
plug.

2.2.5   IMP11-B Maintenance Plug

The maintenance plug for the IMP11-B is used to loop signals to
the IMP back into the IMP11-B. This allows the diagnostics to
test out the IMP11-B logic without an IMP connected.

2.3   GROUNDING

Ensure that the DD11-B or equivalent system unit is grounded to
the cabinet and that the whole system ground is adequately
grounded to earth ground. Consult the PDP11 installation guide
for system grounding.

2.4 SWITCH SETTING

There are a number of switches to set, in order to run the IMP11-B.

2.4.1 KMC11-A Address Switches

The device address or UNIBUS address of the IMP11-B is determined by setting the KMC11-A to the desired UNIBUS address. The possible range of addresses that the KMC11-A can be set to is 760000 to 777770. However, the address should be limited to the floating address space 760010 to 764000 or the IMP-11A addresses (772410 to 772430). Switches 1-10, located on E113 on the M8204, is used to set the address. The switches correspond to the following address bits:

10	9	8	7	6	5	4	3	2	1	Switch #'s
12	11	10	9	8	7	6	5	4	3	Address Bits

The switch in the off (open) position produces a logical 0 on the UNIBUS.

2.4.2 KMC11-A Vector Switches

The base Vector address of the IMP11-B is determined by setting the KMC11-A's Vector address switches. The possible range of addresses is 000 to 770. However, these addresses should be limited to the floating Vector address range (300 to 770). The addresses 500 - 534 are reserved. The DIP SWITCH located in E76 is used to select the vector address. The switches correspond to the following address bits:

6	5	4	3	2	1	Switch #'s
8	7	6	5	4	3	Vector Address Bit

An off switch (open) corresponds to a logical 0 on the UNIBUS.

2.4.3 Line Unit Driver/Receiver Select

The line unit (M8240) is capable of supporting local and distant IMP operations. Switch S1 will enable the proper set of driver/receivers. S1 off will enable the local logic.

2.5 FIELD CHECKOUT PROCEDURE

The filed checkout procedure requires the testing of the IMP11-B with the two diagnostics (static and dynamic) and maintenance plug. Follow the procedure below:

1. Mount the modules and panel in the available space as outlined in Section 2.1. Make sure that jumper CA1 to CB1 is removed from the SPC slot that the KMC11-A resides.

2. Ensure that the power is supplied to the pins as described in Section 2.1.3.

3. Install the cabling to the Indicator Panel and Line Unit module.

4. Set up the KMC11-A to the desired address (address the system software expects the IMP11-B to have). If this information is not available, set up the KMC11-A for an address of 160110 (8) and a vector of 300. See KMC11-A maintenance manual for the address set up.

5. Power up the system and run the following KMC11-A stand alone diagnostics:

    MAINDEC-11-DZKCA
    MAINDEC-11-DZKCC
    MAINDEC-11-DZKCD

6. Having successfully run these three diagnostics, connect the KMC11-A to the line unit via the BC08S-01 cable and install the maintenance plug to the indicator/cable panel. Run the IMP11-B static diagnostic error free.

7. Having run the static diagnostics error free, run the dynamic diagnostic error free. Run the diagnostic in the local and distant modes by switching S1.

At this point, the logic has been verified in the loop around Mode. The logic is now ready to test with the IMP.

CHAPTER 3

OPERATION AND PROGRAMMING

3.1 CONTROLS/SWITCHES

There are three sets of switches to set up for operation of the IMP11-B.

1. Device Address

2. Vector Address

3. Line Unit Local/Distant Select

The Device Address is selected by setting up the switches in DIP E113 on the M8204 KMC11-A module. The address range should be kept to the floating address space 760010 to 764000. See Section 2.4.1 for set up.

The Vector Address is selected by setting up the switches on the DIP E76 on the M8204 module. The vector range should be limited to the floating vector space (300 to 770, excluding 500 to 534). See Section 2.4.2 for set up.

The Local/Distant select switch is used to enable the driver/receiver logic to support local or distant operations. The IMP unit will have either a local or distant Host interface and the Line Unit must be set up to match this interface. Switch S1 on the M8240 module selects local or distant mode operation. See Section 2.4.3 for switch settings.

3.2 INDICATOR PANEL

The LED indicator panel is used to indicate the major status of the IMP11-B logic. It is useful in that it can indicate activity is occurring or a particular part of the logic is set. It obviously can't be used to give quantitative dates, as the speeds at which things occur are too fast for the eye to register.

3.2.1 Indicators

INDICATOR	FUNCTION
IMP LINE ERR	This indicator reflects the state of the IMP LINE ERR FLOP. When this light is on, it records that the IMP ready line has be dropped.
HOST RDY	This indicator indicates that the IMP11-B is one line, and that the IMP11-B relay is energized.
IMP RDY	This indicator is used to show that the IMP is on line.
KMC11 RUN	This bit is used to indicate that the KMC11-A micro code is running.
TX BUFFER EMPTY	This indicator shows that the Line Unit is able to accept a 16 bit word from the KMC11-A.
TX RFN IMP11 BIT	This indicator shows the state of the IMP's Ready For Next Bit line.
TX TY IMP11 BIT	This indicator shows the state of the IMP11-B's Theres Your Bit line.
TX LAST IMP11 BIT	This indicator reflects the IMP11-B's Last Bit line. This line is true once during a 16 bit word and not during every 16 bit word.
RX DATA AVAIL	This indicator indicates that the line unit has assembled a 16 bit word from the IMP and is ready for the KMC11-A to read.
RX RFN IMP BIT	This indicator indicates that the IMP11-B is ready to accept a bit from the IMP.
RX TY IMP11 BIT	This indicator shows the state of the IMP11-B's There's Your Bit line.
RX LAST IMP BIT	This indicator reflects the state of the IMP's Last Bit Line.

3.3 SYSTEM OPERATION

Operation of the IMP11-B microprogram is initiated and directed by a user-produced program residing in the main CPU memory space. Communication between the user program and the IMP11-B is provided by a set of four control and status registers (CSR's), which are integral to the KMC-11 microprocessor. These four 16-bit registers are used for control input, status output, and data input and output. The firmware within the KMC-11 microprocessor is supplied and supported by DEC. No other version of the firmware is supported.

The two low bytes in the first two registers in this group have a fixed format and serve as the command header for the second two registers. The second two registers form a two-word data port for the exchange of unique control/status commands between the IMP11-B and the user program. The contents of the data port are specified by an identification field in the command header. Other specific fields in the two-word command header control interrupt enabling and set up data transfers between the main CPU and the IMP11-B. The second byte of the first word is used to contain a special command issued by the user program for implementing microprocessor start, halt and initialization. Detailed descriptions of each field in these four words are presented in Sections 3.3.3 - 3.3.7.

A user program issues a command to the IMP11-B by storing the command in the pertinent CSR's. The IMP11-B then interprets the command and performs the specified actions. Similarly, the IMP11-B issues a command to the user program by storing the command in the pertinent CSR's and notifying the user program that a command is available for retrieval and execution.

Message data received or transmitted by the IMP11-B is written into or read from user program assigned buffers in main CPU memory. The IMP11-B accesses these buffers through Non Processor Requests (NPR) to a UNIBUS address. A UNIBUS address is defined as an 18-bit address of the main CPU memory location which has been reserved for use by an NPR device.

3.3.1 Command Structure

The functions of the seven IMP11-B control/status/data commands are described in the sections that follow.

3.3.1.1 INITIALIZATION Command - The purpose of the single byte INITIALIZATION command is to clear all condition sensitive logic in the KMC-11 microprocessor and to place the processor in the RUN state. This command must be issued by the user program once prior to starting the IMP11-B line initialization procedure.

3.3.1.2 LINE Initialization Command - This command is used to initialize the line in either the receive or transmit direction. A separate command must be issued for each direction. This command must be issued before any buffer Descriptor Lists will be accepted by the IMP11-B. It can also serve to reset the given direction any time during execution.

3.3.1.3 CONTROL IN Command - These commands are issued by the user program to force control action by the IMP11-B.

3.3.1.3.1 SET/RESET HOST READY - This command is used to set or clear the HOST READY control bit in the IMP11-B. This bit must be set in order for data transfers to occur. The HOST READY bit may be used to signal the other system that the IMP11-B is ready to start data transfer. The clearing and resetting of this bit will be detected by the IMP in the node.

3.3.1.3.2 CLEAR READY LINE ERROR - READY LINE ERROR is latched set whenever the IMP goes not ready. It can only be reset by the user program. The CLEAR READY LINE ERROR command clears the READY LINE ERROR control bit if the IMP NOT READY condition has gone away. The IMP11-B will not restart data transfers as long as the READY LINE ERROR bit is set.

3.3.1.3.3 REQUEST STATUS - This command causes the IMP11-B to pass back the current state of the communication control lines to the user program.

3.3.1.4 BUFFER DESCRIPTOR IN Command - The user program issues this control command to the IMP11-B to assign a new buffer Descriptor List to the designated direction (receive or transmit). A BUFFER DESCRIPTOR IN command points to and defines only one user defined list, and this command must be repeated for each list passed to the IMP11-B. The user program can assign a maximum of two lists in each direction. The command contains the starting list address, expressed as an 18 bit Unibus address.

3.3.1.5 BUFFER OUT Command - The IMP11-B issues this control command to the user program when the buffer assigned to a receive operation is terminated. Generally, a receive buffer is terminated when the buffer is full (byte count = zero). The command contains the 18-bit physical address of the entry in the buffer Descriptor List. The reason for termination is expressed

as a signed octal number -128 - +127. Negative values represent
failure to terminate the buffer successfully.

3.3.1.6 BUFFER DESCRIPTOR OUT Command - The IMP11-B issues this
control command to the user program when a Buffer Descriptor List
assigned to either receive or transmit is terminated.   The
command contains the 16-bit physical starting address of the
Buffer Descriptor List. The reason for termination is expressed
as a signed octal number -128 - +127. Negative values represent
failure to terminate the Buffer Descriptor List successfully.

3.3.1.7 CONTROL OUT Command - The IMP11-B issues one of these
commands to the main CPU when it detects a transmit or receive
error, or on request by the CPU.

3.3.2 Data Transfer Operations

For the purposes of this system overview, the transmit and
receive data command sequences described in this section are
general and are meant to serve as background for the detailed
presentations in the chapters that follow.

3.3.2.1 Initialization Sequence - After the IMP11-B microprogram
is loaded, the first action taken by the user program is to issue
an INITIALIZATION command which performs a MASTER CLEAR on the
KMC-11 microprocessor and places the processor in the Run state.
With this action complete, the IMP11-B is ready to accept the
first command from the user.

3.3.2.2 Line Initialization Sequence - The user program must
issue one LINE INIT command for each direction to be activated.
The command enables the line for subsequent transmission or
reception.

3.3.2.3 Receive/Transmit Sequence - Once the user program has
initialized the line through LINE INIT commands, the IMP-11B is
ready to perform a receive or transmit data operation.

An actual reception or transmission is initiated when the user
program issues a BUFFER DESCRIPTOR IN command.when a buffer is
assigned, it is designated for either reception or transmission.

The IMP-11B informs the user program of a normal receive data

transfer termination by issuing a BUFFER OUT command. The IMP-11B terminates a normal data transfer operation for one of two reasons: the buffer designated by the last Buffer Descriptor List entry has been filled or an End-of-Message sequence has been detected. If a reception error is detected, the IMP-11B informs the user program of the error by issuing a BUFFER OUT command containing the code designating the error condition.

The IMP11-B informs the user program of a normal completion of both transmit and receive Buffer Descriptor Lists by issuing a BUFFER DESCRIPTOR OUT command. If certain line errors are detected, the IMP11-B returns the affected Buffer Descriptor Lists by issuing BUFFER DESCRIPTOR OUT commands containing the code designating the error condition.

3.3.3 Command Structure

As previously shown, the IMP-11B is an NPR device residing on a PDP-11 UNIBUS. Communication between the main CPU-resident user program and the IMP-11B is accomplished through a set of four 16-bit UNIBUS Control and Status registers (CSR's). The eight bytes comprising these four registers are assigned the following addresses in the I/O page floating address space: 76xxx0, 76xxx1, 76xxx2, 76xxx3, 76xxx4, 76xxx5, 76xxx6, and 76xxx7 with the full-word addresses being the four even-numbered locations. In addition, all four UNIBUS CSR's are both byte and word addressable. Within the concept of floating UNIBUS addresses, the actual word and byte addresses are assigned at system configuration time.

In this explanatory narrative, the 8-byte addresses are designated BSEL0 through BSEL7 and the 4-word addresses, SEL0, SEL2, SEL4, and SEL6. The byte and full-word formats for the IMP11-B UNIBUS CSR's, based on these designations, are summarized in Figure 3-1. These address references, as designated in Figure 3-1, are the basis for CSR address identification in the following detailed descriptions of the IMP11-B commands.

Since the IMP11-B is basically an input-output device, it follows that the command set for this device can be categorized as input commands and output commands. As opposed to received and transmitted data, input commands are commands issued to the IMP11-B by the main CPU, output commands are those issued to the main CPU by the IMP11-B. The structure and format of the IMP11-B input and output commands are described in Sections 2.4 and 2.5 respectively.

Figure 3-1   IMP11-B Unibus Register Address Format

BSEL1	BSEL0	SEL0
BSEL3	BSEL2	SEL2
BSEL5	BSEL4	SEL4
BSEL7	BSEL6	SEL6
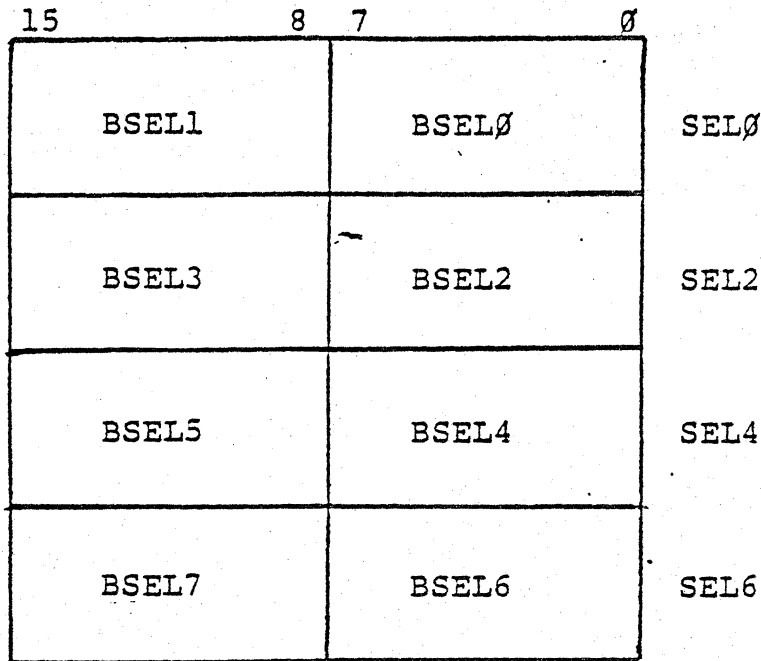
3.3.4 CSR Control

The IMP11-B is the controller of the CSR's and the PDP-11 user program is only to read or write into the data port when permitted by the IMP11-B. A protocol must be adhered to by the user program if it is to successfully issue commands and receive commands from the line unit. BSEL0 is the input control register. BSEL2 is the output control register. The two transfer directions have been split into different registers to avoid race conditions and subsequent data loss. However there is still a possibility of the interrupt enable bit being cleared or reset during certain 1 microsecond windows.

3.3.4.1 Input Control Protocol -
   Figure 3-2   Input Control Register - BSEL0

7	6	5	4	3	2	1	0
RDYI	IEI	RQI	UNUSED		I/O	COMMAND TYPE	
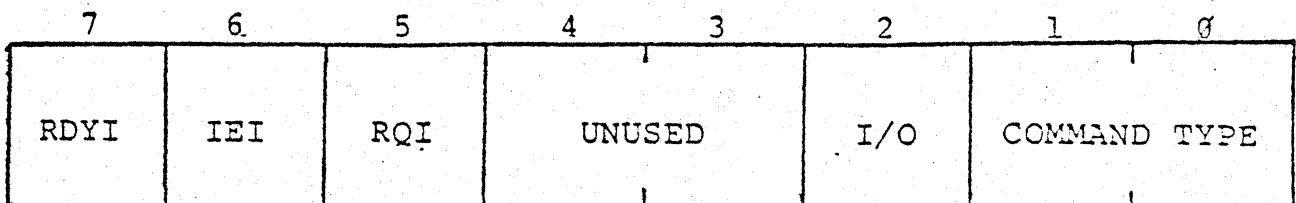
COMMAND TYPE   00 - BUFFER DESCRIPTOR IN
                01 - CONTROL IN
                11 - LINE INIT

I/O   Direction of data transfer - required only on
                BUFFER DESCRIPTOR IN and LINE INIT commands
                (0 = transmit 1 = receive)

ROI   Request Input bit must be set by the user
                program to request control of the 5 data port
                bytes (BSEL3-BSEL7). NOTE: Control is not
                actually granted until RDYI is set by the
                IMP11-B.
                This bit must be cleared after BSEL3-BSEL7
                are loaded to trigger the IMP11-B to accept
                the command

RDYI   when set by the IMP11-B, indicates the user
                program has control of BSEL3-BSEL7

IEI   Input Interrupt Enable - when set by the user
                program (at the same time ROI is set), will
                cause the IMP11-B to generate an interrupt
                vectoring at XX0 when it sets RDYI

The format of the Input Control Register is given in Figure
3-2. In order to pass a command to the IMP11-B the user
program must specify the type of command requested in bits
0-1 of the Input Control Register. For the BUFFER IN and
LINE INIT commands, the direction of data transferred must
also be specified. For the CONTROL IN commands this bit is
ignored.

At this point the user must set the Request Input bit (bit 5
- ROI) to request control of the 5 data port bytes, BSEL3-7.
The IMP11-B will respond to the setting of ROI by asserting
RDYI, which gives control of the data ports to the user
program. Until RDYI is set the user cannot write into the
data ports without the possibility of corruption. The user
has two alternatives after setting ROI, either continually
or periodically testing for RDYI set or setting Input
Interrupt Enable (IEI) with ROI. If interrupt enable is set
the IMP11-B will generate an interrupt vectoring at XX0 when
it sets RDYI.

On detection of RDYI the user program should write all
relevant information into the data ports. Care must be
taken to clear all unused bytes as these ports are not
cleared by the IMP11-B and spurious results may occur.

When the command is complete the user program clears ROI,
which triggers the IMP11-B to accept the command.

At this point the user program is inhibited from writing in

the input control register or any data port until the IMP11-B drops RDYI.

When RDYI is dropped the input cycle is complete and the user can initiate another input command.

3.3.4.2 Output Control Protocol -
   Figure 3-3   Output Control Register - BSEL2

7	6	5	4	3	2	1	0
RDYO	IEO	RQO	UNUSED		I/O	COMMAND TYPE	
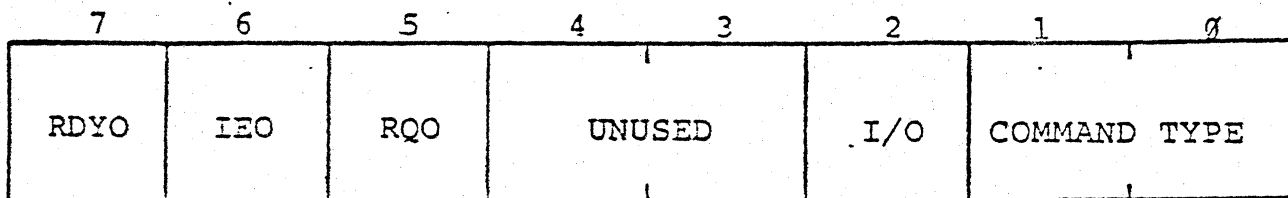
COMMAND TYPE   00 - BUFFER DESCRIPTOR OUT
                01 - CONTROL OUT
                10 - BUFFER OUT

I/O   Direction of transfer, if applicable
                (1 = transmit; 0 = receive)

RDYO   Set by the IMP11-B to indicate it has issued
                an output command in the CSR's. This bit
                must be cleared by the user program to
                indicate it is done with the CSR information.

IEO   Output Interrupt Enable - if this bit has
                been set by the user program, the setting of
                RDYO by the IMP11-B will generate an
                interrupt vectoring at XX4

The format of the Output Control Register is given in Figure
3-3.   When the IMP11-B issues an output command it will set
the command type in bits 0-1 of BSEL2. Bit 2 reflects the
direction of data transfer if required by the command. RDYO
(bit 7) will be set concurrently. If output interrupt
enable is set, the IMP-11B will generate an interrupt
vectoring at XX4.

On detection of RDYO the user program can take whatever
action is required but must indicate the completion of the
output command by dropping RDYO.

3.3.5 Buffer Descriptor List Entry Format

All buffer information is passed to the IMP11-B in the form
of Buffer Descriptor Lists. Each list consists of an
open-ended series of entries as defined in Figure 3-4.

Figure 3-4 Buffer Descriptor List Entry Format

	15											LEOM	BA 17	BA 16		0
N					BUFFER ADDRESS											
N+2												LEOM	BA 17	BA 16		
N+4					WORD COUNT											
N+6								STATUS (0 ON TRANSMIT)								
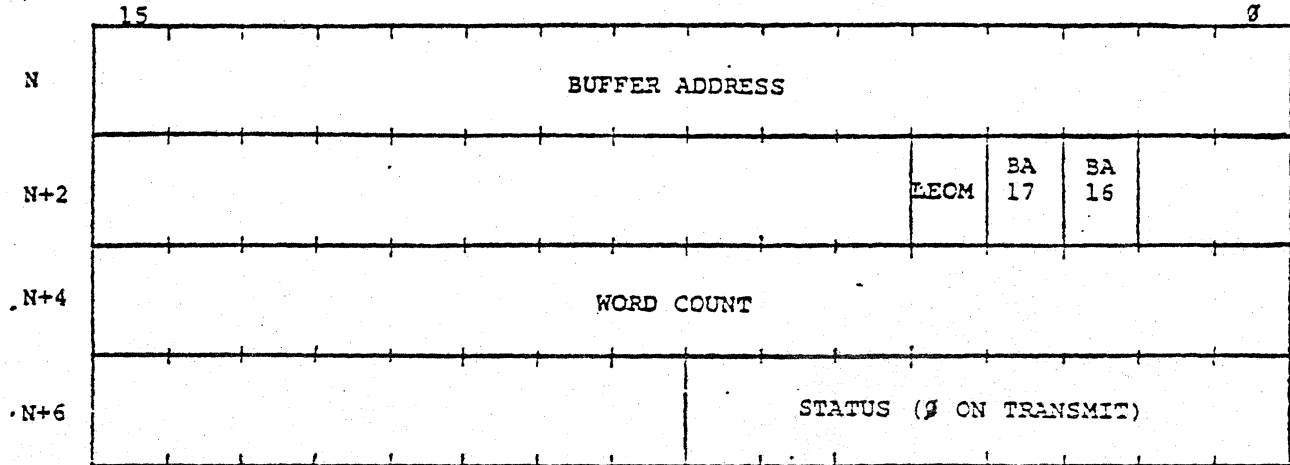
N

BUFFER ADDRESS   Bits 0-15 of the 18-bit physical address
                 of the start of buffer

N+2

BA16, BA17   Bits 16-17 of the 18-bit physical address
                 of the start of buffer

LEOM   Logical end of message occurs at the end
                 of this buffer (yes = 1; no = 0)

N+4

WORD COUNT   The length of the buffer in 16-bit words (odd
                 byte is rounded up to the next full word)

N+6

STATUS   Termination status of transfer (should be
cleared by
                 user program before passing on list to the
IMP11-B)

                 VALUE   DEFINITION

                 1   Buffer word count reached zero

```
2          Receive EOM detected
-4         READY LINE ERROR
-5         Non-existent memory location
```

The last entry in the Buffer Descriptor List must be followed by the list terminator which is a word containing a '1' in Bit 0.

3.3.6 Input Commands

As previously described, the IMP-11B executes four forms of input commands, which are listed below in the general order of user program issuance:

1. INITIALZATION

2. LINE INITIALIZATION

3. CONTROL IN

4. BUFFER DESCRIPTOR IN

As a general rule for input commands, the user program must execute the PDP-11 instruction BISB to store data in BSEL0 and BSEL2, a MOV to store data in SEL4 and SEL6, and a MOVB to store data in BSEL3, BSEL4, BSEL6, and BSEL7.

The format and field descriptions for each command are detailed in the following paragraphs. Some typical examples of PDP-11 instructions and instruction sequences are included to demonstrate the user-program command-issuing process. These examples are presented for explanation only and do not imply a single method of implementation.

3.3.6.1 INITIALIZATION Command -
Figure 3-5 System Initialization (BSEL1)

15	14						8
RUN	MCLR						
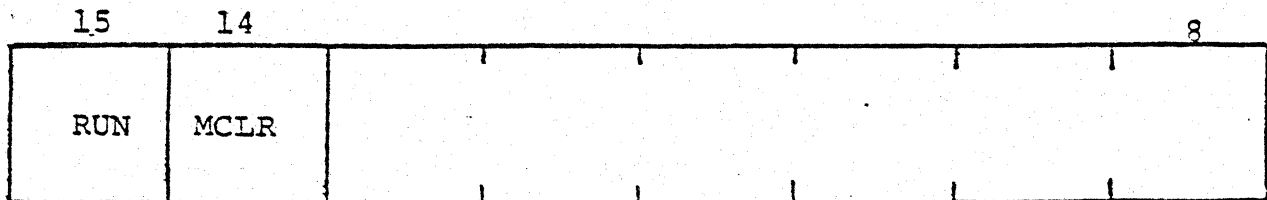
```
RUN          When set, RUN allows the KMC clock to run and
             therefore execute the firmware.
             This bit is cleared by BUS initialization  or
             MASTER CLEAR
```

MCLR   MASTER CLEAR - when set, initializes both the
              KMC and line unit and stops the KMC clock

INITIALIZATION is the first command issued by a user program
at startup time, to initialize the KMC-11 microprocessor and
place the unit in the run state. The format of the
INITIALIZATION command is shown in Figure 3-5.

Initializing the KMC-11 microprocessor by the user program
is done in two steps. First the Master Clear bit is set
followed by setting of the Run bit. After setting the Run
bit, the user program must wait for 1MS before accessing one
of the command headers BSEL0 or BSEL2. The recommended
method for setting the Master Clear and Run bits, and at the
same time implementing the required delay is to write a
non-zero value into BSEL2 and wait for the IMP-11B to clear
the byte before proceeding. For example:

```
    MOV     #40000,SEL0      ;SET MASTER CLEAR BIT
    MOVB    #377,BSEL2       ;WRITE NON-ZERO VALUE IN BSEL2
    MOV     #100000,SEL0     ;SET RUN BIT
A:  TSTB    BSEL2            ;CLEARED YET?
    BNE     A                ;NO
    BR      B                ;YES, PROCEED TO B
```


                         NOTE

    Since the Master Clear bit is not self-clearing, a
    move instead of a bit set instruction is required to
    clear the master clear bit and set the Run bit.

These actions set the Run bit placing the IMP11-B in the
operational state. At this point, the user program can
begin setting up the IMP11-B for subsequent operations.
SEL0 Bits 8 through 13 are designated maintenance bits.
These bits are used by loading, maintenance and diagnostic
routines and have no effect on normal IMP11-B operation.

3.3.6.2 Issuing Input Commands - All input commands other
than INITIALIZE are issued by a user program in two
successive steps. In general, the first step involves a
request for permission to issue an input command and a
response by the IMP11-b that it is ready to accept the
command. Although the programming sequences for the first
step are described for the LINE INIT command, they also
apply to the CONTROL IN and BUFFER DESCRIPTOR IN commands.
The sequence for the second step involves completing the
command by loading BSEL3, SEL4, and SEL6 with the data
appropriate to each command. This sequence is therefore

different for each command.

With the exception of the first LINE INIT command issued at startup time, the user program must check that the RDYI bit has been cleared prior to issuing the next input command (including the second and subsequent LINE INIT commands). The IMP11-B clears RDYI to signal that the last input command issued has been completed. When clearing RDYI, the IMP11-B also clears all other bits in BSEL0 except the IEI bit. An instruction sequence to test the RDYI bit can take the form

```
A:  TSTB  BSEL0
    BMI   A          ;RDYI STILL SET
    BR    B          ;CLEARED-ISSUE COMMAND
```

NOTE

Since the IMP11-B does not clear BSEL3, SEL4, or SEL6, the user must ensure that these registers are cleared by executing appropriate clear instructions prior to issuing a command or by issuing the command with MOV or MOVB instructions.

With the RDYI bit cleared, the initial task to be performed by the user is to set the command identity field (in this example, BSEL0 bits 0 and 1 = 1), the RQI bit, and if necessary the IEI bit. With the RQI bit set, the user program must then wait for the IMP11-B to set RDYI.

How this procedure is programmed depends on whether the state of the IEI bit enables interrupts. The latency between the user program setting the RQI bit and the IMP11-B responding by setting RDYI can range from a minimum of 2 us to a maximum of 5 ms. When using the IEI bit, the user has three alternatives:

1. Set the IEI bit to enable interrupts. As a consequence, the IMP11-B interrupts the main CPU when it sets the RDYI bit. The PDP-11 instruction implementing this alternative can have the form

```
        MOVB  #143,BSEL0  ;SET RQI, IEI, AND INIT IX CODE
```

    When interrupted the user program can proceed directly to load BSEL3, SEL4, and SEL6 with the appropriate data.

2. Leave the IEI bit cleared and check the state of the RDYI bit by setting a timer and performing a test or performing a continuous test loop. The form of the bit test sequence based on a timer is

```
        C:  TSTB  BSEL0
```

```
            BMI   A      ;RDYI SET, LOAD COMMAND
            BR    B      ;RDYI NOT SET, RESET TIMER AND
                         ;RESUME PRIOR TASK AT B.  WHEN TIMER
                         ;GOES OFF REENTER AT C.
```

If a bit test loop is required, the sequence form is

```
      E:    TSTB  BSELO
            BPL   E      ;RDYI NOT SET, BRANCH TO E AND TEST
                         ;AGAIN
            BR    D      ;RDYI SET, GO TO D AND LOAD COMMAND
```

3. Using this alternative, the user program clears IEI (if
    set by the prior command), sets RQI, and then performs
    the housekeeping associated with issuing the current
    command. With the housekeeping done, the user program
    checks RDYI. If RDYI is set, the user program completes
    the command issuing process. If not set, the user
    program sets IEI and resumes a prior task while awaiting
    an interrupt on RDYI set.

    The advantage of this alternative is that interrupt
    overhead is substantially reduced since the IMP11-B
    usually sets RDYI within a few microseconds after the
    user program sets RQI. The form of the instruction
    sequence for this approach is

```
            BICB  #100,BSELO   ;CLEAR IEI
            MOVB  #43,BSELO    ;SET RQI AND COMMAND ID


                  Do housekeeping
```

                              NOTE

      There is a 1 - microsecond window during which
      the IMP11-B can clear IEI. To guard against
      inadvertent clearing the user program sould make
      sure during housekeeping that IEI is actually
      set.

```
            TSTB  BSELO             ;TEST RDYI
            BMI   A                 ;COMPLETE COMMAND
      B:    BISB  #100,BSELO        ;SET IEI
            BITB  #100,BSELO        ;MAKE SURE IEI IS NOT CLEARED
            BEQ   B                 ;IT IS CLEARED - RESET
            BR    TASK              ;RESUME PRIOR TASK
```

The instruction sequence to complete the input command loads
the proper values into the data ports. For LINE INIT, this

sequence is

```
        CLRB    BSEL3           ;NO INFO REQUIRED IN LINE INIT
        CLR     SEL4
        CLR     SEL6
        BICB    #040,BSEL0      ;CLEAR RQI
```

3.3.6.3 LINE INITialization Command - Figure   3-6
illustrates the format for the LINE INIT command, which
clears out all Buffer Descriptor List pointers in the
indicated direction. No notification of aborted buffers or
lists is sent back to the user program. The command also
saves the starting IMP state (Ready / Not Ready). One LINE
INIT command must be issued for each direction to be
activated.

Figure 3-6 LINE INIT Command

	7						0	
	RDYI	IEI	RQI	UNUSED	I/O	1	1	SEL0

15															
						UNUSED									SEL4
						UNUSED									SEL6
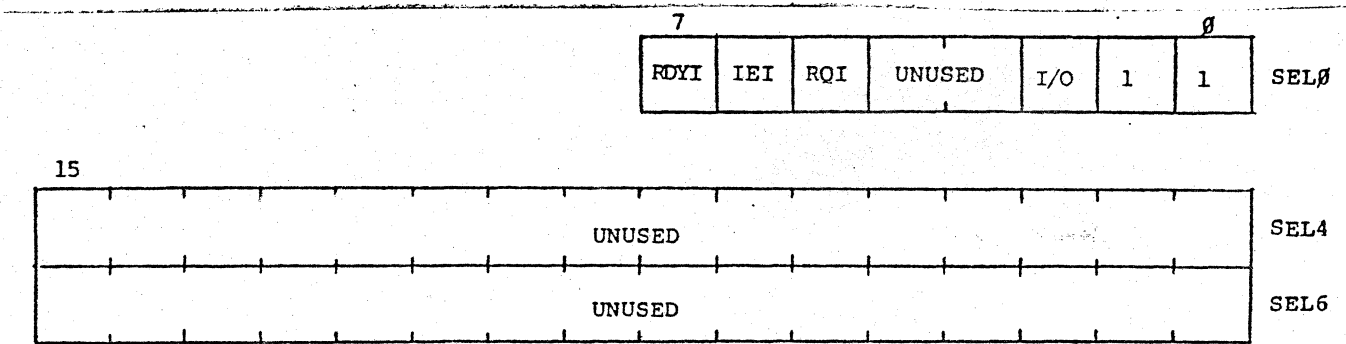
I/O   Direction to be initialized
                 (0 = transmit 1 = receive)

3.3.6.4 CONTROL IN Command - These commands are used for
non-buffer related functions.

For each CONTROL IN command, the low order bits of BSEL7 are
reserved for the subfunction field. The valid values are

        001   Set/Reset Host Ready
        010   Status Request
        100   Clear Ready Line Error

BSEL6 is reserved for the data field. It is only used in
the Host Ready command.

3.3.o.4.1 SET/RESET HOST READY COMMAND - The format of this command is given in Figure 3-7.

Figure 3-7   SET/RESET HOST READY Command

7						0	
RDYI	IEI	RQI	UNUSED	0	0	1	SEL0

15			10	9	8							
UNUSED												SEL4
UNUSED		0	0	1	UNUSED						S/C	SEL6
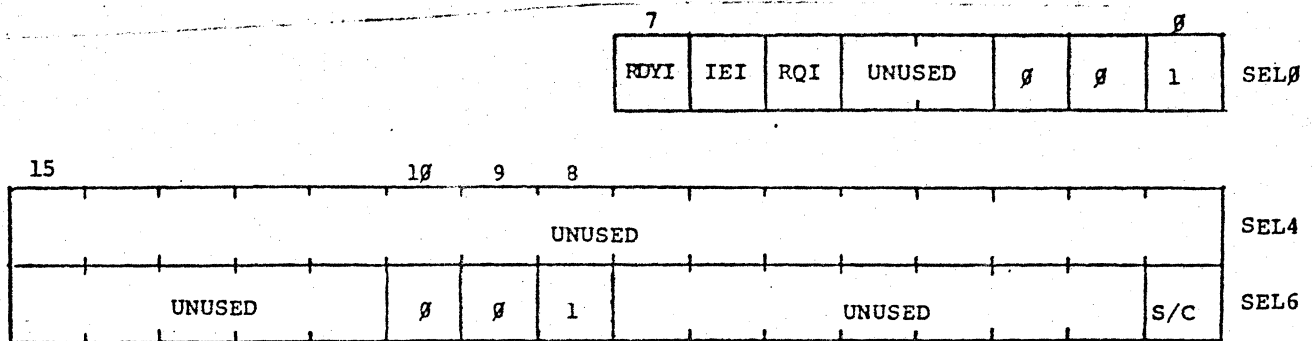
S/C   New value of HOST READY control bit
              (1 = set   0 = clear)

3.3.o.4.2 STATUS REQUEST Command - This command causes the IMP11-B to issue a CONTROL OUT Returned Status command giving current information on both receive and transmit line unit registers. The format for this command is given in Figure 3-8.

Figure 3-8   STATUS REQUEST Command

7						0	
RDYI	IEI	RQI	UNUSED	0	0	1	SEL0

15			10	9	8						
UNUSED											SEL4
UNUSED		0	1	0	UNUSED						SEL6
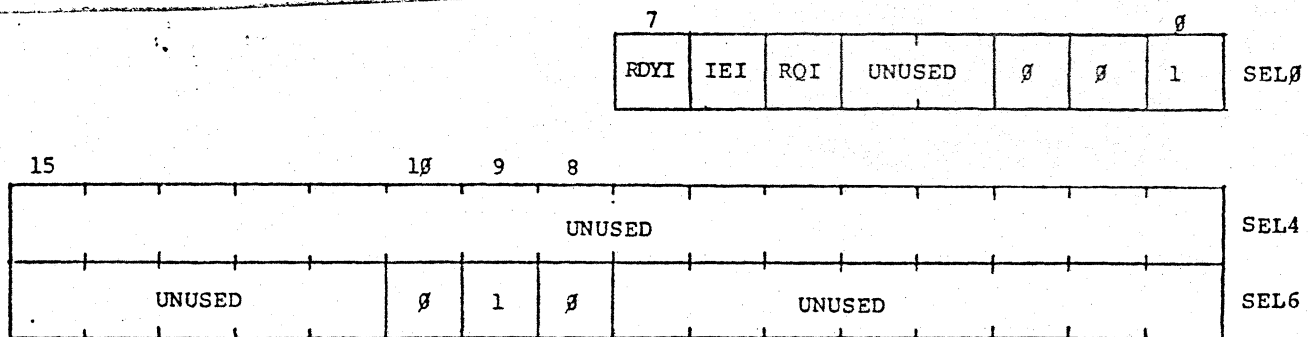
3.3.6.4.3 CLEAR READY LINE ERROR Command - This command attempts to clear the READY LINE ERROR control bit by setting and then clearing the TX ERR CLEAR bit in the line unit register. However, if IMP NOT READY is set, READY LINE ERROR will remain set. The format for this command is given in Figure 3-9.

Figure 3-9   CLEAR READY LINE ERROR Command

RDYI	IEI	RQI	UNUSED	0	0	1	SEL0

(bits 7 ... 0)

UNUSED			SEL4
UNUSED	1	0	0	UNUSED	SEL6

(bits 15 ... 8)
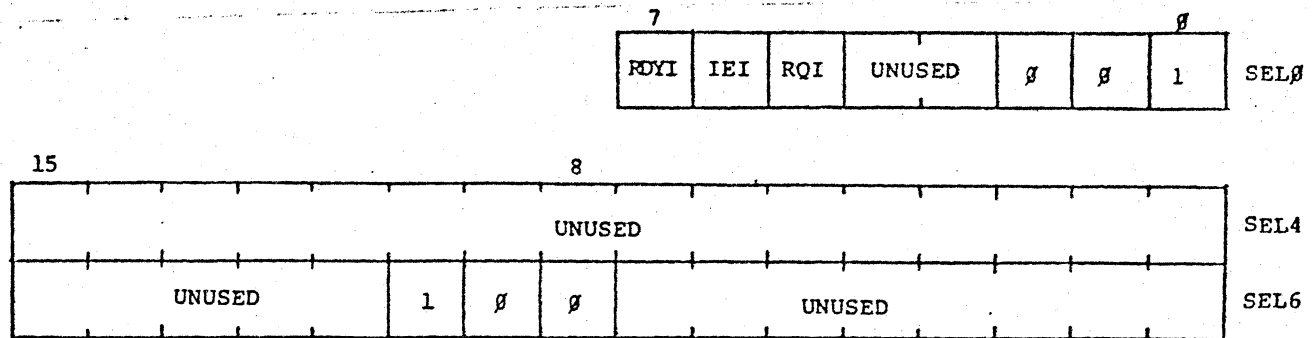
3.3.6.5 BUFFER DESCRIPTOR IN Command - The format for this command is presented in Figure 3-10. Note that SEL4 and Bits 2 and 3 of BSEL7 contain an 18-bit UNIBUS address that is the starting address of the Buffer Descriptor List. The starting address of a Buffer Descriptor List must be word aligned, i.e., on an even address boundary.

Figure 3-10   BUFFER DESCRIPTOR IN Command Format

RDYI	IEI	RQI	UNUSED	I/O	0	0	SEL0

(bits 7 ... 0)

BDL ADDRESS				SEL4
UNUSED	BA 17	BA 16	UNUSED	SEL6

(bits 15 ... 11 10 ...)
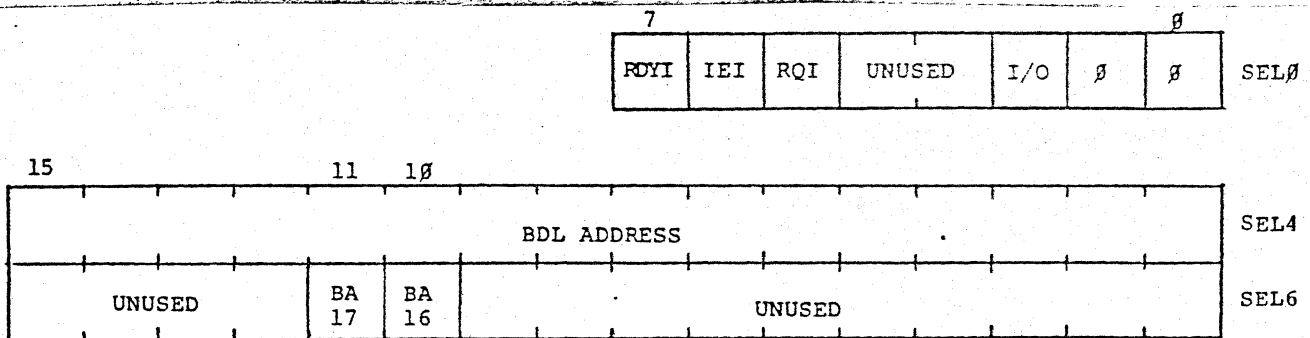
I/O   This bit indicates the transfer direction of
               the Buffer Descriptor List (0 = transmit 1 =
               receive)

BDL ADDRESS   Bits 0-15 of the 18-bit physical adress of
               the start of the Buffer Descriptor List .

BA16, BA17   Bits 16-17 of the 18-bit physical address of
               the start of the BDL

3.3.7 Output Commands

Output commands provide the vehicle whereby the IMP11-B
communicates with the main CPU. The IMP11-B uses the output
commands to convey categories of information:

1. The BUFFER DESCRIPTOR OUT command is used to post normal
    and error terminations of receive and transmit buffer
    Descriptor Lists.

2. The BUFFER OUT command is used to post information
    concerning the completion of received data buffers with
    both normal and error terminations.

3. The CONTROL OUT command is used to post both solicited
    and unsolicited status information.

Figures 3-2 and 3-3 illustrate the identical positional
correspondence between control and command identity bits in
the input and output command headers (BSEL0 and BSEL2,
respectively). The state of the IEO (output interrupt
enable) bit must be established by the user program during
system initialization time. When set, this bit will cause
the IMP11-B to interrupt the main CPU each time an output
command is ready for retrieval by the user program. When
cleared, the IMP11-B does not interrupt, making the user
program responsible for recognizing that an output command
is ready for retrieval.

At initialization time, immediately after issuing the
maintenance command, the user program must establish the
state of the IEO bit. In addition, whether IEO is to be set
or cleared, the remainder of BSEL2 must be cleared to ensure
the integrity of the control and ID bits. For example,

        MOVB   #100,BSEL2   ;CLEAR BSEL2 AND SET IEO

or
        CLRB   BSEL2   ;CLEAR BSEL2 AND IEO

Since the specific state of the IEO bit is implicit in the
design of the user program, this bit must be set to the same
state at each subsequent initialization time. Whatever the
method of command recognition chosen, the user should be
aware that operation in the interrupt mode is by far the
most efficient way of processing output commands.

3.3.7.1 Issuing An Output Command - The IMP11-B issues
output commands in two steps. First, the data pertinent to
the command being issued are stored in BSEL3, SEL4, and SEL6
(Figure 3-1). Once this data storage is complete, the
IMP11-B sets the RUN, RDYO, and identity bits in BSEL2
(Figure 3-3). If required, the OUT I/O bit is set to
indicate that the completion posted involves a receive data
operation or cleared to designate a completion posting for a
transmit data operation.

with the header bits configured and IEO set, the IMP11-B
then interrupts the main CPU causing the user program to
check the ID bits to determine the command type.

A user program, designed to operate in a noninterrupt mode,
must be set up to periodically test the state of the RDYO
bit. A PDP-11 instruction sequence to periodically test the
RDYO bit and when set check the ID bits can take the
following form:

```
A:    TSTB  BSEL2              ;TEST RDYO BIT.
      BPL   B                  ;CLEARED, PERFORM USER ASK AND REENTER
                               ;AT A DURING NEXT PERIOD.
      BITB  #1,BSEL2           ;SET, TEST ID BITS.
      BNE   C                  ;RETRIEVE BUFFER DESCRIPTOR OUT COMMANDS
                               ;AND PROCESS.
      BR    D                  ;RETRIEVE CONTROL OUT COMMAND AND
                               ;PROCESS
```

For interrupt-driven user programs, a test of the RDYO bit
is unnecessary since the interrupt implies that the bit is
set. In this case the first user program action upon
receiving the interrupt is to test the ID bits to determine
the command type to be processed. If the command is
ascertained to be a BUFFER DESCRIPTOR OUT command, the user
program can determine whether the completion being posted
involves a transmit or receive data operation by checking
the OUT I/O bit. For example,

```
E:    BITB  #4,BSEL2           ;CHECK OUT I/O BIT
      BEQ   F                  ;TRANSMIT OPERATION
      BR    G                  ;RECEIVE OPERATION
```

Upon completing the retrieval of the pertinent command, the
user program must clear RDYO to inform the IMP11-B that the
retrieval is complete. For example:

```
      BICB  #200,BSEL2         ;CLEAR RDYO
```

NOTE

1. The IMP11-B will not respond to a user program request to input a command (RQI set to 1 in BSEL0) if an output completion is pending (RDYO = 1).

2. The user must save all required information from the IMP11-B's CSR's before clearing RDYO as the IMP11-B may alter them immediately upon detecting RDYO clear.

3.3.7.2 BUFFER OUT Command - This command is used by the IMP11-B to inform the user program that a receive buffer has been filled or an end of message indication has been detected and data is now available for processing. The format for this command is given in Figure 3-11.

Figure 3-11 BUFFER OUT Command

15					11	10			7								0	
UNUSED									RDYO	IEO	RQO	UNUSED			1	1	0	SEL2
ENTRY ADDRESS																		SEL4
UNUSED				EA 17	EA 16	UNUSED			STATUS									SEL6

ENTRY ADDRESS   Bits 0-15 of the 18-bit physical address of the entry in the Buffer Descriptor List describing the buffer

EA16, EA17   Bits 16-17 of the 18-bit physical address of the BDL entry

STATUS   Buffer termination status (See Section 3.3.5 for list of values)

3.3.7.3 BUFFER DESCRIPTOR OUT Command - As previously stated, this command is used by the IMP11-B to inform the user program that a data transfer operation is complete. Functionally, this command is used to post the use of buffers in the list to the user program. The format for this command is given in Figure 3-12.

Figure 3-12   BUFFER DESCRIPTOR OUT Command

15	11	10		7						0	
UNUSED				RDY0	IE0	RQO	UNUSED	I/O	0	0	SEL2
BDL ADDRESS											SEL4
UNUSED	BA 17	BA 16	UNUSED	STATUS							SEL6
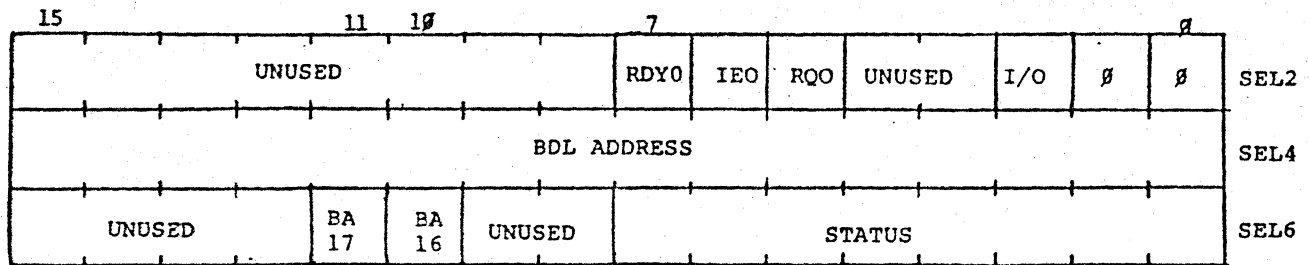
I/O   Direction associated with the Buffer
                 Descriptor List (0 = transmit 1 = receive)

BDL ADDRESS   Bits 0-15 of the 18-bit physical address of
                 the start of the Buffer Descriptor List

BA16, BA17   Bits 16-17 of the 18-bit physical address of
                 the start of the BDL

STATUS   Buffer Descriptor List termination status
                 (See Section 3.3.5 for list of values)

3.3.7.4   CONTROL OUT Command - These commands are used by
the IMP11-B to inform the user program of the current status
of the line on request, plus any errors or status changes
that do not result in a buffer completion.

3.3.7.4.1   RETURNED STATUS - This command is sent in
response to a CONTROL IN Status Request command. It hands
back information concerning the current line unit status.
The information is passed directly from the IMP11-B line
unit registers. The format for this command is given in
Figure 3-13. A full description of each of the status bits
is given in Section 4.2.1.
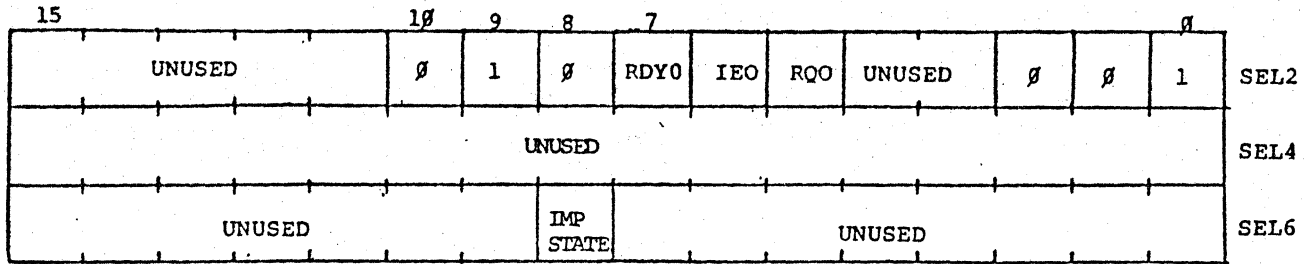
Figure 3-13   RETURNED STATUS Command

15			10	9	8	7						0	
UNUSED			∅	∅	1	RDY0	IE0	RQO	UNUSED	∅	∅	1	SEL2
IMP NOT RDY	UNUSED			RFNB	BUFF EMPTY	UNUSED					TX CLR STATUS	TX CLR STATUS	SEL4
RDY LINE ERR	UNUSED			END MSG	DATA AVAIL	UNUSED					HOST RDY	RX CLR STATUS	SEL6

IMP NOT RDY   IMP NOT READY control line

RFNB   READY FOR NEXT BIT control line

BUFF EMPTY   TRANSMIT BUFFER EMPTY control line

TX CLR ERROR   CLEAR TRANSMIT ERROR control bit

TX CLR STATUS   CLEAR TRANSMITTER STATUS control bit

RDY LINE ERR   READY LINE ERROR control bit

END MSG   END OF MESSAGE REACHED control bit

DATA AVAIL   RECEIVE DATA AVAILABLE control bit

HOST RDY   HOST READY control bit

RX CLR STATUS   CLEAR RECEIVER STATUS control bit

3.3.7.4.2 IMP STATE TRANSITION - This command is sent
whenever a transition in the IMP state is detected. The
IMP11-B uses the latched LINE RDY ERR bit to tell if IMP NOT
RDY had ever occurred, since initialization or the last
time LINE RDY ERROR was cleared. The TX CLR ERROR bit is
set and reset to attempt to clear the LINE RDY ERR bit. If
the IMP NOT RDY state is still present, the LINE RDY ERR
will remain set. If the LINE RDY ERR stays clear, a new IMP
transition has occurred and will be reported in a second IMP
STATE TRANSITION command. The format for this command is
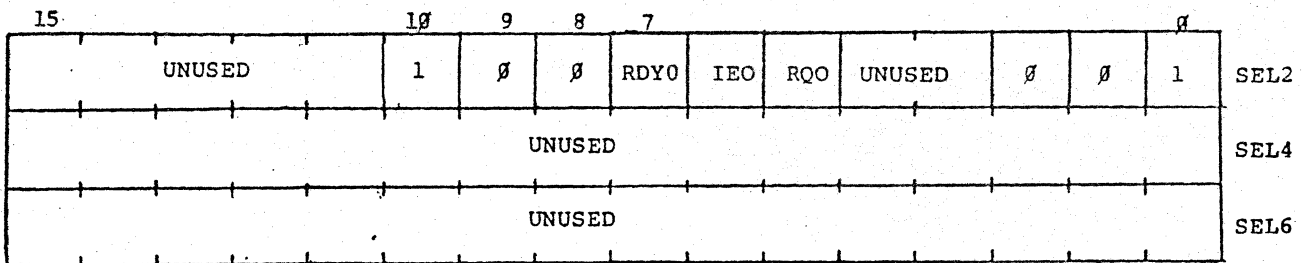given in Figure 3-14.

Figure 3-14 IMP STATE TRANSITION Command

15					10	9	8	7					0	
UNUSED					Ø	1	Ø	RDY0	IEO	RQO	UNUSED	Ø	Ø	1	SEL2
UNUSED															SEL4
UNUSED						IMP STATE		UNUSED							SEL6

```
IMP STATE        The current value of the IMP NOT RDY bit
                 (1 = Not Ready 0 = Ready)
```

3.3.7.4.3 LINE OVERFLOW DETECTED Command - This command is sent whenever the DATA AVAIL control bit is set (i.e., receiver data is available) but there is no buffer in which to store the data. The format for this command is given in Figure 3-15. The data is kept in the line unit registers so the user program can issue a new BUFFER DESCRIPTOR IN (Receive) command and the data will not be lost.

Figure 3-15 LINE OVERFLOW DETECTED Command

15					10	9	8	7					0	
UNUSED					1	Ø	Ø	RDY0	IEO	RQO	UNUSED	Ø	Ø	1	SEL2
UNUSED															SEL4
UNUSED															SEL6

3.3.8 Data Transfer Error Termination Procedures

The following section describes the commands issued by the IMP11-B when error conditions occur and buffers or Buffer Descriptor Lists are terminated by the IMP11-B.

3.3.8.1 IMP NOT READY Termination - When the IMP goes NOT READY, all transfer activity is terminated. This includes the current buffer, the active Buffer Descriptor List, and the waiting Buffer Descriptor List in both directions.

3.3.8.2 NON-EXISTENT MEMORY Termination - If the non-existent memory access occurred during a receive operation, only the affected item is terminated. The current buffer is terminated if the error occurs during data storage. Only the current Buffer Descriptor List is terminated if the error occurs during list entry manipulations. Transmit activity is not affected.

During transmit operations, all transmit operations are terminated. During actual data transfers, the current transmit buffer and active and waiting Buffer Descriptor Lists are terminated. If the error occurs during list manipulations, both the active and waiting transmit Buffer Descriptor Lists are terminated. Receive activity is not affected.

3.3.8.3 Additional Information - If only the current buffer is being terminated, reaching the end of the active Buffer Descriptor List will result in a termination status of '+1' regardless of the status of the terminated buffer.

Separate BUFFER OUT and BUFFER DESCRIPTOR OUT commands will be issued by the IMP11-B for each buffer and list terminated. For example, seven commands may be issued if the IMP NOT READY state occurs.

1. CONTROL OUT - IMP transition to NOT READY

2. BUFFER OUT Receive - current receive buffer

3. BUFFER DESCRIPTOR OUT Receive - active receive list

4. BUFFER DESCRIPTOR OUT Receive - waiting list

5. BUFFER DESCRIPTOR OUT Transmit - active list

6. BUFFER DESCRIPTOR OUT Transmit - waiting list

7. CONTROL OUT - IMP transition back to READY

NO BUFFER OUT Transmit command occurs when the
current transmit buffer is terminated. Statuses of
transmit and receive buffers beyond the current
buffer will not be updated if the active buffer
descriptor list is terminated. It is a good idea
for the user program to fill all status bytes with
'0' before passing them to the IMP11-B to help
identify such situations - especially on transmit
lists.

3.3.9 Loopback Mode

For special diagnostic testing, it is helpful to remove the
IMP11-B from the network and set up a cable to loop back all
transmitted data and control lines to the receive port. All
data will be echoed back correctly. The only change from
normal operation is the 1/2 second delay for HOST READY to
show up on the receive side as IMP READY. This is caused by
the hardware handling of the control relay switches. A
suitable delay must be placed in the user program if such
loop back operation is attempted.

CHAPTER 4

THEORY OF OPERATION

4.1   GENERAL FUNCTIONAL DESCRIPTION

The IMP11-B logic is made up of two parts, the KMC11-A micro
processor and the M8240 line unit. The KMC11-A acts primarily as
an NPR handler and line unit controller. The line unit's main
function is to provide level conversion for the interface and to
assemble/serialize 16 bit data.

Data from PDP11 memory is DMA'ED into the KMC11-A, the firmware
in the KMC11-A then moves it into two 8 bit registers in the line
unit, the line unit then shifts this 16 bit word out to the IMP
(serially).

Data from the IMP is received serially by the line unit, the data
is assembled into two 8 bit bytes in the line unit, the KMC11-A
upon detecting the availability of a 16 bit word moves the word
into the KMC11-A NPR out registers (two 8 bit bytes) and
generates an NPR cycle which moves the data into PDP11 memory.

4.1.1   Indicator Panel

The indicator panel serves two functions. It contains the LED
display of the IMP11-B status and it provides mounting hardware
for connecting the IMP device cable to the line unit.

The indicator panel provides the operator with a visual state of
the IMP11-B logic. It is made up of 14 LED indicators which are
driven from the line unit module by 7438 driver chips. The
indicator panel is connected to the M8240 module with a flat Berg
cable at J3. The operation of the IMP11-B is not dependant upon
the indicator panel, the IMP11-B can run with the cable
disconnected from J3.

The IMP is connected to the IMP11-B from the back side of the
indicator panel. A 'MASSBUS' type connector is provided for
connecting to the IMP device cable. This connector has pin out
for both local and distant logic. The massbus connector is
connected to the line unit module by two BC06R-08 flat cables

thru J1 and J2 of the M8240. See the prints (IMP11-B) for
connections. The cable from J1 contain both the local and
distant driver signals and the output of the HOST RDY relay. The
cable from J2 contain the receiver lines (both local and distant)
for the M8240. The directon of the signal flow is one way in
each of the cables.

4.2 KMC11-A MICRO PROCESSOR/NPR HANDLER

The KMC11-A is a unibus micro processor. It is connected to any
hex height SPC slot with the jumper in CA1 toCB1 removed (this is
to allow the KMC11-A to arbitrate NPR requests passing thru it.
The KMC11-A is used to control the line unit and to perform NPR
transfers to and from the unibus. The firmware or micro code is
loaded into the KMC11-A and started. See the KMC11-A manual of
loading and starting. Once this load has be completed, the
KMC11-A 's firmware will be invisable to the software. The
firmware will act very simular to random control logic. The
system software will pass commands and NPR information to the
KMC11-A and the KMC11-A will control the line unit and do the
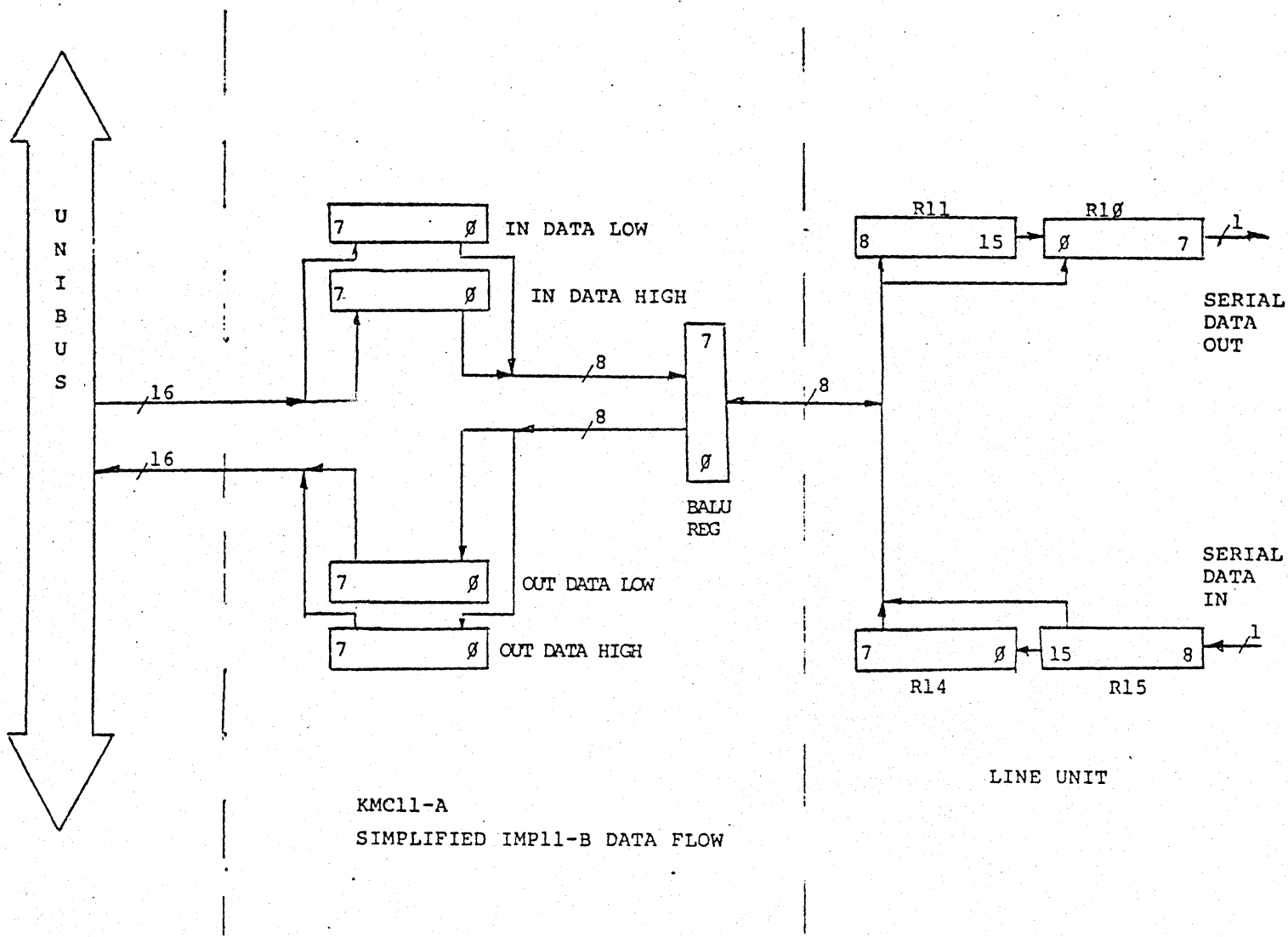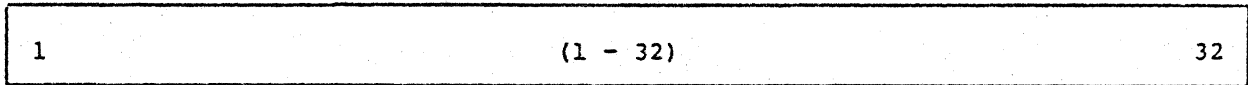necessary NPR cycles to store the data.

Figure 4-1   KMC11-A Simplified Block Diagram

IMP DATA FORMAT
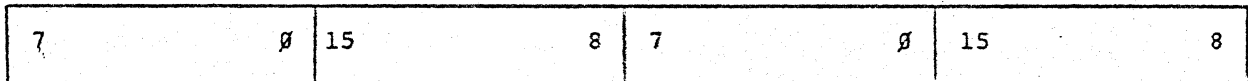
1	(1 - 32)	32

IMP11-B BYTES (8 BITS)

7	Ø	15	8	7	Ø	15	8

    BYTE 1   BYTE 2   BYTE 3   BYTE 4
        PDP11 WORD 1   PDP11 WORD 2

STARTING BIT   LAST BIT

IMP11-B/IMP DATA BIT MAP

Figure 4-2

LINE UNIT DATA OUT REGISTER

7	6	5	4	3	2	1	0	
		TX BUF 0						R10
		TX BUF 1						R11
			ENA LAST BIT			TX ERR CLR	TX CLR STATUS	R12
								R13
								R14
								R15
						HOST RDY.	RX CLR STATUS	R16
							GET IMP WORD	R17

LINE UNIT DATA IN REGISTER

7	6	5	4	3	2	1	0	
								R10
								R11
			ENA LAST BIT			TX ERR CLR	TX CLR STATUS	R12
			IMP NOT RDY			RFN IMP11 BIT	BUFFER EMPTY	R13
		RX BUF 0						R14
		RX BUF 1						R15
						HOST RDY.	RX CLR STATUS	R16
			IMP LINE ERROR			END OF MSG.	DATA AVAIL.	R17

Figure 4-3   IMP11-B/IMP Data Bit Map

4.2.1 Line Unit Control Registers

The KMC11-A controls the line unit thru 8 WRITE ONLY and 8 READ ONLY eight bit registers. In many cases, the information written is reflected back in the read registers. In other cases this is not so, the transmit data registers are write only. The registers are numbered R10 thru R17 for both write and read registers (data out and data out). This convention is used because the register field in the KMC11-A data I/O instruction is set up to define these registers as R10 to R17. See KMC11-A maintenance manual for the instruction format.

The following is a desciption of the line unit registers:

DATA OUT REGISTER (WRITE ONLY)

REG	NAME	FUNCTION
R10 (7-0)	TX BUF 0	This 8 bit register contains the low order byte of the 16 bit PDP11 word. Loading this register should only be done after buffer empty (read reg 13-bit 0) is set. It should be loaded before R11 (TX BUF 1) is loaded.
R11 (7-0)	TX BUF 1	This 8 bit register contains the high order byte of the 16 bit PDP11 word. It should be loaded only after the buffer empty flag has set. Loading this register clears the buffer empty flag and allows the line unit to start transmitting the data (assuming that the IMP is ready to accept the word.).
R12 (4)	ENA LAST	Enable last bit. This bit is used to enable the last bit logic. As soon as the current word being transferred has reached the 16th bit transfer the line unit will raise the last bit line during the 16th bit transfer. This bit is used to signal to the IMP that the last bit transferred is the last bit is the message. This bit is self clering. it should be set prior to loading R10 and R11 as the signal last bit will occur for the next R10 and R11 data.
R12 (1)	TX ERR CLR	This bit is write one/zero. Writing a a zero will clear the IMP line error bit (R17 bit 4 of the data in register) only if the IMP not rdy bit (R13-bit 4 of the data in register) is also cleared. IMP not RDY holds IMP line error set. This bit must be toggled. A one must be

written and then a zero.

R12 (0)	TX CLR STATUS	This bit is write one/zero. It is used to clear the transmit logic. It must be toggle to a one and then reset to a zero.
R16 (1)	HOST RDY	HOST READY. This bit is used by the firmware to put the interface on line. It effectively energizes a relay which the IMP monitors; a closed relay indicates that the IMP11-B or host is online. This bit is write one/zero. It is cleared also by set RX CLR status (R12-BIT 0)
R16 (0)	RX CLR STATUS	This bit is used to clear the receive logic it is write one/zero. It must be toggled to a one and then to a zero. If the bit is left set, it will freeze the receive logic in the reset state.
R17 (0)	GET IMP WORD	This bit is write one only. It is used to force the line unit logic to set the ready for IMP bit line there by requesting IMP data. This bit is required to be set each time to assemble a 16 bit word. The logic will automatically assemble the word as it receives the the data. Once the word is assembled, the data available bit (R17-bit 0 of the data in register) will set indicating that a word (IMP) is available for the KMC11-A to read.

DATA IN REGISTER

REG	NAME	FUNCTION
R10		Not Used
R11		Not Used
R12 (4)	ENA LAST BIT	This bit reflects the status of the enable last bit bit in the data out register.
R12 (1)	TX ERR CLR	This bit reflects the state of the TX ERR CLR bit in the data out register.
R12 (0)	TX CLR STATUS	This bit reflects the state of the TX CLR status bit in the data out registers.

R13 (4)	IMP NOT RDY	IMP not ready. This bit if set indicates that has released its relay and thus has gone off line. As soon as the IMP energizes his relay this bit will clear after a delay of 500 ms. this bit when set will set IMP line error (R17- bit 4 of the data in registers) and hold it set as long as IMP NOT RDY is set. Once IMP NOT RDY is cleared, then IMP line error may be cleared.
R13 (1)	RFN IMP11 BIT	This bit is set by the IMP requesting a data bit. This bit follows the IMP'S "READY FOR NEXT BIT" line .
R13 (0)	BUFFER EMPTY	This bit is used to indicate that the transmit buffer is empty and the next word to transmit may be loaded into TX BUF 0 and TX BUF 1. This bit is cleared as soon as TX BUF 1 is loaded and will set as soon as the 16 bit word loaded is accepted by the IMP. This bit is also set by TX CLR status on initializing.
R14	RX BUF 0	This register contains the low order byte of the received word from the IMP. The data in this register is not valid until the data avail bit in R17 is set. Reading this register has no effect on data avail.
R15	RX BUF 1	This register contains the high byte of the received word from the IMP. The word is not valid until the data avail flag (bit 0 in register 17 is set). Reading the contents of this register will cause the data avail flag to clear. The contents of this register is set to zeros when RX CLR status is toggled.
R16 (1)	HOST RDY	This bit is used to reflect the state of HOST RDY bit in the data out registers
R16 (0)	RX CLR STATUS	This bit is used to reflect the status of the RX CLR status bit in the data out registers.
R17 (4)	IMP LINE ERROR	IMP line error. This bit is used to indicate that the IMP NOT RDY bit has come set at one time or is still set. This bit will immediately set on the setting of the IMP NOT RDY line and stay set until cleared by toggling the TX ERR CLR bit in register R12. This bit will

not clear if IMP NOT RDY remains set. The IMP NOT rdy condition must first be removed.

R17   END OF MSG   This bit is set on the detection of the
(1)   the bit line coming true. This bit will
                           come true at the same time data avail
                           'able comes true even though the last
                           bit signal was detected in the middle of
                           the word. In loop back mode, the last
                           bit line will always be received during
                           the 16th bit time. This bit is cleared
                           by reading R15 or by toggling RX CLR
                           status.

R17   DATA AVAIL   Data AVAILABLE. This line is used to
(0)   flag the validity of the data in R14 and
                           R15. To initiate a receive cycle, it is
                           necessary for the firmware to write a
                           one into bit 0 of R17. This causes the
                           line unit to raise the "READY FOR NEXT
                           IMP BIT" line and there by starting a 16
                           bit serial transfer. Once 16 bits have
                           been assembled, the line unit will set
                           the data avail bit to indicate the
                           completion of a transfer.

4.3 LINE UNIT M8240

The M8240 line unit module is designed to work with a KMC11-A micro processor. It is connected to the KMC11-A with a one foot BC08S which is used to bus the KMC11-A output/input port to a line unit.

The line unit contains transmit logic and receive logic and is capable of supporting full duplex operation. The transmit logic is flag driven. A transfer cycle of one 16 bit word is started with the buffer empty bit being set (R13-bit 0) by either a reset or the completion of a previous transfer. The IMP processor will raise its ready for next bit line to indicate to the line unit that it is ready for data (RFN IMP11 bit true). The KMC11-A firmware on seeing that the buffer empty flop is set can initiate a 16 bit transfer. The KMC11-A, having retrieved a 16 bit word from PDP11 memory will move that data from the in NPR data registers (two 8 bit bytes) into the R10 and R11 data out registers (TX BUF 0 and TX BUF 1). The loading of R11, TX BUF 1, will initiate the actual transfer. Loading R11 clears the buffer empty bit and generates the signal there's your BIT. This first there's your IMP11 bit strobes the DATA into the imp. The IMP on receiving the data will drop its ready for next IMP11 bit. The IMP11-B (line unit) will then drop its there's your IMP11 bit. The IMP on seeing the dropping of the IMP11-B'S there's your bit will raise its ready for next IMP11 bit as soon as it is ready to

accept another data bit. This handshake continues until all 16
bits are accepted by the IMP. Once the 16 th bit is accepted,
the line unit will set its buffer empty bit for the KMC11. In
the meantime the KMC11-A has gone and done another NPR cycle
fetching another 16 bit word. This word is then used for the
second transfer. The transfers will be sustained until the
KMC11-A has exhausted its word count or encountered and error
condition (non existant memory.

The receive logic is initialized so that the line unit must
request a 16 bit word for the IMP. The KMC11-A upon having just
read a 16 bit word will have to initiate the transfer of another
16 bit word from the IMP. This is done by raising the ready for
next IMP bit line to the IMP. The KMC11-A on writing a one into
R17 bit 0, get IMP word, raises this line. The IMP on seeing
this line come true will send over the first data bit with
there's your IMP bit line true. The line unit will strobe this
data into the RX BUF register. The line unit having accepted the
data word will drop its ready for next IMP bit line and the IMP
will drop its there's your IMP bit line. This completes a bit
transfer. The line unit will then raise its ready for next bit
line to request another bit. the sequence continues until a 16
bit word has been assembled; after the 16th bit has been
received, the line unit will not raise its ready for next IMP bit
line. Instead, the line unit will set the data avail'able line
to indicate to the KMC11-A that a 16 bit word has been assembled
and is ready to read. The KMC11-A will then move the data from
RX BUF0 and RX BUF1 into the NPR out registers in the KMC11-A and
PERFORM and npr cycle to store the data in PDP11 memory. The
transfer of data from the IMP is continued until the receive word
count stored away by the firmware has overflowed or a termination
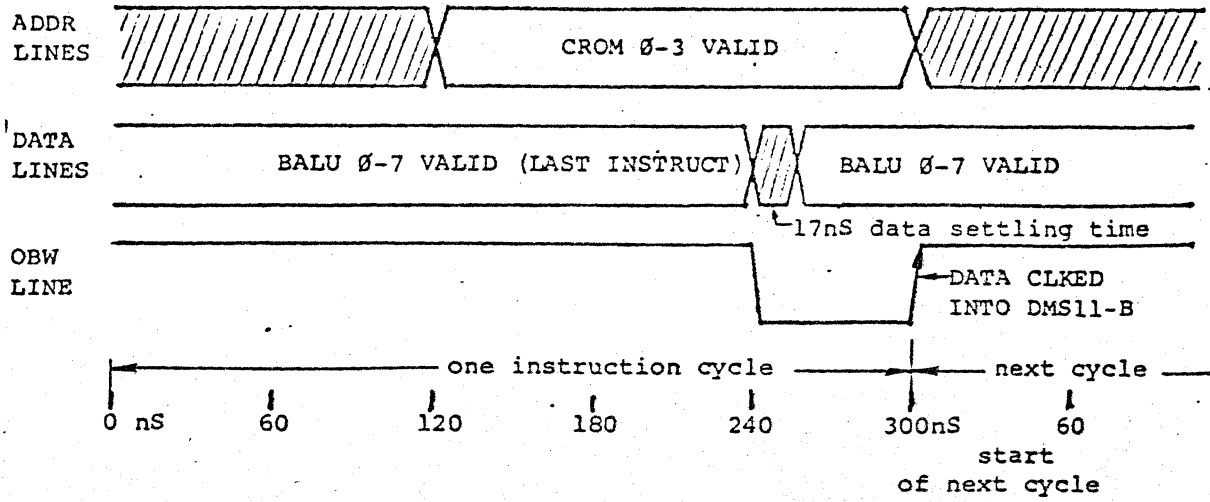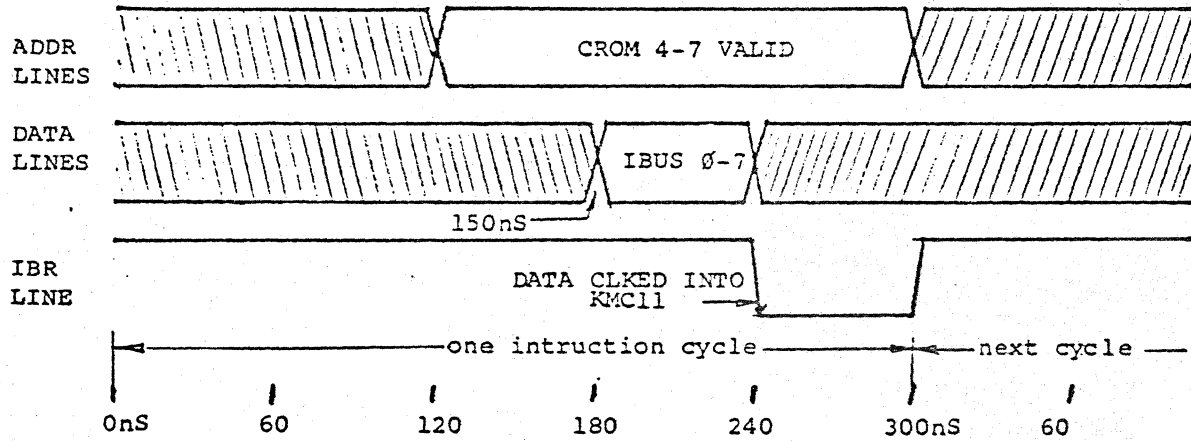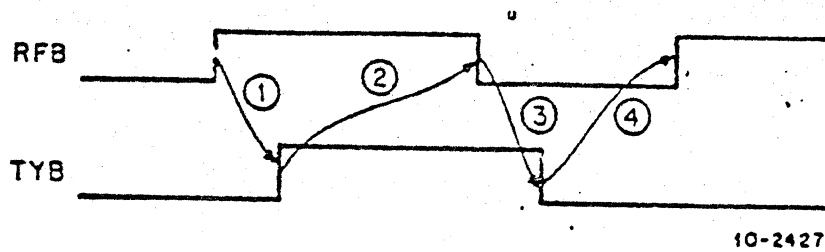condition is encountered (END OF MSG OR ERROR STATE).

Figure 4.2 KMC11-A OUTPUT TIMING

Figure 4-4   KMC11-A Input Timing

10-2427

RFB=READY FOR BIT
TYB=THERE'S YOUR BIT

Figure 4-5   Four Way Handshake

1.   RFB COMES TRUE TO REQUEST DATA.

2.   TYB COMES TRUE ONLY IF RFB IS TRUE.   TYB   STROBES   DATA
     WHEN IT IS TRUE.

3.   RFB CAN GO FALSE AFTER ACCEPTING THE DATA AND   WHEN   TYB
     IS TRUE.

4.   TYB CAN GO FALSE AFTER RFB GOES FALSE.   AFTER   TYB   GOES
     FALSE, THE NEXT REQUEST FOR DATA (RFB) CAN GO TRUE.

4.4 M8240 DRIVER AND RECEIVER LOGIC

The M8240 line unit contains a set of local interface
driver/receivers and a set of distant driver/receivers. The
local interface is used to connect to an IMP local host interface
and the distant interface is used to connect to a distant IMP
host interface. The local/distant set of driver/receivers
(interface) is selected by setting switch 1 on the switch pack on
the line unit. The switch is used to enable the desired set of
driver/receivers.   The local set of driver/receivers are capable
of driving up to a 25 foot cable. Consult the 1822 report by
BB&N for cable type.   The distant set of driver/receivers are
capable of driving up to 2000 ft. of cable (TWP).   Consult the
1822 report for cable type.

```
LOCAL DRIVER TYPE-        74128
LOCAL RECEIVER TYPE-      8T14

DISTANT DRIVER TYPE-      75112
DISTANT RECEIVER TYPE-    75107B
```

The length of the cable will adversely affect the transfer rate
due to propegation delays of the four way handshake. A good rule
of thumb to use for calculating the delay is to use 1 nanosecond
per foot of cable.

CHAPTER 5

MAINTENANCE

5.1 MAINTENANCE PHILOSOPHY

The IMP11-B should be diagnosed using the KMC11-A static
diagnostics and the IMP11-B static and dynamic diagnostics.
Failures should be isolated to a module (KMC11-A or line unit)
and the module should be replaced. Due to the multilayer and
dense boards used, field fixes may sometime do more harm (damage
to modules) than good, so it is recommended that the module be
swapped.

5.2 MAINTENANCE PLUG

A maintenance plug is supplied to allow jumping the input signals
to the output signals. In this way the diagnostics can verify
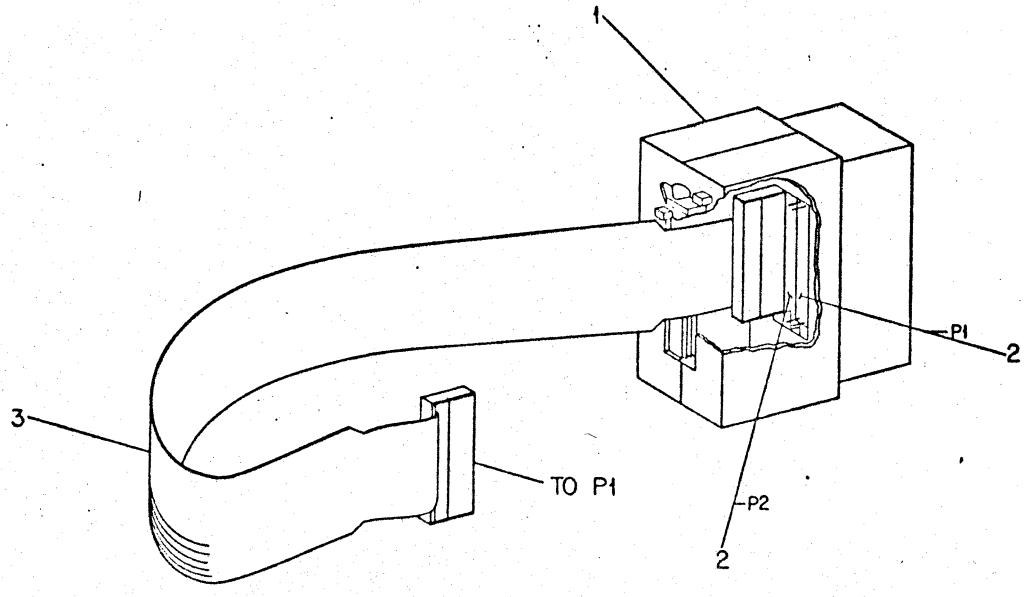correct operation of the two modules.

5.3 DIAGNOSTIC SOFTWARE

The are two IMP11-B diagnostics. The static diagnostic
(YM-Z078A-A) ensures that the logic is functional. The bits in
the line unit are tested through the KMC11-A. The dynamic
iagnostic (YM-Z078A-B) is a reliability diagnostic, which
exercises the IMP11-B by simulating on line operation. Refer to
the diagnostic listings for proper operation.

1	CABLE, BC085 I/O	BC085-01	3
2	PLUG TERMINATOR	121591-31	2
1	PLUG KIT, FLAT CABLE	121591-40	1
	DESCRIPTION	DWG PART NO	ITEM

MAINTENANCE PLUG

APPENDIX A

SHIPPING LIST

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
SHIPPING LIST

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	IMP11-B
1	M8204	KMC11-A uProcessor	1
2	M8240	1822 Line Unit Interface	1
3	YME059B	Indicator/Cable Panel	1
4	BC08R-01	KMC11-A to Line Unit Cable	1
5	BC06R-05	Flat Cable	3
6	YME067B	Maintenance Plug	1
7	1211591-40	Customer Cable Housing	1
8	1211591-31	Customer Cable Terminator	2
9	1210915-15	Customer Cable Connector	2
10	YMC078	Option Description *	1
11	MP00339	KMC11 Print Set *	1
12	M8240-0	M8240 Print Set	1
13	DECSPEC-11-DZ078A	IMP11-B Static Diagnostic & Listing *	1
14	DECSPEC-11-DZ078B	IMP11-B Dynamic Diagnostic & Listing*	1
15	MAINDEC-11-DZKCA	KMC11-A Diagnostic & Listing *	1
16	MAINDEC-11-DZKCC	KMC11-A Diagnostic & LIsting *	1
17	MAINDEC-11-DZKCD	KMC11-A Diagnostic & Listing *	1
	*NOTE: ONLY ONE SET WITH EACH SHIPMENT		

QUANTITY/VARIATION

TITLE	DOCUMENT NUMBER	REV.
IMP11-B 1822 INTERFACE	YMC078C	*

APPENDIX B

IMP11-A CABLING

IMP11-B
DEVICE CABLE WIRING
(LOCAL AND DISTANT HOST)

IMP - IMP11-B DIFFERENTIAL CABLE WIRING LIST

	PIN		SIGNAL NAME
CABLE 1	P1-1	DIF	TY IMP11 BIT H (+)
	P1-2	DIF	TY IMP11 BIT L (-)
	P1-6	DIF	IMP11 DATA BIT H (+)
	P1-7	DIF	IMP11 DATA BIT L (-)
	P1-11	DIF	LAST IMP11 BIT H (+)
	P1-12	DIF	LAST IMP11 BIT L (-)
	P1-16	DIF	RFN IMP BIT H (+)
	P1-17	DIF	RFN IMP BIT L (-)
	P1-21		IMP11 MASTER RDY L
	P1-22		IMP11 READY TEST L
	P1-24		SPARE
	P1-25		SPARE
	P1-3		SHIELD
	P2-1	DIF	TY IMP BIT H (+)
	P2-2	DIF	TY IMP BIT L (-)
	P2-6	DIF	IMP DATA BIT H (+)
	P2-7	DIF	IMP DATA BIT L (-)
	P2-11	DIF	LAST IMP BIT H (+)
	P2-12	DIF	LAST IMP BIT L (-)
	P2-16	DIF	RFN IMP11 BIT H (+)
	P2-17	DIF	RFN IMP11 BIT L (-)
	P2-21		IMP MASTER RDY L
	P2-22		IMP READY TEST L
	P2-24		SPARE
	P2-25		SPARE
	P2-3		SHIELD

IMP - IMP11-B LOCAL CABLE WIRING LIST

	PIN		SIGNAL NAME
CABLE 2	P1-4	LOCAL	TY IMP11 BIT H
	P1-5		RTN
	P1-9	LOCAL	IMP11 DATA BIT H
	P1-10		RTN
	P1-14	LOCAL	LAST IMP11 BIT H
	P1-15		RTN
	P1-19	LOCAL	RFN IMP BIT H
	P1-20		RTN
	P1-21		IMP11 MASTER RDY L
	P1-22		IMP11 READY TEST L
	P1-24		SPARE
	P1-25		SPARE
	P1-3		SHIELD
	P2-4	LOCAL	TY IMP BIT H
	P2-5		RTN
	P2-9	LOCAL	IMP DATA BIT H
	P2-10		RTN
	P2-14	LOCAL	LAST IMP BIT H
	P2-15		RTN

P2-19	LOCAL	RFN IMP11 BIT H
P2-20		RTN
P2-21		IMP MASTER RDY L
P2-22		IMP READY TEST L
P2-24		SPARE
P2-25		SPARE
P2-3		SHIELD

Figure B-1

IMP-IMP11-B DIFFERENTIAL CABLE WIRING LIST

PIN	SIGNAL NAME	PIN	SIGNAL NAME
P1-1	DIF TY IMP11 BIT H (+)	P2-1	DIF TY IMP BIT H (+)
-2	DIF TY IMP11 BIT L (-)	-2	DIF TY IMP BIT L (-)
-6	DIF IMP11 DATA BIT H (+)	-6	DIF IMP DATA BIT H (+)
-7	DIF IMP11 DATA BIT L (-)	-7	DIF IMP DATA BIT L (-)
-11	DIF LAST IMP11 BIT H (+)	-11	DIF LAST IMP BIT H (+)
-12	DIF LAST IMP11 BIT L (-)	-12	DIF LAST IMP BIT L (-)
-16	DIF REN IMP11 BIT H (+)	-16	DIF REN IMP11 BIT H (+)
-17	DIF REN IMP11 BIT L (-)	-17	DIF REN IMP BIT L (-)
-21	IMP MASTER RDY L	-21	IMP MASTER RDY L
-22	IMP READY TEST L	-22	IMP READY TEST L
-24	SPARE	-24	SPARE
-25	SPARE	-25	SPARE
P1-3	SHIELD	P2-3	SHIELD

IMP IMP11 B LOCAL CABLE WIRING LIST

PIN	SIGNAL NAME	PIN	SIGNAL NAME
P1-4	LOCAL TY IMP11 BIT H	P2-4	LOCAL TY IMP BIT H
-5	RTN	-5	RTN
-9	LOCAL IMP11 DATA BIT H	-9	LOCAL IMP DATA BIT H
-10	RTN	-10	RTN
-14	LOCAL LAST IMP11 BIT H	-14	LOCAL LAST IMP BIT H
-15	RTN	-15	RTN
-19	LOCAL REN IMP11 BIT H	-19	LOCAL REN IMP11 BIT H
-20	RTN	-20	RTN
-21	IMP11 MASTER READY L	-21	IMP MASTER RDY L
-22	IMP READY TEST L	-22	IMP READY TEST L
-24	SPARE	-24	SPARE
-25	SPARE	-25	SPARE
-3	SHIELD	P2-3	SHIELD

3
—P2
—TO ITEM 2-P2

TO IMP11-B
PANEL:

PIN 2   PIN 1

TO IMP NODE

—P1

—TO ITEM 2-P1
—P1
3

PIN 40
PIN 39

—P1

—2

—P2

2

THIS CABLE FOR REFERENCE ONLY

NOTES

1. The plug housing, shell, plug modules, crimp pins, and hardware for one cable are supplied.

2. The plug housing (DEC PN 12-11591-02) and CAM are specially made DEC parts; only DEC parts should be used with the IMP11-B connector panel.

3. The inserts (PLUG MODULES) are standard AMP parts as well as the contact pins. See AMP guide.

4. Other types of PLUG MODULES that have square post pins instead of Crimp type pins are available.

5. Use AMP tool # 90309-1 (or equivalent) to crimp PLUG MODULE crimp pins.

6. Local cable should be shielded 12TWP 24 AWG.

7. Distant cable should be shielded 12TWP 20 AWG 110 xxx cable. Use 24 AWG TWP patch cable to connect IMP11-B to distant cable.

8. Consult BBN 1822 report for more on cable material requirements.

9. Maximum length of the Local cable should be no more than thirty (30) feet.

APPENDIX C

SAMPLE IMP11-B FIRMWARE LOAD ROUTINE

```
INIMPB: MOV     #FIRM,R1            ;SET FIRMWARE POINTER
        CLR     2$                 ;SET ADDRESS TO 0
        CLR     @SEL0
        MOV     #40000,@SEL0       ;CLEAR
        NOP
        CLR     @SEL0              ;RESET CLEAR
1$:     MOV     2$,@SEL4           ;LOAD ADDRESS
        BIS     #2000,@SEL0        ;L. A.
        MOV     (R1)+,@SEL6        ;LOAD DATA
        BIS     #20000,@SEL0       ;TOGGLE CRAM WRITE
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        NOP
        BIC     #22000,@SEL0
        INC     2$                 ;BUMP ADDRESS
        CMP     2$,#2000           ;DONE?
        BNE     1$                 ;NO
        BR      INTKMC             ;SKIP
2$:     0

INTKMC: MOV     #15,3$             ;INITIALIZE THE FIRMWARE
        CLR     @SEL0
        MOVB    #277,@BSEL2        ;THIS SHOULD BE CLEARED BY THE FIRMWARE
        MOV     #4000,@SEL0        ;SET MASTER CLEAR
        MOV     #100000,@SEL0      ;SET RUN
        CLR     4$
1$:     INCB    4$                 ;WAIT LOOP
        BNE     1$
        TSIB    @BSEL2             ;DONE?
        BEQ     2$                 ;YES
        DEC     3$                 ;NO
        BNE     1$
        ERR                        ;ERROR
        EMSG3                      ;KMC11 FIRMWARE IS HUNG (LOAD ERROR)
```

```
         BR    INTKMC              ;TRY AGAIN
2$:      RTS   PC                  ;EXIT
3$:      0
4$:      0
```

#FIRM - First Location of firmware buffer.

SEL0 = Location contains KMC11-A SEL0 address.

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