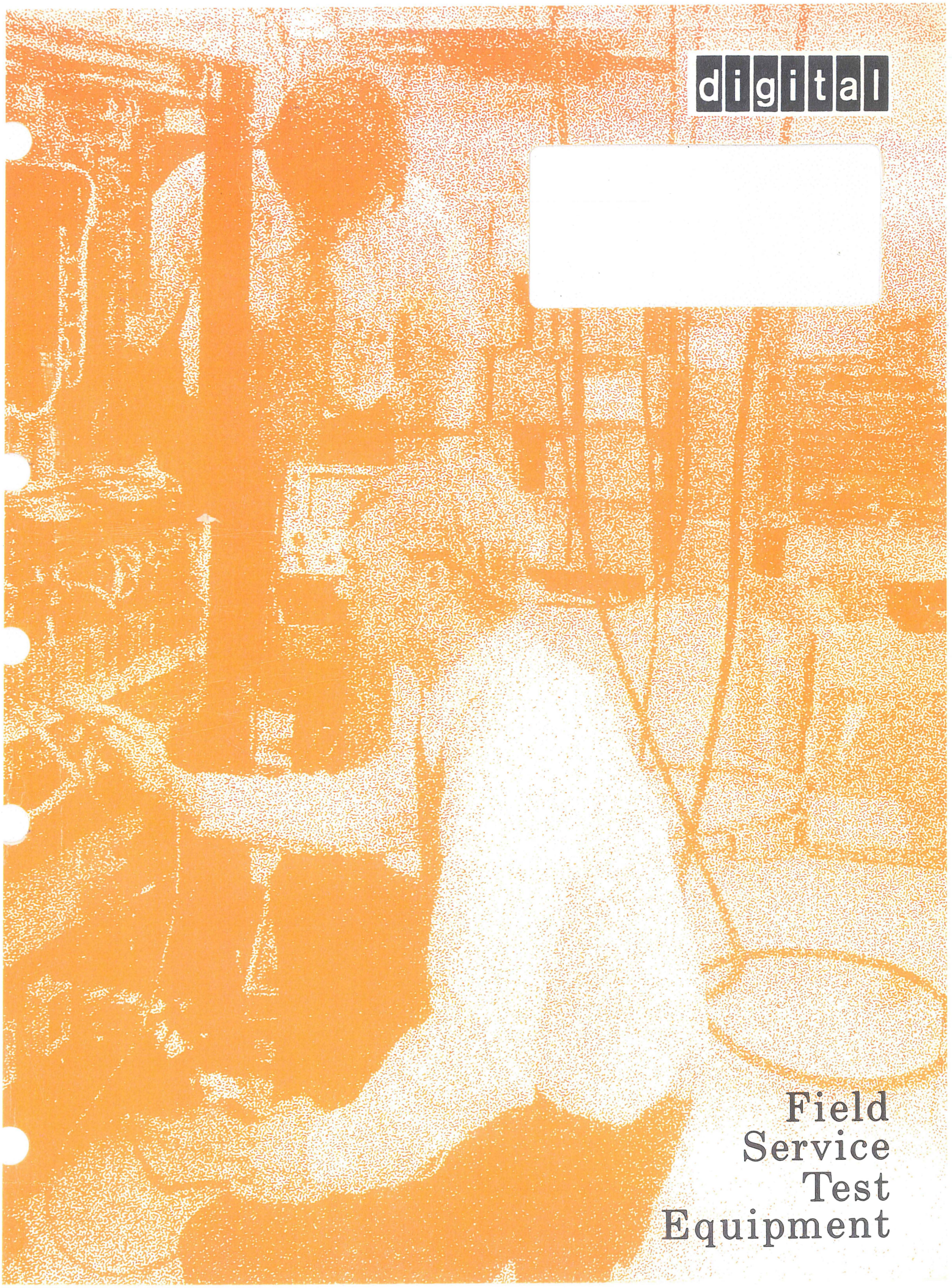

digital

Field Service Test Equipment

Unibus Troubleshooting user's manual

EK-FS002-OP-001

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CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

FIGURES

FIGURES (Cont)

TABLES

PREFACE

This user's manual is a detailed troubleshooting and reference guide for isolating Unibus problems related to (a) systems which are inoperative and (b) systems which are marginal.

Due to the complexities and terminology associated with the Unibus, this manual also contains descriptions, definitions and reference material relative to the Unibus and associated hardware.

NOTE

This manual does not define the optimum system configurations for throughput or latency tolerence which may be dependent on customer usage and applications environment.

This manual supersedes Unibus Margin Tester user's guide, document number EK-FS002-OP-PRE.

NOTE

The M9308 Margin Heads are direct replacements for the M9303 Margin Heads. However, the M9308 allows for greater margining voltage (2.93 to 7.85 V) than the M9303 (4.2 to 7.0 V).

CHAPTER 1
INTRODUCTION

1.1 SYSTEM OVERVIEW

Most of the PDP-11's internal electronic components and system peripherals are connected to and communicate with each other through the Unibus. There are 56 lines on the bus that handle such signals as address, data and control information. Each device, including memory locations and peripheral device registers, is assigned one address on the Unibus.

NOTE

This manual is intended for use by authorized DIGITAL EQUIPMENT CORPORATION personnel only. Information contained in this manual is neither intended to be a product specification nor to supersede or replace any other published information that is available to customers or users of DIGITAL products.

Some PDP-11 system configurations experience permanent and intermittent bus failures due to improper signal termination and loading techniques. (These problems can exist even when the proper guidelines and rules for system configurations are followed.) This manual will assist in the proper procedures for isolating configuration and Unibus problems, and corrective action that can be implemented for better system operation.

Due to complexity of system configuration and operation, all Unibus systems are subject to additional electrical and mechanical factors which may become even more relevant when, and if, these factors interact. If this interaction becomes large enough, it can cause false signal levels that can seriously effect system operation. Some of the signal conditions that can occur because of these additional electrical and mechanical factors follow.

1. Signal caused by dc loading of receivers and drivers
2. Signal loss caused by nonzero resistance of BC11 jumper cable
3. Signal loss caused by connector contact resistance
4. Standing wave reflections from devices on the line
5. Increased propagation delay caused by devices on the line and high frequency cable losses
6. Crosstalk on bus lines caused by the cable or by devices attached to the bus
7. Signal skew caused by multiple high-frequency loading on different lines by a device

1.2 UNIBUS TROUBLESHOOTING TECHNIQUES

Currently, there are three troubleshooting aids that can be used to troubleshoot and isolate Unibus problems.

1. Hi/Lo Terminator Margin Cards
2. Unibus Voltage Margin Tester Box
3. Single-Ended Margining Technique

A fourth troubleshooting aid is the flowchart (refer to Chapter 3) which is organized into a general flow and reference diagram which points out particular sections that contain troubleshooting techniques and supportive information. The supportive information will aid in the understanding of, and provide background for, the use of the Unibus Troubleshooting techniques outlined in Chapter 3 of this manual.

1.3 HI/LO TERMINATOR MARGIN CARDS

The Hi/Lo Terminator Margin Cards are used to replace the M930 bus terminator in the PDP-11 system for margining purposes. The Hi/Lo Terminator Cards are used as a go/no go test and are not to be installed in the system on a permanent basis. (Refer to Chapter 4 for additional operational procedures and descriptions.)

1.4 UNIBUS VOLTAGE MARGIN TESTER BOX

The Unibus Voltage Margin Tester Box is designed to test Unibus driver and receiver terminating networks for the PDP-11 system. The tester is connected to the Unibus through special terminator cards called margining heads. When the tester is cabled to the Unibus, the operator can select which signal(s) (single, groups, or all) is to be tested. (Refer to Chapter 4 for additional operational procedures and descriptions.)

1.5 SINGLE-ENDED MARGINING TECHNIQUE

For some PDP-11 processors (e.g., PDP-11/04 and PDP-11/34), it is not possible to use the M930 margining heads with the Unibus Voltage Margin Tester Box. This is due to additional hardware on the terminator module (boot strap function, sack turnaround, etc.) which must be present in order for the processor to operate normally. It is for these processors that the Unibus Tester Box single-ended margining technique has been developed. However, this technique can be used with any Unibus processor. (Refer to Chapter 4 for additional operational procedures and techniques.)

CHAPTER 2
UNIBUS CONFIGURATION

2.1 GENERAL

After the Unibus option configuration (based on NPR latency, physical location, etc.) is determined, these options must be interconnected using the correct procedure and techniques.

The definitions, rules and guidelines outlined in this section are designed to aid you in configuring an electrically reliable Unibus. *These rules and guidelines are intended for new systems and are not to be considered as a justification for any changes in existing systems, unless Unibus related problems are encountered and cannot be resolved in any other way.*

The configuration rules (Paragraph 2.3) ensure, with reasonable confidence, that Unibus segments will be electrically reliable, i.e., resulting dc bus levels will guarantee an adequate noise margin, and reflections from lumped loads will not be excessive.

To configure a Unibus system, the required order of options on the Unibus, based on NPR latency, physical location, etc., should first be determined. The rules will then determine the length the Unibus cable interconnecting the options and the number and location of bus repeaters. If the number of bus repeaters is excessive, total cable length can sometimes be reduced by rearranging the order of options on the bus (again, paying close attention to NPR latency, etc.). Then, after reapplying the rules in this guide, one or more bus repeaters may be eliminated or located further down the bus to optimize system speed. For large systems, more than one pass of this procedure may be necessary to achieve satisfactory results.

A reasonable effort should always be made to ensure total cable length is as short as possible, particularly if one or more bus repeaters can be eliminated in the process. Bus repeaters are costly and slow down the system. Before implementing configuration rules, the user should carefully read and understand the definitions that follow.

2.2 UNIBUS DEFINITIONS

Prior to configuring the Unibus, review the definitions outlined in Paragraphs 2.2.1 through 2.2.10.

2.2.1 Bus Segment

The Bus Segment is defined as that portion of a Unibus system between and including two terminators. A bus segment consists of: a terminator, a 120 ohm transmission path (cable) with options containing drivers and receivers attached to it, and another terminator in that order. A single bus system is one which has one bus segment. A multiple bus system is one which has more than one bus segment, usually separated by bus repeaters (DB11s) or bus switches (DT03s – which contain bus repeaters).

2.2.2 Bus Cable

A Bus Cable is defined as cable connecting two backplanes which acts as a 120 ohm transmission line with a length of two feet or more. A BC11A cable is defined to be both a cable and a bus element. For our purposes, the cable is a subset of the bus element and should be treated as such. The following bus elements are Unibus cables:

BC11A-2	2-foot Unibus cable (60.96 cm)
BC11A-3	3-foot Unibus cable (91.44 cm)
BC11A-5	5-foot Unibus cable (1.52 m)
BC11A-6	6-foot Unibus cable (1.82 m)
BC11A-8F	8.5-foot Unibus cable (2.59 m)
BC11A-10	10-foot Unibus cable (3.04 m)
BC11A-15	15-foot Unibus cable (4.57 m)
BC11A-20	20-foot Unibus cable (6.07 m)
BC11A-25	25-foot Unibus cable (8.60 m)
BC11A-30	30-foot Unibus cable (9.14 m)
M9202	24-inch folded Unibus cable (60.96 m)

The M9202 is considered to be a cable (for the purposes of this manual) because it contains 2 feet of 120 ohm cable.

2.2.3 Bus Element

A Bus Element is defined as any module, backplane, cable or group of these items that has a common designation which has a direct electrical connection to one or more Unibus signal lines (other than AC LO L or DC LO L). For example, an M930 terminator, an M7821 module, a BB11 backplane, a BC11 cable, and an RK11 controller are Unibus elements. An H720 power supply, an LA36 DECwriter and a BA11 expander box are not Unibus elements.

2.2.4 Lumped Load

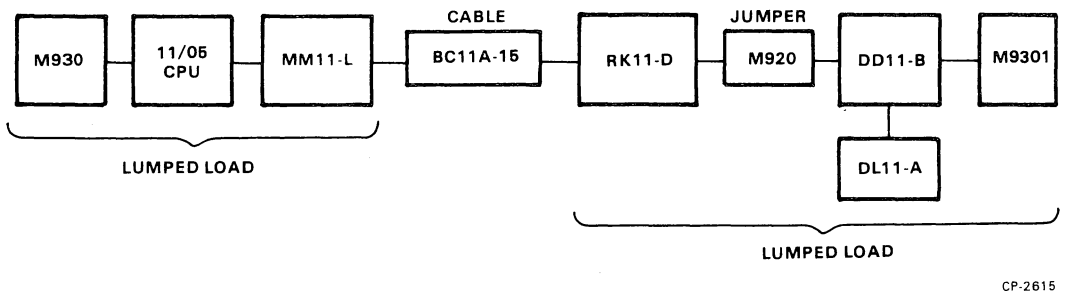
A Lumped Load is defined as a group of Unibus elements, other than cables or jumpers, which are interconnected via Unibus jumpers and direct wiring (backplane wire, PC etch) only. The group is not a lumped load if it uses a Unibus cable to interconnect the Unibus elements or if the elements are separated by a bus repeater. (Be certain the difference between "jumper" and "cable" is understood – see Figures 2-1 and 2-2.)

2.2.5 Bus Jumper

A Bus Jumper is defined as a Unibus element connecting two backplanes which contains less than two feet of cable. The following elements are Unibus jumpers:

M920	jumper
M9200	jumper with boards 1.27 cm (0.5 in) apart
M981	jumper/terminator
BC11A-0	6-inch cable (15.24 cm)

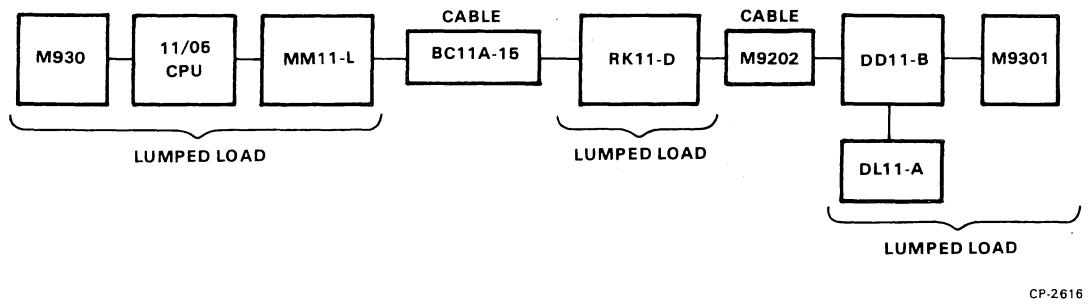
The BC11A-0 is considered to be a jumper (for the purposes of this manual) because it contains less than 60.96 cm (2 feet) of 120 ohm cable.



In this system, there are two lumped loads:

1. M930, 11/05 CPU, and MM11-L
2. RK11-D, DD11-B, DL11-A,and M9301

Suppose the M920 is replaced by an M9202:

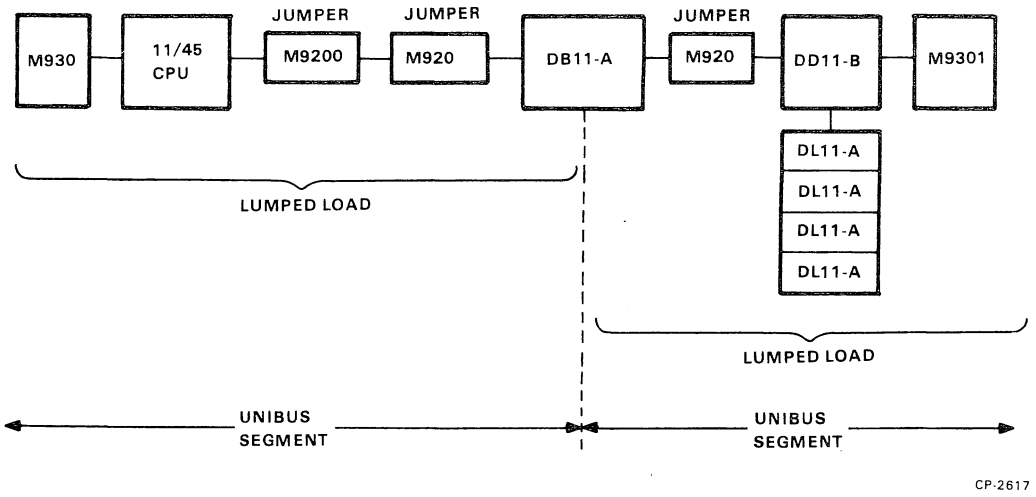


Now there are three lumped loads:

1. M930, 11/05 CPU, and MM11-D
2. RK11-D

DD11-B, DL11-A, and M9301

Figure 2-1 Lumped Loads (Example A)



This system has two Unibus segments separated by a bus repeater, so the system has two lumped loads:

1. M930, 11/45 CPU, DB11-A (left side)
2. DB11-A (right side), DD11-B, four DL11-As, M9301

NOTE
These examples are for illustrative purposes only and do not represent practical configurations.

Figure 2-2 Lumped Loads (Example B)

2.2.6 Bus Terminator

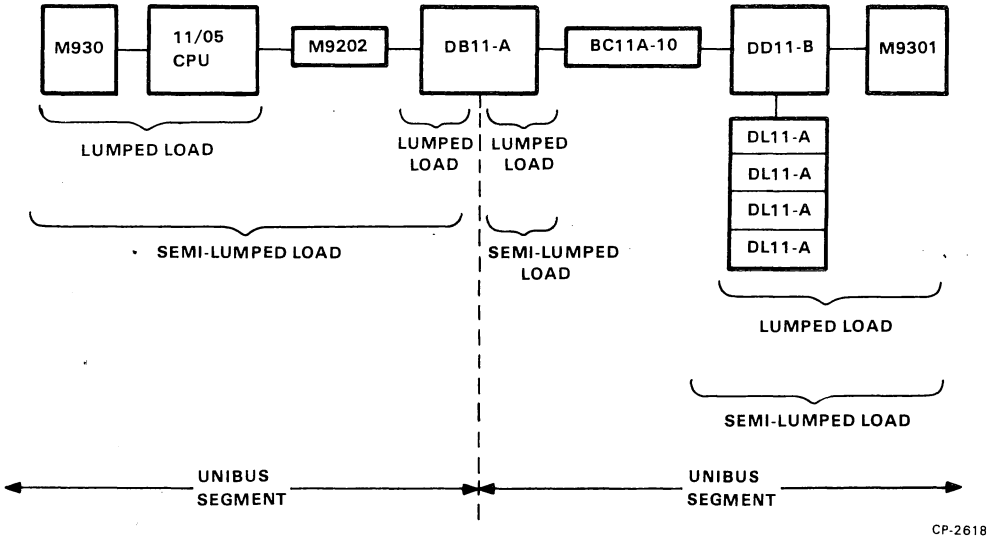
A Bus Terminator is defined as a Unibus element or part of an element containing a resistive network which connects to the end of a Unibus segment and matches the 120 ohm characteristic impedance of the Unibus transmission path. The M930 and M9306 are Unibus terminators if they connect to the Unibus. The following bus elements *contain* Unibus terminators:

M981	jumper/terminator
M9300	Unibus B terminator (M930 + NPR logic)
M9301	bootstrap/terminator
M9302	M930 with SACK return
DT03	bus switch
DB11-A	bus repeater
PDP-11/04	CPU (NOTE: other CPUs also contain terminators)

A Unibus segment must always have a Unibus terminator at each end of its 120 ohm transmission path.

2.2.7 Semi-Lumped Load

A semi-lumped load is defined as a group of lumped loads interconnected by 91.44 cm (3 ft) or less of cable (M9202, BC11-2 or BC11-3) and not separated by a bus repeater. Refer to Figure 2-3.



This system has two Unibus segments, with a total of four lumped loads and three semi-lumped loads.

Lumped loads:

1. M930, 11/45 CPU
2. DB11-A (left side)
3. DB11-A (right side)
4. DD11-B, four DL11s, M9301

Semi-lumped loads:

1. M930, 11/45 CPU, DB11-A (left side)
2. DB11-A (right side)
3. DD11-B, four DL11s, M9301

Figure 2-3 Semi-Lumped Loads (Example C)

2.2.8 AC Unit Load

An ac unit load is defined as a number related to the impedance that a Unibus element presents to a Unibus signal line (due to backplane wiring, PC etch runs, receiver input loading, and driver output loading). This impedance load on a transmission line causes a "reflection" to occur when a step is sent down the line. This reflection shows up on an oscilloscope as a spike occurring shortly after asserting or unasserting edge. An ac unit load is nominally 9.35 pF of capacitance. Nine lumped ac loads reflect 20 percent and 20 lumped ac loads reflect 40 percent of a 25 ns risetime step. AC loads must be distributed on the Unibus in the manner described by the rules in this manual in order to provide bus operation with reflections guaranteed to be at or less than a tolerable level.

The ac unit load rating of Unibus elements is usually based on the greatest of the capacitances that the element presents to the BBSY, SSYN, and MSYN Unibus signal lines. Appendix C contains the ac loading specifications of the Unibus elements. If the element is customer-designed, its ac unit loading must be determined from a reasonable estimate of the equivalent capacitance presented to the Unibus.

2.2.9 DC Unit Load

A dc unit load is defined as a number related to the amount of dc leakage current that a Unibus element presents to a Unibus signal line which is high (undriven). A dc unit load is nominally 105 μA (80 μA – receiver plus 25 μA – driver). However, the dc unit load rating of a bus element is not strictly based on the element's signal line that has the greatest leakage, (e.g., dc leakage is less important on D lines than it is on SSYN). The dc unit loading of an element should always be obtained from the specification for that element (see Appendix D). It should not be obtained from a calculation of the receiver and driver leakage current, unless the element is custom-designed and is not listed in the applicable documentation.

2.2.10 Unibus Length and Loading

The Unibus is a transmission line on which data transfers are asynchronous and interlocked. Significant electrical delay affecting system operation may, therefore, be imposed through unnecessarily long Unibus cables.

With ribbon cable the maximum length is 15.24 m (50 ft). For proper operation, the length of taps or stubs must be minimized. The Unibus signals should have receivers and transmitters in one place (near the Unibus cable) to act as a buffer between the Unibus and the signal lines carrying Unibus signals within the equipment. The maximum length of ribbon cable is obtainable only if the individual tap lengths are less than 5.08 cm (2 in), including printed circuit etches and if the loading is not more than one standard bus load. One bus load is defined as one transmitter and one receiver (see Figure 2-4).

The Unibus is limited to a maximum of 20 bus loads. This limit is set to maintain a sufficient noise margin. For more than 20 bus loads, a Unibus repeater option (DB11-A) is used.

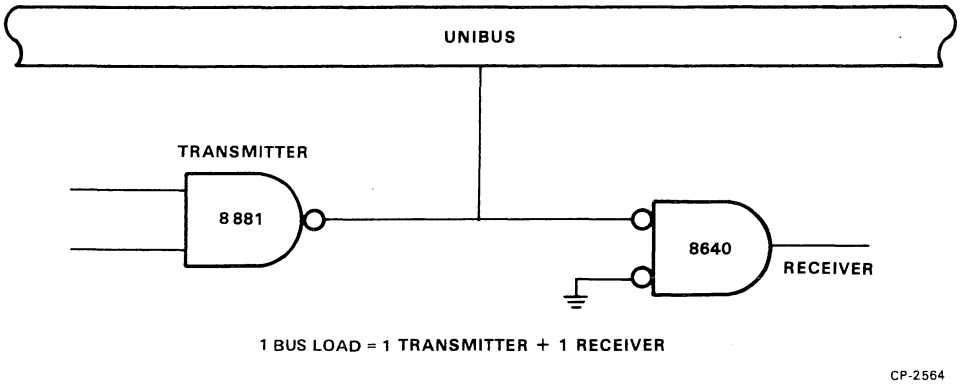


Figure 2-4 Bus Load Example

2.3 UNIBUS CONFIGURATION RULES

The following rules and guidelines are intended to be used for new systems and/or existing systems that experience Unibus problems. The seven rules are listed below for quick reference. A more detailed description, comments, and suggestions are described in the following paragraphs.

Rule No. 1 (Maximum cable length) – The total length of Unibus cable in a Unibus segment should not exceed 15.24 m (50 ft).

Rule No. 2 (Maximum dc loading) – The total number of dc unit loads on a Unibus signal line should not exceed 20. (See Appendix D.)

Rule No. 3 (Maximum lumped loading) – No lumped load on a Unibus segment should contain more than 20 ac unit loads unless the entire segment consists of one lumped load.

Rule No. 4 (Skewed cable lengths) – If (a) a lumped load (called the "affected lumped load") has 2.59 m (8.5 ft) or longer cables connected to both bus in and bus out and (b) the sum of the ac unit loads in the two *lumped loads* connected to the opposite ends of the cables exceeds 18, or (c) the sum of the ac unit loads in the two semi-lumped loads connected to the opposite ends of the cables exceeds 36, then the lengths of these cables should differ by 1.52 m (5 ft) or more with the longer cable being on the end with the greatest number of ac unit loads (if there is a practical choice).

Rule No. 5 (Skewed cable lengths, supplement) – If the length of one of the cables connected to the affected lumped load in Rule No. 4 must be increased because of that rule, then the longer cable should have at its opposite end of the semi-lumped load with the greater number of ac unit loads. This rule should be implemented only if it is practical to do so, i.e, in cases where its implementation will not increase total cable length more than 1.52 m (5 ft).

Rule No. 6 (Violation of Rules No. 1 through No. 5) – Rules No. 1 through No. 5 should not be grossly violated. If a bus segment violates a rule slightly, and for practical reasons reconfiguring is undesirable, then the segment *must* pass voltage-margin tests (a) when the system is originally configured and (b) when any Unibus element is added, deleted, or swapped (including the swapping of a defective module or backplane).

Rule No. 7 (System acceptance) – Even if rules No. 1 through No. 5 are implemented, all Unibus segments of a system should be voltage margined after the system is configured.

2.3.1 Maximum Cable Length (Rule No. 1)

If Rule No. 1 is violated, (a) the dc drop across the bus, when driven at one end and received at the other, may be excessive, and (b) far-end crosstalk may be excessive. In calculating lengths, the M920 should be considered as zero feet, the M9202 as 60.96 cm (2 ft), and the BC11A-0 as 15.24 cm (6 in).

If the length of a segment exceeds 15.24 m (50 ft), reconfiguring (changing the order of bus elements) may reduce the length. If that fails, a DB11-A bus repeater will be necessary.

2.3.2 Maximum dc Loading (Rule No. 2)

If too many dc loads are put on a Unibus segment, the quiescent undriven voltage may be lowered to a level where bus receivers become susceptible to reflections from lumped loads and the overall noise margin on the high end (bus undriven) may become too small. DB11 bus repeaters should be used (as required) to implement this rule.

2.3.3 Maximum Lumped Loading (Rule No. 3)

If a lumped load is too large, it may generate a reflection on the Unibus large enough to create a false logic signal and cause a failure (see Figures 2-5 and 2-6). M9202 folded cables (or BC11A-2s, if M9202 is unavailable) should be used in place of M920s in order to separate large lumped loads. The effect of the M9202 is to cause the peak reflections from the lumped loads it separates to occur at slightly different times. The following examples (see Figures 2-7 and 2-8) illustrate implementation of Rule No. 3.

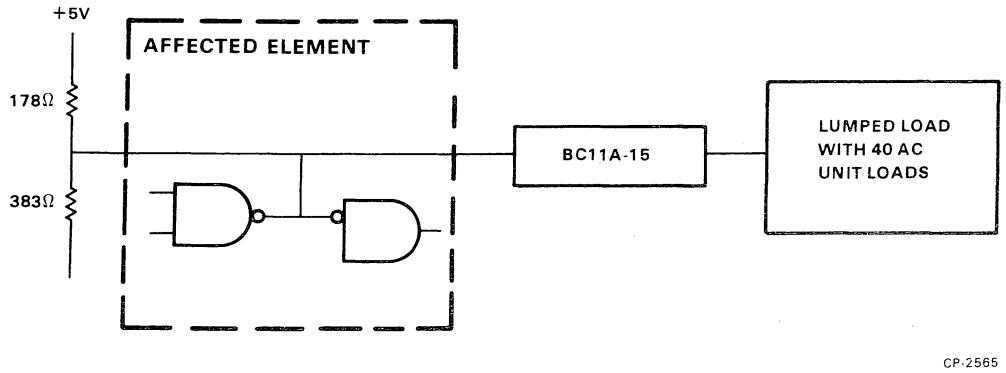


Figure 2-5 Rule No. 3 Violation (Block Diagram)

The system shown in Figure 2-5 violates Rule No. 3. When the driver in the affected bus element unasserts the bus, the receiver in that element will see the following waveform:

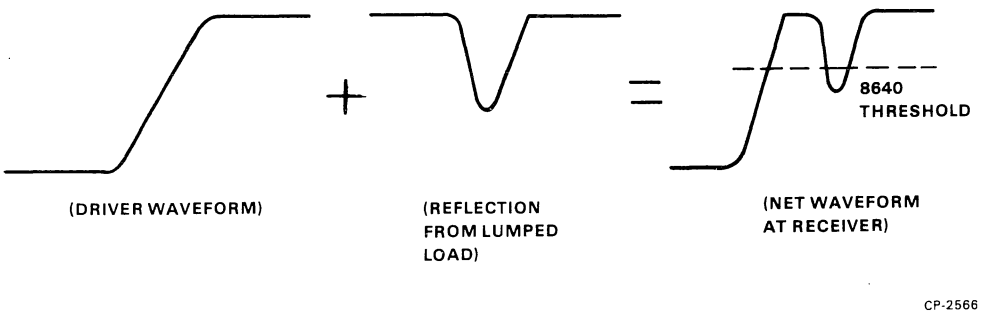


Figure 2-6 Rule No. 3 Violation (Waveform Example)

The reflection may cause the threshold of the 8640 receiver to be crossed a second time, and a failure may result. To implement Rule No. 3, the lumped load must be split into two equal loads by adding an M9202 in place of an M920 (see Figure 2-7).

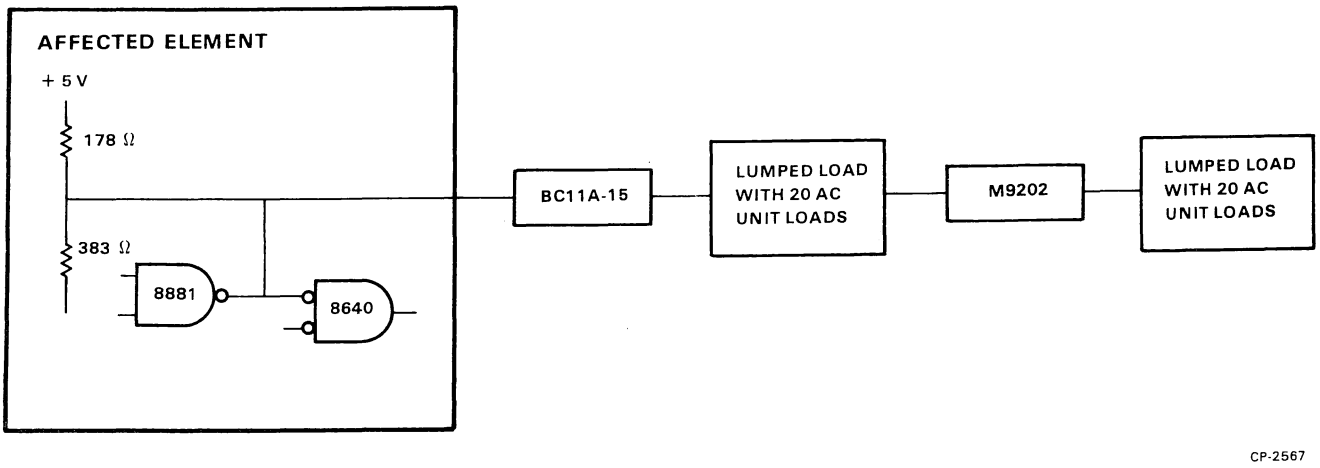


Figure 2-7 Rule No. 3 Implementation (Block Diagram)

The conditions to satisfy Rule No. 3 are now implemented. When the driver in the affected bus element unasserts the bus, the receiver in that element will see the following waveform (Figure 2-8).

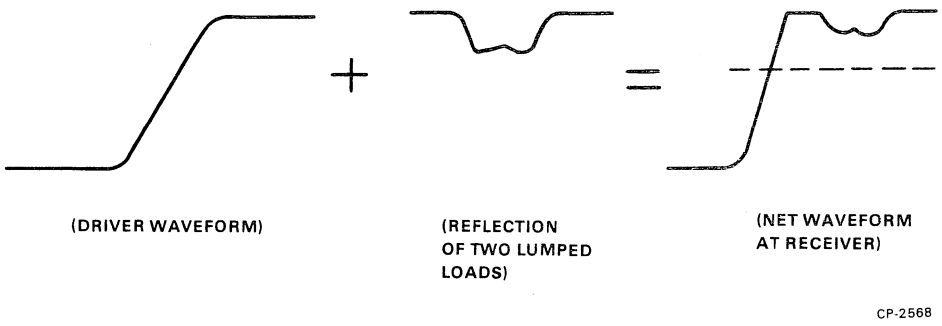


Figure 2-8 Rule No. 3 Implementation (Waveform Example)

Now the 8640 threshold is not crossed and the danger of a failure is reduced.

Rule No. 3 states that there is no limit to the number of ac unit loads on a Unibus segment (unless the entire segment consists of one lumped load). The reason for this statement is that there is no 120 ohm cable in the segment on which reflections can travel. The following segment (Figure 2-9) is an example.

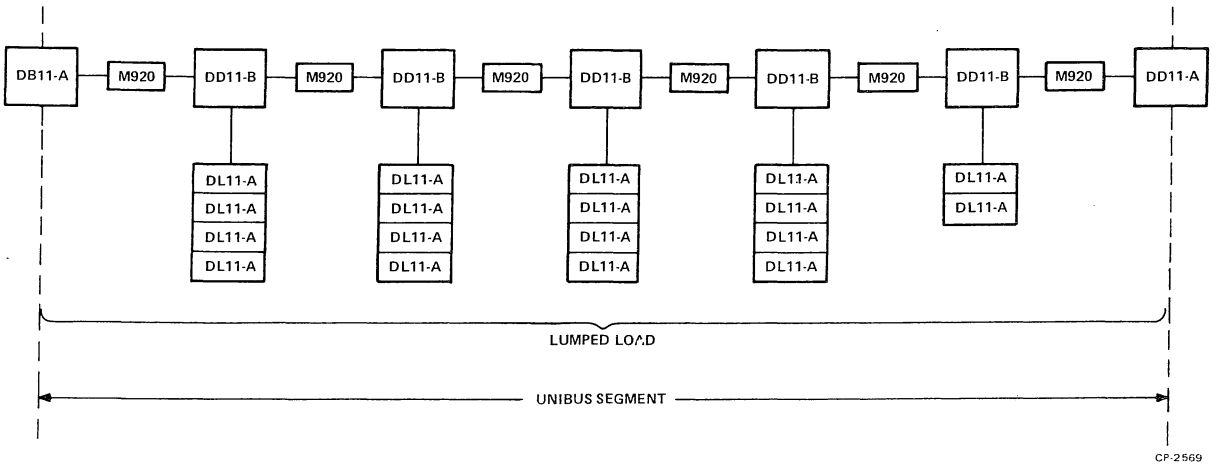


Figure 2-9 Multiple Bus System Example

This segment obeys all configuration rules. It has zero (0) feet of cable, 20 dc unit loads, and an irrelevant number of ac loads. In this configuration none of the M920s have to be replaced by M9202s.

2.3.4 Skewed Cable Lengths (Rule No. 4)

There may be several ways to implement Rule No. 4. Consider the following bus segment (Figure 2-10).

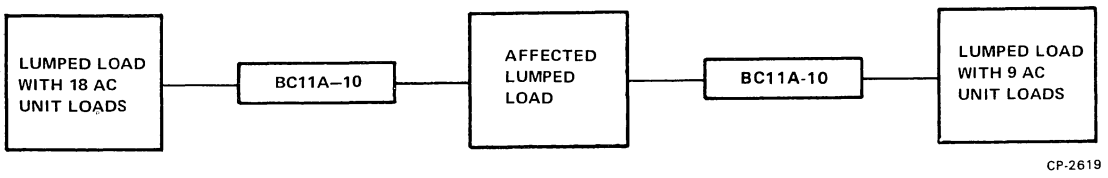


Figure 2-10 Rule No. 4 Violation (Block Diagram)

This segment violates Rule No. 4 because the sum of the lumped loads that are connected to the opposite ends of the cables exceed 18 unit loads. AC unit loads equal 27 (18 + 9 = 27) lumped at the ends of the BC11As of equal length. One way to implement Rule No. 4 is to increase the length of one cable to 4.57 m (15 ft) (see Figure 2-11).

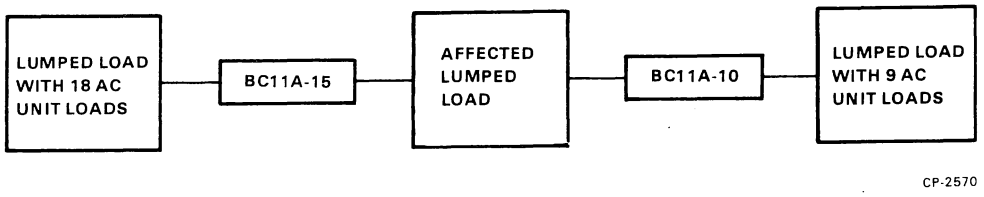


Figure 2-11 Rule No. 4 Implementation (Example A) Block Diagram

Another way is to split the lumped load on the left into two lumped loads using an M9202 (see Figure 2-12).

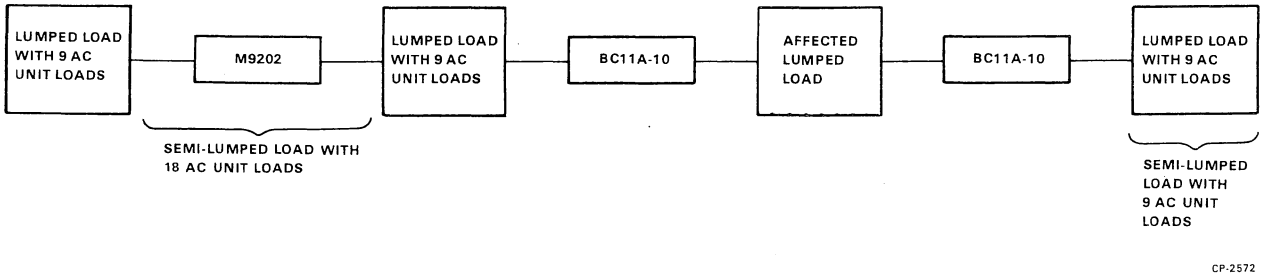


Figure 2-12 Rule No. 4 Implementation (Example B) Block Diagram

When this rule is violated and when a driver in the affected lumped load unasserts the bus, reflections from the ends of its bus in and bus out cables will arrive at the affected lumped load simultaneously and superimpose. The net reflection may cross the 8640 threshold and cause a failure (see Figure 2-13).

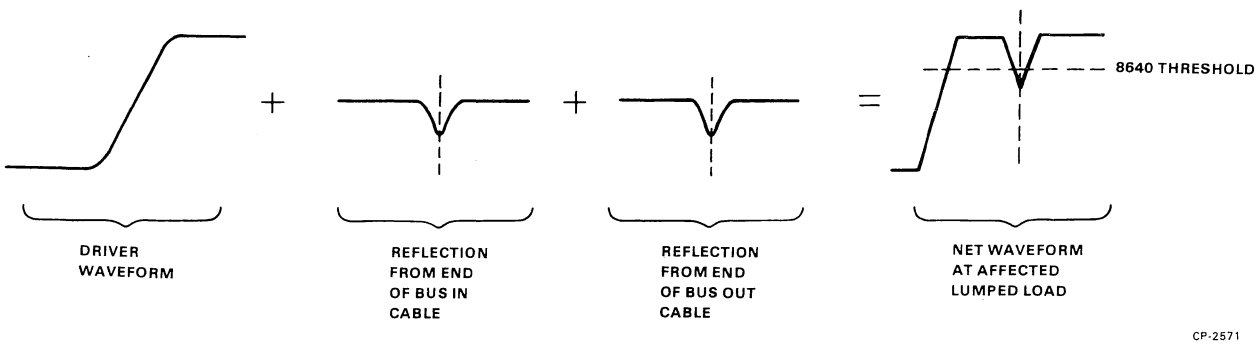


Figure 2-13 Rule No. 4 Violation (Waveform Example)

When the rule is implemented by making the lengths of the bus in and bus out cables different, the reflections will arrive at slightly different times (see Figure 2-14):

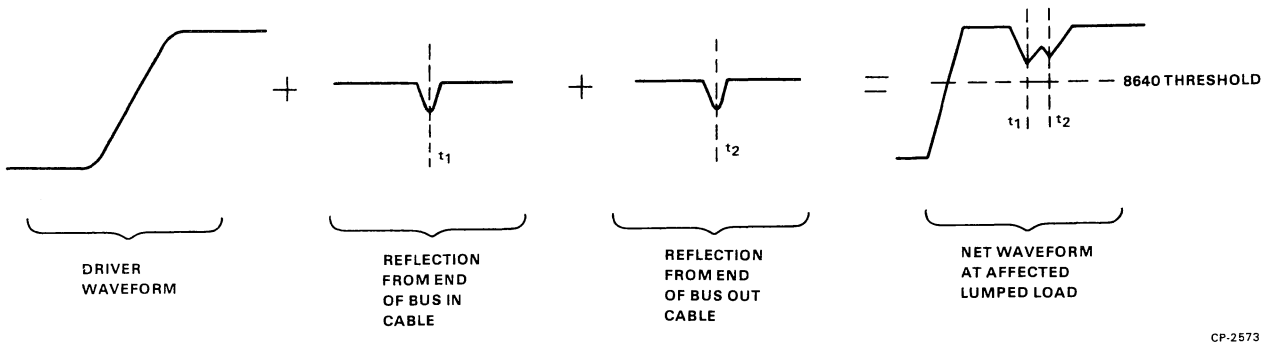


Figure 2-14 Rule No. 4 Implementation (Waveform Example)

Now the reflection does not cross the 8640 threshold and the danger of a failure is reduced.

The configuration in Figure 2-12 does not violate Rule No. 4 because the sum of the ac unit loads lumped at the ends of the BC11A-10 cables is 18 (9 + 9 = 18) and the sum of ac unit loads in the semi-lumped loads at the BC11A-10's ends of the cables is 9 plus the lumped loads (18) for a total of 27 unit loads (9 + 18 = 27).

Either of these methods could be used to implement Rule No. 4 but the second is more desirable in this example because it minimizes the total cable length of the segment.

2.3.5 Skewed Cable Lengths, Supplement (Rule No. 5)

To understand why this rule is necessary, consider the following example (Figure 2-15).

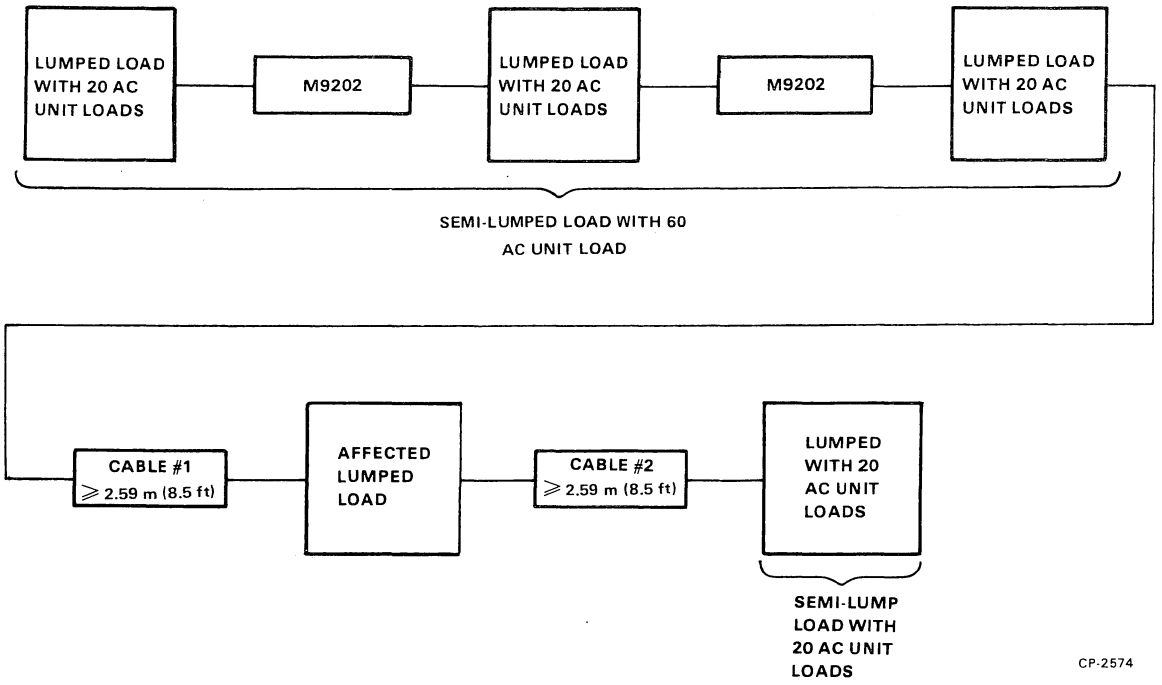


Figure 2-15 Skewed Cable Length Violation

Suppose that the length of cable no. 1 equals the length of cable no. 2. This violates Rule No. 4. In this case, the affected lumped load will see the following waveform (Figure 2-16) when its driver unasserts the bus.

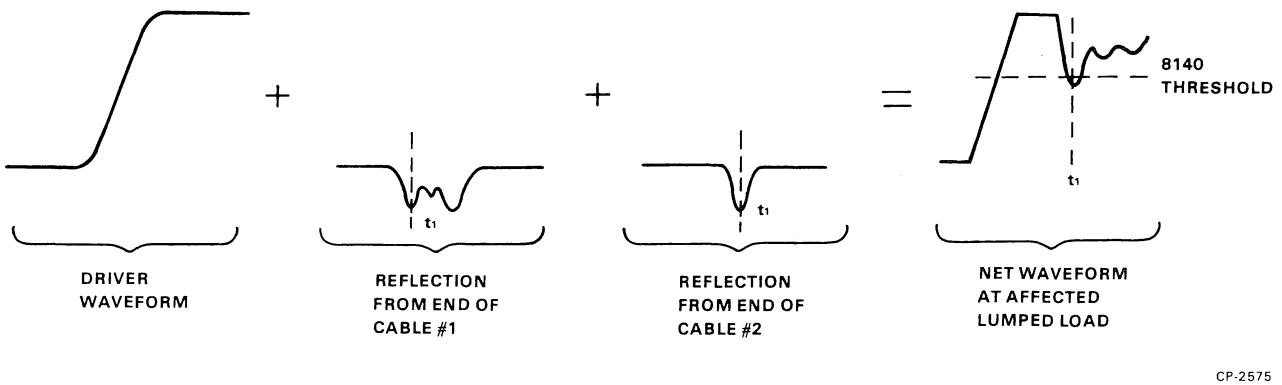


Figure 2-16 Skewed Cable Length Violation (Waveform Example)

The reflection in this waveform crosses the 8640 threshold and may cause a failure. The best way to implement Rule No. 4 in this example is to increase the length of either cable no. 1 or cable no. 2 by 1.52 m (5 ft). Suppose the length of cable no. 2 is increased by 1.52 m (5 ft). (This violates Rule No. 5 because this is the end with the smaller lumped load.) In this case, the affected lumped load will see the following waveform (Figure 2-17) when its driver unasserts the bus.

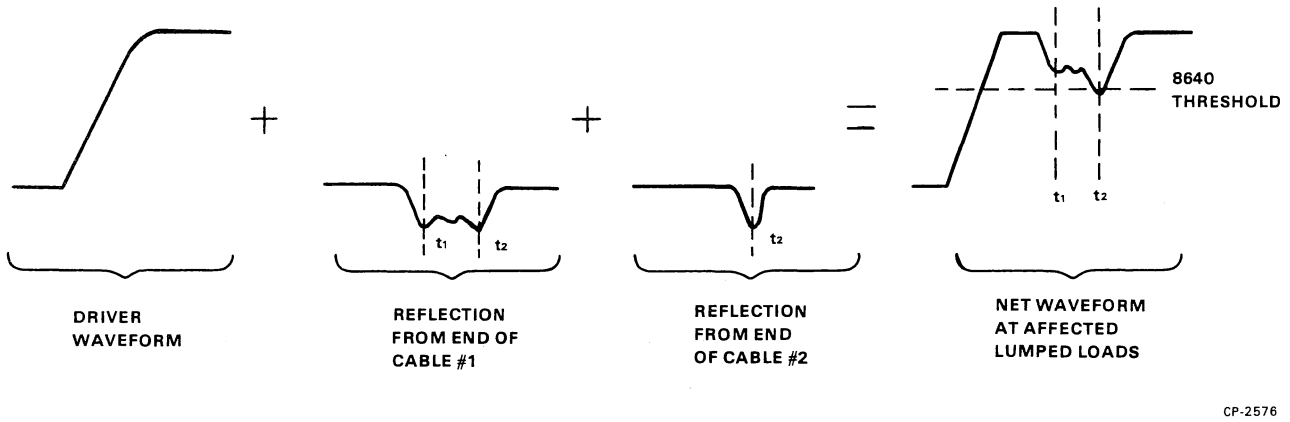


Figure 2-17 Violation of Rule No. 5 (Waveform Example)

The reflection in this waveform also crosses the 8640 threshold and may cause a failure.

Now suppose the length of cable no. 1 is increased by 1.52 m (5 ft) instead of cable no. 2. This will implement Rule No. 5 correctly. In this case, the affected lumped load will see the following waveform (Figure 2-18) when its driver unasserts the bus.

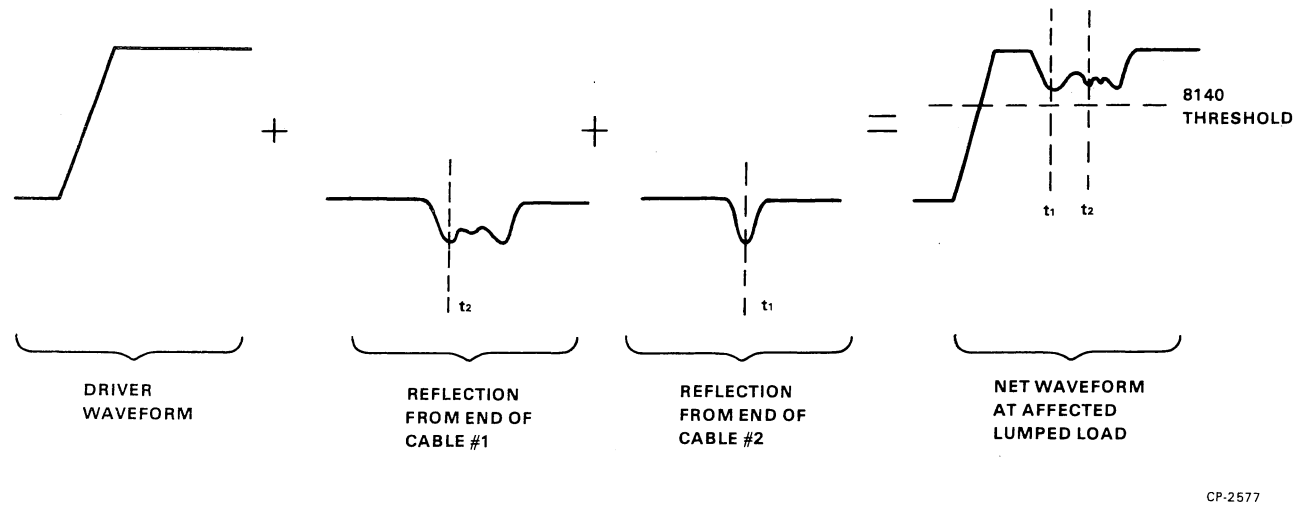


Figure 2-18 Implementation of Rule No. 5 (Waveform Example)

The reflection from the ends of cables no. 1 and no. 2 do superimpose somewhat, but not much. As a result, the 8640 threshold is not crossed.

2.3.6 Rule Violations (Rule No. 6)

Rules No. 1 through No. 5 should be implemented if possible. On rare occasions it may not be practical to do so. For example, the last bus segment on a system may exceed the 15.24 m (50 ft) maximum length rule by 1.52 m (5 ft), and implementing Rule No. 1 may require another DB11-A repeater, which may require another BA11-ES expander box, which may require another H960 cabinet. In this case, it is acceptable to violate Rule No. 1, providing that the system is tagged so that Rule No. 6 is always followed when the system undergoes change or corrective maintenance. Common sense has to be exercised if any of Rules No. 1 through No. 5 is violated.

The voltage margining procedure follows.

1. Replace the two terminators of the segment (M930, M9300, M9301, M9302, M981) with the appropriate low-margin cards (M9304, M9305).

2. Run complete diagnostics and system exercisers.

3. Replace the two low-margin cards by the corresponding high-margin cards (M9304-YA, M9305-YA).

4. Run complete diagnostics and system exercisers.

5. Replace the two high-margin cards with the original terminators.

If any diagnostic or system exerciser fails during this procedure, the system has a problem. It may be necessary to implement a rule violation in order to correct the problem. A Unibus voltage margining tester box (Chapter 4) may be necessary to isolate the problem. To determine if there is a margin problem, failures during margining must correspond with (or compared to) no failures when not margining.

2.3.7 System Acceptance (Rule No. 7)

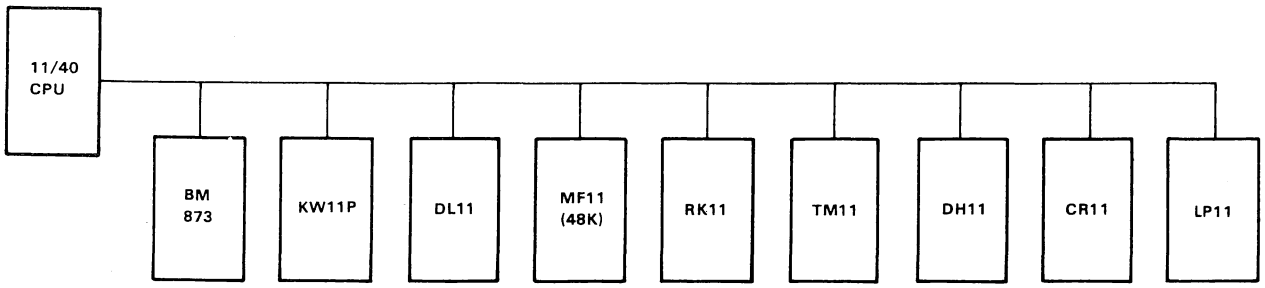
On rare occasions, Rules No. 1 through No. 5 may not be sufficient to eliminate all reflection problems. On these occasions, a Unibus voltage margin tester box (UVM-TA) should be used (along with common sense) to isolate the problem and implement solutions. When an option fails (gives data errors, hangs the bus, etc.) during a margining test, particularly the low-margining test, be suspicious of reflections from surronding options after eliminating weak drivers, leaky receivers, etc. The solution may be to replace an additional M920 in those surrounding options with an M9202 (or even a BC11A-3) in order to further spread out and reduce reflections. If Rules No. 1 through No. 5 do not eliminate a reflection problem, please consult F.S.11 Product Support in Maynard.

2.3.8 Actual Bus Loading

PDP-11 systems are configured to have no more than twenty loads or 15.24 m (50 ft) of Unibus cable on a given bus. Most devices are specified in terms of whole number loads but in fact this is not always the case. Table 2-1 lists realistic numbers for various options and using the system shown (Figure 2-19), it is seen how loading may differ from that determined by conventional configuration guidelines.

NOTE

If quiescent voltages are correct, then dc loading is probably not a problem.



BUS LOADS

CONVENTIONAL	16
ACTUAL (380 RECEIVERS)	23.2
ACTUAL (8640 RECEIVERS)	16.7

CP-2578

Figure 2-19 Actual Bus Loads Example

Caution must be exercised in customer situations – the published loading specifications for each device (as listed in Appendix D) must be used in discussions with non-DEC personnel. Table 2-1 is included only for your information. (Refer to Chapter 3, Paragraph 3.3)

Table 2-1 Realistic Load Values

Option	No. of Drivers	Driver Type	No. of Rcvrs	Max. No. unit loads if Rcvrs are 380s	Max. No. unit loads if Rcvrs are 8640s
AA11A	5	8881	2	1.52	.76
AA11B	5	8881	2	1.52	.76
AA11C	5	8881	2	1.52	.76
AA11D	5	8881	2	1.52	.76
AA11E	5	8881	2	1.52	.76
AD01	3	8881	1	1.119	.7380
AFC11	2	8881	1	1	.6190
BM792Y	1	8881	1	.8809	.5
BM873	0	NONE	2	1.523	.7619
CB11	2	8881	1	1	.6190
CD11	3	8881	1	1.119	.7380
CM11	4	8881	1	1.238	.8571
CR11	4	8881	1	1.238	.8571
DA11B	2	8881	1	1	.6190
DA11F	2	8881	1	1	.6190
DB11A	1	8881	1	.8809	.5
DC11	3	8881	1	1.119	.7380
DH11	1	8881	3	2.404	1.261
DJ11	2	8881	1	1	.6190
DK11	2	8881	1	1	.6190
DL11	4	8881	1	1.238	.8571
DM11BB	2	8881	1	1	.6190
DN11	2	8881	1	1	.6190
DP11	3	8881	1	1.119	.7380
DR11A	4	8881	1	1.238	.8571
DR11B	2	8881	1	1	.6190
DR11C	4	8881	1	1.238	.8571
DT03F	2	8881	1	1	.6190
DX11	2	8881	1	1	.6190
GT40	3	8881	1	1.119	.7380
KE11A	1	8881	1	.8809	.5
KG11	2	8881	1	1	.6190
KW11L	1	8881	1	.8809	.5
KW11P	3	8881	1	1.119	.7380
LC11A	4	8881	1	1.238	.8571
LP11	2	8881	1	1	.6190
LPS11	2	8881	2	1.52	.76
LS11	2	8881	1	1	.6190
LV11	2	8881	1	1	.6190
M792	1	8881	1	.8809	.5
ME11	1	74H01-1	1	1.952	1.571
MF11	1	74H01-1	1	1.952	1.571
MM11	1	74H01-1	1	1.952	1.571

Table 2-1 Realistic Load Values (Cont)

Option	No. of Drivers	Driver Type	No. of Rcvrs	Max. No. unit loads if Rcvrs are 380s	Max. No. unit loads if Rcvrs are 8640s
MR11	1	8881	1	.8809	.5
MS11	2	8881	1	1	.6190
PC11	4	8881	1	1.238	.8571
PR11	4	8881	1	1.238	.8571
RC11	3	8881	1	1.119	.7380
RF11	2	8881	1	1	.6190
RK11C	2	8881	1	1	.6190
RK11D	2	8881	1	1	.6190
RP11	2	8881	1	1	.6190
TA11	3	8881	1	1.119	.7380
TC11	2	8881	1	1	.6190
TM11	2	8881	1	1	.6190
UDC11		8881	2	1.52	.76

2.4 UNIBUS LATENCY

This section is designed to familiarize the Field Service Engineer with the recommended NPR Device Sequence on the Unibus and also provide the ability to determine and minimize possible "Data Late" errors.

The device sequences for a given PDP-11 System (CPU, memories, and devices) can be obtained by applying the algorithm given in Figure 2-20 and Table 2-2.

Table 2-2 Maximum NPR Rates of the NPR Devices with Variable Speed

Device	Maximum Data Transfer Rate	Maximum NPR Rate
CD11-E	1000 card/min	1.33 kHz
CD11-A	1200 card/min	1.6 kHz
DA11-B/DR11-B	500,000 word/s	500 kHz
DH11	16 × 9600 Baud	15.4 kHz
DQ11-DA	10,000 Baud	1 kHz
DQ11-EA	1 Megabaud	100 kHz
GT40	20 μs/point	50 kHz

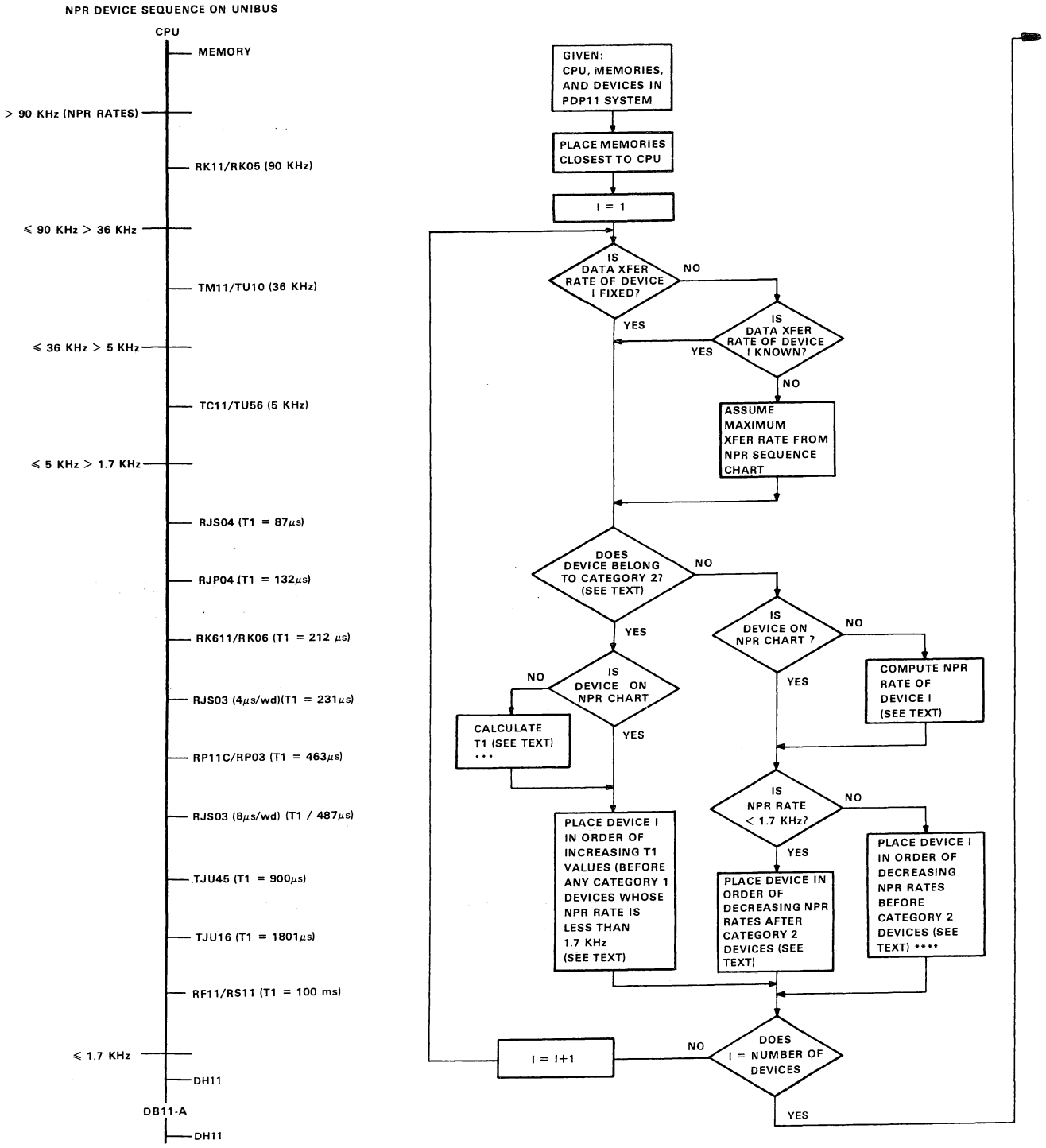
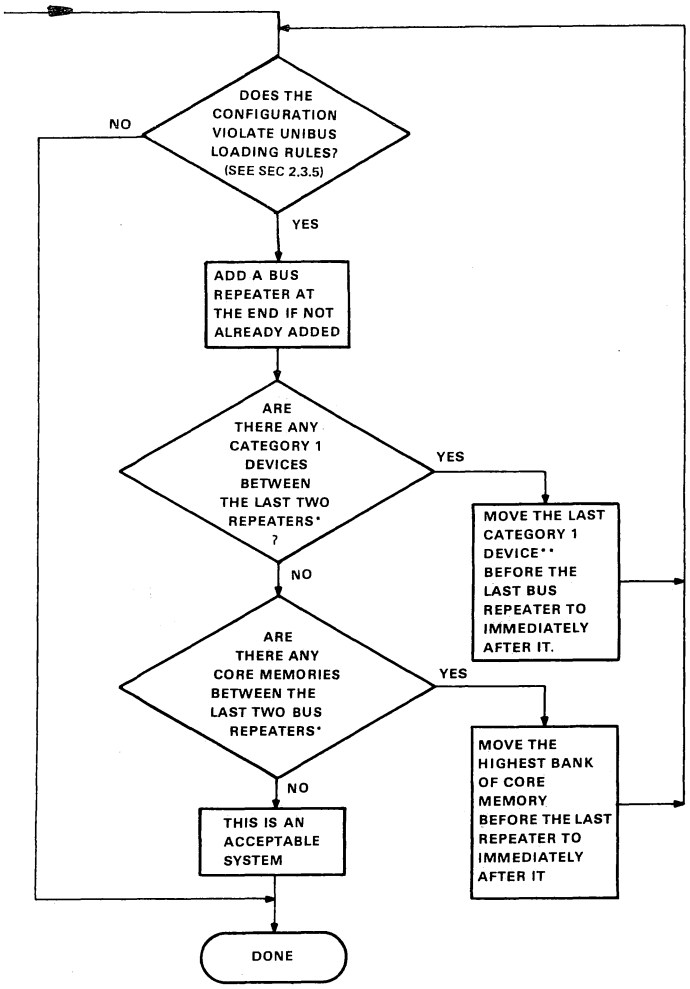


Figure 2-20 Algorithm To Determine NPR Sequence (Sheet 1 of 2)



* If only one BUS REPEATER, this means between the CPU and the BUS REPEATER.

** Or the least frequently used category 1 device.

*** T1 = Maximum tolerance between bus cycles

****Except asyncheonous communication devices (e. g., DH11) which have great latency tolerance capacity. DH11 can be placed in rear of all other devices.

NOTES:

1. Throughput is conditional and is well studied at the CPU. I/O bandwidth is more difficult to determine but has been investigated by Engineering.

2. BR device can be put behind repeaters or behind NPR device. BR device should be placed in front of asynchronous devices. (i.e. NPR11 - DMC11, DVM11 - DC11)???

CP-2686

Figure 2-20 Algorithm To Determine NPR Sequence (Sheet 2 of 2)

Using the procedure outlined in Figure 2-20 and the maximum NPR rates specified in Table 2-2, the following steps should be used to approach a DATA LATE problem.

1. Determine the correct sequence of devices on the Unibus. If the configuration is incorrect, correct it.

2. Determine from the configuration tables whether or not the system is expected to experience DLTs due to Unibus bandwidth (refer to Figure 2-24).

3. If the system is not expected to experience DLTs but nevertheless does, isolate the hardware malfunction with the bus busy measurement technique.

   In some cases, it may be useful to apply the Bus Busy measurement technique to systems which may experience Data Lates due to Unibus bandwidth. In such instances, the technique helps to demonstrate that the hardware is functioning correctly.

NOTE

For the purposes of this manual, bandwidth is defined as the number of bus cycles that can be accommodated and still provide successful execution of the application software.

2.4.1 Device Categories

All existing NPR devices that are connected to the Unibus are considered to be in one of the two defined categories. Note the fact that all communication devices are considered to be in category 1 classification even though some devices have data buffers of more than six words (usually, these devices multiplex more than one line).

Category 1 – Devices whose controllers have six or fewer words of data buffer (excluding RF11/RS11 which, although it has only a one-word data buffer, falls more closely into category 2 simply because it can wait for a maximum of three disk revolution time or 100 ms without getting "data late" errors). Other devices in this category are: CD11, DA11, DH11, DQ11, DR11, GT40, RK11/RK05, TM11/TU10, and TC11/TU56.

Category 2 – Devices whose controllers have more than six words of data buffer (including RF11/RS11 as described under category 1). Devices included in this category are: RJS04, RJP04, RK611/RK06, RJS03, RP11C/RP03, TJU45, TJU16, and RF11/RS11.

2.4.2 NPR Calculations for T1

NPR rates of category 1 devices can be computed in one of the following ways.

NPR RATE = baud rate /10 (may be different for different devices), or

= word/s, or
= card/min × 1.33

Within Category 1, devices with higher NPR rates should be placed before devices with lower NPR rates.

2.4.3 Latency Tolerance Calculations*

The process of determining category 2 device sequence can be simplified by comparing T1 (maximum tolerance between bus cycles) of each device, which can be computed as follows:

$$T1 = TDBS - TBBLUP \times 2$$

where: TDBS = Time to transfer DBS words to/from the device (in μs)
DBS = Data buffer size of the device controller (for RH11, DBS = 66)
TBBLUP = Typical data bubble up time of the device controller (for RH11, TBBLUP = 16 μs)

Please note the following information carefully.

1. If the sector size of a device is larger than DBS, TDBS is simply the product of the instantaneous data transfer rate of the device and the DBS of the device controller. For example, the sector size of RP04 is 256 words (DBS = 66 words), and the instantaneous data transfer rate is 2.48 μs/word, so TDBS = 2.48 $\times$ 66 = 164 μs.

2. If the sector size of a device is smaller than DBS, the sector gap and interleaved sector and gap (if any) must be accounted for to compute TDBS. The situation can be clarified better with the examples that follow. RS03 has sectors of 64 words, sector gaps of 25.6 μs and an instantaneous data transfer rate of 3.6 μs/word. Its DB (or silo) has two more words than a sector; therefore, two words must be gotten to/from the next sector.

   Sector-noninterleaved (4ls/wd): TDBS = 3.6 $\times$ 64 + 25.6 + 3.6 $\times$ 2 = 263 μs
   Sector-interleaved (8 μs/wd): TDBS = (3.6 $\times$ 64 + 25.6) $\times$ 2 + 3.6 $\times$ 2 = 519 μs

NOTE

Within category 2, devices with greater T1 should be placed after devices with smaller T1. All category 2 devices should be placed before category 1 devices with NPR rate less than 1.7 kHz, except for asynchronous communication devices (e.g., DH11) which have great latency tolerance capacity. DH11 can be placed in rear of all other devices.

2.4.4 BR Devices

All the BR devices should be placed after NPR devices. However, sometimes for convenience sake some BR devices may be put before NPR devices (e.g., a DECwriter may be placed next to the CPU).

2.4.5 Unibus Loading Rules

1. Maximum loading before the first bus repeater is 19 dc bus loads; between two adjacent bus repeaters is 18 dc bus loads.

2. Maximum Unibus cable length between the first bus repeater and the CPU or between the adjacent bus repeaters is 15.24 m (50 ft). For example, configure a system with 11/45, 128K of MF11-UP, DL11-A/LA30, KW11-L, RK11/RK05, RJS04, RJP04, DH11, DQ11-EA (at 12.5K baud), RF11/RS11, TJU16, GT40, CD11-E.

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*Latency tolerance capacities of devices in category 2 are defined and computed using "Latency Tolerance Capacities of NPR Controllers/Devices and Configuration Guidelines". 4/23/75.

After going through Figure 2-20 and Table 2-2, the following sequence results.

Device	Unibus Loads
11/45	2
KW11-L	1
DL11A/LA30	1
128K MF11-UP	8
RK11/RK05 (90 kHz)	1
GT40 (50 kHz)	1
RJS04	1
RJP04	1
TJU16	1
RF11/RS11	1
DH11 (15.4 kHz)	2
CD11-E (1.33 kHz)	1
DQ11-EA (1.25 kHz)	1
TOTAL	22 UNIT LOADS

There are a total of 22 unit loads. Therefore, a DB11-A is added at the end and DH11, DQ11-EA and CD11-E are repositioned after DB11-A.

NOTE

The NPR device sequence algorithm does not take into account the measures of the usage of the devices. For example, suppose that in the system given above GT40 is seldom used. GT40 may be placed behind RF11/RS11 to improve system throughput.

2.5 BUS BUSY TEST TECHNIQUES

The following description is designed to aid in determining "nominal" device bus busy times for PDP-11 system configurations. It is intended for use in cases where a system under test is configured correctly, but is still incurring Unibus "Data Late" errors.

Almost every PDP-11 I/O device, transferring data at the NPR level, has a period of time in which a word or byte of data can remain in its data buffer before the next incoming word displaces it. This period of time is known as a device's latency. If, during this period of time, the device is unable to complete a Unibus transfer, the word in the data buffer will be displaced and lost. A data late error will result and the transfer operation must be aborted and restarted. This is obviously an undesirable condition.

Latency, or Data Late, errors may occur as a result of many factors, e.g., device and memory types, Unibus configurations, software in use, and hardware malfunction. This document will address hardware malfunctions.

2.5.1 Bus Busy and Latency Tolerance

In many instances stand-alone diagnostics and system exercisers will provide sufficient information to allow the problem to be identified and isolated. This generally leads to a traditional troubleshooting approach.

Sometimes, however, the malfunction will be more subtle, eluding even the most rigorous diagnostics. In the past, large devices were slow (by today's standards) and there was little concern about how long a device took to complete a transaction on the Unibus. As systems have expanded in size and devices have become faster and software more stringent in its I/O demands, the need for NPR devices to complete their transactions and release the Unibus to another device as soon as possible has become imperative.

If an NPR device holds BBSY asserted on the Unibus for an abnormally long period of time, that device (in some configurations) could "crowd out" another NPR device competing for Unibus time forcing an error condition to occur. It should be evident, then, that Data Lates being reported by one device may be caused by another device on the system being a "bus hog".

The following paragraphs will show how to predict nominal BBSY time for a given configuration and how to measure the actual BBSY times. Guidelines are included to help determine whether or not the measured BBSY times fall within an acceptable range around the predicted value.

2.5.2 Calculating Nominal Bus Busy Times

NOTE

It doesn't matter if the calculations necessary to predict a BBSY time are performed first or if the measurements are made first. In some cases however it is necessary to determine if a device is conducting "single cycle" or "double cycle" transactions, as this will affect the calculations that must be made. This will be true of some Massbus devices (RH11). If in doubt, proceed to Paragraph 2.4.3 and make this determination.

This section deals with calculating or predicting a BBSY time for a device within a given configuration. Component tolerances throughout the system make exact calculations impossible, but typically a device should fall within a plus-or-minus 30 percent range of the predicted value. If, after measuring the real BBSY time, it exceeds the predicted value by more than 30 percent, a potential problem area has been found and steps should be taken to bring the offending device nearer to specification.

For the purposes of this manual, BBSY can be thought of as composing four separate components:

1. Ddv
   This is the internal timing delay of the device itself. The figure can be obtained from Table 2-3.

2. Dma
   This is memory access time or the time it takes memory to assert SSYN after it sees MSYN. This figure can be obtained from Table 2-4.

3. Dtr
   This is the delay associated with Unibus transmitters and receivers. This figure may be obtained from Table 2-5.

4. Dp
   This is the propagation delay of the Unibus itself, taking into account its length and loading properties. This must be calculated from a formula.

Table 2-3 Device Delay (Ddv)

Controller Type	Ddv (in nanoseconds) Single Cycle	Double Cycle
TC, TM, RP11-C, RK11-C, RF11	1100	N/A
DH11	1350	N/A
RK11-D	935	N/A
RH11 680	1355	

Table 2-4 Memory Access Delay (Dma)

Memory Type	Dma (in nanoseconds) Single Cycle	Double Cycle
8K MF11-L	365	730
8K MF11-LP	430	860
16K MF11-U	375	740
16K MF11-UP	460	920
Other Core	410	820

Table 2-5 Transmitter/Receiver Delay (Dtr)

Transmitter/Receiver Type	Dtr (in nanoseconds) Single Cycle	Double Cycle
Dt 8881	60	120
Dt 8838	40	80
Dt 380	40	80
Dt 8640	40	80

Single Cycle = Dp = (3.4 × UL) + (3.5 × dc unit loads)
Double Cycle = Dp = (6.8 × UL) + (7 × dc unit loads)

The summation of these four components yields a BBSY value unique to particular device and configuration.

$$BBSY = Ddv + Dma + Dtr + Dp$$

The first three components of the formula (Ddv, Dma and Dtr) are easily obtained by referring to the referenced tables. Locate in the table the appropriate device, memory type or transmitter/receiver type and extract the number from either the "single cycle" or "double cycle" column as it pertains to the device. Determining "single cycle" or "double cycle" is explained in Paragraph 2.5.3.

The fourth component of the formula (Dp) may be derived in the following manner.

Single Cycle

$$Dp = (3.4 \times U1) + (3.5 \times \text{dc unit loads})$$

or

Double Cycle

$$Dp = (6.8 \times U1) + (7 \times \text{dc unit loads})$$

where:
U1 = Unibus length in meters (feet) between the device and memory

DC Unit Loads = the number of DC Unit Loads between the devices and memory, *including* the dc unit loads presented by memory itself.

To illustrate this, look at the sample configuration shown in Figure 2-21. If the device under test were the RK11-D the value of U1 would be 60.96 cm (2 ft) and the dc unit loads would be 3 (1 dc unit load for each 16K bank of memory). If the device under test were the TM11, U1 would equal 2.13 m (7 ft) and dc unit loads would equal 4.

NOTE

If the device under test is located behind one or more DR11 bus repeaters add 375 ns (for devices doing "single cycle" transfers) or 750 ns (for devices doing "double cycle" transfers) to the calculations for each bus repeater between the device and memory.

2.5.3 Measuring Bus Busy Times

A dual-trace oscilloscope with three probes will be needed to conduct the following tests. The third probe will be used to monitor MSYN in order to determine if some of the NPR devices (such as RH11s) are doing "double cycle" transactions. If it is certain that all the devices to be tested will be conducting "single cycle" transfers only, the third probe may be eliminated and all calculations will be made from figures extracted from the "single cycle" columns in Tables 2-3, 2-4, and 2-5.

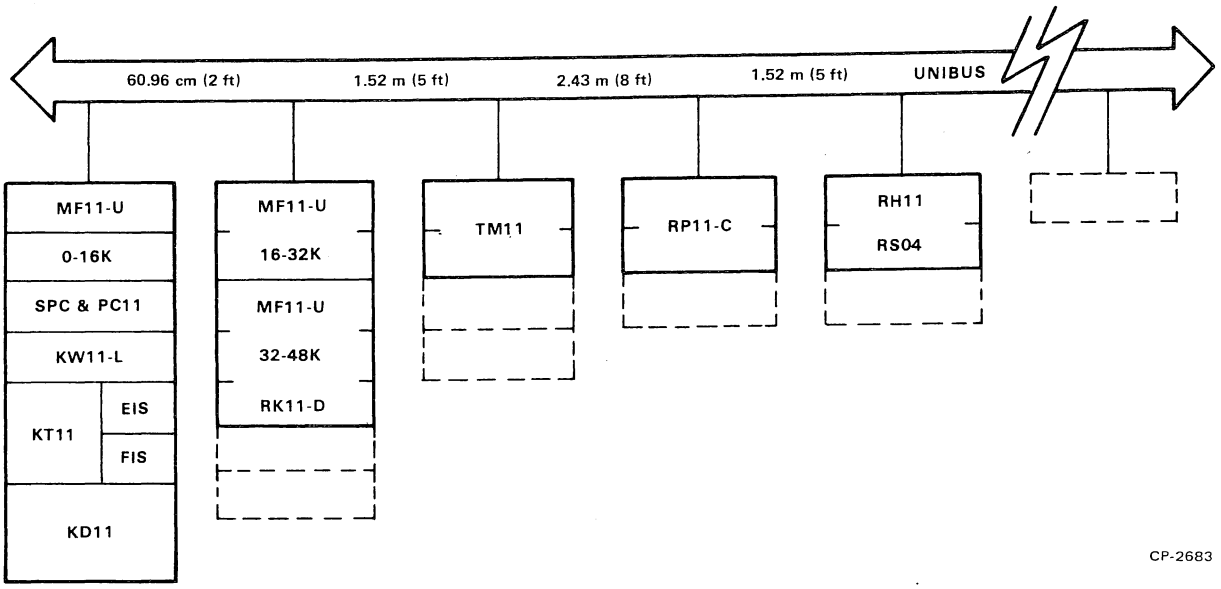


Figure 2-21 Unibus Length Between Device and Memory

Set up the oscilloscope as follows:

Coupling = dc
Trigger = External positive
Mode = Alternate
Vols/Div = .1 (with X10 probes)
Time/Div = .5 microseconds.

Now locate a convenient access to the Unibus. The TC11 (DECtape) is a good access point if available, otherwise any backplane with Unibus-in or Unibus-out will do.

Connect the probe corresponding to external trigger to SACK L at pin AR2.

Connect the probe corresponding to channel 1 to BBSY L at pin AP2.

Connect the probe corresponding to channel 2 to MSYN L at pin BV1.

The software to be run during these tests will be DEC/X11. Before proceeding, note that Table 2-4 (Dma) doesn't include data on MOS or bi-polar memory systems. For this reason, ensure that DEC/X11 doesn't use MOS or bi-polar as write buffer space. If the system under test is an all core system this will not be of any concern. If the system does include MOS or bi-polar it will be necessary to lock the run-time exerciser in memory (via the RUNL command) so that the beginning of DEC/X11s write buffer space (which coincides with the last address + 2 or the last module) is in core. It is acceptable if the DEC/X11 code exercises from MOS or bi-polar as long as the write buffer space is in core. Finally, inhibit write buffer rotation via the ROTOFF command.

Before issuing the RUNL command, DESelect all modules and SELect the module corresponding to the first device to be tested.

NOTE

By testing only one device at a time and by triggering the scope from SACK, it is ensured that the signals seen will be those issued by the device under test.

Once DEC/X11 has been started and the scope trigger has been properly adjusted, the brace should correspond to one of the two figures shown in Figures 2-22 and 2-23. Figure 2-22 shows a device doing single-cycle transaction, and Figure 2-23 shows a device performing double cycle transactions.

The key here is the channel 2 trace displaying MSYN. If MSYN is seen being asserted once during the BBSY time displayed on channel 1, the device is performing single-cycle transfers and the "single cycle" column in Tables 2-3, 2-4 and 2-5 should be used. If MSYN is seen being asserted twice during the BBSY time the device is performing double cycles and the "double cycle" column in the tables should be used for the calculations on that device.

The BBSY time being displayed on channel 1 is the time to be ultimately concerned with. This is the value that should coincide (plus-or-minus 30 percent) with the calculated value.

Once the measurements have been taken for a device, issue a control C from the keyboard to stop the run-time exerciser. When DEC/X11 is ready to accept new commands DESelect the device just tested and SELect the module corresponding to the next device to be tested and repeat these procedures until all NPR devices on the system have been measured.

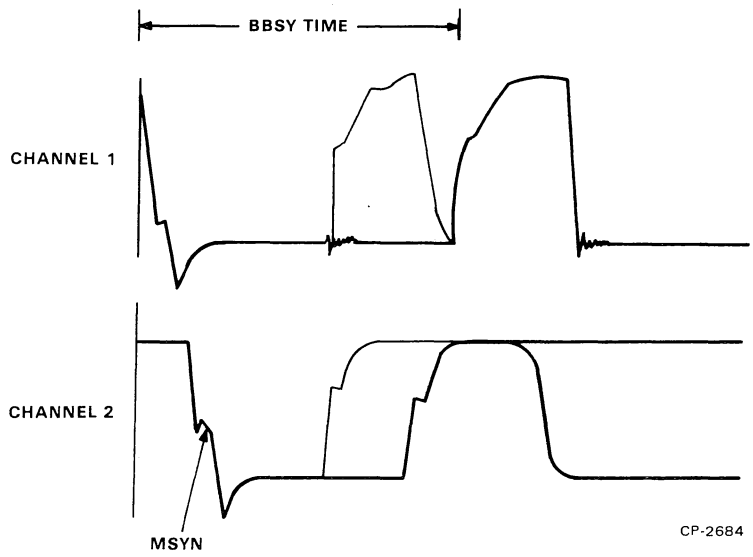


Figure 2-22 Single-Cycle Transaction

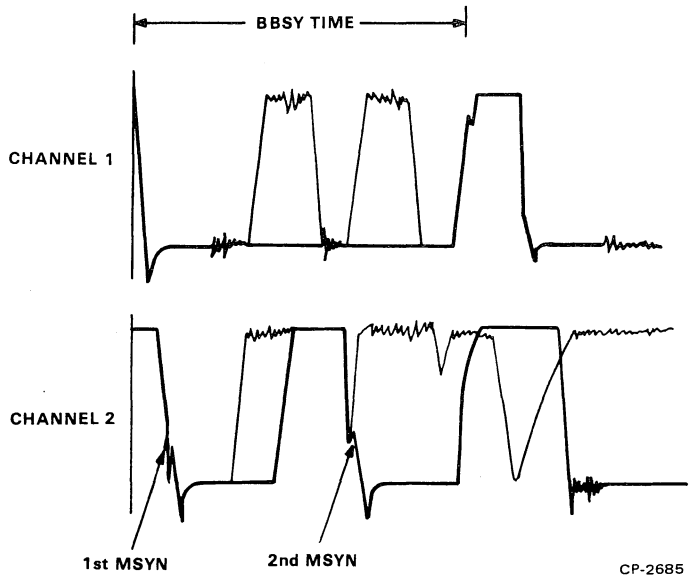


Figure 2-23 Double-Cycle Transaction

2.5.4 Configuration Tables

The configuration table (Figure 2-24) is presented here to familiarize the user with Data Late (DLT) occurrence possibilities of some common PDP-11 systems. No attempt is made in this manual to cover all possible configurations because of the complexity of the problems that could be encountered.

In all configurations, the general rules are:

1. If a configuration runs DLT-free, then a subset of the configuration should also run DLT-free.

2. If a configuration runs with DLT, adding more devices to the system should also give DLT.

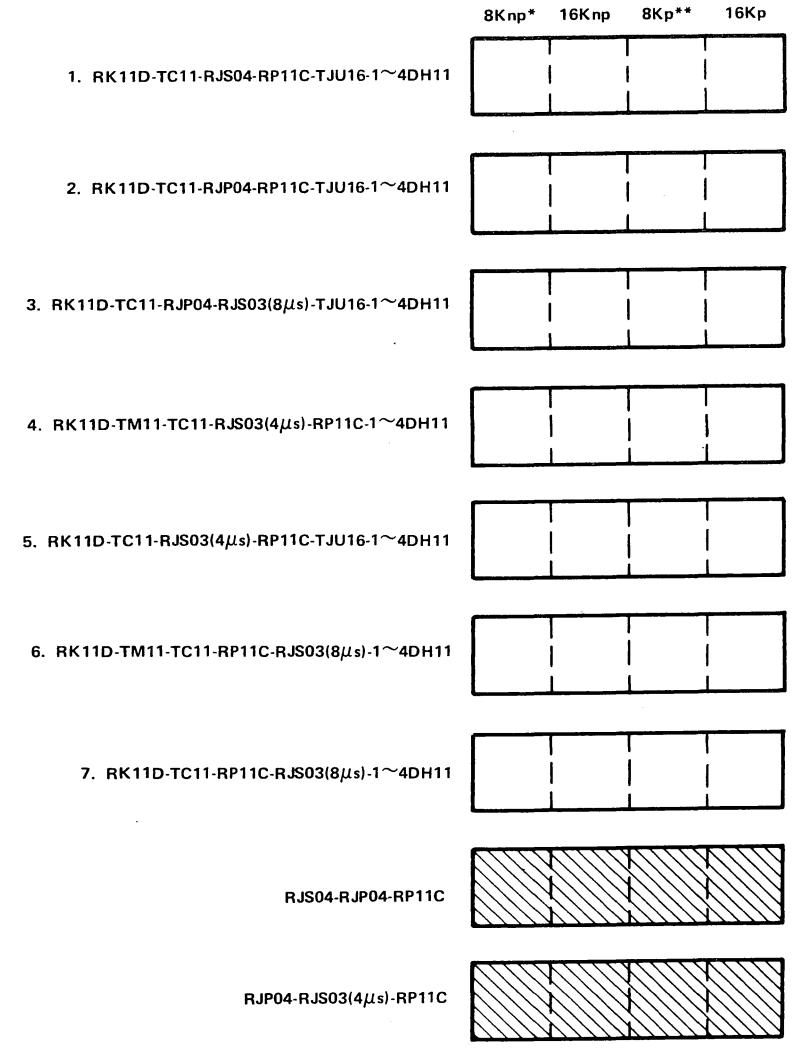


Figure 2-24 DLT Configurations

CHAPTER 3
TROUBLESHOOTING

3.1 GENERAL

This section is designed to aid in isolating and troubleshooting Unibus failures. The Unibus Troubleshooting Flowchart (Figure 3-1) is designed to provide a step-by-step procedure for checking and correcting Unibus problems. The flowchart references chapters and paragraphs (which contain additional information and possible solutions to solve Unibus problems) are included for reference.

3.2 TIMING CONSIDERATIONS*

Some system failures such as address errors, missing data, illegal traps and system halts can occur because of bus timing relationships.

3.2.1 DATO-DATOB

The Unibus specification states that MSYN must be asserted 150 ns (minimum) after the address, control, and data (for DATO and DATOB transactions). This delay includes 75 ns to allow internal logic in the slave device to decode the address. If MSYN is asserted before 150 ns, insufficient deskew and signal decoding at the slave may result in errors. An 8881 driver and an 8640 receiver combination can cause up to 60 ns of skew leaving as little as 15 ns as the allowable skew because of the Unibus transmission media. The most timing-sensitive lines have been found to be BBSY, MSYN, SSYN and INTR. Cable length and configuration can be a noticeable factor in these lines.

3.2.2 DATI-DATIP

For a DATI or DATIP operation, the slave puts requested data on the D lines and then asserts SSYN. The slave should not assert SSYN at the driver input before the data and enable lines are valid at the data driver inputs. The critical point seems to be around 35-40 ns skew in SSYN vs. DATA at which point it is possible for high-speed systems (such as the 11/45 which allows only the 75 ns maximum skew) to clock in erroneous data.

Some memories have a potential problem with this timing relationship in certain systems. When a system is upgraded from an 11/05 or 11/20 to an 11/45 or when more of this memory is added in an extended cabinet by a longer Unibus cable, the risk factor for problems becomes greater. If problems are experienced with these memories (MM11-L, MM11-S, MM11-E, MM11-F) in high-speed systems, consult F.S. Product Support.

*Refer to the 1975 Peripherals Handbook for Unibus timing information.

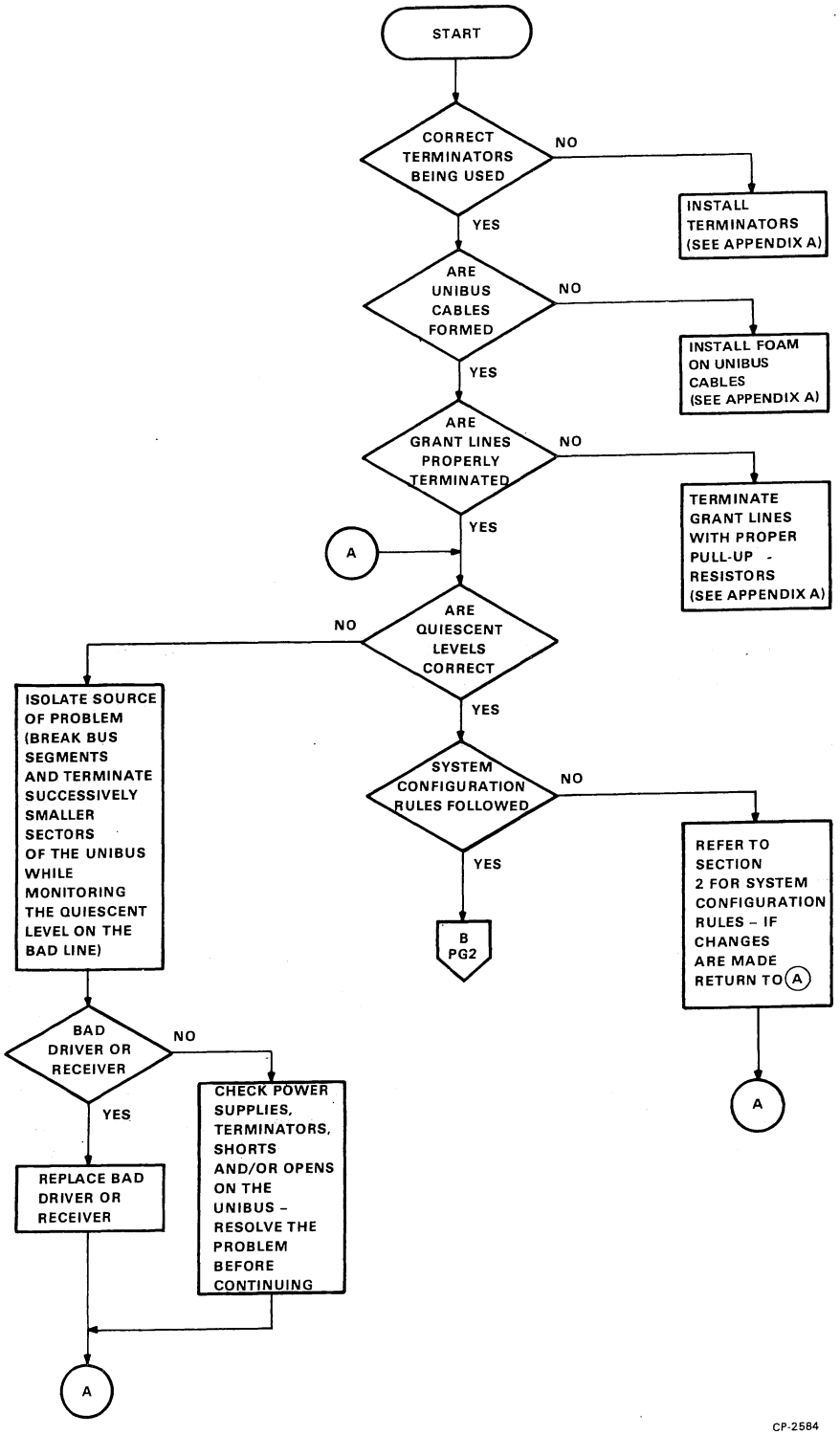


Figure 3-1 Unibus Troubleshooting Flowchart (Sheet 1 of 3)

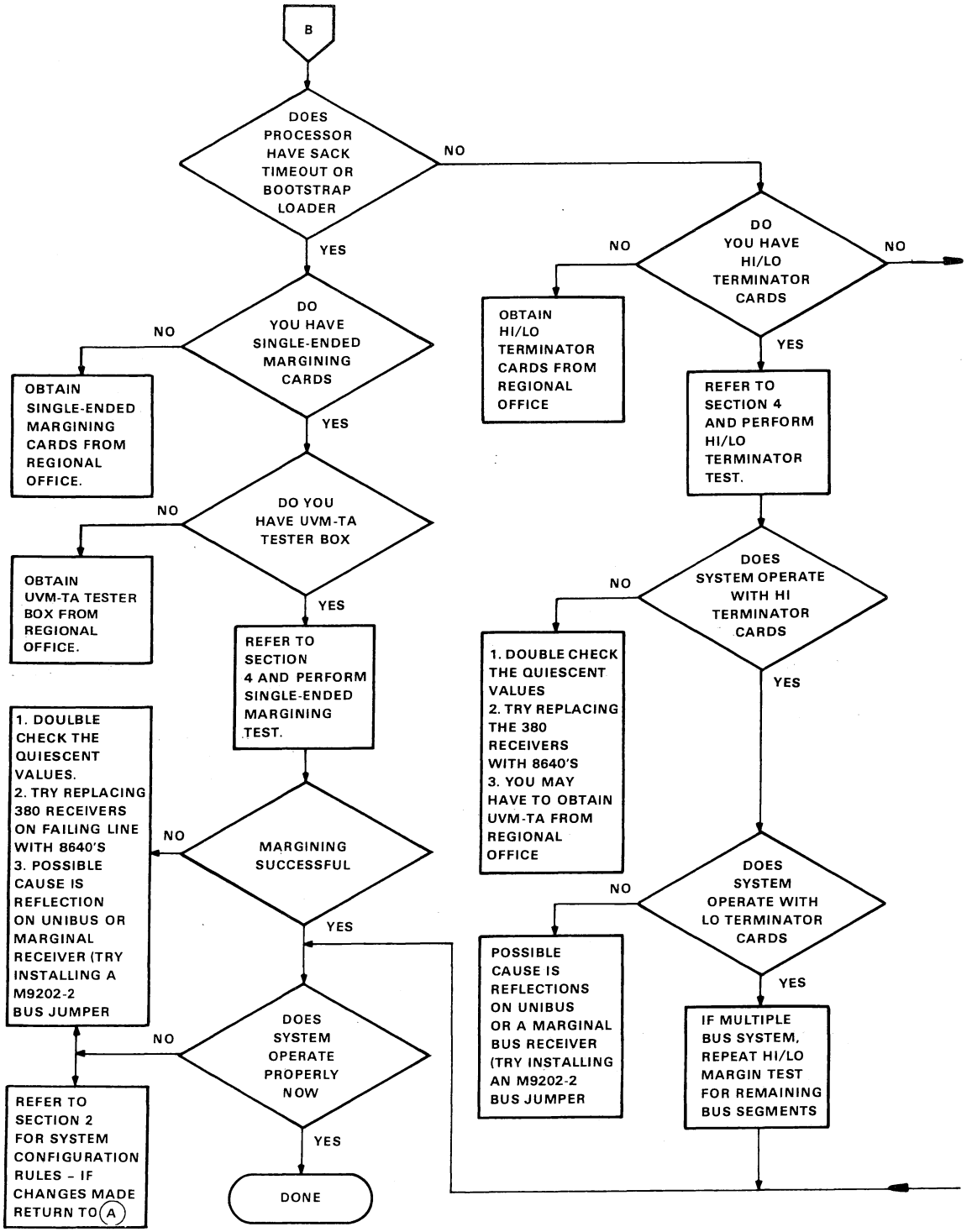


Figure 3-1 Unibus Troubleshooting Flowchart (Sheet 2 of 3)

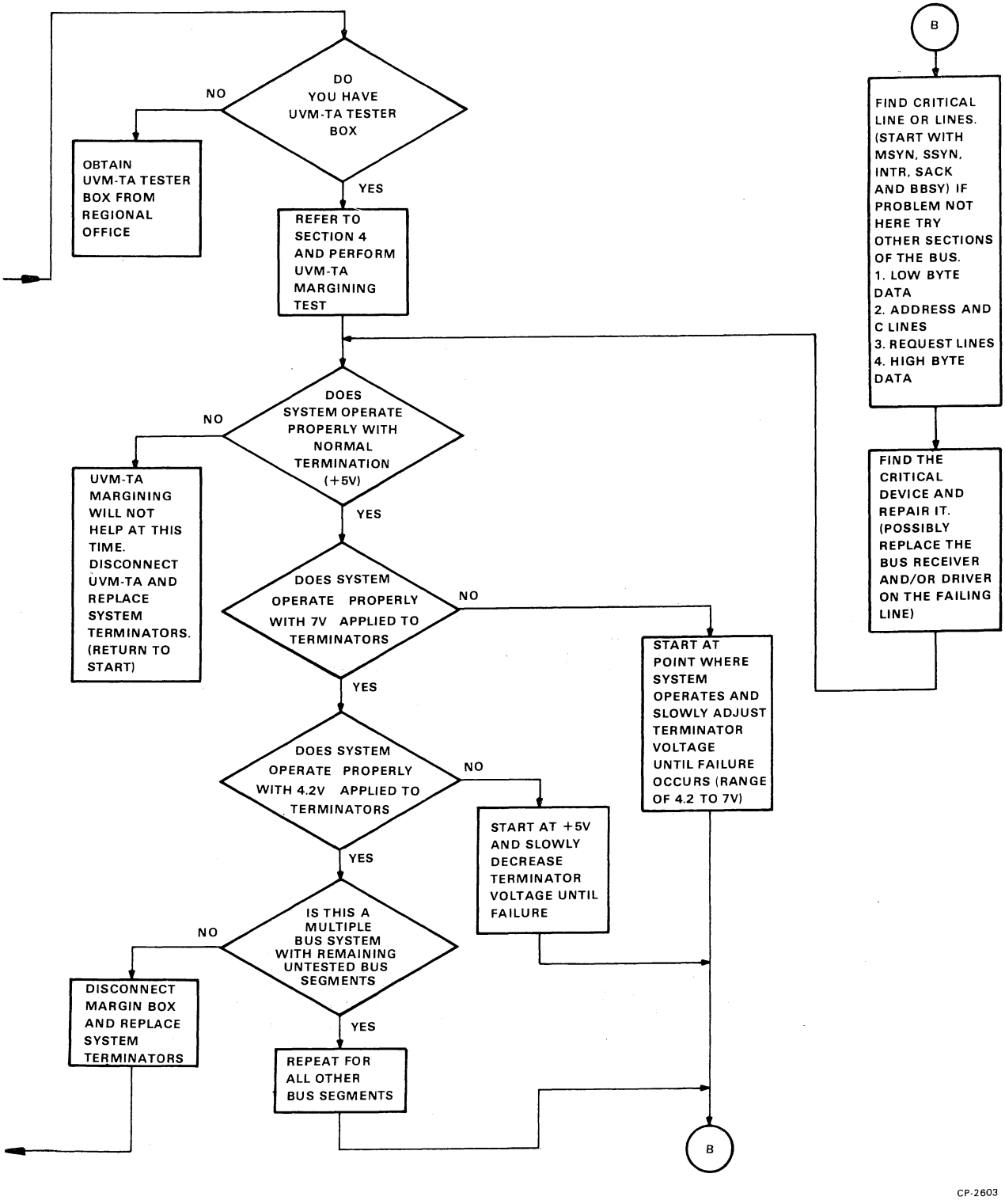


Figure 3-1 Unibus Troubleshooting Flowchart (Sheet 3 of 3)

3.2.3 Interrupt Transactions

A typical 11/45 system will experience problems if the data lags the INTR line on the cable by more than 30-40 ns. Most DEC interfaces assert the vector address and INTR at exactly the same time and Unibus skew times may cause a timing problem if the bus is long. Experiments with a typical system show the vector address lagging INTR on the cable by as much as 30 ns with 9.14 m (30 ft) of Unibus cable and a TC11 or 45 ns with 9.44 m (31 ft) of bus and a DL11. The electrical configuration rules as listed in Chapter 2 will minimize these problems when properly applied.

3.2.4 High-Frequency Cable Losses

The increase in transmission line conductor resistance at high frequencies, known as skin effect, may be a factor in bus analysis. This function exhibits a very fast rise time to 50 percent of the input, but a very slow dribble up from 50 percent to 90 percent of the input.

A 15.24 m (50 ft) bus cable could theoretically have a dribble up noticeable for up to 170 ns in response to a step function at the input.

The bus should, therefore, be kept as short as possible to avoid potential timing problems. The published (i.e., allowable) Unibus length is 15.24 m (50 ft), but it is desirable to use as little cable as possible for a given configuration (see Figure 3-2). Devices should be physically arranged in the same order as they are electrically connected, if possible. (If M9202 folded cables are needed due to physical arrangement, they should not be replaced by M920s in order to decrease bus length.)

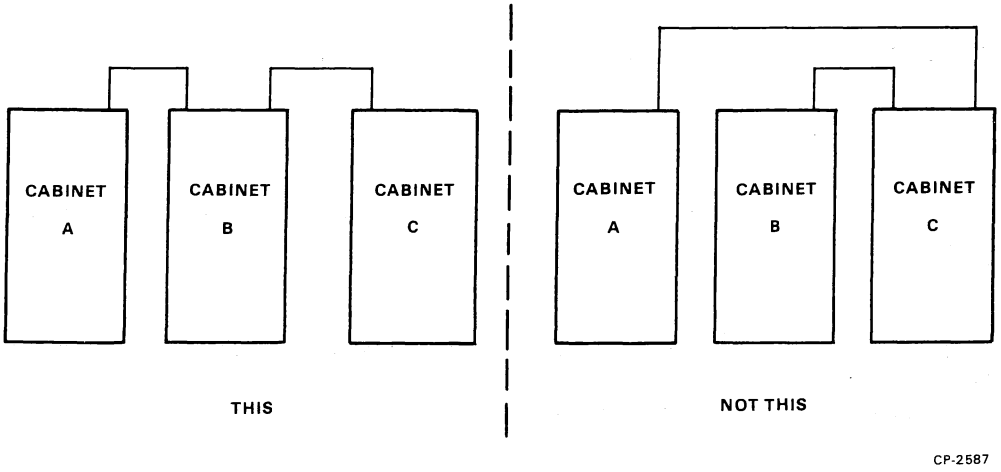


Figure 3-2 System Cabling Configuration Example

3.2.5 Peripheral Data Rate

It is possible to support only a certain rate of data transfer on the Unibus – beyond this rate, data late situations will occur. A method for roughly determining permissible combinations of simultaneous peripheral device activity (such as would occur when executing DECX11) follows.

1. Determine a window for a given system based on the slowest NPR device transfer rate (μs).4 If you have an RK11, RP11, TM11 and TC11, the slowest device will be the TC11 with a transfer rate of 200 μs/word.

   Window = 200 μs (in this case)

2. Determine how many transfers the faster devices will perform in the window time.

   (Window Time)/(Transfer Rate)

   RK11 (11.1 μs/word) 200/11.1 = 18.02
   TM11 (27.7 μs/word) 200/27.7 = 7.22
   RP11 (7.5 μs/word) 200/7.5 = 26.66

3. Calculate the *total* number of transfers occurring within the window.

   TC11 = 1
   RK11 = 18.02
   RP11 = 26.66
   TM11 = 7.22

   Total = 52.90 transfers will occur within 200 μs window.

4. Calculate the time per transfer by dividing the total number of transfers into the window time.

   200 ÷ 52.9 = 3.78 μs/transfer rate

If this figure is greater than 2.5 μs*, the system should run without data lates. (This is approximately a rate of 400 kHz.)

3.3 PROPAGATION DELAY

If a voltage is supplied between any two conductors, they may be considered as a transmission line. The ideal transmission line input impedance looks like pure resistance but, in fact, is mainly a combination of capacitance and inductance (see Figure 3-3).

When the voltage at one end of the transmission line is changed, that change does not instantaneously appear at the other end. There is some delay, which is called propagation delay (see Figure 3-4). The propagation delay of BC11 Unibus cable is approximately 1.4 to 1.9 ns per foot (or .0348 m).

*Bus repeaters and bus switches will decrease the data rate supportable on the bus. A figure of 3.0 may be more applicable on a repeated line.

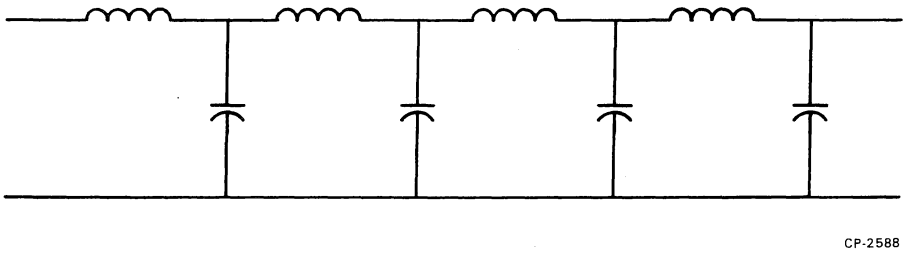


Figure 3-3 Transmission Line Circuit Example

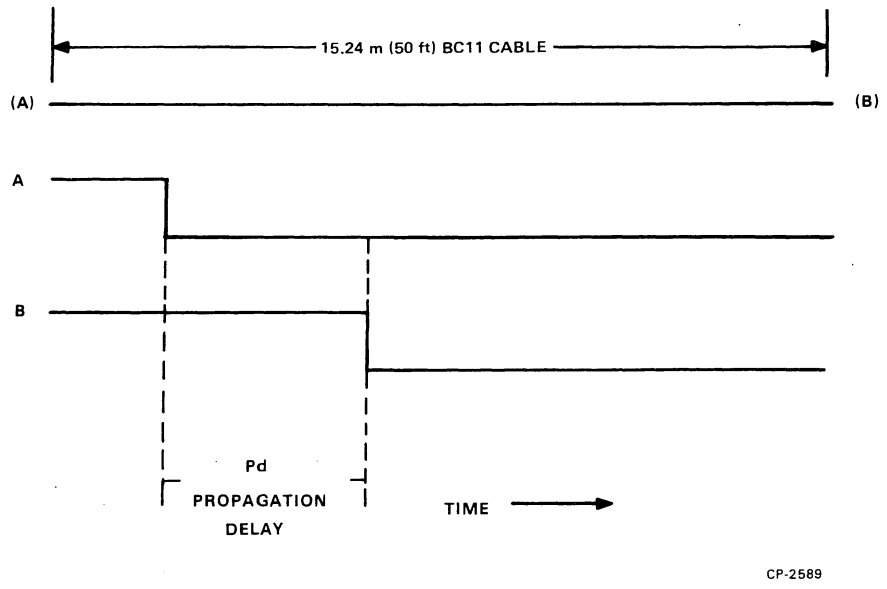


Figure 3-4 BC11-A Unibus Cable Delay Example

A lossless transmission line of infinite length looks like a pure resistance of value Z = L/C. If such a line is broken and terminated with a resistor of this value (R = Z), the line will behave like an infinitely long line, i.e., appear resistive (see Figure 3-5). The impedance (Z) of Unibus BC11 cable is approximately 120 ohms with Unibus foam and as low as 60-80 ohms unfoamed.

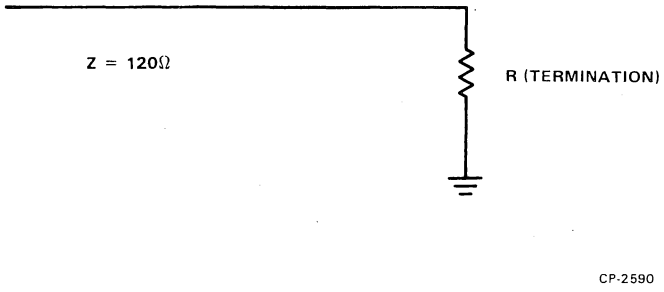


Figure 3-5 BC11 Unibus Cable Impedance Example

When a voltage is applied to the line, the instantaneous power consumed will be:

$$P = E^2/Z \qquad P = E^2/120$$

Suppose now that the terminating resistor (R) is not equal to the characteristic impedance of the line. The power which is traveling down the line *before* it reaches the termination (during propagation delay) is equal to E^2/Z, but the power dissipated in the resistor after propagation delay is approximately equal to E^2/R.

If resistance (R) is greater than the impedance (Z), there will be extra energy available at the termination and since energy cannot simply disappear, it will be reflected back into the line. After one more propagation delay (for the return journey), this reflection will be seen back at the source (see Figure 3-6A).

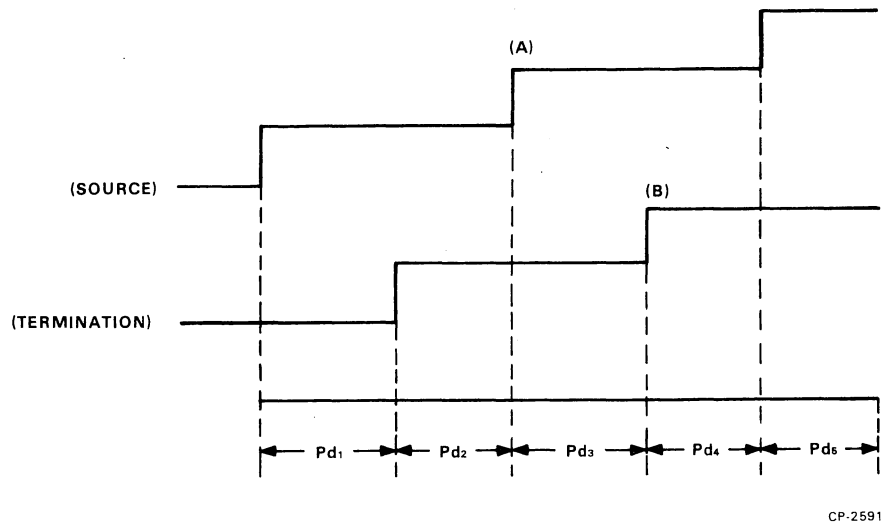


Figure 3-6 Impedance Mismatch Example

Some of this reflection will be dissipated by the source impedance and some will be re-reflected back into the line. When this re-reflection is seen at the termination (Figure 3-6B), (after still another propagation delay), the energy difference will be reflected back to the source. Eventually both source and termination will arrive at the same level. The important point to note here is that what was intended to be a level change with a clean transition did not turn out that way on the line due to a termination mismatch between R and Z.

Essentially the same situation occurs when the termination resistor is smaller than the characteristic impedance of the line. If resistance (R) is less than impedance (Z), there will be a mismatch and this will also be reflected back to the source (see Figure 3-7).

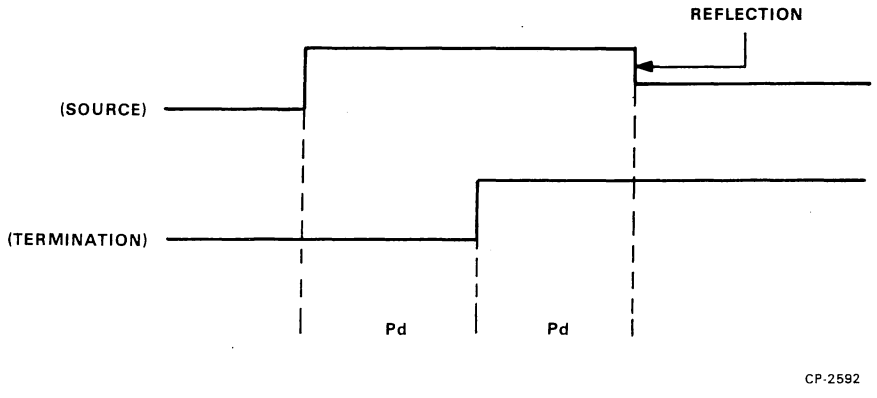


Figure 3-7 Impedance (Low Resistance) Mismatch Example

Note that: (a) transmission line which is not terminated in its characteristic impedance will have reflections and (b) the voltage seen at any point on the line or at any instant in time will be a combination of the incident and reflected voltage.

The amount of reflection depends on the mismatch, and approaches 100 percent for either a shorted or an open line (see Figure 3-8).

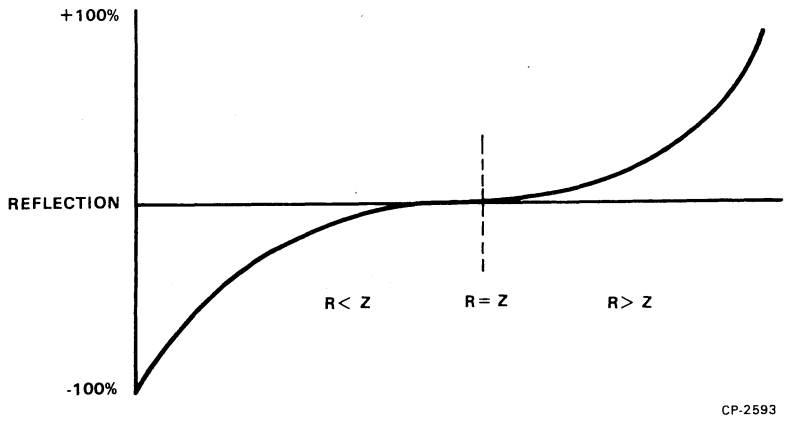


Figure 3-8 Mismatch Reflection Curve Example

Essentially the same thing happens on the negative going edge of a level change so that what seemed to be a clean transition as in Figure 3-9A, may look more like Figure 3-9B.

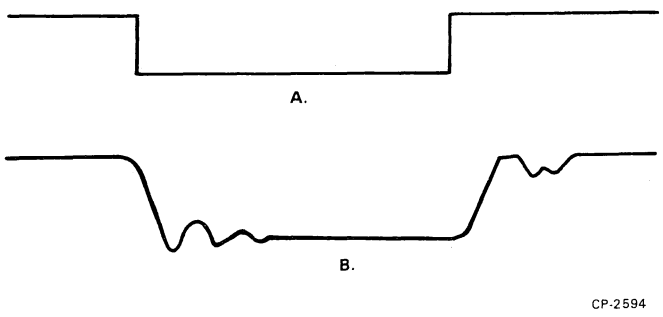


Figure 3-9 BC11 Unibus Cable Mismatch (Waveform Example)

To further compound the problem, each device in the bus contributes its own unique impedance and mismatch in complex time relationships (Figure 3-10).

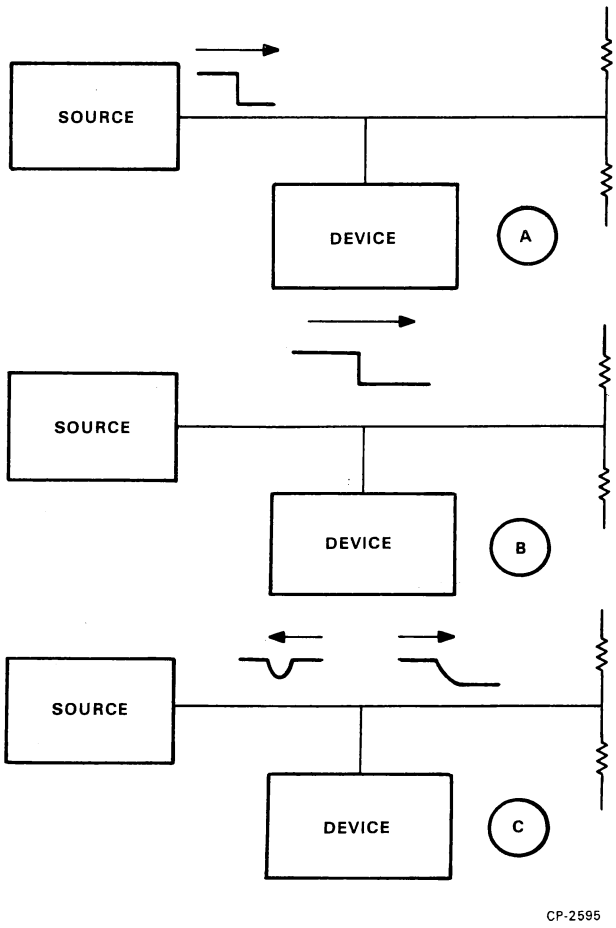


Figure 3-10 System Device Impedance Example

All of this impedance and resistance mismatch is normal and to be expected in Unibus systems. The objective here is to point out the possible impedance mismatch and how to use the appropriate tools to minimize the effects of reflections and "noise". Reference the techniques listed in the following paragraphs.

3.3.1 Line Termination Technique

The question may be asked, how can a 178 and 383 ohm resistor properly terminate a line which has an impedance of 120 ohms?

A perfect power supply has an ac resistance (impedance) of zero ohms, so for ac considerations the termination diagram changes somewhat to that shown in Figure 3-11B and simplified in Figure 3-11C.

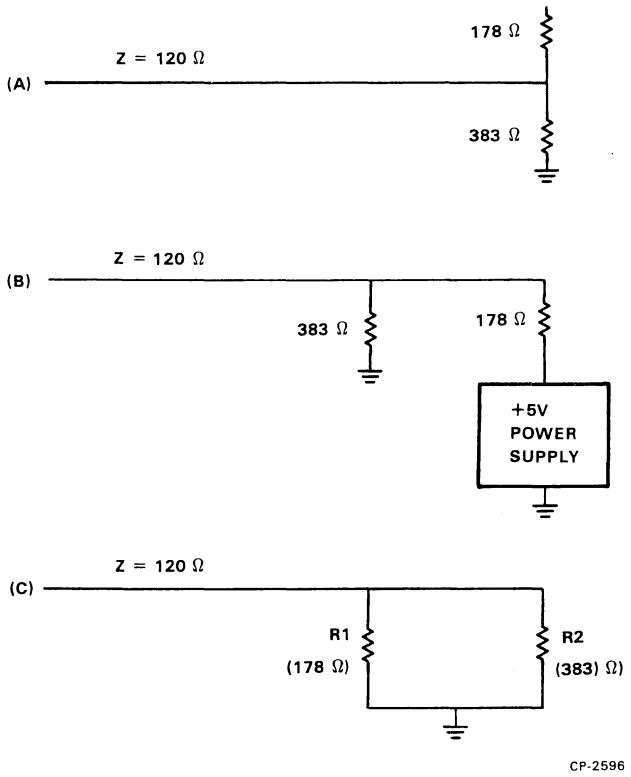


Figure 3-11 Line Termination Technique Example

The choice of these two values satisfies both the quiescent condition and the required termination impedance.

3.4 CABLE AND CONTACT RESISTANCE LOSSES

The threshold point at which a bus receiver switches (asserted) from a 0 to a 1 is approximately 1.3 V. If a driver cannot pull the line low enough to completely assert the line, erratic system operation will occur. There must be adequate low-threshold margin to prevent this problem.

In the asserted (low true) condition, wire and contact resistance may cause the input voltage at a receiver gate to be higher than the driver output.

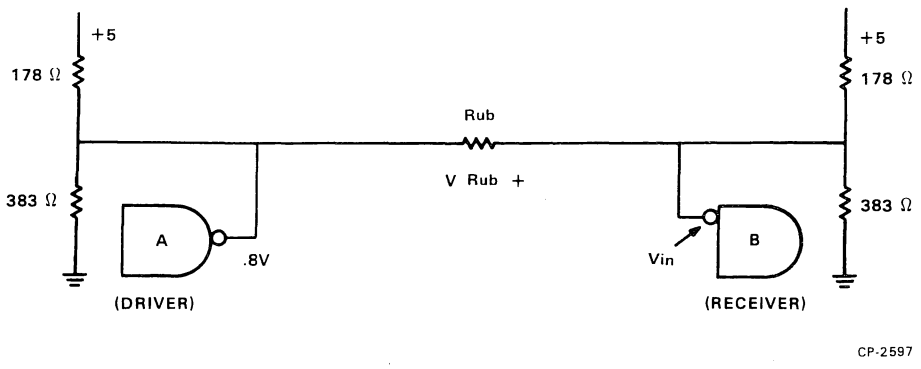


Figure 3-12 Cable Resistance Problems Example

Referring to Figure 3-12, assume a pure cable resistance of 0.6Ω/.3048 m (1 ft)* and ignore contact resistance (which would only aggravate the problem). If the cable between the driver (A) and receiver (B) were 15.24 m (50 ft), then R_{UB} = 30, or 0.6Ω × 15.24 (50) = 9.14 (30).

A voltage will be developed across R_{UB} with the polarity as indicated when the driver asserts the line. This voltage could be as great as 0.7 V.

V_{in} will not be 0.8 V, but instead

$$V_{in} = 0.8\ V + VR_{UB}$$

In this case, V_{in} might be as high as 1.5 V (0.8 +0.7) and erratic system operation may result. Unibus cable card contacts must be clean (to minimize contact resistance) and cable length should be as short as possible (to minimize wire resistance).

*BC11A cable is typically 0.1Ω/0.3048 m (ft). Considering the return path in addition to the signal line, cable resistance is approximately 0.2Ω/0.3048 m (ft) of cable length.

CHAPTER 4
BUS MARGINING

4.1 GENERAL

Experience has shown that a properly functioning Unibus will operate with terminator source voltages of between 4.2 and 7.0 volts without any adverse effects. If the voltage is varied between these values, it may be possible to detect and/or aggravate bus problems and thus make it easier to define and correct the failures. At present, there are two methods that can be used to change the quiescent levels on the Unibus for margining purposes.

1. Use a Unibus Voltage Margin Tester Box to vary the source voltage applied to the terminator network.

2. Use Hi/Lo Terminator Cards to vary the terminator network (rather than the voltage). The hardware required for this method is less expensive and more portable than the Unibus Voltage Margin Tester Box, however, this method is more difficult to use for troubleshooting Unibus failures.

NOTE

A third method, referred to in this manual as the single-ended margining techniques, is an extension of the UVM-TA method described in item 1. This method must be used for those processors that employ Sack turnaround or Bootstrap functions on the terminator cards.

4.2 BUS QUIESCENT LEVELS

Normal bus quiescent levels are listed in Table 4-1. Any level that deviates from the normal level should be considered as a potential failure. In many instances the improper level will be the result of either a defective bus receiver or driver. In the case of AC/DC LOW, these levels are power supply dependent.

Table 4-1 Bus Quiescent Levels

Signal	Quiescent Level
BG 7:4 NPG	+.45 V (±0.35)
AC Low	+4.9V (±0.35)
DC Low All Others (Except BBSY which depends on CPU type)	+3.4V (±0.2 V)

To measure quiescent Unibus levels:

1. Turn the system on with the processor halted. Press the START key and release it (with HALT down).

2. Use a *calibrated* oscilloscope (or voltmeter) to measure the Unibus signal lines. (See chart of Unibus slot backplane pins, Figure 4-1.)

NOTE

To obtain meaningful readings of bus grant lines (BG 4:7 and NPG), they should be measured at the grant input of each device down the length of the bus.

All buses should be checked in multiple bus systems.

4.2.1 Quiescent Conditions

Low true lines: (Address, Data, Control and Arbitration)

The low true Unibus lines are characterized by a termination at both ends and some number of "loads" determined by the system configuration as shown in Figure 4-2.

In the quiescent conditions we are dealing with dc levels. Ignoring loads for a moment, consider the equivalent Unibus line circuit based on termination alone as shown in Figure 4-3.

The quiescent dc level on the line may be calculated using Ohms law, where:

$$I = E/R1+R2 = I = 5/89+191.5 = 0.0178A$$

$$E = (I \times R2) = 0.0178 \times 191.5 = 3.4087\ (3.41)\ \text{volts}$$

If the potential on the line were measured (with respect to ground), it would be 3.41 volts as shown in Figure 4-4.

In theory, the loads should not affect the quiescent level of the bus lines, but in practice this is impossible to achieve. To be considered acceptable, one load cannot contribute more than 210 μA of leakage current (see Chapter 2 for definition of dc unit load), but even this level will have an effect on the quiescent level of the line.

If 20 loads are added to the original example (Figure 4-5), with each drawing 210 μA of current, the calculation changes somewhat.

$$(20 \times 210\ \mu A = 0.0042\ \text{amps of leakage current})$$

The total current through R1 now increases which increases the 1R[1] drop.

The quiescent level of the line will now be approximately 3 volts.

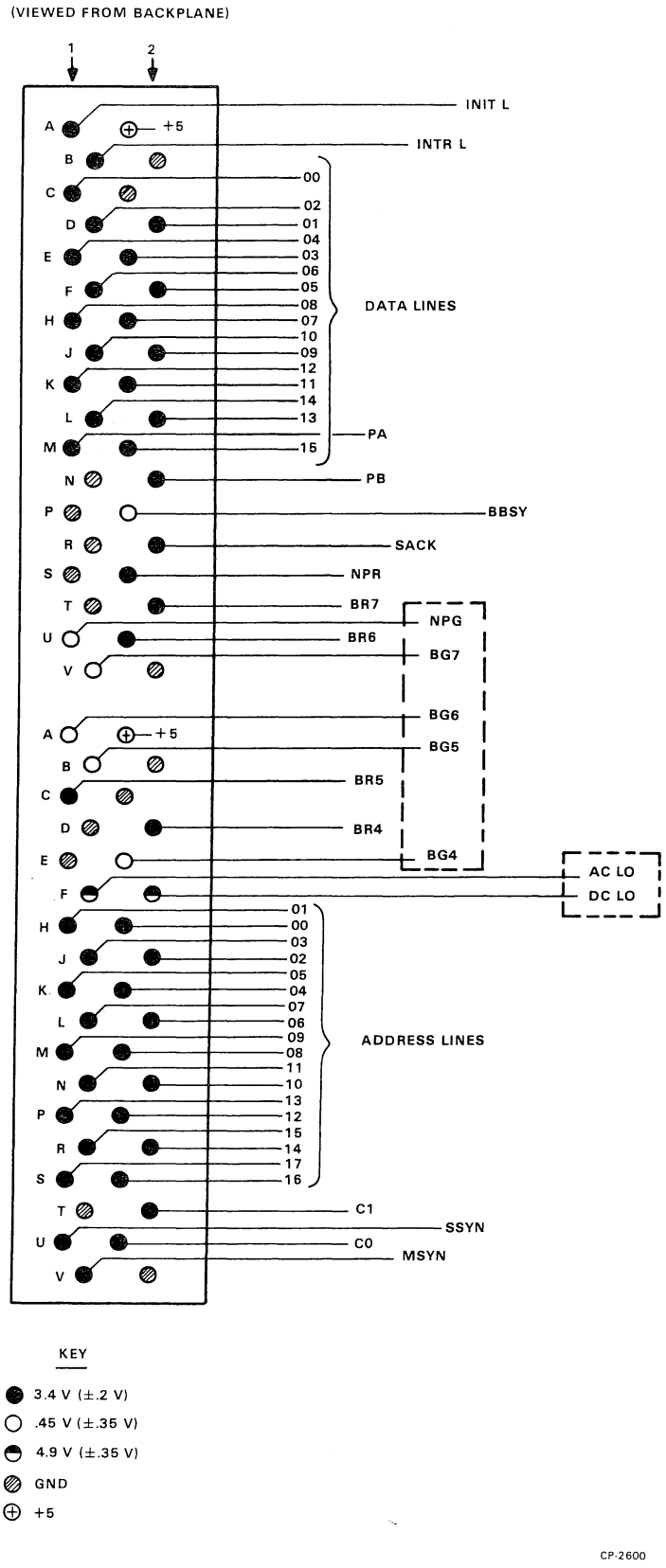


Figure 4-1 Unibus Slot Backplane Signals

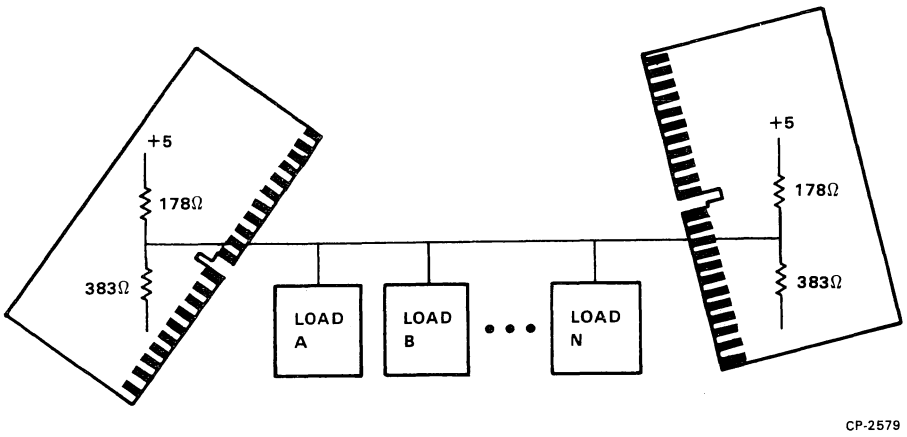


Figure 4-2 Low True Unibus Line

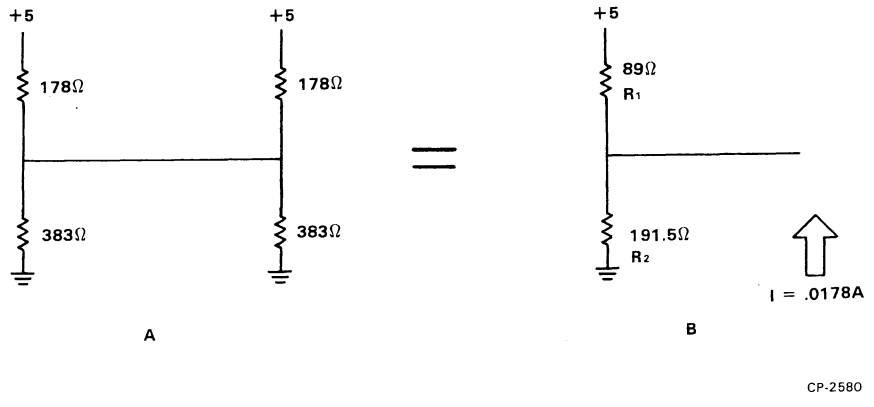


Figure 4-3 Equivalent Unibus Line Circuit

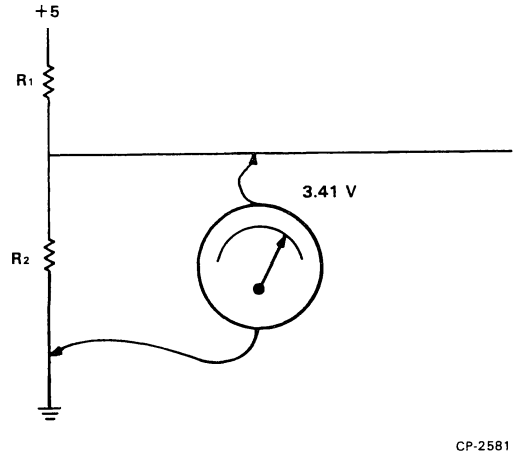


Figure 4-4 Quiescent dc Level Example

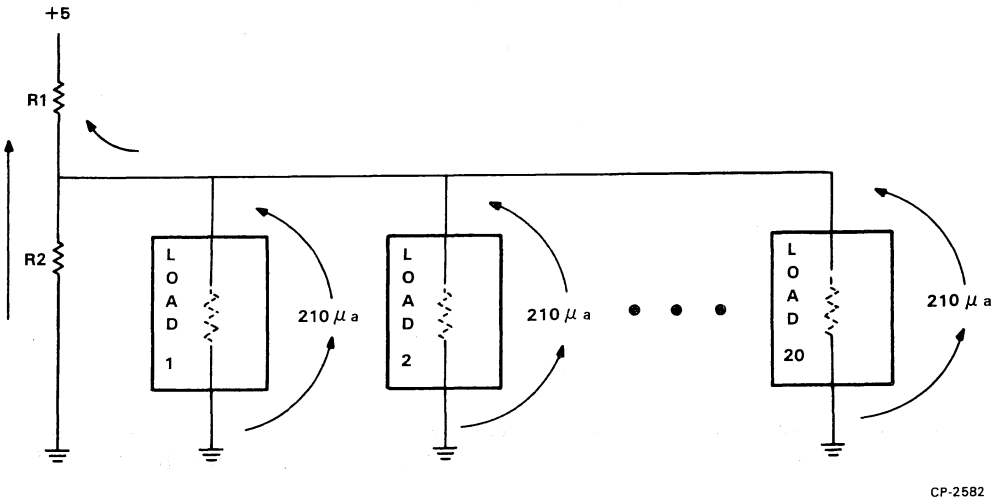


Figure 4-5 Load Current Leakage Example

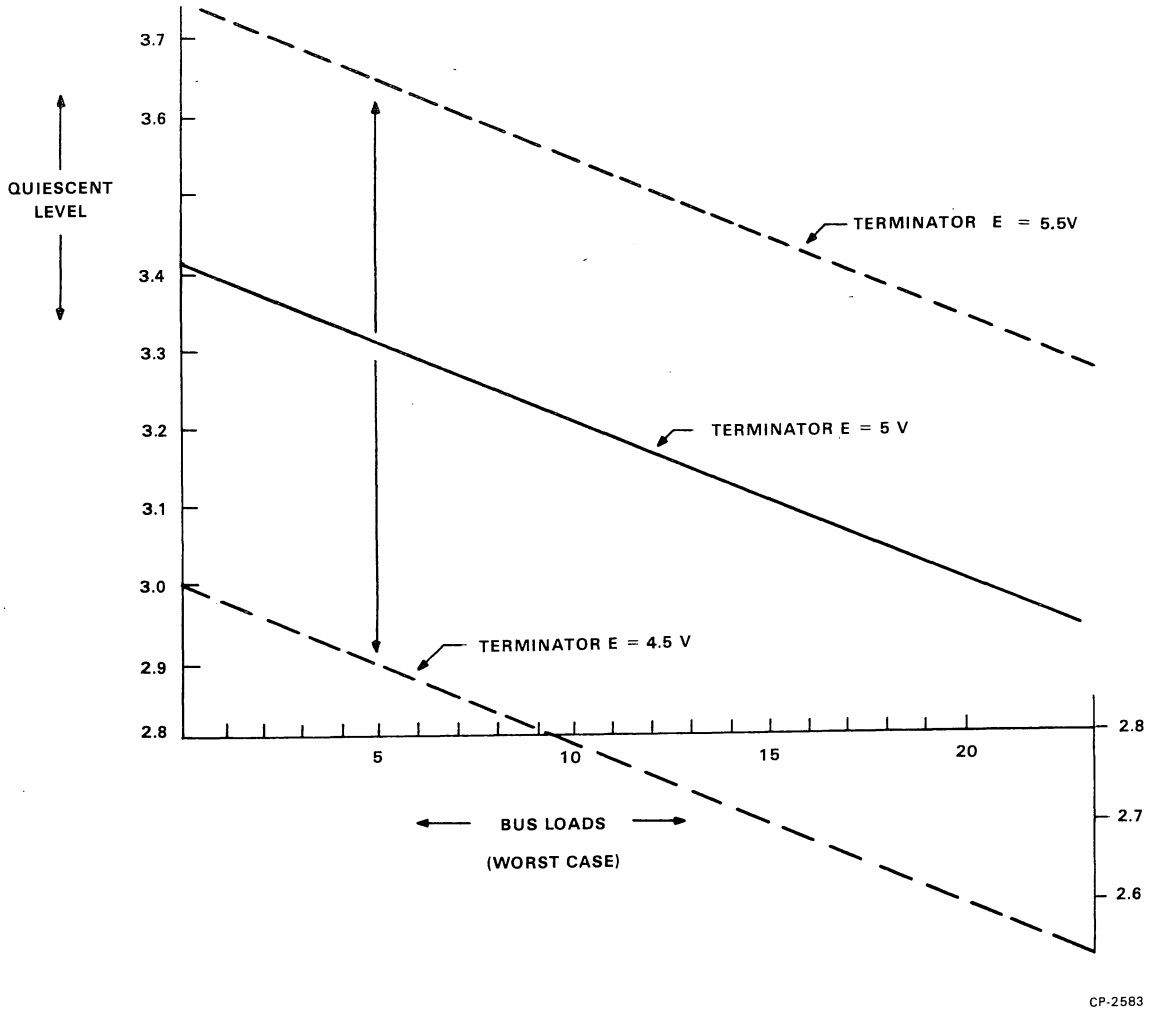


Figure 4-6 Quiescent Level vs. Bus Loading (Worst Case)

By Unibus convention, these lines are asserted true when low (=1) and negated when high (=0). The threshold point at which a receiver switches from a one to a zero is approximately 2.5 V using a DEC 380 Receiver Module (or 1.7 V with an 8640 Receiver Module). If enough loading is present to force the quiescent level low enough (see Figure 4-6), system operation may become extremely erratic. (There must be an adequate noise margin above the threshold level to allow for crosstalk and reflections.)

4.2.2 Multiple Bus System Considerations

Multiple bus systems are those which include bus repeaters or bus switches; the entire Unibus is re-propagated (see Figure 4-7). When margining techniques are employed with multiple bus systems, it is desirable to margin all bus sections on an individual basis. (It is not necessary to margin multiple buses simultaneously.)

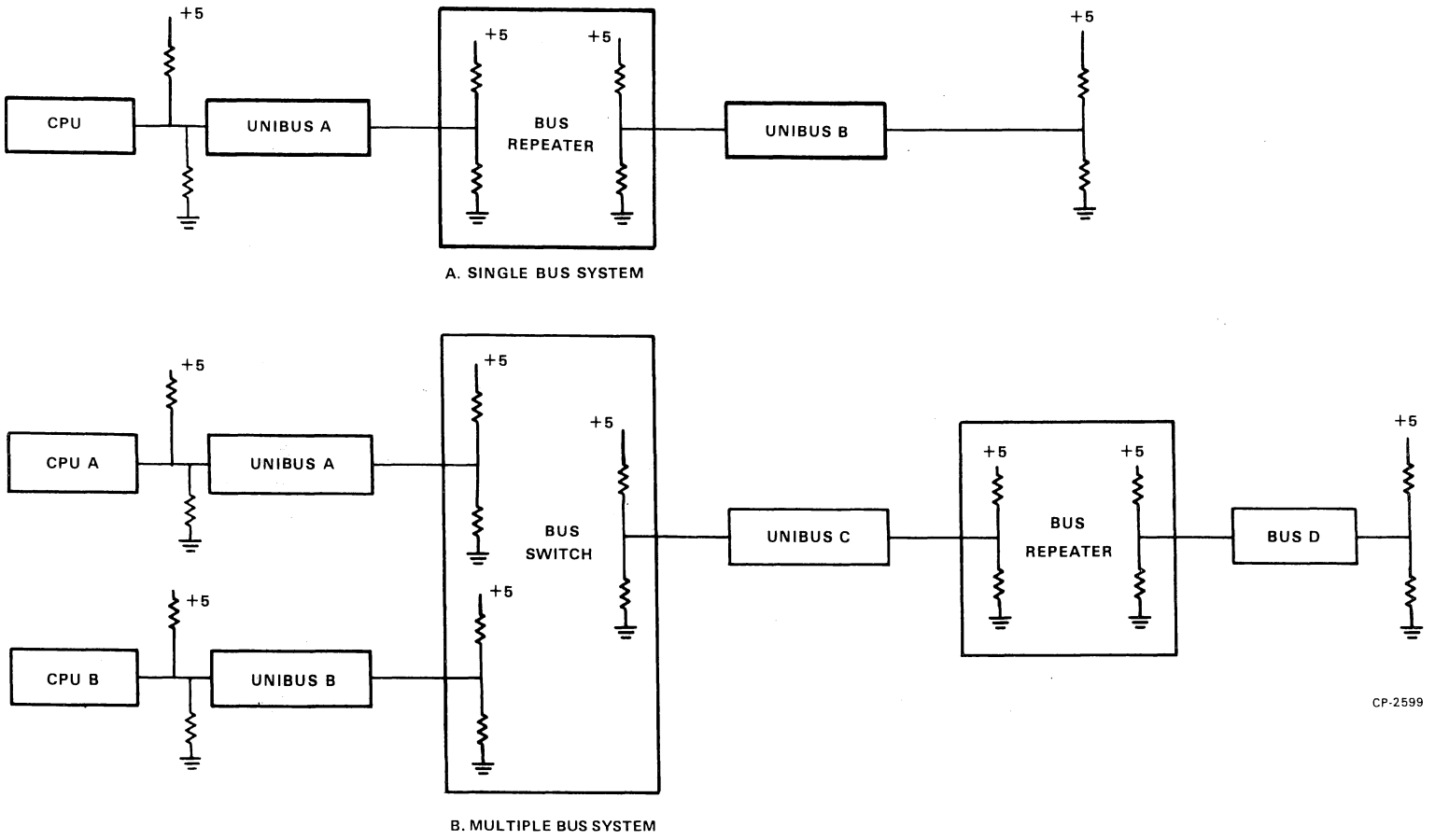


Figure 4-7 Margining Multiple Bus Systems

It is important that the correct termination points are used for any given bus in a system – *do not guess.* Refer to the module utilization prints to determine which terminators go with which bus.

4.2.3 Grant Line Termination

The grant lines on the Unibus represent a special case of termination and assertion levels (high = true).

Grant lines may not always run from one physical end of the bus to the other. The Grant line is broken at each device wired to it and repropagated if that device is not requesting (see Figure 4-8). It should be noted that changing the bus quiescent levels at the terminator will not affect grant lines which have been repropagated. To measure the quiescent level of grant lines or to observe grant line waveforms, it is necessary to check at the specific point of interest.

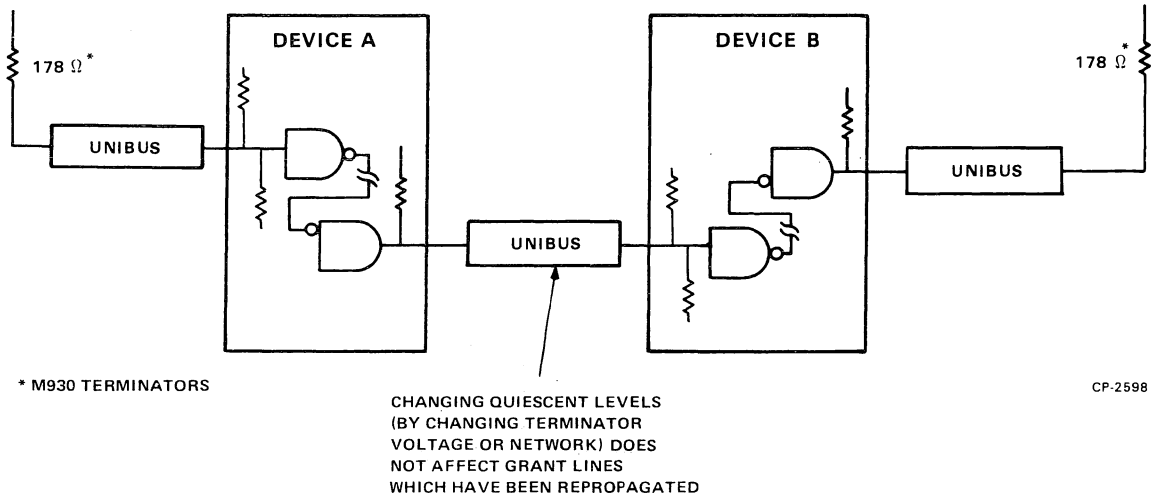


Figure 4-8 Grant Line Bus Margining Technique

4.3 HI/LO TERMINATOR BUS MARGINING

The Hi/Lo Terminator cards (see Figure 4-9) are designed to test the high and low bus margining voltages by varying the terminator network (rather than varying the voltage when using the UVM-TA tester). The M930 terminators must be removed from the system under test and be replaced by M9304 low margin or by the M9304-YA high margin terminator cards.

There is a special terminator used in the 11/35 and 11/40 processors which combines the functions of a terminator and a unibus jumper module (M981). There are Hi/Lo terminator cards to fit this application also (M9305 low margin and M9305-YA high margin).

Margin terminators are used as a go/no go test and are *not* to be installed in the system on a permanent basis. (They are too lar ge to fit in an expander box with the covers closed which will help avoid this mistake.) Figure 4-10 illustrates the circuit representation of the Hi/Lo terminator cards plus representative load values.

WARNING

When using special terminators, it is important that the same type (Hi or Lo) be installed at both ends of the bus for the test to have meaning.

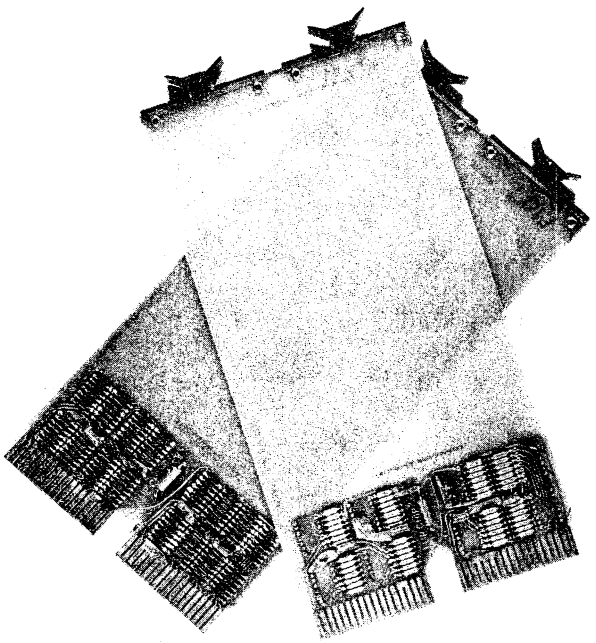


Figure 4-9 Margining Cards

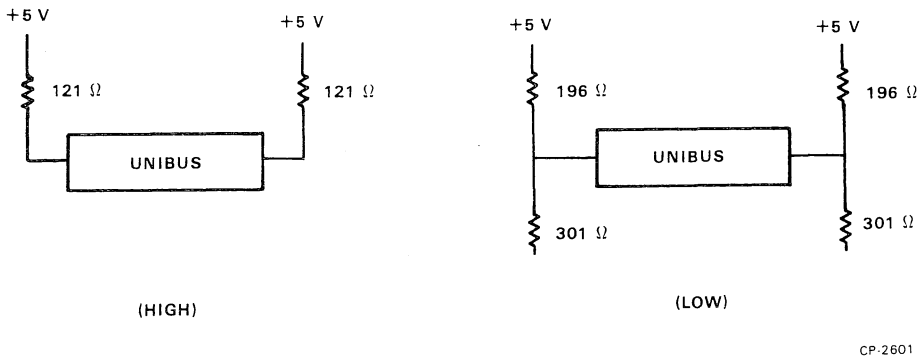


Figure 4-10 Hi/Lo Terminator Circuit Example

High Margin

1. M9304-YA
   (Replaces the M930 Terminator)
2. M9305-YA
   (Replaces the M981 special case 11-35/11-40 terminator)

Quiescent = 5 V–(1R drop caused by loads)

Failures here usually caused by weak drivers, receiver with marginal threshold or dirty bus cable contact fingers.

Low Margin

1. M9304
   (Replaces the M930)
2. M9305
   (Replaces the M981 special case 11-35/11-40 terminators)

Quiescent = 3.03–(1R drop caused by loads)

Failures here usually caused by a receiver with marginal threshold or reflections on MSYN, SSYN, INTR, BBSY.

4.4 UNIBUS VOLTAGE MARGIN TESTER BOX

The Unibus Voltage Margin Tester (UVM-TA) is a portable tester designed to check all Unibus receivers and drivers in a system, either singly or as a group. Figure 4-11 illustrates the circuit representation of the UVM-TA plus representative load values. The control panel (Figure 4-12) furnishes a switch for each of the designated bus signals and is used to provide fixed (+5 V) or variable termination voltage to special terminator boards (called Margining Heads – M9303) which are used in place of the standard M930 terminators. The margining heads cards allow the voltages selected to be applied to each terminating network on an individual basis. Refer to Figure 4-13 for a block diagram overview of the UVM-TA.

NOTE

This does not change the effective Unibus length.

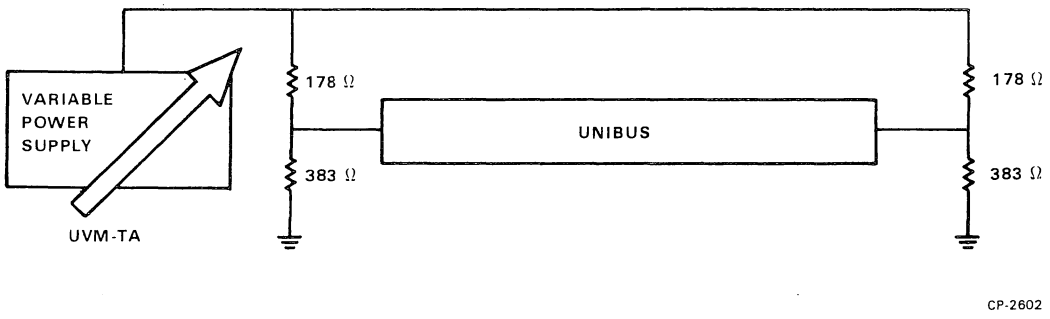


Figure 4-11 UVM-TA Circuit Representation

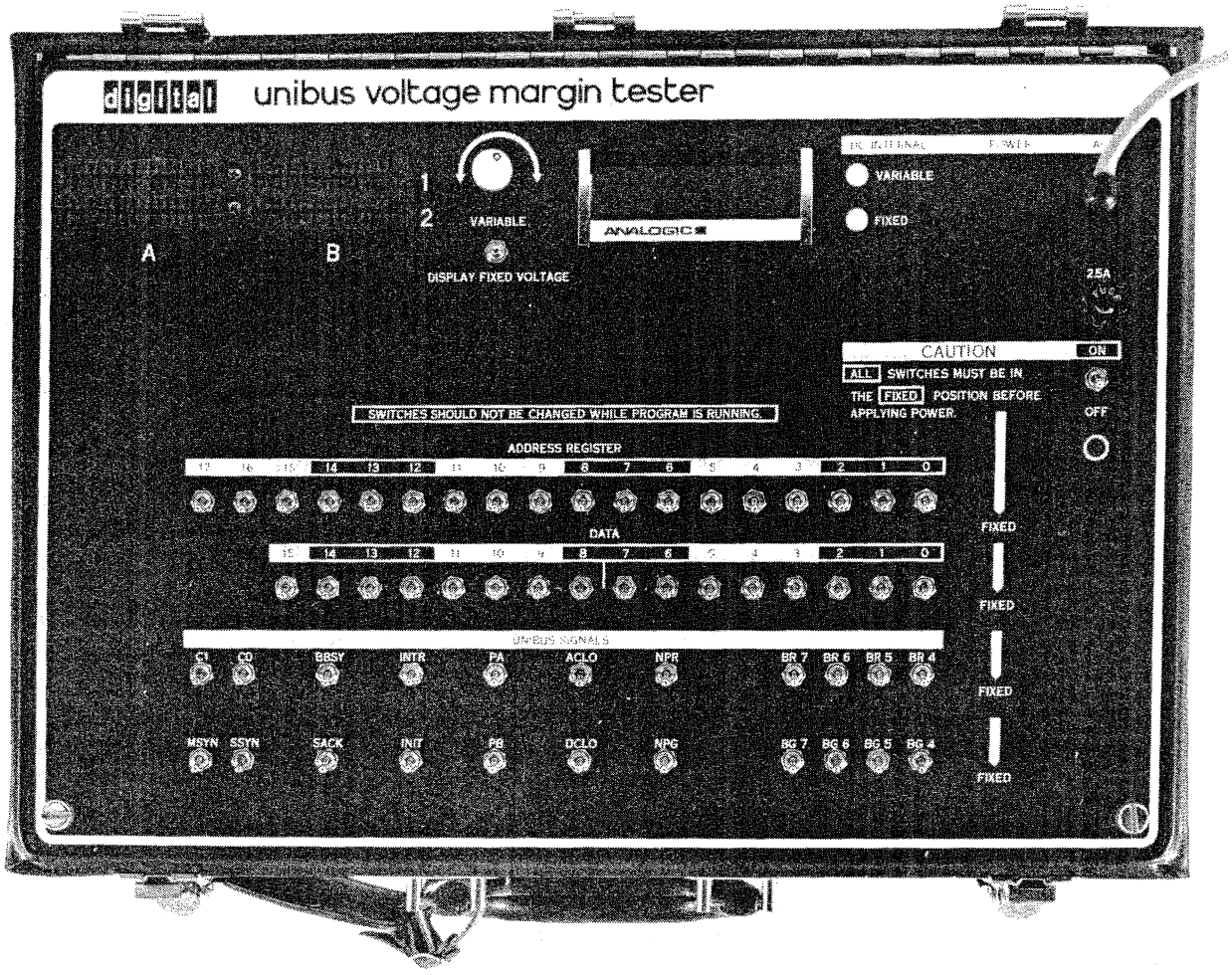


Figure 4-12 Controls and Indicators

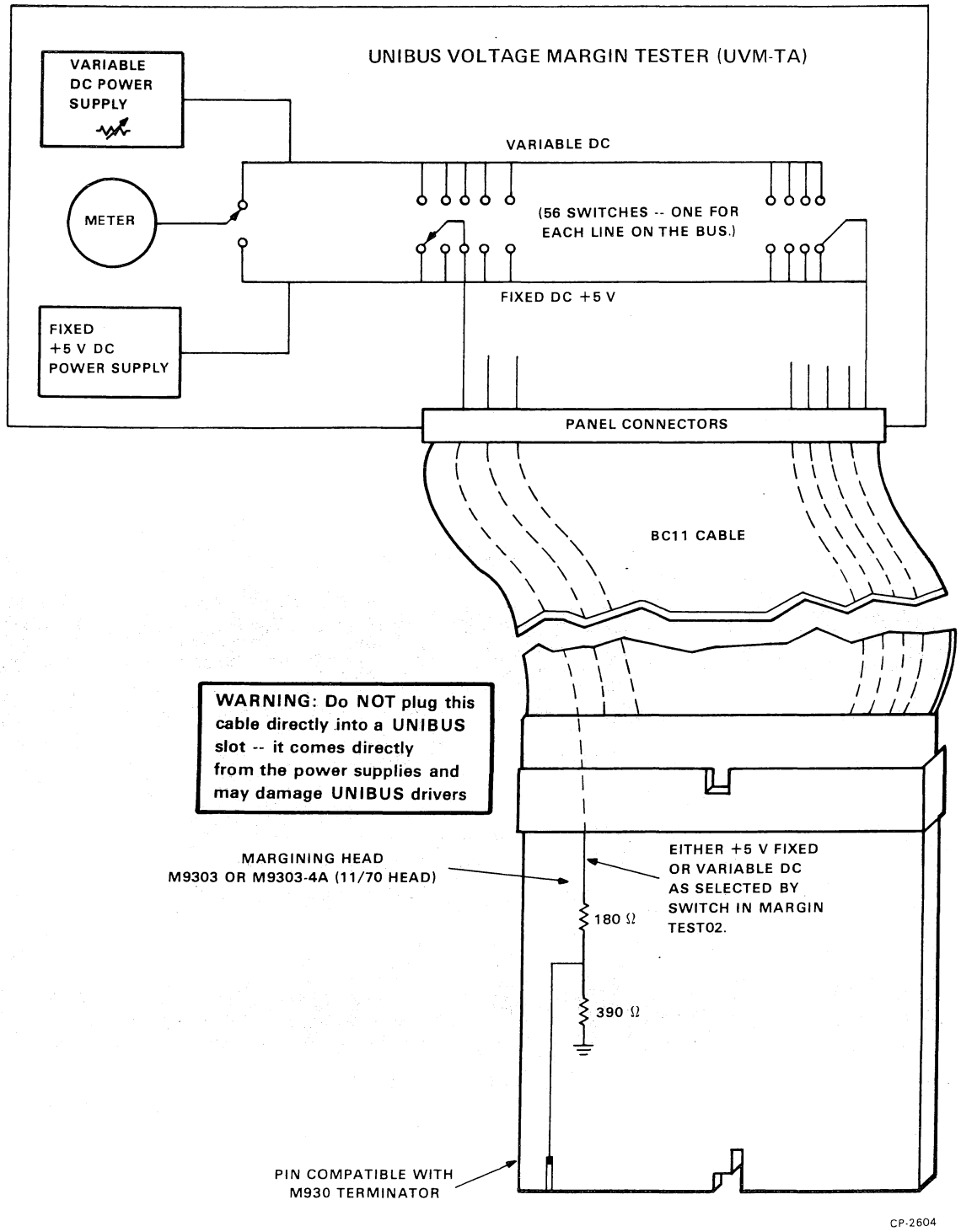


Figure 4-13 UVM-TA Block Diagram

4.4.1 Functional Description

Functionally the UVM-TA consists of a fixed supply, a variable supply, a control panel, Unibus cables, and terminator cards that enable the user to margin voltages in the Unibus sections.

NOTE

The use of the Unibus cable with this tester is as a power transmission cable.

The fixed supply provides the voltage for normal system operation. The variable supply (when selected) provides the variable voltage, for system margining purposes. The front panel controls and indicators control the choice of fixed or variable voltage, vary the voltage, display the voltage, indicate both ac and dc power on, and select individual Unibus signal lines.

CAUTION

This Unibus cable must never be plugged directly into a CPU, option or peripheral while connected to the tester – it should be plugged into the margining head only.

With the recommended program (DECX11 or operating system) running in the system, the user now selects any or all lines to be margined. The respective switches should be placed in the VARIABLE position. The margin voltage can then be varied by using the VARIABLE potentiometer. The voltage level at which the system fails or when the limits of the supply are reached, may be obtained by viewing the metered display.

4.4.2 UVM-TA Operation and Test Procedures

1. Unlatch and remove the top cover from the suitcase tester and place to one side. This allows room for the cabling to be connected into the tester box.

2. Remove test heads M9303, M9303-YA and BC11-A from inside the top cover pocket. Place all signal switches (56 total) in the "down" or FIXED position. Place power switch in the OFF position.

3. Turn system power off. Remove the M930 terminators from both ends of a section of bus in the unit under test and replace with the M9303 margining heads (M9303-YA for 11/40 CPUs).

4. Plug the Unibus cable (BC11A) into the margining heads.

5. Plug the (BC11-A) power cable into the margining heads. Plug the BC11-A cable into tester slots 1 and 2.

CAUTION

Plugging the BC11-A Unibus cable directly into a CPU or peripheral without the test heads M9303-YA may cause the Unibus drivers to burn up.

6. Plug tester box ac cord into a convenient power source. Power can now be applied to the system and the tester.

7. Place power switch in the ON position and adjust the variable voltage to +5 V.

8. Load recommended programs (DECX11 or operating system).

NOTE

Signal switches must not be switched while the system is running. Always halt the system before attempting to change selection switch setting.

There is one switch for each of the designated bus signals and is labeled on the tester box control panel. By setting a switch in the VARIABLE "up" position, the margin voltage displayed is applied to the individual pull-up resistors and thus the signal lines can be margined by varying the VARIABLE potentiometer.

9. With the system halted, put *all* (56) bus signal switches in the VARIABLE "up" position. Restart system running the selected program. Adjust the variable voltage to 6 V and run system for 15 minutes (or longer) with all options selected. Then, increase in .5 V steps (or smaller increments if necessary) until the failure occurs. Record this value.

CAUTION

Halt and restart the program each time a new voltage is selected when running DECX11.

10. Adjust variable voltage to 4.5 V and run system for 10 minutes (or longer). Then, decrease in .5 V steps (or smaller if necessary) until a failure occurs. Record this value.

CAUTION

Halt and restart the program each time a new voltage is used when running DECX11.

11. Every system *must* run between 4.2 V and 7 V. If a system failure occurs, margin the following five signals only:

    SSYN, MSYN, INTR, SACK, BBSY

12. If it is not one of these signals that failed, continue to margin sections of the bus until a line failure or group of lines is isolated as the problem area. Repair the defective line and recheck the margins for:

    a. Low byte data
    b. Address and C lines
    c. Request lines (NPR/BR)
    d. High byte data
    e. Remaining lines

13. When tests are complete, turn power off, remove the special test equipment, replace the terminator cards and remove tester from power source.

4.5 SINGLE-ENDED MARGINING

For some processors, it is not possible to use the M9303 series of margin heads with the voltage margin tester. This is because some machines include additional hardware on the terminator module (boot-strap function, sack turnaround, etc.) which must be present for the machine to operate normally. For these machines, a single-ended margining technique has been developed (PDP-11/04; 11/34). This technique may be used with any Unibus machine.

Single-ended margining is accomplished by placing a voltage margin terminator on only *one* end of a bus segment and varying the voltage applied to it ((see Figure 4-14). This accomplishes the same results, but the considerations are slightly different.

NOTE

Using the M9308 single-ended margin terminator, a system should operate successfully between 7.85 V (high margin) and 2.93 V (low margin) as displayed by the panel meter on the voltage margin tester.

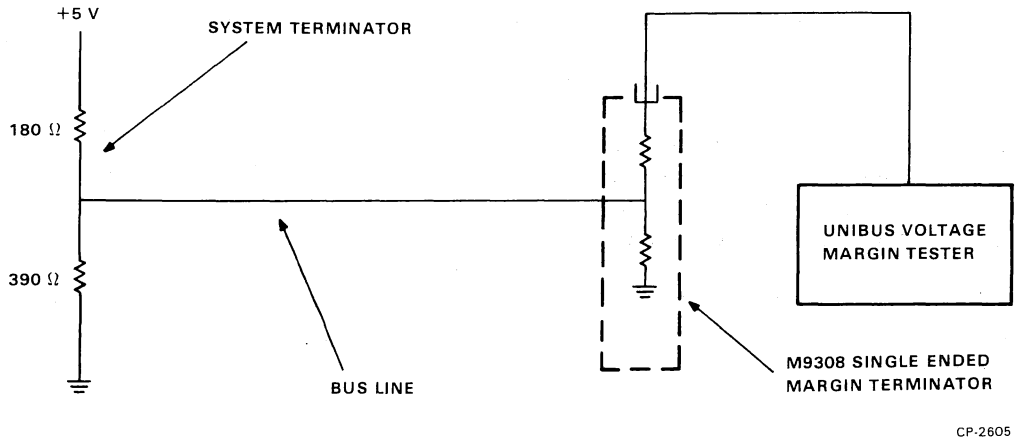


Figure 4-14 Single-Ended Circuit Example

4.5.1 Setup and Operation (Using M9308 Single-Ended Margin Head)

1. Unlatch and remove the top cover from the suitcase tester and place to one side. This allows room for the cabling to be connected into the tester box.

2. Remove test head M9308 and BC11-A from the inside cover top pocket. Place all signal switches (56) in the "down" or FIXED position (↓). Place power switch in the OFF position.

3. Turn system power off. Remove the M930 system terminator (see application table) and install the M9308 margin head. If the M9308 is not used at the electrical end of the bus, disable SACK turnaround with the switch located on the M9308 module.

4. Plug the Unibus cable (BC11A) into the M9308 margining head.

CAUTION

Connecting the BC11 power cable directly into a CPU or peripheral without the margin head may cause equipment damage.

5. Connect the BC11 power cable into tester slots 1 or 2.

6. Plug tester box ac cord into a convenient power source. Power may now be applied to the system and the tester.

7. Place power switch in the ON position and adjust the variable voltage to +4.34 V.

8. Load recommended programs (DECX11 or operating system).

NOTE

Signal switches must not be switched while system is running. Always halt the system before attempting to change selection switch setting.

There is one switch for each of the designated bus signals and is labeled on the tester box control panel. By setting a switch in the VARIABLE "up" position, the margin voltage displayed is applied to the individual pull up resistors – thus, the signal lines can be margined by varying the VARIABLE potentiometer.

9. With the system halted, put all (56) bus signal switches in the VARIABLE position. Adjust variable voltage to 6 V and restart system running program selected. Then, increase in .5 V steps (or smaller increments, if necessary) until a failure occurs. Record this value.

CAUTION

Halt and restart the program each time a new voltage is selected when running DECX11.

10. Adjust variable voltage to 4.0 V and run system for 10 minutes or longer. Then, decrease in .5 V steps (or smaller, if necessary) until a failure occurs. Record this value.

CAUTION

Halt and restart the program each time a new voltage is used when running DECX11.

11. Every system must run between 2.93 V and 7.85 V. If system failure occurs, margin the following five signals only:

SSYN, MSYN, INTR, SACK, BBSY

12. If the problem is not with one of the above signals, continue to margin sections of the bus until a failing line or group of lines is isolated as the problem area. Repair the defective line and recheck margins for:

    a. Low byte data
    b. Address + C lines
    c. Request lines
    d. High byte data
    e. Remaining lines

13. When tests are complete, turn power off, remove the special test equipment, replace the terminator module and remove tester from ac power source. If margin values are recorded for future use, be sure to note that these values were obtained with single-ended techniques.

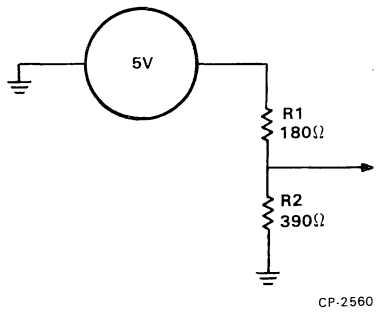
4.5.2 Single-Ended Circuit Consideration

The user of the single-ended margining technique should be aware of the theory and application of the Quiescent Voltage versus UVM-TA Voltage considerations. Calculations are not necessary because Figure 4-15 is designed to provide this information. However, the difference must be made between single-ended and double-ended margining techniques because of the different voltages that must be applied by the UVM-TA tester under these conditions.

Table 4-2 supplies terminator application data for the M9308 single-ended margin head plus double-ended terminators, and how they relate to particular CPU bus segments. In bus segments not including a CPU, the same procedures apply.

According to Thevinen's Theorem, any line or network of impedance and generators, when viewed from any two points in the network, can be replaced by an equivalent voltage source and an equivalent impedance in series. As an example, consider the termination network used on the M930 Unibus terminator.

The voltage looking "back" into the network will be 3.42 V because of the voltage divider action of R1 and R2. This is an equivalent voltage source of 3.42 V.



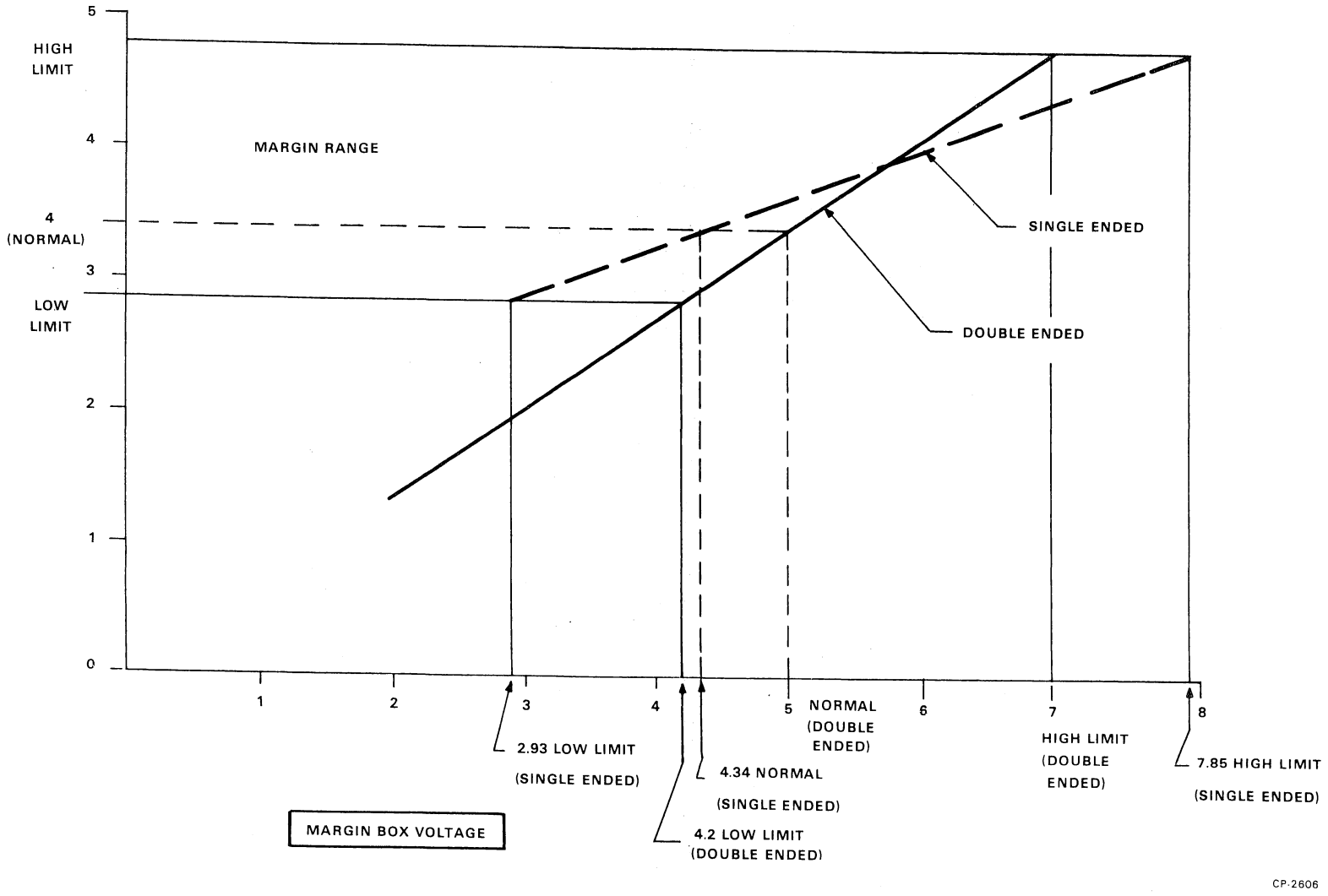
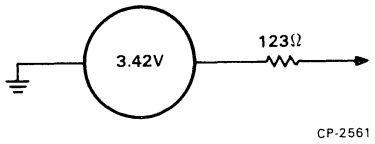


Figure 4-15 Quiescent Voltage vs UVM-TA Voltage

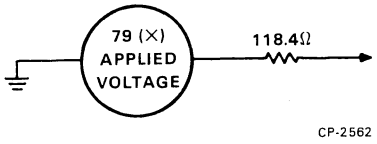
Table 4-2 Terminator Application Data

<table>
<tr><th></th><th>M930</th><th>M9300</th><th>M9301 (YA–YD)</th><th>M9302</th><th>M9303</th><th>M9304</th><th>M9305</th><th>M9306</th><th>M9308</th><th>M981</th></tr>
<tr><td></td><td>Standard Terminator</td><td>Used on RH11</td><td>Bootstrap Terminator YA–YD = Various Bootstrap Progs.</td><td>SACK turn around logic</td><td>Margin Head– Used w/ Bus Margin Tester</td><td>Fixed Margin Term.</td><td>Fixed Margin Term.</td><td>"Magic" Backplane Terminator</td><td>Single-Ended Margin Terminator</td><td>Bus Jumper + Terminator</td></tr>
<tr><td>11/03</td><td colspan="9">Non-Unibus Machine – Terminated on M7264 Module (Expansion Configurations use M9400-XX Terminator)</td><td></td></tr>
<tr><td>11/04</td><td></td><td rowspan="5"></td><td>Near End REQUIRED</td><td>Far End REQUIRED</td><td rowspan="3">Near and Far end– Used with Bus Margin tester and double-ended technique</td><td rowspan="3">Near and Far end fixed-margin technique</td><td rowspan="3"></td><td>Near End w/Opt sw. Panel</td><td rowspan="5">Far End Margin Term. for use with Bus Margin tester and single-ended margin technique</td><td rowspan="5"></td></tr>
<tr><td>11/05
11/10</td><td>Both Ends</td><td>OPTIONAL Near End</td><td>OPTIONAL Far End</td><td>OPTIONAL Either end</td></tr>
<tr><td>11/15
11/20
11/21</td><td>REQUIRED Near End (Mech.)</td><td rowspan="3">OPTIONAL Far End</td><td rowspan="3">OPTIONAL Far End</td></tr>
<tr><td>11/34</td><td></td><td rowspan="2">M9303-YA Near End For Margin</td><td rowspan="2">Far End For Margin</td><td rowspan="2">Near End For Margin</td><td rowspan="2">REQUIRED Near End</td></tr>
<tr><td>11/35
11/40</td><td>Far End</td></tr>
<tr><td>11/45
11/50
11/70</td><td>Both Ends</td><td>OPTIONAL Either End</td><td>OPTIONAL Far End</td><td>Near and Far end For Margin</td><td>Near and Far end For Margin</td><td></td><td>OPTIONAL Either End</td><td></td></tr>
</table>

The Thevinen equivalent impedance, R_{Th} of the circuit is found by shorting the generator and calculating the circuit impedance.



The equivalent voltage source can be represented by a circuit consisting of a 3.42 V source in series with an impedance of 123.157 ohms.



The termination network used on the M9308 single-ended margin terminator consists of 180 ohms to the voltage source and 562 ohms to ground (see Figure 4-16).

If this network is considered a Thevenin generator, it becomes a source of 78.9 percent × voltage applied (because of the voltage divider action) in series with 118.4 ohms.

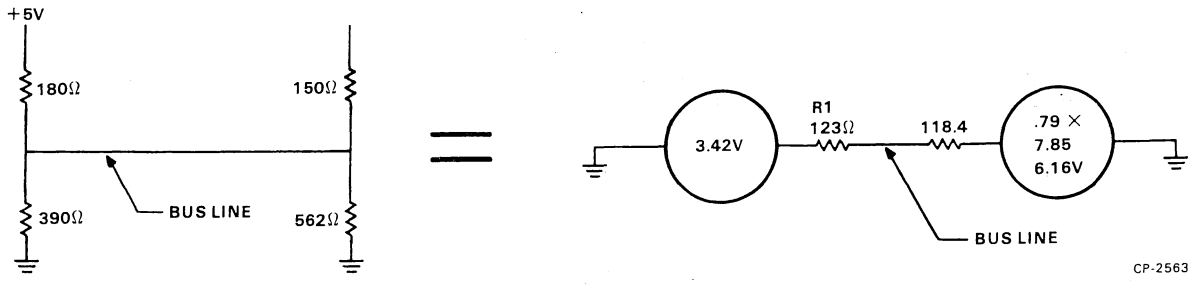


Figure 4-16 M9308 Termination Circuit Example

The voltage seen on the bus line may be computed by considering what happens when these two generators are connected together. For example, if the M9308 has 7.85 volts applied to it:

1. $E = 6.16 - 3.42 = 2.74$ V
2. R_T 123Ω + 118.4Ω = 241.4Ω
3. $I = E/R = 11.35$ mA
4. Voltage drop across R_1 = 11.35 mA × 123Ω = 1.396 V
5. Voltage on the bus line = 3.42 + 1.396 = 4.8 V

In this application (since the Thevenin equivalent impedances are similar), a simple rule of thumb is:

3.42 + (0.79 × UVM–TA)/2 = V bus line

4.5.3 SACK Timeout

In some processors, if SACK is not received within ten ms after a grant is issued, the processor will timeout and proceed as if no grant had been issued (unless, of course, a request line continues to be asserted). In others, the processor will continue to wait for the return of sack; this will cause the bus to hang. This problem is solved on some terminators by turning bus grant around and sending SACK back to the CPU. The processor will then release BBSY and, if no device is requesting, will immediately regain control of the bus through the passive bus release mechanism. The M9308 margin head will turn bus grant around into SACK and set a latch. There is a LED installed on the M9308 to "remember" the fact that a grant was received (not a normal condition at the end of the bus). Switches are provided to enable SACK turnaround and reset the latch (see Figure 4-17).

NOTE

If SACK turnaround is enabled, the M9308 must be used at the electrical end of the bus.

4.6 MODIFYING M930 TERMINATOR CARD

If the test equipment previously described is not avilable, it is still possible to employ voltage margining techniques.

4.6.1 Equipment Required

1. Variable dc power supply with a 1 percent a regulation (or better) and a 2 amp output rating (minimum).
2. Modified M930 Terminators (two each).

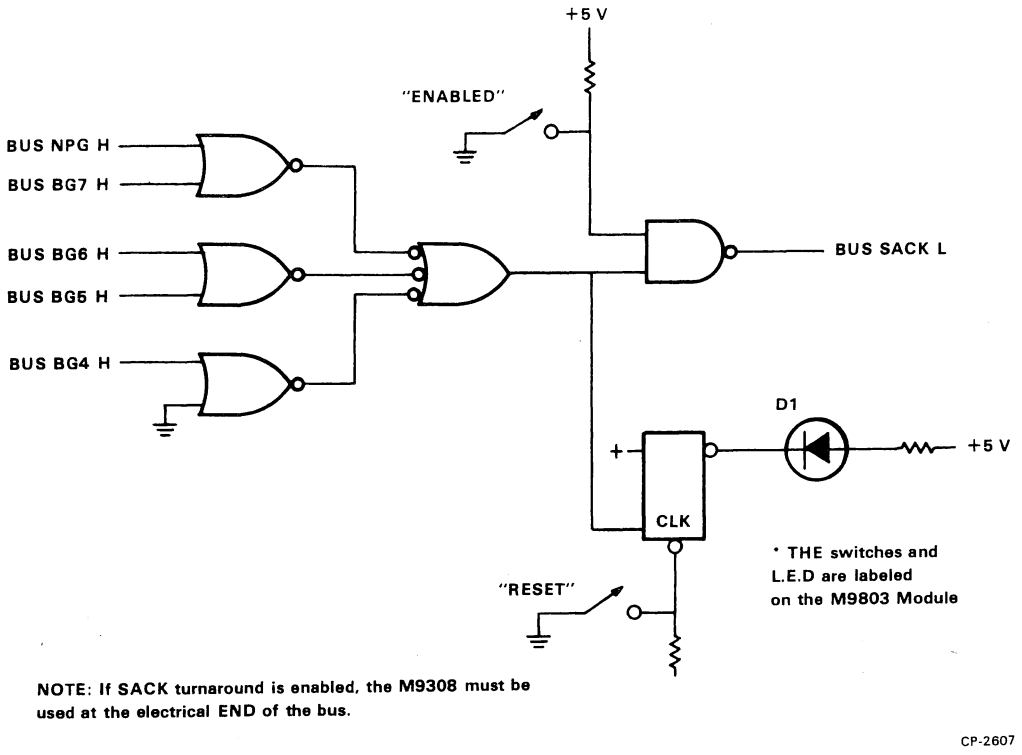


Figure 4-17 M9308 SACK Turnaround Logic

4.6.2 Modifying the M930

1. On side 2 of the M930, cut etch at pin AA2.
2. On side 2 of the M930, cut etch at pin BA2.
3. Attach one end of a 4.57 m (10 ft) piece of No. 16 gauge (or larger) insulated wire to the etch as indicated in Figure 4-18 (step 3). This will be the plus (+) lead to the variable power supply.
4. Attach one end of a 4.57 m (10 ft) piece of No. 16 gauge (or larger) insulated wire to the etch as indicated in Figure 4-18 (step 4). This will be the minus (–) lead to the variable power supply.

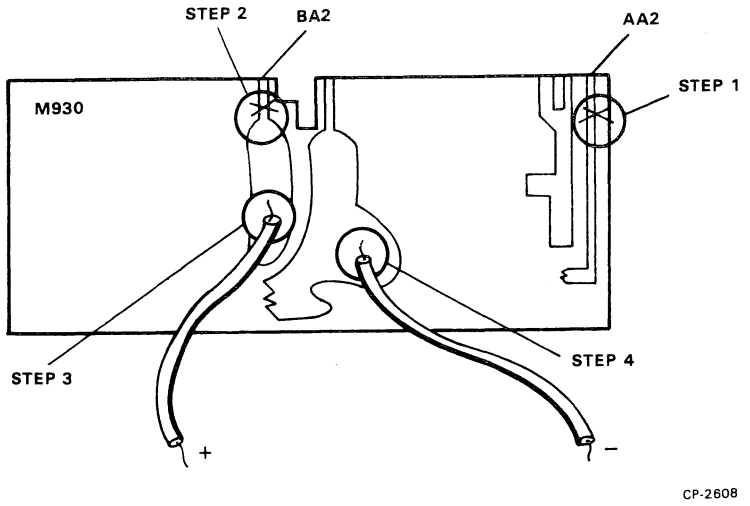


Figure 4-18 M930 Modification Example

4.6.3 Procedure for Use

1. Turn all system power off.
2. Connect modified terminators to the variable power supply (double check polarity).
3. Remove system M930 terminators from Unibus.
4. Install modified terminators in system where standard terminators were.
5. Turn on variable power supply and adjust output to +5 V.
6. Turn on system power.
7. Proceed with bus margining as described in Paragraph 4.3.

CHAPTER 5
UVM-TA TESTER

5.1 UVM-TA OVERVIEW

This chapter provides DIGITAL Field Service personnel with sufficient information to operate and maintain the Unibus Voltage Margin Tester (UVM-TA) and use it to troubleshoot Unibus Problems.

The UVM-TA is a portable device (see Figure 5-1) designed to check all Unibus receivers and drivers in a system by applying a margining voltage to the Unibus lines. The tester provides a dc termination voltage to special terminator boards. These special terminator boards, called margining heads, are used in place of the standard M930 terminator. The margining heads do not change effective Unibus length.

5.2 TESTER KIT COMPONENTS

The complete tester kit consists of the components shown in Table 5-1.

Table 5-1 Tester Kit Components

Number	Description	Part Number
1	UVM-TA Tester	
2	Margining head	M9303
2	Margining head	M9303 YA
TBS	Unibus Cable	BC11-A
1	UVM-TA Troubleshooting Guide	

The UVM-TA is a relatively simple electrical Unibus testing device. It contains two dc power supplies (a fixed supply and a variable supply), a digital voltmeter (DVM) to monitor the power supplier, and 56 SPDT switches.

The fixed 5 Vdc power supply provides the voltage normally used to terminate the Unibus lines. Any of the 56 Unibus line switches placed in the fixed position will connect the terminating network of the selected line to the fixed supply. This allows the operator to keep certain lines at the normal terminating voltage while varying the terminating voltage on other lines. The fixed supply also supplies power to the DVM.

The variable dc power supply provides between 2 and 8 Vdc to margin Unibus lines. The supply is adjustable via a front panel control and is monitored by a DVM also located on the front panel. Any of the Unibus line terminating networks can be connected to this supply by setting the corresponding data switch to VARIABLE.

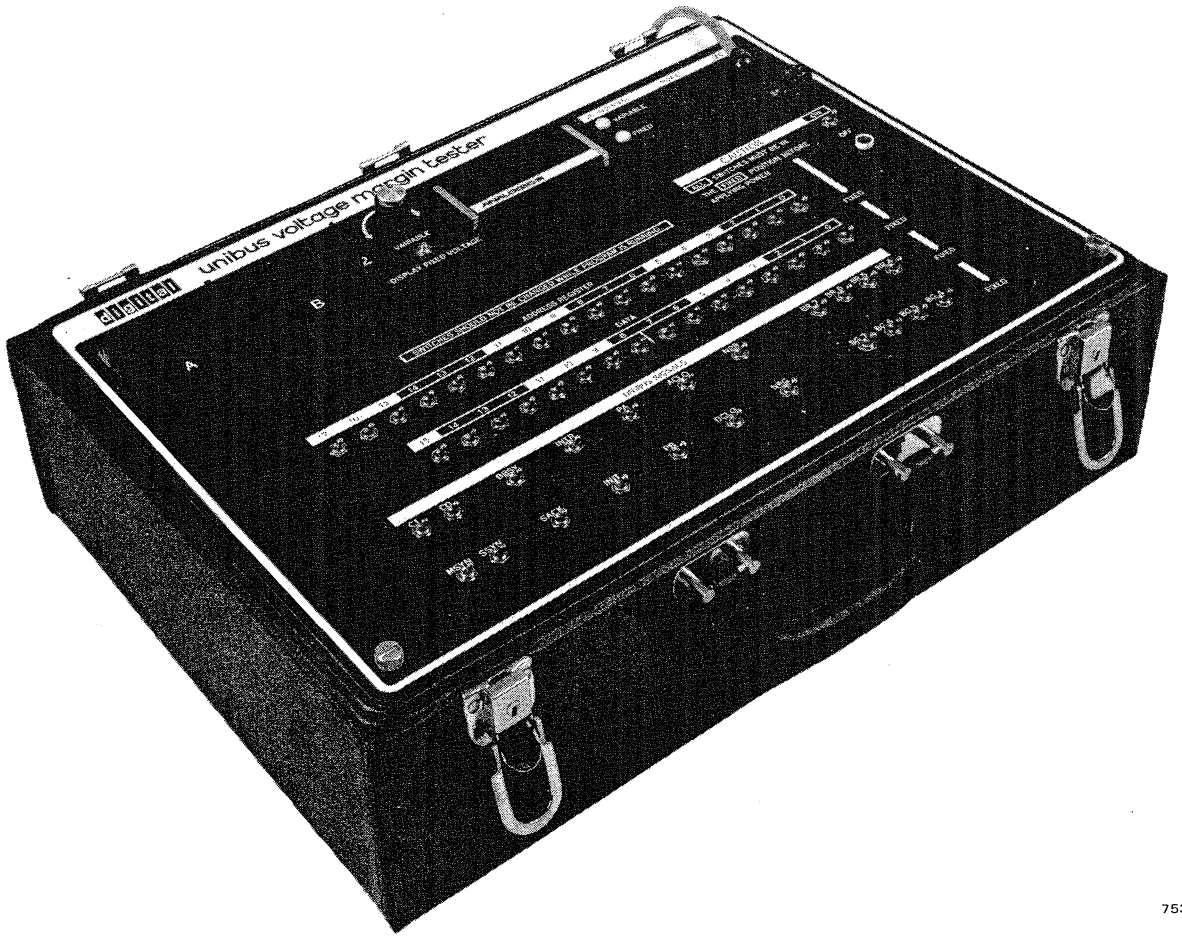


Figure 5-1 Unibus Voltage Margin Tester Box

The front panel DVM normally monitors the variable supply. When the DISPLAY FIXED VOLTAGE button is pressed, the DVM displays the voltage of the fixed supply.

5.3 TESTER SPECIFICATIONS

The tester contains two dc power supplies, a fixed supply and a variable supply.

Fixed supply	5 Vdc at 2 amps
Variable supply	2 V to 3 V at 2 amps

The tester is designed for use in the field. It is packaged in a brief case type carrying case and weighs 35 pounds. The carrying case holds the tester, margining heads, cables and the manual. The tester requires 115 or 230 Vac (10 percent), 50 or 60 Hz single-phase power.

5.4 UNPACKING PROCEDURE.

To unpack the UVM-TA:

1. Remove the carrying case from the shipping carton and inspect for exterior damage. Damage claim should be directed to the responsible shipper.

2. Open the carrying case and inspect the components for damage.

3. Verify that all components are present. (See Paragraph 5.2 for Kit Components).

5.5 ACCEPTANCE TEST

The UVM-TA is shipped ready-to-use. If the unit is not operating properly, refer to Preventive Maintenance (Paragraph 5.9) to diagnose and correct the problem. Service should be performed by qualified personnel only. A Tripplet (model 630-NA) or Simpson (model 260) multimeter is required to perform the acceptance test.

To check out the UVM-TA:

1. Plug tester ac cord into power source.

2. Place 56 signal switches in the down position.

3. Turn tester on. Verify visually that power indicator is on, FIXED DC INTERNAL indicator is on, and DVM is displaying a voltage between 1 and 9 Vdc. An internal fan will come on. This can be verified by listening for the sound of the fan.

4. Using the VARIABLE potentiometer, vary the internal variable dc supply between 2 and 8 volts. This can be verified by observing the DVM. Set the variable dc supply to 6 volts. The VARIABLE DC INTERNAL indicator will be lit. Press DISPLAY FIXED VOLTAGE. DVM will read 5 V.

5. Using the multimeter, probe pin BS1 of the test connector 1. Voltage will read 5 Vdc. Put ADDRESS REGISTER switch in up or VARIABLE position. Voltage will read 6 Vdc. Put switch into FIXED or down position and probe similar pin on test connector 2. Voltage will read 5 Vdc. Switch to up position. Voltage will read 6 Vdc. Leave switch up to indicate it has been tested.

6. Repeat step 5 for remaining 55 Unibus signal switches.

5.6 CONTROLS AND INDICATORS

All controls and indicators for the UVM-TA are located on the front panel of the unit (Figure 5-2). The function of each control and indicator is listed in Table 5-2.

5.7 OPERATING PROCEDURE

Refer to Chapter 4, Paragraph 4.4.2 for operating procedures.

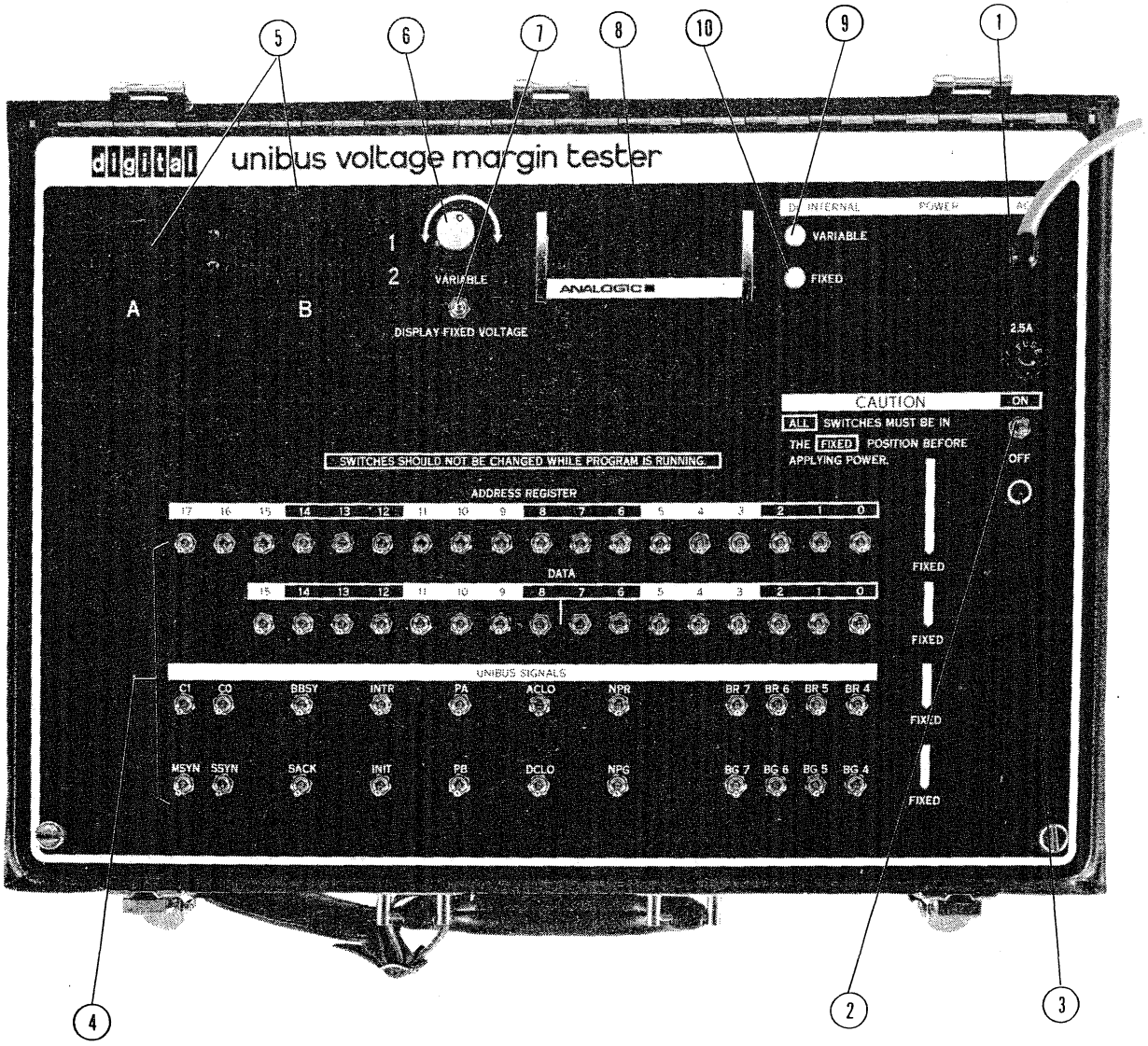


Figure 5-2 Controls and Indicators (Indexed)

Table 5-2 Controls and Indicators (Indexed)

Index No.	Function
1	FUSE 2.5 AMP – Protects tester from current overload.
2	ON/OFF – Switch controls ac power to tester.
3	ON/OFF Indicator – Lights when tester is on.
4	56 single-pole double-throw switches – control margining voltage to each of 56 individual Unibus lines. When in the down position the selected line is connected to a 5 Vdc fixed voltage supply. When in the up position the selected line is connected to variable dc voltage supply.
5	Tester connectors – connects selected voltage levels to margining heads.
6	Controls output voltage of variable voltage.
7	When depressed, digital voltmeter monitors voltage of fixed supply voltage. DVM normally monitors variable supply voltage.
8	Digital voltmeter monitors voltage of selected power supply.
9	VARIABLE lights when variable supply is operating. Brightness is proportional to selected voltage.
10	FIXED lights when fixed supply is operating.

5.8 MAINTENANCE PHILOSOPHY

Tester maintenance consists of preventive and corrective maintenance procedures. The preventive maintenance procedures should be performed regularly in order to detect any damage caused by improper handling of the unit. A troubleshooting flow diagram is provided to aid service personnel in isolating and repairing faults within the tester circuits. The troubleshooting flowchart and corrective maintenance information given in this chapter covers only the tester unit. The flow diagram makes use of the acceptance test procedure outlined in Paragraph 5.5.

To perform disassembly/assembly and preventive and correction maintenance, only a multimeter and standard hand tools are required. Recommended multimeters are: (1) Triplett model 630-NA or (2) Simpson model 260.

5.9 PREVENTIVE MAINTENANCE

As preventive maintenance, the acceptance test procedure should be performed from time to time to ensure complete operational readiness and to check the unit adjustments. The frequency of the checkouts depend on hours of handling, and environmental conditions. The schedule given in Table 5-3 is suggested as a minimum time table.

Table 5-3 Preventive Maintenance Schedule

Performance Interval	Test or Procedure
Monthly	Visually inspect for physical damage; correct if required. Clean externally.
Quarterly	Clean internally with vacuum cleaner or a soft brush Check for looseness of the knobs, switches, and indicators. Perform acceptance test procedure (Paragraph 5.5)

5.10 CORRECTIVE MAINTENANCE

If the tester fails the acceptance test or fails while testing a Unibus system, corrective maintenance must be performed. The flowchart (Figure 5-3) will pinpoint the faulty tester component. However, before using the flowchart, unscrew and lift up the control panel and perform a visual inspection. Look for burnt or damaged wires or components. Replace any faulty wires and component(s), if found, and perform the acceptance test procedure to determine if the tester has been repaired. If not, begin using the flowchart.

CAUTION

Certain circuits in the tester operate at 110 Vac. Special care must be taken when probing near these circuits. Before disconnecting, replacing and/or reconnecting any part other than a fuse, turn tester off and unplug it.

NOTE

Turn tester off when replacing front panel fuse.

5.11 DISASSEMBLY/ASSEMBLY

Many of the components within the tester are also accessible and can be replaced without performing any disassembly. The switches, indicators, and plugs on the tester control panel are easily accessible for repair or replacement. However, to remove either power supply, the transformer, or the fan, the tester must be disassembled. To disassemble the tester, perform the following procedure:

1. Unplug line cord.
2. Remove the tester from its carrying case by slipping it out of the case.
3. Unscrew and lift up the control panel.
4. To remove the power supplies, remove the power supply bracket using a socket screwdriver.
4. Remove the transformer, unscrew the four mounting bolts at the base of the transformer using a screwdriver. Unsolder the transformer connecting leads.
5. To remove the fan, first remove the fan mounting bracket assembly from the tester using a Phillips head screwdriver. Unsolder the fan connecting leads. Then remove the fan from the mounting bracket using a socket head screwdriver and a Phillips head screwdriver.

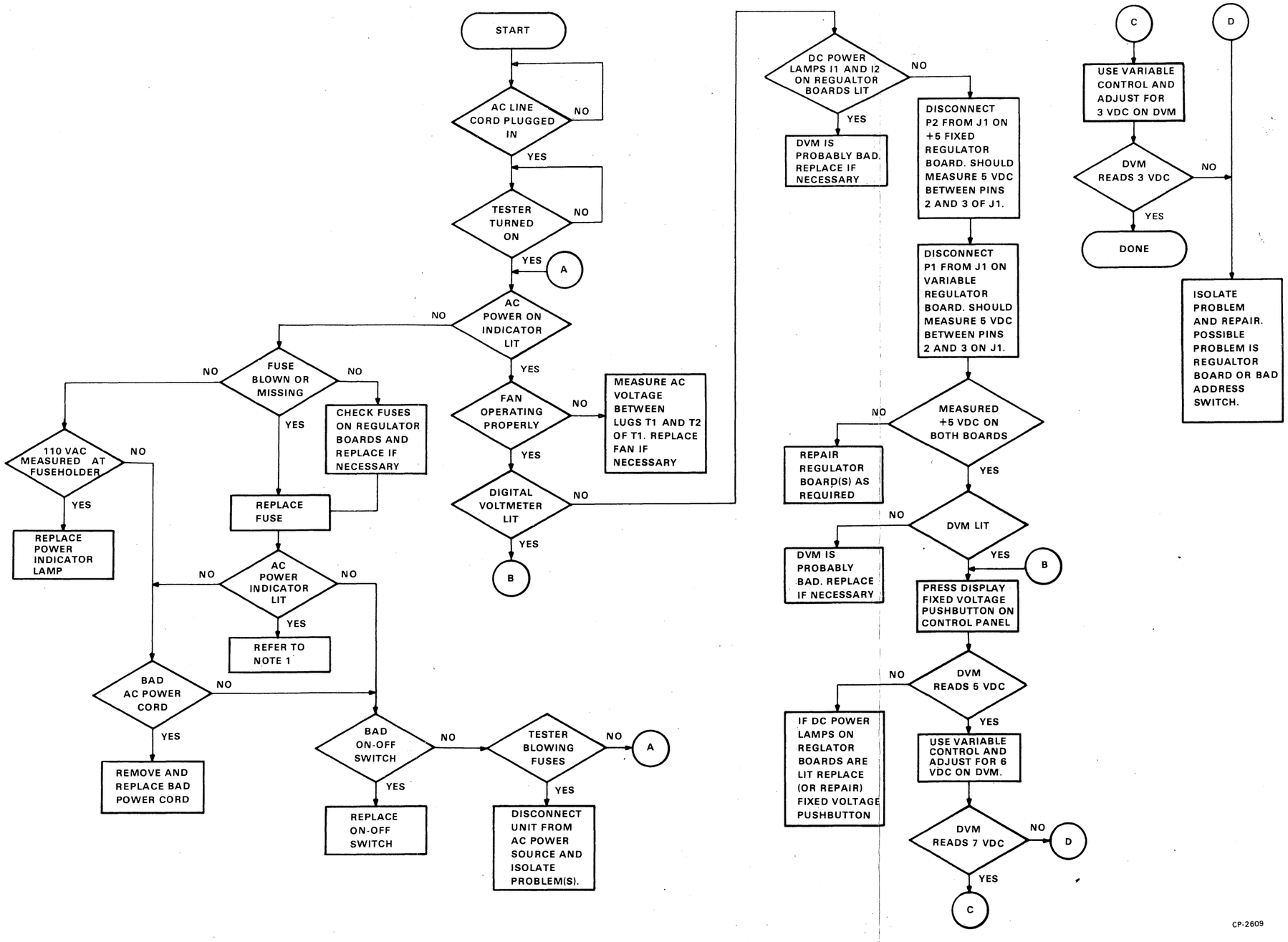


Figure 5-3 UVM-TA Troubleshooting Flowchart

APPENDIX A
ECO HISTORY AND REWORK

A.1 UNIBUS TERMINATORS (M930)

The initial ECOs to the M930 (dated 1970) changed the termination of bus AC and DC LO, which brought the M930 to etch revision B. This etch revision is now obsolete. If system bus problems are suspected for failure, later etch terminators than the B etch should be tried.

A.1.1 Revision C Etch

ECO No.3 to the M930 Unibus Terminators changed the termination resistors tolerance from 5 percent to 1 percent. This change improves the worst case noise tolerance and with suspected bus problems. 1 percent terminators should be used.

CAUTION

Some "C" etch terminators were manufactured with missing etch runs. Pins AN1, AP1, AR1 and AS1 should be connected to pin BE1. These runs were omitted. The missing etch runs are grounds and if not present may contribute to system noise.

A.1.2 Revision D Etch

ECO No.4 to the M930 Unibus Terminators adds four decoupling capacitors and improved grounding. This change significantly decreases noise on the bus. Rev D is the optimum etch revision currently used (Sept. 1976) and should be used if bus problems are suspected because of old type etch boards.

There are other terminators which will be available for new processors and systems in the near future.

A.2 BUS RECEIVERS

A number of integrated circuit types (i.e., chips) have been or will be used as Unibus receivers (Table A-1). Of these, the DEC 380 was most common. It has been phased out and is no longer available. A recent series of ECOs to most options which used the DEC 380 now uses DEC 8640 Bus receivers. The DEC 8640 is a pin-compatible replacement for the DEC 380 and is used in Unibus applications because it has more closely defined specifications and higher noise immunity (see Figure A-1). Substituting one DEC 8640 on a module does not necessitate changing all DEC 380s, these chips may reside in any combination. (This is a phase-in and field rework is not intended except for repair purposes.)

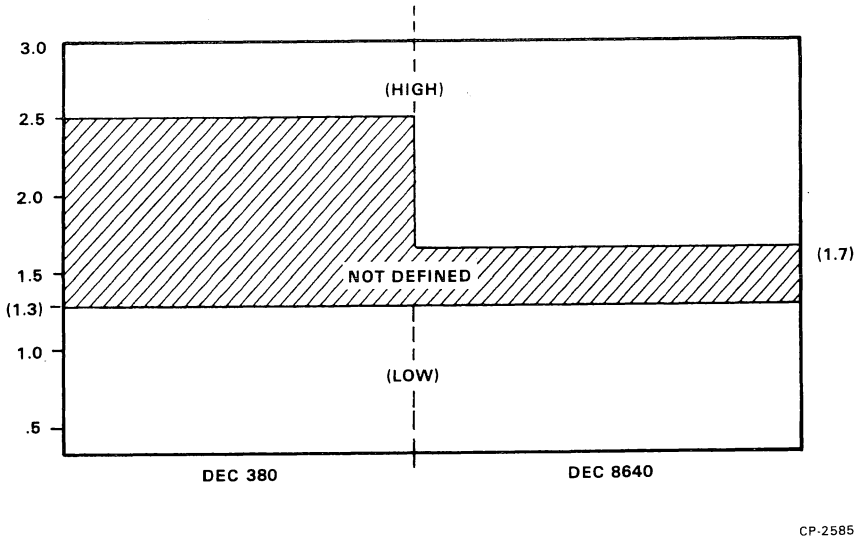


Figure A-1 Comparison of 8640 vs. 380 Threshold (Worst Case)

Table A-1 Unibus I.C. Types

Type	DEC P/N	Function	Note	Input Voltage Low	High	Leakage
Receivers						
380	19-09485	Quad nor	1	1.3	2.5	160
8640	19-11469	Quad nor	2	1.3	1.7	80
11380	19-11113	Quad nor	1	Hysteresis		
8644	Not assigned	Hex inverter	3	1.3	1.7	80
8645	19-12128	7 input nor	3	1.3	1.7	80
314	19-09704	7 input nor	4	1.3	2.5	160
384	19-09486	Quad or	1	1.3	2.5	160
8837	19-11116	Hex inverter	4	1.3	2.5	160
Drivers						
8881	19-09705	Quad nand				25
74H01	19-09849	Quad nand	1			250
Transceivers						
8641	19-11579	Quad transceiver	3			100
8838	19-11117	Quad transceiver	1			100

Notes

1. Not allowed in new designs.
2. Replaces the DEC 380 in Unibus applications.
3. Available in July '75.
4. To be used in new designs only until pin compatible replacements are available.

I.C.	Replacement
314	8645
8837	8644

A.2 BUS DRIVERS

The DEC 8881 is the standard Unibus driver. Others which have been used are listed in Table A-1. Unibus pin assignments are illustrated in Figure A-2.

A.3 GRANT LINE TERMINATION

The terminators on each of the Unibus do *not* terminate grant lines which are received and repropagated. Grant lines are terminated as shown in Figure A-3 (between devices receiving a grant line). A recent series of ECOs that includes all devices using grant lines has changed the previous termination techniques as discussed previously. (A 180Ω pull up resistor has been added to the grant receivers of each device). This significantly reduces reflections and false grants on the bus, i.e., traps to 0, traps to 4 and undefined interrupts.

A.3.1 Rework Procedure

1. Obtain a supply of 180Ω resistors. (These may be ordered under DEC P/N 13-01322).

2. Using the proper print set for each option, locate the grant receiver input.

3. If no 180Ω pull up resistor is installed from the input of the grant receiver to +5 V, install one (refer to the applicable ECOs).

NOTE

Bus switches and repeaters already have these resistors installed.

CAUTION

Some devices receive more than one grant line and many devices receive both NPG and BGxx signals. All grant receivers should be terminated in this manner.

NOTE

To maintain termination consistancy, a 180Ω pull up could be added at the receiver *and* a 390Ω pull down could be added at the driver. If a device with the driver pull down were used with a device which did *not* have the receiver pull up, the assertion level would not be high enough to ensure reliable operation.

A.4 BC11 CABLE FOAM

The BC11A cable (see Figure A-4) consists of two (60 conductor) mylar Flex-print cables used to connect system units in different mounting cabinets or to connect peripheral devices not located within the cabinets. The two Flex-print cables are taped together to form a single flat 120 conductor cable. In system applications, there is little control over how this cable is routed. Impedance of the BC11 cable can vary widely due to physical routing and has been found to be in the range of 60-80Ω in typical systems. (Design specification is 120Ω).

ECO No. BC11A-004 corrects this low-impedance problem with the addition of foam between the two mylar cables. The impedance of the cable is stabilized at 120Ω and is not too sensitive to physical configuration when this foam is installed.

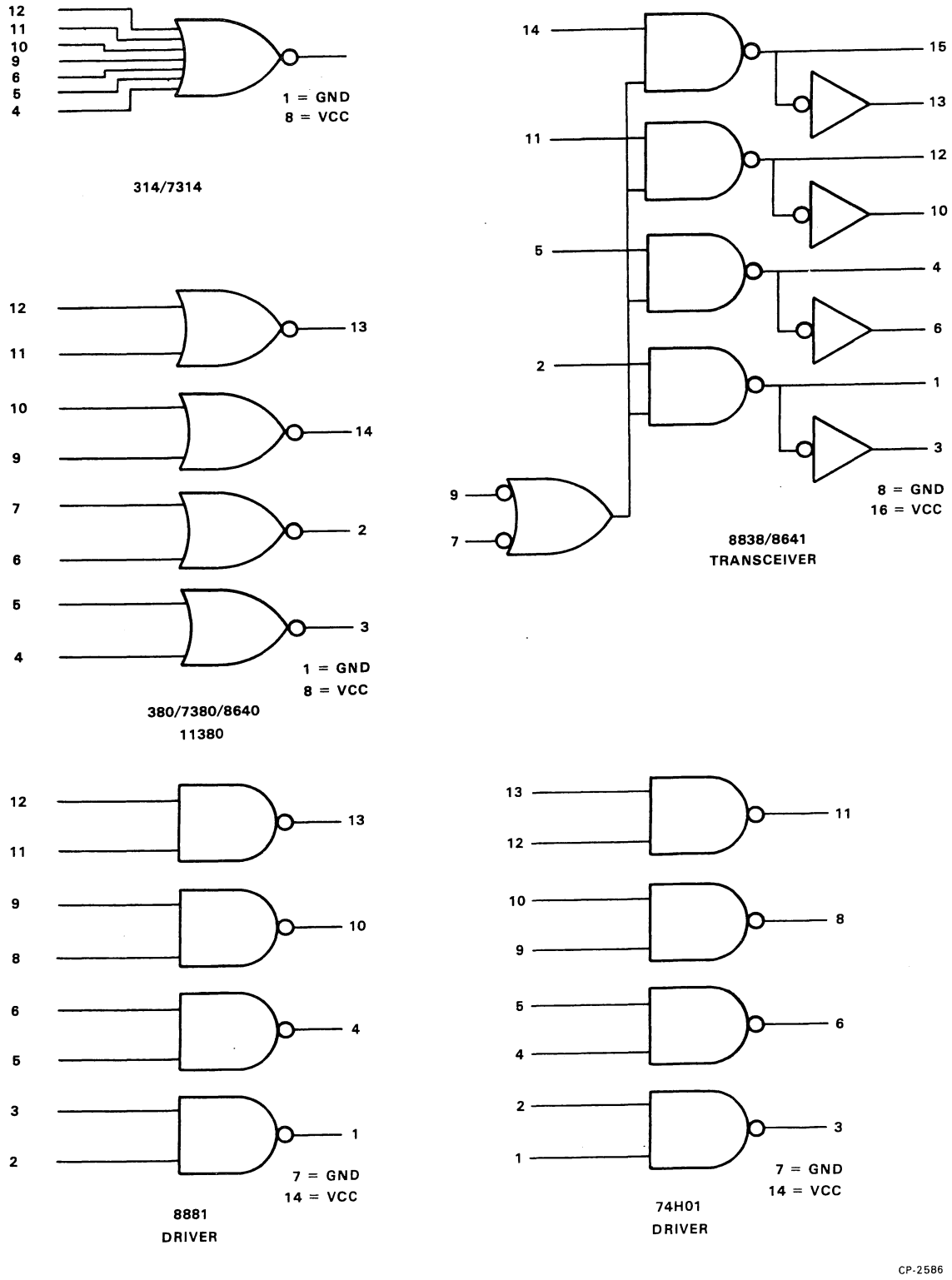


Figure A-2 Pin Assignments of Unibus I.C.s

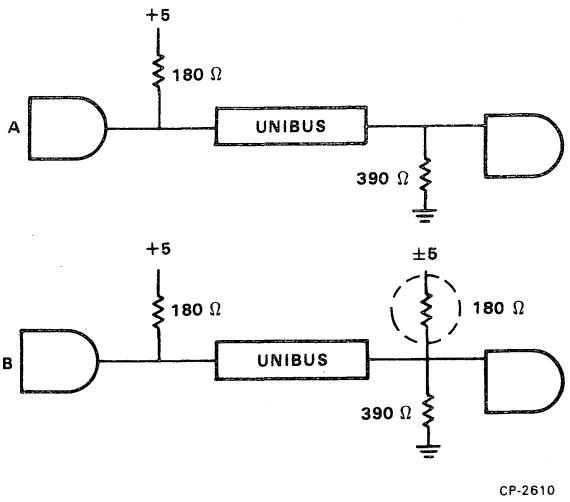


Figure A-3 Grant Line Termination

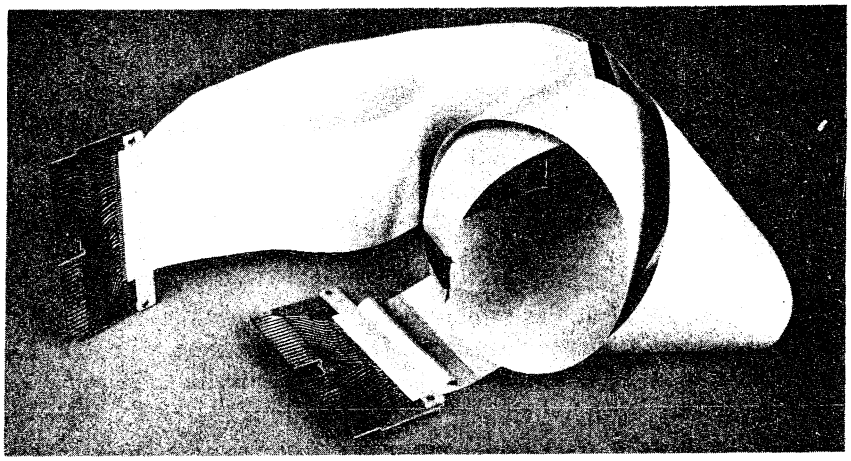


Figure A-4 BC11 Cable

A.4.1 Foam Installation Procedure

Obtain sufficient foam to do the job. This may be ordered under DEC part number 90-08881 (see Figure A-5). The length required will be twice the sum of all BC11 cable lengths in the system, plus twice the length of all *parallel* cable runs.

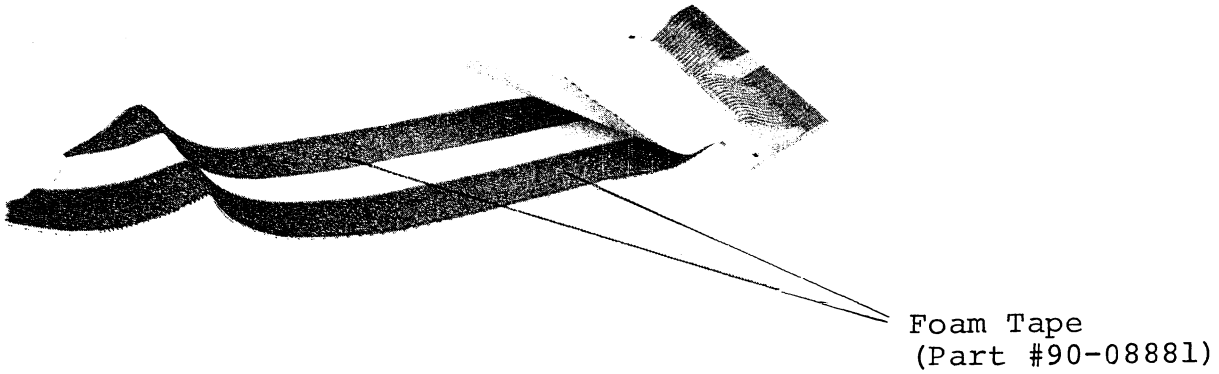


Figure A-5 Foam Tape Installation

Perform the following steps for all BC11 cables in the system:

1. Remove the tape holding the two mylar Flex-print cables together.
2. Examine the cables for any nicks, cuts or sharp creases, discard the cable if unserviceable.
3. Separate the cables and apply the foam tape to both edges for the entire length of the cable.
4. Retape the two mylar cables together with electrical tape. (Foam is sandwiched between cables and a single flat cable results. Do not squeeze the cables together at the taped points.)

NOTE

If two BC11 cables run parallel to each other for any distance, foam should be placed between them. See Figure A-6 for multiple cable foam installation.

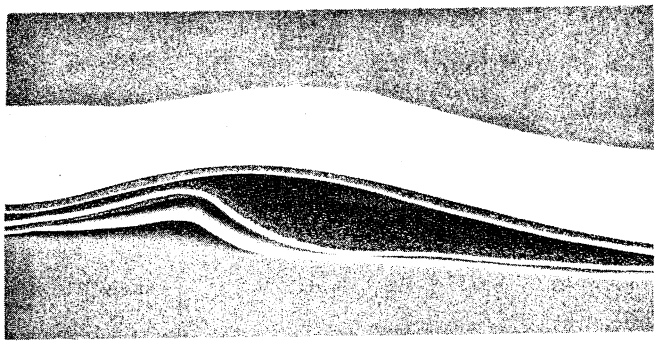


Figure A-6 Multiple Cable Foam Installation

APPENDIX B
M9202-2 UNIBUS JUMPER INSTALLATION

B.1 GENERAL

Reflections on the Unibus can be caused by termination mismatch, stubs, or loads. (Stubs cannot be matched, any stub will cause a reflection.) Backplanes have wires attached to the Unibus which act as stubs. In addition to this, individual modules may have bus lines carried on etch which adds length to the backplane stub. Individual device options cause reflections on the Unibus which are called signatures. These signatures combine to form the composite waveform seen on the bus. (See Figure B-1.)

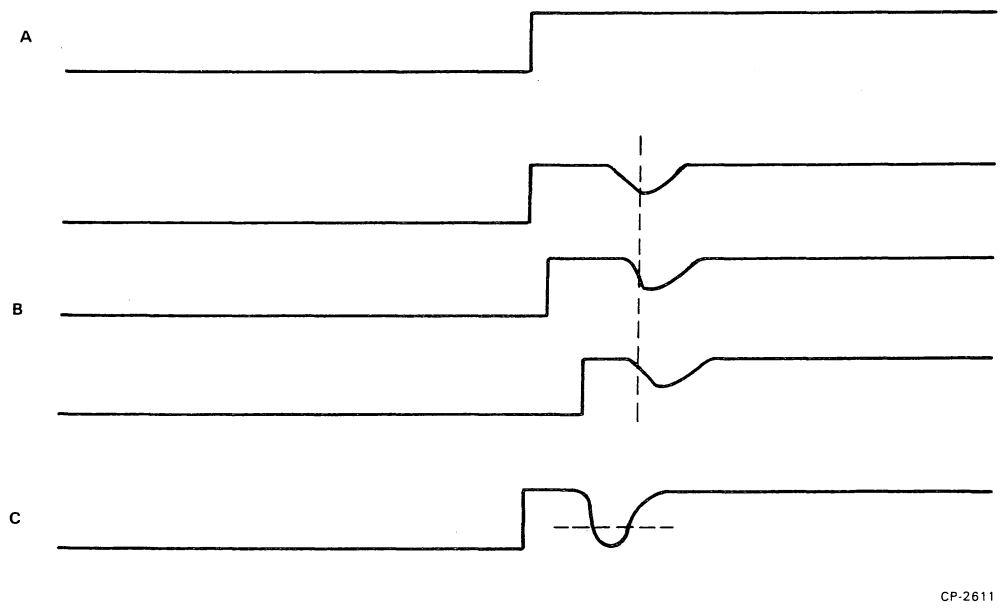


Figure B-1 Composite and Signature Waveforms

A level change, in theory, should be a clean transition.

Devices placed on the bus may contribute signature reflections.

Many devices in close proximity may contribute to composite reflections great enough to cross over the threshold level of bus receiver.

The M920 Unibus jumper module (double module) connects the Unibus from one system unit device to the next. Its length is very short electrically. If device options are installed in close proximity to each other (lumped loads), their signatures may combine to place a large reflection and false information on the bus.

If these signatures could be separated, they would not present such a problem. The M9202-2 Unibus Jumper Module is physically compatible with the M920; however, it induces some delay and lessens the effect of lumped loads. The same signatures shown in Figure B-2 can be separated to reduce the composite signal. This will prevent composite signal from crossing the bus receiver threshold and thus from presenting false information due to large reflections.

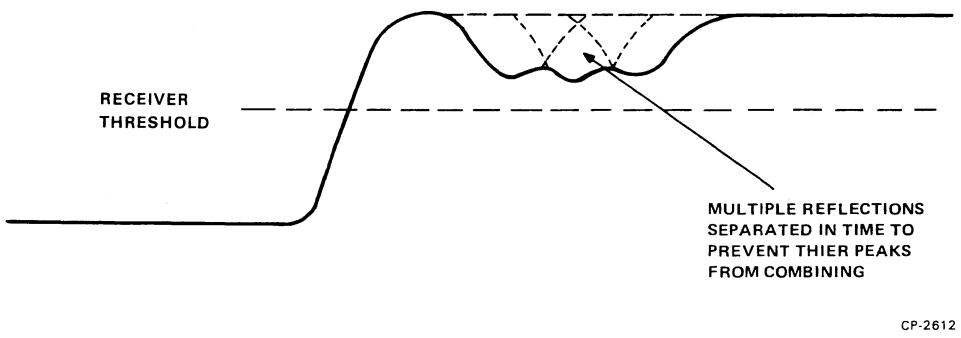


Figure B-2 Separation of Multiple Reflections

This does not altogether eliminate the source of the problem, however, it does offer a reasonable alternative for reducing the effect of reflections.

B.1.2 Jumper Installation

A first pass approximation is to install one M9292-2 bus jumper between each 4 to 8 unit loads (replace the existing M920 with a M9202). (Refer to Chapter 2 for detailed configuration rules.)

NOTE

The M9202 is a useful troubleshooting aid and should be left in the system on a permanent basis if required. The M9202 will not fit in BA11-Cs or BA11-Es mounting boxes. In these systems, use BC11A-2 cables.

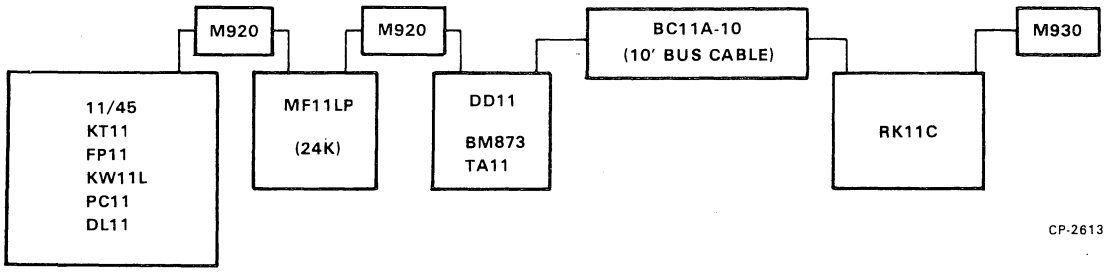


Figure B-3 Configuration Using M920

Using the configuration shown in Figure B-3, the following waveforms (see Figure B-4) were obtained at SSYN on the RK11C backplane.

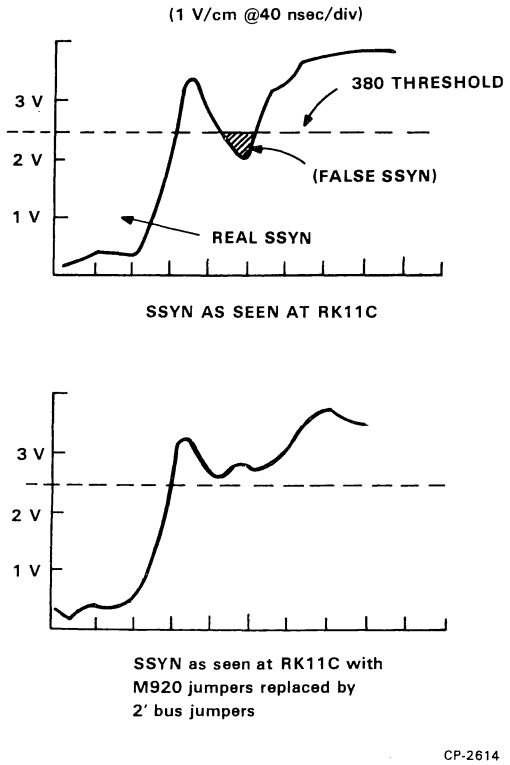


Figure B-4 Jumper Threshold Levels

APPENDIX C
AC AND DC LOAD TABLE

AC & DC LOAD TABLE

DEVICE OPTIONS	LOAD AC	LOAD DC	TDR RESULTS BBSY	TDR RESULTS MSYN	TDR RESULTS SSYN	NOTE;MEASURE DATE (OR OTHER INFOR.)
AA11-K	4	1	2.47	1.80	3.22	121576
AD11-K	4	1	4.00	1.39	2.26	051076
AR11(M7309)	6	1	5.89	3.42	5.16	092375
BM792	2	1				
BM873	4	1	0.75	1.91	3.84	101575
CR11	3	1	1.91	1.00	2.75	092375
CD11	?					
DA11-B	9	1				
DB11-A(LEFT)	6	1	5.75	4.24	4.33	092275
DB11-A(RIGHT)	6	1	5.49	3.30	3.19	092275
DC11	12	1?	12.04	6.89	10.79	081274
DD11-A(OBSOLETE)	3	0	1.94	1.70	2.51	081976
DD11-B	6	0	4.18	3.48	5.38	120174(NEW REV. 3 AC LOAD IS IN PROCESS)
DD11-C	4	0	3.04	2.48	3.89	121576
DD11-D(SLOT1-4)	4	0				121576(SLOT4-2FT-SLOT5)
DD11-P(SLOT1-4)	4	0	2.63		3.68	121576(SLOT4-2FT-SLOT5)
(SLOT5-9)	4	0	?			
DH11-DM11-BB	14	2?	13.30	6.22	11.12	082175
DJ11	5	1	5.09	2.96	5.08	121874
DL11-A(M7800)	3	1	1.64	0.79	2.49	030375
DL11-C	4	1				
DL11-E	3	1	1.76	0.98	2.72	030375
DL11-W(M7856)	3	1	2.45	0.80	2.30	030375
DMC11	3	1	3.13	1.48	0.47	121576
DP11	5	1	4.56	4.75	4.16	030375
DQ11	8	1?	7.27	6.46	7.80	101775
DR11-B	9	1	9.10	8.45	7.88	101775
DR11-C(M7860)	5	1	4.35	4.93	4.11	101675
DR11-K	5	1	4.83	2.16	3.48	101775
DR11-L	3	1	2.90	0.82	2.50	030775
DR11-M	3	1	2.90	0.82	2.50	030775
DT03(CPU)	7	1	4.67	2.96	6.52	
DT03(SHARED)	3	1	3.15	3.07	2.73	
DT06(UNIBUS A)	2	0	1.78	1.75	1.23	081776
(UNIBUS B)	2	0	1.82	1.59	1.74	081776
(A IN & SS)	3	0	2.09	1.47	1.34	081776
(B IN & SS)	2	0	2.78	2.25	2.90	081776
(SR & A OUT)	2	0	1.69	1.46	1.45	081776
(SR & B OUT)	3	0	3.15	1.76	2.07	081776
DU11	4	1	3.69	1.61	1.71	101575
DUP11	3	1?	3.03	1.79	0.50	121576
DV11	12	1	11.63	5.24	10.45	101575
DX11	6	1	3.82	5.26	3.56	101575
KE11-B	4	1				

KG11	4	1	0.19	1.12	3.89	101575
KW11-L(M787)	3	1	3.04	1.17	2.14	011477
KW11-K	4	1	3.83	1.85	1.85	051075
KW11-P(OLD M7228)	5	1				
KW11-P(NEW M7228 REV.F CS J)	4	1	2.02	2.28	3.50	102275
KY11-LA	0					
KY11-LB(M7859)	5	1	4.70	3.18	1.13	122975
LK11	4	1	3.65	1.15	3.87	121576
LP11	5	1	2.95	1.91	4.57	101675
LP20	3	1	3.07	2.80	3.00	052776
LS11	3	1	1.56	7.68?	2.81	050275
LV11	3	1				
M9301	2	1	0.22	1.11	2.05	121576
M7858(PARITY MODULE)	0					
M7859(PROGRAM CONSOLE)	5					
MA11	5	1	0.51?	4.99	5.50	121576
*MOORE SYSTEM DEVICES:						
1)DCC+DD11-A	8	1.57	4.72	4.03	7.47	081976
2)DCC(99550,99551)	5	1.57	2.78	2.33	4.96	081976(EST.)
3)PDI(99556)	3	1.71	3.12	1.18	1.10	081976
4)CALCULATOR(99319)	3	1	0.74	2.30	0.67	081976
MM11-DP	1	1	1.16	1.09	1.12	010576
MS11-JP	1	1	0.56	0.33	0.58	010576
MF11-L(BACKPLANE)	2	0	0.46	1.12	0.30	121975
MF11-L(1X8K)	5	1	2.10	4.90	4.40	
MF11-L(2X8K)	7	1	3.00	7.00	6.00	091975
MF11-L(3X8K)	9	1	5.50	8.70	7.40	091976
MF11-U(2X16K)	8	2	3.76	8.00	6.00	030975
MK11-UP(1X16K)	6	2	2.11	5.59	4.40	091975
MF11-UP(2X16K)	8	3	3.76	8.00	6.00	091975
MF11-W	6	1	1.46	5.46	4.49	
MM11-WP	6	2				
PC11(OLD)	4?	1				
PC11(NEW)	4?	1				
PDP 11/04(M7263,M9301)	8	1	6.13	4.79	7.89	060176
PDP 11/05	10	1	8.45	8.50	9.93	120874
PDP 11/34(WITH M9301)	6	1	4.31	5.38	3.58	121576
PDP 11/35	12	1	10.63	6.03	12.14	121674
PDP 11/45(BUS A,KW11-L)	11	2	10.49	4.07	11.08	101075(DC LOADS:KW11L, CPU)
(BUS B)	2	0				
(BUS B 1 MOS)	5	1	2.07	4.61	5.09	
(BUS B 2 MOS)	9	2	2.56	7.25	8.43	070775
*(MINNTRONICS CACHE)	6	1	2.57	5.24	1.80	
PDP 11/60	7	1?	3.49	7.19	3.26	011877
PDP 11/60(BACKPLANE)	4	0	4.21	3.22	2.98	011477
PDP 11/70(SLOT1-39)	20	6?				(DC LOADS:KW11L,CPU,
(SLOT1-39 BACKPLANE)	5	0	2.51	5.15	2.33	4RH70:SLOT39-2FT-KW11L-
(SLOT40-44 BACKPLANE)	5	0	2.79	5.15	3.32	2FT-SLOT40;REV. J;
RH70	3.45	1	2.36	3.45	1.01	011477)
RC11	5	1	4.16	5.20	4.10	092375
RF11	8	1	5.12	7.33	6.80	101375
RH11	7	1	6.80	5.32	6.51	090575
RK11-D(OLD)	11	1	9.10	10.7	8.20	090575
RK11-D(NEW)	5	1	3.90	4.97	2.78	090575
RK611	6	1	5.56	4.97	4.92	121576
RL11	7	1	6.79	4.70	0.62?	121576
RP11-C(OR E)	8	1				
RX11	6	1	3.49	4.97	2.78	121874
TA11	3	1	2.15	2.43	2.94	

TC11	7	1	6.92	7.00	4.79	091975
TERMINATOR(M930)	0	0				
(M981)	0	0				
TM11	8	1	5.67	7.22	6.44	102974
TMA11	8	1	5.32	6.69	7.50	102974
TMB11	6	2	4.11	4.62	6.05	121576
TR79-F	5	1	4.68	3.22	3.50	092275
VS60	5	1	2.19	5.11	2.63	121576

DATE:01-19-77

NOTE:
1, OPTIMIZE NPR DEVICES SEQUENCE : RK11-D,TM11,TC11,
RJS04,RJP04,RK611,RJS03,RP11C,DMC11(1MB),TJU16,
RF11,DMC11(56KB),DH11.
2, ? MEANS DATA IS SUSPICIOUS.
3, * FOREIGN DEVICES.
4, IF YOU DOUBT SOME OF THE VALUES IN THE TABLE, PLEASE
CONTACT CHIH LI (PK3-2/S17, OR X5229).

APPENDIX D
BUS LOADS

Model Number	Description	MECHANICAL				ENVIRONMENTAL		POWER			PROGRAMMING			UNIBUS				
		Mounting Code	Size (H x W x D)	Cab Incl	Weight	Oper Temp	Rel Humid	Cur needed/(supplied) +5V	115 VAC/Other	Power Dis	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	Page No.	Model Number
			(inches)		(lbs)	(C)	(%)	(amps)		(W)							
AA11-D	D/A Subsystem	SU				10-40	10-90	3	0.5	60	776 756	140,144	4, 5		1	4-5	AA11-D
AD01-D	A/D Subsystem	PAN	5¼					—	0.5	60	776 770	130	4 - 7		1	4-9	AD01-D
AFC11	A/D Subsystem	CAB				10-40	10-90	—	15	1700	772 570	134	4		1	4-13	AFC11
AR11	Analog Subsystem	MOD	hex ht					4	—							4-19	AR11
BA11-ES	Mounting Box	PAN	10½		100			—	—						—	4-22	BA11-ES
BA408	Amplifier	(LPS11)							—						—	4-279	BA408
BA614	D/A Converter	(AA11-D)							—							4-5	BA614
BB11	Blank Mntg Panel	SU						—	—						—	4-24	BB11
BC11A	UNIBUS Cable							—	—						—	6-8	BC11A
BM792	Bootstrap Loader	SPC						0.3	—						1	4-25	BM792
BM873	Restart/Loader	SPC						1.0	— .002A @ −15V						1	4-27	BM873
CD11-A	Card Reader	SU + TT	14 x 24 x 18		85	15-32	20-80	2.5	6	600	772 460	230	4	X	1	4-30	CD11-A
CD11-E	Card Reader	SU + TT	38 x 24 x 38		200	15-32	20-80	2.5	10	1150	772 460	230	4	X	1	4-30	CD11-E
CM11-F	Card Reader	SPC + TT	11 x 19 x 14		60	15-32	20-80	1.5	6	600	777 160	230	6		1	4-43	CM11-F
CR11	Card Reader	SPC + TT	11 x 19 x 14		60	15-32	20-80	1.5	6	600	777 160	230	6		1	4-43	CR11
DA11-B	UNIBUS Link	SU						4	—			124	5	X	1	4-53	DA11-B
DA11-F	UNIBUS Window	SU						5	—			float	7	X	1	4-58	DA11-F
DB11-A	Bus Repeater	SU						3.2	—						1 + 1	4-66	DB11-A
DC11-A	Asynch Line Inter	SU						2.2	—		774 000	float	5		1	4-67	DC11-A
DD11	Periph Mntg Panel	SU						—	—						—	4-75	DD11-A
DF01-A	Acoustic Coupler	TT	6 x 7 x 12		6			—	0.3						—	4-79	DF01-A
DF11	Line Sig Cond	DF slot						—							—	4-81	DF11
DH11	Asynch Line MX	2 SU + PAN	5¼					8.4	— 0.24A @ −15V		float	float		X	2	4-89	DH11
DJ11	Asynch Line MX	SU + PAN	5¼					5	— +15V req'd		float	float			1	4-118	DJ11
DL11-A	Terminal Control	SPC						1.8	— 0.15A @ −15V		777 560	060,064	4		1	4-258	DL11-A
DL11	Asynch Line Inter	SPC						1.8	— 0.15A @ −15V		776 500	float	4		1	4-135	DL11
DM11-BB	Line Multiplexer	(DH11)						2.8			775 000	float			1	4-89	DM11-BB
DN11	Auto Calling Unit	SU						1.4	—		775 200	float	4		1	4-152	DN11
DQ11	NPR Synch Line	SU						6.0	— ±15V req'd		float	float		X	1	4-160	DQ11
DR11-B	DMA Interface	SU						3.3	—		772 410	124	5	X	1	4-195	DR11-B
DR11-C	General Interface	SPC						1.5	—		767 770	float	5		1	4-200	DR11-C
DT03-F	UNIBUS Switch	PAN	5¼						2			user	7		1 + 1	4-210	DT03-F
DU11	Synch Line Inter	SPC						2.0	±15V req'd		float				1	4-214	DU11
GT40	Graphics Terminal	TT	18 x 20 x 24		150	15-32	20-80	—	15	1500	float	float		X	1	4-233	GT40
H312-A	Full Modem							—	—						—	4-239	H312-A
H324	Pushbutton Panel	PAN	5¼					—	—						—	4-26	H324
H720-E	Power Supply	(BA11)			30			(22)	6 (10A) @ −15V	700					—	4-22	H720-E
H722	Transformer	(PC11-A)						—	— 1.5A @ 230 VAC						—	4-313	H722
H742	Power Supply	(H960-D)						—	8 (1A) @ +15V						—	4-240	H742
H744	+5V Regulator	(H742)						(25)	—						—	4-240	H744
H745	−15V Regulator	(H742)						—	— (10A) @ −15V						—	4-240	H745
H960-C	Cabinet	FS	72 x 21 x 30	X	120			—							—	4-240	H960-C
H960-D	Cab (1 drawer)	FS	72 x 21 x 30	X	300			(75)	8						—	4-240	H960-D
KG11-A	Comm Arith Unit	SPC						1.5	—		770 700				1	4-245	KG11-A
KW11-L	Line Clock	MOD	single ht					0.8	—		777 546	100	6		1	4-254	KW11-L
KW11-P	Programmable Clock	SPC						1	—		772 540	104	6		1	4-255	KW11-P
LA36	DECwriter II	FS	33 x 28 x 24		100	10-40	10-90	—	2	300					—	4-258	LA36
LP11-R	Ptr (heavy duty)	SPC + FS	48 x 49 x 36		800	10-40	10-90	1.5	17	2000	777 514	200	4		1	4-261	LP11-R
LP11-V	Line Printer	SPC + FS	45 x 33 x 22		340	10-40	10-90	1.5	4.5	500	777 514	200	4		1	4-261	LP11-V

		MECHANICAL				ENVIRONMENTAL		POWER			PROGRAMMING			UNIBUS				
Model Number	Description	Mounting Code	Size (H x W x D)	Cab Incl	Weight	Oper Temp	Rel Humid	Cur needed/(supplied) +5V	±15 VAC/Other		Power Dis	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	Page No.	Model Number
			(inches)		(lbs)	(°C)	(%)	(amps)			(W)							
LPS11	Lab Periph System	PAN	5¼		80			—	3		300	float	float	4 – 6	opt	2	4-268	LPS11-S
LS11	Line Printer	SPC + TT	12 x 28 x 20		155	10-40	10-90	1.5	3		300	777 514	200	4		1	4-280	LS11
LT33	Teletype	FS	34 x 22 x 19		60	15-32	20-80	—	2		200					—	4-286	LT33
LV11	Electrostatic Ptr	SPC + FS	38 x 19 x 18		160	10-40	10-90	1.5	5		600	777 514		4		1	4-294	LV11
M105	Adrs Select Module	MOD	single ht					0.34	—								6-9	M105
M783	Bus Transmitter	MOD	single ht					0.2	—								6-11	M783
M784	Bus Receiver	MOD	single ht					0.2	—								6-11	M784
M785	Bus Transceiver	MOD	single ht					0.3	—								6-13	M785
M792	Diode ROM	SPC						0.23	—			773 000				1	4-25	M792
M795	Word Count	MOD							—								6-14	M795
M796	Bus Control	MOD							—								6-17	M796
M920	Bus Jumper	MOD							—								6-24	M920
M930	Bus Terminator	MOD	double ht					1.25	—								6-24	M930
M7820	Interrupt Control	MOD	single ht						—								6-25	M7820
M7821	Interrupt Control	MOD	single ht						—								6-29	M7821
ME11-L	Core Memory (8K)	PAN	5¼					—	5		125					1	4-298	ME11-L
MF11-L	Core Memory (8K)	2 SU						3.4	—	6A @ −15V	125					1	4-298	MF11-L
MF11-U	Core Memory (16K)	2 SU						6.1	—	3.4A @ +20V	125					1	4-298	MF11-U
MM11-L	Core Memory (8K)	(MF11-L)						1.7	—	0.5A @ −15V	125					1	4-298	MM11-L
MM11-U	Core Memory (16K)	(MF11-U)						5.4	—	0.5A @ +20V	125					1	4-298	MM11-U
MR11-DB	Bootstrap	2 SPC						0.6	—							2	4-25	MR11-DB
MS11	Semiconductor Mem	(11/45)							—			772 100	114			1	4-303	MS11
PC11	Paper Tape	SPC + PAN	10½		50	10-40	10-90	1.5	3		350	777 550	70, 74	4		1	4-306	PC11
PR11	Paper Tape (rdr)	SPC + PAN	10½		50	10-40	10-90	1.5	3		350	777 550	070	4		1	4-306	PR11
RK05	Disk Drive	PAN	10½		110	10-40	10-90	—	2		160					—	4-314	RK05
RK11-D	Disk & Control	SU + PAN	10½	X	250	10-40	10-90	7.5	2		200	777 400	220	5	X	1	4-314	RK11-D
RJP04	Disk & Control	2 SU + FS	40 x 31 x 32		600	15-32	20-80	16		3 phase power	2100		254	5	X	1	4-326	RJP04
RJS04	Disk & Control	2 SU + PAN	16	X	350	10-40	10-90	16	6	0.6A @ −15V	450	772 040	204	5	X	1	4-336	RJS04
RP03	Disk Drive	FS	40 x 30 x 24		415	15-32	20-80	—	—	6A @ 230 VAC	1300					—	4-375	RP03
RP04	Disk Pack	FS	40 x 31 x 32		600	15-32	20-80	—		3 phase power	2100					—	4-326	RP04
RS04	Disk Drive	PAN	16		120	10-40	10-90	—	6		350					—	4-356	RS04
RP11-C	Disk & Control	CAB + FS		X	740	15-32	20-80	—	7	6A @ 230 VAC	2100	776 710	254	5	X	1	4-375	RP11-C
TA11	Cassette	SPC + PAN	5¼			10-40	20-80	1.5	1		120	777 500	260	6		1	4-385	TA11
TC11-G	DECtape & Control	PAN + PAN	10½ + 10½	X	250	15-32	20-80	—	9		870	777 340	214	6	X	1	4-390	TC11-G
TM11	Magtape & Control	PAN + PAN	26 + 10½	X	500	15-32	20-80	—	9		1000	772 520	224	5	X	1	4-424	TM11
TJU16	Magtape & Control	2 SU + CAB		X	500	15-32	20-80	16	8	0.6A @ −15V	1000				X	1	4-403	TJU16
TU10	Magtape	PAN	26	X	450	15-32	20-80	—	9		1000					—	4-424	TU10
TU16	Magtape	PAN	26	X	450	15-32	20-80	—	8		900					—	4-403	TU16
TU56	DECtape	PAN	10½		80	15-32	20-80	—	3		350					—	4-390	TU56
UDC11	I/O Subsystem	CAB				10-40	10-90	—				771 774	234	4, 6		2	4-438	UDC11
VR01	Display	PAN	10½		30				1		120					—	4-445	VR01
VR14	Display	PAN	10½		75				4		400					—	4-446	VR14
VT01	Display	TT	12 x 12 x 23		50				2.2		250					—	4-448	VT01
VT05	Alphanum Term	TT	12 x 19 x 30		55	10-40	10-90	—	2		130					—	4-449	VT05
VT50	Alphanum Term	TT	14 x 21 x 28		45	10-40	10-90	—	1		110					—	4-455	VT50

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Maynard, Massachusetts

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