DEC-11-HBMAA-E-D

BM792 read-only-memory and MR11-DB bootstrap loader

digital equipment corporation · maynard, massachusetts

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual provides the user with theory of operation, programming information, and schematics necessary to understand and program the BM792 Read-Only-Memory (ROM). The level of discussion assumes that the reader is familiar with basic digital computer theory.

Although the input and output signals of the ROM are carried by the Unibus (TM), it is beyond the scope of this manual to describe the Unibus itself. A detailed description of the Unibus is presented in the *PDP-11 Peripherals Handbook*.

1.2 GENERAL DESCRIPTION

The BM792 is a 32-word read-only-memory (ROM). The diode matrix and address selection circuits that constitute the ROM are mounted on an extra-width quad-board module. This module is inserted in either one of the two small peripheral controller slots in the PDP-11 processor or in one of the four slots in the DD-11 peripheral mounting panel.

The ROM is available either unprogrammed (designated BM792) or preprogrammed (designated BM792-Y X, where the letter in the X position identifies the program). The unprogrammed module can be programmed to form code conversion tables or contain frequently-used mathematical values and subroutines. These applications of the ROM provide an access time of 100 ns, which can increase the program speed.

Preprogrammed ROMs are used for implementing small standard programs required in PDP-11 System operation, such as bootstrap loaders for paper tape or DECtape. The preprogrammed ROMs that are available at publication of this manual are described in the Appendices and listed in Table 1-1. As additional preprogrammed ROMs become available, additional appendices will be published to describe them.

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Table 1-1
Preprogrammed ROMs

Module	Option	No. of Words	Address Range	Power-Up Vector	Devices	No. of Words Read-In	Loading Area
M792-YA	BM792-YA	32	773000-773077	No	KL, DL-A, DL-B, PC, PR	162 max.	Highest Memory
M792-YB	BM792-YB	32	773100-773177	No	TC, RC, RF, RK, RP	256	0 and up
M792-YC	BM792-YC	32	773200-773277	No	CR, CM	Variable	Variable
M792-YD M792-YE	MR11-DB	64	773100-773277	Yes (Except TM)	TC, TM, RC, RF, RK, RP	TM:256 Others:512	0 and up
M792-YF	BM792-YF	32	773200-773277	No	TC, RK, RF	256	0 and up
M792-YH	BM792-YH	32	773300-773377	Yes	TA	64	0 and up

CHAPTER 2
DETAILED DESCRIPTION

2.1 BASIC OPERATION

The ROM diode matrix contains 32 16-bit words, each of which can be applied to the bus under program control. The ROM responds only to a DATI from the Unibus, DATO, DATOB, and DATIP are ignored. A block diagram of the ROM is shown in Figure 2-1.

When both a DATI and a ROM address are sent to the ROM, the word in the addressed location of the diode matrix is applied to the Unibus. When the ROM address is received, the 5-bit code on address lines A01 through A05 is decoded to apply a signal to the cathodes of the diodes in the addressed word location. The word in the addressed location is transferred through the output buffer to data lines D00 through D15 of the Unibus.

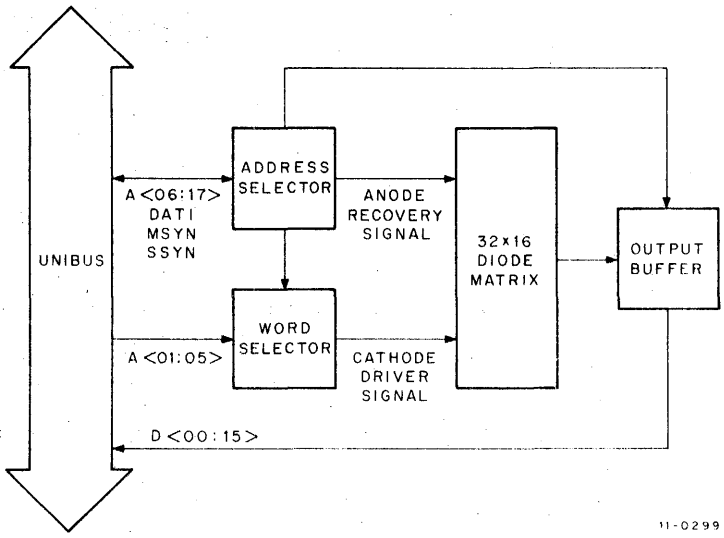

Figure 2-1 ROM Block Diagram

2.2 ADDRESS SELECTION

The address word format for the ROM is shown in Figure 2-2. Octal addresses for the ROM must be of the 773XXX format. The ROM reads-out only full 16-bit words and does not issue byte data; thus, address bit A00 is not used.

The addresses are further divided into eight groups, which are determined by address bits A08, A07, and A06 and listed in Table 2-1.

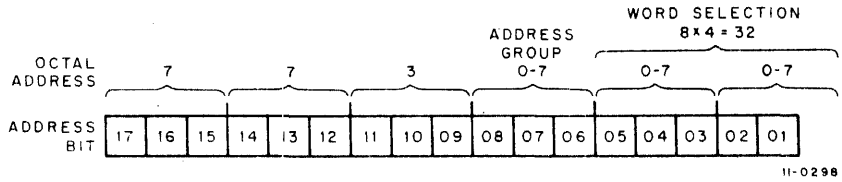

Figure 2-2 ROM Address Word Format

Table 2-1
ROM Addresses

Address Word Bit			Address Ranges	Preprogrammed ROMs
A08	A07	A06		
0	0	0	773000 - 773076	BM792-YA
0	0	1	773100 - 773176	BM792-YB, YD
0	1	0	773200 - 773276	BM792-YC, YE, YF
0	1	1	773300 - 773376	BM792-YH
1	0	0	773400 - 773476	
1	0	1	773500 - 773576	
1	1	0	773600 - 773676	
1	1	1	773700 - 773776	

In a PDP-11 System, only one ROM module can be used for each of the eight address groups. Jumpers on the module are connected in a configuration that causes the module to respond to its designated address group.

For example, when a ROM module is to be addressed in the group 773400 - 773476, bits A08, A07, and A06 of the address word contain binary 100 as shown in Table 2-1. The bus lines for these bits are shown connected to the circuits of the ROM in Figure 2-3, a simplified logic diagram of the address selection circuits. Figure 2-3 also shows the address selection circuit jumpers connected to respond to address group 773400 - 773476. Asserted bus lines are low and unasserted bus lines are high, so that the output of gate E12 at pin 14 is high and the outputs of pins 2 and 3 are low when a valid address is received. Each of the three outputs from the E12 gates is exclusive NORed with a low or a high level, depending on the jumper configuration. The outputs of the three E13 gates must be high to accomplish address selection; therefore, the jumper configuration shown responds to addresses in the 773400 - 773476 group.

The signal, which results from the decoding of bits A08, A07, and A06, is gated with a signal generated by the decoding of an address in the format 773XXX and receiving MSYN (Drawing D-CS-M792-0-1). The resulting signal (pin 10 of gate E17) is gated with a signal generated by the decoding of a DATI on the control lines. Therefore, pin 8 of gate E17 provides a low output signal when the ROM address, MSYN, and DATI are asserted on the bus. This signal at pin 8 is used to accomplish the following in the ROM circuits (see Drawing D-CS-M792-0-1):

1. Assert SSYN on the bus.
2. Activate the word selection circuits.
3. Provide a gating signal to the output buffer.

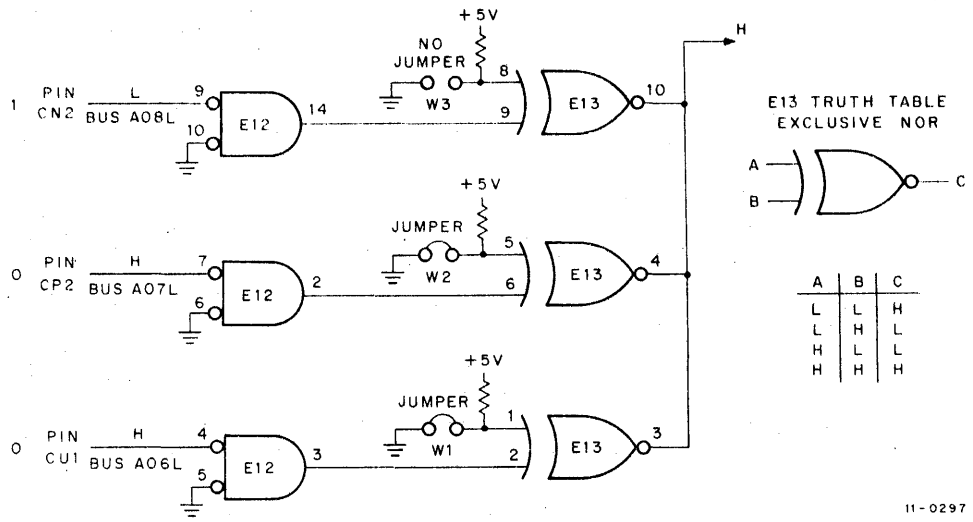

Figure 2-3 Simplified Logic Diagram of ROM Address Selection Circuits for Addresses 773400 – 773476

2.3 WORD SELECTION

Bits A05 – A01 of the address word are decoded by the word selection circuits to select one of the 32 word locations in the diode matrix. A low-level signal is then applied to the diodes in the addressed word location, resulting in 16 bits of data being read out on the data bus lines.

Because address bit A00 is not connected to the ROM, byte addressing is ignored and a 16-bit word is read onto the bus regardless of the state of A00. In the octal coding of the address, A00 is considered in designating the last octal digit. Therefore, the addresses of the words in the ROM use the following sequence:

773X00
773X02
773X04
773X06
773X10
773X12
etc.

An address of 773X01 would address the same location as 773X00, and 773X03 would be the same as location 733X02.

A simplified logic diagram for the word selection circuits is shown in Figure 2-4. This diagram illustrates how the circuits operate for a 773X04 address. Table 2-2 is a truth table for the Binary-Coded Decimal (BCD) decoders that are shown in the diagram and on Drawing D-CS-M792-0-1.

For address 773X04, binary code 000 10 is applied to the word selection circuits on address lines A05 – A01 as shown in Figure 2-4. The D input of BCD 1 receives a low signal from the address selector circuits when addressing and bus signal conditions are satisfied. All inputs to BCD 1 are low with the result that output 0 is low (refer to Table 2-2). Output 0 of BCD 1 is connected to input D of BCD 2. The other inputs of BCD 2 are as shown in Figure 2-4 when address 773X04 is received. Table 2-2 shows that output 2 of BCD 2 is low with the input signal configuration shown. Output 2 of BCD 2 is connected to the cathodes of the 16-bit positions of location 04 in

the ROM. The signal levels on the cathodes of the other 31 word locations are high. Thus, only the diodes in location 04 are forward-biased, allowing the word in this location to be read by the output buffers and applied to the Unibus.

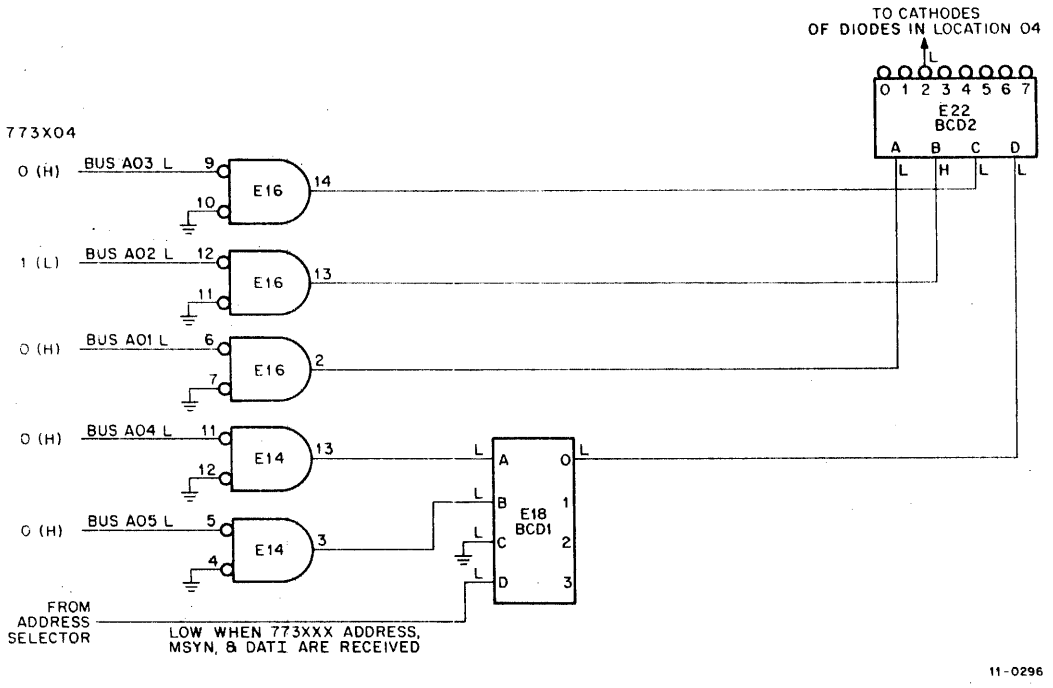

Figure 2-4 Word Selection Circuit for 773X04 Address

2.4 DIODE MATRIX AND OUTPUT BUFFER

The BM792 ROM is supplied with a complete diode matrix. A diode is wired into each of the 16-bit locations of all 32 words. The binary content of each word is determined by the presence or absence of the diodes; thus, the user can program the module by cutting out selected diodes. Presence of a diode in a bit location produces a binary 1 and absence produces a binary 0. The preprogrammed ROMs are manufactured with the diode configuration required for their programs.

A simplified logic diagram of the diode matrix and the output buffer is illustrated in Figure 2-5. The low output buffer gating signal is present when the ROM address, MSYN, and DATI are asserted on the bus (refer to Paragraph 2.2). The word select signal is low when the particular word location is selected by the decoding of bits A05 – A01 (refer to Paragraph 2.3).

Diode D492 for the D01 bit is in the circuit and is forward-biased. Therefore, a low level is gated with the output buffer gating signal, which results in the assertion of a low level on bus line D01 to signify a binary 1. The diode for the D00 bit is cut out of the circuit. Therefore, a high-level signal is gated with the output buffer gating signal, which results in the assertion of a high level on bus line D00 to signify a binary 0. The remaining bit positions in the word are read out on bus lines D02 through D015 at the same time. The configuration of diodes for the bit positions of the word determines the binary content of the word read out on the bus lines.

Table 2-2
BCD Decoder Truth Table

Input				Output							
A	B	C	D	0	1	2	3	4	5	6	7
L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L
L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	H	H	H	H	H	H	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H

L = Low
H = High

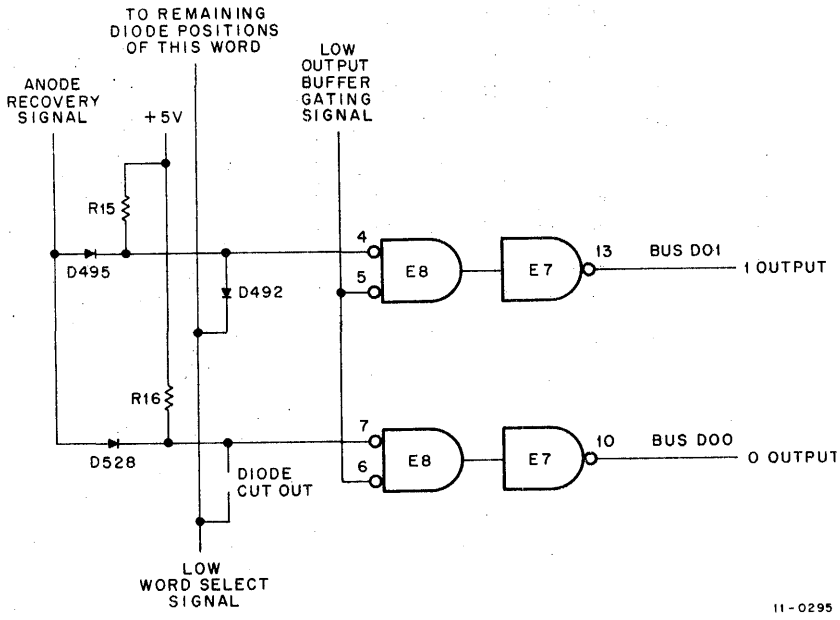

Figure 2-5 Diode Matrix and Output Buffer, Simplified Logic Diagram

2.5 ANODE RECOVERY CIRCUIT

The anode recovery circuit (see Figure 2-6) provides a voltage surge to the anodes of the diodes in the matrix immediately after a word is read out. This voltage surge charges the capacitance of the diode in the matrix and ensures that the anode lines in the matrix are at a high level for the next read out.

Transistors Q1, Q2, and Q3 (see Figure 2-6) are turned off when the ROM is not being addressed. Pin 8 of E17 goes from low to high when the bus addressing signals are concluded. The high signal turns on Q1 and subsequently Q2, which provides the positive voltage surge to the anodes of the diodes in the matrix.

Transistor Q3 of the anode recovery circuit is used as a clamp. When the voltage surge from the collector of Q2 reaches a high enough value, Q3 turns on and grounds out the surge.

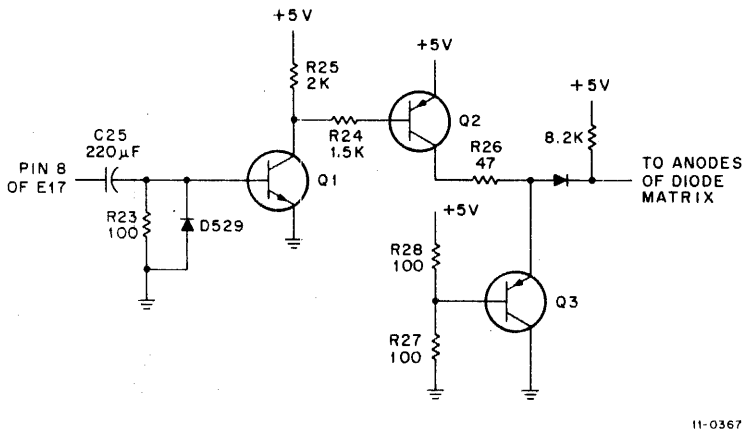

Figure 2-6 Anode Recovery Circuit

CHAPTER 3
PROGRAMMING AND OPERATION

3.1 GENERAL

The ROM operates in a manner similar to other memory devices that can be included in a PDP-11 system. When the ROM is used for storage of constants, the processor may be programmed to address the appropriate ROM location for the required constant. When the ROM is used for storage of a subroutine, a jump instruction is used to get into the subroutine and place the first address in the program counter. Then the program counter is changed to address the other sequential steps in the subroutine. The last step of a subroutine stored on the ROM should be either a jump instruction to a location out of the ROM or a return from subroutine instruction.

3.2 PROGRAMMING THE ROM

Programming the ROM is accomplished by cutting diodes out of the diode matrix in the configuration required for the binary data words to be used. The diode must be removed for each bit position that is to read out as a binary 0.

The physical orientation of the diode matrix with respect to the addresses and the bit positions is shown in Figure 3-1. Address 773X00 is shown with diodes removed in a configuration that reads out the binary word 1 010 010 011 101 011. With Figure 3-1 and a binary listing of up to 32 16-bit words, the user can program his ROM module.

The ROM module must also be programmed to respond to one of the address groups determined by address bits A08, A07, and A06 (refer to Table 2-1). Figure 3-1 shows the locations of the three sets of address-bit jumper terminals which are labeled W1, W2, and W3 on the ROM printed circuit board. The relationship between the jumper terminals and the address bit is as follows:

W1	A06
W2	A07
W3	A08

Jumper wires are connected across each of the three sets of jumper terminals on an unprogrammed ROM when it is shipped from the factory. The jumper wire must be cut out from between the two terminals for each address bit (A08, A07, or A06), that is a binary 1 in the ROM address used.

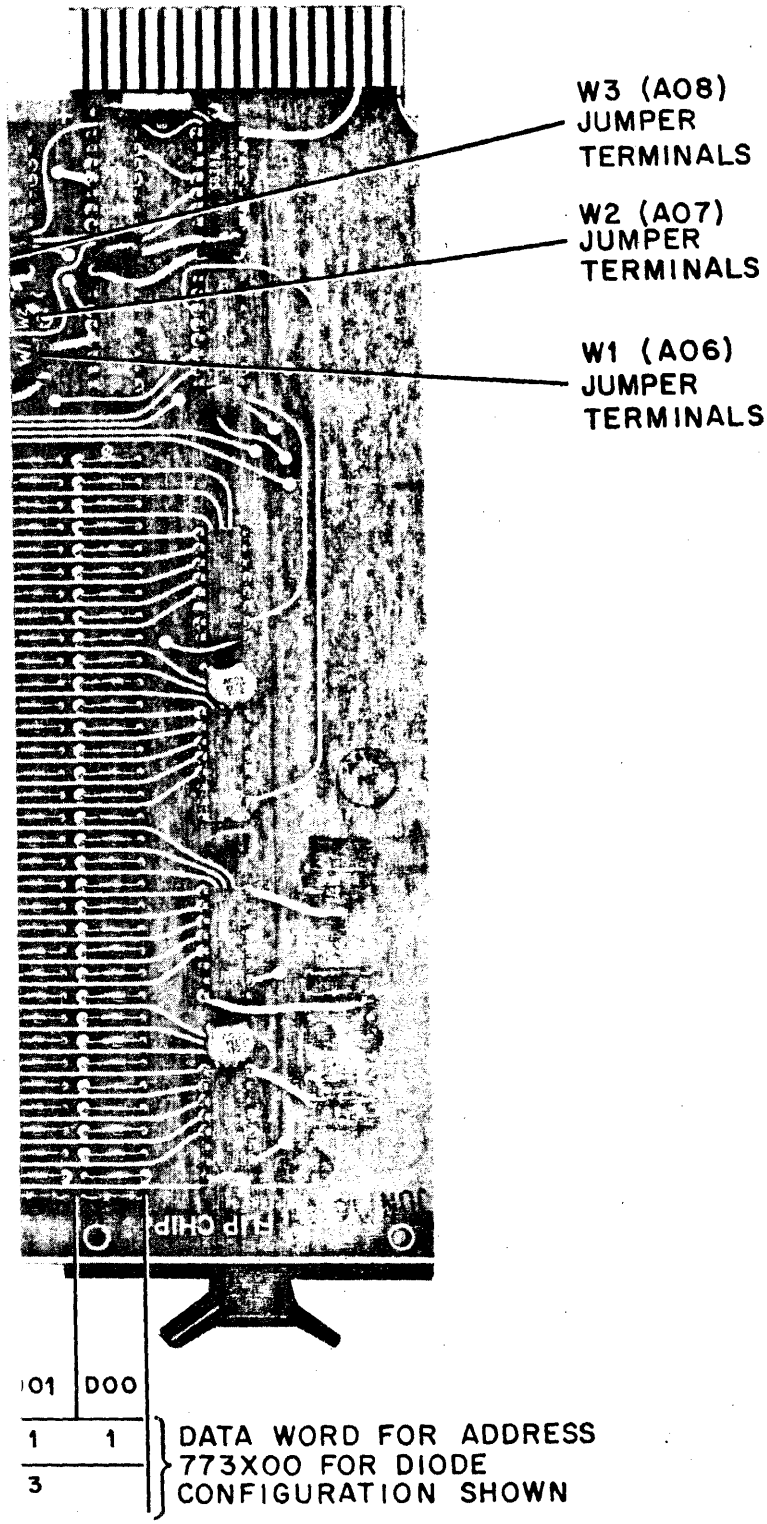

Figure 3-1 Physical Locations of Addresses and Bits in the ROM Diode Matrix

CHAPTER 4
ROM ENGINEERING DRAWINGS

The following engineering drawings are applicable to the BM792 ROM:

Title	Drawing No.	Rev.	Page
ROM Diode Matrix M792	D-CS-M792-0-1	D	4-3
ROM Diode Matrix M792-YA	D-CS-M792-YA-1	H	4-5
ROM Diode Matrix	D-CS-M792-YB-1		4-7
ROM Card Reader Bootstrap	D-CS-M792-YC-1		4-9
ROM Diode Matrix	D-CS-M792-YD-1	A	4-11
ROM Diode Matrix	D-CS-M792-YE-1	A	4-15
ROM Diode Matrix	D-CS-M792-YF-1		4-19
Cassette Bootstrap ROM	D-CS-M792-YH-1		4-23

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UNLESS OTHERWISE INDICATED:
Ø = SPLIT LUGS, ---- = JUMPERS
CAPACITORS ARE .01uf, 100V, 20%
RESISTORS ARE 8.2K, 1/4W, 5%
DIODES ARE D664

E2, E4, E6, E8, E10, E12, E14, E15, E16 = DEC380
E17 = DEC7400N
E1, E3, E5, E7, E11 = DEC8881
E13 = DEC8242
E9 = DEC314
E18 – E22 = DEC8251

PIN 8 = +5V ON DEC380, DEC314
PIN 1 = GND

PIN 14 = +5V ON DEC8881, DEC8242, DEC7400N
PIN 7 = GND

PIN 16 = +5V ON DEC8251
PIN 8 = GND

E19–22 PINS 6 AND 7 NOT CONNECTED
E18 PINS 4,5,6,7,9 NOT CONNECTED
W1, W2, W3 DESIGNATES WIRE JUMPERS

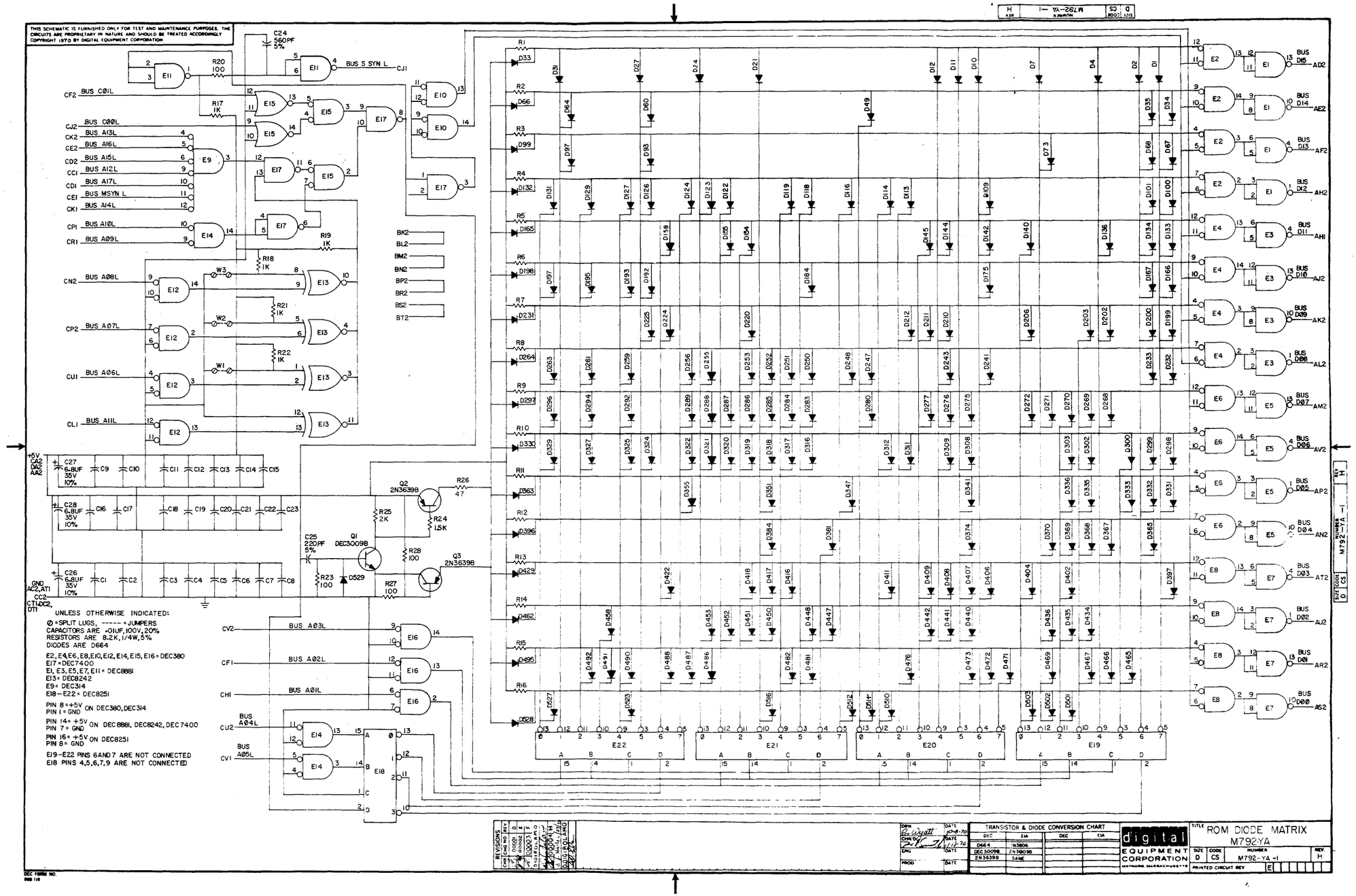
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	1N3604		
DEC3009B	2N3009		
2N3639B	NONE		

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: ROM DIODE MATRIX M792

SIZE D | CODE CS | NUMBER M792-0-1 | REV D

PRINTED CIRCUIT REV B C D E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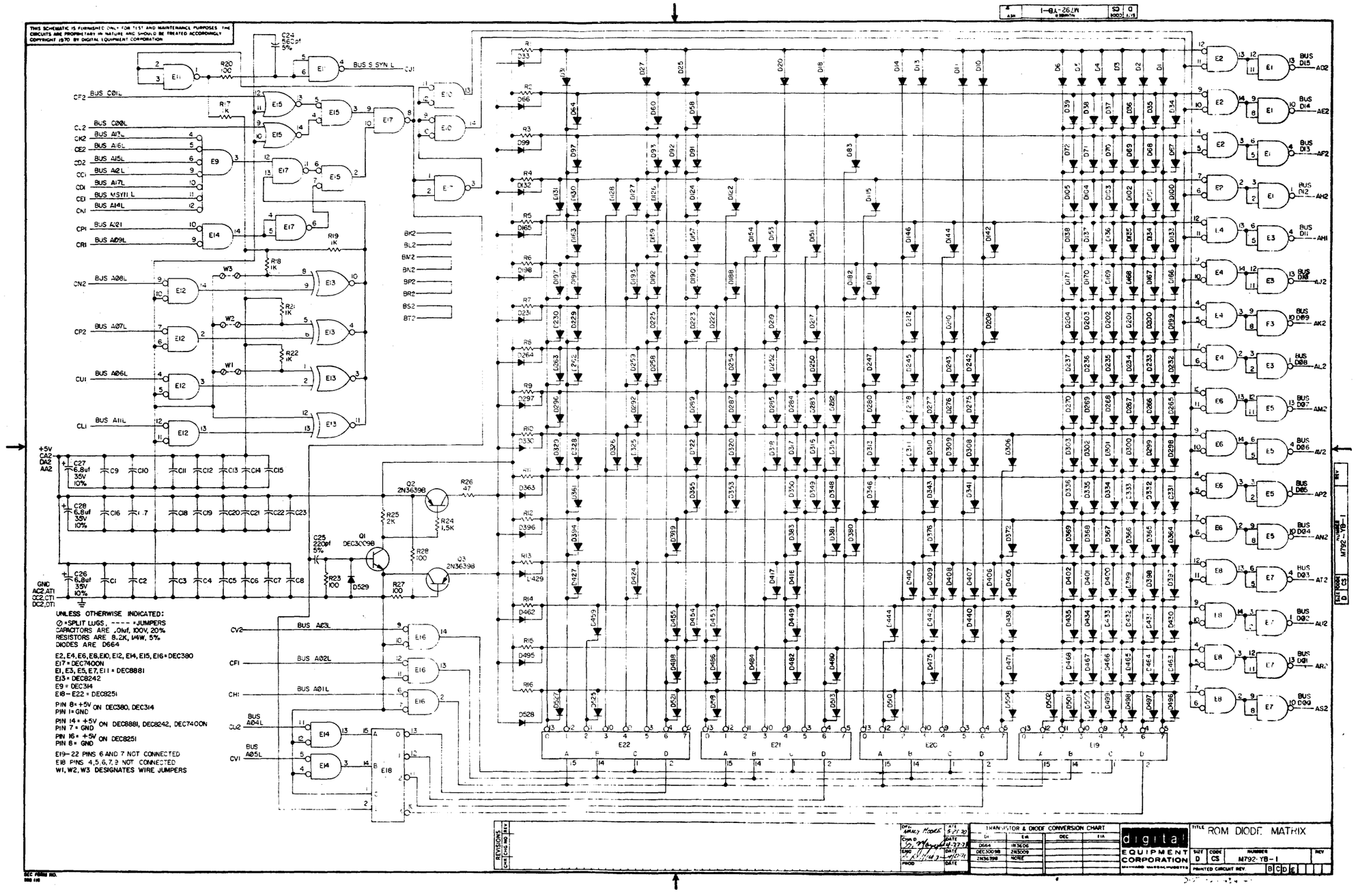
E17 = DEC7400
E1, E3, E5, E7, E11 = DEC8881
E13 = DEC8242
E9 = DEC314
E18 – E22 = DEC8251
PIN 8 = +5V ON DEC380, DEC314
PIN 1 = GND
PIN 14 = +5V ON DEC8881, DEC8242, DEC7400
PIN 7 = GND
PIN 16 = +5V ON DEC8251
PIN 8 = GND
E19 – E22 PINS 6 AND 7 ARE NOT CONNECTED
E18 PINS 4,5,6,7,9 ARE NOT CONNECTED
TRANSISTOR & DIODE CONVERSION CHART
DEC 3009B 2N3639B
DEC 3009B 2N3009B
2N3639B SAME
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE ROM DIODE MATRIX
M792-YA
SIZE D CODE CS NUMBER M792-YA-1 REV. H
PRINTED CIRCUIT REV E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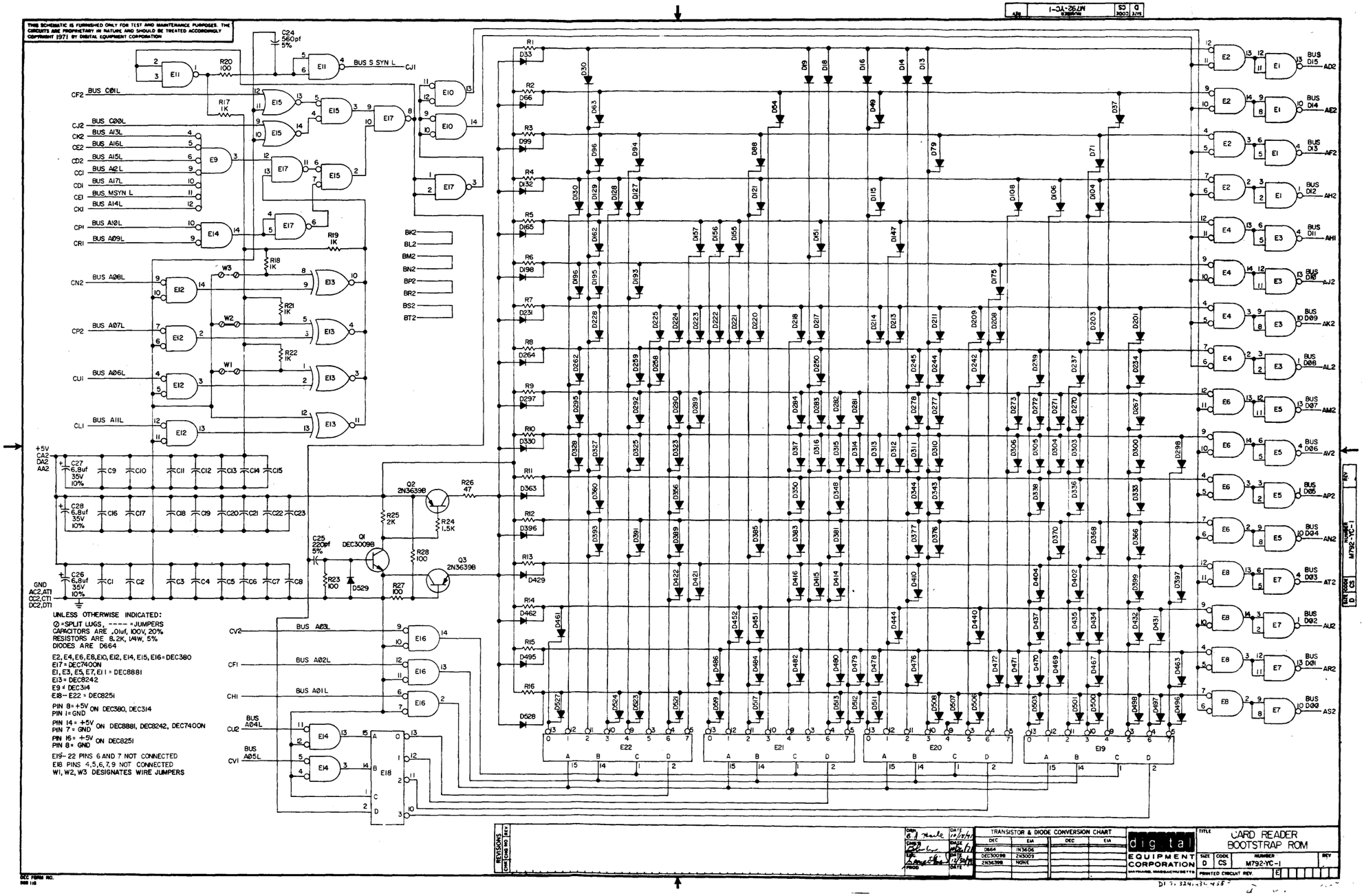
E17 = DEC7400N
E1, E3, E5, E7, E11 = DEC8881
E13 = DEC8242
E9 = DEC314
E18 - E22 = DEC825I
PIN 8 = +5V ON DEC380, DEC314
PIN 1 = GND
PIN 14 = +5V ON DEC8881, DEC8242, DEC7400N
PIN 7 = GND
PIN 16 = +5V ON DEC825I
PIN 8 = GND
E19 - 22 PINS 6 AND 7 NOT CONNECTED
E18 PINS 4,5,6,7,9 NOT CONNECTED
W1, W2, W3 DESIGNATES WIRE JUMPERS
TRANSISTOR & DIODE CONVERSION CHART
digital
EQUIPMENT CORPORATION
ROM DIODE MATRIX
M792-YB-1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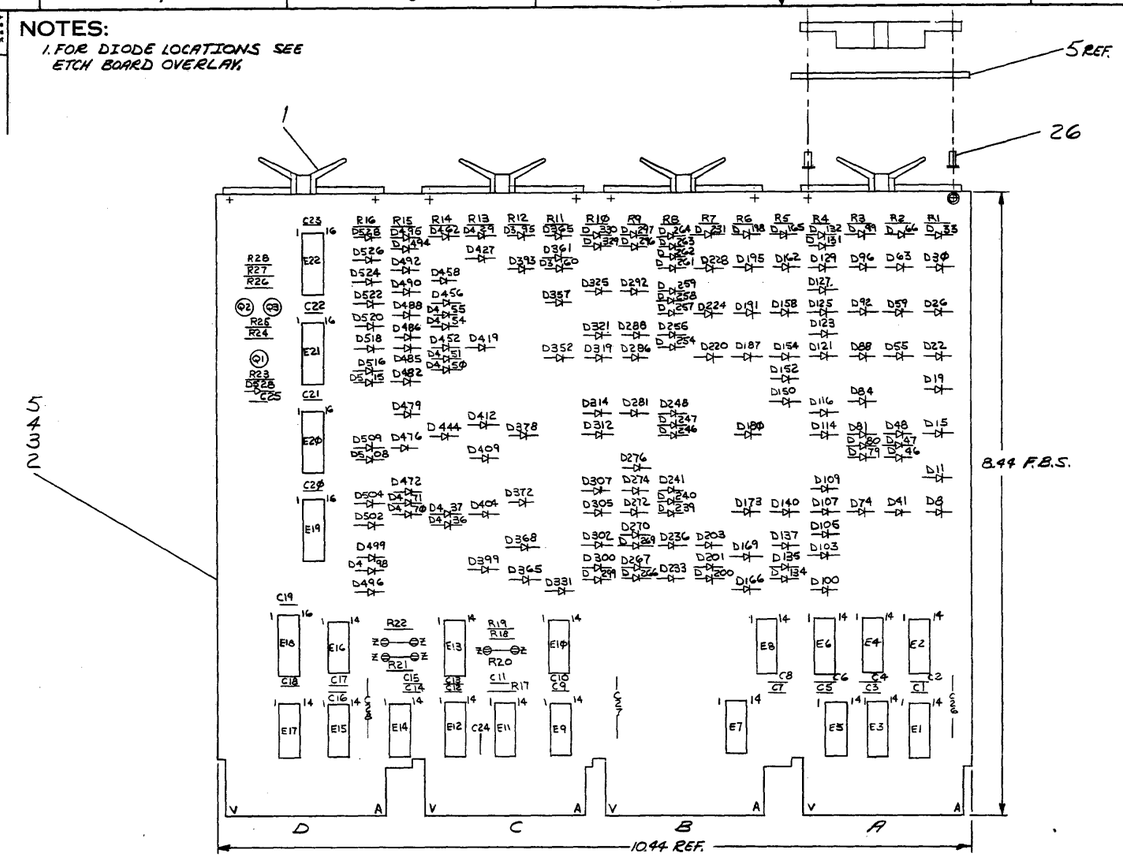
PIN 1=GND
PIN 14=+5V ON DEC8881, DEC8242, DEC7400N
PIN 7=GND
PIN 16=+5V ON DEC8251
PIN 8=GND
E19-22 PINS 6 AND 7 NOT CONNECTED
E18 PINS 4,5,6,7,9 NOT CONNECTED
W1, W2, W3 DESIGNATES WIRE JUMPERS
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA
D664 1N3606
DEC30098 2N3009
2N3639B NONE
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE CARD READER BOOTSTRAP ROM
SIZE D CODE CS NUMBER M792-YC-1 REV
PRINTED CIRCUIT REV. E
M792-YC-1

This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.

NOTES:

1. FOR DIODE LOCATIONS SEE ETCH BOARD OVERLAY.



QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
6		SPLIT LUGS	9006735	26
8		EYELET #GS4-7 E.B. STIMPSON	9006732	25
165	SEE NOTE #1	DIODE D664	1100114	24
1	E13	I.C. DEC 8242	1909712	23
5	E1, E3, E5, E7, E11	I.C. DEC 8881	1909705	22
1	E9	I.C. DEC 314	1909704	21
5	E18-E22	I.C. DEC 8251	1909594	20
9	E2, E4, E6, E8, E10, E12 E14-E16	I.C. DEC 380	1909485	19
1	E17	I.C. DEC 7400N	1905575	18
1	Q1	TRANSISTOR DEC 3009B	1503100	17
2	Q2, Q3	TRANSISTOR 2N3639B	1502762	16
16	R1-R16	RES. 8.2K 1/4W 5%	1303179	15
1	R24	RES. 1.5K 1/4W 5%	1300391	14
5	R17-R19, R21, R22	RES. 1K 1/4W 5%	1300365	13
1	R25	RES. 2K 1/4W 5%	1302388	12
4	R20, R23, R27, R28	RES. 100Ω 1/4W 5%	1300229	11
1	R26	RES. 47Ω 1/4W 5%	1300202	10
3	C26-C28	CAP 6.8 μF 35V 10%	1005306	9
23	C1-C23	CAP. .01μF 100V 20% DISC	1001610	8
1	C24	CAP. 560μμF 100V 5% DM	1000025	7
1	C25	CAP. 220μμF 100V 5% DM	1000021	6
1		ETCHED CIRCUIT BOARD	5008917	5
REF		MODULE ECO HISTORY	B-MH-M792-YD-6	4
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M792-YD-5	3
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M792-YD-4	2
4		HANDLE FLIP CHIP-MAGENTA	9008337-06	1

PARTS LIST

FIRST USED ON OPTION MODEL: 11/45

ETCH BOARD REV: E

IC TYPE	GND	+ 5V
8251	8	16
319	1	8
380	1	8

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

DEC NO.	EIA NO.	DEC NO.	EIA NO.
D664	1N3606		
DEC 3009B	2N3646		
2N3639B	SAME		

SEMICONDUCTOR CONVERSION CHART

REVISIONS: CHK | CHANGE NO. | REV

A. HELENIUS 7-27-72 — M792-YD-00001 — ORIGINATED — A

DRN. A. Kibort DATE 5-12-72
CHK'D. DATE 5/14/72
ENG. DATE 5/24/72
PROJ. ENG. DATE 5/25/72
PROD. DATE 5/25/72

NEXT HIGHER ASSY: B-DD-MR11-DB

SCALE
SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

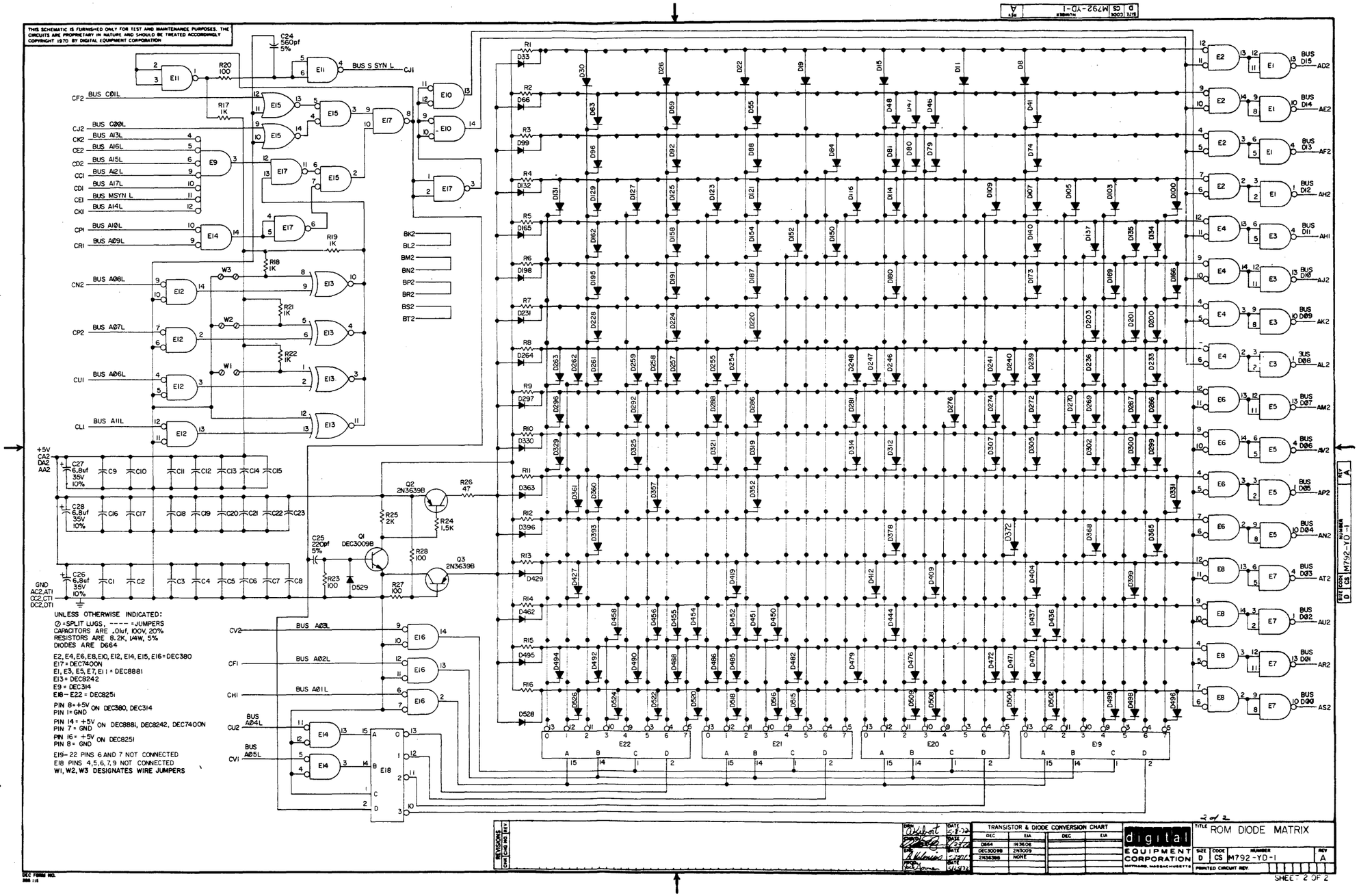
TITLE: ROM DIODE MATRIX

SIZE D | CODE CS | NUMBER M792-YD-1 | REV. A

DIST.

BRUNING 40-522 16699

DEC FORM NO DRD-135A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UNLESS OTHERWISE INDICATED:
Ø = SPLIT LUGS, ---- = JUMPERS
CAPACITORS ARE .01uf, 100V, 20%
RESISTORS ARE 8.2K, 1/4W, 5%
DIODES ARE D664
E2, E4, E6, E8, E10, E12, E14, E15, E16 = DEC380
E17 = DEC7400N
E1, E3, E5, E7, E11 = DEC8881
E13 = DEC8242
E9 = DEC314
E18 – E22 = DEC8251
PIN 8 = +5V
PIN 1 = GND
ON DEC380, DEC314
PIN 14 = +5V
PIN 7 = GND
ON DEC8881, DEC8242, DEC7400N
PIN 16 = +5V
PIN 8 = GND
ON DEC8251
E19 – 22 PINS 6 AND 7 NOT CONNECTED
E18 PINS 4, 5, 6, 7, 9 NOT CONNECTED
W1, W2, W3 DESIGNATES WIRE JUMPERS
TRANSISTOR & DIODE CONVERSION CHART
DEC
EIA
D664
IN3606
DEC30098
2N3009
2N3638B
NONE
digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE ROM DIODE MATRIX
SIZE D
CODE CS
NUMBER M792-YD-1
REV A
PRINTED CIRCUIT REV.
SHEET 2 OF 2
REVISIONS
DEC FORM NO.

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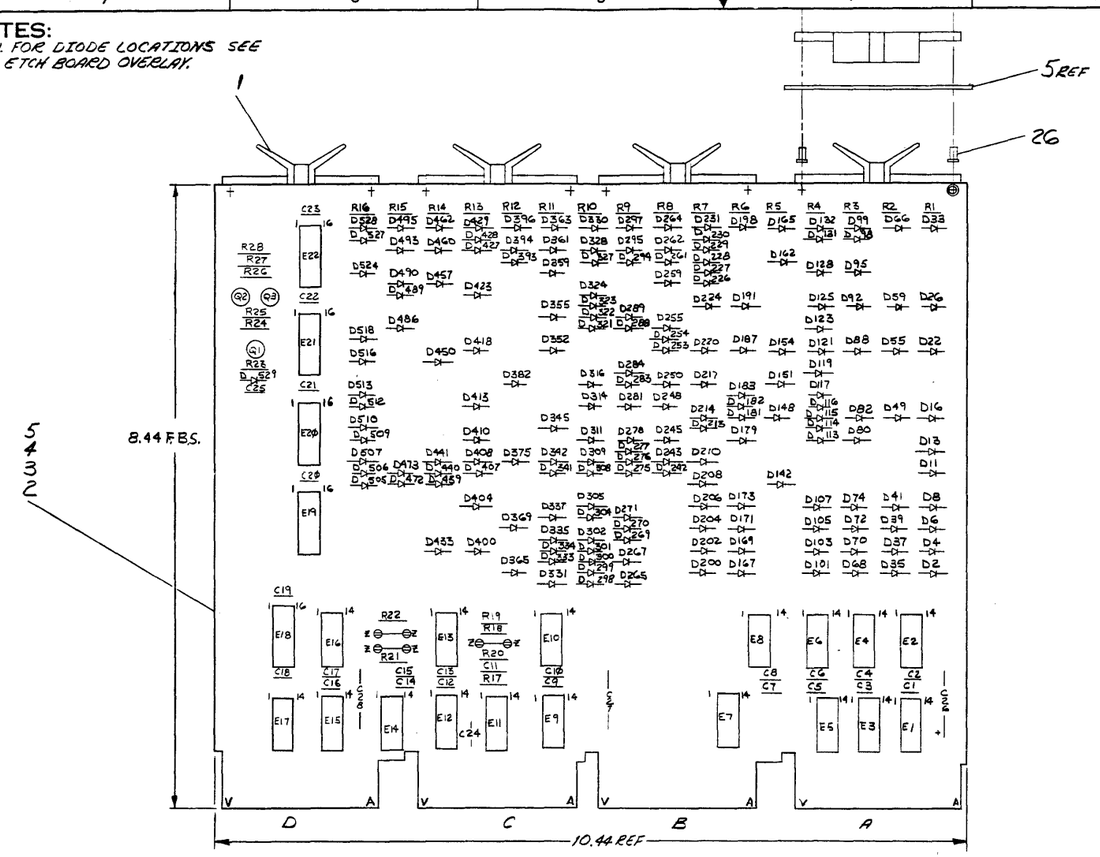
NOTES:
1. FOR DIODE LOCATIONS SEE ETCH BOARD OVERLAY.



QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
6		SPLIT LUGS	9006785	26
8		EYELET #GS4-7 E.B. STIMPSON	9006732	25
1	E13	I.C. DEC 8242	1909712	24
5	E1, E3, E5, E7, E11	I.C. DEC 8881	1909705	23
1	E9	I.C. DEC 314	1909704	22
5	E18-E22	I.C. DEC 8251	1909594	21
9	E2, E4, E6, E8, E10, E12, E14-E16	I.C. DEC 380	1909485	20
1	E17	I.C. DEC 7400N	1905575	19
1	Q1	TRANSISTOR DEC3009B	1502100	18
2	Q2, Q3	TRANSISTOR 2N3639B	1502762	17
16	R1-R16	RES. 8.2K 1/4W 5%	1303179	16
1	R24	RES. 1.5K 1/4W 5%	1300391	15
5	R17-R19, R21, R22	RES. 1K 1/4W 5%	1300365	14
1	R25	RES. 2K 1/4W 5%	1302388	13
4	R20, R23, R27, R28	RES. 100Ω 1/4W 5%	1300229	12
1	R26	RES. 47Ω 1/4W 5%	1300202	11
186	SEE NOTE #1	DIODE D664	1100114	10
3	C26-C28	CAP. 6.8μF 35V 10% TANT	1005306	9
23	C1-C23	CAP. .01μF 100V 20%	1001610	8
1	C24	CAP. 560μμF 100V 5% DM	1000025	7
1	C25	CAP. 220μμF 100V 5% DM	1000021	6
1		ETCHED CIRCUIT BOARD	5008917	5
REF		MODULE ECO HISTORY	B-MH-M792-YE-6	4
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M792-YE-5	3
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M792-YE-4	2
4		HANDLE, FLIP CHIP-MAGENTA	9008337-06	1

PARTS LIST

FIRST USED ON OPTION MODEL: 11/45

ETCH BOARD REV: E

IC TYPE	GND	+ 5V
DEC 8251	8	16
DEC 314	1	8
DEC 380	1	8

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

DEC NO.	EIA NO.	DEC NO.	EIA NO.
2N3639B	SAME		
DEC 3009B	2N3646		
D664	1N3606		

SEMICONDUCTOR CONVERSION CHART

REVISIONS: CHK | CHANGE NO. | REV

A HELENIUS 7-27-72 — M792-YE-00001 — ORIGINATED — A

DRN. A. Kelsey DATE 5/17/72
CHK'D. DATE
ENG. H. Helenius DATE
PROJ. ENG. H. Helenius DATE 5/25/72
PROD. Vace Gorman DATE 5/25/72

NEXT HIGHER ASSY: B-DD-MR11-DB

SCALE: —

SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: ROM DIODE MATRIX

SIZE D | CODE CS | NUMBER M792-YE-1 | REV. A

DIST.

BRUNING 40-522 16699

DEC FORM NO DRD-135A

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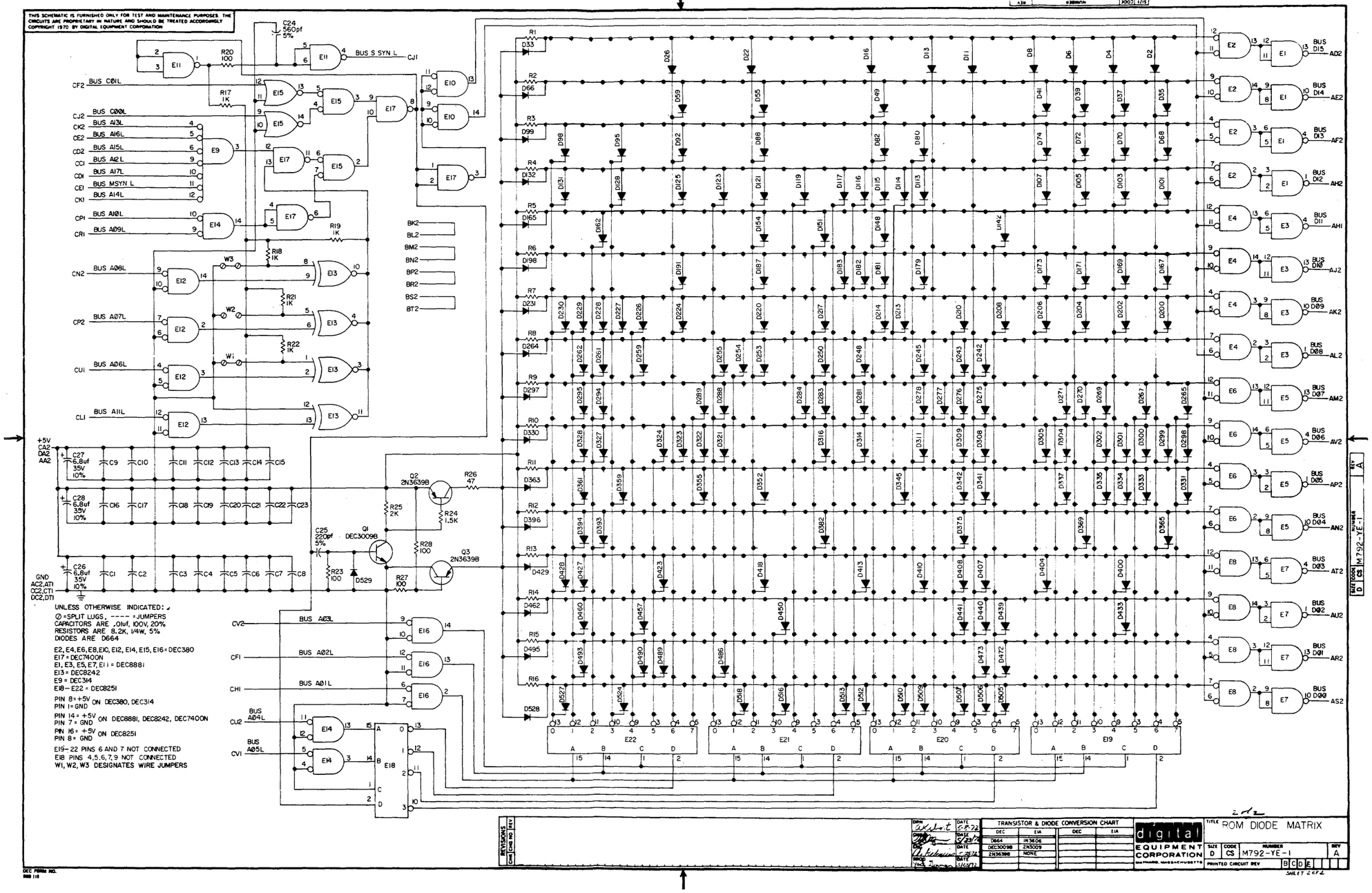

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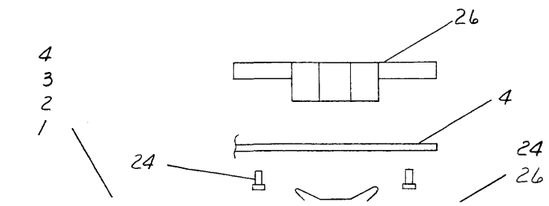
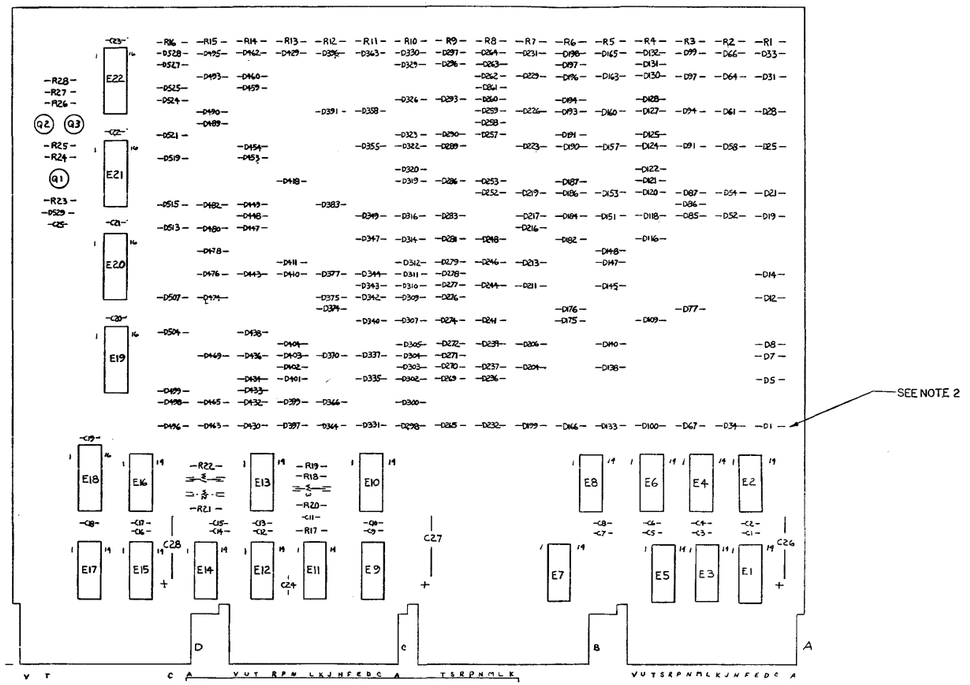
NOTES:

1. ON ITEM #9 USE OVERLAY TO DETERMINE WHICH 208 DIODES OF D1 THRU D529 ARE USED.
2. ON ITEM #19 ALL 9 CHIPS MUST BE EITHER DEC 380'S OR ITS SUBSTITUTE, 11380 IC'S. COMBINATIONS ARE NOT ALLOWED ON THE SAME OPTION.





ALLOWABLE SUBSTITUTION LIST			
ORIG PART #	SUBSTITUTION PART		ITEM #
	DESCRIPTION	PART #	
1909485	IC 11380	1911113	19

DEC 8251	8	16
DEC 314	1	8
DEC 380	1	8
IC TYPE	GND	+ 5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

DRWING 40 522 18699

DEC FORM NO. DRD-135A

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	X-CO-M792-YF-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M792-YF-5	2
REF		MODULE ECO HISTORY	B-MH-M792-YF-6	3
1		ETCHED CIRCUIT BOARD	5C0897	4
1	C25	CAP 220PF 100V 5% DM	1000021	5
1	C24	CAP 560 PF 100V 5% DM	1000025	6
23	C1 THRU C23	CAP .01UF 100V 20% DISC	1001010	7
3	C26, C27, C28	CAP 6.8UF 35V 10% SLANT	1005306	8
208	D1 THRU D529 SEE NOTE #1	DIODE D664	1100114	9
1	R26	RES 47 1/4 W 5%	1300202	10
4	R20, R23, R27, R28	RES 100 1/4 W 5%	1300229	11
5	R17, R18, R19, R21, R22	RES 1K 1/4 W 5%	1300305	12
1	R25	RES 2K 1/4 W 5%	1302383	13
1	R24	RES 1.5K 1/4 W 5%	1300391	14
16	R1 THRU R16	RES 8.2K 1/4 W 5%	1303179	15
2	Q2, Q3	TRANSISTOR 2N3639B	1502762-00	16
1	Q1	TRANSISTOR DEC 3009 B	1503100	17
1	E17	IC DEC 7400	1905575	18
SEE NOTE 2 9	E2, E4, E6, E8, E10 E12, E14, E15, E16	IC DEC 380 A	1909485	19
5	E18 THRU E22	IC DEC 8251 B	1909594	20
1	E9	IC DEC 314 A	1909704	21
5	E1, E3, E5, E7, E11	IC DEC 8881	1909705	22
1	E13	IC DEC 8212	1909712	23
8		EYELET #GS4-7	9006732	24
6		SPLIT LUG	9006785	25
4		HANDLE, FLIPCHIP MAGENTA	9008537-5	26

PARTS LIST

ETCH BOARD REV E

FIRST USED ON OPTION MODEL M972-YF

REVISIONS					
REV	CHANGE NO.	CHK			
A	M792-YF-0000	R. Eliason	7/21/73		
B	M792-YF-2	Nelson Roy	9/13/73		

SEMICONDUCTOR CONVERSION CHART			
DEC NO.	EIA NO.	DEC NO.	EIA NO.
		2N3639B	2N3639B
		DEC 3009B	2N3009
		D664	1N3606

DRN. L. Kalagher DATE 10-27-72
CHK'D. J. Guttag DATE 11-27-72
ENG. E. Gault DATE 12-28-72
PROJ. ENG. E. Gault DATE 12-28-72
PROG. A. Fairbairn DATE 12/19/72

NEXT HIGHER ASSY B-DD-M792-YF

SCALE ++

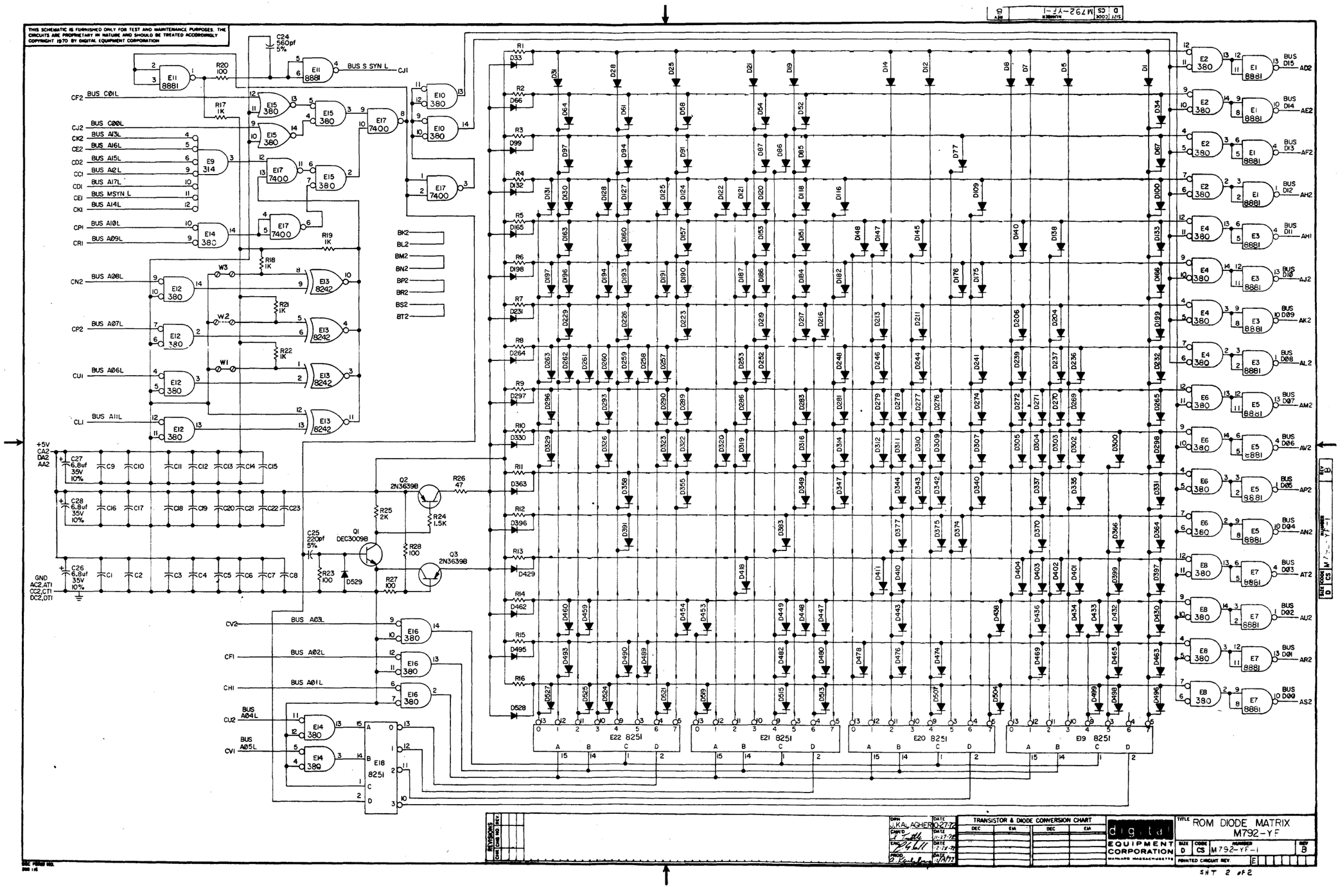
SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE ROM DIODE MATRIX

SIZE D CODE CS NUMBER M792-YF-1 REV. B

DIST.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TRANSISTOR & DIODE CONVERSION CHART
digital
EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS
TITLE ROM DIODE MATRIX M792-YF
SIZE D CODE CS NUMBER M792-YF-1 REV B
PRINTED CIRCUIT REV E
SHT 2 OF 2

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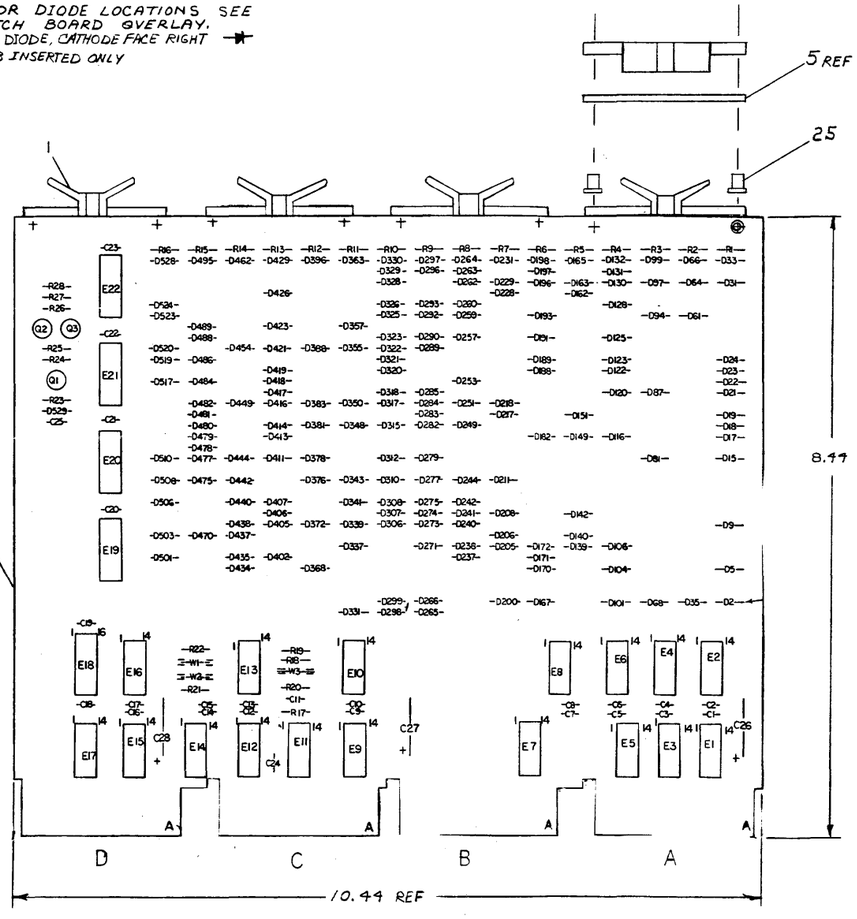
NOTES:

1. FOR DIODE LOCATIONS SEE ETCH BOARD OVERLAY.
2. ALL DIODE, CATHODE FACE RIGHT →
3. W3 INSERTED ONLY



QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
4		HANDLE FLIPCHIP MAGENTA	9008337-06	1
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M792-YH-1	2
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M792-YH-S	3
REF		MODULE ECO HISTORY	B-MH-M792-YH-6	4
1		ETCHED CIRCUIT BOARD	5006917	5
1	C25	CAP. 220 MMF 100V 5% DM	1000021	6
1	C24	CAP. 560 MMF 100V 5% DM	1000025	7
23	C1 THRU C23	CAP. .01 MF 100V 20% DISC	1001610	8
3	C26 THRU C28	CAP. 6.8 MF 35V 10%	1005306	9
1	R26	RES. 47Ω 1/4W 5%	1300802	10
4	R20, R23, R27, R28	RES. 100Ω 1/4W 5%	1300224	11
1	R25	RES. 2K 1/4W 5%	1302388	12
5	R17, R19, R21, R22	RES. 1K 1/4W 5%	1300365	13
1	R24	RES. 1.5K 1/4W 5%	1300391	14
16	R1 THRU R16	RES. 8.2K 1/4W 5%	1303179	15
2	Q2, Q3	TRANSISTOR 2N3639B	1502762	16
1	Q1	TRANSISTOR DEC 3009B	1503100	17
1	E17	I.C. DEC 7400N	1905575	18
9	E2, E4, E6, E8, E10, E12, E14, E16	I.C. DEC 380	1904485	19
5	E18 THRU E22	I.C. DEC 8251	1909594	20
1	E9	I.C. DEC 314	1909709	21
5	E1, E3, E5, E7, E11	I.C. DEC 8881	1909705	22
1	E13	I.C. DEC 8242	1909712	23
185	SEE NOTE #1	DIODE D664	1100114	24
8		EYELET #654-7 E.B. STIMPSON	9006732	25
6		SPLIT LUGS	9006735	26
A/R	W3	BUS WIRE	9107560-01	27

FIRST USED ON OPTION MODEL 11/40

PARTS LIST

ETCH BOARD REV E

8251	8	16
314	1	8
380	1	8
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

ORIGINATED	CHANGE NO.	REVISIONS	DEC NO.	EIA NO.	DEC NO.	EIA NO.
			D664	1N3606		
			DEC 3009B	2N3646		
			2N3639B	SAME		

SEMICONDUCTOR CONVERSION CHART

DRN C. Wilson 3/1/73 | CHK D. Hogan 3/2/73 | ENG F. Simon 3/26/73 | PROJ ENG F. Simon 3/26/73 | PROJ Ralph L. 3/29/73

NEXT HIGHER ASSY A-PL-BM792-YH

SCALE — | SHEET 1 OF 2

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE CASSETTE BOOTSTRAP RCM

SIZE D | CODE CS | NUMBER M792-YH-1 | REV. *

DIST.

DEC FORM NO DRD 135A

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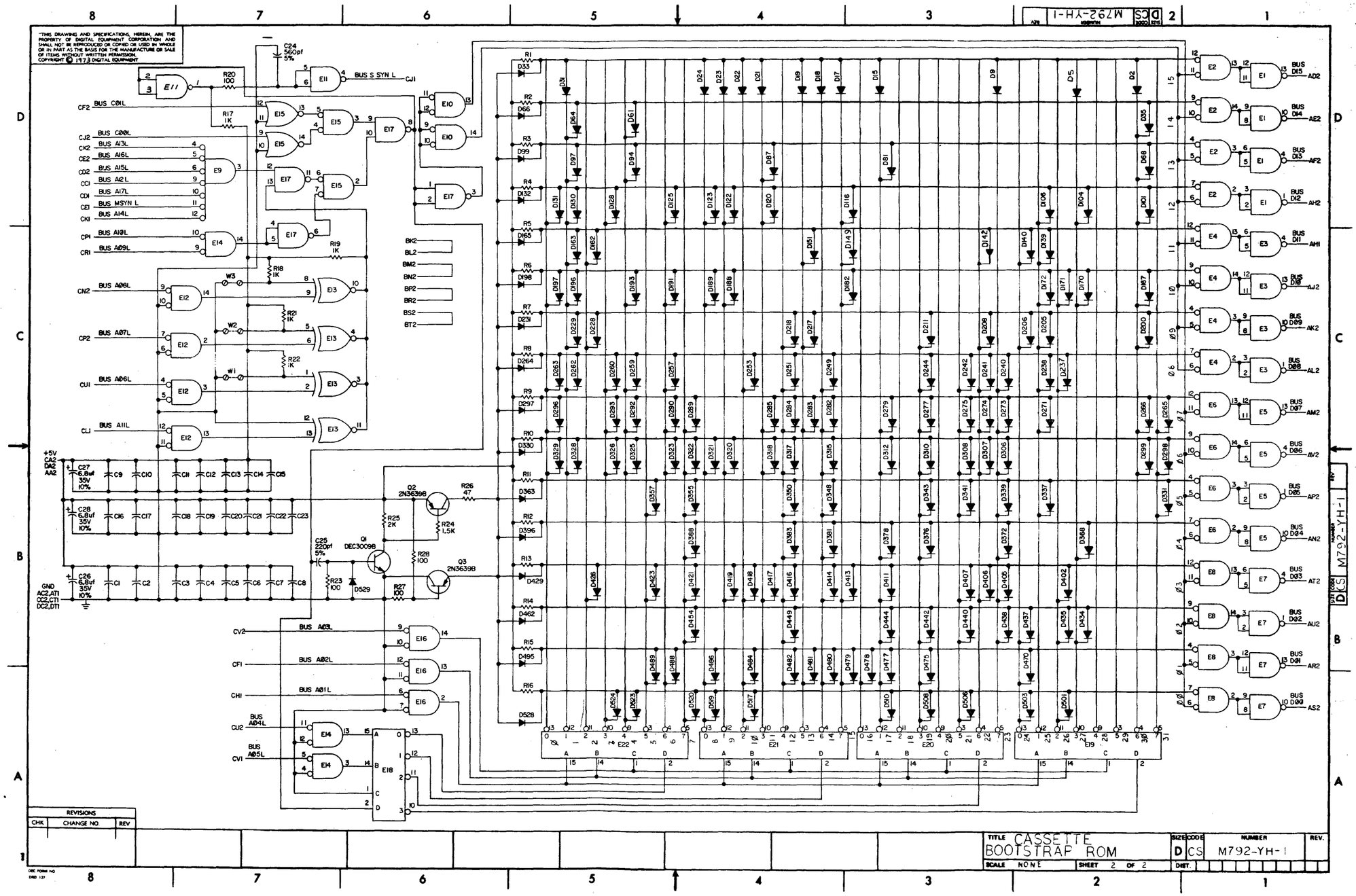

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
CASSETTE BOOTSTRAP ROM	D	CS	M792-YH-1	
SCALE NONE	SHEET 2 OF 2		DIST.	

APPENDIX A
BM792-YA PAPER-TAPE BOOTSTRAP LOADER

The BM792-YA ROM is shipped with jumper wires connected for address group 773000 - 773076, and its diode matrix is preprogrammed for a paper-tape bootstrap read-in loader program. The BM792-YA can only be used in a PDP-11 System that has at least 4K of read-write memory and either a Teletype® (KL11) or a high-speed paper-tape reader (PR11 or PC11), or both. If neither the high-speed reader nor the low-speed reader (Teletype) is available, the paper-tape bootstrap loader program will not function properly.

An absolute loader or dump program contained on a bootstrap format paper tape (described in Chapter 5 of the *Paper-Tape Software Programming Handbook,* DEC-11-GGPA-D) is loaded into read-write memory by the paper-tape bootstrap loader. The sequence of operations used by the paper-tape bootstrap loader is:

1. Determines which paper-tape reader is available. Checks the high-speed reader first and then the low-speed reader. The high-speed reader is considered unavailable if no tape is in it.
2. Determines the size of the read-write memory of the system.
3. Stores the device address (determined in Step 1 above) in the last location of read-write memory. This action is required by the absolute loader program.
4. Loads the absolute loader program from the bootstrap format tape into the read-write memory.
5. Jumps to program loaded, as specified on the bootstrap format tape.

The paper-tape bootstrap loader program and the absolute loader program require the use of 96 locations at the high end of the read-write memory. Memory locations 4, 14, 16, 20, and 22 are modified during the operation of the paper-tape bootstrap loader program. Also, the illegal memory reference (bus time-out) trap at location 4 is used extensively by this loader.

A program listing for the paper-tape bootstrap loader is provided in Table A-1. Hardware addresses in the PDP-11 use 18 bits with the result that bits A15, A16, and A17 are considered in designating the most significant octal digit of the address. The software assembler program uses 16-bit addresses so that only bit A15 is used to designate the most significant octal digit of the address. Therefore, the addresses in Table A-1 are listed as 173XXX instead of 773XXX.

The operating procedure for loading a bootstrap format paper tape with the paper-tape bootstrap loader is:

Step	Procedure
1	Set the HALT/ENABLE switch to HALT, then to ENABLE.
2	Place the bootstrap format paper tape in the reader to be used, with the special tape leader placed over the read head.
3	If the high-speed reader is to be used, set the switch to ON.

®Teletype is a registered trademark of Teletype Corporation.

Step	Procedure
4	If the low-speed reader is to be used, set the high-speed reader switch to OFF and set the low-speed reader switch to START.
5	Set the starting address, 773000, into the SWITCH REGISTER.
6	Depress the LOAD ADDR switch.
7	Depress the START switch. After a short pause, the paper tape should read in.

Table A-1

BM792-YA Paper-Tape Bootstrap Loader Program

```
                                ;REGISTERS USED: R1,R2,R3,R4,SP
        000001                  R1=%1                           ;ADDRESS POINTER
        000002                  R2=%2                           ;TEMPORARY STORAGE
        000003                  R3=%3                           ;TEMPORARY STORAGE
        000004                  R4=%4                           ;DEVICE POINTER
        000006                  SP=%6                           ;STACK POINTER
        000007                  PC=%7                           ;PROGRAM COUNTER

        177550                  HSR=177550                      ;HIGH SPEED READER ADDRESS
        177560                  LSR=177560                      ;LOW SPEED READER ADDRESS

173000  012701  160000  START:  MOV     #160000,R1              ;SET MEMORY CHECK LIMITS
173004  012702  000006          MOV     #6,R2                   ;TRAP VECTOR IS LOCATION 4/6
173010  012703  173100          MOV     #DEV+4,R3               ;POINTER TO DEVICE ADDRESSES
173014  005012                  CLR     @R2                     ;CLEAR TRAP STATUS AT LOCATION 6
173016  012742                  MOV     PC,-(R2)                ;SET TRAP ADDRESS IN LOCATION 4
173020  110776                  MOVB    PC,SP                   ;SET UP STACK OUT OF THE WAY
173022  014304  DEV1:  MOV     -(R3),R4                ;GET DEVICE ADDRESS
173024  005714                  TST     @R4                     ;CHECK AVAILABILITY OF DEVICE
173026  100775                  BMI     DEV1                    ;BRANCH IF HSR IS OUT OF TAPE (BIT 15)
173030  010712                  MOV     PC,@R2                  ;RESET TRAP ADDRESS AT LOCATION 4
173032  012706  000024          MOV     #24,SP                  ;SPECIAL ADDRESS USED AS MASK LATER
173036  010441                  MOV     R4,-(R1)                ;DO MEM CHK: READER STATUS ADDRESS IS MOVED
173040  042701                  BIC     SP,R1                   ;SET R1=X7752, MASK IN SP=24
173042  010111                  MOV     R1,@R1                  ;STORE OWN ADDRESS IN POINTER
173044  111102  LOOP1: MOV     @R1,R2                  ;GET BYTE POINTER
173046  105214                  INC     @R4                     ;ENABLE READER
173050  105714                  TSTB    @R4                     ;TEST DONE BIT (BIT 07)
173052  100376                  BPL     .-2                     ;WAIT UNTIL READY
173054  116412  000002          MOVB    2(R4),@R2               ;THEN PICK IT UP AND STORE IT
173060  005211                  INC     @R1                     ;BUMP POINTER
173062  123227  000375          CMPB    R2,#375                 ;STORED JUMP OFFSET?
173066  001366                  BNE     LOOP                    ;NOT YET
173070  105222                  INCB    (R2)+                   ;YES, ALL DONE
173072  000142                  JMP     -(R2)                   ;GO EXECUTE AS BRANCH

                                ;DEVICE ADDRESSES FOLLOW - DO NOT CHANGE THE ORDER

173074  177560  DEV:   LSR                             ;LOW SPEED READER
173076  177550                  HSR                     ;HIGH SPEED READER
```

APPENDIX B
BM792-YB BULK STORAGE BOOTSTRAP LOADER

The BM792-YB ROM is shipped with jumper wires connected for address group 773100-773176, and its diode matrix is preprogrammed for a bulk storage (disk or DECtape) bootstrap loader program. The BM792-YB is used in a PDP-11 System that has at least 4K of read-write memory and one or more mass storage devices, such as disk or DECtape.

The actual bootstrap loader program, stored in the first 256 words of a disk or DECtape, is transferred from the device into read-write memory by the BM792-YB program. The transfer is started from location 0 of the device, and the loaded routine is assumed to be operative at read-write memory location 0. The BM792-YB program jumps to location 0 after a satisfactory completion of the transfer, so that there is automatic starting of the actual bootstrap loader program. If error conditions occur during the running of the BM792-YB program, the program starts over again.

The sequence of operations used by the bulk storage bootstrap loader is as follows:

1. It determines whether the device is a disk or DECtape from the address set in the SWITCH REGISTER.
2. If the device is a DECtape transport, it moves the tape until the front endzone is sensed.
3. It reads 256 words stored in the device, starting with address 0 of the device.
4. The loader then stores the 256 words in read-write memory sequential locations, starting with location 0.
5. The loader checks for errors and starts the program over if any errors occur.
6. The loader then jumps to read-write memory location 0 for automatic starting of the actual bootstrap loader program.

A program listing for the bulk storage bootstrap loader is provided in Table B-1. Hardware addresses in the PDP-11 use 18 bits; thus, bits A15, A16, and A17 are considered in designating the most significant octal digit of the address. The software assembler uses 16-bit addresses; consequently, only bit A15 is used to designate the most significant octal digit of the address. Therefore, the addresses in Table B-1 are listed as 173XXX instead of 773XXX.

The operating procedure for use of the BM792-YB bulk storage bootstrap loader is as follows:

Step	Procedure
1	Set the HALT/ENABLE switch to HALT, then to ENABLE.
2	Set the ROM address, 773100, into the SWITCH REGISTER.
3	Depress the LOAD ADDR switch.

(continued on next page)

Step	Procedure
4	Set the address of the word count register of the disk or DECtape to be used into the SWITCH REGISTER. The standard addresses for the word count registers of the DEC devices are as follows:

RC11 Disk	777450
RF11 Disk	777462
RK11 Disk	777406
RP11 Disk	776716
TC11 DECtape	777344

5	Depress the START switch. The disk or DECtape data should then read into the read-write memory.

Table B-1

BM792-YB Bulk Storage Bootstrap Loader Program

```
                ; REGISTER ASSIGNMENTS:
            000000 R0=%0
            000001 R1=%1
                ;
173100 013701           MOV     @#177570,R1     ;READ SWITCH REG FOR ....
       177570
173104 000005 BEGIN:    RESET                   ;FORCE CLEAR IF RETRY
173106 010100           MOV     R1,R0           ;....DEVICE WC ADDRESS
173110 012710           MOV     #-256.,@R0      ;SET TO READ 256 WORDS
       177400
173114 020027           CMP     R0,#177344      ;IS IT DECTAPE?
       177344
173120 001007           BNE     START           ;NO. GO TO START
173122 012740           MOV     #4002,-(R0)     ;YES. MOVE TAPE TO FRONT
       004002
173126 005710           TST     @R0             ;WAIT FOR ERROR!
173130 100376           BPL     .-2
173132 005740           TST     -(R0)           ;IS IT ENDZONE?
173134 100363           BPL     BEGIN           ;NO. TRY AGAIN
173136 022020           CMP     (R0)+,(R0)+     ;ADJUST POINTER
173140 012740 START:    MOV     #5,-(R0)        ;NOW START ACTUAL READ
       000005
173144 105710           TSTB    @R0             ;WAIT FOR DONE
173146 100376           BPL     .-2
173150 005710           TST     @R0             ;ERROR ENCOUNTERED?
173152 100754           BMI     BEGIN           ;IF SO START OVER
173154 105010           CLRB    @R0             ;FOR DECTAPE,STOP TRANSPORT
173156 000137           JMP     @#0             ;GO TO ROUTINE LOADED
       000000
       000001           .END


BEGIN       000004R         R0      =%000000        R1      =%000001
START       000040R         .       = 000062R
```

APPENDIX C
BM792-YC CARD READER BOOTSTRAP LOADER

The BM792-YC ROM is shipped with jumper wires connected for address group 773200-773276. Its diode matrix is preprogrammed for loading binary data into the PDP-11 memory from cards using the CR11 or CM11 Card Reader. If the data represents a PDP-11 program, the program can be automatically started upon completion of loading. The BM792-YC is used in PDP-11 Systems that have at least 4K of read-write memory and a card reader.

On the card that is read, each pair of columns (column 1 and column 2; 3 and 4; etc.) beginning with column 1 contains two 8-bit bytes which represent one 16-bit word. Also a control bit can be contained in the second column of a pair. The eight bits that represent each byte are punched or marked in rows 2 through 9 of each column.

The first column of a pair contains the high-order byte (PDP-11 bits 15-8) of the word and the second column of the pair contains the low-order byte (PDP-11 bits 7-0) of the word. A control bit punched or marked in row 0 of the second column of a pair designates that the word in those two columns is a new Loading Address. Each Loading Address must be equal to zero modulo two because loading must begin at a word boundary in memory rather than a byte boundary. Loading is accomplished one word at a time, thus a new Loading Address can appear anywhere on the card. However, a Loading Address must be in the first two columns of the first card read.

The absence of control bits in rows 12, 11, 1, and 0 of the second column of a pair designates the word as a Data Word to be loaded into the PDP-11 memory. The Data Word can represent a machine instruction or data. After each Data Word is loaded into memory the current loading address is incremented by two.

A control bit in row 1 of the second column of a pair designates the word as a Transfer Address. When a Transfer Address is read, the bootstrap program issues a RESET and branches to the Transfer Address. The card which contains the Transfer Address passes through the card reader, but no other Loading Addresses or Data Words are read from it.

A program listing for the card reader bootstrap loader is provided in Table C-1. Hardware addresses in the PDP-11 use 18 bits; thus, bits A15, A16, and A17 are considered in designating the most significant octal digit of the address. The software assembler uses 16-bit addresses; consequently, only bit A15 is used to designate the most significant octal digit of the address. Therefore, the addresses in Table C-1 are listed as 173XXX instead of 773XXX.

The operating procedure for use of the BM792-YC card reader bootstrap loader is as follows:

Step	Procedure
1	Set the HALT/ENABLE switch to HALT, then to ENABLE.
2	Load the input hopper of the card reader with the cards to be read.
3	On the card reader set the MODE switch to REMOTE.
4	On the card reader depress the RESET switch and observe that the associated green indicator lights. The card reader is now on-line.
5	Set the starting address, 773200, into the switch register.
6	Depress the LOAD ADDR switch.
7	Depress the START switch. After a short pause, the card reader should read the data on the cards into the computer memory.

Table C-1
BM792-YC Card Reader Bootstrap Loader Program

```
 1
 2                                        ;CR BOOTSTRAP
 3                                        ;
 4          173200                        .=173200
 5          000400                        BIT08=400
 6          001000                        BIT09=1000
 7          040000                        BIT14=40000
 8          000000                        R0=%0
 9          000001                        R1=%1
10          000002                        R2=%2
11          000003                        R3=%3
12          000004                        R4=%4
13          000007                        PC=%7
14          177160                        CRS=177160                          ;CR STATUS REGISTER ADDRESS
15                                        ;
16  173200  000005                        START:  RESET                       ;CLEAR ALL PRESENT DEVICES
17  173202  012700  177160                       MOV     #CRS,   R0          ;LOAD STATUS REGISTER ADDRESS
18  173206  010001                               MOV     R0,     R1          ;MOVE TO R1
19  173210  032721  001400                       BIT     #BIT08!BIT09,(R1)+  ;TEST CR READY AND GET CRB ADDRESS
20  173214  001371                               BNE     START               ;AND WAIT FOR READY, ON-LINE
21  173216  005210                        NEXTC:  INC     @R0                 ;READ A CARD
22  173220  005003                        NEXTV:  CLR     R3                  ;CLEAR DATA CONTENTS
23  173222  005004                               CLR     R4                  ;AND COLUMN FLAG
24  173224  032027  040000                TESTCD: BIT     @R0,    #BIT14      ;IS CARD DONE FLAG SET
25  173230  001372                               BNE     NEXTC               ;YES, READ A CARD
26  173232  105710                        WAITC:  TSTB    @R0                 ;IS COLUMN READY FLAG SET
27  173234  100373                               BPL     TESTCD              ;NO, WAIT FOR COLUMN AND/OR CARD DONE
28  173236  000303                               SWAB    R3                  ;REARRANGE THINGS
29  173240  151103                               BISB    @R1,    R3          ;AND GET THIS COLUMN
30  173242  005104                               COM     R4                  ;IS THIS SECOND COLUMN OF PAIR
31  173244  100772                               BMI     WAITC               ;FIRST, GET ANOTHER
32  173246  121761  000001                      CMPB    @PC,    1(R1)       ;TEST HIGH BYTE OF CRB
33  173252  001425                               BEQ     TRANSF              ;ROW 1 IS TRANSFER FLAG
34  173254  003002                               BGT     DATA                ;ROW 0,1=0 IMPLIES DATA
35  173256  010302                               MOV     R3,     R2          ;OTHERWISE ROW 0=1 IMPLIES LOAD ADD
36  173260  000757                               BR      NEXTV               ;AND START NEW PAIR
37  173262  010322                        DATA:   MOV     R3,     (R2)+       ;STORE DATA WORD
38  173264  000755                               BR      NEXTV               ;AND GET NEW COLUMN PAIR
39  173266  032027  040000                TRANSF: BIT     @R0,    #BIT14      ;WAIT FOR CARD DONE
40  173272  001775                               BEQ     TRANSF              ;IN A TIGHT LOOP
41  173274  000005                               RESET                       ;THEN CLEAR CR FLAGS
42  173276  000113                               JMP     @R3                 ;AND TRANSFER TO LOADED PROGRAM
43          000001                               .END
```

```
BIT08   000400
BIT09   001000
BIT14   040000
CRS     177160
DATA    173262
NEXTC   173216
NEXTV   173220
PC      000007R
R0      000000R
R1      000001R
R2      000002R
R3      000003R
R4      000004R
START   173200
TESTCD  173224
TRANSF  173266
WAITC   173232
```

APPENDIX D
MR11-DB BULK STORAGE BOOTSTRAP LOADER

The MR11-DB is a 64-word bootstrap loader for the following bulk storage control devices: RF11, RK11, TC11, TM11, RP11, and RC11. This option can be used in any PDP-11 system. It includes a feature of special value to PDP-11/45 systems that are equipped with MS11 Semiconductor Memory (MOS or bi-polar) Systems. On those PDP-11/45 systems, the KB11-A start vector for power up can be selected for bootstrap load from any of the above-listed devices, except the TM11, which loses vacuum on power fail.

The MR11-DB option consists of two programmed ROM diode matrix modules. The M792-YD ROM Diode Matrix stores the first 32 words of the bootstrap loader program at addresses 773100-773176. The M792-YE ROM Diode Matrix stores the second 32 words of the bootstrap loader program at addresses 773200-773276.

Table D-1 is a program listing of the MR11-DB Bootstrap Loader program that is encoded on the two ROM diode matrix modules. PDP-11 hardware addresses use 18 bits. The software assembler uses 16-bit addresses. Therefore, the addresses listed in Table D-1 are listed as 173XXX, instead of 773XXX.

KEY START LOADING

Operate the MR11-DB Bulk Storage Bootstrap Loader as follows:

1. Set the HALT/ENABL switch to HALT, then to ENABL.
2. Set the console switches to the starting address assigned to the selected bulk storage device control, as listed in Table D-2.
3. Press LOAD ADRS.
4. Press START.

The processor will start executing the bulk storage bootstrap loader program at the selected address. The program loads the first 512 words or bytes from unit 0 into memory, starting at memory location 0. After the bootstrap is loaded from the bulk storage device, the loader program causes the processor to start executing the bootstrap at location 0.

NOTE

When magnetic tape is the bulk storage medium, magnetic drive unit 0 must be selected and positioned at the load point.

Loading from Disks – The program starts at the selected address, then branches to a common routine that resets all Unibus devices. Thus, disk address registers and current memory address registers are initialized to 0. The pointer to the device's word count register is located in R1. Then, the word count register is loaded with the 2s

complement of 512. The device command to read and go is issued to the device command register. As the 512-word record is read into memory from the disk, the loader program checks for errors. If an error is detected, the entire routine is repeated, starting at the selected address. When no errors are detected and the last word has been transferred, the PC is cleared, and the bootstrap is executed, starting at memory location 0.

Loading from Tapes – The program starts at the selected address for DECtape or magtape; then branches to a common tape routine which first resets all the device registers. Then, the device's word count register (or byte count) is decremented by one. If the routine is entered from the TC11 address, a first command is issued to rewind the DECtape to the forward end zone. If the routine is entered from the TM11 address, a first command is issued to advance the magnetic tape one record. After the specified operation is done and checked for errors, the program branches to the common disk loading routine that reads a 512-word or byte record into memory from the selected tape storage device.

POWER UP LOADING

The MR11-DB provides for automatically loading a bootstrap program from a pre-selected bulk storage device during the power up sequence. This feature is provided for PDP-11/45 systems with MOS or bipolar memory and no power backup. The KB11-A Central Processor Unit in those systems has a start vector jumper field located on DAP module M8100. Table D-3 lists the start vector jumper connections required to select the specific MR11-DB starting address for each type of bulk storage device.

START VECTOR PROGRAM OPERATION

The start vector jumpers on the DAP module select bits SV(07:00) of the start vector. Bits SV(01:00) are always 0. High-order bits of the starting address are generated by CPU sign-extension logic, blocking bits 11 and 8. A hard-wired address 773XXX with the SV(07:00) offset is generated. The power up sequence uses the resultant address to load the PC and PS from the address pointed to by the start vector.

For example, jumper selection of the RK11 provides start vector 260. The resultant address, 173260, accesses a location provided by the MR11-DB, to load the PC with starting address 173110 and the PS with 000340. The bulk storage program loader proceeds to load a bootstrap from the RK11, with the CPU operating at priority level 7, which prevents external devices from interrupting the program.

INSTALLATION

PDP-11/45 Systems – Install the M792-YD and M792-YE modules that comprise the MR11-DB option in two of the three spaces reserved on the CPU backplane for small peripheral controllers. The quad-height slots are designated 26, 27, and 28. Refer to Table D-3 and remove jumpers W1 through W6, as required, from the DAP module to select the bulk storage device that is to provide the bootstrap program during power up.

NOTE

The TM11 must be restarted manually, with the tape drive positioned at the load point. Therefore, power up start vector selection is not provided.

Other PDP-11 Systems – Install the MR11-DB modules on a DD11-A Peripheral Mounting Panel that is connected to the Unibus by an M920 Unibus Connector module.

Table D-1

MR11-DB Bulk Storage Program Loader Listing

```
1/3100  010732          RF11:   MOV     %7,%2           ;FIXED HEAD DISK (256KW)
1/3102  000451                  BR      OTHER
1/3104  177462                  177462
1/3106  000005                  5

1/3110  010732          RK11:   MOV     %7,%2           ;MOVING HEAD DISK (CARTRIDGE)
1/3112  000445                  BR      OTHER
1/3114  177406                  177406
1/3116  000005                  5                       ;COMMAND WORD

1/3120  010732          TC11:   MOV     %7,%2
1/3122  000417                  BR      TAPES
1/3124  177344                  177344                  ;ADRS OF WORD COUNT
1/3126  000005                  5                       ;LAST COMMAND
1/3130  004003                  4003                    ;FIRST COMMAND
1/3132  100000                  100000                  ;DONE MASK
1/3134  024000                  24000                   ;ERROR MASK

1/3136  010732          TM11:   MOV     %7,%2
1/3140  000410                  BR      TAPES
1/3142  172524                  172524                  ;ADRS OF BYTE COUNT
1/3144  060003                  60003                   ;LAST COMMAND
1/3146  060011                  60011                   ;FIRST COMMAND
1/3150  000200                  200                     ;DONE MASK
1/3152  100000                  100000                  ;ERROR MASK

1/3154  010732          RP11:   MOV     %7,%2           ;MOVING HEAD DISK (PACK)
1/3156  000423                  BR      OTHER
1/3160  176716                  176716
                                                        ;COMMAND WORD (5) IS THE RESET
1/3162  000005          TAPES:  RESET
1/3164  010200                  MOV     %2,%0           ;GET THE ADDRESS OF THE BRANCH
1/3166  005720                  TST     (0)+            ;%0 TO POINT AT LAST COMMAND
1/3170  012001                  MOV     (0)+,%1         ;GET THE WORD COUNT ADDRESS
1/3172  005311                  DEC     (1)             ;SET UP FOR ADVANCE 1 RECORD
1/3174  005720                  TST     (0)+            ;MOVE %0 TO FIRST COMMAND
1/3176  012041                  MOV     (0)+,-(1)       ;COMMAND WORD TO COMMAND REG.
1/3200  031011                  BIT     (0),(1)         ;LOOK FOR DONE INDICATORS
1/3202  001776                  BEQ     .-2             ;NONE SET, TRY AGAIN
1/3204  005720                  TST     (0)+            ;DONE FIRST COMMAND, CHECK FOR ERROR
1/3206  031041                  BIT     (0),-(1)        ;LOOK FOR SET ERROR BITS
1/3210  001406                  BEQ     OTHER           ;NO ERRORS - TRY THE READ
1/3212  000112          AGAIN:  JMP     (2)             ;RERUN FOR ERRORS

1/3214  173100          RFVEC:  RF11                    ;RF11 POWER UP VECTOR
1/3216  000340                  340

1/3220  010702          RC11:   MOV     %7,%2           ;FIXED HEAD DISK (64KW)
1/3222  000401                  BR      OTHER
1/3224  177450                  177450                  ;ADRS OF WORD COUNT (COMMAND+2)
                                                        ;COMMAND WORD (5) IS THE RESET
1/3226  000005          OTHER:  RESET
1/3230  010200                  MOV     %2,%0           ;%0 TO POINT AT WORD COUNT ADRS
1/3232  005720                  TST     (0)+            ;POINT TO ADDRESS
1/3234  012001                  MOV     (0)+,%1         ;WORD COUNT ADRS TO %1
1/3236  012711  177000          MOV     #-1000,(1)      ;LOAD WORD COUNT
1/3242  011041                  MOV     (0),-(1)        ;COMMAND TO COMMAND REGISTER
1/3244  032711  100200          BIT     #100200,(1)     ;CHECK FOR ERROR OR DONE
1/3250  001775                  BEQ     .-4             ;IF NEITHER, KEEP LOOKING
1/3252  100757                  BMI     AGAIN           ;ERROR, TRY AGAIN
1/3254  005007                  CLR     %7

1/3256  000000                  0                       ;FILLER
1/3260  173110          RKVEC:  RK11                    ;RK11 POWER UP VECTOR
1/3262  000340                  340
1/3264  173220          RCVEC:  RC11                    ;RC11 POWER UP VECTOR
1/3266  000340                  340
1/3270  173154          RPVEC:  RP11                    ;RP11 POWER UP VECTOR
1/3272  000340                  340
1/3274  173120          TCVEC:  TC11                    ;TC11 POWER UP VECTOR
1/3276  000340                  340

        000001          .END
```

Table D-2
Starting Address

Bulk Storage Device Control	Starting Address (octal)
RF11 (for RS11 DECdisk)	773100
RK11 (for RK02 DECpack)	773110
TC11 (for TU56 DECtape)	773120
TM11 (for TU10 Magtape)	773136
RP11 (for RP02 Disk Pack)	773154
RC11 (for RS64 DECdisk)	773220

Table D-3
Power Up Start Vector Jumper Connections

Bulk Storage Control Device	Power Up Vector Address	Jumpers on DAP Module					
		W1	W2	W3	W4	W5	W6
RF11	773214	In	In	Out	Out	Out	In
RK11	773260	Out	Out	In	In	Out	In
TC11	773274	In	In	In	In	Out	In
TM11	None	–	–	–	–	–	–
RP11	773270	Out	In	In	In	Out	In
RC11	773220	Out	Out	In	Out	Out	In

MAINTENANCE

Diagnostic program MAINDEC-11-DZMRA-D is provided with the MR11-DB Bulk Storage Bootstrap Loader option. The diagnostic program can be used to troubleshoot and maintain the MR11-DB hardware. The available tests are:

PRG0: Logic Tests
PRG1: ROM data dump
PRG2: Single ROM address read data loop

These tests can also be used to check data reliability and as a post-installation checkout procedure. Complete operating procedure is described in the MAINDEC description supplied as part of the diagnostic program package.

Module schematics, parts lists, and component location drawings for the M792-YD and M792-YE ROM Diode Matrix modules are located in the MR11-DB engineering drawing set. Module Schematics of the two modules are also provided in Chapter 4 of this manual.

APPENDIX E
BM792-YF BULK STORAGE BOOTSTRAP LOADER

The BM792-YF ROM is shipped with jumper wires connected for address group 773200-773276, and its diode matrix is preprogrammed for a bulk storage (disk or DECtape) bootstrap loader program. The BM792-YF can only be used on a PDP-11 System that has at least 4K of read-write memory and one or more mass storage devices, such as a disk or DECtape.

The actual bootstrap loader program, stored in the first 256 words of a disk or DECtape, is transferred from the device into read-write memory by the BM792-YF program. The transfer is started from location 0 of the device, and the loaded routine is assumed to be operative at read-write memory location 0. The BM792-YF program jumps to location 0 after a satisfactory completion of the transfer, so that there is automatic starting of the actual bootstrap loader program. If error conditions occur during the running of the BM792-YF program, the program starts over again.

The sequence of operations used by the bulk storage bootstrap loader is as follows:

1. It determines whether the device is a disk or DECtape from the address set in the Switch register.
2. If the device is a DECtape transport, it moves the tape until the front endzone is sensed.
3. It reads 256 words stored in the device, starting with address 0 of the device.
4. The loader then stores the 256 words in read-write memory sequential locations, starting with location 0.
5. The loader checks for errors and starts the program over if any errors occur.
6. The loader then jumps to read-write memory location 0 for automatic starting of the actual bootstrap loader program.

A program listing for the bulk storage bootstrap loader is provided in Table E-1. Hardware addresses in the PDP-11 use 18 bits; thus, bits A15, A16, and A17 are considered in designating the most significant octal digit of the address. The software assembler uses 16-bit addresses; consequently, only bit A15 is used to designate the most significant octal digit of the address. Therefore, the addresses in Table E-1 are listed as 173XXX instead of 773XXX.

The operating procedure for use of the BM792-YF bulk storage bootstrap loader is as follows:

Step	Procedure
1	Set the HALT/ENABLE switch to HALT, then to ENABLE.
2	Set the ROM address, 7732XX, into the Switch register.

XX	Equipment
00	RK11 Disk
06	RF11 Disk
14	TC11 DECtape

(continued on next page)

Step	Procedure
3	Depress the LOAD ADDR switch.
4	Depress the START switch. The disk or DECtape data should then read into the read-write memory.

Table E-1
BM792-YF Bulk Storage Bootstrap Loader Program

```
                        ;REGISTERS USED
        000000          R0=%0
        000001          R1=%1

173200  012701  177406  RKBOOT: MOV     #177406,R1      ;SET UP RK11 ADDRESS
173204  000405          BR      BEGIN
173206  012701  177462  RFBOOT: MOV     #177462,R1      ;SET UP RF11 ADDRESS
173212  000402          BR      BEGIN
173214  012701  177344  DTBOOT: MOV     #177344,R1      ;SET UP DECTAPE ADDRESS

173220  000005          BEGIN:  RESET
173222  010100          MOV     R1,R0           ;SET WORD COUNT
173224  012710  177400  MOV     #-256.,@R0      ;TO READ 256 WORDS
173230  020027  177344  CMP     R0,#177344      ;IS THIS DECTAPE BOOT?
173234  001007          BNE     START           ;IF NOT, SKIP SEARCH CODE
173236  012740  004002  MOV     #4002,-(R0)     ;SEARCH BACKWARD
173242  005710          TST     @R0             ;LOOP UNTIL
173244  100376          BPL     .-2             ;ERROR FLAG
173246  005740          TST     -(R0)           ;IF NOT 'END ZONE',
173250  100363          BPL     BEGIN           ;TRY AGAIN
173252  022020          CMP     (R0)+,(R0)+     ;RESET R0

173254  012740  000005  START:  MOV     #5,-(R0)        ;ISSUE READ COMMAND
173260  105710          TSTB    @R0             ;LOOP UNTIL
173262  100376          BPL     .-2             ;READY
173264  005710          TST     @R0             ;IF ERROR,
173266  100754          BMI     BEGIN           ;TRY AGAIN
173270  000005          RESET                   ;STOP ANY TAPE MOTION
173272  000137  000000  JMP     @#0             ;GO TO THE BOOT
```

APPENDIX F
BM792-YH CASSETTE BOOTSTRAP LOADER

The BM792-YH ROM is shipped with jumper wires connected for address group 773300-773376, and its diode matrix is preprogrammed for a tape cassette (TA11/TU60 Cassette System) bootstrap loader program. This quad-sized module is one of the Small Peripheral Controllers (SPC) and can be mounted in any SPC slot in a DD11-A, DD11-B, or most PDP-11 family processors. Any PDP-11 System that has 4K of read-write memory and a cassette can use the BM792-YH.

The actual bootstrap loader program, stored in the first 128 bytes of a cassette tape, is transferred from the cassette into read-write memory by the BM792-YH program. The bytes are consecutively read from the cassette and loaded into memory locations 0 through 177 (octal). When the loading is complete, program control is transferred to location 0 so that the loaded program can be executed. At the point when the program control is transferred, the cassette is positioned at the end of the second block of the first file so that the loaded program can continue to read in additional data.

The sequence of operations used by the cassette bootstrap loader is as follows:

1. The cassette is rewound and then spaced forward one block. This action skips the header block (normally 32 bytes) associated with the first file and positions the tape at the second block of the first file.
2. The BM792-YH program consecutively reads 128 bytes from the cassette tape into read-write memory locations 0 through 177 (octal).
3. The first byte read is compared to octal 240 (NOP) and if it does not equal octal 240, the program comes to a halt at location 173350. To restart the program from this halt, the CONT switch is depressed.
4. After the 128 bytes are read, the loader program checks the TA11 error bit (block check error, off-line error, etc.) and if an error is detected, the program comes to a halt at location 173350 and can be restarted by depressing the CONT switch.
5. If no error is detected, program control is transferred to location 0 to execute the loaded program.

A program listing for the cassette bootstrap loader is provided in Table F-1. Hardware addresses in the PDP-11 use 18 bits; thus, bits A15, A16, and A17 are considered in designating the most significant octal digit of the address. The software assembler uses 16-bit addresses; consequently, only bit A15 is used to designate the most significant octal digit of the address. Therefore, the addresses in Table F-1 are listed as 173XXX instead of 773XXX.

The BM792-YH program has no provisions for initializing the system since it does not issue a RESET instruction. Initialization is necessary because other devices may issue interrupts or an internal processor option may be enabled. When the BM792-YH program is started from the console, initialization is performed because the START

Table F-1

BM792-YH Cassette Bootstrap Loader Program

```
                                        .ABS
        173300                          .=173300
        000000                  R0=%0
        000001                  R1=%1
        000002                  R2=%2
        000003                  R3=%3
        000007                  PC=%7

173300  012700  177500          CBOOT:  MOV #177500,R0   ;R0 HOLDS ADDRESS OF TA11
173304  005010                          CLR (R0)         ;SELECT UNIT ZERO
173306  010701                  RESTRT: MOV PC,R1        ;USE FOR PIC
173310  062701  000052                  ADD #TABLE-.,R1  ;R1 HOLDS ADDRESS OF COMMAND TABLE
173314  012702  000375                  MOV #375,R2      ;MEMORY POINTER AND DATA FLAG
173320  112103                          MOVB (R1)+,R3    ;MOVE TEST BITS TO R3

173322  112110                  LOOP1:  MOVB (R1)+,(R0)  ;MOVE COMMAND FROM TABLE TO TA11
173324  100413                          BMI DONE         ;IF COMMAND IS NEGATIVE, THEN QUIT
173326  130310                  LOOP2:  BITB R3,(R0)     ;TEST READY AND TRANSFER REQUEST BITS IN TACS
173330  001776                          BEQ LOOP2        ;BRANCH IF BITS ARE NOT SET
173332  105202                          INCB R2          ;ADVANCE MEMORY POINTER
173334  100772                          BMI LOOP1        ;IF MINUS, TRY ANOTHER TABLE COMMAND
173336  116012  000002                  MOVB 2(R0),(R2)  ;READ DATA INTO MEMORY
173342  120337  000000                  CMPB R3,@#0      ;FIRST BYTE READ SHOULD BE '240'
173346  001767                          BEQ LOOP2        ;IF EQUAL, GO READ ANOTHER BYTE

173350  000000                  STOP:   HALT             ;HALT ON ERROR
173352  000755                          BR RESTRT        ;RESTART ON CONTINUE

173354  005710                  DONE:   TST (R0)         ;CHECK FOR ERROR
173356  100774                          BMI STOP         ;BRANCH TO HALT ON ERROR
173360  005007                          CLR PC           ;JUMP TO 0

173362                          TABLE:                   ;HIGH BYTE                LOW BYTE
173362  017640                  .WORD   037*400 + 240    ;ILBS+REWIND+GO           READY+TRANSFER REQUEST
173364  002415                  .WORD   005*400 + 015    ;READ+GO                  SPACE FORWARD BLOCK+GO
173366  112024                  .WORD   224*400 + 024    ;READ+ILBS+END TABLE      READ+ILBS
173370  000000  000000          .WORD   0,0              ;TWO WORDS OF FILLER

173374  173300                  VECTOR: CBOOT            ;POWER-UP VECTOR (PC)
173376  000340                          000340           ;POWER-UP STATUS (PS)
```

switch initializes the system prior to starting. However, if the BM792-YH program is started by a program transferring control to location 173300, then that program must issue a RESET instruction prior to the JMP 173300.

Normally, the PDP-11 processor's power-up vector is address 24/26; however, processors such as the PDP-11/40 and PDP-11/45 have jumper selectable power-up vectors that allow the vector address to be set to an address within a restricted range in the highest 4K-words of Unibus address. The power-down vector remains at 24/26.

The BM792-YH provides a power-up vector at address 173374/6. When the power-up trap sequence executes with a vector address set to 173374/6, program execution begins at 173300 with a priority level of 7.

The operating procedure for use of the BM792-YH cassette bootstrap loader when the cassette is operating from cassette unit number 0 at the standard octal address of 777500 is as follows:

Step	Procedure
1	Write-lock the cassette for security.
2	Mount the cassette in cassette unit number 0 (left-hand drive unit on the TU60).
3	Set the HALT/ENABLE switch to HALT, then to ENABLE.
4	Set the ROM address, 773300, into the Switch register.
5	Depress the LOAD ADDR switch.
6	Depress the START switch. The cassette data should then read into the read-write memory.

The operating procedure to bootstrap load from cassette unit number 1 or from a cassette unit other than one at the standard octal address of 777500 is as follows:

Step	Procedure
1	Write-lock the cassette for security.
2	Mount the cassette in the selected unit.
3	Set the HALT/ENABLE switch to HALT, then to ENABLE.
4	Set the R0 address, 777700, into the Switch register.
5	Depress the LOAD ADDR switch.
6	Set the address of the cassette unit into the Switch register.
7	Depress the DEP switch. This loads R0 with the address of the cassette unit.
8	With the Switch register still set at the address of the cassette unit, depress LOAD ADDR switch.
9	Set the octal designation for the cassette unit number into Switch register (000 for unit number 0 or 400 for unit number 1).
10	Depress the DEP switch. This establishes bit 08, the Unit Select bit, of the TA11 Command and Status register.
11	Set the R7 address, 777707 into the Switch register.
12	Depress the LOAD ADDR switch.

(continued on next page)

Step	Procedure
13	Set 773306 into the Switch register.
14	Depress the DEP switch. This sets the PC to the BM792-YH restart address.
15	Depress the CONT switch. This starts the processor without system initialization. When started at address 773306, the BM792-YH program uses R0 to reference the cassette registers but does not modify R0 or the Unit Select bit. When the 128-byte program is loaded from the cassette into the read-write memory, this 128-byte program determines whether read-in will continue from this same cassette. R0 and the Unit Select bit can be modified by the loaded program so that a different cassette can be accessed for loading.