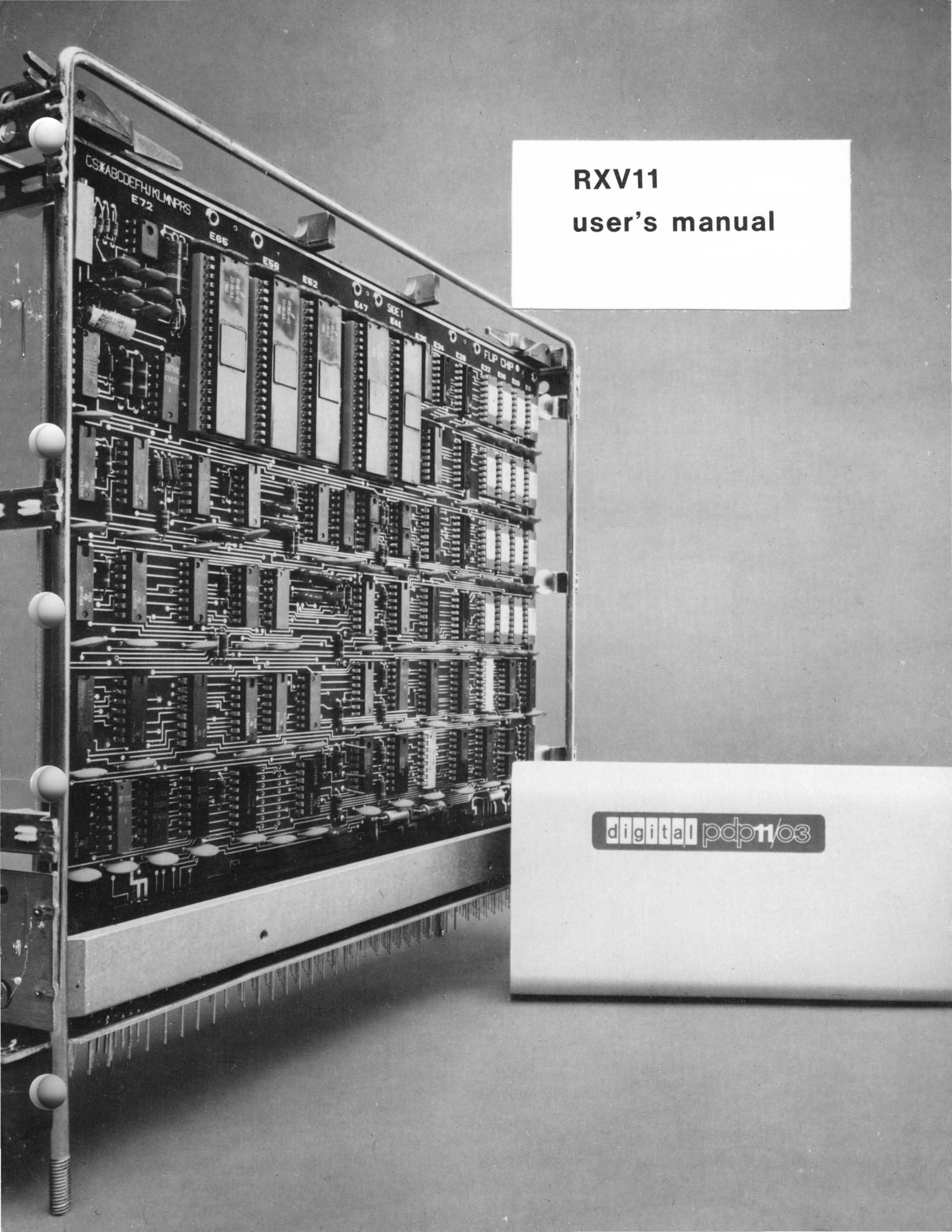

RXV11
user's manual

EK-RXV11-OP-002

RXV11
user's manual

digital equipment corporation • maynard, massachusetts

1st Edition, December 1975
2nd Edition, May 1976
3rd Printing (Rev), December 1976

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

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ILLUSTRATIONS

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

This manual contains installation, operation, and programming instructions for the RXV11 Floppy Disk System. Chapter 2 (Installation) contains unpacking, installation and operation information. Chapter 2 also provides information on the proper care of the floppy disk media and should be read carefully.

The RXV11 Floppy Disk System consists of an RX01 floppy disk drive, interconnecting cable, and an RXV11 interface for an LSI-11 or PDP-11/03 system.

The RX01 is a low cost, random access, mass memory device that stores data in fixed length blocks on a preformatted, IBM-compatible, flexible diskette. Each drive can store and retrieve up to 256K 8-bit bytes of data. The RX01 consists of one or two flexible disk drives, a single read/write electronics module, a microprogrammed controller module, and a power supply, contained in a rack-mountable enclosure. A cable is included for connection to the RXV11 interface module.

The RX01 performs implied seeks. Given an absolute sector address, the RX01 locates the desired sector and performs the indicated function, including automatic head position verification and hardware calculation and verification of the Cyclic Redundancy Check (CRC) character. The CRC character that is read and generated is compatible with IBM 3740 equipment.

The RX01 connects to the M7946 RXV11 interface module, which converts the RX01 I/O bus to the LSI-11 I/O bus structure. It controls interrupts to the processor initiated by the RX01, decodes device addresses for register selection, and handles data interchange between the RX01 and the processor. The RXV11 interface module receives dc operating power from the backplane in which it is installed.

1.2 REFERENCES

This manual should be used in conjunction with one or more of the following manuals:

LSI-11, PDP-11/03 Processor Handbook
LSI-11, PDP-11/03 User's Manual
LSI-11, PDP-11/03 Configuration and Installation Guide
RX01/RX8/RX11 Floppy Disk System Maintenance Manual

1.3 PHYSICAL DESCRIPTION

Each RXV11 Floppy Disk System consists of the following components:

RX01 Floppy Disk Drive
M7946 RXV11 Interface Module
BC05L-15 Interface Cable

System components are shown in Figure 1-1.

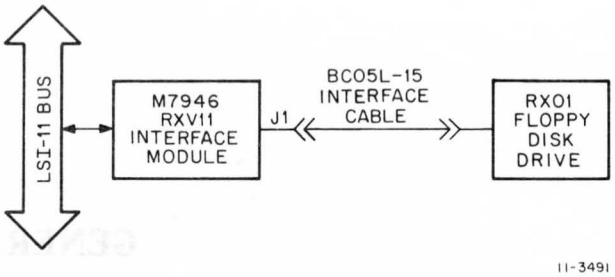


Figure 1-1 RXV11 Floppy Disk System Components

All RX01 subsystem components are housed in a 10-1/2 in. rack-mountable box. The box includes a power supply for all RX01 circuits and an appropriate ac power cable and plug. Interface between the RX01 floppy disk drive and the RXV11 interface module is provided by the standard length (15 ft) 40-conductor BC05L-15 interface cable. Figure 1-2 is a front view of an RX01 dual floppy disk drive.

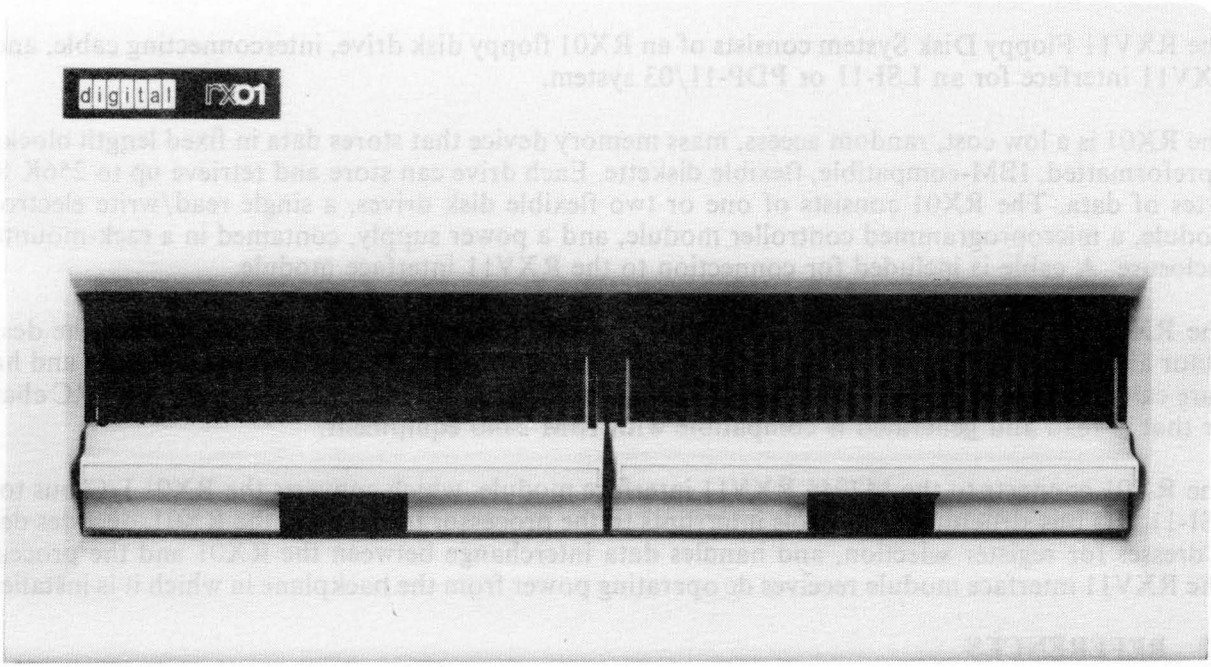


Figure 1-2 Floppy Disk Drive (Front View)

A detailed description of the RX01 floppy disk drive is contained in the *RX01/RX8/RX11 Floppy Disk System Maintenance Manual.*

The RXV11 interface circuits are contained on the M7946 module. This module measures 8-1/2 in. × 5 in. and requires one device location on the LSI-11 I/O bus.

1.4 FLOPPY DISK TECHNOLOGY

1.4.1 The Media

The media used for floppy disk data storage and retrieval is an industry-compatible "diskette" (floppy disk) shown in Figure 1-3.

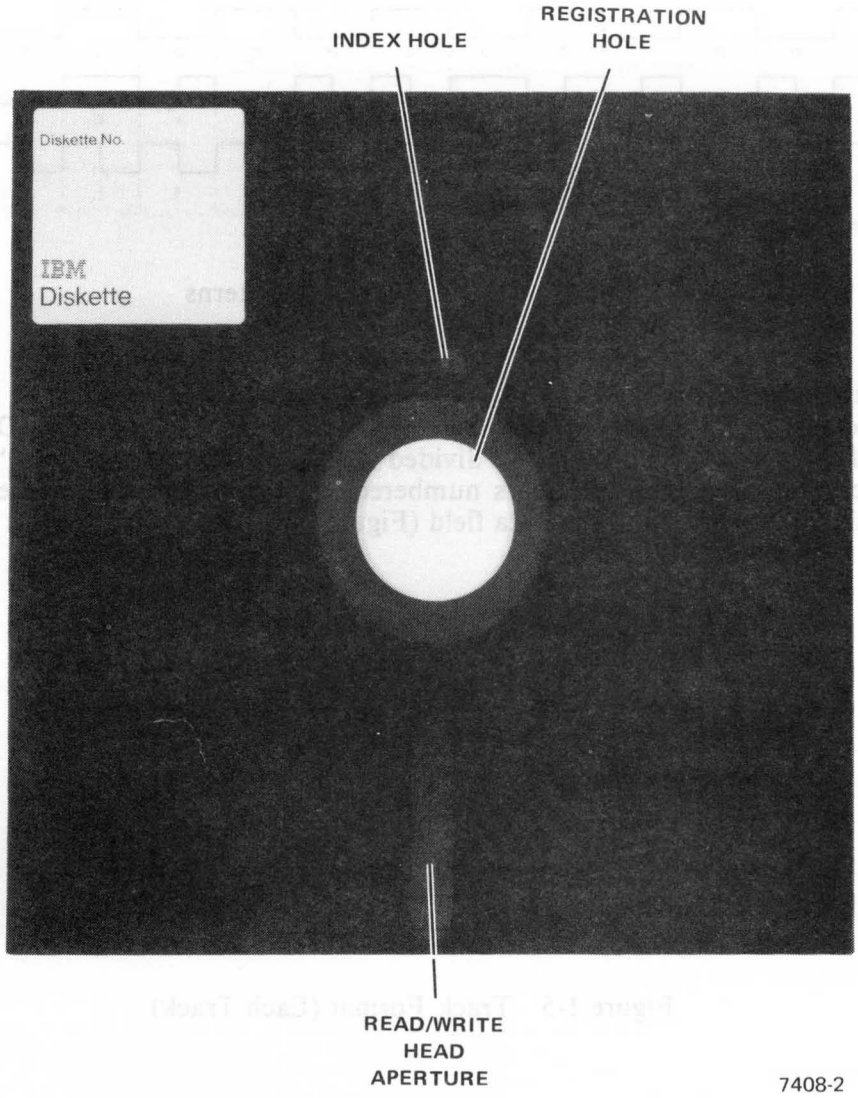


Figure 1-3 Diskette Media

The diskette media was designed by applying magnetic tape technology to magnetic disk architecture. This resulted in a flexible oxide-on-mylar surface encased in a plastic envelope with a hole for the read/write head, a hole for the drive spindle hub, and a hole for the "hard" (physical) index mark. The envelope is lined with a fiber material that cleans the diskette surface. The diskette is supplied to the customer preformatted (in IBM format) and pretested.

1.4.2 Recording Scheme

The recording scheme used is "double frequency." In this method, data is recorded between bits of a constant clock stream. The clock stream consists of a continuous pattern of one flux reversal every four μs (Figure 1-4). A data "one" is indicated by an additional reversal between clocks (i.e., doubling the bit stream frequency; hence the name). A data "zero" is indicated by no flux reversal between clocks.

A continuous stream of ones, shown in the bottom waveform in the figure, would appear as a "2F" bit stream, and a continuous stream of zeros, shown in the top waveform, would appear as a "1F" or fundamental frequency bit stream.

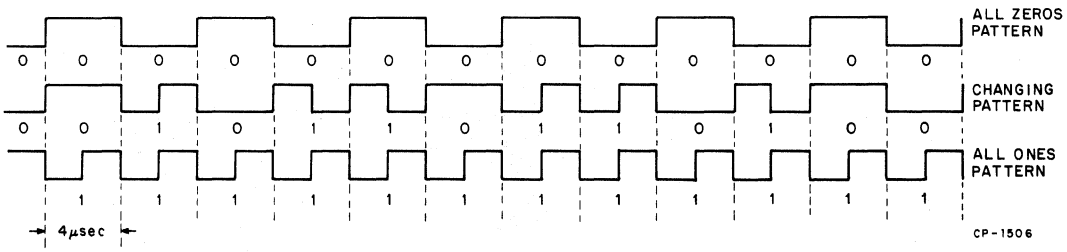


Figure 1-4 Flux Reversal Patterns

1.4.3 Recording Format

The recording format of the RXV11 Floppy Disk System is industry-compatible. Data is recorded on only one side of the diskette. This surface is divided into 77 concentric circles or "tracks" numbered 0–76. Each track is divided into 26 sectors numbered 1–26 (Figure 1-5). Each sector contains two major fields: the header field and the data field (Figure 1-6).

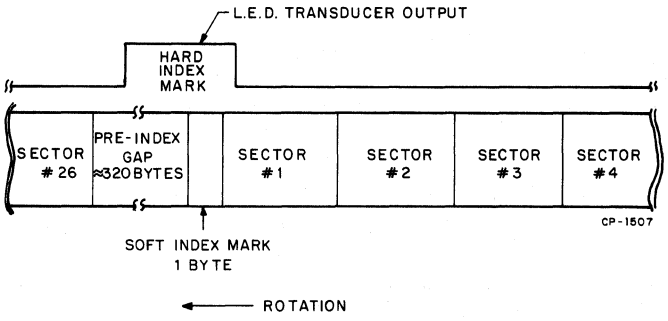


Figure 1-5 Track Format (Each Track)

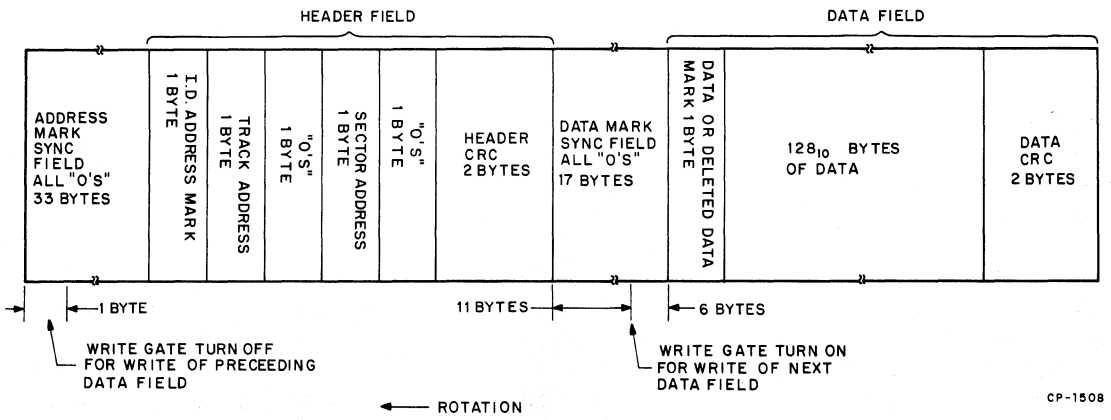


Figure 1-6 Sector Format (Each Sector)

1.4.3.1 Header Description – The header field is broken into seven bytes (eight bits/byte) of information and is preceded by a field of zeros for synchronization.

1. Byte No. 1: ID Address Mark – This is a unique stream of flux reversals (not a string of data bits) that is decoded by the controller to identify the beginning of the header field.

2. Byte No. 2: Track Address – This is the absolute ($0–114_8$) binary track address. Each sector contains track address information to identify its location on 1 of the 77 tracks.

3. Byte No. 3 – Zeros (one byte)

4. Byte No. 4: Sector Address – This is the absolute binary sector address ($1–32_8$). Each sector contains sector address information to identify its circumferential position on a track.

5. Byte Nos. 6 and 7: CRC – This is the Cyclic Redundancy Check character that is calculated for each sector from the first five header bytes using a polynomial division algorithm designed to detect the types of failures most likely to occur with "double frequency" recorded data and the floppy media.

1.4.3.2 Data Field Description – The data field is broken into 131 bytes of information and is preceded by a field of zeros for synchronization and the header field (Figure 1-6).

1. Byte No. 1: Data or Deleted Data Address Mark – This is a unique string of flux reversals (not a string of data bits) that is decoded by the controller to identify the beginning of the data field. The deleted data mark is not used during normal operation, but the RX01 can identify and write deleted data marks under program control, as required. The deleted data mark is only included in the RXV11 system to be IBM-compatible. One or the other data address marks precedes each data field.

2. Byte Nos. 2–129 – These bytes comprise the data field used to store 128 8-bit bytes of information.

NOTE
Partial data fields are not recorded.

3. Byte Nos. 130 and 131 – These bytes comprise the CRC character that is calculated for each sector from the first 129 data field bytes, using the industry-standard polynomial division algorithm designed to detect the types of failures most likely to occur in double-frequency recording on the floppy media.

1.4.3.3 Track Usage – The RX01 is capable of recording any system structure through the use of special systems programs, but normal operation will make use of all the available tracks as data tracks. Any special file structures must be accomplished through user software.

1.4.3.4 CRC Capability – Each sector has a two-byte header CRC character and a two-byte data CRC character to ensure data integrity. The CRC characters are generated by the hardware during a write operation and checked to ensure that all bits were read correctly during a read operation. The CRC character is the same as that used in the IBM 3740 series of equipment. A complete description of CRC generation and checking is presented in the *RX01/RX8/RX11 Floppy Disk System Maintenance Manual.*

1.5 CONFIGURATION

Option number designations are as follows:

RXV11-AA Single Drive System, 115 V/60 Hz
RXV11-AC Single Drive System, 115 V/50 Hz
RXV11-AD Single Drive System, 230 V/50 Hz
RXV11-BA Dual Drive System, 115 V/60 Hz
RXV11-BC Dual Drive System, 115 V/50 Hz
RXV11-BD Dual Drive System, 230 V/50 Hz

NOTE

50 Hz versions are available in voltages of 105, 115, 220, and 240 Vac by field-pluggable conversion. Refer to the RX01/RX8/RX11 Floppy Disk System Maintenance Manual for complete input power modification details.

1.6 OPTIONS

Additional diskettes can be ordered using the following option numbers:

RX01K-5 – Five formatted blank diskettes
RX01K-10 – Ten formatted blank diskettes

1.7 SPECIFICATIONS

System Reliability

Minimum number of revolutions per track	1 million/media (head-loaded)
Seek error rate	1 in 10^6 seeks
Soft read error rate	1 in 10^9 bits read
Hard read error rate	1 in 10^{12} bits read

NOTE

The above error rates only apply to media that is properly cared for. Seek error and soft read errors are usually attributable to random effects in the head/media interface, such as electrical noise, dirt, or dust. Both are called "soft" errors if the error is recoverable in ten additional tries or less. "Hard" errors cannot be recovered. Seek error retries should be preceded by an Initialize.

Drive Performance

Capacity (8-bit bytes)	
Per diskette	256,256 bytes
Per track	3,328 bytes
Per sector	128 bytes

Data transfer rate	
Diskette to controller buffer	4 μs/data bit (250K bps)
Buffer to RXV11 interface	2 μs/bit (500K bps)
RXV11 interface to LSI-11 I/O bus	18 μs/8-bit byte (<50K bytes/sec)
Track-to-track-move	10 ms/track maximum
Head settle time	20 ms maximum
Rotational speed	360 rpm ÷ 2.5%; 166 ms/rev nominal
Recording surfaces per disk	1
Tracks per disk	77 (0–76) or ($0–114_8$)
Sectors per track	26 (1–26) or ($0–32_8$)
Recording technique	Double frequency
Bit density	3200 bpi at inner track
Track density	48 tracks/in.
Average access	488 ms, computed as follows:

Seek		Settle		Rotate		Total
(77 tks/2)	×	10 ms	+	20 ms	+	(166 ms/2) = 488 ms

Environmental Characteristics

Temperature	
RX01, operating	15° to 32° C (59° to 90° F) ambient; maximum temperature gradient = 20° F/hr (-6.7° C/hr)
RX01, nonoperating	-35° to +60° C (-30° to +140° F)
Media, nonoperating	-35° to +52° C (-30° to +125° F)

NOTE

Media temperature must be within operating temperature range before use.

Relative humidity	
RX01, operating	25° C (77° F) maximum wet bulb 2° C (36° F) minimum dew point 20% to 80% relative humidity
RX01, nonoperating	5% to 98% relative humidity (no condensation)
Media, nonoperating	10% to 80% relative humidity
Magnetic field	Media exposed to a magnetic field strength of 50 oersteds or greater may lose data.

Electrical

Power consumption	
RX01	3 A at 24 V (dual), 75 W; 5 A at 5 V, 25 W
RXV11 interface (M7946)	Not more than 1.5 A at 5 Vdc
Power input (ac)	4 A at 115 Vac 2 A at 230 Vac

CHAPTER 2
INSTALLATION AND OPERATION

2.1 GENERAL

This chapter provides information on installing and operating the RXV11 Floppy Disk System. This information includes:

Site Preparation – The planning required to make the installation site suitable for operation of the floppy disk system, including space, cabling, power requirements, and fire and safety precautions.

Environmental Considerations – The specific environmental characteristics of the floppy disk system, including temperature, relative humidity, air conditioning and/or heat dissipation, and cleanliness.

Installation – The actual step-by-step process of installing the floppy disk system from unpacking through the preliminary installation checks, power conversion techniques, and acceptance testing.

Operation – The recommended practices for using the floppy disk system, handling the media, and shipping and storing the diskettes.

2.2 SITE PREPARATION

2.2.1 Space

The RX01 is a cabinet-mountable unit that may be installed in a standard Digital Equipment Corporation cabinet. This rack-mountable version is approximately 10-1/2 in. (28 cm) high, 19 in. (48 cm) wide, and 16-1/2 in. (42 cm) deep (Figure 2-1).

Provision should be made for service clearances of approximately 22 in. (56 cm) at the front and rear of the cabinet.

2.2.2 Cabling

The standard BC05L-15 interface cable provided with the RXV11 is 15 ft (4.6 m) in length, therefore, the positioning of the RX01 in relation to the backplane in which the RXV11 interface is to be installed should be considered. The RX01 should be placed near the console terminal so that the operator will have easy access to load or unload disks. The ac power cord is approximately 9 ft (2.7 m) long.

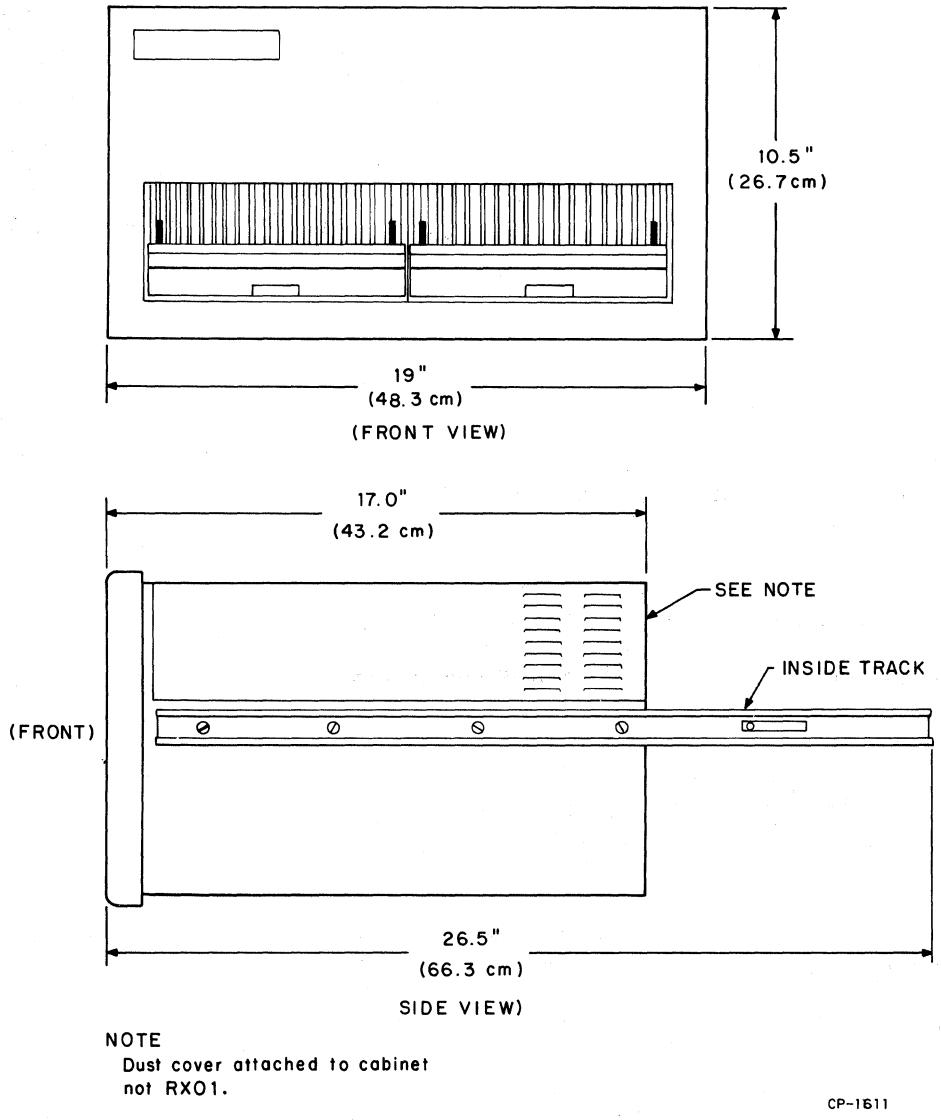


Figure 2-1 RX01 Overall Dimensions

2.2.3 AC Power

The RXV11 Floppy Disk System is available in three ac voltage/model configurations:

Models	Voltage/Frequency
RXV11-AA, -BA	100 – 132 Vac, 60 Hz
RXV11-AC, -BC	100 – 132 Vac, 50 Hz
RXV11-AD, -BD	180 – 264 Vac, 0 Hz, in one of two voltage ranges. The actual voltage range is user-selected by installing the appropriate power harness during system installation, as follows:

Voltage Range	Power Harness Part Number
180–240	70-10696-04
200–264	70-10696-03

When installing the 180–264 Vac models, the user must select and install the proper power harness for the power line voltage available, as listed above. The harness part number is stamped on jumper connector P1. Install the selected power harness after unpacking the RX01, but *before* installing it in a cabinet. Proper power harness installation is shown in Figure 2-2. The longer set of wires from P1 terminate in P3; the shorter set of wires from P1 terminate in P2.

Application of primary ac power is controlled by the system in which the RX01 is installed. The line cord must normally be plugged into a "switched ac" receptacle which is part of the system's ac power distribution system.

Figure 2-2 Power Harness Installation

2.2.4 Fire and Safety Precautions

The RXV11 Floppy Disk System presents no additional fire or safety hazards to an existing computer system. Wiring should be carefully checked, however, to ensure that the capacity is adequate for the added load and for any contemplated expansion.

2.3 ENVIRONMENTAL CONSIDERATIONS

2.3.1 General

The RXV11 is capable of efficient operation in computer environments; however, the parameters of the operating environment must be determined by the most restrictive facets of the system, which in this case are the diskettes.

2.3.2 Temperature, Relative Humidity

The operating ambient temperature range of the diskette is 59° to 90° F (15° to 32° C) with a maximum temperature gradient of 20° F/hr (-6.7° C/hr).

The diskette nonoperating temperature range (storage) is increased to -30° to 125° F (-34.4° to 51.6° C);

CAUTION

Care must be taken to ensure that the diskette temperature has stabilized within the operating temperature range before use. This range will ensure that the diskette will not be operated above its absolute temperature limit of 125 degrees F.

The RX01 is designed to operate efficiently within a relative humidity range of 20 to 80 percent, with a maximum wet bulb temperature of 77° F (25° C) and a maximum dew point of 36° F (2° C).

2.3.3. Heat Dissipation

The heat dissipation factor for the RX01 floppy disk drive is less than 225 Btu/hr.

2.3.4 Radiated Emissions

Sources of radiation, such as FM, vehicle ignitions, and radar transmitters located close to the computer system, may affect the performance of the RXV11 Floppy Disk System because of the possible adverse effects magnetic fields can have on diskettes. A magnetic field with an intensity of 50 oersteds or greater might destroy all or some of the information recorded on the diskette.

2.3.5 Cleanliness

Although cleanliness is important in all facets of a computer system, it is particularly important in the case of moving magnetic media, such as the diskettes used in the RX01. Diskettes are not a sealed unit and are vulnerable to dirt. Minute obstructions, such as dust specks or fingerprint smudges, may cause data errors. Hence, the RX01 should not be located in an unusually contaminated atmosphere, especially one with abrasive particles. (Refer to Paragraph 2.6.2.)

NOTE

Removable media involve use, handling, and maintenance which are beyond DIGITAL's direct control. DIGITAL disclaims responsibility for performance of the equipment when operated with media not meeting DIGITAL specifications or with media not maintained in accordance with procedures approved by DIGITAL. DIGITAL shall not be liable for damages to the equipment or to media resulting from such operation.

2.4 INSTALLATION

2.4.1 General

The RXV11 Floppy Disk System can be shipped installed in a cabinet as an integral part of a system, or as a separate option packed in a separate container. If the RX01 is shipped in a cabinet, position the cabinet in the final installation location and proceed with operation (Paragraph 2.5). The following paragraphs contain detailed information for installing the RXV11 when it is received as a separate option.

2.4.2 Tools

Installation of an RXV11 Floppy Disk System requires no special tools or equipment. Normal hand tools are all that are necessary.

2.4.3. RX01 Unpacking, Inspection, and Installation

1. Open the carton (Figure 2-3) and remove the corrugated packing pieces. Carefully store the two diskettes (Paragraph 2.6.2) for use after installation. The RXV11 interface module (M7946) installation is described in Paragraph 2.4.4; carefully store the module until it is installed.

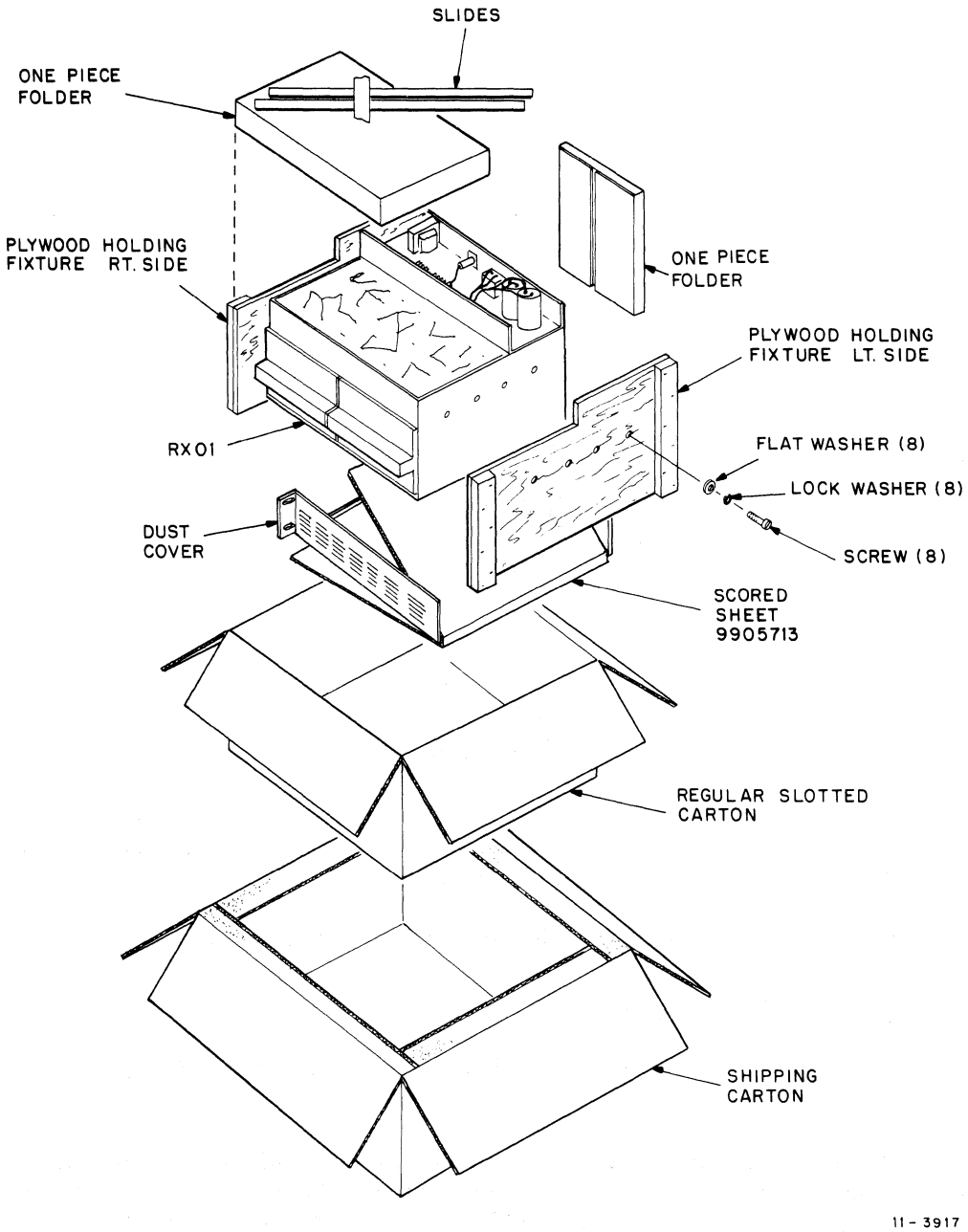


Figure 2-3 RX01 Unpacking

2. Lift the RX01 out of the carton.

3. Remove the shipping fixtures from both sides of the RX01 and inspect for shipping damage.

NOTE
If any shipping damage is found, the customer should notify the carrier of the damage.

4. Attach the *inside* tracks of the chassis slides (Figure 2-1) to the RX01.

5. Locate the proper holes in the cabinet rails in which the RX01 is to be installed (Figure 2-4). Attach the *outside* tracks to the cabinet rails.

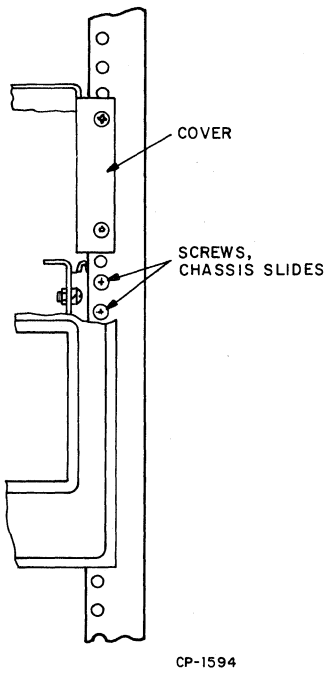


Figure 2-4 RX01 Cabinet Mounting Details

6. Place the tracks attached to the RX01 inside the extended cabinet tracks and slide the unit in until the tracks lock in the extended position.

7. Install the RX01 cover above the RX01 and secure it to the cabinet rails.

2.4.4 RXV11 Interface Module Installation

1. Loosen the screws securing the upper module (M7726) in the RX01 and swing it up on the hinge.

2. Inspect the wiring and connectors for proper routing and ensure that they are seated correctly (Figure 2-5). The BC05L-15 cable is secured to the RX01 by a clamp on the rear of the unit. The red edge of the cable should be located on the left end of the connector at the M7726, as shown in the figure.

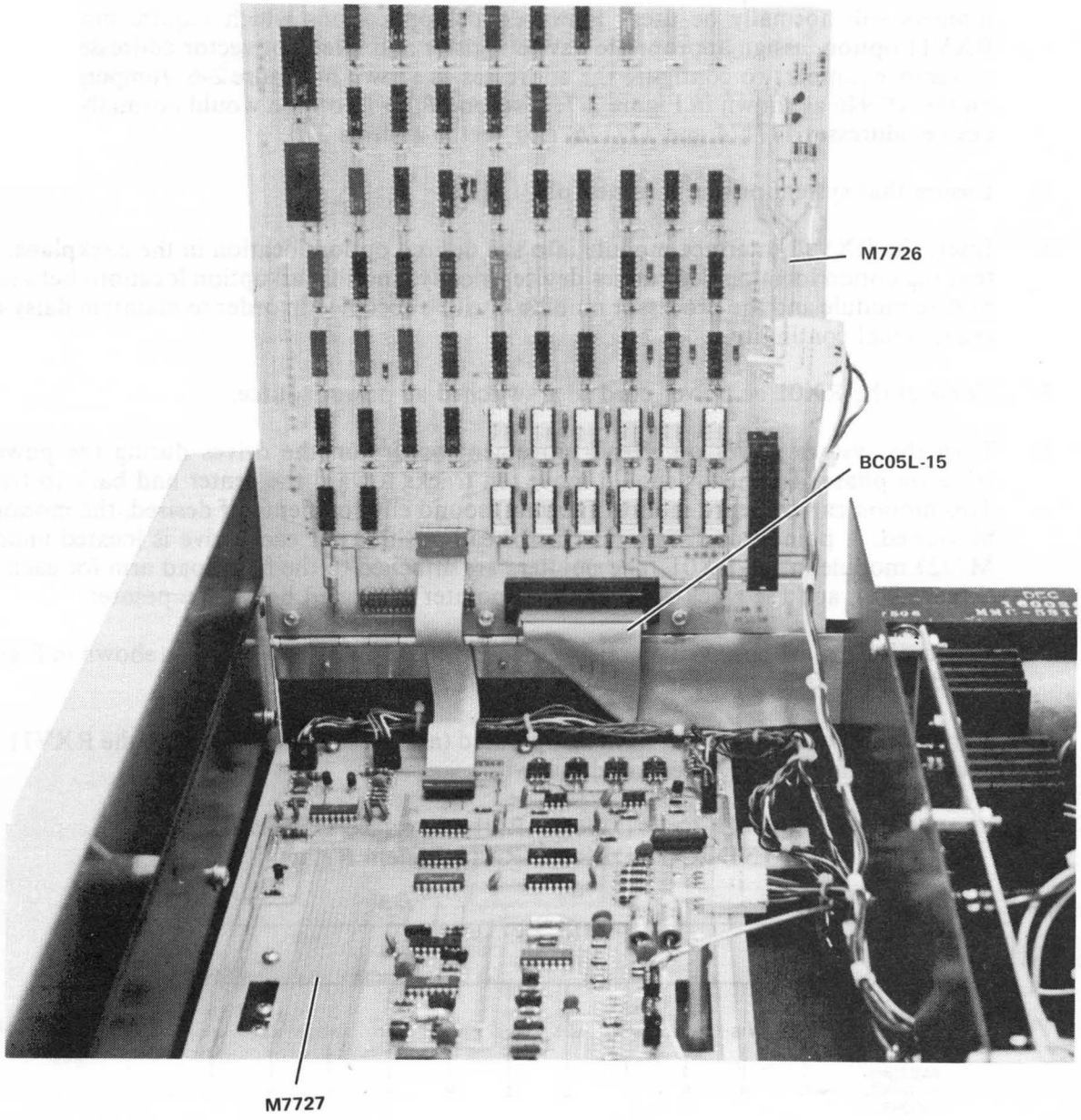


Figure 2-5 RX01 Cable Connections

3. Route the BC05L-15 cable to the backplane in which the RXV11 interface module is to be installed. Connect the cable to J1 on the interface module with the red stripe toward the center of the module (pin A end of J1).

4. All RXV11 interface modules are shipped with factory installed jumpers for the following device register addresses:

   RXCS = 177170
   RXDB = 177172

Interrupt vector jumpers are installed for vector address = 264. The factory configured jumpers will normally be used. However, in applications which require more than one RXV11 option, assign appropriate device register and interrupt vector addresses and install or remove jumpers to configure the addresses as shown in Figure 2-6. Jumpers are located on the M7946 as shown in Figure 2-7. A second RXV11 option would normally be assigned device addresses 177174 and 177176, and vector address 270.

5. Ensure that system power is turned off.

6. Insert the RXV11 interface module into the desired option location in the backplane. Note that the option location determines device priority, and that all option locations between the M7946 module and the processor module must be occupied in order to maintain daisy-chain grant signal continuity.

7. Connect the RX01 ac power cord to a switched ac power source.

8. Turn the system power on. Head movement occurs on the drives during the power up initialize phase. The heads should move ten tracks toward the center and back to track 0. This motion can be heard in most (normal) sound environments. If desired, the motion can be viewed. A pointer and scale for track/head position for each drive is located under the M7727 module in the RX01. The pointers are attached to the head load arm for each drive (Figure 2-8), and the track scale for each pointer is located below the pointer.

   The motion can be observed by raising the M7726 module to the position shown in Figure 2-5 and viewing from the rear edge of the M7727 module.

9. If the RXV11 system is being initially operated (after installation), execute the RXV11 diagnostic programs in the order listed below:

   MAINDEC-11-DZRXB RX11 Interface Diagnostic
   MAINDEC-11-DZRXA RX11 System Reliability Test

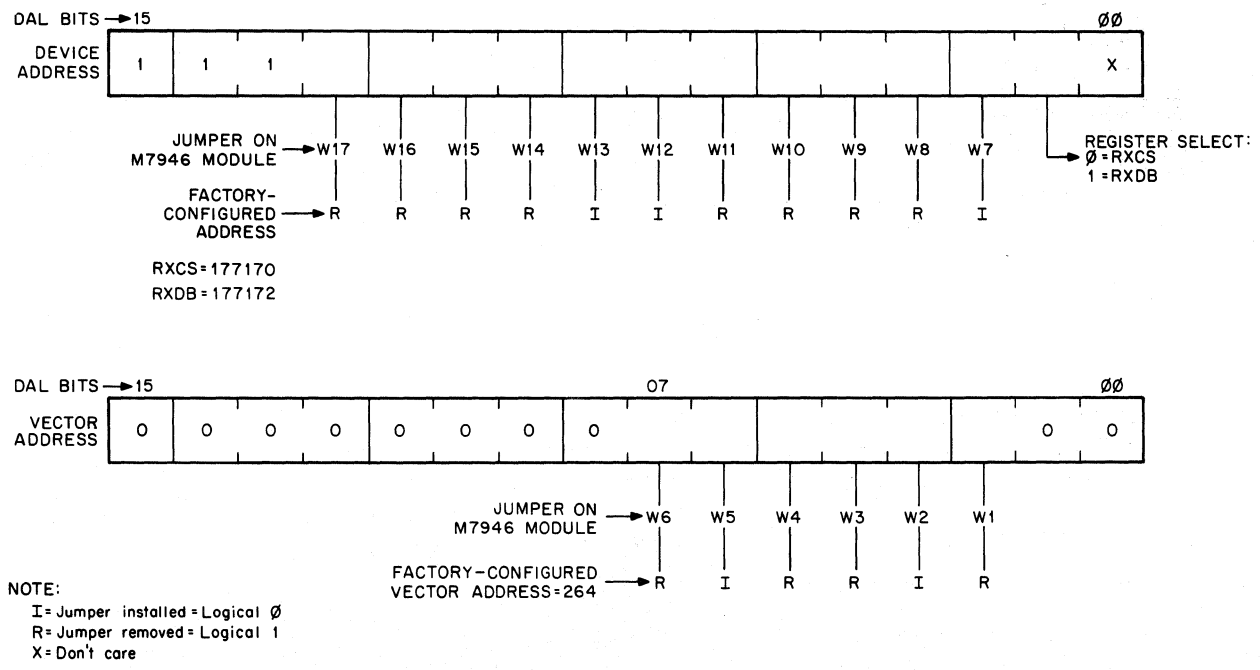


Figure 2-6 Device Register and Interrupt Vector Addressing

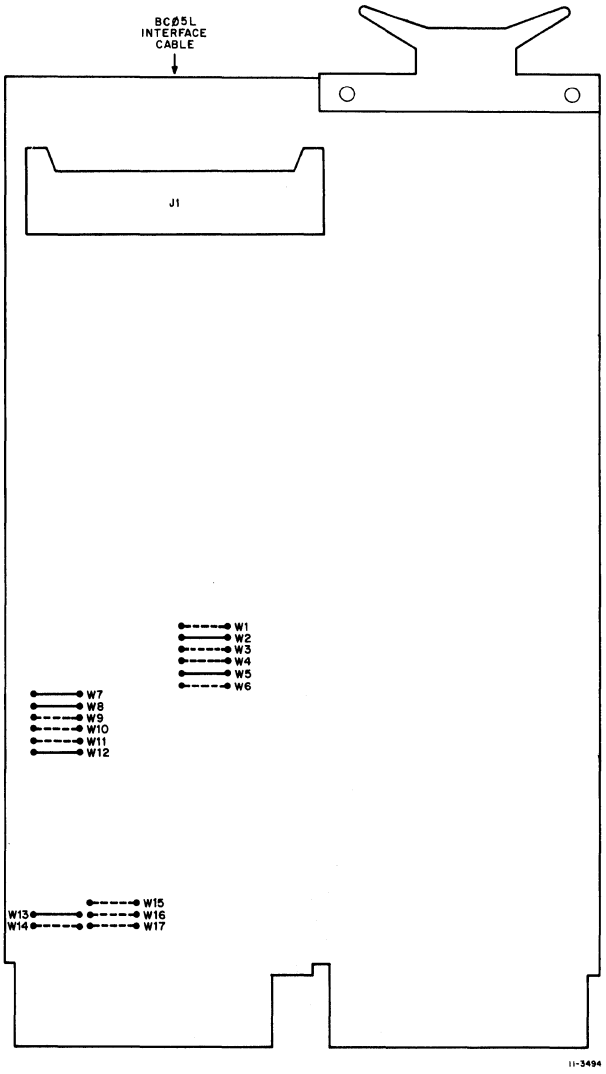


Figure 2-7 RXV11 Device Register and Interrupt Vector Jumper Locations

2.5 OPERATION

2.5.1 Operator Control

The simplicity of the RX01 precludes the necessity of operator controls and indicators. A convenient method of opening the unit for diskette insertion and removal is provided. On each drive there is a simple pushbutton, which is compressed to allow the spring-loaded front cover to open. The diskette may be inserted or removed, as shown in Figure 2-9, with the label up. The front cover will automatically lock when the bar is pushed down.

CAUTION

The drive(s) should not be opened while they are being accessed because data may be incorrectly recorded, resulting in a CRC error when the sector is read.

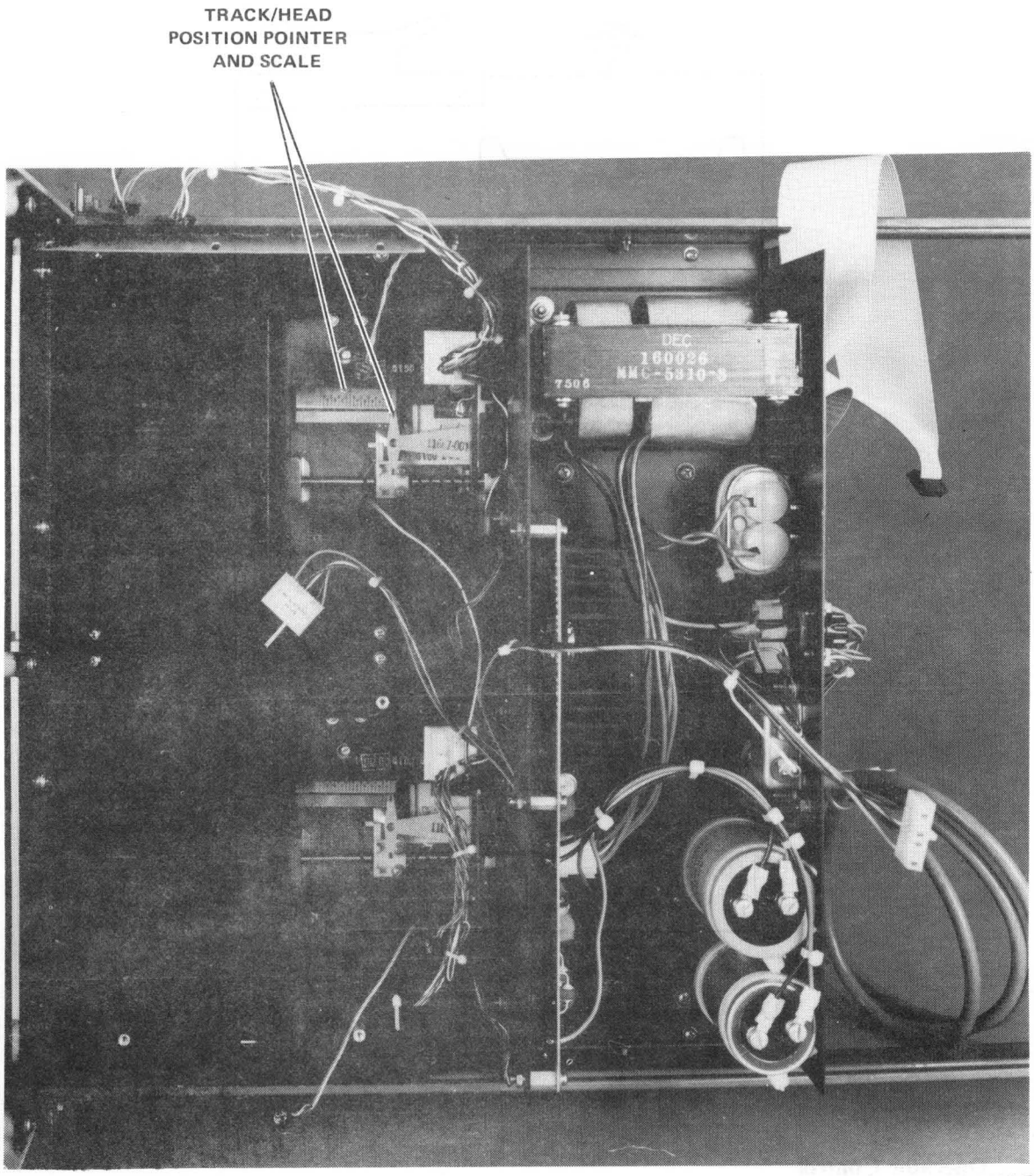


Figure 2-8 Track/Head Position Components

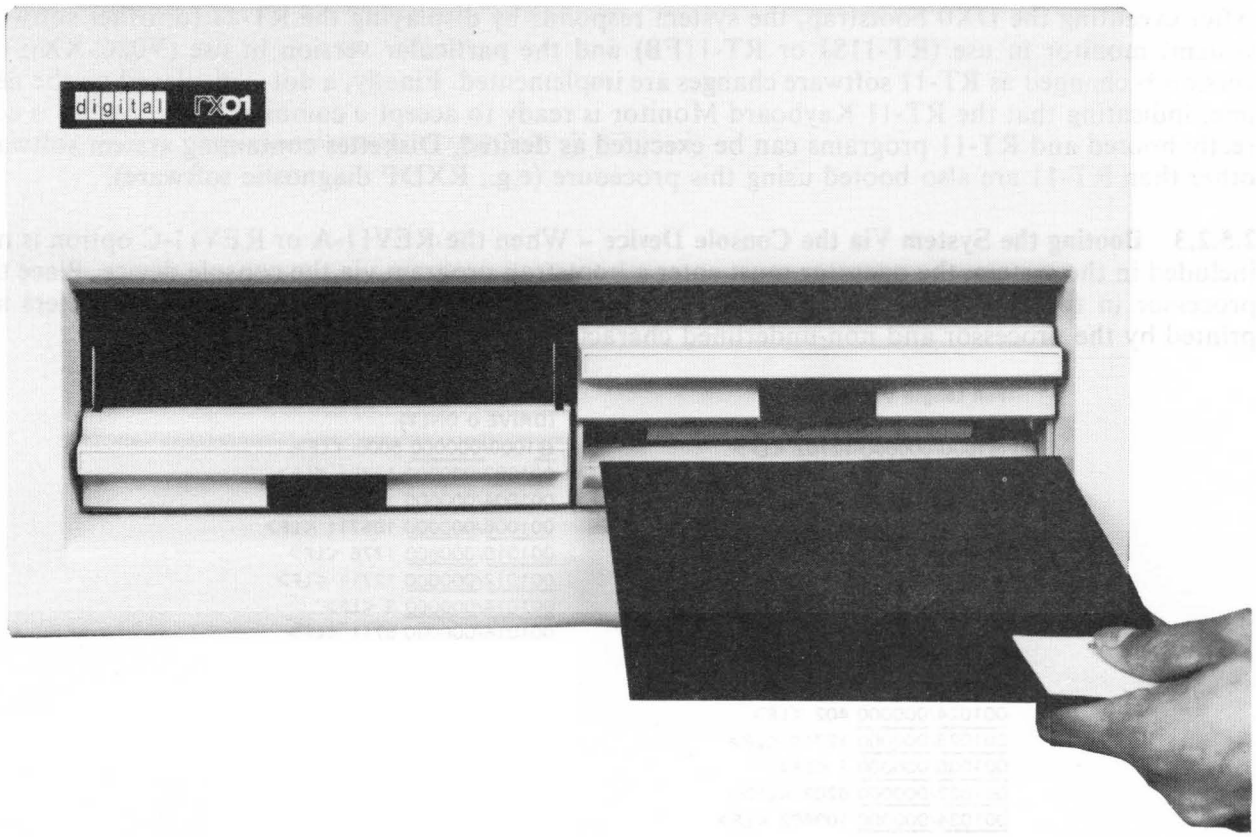


Figure 2-9 Diskette Insertion

2.5.2 Bootstrapping the RXV11

2.5.2.1 General – The RXV11 bootstrap loader program loads the system monitor from disk into system memory. No system operation can occur until the monitor is contained in system memory. Bootstrapping ("booting") the system can be accomplished via a hardware-implemented bootstrap in the REV11-A or REV11-C option, or it can be entered and executed via the console device.

2.5.2.2 Booting the System Using the REV11-A or REV11-C – The REV11-A or REV11-C implements the RXV11 bootstrap (and other bootstrap programs) in four preprogrammed ROM chips. When system power is applied, and LSI-11 processor Mode 2 power-up sequence is configured on the processor module, the system responds with a dollar sign ($) on a new line. The operator then responds by typing the device to be bootstrapped. DX (or DX0) is disk drive 0; DX1 is disk drive 1 in dual-drive RXV11 systems. A normal sequence of operations from power up through booting DX0 (containing RT-11) is shown below.

```
$DX <CR>
RT-11SJ V02C-XX
.
```

After executing the DX0 bootstrap, the system responds by displaying the RT-11 (or other software system) monitor in use (RT-11SJ or RT-11FB) and the particular version in use (V02C-XX); the version is changed as RT-11 software changes are implemented. Finally, a dot is displayed on the next line, indicating that the RT-11 Keyboard Monitor is ready to accept a command. The system is correctly booted and RT-11 programs can be executed as desired. Diskettes containing system software other than RT-11 are also booted using this procedure (e.g., RXDP diagnostic software).

2.5.2.3 Booting the System Via the Console Device – When the REV11-A or REV11-C option is not included in the system, the operator must enter a bootstrap program via the console device. Place the processor in the Halt mode and proceed as shown below; observe that underlined characters are printed by the processor and non-underlined characters are entered by the operator:

Full Length Version
(DRIVE 0 or DRIVE 1):

@1000/000000 12702 <LF>
001002/000000 1002n7 <LF> *
001004/000000 12701 <LF>
001006/000000 177170 <LF>
001010/000000 130211 <LF>
001012/000000 1776 <LF>
001014/000000 112703 <LF>
001016/000000 7 <LF>
001020/000000 10100 <LF>
001022/000000 10220 <LF>
001024/000000 402 <LF>
001026/000000 12710 <LF>
001030/000000 1 <LF>
001032/000000 6203 <LF>
001034/000000 103402 <LF>
001036/000000 112711 <LF>
001040/000000 111023 <LF>
001042/000000 30211 <LF>
001044/000000 1776 <LF>
001046/000000 100756 <LF>
001050/000000 103766 <LF>
001052/000000 105711 <LF>
001054/000000 100771 <LF>
001056/000000 5000 <LF>
001060/000000 22710 <LF>
001062/000000 240 <LF>
001064/000000 1347 <LF>
001066/000000 122702 <LF>
001070/000000 247 <LF>
001072/000000 5500 <LF>
001074/000000 5007 <CR>

Abbreviated Version
(DRIVE 0 ONLY):

@1000/000000 5000 <LF>
001002/000000 12701 <LF>
001004/000000 177170 <LF>
001006/000000 105711 <LF>
001010/000000 1776 <LF>
001012/000000 12711 <LF>
001014/000000 3 <LF>
001016/000000 5711 <LF>
001020/000000 1776 <LF>
001022/000000 100405 <LF>
001024/000000 105711 <LF>
001026/000000 100004 <LF>
001030/000000 116120 <LF>
001032/000000 2 <LF>
001034/000000 770 <LF>
001036/000000 0 <LF>
001040/000000 5007 <CR>

*n = 4 for Unit 0
n = 6 for Unit 1
<LF> = Line Feed
<CR> = Carriage Return
Starting address = 1000

The bootstrap program can be started at location 1000. Enable the Run mode by placing the HALT/ENABLE switch (on the PDP-11/03 panel, or an equivalent LSI-11 switch) in the ENABLE position. Start the program using the Go command, as follows:

@1000G

After a few seconds the RT-11 (or other software system) monitor will be loaded in system memory. The monitor will identify itself on the console device by typing a message, as previously described.

2.6 DISKETTE HANDLING PRACTICES AND PRECAUTIONS

2.6.1 General

To prolong diskette life and to prevent errors when recording or reading, reasonable care should be taken when handling the media. The following handling recommendations should be followed to prevent unnecessary loss of data or interruptions of system operation.

1. Do not write on the envelope containing the diskette. Write any information on a label prior to affixing it to the diskette.

2. Paper clips should not be used on the diskette.

3. Do not use writing instruments that leave flakes, such as lead or grease pencils, on the jacket of the media.

4. Do not touch the disk surface exposed in the diskette slot or index hole.

5. Do not clean the disk in any manner.

6. Keep the diskette away from magnets or tools that may have become magnetized. Any disk exposed to a magnetic field may lose information.

7. Do not expose the diskette to a heat source or sunlight.

8. Always return the diskette to the envelope supplied with it to protect the disk from dust and dirt. Diskettes not being used should be stored in a file box (user-supplied) if possible.

9. When the diskette is in use, protect the empty envelope from liquids, dust, and metallic materials.

10. Do not place heavy items on the diskette.

11. Do not store diskettes on top of computer cabinets or in places where dirt can be blown by fans into the diskette interior.

12. If a diskette has been exposed to temperatures outside the operating range, allow five minutes for thermal stabilization before use. (The diskette must be removed from its shipping container during this time.)

2.6.2 Diskette Storage

Store diskettes in their envelopes in horizontal stacks of ten diskettes or less. If vertical storage is necessary, the diskettes should be supported so that they do not lean or sag, but should not be subjected to compressive forces. Permanent deformation may result from improper storage. Store diskettes in an environment similar to that of the operating system, within the operating environment range specified in Paragraph 1.7. When diskettes do not need to be available for immediate use, they should be stored within the specified nonoperating environment range of the media.

2.6.3 Shipping Diskettes

Diskettes (not originally packed with the RX01) can be safely shipped in their original cartons. In general, the diskettes must be protected from magnetic fields and excessive temperatures during shipment. Good protection from magnetic fields is provided by physical separation from the possible source. If the original shipping carton is not used, pack diskettes with at least three inches of packing material (or spacers) on both sides and along all edges. This separation will make special magnetic shielding unnecessary.

Avoid exposure of the diskettes to excessive temperatures. Label the packages with the following statement:

DO NOT EXPOSE TO PROLONGED HEAT OR SUNLIGHT

When received, the diskette carton should be examined for damage. Deformation of the carton may indicate possible damage of the diskette(s). The shipping carton should be retained (if it is intact) for diskette storage or for future shipping.

CHAPTER 3
PROGRAMMING THE RXV11

3.1 GENERAL

All software control of the RXV11 is performed by means of two device registers: the RXV11 Command and Status register (RXCS) and a multipurpose RXV11 Data Buffer register (RXDB). These registers can be read or loaded by programs using instructions referring to their device addresses. The RX01 contains a read/write data buffer that can contain one full sector (128 8-bit bytes) of diskette data. This buffer and other RXV11 registers are located as shown in Figure 3-1. The program has direct access to the RXCS and RXCB registers only. Access to registers and the read/write buffer in the RX01 is via the RXDB.

Read and write data transfers always require two steps. When writing data, the program first fills the buffer with write data via program transfers with the RXDB. Once the buffer is filled, the program issues a write sector command via the RXCS and the buffer's contents are written onto the diskette. During a read operation, the diskette data is first read into the buffer. The program then reads the data via the RXDB.

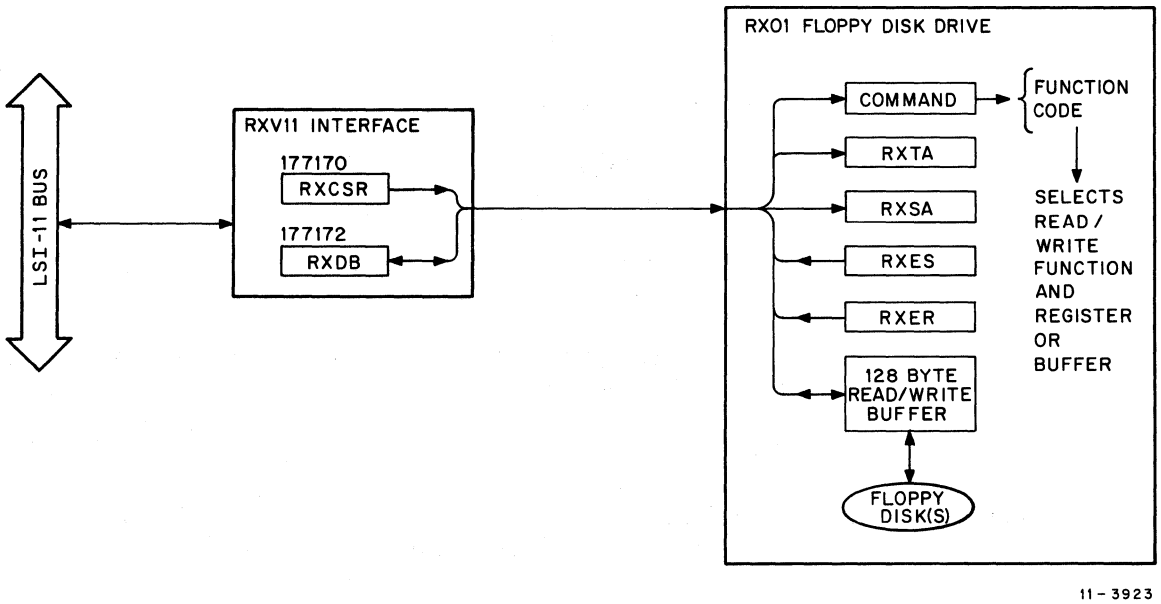


Figure 3-1 RXV11 System Register Functions

3.2 REGISTER AND VECTOR ADDRESSES

The RXCS register is normally assigned device address 177170, and the RXDB register is assigned device address 177172. The vector address is 264.

3.3 REGISTER DESCRIPTION

3.3.1 RXCS - Command and Status (177170)

Loading this register while the RX01 is not busy and with bit 0 = 1 will initiate a function as described below and indicated in Figure 3-2. Bits 0–4 are write-only bits.

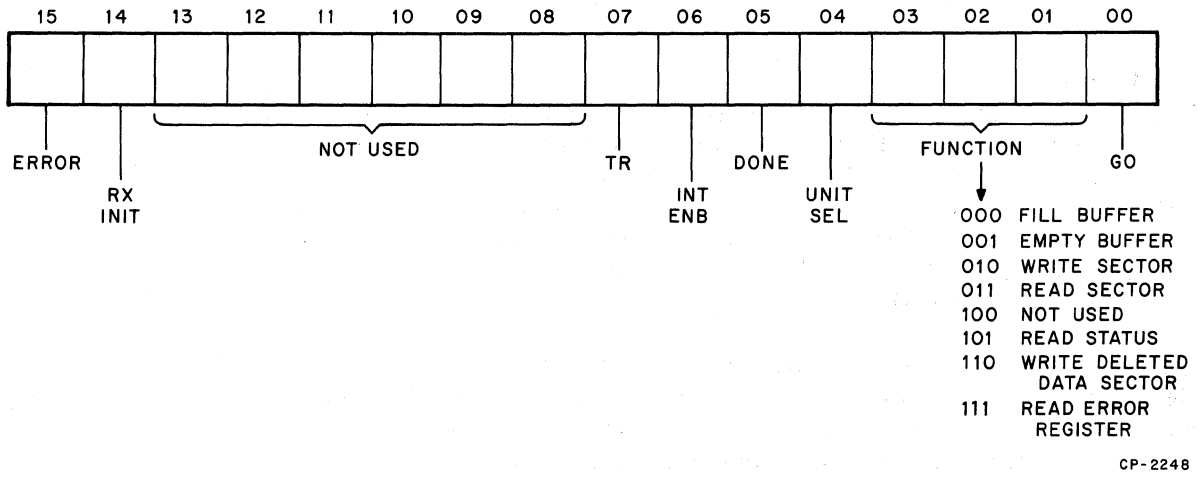


Figure 3-2 RXCS Format

Bit No.	Description
0	Go - Initiates a command to RX01. This is a write-only bit.
1–3	Function Select - These bits code one of the eight possible functions described in Paragraph 3.4. These are write-only bits.
4	Unit Select - This bit selects one of the two possible disks for execution of the desired function. This is a write-only bit.
5	Done - This bit indicates the completion of a function. Done will generate an interrupt when asserted if Interrupt Enable (RXCS bit 6) is set. This is a read-only bit.
6	Interrupt Enable - This bit is set by the program to enable an interrupt when the RX01 has completed an operation (Done). The condition of this bit is normally determined at the time a function is initiated. This bit is cleared by the LSI-11 bus initialize (BINIT L) signal, but it is not cleared by the RXV11 Initialize bit (RXCS bit 14). This is a read/write bit.
7	Transfer Request - This bit signifies that the RXV11 needs data or has data available. This is a read-only bit.
8–13	Unused

Bit No.	Description
14	RXV11 Initialize – This bit is set by the program to initialize the RXV11 without initializing all of the devices on the LSI-11 Bus. This is a write-only bit.

CAUTION

1. Loading the lower byte of the RXCS will also load the upper byte of the RXCS.

2. Setting this bit (BIS instruction) will not clear the interrupt enable bit (RXCS bit 06).

Upon setting this bit in the RXCS, the RXV11 will negate Done and move the head position mechanism of drive 1 (if two are available) to track 0. Upon completion of a successful Initialize, the RX01 will zero the Error and Status register, set Initialize Done, and set RXES bit 7 (DRV RDY) if unit 0 is ready. It will also read sector 1 of track 1 on drive 0.

15 Error – This bit is set by the RX01 to indicate that an error has occurred during an attempt to execute a command. This read-only bit is cleared by the initiation of a new command or by setting the Initialize bit. When an error is detected, the RXES is automatically read into the RXDB.

3.3.2 RXDB – Data Buffer Register (177172)

This RX01 interface register serves as a general purpose data path between the RX01 and the interface. It may represent one of five RX01 registers according to the protocol of the command function in progress (Paragraph 3.4). The RX01 registers include RXDB, RXTA, RXSA, RXES, and RXER.

This register is read/write if the RX01 is not in the process of executing a command; that is, it may be manipulated without affecting the RX01 subsystem. If the RX01 is actively executing a command, this register will only accept data if RXCS bit 7 (TR) is set. In addition, valid data can only be read when TR is set.

CAUTION

Violation of protocol in manipulation of this register may cause permanent data loss.

3.3.2.1 RXDB – RX Data Buffer (Figure 3-3) – All information transferred to and from the floppy media passes through this register and is addressable only under the protocol of the function in progress.

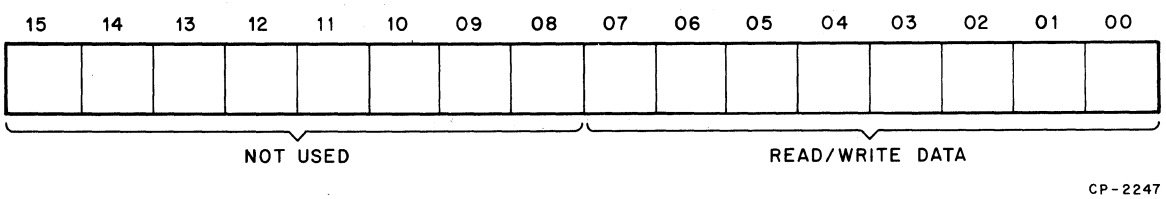


Figure 3-3 RXDB Format

3.3.2.2 RXTA – RX Track Address (Figure 3-4) – This register is loaded to indicate on which of the 114_8 tracks a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.

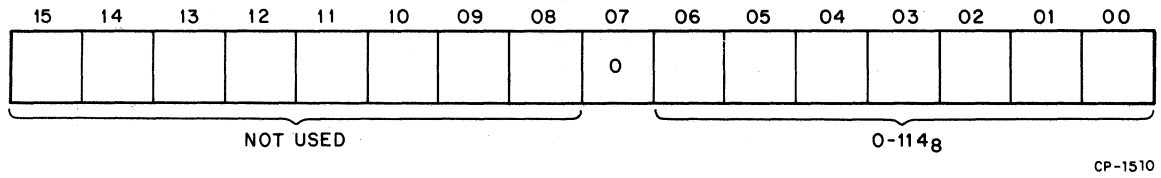


Figure 3-4 RXTA Format

3.3.2.3 RXSA – RX Sector Address (Figure 3-5) – This register is loaded to indicate on which of the 32_8 sectors a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.

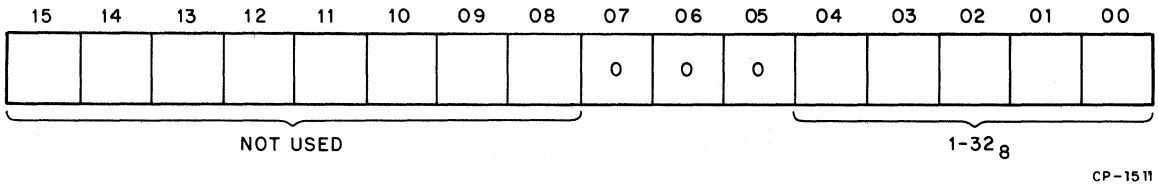


Figure 3-5 RXSA Format

3.3.2.4 RXES – RX Error and Status (Figure 3-6) – This register contains the current error and status conditions of the drive selected by bit 4 (Unit Select) of the RXCS. This read-only register can be addressed only under the protocol of the function in progress. The RXES is located in the RXDB upon completion of a function.

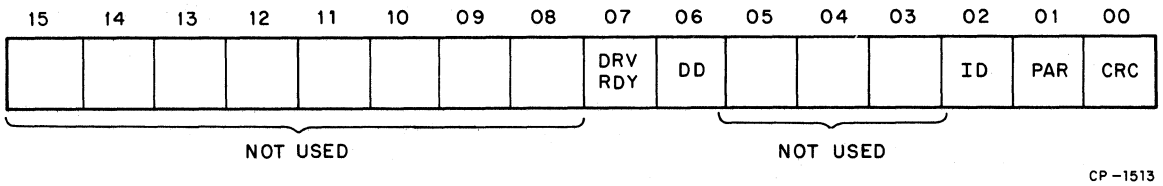


Figure 3-6 RXES Format

RXES bit assignments are:

Bit No.	Description
0	CRC Error – A cyclic redundancy check error was detected as information was retrieved from a data field of the diskette. The RXES is moved to the RXDB, and Error and Done are asserted.
1	Parity Error – A parity error was detected on command or on address information being transferred to the RX01 from the LSI-11 Bus interface. A parity error indication means that there is a problem in the interface cable between the RX01 and the interface. Upon detection of a parity error, the current function is terminated; the RXES is moved to the RXDB, and Error and Done are asserted.
2	Initialize Done – This bit is asserted in the RXES to indicate completion of the Initialize routine, which can be caused by RX01 power failure, system power failure, or programmable or LSI-11 Bus Initialize.
3–5	Unused
6	Deleted Data Detected – During data recovery, the identification mark preceding the data field was decoded as a deleted data mark (Paragraph 1.4.3).
7	Drive Ready – This bit is asserted if the unit currently selected exists, is properly supplied with power, has a diskette installed correctly, has its door closed, and has a diskette up to speed.

NOTE 1

The Drive Ready bit is only valid when retrieved via a Read Status function or at completion of Initialize when it indicates status of drive 0.

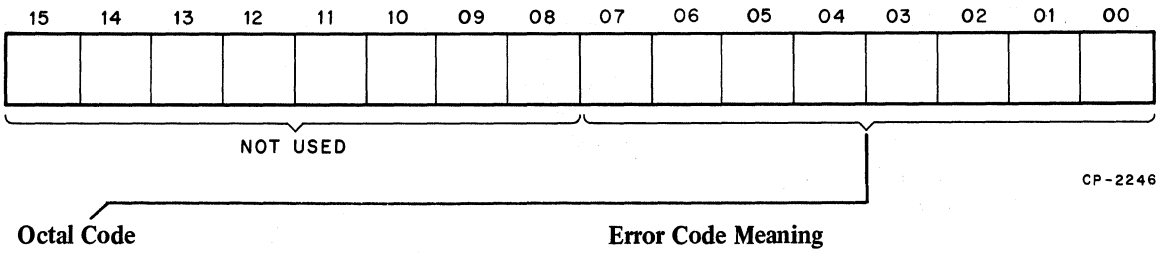
NOTE 2

If the Error bit was set in the RXCS but Error bits are not set in the RXES, then specific error conditions contained in the RXER can be accessed from the RXDB via a Read Error Register function (Paragraph 3.4.7)

3.3.2.5 RXER – RX Error (Figure 3-7) – This register is located in the RX01 and contains specific RX01 error information. This information is normally accessed when the RXCS error bit 15 is set but RXES error bits 0 and 1 are not set. This is a read-only register.

3.4 FUNCTION CODES

Data storage and recovery on the RXV11 system is accomplished by careful manipulation of the RXCS and RXDB registers according to the strict protocol of individual functions. The penalty for violation of protocol can be permanent data loss. Each of the functions are encoded and written into RXCS bits 1–3, as shown in Figure 3-1. Programming protocol for each function is described below.



Octal Code	Error Code Meaning
0010	Drive 0 failed to see home on Initialize.
0020	Drive 1 failed to see home on Initialize.
0030	Found home when stepping out 10 tracks for INIT.
0040	Tried to access a track greater than 77.
0050	Home was found before desired track was reached.
0060	Self-diagnostic error.
0070	Desired sector could not be found after looking at 52 headers (2 revolutions).
0110	More than 40 μs and no SEP clock seen.
0120	A preamble could not be found.
0130	Preamble found but no I/O mark found within allowable time span.
0140	CRC error on what we thought was a header.
0150	The header track address of a good header does not compare with the desired track.
0160	Too many tries for an IDAM (identifies header).
0170	Data AM not found in allotted time.
0200	CRC error on reading the sector from the disk. No code appears in the ERREG.
0210	All parity errors.

Figure 3-7 RXER Format

3.4.1 Fill Buffer (000)

This function is used to fill the RX01 buffer with 128 8-bit bytes of data from the host processor. Fill Buffer is a complete function in itself; the function ends when the buffer has been filled. The contents of the buffer can be written onto the diskette by means of a subsequent Write Sector function, or the contents can be returned to the host processor by an Empty Buffer function.

RXCS bit 4 (Unit Select) does not affect this function, since no diskette drive is involved. When the command has been loaded, RXCS bit 5 (Done) is negated. When the TR bit is asserted, the first byte of data may be loaded into the data buffer. The same TR cycle will occur as each byte of data is loaded. The RX01 counts the bytes transferred; it will not accept less than 128 bytes and will ignore those in excess. Any read of the RXDB during the cycle of 128 transfers results in invalid read data.

3.4.2 Empty Buffer (001)

This function is used to empty the internal buffer of the 128 data bytes loaded from a previous Read Sector or Fill Buffer command. This function will ignore RXCS bit 4 (Unit Select) and negate Done.

When TR sets, the program may unload the first of 128 data bytes from the RXDB. Then the RXV11 again negates TR. When TR resets, the second byte of data may be unloaded from the RXDB, which again negates TR. Alternate checks on TR and data transfers from the RXDB continue until 128 bytes of data have been moved from the RXDB. Done sets, ending the operation and initiating an interrupt if RXCS bit 6 (Interrupt Enable) is set. RXES contents are moved to the RXDB where they can be read.

NOTE

The Empty Buffer function does not destroy the contents of the sector buffer.

3.4.3 Write Sector (010)

This function is used to locate a desired track and sector and write the sector with the contents of the internal sector buffer. The initiation of this function clears bits 0, 1, and 6 of RXES (CRC Error, Parity Error, and Deleted Data Detected) and negates Done.

When TR is asserted, the program must first move the desired sector address into the RXDB, which will negate TR. When TR is again asserted, the program must move the desired track address into the RXDB, which will negate TR. If the desired track is not found, the RXV11 will abort the operation, move the contents of the RXES to the RXDB, set RXCS bit 15 (Error), assert Done, and initiate an interrupt if RXCS bit 6 (Interrupt Enable) is set.

TR will remain negated while the RX01 attempts to locate the desired sector. If the RX01 is unable to locate the desired sector within two diskette revolutions, the RXV11 will abort the operation, move the contents of the RXES to the RXDB, set RXCS bit 15 (Error), assert Done, and initiate an interrupt if RXCS bit 6 (Interrupt Enable) is set.

If the desired sector is successfully located, the RXV11 will write the 128 bytes stored in the internal buffer followed by a 16-bit CRC character that is automatically calculated by the RX01. The RXV11 ends the operation by asserting Done and initiating an interrupt if RXCS bit 6 (Interrupt Enable) is set.

NOTE 1

The contents of the sector buffer are not valid data after a power loss has been detected by the RX01. The Write Sector function, however, will be accepted as a valid function, and the random contents of the buffer will be written, followed by a valid CRC.

NOTE 2

The Write Sector function does not destroy the contents of the sector buffer.

3.4.4 Read Sector (011)

This function is used to locate a desired track and sector and transfer the contents of the data field to the μCPU controller sector buffer. The initiation of this function clears bits 0, 1, and 6 of RXES (CRC Error, Parity Error, Deleted Data Detected) and negates Done.

When TR is asserted, the program must first move the desired sector address into the RXDB, which will negate TR. When TR is again asserted, the program must move the desired track address into the RXDB, which will negate TR.

If the desired track is not found, the RXV11 will abort the operation, move the contents of the RXES to the RXDB, set RXCS bit 15 (Error), assert Done, and initiate an interrupt if RXCS bit 6 (Interrupt Enable) is set.

TR and Done will remain negated while the RX01 attempts to locate the desired track and sector. If the RX01 is unable to locate the desired sector within two diskette revolutions after locating the presumably correct track, the RXV11 will abort the operation, move the contents of the RXES to the RXDB, set RXCS bit 15 (Error), assert Done, and initiate an interrupt if RXCS bit 6 (Interrupt Enable) is set.

If the desired sector is successfully located, the control will attempt to locate a standard data address mark or a deleted data address mark. If either mark is properly located, the control will read data from the sector into the sector buffer.

If the deleted data address mark was detected, the control will assert RXES bit 6 (DD). As data enters the sector buffer, a CRC is computed, based on the data field and CRC bytes previously recorded. A non-zero residue indicates that a CRC error has occurred. The control sets RXES bit 0 (CRC Error) and RXCS bit 15 (Error). The RXV11 ends the operation by moving the contents of the RXES to the RXDB, sets Done, and initiates an interrupt if RXCS bit 6 (Interrupt Enable) is set.

3.4.5 Read Status (101)

The RXV11 will negate RXCS bit 5 (Done) and begin to assemble the current contents of the RXES into the RXDB. RXES bit 7 (Drive Ready) will reflect the status of the drive selected by RXCS bit 4 (Unit Select) at the time the function was given. All other RXES bits will reflect the conditions created by the last command. RXES may be sampled when RXCS bit 5 (Done) is again asserted. An interrupt will occur if RXCS bit 6 (Interrupt Enable) is set. RXES bits are defined in Paragraph 3.3.2.4.

NOTE

The average time for this function is 250 ms. Excessive use of this function will result in substantially reduced throughput.

3.4.6 Write Sector with Deleted Data (110)

This operation is identical to function 010 (Write Sector) with the exception that a deleted data address mark precedes the data field instead of a standard data address mark (Paragraph 1.4.3.2).

3.4.7 Read Error Register Function (111)

The Read Error Register function can be used to retrieve explicit error information contained in the RXER when the RXCS error bit 15 is set. The function is initiated, and bits 0–6 of the RXES are cleared. Out is asserted and Done is negated. The controller then generates the appropriate number of shift pulses to transfer the specific error code from the RXER to the Interface register and completes the function by asserting Done. The RXDB program can then read the error code to determine the type of failure that occurred (Figure 3-6).

NOTE

Care should be exercised in use the of this function since, under certain conditions, erroneous error information may result (Paragraph 3.6).

3.4.8 Power Fail

There is no actual function code associated with Power Fail. When the RX01 senses a loss of power, it will unload the head and abort all controller action. All status signals are invalid while power is low.

When the RX01 senses the return of power, it will remove Done and begin a sequence to:

1. Move drive 0 head position mechanism to track 0.
2. Clear any active error bits.
3. Read sector 1 of track 1 of drive 0 into the sector buffer.
4. Set RXES bit 2 (Initialize Done) (Paragraph 3.3.2.4) after which Done is again asserted.
5. Set Drive Ready of the RXES according to the status of drive 0.

There is no guarantee that information being written at the time of a power failure will be retrievable. However, all other information on the diskette will remain unaltered.

A method of aborting a function is through the use of RXCS bit 14 (RXV11 Initialize); however, this will not clear the interrupt enable bit (RXCS bit 06). Another method is through the use of the system Initialize signal that is generated by the PDP-11 RESET instruction, the console ODT Go command, or system power failure.

3.5 PROGRAMMING EXAMPLES

3.5.1 Read Data/Write Data

Figure 3-8 presents a program for implementing a Write, Write Deleted Data, or a Read function, depending on the function code that is used. The first instructions set up the error retry counters, PTRY, CTRY, and STRY. The instruction RETRY moves the command word for a Write, Write Deleted Data, or Read into the RXCS.

The set of three instructions beginning at the label 1$ moves the sector address to the RXV11 after Transfer Request (TR), which is bit 7, has been set. The three instructions beginning at the label 2$ move the track address to the RXV11 after TR has been set. The group of instructions beginning at the label 3$ looks for the Done flag to set and checks for errors.

An error condition, indicated by bit 15 setting, is checked beginning at ERFLAG. If bit 0 is set, a CRC error has occurred, and a branch is made to CRCER. If bit 1 is set, a parity error has occurred, and a branch is made to PARER. If neither of the above bits is set, a seek error is assumed to have occurred and a branch is made to SEEKER, where the system is initialized. In the case of a Write function, the sector buffer is refilled by a JMP to FILLBUF. In the case of a Read function, a JMP is made to EMPBUFF.

In each of the PAR, CRC, and SEEK routines, the command sequence is retried ten times by decrementing the respective retry counter. If an error persists after ten tries, it is a hard error. The retry counters can be set up to retry as many times as desired.

NOTE

A Fill Buffer function is performed before a Write function, and an Empty Buffer function is performed after a Read function.

3.5.2 Empty Buffer Function

Figure 3-9 shows a program for implementing an Empty Buffer function. The first instruction sets the number of error retries to ten. The address of the memory buffer is placed in register R0, and the Empty Buffer command is placed in the RXCS. Existence of a parity error is checked starting at instruction 3$. If a parity error is detected, the Empty Buffer command is loaded again. If an error persists for ten retries, the error is considered hard.

If no error is indicated, the program looks for the Transfer Request (TR) flag to set. The Error flag is retested if TR is not set. Once TR sets, a byte is moved from the RXV11 sector buffer to the core locations of BUFFER. The process continues until the sector buffer is empty and the Done bit is set.

3.5.3 Fill Buffer Function

Figure 3-10 presents a program to implement a Fill Buffer function. It is very similar to the Empty Buffer example.

```
                                        .ABS
                                    ;PROGRAMMING EXAMPLES FOR THE RX11/RX01 FLEXIBLE DISKETTE
                                    ;
                                    ;THE FOLLOWING IS THE RX11 STANDARD DEVICE ADDRESS AND VECTOR ADDRESS
                                    ;
            177170                  RXCS=177170                     ; COMMAND STATUS REGISTER
            177172                  RXDB=177172                     ; DATA BUFFER REGISTER
            177172                  RXSA=177172                     ; SECTOR ADDRESS REGISTER
            177172                  RXTA=177172                     ; TRACK ADDRESS REGISTER
            177172                  RXES=177172                     ; ERROR STATUS REGISTER
                                    ;
                                    ;THE FOLLOWING IS A PROGRAMMING EXAMPLE OF THE PROTOCOL REQUIRED
                                    ;TO WRITE, WRITE DELETED DATA, OR READ AT SECTOR "S" (THE CONTENTS OF PROGRAM
                                    ;LOCATION SECTOR) OF TRACK "T" (THE CONTENTS OF PROGRAM LOCATION TRACK)
                                    ;
000000  012767  177770  000320    START:  MOV #-10, PTRY          ; PARITY RETRY COUNTER
000006  012767  177770  000314            MOV #-10, CTRY          ; CRC RETRY COUNTER
000014  012767  177770  000310            MOV #-10, STRY          ; SEEK RETRY COUNTER
                                    ;
                                    ;WRITE, WRITE DELETED DATA, OR READ
                                    ;
                                    ; BITS 4 THRU 1 OF PROGRAM LOCATION COMMAND CONTAIN THE FUNCTION
                                    ;
                                    ; BIT 4 = 1 MEANS UNIT 1 ( = 0 MEANS UNIT 0)
                                    ;
                                    ; BITS 3 THRU 1 IS THE COMMAND ( 4 = WRITE, 14 = WRITE DELETED DATA, 6 = READ)
                                    ;
000022  016767  000306  177140    RETRY:  MOV COMMAND, RXCS       ; UNIT + (WRITE, WRITE DELETED DATA, OR READ)
                                    ;
                                    ;WAIT FOR THE TRANSFER REQUEST FLAG THEN TRANSFER THE SECTOR ADDRESS
                                    ;
000030  105767  177134            1$:     TSTB RXCS               ; TEST FOR THE TRANSFER REQUEST FLAG
000034  001775                            BEQ 1$                  ; BEQ UNTIL THE TRANSFER REQUEST FLAG SETS
000036  116767  000274  177126            MOVB SECTOR, RXSA       ; LOAD SECTOR ADDRESS
                                    ;
                                    ;WAIT FOR THE TRANSFER REQUEST FLAG THEN TRANSFER THE TRACK ADDRESS
                                    ;
000044  105767  177120            2$:     TSTB RXCS               ; TEST FOR THE TRANSFER REQUEST FLAG
000050  001775                            BEQ 2$                  ; BEQ UNTIL THE TRANSFER REQUEST FLAG SETS
000052  116767  000262  177112            MOVB TRACK, RXTA        ; LOAD TRACK ADDRESS
                                    ;
                                    ;THE SECTOR AND TRACK ADDRESSES HAVE BEEN TRANSFERRED TO THE RX01
                                    ;
                                    ;WSAIT FOR THE DONE FLAG AND CHECK FOR ANY ERRORS
                                    ;
                                    ;IF THE FUNCTION HAS COMPLETED SUCCESSFULLY (NO ERROR FLAG) THEN HALT
                                    ;
000060  032767  000040  177102    3$:     BIT #DONEBIT, RXCS      ; TEST FOR THE DONE FLAG
000066  001774                            BEQ 3$                  ; BEQ UNTIL THE DONE FLAG SETS
000070  005767  177074                    TST RXCS                ; TEST FOR THE ERROR FLAG
000074  001001                            BNE ERFLAG              ; BNE IF AN ERROR HAS OCCURED
000076  000000                            HALT                    ; OK = COMPLETED
                                    ;THE ERROR FLAG IS SET
                                    ;
                                    ;THE CONTENTS OF THE RXES IS THE ERROR STATUS
                                    ;
                                    ;IF THE RXES BITS 1 AND 0 = 0 THEN SOME TYPE OF SEEK ERROR OCCURED
                                    ;IF THE RXES BIT 0 = 1 THEN A CRC ERROR HAS OCCURED
                                    ;IF THE RXES BIT 1 = 1 THEN A PARITY ERROR HAS OCCURED
                                    ;
000100  032767  000003  177064    ERFLAG: BIT #3, RXES            ; TEST FOR CRC AND PARITY ERRORS
000106  001414                            BEQ SEEK                ; NOT A PARITY OR CRC [MUST] BE A SEEK
000110  032767  000002  177054            BIT #2, RXES            ; TEST FOR PARITY ERROR
000116  001404                            BEQ CRC                 ; NOT A PARITY ERROR [MUST] BE A CRC
                                    ;
                                    ;A PARITY ERROR HAS OCCURED
                                    ;
                                    ;INCREMENT AND TEST THE PARITY ERROR RETRY COUNTER PROGRAM LOCATION " PTRY "
                                    ;
                                    ;AND RETRY THE " COMMAND " UNTIL THE PARITY ERROR RECOVERS
                                    ;
                                    ;OR UNTIL THE PTRY COUNTER OVERFLOWS TO 0
                                    ;
000120  005267  000202                    INC PTRY
000124  001336                            BNE RETRY               ; RETRY THE COMMAND
000126  000000                            HALT                    ; HARD PARITY ERROR
                                    ;
                                    ;A CRC ERROR HAS OCCURED
                                    ;
                                    ;INCREMENT AND TEST THE CRC ERROR RETRY COUNTER PROGRAM LOCATION " CTRY "
                                    ;
                                    ;AND RETRY THE COMMAND UNTIL THE CRC ERROR RECOVERS
                                    ;
                                    ;OR UNTIL THE CTRY COUNTER OVERFLOWS TO 0
                                    ;
000130  005267  000174            CRC:    INC CTRY
000134  001332                            BNE RETRY               ; RETRY THE COMMAND
000136  000000                            HALT                    ; HARD CRC ERROR
                                    ;THE ERROR FLAG IS SET
                                    ;
                                    ;THE ERROR IS [NOT] A PARITY ERROR AND IS [NOT] A CRC ERROR
                                    ;
                                    ;THEREFORE IT MUST BE A SEEK ERROR
                                    ;
                                    ; (STATE OF RXCS BITS 0 AND 1 ARE 0)
                                    ;
000140  012767  040000  177022    SEEK:   MOV #INIT, RXCS         ; INITIALIZE
                                    ;
                                    ;INCREMENT AND TEST THE SEEK ERROR RETRY COUNTER PROGRAM LOCATION " STRY "
                                    ;
                                    ;AND RETRY THE COMMAND UNTIL THE SEEK ERROR RECOVERS
                                    ;
                                    ;OR UNTIL THE CTRY COUNTER OVERFLOWS TO 0
                                    ;
000146  005267  000160                    INC STRY
000152  001323                            BNE RETRY               ; RETRY THE COMMAND
000154  000000                            HALT                    ; HARD SEEK ERROR
```

Figure 3-8 Write/Write Deleted Data/Read Example

```
160                                     ;THE FOLLOWING IS A PROGRAMMING EXAMPLE OF PROTOCOL REQUIRED TO
161                                     ;
162                                     ;EMPTY THE  SECTOR BUFFER OF 128 8-BIT BYTES
163                                     ;
164  000242  012767  177770  000056     EENTRY: MOV #-10, PTRY          ; 8 TRYS TO EMPTY THE SECTOR BUFFER
165  000250  012700  000342             ESETUP: MOV #BUFFER, R0         ; PROHGRAMS DATA BUFFER
166  000254  016767  000054  176706             MOV COMMAND, RXCS       ; ISSUE THE COMMAND
167                                     ;
168                                     ;WAIT FOR A TRANSFER REQUEST FLAG BEFORE TRANSFERRING DATA TO THE PROGRAMS
169                                     ;
170                                     ;DATA BUFFER FRON THE RX01 SECTOR BUFFER
171                                     ;
172                                     ;WAIT FOR A DONE FLAG TO INDICATE THE COMPLETION OF THE EMPTY BUFFER COMMAND
173                                     ;
174                                     ;PRIOR TO TESTIN G THE ERROR FLAG
175                                     ;
176  000262  105767  176702             ELOOP:  TSTB RXCS               ; TEST FOR TRANSFER REQUEST FLAG
177  000266  001014                             BNE EMPTY               ; BNE IF TRANSFER REQUEST FLAG IS SET
178  000270  032767  000040  176672             BIT #DONEBIT, RXCS      ; TEST FOR DONE FLAG
179  000276  001771                             BEQ ELOOP               ; BEQ UNTIL THE DONE FLAG SETS
180                                     ;
181                                     ;THE DONE FLAG IS SET
182                                     ;
183                                     ;TEST FOR ANY ERRORS (ONLY ERROR POSSIBLE IS A PARITY ERROR)
184                                     ;
185  000300  005767  176664                     TST RXCS
186  000304  001001                             BNE 1$
187  000306  000000                             HALT                    ; NO ERRORS = OK = COMPLETE
188                                     ;
189                                     ;INCFEMENT AND TEST THE PARITY ERROR RETRY PROGRAM LOCATION " PTRY "
190                                     ;
191                                     ;AND RETRY THE COMMAND UNTIL THE ERROR RECOVERS
192                                     ;
193                                     ;OR UNTIL THE PTRY CUNTER OVERFLOWS TO 0
194                                     ;
195  000310  005267  000012             1$:     INC PTRY
196  000314  001355                             BNE ESETUP              ; RETRY TO EMPTY THE SECTOR BUFFER
197  000316  000000                             HALT                    ; HARD PARITY ERROR
198                                     ;
199                                     ;THE TRANSFER REQUEST FLAG IS SET
200                                     ;
201                                     ;TRANSFER DATA TO THE PROGRAM  DATA BUFFER FROM THE RX01 SECTOR BUFFER .
202                                     ;
203  000320  116730  176646             EMPTY:  MOVB RXDB, @(R0)+
204  000324  000756                             BR ELOOP
205                                     ;THE FOLLOWING 3 PROGRAM LOCATIONS ARE THE ERROR RETRY COUNTERS
206                                     ;
207  000326  000000                     PTRY:   0                       ; PARITY ERROR RETRY COUNTER
208  000330  000000                     CTRY:   0                       ; CRC ERROR RETRY COUNTER
209  000332  000000                     STRY:   0                       ; SEEK ERROR RETRY COUNTER
210                                     ;
211                                     ;PROGRAM LOCATION " COMMAND " CONTAINS THE COMMAND TO BE ISSUED VIA THE LCD IOT
212                                     ;
213                                     ;WRITE (4), WRITE DELETED DATA (14), OR READ (6), OR EMPTY BUFFER (2)
214                                     ;
215  000334  000000                     COMMAND:        0               ; 4, 14, 6, OR 2 + (GO BIT 1 = 1)
216                                     ;
217                                     ;PROGRAM LOCATION " SECTOR " CONTAINS THE SECTOR ADDRESS (1 TO 32 OCTAL)
218                                     ;
219  000336  000000                     SECTOR: 0                       ; 1 TO 32 OCTAL
220                                     ;
221                                     ;PROGRAM LOCATION " TRACK " CONTAINS THE TRACK ADDRESS (0 TO 114 OCTAL)
222                                     ;
223  000340  000000                     TRACK:  0                       ; 0 TO 114 OCTAL
224                                     ;
225                                     ;PROGRAM EQUIVALENTS
226                                     ;
227          000040                     DONEBIT=40
228          040000                     INIT=40000
229          000342                     BUFFER=.
230          000542                             .=BUFFER+200
231          000001                             .END
232
```

Figure 3-9 Empty Buffer Example

```
111                                     ;THE FOLLOWING IS A PROGRAMMING EXAMPLE OF THE PROTOCOL REQUIRED TO
112                                     ;
113                                     ;FILL THE SECTOR BUFFER WITH 128 8-BIT BYTES
114                                     ;
115                                     ; NOTE: THE DATA TO FILL THE SECTOR BUFFER CAN BE ASSEMBLED IN CORE IN THE
116                                     ;       EVEN ADDRESSES BYTES OF 128 WORDS OR IN BOTH BYTES OF 64 WORDS
117                                     ;
118  000156  012767  177770  000142    FENTRY: MOV #-10, PTRY          ; 8 TRYS TO FILL THE SECTOR BUFFER
119  000164  012700  000342            SETUP:  MOV #BUFFER, R0         ; PROGRAMS DATA BUFFER
120  000170  016767  000140  176772            MOV COMMAND, RXCS       ; ISSUE THE COMMAND
121                                     ;
122                                     ;WAIT FOR A TRANSFER REQUEST FLAG BEFORE TRANSFERRING DATA FROM THE PROGRAMS
123                                     ;
124                                     ;DATA BUFFER TO THE RX01 SECTOR BUFFER
125                                     ;
126                                     ;WAIT FOR A DONE FLAT TO INDICATE THE COMPLETION OF THE FILL BUFFER COMMAND
127                                     ;
128                                     ;PRIOR TO TESTING THE ERROR FLAG
129                                     ;
130  000176  105767  176766            LOOP:   TSTB RXCS               ; TEST FOR TRANSFER REQUEST FLAG
131  000202  001414                            BEQ FILL                ; BEQ IF TRANSFER REQUEST FLAG SET
132  000204  032767  000040  176756            BIT #DONEBIT, RXCS      ; TEST FOR THE DONE FLAG
133  000212  001771                            BEQ LOOP                ; BEQ UNTIL THE DONE FLAG SETS
134                                     ;
135                                     ;THE DONE FLAG IS SET
136                                     ;
137                                     ;TEST FOR ANY ERRORS (ONLY ERROR POSSIBLE IS A PARITY ERROR)
138                                     ;
139  000214  005767  176750                    TST RXCS
140  000220  001001                            BNE 1$
141  000222  000000                            HALT                    ; NO ERRORS = OK = COMPLETE
142                                     ;
143                                     ;INCREMENT AND TEST THE PARITY ERROR RETRY PROGRAM LOCATION " PTRY "
144                                     ;
145                                     ;AND RETRY THE COMMAND UNTIL THE ERROR RECOVERS
146                                     ;
147                                     ;OR UNTIL THE PTRY COUNTER OVERFLOWS TO 0
148                                     ;
149  000224  005267  000076            1$:     INC PTRY
150  000230  001355                            BNE SETUP               ; RETRY TO FILL THE SECTOR BUFFER
151  000232  000000                            HALT                    ; HARD PARITY ERROR
152                                     ;
153                                     ;THE TRANSFER REQUEST FLAG IS SET
154                                     ;
155                                     ;TRANSFER DATA FROM THE PROGRAMS DATA BUFFER TO THE RX01 SECTOR BUFFER
156                                     ;
157  000234  113067  176732            FILL:   MOVB @(R0)+, RXDB       ; PROGRAMS DATA BUFFER IS 64 WORDS IN LENGTH
158  000240  000756                            BR LOOP
```

Figure 3-10 Fill Buffer Example

3.6 RESTRICTIONS AND PROGRAMMING PITFALLS

A set of restrictions and programming pitfalls for the RXV11 is presented below.

1. Depending on how much data handling is done by the program between sectors, the minimum interleave of two sectors may be used, but to be safe a three-sector interleave is recommended.

2. If an error occurs and the program executes a Read Error Register function (111), a parity error may occur for that command. The error status would not be for the error in which the Read Error Register function was originally required.

3. The DRV SEL RDY bit is present only at the time of a Read Status function (101) for both drives, and after an Initialize, depending on the status of drive 0.

4. It is not required to load the Drive Select bit into the RXCS when the command is Fill Buffer (000) or Empty Buffer (010).

5. Sector Addressing: 1–26 *(No sector 0)*
   Track Addressing: 0–76

6. A power failure causing the recalibration of the drives will result in a Done condition, the same as finishing the reading of a sector. However, during a power failure, RXES bit 2 (Initialize Done) will set. Checking this bit will indicate a power fail condition.

7. Excessive usage of the Read Status function (101) will result in drastically decreased throughput, because a Read Status function requires between one and two diskette revolutions or about 250 ms to complete.

3.7 ERROR RECOVERY

There are two error indications given by the RXV11 system. The Read Status function (Paragraph 3.4.5) will assemble the current contents of the RXES (Paragraph 3.3.2.4), which can be sampled to determine errors. The Read Error Register function (Paragraph 3.4.7) can also be used to retrieve explicit error information from the RXER.

A list of error codes associated with the RXER is shown in Figure 3-7.

NOTE

A Read Status function is not necessary if the DRV RDY bit is not going to be interrogated, because the RXES is in the Interface register at the completion of every function.

CHAPTER 4
TECHNICAL DESCRIPTION

4.1 GENERAL

This chapter contains a description of the hardware comprising the RXV11 Floppy Disk System. An overall system block description covers all hardware components in the RXV11 option. A detailed description is included for the RXV11 interface module only. Refer to the *RX01/RX8/RX11 Floppy Disk System Maintenance Manual* for detailed descriptions of hardware contained in the RX01 floppy disk drive.

4.2 RXV11 SYSTEM BLOCK DIAGRAM

The RXV11 Floppy Disk System consists of four elements (Figure 4-1):

1. Drive mechanics, which includes actuators and transducers (up to two per controller).
2. Read/write electronics, which interfaces drive mechanics to the μCPU controller.
3. μCPU controller, which includes all control logic.
4. RXV11 interface, which interfaces the LSI-11 I/O bus to the RX01.

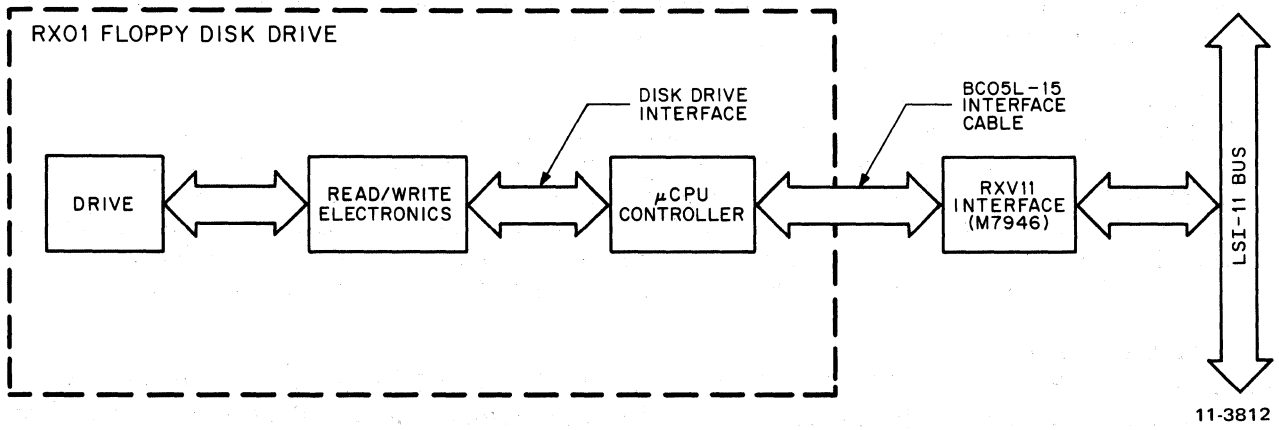


Figure 4-1 RXV11 System Block Diagram

There are three levels of data transmission in the floppy disk system (Figure 4-1):

1. The LSI-11 I/O bus for data transmission between the RXV11 interface module and the LSI-11 processor module.

2. The RX01 data bus for data transmission between the RX01 μCPU controller and the RXV11 interface module (BC05L-15 interface cable).

3. The disk drive interface for data and control information transmission between the read/write electronics and the RX01 μCPU controller.

In addition to the data transmission signals, analog signals between the read/write electronics and mechanical drive control head motion and sense diskette speed and position.

4.3 RX01/M7946 INTERFACE SIGNALS

Connector J1 on the RXV11 interface module (M7946) provides the interface for the following RX01 signals:

RX INIT L
The RX01 responds to RX INIT L by negating DONE L and moving the head position mechanism of both drives (if two are available) to track zero. The RX01 will also read sector 1 of track one of drive zero and then assert RX DONE L (without error) to indicate successful completion of the Initialize function.

RX DONE L
The RX01 asserts RX DONE L to indicate that no RX01 function is in progress. Initiating any function will cause RX DONE L to go false for the duration of that function. Attempting to initiate any function other than Initialize while RX DONE L is false is illegal and may result in an error.

RX RUN L
The RXV11 interface asserts RX RUN L to initiate command or data transfers between the interface module and the RX01 μCPU controller. If asserted when RX DONE L is asserted, the byte transferred from the RXV11 interface module to the RX01 is treated as a command. If asserted while RX DONE L is negated, a command is being executed and the byte transferred is considered to be read or write data, sector or track address, or error and status information.

RX OUT L
The RX01 μCPU controller controls this signal to inform the RXV11 interface module of the direction in which it is prepared to transfer a byte. When asserted (low), the direction of serial data transmission is from the RX01 to the RXV11 interface module. When not asserted (high), serial data transmission is from the RXV11 interface module to the RX01. RX OUT L is never asserted when RX DONE L is asserted; when RX DONE L is asserted, the transfer is a command byte from the RXV11 interface module to the RX01. RX INIT L, when asserted, causes RX OUT L to become negated.

RX TRANS REQ L
RX TRANS REQ L, used with RX RUN L and RX OUT L signals, comprise the basic control signal interface between the RX01 and the RXV11 interface module. The RX01 asserts this signal after receiving a new command to indicate that it is ready to receive an address or data byte, or it is ready to output an error status byte or data to the RXV11 interface. Note that this signal is not asserted to initiate a command byte; it is asserted by the RX01 to request transfer of each non-command byte during the execution of a command.

RX DATA L
RX DATA L is the bidirectional serial data line over which all command and data bytes are transferred.

RX SHIFT L
RX SHIFT L is a series of pulses generated by the RX01 which serially shift commands and data into or out of the RXV11 interface module. Pulse width is 200 ns (nominal); pulses occur at 1 μs intervals (nominal).

RX ERROR L
The RX01 asserts this signal when an error is detected. An error results in the RX01 sending RXES information to the RXV11 interface and aborting the present operation; RX DONE L is then asserted. This signal is cleared either by the RXV11 interface asserting RX INIT L or by sending a new command to the RX01.

8/12 BITS L
Not used in RXV11 systems; terminated in RX01.

4.4 INTERFACE MODULE LOGIC FUNCTIONS

4.4.1 General
RXV11 Interface logic functions are contained on a single 5 × 8.5 × 0.5 in. module. The module can be installed in any option location in the LSI-11 bus-structured backplane. All command and data transfers between the LSI-11 processor and the RXV11 are executed under program control via this module. Figure 4-2 is a block diagram illustrating the logic functions which comprise the M7946 module.

The M7946 interfaces with the LSI-11 bus via bus receivers, bus drivers, and bus transceivers.

4.4.2 Address Decoding Logic
Address decoding occurs on the leading edge of BSYNC L assertion. SYNC H clocks address decoding logic to produce an active or passive ME H signal. The ME H signal is a result of comparing DAL REC 2–12 H bits to the address configured on address jumpers W7–W17 at SYNC H time. When the RXV11's address is decoded, ME H goes active, enabling an RXV11/LSI-11 bus data or command transfer. Note that address bit DAL REC 1 H is applied to I/O control logic; this bit is used in selecting either Command/Status (CS) or Data Buffer (DB) data transfers.

4.4.3 I/O Control Logic
I/O control logic circuits control the actual command, status, or read/write data transfer between the LSI-11 Bus and the addressed RXV11 register. Control signals CS H and DB H are generated by this logic function in response to address bit DAL REC 1 H to select either the RXCS or RXDB register. The actual signal sequence for LSI-11 Bus cycle operations involving this function are as described in the *LSI-11, PDP-11/03 User's Manual,* Chapter 3.

4.4.4 RX Data Buffer (RXDB) Register
The RXDB is the main command/data interface function on the M7946 module. It is an 8-bit parallel load, parallel read shift register. Parallel load occurs during DATO bus cycle execution; RX BUSY H loads command or write data bits present on DAL REC 0–7 H into the shift register. BSHIFT L pulses then serially shift the command or data byte bits out of RXDB bit D07 L, and into the serial bus interface and parity logic. Serial command/data and parity bits are then shifted to the RX01 via the bidirectional RX DATA L signal.

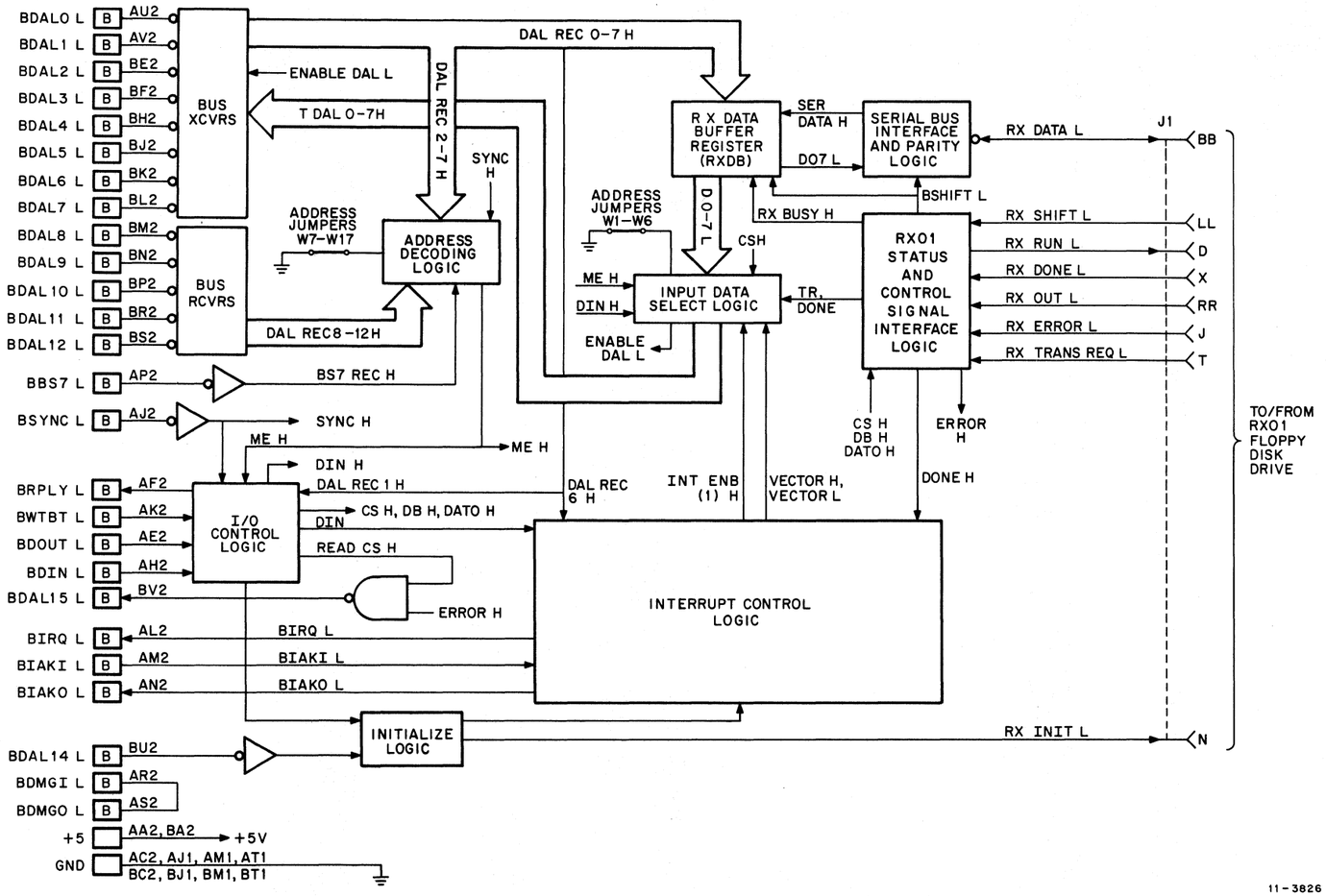


Figure 4-2 RXV11 Interface Module (M7946) Logic Block Diagram

During a data read operation, the process is reversed. RX01 serial data bits are received via the RX DATA L signal, serial bus interface and parity logic, and shifted into the RXDB via SER DATA H. Once the data byte is available, a DATI bus cycle can be initiated. Parallel read data bits D0–7 L are gated through input data select logic and routed over TDAL 0–7 H to bus transceivers which place the read data onto BDAL 0–7 L.

4.4.5 RX Command/Status (RXCS) Register

The RXCS function is actually not a register. It is a group of command/status bits which are program-accessible via a register address. Only ten of the sixteen RXCS bits are used. Six are write-only bits, three are read-only bits, and one is a read/write bit. During a RXCS read operation, CS H and READ CS H go high, enabling the status of ERROR H, TR, INT ENB (1) H, and DONE bits onto BDAL 15 L, BDAL 7 L, BDAL 6 L, and BDAL 5 L, respectively. Note that input data select logic routes bits 5, 6, and 7 as during the RXDB read operation.

During a RXCS write operation, either a command (contained in RXCS bits 1–3) is being transmitted to the RX01, interrupts are being enabled or disabled (RXCS bit 6 set or reset), or the RXV11 is being initialized (RXCS bit 14 is set). RXCS bit 0 (Go bit) is a logical 1 during a RXCS write operation when a command transfer is being executed. This causes the RXDB to parallel-load the command byte and serially transmit it to the RX01, as previously described for a data write operation. When RXCS bit 0 is a logical 0 during a RXCS write operation, the command bits are not transmitted to the RX01. Instead, the RXV11 is either being initialized (RXCS bit 14 = 1) or the INT ENB (RXCS bit 6) bit is being set or reset.

4.4.6 RX01 Status and Control Signal Interface Logic

RX01 status and control signal interface logic is the control interface between the RX01 and the RXV11 interface logic. All control and timing signals required for command or status transfers between the RXV11 interface and the RX01 directly involve this logic function. TR, DONE, and ERROR RXCS signals are produced by this logic function.

4.4.7 Interrupt Control Logic

The interrupt control logic function contains the Interrupt Enable flip-flop (RXCS bit 6). When set, the circuit requests interrupt service when the DONE H signal goes active. The interrupt sequence is initiated by the logic when it asserts BIRQ L. The processor responds by asserting BIAKI L and BDIN L, causing VECTOR H and VECTOR L to go to their respective active states. VECTOR H and VECTOR L cause input data select logic to enable the vector address, configured by jumpers W1–W6, onto the BDAL bus. The actual sequence of operations for interrupt operation is described in the *LSI-11, PDP-11/03 User's Manual,* Chapter 3.

4.4.8 Initialize Logic

Initialize logic is activated whenever a DATO cycle is executed with the RXCS and BDAL 14 L is asserted. This is equivalent to writing a logical 1 into RXCS bit 14. The logic responds by generating an active RX INIT L signal (pulse) which initializes the RX01 floppy disk drive. RX INIT L only remains active for the duration of the bus cycle.

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