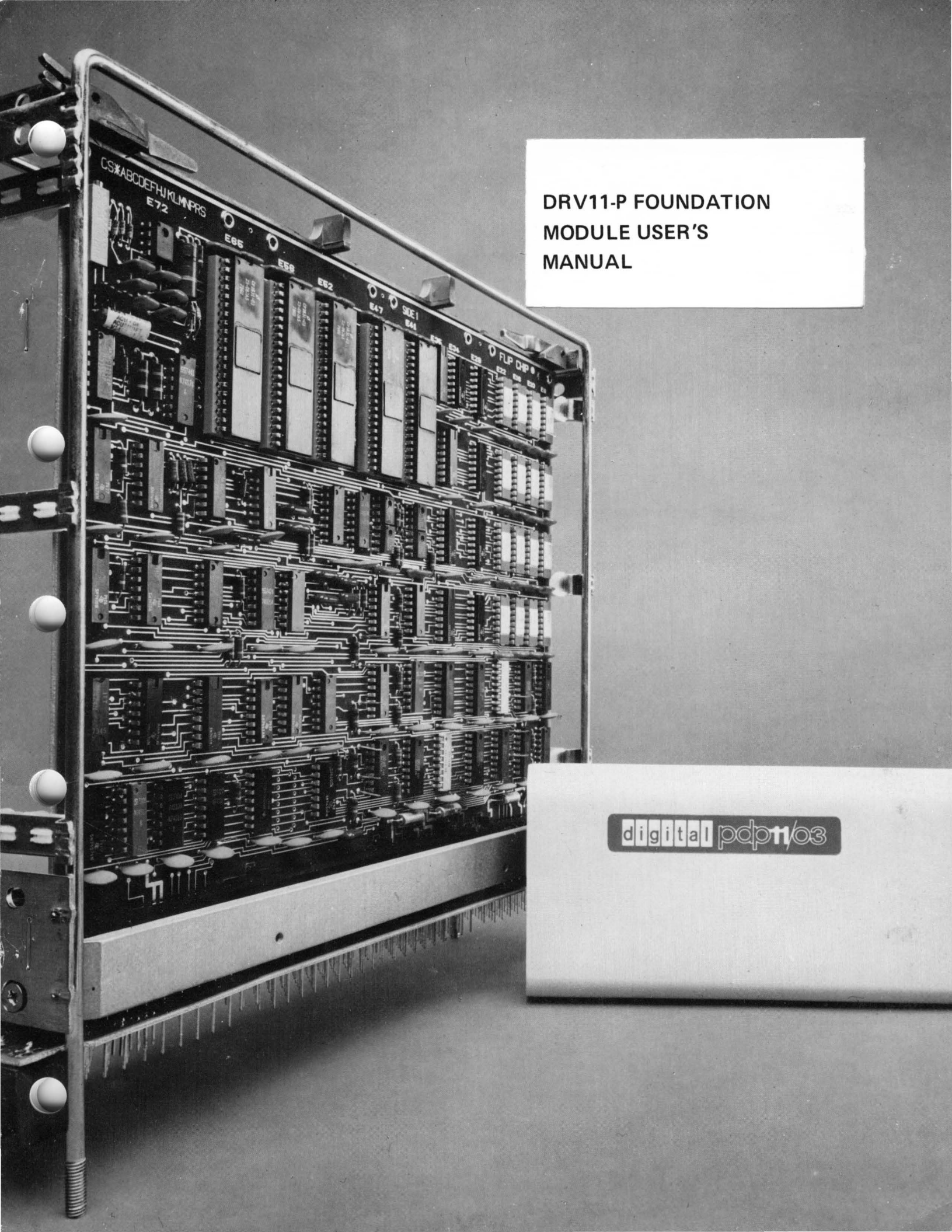
DRV11-P FOUNDATION
MODULE USER'S
MANUAL
digital pdp11/03

EK-DRV11-OP-002

DRV11-P FOUNDATION MODULE USER'S MANUAL

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INTRODUCTION

The DRV11-P is an LSI-11 bus compatible foundation wire-wrap interface module. Approximately one-quarter of the module is occupied by bus transceivers, vector address generator logic, device address comparator logic, protocol logic, and interrupt logic, as well as a 40-pin I/O connector. The remaining three-quarters of the module are for user application and has plated-through holes to accept IC's, and wire-wrap pins (WP) for interconnecting the user's circuits. The plated-through holes can accept 6, 8, 14, 16, 18, 20, 22, 24, and 40-pin dual-in-line IC's or IC sockets in various mounting areas of the module, or discrete components can be inserted into the plated-through holes. DRV11-P is a quad height, extended length, single width module which can be inserted into any one of the available interface option locations of any LSI-11 or PDP-11/03 backplane. The module occupies four backplane slots. A basic block diagram illustrating the DRV11-P LSI-11 bus interface logic is shown in Figure 1.

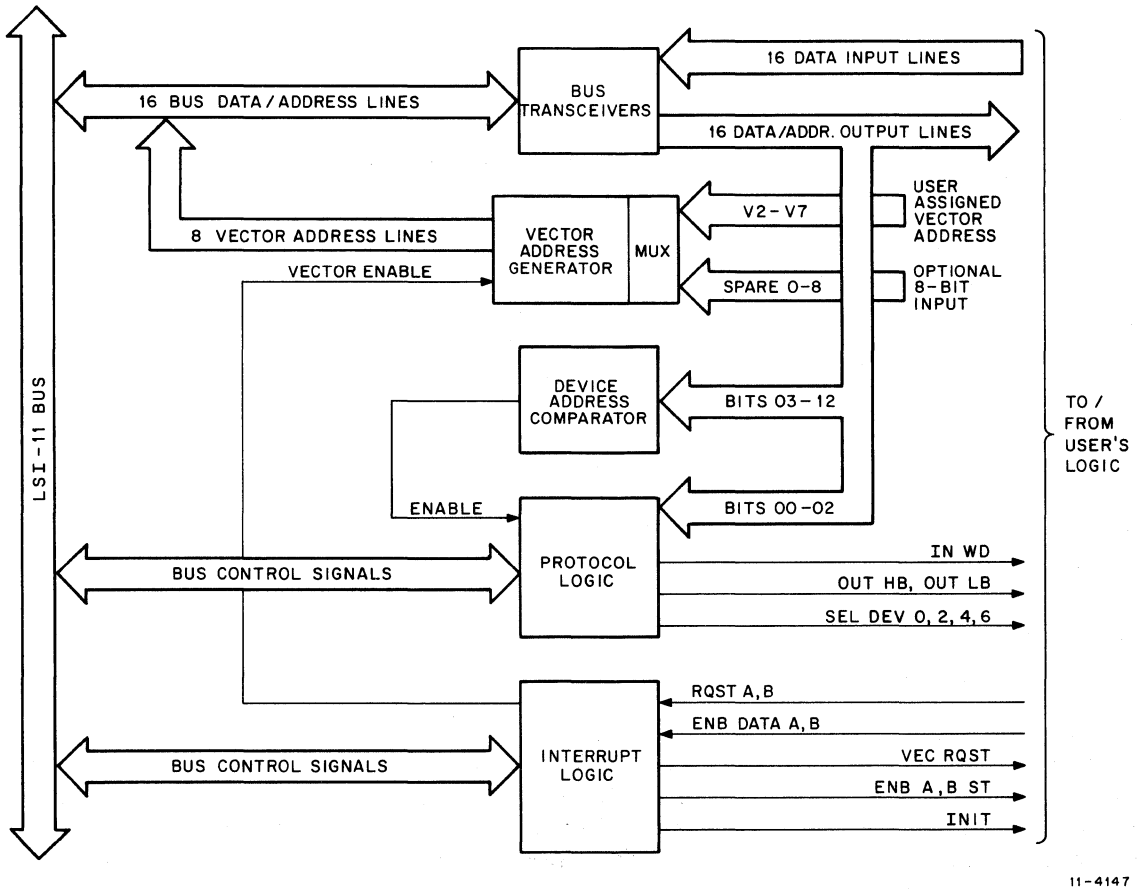

Figure 1 DRV11-P Basic Block Diagram

SPECIFICATIONS

The following specifications and particulars are for informational purposes only and are subject to change without notice.

Physical

Quad-height, extended length, single-width module

Dimensions

10.5 in. H, 8.5 in. L, 0.5 in. W (26.67 cm H, 21.59 cm L, 1.27 cm W)

User IC Capacity

Maximum IC density for all user areas is approximately 50 ICs, depending on IC types (see text for particulars).

Weight

12 oz. (340 gr.)

Electrical

Bus Loading

DRV11-P presents a maximum of one LSI-11 bus load to the bus.

User Lines

All user lines available at wire-wrap pins are TTL compatible; logic levels are as follows:

Inputs – High = 1 = 2.0V min.
Low = 0 = 0.8V max.

Outputs – High = 1 = 2.4V min.
Low = 0 = 0.4V max.

Bus Lines

All user bus lines available at wire-wrap pins have logic levels as follows:

Inputs – High = 1 = 1.7V min.
Low = 0 = 1.3V max.

Outputs – High = 1 = 2.0V min.
Low = 0 = 0.8V max.

Logic Power Requirements

+5V @ 1.0 A (max.) not including user logic.

Environmental

Temperature

Storage: -40° to 66° C (-40° to 150° F)
Operating: 5° to 50° C (41° to 122° F)

Relative Humidity

10% to 95% non-condensing

FUNCTIONAL DESCRIPTION

The DRV11-P is supplied with the logic necessary for interfacing to the LSI-11 bus. This logic includes bus transceivers, a device address comparator, protocol logic, interrupt logic, vector address comparator, and bus receivers and inverters. Figure 2 shows the inter-relationship between the aforementioned logic functions and the user's wire-wrap pins. A brief description of each logic function is provided in the following paragraphs.

Bus Transceivers

Referring to Figure 2, sheet 1, data output lines D00 through D15 reflect the state of the bus BDAL lines and will contain address and data information for any bus transfer, regardless of the device involved. Output data is usually clocked into a register for use by the interface or a peripheral since the length of time that the data is available on the bus during the bus cycle is very short. The device address comparator and the protocol logic determine if the data currently on the D00-D15 lines is intended for the DRV11-P.

Input data present at the IN00-IN15 lines will be applied to the bus when the TRANS ENB A, B, C, and D lines are asserted low. These lines are asserted by the protocol logic to gate data onto the bus at

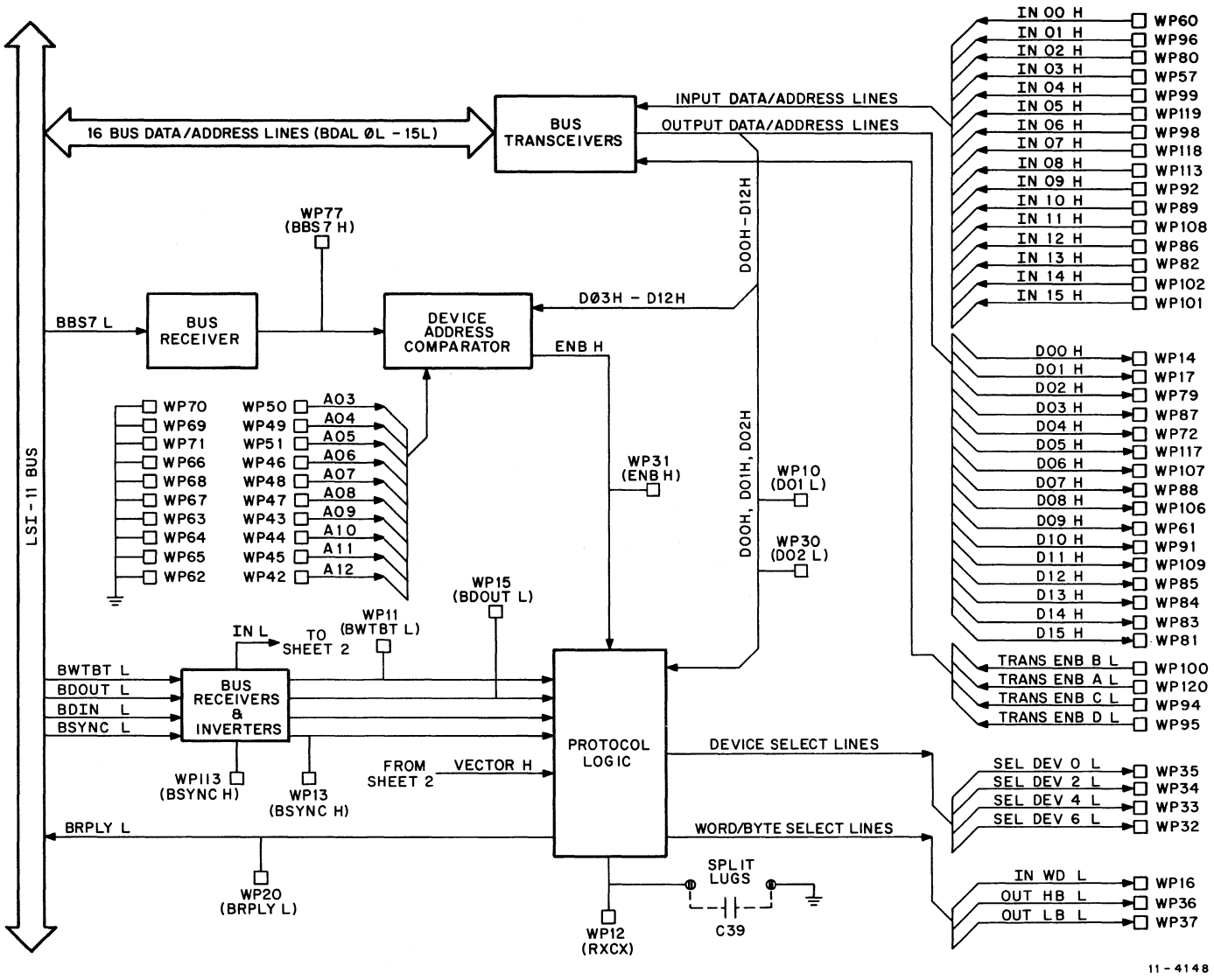

Figure 2 DRV11-P Block Diagram (Bus Transceivers, Device Address Comparator, and Protocol Logic) (Sheet 1 of 2)

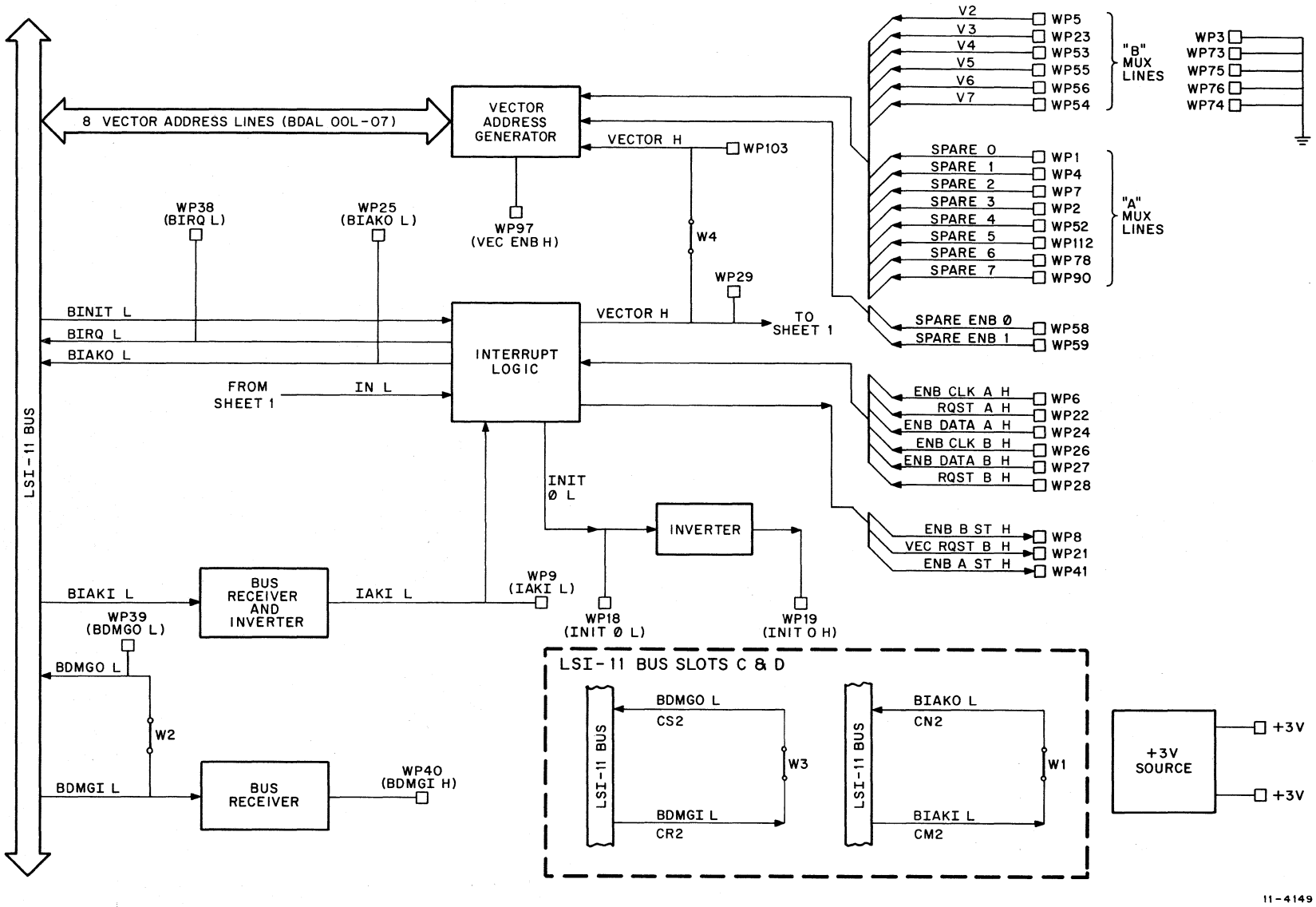

Figure 2 DRV11-P Block Diagram (Vector Address Generator and Interrupt Logic)
(Sheet 2 of 2)

the proper time during a bus cycle when addressed by the processor. The SEL DEV and IN WD lines would be driven by the protocol logic to select a user's register. The bus transceivers consist of four type 8641 ICs. (User wire-wrap pins (WP) for interconnecting the bus transceivers to the user's circuits are listed and defined in Table 2.)

Device Address Comparator

The device address comparator (Figure 2, sheet 1) receives address bits D03H - D12H from the bus transceivers and compares these bits to the device address assignment bits (A03 - A12) wired by the user on the DRV11-P module. If the two addresses compare, an ENB H signal is applied to the protocol logic. The device address comparator logic is designed around two type 8136 ICs. The user's device address is selected by means of wire-wrap pins. Wire-wrapping a device address pin to a ground pin makes that device address bit a "zero." Device address bits which are to be "ones" are left unwrapped. These bits will be pulled-up to +5V ("one" state) via resistors on the module. (Wire-wrap pins (WP) for device address selection are listed and defined in Table 2.)

Device Address Selection

The DRV11-P will respond to up to four consecutive addresses in the bank 7 area (addresses between 160000_8 and 177776_8). The register addresses are sequential by even numbers and are as follows:

Register	BBS7	Octal Address
1	1	1xxxx0
2	1	1xxxx2
3	1	1xxxx4
4	1	1xxxx6

The user selects a base address ending in zero for assignment to the first register by means of wire-wrap pins on the DRV11-P module. The module decodes this base address and the remaining register addresses are then properly decoded by the DRV11-P as they are received from the LSI-11 processor.

Figure 3 shows the address select format and presents the wire-wrap pin-to-bit relationship for device address selection. Bits to be decoded as "ZERO" bits in the base address are wire-wrapped to ground wire-wrap pins (WP). Bits to be decoded as "ONE" bits are left unwrapped as these bits are pulled up to the one state.

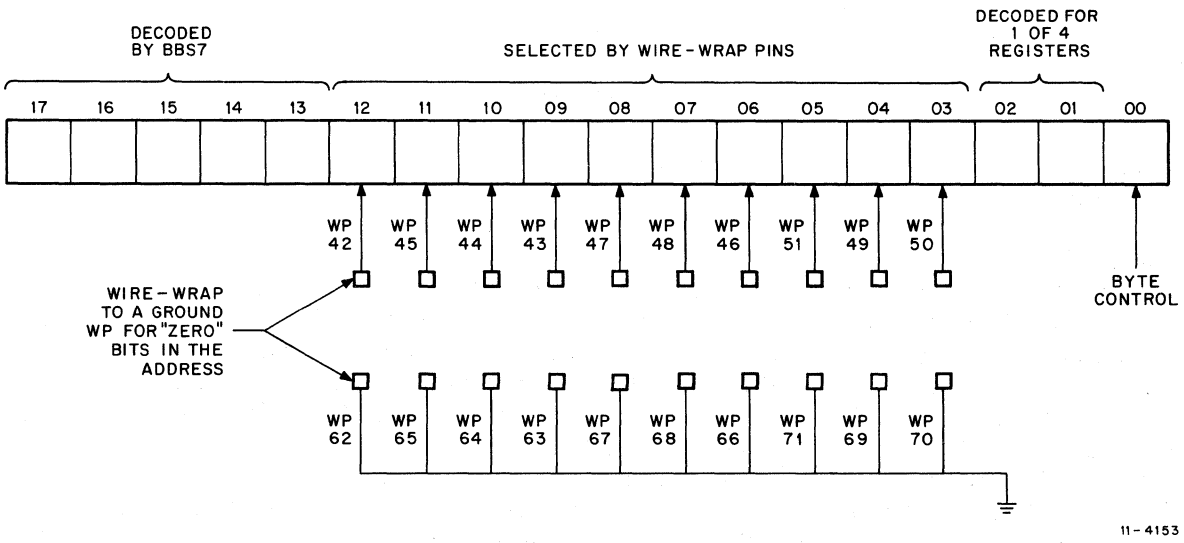

Figure 3 DRV11-P Device Address Select Format

Protocol Logic

The protocol logic (Figure 2, sheet 1) functions as a register selector, providing the signals necessary to control data flow into and out of up to four user word registers (8 bytes). Designed around a special DEC IC (DC004), the protocol logic operates as follows: when the proper device address has been decoded by the device address comparator ENB H goes high, and is applied to a latch in the protocol logic. Address bits D01 H and D02 H are decoded by the protocol logic producing one of the SEL DEV outputs, while bit D00 H and BWTBT are decoded for output word/byte selection (OUT HB L, OUT LB L). The device select lines (SEL DEV 0L, 2L, 4L, 6L) and word/byte select lines (IN WD L, OUT HB L, OUT LB L) are for user application and are available at wire-wrap pins (WP). Table 2 lists and defines the wire-wrap pins associated with the protocol logic. Generally, each DEV SEL output is used to select one of four user's registers, and the word/byte lines are used to determine the type of transfer (word or byte) to or from these registers. The active state of the user's lines from the protocol logic is a low assertion and the lines are TTL compatible. The DEV SEL lines can sink up to 20 mA. Split lugs are provided on the DRV11-P to accommodate C39. This capacitor may be installed by the user to vary the delay between BDIN L, BDOUT L, and VECTOR H inputs and the BRPLY output. Additional information on the DC004 protocol logic IC is contained in the Appendix.

The BRPLY L signal is normally issued within 85 ns (max.) of receiving either BDIN L or BDOUT L, depending on the bus cycle. If the user's interface requires more time before ending the bus cycle, the BRPLY L signal can be delayed up to a maximum of 10 μs by adding capacitor C39 across the split lugs in the BRPLY delay circuit. The amount of capacitance required for various delays is given in Table 1.

Table 1 C39 R-C Delays for BRPLY

Resistor (Constant)	Capacitance (C39 option)	*Delay (Typical)
680 ohms	0 pf	50 NS
680 ohms	100 pf	75 NS
680 ohms	120 pf	80 NS
680 ohms	470 pf	165 NS
680 ohms	560 pf	185 NS
680 ohms	680 pf	210 NS
680 ohms	1200 pf	340 NS

*Typical BRPLY Delay with respect to BDOUT and BDIN.

The BRPLY L signal is issued as the result of a signal on the VECTOR H input. This is used when giving a vector address during an interrupting process.

Interrupt Logic

The interrupt logic (Figure 2, sheet 2) performs an interrupt transaction that uses the "pass-the-pulse" type arbitration scheme to assign priorities to peripheral devices. The DRV11-P interrupt logic has two channels (A and B) for generating two interrupt requests. Channel A has higher priority than Channel B. If a user's device wants control of the LSI-11 bus, the interrupt enable flip-flop within the interrupt logic must first be set. This is accomplished by asserting (logic 1) the ENB DATA line and then clocking the enable flip-flop by asserting (positive transition) the ENB CLK line. With the interrupt enable flip-flop set, the user's device may then make a bus request by asserting (logic 1) RQST. When RQST is asserted, and if the interrupt enable flip-flop is set, the interrupt logic asserts (logic 0) BIRQ L, thus making a bus request. When the request is granted, the processor asserts (logic 0) BDIN L

(Figure 2, sheet 1) which is applied to the interrupt logic as IN L (Figure 2, sheet 2). IN L causes the interrupt logic to assert (logic 1) VECTOR H which is applied to the vector address generator. A vector address is thus placed on the LSI-11 bus to indicate the starting address of the service routine for the user's device which made the bus request.

As mentioned previously, two interrupt request channels (A and B) are contained within the interrupt logic. These channels can be used to service two user devices. However, because channel A has a higher priority than channel B, fast peripheral devices which cannot recover data if not serviced promptly should use channel A.

There are three status lines from the DRV11-P interrupt logic available to the user. These are: (1) ENB B ST H, (2) ENB A ST H, and (3) VEC RQST B H. ENB B ST H and ENB A ST H indicate the status of the interrupt logic interrupt enable flip-flops. Each line is asserted (logic 1) when the appropriate enable flip-flop is set. The VEC RQST B line is asserted (logic 1) when the user's device connected to channel B has been granted use of the bus. When VEC RQST B is unasserted (logic 0) and VECTOR H is asserted, the user's device connected to channel A of the interrupt logic has been granted use of the bus. These status lines can function as part of the user's control and status register (CSR) which can be constructed on the DRV11-P module. Additionally, the INIT 0 and INIT 0 H outputs from the interrupt logic can be used to initialize the user's logic. Additional information on the special DEC interrupt IC (DC003) is contained in the Appendix.

All user's input and output lines for the DRV11-P interrupt logic are TTL compatible. Wire-wrap pins (WP) for input and output lines are listed and defined in Table 2.

Vector Address Generator

The vector address generator (Figure 2, sheet 2) produces a vector address which indicates the starting location in memory where a service routine is stored for the user's device requesting interrupt service. The vector address is selected by the user by means of wire-wrap pins (WP) on the DRV11-P. Vector address bits V3 through V7 are hard-wired by the user for either logic ones or zeros. Wire-wrapping a vector address pin to a ground pin makes that vector address bit a "ZERO." Vector address bits which are to be "ONES" are left unwrapped. These bits will be pulled-up to +5V ("one" state) via resistors on the DRV11-P. When VECTOR H from the interrupt logic goes high (logic 1), eight vector address bits are gated onto the LSI-11 bus. It should be noted that the user can generally select the state of only six of the eight vector address bits. The remaining bits, V00 and V01 are preset by the DRV11-P vector address generator. With this arrangement, the user can select a vector address in the normal user range of 000_8 to 374_8. However, by adding one gate to the vector address generator encode logic, the user can accommodate nine bits in the vector address and thus extend the addressing to 774_8.

The vector address generator is primarily designed around two type 74157 multiplexer ICs. Each 74157 has two separate four-bit inputs which are multiplexed. Thus, both 74157s can accommodate two 8-bit bytes, one of which is used for vector addressing. This leaves one spare 8-bit input for user application. The SPARE input can be used to gate onto the bus the lower byte of the user's CSR on the DRV11-P. The data on the SPARE input can be gated to the LSI-11 bus by driving both SPARE ENB 0 and SPARE ENB 1 inputs low (logic 0). This is best accomplished by using one of the SEL DEV lines from the protocol logic (Figure 2, sheet 1) along with the IN WD line. However, the actual use of the SPARE inputs is at the user's discretion, but SPARE ENB 0 and SPARE ENB 1 should not be permanently held low as this could affect vector addressing. If not used, these inputs should be connected to the +3V source.

All user input lines to the vector address generator are TTL compatible. These lines and their associated wire-wrap pins (WP) are listed and defined in Table 2.

Table 2 User Wire-Wrap Pins

Wire-Wrap Pin	Mnemonic	Function
WP1	SPARE 0	Spare input to the vector address multiplexer. This input can be used to read part of a control/status register.
WP2	SPARE 3	See WP1.
WP3		Ground for vector address bit V3. See WP23.
WP4	SPARE 1	See WP1.
WP5	V2	Vector address bit 02.
WP6	ENB CLK A H	ENB CLK A H is the clock input to the Enable A Flip-Flop of the A interrupt logic. When ENB CLK A H goes high, ENB DATA A is clocked into the Enable A Flip-Flop.
WP7	SPARE 2	See WP1.
WP8	ENB B ST H	ENB B ST H is the status output from the Enable B Flip-Flop of the B interrupt logic. When ENB B ST H is high, the Enable B Flip-Flop is set.
WP9	IAKI L	Test point for the BIAK I bus signal. BIAKI L is the processor's response to BIRQ L and is daisy-chained such that the first requesting device blocks the signal propagation. Nonrequesting devices pass the signal on as BIAKO L. The leading edge of BIAKI L causes BIRQ L to be unasserted by the requesting device.
WP10	D01 L	Test point for data/address bit one. Useful when testing the protocol logic. D01 is latched in the protocol logic at the asserted edge of BSYNC L. D01 and D02 are decoded to produce the SEL DEV outputs.

Table 2 User Wire-Wrap Pins (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP11	BWTBT L	Test point for the BWTBT bus signal, while BDOUT L is asserted, BWTBT L indicates a byte or word operation: BWTBT L asserted indicates byte operation; BWTBT L unasserted indicates word operation. BWTBT L decoded with BDOUT L and BDAL 0 L forms OUT LB L or OUT HB L.
WP12	R_X C_X	Test point for monitoring the delay of BRPLY.
WP13	BSYNC H	Test point for the BSYNC L bus signal. BSYNC L indicates that the address is valid. At the assertion of BSYNC L, address information is trapped in four latches. While unasserted, disables all outputs except the vector term of BRPLY L. BSYNC L is held throughout the entire bus cycle.
WP14	D00 H	One of 16 data or address lines from the transceivers for user applications. Address bit 00 is used for byte selection: 0 = low byte; 1 = high byte.
WP15	BDOUT L	Test point for the BDOUT L bus signal. BDOUT is a strobe signal to effect a data output transaction. BDOUT L is decoded with BWTBT L and BDAL0 to form OUT LB L and OUT HB L. BDOUT L also causes BRPLY L to be issued through the delay circuit.
WP16	IN WD L	In Word (IN WD) is used to gate input data from a selected register onto the LSI-11 bus. Enabled by BSYNC L and strobed by BDIN L.
WP17	D01 H	One of 16 data or address lines from the transceivers for user applications.
WP18	INIT 0 L	An initialize signal (asserted low) for user applications.
WP19	INIT 0 H	An initialize signal (asserted high) for user applications.

Table 2 User Wire-Wrap (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP20	BRPLY L	Test point for the BRPLY L bus signal. BRPLY L is generated by VECTOR H (vector term), or by BSYNC and ENB in combination with either BDIN L, or BDOUT L. Capacitor C37 can be added by the user to extend the delay.
WP21	VEC RQST B H	Used to distinguish whether device A or device B is making a request. VECT RQST B H is asserted for device B requests and unasserted for device A requests.
WP22	RQST A H	When RQST A H is asserted, the bus request flip-flop for device A in the interrupt logic is enabled, and BIRQ L becomes asserted if the interrupt enable flip-flop is set.
WP23	V3	Vector address bit 03. WP23 is used to select the state of vector address bit 03. When not wrapped to a ground pin, vector address bit 03 is a "one." When wrapped to WP3, vector address bit 03 is a "zero."
WP24	ENB DATA A H	Interrupt enable A data line. The level on this line, in conjunction with the ENB CLK A H (see WP6) line, determines the state of the A interrupt enable flip-flop within the interrupt logic.
WP25	BIAKO L	Test point for the BIAKO L bus signal. BIAKO L is the daisy-chained signal that is passed by all devices not requesting interrupt service (see WP9).
WP26	ENB CLK B H	ENB CLK B H is the clock input to the enable B flip-flop of the B interrupt logic. When ENB CLK B H goes high, ENB DATA B is clocked into the enable B flip-flop.
WP27	ENB DATA B H	Interrupt enable B data line. The level on this line, in conjunction with the ENB CLK B H (see WP26) lines, determines the state of the B interrupt enable flip-flop within the interrupt logic.

Table 2 User Wire-Wrap (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP28	RQST B H	When RQST B H is asserted, the bus request flip-flop for device B in the interrupt logic is enabled, and BIRQ L becomes asserted if the interrupt enable flip-flop is set.
WP29	VECTOR H	Test point for VECTOR H. This signal causes BRPLY L (vector term) to be generated through a delay independent of BSYNC L and ENB H. VECTOR H also gates the vector address onto the LSI-11 bus via the vector address generator.
WP30	D02 L	Test point for data/address bit two. Useful when testing the protocol logic. D02 is latched at the asserted edge of BSYNC L. D02 and D01 are decoded to produce the SEL DEV outputs.
WP31	ENB H	Test point for ENB H. This signal is the result of a compare between the device address on the LSI-11 bus and the device address established by the user. When the addresses compare, ENB H is asserted and sent to the protocol logic.
WP32	SEL DEV 6 L	One of four select signals that is true as a function of BDAL1 L and BDAL2 L if ENB H (see WP31) is asserted at the asserted edge of BSYNC L. The four select signals indicate that a user's register has been selected for a data transaction. The select signals remain asserted until BSYNC L becomes unasserted.
WP33	SEL DEV 4L	See WP32.
WP34	SEL DEV 2L	See WP32.
WP35	SEL DEV 0L	See WP32.
WP36	OUT LB L	Out Low Byte is used to load (write) data into the low byte of a selected user register. See WP37.

Table 2 User Wire-Wrap (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP37	OUT HB L	Out High Byte is used to load (write) data into the high byte of a selected user register. If used with OUT LB L, the higher, lower, or both bytes can be written. OUT HB L is enabled by BSYNC L and the decode of BWTBT L and BDAL0 L, and strobed by BDOUT L.
WP38	BIRQ L	Test point for the BIRQ L bus signal. This signal is asserted by a device needing interrupt service.
WP39	BDMGO L	This signal is generated by DMA devices as a result of arbitrating the BDMGI L line. Jumper W2 must be removed if the DRV11-P is to be used for DMA service.
WP40	BDMGI H	Used as a source for the BDMGI signal to drive the user's DMA request arbitration logic. See WP39.
WP41	ENB A ST H	ENB A ST H is the status output from the enable A flip-flop of the A interrupt logic. When ENB A ST H is high, the enable A flip-flop is set.
WP42	A12	Used to select the user's device address along with WP45, 44, 43, 47, 48, 46, 51, 49, 50. When not wrapped to a ground pin, the particular device address bit will be a "one." When wrapped to a ground pin (WP62 for bit A12), the particular bit will be a "zero."
WP43	A09	User's device address bit 09. The associated ground pin is WP63. See WP42.
WP44	A10	User's device address bit 10. The associated ground pin is WP64. See WP42.
WP45	A11	User's device address bit 11. The associated ground pin is WP65. See WP42.
WP46	A06	User's device address bit 06. The associated ground pin is WP66. See WP42.
WP47	A08	User's device address bit 08. The associated ground pin is WP67. See WP42.

Table 2 User Wire-Wrap (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP48	A07	User's device address bit 07. The associated ground pin is WP68. See WP42.
WP49	A04	User's device address bit 04. The associated ground pin is WP69. See WP42.
WP50	A03	User's device address bit 03. The associated ground pin is WP70. See WP42.
WP51	A05	User's device address bit 05. The associated ground pin is WP71. See WP42.
WP52	SPARE 4	See WP1.
WP53	V4	Vector address bit 03. The associated ground pin is WP73. See WP23.
WP54	V7	Vector address bit 07. The associated ground pin is WP74. See WP23.
WP55	V5	Vector address bit 05. The associated ground pin is WP75. See WP23.
WP56	V6	Vector address bit 06. The associated ground pin is WP76. See WP23.
WP57	IN03 H	One of 16 data or address lines to the transceivers for user applications.
WP58	SPARE ENB 0	SPARE ENB 0 and SPARE ENB 1 (WP59) both must be driven low to write data from SPARE inputs 0 through 7 to the LSI-11 bus via the transceiver. For 8-bit input applications, SPARE ENB 0 could be driven by one of the SEL DEV lines, while SPARE ENB 1 could be driven by IN WD L.
WP59	SPARE ENB 1	See WP58.
WP60	IN00 H	See WP57.
WP61	D09 H	See WP17.
WP62		Ground for user's device address bit A12. See WP42.
WP63		Ground for user's device address bit A09. See WP42.

Table 2 User Wire-Wrap (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP64		Ground for user's device address bit A10. See WP42.
WP65		Ground for user's device address bit A11. See WP42.
WP66		Ground for user's device address bit A06. See WP42.
WP67		Ground for user's device address bit A08. See WP42.
WP68		Ground for user's device address bit A07. See WP42.
WP69		Ground for user's device address bit A04. See WP42.
WP70		Ground for user's device address bit A03. See WP42.
WP71		Ground for user's device address bit A05. See WP42.
WP72	D04 H	See WP17.
WP73		Ground for vector address bit V4. See WP23.
WP74		Ground for vector address bit V5. See WP23.
WP75		Ground for vector address bit V6. See WP23.
WP76		Ground for vector address bit V7. See WP23.
WP77	BBS7 H	Test point for the Bank 7 Select (BBS7) bus signal. This line is asserted by the bus master when an address in the upper 4K bank (28-32K range) is placed on the LSI-11 bus.
WP78	SPARE 6	See WP1.
WP79	D02 H	See WP17.
WP80	IN 02 H	See WP57.

Table 2 User Wire-Wrap (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP81	D15 H	See WP17.
WP82	IN 13 H	See WP57.
WP83	D14 H	See WP17.
WP84	D13 H	See WP17.
WP85	D12 H	See WP17.
WP86	IN 12 H	See WP57.
WP87	D03 H	See WP17.
WP88	D07 H	See WP17.
WP89	IN 10 H	See WP57.
WP90	SPARE 7	See WP1.
WP91	D10 H	See WP17.
WP92	IN 09 H	See WP57.
WP93		NOT USED.
WP94	TRANS ENB C L	Enables user's data to be placed onto the LSI-11 bus. Both TRANS ENB C and A (WP94 and WP120) and TRANS ENB D and B (WP95 and WP100) must be driven low prior to the processor's read data time.
WP95	TRANS ENB D L	See WP94.
WP96	IN 01 H	See WP57.
WP97	VEC ENB H	Test point for VEC ENB H. This signal gates the vector address to the LSI-11 bus, provided that jumper W4 has not been removed. WP97 can be used as the source for VEC ENB H when adding an additional gate to the DRV11-P for vector address expansion up to 774_8.
WP98	IN 06 H	See WP57.
WP99	IN 04 H	See WP57.

Table 2 User Wire-Wrap (Cont)

Wire-Wrap Pin	Mnemonic	Function
WP100	TRANS ENB B L	See WP94.
WP101	IN 15 H	See WP57.
WP102	IN 14 H	See WP57.
WP103		Used to pull-up the VEC ENB H line when jumper W4 is removed.
WP104		NOT USED.
WP105		NOT USED.
WP106	D08 H	See WP17.
WP107	D06 H	See WP17.
WP108	IN 11 H	See WP57.
WP109	D11 H	See WP17.
WP110		NOT USED.
WP111		NOT USED.
WP112	SPARE 5	See WP1.
WP113	IN 08 H	See WP57.
WP114		NOT USED.
WP115	BSYNC H	Test point for BSYNC H. At the asserted edge of this signal, address information is trapped in four latches. BSYNC H is the inversion of BSYNC L. See WP13.
WP116		NOT USED.
WP117	D05 H	See WP17.
WP118	IN 07 H	See WP57.
WP119	IN 05 H	See WP57.
WP120	TRANS ENB A L	See WP94.
+3V		There are two +3V source wire-wrap pins on the DRV11-P. Each +3V source can drive up to 13 TTL unit loads. These sources can be used for pulling-up unused TTL inputs.

Vector Address Selection

Vector addresses 0-774_8 are reserved for users of the LSI-11 system. As manufactured, the DRV11-P can vector address in the range from 0-374_8. However, by adding one gate to the DRV11-P vector address logic, the user can extend the vector address to 774_8. The user selects the interrupt vector address by means of wire-wrap pins (WP) on the DRV11-P module.

Figure 4 shows the vector address select format and presents the wire-wrap pin-to-bit relationship for vector address selection. Bits to be decoded as "ZERO" bits in the vector address are wire-wrapped to ground wire-wrap pins (WP). Bits to be decoded as "ONE" bits are left unwrapped as these bits are pulled-up to the one state.

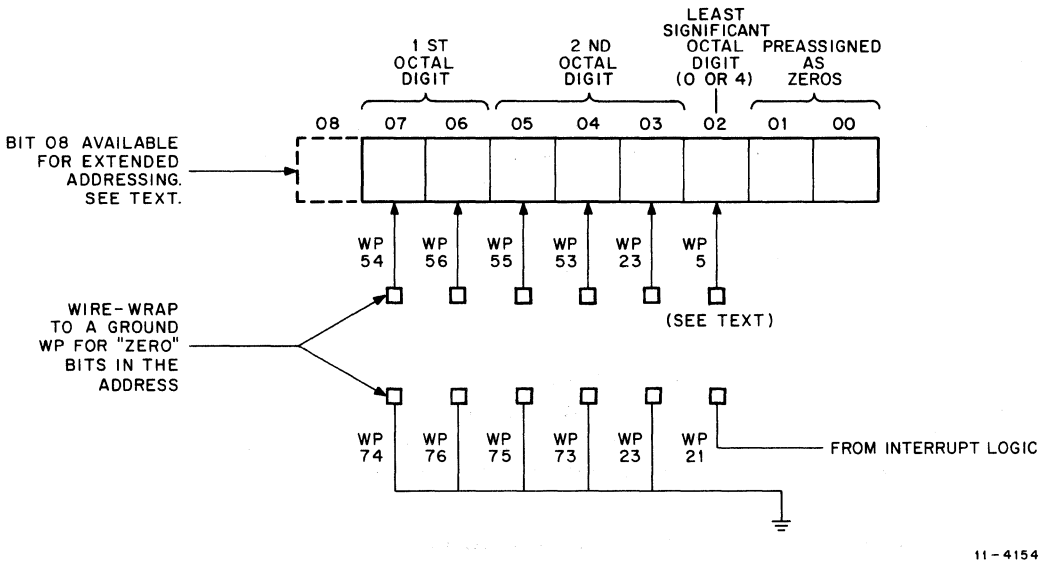

Figure 4 DRV11-P Vector Address Select Format

It is recommended that WP5 (vector bit 02) be wrapped to WP21 (VEC RQST B H). This will automatically decode the least significant bit of the vector address as a 0 or a 4. When the VECTOR H signal is issued as a result of the B half of the interrupt logic becoming bus master, the VEC RQST B H (WP5) signal is also issued changing bit 02 of the vector address, thus presenting a different vector address for interrupt B.

The VEC RQST B H line can be thought of as a one bit code indicating which half of the interrupt logic is bus master. When bit 02 of the vector address is a zero, the A half is bus master; a one indicates that the B half is master.

Bus Receivers

All LSI-11 bus data and control lines are fully buffered on the DRV11-P module. Buffering for the data and address lines (BDAL) is accomplished by the bus transceivers. Bus control lines (BWTBT, BDOUT, BDIN, BSYNC, BBSY, BIAKI, and BDMGI) are buffered on the DRV11-P with type 8640 bus receivers. These receivers are high impedance receivers with the following input levels:

High = 1.7V min.
Low = 1.3V max.

The receivers have standard TTL compatible outputs which are made available (for most bus signals) to the user by means of wire-wrap pins (WP). The bus signals and the associated wire-wrap pins for user application are listed and defined in Table 2.

+3V Source

There are two +3V wire-wrap pins (Figure 2, sheet 2) on the DRV11-P module. These pins provide a source of +3V for pulling-up unused TTL inputs. Each +3V source is capable of driving up to 13 TTL unit loads. The +3V sources are derived from resistor dividers placed across the +5V logic source.

USER I/O LINES AND ASSOCIATED WIRE-WRAP PINS (WP)

There are 112 user I/O lines and 122 wire-wrap pins (not counting the 40-pins for the I/O connector and the 70-pins for C and D module fingers) for user applications. A functional description of the user I/O lines was presented in the Functional Description paragraphs. All user I/O lines are TTL compatible and are listed and described in Table 2 along with the associated wire-wrap pin (WP). LSI-11 bus signals are not included. A description of the bus signals can be found in the LSI-11 PDP-11/03 User's Manual.

PHYSICAL DESCRIPTION

Figure 5 shows the physical layout of the DRV11-P. There are 12 vertical user areas for IC placement. User area "A" can accommodate ICs with pins on 0.3 in. (0.762 cm), 0.4 in. (1.01 cm), and 0.6 in. (1.52 cm) centers. This first area can be dedicated to any IC or IC sockets with the above mentioned pin centers, or a mixture of ICs with those pin centers can be installed.

User areas "B" through "L" and area "N" can accommodate ICs or IC Sockets with 0.3 in. (0.762 cm) pin centers. Whereas area "M" can accommodate ICs or IC Sockets with 0.3 in. (0.762 cm) and/or 0.4 in. (1.01 cm) pin centers.

As an aid to exact location of wire-wrap pins and IC connections, each vertical column is assigned an alphabetic designation and each horizontal row is assigned a numeric designation. A specific wire-wrap pin can be specified by referring to column A through L and row 1 through 64. In the same way, an IC connection can be specified by referring to column M through CC and row 1 through 31.

The maximum ICs which the DRV11-P can accommodate is listed in Table 3.

User areas "A," "B," "C," and "E" are equipped with a ground wire-pin (-) and a +5V wire-wrap pin (+) at both ends of each column of wire-wrap pins. These ground and +5V pins are to be used for supplying +5V and ground to the user's logic. The capacitors above (C36, C34, C32, C30, and C28) and below (C35, C33, C31, C29 and C27) the user areas provide decoupling for the +5V source.

Additional decoupling capacitors can be added by the user as required.

User areas "F" through "N" only have ground (-) and +5V (+) wire-wrap pins at the lower end of each column of wire-wrap pins. Capacitors C26 through C20 provide the +5V decoupling for these user areas.

A 40-pin connector is provided in the upper right of the DRV11-P module. This connector can be used as an I/O connector for interfacing to a user's I/O device. Each connector pin is brought to a wire-wrap pin on the module. Module wire-wrap pins are designated the same as the connector pins. Figure 5 shows the designations for all the connector wire-wrap pins. The actual module only has designations for pins A and UU. Three wire-wrap pins to the right of the 40-pin connector are ground pins and can be used for cable grounds.

Table 4 lists cables, available from Digital Equipment Corporation, which have 40-pin connectors that mate with J1 on the DRV11-P. Standard length cables are listed. Non-standard lengths may be ordered at additional cost. Contact the nearest Digital Equipment Corporation Sales Office for prices and availability. The desired cable length (xx) must be specified when ordering.

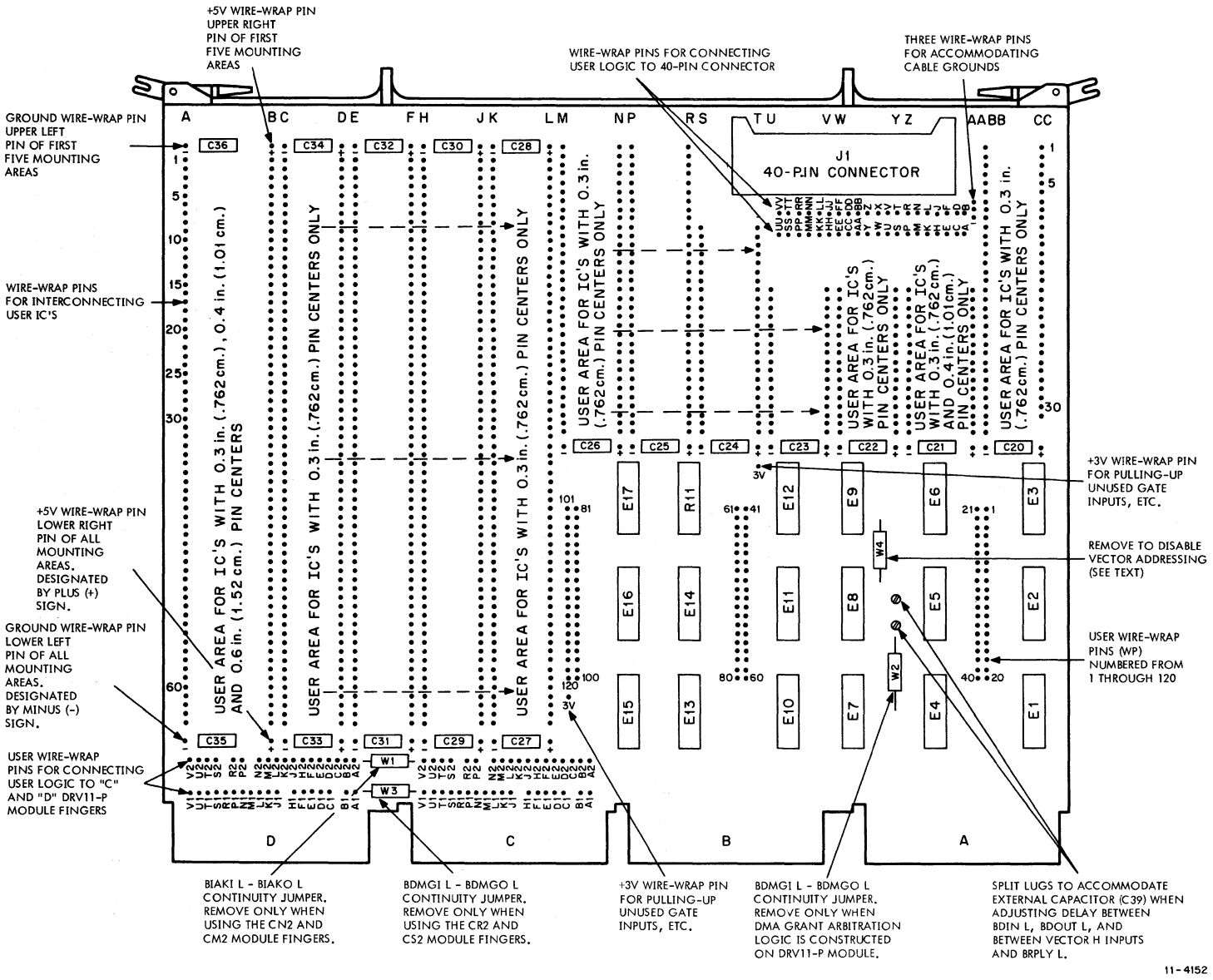

Figure 5 DRV11-P Physical Layout

Table 3 Maximum DRV11-P IC Density

(All Areas)

IC Type	Max. ICs
6 pin	122
8 pin	97
14 pin	61
16 pin	52
18 pin	44
20 pin	43
22 pin	6
24 pin	5
40 pin	3

Table 4 Recommended Cable Assemblies

Cable No.	Connectors	Type	Length (ft./m.)
BC07A-xx	H856 to open end	20-twisted pair	10, 15, 25 ft. 3.050, 4.575, 7.625 m.
BC07D-xx	H856 to open end	2, 20-conductor ribbon	10, 15, 25 ft. 3.050, 4.575, 7.625 m.
BC08R-xx	H856 to H856	Shielded flat	1, 6, 10, 12, 20, 50, 75, 100 ft. 0.305, 1.830, 3.050, 3.660, 6.100, 15.250, 22.875, 30.500 m.
BC04Z-xx	H856 to open end	Shielded flat	6, 10, 15, 25, 50 ft. 1.830, 3.050, 4.575, 7.625, 15.250 m.

In the lower right area of the module are the ICs which constitute the bus interface logic (as described in the Functional Description paragraphs) and the 122 user wire-wrap pins. These user wire-wrap pins are the sources for logic signals which are to be used to drive the user's logic circuits. All 122 wire-pins are listed and described in Table 2. Also contained in the lower right area are two split lugs. Capacitor C39 (not supplied with the DRV11-P) can be soldered across these lugs to vary the delay between BDIN L, BDOUT L, and between VECTOR H inputs and BRPLY L if the normal tolerance for this delay does not meet with the user's requirements (refer to Table 1 and the Protocol Logic paragraph).

Jumpers W2 and W4 are also contained in this area of the module. W2 provides BDMGI L and BDMGO L continuity for the LSI-11 bus. This jumper should be removed only if the user constructs a DMA (direct memory access) interface on the DRV11-P and DMA grant arbitration logic is included. W4 enables or disables vector addresses. With W4 installed, a vector address will automatically be placed onto the bus when an interrupt is generated. If W4 is removed and WP103 is wire-wrapped to a ground wire-wrap pin, the DRV11-P will interrupt but will not place a vector address onto the bus.

The last module area to be discussed is the area directly above module fingers C and D. This area contains jumpers W1 and W3. W1 should be removed only if the user constructs circuitry on the module which uses the BIAKO L (finger CN2) and BIAKI L (finger CM2) lines of the C and D bus slots. W3 should be removed if the BDMGO L (finger CS2) and BDMGI L (finger CR2) lines of the C and D bus slots are used. The balance of this area is dedicated to user wire-wrap pins for the C and D fingers. As indicated in Figure 5, these wire-wrap pins have a one-to-one correlation with the C and D module fingers.

All wire-wrap pins accept 30-gauge wire and there are two holes in the DRV11-P module which can be used for custom mounting of the module. One hole is in the approximate center of the module, while the second is to the left of the 40-pin connector.

MODULE INSTALLATION

With the exception of the first slot (the LSI-11 processor always occupies the first slot), the DRV11-P can be installed into any four slots of the LSI-11 backplane. However, if the DRV11-P is configured as a DMA module and if an REV11 DMA refresh option is used, the DRV11-P must be at a lower priority than the REV11. When inserting the module into the backplane, make sure that the deep notch on the module seats against the connector block rib. Do not insert or remove the module with power applied. Connect the user I/O cables to J1 on the DRV11-P.

WIRE-WRAP TOOLS

The wire-wrap pins (WP) used on the DRV11-P are sized for 30-gauge wire and wire-wrap accessories. Table 5 lists 30-gauge wire-wrap tools which can be purchased from Digital Equipment Corporation. Contact the nearest Digital Equipment Corporation Sales Office for prices and availability.

Table 5 Wire-Wrap Tools

Part No.	Description
H810-A	Pistol grip mechanical wire-wrap tool for 30-gauge wire.
H810-D	Battery powered wire-wrap gun for 30-gauge wire.
H811-A	Hand wire-wrap tool for 30-gauge wire.
H812-A	Hand unwrapping tool for 30-gauge wire.

DRV11-P PARTS LIST

Table 6 lists the parts supplied with the DRV11-P option by part number, description, and quantity.

RELATED LITERATURE

In addition to the data contained in this manual, the LSI-11 PDP-11/03 User's Manual and the LSI-11 PDP-11/03 Processor Handbook contain useful information on interface circuits as well as installing and operating interface module such as the type which the user might configure on the DRV11-P. Handbooks may be ordered from the nearest Digital Equipment Corporation Sales Office.

Table 6 DRV11-P Parts List

Part No.	Description	Quantity
M7948	LSI-11 Foundation Module	1
MP00119	Field Maintenance Print Set	1 Set
EK-DRV11-OP-001	DRV11-P Foundation Module User's Manual	1

APPENDIX A
IC DESCRIPTIONS

The special purpose ICs designed and manufactured by Digital Equipment Corporation and used in the DRV11-P are described in this Appendix. These ICs are the DC003 interrupt logic and the DC004 protocol logic. A brief description of each IC, the signal lines, IC pinning, a timing diagram, and a simplified logic diagram are supplied.

A.1 DC003 INTERRUPT LOGIC

The interrupt chip is an 18-pin, 0.300″ center, DIP device that provides the circuits to perform an interrupt transaction in a computer system that uses a "pass-the-pulse" type arbitration scheme. The device is used in peripheral interfaces and provides two interrupt channels labeled "A" and "B," with the A section at a higher priority than the B section. Bus signals use high-impedance input circuits or high-drive-open-collector outputs, which allows the device to directly attach to the computer systems bus. Maximum current required from the Vcc supply is 140 mA.

Figure A-1 is a simplified logic diagram of the DC003 IC. Timing for the "A" interrupt section is shown in Figure A-2, while Figure A-3 shows the timing for both "A" and "B" interrupt sections. Table A-1 describes the signals and pins of the DC003 by pin and signal name.

A.2 DC004 PROTOCOL LOGIC

The protocol chip is a 20 pin 0.300" center, DIP device that functions as a register selector, providing the signals necessary to control data flow into and out of up to four word registers (8 bytes). Bus signals can directly attach to the device because receivers and drivers are provided on the chip. An RC delay circuit is provided to slow the response of the peripheral interface to data transfer requests. The circuit is designed such that if tight tolerance is not required, then only an external 1K ±20 percent resistor is necessary. External RC's can be added to vary the delay. Maximum current required from the V_{CC} supply is 120 mA.

Figure A-4 is a simplified logic diagram of the DC004 IC. Signal timing with respect to different loads are tabularized in Table A-2 and are shown in Figure A-5. Figure A-6 shows the loading for the test conditions in Table A-2. Signal and pin definitions for the DC004 are presented in Table A-3.

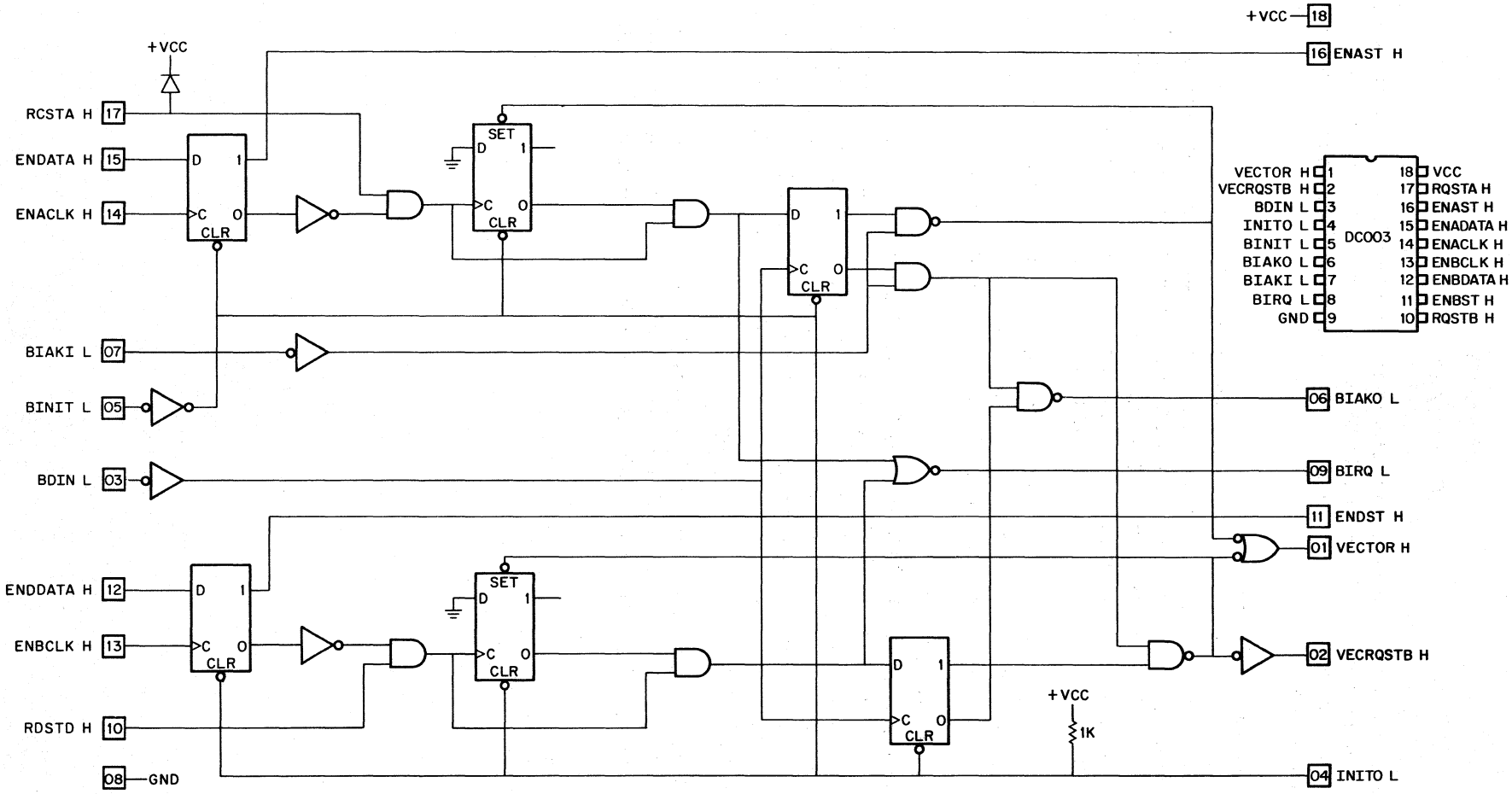

Figure A-1 DC003 Simplified Logic Diagram

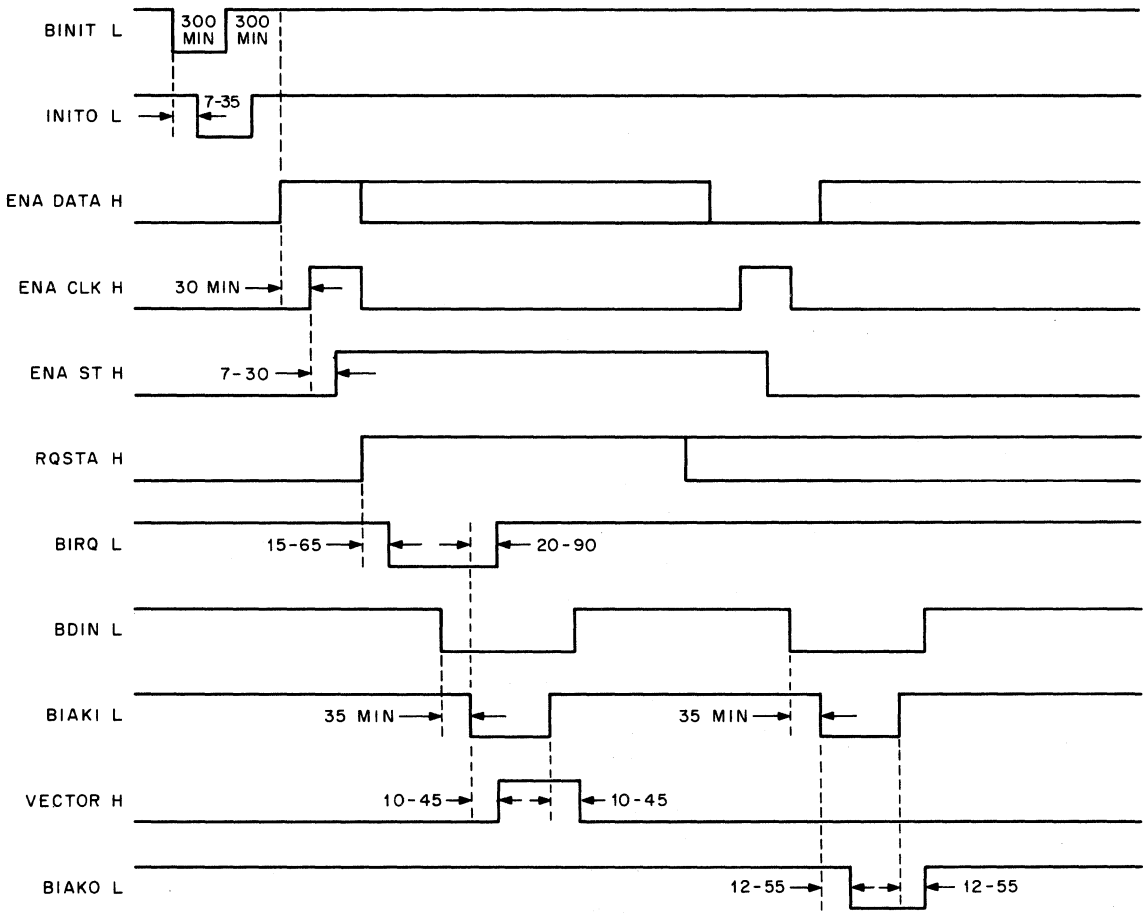

Figure A-2 DC003 "A" Interrupt Section Timing Diagram

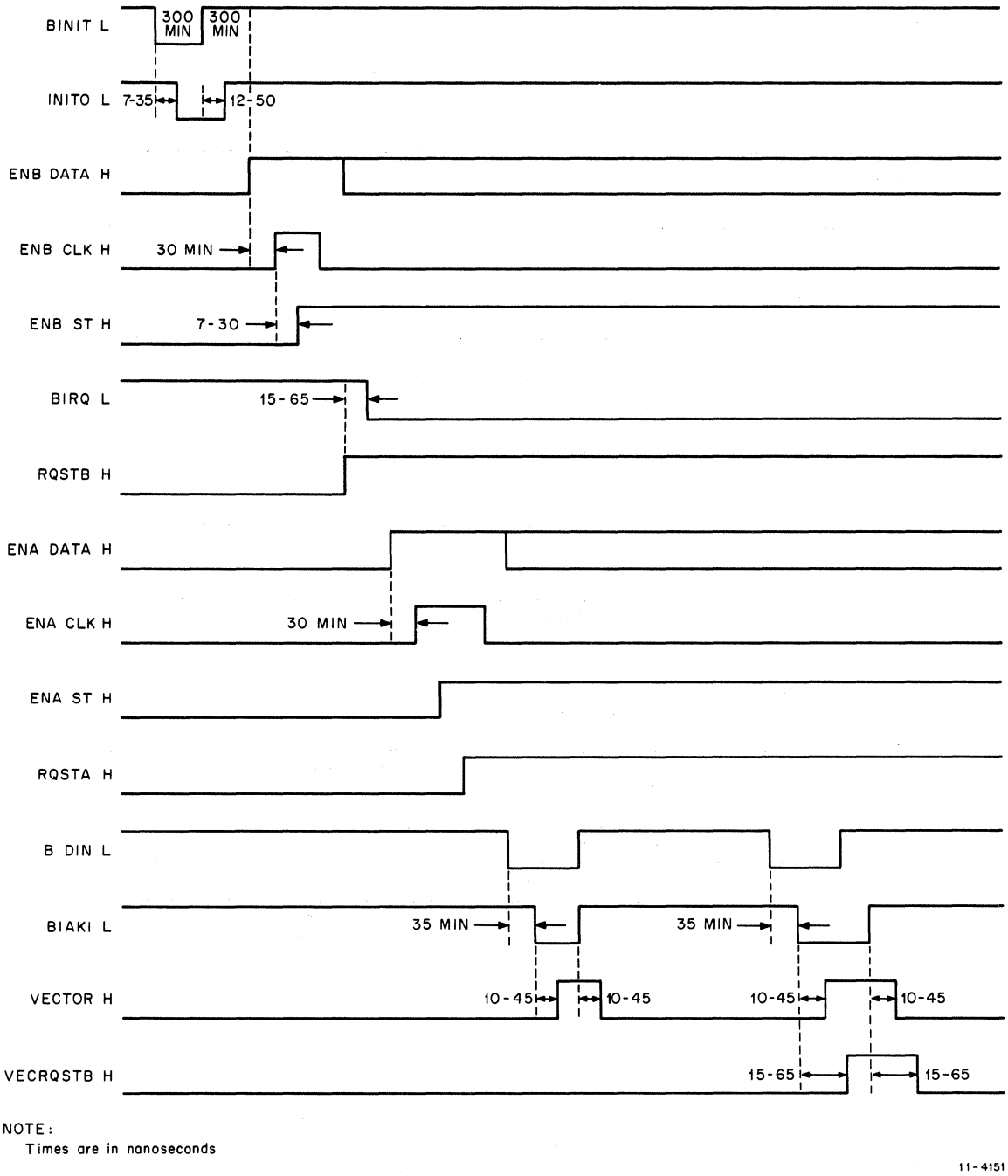

Figure A-3 DC003 "A" and "B" Interrupt Sections Timing Diagrams

Table A-1 DC003 Pin/Signal Descriptions

Pin	Signal	Description
1	VECTOR H	INTERRUPT VECTOR GATING SIGNAL. This signal should be used to gate the appropriate vector address onto the bus and to form the bus signal called BRPLY L.
2	VEC RQSTB H	VECTOR REQUEST "B" SIGNAL. When asserted indicates RQST "B" service vector address is required. When unasserted indicates RQST "A" service vector address is required. VECTOR H is the gating signal for the entire vector address: VEC RQST B H is normally bit 2 of the vector address.
3	BDIN L	BUS DATA IN. This signal generated by the processor BDIN always preceeds a BIAK signal.
4	INITO L	INITIALIZE OUT signal. This is the buffered BINIT L signal used in the device interface for general initialization.
5	BINIT L	BUS INITIALIZE signal. When asserted, this signal brings all driven lines to their unasserted state (except INITO L).
6	BIAKO L	BUS INTERRUPT ACKNOWLEDGE signal (OUT). This signal is the daisy-chained signal that is passed by all devices not requesting interrupt service (see BIAKI L). Once passed by a device, it must remain passed until a new BIAKI L is generated.
7	BIAKI L	BUS INTERRUPT ACKNOWLEDGE signal (IN). This signal is the processor's response to BIRQ L true. This signal is daisy-chained such that the first requesting device blocks the signal propagation while non-requesting devices pass the signal on as BIAKO L to the next device in the chain. The leading edge of BIAKI L causes BIRQ L to be unasserted by the requesting device.
8	BIRQ L	ASYNCHRONOUS BUS INTERRUPT REQUEST from a device needing interrupt service. The request is generated by a true RQST signal along with the associated true interrupt enable signal. The request is removed after the acceptance of the BDIN L signal and on the leading edge of the BIAKI L signal or the removal of the associated interrupt enable or due to the removal of the associated request signal.
10 17	REQSTB H REQSTA H	DEVICE INTERRUPT REQUEST SIGNAL. When asserted with the enable "A" flip-flop asserted will cause the assertion of BIRQ L on the bus. This signal line normally remains asserted until the request is serviced.

Table A-1 DC003 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
11 16	ENB ST H ENA ST H	INTERRUPT ENABLE "A" STATUS signal. This signal indicates the state of the interrupt enable "A" internal flip-flop which is controlled by the signal line ENA DATA H and the ENA CLK H clock line.
12 15	ENB DATA H ENA DATA H	INTERRUPT ENABLE "A" DATA signal. The level on this line, in conjunction with the ENA CLK H signal, determines the state of the internal interrupt enable "A" flip-flop. The output of this flip-flop is monitored by the ENA ST H signal.
13 14	ENB CLK H ENA CLK H	INTERRUPT ENABLE "A" CLOCK. When asserted (on the positive edge), interrupt enable "A" flip-flop assumes the state of the ENA DATA H signal line.

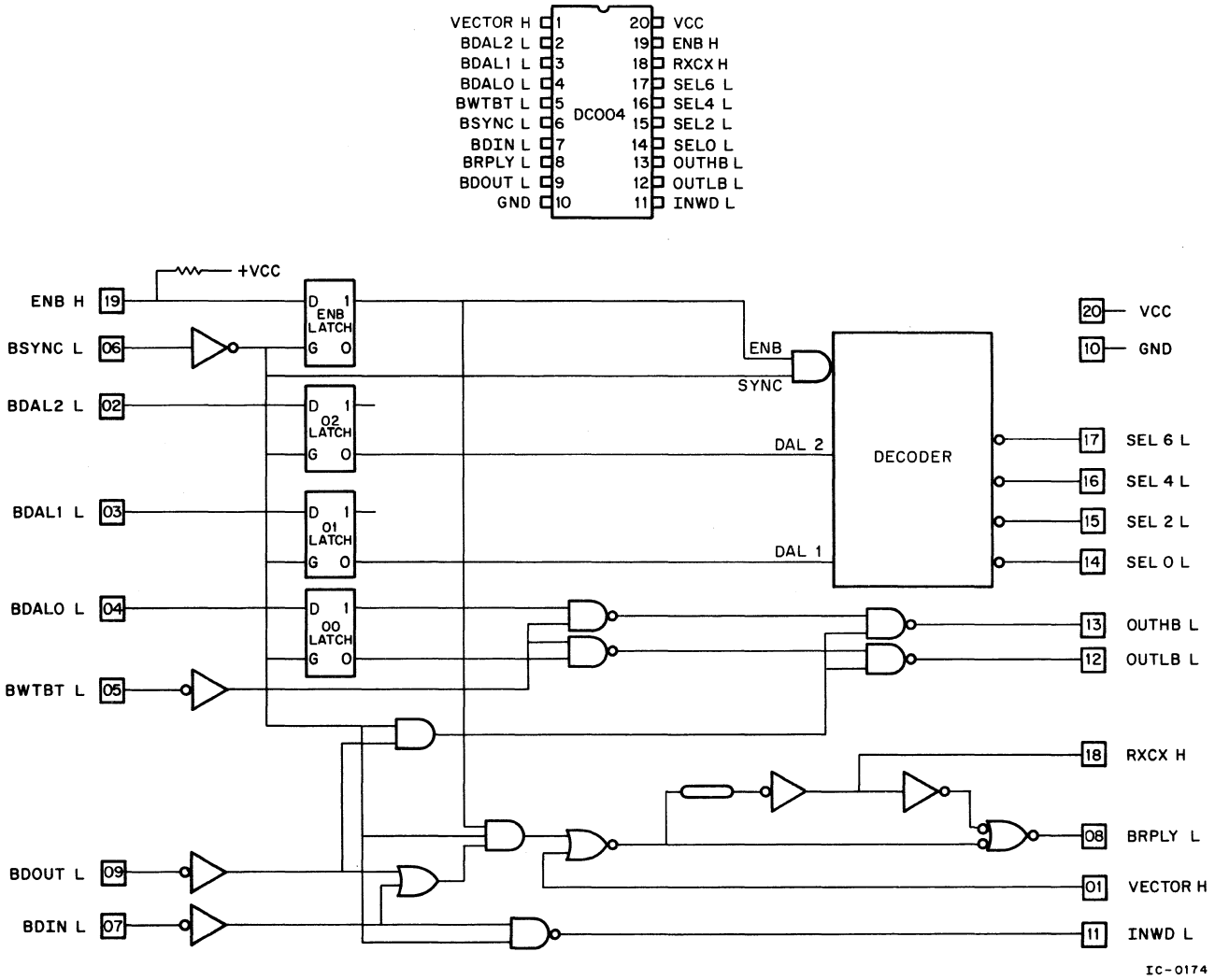

Figure A-4 DC004 Simplified Logic Diagram

Table A-2 DC004 Signal Timing vs Output Loading

	Signal	With Respect to	Signal	Test Cond.	Output Being Asserted Min (ns)	Output Being Asserted Max (ns)	Output Being Asserted Min (ns)	Output Being Asserted Max (ns)	Fig. A-5 Ref.
	SEL (0,2,4,6) L		BSYNC L	Load B	15	35	5	25	t_5, t_6
				Load C	15	40	5	30	
	OUTLB L		BDOUT L	Load B	5	25	5	25	t_9, t_{10}
				Load C	5	30	5	30	
	OUTHB L		DBOUT L	Load B	5	25	5	25	t_9, t_{10}
				Load C	5	30	5	30	
	INWD L		BDIN L	Load A	5	25	5	25	t_{11}, t_{12}
				Load B	5	30	5	30	
Pin 18 Connection RX = 1K ±5% 350Ω ±5% 15 pf ±5%	BRPLY L (Load A)		OUTLB L (Load B)		20	60	-10	45	t_{13}, t_{14}
	BRPLY L (Load A)		OUTHB L (Load B)		20	60	-10	45	t_{13}, t_{14}
	BRPLY L (Load A)		INWD L (Load B)		20	60	-10	45	t_{13}, t_{14}
	BRPLY L (Load A)		VECTOR H		30	70	0	45	t_{13}, t_{14}
Pin 18 Connection RX = 4.64K ±1%	BRPLY L (Load A)		OUTLB L (Load B)		300	400	-10	45	t_{13}, t_{14}
	BRPLY L (Load A)		OUTHB L (Load B)		300	400	-10	45	t_{13}, t_{14}

Table A-2 DC004 Signal Timing vs Output Loading (Cont)

	With Respect Signal	to Signal	Test Cond.	Output Being Asserted Min (ns)	Output Being Asserted Max (ns)	Output Being Asserted Min (ns)	Output Being Asserted Max (ns)	Fig. A-5 Ref.
CX = 220 pf ±1%	BRPLY L (Load A)	INWD L (Load B)		300	400	-10	45	t_{13}, t_{14}
	BRPLY L (Load A)	VECTOR H		330	430	0	45	t_{13}, t_{14}

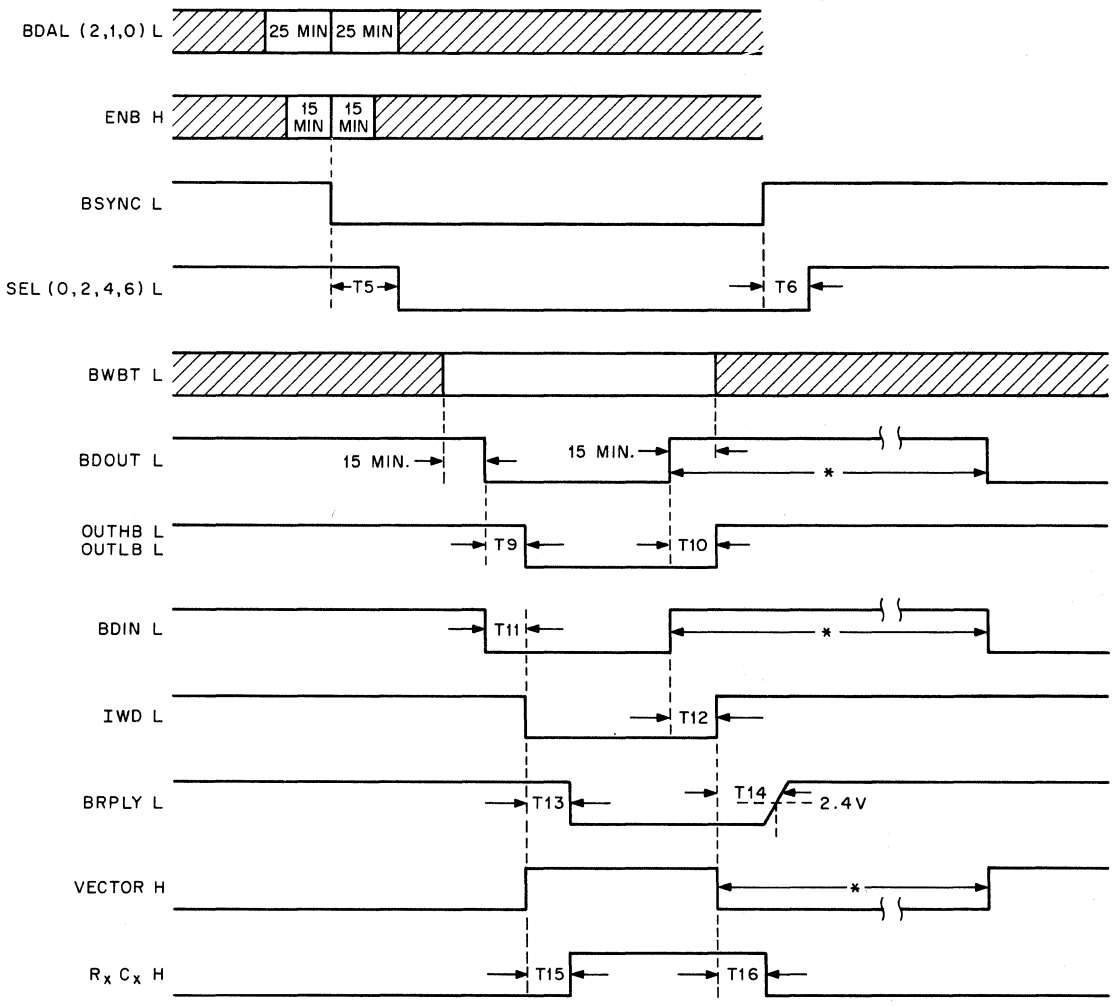

Figure A-5 DC004 Timing Diagram

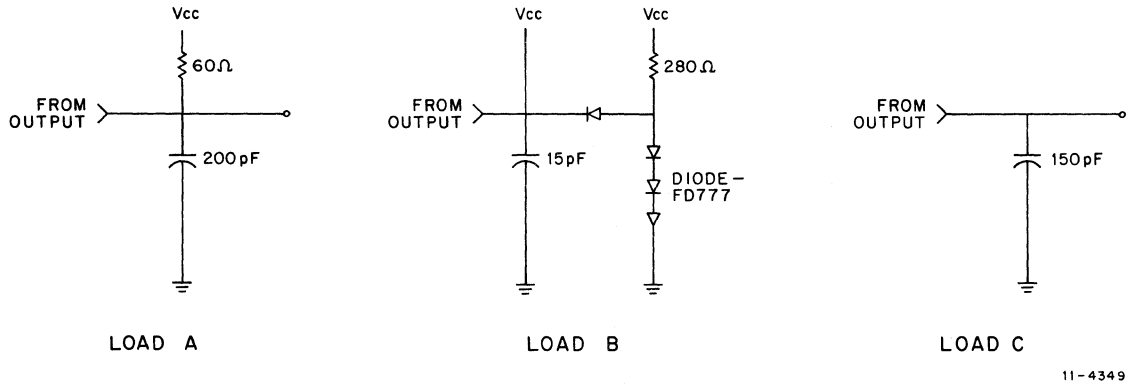

Figure A-6 DC004 Loading Configurations for Table A-2

Table A-3 DC004 Pin/Signal Descriptions

Pin	Signal	Description
1	VECTOR H	VECTOR. This input causes BRPLY L to be generated through the delay circuit. Independent of BSYNC L and ENB H.
2 3 4	BDAL2 L BDAL1 L BDAL0 L	BUS DATA ADDRESS LINES. These signals are latched at the assert edge of BSYNC L. Lines 2 and 1 are decoded for the select outputs; line 0 is used for byte selection.
5	BWTBT L	BUS WRITE/BYTE. While the BDOUT L input is asserted, this signal indicates a byte or word operation: Asserted = byte, unasserted = word. Decoded with B OUT L and latched BDAL0 L to form OUTLB L and OUTHB L.
6	BSYNC L	BUS SYNCHRONIZE. At the assert edge of this signal, address information is trapped in four latches. While unasserted, disables all outputs except the vector term of BRPLY L.
7	BDIN L	BUS DATA IN. This is a strobing signal to effect a data input transaction. Generates BRPLY L through the delay circuit and INWD L.
8	BRPLY L	BUS REPLY. This signal is generated through an RC delay by VECTOR H, and strobed by BDIN L or BDOUT L, and BSYNC L and latched ENB H.
9	BDOUT L	BUS DATA OUT. This is a strobing signal to effect a data output transaction. Decoded with BWTBT L and BDAL0 to form OUTLB L and OUTHB L. Generates BRPLY L through the delay circuit.
11	INWD L	IN WORD. Used to gate (read) data from a selected register on to the data bus. Enabled by BSYNC L and strobed by BDIN L.
12 13	OUTHB L OUTLB L	OUT LOW BYTE, OUT HIGH BYTE. Used to load (write) data into the lower, higher, or both bytes of a selected register. Enabled by BSYNC L and decode of BWTBT L and latched BDAL0 L, and strobed by BDOUT L.
14 15 16 17	SEL0 L SEL2 L SEL4 L SEL6 L	SELECT LINES. One of these four signals is true as a function of BDAL2 L and BDAL1 L if ENB H is asserted at the assert edge of BSYNC L. They indicate that a word register has been selected for a data transaction. These signals never become asserted except at the assertion of BSYNC L (then only if ENB H is asserted at that time) and once asserted, are not unasserted until BSYNC L becomes unasserted.

Table A-3 DC004 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
18	RXCX	EXTERNAL RESISTOR CAPACITOR NODE. This node is provided to vary the delay between the BDIN L, BDOUT L, and VECTOR H inputs and BRPLY L output. The external resistor should be tied to VCC and the capacitor to ground. As an output, it is the logical inversion of BRPLY L.
19	ENB H	ENABLE. This signal is latched at the asserted edge of BSYNC L and is used to enable the select outputs and the address term of BRPLY L.

Reader's Comments

DRV11-P FOUNDATION MODULE
USER'S MANUAL
EK-DRV11-OP-002

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