Digital Equipment Corporation
Maynard, Massachusetts

digital

GLC-8
Maintenance Manual

DEC-08-H8CA-D

GLC-8
MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION ▫ MAYNARD, MASSACHUSETTS

1st Printing May 1969

Instruction times, operating speeds and the like are included in this manual for reference only; they are not to be taken as specifications.

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CHAPTER 1
GENERAL INFORMATION

This manual provides operation and maintenance information for the GLC-8* System. The GLC-8 System is designed to acquire, analyze, and record analog data from gas chromatographs. The basic data acquisition and processor unit of the GLC-8 System is the PDP-8/I Computer (see Figure 1-1). The versatility of the PDP-8/I and its specially designed interface enables the GLC-8 System to perform the following functions sequentially for up to 22 on-line gas chromatographs. As many as 64 gas chromatographs can be connected on line.

a. Collect analog data from the gas-chromatographs
b. Calculate peak areas and peak retention times
c. Corrects for baseline shift
d. Allocate the areas of overlapping peaks
e. Identify peaks
f. Apply response factors
g. Calculate component concentration
h. Print the chromatogram analysis report

1.1 DESCRIPTION OF EQUIPMENT

The GLC-8 System consists of five basic components; a local operator control, gas chromatograph-computer interface, PDP-8/I computer, disk memory, and teletype. Each of these basic system components are described in the following paragraphs and tables. A simplified illustration of the GLC-8 System is shown in Figure 1-2.

1.1.1 Local Operator Control (LOC)

Each gas chromatograph station has a LOC box for selecting system mode of operation. Two LOC models are available with the GLC-8 System, H300 and H301. The H300 LOC, designed to perform functions directly related to the GLC-8 System, is used to communicate with the GLC-8 program and indicate program status. The H301 LOC is identical to the H300 except for the addition of relays to provide the system with additional control capabilties.

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* Gas-Liquid Chromatography

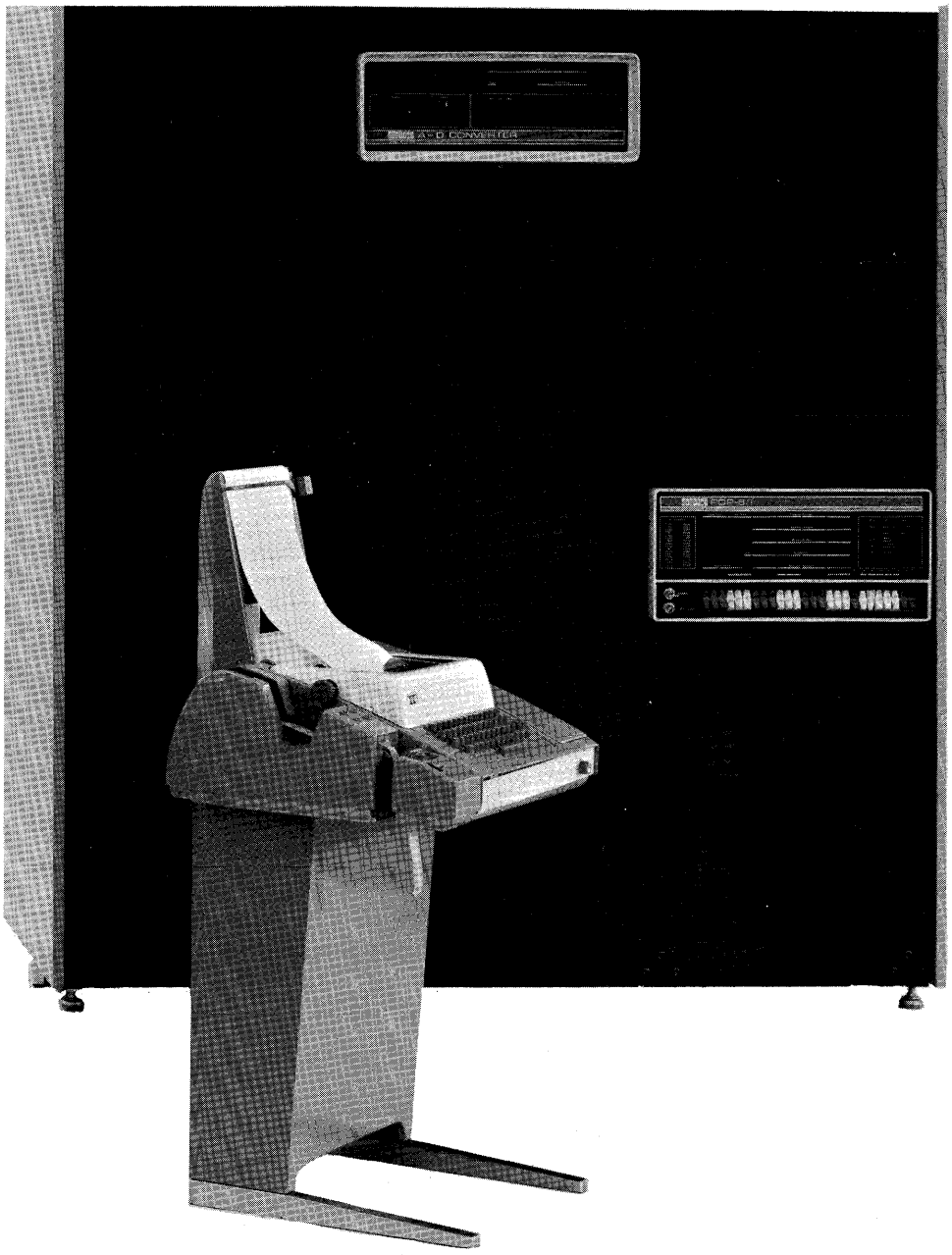


Figure 1-1 GLC-8 System with Teletype

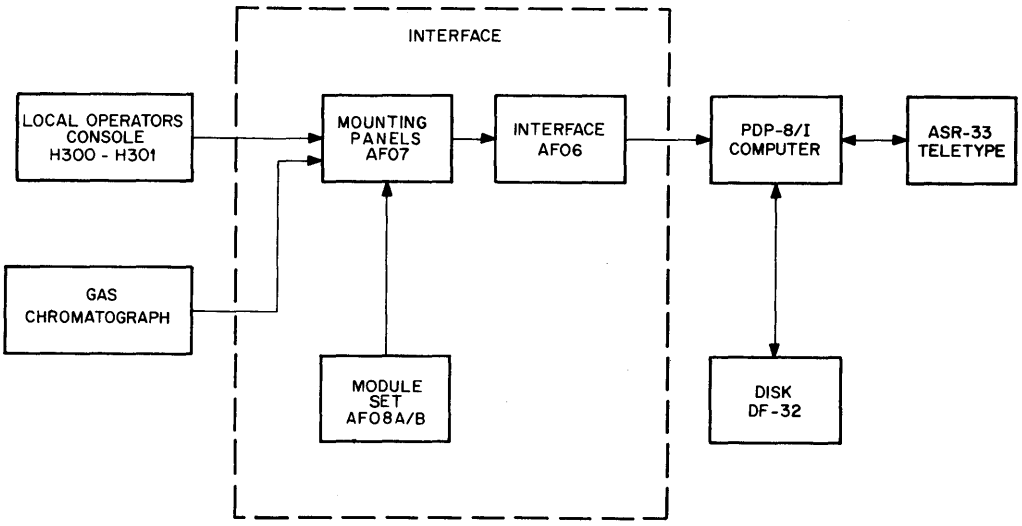


Figure 1-2 GLC-8 System Simplified Block Diagram

1.1.2 Gas Chromatograph/GLC-8 System Interface

The interface between the on-line gas chromatographs and GLC-8 System has three basic units: the AF06 System Interface, the AF08 A/B Module Set, and the AF07 Mounting Panels.

The AF06 performs the analog-to-digital conversion of the on-line gas chromatograph data and the control functions for the GLC-8 System. Two types of AF06 System Interfaces are available - the AF06-AA for 60 Hz primary power operation and the AF06-AB for 50 Hz primary power. The components of these system interface units are listed in Table 1-1. As shown in the table, the components are identical for each unit with the exception of the power supplies.

The AF08 A/B Module Set performs the filtering and control for each on-line gas chromatograph. Components of the AF08 A/B are listed in Table 1-2. One AF08 A/B is required for each gas chromatograph connected to the GLC-8 System.

The third basic component of the Gas Chromatograph/GLC-8 System Interface is the AF07 Mounting Panel (refer to Table 1-3). The AF07 is prewired to accommodate eight AF08 A/B Module Sets and eight A210 or A211 Amplifier Modules. One AF07 is required for every eight (or fraction thereof) gas chromatographs added to the GLC-8 System.

The amplifiers used with the GLC-8 are the A210 times one (X1) and A211 times ten (X10) Modules. The selection of these modules is dependent on the signal level from the gas chromatographs, i.e., low level signals (1 μV to 1V) will require the gain of the X10 amplifier and high level signals (10 μV to 10V) the X1 amplifier.

1.1.3 PDP-8/I General-Purpose Computer

The PDP-8/I is a general-purpose, random-access computer with a 1.5 μs cycle time. The basic system has a 4,096 12-bit word core memory. A teletype printer-keyboard with paper tape reader and punch is the standard I/O device.

For the GLC-8 System, the PDP-8/I has two options for greater data handling capability - the KE8/I Extended Arithmetic Element (EAE) and an additional 4,096 word memory.

1.1.4 Disk Memory

The GLC-8 System disk memory is a Type DF32 Random Access Disk File. This disk provides the GLC-8 System a randomly accessible bulk storage of 32,768 12-bit data words plus a 13th bit for parity.

1.1.5 Input/Output Data Transfer

The GLC-8 System uses an ASR33 Teletypewriter as the standard input/output transfer device. The teletype is used to communicate with the GLC-8 and prints a complete analysis report of the chromatogram on its teleprinter. The GLC-8 will support up to nine teletypes.

1.2 SPECIFICATIONS

There are three catagories of specifications for the GLC-8 System - performance, power, and environmental.

1.2.1 Performance Specifications

a. System

Line Noise (50 or 60 Hz):	$\leq$ 50 mV, P-P RFO at a gain of X256.
Gaussian Noise:	$\leq$ 50 mV RMS RFO at a gain of X256.
Bandwidth:	2 Hz for the A216 filter 10 Hz for the A213 filter
Rolloff:	A213 - 6 db per octave to 10 Hz -24 db per octave after 10 Hz A216 12 db per octave
Common Mode Rejection:	120 db at 50 or 60 Hz
Normal Mode Rejection:	60 db at 50 or 60 Hz
Common Mode Voltage:	270V maximum

Drift-X1 (A210) Buffer Amplifier and filter:	50 μV per C°
Drift-X10 (A211) Buffer Amplifier and filter:	300 μV per C°
Offset:	±1 mV input (adjustable) equals 0V output for both of the adjustable X1 and X10 Buffer Amplifiers
Sampling Rate; Four Times Line Frequency:	A total of 240 points per second (60 Hz) with individual channels at program selectable rates of 60, 30, 15, 7-1/2, or 3-3/4 points per second. For 50 Hz, selectable rates are 50, 25, 12-1/2, 6-1/4 or 3-1/8 points per second. Each is synchronized with the power network for either 50 or 60 Hz noise elimination. Noise elimination is synced with the 60 Hz line frequency.
Resolution	One part in 4096
Repeatibility	$\leq \pm 0.1$ percent
Margins	+10 ±5V, -15±3.0V
Settling Time:	Input amplifiers <0.44 seconds to within 0.025% f.s.
Variable Gain Amplifier:	≤25 ms to within 0.025% f.s.
Overload Recovery Time	
Input Amplifier:	≤0.2 ms
Variable Gain Amplifier:	≤10 μs
Individual Analog Channels:	Each channel has an isolation amplifier/ filter and multiplexing relay. The channel input impedance is one megohm and the bandwidth is 2 Hz for the A216 Filter and 4 Hz for the A213 Filter. Line unbalance, 1000 ohms.
Accuracy:	A213 Filter, ±2.0 percent. A216 Filter, ±0.1 percent.

b. Local Operator Consol (LOC), H300/H301

One LOC is required for each chromatograph.

The following contact specifications pertain to the H301 LOC.

Current (max):	500 mA
Voltage (max):	250V
Voltage (max):	10V
Resistance (max):	200 MΩ
Operate time (max):	0.7 ms
Release time (max):	0.05 ms
Bounce time (max):	0.3 ms
Life (at rated load):	10^7 operations

c. Interface

Buffer Amplifier: A210 (X1) or A211 (X10)	Gain must be specified when ordering equipment
Input:	Differential
Input Impedance:	One MΩ +0.1%
Input Voltage:	A210: +10V A211: +1V
Filter, A213 or A216:	A213: Bandwidth, 10 Hz Rolloff, 24 db per octave Gain, 1.0 ±2 % at dc A216: Bandwidth, 2 Hz Rolloff, 12 db per octave Gain, +1 ±0.05 % at dc
Low Level and High Level Multiplexer, AM03 and AM08:	Refer to the instruction book associated with this equipment for the performance specifications.
AM08 Timing:	M1 - 1.0 ms M2 - 1.9 ms M3 - 1.9 ms M4 - 1.0 ms M5 - 1.0 ms
Program Amplifier, AG04:	Gain is selectable by program control. With the A210 amplifier, the gains are 1, 2, 4, 8, 16, 32, 64, 128, and 256. With the A211 amplifier, the gains are 10, 20, 40, 80, 160, 320, 640, 1280, and 2560. Depending on the gain of the Buffer Amplifiers the full scale range is 10 μV to 10V for the A210 Amplifier (X1) and 1 μV for 1V for Amplifier A211 (X10)
Converter ADC1-A:	Refer to the instruction book associated with this equipment for the performance specifications.
Line Frequency Clock DK01A:	Output is four times the input line frequency.
Clock Pulses:	4.17 ms ±0.25 ms at 60 Hz 5.00 ms ±0.30 ms at 50 Hz
Clock Jitter:	≤10 μs at 60 Hz ≤12 μs at 50 Hz
Connections:	The GLC-8 System can be connected to thermal conductivity, flame ionization, and electron capture detectors.

Table 1-1
AF06 Interface Components

Component Name	Model Number	
	AF06-AA	AF06-AB
Analog/Digital Converter	ADC1-A (AF01)	ADC1-A (AF01)
Interface (ADC1-A to PDP-8/I)	ADC-8	ADC-8
Multiplexer Control	AM08	AM08
Low-Level Multiplexer	AM03-A	AM03-A
Console Control (Up to 8 AF17)	AF16	AF16
Variable Gain Amplifier	AG04	AG04
Four Times Line Frequency Clock	DK01-A	DK01-A
Dual Floating Regulated Power Supply	H713	H713
Margin Check Power Supply	734B (60 Hz)	734C (50 Hz)
Power Supply	783 (60 Hz)	783A (50 Hz)

Table 1-2
AF08 A/B Module Set Components

Component Name	Module Number
Filter 2 (Hz)	A216
Input Amplifier (AF08B only)	A210
Times Ten Input Amplifier (AF08A only)	A211
Diode Gate	R113
Insert Bus Gate	R123
Flip-Flops	R203 (2)
Cable Connector	W023
Indicator and Relay Driver	W051

Table 1-3
AF07 Mounting Panel Components

Component Name	Model Number
Control Panel for Local Operator Console	AF17
Amplifier Mounting Panel Connectors	H303
Inverter Module	R107
Pulse Output Converter	W640

Table 1-4
Optional Module

Component Name	Model Number
Filter (10 Hz)	A213

1.2.2 Power Specification

Table 1-5
System Power

Input AC Voltage	AC Current Nominal (Amps)	Power Dissipation	Heat Dissipation	DC Current			
				+10V	-15V	+15V Reg.	-15V Reg.
115 ±10 Vac 60 ±0.12 Hz single phase 220 ±20 Vac 50 ±0.10 Hz single phase 110 ±15 Vac at 50 Hz single phase	13.0A incorporates 30A Twist Lock AC Plug	1393W Plus 3.9 W/CH	4752 BTU/hr Plus 13.3 BTU/hr per channel	3.24A Plus 5.6 A/CH	11.97A Plus 0.2A/CH	20 MA Plus 23 MA per CH	20 MA Plus 23 MA per CH

Table 1-6
Unit Power

Equipment	AC Current Nominal (Amps)	Power Diss. (Watts)	Heat Diss. (BTU/hr)	DC Current			
				+10V	-15V	+15V Reg.	-15V Reg.
PDP-8/I	7.5	780	2660	-	5A	-	-
DF-32	3.0	500	1700	2A	4A	-	-
PT08	-	15	52	1A	0.3A	-	-
ADC1-A	0.5	55	188	-	-	-	-
AM08	-	20	68	46 MA	1.3A	-	-
AF16	-	21	72	188 MA	1.3A	-	-
AF17	-	25	8.5	5.6 MA	0.16A	-	-
AG04	-	2	7	2 MA	0.7A	20 MA	20 MA
AM03 (1 CH)	-	0.65	2.2	-	0.04A	-	-
H303 (1 CH)	-	0.7	2.4	-	-	30 MA	30 MA
783 (Extra)	2.0	-	-	-	-	-	-

1.2.3 Environmental Specifications

The ambient temperature at the installation site should be maintained between 0° C (32° F) and 50° C (122° F). Normal humidity is from 20% to 80%. All exposed surfaces of the cabinets and hardware are treated to prevent corrosion; however, exposure of the GLC-8 System to extreme humidity conditions for long periods of time should be avoided.

Because of amplifier drift, the above ambient temperature should be maintained within ±5° C (±9F). Thermal gradients exceeding ±5° C will cause inaccurate analog data. Below the temperature gradient, the system program can correct for the drift.

CAUTION

Avoid high thermal gradients.

CHAPTER 2
OPERATION AND PROGRAMMING

Operation and programming information relating to the GLC-8 system hardware is contained in this Chapter.

2.1 SYSTEM OPERATION

The GLC-8 uses a monitor program which is designed specifically to monitor and control every operational phase of the gas chromatograph. Organization of the GLC-8 System program is divided into two basic parts, foreground program and background program.

The GLC-8 program uses a clock pulse to drive the monitor. The foreground program provides the necessary programming to perform the following:

a. control of all I/O operations,

b. real-time decision making, and

c. immediate calculations, modifications and organization of the received analog data.

The background portion of the program is activated when it receives low priority monitor requests. The background program sequentially performs:

a. analysis calculations

b. report formatting,

c. interpretation of the operator conversation mode.

During a clock interrupt period, the A-D conversion data is taken to maximize noise rejection benefits of the synchronous sampling technique.

The Local Operator Console (LOC) pushbutton requests, Table 2-1, are sampled and the channel status is indicated on the LOC (see Figure 2-1). The next channel scheduled is now selected with the proper gain selection set into the programmable amplifier. Gain selection is such that the gas chromatograph signal level is within the operational range of the A-D converter. Channel and gain changes are performed at the clock interrupt period to allow the associated relays sufficient time to energize and settle down during the next clock interrupt.

The next channel is selected in accordance with the requested gas-chromatographs and the required sampling rate. Each chromatograph may be scanned at different rates; however, the intervals between successive scans are constant and occur at a maximum multiple of four clock interrupts.

One of the on-line teletypes is serviced for the purpose of inputting one character if required to do so. On successive interrupts, each system teletype is serviced by this polling technique. At this time, the program interrupt level performs analog data calculations, modifications to the program, proper organization, and execution of user time dependent functions; it then returns to the interrupted software level.

Table 2-1
H300 and H301 Local Operator Control Consoles

Lamp and Pushbutton	Symbol	Function
CLEAR Pushbutton	S1	Cancels the analyzing run either before or after the starting of the run; also causes the method to be unassigned
READY Lamp	L1	Before the sample is injected into the gas-chromatograph, this light indicates that the analysis run can be initiated
START Pushbutton	S2	Initiates analyzing run after injection of the sample
SAMP Lamp	L2	Indicates that the injected sample is being analyzed
STOP Pushbutton	S3	Depressing this pushbutton prematurely terminates the analysis run
COMP Lamp	L3	Indicates that the analysis run is in the reporting cycle

Disk interrupts can occur at any time by generating a disk handling code which executes the proper handling and transfer control.

2.2 SYSTEM SUPPORT DOCUMENTATION

With the exception of the LOC console, the operation of each console is described in detail in the technical manuals supplied with each equipment. Efficient use of the GLC-8 is described in the GLC-8 Users Guide, DEC-08-GAYN-D.

2.3 SPECIAL MAINTENANCE IOT CODES

IOT codes 6154 and 6164 enable synchronous sampling on every fourth clock pulse. These clock interrupts enable synchronous sampling at the same phase as the input line frequency.

2.4 DISK AND CLOCK INTERRUPT LIMITATIONS (See Figure 6-1)

System software expects two types of interrupts, one from the disk and the other from the clock. To accomplish this, PI ON-OFF switches are included in some GLC-8 equipments to disable interrupts from the following GLC-8 optional equipments:

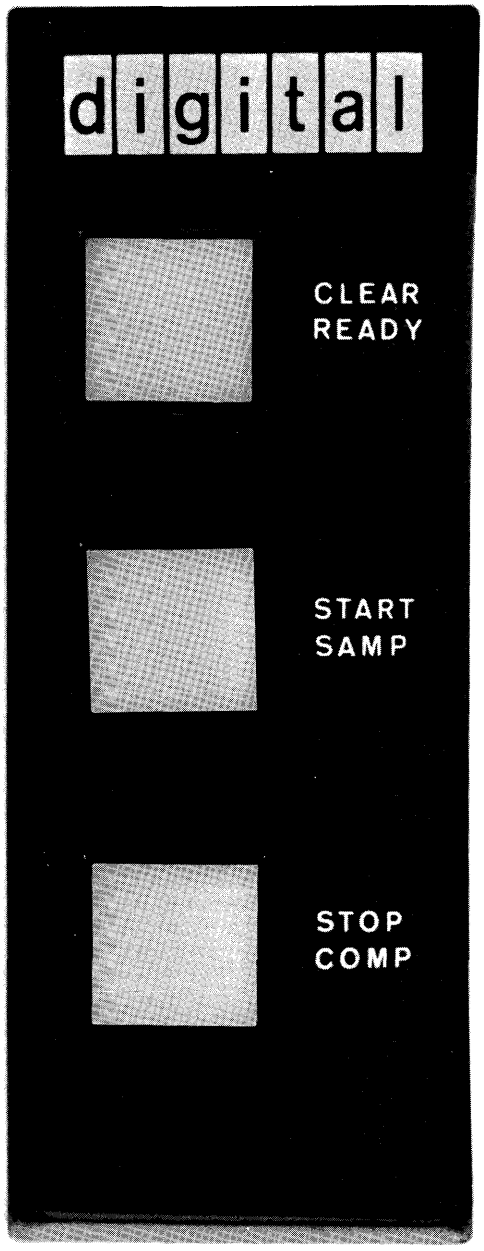


Figure 2-1 H300 and H301 Local Operator Console

a. PDP-8/I Computer (TTY interrupt)

b. PT08 Single/Dual Channel Teletype Interface (remote TTY interrupt)

c. ADC1-A Analog-to-Digital Converter (A/D interrupt)

NOTE

The PI ON-OFF switches must be set OFF during system operation, and must be set ON when performing maintenance diagnostics.

2.5 IOT INSTRUCTIONS

The IOT instruction codes associated with the GLC-8 are shown in Tables 2-2 through 2-7, and the associated equipment IOT codes are shown in Tables 2-8 and 2-9. Figures 2-2, 2-3, and 2-4 are the bit assignment diagrams for the IOT codes.

Table 2-2
Clock IOT Codes (DK01)

IOT Instruction	Function
6141	Skip on Clock Flag
6142	Clear Clock Flag
6144	Enable Clock

Table 2-3
Variable Gain Amplifier (AG04) IOT Codes

IOT Instruction	Function
6151	Clears Gain Control Register
6152	Load Variable Gain Register from AC05-11.

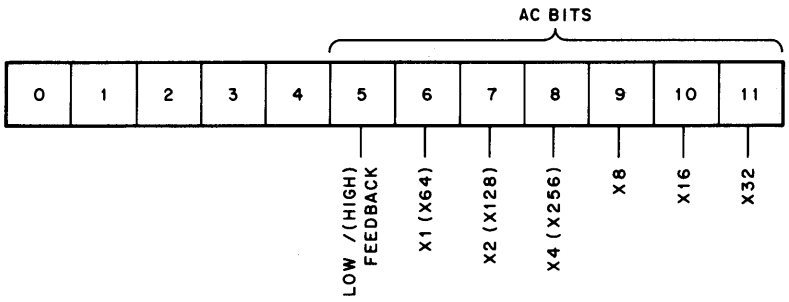


Figure 2-2 AG04 Variable Gain Amplifier Control Bit Assignment

Table 2-4
Digital Output Register IOT Codes (AF17)

IOT Instruction	Function
6161	Clear Digital Output Register
6162	Loads Digital Output Register from AC06-11

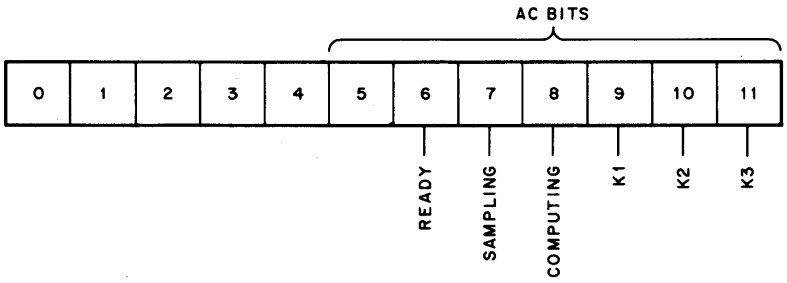


Figure 2-3 Digital Output Register Bit Assignment Diagram

Table 2-5
Digital Input Register IOT Codes (AF17)

IOT Instructions	Function
6171	Clears PDP-8 Accumulator
6172	Loads Digital Input Register into AC 06-11

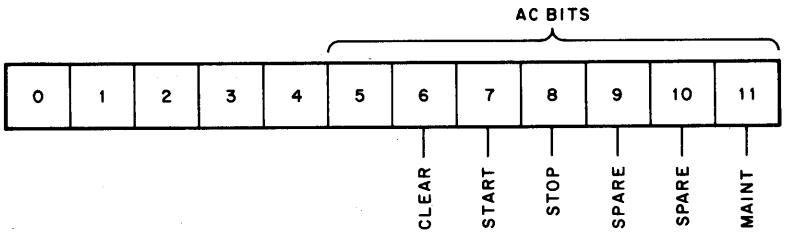


Figure 2-4 Digital Input Register Bit Assignment Diagram

Table 2-6
Calibration IOT Codes (DK01)

IOT Instruction	Function
6154	Set the CAL flag
6164	Clears the CAL flag

Table 2-7
Miscellaneous IOT Code

IOT Instruction	Function
6174	Not Used

Table 2-8
AM08, AF16 64 Channel Codes

IOT Instruction	Mnemonic Code	Function
6542	ADSC	Clears channel-address register
6544	ADIC	Loads channel-address register

Table 2-9
A/D Converter Codes (ADC-1)

IOT Instruction	Mnemonic Code	Function
6531	ADSF	Skip on an A/D Done Flag
6532	ADCV	Clear Done Flag and convert
6534	ADRB	Clear Done Flag and read A/D converter buffer

2.6 DIAGNOSTIC PROGRAM

The following program provides H300 or H301 READY, indicating output to Channel 5. The program then waits for the H300 or H301 LOC START pushbutton to be depressed, illuminating the SAMP lamp; converts synchronously on Channel 5; and halts the machine.

```
START   CLA CLL          /Clear the AC and Link
        JMS SYNC         /Go to Sync on clock pulse
        TAD KCHAN        /Get channel number
        IOT 6416         /Select analog and digital channel
        CLA              /Clear the AC
        JMS SYNC         /Sync on the clock pulse to make sure channel
                         /is selected
        TAD KREADY       /Get READY bit 6
        IOT 6163         /Clear and load digital output register
        IOT 6173         /Clear AC and read digital input register into AC
        AND K20          /Mask out all but START bit 7
        SNA              /Is read bit on
        JMP.-3           /No, try again
        CLA              /Yes, clear the AC
        TAD KSAMPL       /Get SAMPLING bit 7
        IOT 6163         /Clear and load digital output register
        CLA              /Clear the AC
        JMS SYNC         /Go to Sync on clock pulse
        TAD PAG 1        /Get gain of one for programmable gain amplifier
        IOT 6153         /Clear AC and load programmable gain amplifier
        JMS SYNC         /Go to Sync on clock flag to ensure relays in pro-
                         /grammable gain amplifier are selected and Sync
                         /for sampling
        IOT 6532         /Convert A/D Converter
        IOT 6531         /Skip on A/D Done flag
        JMP.-1           /Not Yet
        IOT 6534         /Read A/D Converter buffer into AC
        HLT              /Job done
SYNC:0                   /PC store
        IOT 6145         /Enable clock flag and skip on flag
        JMP.-1           /Not up yet
```

```
IOT 6142                /Clear flag
JMP @ SYNC              /Return
KCHAN:  0005
KREADY: 0040
K20:    0020
KSAMPL: 0020
PAG01:  0004
```

CHAPTER 3
INTERFACE ANALYSIS

The circuit analysis of the GLC-8 Interface is described in the following sections. Note that the drawings referenced in these sections which are prefixed by a three (located in Chapter 3 of this manual) are simplified diagrams of the block schematics. For detailed circuit information, refer to the drawings prefixed by a six (located in Chapter 6 of this manual).

3.1 GLC-8 SYSTEM SIGNAL FLOW (See Figure 3-1)

3.1.1 Analog Signal Flow

Because gas chromatographs are normally located some distance away from the GLC-8 system, information transmitted from a gas chromatograph to the GLC-8 interface system is subjected to both common-mode and normal-mode noise pickup.

Common-mode noise is defined as the signal which is added to the source signal due to differences in ground potential. This noise signal is common to both the source signal and the source return. Normal-mode noise is defined as the signal which is superimposed in series with the source generator due to static or magnetic coupling.

To minimize common-mode and normal-mode noise pickup, a shielded, twisted-pair cable is recommended for carrying the analog signal from the chromatograph to the GLC-8 interface. The shield of this cable should be connected to ground at the source end only, as shown in Figure 3-1.

Common-mode noise rejection is accomplished in the GLC-8 Interface by the use of a differential input amplifier on each channel. Normal-mode noise rejection is accomplished by limiting the bandwidth of the input amplifier and by filtering the signal at the output of the amplifier. A complete description of the input amplifier and filter is given in Paragraphs 3.8 and 3.9.

Up to a maximum of nine teletypes, including the console teletype, can be connected to the GLC-8 System. The standard IOT device for the PDP-8/I is the ASR-33 Teletype. The ASR-33 is used to communicate operator commands to the GLC-8 System and for printing the analysis report.

Figure 3-2 shows the interconnection of the AF06 and AF07 Interface Components and the AF08 Module Set.

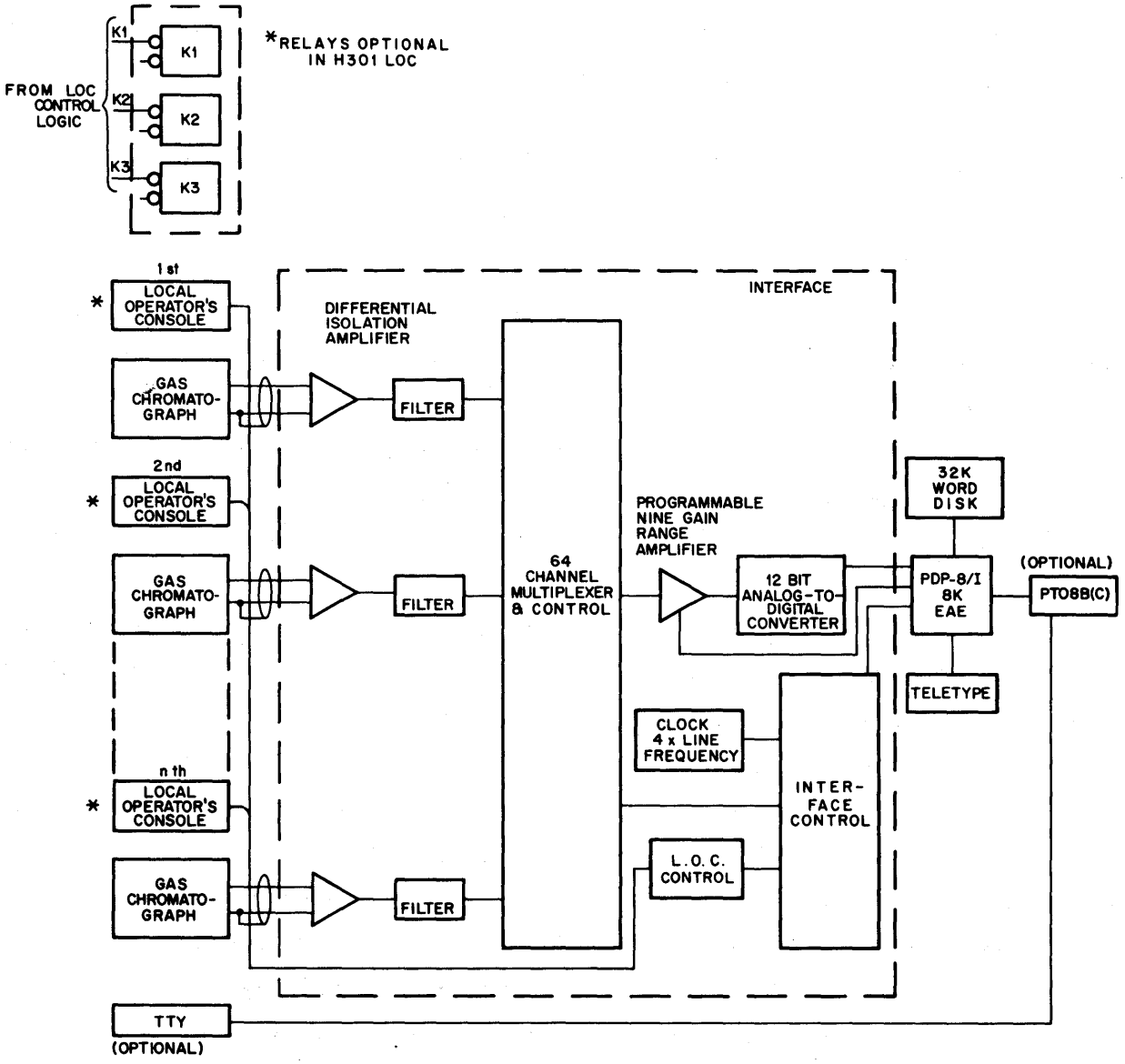


Figure 3-1 System Configuration

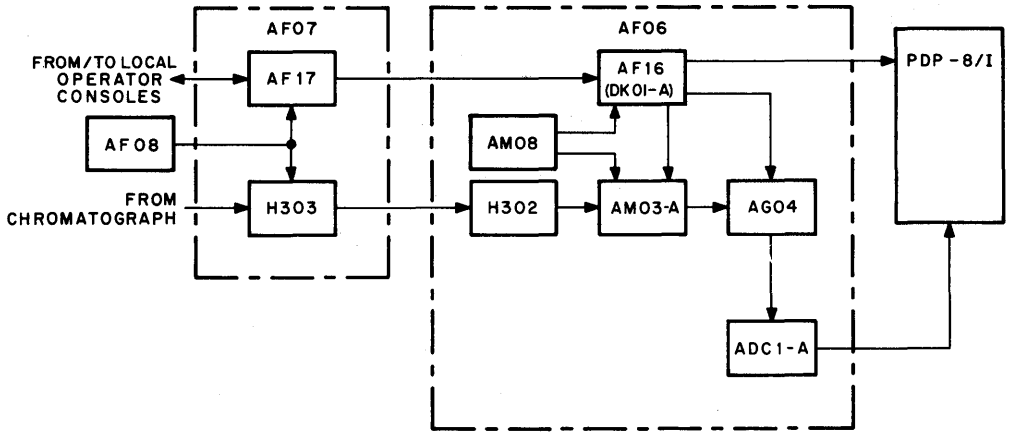


Figure 3-2 AF06, AF07, and AF08 Interconnection Diagram

3.2 AF16 CHROM CONTROL LOGIC

3.2.1 Variable Gain Amplifier Control (See Figures 3-3 and 6-2)

The input IOT instructions 6151 and 6152 are decoded by W103 Device Selector modules within the control logic, and the BAC bits 5 through 11 are obtained from the PDP-8/I. The selectable gain either increases or decreases, in powers of two, from a LOW FEEDBACK gain of X1 to a HIGH FEEDBACK gain of X256.

The IOT instruction 6151 first clears all of the gain control registers, setting them to the zero state or the LOW FEEDBACK mode (low gain). The IOT instruction 6152 strobes all the gain registers, allowing the information in the accumulator to be read into the flip-flop control registers. This IOT instruction sets the appropriate bits in the one state. When BAC bit 5 is HI, or a one, and IOT 6152 is issued, the Variable Gain Amplifier Control register is set in the HIGH FEEDBACK mode (high gain).

Selected HIGH or LOW gain, is dependent on the mode of the HIGH-LOW FEEDBACK flip-flop and on which of the BAC bits 6 through 11 are HI. Only one of these bits (6 through 11) should be HI at any one time.

3.2.2 Local Operator Console Channel Selector

Refer to Figure 3-4 and 6-3.

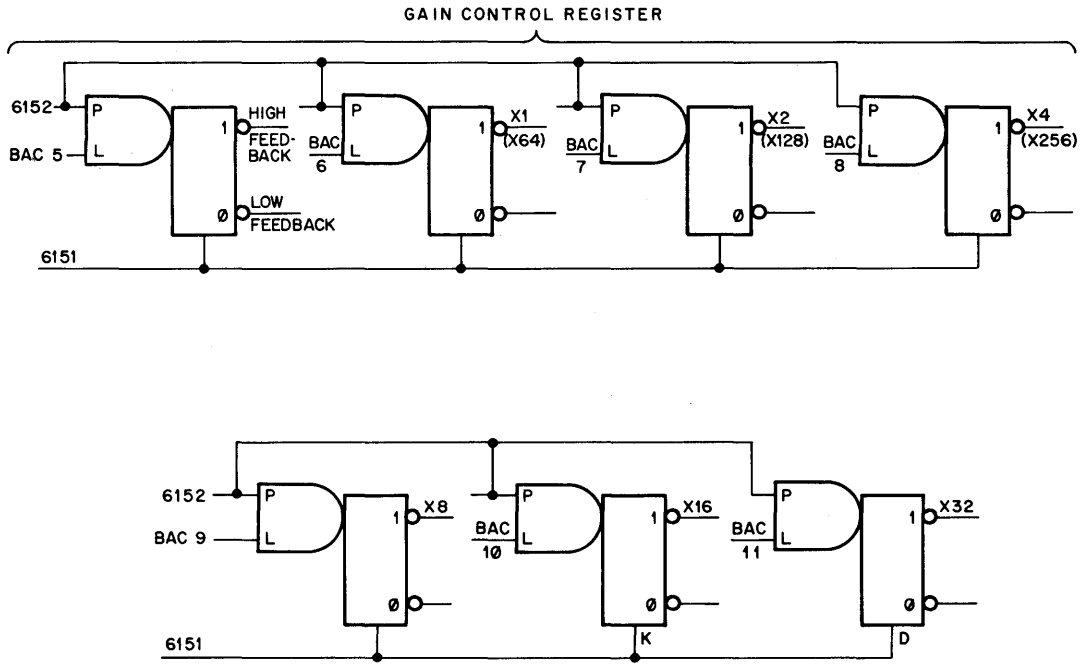


Figure 3-3 Variable Gain Amplifier Control, Simplified Diagram

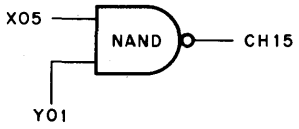


Figure 3-4 LOC Channel Selector Amplified Control, Simplified Diagram

Inside the cabinet of the GLC-8 System, common-mode noise is a minimal; therefore, single ended output from the amplifier is sufficient. However, normal-mode noise due to magnetic coupling is still prevalent. Therefore, twisted pair wire is used from the output of the amplifiers, through the filters and 64 channel multiplexer, and to the AG04 Programmable Amplifier. The output of the AG04 Amplifier is connected to the ADC1-A converter through a coaxial cable. The converter then converts to a digital word and places it on the PDP-8/I I/O bus.

3.2.3 Digital Signal Flow

The DK01-A Four Times Line Frequency Clock provides the program interrupt and skip instructions required by the PDP-8/I. The single program interrupt, operating synchronously from the power line frequency, provides control and timing information to the program.

The H300 or H301 LOC houses the program control pushbuttons used for operating the GLC-8 System. Pushbutton functions are transferred to the PDP-8/I input mixer bus by way of the LOC control logic.

The channel select circuitry is a 64-stage modular digital multiplexer providing X-Y coordinate addressing for the AF17 LOC control logic channels 0 through 63.

Channel selection is performed by an 8 by 8 X and Y matrix consisting of 64 NOR gates. The matrix signals are cabled from the AM03-A Low-Level Multiplexer and are buffered and inverted in the AF16 by the 3 R107 Inverter modules (see Figures 3-5 and 6-4).

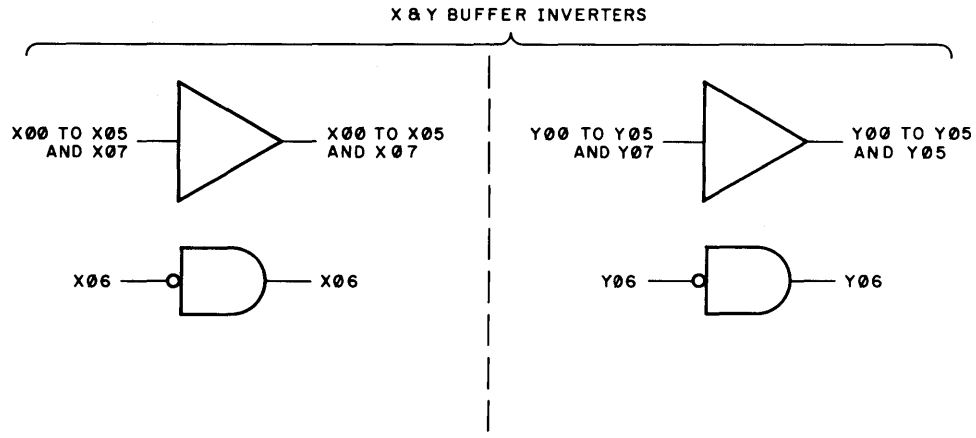


Figure 3-5 Channel Selector Interface, Simplified Diagram

Channel selection is dependent upon which X and Y points the control signals are applied to. For example, if the control signals are applied to X05 and Y01, and they are both HI, channel 15 NAND gate will be enabled and its LO output fed to the AF17 channel 15 control logic circuit.

Activation of the H300 or H301 LOC relays and lights for a particular channel is dependent upon the selected channel in this matrix and the accumulator binary bits occupying positions 06 through 11 (see Figure 3-7).

Mounting and wiring facilities are provided in groups of eight channels, which are expandable to 64. The number of channels provided is dependent on the user's requirements.

3.2.4 Chrom and LOC IOT Decoding (See Figures 3-6 and 6-5)

Input/Output Transfer instructions used in the DK01-A Clock, AG01 Variable Gain Amplifier, and AF17 LOC Control Logic are decoded by the W103 Device Selector modules in the AF16 Chrom Control Logic.

The W103 Device Selector module selects a device by ANDing the instruction word, held in the memory buffer (MB), and IOP pulses 1, 2, or 4.

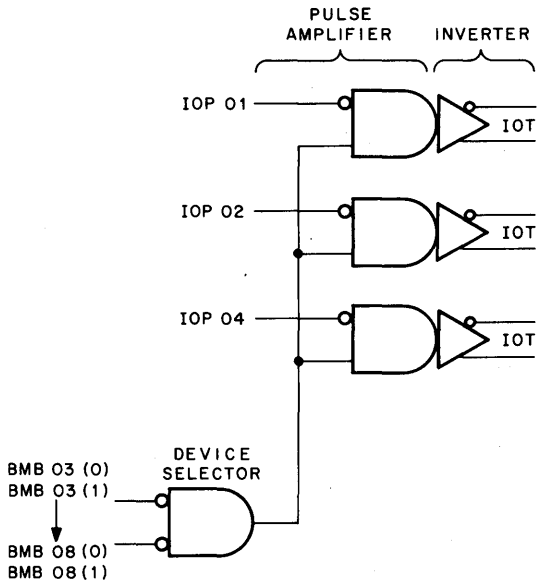


Figure 3-6 Chrom and LOC, IOT Decoding, Simplified Diagram

3.2.5 Channel Selector to LOC Control Logic Cables (See Figure 6-6)

These cables interconnect the AF16 LOC Channel Selector and the AF17 LOC Control Logic, Channels 00 through 07.

Cables A29 through A32 and B29 through B32 carry the 64-channel output signals from the digital multiplexer. Each cable has eight channels on it. Since there are eight such cables, the full complement of 64 channels is accommodated.

Cable B28 carries two types of signals to the AF17 circuitry, one is the buffered information from the PDP-8/I accumulator and the other is the IOT instruction bit codes for channel selection.

Cable A26 carries the input mixer (IM) bit information from either the H300 or the H301 Local Operator Console STOP, START, and CLEAR pushbuttons. Cable A28 carries the X and Y selection signals from the AM03-A Low-Level Multiplexer to the AF16 Chrom Control. Channel selection is dependent on these two signals.

Cable A27 carries the LOW and HIGH FEEDBACK signals and the associated LOW and HIGH FEEDBACK gain signals. This cable is connected from the AF16 Variable Gain Amplifier control to the AG04 Variable Gain Amplifier. The gain factors in brackets pertain to high feedback and those not in brackets to low feedback.

3.2.6 Input/Output Bus Cable (See Figure 6-7)

This cable is connected from the PDP-8/I computer to the AF16 circuitry. The signals carried by each of these cables are indicated on the drawing.

3.3 AF17 LOC CONTROL LOGIC

3.3.1 Local Operator Console Control Logic (See Figures 3-7, 6-8, and 6-9)

The LOC control logic consists of eight identical channels 0 through 7. Circuitry for these channels is housed in one mounting panel along with IOT and BAC buffer logic. Any subsequent combinations of eight channels, up to the maximum of 64, are housed in their own separate mounting panels. The G704 modules located in A26 and B26 are clamp loads which are connected to the H300 or H301 LOC pushbuttons associated with each channel as shown in Figure 6-9.

Complementing each channel is an H300 or H301 LOC box. For purposes of simplicity, only channel 0 will be discussed. All other channels function in an identical manner.

The ANDing together of the IOT code 6172B, which is obtained from the IOT and BAC Buffer Logic (see Figure 6-8), and the channel 0 level, which is obtained from the LOC Channel Selector (see Figure 6-2), generates a strobe pulse. This pulse strobes the six IM 6 through 11 NAND gates allowing the H300 or H301 LOC box START, STOP, and CLEAR signals to be read into the PDP-8/I input mixer bus.

Input S to the IM 11 NAND gate is floating; consequently, when the strobe pulse is present, the IM 11 bit will be HI indicating to the operator that the IOT code 6172B and the signal from the selected channel are present. With this facility, it is not necessary to depress a LOC box pushbutton to determine the presence of these levels.

Inputs R and L to the IM09 and 10 NAND gates are tied to ground so that when they are ANDed with the strobe pulse they will give a HI out to the PDP-8/I bus. These two NAND gates do not perform any function in the GLC-8 System but are available for the inclusion of additional functions if required.

The channel 0 input level is also fed to two other NAND gates, one is associated with clearing the relay and light data registers and the other with setting the data registers.

When the channel 0 level is NANDed with the IOT code 6161B, a reset strobe pulse is generated initially clearing all data flip-flop registers (setting them in the zero state). In this state the lights will not illuminate because a LO output is present from the associated inverter and the relays will not pickup because a HI output is present from their associated inverters.

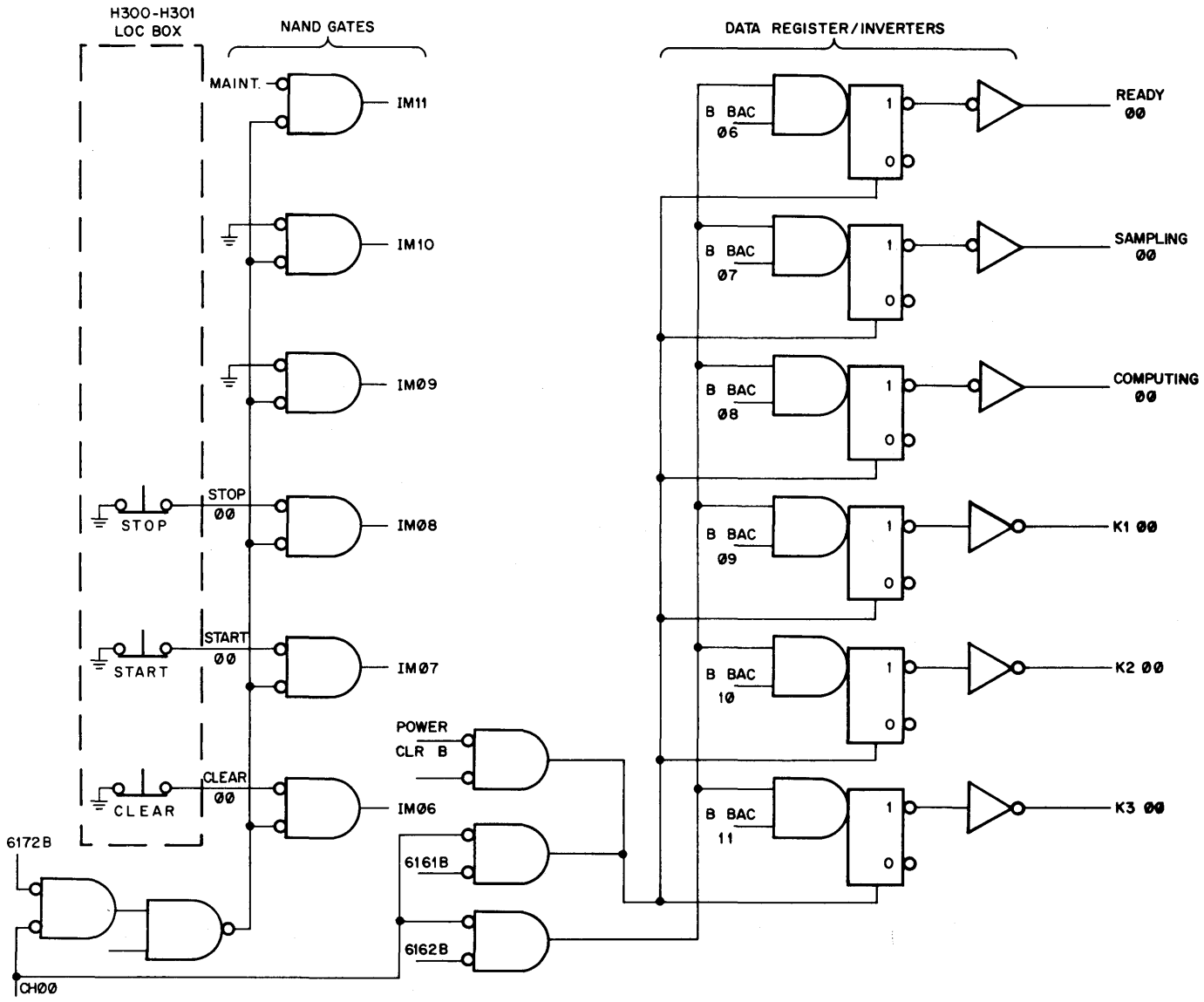


Figure 3-7 AF17 LOC Control Logic, Simplified Diagram

Following the clearing of the data registers, channel 0 is ANDed with the IOT code 6162B to generate a set strobe pulse setting the data registers in the one state. This allows the buffered BAC bits 6 through 11 to be read into the light and relay data registers.

If B BAC bit 6, 7, or 8 is present, the associated READY, SAMPLING, or COMPUTING lights will illuminate. On the other hand, when B BAC bit 9, 10, or 11 is present either relay K1, K2, or K3 will pickup.

When the GLC-8 System is initially turned on, the buffered power clear input (PWR CLR B) clears all of the data flip-flop registers, setting them to the zero state to prevent the relays from coming up in the wrong mode. This power clear level is generated in the AF16 and buffered in the AF17.

There is one set of clamp loads for each of the possible 64 LOC boxes which serve to discharge the cable capacity existing between the logic channels and the LOC pushbuttons when the latter are depressed. This neutralizes the capacity and provides faster switching.

3.3.2 H300-H301 Local Operators Console Cables (See Figure 6-10)

These cables connect the input and output signal levels from the AF16 to the AF17 and from AF17 to the H300 and H301 LOC.

Cables A30 and B30 carry the internally generated power clear signal to the AF17 and the IM levels to the PDP-8/I I/O bus. The A31 and B31 cables carry the BAC levels from the PDP-8/I I/O bus to the AF17 and the IOT instruction codes from the AF16 to the AF17.

One A32 cable is required for each AF17 mounted in the rack. For example, if there are four AF17 mounting panels mounted in the rack, then four A32 cables must be used. The first cable will carry channels 0 through 7, the second channels 10 through 17, the third channels 20 through 27, and the fourth channels 30 through 37 and so on until the full complement of channels has been interconnected (see Figure 6-17).

Cables A01 through A04, and B01 through B04, connect the light and relay input/output controlling levels from the H300 or H301 LOC to the AF17 logic control circuitry shown in Figure 6-7.

3.4 AG04 VARIABLE GAIN AMPLIFIER (See Figures 3-8 and 6-11)

The AG04 Amplifier is made up of two individual modules, one an A212 Variable Gain Amplifier and the other a W802 Relay Multiplexer.

The A212 module contains the high and low feedback gain components, a chopper stabilized amplifier module, high feedback gain adjustment controls, and an overload protection circuit. The W802 module consists of eight relay driver NAND gates, six for energizing the gain relays, and two for energizing either the LOW or HIGH FEEDBACK relays.

The selection of either the high or low gain is dependent on which relay driver NAND gate is enabled by a LO input. When a NAND gate has been enabled, the associated relay becomes energized, allowing the gain signal, connected to its contacts, to pass through to either the HIGH or LOW FEEDBACK bus. The relays are double-pole types with one set of contacts for the high feedback gain and the other for the low feedback gain.

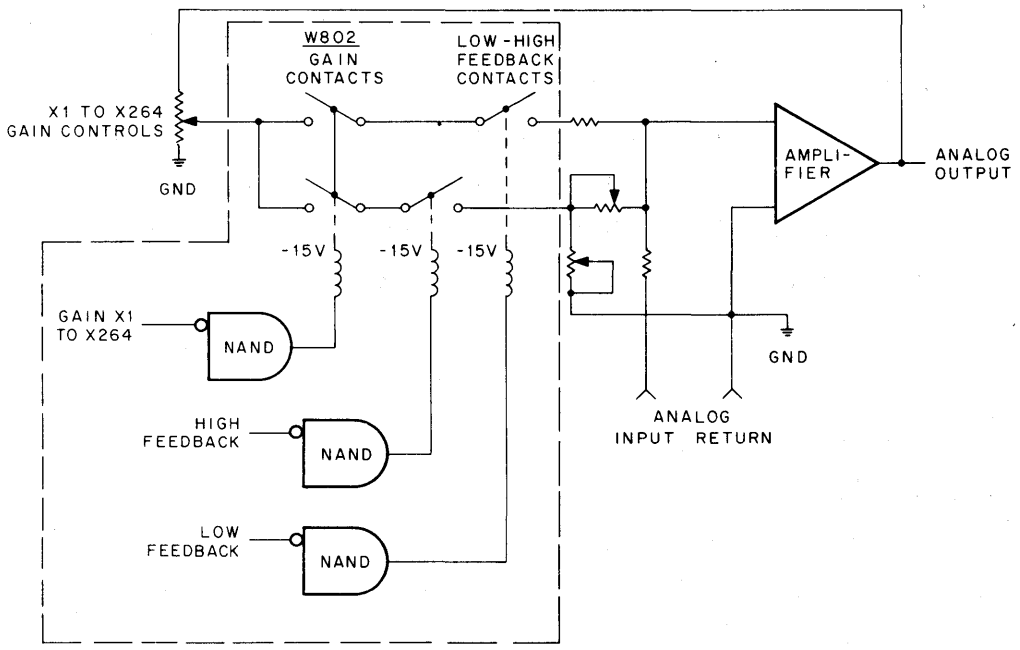


Figure 3-8 AG04 Variable Gain Amplifier, Simplified Diagram

3.5 DK01-A FOUR TIMES LINE FREQUENCY CLOCK (See Figures 3-9,3-10, 3-11, and 3-12)

The clock generates an output frequency which is four times that of the input line frequency. The input frequency to the clock is the 50 or 60 Hz from the filament transformer.

The line frequency sine wave input is fed into the A310 module, which functions as an integrator, inverter, and comparator. The input sine wave is integrated and inverted; the resulting two sine waves are displaced from each other by 90 degrees. These sine waves are then fed into the comparator circuit, which generates two square waves, 90 degrees out-of-phase with each other. Refer to Figure 3-9.

For purposes of simplicity, only the upper circuit, shown on Figure 6-12, will be discussed (both the upper and the lower section are identical).

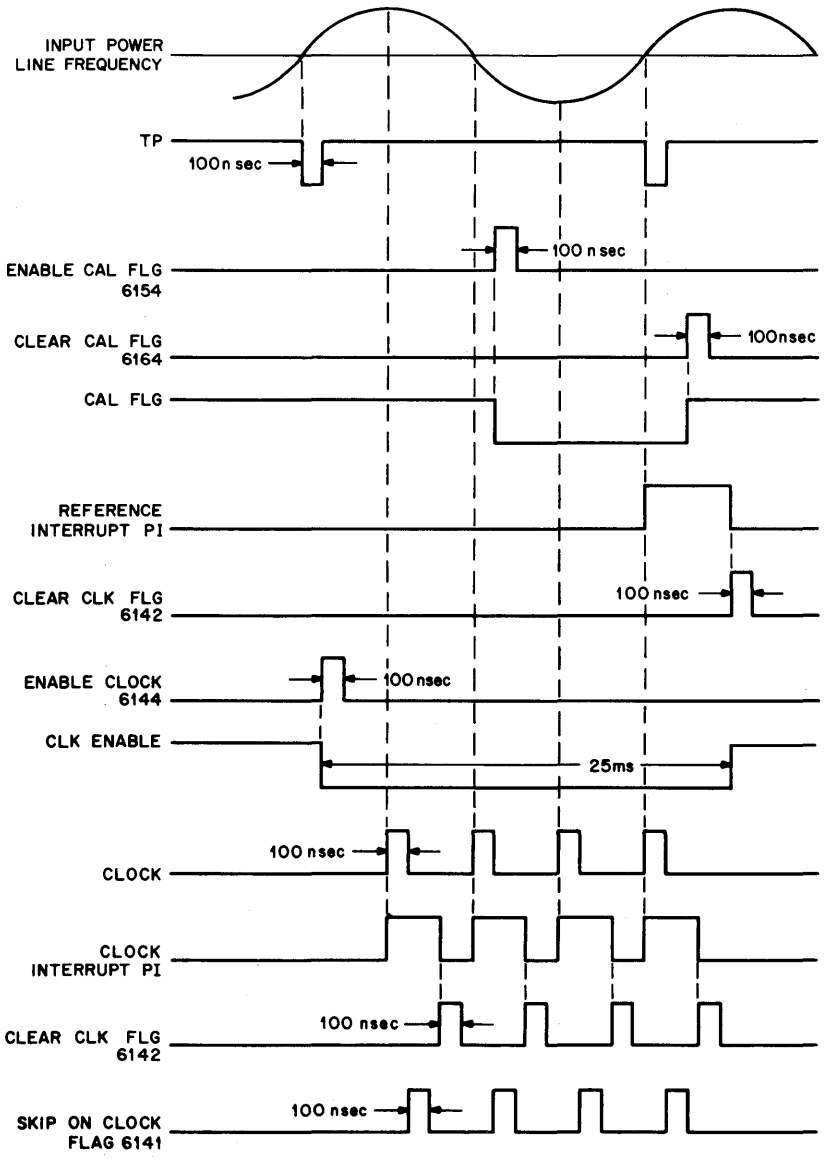


Figure 3-9 DK01A Timing Diagram

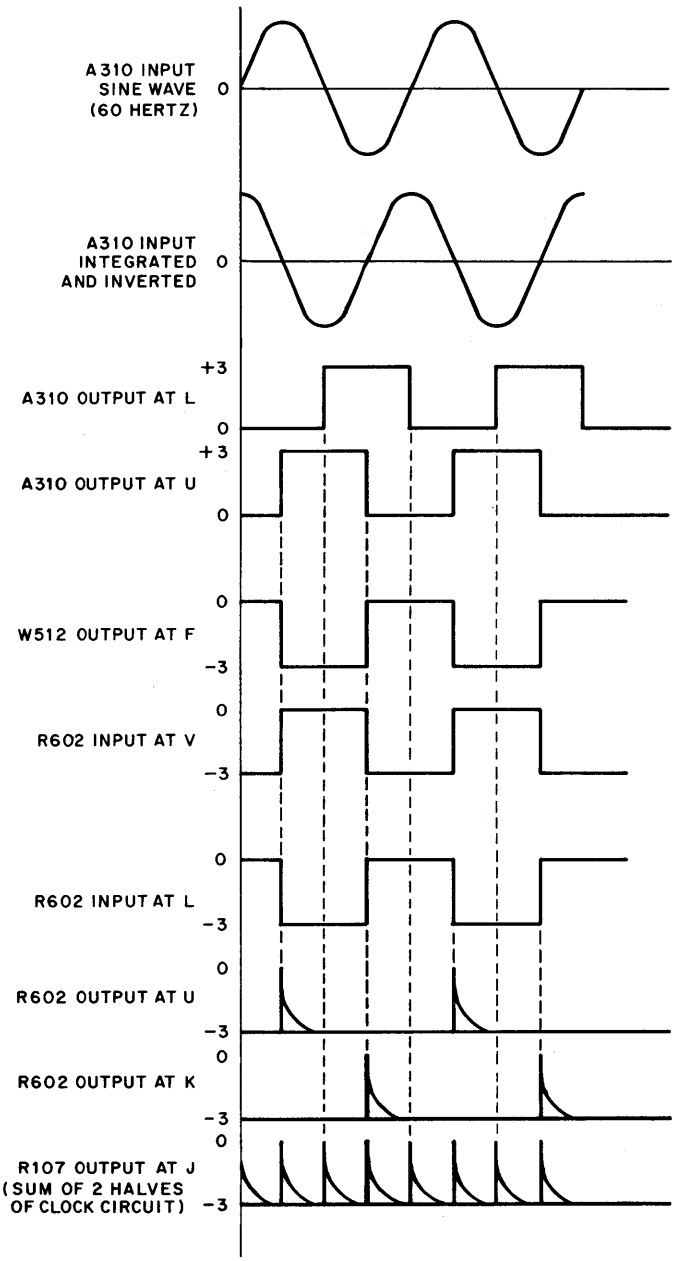


Figure 3-10 Four Times Line Frequency Clock Pulsetrain

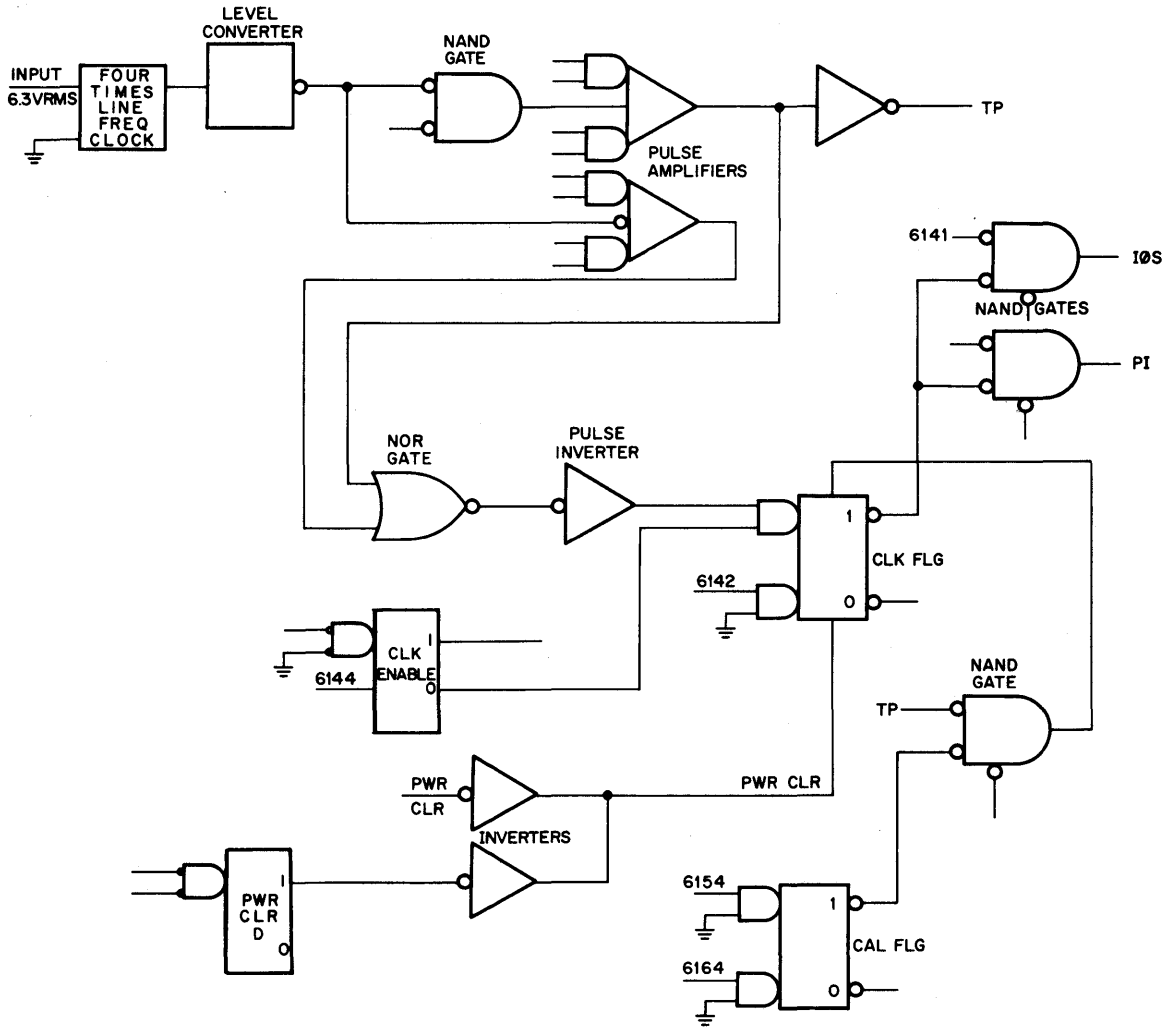


Figure 3-11 Four Times Line Frequency Clock, Simplified Diagram

The output square wave from A310 is fed to the input of the W512 level converter, which converts the square wave input positive logic level to a LO negative logic output. This LO negative logic is then fed to NAND inverter R121 and the R602 pulse amplifier.

The LO input to the R121 NAND inverter enables this stage, providing an output positive going square wave which is fed to the R602 pulse amplifier, where the input square wave is converted to a positive-going output pulse.

The W512 LO negative logic output level is also fed to a second R602 pulse amplifier which places it 180 degrees out-of-phase with the output from the R121 NAND gate inverter. The R602 pulse amplifier outputs are now 180 degrees out-of-phase with each other. The signals are then fed to the R121 NOR gate, which inverts them to LO outputs. They are, in turn, fed to inverter R107. The output from the inverter is a pulse train of positive-going pulses four times that of the input 50 or 60 Hz line frequency.

IOT instruction 6144 sets the R303 integrating one-shot in the zero state (25 ms). The HI output from the zero side of R303 is ANDed with the clock pulses to set the CLK FLAG flip-flop. The output from the one side enables the PI NAND gate R111 causing a program interrupt (PI) to the PDP-8/I.

When the program has recognized this event by testing the CLK FLAG flip-flop with an IOS pulse, generated by ANDing together the flag flip-flop output and the IOT instruction 6141, it issues the IOT instruction 6142 which causes a skip on the CLK FLAG flip-flop. When this is recognized by the program, a one is added to memory. This instruction inhibits the PI and IOS NAND gates.

When the PDP-8/I is initially turned on, the internally generated power clear pulse clears both the CLK FLAG and CAL FLG R202 flip-flops and the Digital Output Register, setting them all to the zero state. The CAL FLG HI output inhibits the R111 NAND gate to prevent the generation of PI and IOS pulses.

A 6154 IOT instruction sets the R202 CAL FLG flip-flop to the one state with the LO output from one side combining with the timing pulse (TP) to enable the R111 NAND gate. The HI output from this NAND gate sets the TIMING PULSE flip-flop to the one state. Its LO output enables the PI NAND gate, thereby generating a program interrupt. This LO output is also fed to the IOS NAND gate, which are enabled when the 6141 IOT instruction is present.

The IOT instruction 6164 clears the CAL FLG flip-flop setting it to zero state, thereby inhibiting the TP NAND gate.

3.6 H303 AMPLIFIER MOUNTING PANEL (See Figures 6-13 and 6-14)

This mounting panel houses the buffer amplifiers and filter, the function of which is to amplify and filter the input chromatograph analog signals. Located on the right hand side of this panel, are individual chromatograph channel input signal connectors, identified as CH0 through CH8 and two output connectors J1 and J2.

The analog signal from each chromatograph connected on the line is looped from the channel input connectors through the buffer amplifier and filter to the output connectors J1 or J2 for application to the H302 Mounting Panel.

Signals inputs on channel connectors CH0, CH1, CH4, and CH5 terminate in J1; and CH2, CH3, CH6, and CH7 terminate in J2.

3.7 H302 CONNECTOR PANEL ASSEMBLY (See Figures 6-15 and 6-16)

This panel assembly consists of 16 input connectors, J1 through J16, and two 32 channel output connectors, P1 and P2. The function of this panel is to take the analog output signals from J1 and J2 on the H303 Amplifier Panel and loop the signals through to the output connectors P1 and P2. From P1 and P2, the signals are then fed to the AM03 Low-Level Multiplexer.

The H302 Panel Assembly is interconnected to the H303 Amplifier Mounting Panel as shown in Figure 6-17.

NOTE

In Figure 6-17, note that the equipment is being viewed from the rear of the racks and not the front. When viewing the racks from the front, the view shown in the figure must be reversed.

3.8 INPUT BUFFER AMPLIFIER (See Figures 3-12 and 6-18)

There are two types of input amplifiers, A210 (gain of X1) and A211 (gain of X10). Both amplifiers operate identically.

The input to each amplifier is a high-impedance balanced differential stage. This high input impedance ensures that common-mode noise currents are held to a minimum and loading of the source is avoided. Because the input is differentially balanced, there is a high common-mode rejection ratio.

Common-mode noise currents are equal in both amplifier input terminal pins N and P. These currents generate equal voltage drops across the input resistors, causing a zero differential voltage at the input to the operational amplifier. As the amplifier responds only to differences in voltage, there will be no output due to the common-mode noise. A line balance trim is provided to compensate for source and cable unbalance, thereby maintaining equal common-mode noise currents in each input terminal. Two additional potentiometers are provided, one for zero offset balance and one for gain adjust.

Normal-mode noise is reduced by the use of capacitors in the feedback loop which in effect, reduce the bandwidth of the amplifier.

3.9 INPUT FILTER (See Figures 3-12 and 6-18)

There are two filter models. In earlier GLC-8 Systems the A213 filter was used, but in the later GLC-8 System, the A216 filter is used.

The A216 filter is an active low-pass, Butterworth-type filter with a cutoff frequence of approximately 2 Hz. A low-drift, low-noise operational amplifier is used with two frequency determining networks (poles) arranged to ensure a flat pass band and rolls off at a -12 db/octave rate beyond the cutoff frequency. The filter has a gain of -1; a 100K potentiometer is provided for zero balancing.

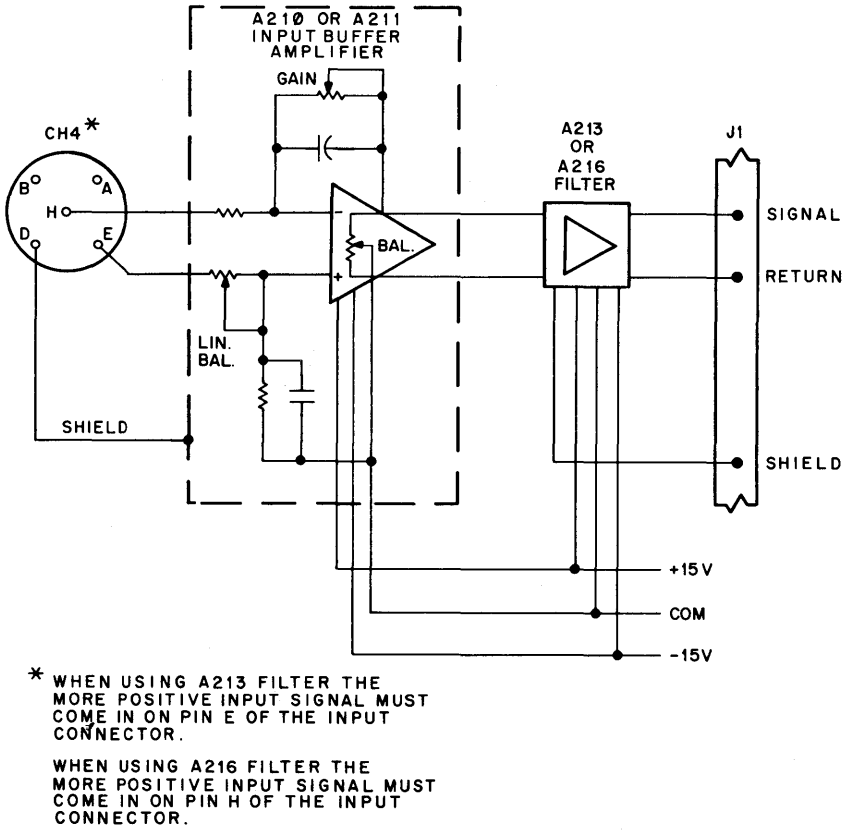


Figure 3-12 Input Buffer Amplifier, Simplified Diagram

3.10 POWER SUPPLIES

3.10.1 H713 Dual ± 15V Power Supply (See Figures 6-19 and 6-20)

This equipment is a dual ±15 Vdc floating regulated power supply which provides the required power for the GLC-8 System. The current provided by each 15V supply is a 1.5A and the voltage regulation is 0.2 percent.

Each 15V output has overload protection capable of withstanding output shorts indefinitely. Ripple content of the output voltages is two mV RMS maximum.

Input power to the supply is 105 to 125 Vac at 47 to 400 Hz. Line voltage regulation is 0.05 percent.

3.10.2 +10, -15V Power Supply, Model 783 (See Figure 6-21)

This supply furnishes +10 and -15 Vdc to the GLC-8 equipments. Rectification is provided by diodes D1 through D4. Filtering is provided by C2 and R1 for the +10V output and C1 for the -15V output. The Power Supply specifications are outlined in the Performance Specification section of this manual.

The 783A Power Supply is identical to the 783, except that it is designed to operate from a 50 Hz line frequency.

3.10.3 Variable 0-20V Power Supply, Model 734B (See Figure 6-22)

This supply furnishes ± 0-20 Vdc to the equipments for purposes of margin checking logic racks. Rectification is provided by four 1N3208 diodes. Filtering is provided by C2 and R1. Both outputs are protected against overload conditions by the Slo-Blo fuse F1. The output voltages are monitored by the 0-30 Vdc meter.

Five output voltage connection points are provided for each of the +10 and -15V supplies (the five separate ground points are common to both supplies). When the +10, -15V select switch is in the 10V position, the -15V leg is connected to the ground terminals; when the switch is in the -15V position, the -10V leg is connected to the ground terminals.

The 734C Variable 0-20V Power Supply is identical to the 734B, except that it is designed to operate from a 50 Hz line frequency.

CHAPTER 4
INSTALLATION

This Chapter provides the necessary information for GLC-8 System installation. The gas chromatographs used in conjunction with the GLC-8 vary according to the individual application; consequently, the information in this Chapter is generalized. It is assumed that customer technical personnel will be available to determine the individual applications and environments of the equipment.

Figure 4-1 illustrates the equipments (mounted in the H961 cabinet) which make up the analog and digital portion of the GLC-8 System. The equipments mounted in the PDP-8/I computer cabinet make up the basic computer system.

Figure 6-23 depicts the GLC-8 System interface cable connections, Figure 6-24 shows the physical size of the H961 cabinet, and Figure 6-25 shows the AF17 assembly wiring.

4.1 MECHANICAL

The following dimensions pertain to two GLC-8 H961 analog and digital cabinets and the PDP-8/I computer cabinet mounted side-by-side:

Width: 62-1/8 inches

Height: 71-11/32 inches

Depth: 48-1/8 inches (includes analog and digital dress panel and PDP-8/I cabinet rear door open)

4.1.1 LOC Box

The outline dimensions, mounting hole pattern, and location of connectors of the LOC are shown in Figure 4-2.

4.2 PARTS REQUIRED FOR PRE-INSTALLATION

Table 4-1 lists the parts supplied with each AF08 Interface for installation of the GLC-8. It should be noted that the table lists the unit quantity of parts required to interface a gas chromatograph, not the total quantity to interface a GLC-8 System. The total quantity of parts required for a particular installation is determined by the number of gas chromatographs, and LOCs on-line with the GLC-8.

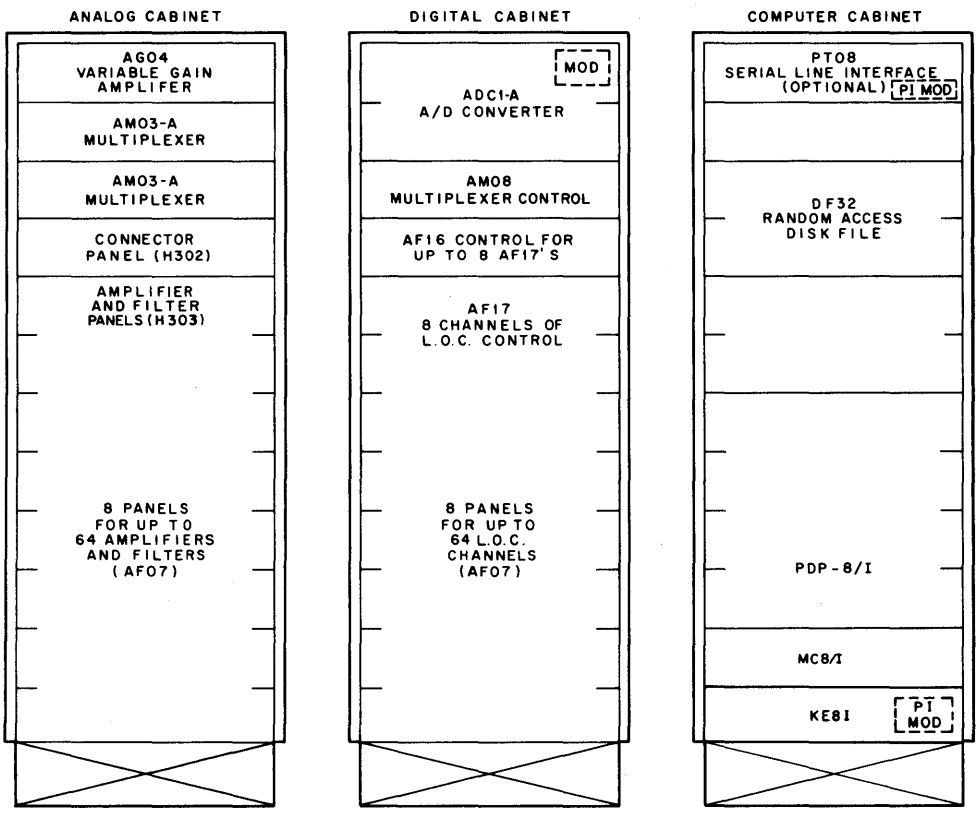


Figure 4-1 Equipment Location in H961 Rack Diagram

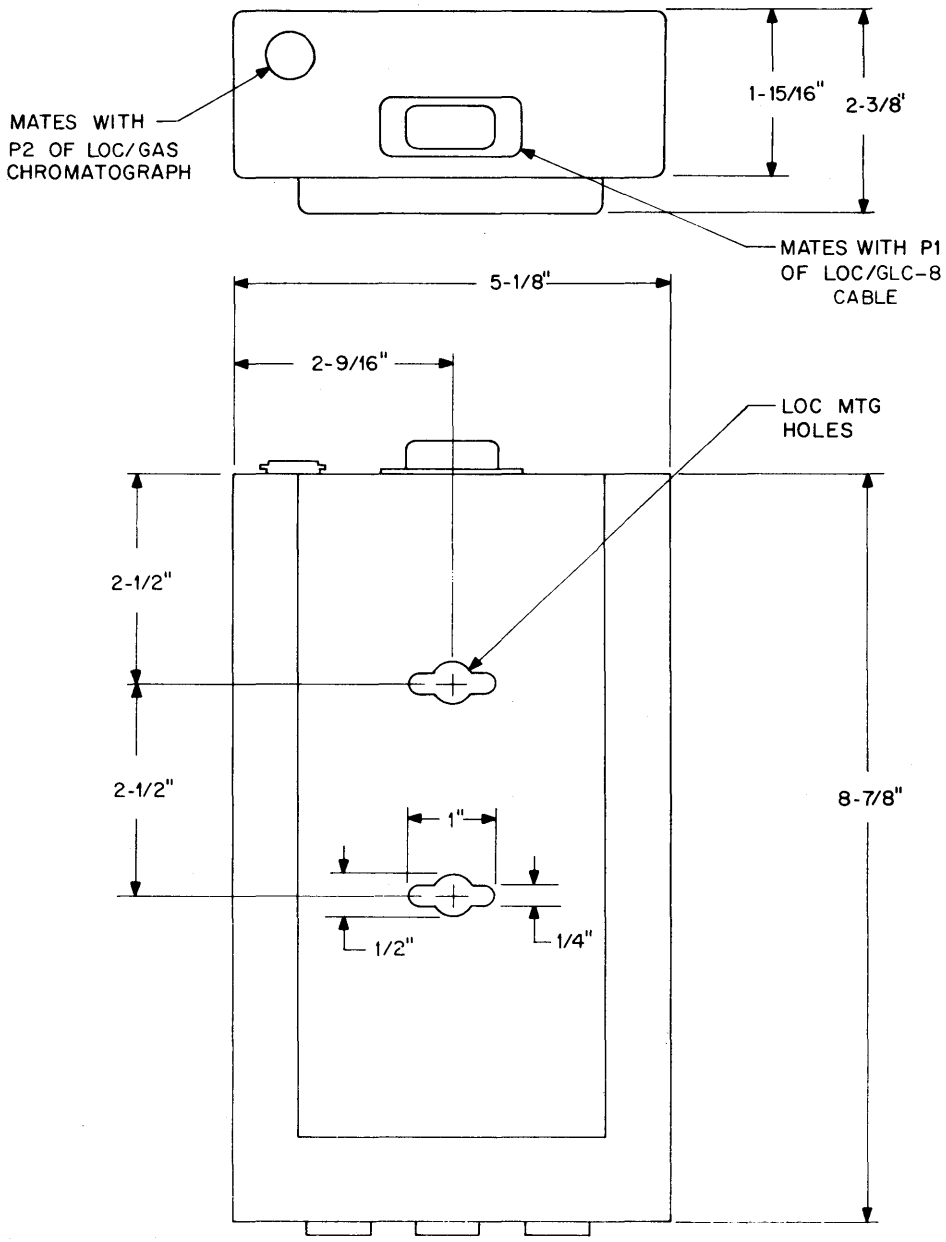


Figure 4-2 Local Operator Console, Outline Drawing

NOTE

The following parts, necessary for making up the GLC-8 cables, are furnished to the customer prior to his receiving the GLC-8 system. This allows him to install these cables immediately upon receipt of his equipment. The cable connector part numbers are listed here for reference purposes only.

Table 4-1
Parts Required for Installation

Name	Part Number	Quantity	Use
Connector	57-30140 (DEC Stock No.)	1	Part of cable assembly used to interface LOC H300 or H301 at the LOC
Connector	126-195 (Amphenol)	1	Part of cable assembly used to interface relays of LOC H301 with gas chromotograph at the LOC
Connector, Module	W023	1	Part of cable assembly used to interface LOC H300 or LOC H301 with GLC-8 at the GLC-8
Connector	126-217 (Amphenol)	1	Part of cable assembly used to interface GLC-8 with gas chromatograph at the GLC-8

4.3 PARTS REQUIRED BUT NOT SUPPLIED

Table 4-2 lists the cables that are required for installation but not supplied.

4.4 POWER REQUIREMENTS

The GLC-8 requires a power source of 115 ± 17V, 60 ± 0.5 Hz at 20A minimum. The equipment is available upon request to operate from a 220 ± 33V, 50 ± 0.5 Hz single-phase power source or from a 110 ± 15V, 50 ± 0.5 Hz single-phase power source. The normal source of power (115V) must be equipped with a 30A 3-Terminal Hubbell twist-lock receptacle (DEC Part #12-3485, Hubbell Cat. #331) to accommodate the power cable of the GLC-8. Optional equipment, such as the LOC and teletype receive power from the GLC-8. The teletype has its own ac power cord which can be connected directly to an external source other than the GLC-8.

Table 4-2
Parts Required Not Supplied

Name	Part Number	Description
GLC-8/Gas Chromatograph Cable	8762 (Belden)	Wire: 20 AWG, twisted pair, shielded.
LOC/GLC-8 Cable (H300 or H301)	8457 (Belden)	Wire: 22 AWG, 12-conductor cable.
LOC/GAS Chromatograph Cable (H300)	8456 (Belden)	Wire: 22 AWG, 10-conductor cable.

4.5 ENVIRONMENTAL CONSIDERATIONS

The PDP-8/I (the computer base of the GLC-8) can operate at an installation with an ambient temperature from 32° to 122° F (0° to 50° C) with no degradation in performance. However, when dealing with the temperature sensitive differential isolation amplifiers, found at the analog interface of the GLC-8, consideration must be given to rapid changes in ambient temperatures, a one-degree centigrade change in temperature can produce 50 μV drift when using the A210 amplifier and a 300 microvolt drift when using the A211 amplifier. (The baseline correction algorithm of the GLC-8 will compensate for slow changes in ambient temperature.)

CAUTION

To avoid sudden changes in temperature, the GLC-8 should not be located near windows, thermostatically controlled blowers, and other areas where sudden changes in temperature may occur.

4.6 INSTALLATION CONSTRAINTS AND RECOMMENDATIONS

There are several vital factors that must be considered when transmitting the low-level analog signals of the gas chromatograph to the GLC-8. The most significant of these are:

a. normal-mode noise

b. common-mode noise

c. distance between transducer and computer.

These factors are of paramount importance in obtaining accurate gas chromatography results.

4.6.1 Normal-Mode Noise

Normal-mode noise arises from electromagnetic fields and other sources of noise penetrating the loop formed between the signal wires. This type of noise can be minimized by the use of two-conductor, twisted-pair shielded wire with the shield covered by an insulator. (The recommended Belden Type 8762, Table 4-2, is an excellent example of this type of cable.) Although tests have shown that the effects of induced noise are minimal using this type of cable, it is recommended that additional precautions be taken, for example:

a. Signal cables should not be run with power or other high voltage cables.

b. Cables should be run perpendicular to the electromagnetic fields produced by unshielded transformers and motors.

c. Cables should be run out of the way of flourescent lamps and other sources of high frequency noise.

d. Cables should be run in conduit or floor trenches so that signal leads are completely isolated.

4.6.2 Common-Mode Noise

Common-mode noise arises as a result of differences in the ground reference planes of the gas chromatograph and the GLC-8. The GLC-8 has a common-mode rejection of 120 db at 50/60 Hz. Hence, for each volt of common mode noise introduced, 1 μV of common-mode noise is seen at the A/D converter. To ensure minimal common-mode noise, the shield of the GLC-8/gas chromatograph cable should be driven at the same potential as the signal return line. This is accomplished by returning the signal return and the shield to common ground at the gas chromatograph and floating the shield at the GLC-8.

Ground currents flowing between the GLC-8 and the gas chromatograph will appear as common mode voltage at the GLC-8 interface. The isolation amplifier at the input of each channel of the GLC-8 is a balanced differential amplifier. Ground currents flowing equally in the signal and signal return lines are, therefore, rejected.

4.6.3 Ground Currents

Analog Signal Cables Length - The minimum-noise system is further constrained by the distance between the GLC-8 and the gas chromatograph. From tests performed in DEC's test laboratories, it has been observed that analog signal cables can be run 500 ft under unfavorable conditions, with no degradation in gas chromatography accuracy. Since the specifications of various gas chromatographs differ, it is impossible to specify the maximum distance that the GLC-8 may be located away from the gas chromatograph. The customer should determine the greatest distance at which he can operate his

strip-chart recorder and use this as the criterion for extablishing the maximum distance permissible between the GLC-8 and gas chromatograph.

4.7 CABLE FABRICATION

Cables should be fabricated according to the instructions contained in the following paragraphs. The length of cables is determined by the demands of the installation and the constraints cited in the installation and planning section. Cables should be checked for continuity and isolation resistance after fabrication using a suitable multimeter.

4.7.1 Gas Chromatograph/GLC-8 Cable Assembly

The cable interfacing each gas chromatograph connected on-line with the GLC-8 should be fabricated in accordance with Figure 4-3. The cable, at the gas chromatograph end, should be tinned or equipped with lugs depending on the method of termination.

4.7.2 LOC/GASCHROM-8 Cable Assembly

The cable interfacing each LOC, both H300 and H301, to the GLC-8 should be fabricated in accordance with Figure 4-4.

4.7.3 LOC/Gas Chromatograph Cable Assembly

The cable interfacing the relays of the LOC H301 with the gas chromatograph should be fabricated in accordance with Figure 4-5. This cable is not required for the H300 LOC.

4.7.4 Teletype ASR-33 (Optional)/GLC-8 Cable Assembly

Teletype cable assemblies are supplied with the ASR-33 Teletype according to the length specified by the customer.

4.8 CABLE INSTALLATION

Installation consists of connecting the Gas Chromatograph/GLC-8 cable assembly (see Figure 4-3) to the gas chromatograph, routing the cabling through conduit to the selected location for the installation and planning section. The suggested procedure is as follows:

a. As shown in Figure 4-6 the cable assembly should be connected to the output of the electrometer amplifier or the thermo-conductivity cell ahead of the strip-chart recorder attenuator. A change of inverted attenuation while the gas chromatograph is on-line with the GLC-8 will cause a discontinuity of signal and corresponding in-accurate gas chromatography results.

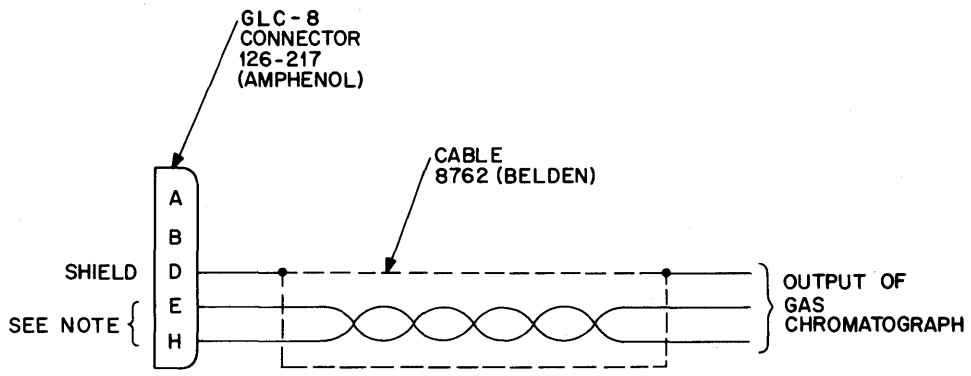


Figure 4-3 Gas Chromatograph/GLC-8 Cable Assembly, Fabrication Drawing

NOTE

When using A213 filter the more positive input signal must come in on Pin E of the input connector.

When using A216 filter the more positive input signal must come in on Pin H of the input connector.

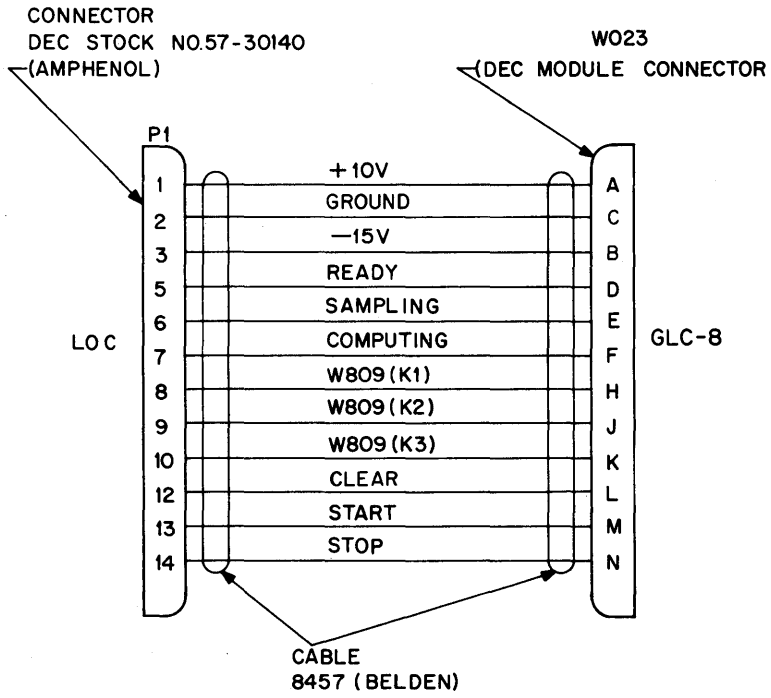


Figure 4-4 LOC/GLC-8 Cable Assembly, Fabrication Drawings

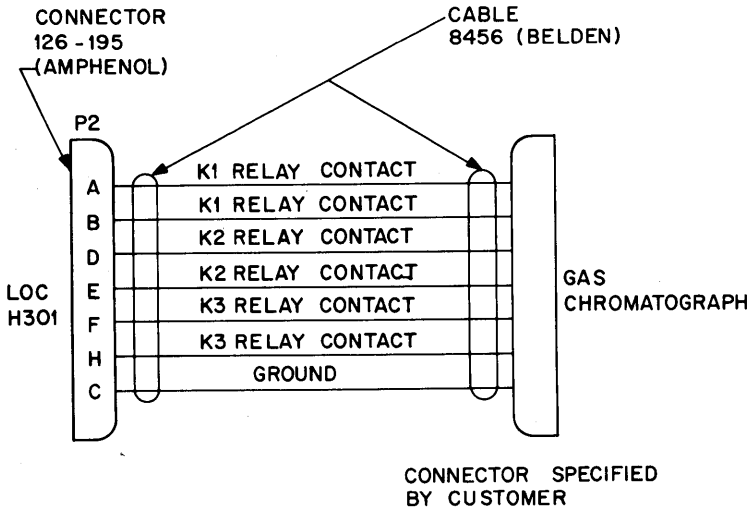


Figure 4-5 LOC/Gas Chromatograph Cable Assembly, Fabrication Drawing

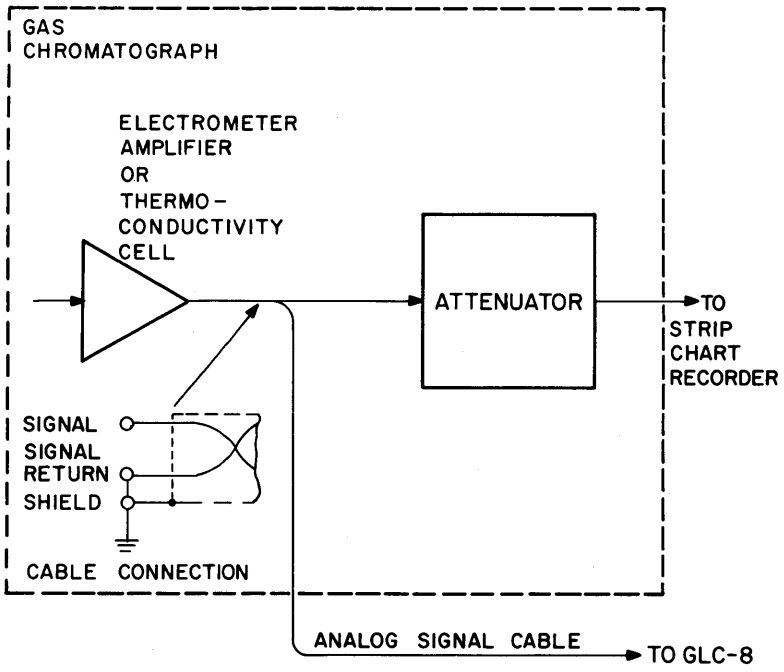


Figure 4-6 Installation of Analog Cable Assembly

b. Both the signal return line and the shield should be terminated at signal ground at the gas chromatograph, as shown in Figure 4-6 and the shield floated at the GLC-8. Refer to the installation and planning section.

c. On completion of the installation of the cable assembly, the common-mode noise content of the installation is measured to determine the error introduced into the system due to common-mode noise. The output of the gas chromatograph is measured from both signal line to shield and from signal return line to shield at the GLC-8 connector with an oscilloscope and preamplifier. The test set-up for measurement of common-mode noise is shown in Figure 4-7. As previously mentioned, the system has a common mode rejection ratio of 120 db, at 60 Hz with a worst case source unbalance of 1000 ohms. Therefore, for each volt of common-mode voltage measured, one microvolt of noise will be seen at the A/D converter. If the minimum signal output of the gas chromatograph is 10 μV, it follows that the maximum noise that the system can tolerate is 10V. If the measured common-mode noise is 10V or greater, the grounding system of the gas chromatographs should be modified as indicated in the installation and planning sections.

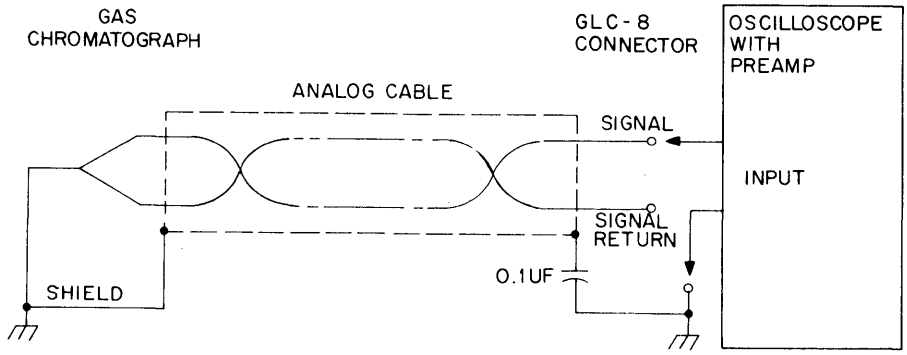


Figure 4-7 Common Mode Noise Analysis Test Setup

4.8.1 Power Cable

The H961 Cabinets housing the GLC-8 equipments have only one 115 Vac receptacle. Power may be turned ON or OFF from the PDP-8/I operator's console.

4.8.2 GLC-8, Analog and LOC Cable Runs

These cables are connected to the H961 Cabinets through a drop panel in the bottom of the cabinets. Subflooring, although desirable, is not necessary, because casters elevate the cabinets from the floor to give sufficient cable clearance.

4.8.3 H300 Local Operator Console

Cables which interconnect the H300 LOC to the AF17 digital control logic circuitry are shown in Figure 4-8, 6-7, 6-8, and 6-9.

4.8.4 H301 Local Operator Console

The cable which interconnects the H301 LOC to the AF17 digital control logic circuitry is shown in Figures 4-9 and 6-30.

4.8.5 Interfacing of Equipments

H300 and H301 LOC and analog signal interfacing is accomplished using the cables shown in Figures 4-8 and 4-9.

4.9 MODULE LOCATIONS IN MOUNTING FRAMES

The drawings listed below show the exact location of the modules in their mounting frames within the GLC-8 System,

AF16 Control Logic, Figure 6-31

AF17 LOC Control Logic, Figure 6-32

AG04 Variable Gain Amplifier, Figure 6-33

4.10 ASSOCIATED EQUIPMENT PUBLICATIONS

During installation of the GLC-8 System, the following publications are available to facilitate installation:

GLC-8 Diagnostic MAINDEC 8I-D6

Low Level Multiplexer Diagnostic AM03/AM08 MAINDEC-08D60A-D-D

Analog-Digital Converter ADC1-A, (Model AF01)

PDP-8/I Multiplexer Subsystem DEC-08-H6AA-D

GLC-8 Chromatographers User's Guide DEC-CP-GAYA-D

PDP-8/I Maintenance Manual DEC-8I-HR1A-D

Extended Arithmetic Element (EAE), Model KE8/I

Memory Extender, Model MC8/I

Disk, Model DF-32

4.10.1 Optional Equipment Publication

The following publication pertains to the teletype which interfaces with the GLC-8 System.

Teletype System, Model PT08

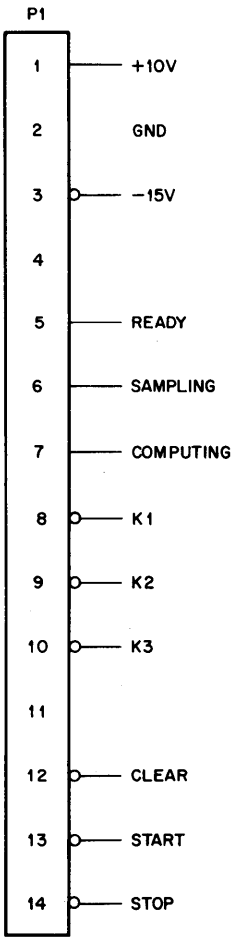


Figure 4-8 H300 Interface Cable

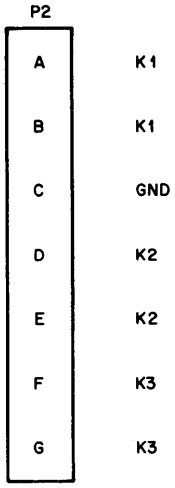


Figure 4-9 H301 Interface Cable

CHAPTER 5
MAINTENANCE

5.1 GENERAL

This Chapter contains the information necessary to maintain the GLC-8 System. When operated under normal conditions, the system requires very little maintenance (periodic performance of diagnostic programs, cleaning, and inspection). If preventive maintenance is required, follow the procedures outlined in this Chapter to return the equipment to optimum operating efficiency.

If a component or module requires replacement, obtain the description from the recommended spare parts list outlined in this Chapter.

Do not replace a faulty component without first determining the cause of the failure. Refer to the Block Schematics associated with each module to determine the location of the components in question.

When conducting a maintenance analysis on the system, make certain that the input conditions required to produce a specified output are met; otherwise, erroneous output readings will result, indicating a non-existing fault.

5.2 SPECIAL MAINTENANCE IOT INSTRUCTIONS

The function of the special maintenance IOT instructions 6154 and 6164 are fully described in Operation and Programming, Chapter 2, paragraph 2.3.

5.3 GLC-8 KEY SHEET

A key sheet (KS) is provided with each GLC-8 System and is relevant only to the particular system. The KS documents the standard options, special features, and the system and installation drawings incorporated into each GLC-8 System.

If a customer has a question concerning his system, it is important that he provide DEC personnel with all relevant information on this sheet, including serial and drawing numbers.

5.4 MASTER DRAWING LIST

A master drawing list (MDL) is provided on each KS for each option in a GLC-8 System. The MDL for a particular piece of equipment provides the user with a complete breakdown of all drawings common to that equipment. If drawings are to be ordered for customer use, or for service consultation, the complete drawing number must be specified in order to provide fast and efficient service.

5.5 GLC-8 MAINDEC 8I-D6BA-(D) DIAGNOSTIC PROGRAMS

The GLC-8 diagnostic programs are used to test the unique hardware features of the system that cannot be tested with existing MAINDECs. The features include the real-time clock, special interrupt modifications, LOC boxes, and programmable amplifier.

The programs are designed to facilitate troubleshooting by selectively exercising every circuit in the machine. Instructions and procedures for loading, operating, and interpreting the results of diagnostic tests are written in clear, concise language for beginning maintenance personnel.

Detailed error messages are printed out to tell the maintenance personnel exactly which instruction, or bit configuration, has failed. Error codes direct the troubleshooter to specific modules when a fault condition is detected.

The program tests are divided into five sections. The first tests the real-time clock, with tests on flags, interrupts, clock enable logic, and stability and repeatability.

For the second program, there is a special option to inhibit the interrupts of the AD converter, TTY, and the PT08. These devices are tested to determine if their flag may be raised without causing an interrupt, and all other devices are tested to see when a flag is raised that an interrupt is also raised.

The third section tests to see that the local operator consoles may be selected and the computer can read the status of the push-buttons, and that the LOC box console lights can be controlled by the PDP-8/I.

The fourth section is a check of the programmable gain amplifier. In most of the tests, errors are detected by the PDP-8/I; scope loops are a function of the switch register. For LOC channel selection, most error detection requires operator observance.

5.6 H300 AND H301 LOC CABLE CONNECTORS

Figure 5-1 shows the LOC input/output cable connectors and the signal termination points.

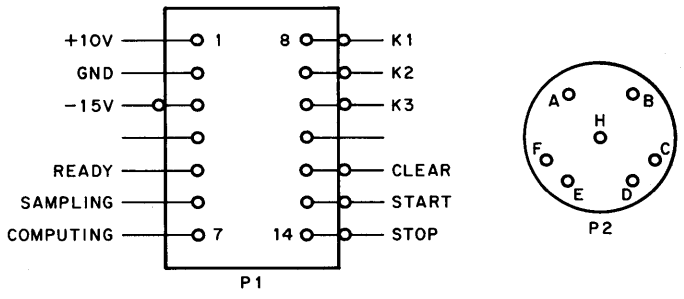


Figure 5-1 H300 and H301 LOC
Cable Connectors

5.7 H303 INPUT PANEL CONNECTOR

Figure 5-2 shows the H303 Input Panel connector and the signal termination points.

Connector Pin	Signal
D	Shield
H	See Note
E	See Note

NOTE

When using the A213 filter, the more positive input signal must come in on pin E of the input connector with the return on pin H.

When using the A216 filter, the more positive input signal must come in on pin H of the input connector with the return on pin E.

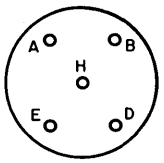


Figure 5-2 H303 Input Panel Connectors

5.8 PREVENTIVE MAINTENANCE

A systematic preventive maintenance program can be a useful tool to avert system failures. Proper application of a preventive maintenance program is an aid to both serviceman and user, since detection and prevention of probable failures can substantially reduce maintenance and downtime.

Scheduling of computer usage should always include time for maintenance purposes. Careful diagnostic testing can indicate problems which may only occur intermittently during on-line operation.

Weekly program checks and thorough preventive maintenance should be followed, based on the following criteria:

electrical - 1000 hours

mechanical - 500 hours

or at least quarterly.

5.8.1 Preventive Maintenance Tasks

The following tasks should be performed quarterly:

a. Clean the exterior and interior of the equipment cabinet using a vacuum cleaner, air blower, or a brush with long soft bristles, and/or cloths moistened in nonflammable solvent. If an air hose is used for cleaning, do not disturb components or wiring.

b. Clean the air filter by removing the retaining bar and machine screw. Use a vacuum cleaner to remove accumulated dirt and dust. Replace filter in the GLC-8 racks.

c. Lubricate hinges, slide mechanisms, and casters, with a light machine oil. Wipe off excess oil.

d. Visually inspect equipment for general condition. Repaint any scratched areas with DEC black paint or Krylon glossy white No. 1501.

e. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strains and mechanical security. Tape, solder, or replace any defective wiring or cable covering.

f. Inspect the following for mechanical security: keys, switches, control knobs, lamps, connectors, transformers, fans, capacitors, etc. Tighten or replace as required.

g. Inspect all module mounting panels to ensure that each module is securely seated in its connector. Remove and clean any module which may have collected dirt or dust due to improper air filter servicing.

h. Inspect power supply components for leaky capacitors, overheated resistors, etc. Replace any defective components.

i. Check the output voltage and ripple content of the H713 power supply as specified in the Performance Specifications. Use a multimeter to make these measurements without disconnecting the load. Use an oscilloscope to measure p-p ripple on all dc outputs of the supply. The outputs of the supplies are adjustable; therefore, if any output voltages are not within the specified tolerance, readjust the output voltages. If the desired output voltages are not attainable, initiate power supply maintenance. Refer to the block schematic associated with the power supply in question. If ripple content is not within specifications, the supply is considered defective and corrective maintenance should be performed.

j. Run all GLC-8 programs to verify proper equipment operation. Each program should be allowed to run for at least 10 minutes.

k. Perform all preventive maintenance operations for each peripheral device included in the system.

l. Enter preventive maintenance results in the log book.

m. Run voltage margins while running diagnostics.

n. While running the diagnostics, vibrate the modules and wiring panels.

o. While running the diagnostics, check all analog adjustments.

5.9 CORRECTIVE MAINTENANCE

The GLC-8 System is constructed of highly reliable modules. The reliability of these circuits, in conjunction with performance of the preventive maintenance tasks ensures relatively little equipment downtime due to failure. If a malfunction occurs, maintenance personnel should analyze the condition and correct it as indicated in the following procedures. The following test equipments are required:

a. broad band-width oscilloscope,

b. Tektronix Type P6019 current probe,

c. multimeter

It is virtually impossible to outline any specific procedures for locating faults within complex digital systems such as the GLC-8. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should become thoroughly familiar with the system concept, the logic drawings, the operation of specific module circuits, and the location of mechanical and electrical componets. Diagnosis and remedial action for a fault condition can be undertaken logically and systematically in the following phases:

a. Preliminary Investigation

b. System Troubleshooting

c. Logic Troubleshooting

d. Circuit Troubleshooting

e. Repair/Replacement

f. Validation Tests

g. Recording

5.9.1 Preliminary Investigation

Before commencing troubleshooting procedures, explore every possible source of information. Analyze the problem before attempting to troubleshoot the system. Gather all available information from users who have encountered the problem, and check the system log book for any previous references to the problem.

Do not attempt to troubleshoot by use of complex system programs alone. Run the GLC-8 MAINDEC 8I-D6BA-(D) Diagnostic programs and select the shortest, simplest program available which exhibits the error conditions. GLC-8 programs are carefully written to include program loops for assistance in system and logic troubleshooting.

5.9.2 System Troubleshooting

When the problem is understood and the proper program has been selected, the logic section of the system at fault should be determined. Obviously, the program which has been selected gives a reasonable idea of what section of the system is failing. However, faults in equipment which transmit or receive information, or improper connection of the system, frequently give fault indications similiar to those caused by computer malfunctions.

Disconnect any peripheral devices which are not necessary to operate the program. At this time, reduce the program to its simplest scope loop and duplicate this loop in a dissimilar portion of memory to verify, for instance, that an operation failure is not dependent upon memory location. This process can aid in distinguishing memory failures from processor failures. Use of the techniques described above often pinpoints the problem to a few modules.

5.9.3 Logic Troubleshooting

Before attempting to troubleshoot the logic, make sure that proper and calibrated test equipment is available. Always calibrate the vertical preamp and probes of an oscilloscope before using. Make sure the oscilloscope has a good ac ground and keep the dc ground from the probe as short as possible.

Use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep can be synchronized by control pulses or by level transitions which are available on individual module terminals at the wiring side of the logic.

CAUTION

When probing the logic, do not short between pins. Shorting of signal pins to power supply pins may result in damaged components.

5.9.4 Circuit Troubleshooting

Engineering schematic diagrams of each module are supplied with the GLC-8 System; refer to these diagrams for detailed circuit information.

Visually inspect the module on both the component side and the printer wiring side to check for overheated or broken components or etch. If this inspection fails to reveal the cause of trouble or to confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

To avoid damaging components, do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20Ω forward and more than 1000Ω reverse. If readings in each direction are the same and no parallel paths exist, replace the diode.

Measure the emitter-collector, collector-base, and emitter-base resistances of transistors in both directions. Short circuits between collector and emitter, or an open circuit in the base-emitter path, cause most failures. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100Ω resistance exists between the emitter and the base, or between the collector and the base in the forward direction, and an open circuit condition exists in the reverse direction. To determine forward and reverse directions, consider a transistor as two diodes connected back to back. In this analogy, PNP transistors would have both cathodes connected together to form the base, and both the emitter and collector assume the function of an anode. In NPN transistors, the base would be a common-anode connection; and both the emitter and collector, the cathode.

Multimeter polarity must be checked before measuring resistance, because many meters apply a positive voltage to the common lead when in the resistance mode.

As ICs contain complex integrated circuits with only the input, output, and power terminals available, static multimeter testing is limited to continuity checks for shorts between terminals. IC checking is best done under dynamic conditions using a module extender to make terminals readily accessible. Using GLC-8 logic diagrams and module schematics, proceed as follows to locate an IC on a circuit board:

Step	Procedure
1	Hold the module with the handle in your left hand; component side facing you.
2	ICs are numbered starting at the contact side of the board, upper right hand corner.
3	The numbers increase toward the handle.
4	When a row is complete, the next IC is located in the next row at the contact end of the boards (see Figure 5-3).
5	The pins on each IC are located as illustrated in Figure 5-4.

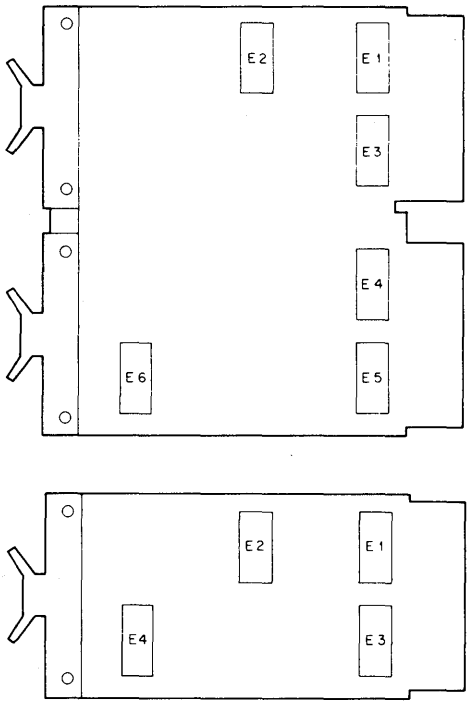


Figure 5-3 IC Location

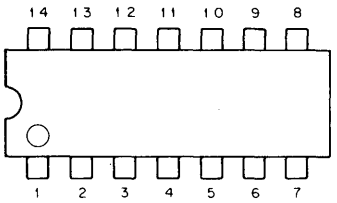


Figure 5-4 IC Pin Location

5.9.5 Validation Tests

Always return repaired modules to the location from which they were removed. If a defective module is replaced by a new one while repairs are being made, tag the defective module, and note the location from which it was taken and the nature of the failure. When repairs are completed, return the repaired module to its original location, and confirm that the repairs have resolved the problem by running all tests which originally exhibited the problem.

NOTE

If modules have been moved during the troubleshooting period, return all modules to their original positions before running the validation tests.

5.9.6 Recording

A log book is supplied with each GLC-8 System. Corrective maintenance is not complete until all activities are recorded in the log book. Record all data indicating the symptoms of the fault, the method of fault detection, the component at fault, and any comments which would be helpful in maintaining the equipment in the future.

The log should be maintained on a daily basis, recording all operator usage and corrective maintenance results.

5.10 ADJUSTMENTS

Adjustments of the GLC-8 should never be undertaken until it has been confirmed that a failure is due to circuit aging or misalignment, rather than a component failure. Replacement of certain components or correcting an unsatisfactory environment may eliminate the need for adjustment.

5.11 TRANSISTOR ABUSES

5.11.1 General

A manufacturer's transistor and IC specification sheet not only describes the device, but warns of its limitations and assumes that the user is somewhat familiar with the type of device described, as well as its application. When this knowledge is lacking, additional information is available in the form of application notes, technical tips, articles in technical periodicals, promotional material, manuals, etc.

No matter how carefully the manufacturer prepares his specification sheet, he cannot guarantee his device against mechanical and electrical abuses.

Over the years transistors and ICs have acquired a reputation for high reliability and ruggedness but there are limitations that the user must become familiar with if he is to maintain reliable semiconductor circuits. The following paragraphs discuss some of the more common handling abuses to which transistors and ICs are subjected.

5.11.2 Mechanical Abuses

Shock

Semiconductor material is hard and brittle and can be damaged by a high impact shock. For example, dropping a device 4-1/2 inches onto a hardwood bench subjects the device to around 500g; a drop of 30 inches onto concrete may increase the impact shock from 7000 to 20,000g; snapping rather than sliding a transistor into a clip causes a shock to 600g; and carelessly clipping a transistor lead may generate a shock wave of several thousand g. Any high impact shock, therefore, can cause a fracture in the semiconductor material, or lead breakage, which completely ruins the semiconductor device.

Lead Bending

Bending a wire back and forth sharply will usually cause a break or fracture. This is especially true of transistor leads at the point where they enter, or attach to, the header. Leads bent during testing or handling may easily break later because the "bending life" of the lead has already been exhausted. Plated leads which are subjected to excessive bending and twisting can crack at the header, allowing moisture to enter and contaminate the device, thereby causing gradual degradation of gain and voltage characteristics. To prevent this damage, always allow a clearance of at least 1/16 to 1/8 inch between the header and the start of a lead bend.

Overheating

If, during soldering, the maximum specified junction temperature of a device is exceeded, the device can be destroyed. Heat transmitted over connecting leads and printed circuit board leads to the header can also be destructive. Junctions can be shorted. Lead connections may open. Unequal expansion between the header and the package may break the hermetic seal. Safety precautions include the removal of the transistor and IC from the immediate socket to which heat is being applied, keeping in mind that the heat can quickly travel along connecting wires to neighboring sockets; the use of heat shunts (clips, pliers, etc.) connected between the heat source and the devices; and the use of a soldering iron of heat delivery adequate for the job to be done.

5.11.3 Electrical Abuses

Excessive Voltage

Never exceed the absolute maximum voltages (usually specified at 25° C) given by the manufacturer. In signal amplifier circuits, peak-to-peak voltage swings should not exceed the inter-element absoulte maximum voltages of the transistors. A good rule is to use a supply voltage equal to half the maximum voltage rating. Maximum inter-element voltages can also be exceeded by voltage transients (inductive and capacitive kicks, etc.) when connecting a transistor into a hot circuit.

NOTE

Before removing or replacing a transistor in a circuit, always turn the power OFF.

Using an ohmmeter to test transistors can also cause damage by application of excessive voltage. Since the emitter-base reverse breakdown voltage for most transistors is from 1V to 5V , the transistor can easily be damaged when subjected to the high voltage ranges of an ohmmeter (many use 22-1/2 volt batteries). When measuring breakdown voltage, always use a current limiting resistor. Voltage spikes can cause a build-up of impurities concentrated at a point in the collector and emitter junctions and can result in punch-through (internal short from collector to emitter) across the base region.

Excessive Power

Exceeding the maximum junction temperature of a transistor can permanently change the gain, the breakdown voltage, and cause opens and shorts. To guard against such damage when testing for gain at excessive power dissipation levels, use a protective heat sink or test with a low duty cycle pulse.

5.12 COMPONENT BOARD AND COMPONENT REPLACEMENT SERVICE NOTES

5.12.1 Pre-replacement Servicing Aids

a. When soldering semiconductor devices (transistors, diodes, rectifiers and integrated circuits) which are defective, use only a six-volt soldering iron with an isolation transformer.

CAUTION

Use of an iron without an isolation transformer may result in excessive voltages presented at the iron tip.

b. In replacing components, use a heat sink (for example, a pair of pliers) to grip the lead between the joint and the device being soldered.

c. Perform the soldering replacement operation in the shortest possible time to prevent damage to the component and breaking of the copper foil on the board.

CAUTION

Never attempt to remove solder from terminal points by heating and rapping the module against another surface. This can result in component or module damage. Always remove solder by using a solder-sucking tool.

d. When removing any part of the equipment for repair and replacement, make certain that all leads or wires which have been unsoldered are legibly tagged or marked for identification with their associated terminals. When a component has been removed it should be replaced by a new component of the same value and tolerance.

e. In all soldering and unsoldering operations do not allow any solder or flux to fall on adjacent components or copper foil runs. When the repair has been completed, remove the excess flux by washing the junctions with a solvent such as trichlorethylene. Be careful not to expose painted or plastic surfaces to this solvent.

5.12.2 Integrated Circuit Replacement

Step	Procedure
1	ICs can be easily removed by using a solder-sucking tool to remove all excessive solder from the contacts after the soldering iron has been applied to melt the solder.
2	Next straighten the leads of the IC and lift the component from the printed board. If it is not desirable to save the defective IC for test purposes, then the terminals can be cut at the body of the component and each terminal removed from the board individually.

5.12.3 Component Replacement

Step	Procedure
1	Cut the component leads from the top of the component board then apply the soldering iron to the folded over side on the copper foil side of the board. When the solder starts to flow, remove excess solder by using the solder-sucker. Remove the lead and free the other cut lead in the same manner.
2	When installing a new component, observe the length and dress of the leads on the old component, then cut and bend the leads of the new component accordingly.
3	Try placing the leads in the holes. If residual solder prevents a lead from entering the hole, very gently ream out the solder with a sharply pointed, square tipped awl. Then place the leads in the holes so that the component is held in place by friction or slight spring tension of the leads.
4	Using a high grade electrical solder, apply the soldering iron tip, then the solder to the junction of the hole so that a very small amount of solder flows around the lead and into the hole, thus bonding the lead to the board.
5	Examine the joint carefully. A good joint should withstand a light pull by the fingers. Clear away any loose solder, making sure that no solder scraps fall where they might cause a short.

5.12.4 Copper Foil Repair

In the unlikely event of a break in the copper foil strip, the strip can be repaired by placing a short piece of tinned wire across the break and flowing solder over the length of the wire. Be careful that excess solder does not short adjacent strips.

5.13 ALIGNMENT PROCEDURES

5.13.1 Test Equipment

To service the GLC-8 System the Test Equipment outlined in Table 5-1 is recommended. If the recommended equipment is not available alternate equipment with the same performance specifications should be used.

5.14 FRONT END ADJUSTMENTS

Front end adjustments have been preset at the factory and should not require readjustment. If they should become misaligned and require realignment, the procedures in this section should be followed. Refer to Table 5-2 for the control functions.

Some adjustments can be performed using the A212 Program Amplifier and the ADC1-A Converter, which converts synchronously with the line frequency. Where it is indicated, use a high gain oscilloscope.

Adjustments should be performed using an Electronic Development Corporation (EDC) precision power supply, Model MV100G and the GLC-8 MAINDEC 8I-D6 diagnostic programs (when required).

System adjustments start with the ADC1-A Converter and proceed toward the A210 and A211 Buffer Amplifiers so that the preceding option can be used as a reference for the other adjustments. Because of this, all adjustments must be performed in the order set forth in the following section.

The GLC-8 System program has provisions to select channels, gain, and outputs to the teletypes or display the outputs on the ADC1-A Converter lights. The program is written to convert at the line frequency rate on the same phase of the cycle, thereby eliminating the sampling of internal and external noise.

5.14.1 A-D Converter (ADC1-A)

The calibration and adjustment procedures for this unit are provided in its associated instruction book, DEC-00-16AA-D. Because of this unit being used as a standard for all other adjustments, it must first be established that it is operating correctly before proceeding with the following adjustments.

Table 5-1
Maintenance Equipment

Equipment	Specifications	Equivalent
Multimeter	10K ohms/volt - 20 K ohms/volt	Triplett Model 310
Oscilloscope	dc to 50 mc with calibrated deflection factors from 5 mV to 10V/div. Maximum horizontal sweep rate of 0.1 μs/div. Delaying sweep is desirable and dual trace is a necessity.	Tektronix Type 453
Probes	X10 with response characteristics matched to oscilloscope and a X1 probe.	Tektronix Type P6010 Probe Type P6011
Clip-on current probe	2 mA/mV or 10 mA/mV	Tektronix Type P6019 with passive terminator
Recessed Probe Tip		Tektronix
Unwrapping tool for 24 gauge		Gardner Denver H812-505-244-475
Unwrapping tool for 30 gauge		Gardner-Denver H812A-505-244-475
Wire-Wrap Tool		Gardner-Denver A-20557-29
24 and 30 Gauge bit for wrap tool (H810)		Gardner-Denver 504221
Sleeve for 30 gauge bit		Gardner-Denver 500350
Sleeve for 24 gauge bit		Gardner-Denver 18840
Spray paint		Krylon 1501 Glossy white
Spray paint		DEC black
IC Card Module Extender		DEC No. W982
Flip-Chip Module Extender		DEC No. W980
Jumper Wires		Assorted lengths affixed with 24 and 30 gauge termipoint connectors

Table 5-1 (Cont)
Maintenance Equipment

Equipment	Specifications	Equivalent
Null Meter Model MV100G (Precision Power Supply)	Measurement Mode Range: 0 to ±11.1110 Vdc (resolution: 1 μV) Input Impedance: infinite at null; 200 KΩ off null. Max. Sensitivity: 25 μV/minor division. Zero Control: Front panel zero meter control calibration balances automatically. Output Mode Range: 0 to ±11.1110 Vdc (resolution: 1 μV) Absolute Accuracy: ±.01% or 50 μV (of setting) High range and .01% or ±2 μV (of setting) low range Output Current: 10 mA Power Requirements: 105 to 125 Vac; 50-65 Hz; 2W Protection: Short circuit and overload protected front panel overload indicator; recovery automatic. Vernier: ±.001V (W/Disable switch for zero) Output Impedance: < .03 ohms on high range and < 20 ohms on low range.	Electronic Development Corporation

Table 5-2
Programmable and Buffer Amplifier Controls

Programmable Amplifier, A212	
Control	Function
Balance	Adjusts the offset voltage
X1, X2, X4, X8, X16, X32, X64	Adjusts the individual gains of the amplifier.
High gain and Shunt Control	Adjusts the high gain output of the amplifier (X64, X128, X256)

Table 5-2 (Cont)
Programmable and Buffer Amplifier Controls

Buffer Amplifier, A210 (X1) and A211 (X10)	
Control	Function
Balance	Adjusts the offset voltage
Line Balance	Adjust for an input line unbalance of up to 1KΩ
Gain	Adjusts the output gain of the amplifier
	Filter, A216
Balance	Adjust the offset voltage

5.14.2 Program Amplifier A212

See Figure 5-5 and 6-34.

Balance Control

Step	Procedure
1	Connect input leads, pins AP-AN together.
2	Using the GLC-8 MAINDEC 8I/D8BA Program calibration routines, select a non-existing channel with a gain of X256.
3	Adjust the balance control for a minimum output from the A-D converter of approximately 0001.

NOTE

Because of the relatively high output impedance of the E.D.C. Power Supply, 20Ω, at its low output voltage terminal, and the low impedance input of the A212 programmable amplifier 2KΩ, a A216 filter amplifier must be used for impedance matching when making the following adjustments:

If the A216 filter amplifier offset needs adjustment, refer to 5.12.4

Step	Procedure
1	Connect the E.D.C. Power Supply to the A216 filter, connector pins V and U.
2	Remove the buffer amplifier.
3	Using the GLC-8 MAINDEC 8/I/D6BA program calibration routines, select the channel that the A216 amplifier is in, and select the appropriate gain and input voltage settings in the following table:

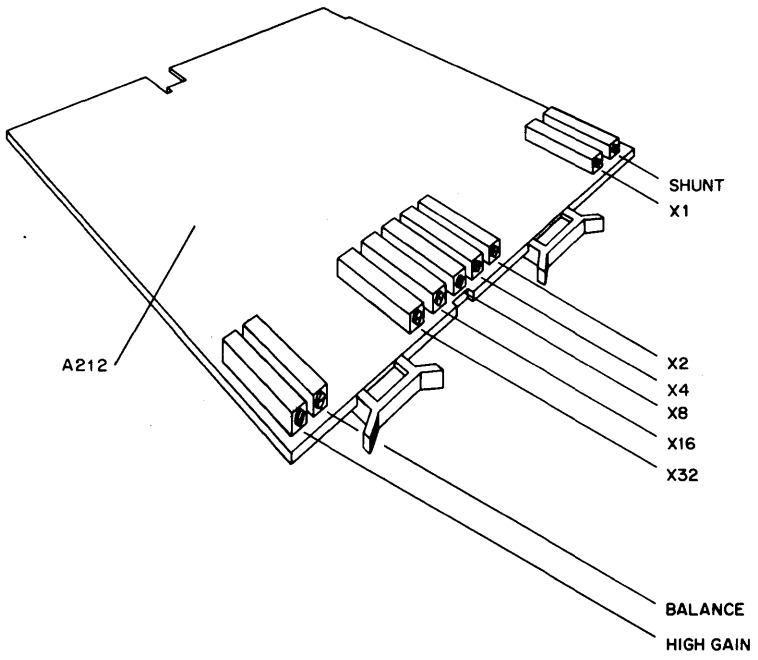


Figure 5-5 A212 Variable Gain Amplifier Control Location Diagram

Gain	Input (Volts)
X1	9.9963
X2	4.9981
X4	2.4491
X8	1.2495
X16	0.6247
X32	0.3123

4 Adjust the appropriate gain controls for an output from the A-D converter between 7777 and 7776.

High Gain Controls

Step	Procedure
1	Repeat Step 1 of the Low Gain Controls section.
2	Remove the buffer amplifier.
3	Using the GLC-8 MAINDEC 8/ID6BA program calibration routines, select the channel the A216 filter amplifier is in and select the appropriate gain and input voltage setting in the table below:

Gain	Input (Millivolts)
X64	136.740
X128	68.369
X256	34.184

4	Adjust the appropriate control for an output from the A-D converter between 7000 and 7001 by performing Steps 5 through 8.
5	Adjust the X64 range with the high gain control.
6	Adjust the X128 range with the shunt control.
7	Adjust the X256 range with the shunt control to its half range point only. This is between the original setting and the correct setting.
8	Repeat Steps 5 through 7 until all of these adjustments are properly aligned.

5.14.3 A213 Filter

This filter has no adjustments.

5.14.4 A216 Filter

Balance Control

Step	Procedure
1	Remove the channel buffer amplifier.
2	Short input pins V and U of the A216 filter.
3	Using the GLC-8 MAINDEC 8I/D6BA program calibration routines, select the appropriate channel, with a gain of X256.
4	Adjust the balance control for a minimum output from the A-D converter of approximately 0001.

5.14.5 A210 Buffer Amplifier

(See Figure 5-6 and 6-35)

Balance Control (Initial Adjustment)

Step	Procedure
1	Connect both the input pins N and P to the common pin F.
2	Using the GLC-8 MAINDEC 8/I/D6BA program calibration routines, select the appropriate channel with a gain of X256.
3	Adjust the balance control for a minimum output from the A-D converter of approximately 0020.

Gain Control (Initial Adjustment)

1	Connect the E.D.C. Power Supply to pins N and P of the A210 buffer amplifier.
2	Tie pin P of the A210 buffer amplifier to pin F.
3	Using the GLC-8 MAINDEC 8/I/D6BA program calibration routines, select the appropriate channel with a gain of X1.
4	Adjust the gain control for an output from the A-D converter between 7777 and 7776 with an input of 9.9963V.

Line Balance Control (Initial Adjustment)

Step	Procedure
1	Connect the A210 amplifier pins N and P together, then connect them to pin H on the A310 module (AF16 A25, DK01).
2	Adjust the output of the A210 buffer amplifier, pin V, to a minimum value of approximately 10 mV while monitoring it with an oscilloscope. This adjustment should be made with a plastic or nylon screwdriver.

Gain Control (Final Adjustment)

1	Repeat Steps 1 through 4 of the previous Gain Control Section (initial adjustment), omitting Step 2.

Line Balance Control (Final Adjustment)

1	Repeat Steps 1 and 2 of the Line Balance Control (initial adjustment).

Balance Control (Final Adjustment)

1	Repeat Steps 1 and 2 of the Balance Control (Initial Adjustment) Section.
2	Adjust the balance control for an output from the A-D converter of 0200.

Common Mode Control (only existed in early models)

1	Repeat Steps 1 and 2 of the Line Balance Control (initial adjustment) procedure, adjusting the common mode control instead of line balance control.
2	Recheck the Line Balance Control (Initial Adjustment), Gain Control (Final Adjustment), and Balance Control (Final Adjustment) settings.

Line Balance Control Readjustment

If the gas chromatograph DC Line unbalance resistance is great enough to require a readjustment, the following procedures should be followed:

1	Obtain from the customer the DC Line unbalance resistance of the gas chromatograph.
2	Obtain a resistor equal to the line unbalance resistance in Step 1 and connect it in series to pin N of the A210 Buffer Amplifier.

Step	Procedure
3	Repeat the Line Balance Control (Initial Adjustment) steps with the added offset resistance.
4	Repeat the Gain Control (Final Adjustment) step with the added offset resistance.

5.14.6 A211 Buffer Amplifier

(See Figure 5-6 and 6-36.)

All of the following adjustments pertain to the procedures of Section 5.12.5 for the A210 Buffer Amplifier. It should be noted that the A-D converter readings are different for the A211 Buffer Amplifier.

Step	Procedure
1	Repeat the Balance Control (Initial Adjustment) procedure, noting that the output from the A-D converter is approximately 0010.
2	Repeat Gain Control (Initial Adjustment) procedure, noting that the output from the A-D converter is between 7777 and 7776.
3	Repeat Line Balance Control (Final Adjustment) procedure.
4	Repeat the Gain Control (Final Adjustment) procedure, noting that the input voltage should be 0.9996 and the output from the A-D converter is between 7777 and 7776.
5	Repeat the Line Balance Control (Final Adjustment) procedure.
6	Repeat the Line Balance Control (Final Adjustment) procedure, noting that the programmable amplifier is now set to a gain of X1 and the output from the A-D converter is adjusted to 0006.
7	Repeat the Common Mode Control procedure.
8	Repeat the Line Balance Control Readjustment procedure, noting the gain and offset voltage differences.

5.15 MODULE HANDLING

To insert or extract modules, first turn OFF all power. To gain access to components on a module, remove the module by exerting a straight even pull on the module handle to prevent twisting of the printed-wiring board. Insert a Type W380 Flip-Chip Module Extender into the vacated module mounting panel, then insert the module into the extender.

Each module used in the GLC-8 System is shown in Figures 6-37 through 6-56.

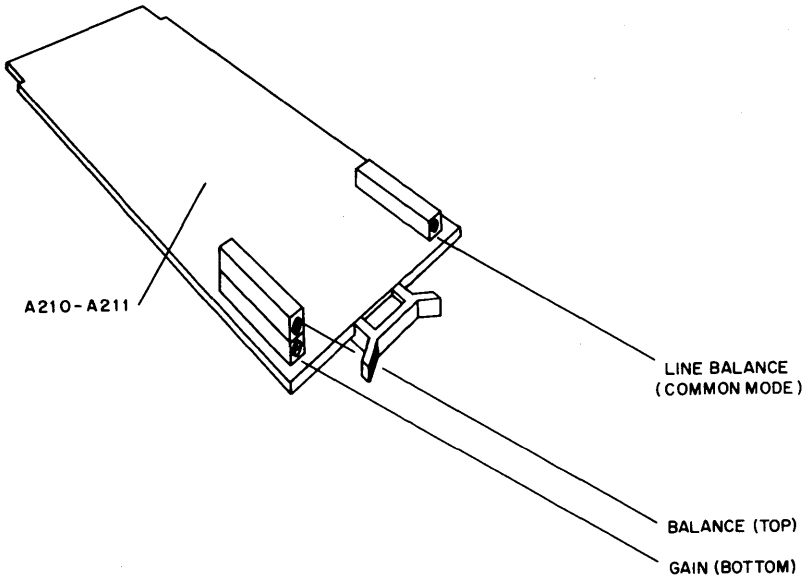


Figure 5-6 A210 and A211 Input Buffer Amplifier Control Location Diagram

5.16 SPARE PARTS

It is suggested that the customer set up a spare parts inventory which should include those items listed in Tables 5-3 to 5-17 which he feels he cannot successfully repair or replace or which are not available from local electronic supply houses.

Table 5-3
Recommended Spare Tool List
For the ASR33 Teletype

DEC Code #	Description	Quantity
110443	Scale, 8 oz	1
110444	Scale, 32 oz	1
82711	Scale, 64 oz	1
117781	Set of gauges	1
94644	Offset Screwdriver	1
94645	Offset Screwdriver	1
151351	Hook, 8 crochet	1
151959	Hook, 12 crochet	1
142555	Spring Hook Push	1
142554	Spring Hook Pull	1
151384	Screw Holder	1
181465	Handwheel Adaptor	1
161430	Handwheel	1
172060	Contact adjustment tool	1
180587	Gauge	1
180588	Gauge	1
180993	Bending Tool	1
183103	Gauge	1
182697	Extractor	1
151392	Tweezer	1
6617	Tommy Wrench	1
73404	Tommy Wrench	1
151383	Key Lever Remover	1

Table 5-4
Recommended Mechanical Spares
For H300 - H301 LOC

Dialco Vendor Part	Vendor Part Number
Dialco Switch	513-0201-604
Dialco Lamp	387
Lens	187-5075

Table 5-5
Recommended Diode Spares

DEC Code #	Description	Quantity
11-00113	D662	10
11-00114	D664	10
11-02451	1N753	2
11-03183	MR2064	2
11-03309	D671	2
11-05275	D672	10

Table 5-6
Recommended Transistor Spares

DEC Code #	Description	Quantity
15-02155	DEC 1008-S	5
15-02937	2N3568	2
15-03100	DEC 3009B-S	10
15-03399	DEC 3790-S	2
15-03409	6534 D	10

Table 5-7
Recommended Delay Line Spare

DEC Code #	Description	Quantity
16-05530	Delay Line-L501D501A	1

Table 5-8
Recommended Pulse Transformer Spares

DEC Code #	Description	Quantity
52-00672	2037	5
52-02123	2052	5

Table 5-9
Recommended Miscellaneous Spares

DEC Code #	Description	Quantity
12-5375 (RS-9-3-FB)	Rocker Switch	4
12-5941 (RS-50-FB-PC)	Rocker Switch	4
12-5317	Rocker Handles	4
12-5550 (2313)	Indicator Bulbs	6
34-4235	Power Lock Switch	1

Table 5-10
Recommended Integrated Circuit Spares

DEC Code #	Description	Quantity
19-05521	MC 1540G	2
19-05547	SN7474	5
19-05575	TI SN7400N	5
19-05576	TI SN7410N	5
19-05577	TI SN7420N	5
19-05578	TI SN7430N	2
19-05579	TI SN7440N	5
19-05580	TI SN7450N	2
19-05581	TI SN7460N	5
19-05582	TI SN7453N	5
19-05584	TI SN7482N	2

Table 5-11
Recommended Module Spares
For AF06, AF07, AF08

Modules	Module Number	Quantity
Guarded Relay Multiplexer Switch	A111	1
Input Buffer Amplifier*	A210	1
Input Buffer Amplifier*	A211	1
Variable Gain Amplifier	A212	1
Low Pass Filter*	A213	1
Low Pass Filter*	A216	1
Four Times Line Frequency Clock	A310	1
Slicer Flip-Flop	A501	1
Difference Amplifier	A502	1
3 Bit DAC	A601	1
2 Bit DAC	A604	1
2 MA Level Terminator	G704	1
Inverter	R107	1
Diode Gate	R111	1
Diode Gate	R113	1
NAND/NOR Gate	R121	1
NOR Gate	R122	1
Diode Gate	R123	1
Diode Gate	R141	1
Binary to Octal Decoder	R151	1
Dual Flip-Flop	R202	1
Triple Flip-Flop	R203	1
Dual Flip-Flop	R205	1
Delay	R302	1
Integrating One Shot Multivibrator	R303	1
Pulse Amplifier	R602	1
Pulse Amplifier	R603	1
Signal Cable Connector	W021	1

* One per H303, where applicable

Table 5-11 (Cont)
Recommended Module Spares
For AF06, AF07, AF08

Modules	Module Number	Quantity
Cable Connector	W023	1
100 MA Indicator Relay Driver	W051	1
Device Selector	W103	1
Schmitt Trigger	W501	1
Positive Level Converter	W512	1
Pulse Amplifier	W640	1
Relay Multiplexer	W802	1
Relay**	W809*	1

* One per H303, where applicable.
** For H301 only.

Table 5-12
Recommended Printer Keyboard
Model ASR33 Spares

DEC Code #	Description	Quantity
181821	Circuit Board	1
183071	Tape Feed Sprocket	2
182240	Lever, Universal	2
120167	Fuse (3.2 amp)	2
180979	Distributor Brush	2
181420	Driven Gear	1
181411	Drive Gear	1
181409	Belt	2
181007	Shaft	1
181002	Bearings	2

Table 5-13
Recommended PT08 Module Spares

Module	Module #	Quantity
Clock	R401	1
+3.6V integrated CKT Power Supply	W705	1
Device Selector	W103	1
Teletype Transmitter	W707	1
Teletype Receiver	W706	1

Table 5-14
Recommended DF-32 Module Spares

Module	Module Number	Quantity
Diode Cluster	R002	2
Inverter	R107	6
Diode Gate	R111	3
Diode Gate	R113	4
Diode Gate	R123	5
Dual Flip-Flop	R202	5
Triple Flip-Flop	R203	5
Dual Flip-Flop	R205	5
Delay	R302	1
Pulse Amplifier	R602	3
Pulse Amplifier	R603	4
Clamped Loads	W005	1
Signal Cable Connector	W021	12
Device Selector	W103	4

Table 5-14 (Cont)
Recommended DF-32 Module Spares

Module	Module Number	Quantity
Difference Amp	W532	2
Disk Preamplifier	G083	2
Disk Writer	G284	1
Series Switch	G285	1
Center Tap Selector	G286	1
Relays	G803	2

Table 5-15
Recommended PDP-8/I Module Spares

Module	Module Number	Quantity
Sense Amplifier	G021	1
Memory Selector	G221	1
Inhibit Driver	G228	1
Resistor Board	G624	1
Negative Regulator	G805	1
Regulator Control	G826	1
10 2-Input NAND Gates	M113	2
8 3-Input NAND Gates	M115	1
6 4-Input NAND Gates	M117	1
AND/NOR Gate	M160	1
Flip-Flop	M216	1
Major Register	M220	1
Delay Line	M310	2
Variable Delay	M360	1
Variable Clock	M452	1
Negative Input Converter	M506	1
6 4-Input NOR Buffers	M617	1
Negative Output Converter	M650	1
Manual Timing Generator	M700	1
Teletype Receiver	M706	1
Teletype Transmitter	M707	1

Table 5-16
Recommended KE8I and MC8I Module Spares

Module	Module Number	Quantity
Sense Amplifier	G021	1
Memory Selector	G221	1
Inhibit Driver	G228	1
Resistor Board	G624	1
10 2-Input NAND Gates	M113	1
Variable Delay	M360	1
6 4-Input NOR Buffers	M617	1
8 3-Input NAND Gates	M115	1
6 4-Input NAND Gates	M117	1
Expander	M160	1
Flip-Flop	M216	1
Delay Line	M310	1

CHAPTER 6
GLC-8 ENGINEERING DRAWINGS

The following Engineering Drawings are included in Chapter 6:

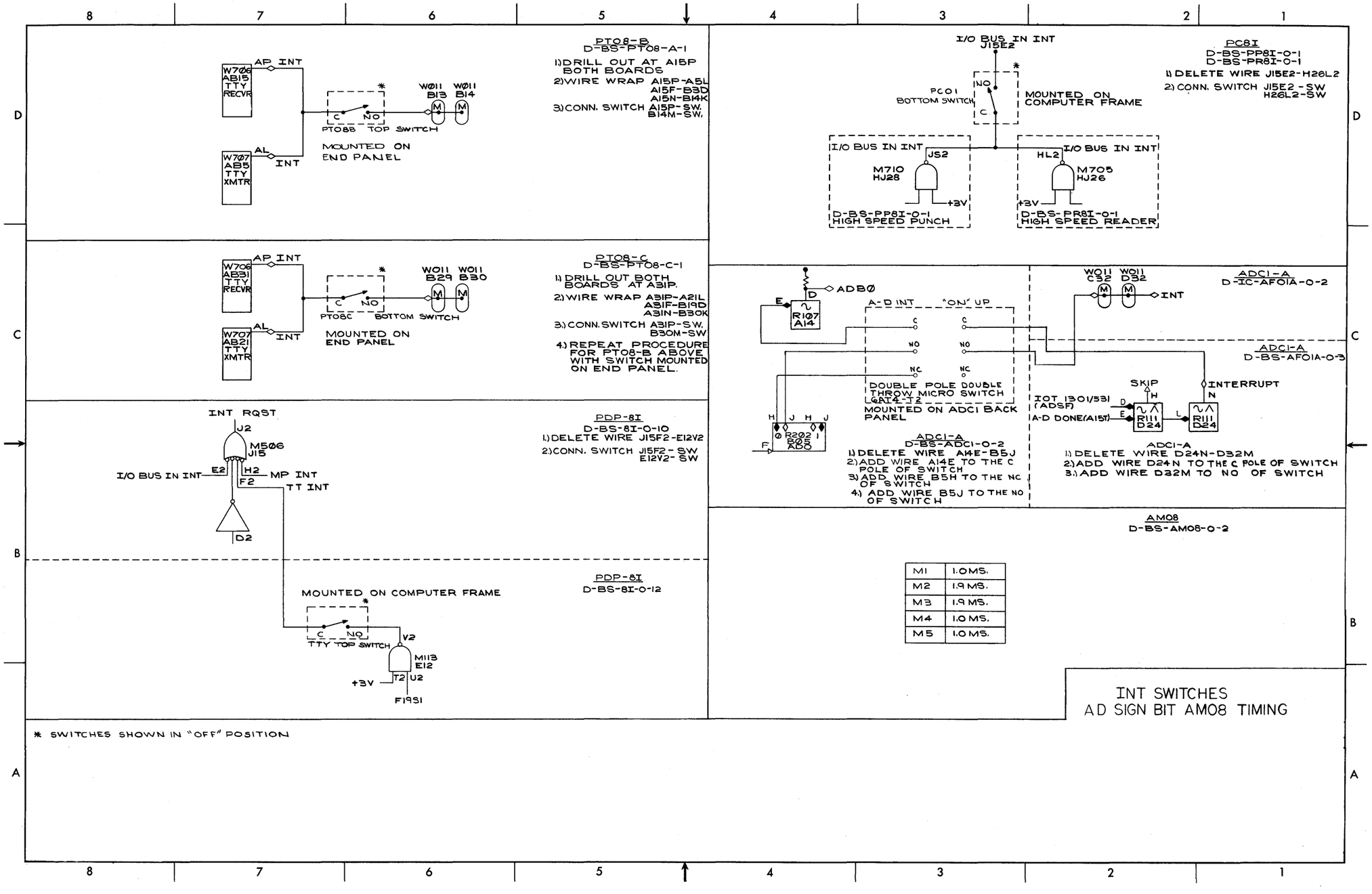


Figure 6-1 D-BS-AF06-A-3 AF06 Modification Block Schematic

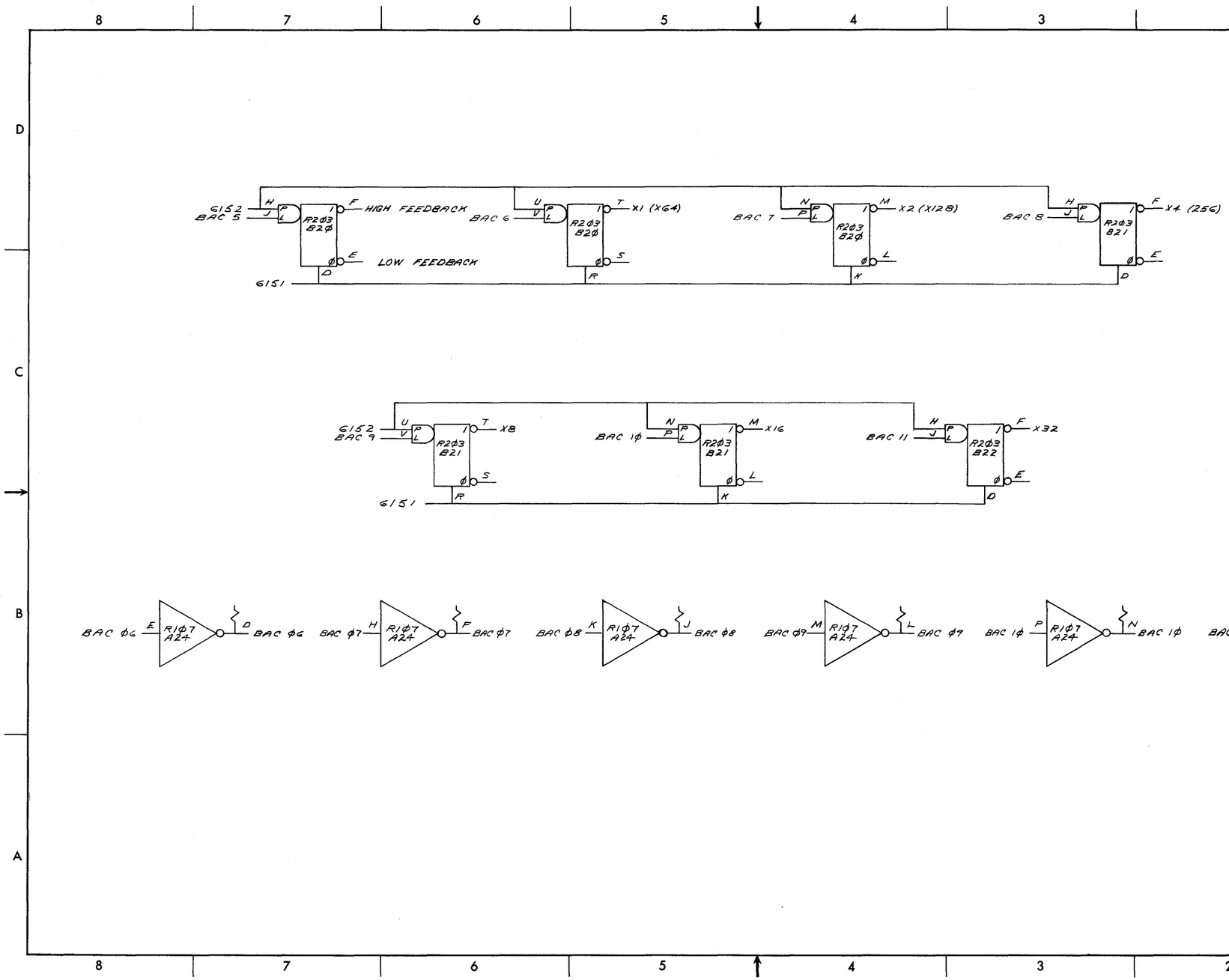


Figure 6-2 D-BS-AF16-0-2 Variable Amplifier Gain Control Block Schematic Diagram

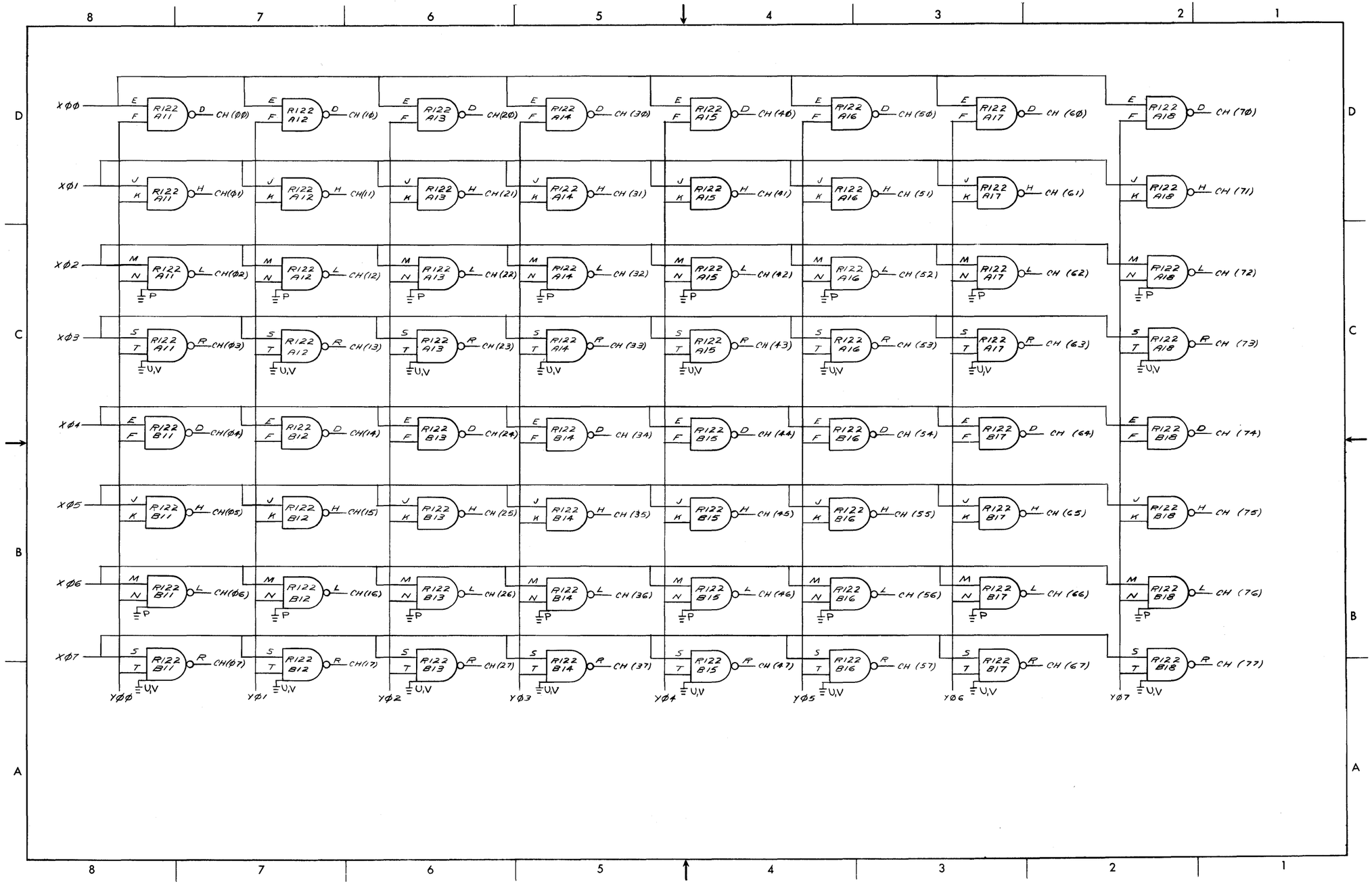


Figure 6-3 D-BS-AF16-0-3 LOC Channel Selector Block Schematic Diagram

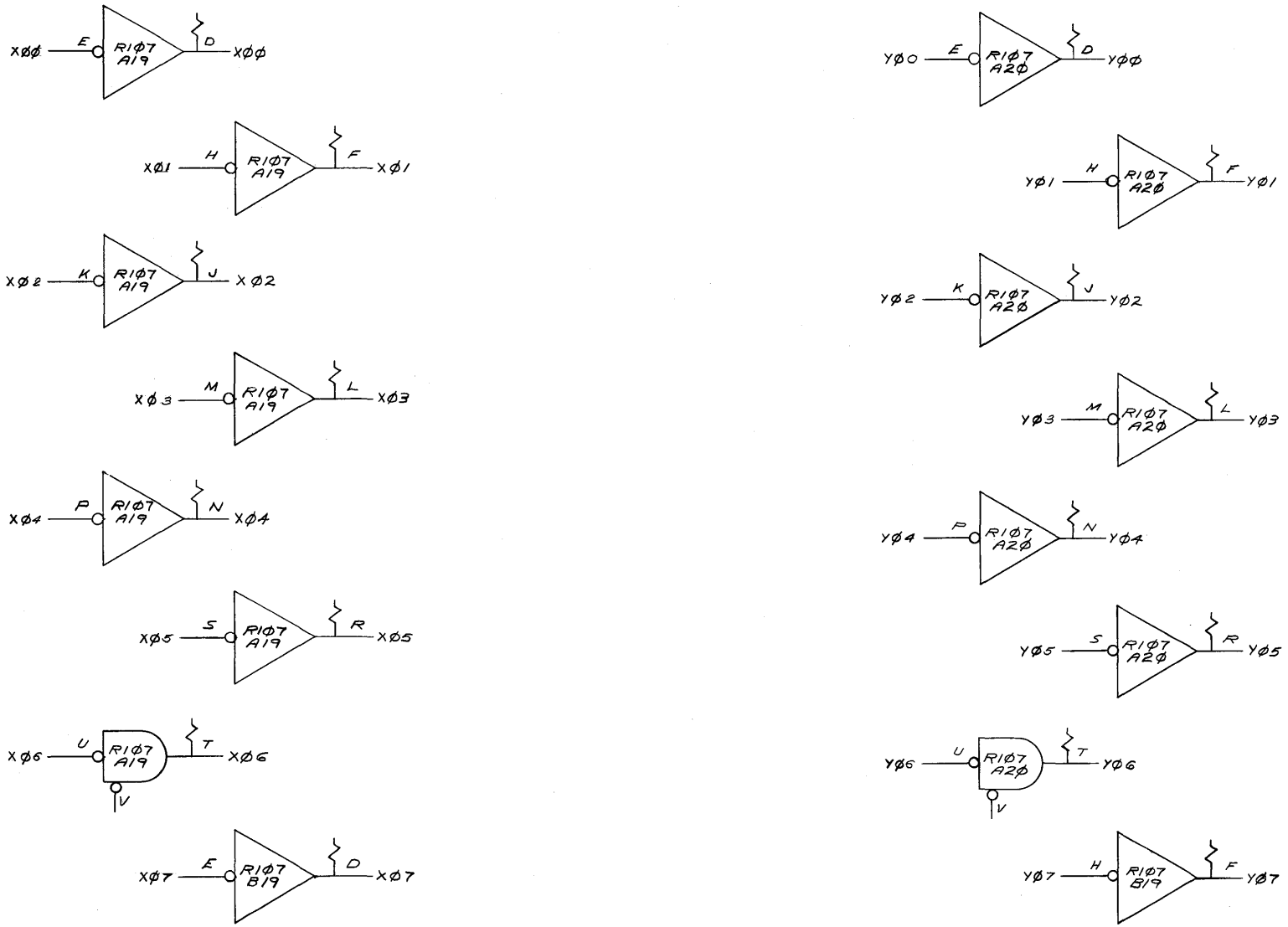


Figure 6-4 B-BS-AF16-0-5 Channel Selector Interface Block Schematic Diagram

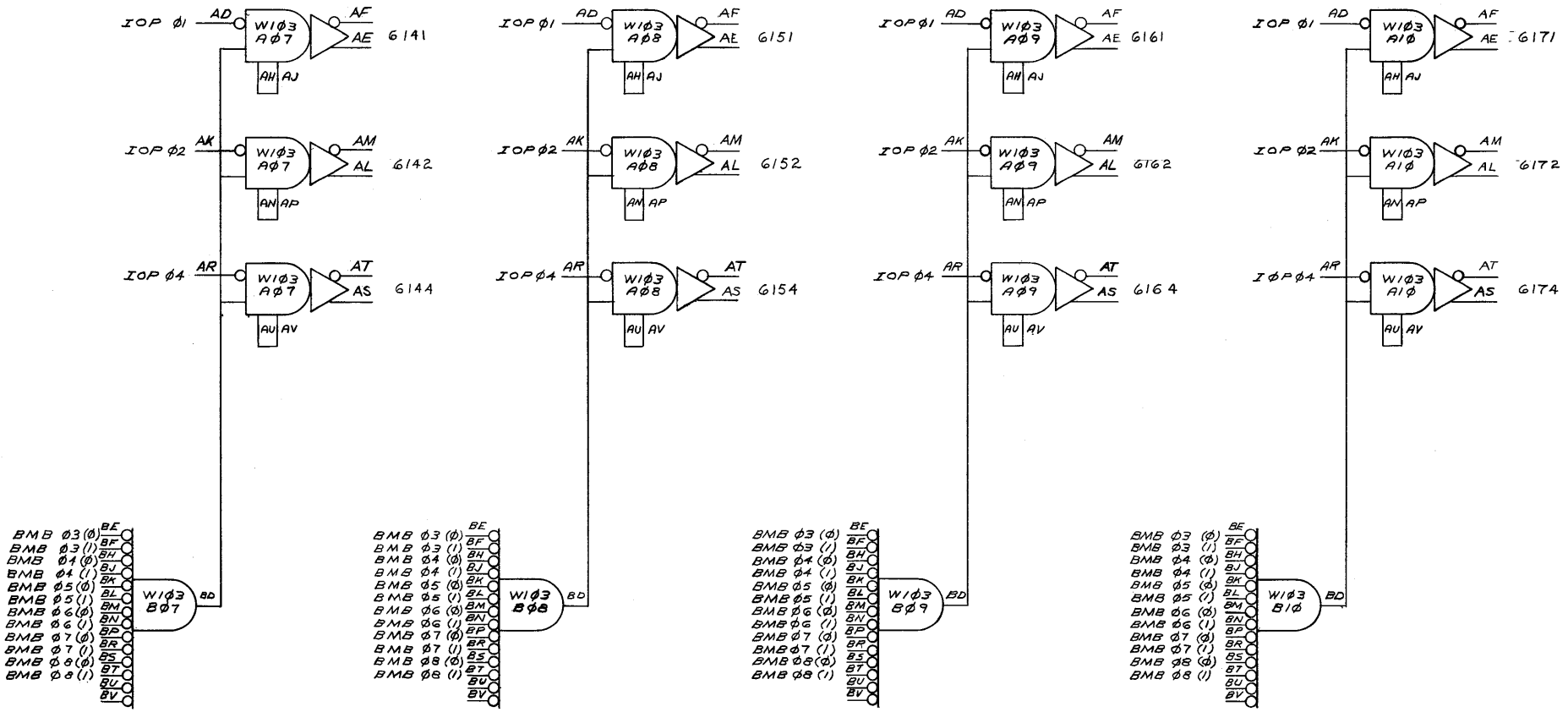


Figure 6-5 B-BS-AF16-0-4 Chrom and LOC, IOT Decoding Block Schematic Diagram

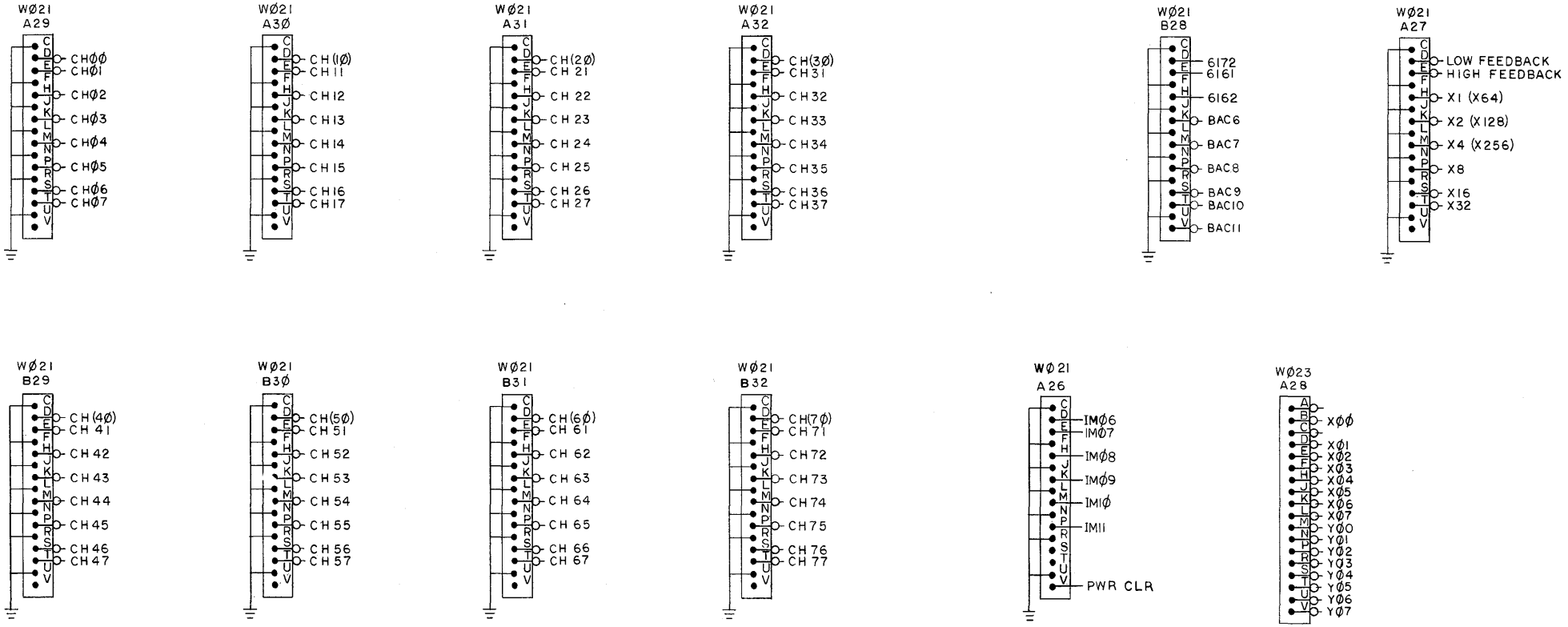


Figure 6-6 D-IC-AF16-0-6 Chrom to LOC Cable Interconnection Diagram

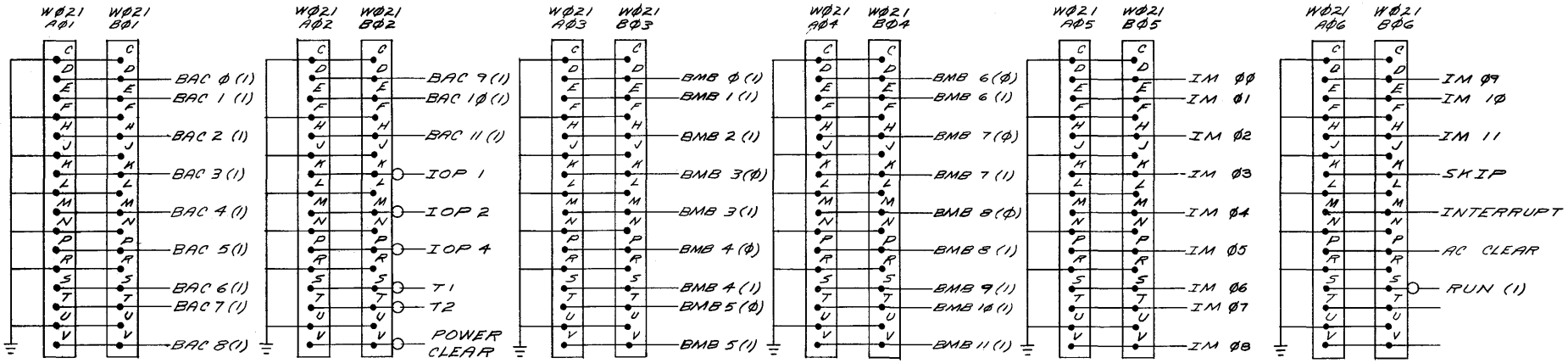


Figure 6-7 D-IC-AF16-0-7 I/O Connection Diagram

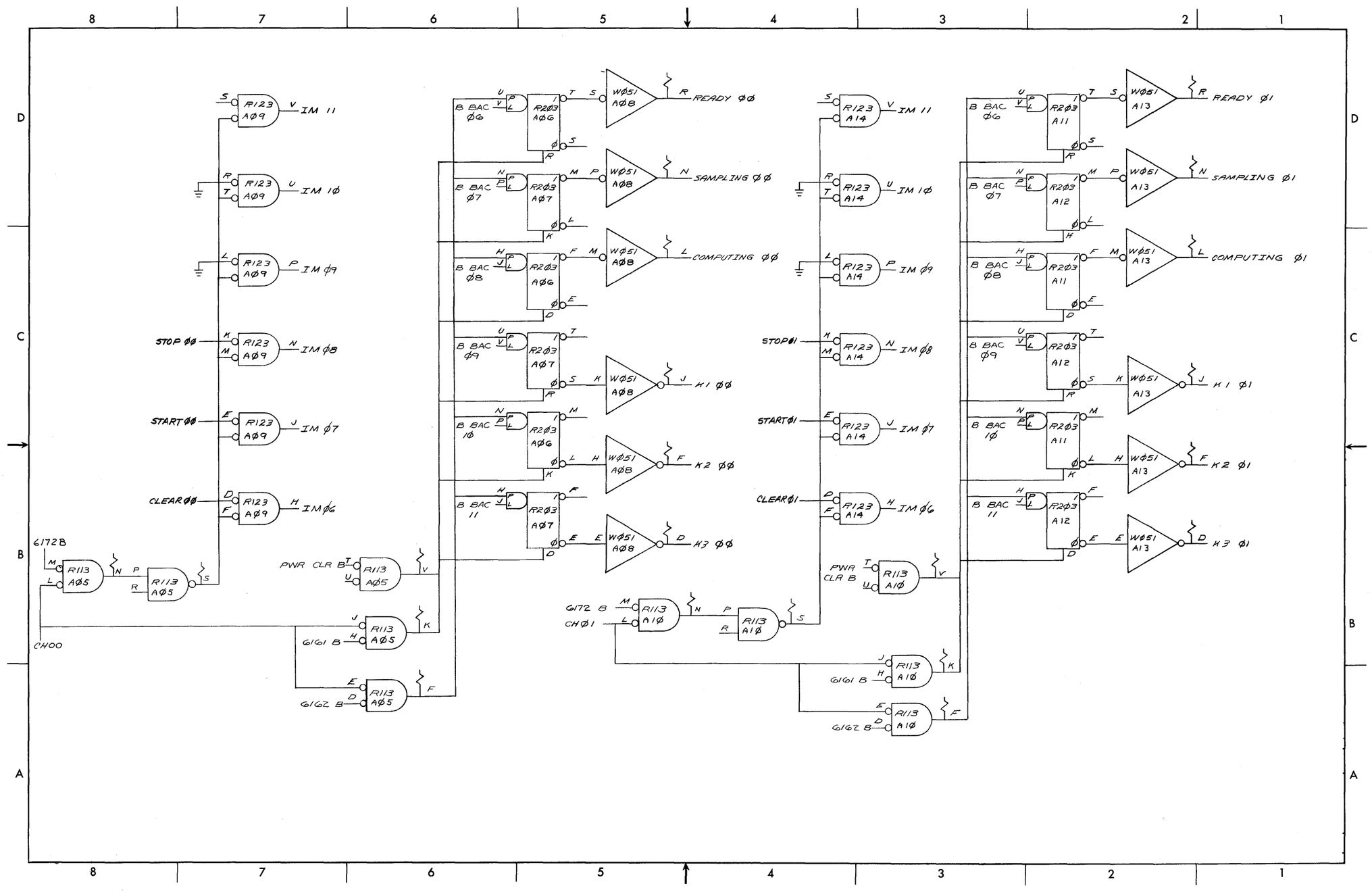


Figure 6-8 D-BS-AF17-0-3 LOC Control Logic (Ch. 00 to 07) Block Schematic Diagram (Sheet 1)

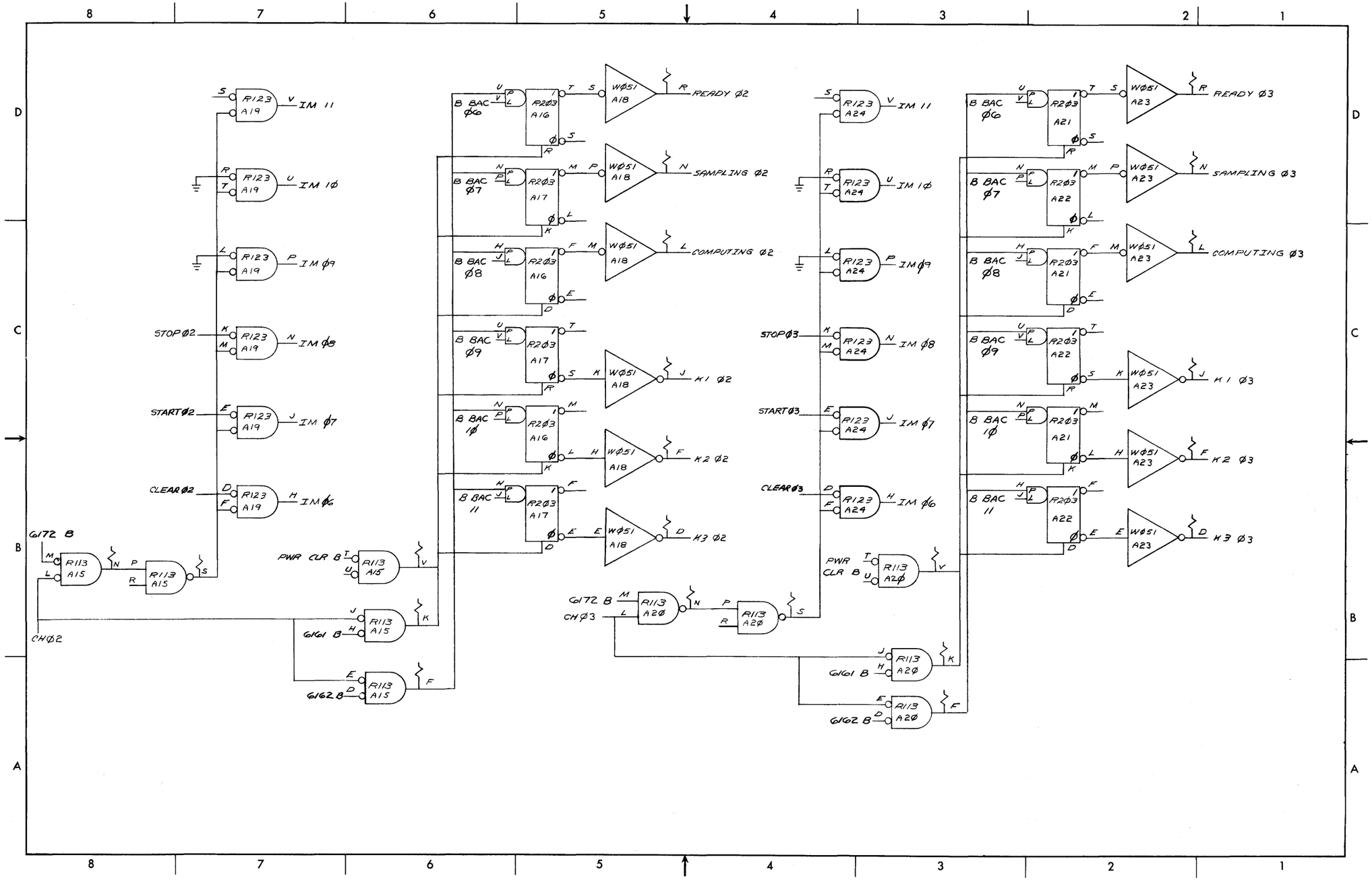


Figure 6-8 D0BS-AF17-0-3 LOC Control Logic (Ch. 00 to 07) Block Schematic Diagram (Sheet 2)

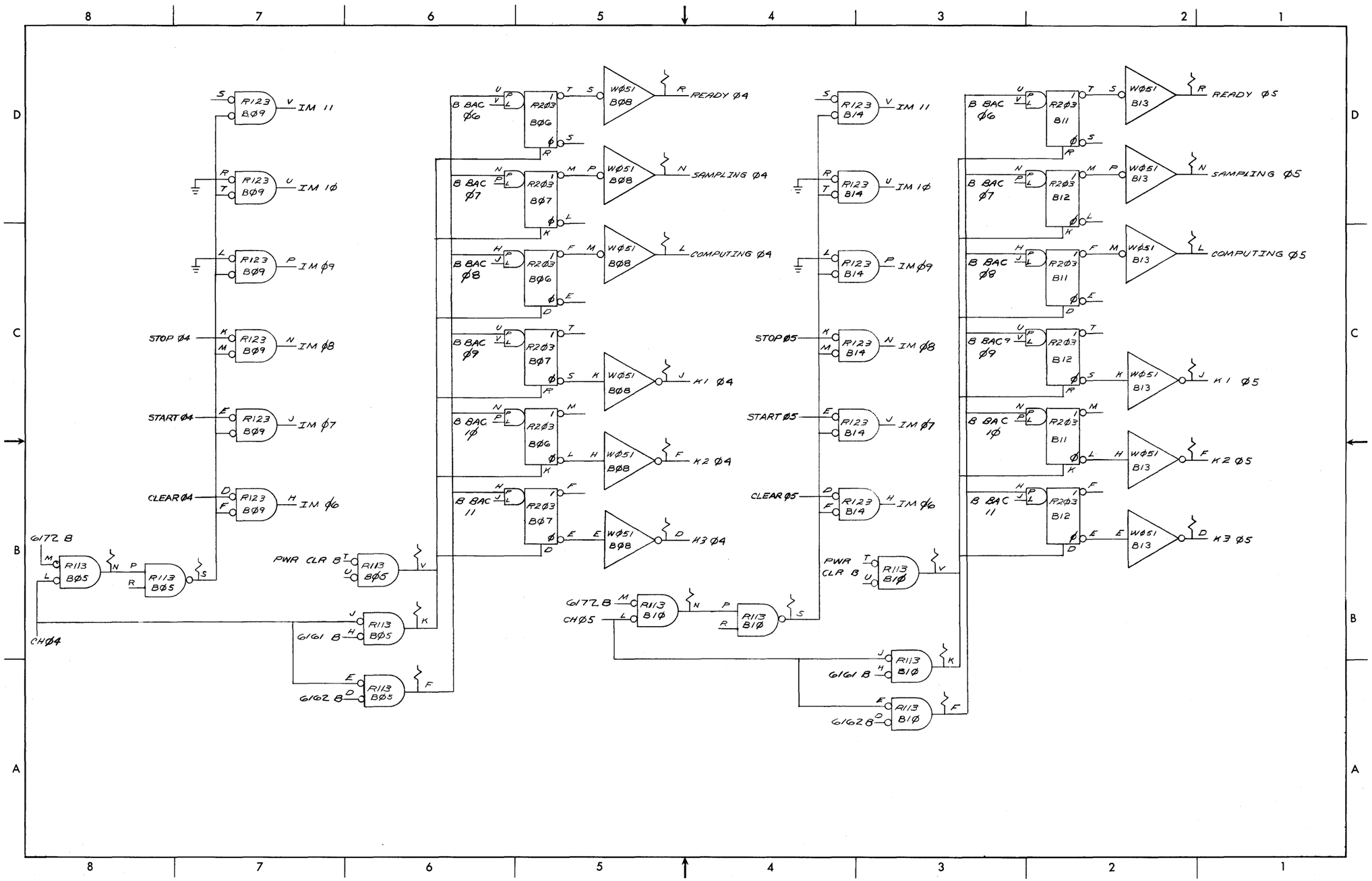


Figure 6-8 D-BS-AF17-0-3 LOC Control Logic (Ch. 00 to 07) Block Schematic Diagram (Sheet 3)

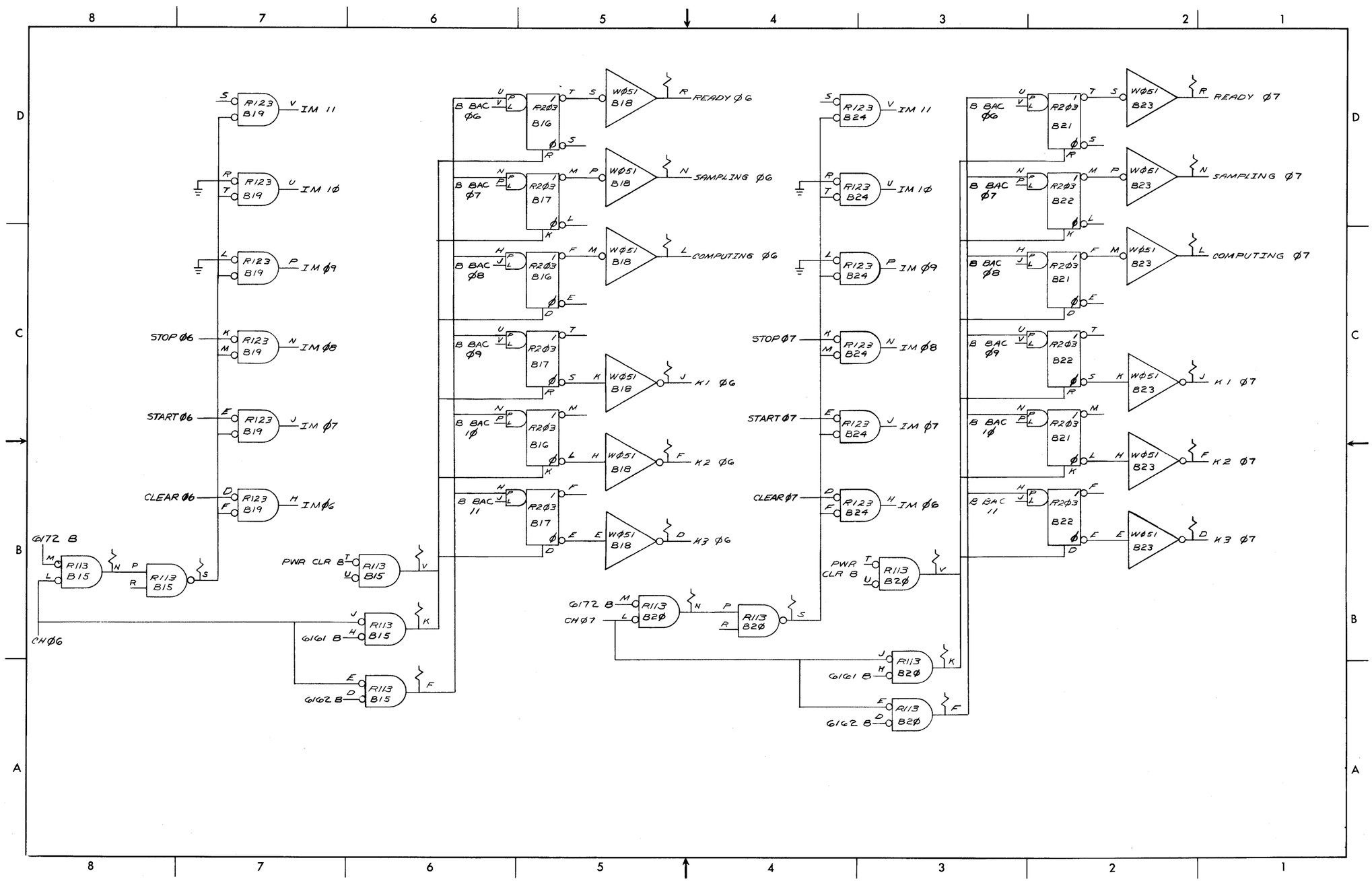


Figure 6-8 D-BS-AF17-0-3 LOC Control Logic (Ch. 00 to 07) Block Schematic Diagram (Sheet 4)

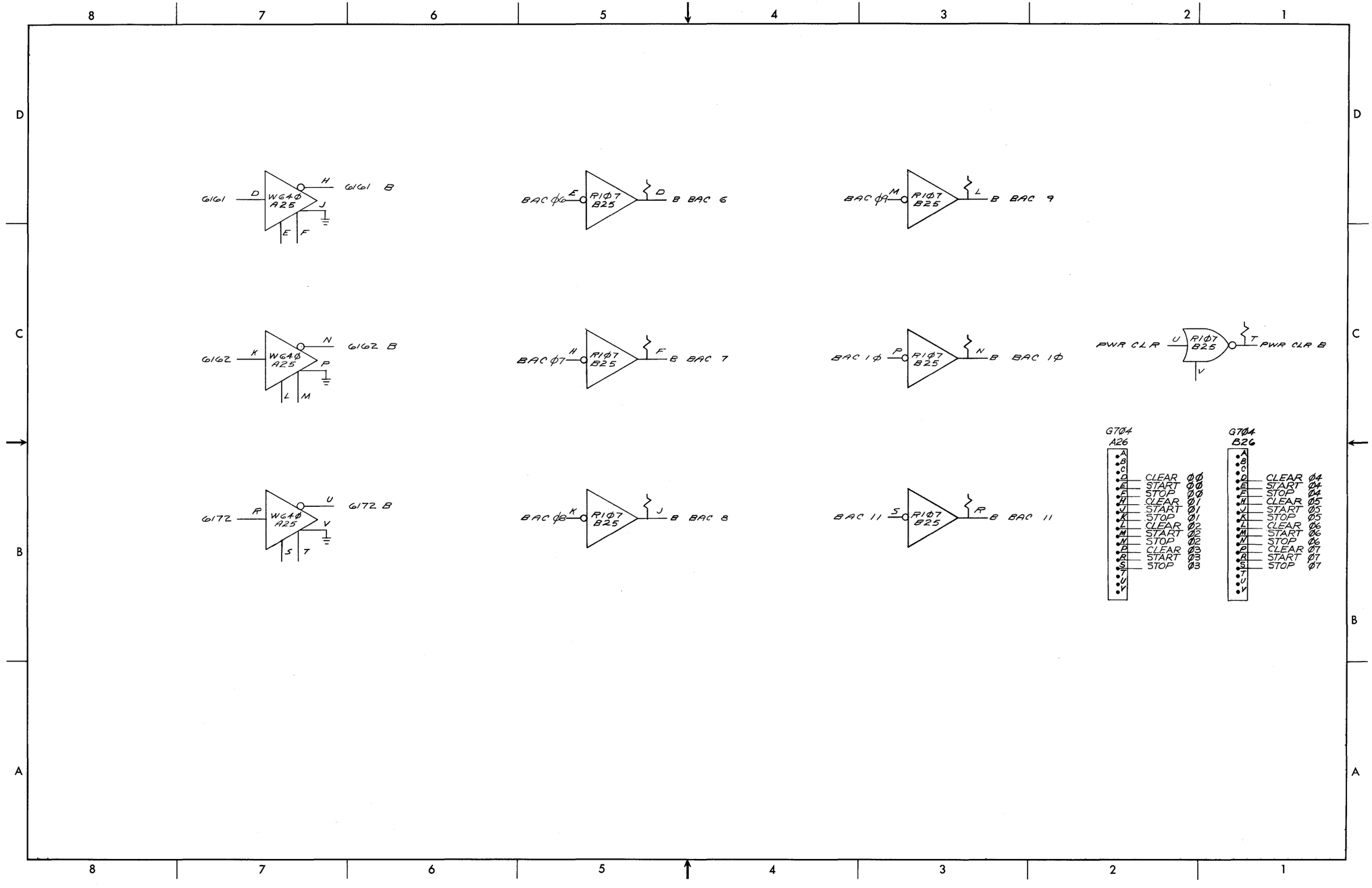


Figure 6-9 D-BS-AF17-0-2 IOT and BAC Buffer Logic Block Schematic Diagram

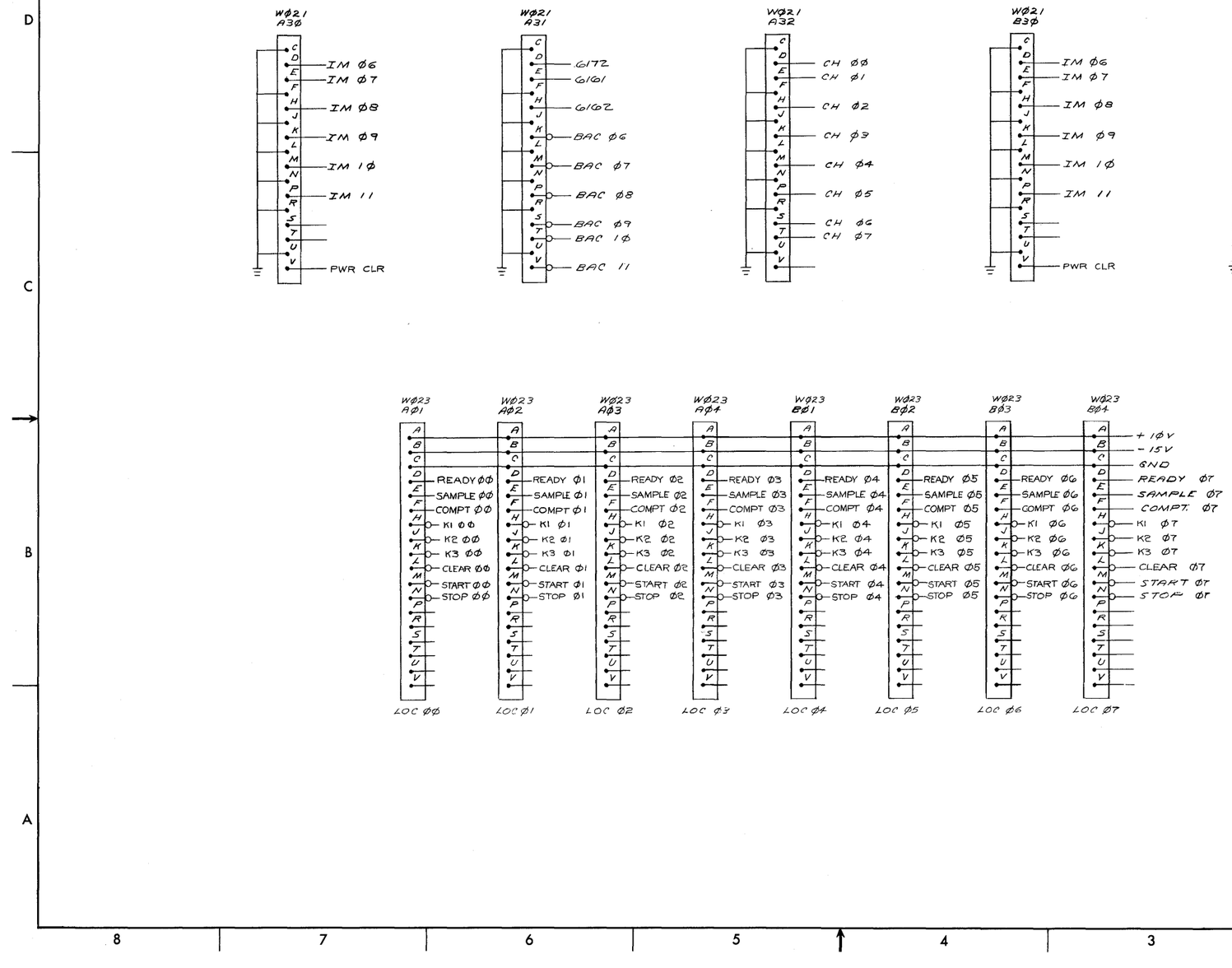


Figure 6-10 D-IC-AF17-0-4 H300 and H301 LOC Control Cable Diagram

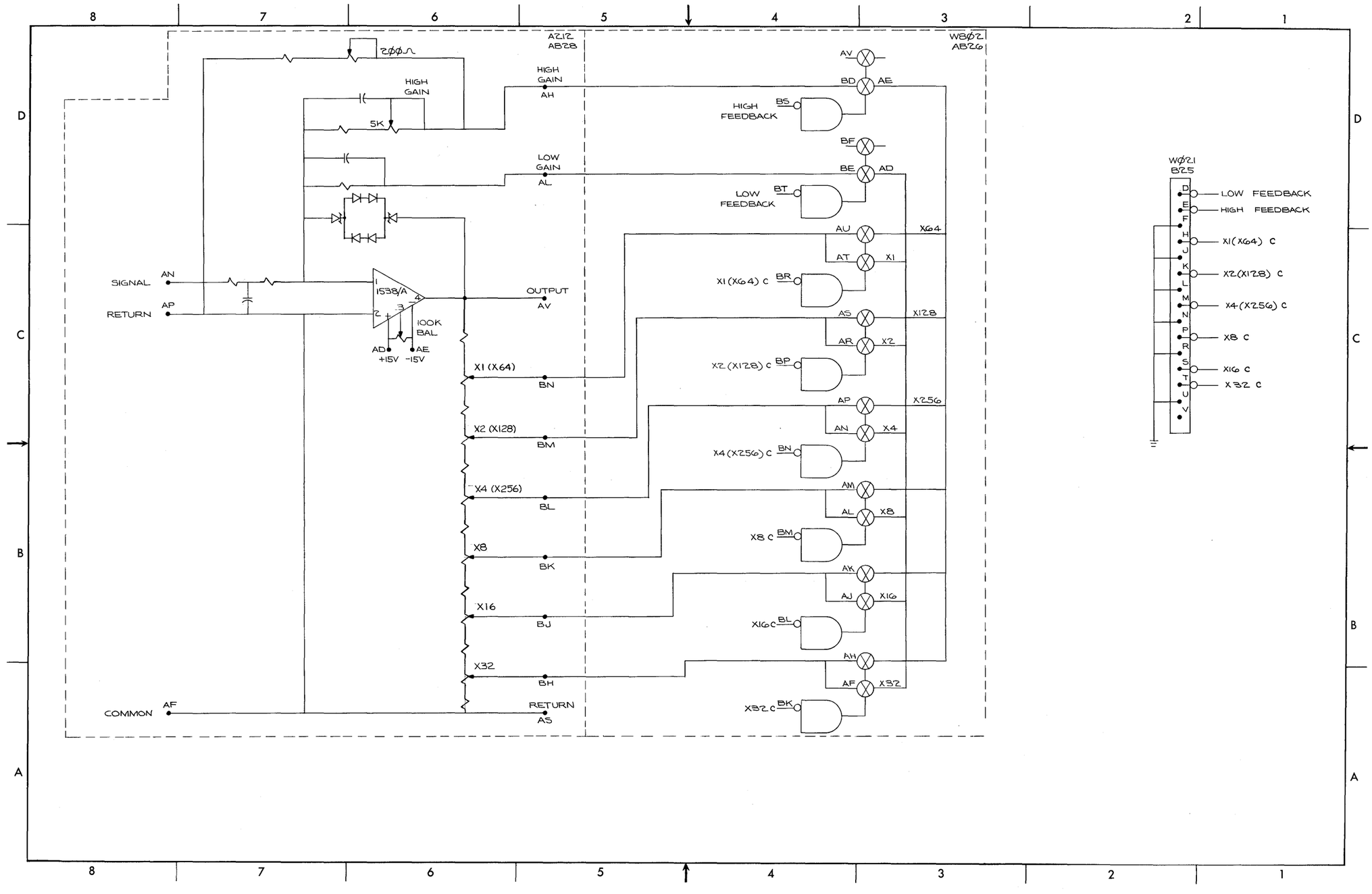


Figure 6-11 D-BS-AG04-0-2 Variable Gain Amplifier Block Schematic Diagram

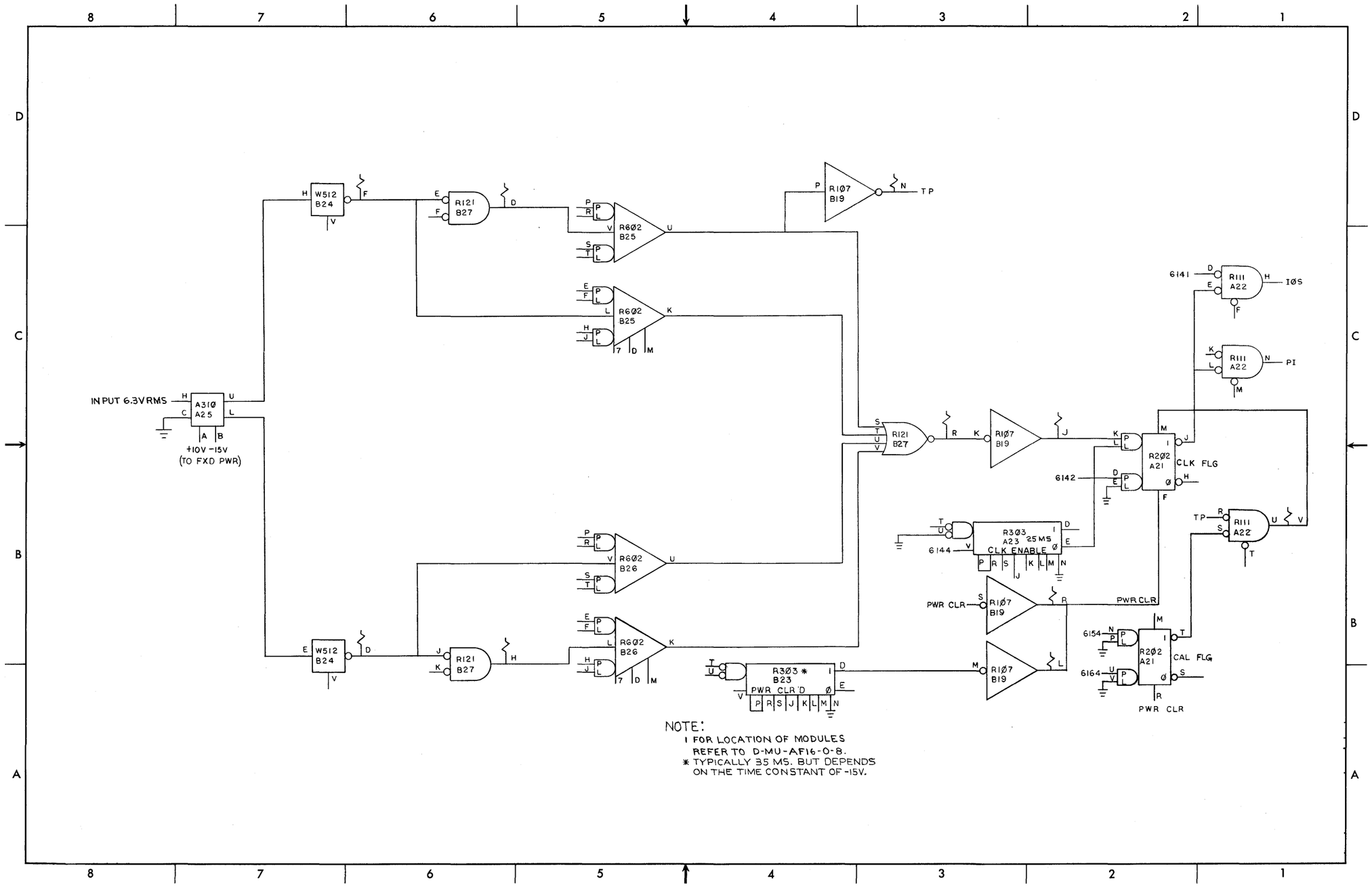


Figure 6-12 D-BS-DK01-A-1 Four Times Line Frequency Clock Block Schematic Diagram

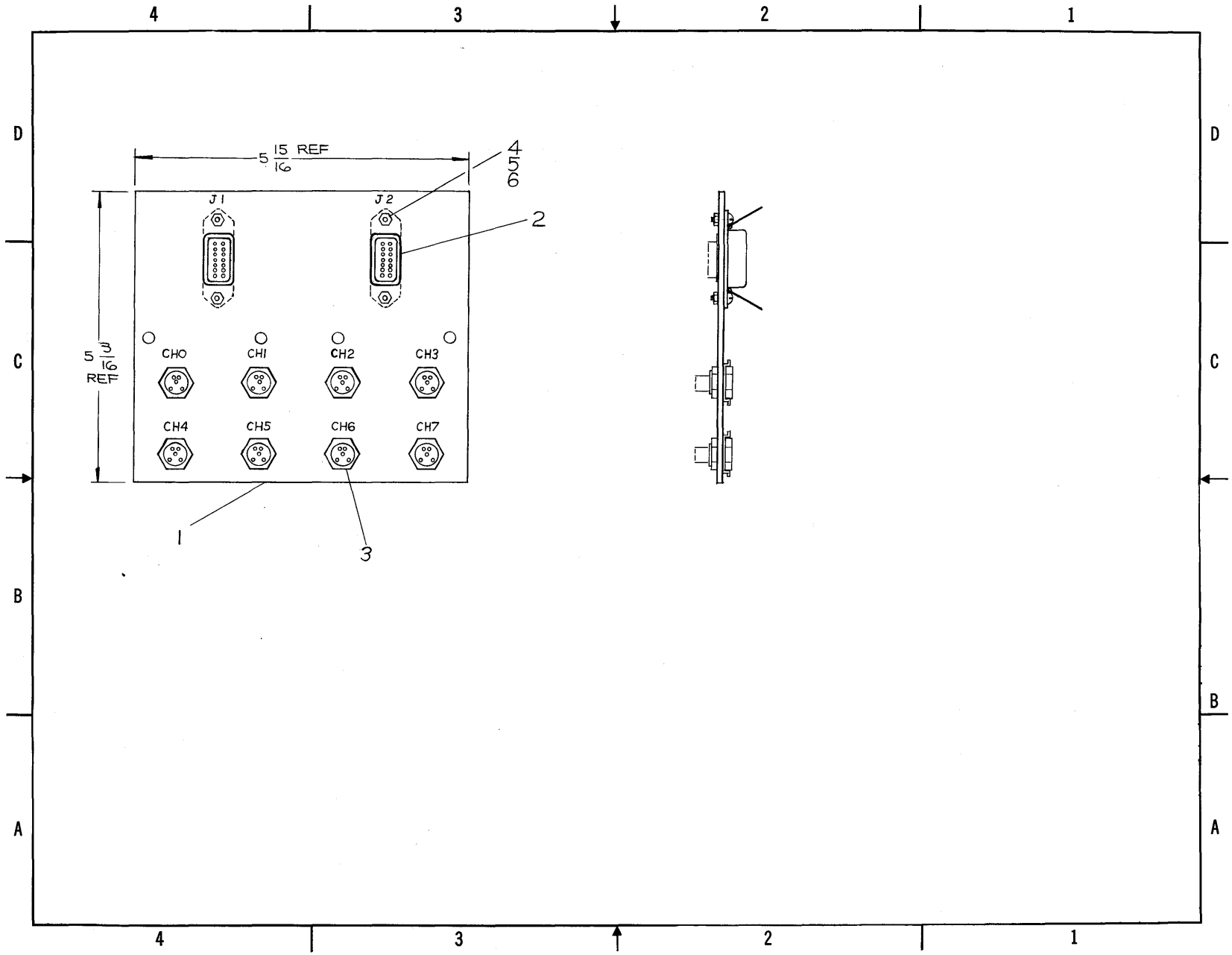


Figure 6-13 C-AD-7005925-0-0 H303 Amplifier Mounting
Panel Connector Location Diagram

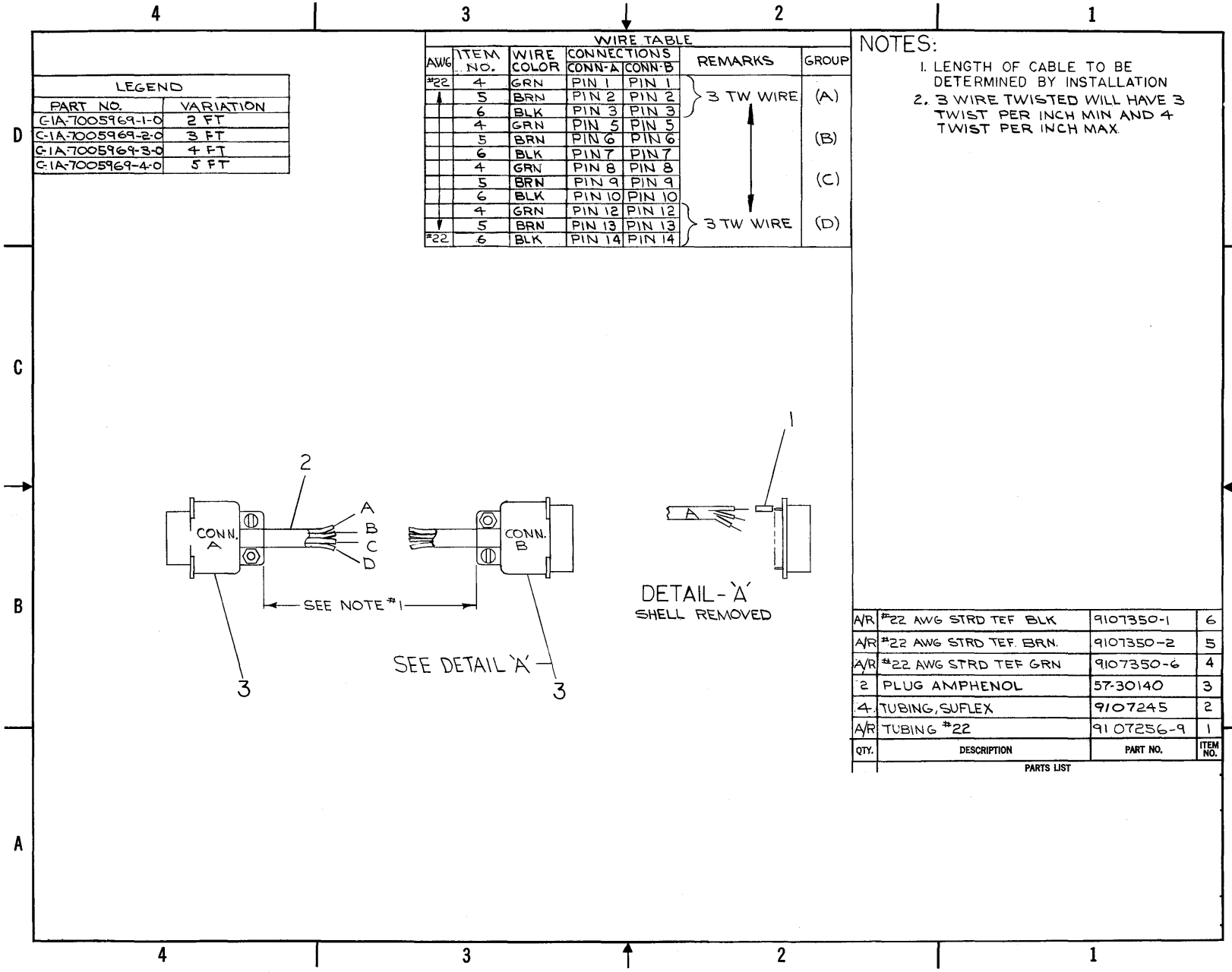


Figure 6-14 C-IA-7005969-0-0 H303 Amplifier Mounting Panel Cable Assembly Diagram

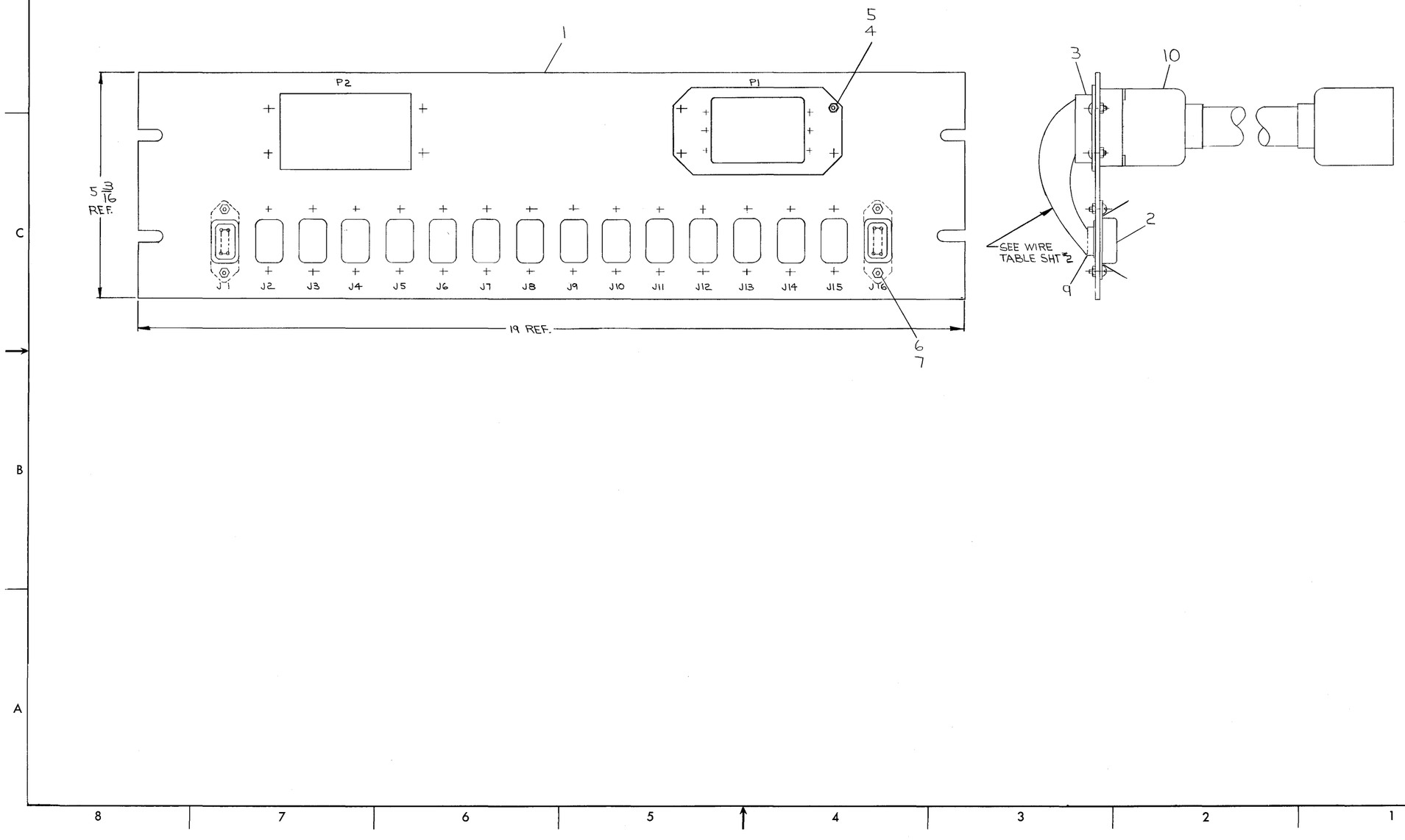
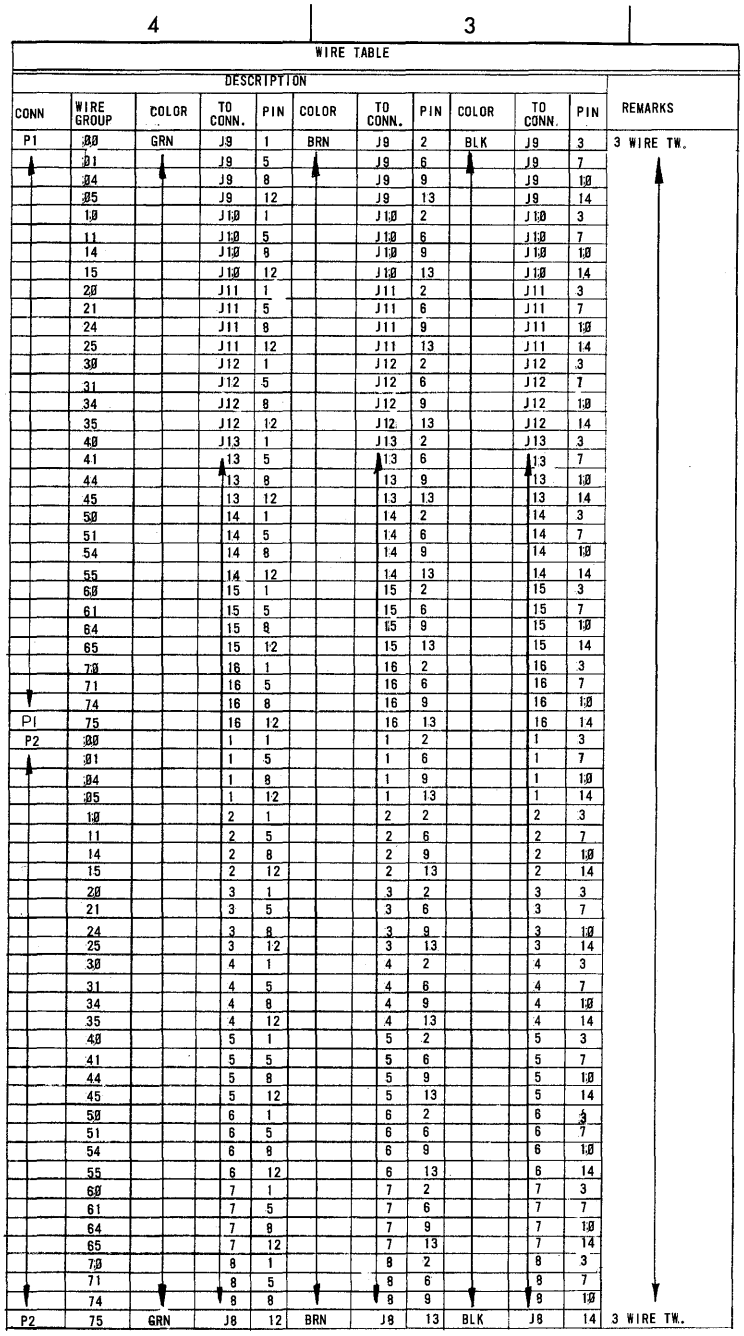


Figure 6-15 D-UA-H302-0-0 H302 Panel Connector Location Diagram (Sheet 1)



4					3						
WIRE TABLE											
DESCRIPTION											
CONN	WIRE GROUP	COLOR	TO CONN.	PIN	COLOR	TO CONN.	PIN	COLOR	TO CONN.	PIN	REMARKS
P1	00	GRN	J9	1	BRN	J9	2	BLK	J9	3	3 WIRE TW.
	01		J9	5		J9	6		J9	7	
	04		J9	8		J9	9		J9	10	
	05		J9	12		J9	13		J9	14	
	10		J10	1		J10	2		J10	3	
	11		J10	5		J10	6		J10	7	
	14		J10	8		J10	9		J10	10	
	15		J10	12		J10	13		J10	14	
	20		J11	1		J11	2		J11	3	
	21		J11	5		J11	6		J11	7	
	24		J11	8		J11	9		J11	10	
	25		J11	12		J11	13		J11	14	
	30		J12	1		J12	2		J12	3	
	31		J12	5		J12	6		J12	7	
	34		J12	8		J12	9		J12	10	
	35		J12	12		J12	13		J12	14	
	40		J13	1		J13	2		J13	3	
	41		J13	5		J13	6		J13	7	
	44		J13	8		J13	9		J13	10	
	45		J13	12		J13	13		J13	14	
	50		J14	1		J14	2		J14	3	
	51		J14	5		J14	6		J14	7	
	54		J14	8		J14	9		J14	10	
	55		J14	12		J14	13		J14	14	
	60		J15	1		J15	2		J15	3	
	61		J15	5		J15	6		J15	7	
	64		J15	8		J15	9		J15	10	
	65		J15	12		J15	13		J15	14	
	70		J16	1		J16	2		J16	3	
	71		J16	5		J16	6		J16	7	
	74		J16	8		J16	9		J16	10	
P1	75		J16	12		J16	13		J16	14	
P2	00		J1	1		J1	2		J1	3	
	01		J1	5		J1	6		J1	7	
	04		J1	8		J1	9		J1	10	
	05		J1	12		J1	13		J1	14	
	10		J2	1		J2	2		J2	3	
	11		J2	5		J2	6		J2	7	
	14		J2	8		J2	9		J2	10	
	15		J2	12		J2	13		J2	14	
	20		J3	1		J3	2		J3	3	
	21		J3	5		J3	6		J3	7	
	24		J3	8		J3	9		J3	10	
	25		J3	12		J3	13		J3	14	
	30		J4	1		J4	2		J4	3	
	31		J4	5		J4	6		J4	7	
	34		J4	8		J4	9		J4	10	
	35		J4	12		J4	13		J4	14	
	40		J5	1		J5	2		J5	3	
	41		J5	5		J5	6		J5	7	
	44		J5	8		J5	9		J5	10	
	45		J5	12		J5	13		J5	14	
	50		J6	1		J6	2		J6	3	
	51		J6	5		J6	6		J6	7	
	54		J6	8		J6	9		J6	10	
	55		J6	12		J6	13		J6	14	
	60		J7	1		J7	2		J7	3	
	61		J7	5		J7	6		J7	7	
	64		J7	8		J7	9		J7	10	
	65		J7	12		J7	13		J7	14	
	70		J8	1		J8	2		J8	3	
	71		J8	5		J8	6		J8	7	
	74		J8	8		J8	9		J8	10	
P2	75	GRN	J8	12	BRN	J8	13	BLK	J8	14	3 WIRE TW.

Figure 6-15 D-UA-H302-0-0 Panel Connector Location Diagram (Sheet 2)

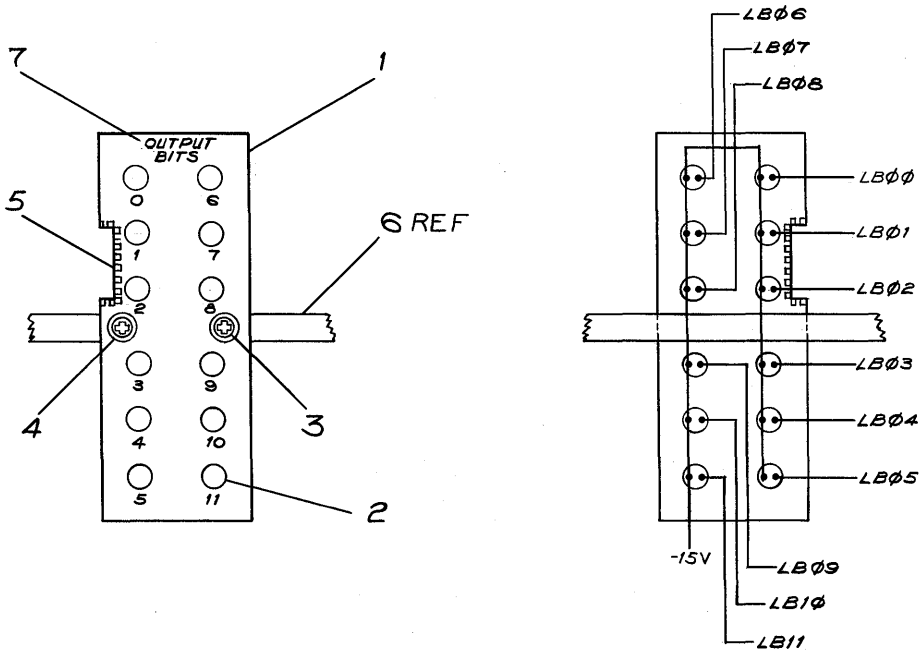


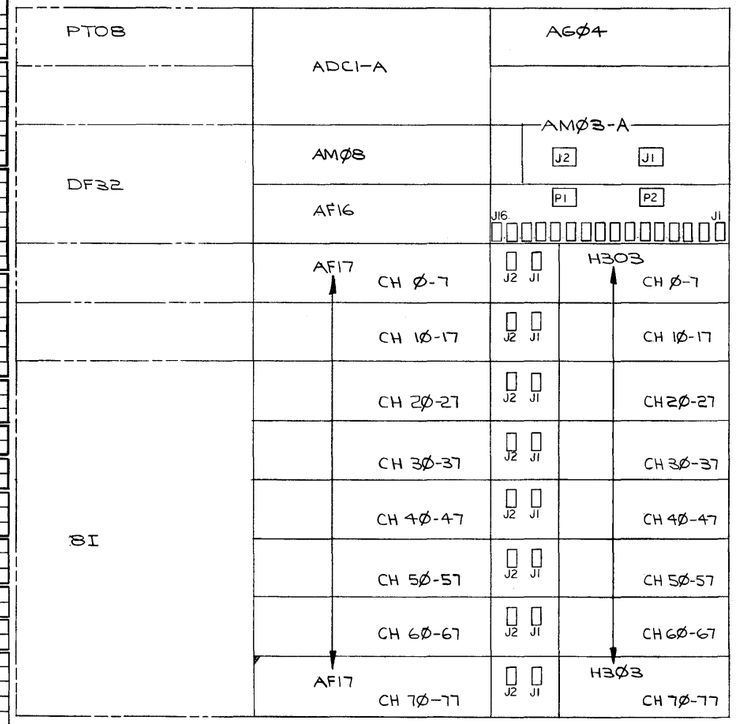
Figure 6-16 D-IA-7005949-0-0 H302 Panel Cable Wiring Diagram

LOCATIONS			DESCRIPTIONS		SIGNALS
BI	DF32		TYPE	LENGTH	
J01	C09		W031-W031	7405552-4	BAC 0-8
J02	C10				BAC 9-11 IOPS
J03	C11				MB 0-5
J04	C12				MB 6-11
J05	C13				IB 0-8
J06	C14				IB 9-11, SKIP, INT
J07	C15				DA 0-8
J08	C16				DA 9-11 BRK RQ
J09	C17				DATA 0-8
J10	C18				DATA 9-11, 3CYC
J11	C19		W031-W031	7405552-4	EXTD ADD 0-2
DF32	PTO8		W011-W021		
D09	A6			7405820-1	BAC 0-8
D10	B6				BAC 9-11 IOPS
D11	A8				MB 0-5
D12	B8				MB 6-11
D13	A13				IB 0-8
D14	B13		W011-W021	7405820-1	IB 9-11 SKIP, INT
PTO8	ADC1-A		W031-W031		
A7	C27			7005550-7	BAC 0-8
B7	C28				BAC 9-11 IOPS
A9	C29				MB 0-5
B9	C30				MB 6-11
A14	C31				IB 0-8
B14	C32		W031-W031	7005550-7	IB 9-11 SKIP, INT
ADC1-A	AMO8		W011-W021		
D27	A1			7405556-2	BAC 0-8
D28	A2				BAC 9-11 IOPS
D29	A3				MB 0-5
D30	A4				MB 6-11
D31	A5				IB 0-8
D32	A6		W011-W021	7405556-2	IB 9-11 SKIP, INT
AMO8	AF16				
B1	B1		W011-W021	7405556-1	BAC 0-8
B2	B2				BAC 9-11 IOPS
B3	B3				MB 0-5
B4	B4				MB 6-11
B5	B5				IB 0-8
B6	B6		W011-W021	7405556-1	IB 9-11 SKIP, INT
AMO8	AMO3				
B31	C31		W023-W023	7405151-1	Z REG 0-15
B32	C32		W023-W023	7405151-1	X & Y REG 0-7
AMO8	ADC1-A				
A32	D6		W021-W011	7405556-2	CONTROL SIGNAL
AMO3-A	AF16				
B32	A28		W023-W023	7405151-1	X & Y CORD
AMO3-A	H302				
J1	P1		WINCH-WINCH	7005939	ANALOG SIGNALS
J2	P2		WINCH-WINCH	7005939	ANALOG SIGNALS
AF16	AF17				
A26	A30		W021-W011	7405556-2	IM 6-11
B28	A31		W021-W011	7405556-2	IOTS, BAC 6-11
AF16	AG04				
A27	B29		W011-W021	7405556-3	AMPL GAIN
AG04 OUTPUT	ADC1 INPUT		BNC-BNC	7005977	ANALOG SIGNAL
AF17	AF17				
B30	A30		W021-W011	7405556-1	IM 6-11
B31	A31		W021-W011	7405556-1	BAC 6-11, IOTS

LOCATIONS			DESCRIPTIONS	
AF16	AF17	CHANNEL	TYPE	LENGTH
A29	A32	0-7	W021-W021	7405524-3-0
A30	A32	10-17		7405524-3-0
A31	A32	20-27		7405524-1-0
A32	A32	30-37		7405524-1-0
B28	A32	40-47		7405524-1-0
B30	A32	50-57		7405524-2-0
B31	A32	60-67		7405524-2-0
B32	A32	70-77	W021-W021	7405524-2-0

LOCATIONS			DESCRIPTION	
H302	H303	CHANN	TYPE	LENGTH
J1	J1	0-7	AMP-AMP	7005969-1
J9	J2			
J2	J1	10-17		7005969-1
J10	J2			
J3	J1	20-27		7005969-2
J11	J2			
J4	J1	30-37		7005579-2
J12	J2			
J5	J1	40-47		7005969-3
J13	J2			
J6	J1	50-57		7005969-3
J14	J2			
J7	J1	60-67		7005969-4
J15	J2			
J8	J1	70-77	AMP-AMP	7005969-4
J16	J2			

REF. FOR ATTACHMENT TO BI CABINET



REAR VIEW

Figure 6-17 D-AR-AF06-A-2 GLC-8 Interface System Cable Configuration Diagram

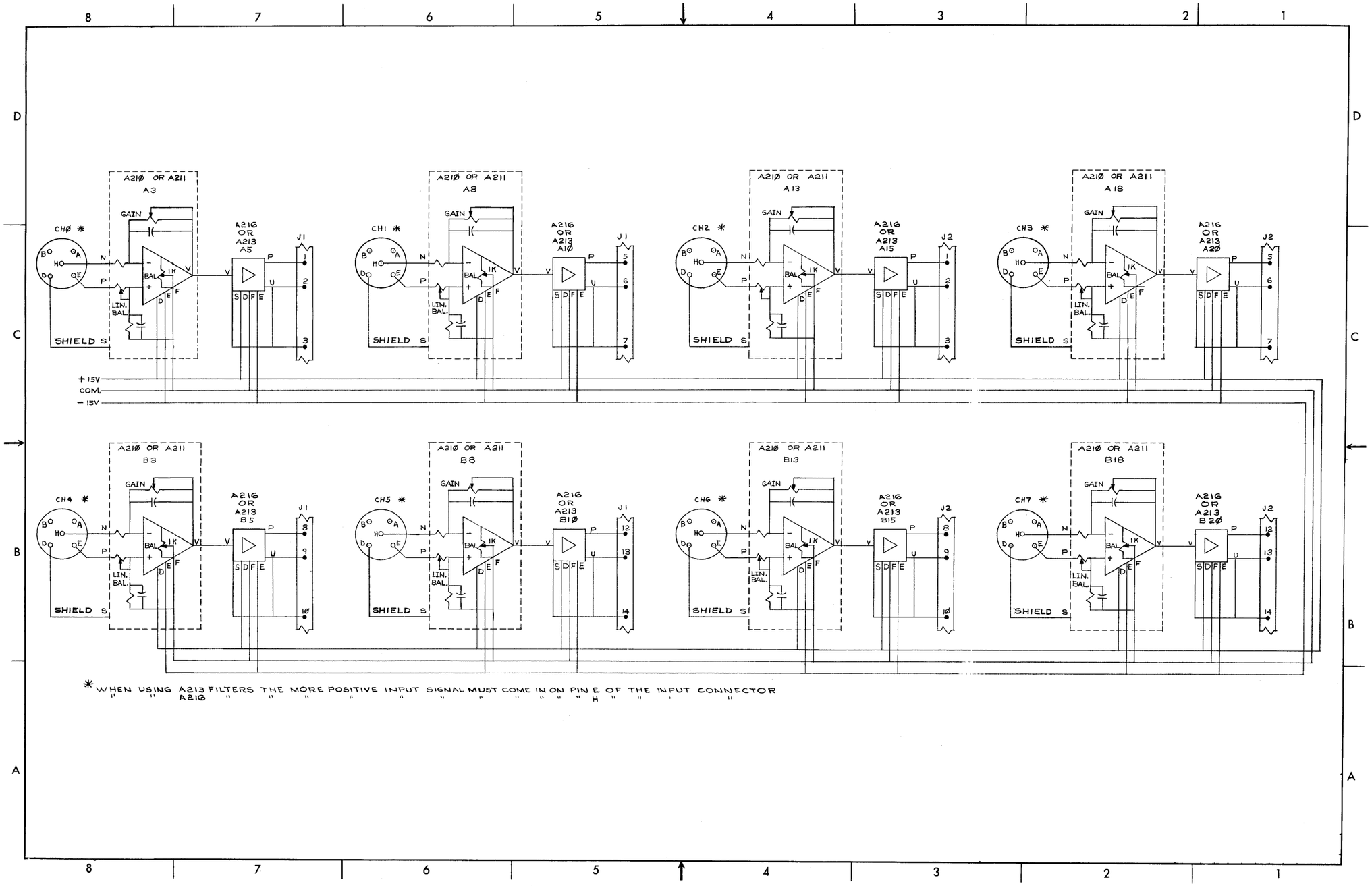


Figure 6-18 D-BS-H303-0-2 Input Buffer Amplifier Block Schematic Diagram

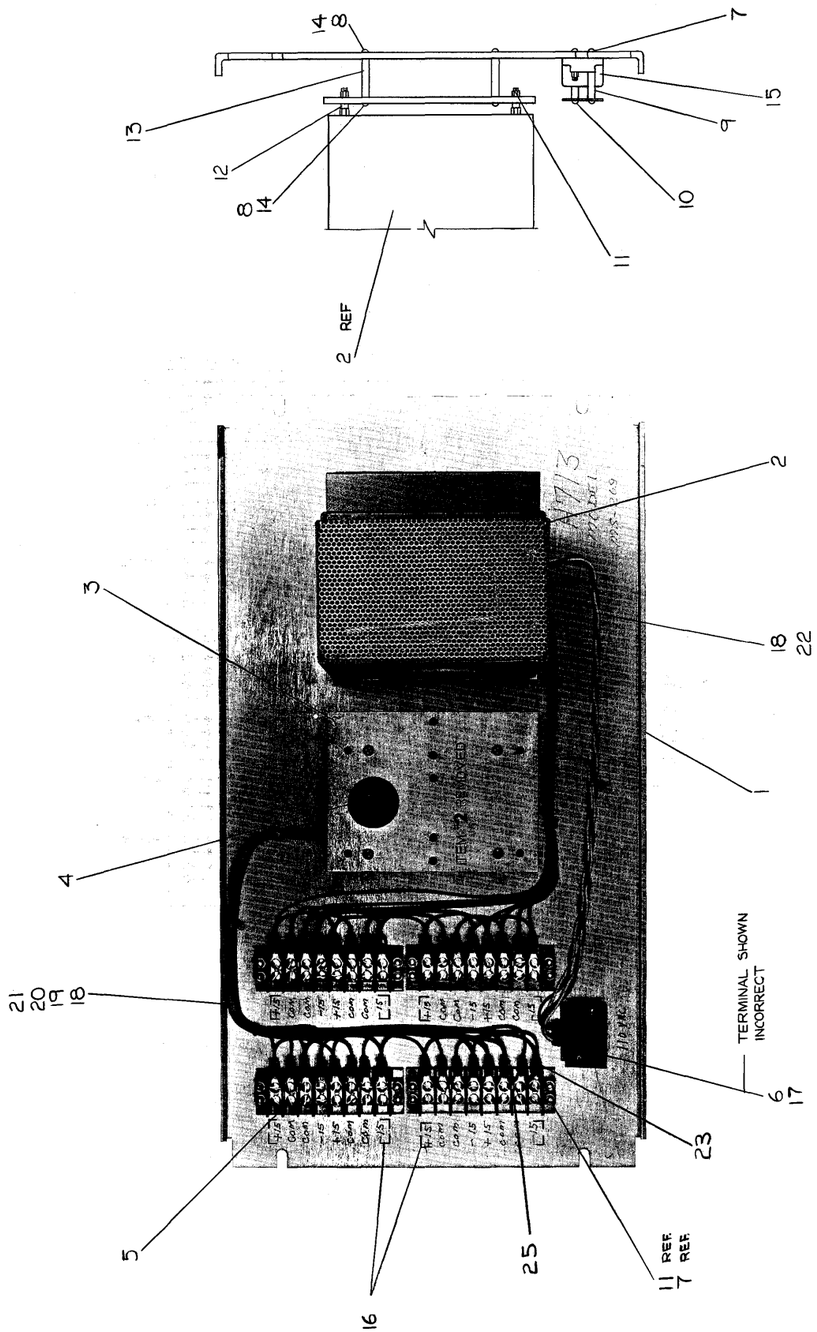


Figure 6-19 D-UA-H713-0-0 H713 Power Supply Wiring Diagram (Sheet 1)

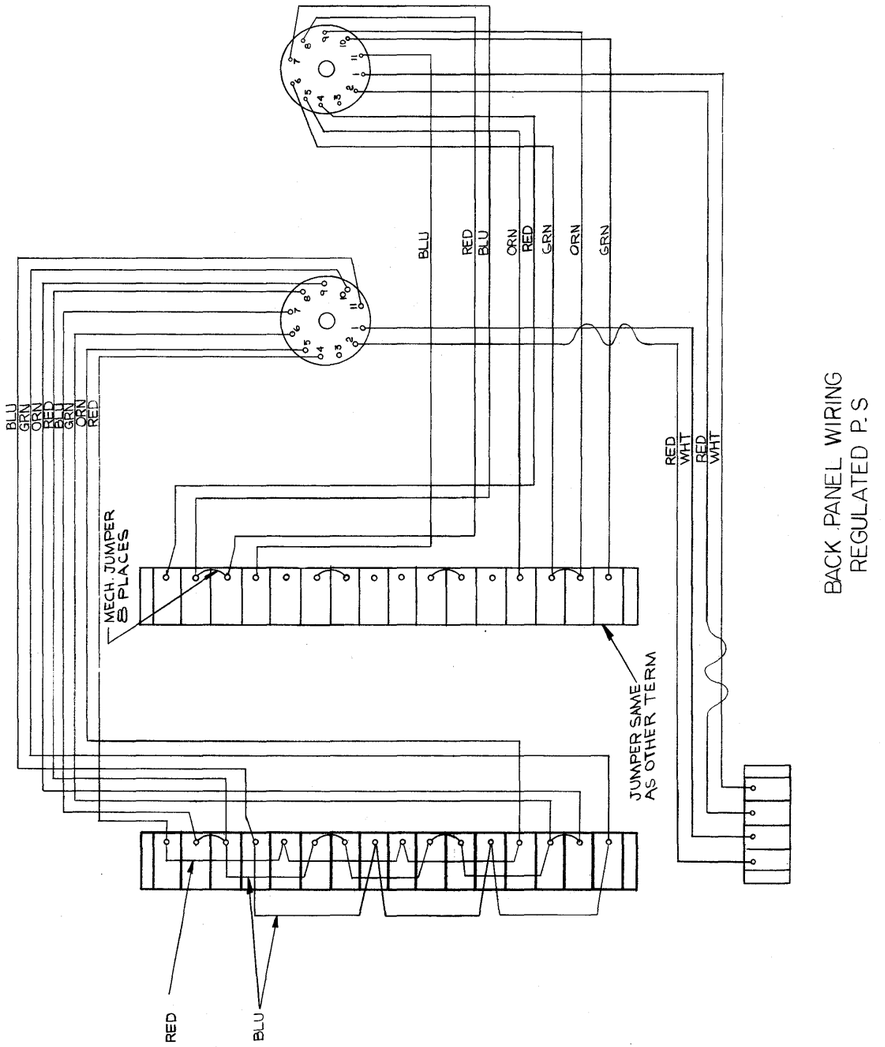


Figure 6-19 D-UA-H713-0-0

H713 Power Supply Wiring Diagram (Sheet 2)

Not Available

Figure 6-21 B-CS-H783-0-1 783 Power Supply Block Schematic Diagram

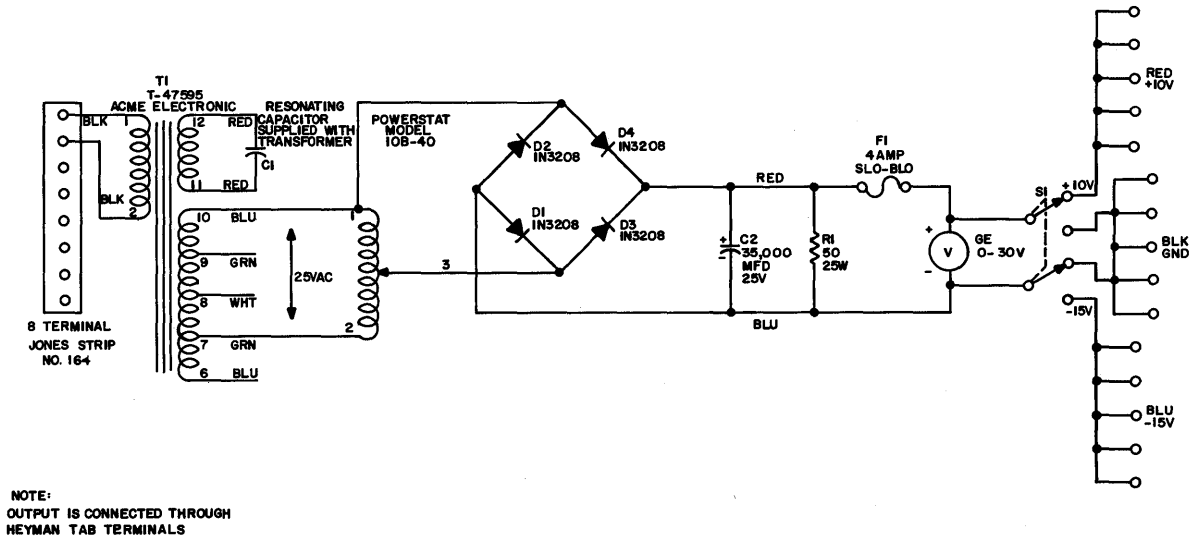


Figure 6-22 CS-B-734B 734B Variable Power Supply Block Schematic Diagram

Not Available

Figure 6-23 D-AR-AF06-A-2 System Interface Cable Interconnection Diagram

Not Available

Figure 6-24 D-UA-H961-0-0 H961 Rack Installation Diagram

NOTES:

1. CONNECTIONS ON ITEMS *1 & *2 TO BE SOLDERED AND LOCATED AT MINIMUM PRACTICAL HEIGHT ABOVE BLOCK
2. ALL CONN BLOCKS TO BE GROUNDED TO GND LUGS AS SHOWN.
3. USE YELLOW WIRE (ITEM *3) FOR MACHINE WRAPPED & BLUE WIRE (ITEM *4) FOR HAND WRAPPED WIRING.

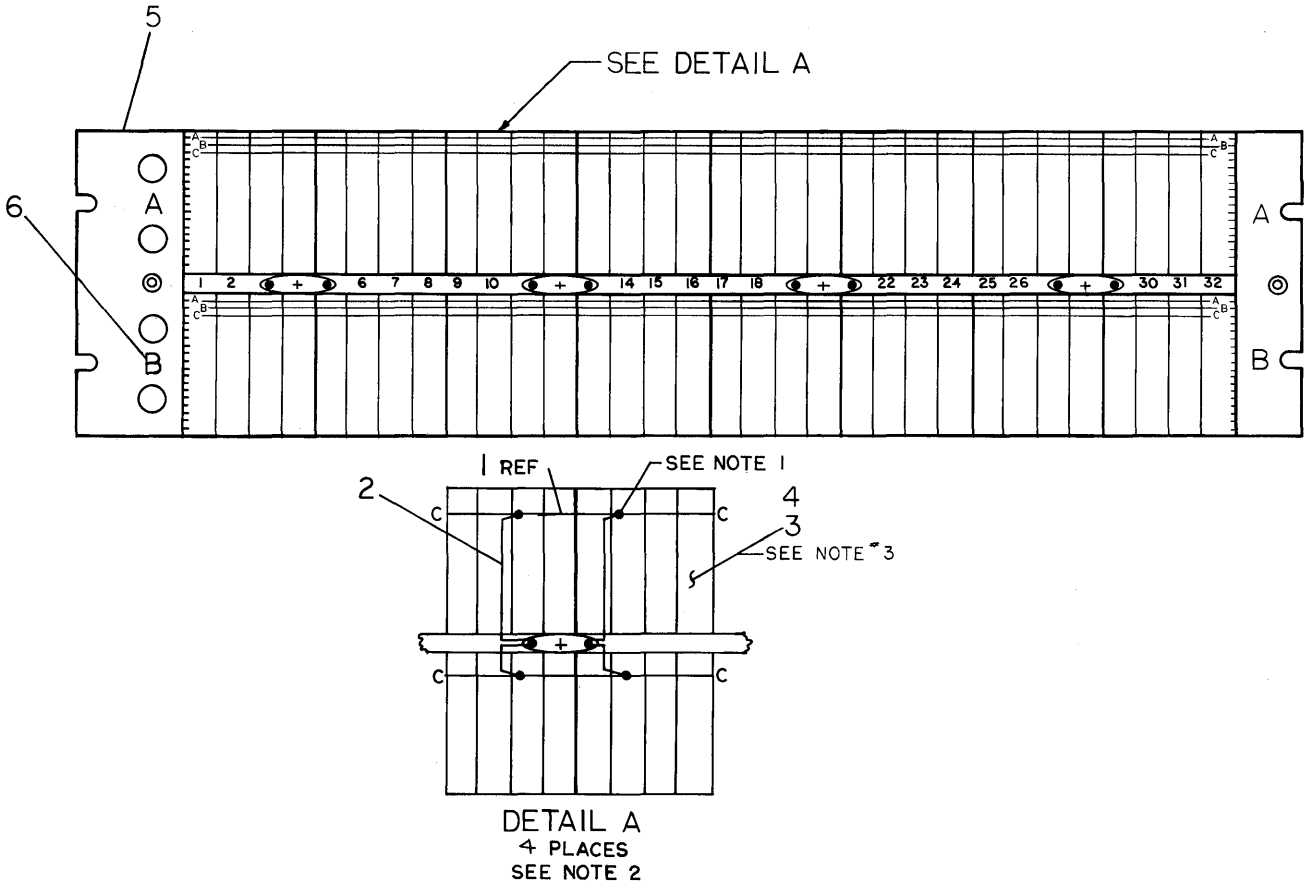


Figure 6-25 C-AD-7005956-0-0 A17 Assembly Wiring Diagram

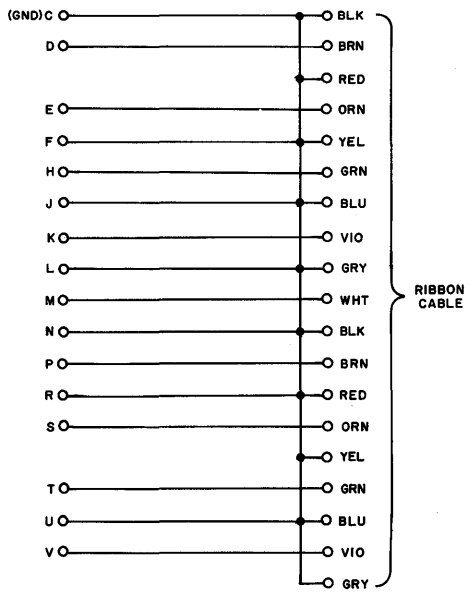


Figure 6-26 B-CS-W021-1-0 W021 Signal Cable Connector Block Schematic Diagram

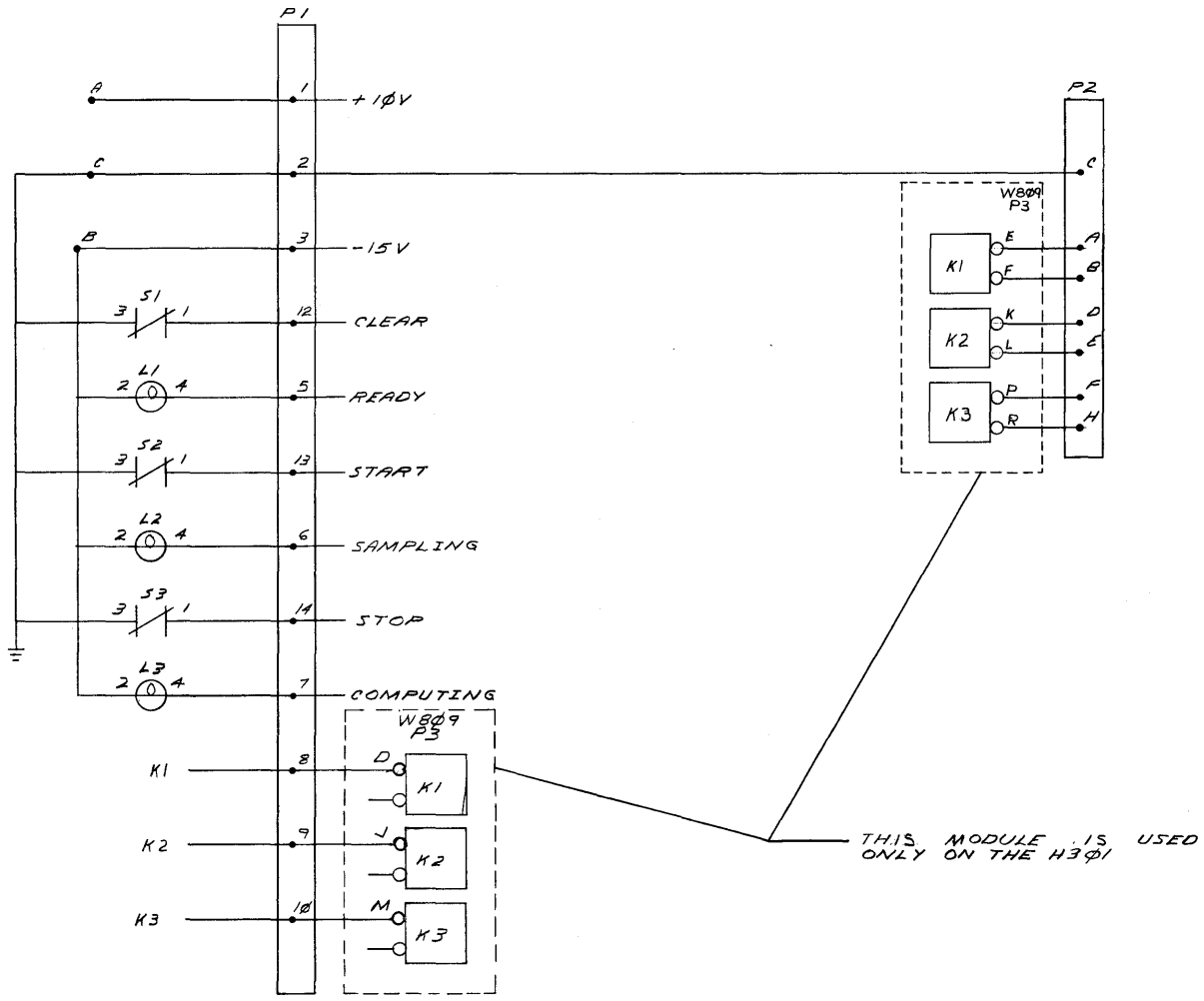


Figure 6-27 D-BS-H300-0-2 H300 Cable Connection Diagram

WIRE TABLE

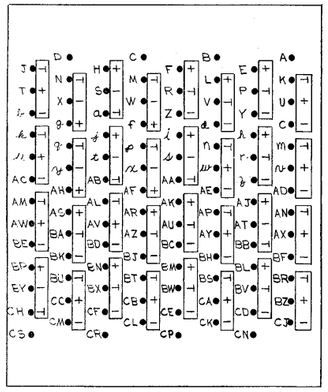
ITEM NO.	AWG	DESCRIPTION COLOR	CONNECTIONS FROM	TO	REMARKS
5	22	GRN	J1 BN	ØØ *	3 WIRE TW
4		BRN	CF	ØØ	
3		BLK	BX	ØØ	
5		GRN	BP	Ø1	
4		BRN	BY	Ø1	
3		BLK	CH	Ø1	
5		GRN	BL	Ø4	
4		BRN	CD	Ø4	
3		BLK	BV	Ø4	
5		GRN	BM	Ø5	
4		BRN	CE	Ø5	
3		BLK	BW	Ø5	
5		GRN	AV	1Ø	
4		BRN	BD	1Ø	
3		BLK	AL	1Ø	
5		GRN	AW	11	
4		BRN	BE	11	
3		BLK	AM	11	
5		GRN	AJ	14	
4		BRN	AT	14	
3		BLK	BB	14	
5		GRN	AK	15	
4		BRN	BC	15	
3		BLK	AU	15	
5		GRN	CB	2Ø	
4		BRN	CL	2Ø	
3		BLK	BT	2Ø	
5		GRN	CC	21	
4		BRN	CM	21	
3		BLK	BU	21	
5		GRN	BZ	24	
4		BRN	CJ	24	
3	22	BLK	J1 BR	24 *	3 WIRE TW

ITEM NO.	AWG	DESCRIPTION COLOR	CONNECTIONS FROM	TO	REMARKS
5	22	GRN	J1 CA	25 *	3 WIRE TW
4		BRN	CK	25	
3		BLK	BS	25	
5		GRN	AR	3Ø	
4		BRN	BJ	3Ø	
3		BLK	AZ	3Ø	
5		GRN	AS	31	
4		BRN	BK	31	
3		BLK	BA	31	
5		GRN	AX	34	
4		BRN	BF	34	
3		BLK	AN	34	
5		GRN	AY	35	
4		BRN	BH	35	
3		BLK	AP	35	
5		GRN	AF	4Ø	
4		BRN	X	4Ø	
3		BLK	P	4Ø	
5		GRN	AH	41	
4		BRN	y	41	
3		BLK	q	41	
5		GRN	V	44	
4		BRN	AD	44	
3		BLK	m	44	
5		GRN	W	45	
4		BRN	AE	45	
3		BLK	n	45	
5		GRN	f	5Ø	
4		BRN	w	5Ø	
3		BLK	M	5Ø	
5		GRN	g	51	
4		BRN	X	51	
3	22	BLK	J1 N	51 *	3 WIRE TW

ITEM NO.	AWG	DESCRIPTION COLOR	CONNECTIONS FROM	TO	REMARKS
5	22	GRN	J1 U	54 *	3 WIRE TW
4		BRN	C	54	
3		BLK	K	54	
5		GRN	L	55	
4		BRN	d	55	
3		BLK	V	55	
5		GRN	J	6Ø	
4		BRN	I	6Ø	
3		BLK	AB	6Ø	
5		GRN	U	61	
4		BRN	AC	61	
3		BLK	K	61	
5		GRN	h	64	
4		BRN	Z	64	
3		BLK	r	64	
5		GRN	i	65	
4		BRN	S	65	
3		BLK	AA	65	
5		GRN	H	7Ø	
4		BRN	S	7Ø	
3		BLK	d	7Ø	
5		GRN	T	71	
4		BRN	b	71	
3		BLK	J	71	
5		GRN	E	74	
4		BRN	Y	74	
3		BLK	P	74	
5		GRN	F	75	
4		BRN	Z	75	3 WIRE TW
3	22	BLK	J1 R	75 *	

NOTES:

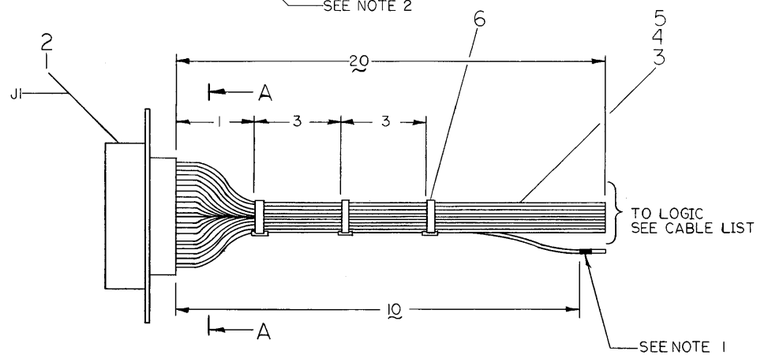
1. LABLE EACH WIRE WITH IDENTIFICATION AS SHOWN ON THE WIRE TABLE(LETTERS WITH AN * ASTERICK BESIDE IT.)
2. 3 WIRE TWISTED WILL HAVE 3 TWISTS PER INCH MIN. AND 4 TWISTS PER INCH MAX.



VIEW A-A

+ = HI GREEN
− = LO BROWN } TWISTED
↓ = GUARD BLACK

SEE NOTE 2



QTY.	DESCRIPTION	PART NO.	ITEM NO.
3	TY RAP # SST-1-B	9007031	6
A/R	#22 AWG. STRD. TEF. GRN.	9107350-3	5
A/R	#22 AWG. STRD. TEF. BRN.	9107350-2	4
A/R	#22 AWG. STRD. TEF. BLK.	9107350-1	3
104	PINS #100-20185 WINCHESTER	12-05732	2
1	WINCHESTER CONN #XAC-104-ST-2016	12-05730	1

PARTS LIST

Figure 6-28 D-IA-7005805-0-0 H300 Winchester Cable Harness Diagram

WIRE TABLE

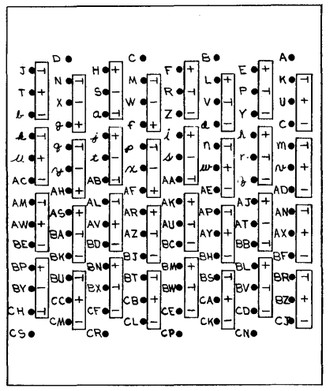
ITEM NO.	AWG	DESCRIPTION COLOR	CONNECTIONS FROM	CONNECTIONS TO	REMARKS
5	22	GRN	J1 BN	J2 BN	3 WIRE TW
4	↑	BRN	CF	CF	
3		BLK	BX	BX	
5		GRN	BP	BP	
4		BRN	BY	BY	
3		BLK	CH	CH	
5		GRN	BL	BL	
4		BRN	CD	CD	
3		BLK	BV	BV	
5		GRN	BM	BM	
4		BRN	CE	CE	
3		BLK	BW	BW	
5		GRN	AV	AV	
4		BRN	BD	BD	
3		BLK	AL	AL	
5		GRN	AW	AW	
4		BRN	BE	BE	
3		BLK	AM	AM	
5		GRN	AJ	AJ	
4		BRN	AT	AT	
3		BLK	BB	BB	
5		GRN	AK	AK	
4		BRN	BC	BC	
3		BLK	AU	AU	
5		GRN	CB	CB	
4		BRN	CL	CL	
3		BLK	BT	BT	
5		GRN	CC	CC	
4		BRN	CM	CM	
3		BLK	BU	BU	
5		GRN	BZ	BZ	
4	↓	BRN	CJ	CJ	3 WIRE TW
3	22	BLK	J1 BR	J2 BR	

ITEM NO.	AWG	DESCRIPTION COLOR	CONNECTIONS FROM	CONNECTIONS TO	REMARKS
5	22	GRN	J1 CA	J2 CA	3 WIRE TW
4	↑	BRN	CK	CK	
3		BLK	BS	BS	
5		GRN	AR	AR	
4		BRN	BJ	BJ	
3		BLK	AZ	AZ	
5		GRN	AS	AS	
4		BRN	BK	BK	
3		BLK	BA	BA	
5		GRN	AX	AX	
4		BRN	BF	BF	
3		BLK	AN	AN	
5		GRN	AY	AY	
4		BRN	BH	BH	
3		BLK	AP	AP	
5		GRN	AF	AF	
4		BRN	X	X	
3		BLK	P	P	
5		GRN	AH	AH	
4		BRN	y	y	
3		BLK	q	q	
5		GRN	V	V	
4		BRN	AD	AD	
3		BLK	m	m	
5		GRN	W	W	
4		BRN	AE	AE	
3		BLK	n	n	
5		GRN	f	f	
4		BRN	w	w	
3		BLK	M	M	
5		GRN	g	g	
4	↓	BRN	X	X	3 WIRE TW
3	22	BLK	J1 N	J2 N	

ITEM NO.	AWG	DESCRIPTION COLOR	CONNECTIONS FROM	CONNECTIONS TO	REMARKS
5	22	GRN	J1 U	J2 U	3 WIRE TW
4	↑	BRN	C	C	
3		BLK	K	K	
5		GRN	L	L	
4		BRN	d	d	
3		BLK	V	V	
5		GRN	J	J	
4		BRN	t	t	
3		BLK	AB	AB	
5		GRN	U	U	
4		BRN	AC	AC	
3		BLK	k	k	
5		GRN	h	h	
4		BRN	Z	Z	
3		BLK	r	r	
5		GRN	l	l	
4		BRN	S	S	
3		BLK	AA	AA	
5		GRN	H	H	
4		BRN	S	S	
3		BLK	a	a	
5		GRN	T	T	
4		BRN	b	b	
3		BLK	J	J	
5		GRN	E	E	
4		BRN	Y	Y	
3		BLK	P	P	
5		GRN	F	F	
4	↓	BRN	Z	Z	3 WIRE TW
3	22	BLK	J1 R	J2 R	

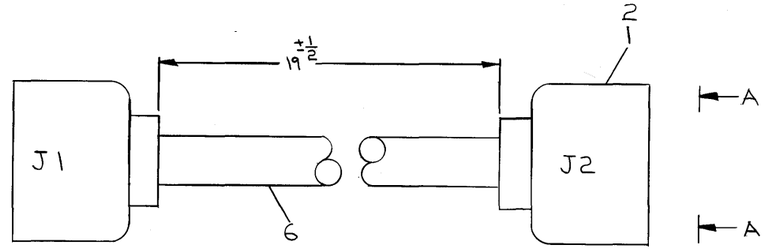
NOTES:

1. 3 WIRE TWISTED WILL HAVE 3 TWIST PER INCH MIN AND 4 TWISTS PER INCH MAX.



VIEW A-A

+ = HI GREEN
− = LO BROWN } TWISTED
↓ = GUARD BLACK



FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
D-UA-H302-0-0	A/R	TUBING, SUFLEX 1" DIA	9107248	6
	A/R	#22 AWG. STRD. TEF. GRN.	9107350-6	5
	A/R	#22 AWG. STRD. TEF. BRN.	9107350-2	4
	A/R	#22 AWG. STRD. TEF. BLK.	9107350-1	3
	192	PINS #100-2020P WINCHESTER	1205731	2
	2	CONN. WINCHESTER #XAC-109-PD-3700	125729	1

PARTS LIST

Figure 6-29 D-IA-7005939-0-0 H300 Multiplexer Input Cable Diagram

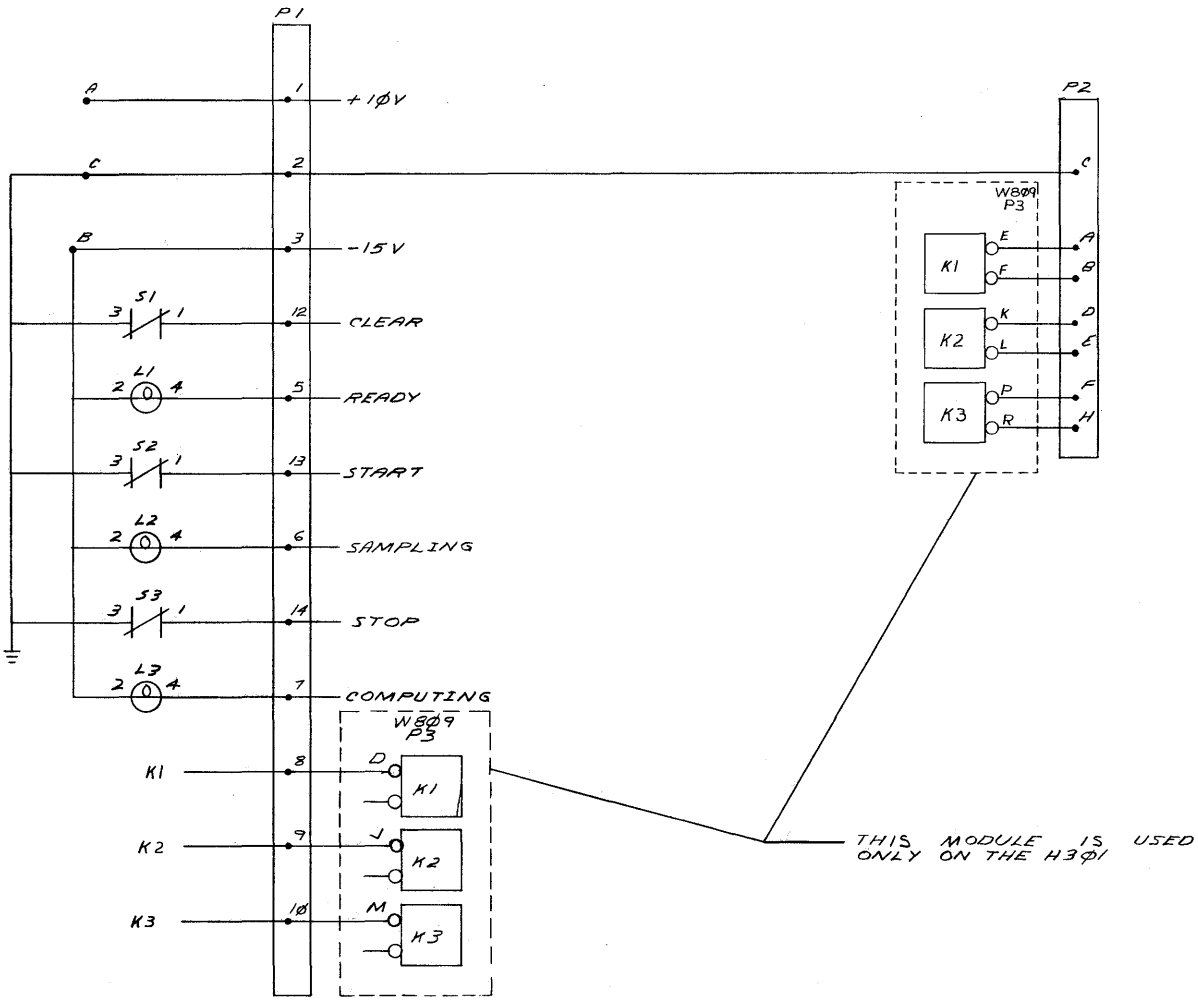


Figure 6-30 D-BS-H300-0-2 H301 Cable Connector Diagram

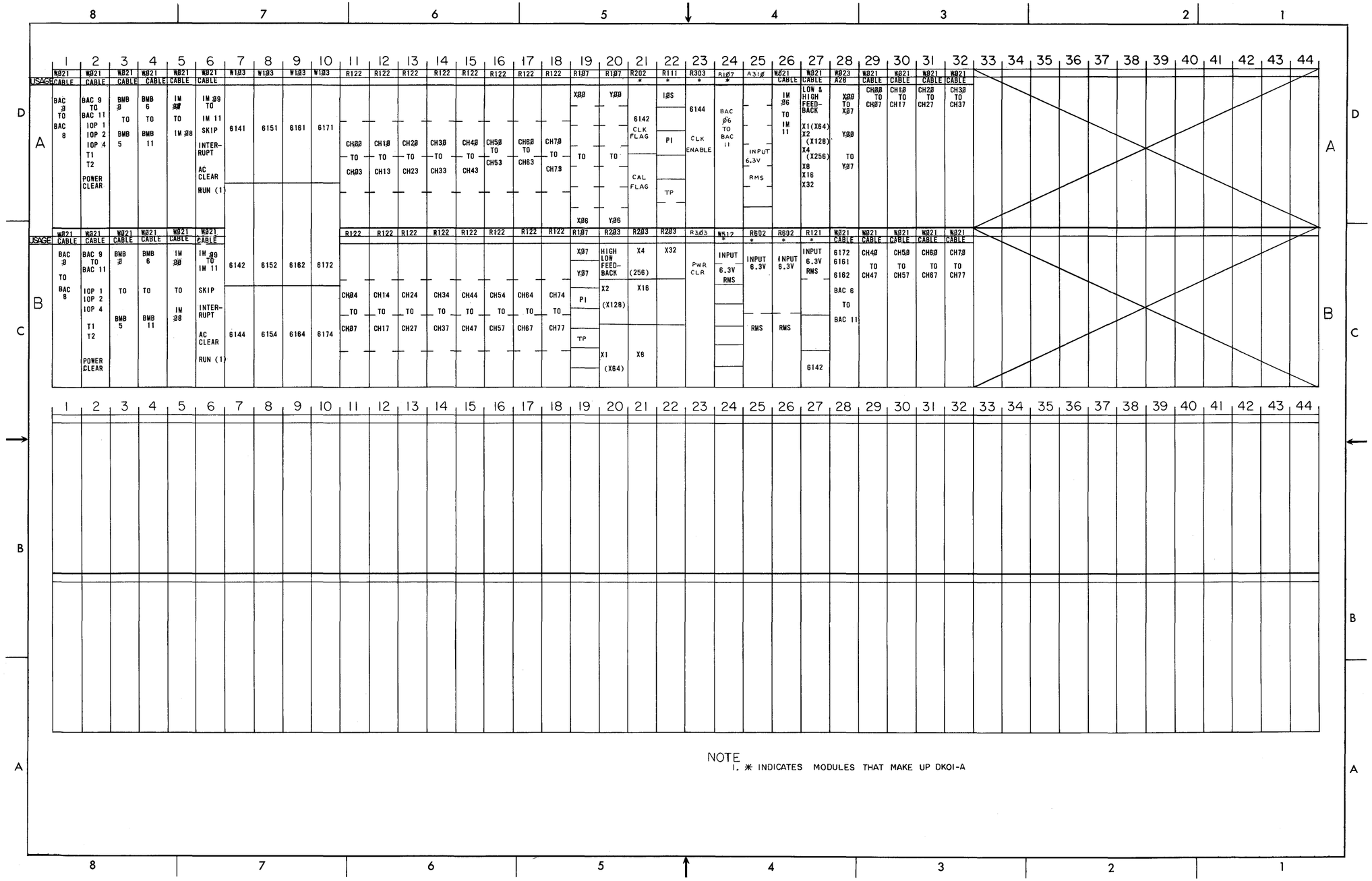


Figure 6-31 D-MU-AF16-0-8 AF16 Module Utilization Diagram

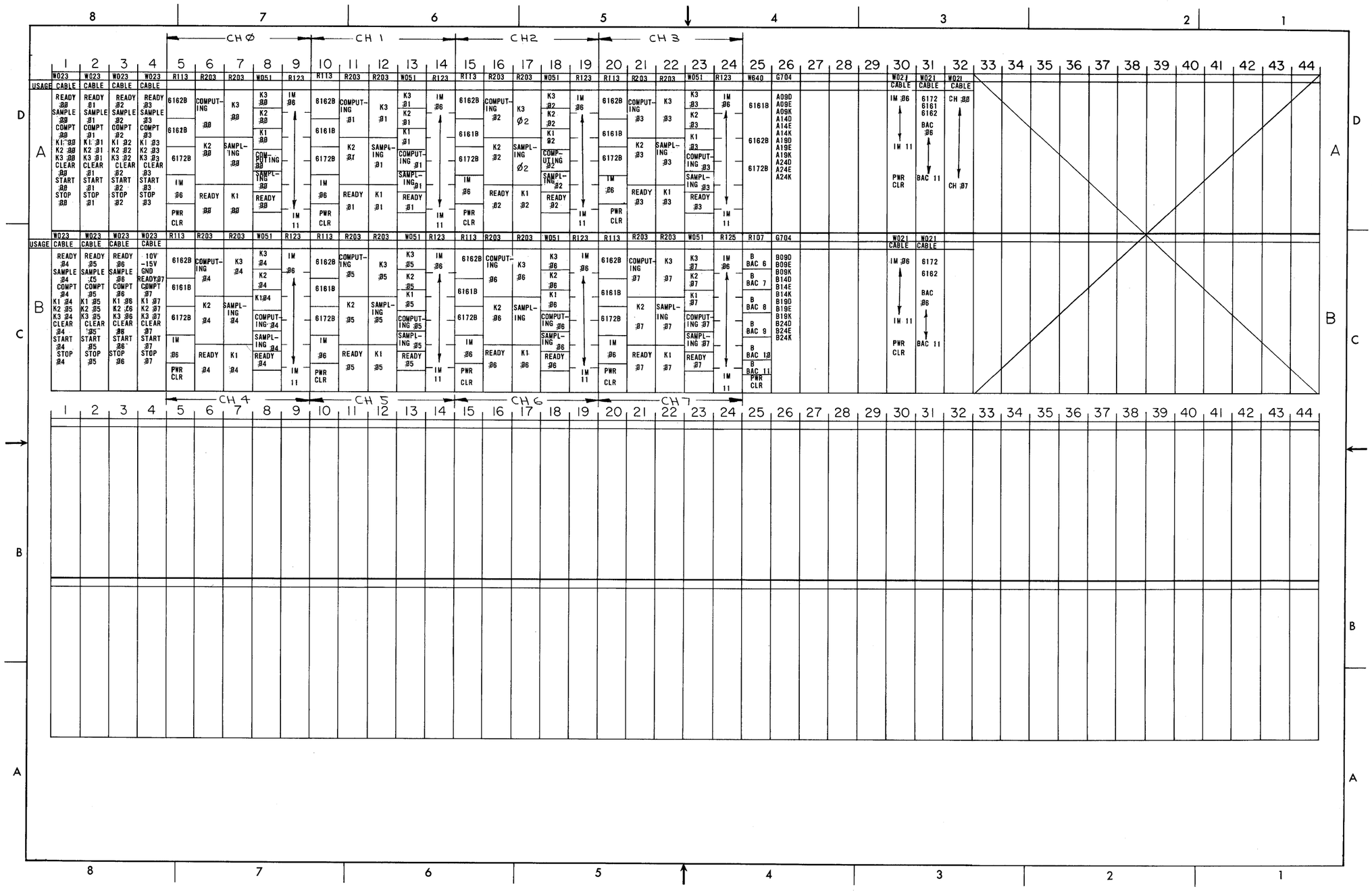


Figure 6-32 D-MU-AF17-0-6 AF17 Module Utilization Diagram

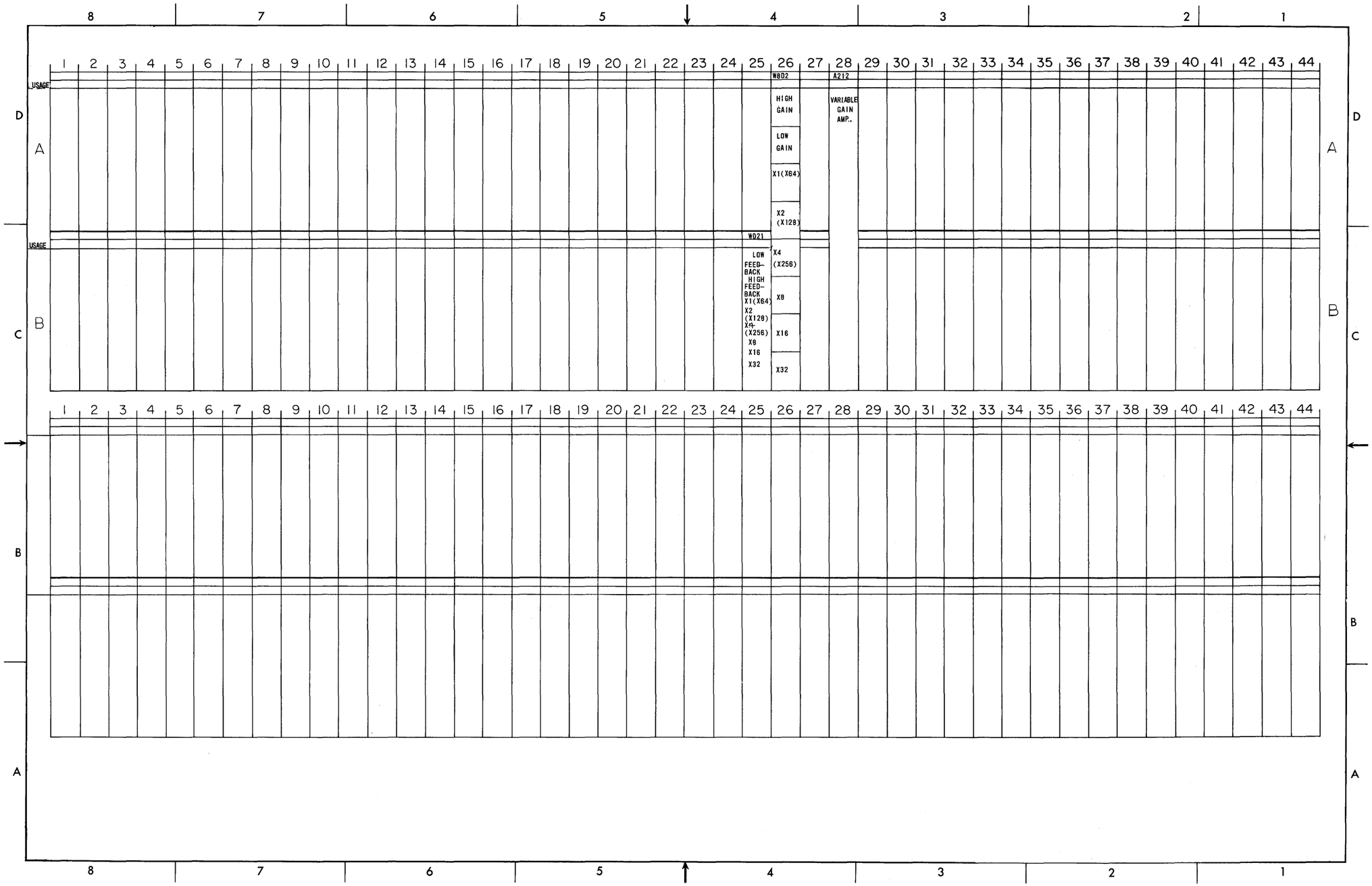
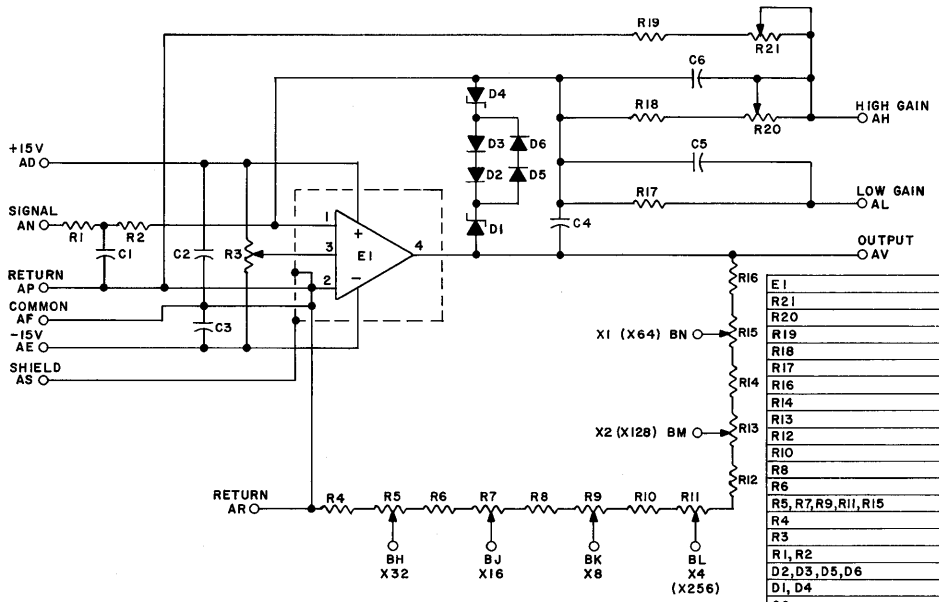


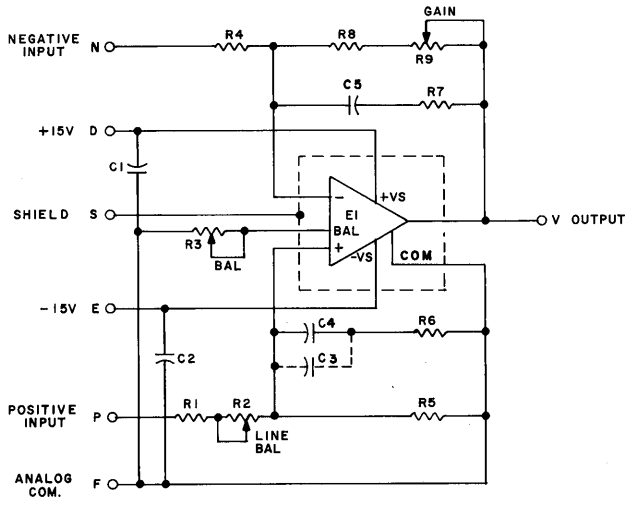
Figure 6-33 D-MU-AG04-0-3 AG04 Module Utilization Diagram



E1	B.B. AMPLIFIER 1538/A	1909304
R21	RES. 200 POT 275P	1305634
R20	RES. 5K POT 275P	1305451
R19	RES. 1.69K 1/8W .1%	1309297
R18	RES. 113K 1/8W .1%	1309296
R17	RES. 1.8K 1/8W .1%	1309295
R16	RES. 105 1/8W .1%	1309294
R14	RES. 866 1/8W .1%	1309293
R13	RES. 50 POT 76PR	1309143-03
R12	RES. 768 1/8W .1%	1309292
R10	RES. 392 1/8W .1%	1309291
R8	RES. 154 1/8W .1%	1309290
R6	RES. 63.4 1/8W .1%	1309289
R5,R7,R9,R11,R15	RES. 20 POT 76PR	1309143-02
R4	RES. 64.9 1/8W .1%	1309288
R3	RES. 100K POT 76PR	1309143-14
R1,R2	RES. 1K 1/8W .1% 25MFP	1304865
D2,D3,D5,D6	DIODE D662	1100113
D1,D4	DIODE IN758	1103116
C6	CAP. 330MMF 100V 5% D.M.	1000023
C5	CAP. .1MFD 100V 20% DISC	1000030
C4	CAP. 33MMF 100V 5% D.M.	1000009
C1,C2,C3	CAP. .01MFD 100V 20% DISC	1001610
	PARTS LIST	A-PL-A212-0-0
REFERENCE DESIGNATION	DESCRIPTION	PART NO.

PARTS LIST

Figure 6-34 B-CS-A212-0-1 A212 Variable Gain Amplifier Circuit Schematic

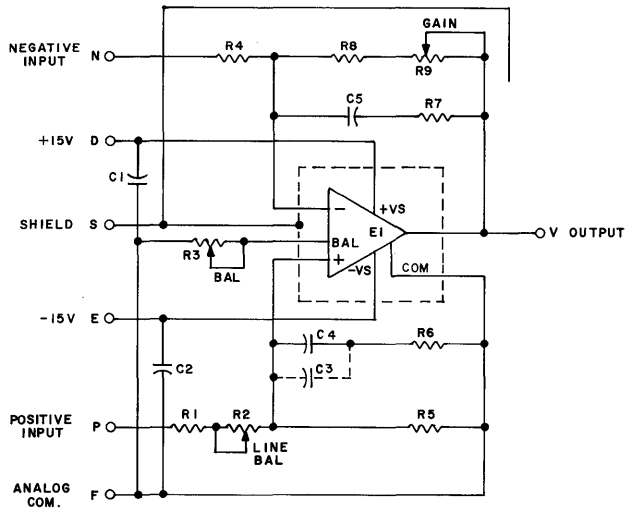


NOTE:
C3 IS TO BE INSTALLED
BY CUSTOMER

E1	AMPLIFIER A301	1909214-00
R9	RES. 10K POT 271	1309311
R6,R7	RES. 10K 1/8W .1% 25MF	1305431
R4,R5	RES. 1MEG 1/8W .1% 25MF	1309299
R3	RES. 1K POT 271	1305391
R2	RES. 10K POT 78PR	1305326
R1,R8	RES. 995K 1/8W .1% 25MF	1309298
C4,C5	CAP. .047MFD 100V 1.0% MYLAR	1009300
C1,C2	CAP. .01MFD 100V 20% DISC	1001610
	PARTS LIST	A-PL-A210-0-0
REFERENCE DESIGNATION	DESCRIPTION	PART NO.

PARTS LIST

Figure 6-35 B-CS-A210-0-1 A210 Input Amplifier Circuit Schematic Program

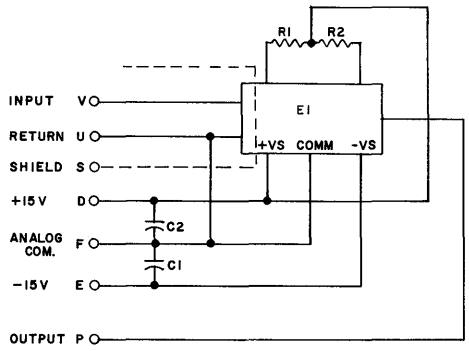


NOTE:
C3 IS TO BE INSTALLED AT FACTORY

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-A211-0-0
E1	AMPLIFIER A301	1909214-00
R9	RES. 50K POT 271	1309287
R8	RES. 9.975MEG 1/8W .1% 25MF	1309309
R6,R7	RES. 10K 1/8W .1% 25MF	1305431
R5	RES. 10MEG 1/8W .1% 25MF	1309310
R4	RES. 1MEG 1/8W .1% 25MF	1309299
R3	RES. 1K POT 271	1305391
R2	RES. 10K POT 78PR	1305326
R1	RES. 995K 1/8W .1% 25MF	1309298
C4,C5	CAP. .0047MFD 1%	1009312
C1,C2	CAP. .01MFD 100V 20% DISC	1001610

PARTS LIST

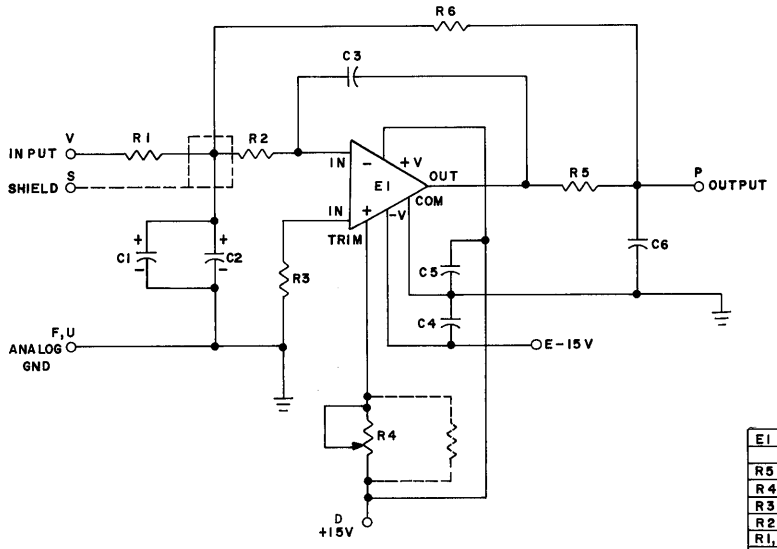
Figure 6-36 B-CS-A211-0-1 A211 Times Ten Input Amplifier Circuit Schematic Diagram



REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-A213-0-0
E1	FILTER #5340	1909215
R1, R2	RES. 128K 1/8W .1% MF	1305516
C1, C2	CAP. .01MFD 100V 20% DISC	1001610

PARTS LIST

Figure 6-37 B-CS-A213-0-1 A213 Low Pass Filter Block Schematic Diagram

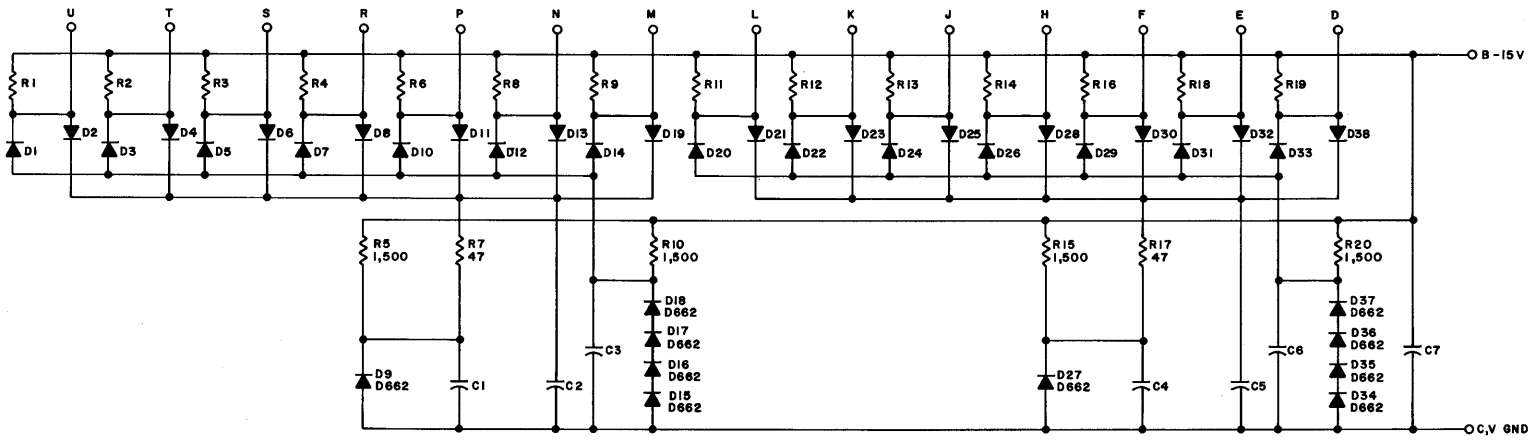


NOTE
DOTTED RESISTOR IS OPTIONAL
1/8 W 1%

E1	OPERATIONAL AMPLIFIER 183J	
R5	RES. 100 1/4W 5% CC	1300229
R4	RES. 100 K HELITRIM POT76 PR	1309143-14
R3	RES. 15 K 1/4W 5% CC	1300496
R2	RES. 8.2 K 1/4W 5% CC	1303179
R1, R6	RES. 16 K .30W .01% 5 MF	1305513
C6	CAP. .47MFD100V 10% MYLAR	1000040
C4,C5	CAP. .01 MFD 100V 20% DISC	1001610
C3	CAP. 4 MFD 50V 10% MYLAR	1009324
C2	CAP. 6.8MFD 35V 10%	1005306
C1	CAP. 10 MFD 35V 20% STANT	1000069
	PARTS LIST	A-PL-A216-0-0
REFERENCE DESIGNATION	DESCRIPTION	PART NO

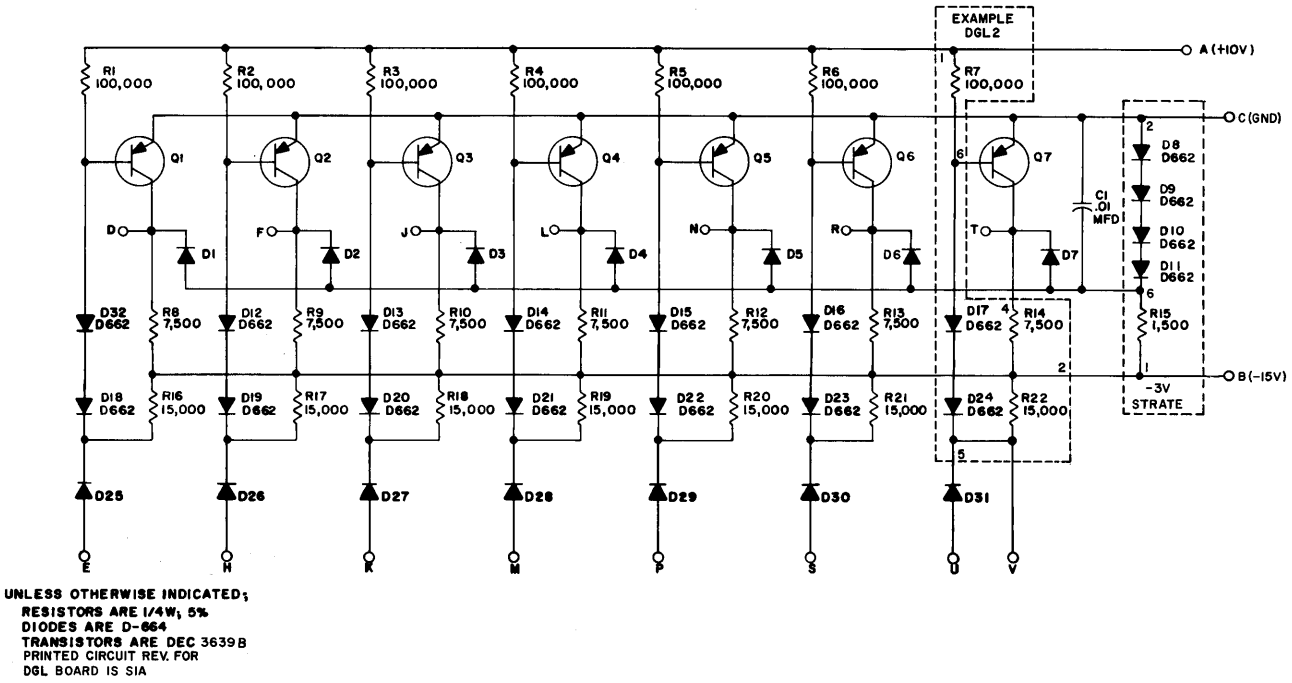
PARTS LIST

Figure 6-38 B-CS-A216-0-1 A216 Low Pass Filter Block Schematic Diagram



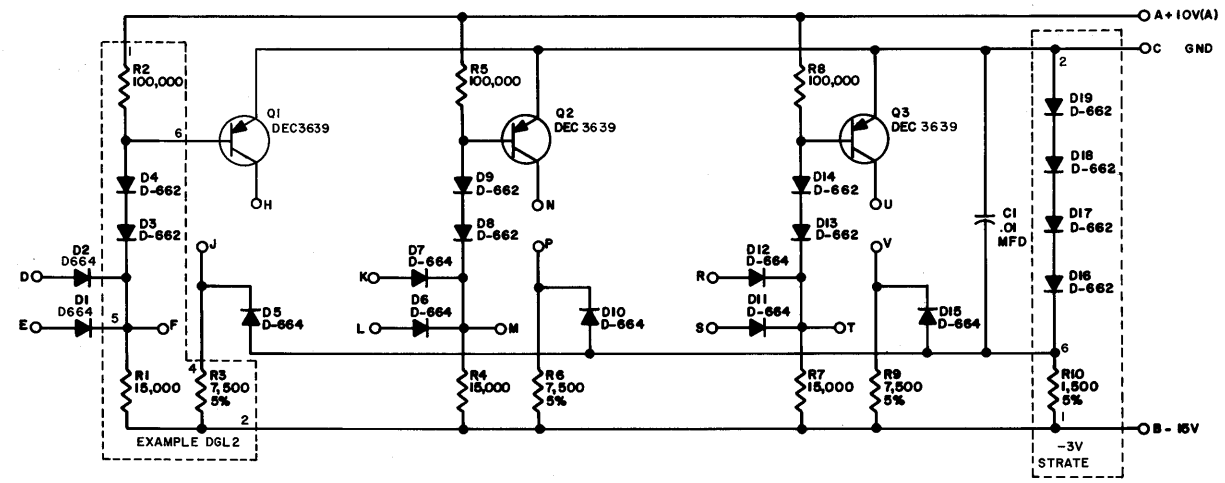
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 5%
RESISTORS ARE 7,500
CAPACITORS ARE .01 MFD
DIODES ARE D664

Figure 6-39 C-CS-G704-0-1 G704 MA Level Termination Block Schematic Diagram



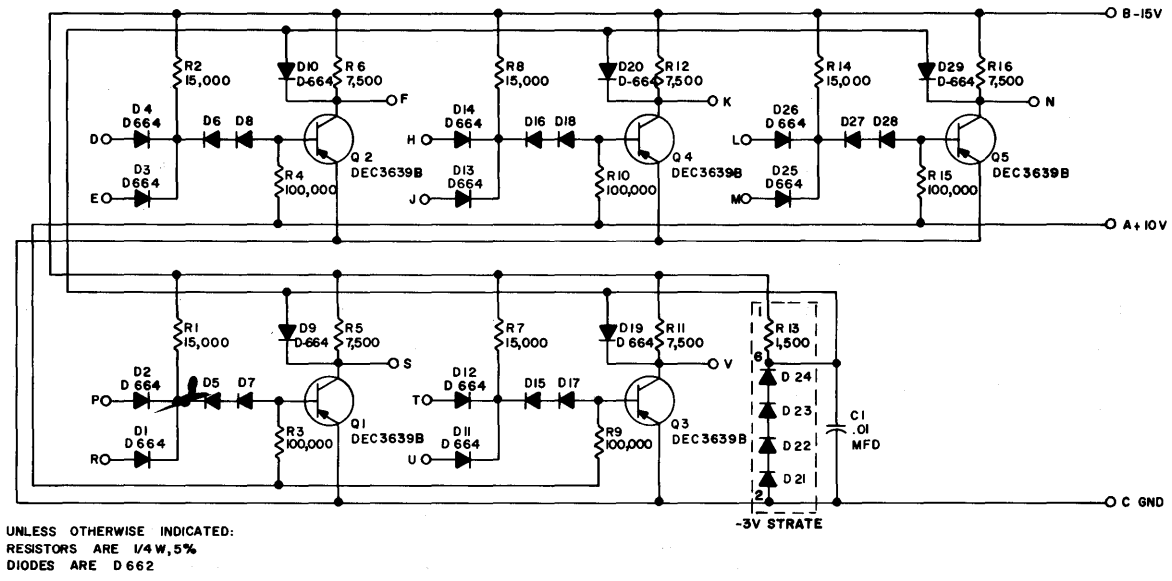
UNLESS OTHERWISE INDICATED;
RESISTORS ARE 1/4W; 5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639B
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIA

Figure 6-40 B-CS-R107-0-1 R107 Inverter Block Schematic Diagram



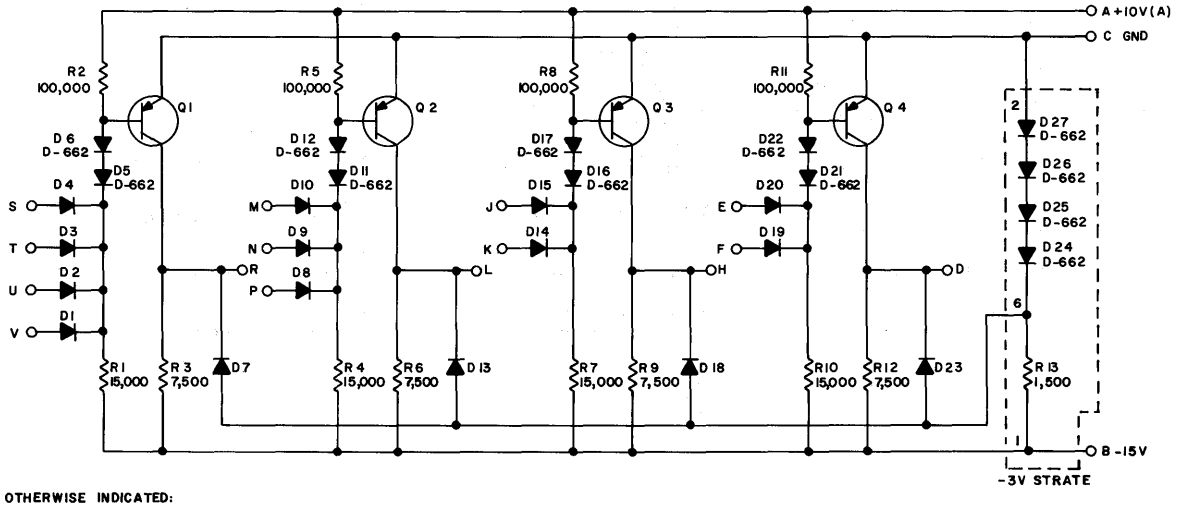
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIB

Figure 6-41 B-CS-R111-0-1 R111 Diode Gate Block Schematic Diagram



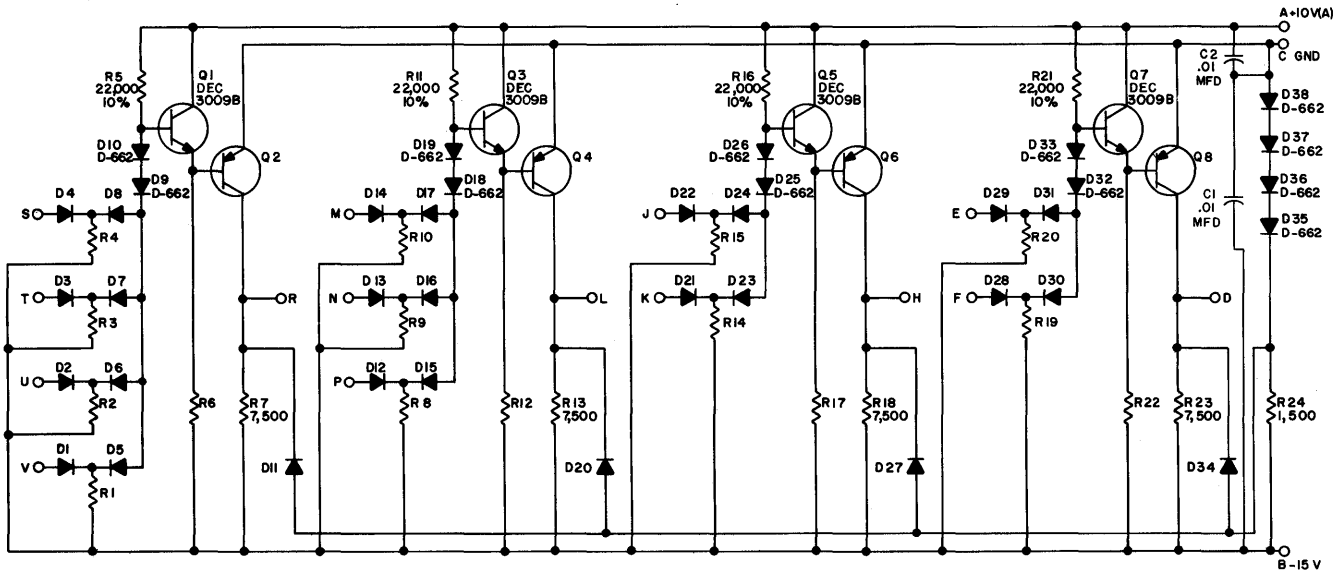
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 5%
DIODES ARE D 662

Figure 6-42 B-CS-R113-0-1 R113 Diode Gate Block Schematic Diagram



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639B
DIODES ARE D-664
RESISTORS ARE 1/4 W, 5%

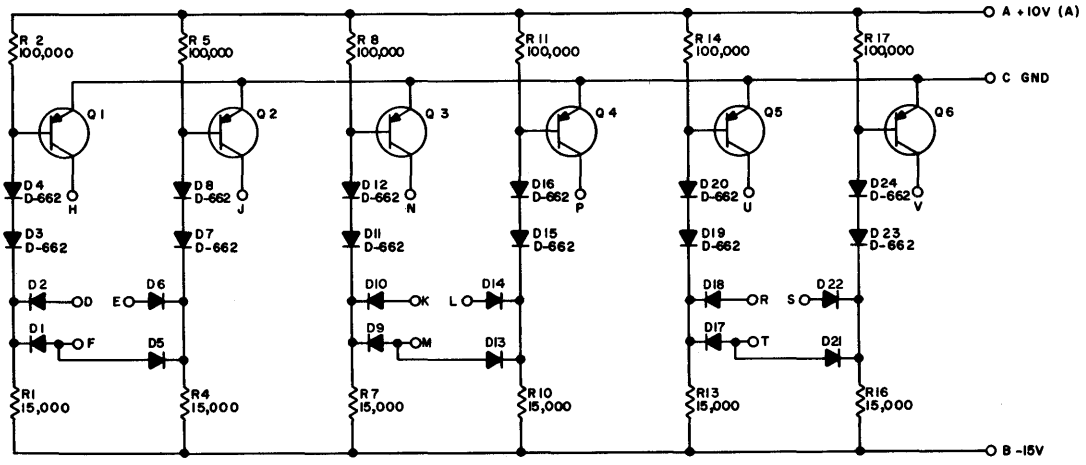
Figure 6-43 B-CS-R121-0-1 R121 NAND/NOR Gate Block Schematic Diagram



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 15,000; 1/4W; 5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639B

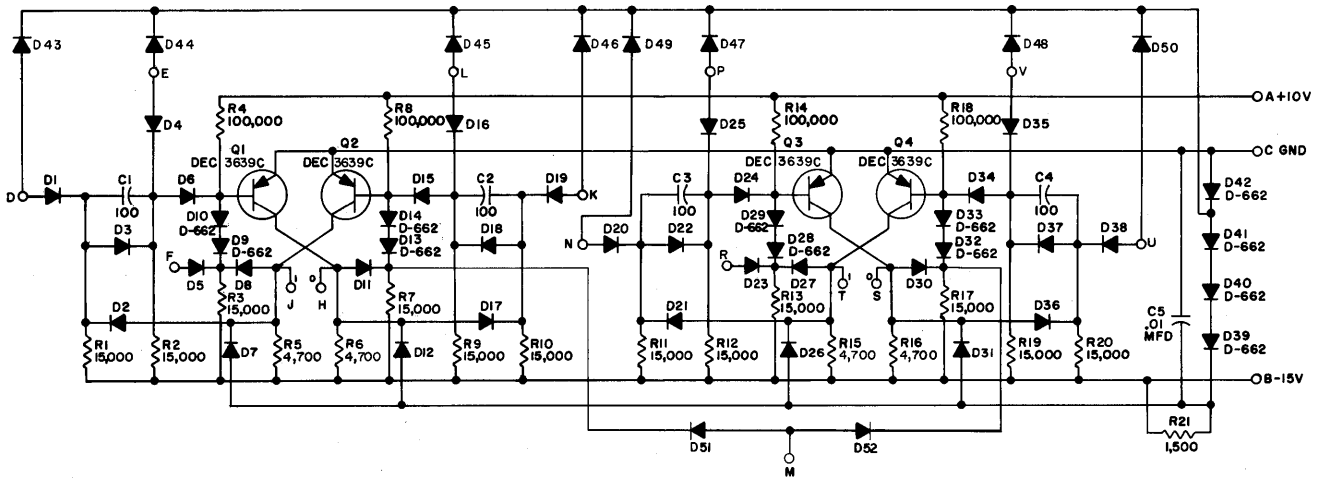
PARTS LIST A-PL-R122

Figure 6-44 B-CS-R122-0-1 R122 NOR Gate Block Schematic Diagram



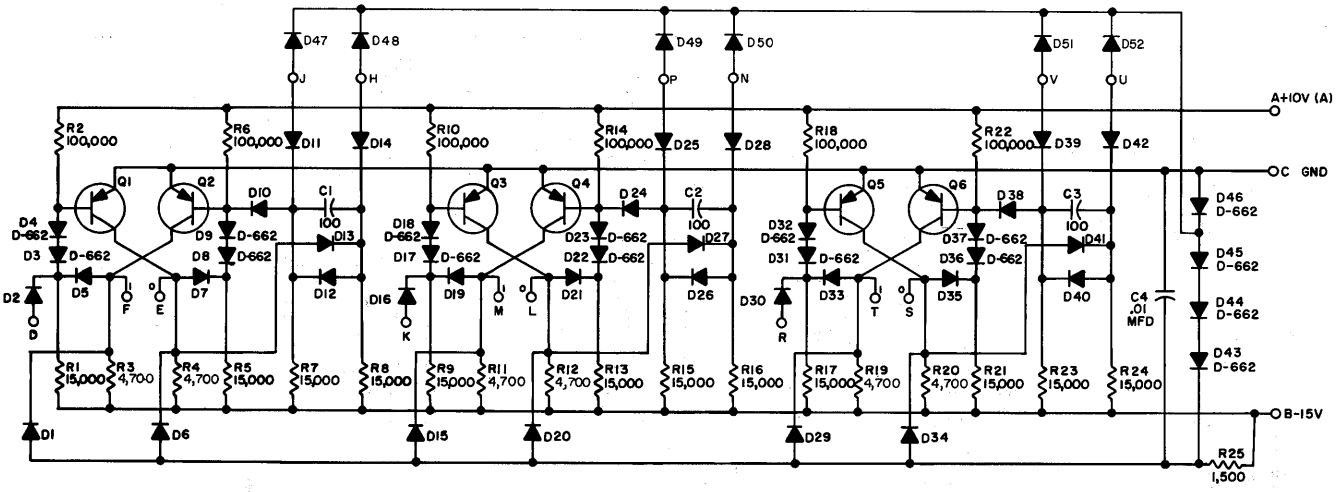
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4 W, 5%
DIODES ARE D-664

Figure 6-45 B-CS-R123-0-1 R123 Diode Gate Block Schematic Diagram



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

Figure 6-46 B-CS-R202-0-1 R202 Dual Flip-Flop Block Schematic Diagram



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639C

Figure 6-47 B-CS-R203-0-1 R203 Triple Flip-Flop Block Schematic Diagram

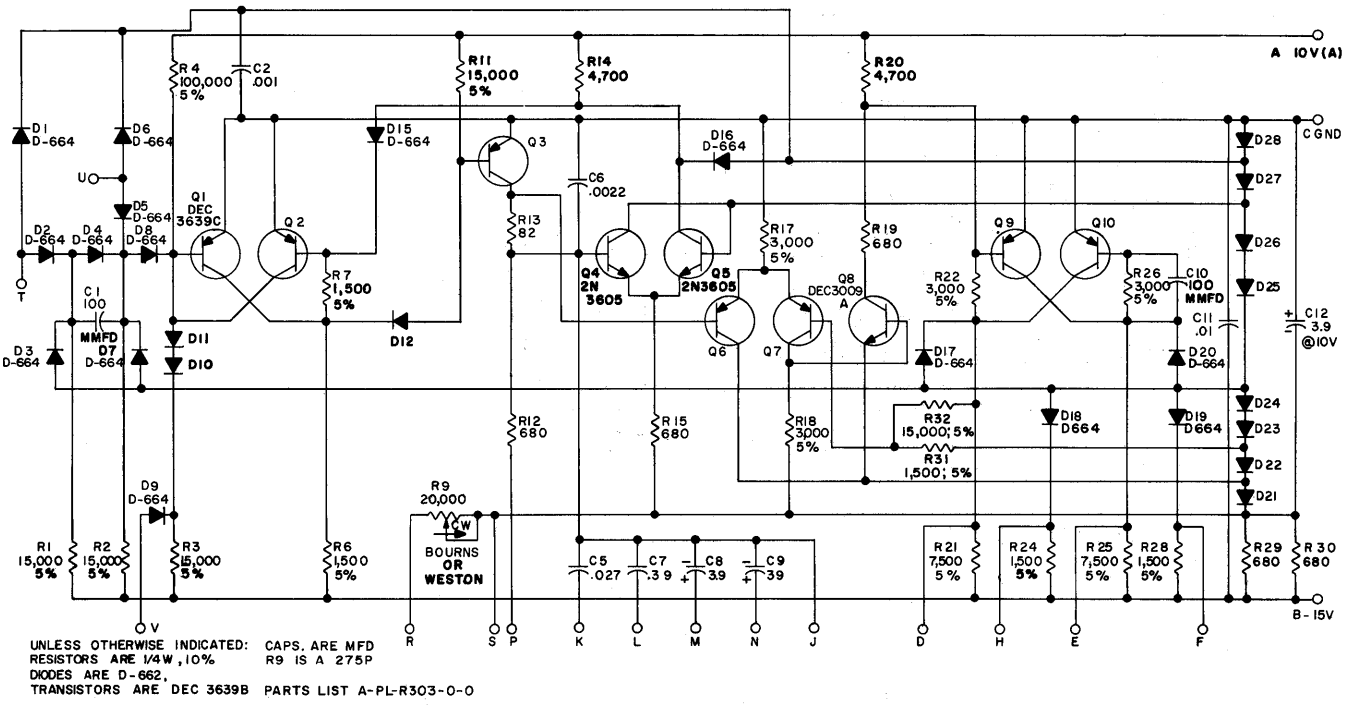


Figure 6-48 B-CS-R303-0-1 R303 Integrating One-Shot Multivibrator Block Schematic Diagram

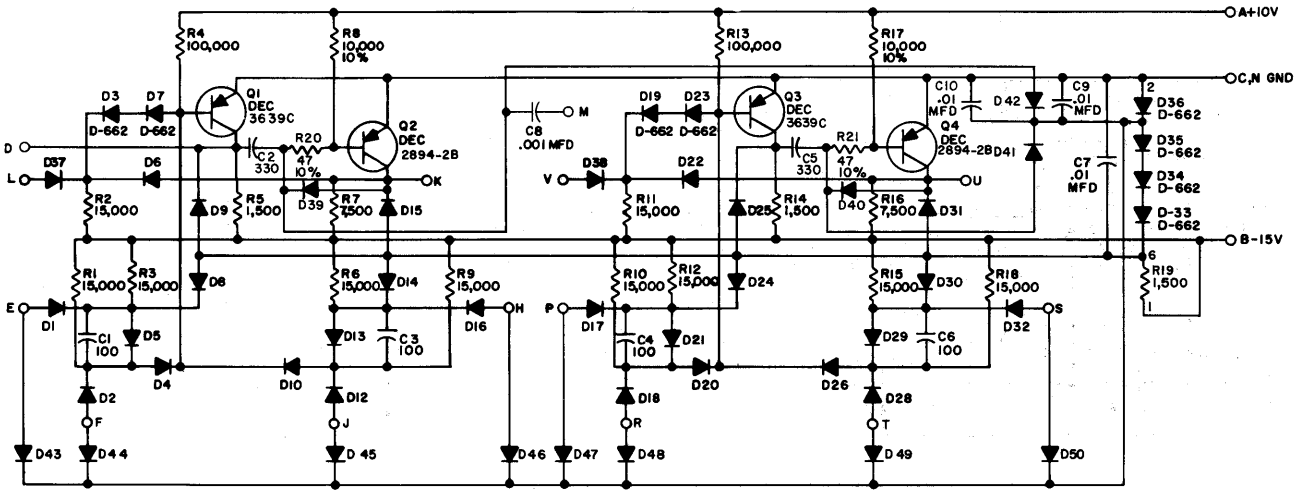
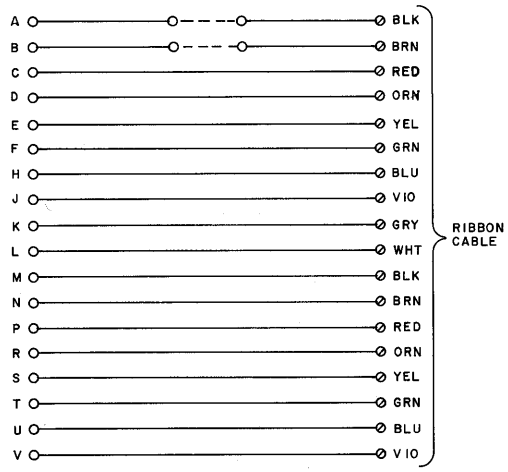
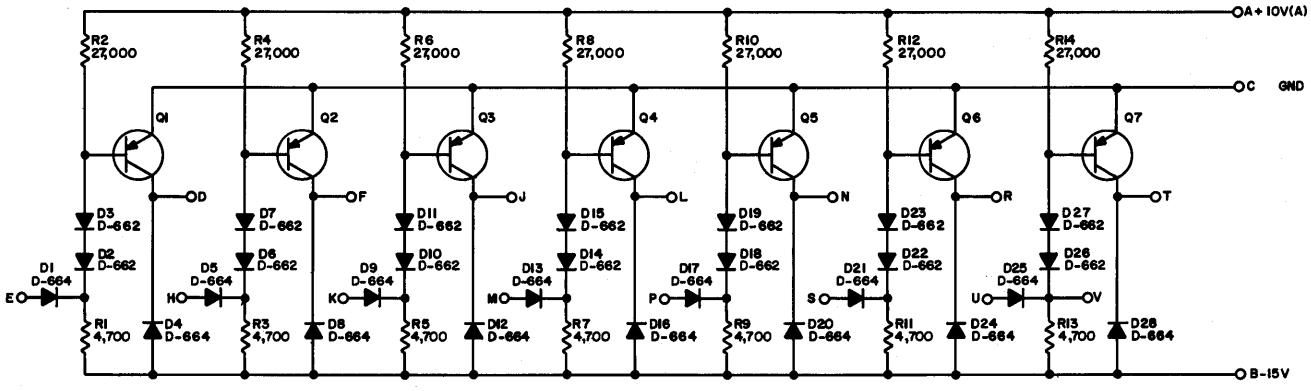


Figure 6-49 B-CS-R602-0-1 R602 Pulse Amplifier Block Schematic Diagram



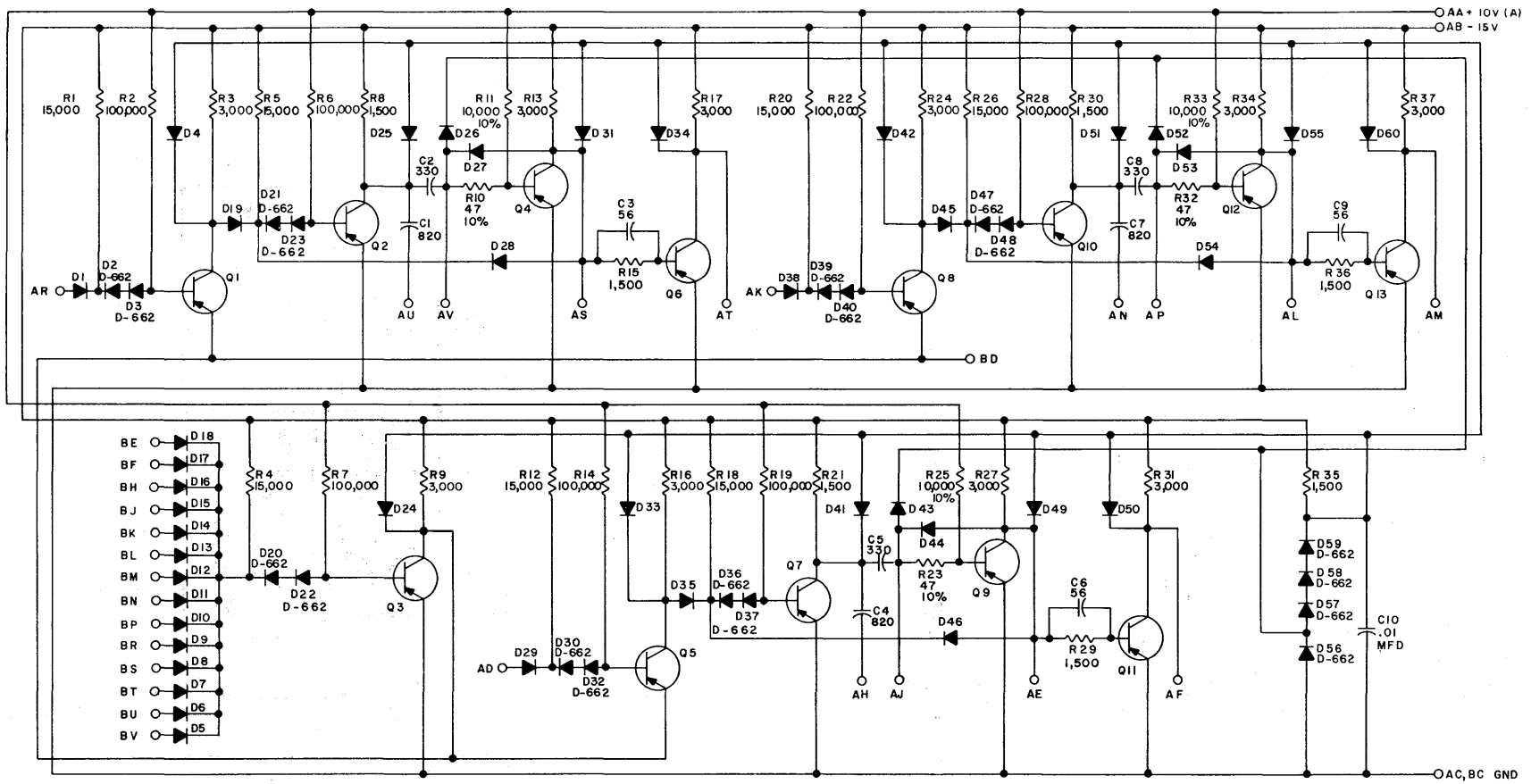
NOTE:
Ø ARE SPLIT LUGS

Figure 6-50 B-CS-W023-0-1 W023 Cable Connector Diagram



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
TRANSISTORS ARE DEC 6534B

Figure 6-51 B-CS-W051 W051 100MA Indicator and Relay Driver Block Schematic Diagram



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4 W, 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

Figure 6-52 C-RS-C-W103-0-1 W103 Device Selector Block Schematic Diagram

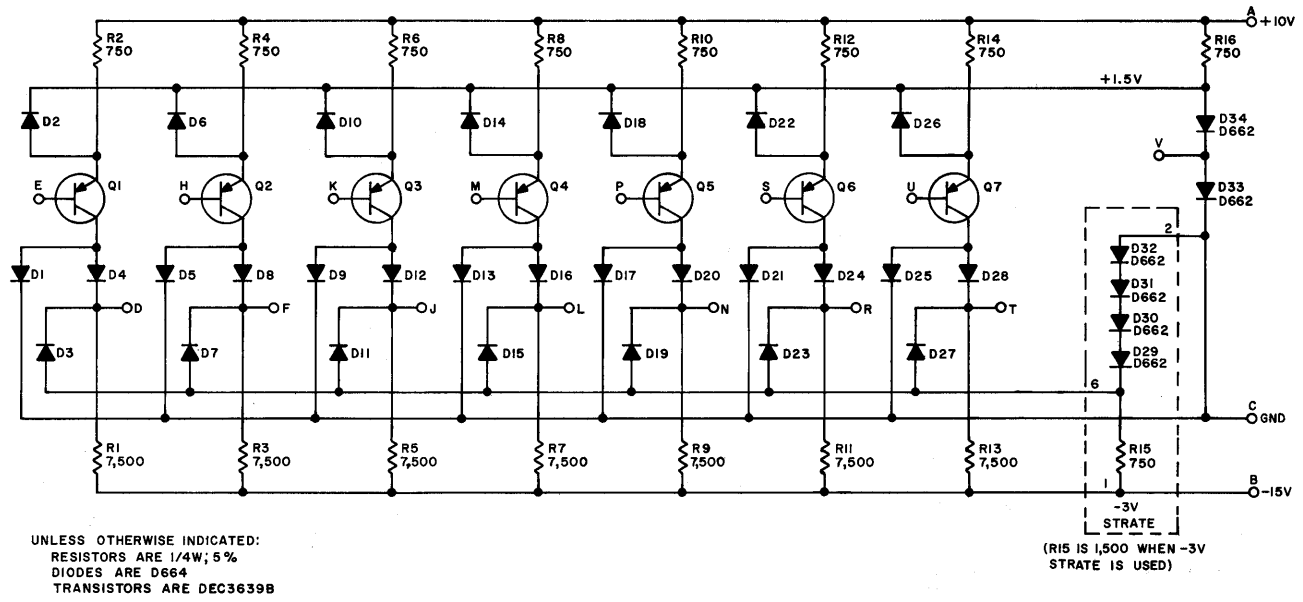


Figure 6-53 B-CS-W512-0-1 W512 Positive Level Converter Block Schematic Diagram

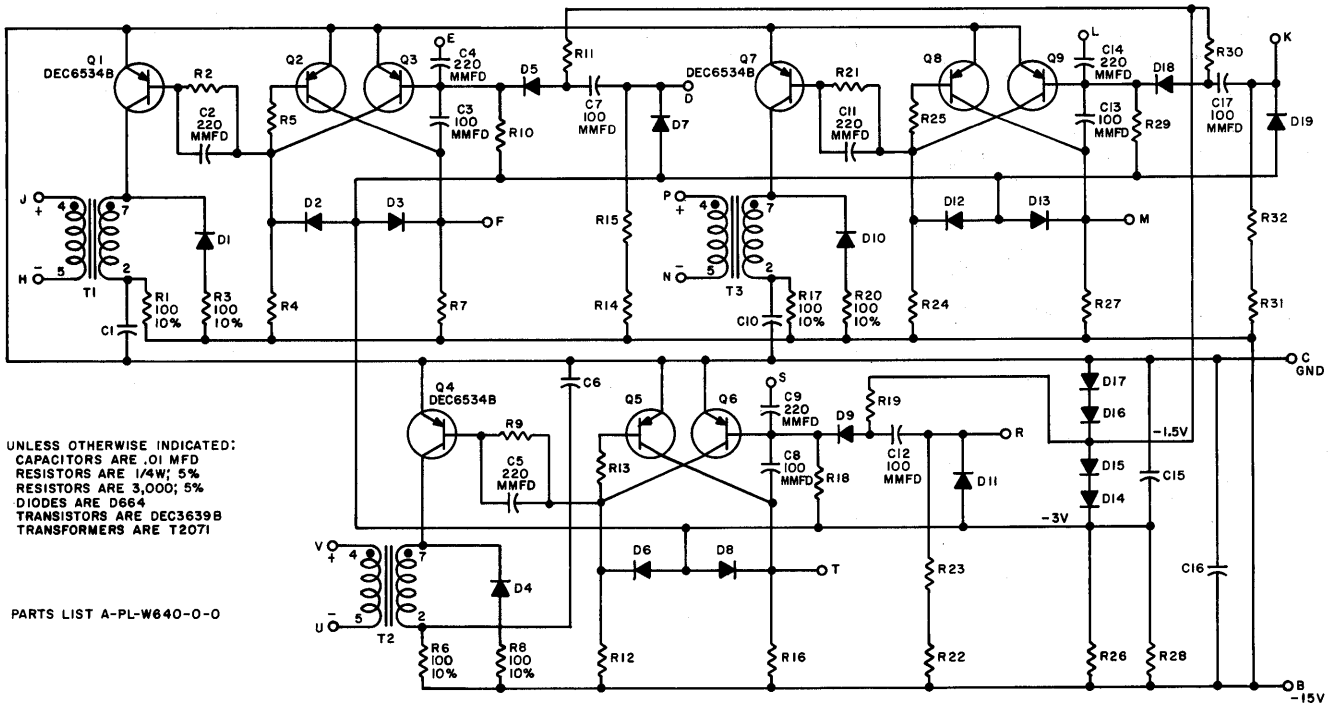
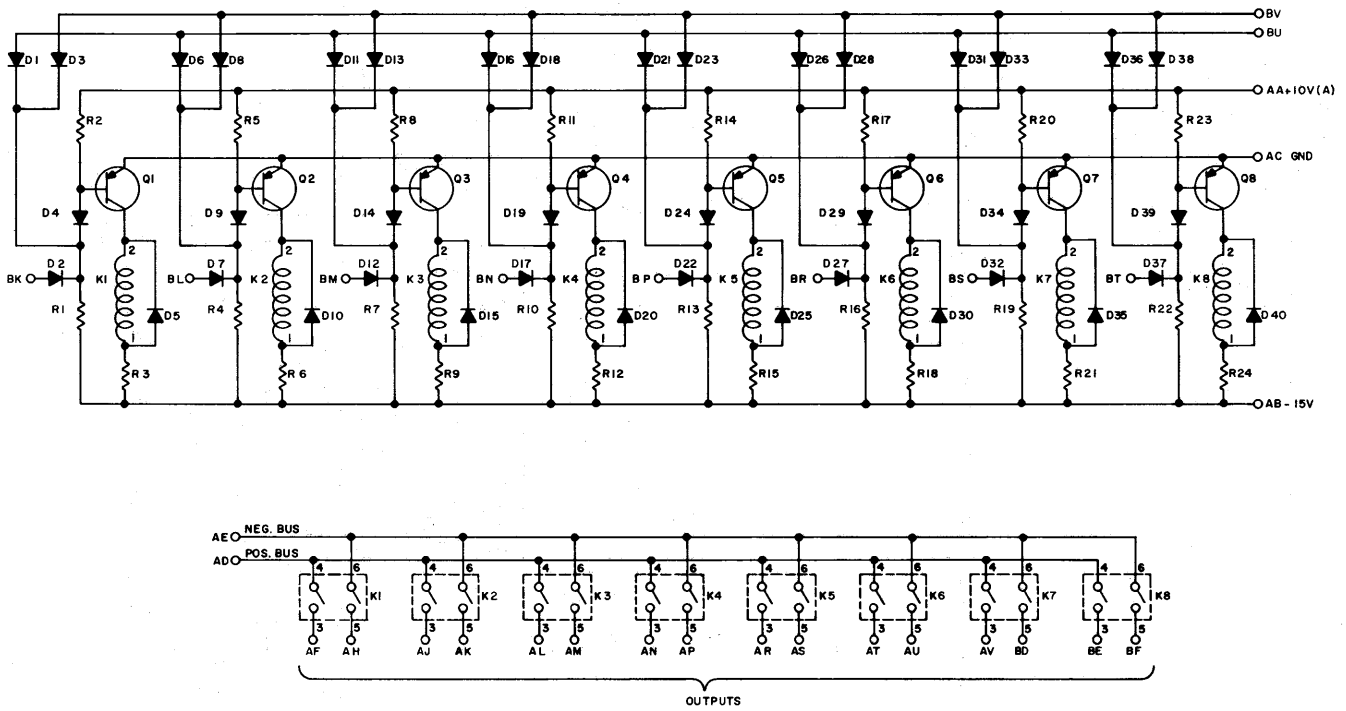


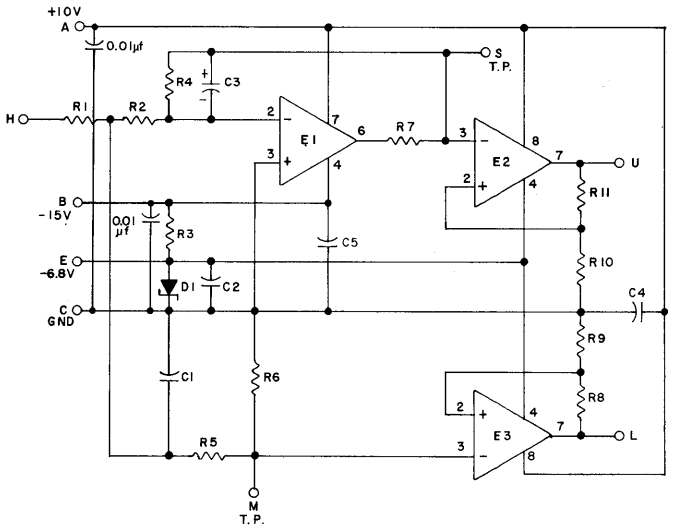
Figure 6-54 B-CS-W640-0-1 W640 Pulse Amplifier Block Schematic Diagram



K1-K8	RELAY, REED 12V-RLR0006	1205296
Q1-Q8	TRANSISTOR DEC6534D	1503409
R3,R6,R9,R12,R15,R18,R21,R24	RES. 120 1/4W 5% CC	1300247
R2,R5,R8,R11,R14,R17,R20,R23	RES. 68K 1/4W 10% CC	1300526
R1,R4,R7,R10,R13,R16,R19,R22	RES. 15K 1/4W 10% CC	1300494
D4,D9,D14,D19,D24,D29,D34,D39	DIODE D668	1102161
D35-D38,D40 D20-D23,D25-D28,D30-D33, D1-D3,D5-D8,D10-D13,D15-D18,	DIODE D664	1100114
	PARTS LIST	A-PL-W802-0-0
REFERENCE DESIGNATION	DESCRIPTION	PART NO.

PARTS LIST

Figure 6-55 C-CS-W802-0-1 W802 Relay Multiplexer Block Schematic Diagram



NOTE:
PIN 1 ON E2 & E3 = GND

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	
E2,E3	AMPLIFIER µA710	1905620
E1	AMPLIFIER µA741-C	1909234
R9,R10	RES. 100 1/4W 5% CC	1300229
R7	RES. 47 1/4W 5% CC	1300202
R6	RES. 2.2K 1/4W 5% CC	1300417
R5	RES. 4.7K 1/4W 5% CC	1300447
R4	RES. 133K 1/8W 1% 100MFP	1305130
R3	RES. 470 1/4W 10% CC	1300317
R2	RES. 10K 1/8W 1% 100MFP	1303312
R1,R8,R11	RES. 1K 1/4W 5% CC	1300365
D1	DIODE 1/4M 6.8 AZ5	1100102
C3	CAP. 1.0MFD 35V 10% S.TANT	1001776
C2,C4,C5	CAP. .01MFD 100V 20% DISC	1001610
C1	CAP. .1MFD 100V 20% DISC	1000030
	PARTS LIST	A-PL-A310-0-0

PARTS LIST

Figure 6-56 B-CS-A310-0-1 A310 Four Times Line Frequency Clock Circuit Schematic Diagram

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