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CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

This chapter identifies and describes the modular parts of the XVM System hardware and shows how they are incorporated into the system. Figure 1-1 shows the physical location of these parts in the XVM System configuration. Figure 1-2 is a block diagram of the interconnection of the elements of the system which are covered by this manual. Other options are described in separate manuals.

1.2 SYSTEM DESCRIPTION

The XVM System consists of a KP15-C Central Processor, KD15 I/O Processor, KC15 Console, ME15 and/or MF15 Memory, associated cabinets, hardware, power supplies, and any of a large number of options.

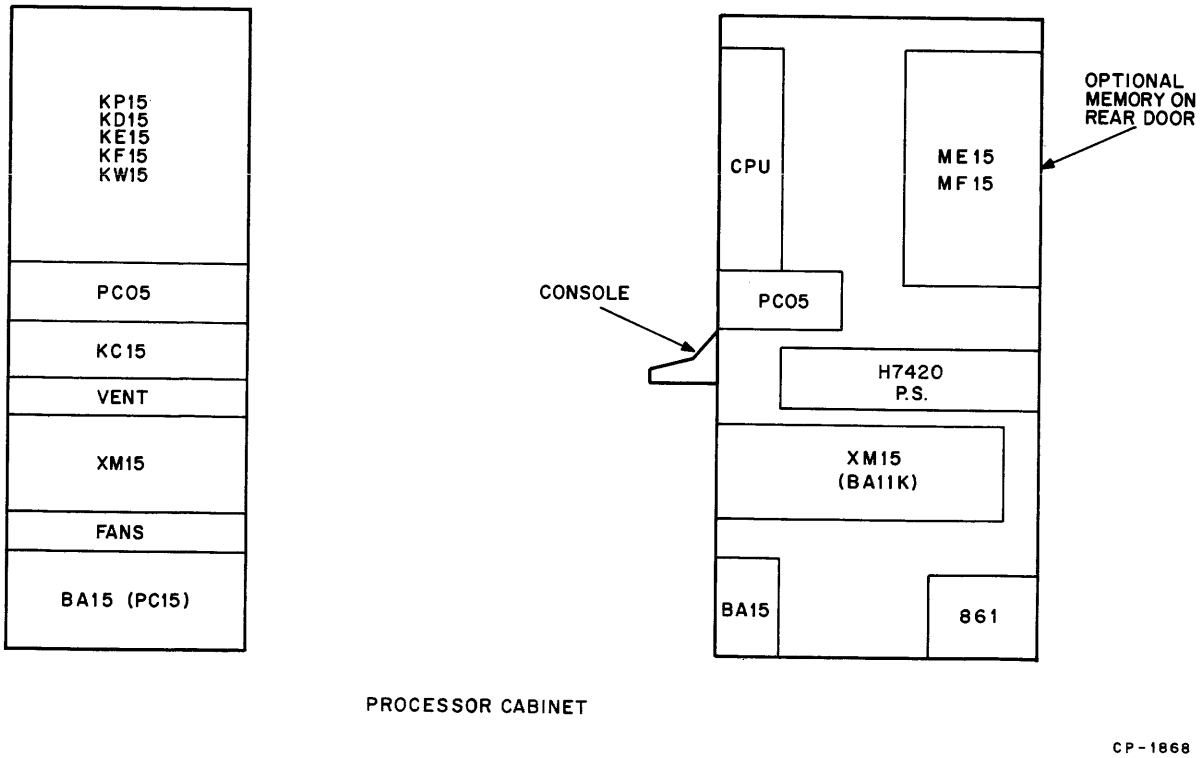

Figure 1-1 XVM Configuration Diagram

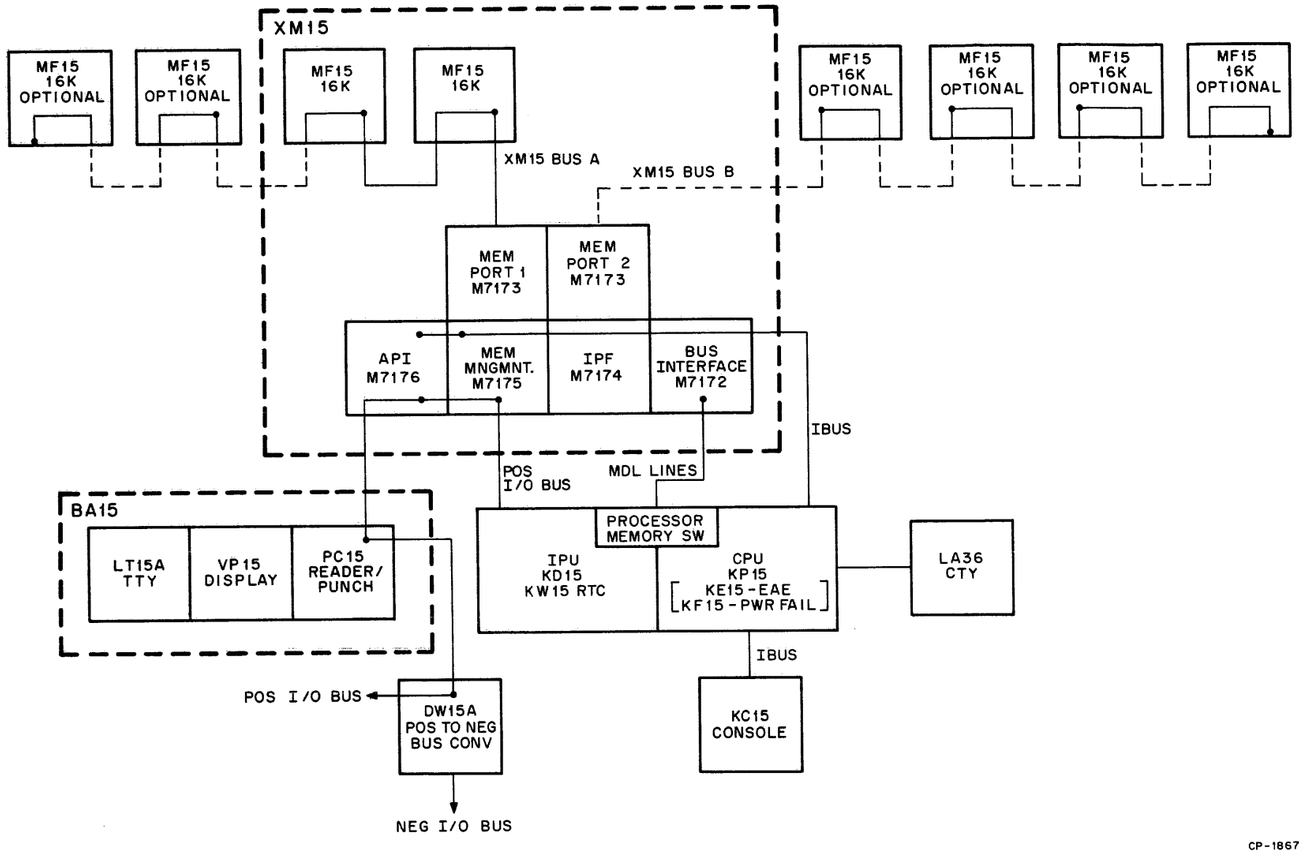

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Figure 1-2 XVM System Block Diagram

Hardware configurations, for which special software systems have been developed, are designated as follows:

a. XV100 System – consists of one KP15-C Central Processor, one XM15-UJ/UK Memory Processor with 32K of MF15 core memory, one LA36 CA/CB DECwriterII keyboard-printer, one PC15/A Paper Tape reader-punch, one KC15-C Console, one BA15 Expander, one H7420 A/B Power Supply, one H740-D Power Supply, two H744 Regulators, and one PDP15-C Power Harness. All system components are housed in one cabinet. MF15 core memory options are available to expand the basic XV100 System to include up to 128K of memory. Additionally, XV100-AA is available for 115 V, 60 Hz operation; the AB version is for 230 V, 50 Hz. Figure 1-3 illustrates a typical XV100 System.

b. XV200 System – consists of the XV100 System and an RK15-JE/JF Unichannel System with a PDP-11/10 peripheral processor containing 8K of MM11 core memory. All XV200 System components are housed in two cabinets. The XV200 memory can be expanded up to 128K with the optional MF15 core memory units. XV200-AA is for 115 V, 60 Hz operation; XV200-AB is for 230 V, 50 Hz. Figure 1-4 illustrates the typical XV200 System.

c. XM15 – The XM15-BA/BB contains the Memory Management logic (no peripherals) of the XV100 System and is designed as an add-on unit to update an existing PDP-15 system. XM15-BA/BB is the basic unit and has no memory. Options are available which add MF15 core memory units in 32K increments up to 128K. The XM15-BA/BB is housed in an H950 cabinet as illustrated in Figure 1-5.

1.3 CENTRAL PROCESSOR

1.3.1 KP15-C Central Processor

The KP15-C Central Processor functions as the main component of the computer by carrying on bidirectional communication with both the memory and the I/O Processor. Provided with the capability to perform all required arithmetic and logical operations, the central processor controls and executes stored programs. It accomplishes this with an extensive complement of registers, control lines, and logic.

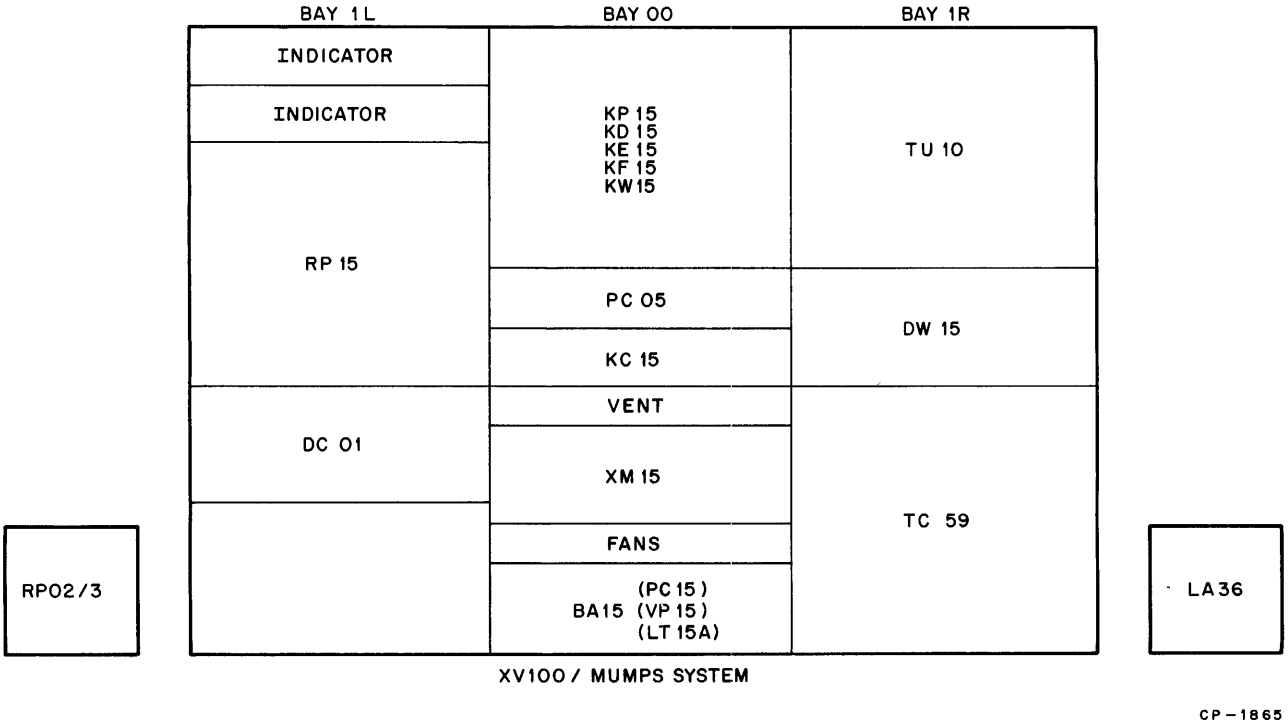

Figure 1-3 XV100 System Configuration Diagram

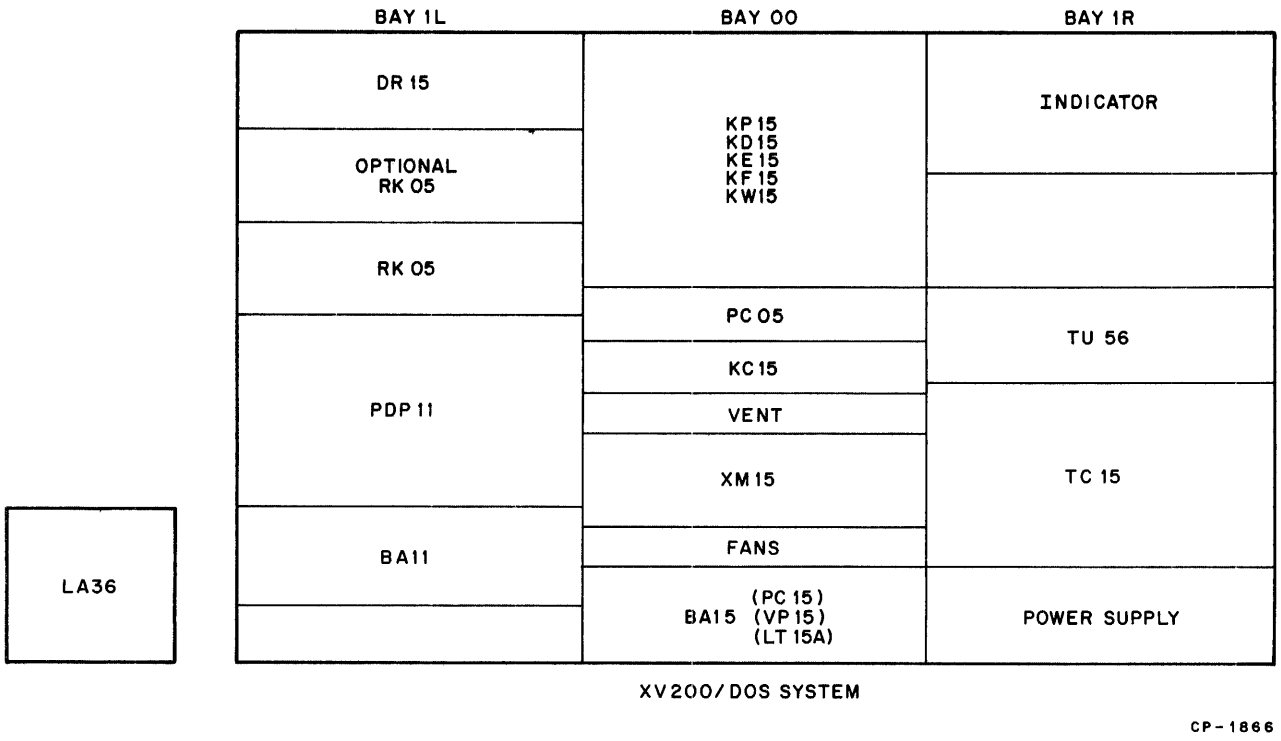

Figure 1-4 XV200 System Configuration Diagram

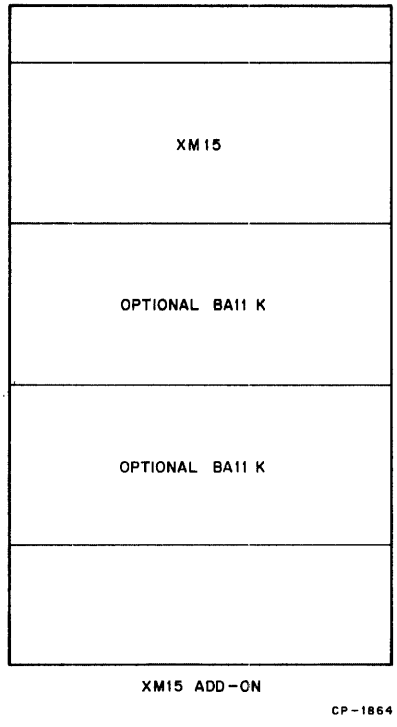

Figure 1-5 XM15 Field Conversion Configuration Diagram

1.3.2 Terminal Control

The Terminal Control provides the control for the console terminal, normally an LA36 DECwriter. Logic is provided for the hardware read in of tapes from a Teletype® reader in systems without high-speed tape facilities. Characters may be read from the keyboard in either half-duplex mode (characters echoed onto the printer) or full-duplex mode.

1.3.3 KC15-C Console

The KC15-C Control Console provides facilities for operator initiation of programs, monitoring of central processor (CPU) and I/O Processor (IPU) registers, starting program execution and the manual examination and modification of memory contents.

1.3.4 KE15-C Extended Arithmetic Element

The KE15-C Extended Arithmetic Element (EAE) facilitates high-speed arithmetic operations and register manipulations. The EAE adds an 18-bit Multiplier Quotient (MQ) register to the system, as well as a 6-bit Step Counter (SC) register. Worst case multiplication time is 7.4 μs; division time is 7.65 μs.

1.3.5 KF15 Power Fail

The KF15 Power Fail offers maximum protection to programs during power failure and recovery of power after failure. It enables the XVM System to store active registers in memory before power diminishes to a point beyond which data will be lost. The KF15 also enables the XVM, upon restoration of power, to restore these registers and continue with the program that was previously in progress.

1.4 I/O PROCESSOR

1.4.1 KD15-C I/O Processor

The KD15-C Processor (IPU) is an autonomous subsystem of XVM which supervises and synchronizes all IOT and Data Channel (DCH) transfers between the devices and the XVM central processor and memory. The I/O Processor contains the arithmetic and control logic hardware to supervise all I/O device activity. However, the IPU is a passive system in that it responds to requests for activity from devices or from the CPU rather than initiating activity.

1.4.2 KW15 Real-Time Clock

The KW15 Real-Time Clock gives the user a time reference capability. The real-time clock produces clock pulses at a rate of 1 every 16.7 ms for 60 Hz systems; these systems increment core location 07, which can be preset and monitored under program control.

1.5 MEMORY

The XM15 Memory Processor can be equipped with either 32K of MF15 internal core memory or 24K of ME15 internal core memory. Memory units can be added to the XVM System (external to the XM15) to produce a total memory of 128K. Added memory may be either MF15 or ME15, or a mixture of both.

1.5.1 MF15 Memory

The MF15 Memory is the primary storage area for the computer. Memory is organized into banks – each bank is a unit of 16K words. The Central Processor and I/O Processor have provisions to address up to 128K words of core memory. Any word in core memory may be addressed by either the Central Processor, the I/O Processor, the IPF (instruction pre-fetch), or an external processor. The XM15 Memory Processor houses 32K of MF15 core memory. 64K of additional MF15 memory can be accommodated on the rear door of the XVM Central Processor for a total of 96K. Users desiring an additional 32K of memory (for a total of 128K) will require an additional cabinet to house the added memory. Further information on the MF15 core memory can be found in the *MF15-U Core Memory Maintenance Manual, EK-MF15-MM-001.*

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1.5.2 ME15 Memory

The ME15 Core Memory can provide the XVM System with up to 128K of 18-bit words. 24K of ME15 memory can be housed in the XM15 and an additional 48K of ME15 can be placed on the rear door of the Central Processor cabinet. Memory capacity beyond 72K (up to 128K) requires the addition of a separate cabinet to the XVM System to house the added memory units. For additional information on the ME15 Core Memory, refer to the *ME15 Core Memory Maintenance Manual, EK-ME15-MM-001.*

1.6 BA15 PERIPHERAL EXPANDER

The BA15 houses power and I/O bus interface logic for the PC15, LT15-A, and VP15 which are described in Paragraphs 1.6.1 through 1.6.3. Only one BA15 is required per XVM System. The BA15 is located in the Central Processor cabinet, as illustrated in Figure 1-1.

1.6.1 PC15 High-Speed Paper-Tape Reader/Punch

The PC15 includes a PC05 Reader/Punch and the control to interface it to the XVM. Characters can be read from paper tape at a maximum rate of 300 characters per second or punched at a rate of 50 characters per second. When this option is installed, the PC15, instead of the TTY, is used for hardware READIN.

1.6.2 LT15-A Single Teletype Control (Optional)

This option provides the logic to receive and transmit information to and from an ASR33 or KSR35 Teletype, an LA36 DECwriter, or other serial device. The LT15-A provides a second serial terminal capability for the XVM System.

1.6.3 VP15 Display Control (Optional)

This option interfaces the XVM to various display devices by providing the digital-to-analog converters and the control logic for the X and Y positioning, as well as the intensification of the VP15-A Storage Tube Display, VP15-B Oscilloscope Display, or VP15-C X-Y Oscilloscope Display.

1.7 XM15 MEMORY PROCESSOR

The XM15 houses the Memory Management logic for the XVM System. The XM15 contains power, I/O bus interface, memory bus interface, and various control functions for the operation of the M7176 Automatic Priority Interrupt logic, the M7175 Memory Management logic, the M7174 Instruction Prefetch logic, and the M7173 Memory Port. The various XM15 functions are discussed in the following paragraphs.

1.7.1 M7176 Automatic Priority Interrupt (API)

The M7176 API provides eight levels of priority interrupts for the XVM System. Of these eight levels, the upper four are assigned to I/O devices and are initiated by flags (interrupt requests) from the devices. The lower four levels are programming levels and are initiated by software requests. High data rate or critical devices are assigned to high priority levels and can interrupt slower device service routines. The M7176 holds the lower device interrupt request until it can be serviced. The source of the interrupt is also directly identified, eliminating the need for flag search routines.

A self-starting, high resolution (18 bits) task accounting clock is also contained on the M7176. The accounting clock provides essential data that allows accurate appropriation of machine cost among multi-users of the XVM System. A single IOT reads and clears the contents of the task accounting clock register.

1.7.2 M7175 Memory Management

The M7175 provides the XVM System core memory with protect features to trap HALT, IOT, OAS and chained Execute instructions and the addressing of a nonexistent memory bank. A boundary register and two relocation registers, and associated control logic, are used to establish the limits of the user's program and to relocate the program upward in memory from the real machine location.

The boundary register functions in two modes: protect and relocate. In the protect mode, the boundary register sets the lower memory limit for the user's program. In the relocate mode, the boundary register establishes the upper memory limit for the program, while the lower limit is established by the first relocation register. The second relocation register, called the share register, provides for memory segmentation in a multi-user environment.

In addition, there are software-controlled modes which allow:

a. Selection of indirect addressing with 15, 16, or 17 bits
b. Relocation disabling
c. User IOT enabling
d. Write protection of the shared segment
e. Specifying the shared segment length.

1.7.3 M7174 Instruction Prefetch (IPF)

The M7174 IPF provides the XVM System with improved instruction fetch times by prefetching presumed instructions from memory. The IPF does this by monitoring requests to memory and synchronizing itself to the current instruction address. The IPF then attempts to prefetch up to four locations ahead of the processor. Simultaneously, the IPF continues to monitor memory references and, whenever possible, provides the requested instructions directly from its internal register file. Provisions to pause during operand and/or defer cycles to minimize memory conflicts are also provided by the IPF. Whenever the IPF fails to supply the requested instruction, or if it senses that the current instruction will cause the program to break sequence, the IPF will abort the current contents of its register file. The IPF may be enabled and disabled under program control, or manually by means of a switch on the M7172 Bus Interface module.

1.7.4 M7173 Memory Port

The M7173 Memory Port arbitrates requests for memory access directly from the XVM, IPF, and the external processor input. M7173 drives, receives, and deskews the XM15 memory bus. On the external processor input, there are upper and lower limit address selection, negative address relocation (XV200 Unichannel systems) and "address float" which allows positive address relocation. The IPF and XVM inputs do not provide boundary or relocation selection. In addition, the M7173 performs four-way memory interleaving functions. The XM15 houses a second memory port to allow greater flexibility in multi-processor configurations, memory interleaving and distribution, and improved IPF performance.

1.7.5 M7172 Bus Interface

The M7172 Bus Interface receives, drives, and deskews the processor memory bus. The M7172 converts processor address and control information to signals compatible to the XM15 and its memory bus and communicates with the memory port and IPF. Temporary storage for the current memory read data is also provided.

1.7.6 Internal Memory

The XM15 contains either 32K of MF15 core memory or 24K of ME15 core memory and is the basic memory unit for the processor.

1.8 SYSTEM INTERCONNECTIONS

1.8.1 XM15 Bus

The XM15 Bus is the bus between the memory port in the XM15 and the internal and external memory. If the second port is used in the XM15, there will be two independent XM15 buses.

The XM15 Bus connects all memory to the XM15. In addition, the XM15 Bus may be connected to the external processor input of another XVM System to form a multi-processor system with two or more XVMs. Except for the absence of bus arbitration signals, the XM15 Bus is compatible with the Unibus.

1.8.2 CPU and IPU-to-Memory Bus (MDLs)

The Central Processor and I/O Processor each asynchronously access memory over the same MDL bus. The priority structure concerning which processor's request is sent to the XM15 is determined by the processor Memory Port Switch. The I/O Processor is given first priority. The MDL bus consists of 18 bidirectional lines over which address and then data information is transmitted to and from the XM15. Various control signals are on this bus, as well as provisions for interfacing the optional floating-point processor (FP15).

1.8.3 IPU-to-I/O Devices (I/O Bus)

The I/O Processor communicates with all devices over a common I/O Bus which contains bidirectional data lines, address lines, enable, request, and grant lines for API and data channel, and others such as program interrupt and skip request.

1.8.4 Console-to-CPU (IBus)

The IBus contains bidirectional lines to transmit information to the lights on the console and to switch information from the console to the Central Processor. Several control lines are also located on the cable. The ME15/MF15 memory does not use the IBus.

1.8.5 API to Central Processor Bus

Because the XM15 contains several internal options which deal with the operation of the Central Processor, a special cable (API cable) is required so that the option may utilize these internal Central Processor signals.

1.9 SYSTEM SPECIFICATIONS

Functional Characteristics

Word Length	18 bits
Cycle Time	Refer to Table 1-1
Core Memory Capacity	8192 words, expandable to 131,072 words in 8K increments with ME15 Memory; 16K increments with MF15 Memory.
Core Memory Access	
Page Mode	
Direct	4096 words
Indirect	32K, 64K or 128K words
Indexed	131,072 words
Bank Mode	
Direct	8192 words
Indirect	32K, 64K or 128K words
LA36	30 characters per second (300 baud)
Program-controlled I/O Capacity	Up to 256 device codes including prewired CPU and IPU IOTs
Data Channel Capacity	Up to 8 device controllers

Table 1-1
XM15 Typical Cycle Times

Test Mode	NOP (1 Read cycle)	LAC (2 Read cycles)	DAC (1 Read & 1 Write cycle)	ISZ (2 Reads & 1 Write cycle)	Mean Memory Cycle Time
IPF on User Mode off	0.94 μs	2.14 μs	1.92 μs	3.28 μs	1.04 μs
IPF on User Mode on	0.97 μs	2.36 μs	2.03 μs	3.50 μs	1.10 μs
IPF off User Mode off	1.36 μs	2.73 μs	2.50 μs	3.90 μs	1.31 μs
IPF off User Mode on	1.46 μs	2.92 μs	2.57 μs	4.06 μs	1.38 μs

NOTES
1. The standard MF15 memory was used for testing. XM15's equipped with ME15 will attain an improvement of 4%.
2. The mean memory cycle is based on the total memory cycles for the instructions given (total cycles equals eight).

Operating Characteristics (H963D Cabinet; CP, I/O and Memory)

XVM Power Requirements (CPU cabinet with 96K of MF15 memory)	95 – 130 V or 190 – 260 V, 47 – 63 Hz, three phase, 18 A
XVM Power Consumption	2.0 KW max
Power Supply Outputs	Refer to Table 7-5
Logic Levels	0 – 0.4 V = logic 0 2.4 – 5 V = logic 1
Test Temperature Range	50° – 120° F
Relative Humidity	10–95%
XVM Heat Dissipation (CPU cabinet with 96K of MF15 memory)	6750 BTU/hr.
Dimensions	
Cabinet Height	71-7/16 in.
Cabinet Width	21-11/16 in.
Cabinet Depth	30 in.
Door Clearance (rear)	18-7/32 in.
Cabinet Weight (loaded)	600 lbs.

CHAPTER 2
XVM MEMORY SYSTEM

2.1 INTRODUCTION

This chapter is a three-section chapter which provides a functional description of the XVM Memory System. Section 1 pertains to the XM15 Memory Processor with discussions at the XM15 level and at the module level. Section 2 contains general information on the MF15 Core Memory. Section 3 provides general information on the ME15 Core Memory.

SECTION 1 - XM15 FUNCTIONAL DESCRIPTION

2.2 GENERAL DESCRIPTION

The primary function of the XM15 is to receive and process all requests made to memory. In addition, the XM15 provides mounting space and power for the Automatic Priority Interrupt (API) module (M7176). Figure 2-1 illustrates the functional location of the XM15 Memory Processor in the XVM System.

Figure 2-2 is a functional diagram of the XM15 Memory Processor. During a typical reference to memory sequence, the XVM Processor drives the address and control signals onto the Processor Memory Data Lines (MDLs). The M7172 Bus Interface module receives the address and control signals and demultiplexes the MDLs by latching the address and control bits. The M7172 passes the address to the XM15 internal bus where bits 0–9 are routed to the M7175 Memory Management module. The remaining address bits are routed directly to the M7173 Memory Ports.

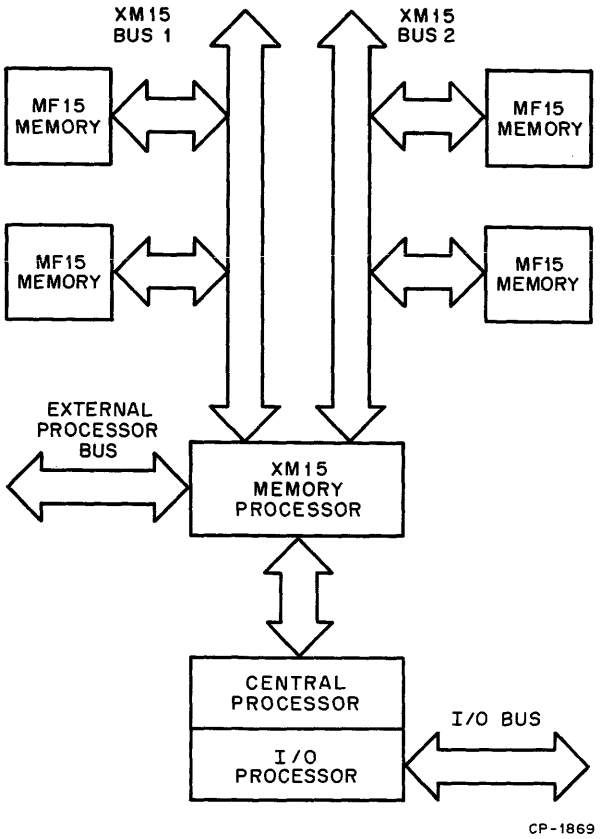


Figure 2-1 XM15 Functional Location

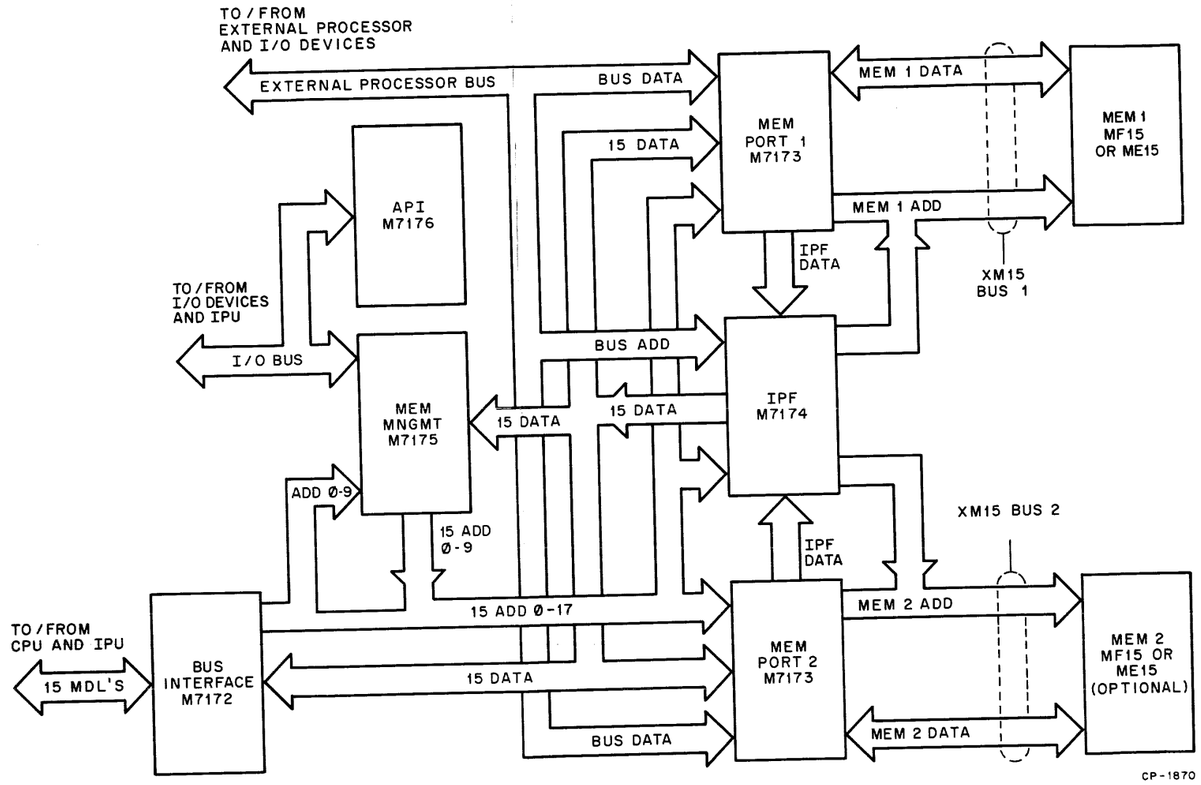


Figure 2-2 XM15 Functional Block Diagram

The M7175 Memory Management module performs all address modifications, as required by the operating system software, by loading multiple relocation registers and by selecting various address modes. Relocation data and address mode control are provided by IOT commands via the I/O Bus (IOB). Address bits 0–9 from M7175 then join the remaining address bits on the XM15 internal address bus. The complete address is examined by the M7173 Memory Ports and the M7174 IPF module to determine the correct destination of the memory request.

In a system using the two Memory Ports, one of the two M7173 Memory Ports will be selected by the incoming address. Once selected, the Memory Port arbitrates all current requests. Requests may also come from the External Processor Bus and/or the M7174 IPF module. First priority is given to the XVM requests and are therefore processed immediately. The address will be interleaved while the Memory Port arbitrates incoming requests. The Memory Port then begins driving the memory address and deskews the address according to the type and mixture of memory (MF15 and/or ME15) on the XM15 Bus. At the end of deskew time, the selected memory bank (Memory 1 or Memory 2) retrieves or writes the data from/to the location specified by the address. In the case of a read, the data driven by memory through the selected M7173 Memory Port is first deskewed by the Memory Port and then latched by the M7172 Bus Interface module. This scheme releases the selected Memory Port and the XM15 Bus at the earliest possible time. The M7172 Bus Interface then signals the XVM Processor that data is ready, thus completing the memory reference.

For all memory reads, the M7172 Bus Interface determines if the XVM Processor is in an instruction Fetch Cycle and signals the M7173 Memory Ports and the M7174 IPF module when this condition exists. During an instruction fetch, the Memory Ports are inhibited and the IPF module is allowed to process the request. The current state of the IPF module may be IOT-disabled, idle, or enabled. When the IPF is IOT-disabled, the Memory Port honors the request as previously discussed. When enabled, the IPF module examines the memory address to determine if the requested instruction is contained in the IPF module register file. If present, the instruction is driven by the IPF module to the M7172 Bus Interface where it is latched. Failure ofthe M7174 IPF module to provide the requested instruction causes the IPF module to abort and flush its register file. The abort also allows the Memory Port to honor the request in the normal fashion.

Aborts, or following an IOT enable, causes the M7174 IPF module to enter the idle state. In the idle state, the IPF module waits for the first instruction cycle but does not inhibit the M7173 Memory Port. When the address is stable on the XM15 internal bus, the IPF module loads the address into its internal program counters and increments the counters by one. The IPF module then posts a request to the appropriate Memory Port. Memory Port priority structure provides the IPF module with a priority of three. However, in a two-Memory Port system, the Memory Port selected may be opposite that of the currently active Memory Port. Thus, the IPF module request will be honored immediately. The IPF module then drives its address directly to memory while the Memory Port maintains the control signals. Data returning from memory is driven via the Memory Port over the IPF data lines and is loaded into the IPF module register file. This action places the IPF module in the enable state. Once in the enable state, the IPF module attempts to retrieve up to four memory locations in advance of the XVM instruction requests. Simultaneously, the IPF module processes new requests for instructions from the XVM and replaces each, as they are used, with the next sequential location from memory. The IPF module continues to function until disabled by an IOT or disabled manually by a switch on the M7172 Bus Interface module.

The M7173 Memory Ports also receive requests for memory access from an external processor via the XM15 External Processor Bus. The external processor may be a PDP-11 peripheral processor of an XV200 System, as shown in Figure 2-3, or an XM15 Memory Processor System of another XVM System, as shown in Figure 2-4. Data is handled in the same manner as normal XVM data, however, the address is driven directly to memory through the M7174 IPF module. The IPF module multiplexes its own address with the address from the external processors. External processor requests are given second priority in the Memory Ports.

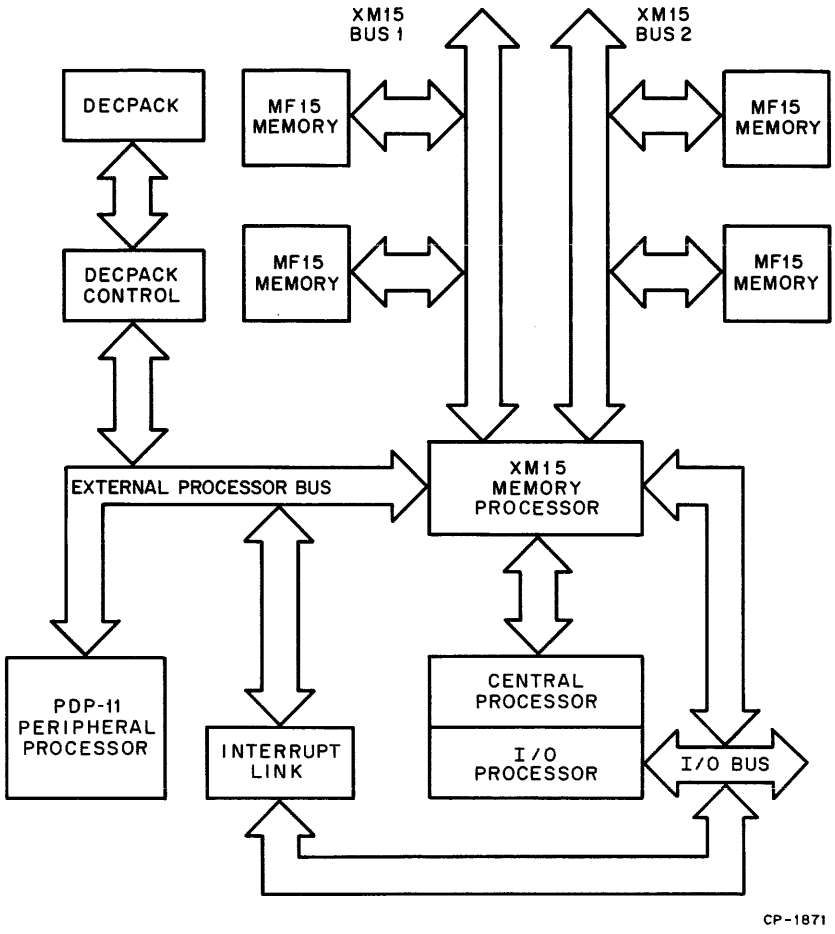


Figure 2-3 Typical XV200 System With Peripheral Processor

The XM15 M7176 API module functions independently of the XM15 memory processing modules. The M7176 provides four levels of software-controlled interrupts and four levels of hardware interrupts. All interrupt levels are automatically vectored to the appropriate service routine entry locations. Provisions are made for testing and software control, such as enabling and disabling different interrupt levels.

A Task Accounting Clock is also contained on the M7176 API module. This clock is a self-starting, high-resolution (10 μs) clock which can be used to provide data to allow accurate appropriation of machine cost among multi-users of the XVM System. The Task Accounting Clock registers are read and cleared by a single IOT.

2.3 BUS INTERFACE (M7172)

2.3.1 Memory Read Operation

Figure 2-5 is a functional block diagram of the M7172 Bus Interface module. For a memory read operation, MDL 00–17 is received by the M7172 module for both address and data information. At the beginning of an XVM CPU memory request, the MDLs will be driven with the address of the requested memory location. These lines are applied to the input of the address register in the M7172 module, and approximately 40 ns later, the control logic produces the LD ADD signal. At this time, the address is held in the register and an address acknowledge signal is sent to XVM CPU. From this time on, the actual memory request is handled almost entirely by the M7172 Bus Interface module.

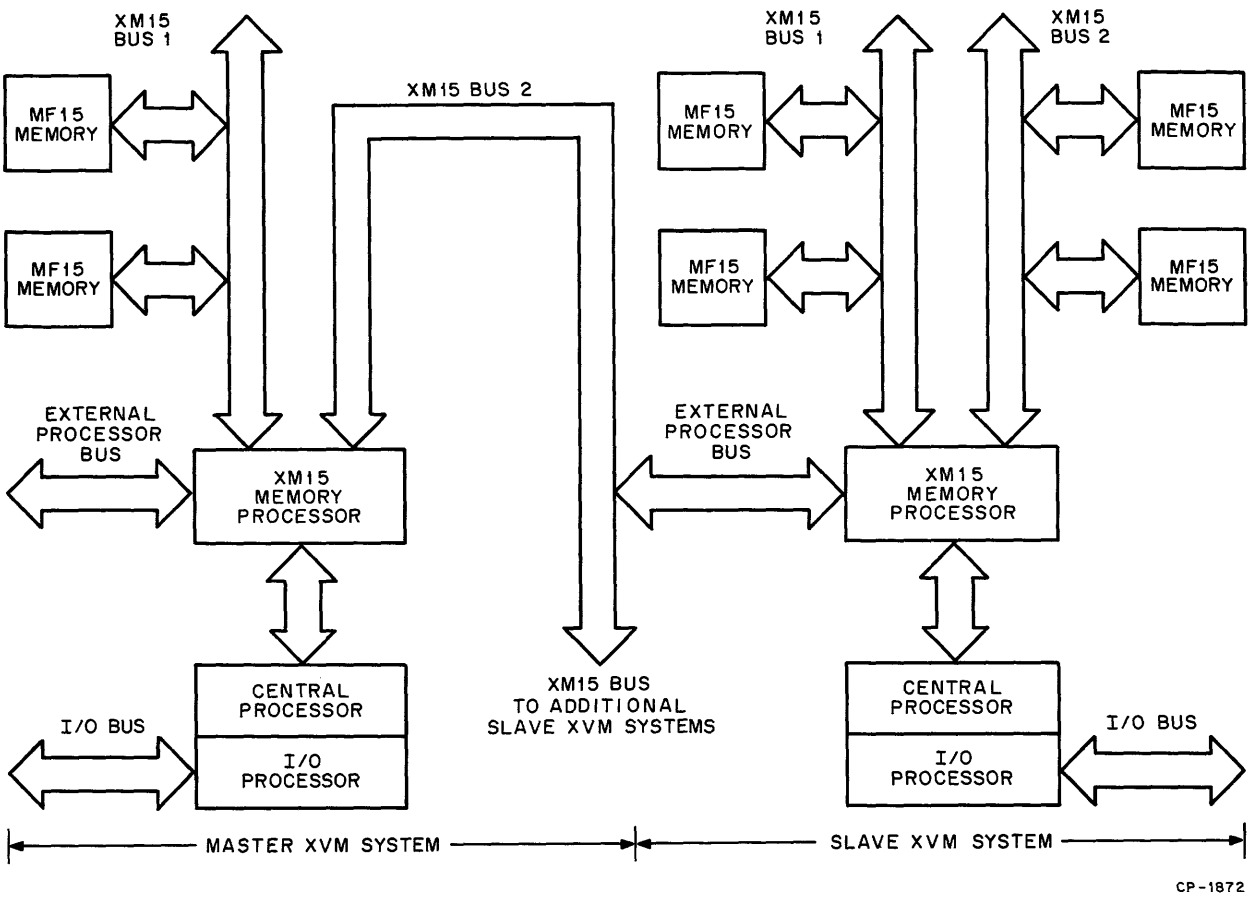
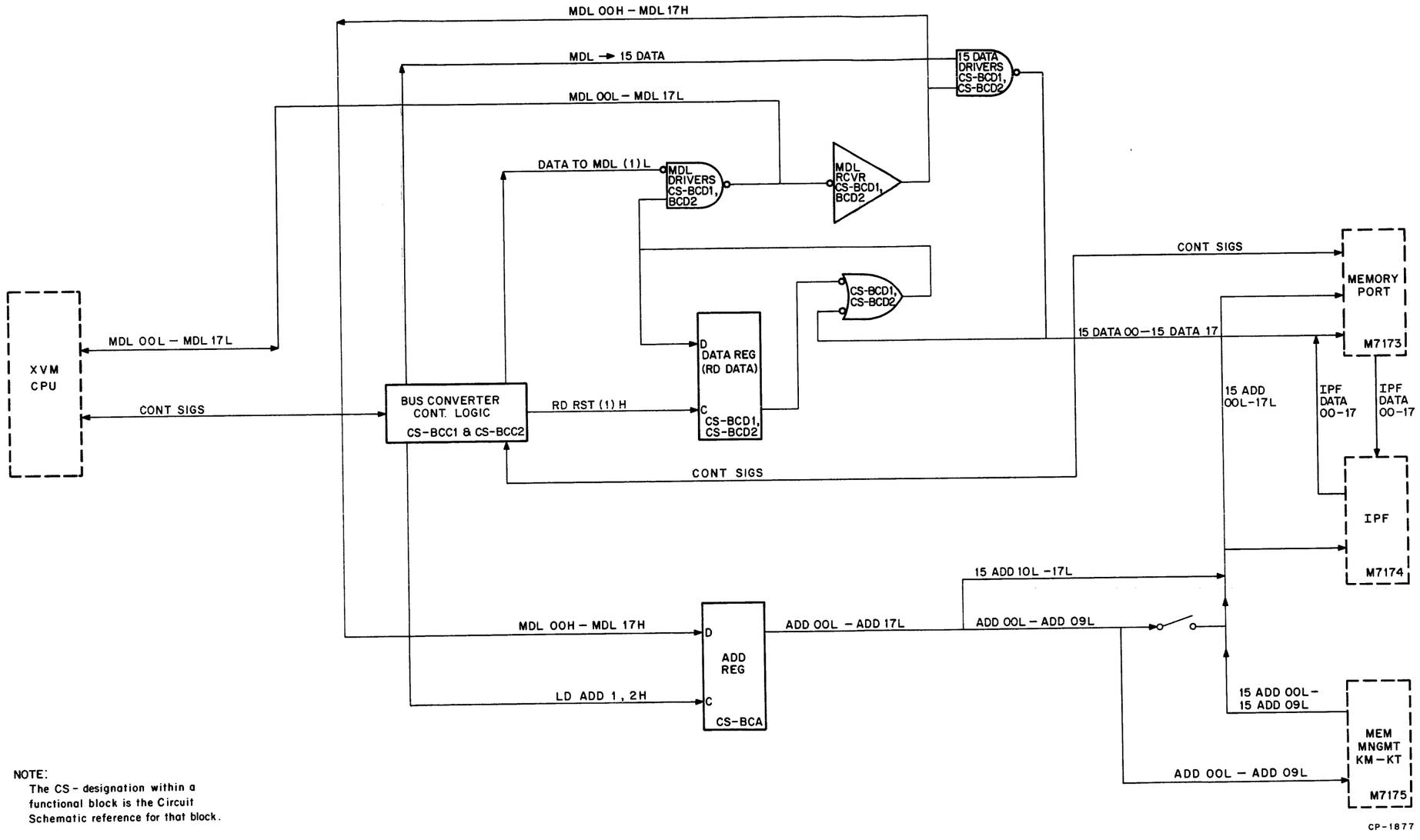


Figure 2-4 Master-Slave XVM System

Internal to the M7172, the memory read and memory write signals from the XVM CPU are converted into Unibus convention. That is, they are converted into control signals C0 and C1 and are presented to the XM15 internal bus. After an appropriate amount of time for address deskew, MSYNC is asserted on the internal bus. The address at MSYNC time can take one of two different paths. One path feeds directly to the internal bus where bits 10–17 are always driven. However, bits 0–9 may either be driven directly through switch selection or they will follow a separate path to the M7175 Memory Management module. In the M7175, the address bits will either be modified or passed directly onto the internal bus.

The internal bus presents all 18 bits, including any modification of the upper 10, to both M7173 Memory Ports and the M7174 IPF in an attempt to satisfy the memory request. If the memory request was for an instruction, this is detected by the M7172 Bus Interface module. A control signal is then sent to the IPF to indicate that this is an instruction request. At this time, the IPF examines the incoming address to determine whether or not the data is currently stored in the register file of the IPF. If not in the register, the address is presented to the Memory Ports along with MSYNC and the proper control signals for port selection. The address is then passed onto the XM15 bus and forwarded to the memories.



NOTE:
The CS- designation within a functional block is the Circuit Schematic reference for that block.

Figure 2-5 M7172 Bus Interface Functional Diagram

Data flow from the IPF or Memory Ports is driven onto the internal bus where it is presented to the M7172 Bus Interface module. At this point in time, the data is ORed and driven onto the MDL lines. At read-restart time, the data is loaded into the M7172 data register. All read data returning from memory or the IPF is loaded into this data register. Figure 2-5 shows the ORing of the data coming back from the Memory Ports with the data from the M7172 data register. This is done so that the data is presented immediately to the MDL driver, even before it has been strobed into the data register. This allows overlapping the deskew of the drivers with the time for loading and resettling of the data register. As soon as read-restart is issued, the Memory Port is released; that is, the internal MSYNC is dropped. Read-restart is then sent back to the XVM CPU, indicating that valid data is now being driven on the MDLs.

2.3.2 Memory Write Operation

For Memory Write Operations, the initial procedures are the same as those previously discussed for the read operation. That is, the address is first driven on the MDL lines and loaded by LD ADD in the M7172 address registers. The XVM then receives an address acknowledge from M7172 and then proceeds to place data on the MDL lines. Data on the MDL lines is driven through the 15 data drivers to the internal bus. The internal bus consists of separate address and data lines. The address driven out from the address register is presented to the IPF and Memory Ports, while the data is driven from the MDLs through the 15 data drivers and is presented to the internal bus. For write operations, the IPF examines the address to see whether or not the write is an attempt to alter data already in the IPF register file. If in the register file, the IPF will abort. At the same time, the Memory Ports will recognize that the XVM CPU is requesting a write to memory and will immediately load the write data into a holding register in the Memory Port. Even if the Memory Port is currently controlled by another device, the loading of the holding register will occur. This allows the release of the XVM from driving the write data on the MDLs.

The asynchronous nature of the M7172 Bus Interface allows sending control signals to the XVM sooner, but, at the same time, the Bus Interface ensures that a new request does not enter until the old request has been completely processed. This is accomplished at the beginning of each cycle through the Bus Interface by setting a busy flip-flop, which locks out further requests.

2.4 MEMORY PORT (M7173)

The M7173 Memory Port module contains memory request arbitration circuitry, data and address receivers and drivers, data multiplexers and holding registers, and memory control drivers. The M7173 can be functionally divided into port data circuits (Figure 2-6) and port address circuits (Figure 2-7). Memory requests from the external processor or IPF have their address and control signals processed by the M7174 IPF module rather than by the M7173.

2.4.1 Memory Port Data Flow

Figure 2-6 shows the M7173 data flow circuits. For a memory read by the XVM CPU or I/O Processor, assuming that Memory Port control is given to the XVM, the Memory Port posts a request to memory and, at the completion of memory access time, memory data (MEM 17L - 00L) is presented to the M7173 memory data receivers. The memory data receivers invert the data and present it to a pair of internal bus drivers (15 data driver and IPF driver). If this particular memory request is for the XVM, ENB 15 DATA will be true and the memory data is passed to the internal bus as 15 00L - 15 17L. 15 00L - 15 17L is received and loaded into the M7172 Bus Interface read data register.

For memory write operations, M7172 drives 15 00L - 15 17L to the internal bus where the data is presented to the 15 data register in the M7173. The loading of the data into the port's 15 data register is not held up for port arbitration. Rather, the data is loaded as soon as 15 MSYNC is presented to M7173 and the XVM is allowed to drop the data. The remainder of the write operation to memory will proceed automatically in the port when control is given to the XVM. The output of the M7173 15 data register is presented to the data multiplexer (MUX) where the port control arbitration logic selects either 15 data or external processor data (BUS 17L - BUS 00L). Having selected 15 data, the output of the MUX is presented to the M7173 memory data drivers and is driven to the memory bus as MEM 17L - 00L, thus completing the write operation.

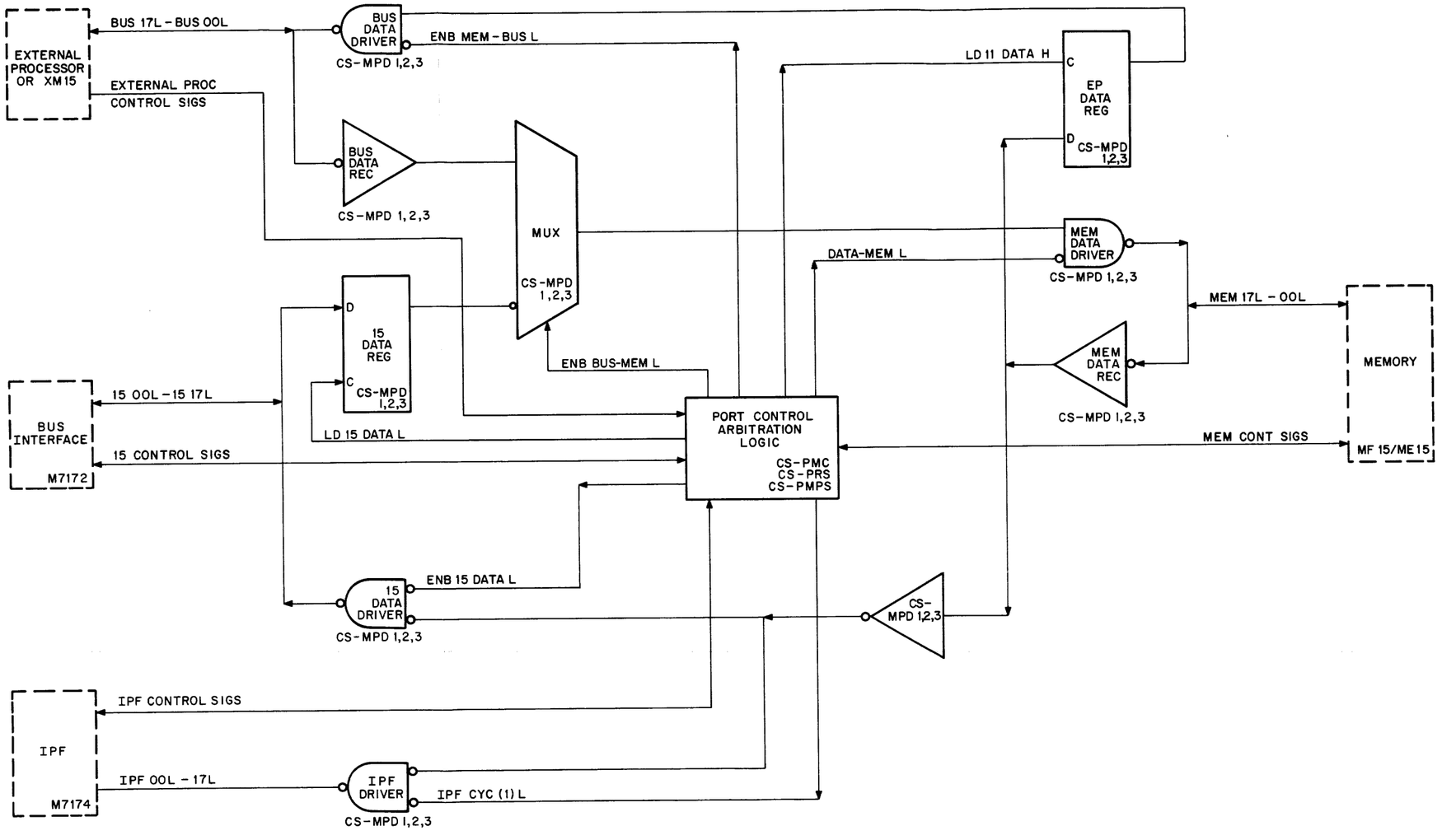
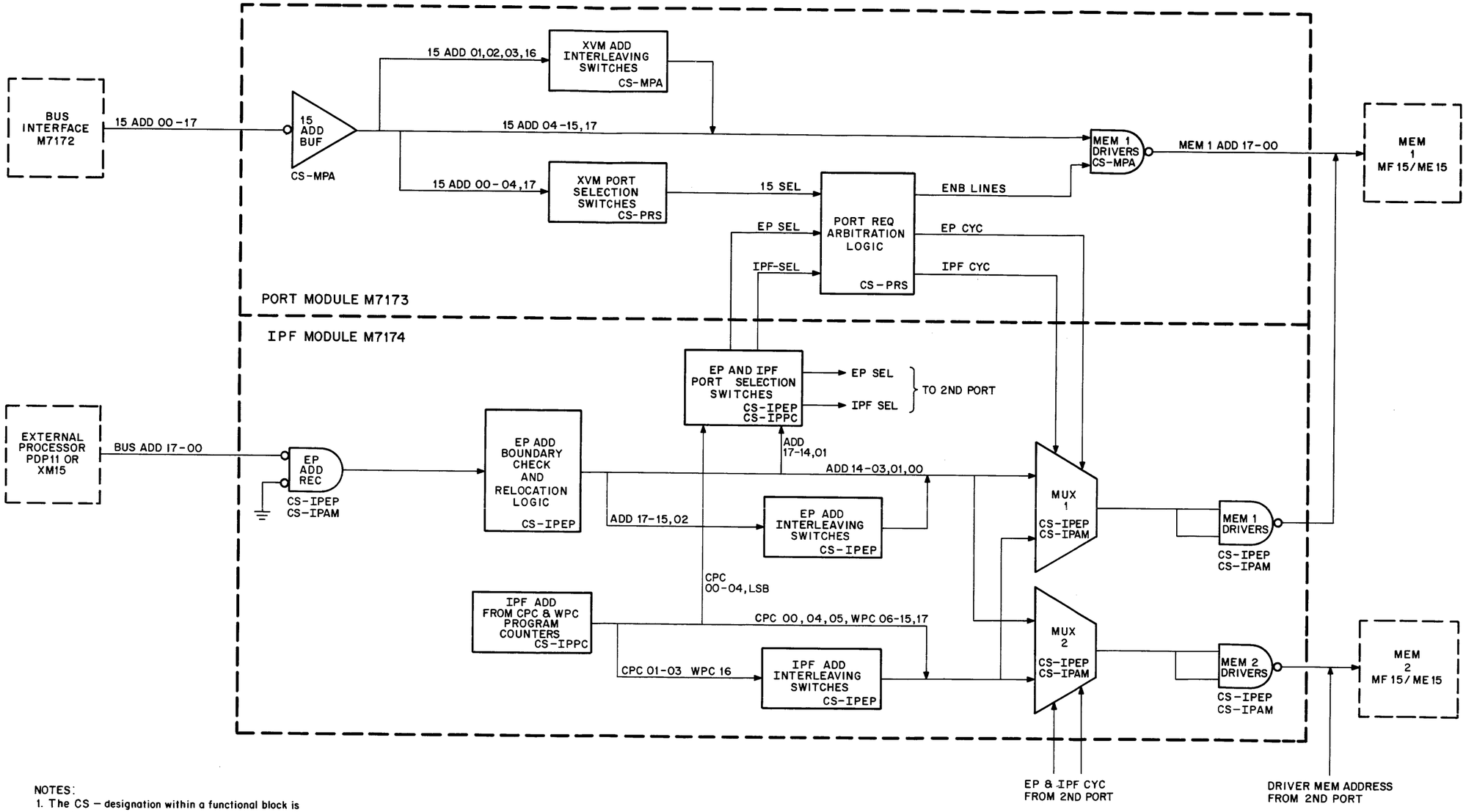


Figure 2-6 M7173 Memory Port Data Flow Functional Diagram



NOTES:
1. The CS – designation within a functional block is the Circuit Schematic reference for that block.
2. The M7173 Port Circuits are duplicated if two Memory Ports are present in the XM15.

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Figure 2-7 Memory Port Address Flow Functional Diagram

For external processor memory reads and memory writes, bus data (BUS 17L – BUS 00L) provides the path from the external processor to the M7173 Memory Port. When the port control arbitration logic has given the current request to the external processor, data is returned on the memory data lines (MEM 17L – 00L) where it is received by the M7173 memory data receivers and presented to the External Processor (EP) data register. At SSYNC time LD 11 DATA loads the EP data register.

The EP data register output is then presented to the M7173 bus data drivers. ENB MEM → BUS L then drives the data to the external processor bus where the data is received by the external processor.

For memory write operations, the external processor presents the data to BUS 17L – BUS 00L and it is received by the M7173 bus data receivers. The output of the bus data receivers is presented to the MUX. However, this time the MUX is selected to take external processor data and present it to the memory data drivers where it is driven to the memory (as MEM 17L – 00L) to be written.

For IPF memory reads, the IPF receives control from the M7173 control arbitration logic. The memory read data (MEM 17L – 00L) is driven from memory through the M7173 memory data receivers, through an inverter, and is presented to a pair of internal bus drivers (15 data driver and IPF driver). However, this time the IPF driver is enabled by IPF CYC (1) L. The data is driven to the M7174 IPF module where it is written into the IPF file. *Note that the IPF does not make memory writes. IPF data flow is one way; that is, memory reads only.*

2.4.2 Memory Port Address Flow

The address flow circuits are shown in Figure 2-7. Note that the M7174 IPF module, as well as the M7173 Memory Port module, contain circuits which operate in conjunction with each other to process memory addresses. All memory requests, regardless of the source (XVM processor, external processor, or the IPF module), are handled on the M7173 Memory Port module. The circuitry consists of buffers and receivers, address multiplexers (to select the device currently accessing memory) and memory address drivers.

Whenever the M7172 Bus Interface processes a request from the XVM CPU, it presents 18 bits of address (15 ADD 00–17) to the 15 internal bus. The address is buffered in the M7173 by the 15 address buffers and is divided into three basic address flows:

1. Address bits (15 ADD 04–15, 17) which are applied directly to the M7173 memory address drivers
2. 15 ADD 01, 02, 03, and 16, which are applied to the XVM address interleaving switches
3. 15 ADD 00–04, and 17, which are applied to the M7173 XVM port selection switches.

At the XVM port selection switches 15 ADD 00–04, 17 generate 15 SEL (depending on the amount of memory behind the port module and the mode of memory interleaving). 15 SEL is passed to the M7173 port request arbitration logic. (In a two-Memory Port system, both ports receive 15 MSYNC. However, only one port will be selected at a time by the port request arbitration logic.) 15 ADD bits 01, 02, 03, and 16 are passed to the XVM address interleaving switches where second level interleaving is performed. (First level interleaving is performed in the memories on the LSB bank and word bits of the address.) In the M7173, the bits involved in second level interleaving cause the second LSB bank and word bits to be interleaved. This results in four-way interleaving. With the bits interleaved and the selection accomplished and 15 ADD 04–15, 17 applied to the M7173 memory address drivers, the port request arbitration logic selects one of the three (15 SEL, EP PORT SEL, or IPF PORT SEL) requesting inputs for the current memory cycle. When the port request arbitration logic makes its selection and generates address enables (ENB LINES if the XVM processor gains memory access, External Processor Cycle [EP CYC] if the external processor gains memory access, or IPF Cycle [IPF CYC] if the IPF module gains the current memory access) MSYNC is posted to the memory. The memory cycle processes as normal.

For requests from the External Processor (EP), BUS ADD 17–00 is received by the M7174 IPF module where port selection and memory interleaving processes, similar to those described for the M7173 address bits, are performed. In addition and prior to the selection and interleaving, the external processor's address bits are checked for boundary conditions and the address is relocated by the M7174 EP address boundary check and relocation logic. (The boundary conditions and the relocation factor are switch-selectable.) The output of the M7174 EP address boundary check and relocation logic is now split into three groups. In this case, ADD 14–03, 01, 00 are passed directly to the M7174 address multiplexers (MUX). ADD 17–14 and 01 are applied to the M7174 EP port selection switches. ADD 17–15 and 02 go to the EP address interleaving switches.

The M7174 EP port selection switches generate the External Processor Select (EP SEL) signal to the appropriate port (assuming a two-port system). The address is interleaved, in a manner previously described for the M7173 Memory Port module. The resultant address, that is, the combination of the interleaved (ADD 17–15, 02) and the direct address (ADD 14–03, 01, 00) bits are presented to the M7174 address multiplexers (MUX). EP CYC from the M7173 port request arbitration logic selects which of the M7174 MUX inputs is to be driven to memory.

Note that the address multiplexers (MUX) and the memory address drivers are duplicated on the M7174 IPF module. This duplication accomplishes independent addressing whenever there are two M7173 Memory Port modules in the XM15. Independent operation on two separate memory buses (XM15 BUS 1 and XM15 BUS 2) occurs by allowing one Memory Port module to select one M7174 MUX to drive its corresponding memory address drivers while the second M7174 MUX and memory address drivers handle another requesting device. For example, the IPF or the external processor can drive one memory bus while the XVM drives the other. Another example would be the IPF and external processor each driving one bus while the XVM is idle.

The bit numbering scheme for the external processor follows Unibus convention. That is, the MSB of the address is bit 17 and the LSB is bit 0. However, for XVM addressing in the M7173 module (Figure 2-7) the address bits follow XVM convention – the MSB is bit 0 and the LSB is bit 17. Also, bit 0 of the external processor is a byte address bit, whereas the XVM does not use byte addressing. The actual conversion from one bit numbering scheme to the other occurs at the M7173 and M7174 memory address drivers.

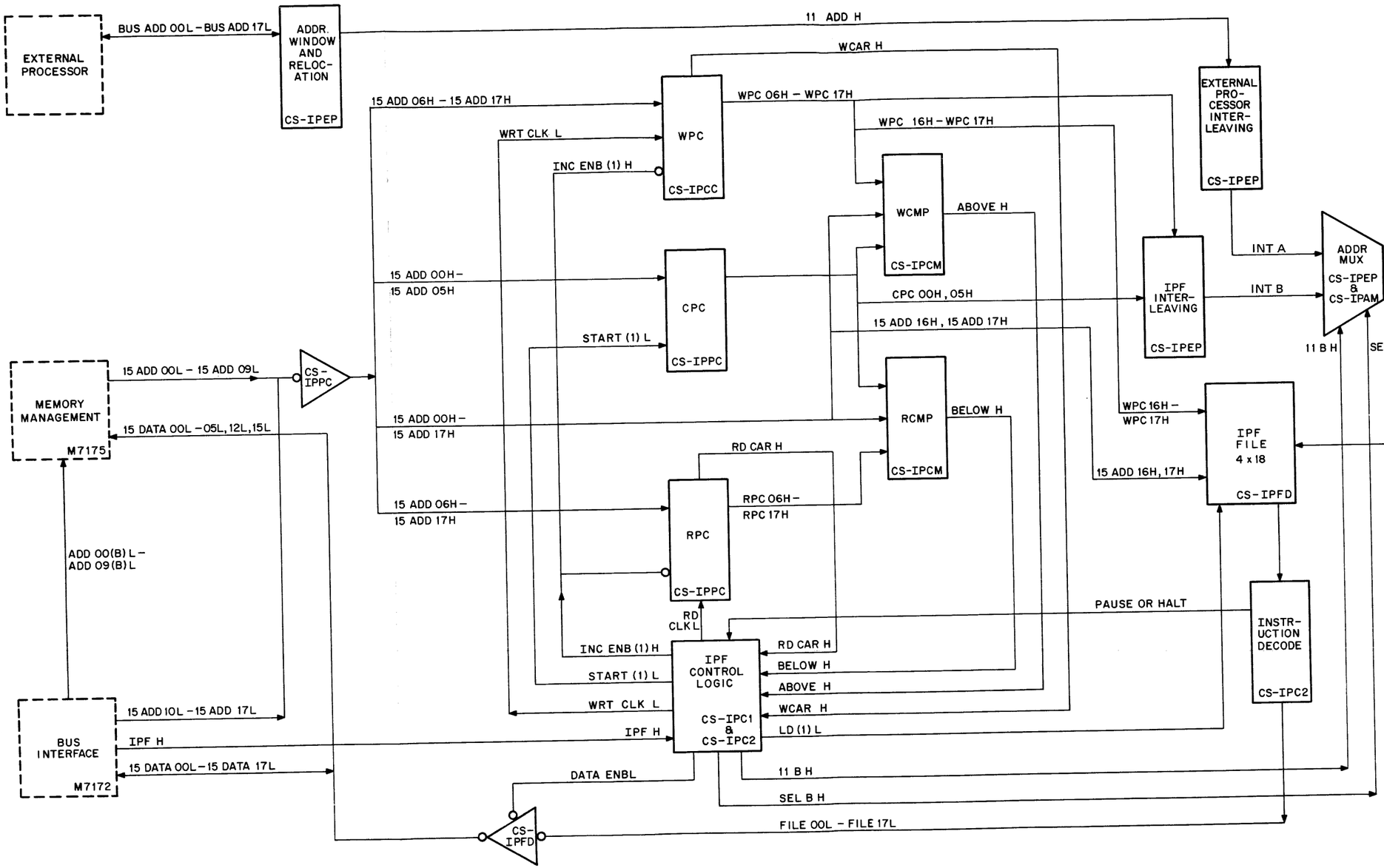
All switch selections for the M7173 and M7174 modules regarding port selection and memory interleaving are set up once the configiration of the XVM System is established. The equivalent switches (port selection or interleaving) for the three possible input devices (XVM, external processor, and IPF) are normally set in a similar manner. That is, once the interleaving format is established, the M7173 XVM interleaving switches and the M7174 EP address and IPF address interleaving switches are set to the same switch pattern. Similarly, the M7173 XVM port selection switches and the M7174 EP and IPF port selection switches are set to the same pattern.

2.5 INSTRUCTION PREFETCH (IPF M7174)

The M7174 IPF module has four types of operations that can occur:

1. The start-up sequence,
2. A memory read sequence (IPF write)
3. An instruction request sequence
4. An abort sequence.

External processor address multiplexing is also handled by the IPF module. Figure 2-8 is a block diagram of the M7174 IPF module. This diagram and the aforementioned operations are discussed in the following paragraphs.



NOTE:

The CS – designation within a functional block is the Circuit Schematic reference for that block.

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Figure 2-8 M7174 Instruction Prefetch Functional Diagram

2.5.1 Start-Up Sequence

If the IPF module has not been disabled by an IOT, the Start-Up Sequence will occur automatically and will be the first operation to be initiated. The Start-Up Sequence will also occur whenever the XVM console key functions of DEP, EXAM, or DEP NEXT are operated. The sequence of events which occur during start-up begin by the receipt of the 15 address bits (15 ADD 00–09 from the M7175 Memory Management module, and 15 ADD 10–17 from the M7172 Bus Interface module). Following the receipt of the 15 ADD bits, MSYNC is asserted and if an instruction is being requested, the M7172 Bus Interface module will have asserted the signal IPF H, which indicates to the IPF module that it is an instruction request. The IPF control logic recognizes that it has not been previously started and initiates a start timing sequence.

At this time ENB is false. This allows the START signal (first event in the timing sequence) to load 15 ADD 00–05 into the CPC (Common Program Counter). The RPC (Read Program Counter) and the WPC (Write Program Counter) are in the load mode. RD CLK and WRT CLK are now produced by the IPF control logic and load the 15 ADD 06–17 bits into the RPC and WPC respectively. When set, the INC ENB flip-flop causes the RPC and WPC to switch to the increment mode. Subsequently, the RPC is incremented byone (by RD CLK). The contents of the RPC now indicate the first instruction address to be loaded into the IPF file. The instruction will come from the memory location one greater than the current address being requested by the XVM CPU. During this same time period, the IPF issues an Abort Clear which causes the M7172 Bus Interface module to negate IPF H. This allows the requested instruction to be processed directly through the M7173 Memory Port module rather than the IPF module. Following the Start-Up Sequence, the ENB flip-flop is set and the IPF module automatically begins to do memory read operations.

2.5.2 Memory Read Sequence (IPF Write)

The Memory Read Sequence begins when the IPF control logic issues WRT CLK to the WPC and increments the WPC by one. WPC and RPC are now equal and IPF MSYNC and IPF Port Select are asserted to the Memory Port. In a two-port system, the address that is being requested would normally be on the Memory Port opposite that currently being accessed by the XVM CPU. Therefore, the M7173 Memory Port module responds rapidly to the request and the IPF asserts LD (1) L. LD (1) L conditions the file to receive data from the port. For example, if the XVM CPU is requesting location 1000 in port 1, then the first instruction the IPF requests is from location 1001 in port 2. This essentially provides overlap of the two memory accesses whenever this situation occurs. Approximately 600–650 ns after the assertion of MSYNC, the data is driven from the M7173 Memory Port back to the IPF module. SSYNC is then asserted by the Memory Port, indicating that the data is stable and valid. At this time, the IPF control logic negates LD (1) L, which causes the data to be latched into the IPF file, thus completing the first memory reference for the IPF. The write file address is selected by WPC bits 16 and 17.

From now on, the write section of the IPF will continually access memory, fetching additional instructions and following the same sequence just described. The IPF will fetch a specified number of locations in sequence. The number of locations being fetched is controlled by the IPF control logic Full Counter. The Full Counter may be set for either 1, 2, or 4 words to be fetched and loaded into the IPF file. After incrementing the WPC and asserting MSYNC (as previously described), the Full Counter is incremented by one. The Full Counter indicates the number of memory references made which have not yet been read out of the IPF file. During successful instruction requests (Paragraph 2.5.3), the Full Counter is decremented.

At some point in time, while the filling procedure for the IPF file is taking place, the processor will come back and request another instruction. As before, the M7175 Memory Management module will drive the address to the IPF module, MSYNC will be asserted, and the M7172 Bus Interface will have driven IPF H, indicating an instruction fetch. However, at this time the IPF module is no longer in an idle condition. The Start-Up Sequence is bypassed and the IPF module enters the Instruction Request sequence.

2.5.3 Instruction Request Sequence

For the Instruction Request Sequence, the contents of the RPC and WPC indicate the lower and upper boundary addresses (respectively) of the IPF file. (It should be noted that the CPC is never incremented. Therefore, the RPC and WPC are not incremented across a 4K boundary and the CPC indicates the current 4K memory segment.) The contents of the IPF program counters are compared against the incoming address for the conditions ABOVE (from WCMP-Write Comparator) or BELOW (from RCMP - Read Comparator). If either ABOVE or BELOW is asserted, then a MISS condition exists and the IPF does an Abort sequence (Paragraph 2.5.4).

However, if ABOVE or BELOW is not asserted, the requested instruction is contained in the IPF file. The IPF file is addressed with ADD 16,17 and the three state drivers are enabled with DATA ENBL. IPF file data (FILE 00 - FILE 17) is thus driven back to the M7172 Bus Interface module where it is latched into a holding register.

After the data has been read out of the IPF file and accepted by the Bus Interface module, the RPC is incremented by one or more locations. This is done to bring the contents of the RPC up to the value of the currently requested address, plus one, and ensures that the lower boundary (contents of RPC) of the IPF file is always one greater than the file location just read. This ensures that locations skipped over, in the case of a SKP or similar situation, will not go unused in the continuing refill process of the IPF file.

An instruction request can occur during a memory read operation, except for a very small period of time when the instruction program counters in the IPF module cannot be altered because of an incoming request. This allows overlap of the memory read and the instruction request operations.

2.5.4 Abort Sequence

If during an instruction request sequence either ABOVE or BELOW is asserted, a MISS condition occurs. When a MISS is detected, the IPF begins an Abort Sequence. The Abort Sequence consists of clearing the IPF H signal to the M7172 Bus Interface module to allow the request to be processed through the M7173 Memory Port. The clearing process also clears the control functions of the IPF control logic. When the clearing operations are completed, the IPF is in an idle state and begins another Start-Up Sequence to resynchronize itself to the current instruction address.

The Abort Sequence can also be caused by other events, such as the XVM CPU attempting to write new data into a memory location that has already been written into the IPF file. This invalidates the data in the IPF file. The IPF therefore aborts and performs a Start-Up Sequence on the next instruction address.

Aborts can also be caused by instructions leaving the IPF file that cause the processor to break sequence. Decoding of the IPF file output, detects JMP, JMS, or CAL instructions, and by knowing in advance that the processor is going to break sequence, the IPF can do a HALT function, which allows the IPF to come to an orderly halt. The IPF then aborts the current IPF file contents and begins to resynchronize itself to the new address by performing the Start-Up Sequence.

2.5.5 IPF Pause

The Pause ensures that the IPF does not interfere with the operand or defer cycles of specific instructions. In this situation, the data output of the IPF file is decoded for the detection of these instructions. When the IPF issues a read operand instruction, a pause flip-flop sets (pause one and/or pause two). Setting a pause flip-flop holds off memory operations by the IPF until one or two memory cycles have been completed. Two memory cycles, while pausing, are required for a memory read operand indirect operation where two references are required in addition to the instruction reference. After the required number of memory references have been counted, the IPF resumes making memory accesses in an attempt to fill the IPF file. A DAC or DZM indirect instruction will cause the IPF to pause one memory cycle, as will a read operand instruction.

2.5.6 External Processor Addressing

A feature of the IPF module which is independent of the overall IPF function is that of processing external processor addresses. Contained on the IPF module is the logic necessary to receive external processor addresses. Addresses are checked for upper and lower boundary conditions and may be relocated. (The boundaries and relocation are selectable for various XVM System configurations.) In addition, Memory Port selection for the external processor and address bit interleaving for the relocated addresses are provided. Finally, a pair of multiplexers direct the IPF address, or the address of the external processor, to either XM15 BUS 1 or XM15 BUS 2. The multiplexing allows the external processor to access one of the XVM memories while the IPF module accesses the other memory. Control and selection of the IPF multiplexers are accomplished by the signals 11A H, 11B H and SEL A H, SEL B H.

2.6 MEMORY MANAGEMENT (M7175)

The M7175 Memory Management module contains relocation registers, address comparators, and instruction decode circuitry to provide the XVM with a variety of Memory Management features. There are two basic modes of operation for the M7175 module:

a. The Protect Mode (Figure 2-9)
b. The Relocate Mode (Figure 2-10).

A jumper on the M7175 module provides the means by which either mode is selected.

2.6.1 Protect Mode

The memory Protect Mode provides the XVM with memory protection capabilities. The M7175 uses a boundary register (Figure 2-11) to establish the lower limit of the user's program. There are facilities to trap IOTs, HLTs, OASs, XCTs of XCTs, boundary violations, and addressing of nonexistent memory. The M7175 also allows addressing below the boundary on all read instructions except JMP and ISZ. Indirect address width control (G Mode) is allowed in the Protect Mode. There are two states of operation in the XVM Protect system - User Mode and Monitor Mode. In the Monitor Mode, the Protect hardware is disabled and the machine functions as it would without the Protect hardware. When in User Mode, the Protect logic is enabled.

The M7175 Memory Management module is activated by the IOT, MPEU. This first sets PRE, which in turn conditions UM (User Mode) to set on the next memory reference. With PRE and UM set, the M7175 monitors instructions as they are read from memory, as well as the addresses of core locations being referenced. To monitor the instructions read from core, a register is used to save the instruction. To monitor addresses, MSYNC is delayed before going to memory until the address is checked. When the comparison of the boundary register and the address is performed, and if a carry is generated, the address is less than the boundary register and therefore is a Protect violation.

2.6.1.1 Traps - If the memory protect logic detects an illegal instruction (HLT, OAS, IOT, XCT of XCT), or an address below the boundary register which is preset by the programmer, or a reference to a nonexistent memory (NEXM), then the trap process begins. Traps, except for NEXM, may be disabled by setting R DIS in the MM register, and IOTs will be allowed if IOT Permit is set in the MM register. Since a HLT or OAS may be microcoded with other operate instructions, the HLT or OAS function is inhibited and the other portion of the microcode is allowed to be executed before the trap interrupt occurs.

The trap interrupt goes to address 20, if PIE is not set, and to 0 if PIE is set. It operates essentially the same as a CAL or a program interrupt in that it stores the LINK, BANK MODE, USER MODE, and PC+1 in 20 or 0. There are two exceptions to this: If it is a jump below the boundary, the address to which it tried to jump will be saved. If it is a jump indirect to a nonexistent memory, the address in the nonexistent memory will be stored.

A nonexistent memory violation is detected by comparing the M7175 output address with the NEXM switches. If User Mode is on and the program tries to address nonexistent memory, a trap occurs. A nonexistent memory flag is set, and the computer restarts in a CAL just like any other violation. If User Mode is off and the program tries to address nonexistent memory, the computer hangs up and the nonexistent memory flag gets set.

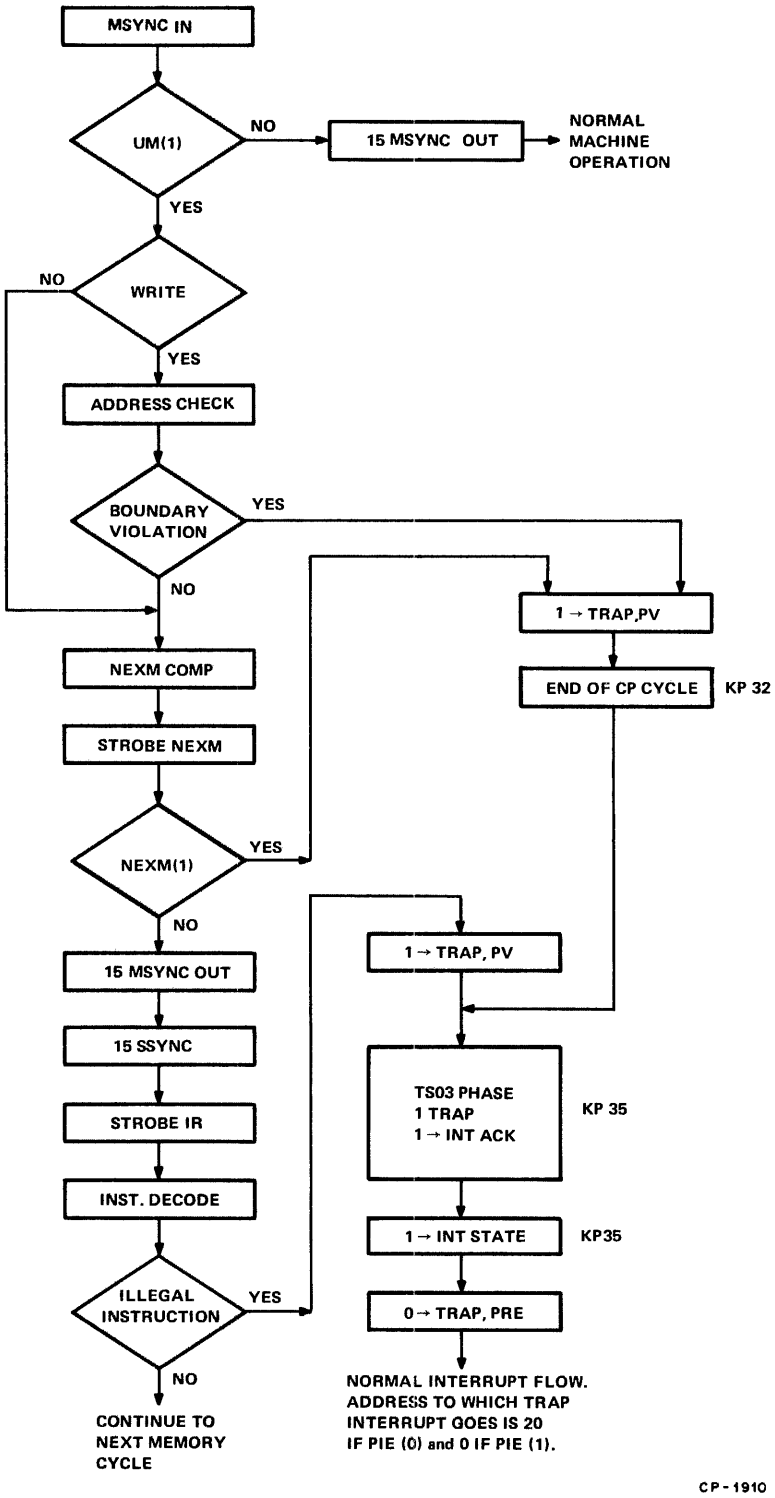


Figure 2-9 Memory Protect Flow Diagram (M7175)

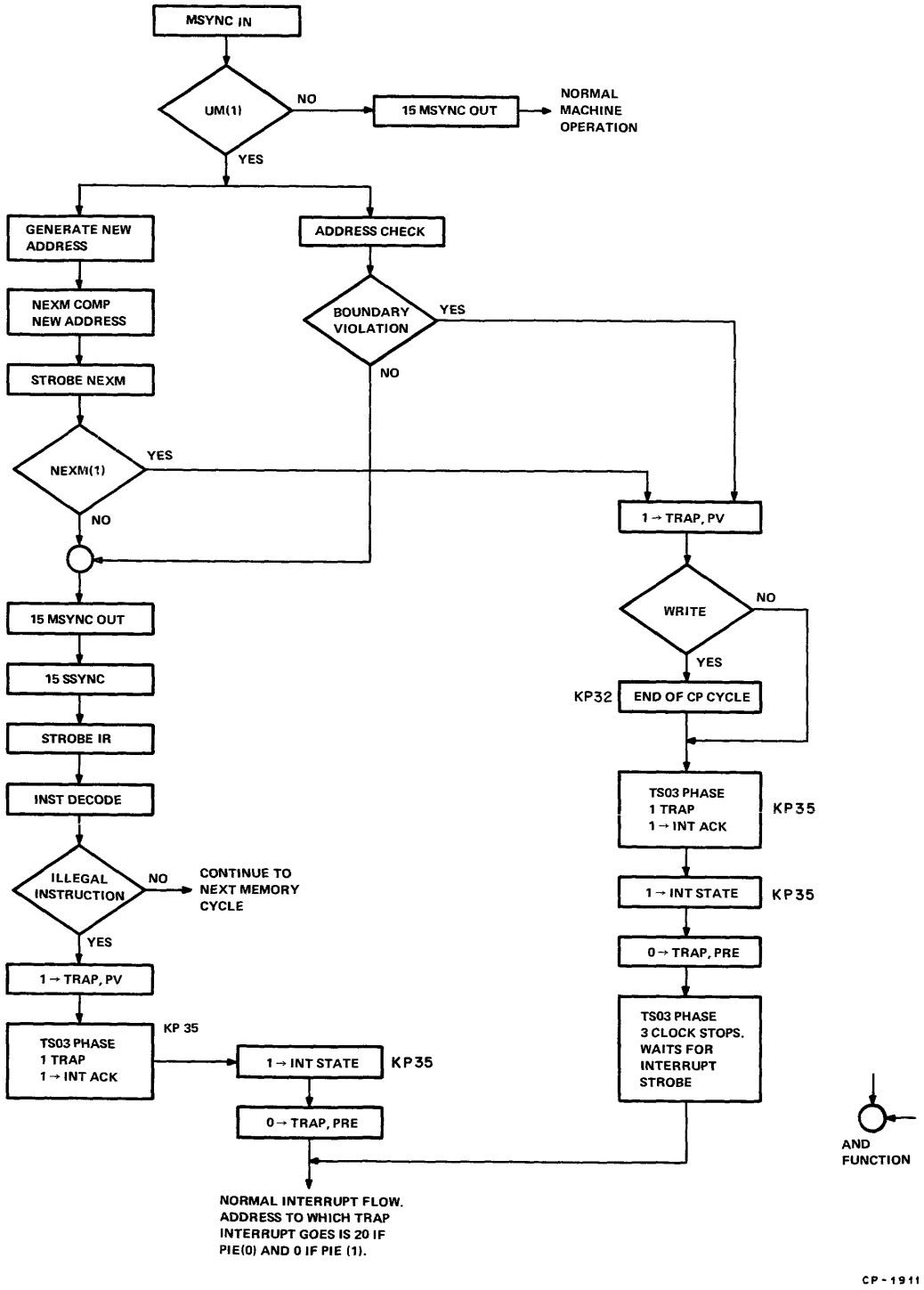
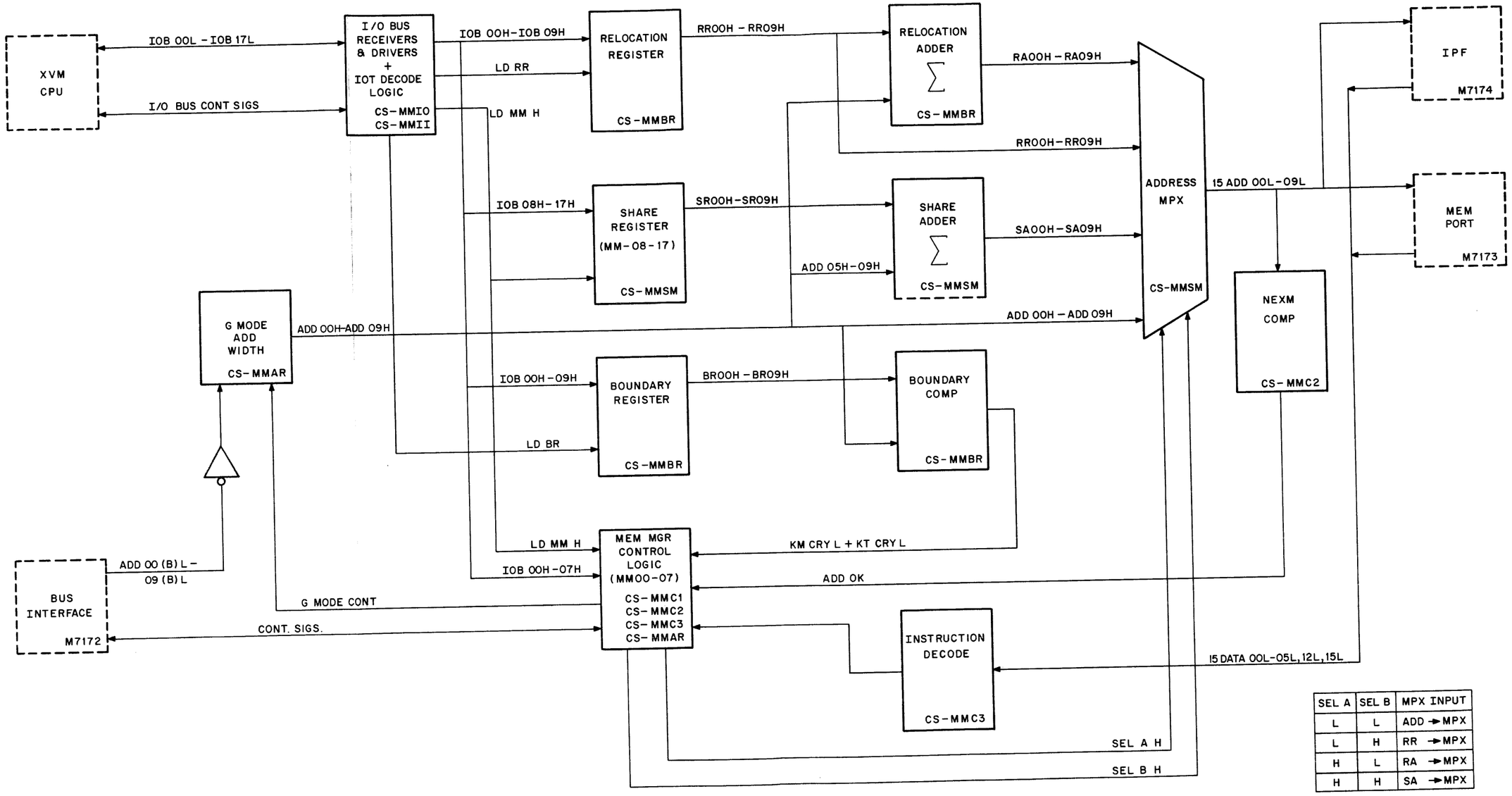


Figure 2-10 Memory Relocate Flow Diagram (M7175)



SEL A	SEL B	MPX INPUT
L	L	ADD → MPX
L	H	RR → MPX
H	L	RA → MPX
H	H	SA → MPX

NOTE:

The CS- designation within a functional block is the Circuit Schematic reference for that block.

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Figure 2-11 M7175 Memory Management Functional Diagram

A CAL, PI, or API will cause User Mode to be turned off and no violation will occur. The CAL and PI will save the state of User Mode. On an API break, the instruction in the break address must be a JMS, JMS I, or CAL if the state of the User Mode is to be saved.

Protect mode IOTs are as follows:

MPSK	701701	Skip on memory protect violation flag.
MPCV	701702	Clear memory protection flag.
MPLD	701704	Load boundary register.
MPSNE	701741	Skip on nonexistent memory flag.
MPEU	701742	Enter User Mode.
MPCNE	701744	Clear nonexistent memory flag.
LDMM	700024	Load the MM register.
ORMM	700022	OR the MM into the AC.

2.6.2 Relocation Mode

When the Relocation Mode is selected, the operating system's monitor maintains control over the M7175 Memory Management module by issuing IOTs and data via the I/O bus. The data is directed to the M7175 (Figure 2-11) relocation register, the share register, and the Memory Management (MM) register. The Memory Management register also contains the major control functions for the M7175 module. Figure 2-11 shows the bit assignments for the MM register. The instruction and boundary checking discussed under the Protect Mode (Paragraph 2.6.1) are performed in the Relocation Mode. Address modification and checking is performed by the various registers when the M7175 module is in User Mode. When the M7175 is in Monitor Mode (Executive) no address modification or instruction checking is performed. Four different addresses can be issued, depending on the incoming address and the various control states within the M7175 module. In addition, the address width may be modified.

2.6.2.1 Address Width – G Mode is a feature that allows the M7175 to modify the indirect address width; that is, to truncate either one or two of the most significant bits of the incoming address. This is used to control the addressing range of indirect references through the M7175 Memory Management module. The address width selection for G Mode is as follows:

0 Pass 18 bits of address through the M7175 module (normal mode). CPU does 15 bit defers.

1 Pass the lower 16 bits of address through the M7175 module. CPU does 18 bit defers.

2 Pass 18 bits of address through the M7175 module. CPU does 18 bit defers.

3 Pass the lower 17 bits of address through the M7175 module. CPU does 18 bit defers.

NOTE

In G Mode 1, 2, or 3, PC 0–2 will be stored during a JMS rather than L, BM, or UM bits. G1 and G0 of the MM register are used to select the mode.

2.6.2.2 Address Relocation – A normal relocation is provided by the M7175 relocation register and adder where a user's program is relocated by a factor loaded into the relocation register. In addition, the user's program addresses are checked against the boundary register to determine that the user has not violated the upper limit of his address space. Note that the boundary register function is the opposite of that in the Protect Mode; that is, a violation occurs when an address exceeds the boundary.

The Share Mode may be implemented if selected in the Memory Management (MM) register. When selected, addresses in a specified range (Table 2-1), are relocated by the share register and share adder and not the relocation register. Share addressing is not allowed in the Protect Mode.

Table 2-1
Share Mode Address Range

GM 1,0	Indirect Address Width	Share Addresses ISAS + ESAS = .5K SLR = 0	Share Addresses ISAS + ESAS = 1K SLR = 1	Share Addresses ISAS + ESAS = 4K SLR = 2	Share Addresses ISAS + ESAS = 8K SLR = 3
0	Normal Addressing 15 bits (32K)	ISAS 60000 - 60377 ESAS 60400 - 60777	ISAS 60000 - 60377 ESAS 60400 - 61777	ISAS 60000 - 60377 ESAS 60400 - 67777	ISAS 60000 - 60377 ESAS 60400 - 77777
1	Wide Addressing 16 bits (64K)	ISAS 160000 - 160377 ESAS 160400 - 160777	ISAS 160000 - 160377 ESAS 160400 - 161777	ISAS 160000 - 160377 ESAS 160400 - 167777	ISAS 160000 - 160377 ESAS 160400 - 177777
2	Wide Addressing 18 bits (256K)	ISAS 760000 - 760377 ESAS 760400 - 760777	ISAS 760000 - 760377 ESAS 760400 - 761777	ISAS 760000 - 760377 ESAS 760400 - 767777	ISAS 760000 - 760377 ESAS 760400 - 777777
3	Wide Addressing 17 bits (128K)	ISAS 360000 - 360377 ESAS 360400 - 360777	ISAS 360000 - 360377 ESAS 360400 - 361777	ISAS 360000 - 360377 ESAS 360400 - 367777	ISAS 360000 - 360377 ESAS 360400 - 377777

Normal relocation, share relocation, and boundary comparisons occur in parallel with each other on any address entering the M7175 module.

Address decoding, plus the condition of various bits in the Memory Management (MM) register (Figure 2-13),/ determine which of the four possible addresses is passed to the M7173 Memory Port module. When this determination has been made, the M7175 address multiplexer (Figure 2-11) is driven by the appropriate select lines (SEL A H or SEL B H) and the relocated address (RA 00 – RA 09), the share address (SA 00 – SA 09), the incoming address (ADD 00 – ADD 09), or the contents of the relocation register is placed on the XM15 internal bus. Each of these addresses serves a specific purpose. The four types of address are:

1. Relocated addresses
2. Shared addresses
3. The contents of the relocation register
4. The unmodified address.

2.6.2.3 Address Generation – The Relocated Address (RA) is the normal relocation for user programs.

SA addresses are addresses that fall within the External Shared Address Space (ESAS) and are relocated by the share register. The ESAS is a virtual address space beginning immediately above the Internal Shared Address Space (ISAS) and continuing to a length specified by the Segment Length Register (SLR). Note that the length set in the SLR = ISAS + ESAS. In physical memory the ESAS begins at a location specified by the contents of the Share Address Register (SR) + 256 and ends according to the SLR. Note that ESAS may be internal or external to the users area. Figure 2-12 represents a typical core map produced when share and normal relocation are used in conjunction with each other. Here the user's program is normally relocated unless a reference is made to the shared addresses (ESAS or ISAS).

The third address is the contents of the Relocation Register (RR) which is not passed through the relocation adder (Figure 2-11). This address is used in conjunction with share addressing for a subset of addresses contained in the shared address range; this subset is called ISAS. ISAS is a virtual address space, the beginning of which is defined by bits G0 and G1 of the MM register (Figure 2-13) and continuing to a length of 256 locations. In physical memory, ISAS begins at the location specified by the relocation register and is 256 locations long.

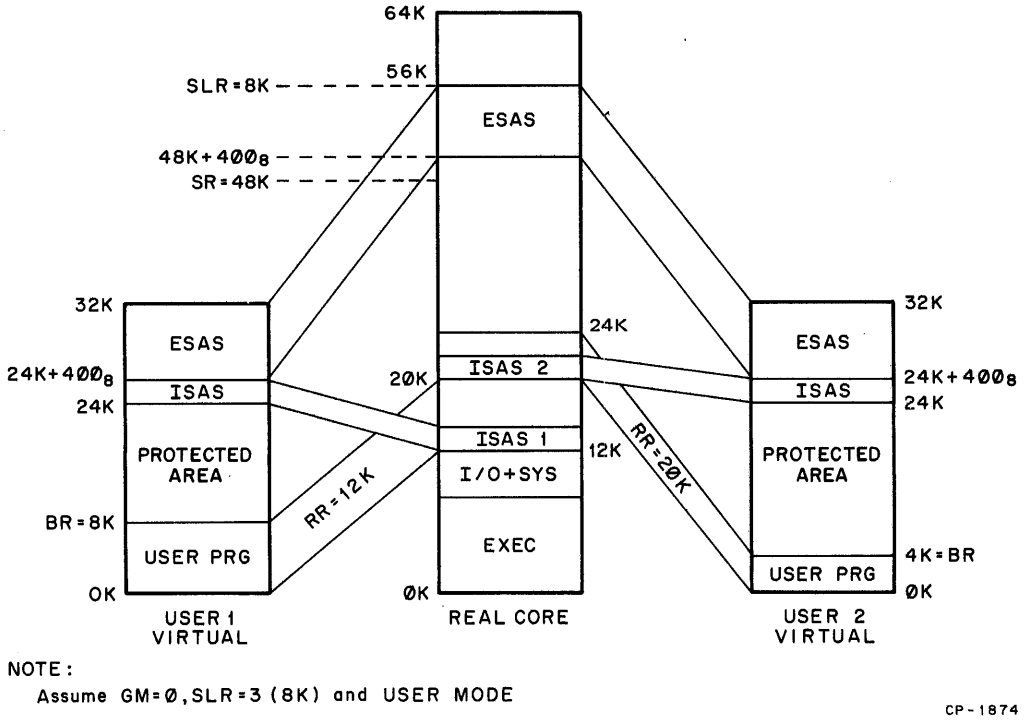


Figure 2-12 Typical Core Map

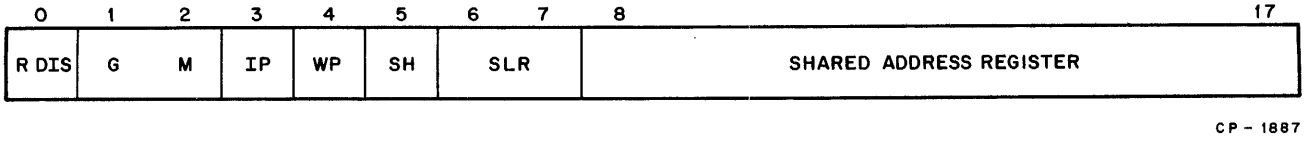


Figure 2-13 M7175 Memory Management (MM) Register Format

The unmodified address (ADD) is used by I/O or whenever the XVM System is in the Monitor Mode.

When the M7175 address multiplexer (Figure 2-11) is properly selected and the address is driven onto the XM15 internal bus, the Nonexistent Memory (NEXM) comparator examines the address to ensure that the address has not exceeded the amount of memory available. The address is then passed to the M7173 Memory Port. The port then arbitrates the request and allows access to memory.

2.6.2.4 Illegal Instructions – When data is returned to the M7175 module via the Memory Port, the M7175 module examines the instruction code bits, along with two other key bits of the returning instruction, to determine whether the instruction is legal. In User Mode, IOTs, Execute of an Execute, and HALT or OAS are not normally permitted. The detection of any of these instructions causes the M7175 module to raise a protect violation flag and signal the XVM CPU that a violation has occurred. This causes a trap in the CPU. If the instruction is not a protected instruction, the data is processed without the trap and the next request is processed through the M7175 Memory Management module.

2.6.2.5 Interrupts – A CAL, PI, or API will cause User Mode and the G and Share Modes to be turned off and no violation will occur. The CAL and PI will save the state of the User Mode prior to clearing the UM flip-flop. On an API break, if the state of User Mode is to be saved, the break address must contain a JMS, JMS I, or a CAL. If User Mode is on and the program tries to address nonexistent memory, a trap occurs. The NEXM flag gets set, and the computer restarts in a CAL or PI, just like any other violation. If User Mode is off and the program tries to address nonexistent memory, the computer hangs up and the NEXM flag gets set.

Relocate mode IOTs are as follows:

MPSK	701701	Skip on memory protect violation flag.
MPCV	701702	Clear memory protect violation flag.
MPLD	701704	Load Boundary register.
MPSNE	701741	Skip on nonexistent memory flag.
MPEU	701742	Enter User Mode.
MPCNE	701744	Clear nonexistent memory flag.
MPLR	701724	Load relocation register.
ORMM	700022	OR the MM register into the AC.
LDMM	700024	Load the MM from the AC.

2.6.3 Memory Management (MM) Register

The MM register contains mode control bits, the Share Address Register (SR), and the Segment Length Register (SLR). The MM register is read to the AC by IOT 700022 and is loaded from the AC by IOT 700024. MM register bit assignments are shown in Figure 2-13 and are described as follows.

R DIS – Relocate Disable (Bit 0)

When set, inhibits relocation and all protect violations (except NEXM) while in User Mode. This allows the use of G Mode without the protection or relocation features. When bit 0 is clear, normal relocation and protection occur, except as determined by Share Mode and IOT Enable.

GM – G Mode (Bits 1, 2)

The G Mode is entered whenever the system is in User Mode and the G0, G1 bits (MM bits 1 and 2) are set to binary 1, 2, or 3. The MM signals the CPU to pass 18 bits of any defer address and causes PC bits 0–2 to be stored during a JMS instruction rather than L, BM and UM. While in G Mode, G0, G1 select the address width through M7175.

G0, G1 =

00 – normal mode, not G Mode
01 – G Mode with 16 bit defers
02 – G Mode with 18 bit defers
03 – G Mode with 17 bit defers

G0, G1 bits also determine the virtual position of the Shared Address Space (SAS).

IP - IOT Permit (Bit 3)
Bit 3 of the MM, when set, allows execution of IOTs while in User Mode.

WP - Write Protect (Bit 4)
Bit 4 of the MM, when set, write protects the External Shared Address Space (ESAS). A protect violation and trap occurs if an ESAS write is attempted.

SH - Share (Bit 5)
Bit 5 of the MM enables Share Mode when set.

SLR - Segment Length Register (Bits 6, 7)
These bits determine the size of the external shared segments. Always equals ISAS + ESAS.

Bits 6, 7

= 0 = 1000_8 (512_{10}) Locations
= 1 = 2000_8 (1024_{10}) Locations
= 2 = 10000_8 (4096_{10}) Locations
= 3 = 20000_8 (8192_{10}) Locations

Shared Address Register - SA (Bits 8–17)
The Shared Address Register (bits 8–17 of the MM) contains the relocation factor for the share address. It points to the position of ESAS - 256 in core.

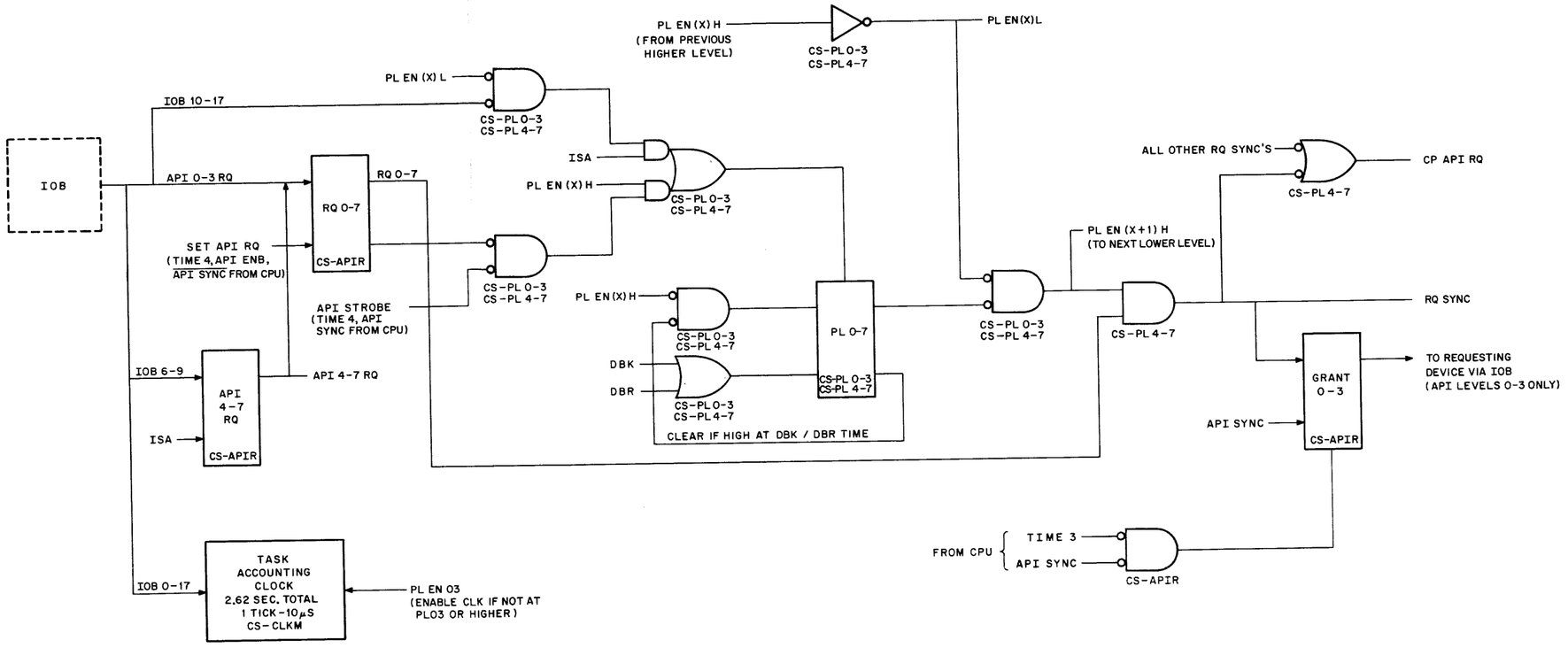
2.7 AUTOMATIC PRIORITY INTERRUPT (API M7176)

The M7176 Automatic Priority Interrupt module contains all the circuitry necessary to receive, synchronize, and arbitrate four different levels of vectored hardware interrupts. In addition, four levels of software-initiated interrupts can also be handled by the M7176. Figure 2-14 shows a simplified logic diagram for one of the M7176 interrupt levels. With minor exceptions, the M7176 discussion which follows applies to all interrupt levels.

2.7.1 Hardware Requests

The hardware automatic priority interrupt sequence is inititated by a device on the I/O Bus (IOB) on one of four levels (levels 0, 1, 2, or 3). An API request (API 0–3 RQ) is received by the M7176 and is presented to a series of request flip-flops (RQ 0–7). At some future point in time, the I/O Processor timing chain produces TIME 4. During TIME 4, with API ENB and API SYNC, SET API REQ is produced, strobing the RQ flip-flops. All interrupt request levels currently making a request are loaded into the RQ flip-flops at this time.

The output of the RQ flip-flops is passed through to the output circuitry of the M7176 and is used to generate Request Sync (RQ SYNC). RQ SYNC, along with any other pending request signals, generates CP API RQ. CP API RQ is passed back to the Central Processor where it is synchronized with the CP timing chain. In addition, RQ SYNC is presented to the M7176 Grant flip-flops (GRANT 0–3) for hardware interrupts on levels 0, 1, 2, and 3. When API SYNC returns from the Central Processor, the corresponding Grant flip-flop sets, thus producing an API GRANT signal to the device on the IOB making the request. In the device, EN A sets to allow the device to send its unique entry address to the IPU via the I/O Bus. Table 2-2 lists the channel number, the assigned priority level, and the unique entry addresses for the XVM API system.



NOTE:
The CS- designation within a functional block is the Circuit Schematic reference for that block.

CP-1881

Figure 2-14 M7176 Automatic Priority Interrupt Functional Diagram

Table 2-2
Standard API Channel/Priority Assignments

Octal Channel Number	Device Name	Device Mnemonic	Priority Level Assigned	Unique Entry Point Octal Address
0	Software Priority	---	4	40
1	Software Priority	---	5	41
2	Software Priority	---	6	42
3	Software Priority	---	7	43
4	DECtape	TC02,TC15	1	44
5	Magtape	TC59	1	45
6	Not assigned		1	46
7	Not assigned		1	47
10	High Speed Tape Reader	PC15	2	50
11	Real Time Clock	KW15	3	51
12	Power Fail	KF15	0	52
13	Not Assigned			53
14	Display Control	VP15 or VT15	2	54
15	Card Reader	CR03B/CR15	2	55
16	Line Printer Control	LP15C or F	3	56
17	A/D Conv.	AD15	0	57
20	Inter Processor Buffer	DB09	3	60
21				61
22	637 Data Phone	DP09	2	62
23	DEC Disk Control	RF15	1	63
24	Disk Pack Control	RP15	1	64
25	Plotter	XY 15	2	65
26	Not Assigned			66
27	Not Assigned			67
30	Line Scanner	DC01		70
31	Digital Controller	UDC15/DC01		71
32	Analog Converter	ADC15/DC01		72
33	Writing Tablet	VW01/DC01		73
34	Teletype Keyboard	LT19/LT15A/DC01	3	74
35	Teletype Printer	LT19/LT15A/DC01	3	75
36	DECtape (DCH channel 36)	TC02/TC15*/DC01	1	76
37	Dataphone	DP09*/DC01	2	77

NOTE: The above table channel assignments should remain fixed for software compatibility, but the suggested priority levels may be changed at the discretion of the user.

*Channel allocated for system with more than one of the above options.

In addition to clocking the Grant flip-flops, API SYNC is used internal to M7176, along with TIME 4, to produce API STROBE. Gated with the previously set RQ flip-flops, API STROBE is passed to an AND/NOR gate and direct-sets a Priority Level (PL) flip-flop if the Priority Level Enable [PL EN (X) H] from the previous higher level is present (no higher PL is set). Once a PL level flip-flop is set, the flip-flop drops RQ SYNC. The PL remains set until the software issues a Debreak (DBK) or a Debreak Restore (DBR) instruction. DBK or DBR instructions clock the PL flip-flops. This is done in such a manner that if the PL flip-flop is the highest currently set priority level it will be cleared. Note that more than one priority level can be set at any given time and only the highest PL flip-flop will be cleared by a DBK or DBR instruction. This is accomplished by gating the data input to the PL flip-flops and prevents clearing the current request level if a higher level PL flip-flop is set. The state of the PL flip-flops can be read by the software via an IOT. The complete API flow is diagramed in Figure 2-15.

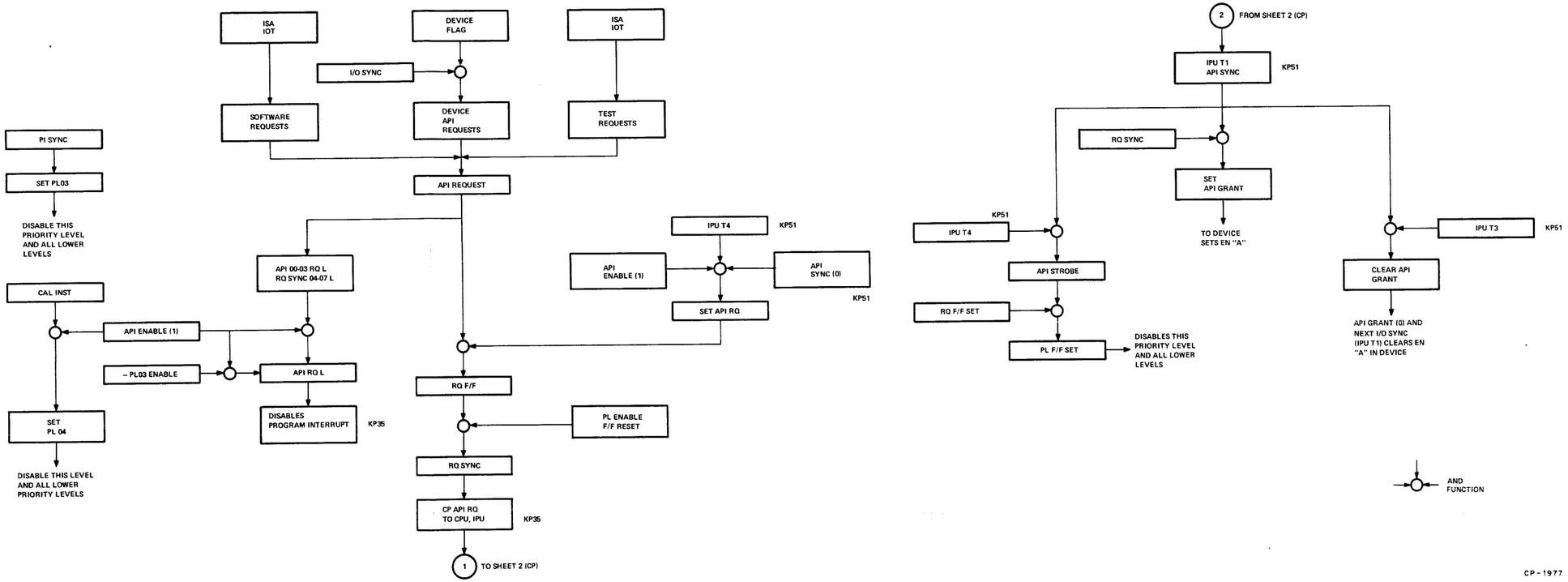


Figure 2-15 API Flow Diagram (M7176)
(Sheet 1 of 2)

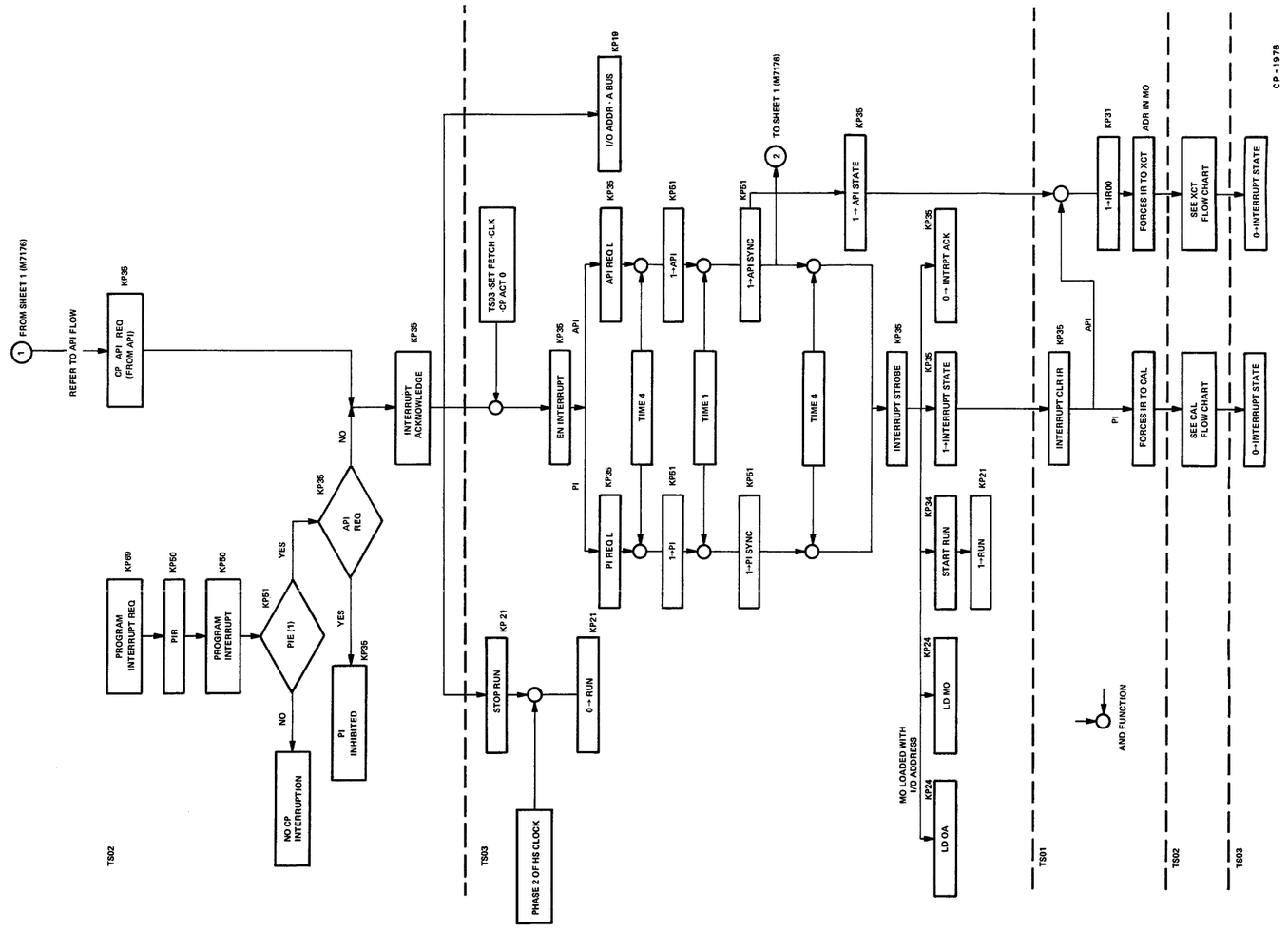


Figure 2-15 API Flow Diagram (M7176)
(Sheet 2 of 2)

2.7.2 Software Requests

Software API requests are handled in a manner similar to hardware requests. Software requests are initiated when the software issues the Initiate Selected Activity (ISA) IOT. This causes IOB 6–9 to be loaded into the M7176 API 4–7 RQ flip-flops. The output of these flip-flops is processed in a manner similar to API 0–3 RQ hardware requests as discussed earlier. Note that software requests on levels 4–7 are of lower priority than the hardware requests, and once set, cannot be cleared by an ISA instruction.

The ISA IOT also allows the software to directly set priority levels. This is accomplished by issuing ISA and taking the state of IOB 10–17 [conditioned by PL EN (X) L] and direct setting the PL flip-flop. This has the effect of locking out all lower priorities, but does not cause an API break. The lower PLs will be released when the software executes a DBK or DBR. Note that in the case just presented grants will not be asserted on the IOB because there is no I/O device requesting API service.

2.7.3 Test Requests and Special API Requests

For diagnostic purposes, the M7176 Automatic Priority Interrupt module contains software-controlled test request flip-flops which are used to exercise the API circuitry. M7176 also contains circuitry for generating API requests for the Real-Time Clock overflows and/or a Power Fail condition.

2.7.4 Task Accounting Clock

One additional function performed by the M7176 API module which is totally unrelated to API requests is the Task Accounting Clock. The clock consists of a 1 MHz free-running oscillator which is divided by 10 to produce 10 μs clock ticks. Total clock capacity of the 18-bit clock register is 2.62 seconds. The Task Accounting Clock is read by an IOT via IOB 0–17. Following the read IOT, the clock runs continuously from zero, except when API levels 0–3 are being processed. The disabling during the processing of these API levels is accomplsihed by monitoring the condition of priority level three enable. The Task Accounting Clock is used by software for various timing purposes and is a read-only clock. Task clock overflow is not prevented or detected; therefore, it must be serviced no less than each 2.62 seconds of run time.

2.8 MEMORY

The XVM System can be equipped with either MF15 or ME15 memory, or both. Memory internal to the XM15 Memory Processor can be MF15 (32K) or ME15 (24K). Additional memory units can be added to the XVM System (external to the XM15) to produce a total memory capacity of 128K. Both memory types may be intermixed in the XVM System, but cannot be intermixed within the same cabinet due to differing power requirements. The MF15 and ME15 are 18-bit, planar, 3-D, coincident-current, random-access core memories.

2.8.1 MF15 Memory

MF15 memory is available in 32K increments. The first 32K increment can be installed into the XM15 Memory Processor box (Figure 2-16); the next two increments (64K) are placed on the rear door of the Central Processor cabinet (Figure 2-17) for a total of 96K. MF15 memory capacity beyond 96K (to a total of 128K) requires an additional cabinet to house the last 32K increment. Figure 2-18 shows the module complement and the MF15 logic panel slot assignments.

2.8.2 ME15 Memory

ME15 memory is available in 8K increments. The first three increments (24K) can be installed into the XM15 Memory Processor box (Figure 2-16); the next six 8K increments (48K) are placed on the rear door of the Central Processor cabinet (Figure 2-17) for a total of 72K. ME15 memory capacity beyond 72K (to a total of 128K) requires an additional cabinet to house the last seven increments (56K). Figure 2-19 shows the module complement and the ME15 logic panel slot assignments.

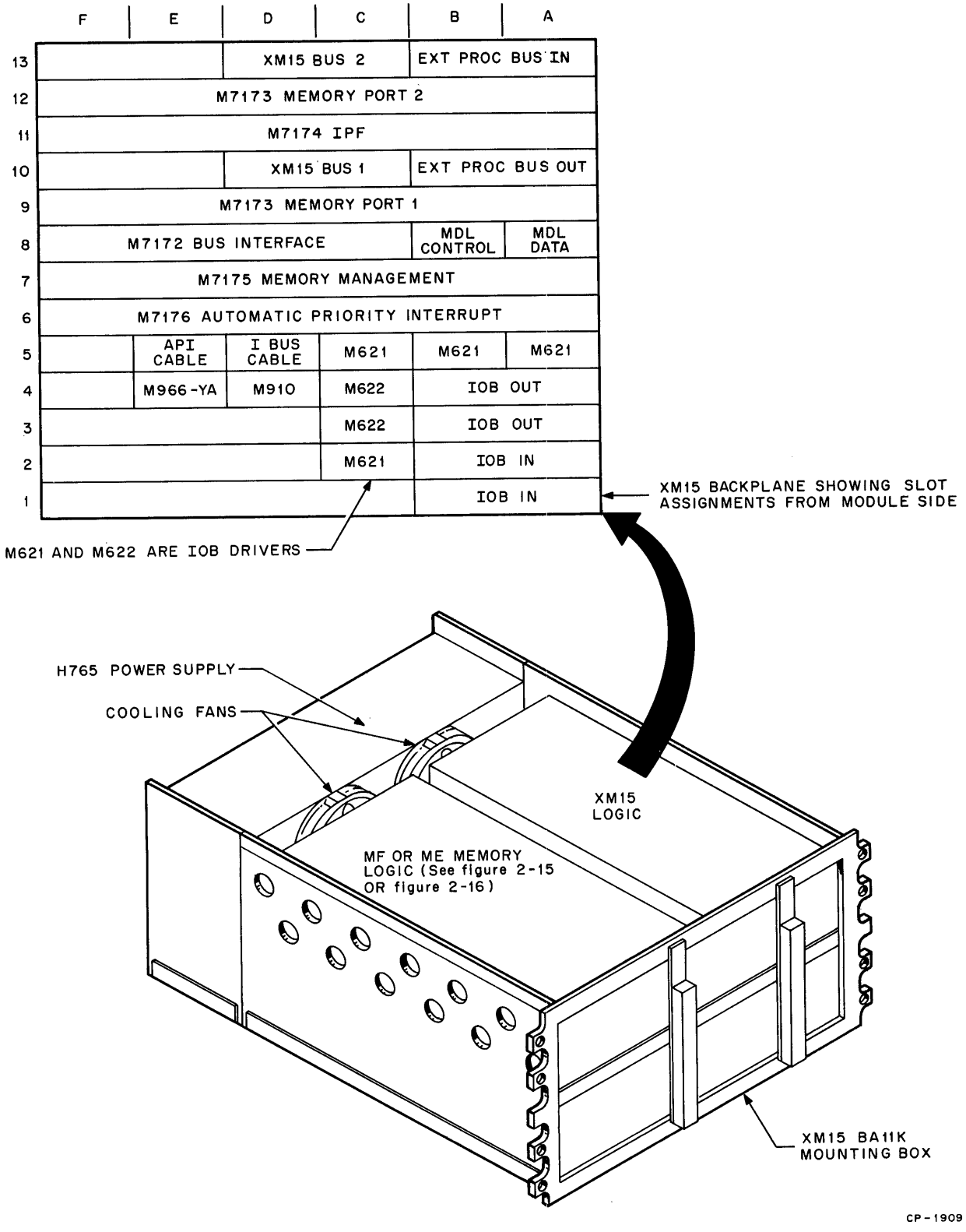


Figure 2-16 XM15 Assigned Module Slots (Module Side)

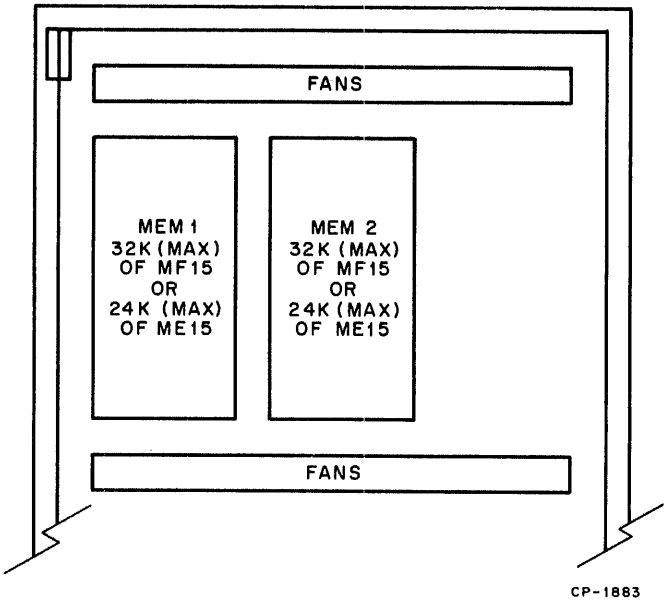


Figure 2-17 ME15 or MF15 Panel Layout - Rear Door of CPU Cabinet

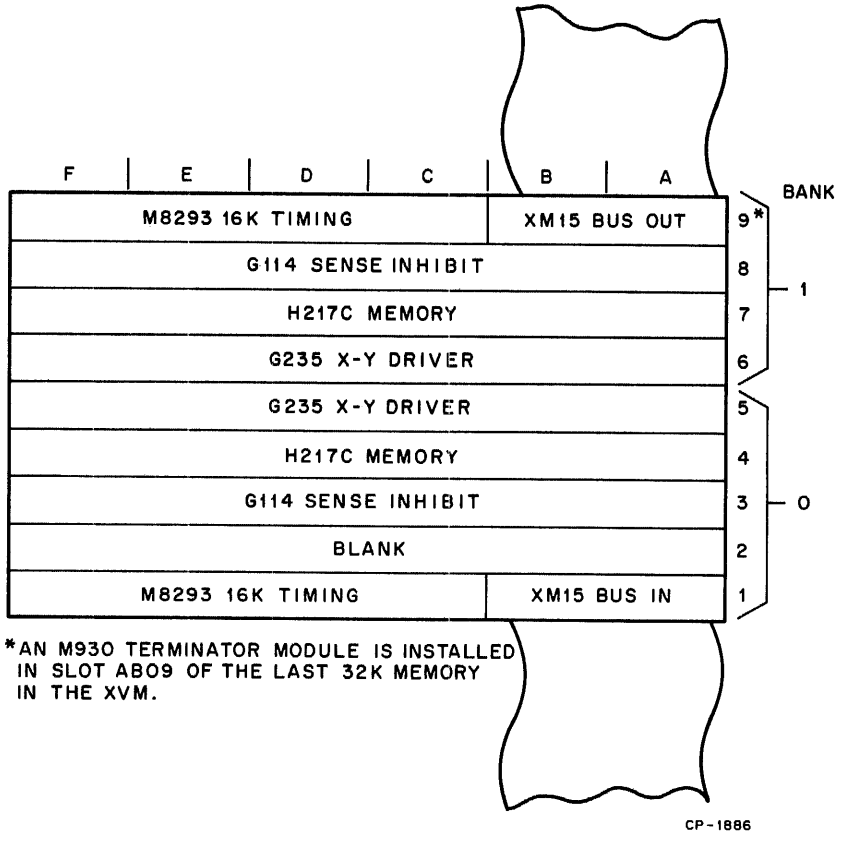


Figure 2-18 MF15 Assigned Module Slots (Module Side)

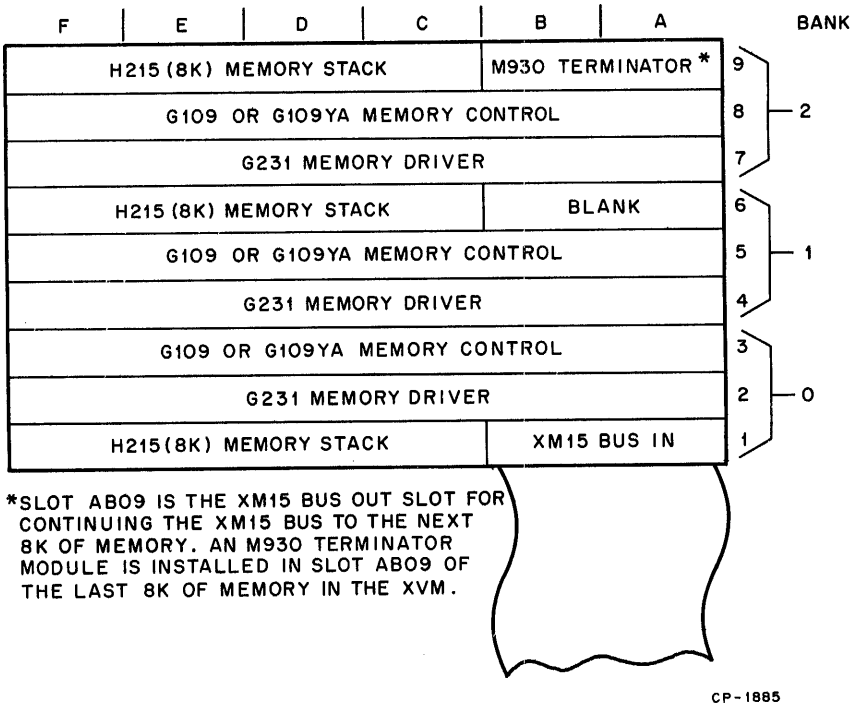


Figure 2-19 ME15 Assigned Module Slots (Module Side)

2.8.3 Memory Intermixing and Address Interleaving

The XM15 Memory Processor will accommodate both MF15 and ME15 memories provided that the following rules are observed:

1. ME and MF memories cannot be mixed on the CPU cabinet rear door due to power supply constraints.

2. Two-Way Address Interleaving

   a. Two-way address interleaving requires two like (two ME or two MF) units of memory. Interleaving selection is made in the memory pairs (Figure 2-20).

   b. Unpaired units of memory are permitted on the same XM15 Bus only when address interleaving is not selected in the unpaired memory.

3. Four-Way Address Interleaving

   a. Four-way address interleaving is accomplished in two steps. First, the M7173 Memory Port module interchanges the LSB+1 address bit with the LSB+1 memory select bit. Then, when the address arrives at the memories, the LSB address bit and the LSB memory unit select bit are interchanged. Thus, for any four sequential addresses the interleaved memories will be selected consecutively.

   b. To obtain four-way interleaving, there must be multiples of four units of like memory on the XM15 Bus (Figure 2-21). Only one additional pair of like memory units may be on the same XM15 Bus, but interleaving cannot be selected in that memory pair. In this case the interleaving occurring in the M7173 Memory Port module causes word pairs to be accessed alternately from one memory unit and then from the other.

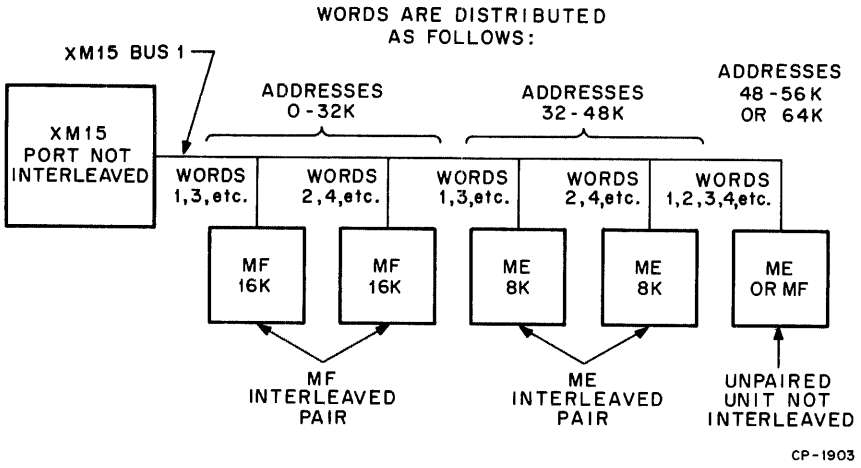


Figure 2-20 Two-Way Interleaving

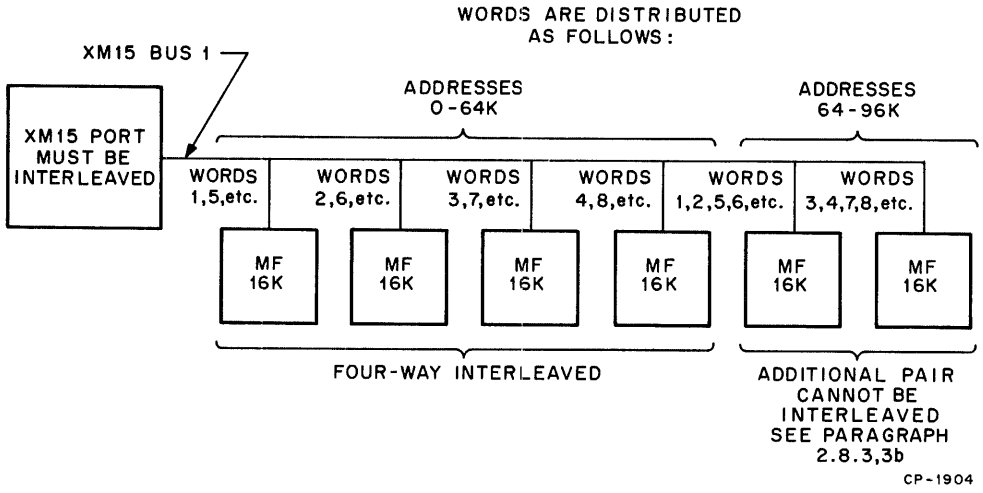


Figure 2-21 Four-Way Interleaving

4. Block Mode

   a. The memories in a dual port (two M7173 modules) XM15 may be selected in Block Mode. If Block Mode is chosen, the memory must be divided between the two XM15 Buses. The division can occur at the 8K, 16K, 32K, or 64K boundary. The low block (M7173 Memory Port 1 on the XM15 Bus) must have an equal or greater amount of memory than the high block (M7173 Memory Port 2 on the XM15 Bus) (Figure 2-22).

   b. Two- or four-way interleaving on each XM15 Bus is permitted with Block Mode, subject to 1, 2, and 3 above.

   c. Two-by-two-way interleaving is not possible, except when LSB Block Mode is selected (see 5 below).

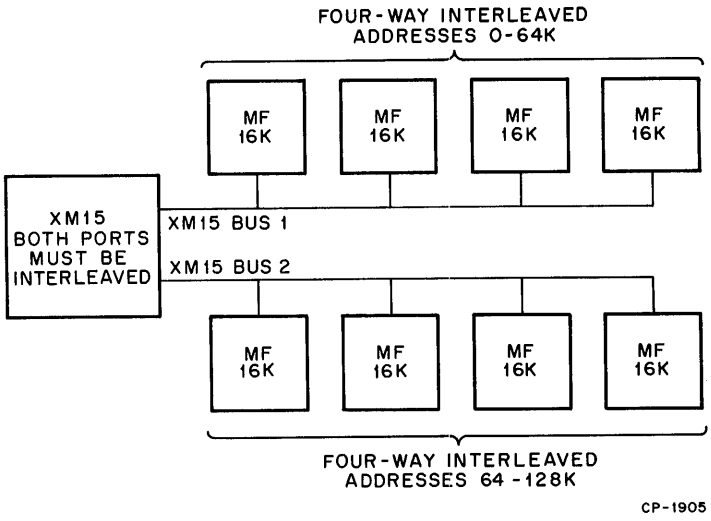


Figure 2-22 Four-Way Interleaving - Block Mode

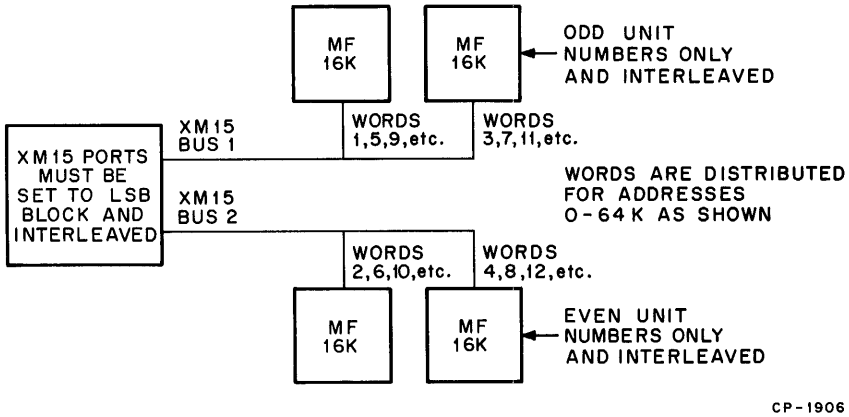


Figure 2-23 Two-By-Two-Way Interleaving

5. Two-by-two-way interleaving is a combination of LSB Block Mode and four-way interleaving, however, the division of memory is not high and low block, but is a division into odd and even memory addresses. The M7173 Memory Ports will be alternately selected for sequential addresses and the memories on each XM15 Bus will also be alternately selected. The mode requires that even address units of memory be placed on M7173 Memory Port 1 on the XM15 Bus and the odd on port 2. Four-way address interleaving must be selected (Figure 2-23).

6. The XM15 Bus can support eight bus loads. The total bus (ME and/or MF) load equals the sum of the memory units and any external XM15 Memory Processors.

SECTION 2 - MF15 CORE MEMORY

2.9 GENERAL DESCRIPTION

The MF15 is an 18-bit, planar, 3-D, coincident current, random access core memory which is available for the XVM System in 32K increments, up to a total of 128K. The MF15 is supplied with a cooling enclosure (for rear door mounting), and the necessary timing, sense inhibit, and driver modules.

2.9.1 MF15 Physical Description

The MF15 core memory (32K) supplied with the XM15 Memory Processor contains the following modules (Figures 2-16 and 2-18):

Two M8293 16K Timing modules
Two G114 Sense Inhibit modules
Two H217C (16K) Memory stacks
Two G235 X-Y Driver modules
One M930 Terminator

These modules are plugged into a logic panel adjacent to the XM15 Memory Processor logic panel and receive power and cooling from the XM15 mounting box.

When the XM15 Memory Processor is expanded to 64K or 96K of memory, the additional 32K or 64K of MF15 memory is placed on the rear door of the XVM Central Processor (Figures 2-17 and 2-18). The additional MF15 memory includes an enclosure with fans at top and bottom for cooling, and one or two logic panels (depending on the amount of memory). Each logic panel is six module slots high and nine module slots wide. MF15 modules supplied with the added 32K (double the amount for 64K) are the same as those supplied (except for the M930) with the XM15 (see previous paragraph). The M930 terminator is not supplied with add-on memory units. The M930 becomes available from the MF15 contained within the XM15 mounting box. The M930 terminator is plugged into slot AB09 (Figure 2-18) of the last 32K increment of memory (memory 1 or memory 2 in Figure 2-17) on the rear door mounting enclosure logic panel.

Memory expansion beyond 96K requires an additional cabinet with one or two BA11-K mounting boxes to house the added memory units. XM15 memory can be expanded up to 128K of MF15. MF15 memory for each BA11-K mounting box includes the same module complement (except for the M930 terminator) as supplied with the XM15. Each BA11-K is also supplied with an H765 power supply to power the MF15 memory units and fans to provide proper memory cooling.

2.9.2 MF15 Module Descriptions

A capsule description of each of the MF15 modules is as follows:

M8293 16K Timing-Hex Height by 8-1/2 Inches Wide.
The M8293 contains the control and address portion of the XM15 Bus interface, device selection, power monitor, read-write-inhibit control logic, and the memory address latches.

G114 Sense Inhibit-Hex Height by 8-1/2 Inches Wide.
The G114 contains the data portion of the XM15 Bus interface, the data register, timing buffers, inhibit drivers, sense amplifiers and threshold circuits.

G235 X-Y Driver-Hex Height by 8-1/2 Inches Wide.
The G235 contains the decoders, X-Y drivers and switches, associated timing and control for the X-Y drivers, sense strobe control, bias source generator, and current sources.

H217-C Memory
The H217-C memory stack provides core storage for 16,384 18-bit words. The H217-C is quad-height by 8-1/2 inches wide.

M930 Terminator
The M930 is a resistive terminator used to properly terminate the memory bus. Only one M930 terminator is required.

2.9.3 MF15 Specifications
The general MF15 core memory specifications are listed in Table 2-3.

2.9.4 Functional Description
The MF15 memory is a read/write, random access, coincident current, magnetic core type with a cycle time of 1040 ns when used with a basic XM15. It is organized in a 3-D, 3-wire, planar configuration. Word length is 18 bits. The major functional units of the memory are briefly described in the following paragraphs. Figure 2-24 shows the composition and interfacing of an MF15 that consists of one stack (16K) of memory.

2.9.4.1 M8293 Timing Module – The 16K Timing module (M8293) contains the control and address portion of the XM15 Bus interface, device selection, power monitor, read-write-inhibit control logic, and the memory address latches.

a. XM15 Bus Interface – The XM15 Bus interface accepts address and control information from the XM15 Bus. The address information is distributed to the device selector and the address latches. The control signals are supplied to the read, write, and inhibit control logic to initiate the read or write currents in memory. The control signals are BUS C00 and BUS C01 and specifY the type of data transfer (read, write, read/pause/write). If a byte operation is specified, MEM A00L is examined and specifies the appropriate byte.

b. Device Selection – The device selection logic compares the XM15 Bus address with a prewired jumper configuration. If the address compares, a memory cycle is initiated on the receipt of MSYN. If the address does not compare with the jumper address, the XM15 Bus has addressed some other device and no memorY cycle is initiated.

c. Read-Write-Inhibit Control Logic – The read-write-inhibit control logic operates the timing and control signals to turn on the read, write, and inhibit currents in memory. This is accomplished by propagating a voltage pulse through delay lines and setting the resetting flip-flops. The logic also provides clocking and clearing controls for the data register and controls the time at which the data and SSYN are placed on or taken off the XM15 Bus. In addition, a locking function is provided to lock the address and control information into address latches for use during the memory cycle.

d. Address Latches – The address latch logic consists of 7475 quad latches which store the address received from the XM15 Bus for the device selector and stack address decoding circuits. When memory is not busy, the latches are left open and the output merely follows the input. When memory is busy, the output is latched to its previous state. This preserves the address during a memory cycle so that the processor can process other devices without being delayed by the memory.

e. Power Monitor and Initialize – The power monitor and initialize logic is initiated as a result of BUS INIT or DC LO from the XM15 Bus. Both conditions indicate that further memory operations are to be discontinued. A 2 μs delay is provided to allow memory to complete the current cycle, then the current sources are inhibited.

Table 2-3
MF15 Memory Specifications

Type:	Magnetic core, read/write, coincident current, random access
Organization:	Planar, 3D, 3-wire
Capacity:	16,384 (16K) words; 18-bit
Maximum Access Time and Cycle Time:	

Bus Mode	Cycle Time	Access Time
READ	1,000 ns	425 ns
WRITE	1,000 ns	125 ns
READ/PAUSE/WRITE	1,100 ns	N/A

X-Y Current Margins:	±6% @ 0° C ±7% @ 25° C ±6% @ 50° C
Voltage Requirements:	+5 V ± 5% with less than 0.2 V ripple +20 V ± 5% with less than ±5% ripple -5 V ± 5% with less than ±5% ripple
Average Current Requirements:	Stand by: +5 V: 5.38 A −5 V: 0.41 A +20 V: 0.5 A Memory Active: +5 V: 6.1 A −5V: 0.51 A +20 V: 3.4 A
Power Dissipation (Worst Case):	M8293 Timing Module ~7 W G235 X-Y Driver Module ~33 W H217C Stack Module ~40 W G114 Sense Inhibit Module ~40 W Total at Maximum Repetition Rate: ~120 W
Environment:	
Ambient Temperature:	0° to 50° C (32° to 122° F)
Relative Humidity:	0–90% (non-condensing)

2.9.4.2 G114 Sense Inhibit Module – The G114 Sense Inhibit module contains the data portion of the XM15 Bus interface, the data register, timing buffers, inhibit drivers, sense amplifiers and threshold circuit.

a. XM15 Bus Interface – The data portion of the XM15 Bus interface consists of type 380 receivers which apply XM15 Bus data to the data input of the data register (information register). This register is clocked under control of the timing signals from the 16K Timing module. Also, the XM15 Bus interface supplies data from the data register to the XM15 Bus via 8881 bus drivers under control of these timing signals.

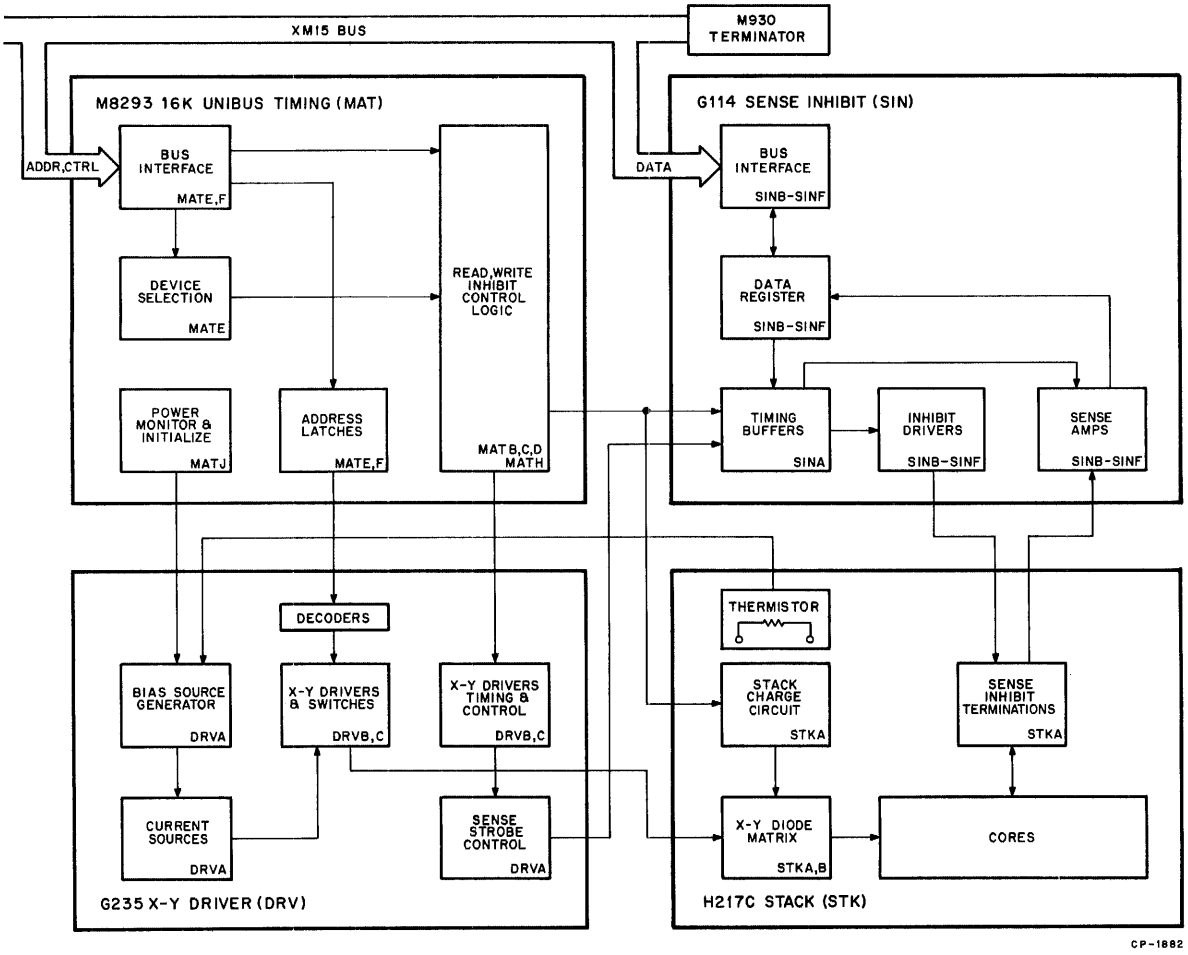


Figure 2-24 MF15 Simplified Block Diagram

b. Data Register – The data register is an 18-bit flip-flop register used to store the contents of a word after it is destructively read from memory; the same word can then be written back into memory (restored) when in the read mode. The register is also used to accept data from the XM15 Bus lines to accommodate the loading of incoming data into the core memory during the write or read/pause/write cycles.

c. Timing Buffers – The timing buffers are used to buffer the timing signals between the timing and control board and the G114 Sense Inhibit module.

d. Inhibit Drivers – Each bit mat contains a single inhibit/sense line that passes through all cores on the mat. A bit mat is a core array of 16,384 cores associated with a particular bit position in all the words in memory. To write a 0 into a selected bit, an inhibit current is passed through the inhibit/sense line that cancels the write current in the Y line. The core does not switch, so it remains in the 0 state. Cores are left in the 0 state at the end of the read portion of the cycle. With no inhibit current, the currents in the X and Y lines switch the core to the 1 state during write sequences.

e. Sense Amplifiers Threshold – During a read operation, the sense amplifier picks up a voltage induced in the sense/inhibit winding when a core is switched from a 1 to a 0. This signal is detected and amplified by the sense amplifier whose output sets a data register flip-flop to store a 1. In effect, a 1 is read when the core is switched to the 0 state. Cores which were previously set to 0 do not switch and are not affected.

   The threshold circuit provides a reference threshold voltage to the sense amplifiers. In a read operation, if the threshold voltage (17 mV) is exceeded during sense strobe time, the sense amplifier produces an output.

2.9.4.3 G235 X-Y Driver Module – The G235 X-Y Driver module contains the decoders, X and Y drivers and switches, associated timing and control for the X and Y drivers, sense strobe control, bias source generator, and current sources.

a. Decoders – The decoders decode 14 of the 18 bits of the XM15 Bus address. Seven of the 14 address bits are used for X address selection and seven are used for Y address selection. Four of the seven X bits are applied to the X switches and three to the X drivers. The same situation occurs for the Y drivers. The four bits not sent to the decoders are used for decoding device selection and byte operation. The decoded X and Y bits ultimately specify one core out of 16,384 for each bit of an 18-bit word.

b. Switches and Drivers – The switches and drivers direct the flow of current through the magnetic cores to ensure the proper polarity for the desired function. This action is necessary because a single X read/write line is used, a single Y read/write line is used, and the current for a write operation is opposite in polarity to the current required for a read operation. There are separate switches and drivers for the read and write circuits in the selection matrix.

c. Drivers Timing and Control – The drivers timing and control logic receives inputs from the timing and control module and combines the timing signals to derive specific timing pulses and proper timing relationships required by all X-Y drivers and switches as well as current sources.

d. Sense Strobe Control – The sense strobe control is a one-shot multivibrator whose duration can be controlled by an external voltage input. The control determines when the sense amplifiers are examined.

e. Bias Source Generator – The bias source generator is a dc, temperature-compensated, bias current used to control the amplitude of the current from the X and Y current generators and inhibit current sources.

f. Current Sources – X and Y current generators provide the current necessary to change the state of the magnetic cores. The rise time and amplitude of the output-current waveform have been selected to provide optimum switching of the core states and maximum signal-to-noise ratio for a wide range of temperatures.

2.9.4.4 H217-C Memory Stack Module – The H217-C memory stack module contains the ferrite core array, X-Y diode matrices, Sense/inhibit terminations, stack charge circuit, and a thermistor to provide termperature compensation for the bias current.

a. Ferrite Core Array – The core array is contained on the H217-C memory stack module and consists of a planar array of 128 × 128 × 18 mats, or a total of 294,912 cores.

b. X-Y Diode Matrix – The X-Y diode matrix is used in conjunction with the drivers and switches and is used to select one of 128 X lines and one of 128 Y lines.

c. Sense Inhibit Terminations – The sense inhibit terminations terminate the sense inhibit lines in order to minimize tramsmission line reflections. This is necessary in order that the sense amplifiers can sense core switching with minimum distortion.

d. Stack Charge Circuit – The stack charge circuit is used to bias the X and Y drive lines to near ground potential during read time, and to near +20 V during write time. The purpose of this is to back-bias the diodes on the X-Y matrix to prevent loss of drive currents due to charging capacitance through unselected diodes.

2.9.5 MF15 Memory Operations

The MF15 core memory has four basic modes of operation. The main function of the memory is to store data for retrieval at a later time. Data is stored in memory during the write cycle or read from memory during the read cycle. An additional mode, called the read/pause/write cycle, eliminates restore and clear operations when they are not required, thus increasing the overall efficiency of the memory. Byte modes are used by the PDP-11 external processor, which may be part of the XVM System. The XVM Processor does not use byte addressing.

2.9.5.1 Write Cycle (WRT) – The Write Cycle is the memory cycle used by the master device to transfer data into core memory. To ensure that proper data is stored, the XM15 Bus data is first clocked into the data register, then the memory location is cleared by reading the cores (thereby setting them all to 0) before writing in the new data. During a write operation, the memory first performs the read operation to clear the cores and then performs a write cycle to transfer data from the data register into the selected core location. Access time is given in Table 2-3.

2.9.5.2 Read Cycle (RD) – The Read Cycle is a read/restore memory cycle. During this operation, the memory reads the information from the selected core location, transfers it to the XM15 Bus, and then writes the information back into the memory location. This last step is necessary because the core memory is a destructive readout device. During the first (read) part of the cycle, the memory strobes the data into a data register and then gates the data to the XM15 Bus. Then, during the second (write) part of the cycle, the memory restores the data back into the addressed memory location.

2.9.5.3 Read/Pause/Write Cycle (RPW) – Because data is destroyed when reading from a particular memory location, it must be restored. However, sometimes it is not desirable to restore the information immediately after reading because the location is to have new data written into it. In this instance, eliminating the restore operation decreases the memory cycle time by approximately 50 percent. The read/pause/write operation is used for this purpose. The data is read from memory and the restore cycle is inhibited. Because no restore cycle is used, a RPW must always include a write cycle on the same address, or data will be destroyed.

2.9.5.4 Byte Read/Pause/Write and Byte Clear/Write – The byte read/pause/write cycle is similar in function to the (WRT) cycle (Paragraph 2.9.5.1), except that the data is transferred into core memory from the XM15 Bus in byte form rather than as a full word. Actually, an entire word is loaded into the selected memory location, the selected byte is new data from the XM15 Bus and the nonselected byte is restored data from the word previously stored in that memory location.

During the read cycle, the nonselected byte is saved by reading it into the data register while the selected byte is transferred into the data register from the XM15 Bus.

For write cycles, the word is loaded into memory location from the data register. In effect, the memory is read first and then simultaneously performs a restore cycle for the nonselected byte and a write cycle for the selected byte.

Byte clear/write clears (zeros) the selected byte bits in the selected memory locations while performing a write cycle.

If the external processor selects byte addressing, then the following applies:

a. Bit 17 of the 18-bit memory location will be cleared when the high byte (MEM ADD 0 true) is written.

b. Bit 16 of the location will be cleared when the low byte (MEM ADD 0 false) is written.

The high byte is MEM D15-18, the low byte is MEM D07-00. The XVM Processor cannot perform byte addressing, however, byte addressing is used by the PDP-11 external processor when connected to the XM15 Memory Processor.

2.9.6 MF15 Related Literature

Additional information on the MF15 core memory can be found in the *MF15 Core Memory Maintenance Manual, EK-MF15-MM-001*. This manual is available from the nearest Digital Equipment Corporation Sales Office.

SECTION 3 - ME15 CORE MEMORY

2.10 GENERAL DESCRIPTION

The ME15 is an 18-bit, planar, 3-D,coincident current, random access core memory which is available for the XVM System in 8K increments, up to a total of 128K. The ME15 is supplied with a cooling enclosure (included for rear door mounting only), and the necessary timing, sense inhibit, and driver modules.

2.10.1 ME15 Physical Description

The ME15 core memory (24K) supplied with the XM15 Memory Processor contains the following modules (Figures 2-16 and 2-19):

Three G109 or G109-YA Memory Controls
Three G231 Memory Drivers
Three H215 (8K) Memory Stacks
One M930 Terminator

These modules are plugged into a logic panel adjacent to the XM15 Memory Processor logic panel and receive power and cooling from the XM15 mounting box.

When the XM15 Memory Processor is expanded to 72K of memory, an additional 48K of ME15 memory is placed on the rear door of the XVM Central Processor (Figures 2-17 and 2-19). The additional 48K of ME15 memory includes an enclosure with fans at top and bottom for cooling and two logic panels. Power is supplied by H7420 additional regulators mounted in the CPU's H7420 power supply.

Each logic panel is six module slots high and nine module slots wide. ME15 modules supplied for rear door mounting are as follows:

Six G109 or G109-YA Memory Controls
Six G231 Memory Drivers
Six H215 (8K) Memory Stacks

The M930 terminator module is not supplied with add-on memory units. The M930 becomes available from the ME15 memory contained within the XM15 mounting box. The M930 terminator is plugged into slot AB09 of memory two (Figures 2-17 and 2-18) on the rear door mounting enclosure logic panel.

Memory expansion beyond 72K requires an additional cabinet with one or two BA11-K mounting boxes to house the added memory units. Beyond 96K, the second M7173 Memory Port module must be installed in the XM15 Memory Processor (Figure 2-16). ME15 memory for the first additional BA11-K mounting box (48K of ME15) includes:

Two logic panels for the BA11-K
Six G109 or G109-YA Memory Controls
Six G231 Memory Drivers
Six H215 (8K) Memory Stacks

The second additional BA11-K mounting (8K of ME15) includes:

One logic panel for the BA11-K
One G109 or G109-YA Memory Control
One G231 Memory Driver
One H215 (8K) Memory Stack

Each BA11-K mounting box is also supplied with an H765 power supply to power the ME15 memory units and fans to provide proper memory cooling.

2.10.2 ME15 Module Descriptions

A capsule description of each of the ME15 modules is as follows:

G109 Memory Control
Hex height by 8-1/2 inches wide. The G109 contains the control logic, inhibit drivers, sense amplifiers, and an 18-bit data register to service one H215 Memory Stack (8K).

G231 Memory Driver
Hex height by 8-1/2 inches wide. The G231 contains address selection logic, a current generator, and X-Y switches and drivers for one 8K H215 Memory Stack.

H215 Memory Stack
The H215 provides core storage for 8192 18-bit words. The H215 is quad height by 8-1/2 inches wide.

M930 Terminator
The M930 is a resistive terminator used to properly terminate the memory bus. Only one M930 terminator is required for each XM15 Bus.

2.10.3 ME15 Specifications

The general ME15 core memory specifications are listed in Table 2-4.

2.10.4 ME15 Functional Description

The ME15 memory is a read/write, random access, coincident current, magnetic core type with an unopposed cycle time of 950 ns when used with a basic XM15. It is organized in a 3-D, 3-wire, planar configuration. Word length is 18 bits.

The major functional units of the memory are briefly described in the following paragraphs. Figure 2-25 shows the composition and interfacing of an ME15 that consists of one stack (8K) of memory.

2.10.4.1 G109-YA Control Module – The G109-YA Control Module contains the memory control circuits, inhibit drivers, sense amplifiers, data register, device selector, threshold circuit, and –5 V supply.

a. Memory Control Circuits – Control circuits are provided to acknowledge the request from the XM15 module; determine which of the three basic operations (read, write, read/ pause/write) is to be performed; and set up the appropriate timing and control logic to execute the desired read or write operation. The actual read or write operation is selected by the control lines (C00 and C01) from the XM15. The memory control logic also transfers data to and from the XM15 Bus.

b. Inhibit Driver – Each bit mat contains a single inhibit/sense line that passes through all cores on the mat. To write a 0 into a selected bit, an inhibit current is passed through the inhibit/sense line that cancels the write current in the Y line. The core does not switch so it remains in the 0 state. With no inhibit current, the currents in the X and Y lines switch the core to the 1 state.

Table 2-4
ME15 Memory Specifications

Type:	Magnetic core, read/write, coincident current, random access
Organization:	Planar, 3D, 3-wire
Maximum Capacity:	131,072 (128K), 18-bit

Bus Mode	Cycle Time	Access Time
READ	900 ns	400 ns
WRITE	900 ns	200 ns
READ/PAUSE/WRITE	900 ns	N/A

X-Y Current Margins:	±6% @ 0° C ±7% @ 25° C ±6% @ 50° C
Strobe Pulse Margins:	±30 ns @ 0° C ±40 ns @ 25° C ±30 ns @ 50° C
Voltage Requirements:	+5 V ± 5% with less than 0.05 V ripple -15 V ± 5% with less than 0.05 V ripple
Average Current Requirements:	Stand by: +5 V: 2.2 A -15 V: 0.5 A Memory Active: +5 V: 5.4 A -15 V: 6.0 A
Power Dissipation (Worst Case):	G109-YA Control Module: ~60 W G231 Drive Module: ~40 W H214 Stack Module: ~20 W Total at Maximum Repetition Rate: ~140 W
Ambient Temperature:	0° to 50° C (32° to 122° F)
Relative Humidity:	0–90% (non-condensing)

c. Sense Amplifiers - During a read operation, the sense amplifier picks up a voltage induced in the sense/inhibit winding when a core is switched from a 1 to a 0. This signal is detected and amplified by the sense amplifier whose output sets a data register flip-flop to store a 1. In effect, a 1 is read but the core is switched to the 0 state. Cores that were previously set to 0 are not affected.

d. Data Register - The data register is an 18-bit flip-flop register used to store the contents of a word after it is read out of the destructive memory; the same word can then be written back into memory (restored) when in the read cycle. The data register is also used to accept data from the XM15 Bus to accommodate the loading of incoming data into the core memory during a write cycle.

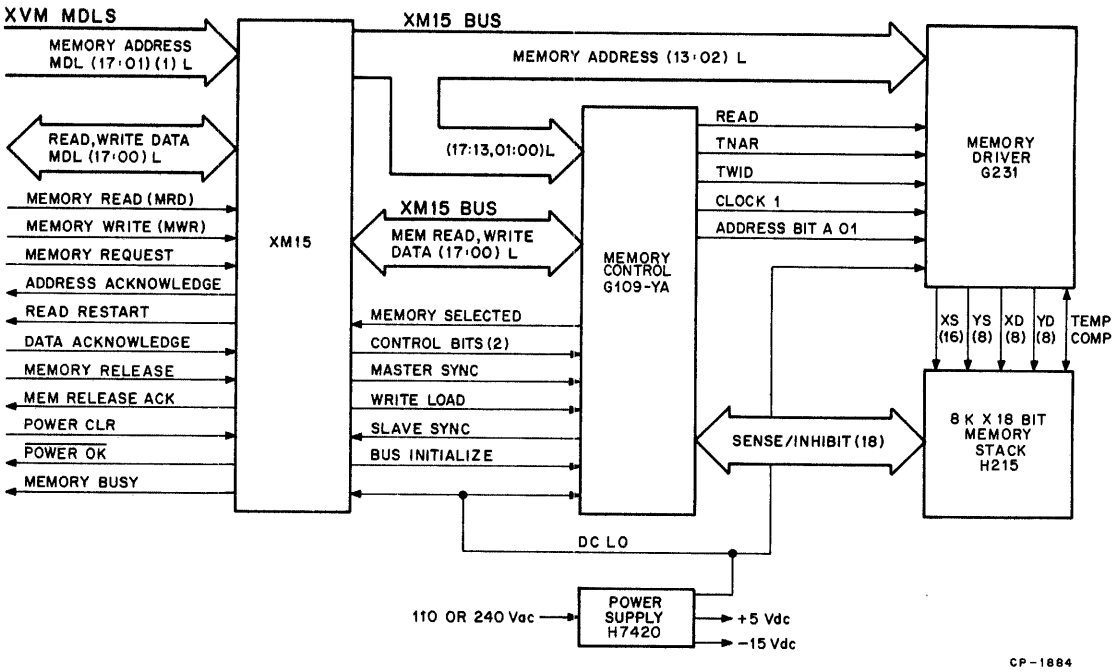


Figure 2-25 Module Interfacing for an 8K ME15

e. Device Selector - The device address is decoded in the device selector to determine if the memory bank has been addressed. BUS A14 L - BUS A17 L are used for device selection. DC LO L, indicating low ac line voltage to the power supply, is another input to this circuit. The memory bank cannot be selected if this signal is asserted.

f. Threshold Circuit and -5 V Supply - The threshold circuit provides a reference threshold voltage to the sense amplifiers. During a read operation, if the threshold voltage (-5.2 V) is exceeded, the sense amplifier produces an output. The -5 V supply provides a negative voltage for the sense amplifiers.

2.10.4.2 G231 Driver Module - The G231 Driver module contains the address selection logic, switches and drivers, current generator, stack discharge circuit, and DC LO protection circuit.

a. Word Address Selection Logic - The core memory receives 13 bits of the 18-bit address output from the XM15. The address is latched and retained if this 8K memory bank is the selected device. This 13-bit portion of the address pinpoints a specific 18-bit word location. The X and Y portion of the address is coded through selection switches and a diode matrix to enable passage of read/write current through the selected X and Y drive lines of the memory. The coincidence of these currents selects the specific memory location.

b. Switches and Drivers - The switches and drivers direct the flow of current through the magnetic cores to ensure the proper polarity for the desired function. This action is necessary because a single read/write line is used, and the current for a write operation is opposite in polarity to current required for a read operation. There are separate switches and drivers for the read and write circuits in the selection matrix.

c. Current Generators – X and Y current generators provide the current necessary to change the state of the magnetic cores. The linear rise time and amplitude of the output current waveform have been selected to provide optimum switching of the core states and maximum signal-to-noise ratio for a wide range of temperatures.

d. Stack Discharge Circuit – The stack discharge circuit maintains the proper stack charge voltage during operation: approximately 0 V during a read operation and approximately 14 V during a write operation.

e. DC LO Protection Circuit – If any dc voltage is out of tolerance, DC LO L is asserted on the XM15 Bus. It is sensed by the DC LO protection circuit, which inhibits the memory operation by opening the –15 V line to the current source. This prevents spurious memory operation.

2.10.4.3 H215 Stack Module – The H215 Stack module contains the ferrite core array and the X-Y diode matrices. The core array consists of 18 mats, each wired in a 128 × 64 matrix. The stack also contains the resistor-thermistor combination to control the X-Y current generator temperature compensation.

2.10.5 ME15 Memory Operations

The ME15 core memory has four basic modes of operation. The main function of the memory is to store data for retrieval at a later time. Data is stored in memory during the write cycle, and retrieved or read from memory during the read cycle. An additional mode, called the read/pause/write cycle eliminates restore and clear operations when they are not required, thus increasing the overall efficiency of the memory. Byte modes are used by the PDP-11 external processor which may be part of the XVM System. The XVM Processor does not use byte addressing.

2.10.5.1 Write Cycle – The write cycle is used by the master device to transfer data into core memory. To ensure that correct data is stored, the addressed location must first be cleared by reading the cores (thereby switching them all to zero) before writing new data. The ME15 first performs a read operation, clearing the 18 cores (one word) at the specified location. Then, a write operation is performed to transfer data from the XM15 Bus to the selected cores.

2.10.5.2 Read Cycle – The read cycle is a read/restore memory cycle. During this operation the memory reads the information from the selected core location, transfers it to the XM15 Bus, and then writes the same information back into the same location. This last step is necessary because the core memory is a Destructive Readout (DRO) device. During the first part of the read cycle the memory loads the data into a register. At the same time, the memory applies the data to the bus. Then, during the second part of the read cycle, the memory takes the data from the register and writes it back into the addressed memory location.

2.10.5.3 Read/Pause/Write Cycle – Normally when memory is read the information in the accessed location is destroyed and must be restored. However, at times, the data read need not be restored. If modified data is to be written into the same memory location (the old data will not be required again), the restore portion of the read operation is unnecessary. Likewise, the clear portion of the subsequent write operation is superfluous because all cores at the addressed location were already switched to 0 when the read was executed. The read/pause/write operation is used for this purpose. It eliminates half of both the read and write cycles and results in an overall time reduction of about 25 percent.

2.10.5.4 Byte Read/Pause/Write and Byte Clear/Write – If the external processor selects byte addressing, the following applies:

a. Bit 17 of the 18-bit memory location will be cleared when the high byte (MFM ADD 0 true) is written.

b. Bit 16 of the location will be cleared when the low byte (MEM ADD 0 false) is written.

The high byte is MEM 15–00; the low byte is MEM 07–00. The XVM Processor cannot perform byte addressing, however, byte addressing is used by the PDP-11 external processor when connected to the XM15 Memory Processor.

2.10.6 ME15 Related Literature

Additional information on the ME15 core memory can be found in the *ME15 Core Memory Maintenance Manual, EK-ME15-MM-001*. This manual is available from the nearest Digital Equipment Corporation Sales Office.

CHAPTER 3
CENTRAL PROCESSOR

3.1 INTRODUCTION

This chapter describes the XVM internal CPU registers. Most of these are 18 bits long; they appear in prints KP01 through KP18, one bit of each register per page. The exceptions are the 6-bit Instruction Register on KP31 and the 1-bit Link on KP22. The buses mentioned below are described in Paragraph 3.3. Refer to the block diagram shown on drawing KP70.

3.2 CPU REGISTERS

3.2.1 Accumulator (AC)

This is the main data register in the CPU; most instructions reference and/or modify the Accumulator. It is loaded from the D (SHIFT) Bus by the LD AC strobe (KP24).

3.2.2 Link (L)

Essentially a high-order extension of the AC, the Link is also strobed by LD AC. Its input circuitry (KP22) is similar to the AC shift bus, but is more complex because of its arithmetic functions: it contains the carry from the high order bit after a TAD, and indicates an arithmetic overflow if set after an ADD. The Link may also be cleared, complemented, and tested by OPR instructions. It is also used by the Extended Arithmetic Element (EAE) option.

3.2.3 Program Counter (PC)

The Program Counter contains the address in core of the next instruction to be executed by the XVM. It is loaded from the SUM Bus by the LD PC strobes (KP24). To accommodate the various addressing modes (Paragraph 3.6), the PC bits are broken into three groups which are strobed separately. It is possible to load bits 6–17, bits 5–17, or all bits of the PC.

3.2.4 Memory Input Register (MI)

All words read from the XM15 into the CPU first enter the MI. The LD MI strobe (see KP32) causes the Memory Data Lines to be read into the MI. This register is made up of clocked set-reset flip-flops for speed of operation.

3.2.5 Memory Output Register (MO)

This register holds all information going from the CPU to the Memory Data Lines. This includes all addresses, as well as data for write cycles. The MO is loaded by LD MO from the SUM Bus. The PC may be loaded directly into the MO by the signal JAM PC to MO (see KP23, KP24). This causes a direct set of all MO bits, then clears all MO bits whose corresponding PC bits are 0.

3.2.6 Operand Address Register (OA)

The OA is used for temporary storage of the operand address, computed for all memory reference instructions. It is loaded from the SUM Bus by the LD OA strobe (see KP24).

3.2.7 Instruction Register (IR)
This is a 6-bit register used to hold the 4-bit instruction code, the indirect bit, and the index bit (see KP31). It is loaded from MI bits 0–5 by the load IR strobe (see KP31). Some of the more time-critical instruction decoding is done directly from the MI, but most is done from the IR after it is loaded (see KP28, KP29, and KP30).

3.2.8 Index Register (XR)
This register holds a quantity which is added into the operand address of indexed instructions. It is loaded from the SHIFT Bus by LD XR (see KP24, KP29).

3.2.9 Limit Register
This register holds a quantity which can be tested against the XR by an AXS instruction. It is loaded from the SHIFT Bus by the LD LR strobe (see KP24, KP29).

3.3 BUS STRUCTURE
Most of the CPU internal data routine is handled by five internal buses, designated A, B, C, D (or SHIFT), and SUM. Like the registers, these appear on prints KP01–KP18, one bit of each per page (Figure 3-1).

3.3.1 C Bus
This bus carries one of seven possible signals, according to the enabling level it receives:

1. The AC (buffered, called BAC), enabled by the BAC-C signal (see KP19).
2. The DS (data switches) register, gated by DS-C (see KP19).

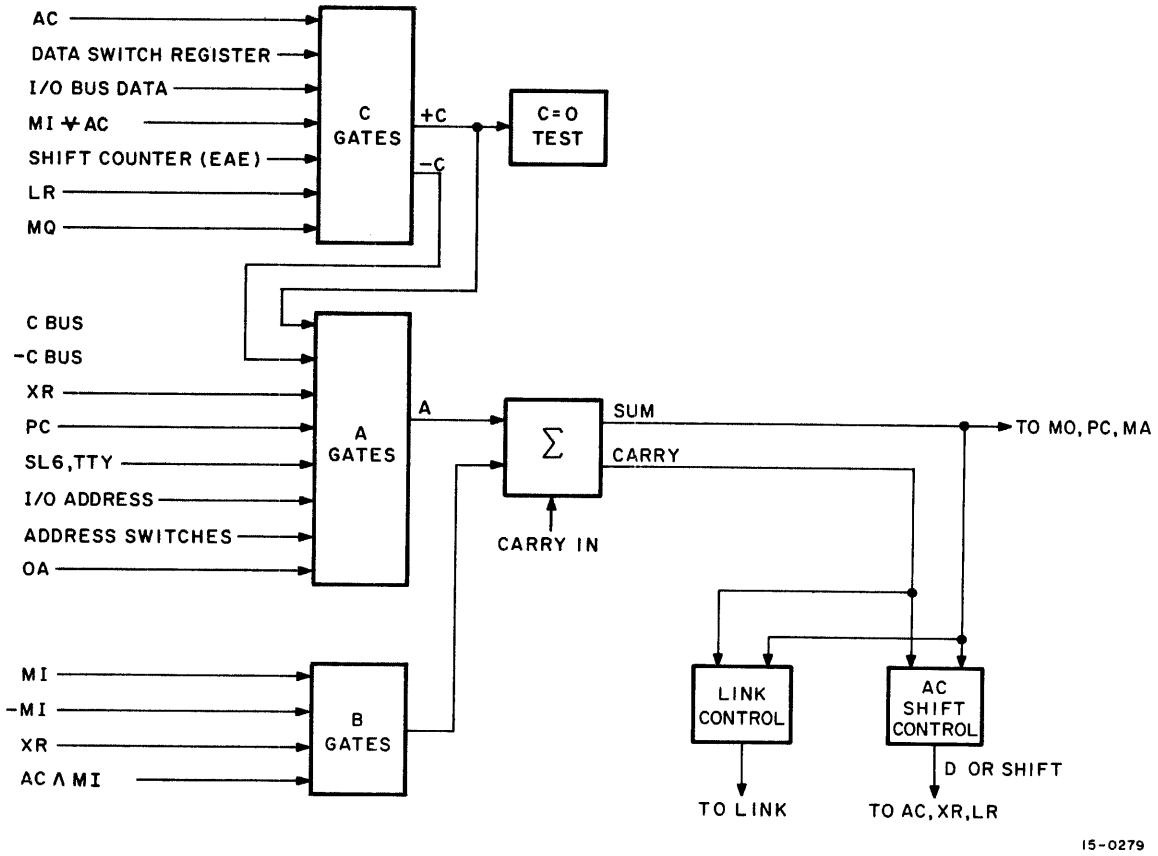


Figure 3-1 CPU Bus Structure

3. The I/O Bus data lines, gated by I/O BUS-C (see KP19).

4. The exclusive-OR of the MI and the AC, gated by XOR-C (see KP19).

5. The Step Counter (from the EAE, print KE03) gated by SC-C (see KP19, KE04).

6. The MQ (from the EAE, print KE01, KE02) gated by MQ-C (see KP19, KE04).

7. The LR, gated by LR-C (see KP19, KP29).

3.3.2 A Bus

The A Bus is one of the inputs to the adder, and carries one of eight possible signals:

1. The C Bus, gated onto the A bus by C-A (see KP19)

2. The complement of the C Bus, gated by -C-A (see KP19)

3. The XR, gated by the XR-A signals (see KP19). These are split into XR-A 0-2, XR-A 3-5, and XR-A 6-17 to accommodate the various address modes (Paragraph 3.6).

4. The PC, gated by the PC-A signals (see KP19). These signals, too, are divided into groups of bits to accommodate the various address modes. The groups are 1–2, 3–4, 5, and 6–17. Bit 0 is never enabled.

   The signal L BM UM-A causes the Link, the Bank Mode flip-flop, and the User Mode flip-flop to be placed on the high-order three bits of the A Bus, and the PC on bits 3–17. This is used by the JMS and CAL instructions to store the processor status.

5. The AC, left-shifted six places, with TT DATA lines (from KP66) filling in the six low order bits, gated onto the A Bus by SL6-A (see KP19). This is used during TTY hardware readin.

6. The I/O ADDRESS lines, gated by IO ADD-A (see KP19).

7. The console ADDRESS SWITCH signals (Paragraph 3.11) gated by ADDR SW-A (see KP19).

8. The OA gated by OA-A.

3.3.3 B Bus

This bus is the second input to the adder and carries one of four signals, depending on the enabling level received:

1. The MI, gated by the MI-B signals (see KP47). To allow for the various addressing modes, the MI-B signal is split to allow gating of groups of bits, as follows: 0–2, 3–4, 5, 6–8, and 9–17.

2. The MI complemented, gated by the -MI-B signals (see KP19). These are split into -MI-B 0–8 and -MI-B 9–17.

3. The XR, gated by the XR-B signals (see KP19). These are split into XR-B 0–2, 3–5, and 6–17.

4. The logical AND of the MI and the AC (buffered), gated by AND-B (see KP19).

3.3.4 Sum Bus

The Sum Bus is the output of the 18-bit adder. It carries the sum of the A Bus and the B Bus, plus 1, if the low order CARRY INSERT of the adder is high. Often, only one of the buses will have an enable signal, the other bus being 0.

3.3.5 Shift Bus (D Bus)

Although the Shift Bus is used as input to the XR and LR, as well as the AC, its primary purpose is to implement the various AC rotates and shifts. This is done by gating various shifted positions of the AC onto the bus, then strobing the bus back into the AC. The Link input circuitry contains gating corresponding to the Shift Bus gating. The eight Shift Bus signals and their enabling levels are as follows:

1. Sum Bus unshifted, gated by NO SHIFT-D (see KP19). This is used for all unshifted transfers into the XR, LR, and AC.

2. AC with halves swapped (bits 0–8 swapped with bits 9–17) gated by SW-D (see KP19).

3. Sum Bus, rotated 1 left (including Link), gated by RAL-D (see KP19).

4. Sum Bus, rotated 1 right (including Link), gated by RAR-D (see KP19).

5. Sum Bus, rotated 2 left (including Link), gated by RTL-D (see KP19).

6. Sum Bus, rotated 2 right (including Link), gated by RTR-D (see KP19).

7. Sum Bus, shifted 1 left, with AC00 entering Link and MQ00 entering AC17, gated by DIVSHIFT-D (see EAE).

8. Sum Bus, shifted 1 right, with Link entering AC00, gated by MULSHIFT-D (see EAE).

3.4 DATA MANIPULATION HARDWARE

The bus structure described in Paragraph 3.3 not only transports data, but performs the logical AND, XOR, and complement operations and all shifts. The adder performs the addition of the A and B Bus. Normally, this is a simple binary add, compatible with 2's complement representation for negative numbers, with the high order carry placed in the link. The adder is also used for all incrementing, by forcing a low order carry insert (see KP48). One's complement add uses the same adder circuits, but any high order carry must be reinserted at the low end, and the adder must be allowed to settle a second time. The link is used to indicate an arithmetic overflow, in which both operands are of the same sign and the result has the opposite sign (see KP22).

Internally, the adder uses a conditional sum technique for speed. The 18-bit adder is divided into three groups of six bits each. Within each group, the addition is performed by two separate 6-bit adders. One adder assumes a carry in, and the other assumes no carry in. The low order adder requires about 48 ns to settle, but the second and third groups can operate much faster; when they receive the carry they gate the proper sum, already calculated, to the output. Thus, total adder settling time is 82 ns.

Comparison and testing of data is handled in several ways. A high-order carry from the adder, while incrementing, indicates that the ISZ skip should be taken (see KP23). The zero tests for SAD and OPR are performed by a C Bus zero test circuit (see KP33). The test portion of the AXS instruction is carried out by subtracting the LR from the XR (add, with LR complemented and carry insert high) and skipping if the result is positive (see KP29).

3.5 CONTROL STATE GENERATION

At any given time, the CPU may be in one of five major states: Fetch, Defer, Execute, Increment, or EAE. From one to four of these states are used in the execution of an instruction; the exact number and sequence depends upon the instruction type. (See Paragraphs 3.8, 3.9 and 3.10 for more information on this subject).

Each major state is made up of three 250-ns time states, designated TS01, TS02, and TS03. The only exception to this occurs during the Execute state of the ADD (1's complement) instruction. In this single instance, an extra time state (designated TS02A) is inserted between time states TS02 and TS03, thus stretching the Execute cycle to 1000 ns. This allows extra time to perform the end-around carry as described in Paragraph 3.4.

Each of the 260-ns time states is further divided into four 65-ns phases, numbered 0–3. Each phase corresponds to a complete cycle of a 65-ns pulse generator called the high-speed clock.

The circuitry to produce the major states is shown in KP20; the state, phase, and clock logic are shown in KP21; a general timing diagram appears in KP79. Each major state, time state, and phase is represented by a flip-flop; only one flip-flop in each of the three groups is set at once. The phase is changed by the falling edge of the HS CLOCK; the time state changes on the phase 3-phase 0 transition; the major state changes on the time state TS03 time state TS01 transition. A 30-ns pulse called CLOCK is generated during the last half of every phase 3. This is used to generate most of the register load strobes.

Because the XM15 Memory Processor has its own internal timing mechanisms, and the I/O Processor has priority over Central Processor requests, some provision is needed to stop the control state progression while awaiting completion of XM15 service. This is accomplished by means of the STOP CLK signal (see KP21) which holds the high-speed clock in the high condition. As soon as this line is released, normal cycling resumes. In this way the processor can be held in time state TS03, phase 3, to await RD RST during memory read cycles, and the time state TS02, phase 3, to await ADR ACK during memory writes. Other signals inhibit processor state changes by freezing the enabling levels on the flip-flops. These are described in later paragraphs, along with their uses.

3.6 ADDRESSING

3.6.1 Page Mode

The address portion of an XVM instruction is 12 bits long, sufficient to directly address only 4K of the computer's possible 128K of core memory. The address, therefore, refers to a word in the 4K memory page in which the program is currently running; PC bits 1–5 are appended to MI bits 6–17 to form the address sent out on the MO. Bit 0 is not needed (Figure 3-2).

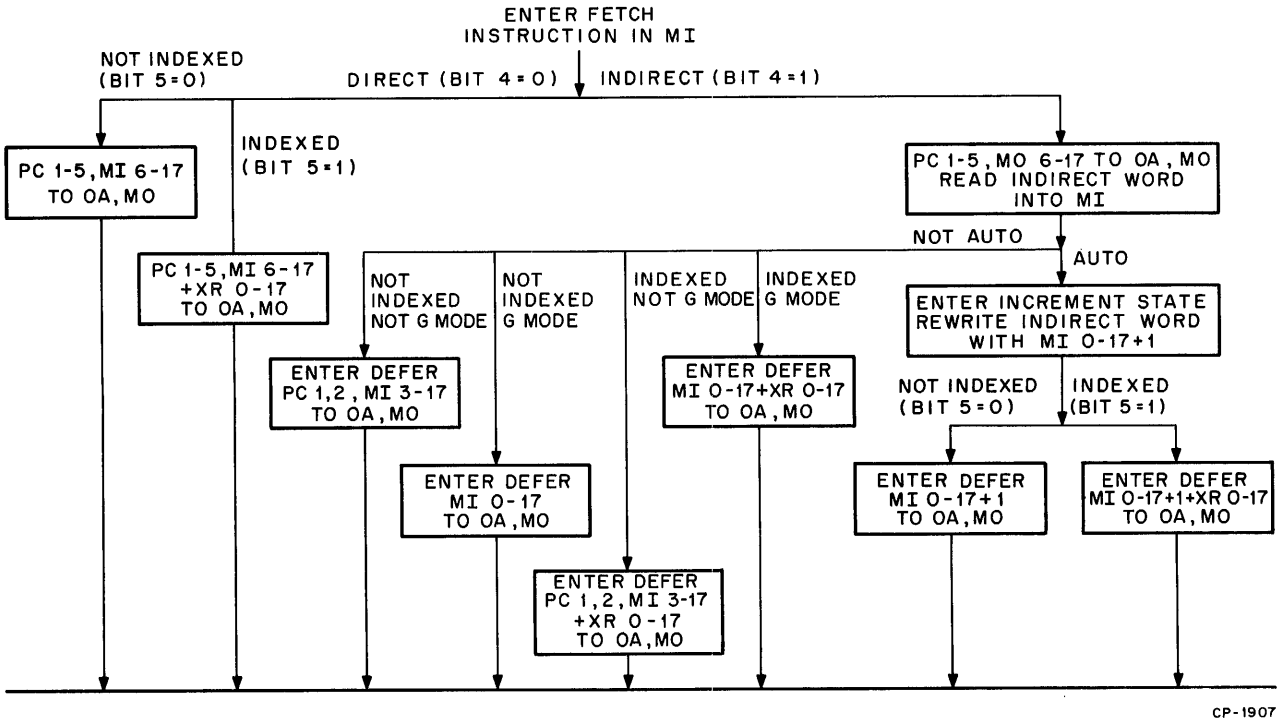


Figure 3-2 Page Mode Address Formation

If the instruction is indirect, the address is formed as above, and a deferred address word is obtained from the location referenced. Bits 0, 1, and 2 of this word are reserved for processor status bits (Link, Bank Mode, User Mode); except during G Mode (Paragraph 3.6.3) they are deposited by JMS or CAL and used later to restore the CPU to its previous status. Thus, only 15 bits of the deferred word may be used as a final address. PC bits 1–2 are appended to MI bits 3–17 in this case.

If the instruction is to be indexed, the XR is added to the final operand address. In this way, the programmer can reference an address outside the 32K bank in which his program is running. Since the MI bits use part of the B Bus, and the PC bits use part of the A Bus, the XR must be split between the two to add properly. For direct addressing the A Bus carries PC 1–5 and XR 6–17, while the B Bus carries XR 0–5 and MI 6–17. For indirect addressing the A Bus holds PC 1–2 and XR 3–17, and B carries XR 0–2 and MI 3–17.

3.6.2 Bank Mode

For compatibility with PDP-9 programs, the processor may be put into Bank Mode (Figure 3-3). This eliminates all indexing, and thus the possibility of addressing outside the current 32K; except when G Mode is selected (Paragraph 3.6.3). Bit 5 is used as part of the instruction address field, expanding direct addressing capabilities to 8K. PC bits 1–4 are now used, along with MI bits 5–17. Deferred addresses are handled in the same way as in Page Mode.

During jumps, the final address, formed as described, is placed in the PC. During normal program incrementation and skips, however, only PC bits 6–17 (5–17 in Bank Mode) are altered. This causes the program to wrap-around within its own 4K or 8K, when an attempt is made to cross the boundary without a jump.

3.6.3 G Mode

During G Mode addressing, the indirect address is obtained from the MI bits 00–17 (up to 256K) and then may be modified by the XM15 logic. The XM15 modifies the address by truncating one or two of the MSB address bits. The CPU always performs 18 bit defers in G Modes 1, 2, or 3. The address width selection for G Mode is as follows:

0 Pass 18 bits of address through the M7175 module (normal mode). CPU does 15 bit defers.

1 Pass the lower 16 bits of address through the M7175 module.

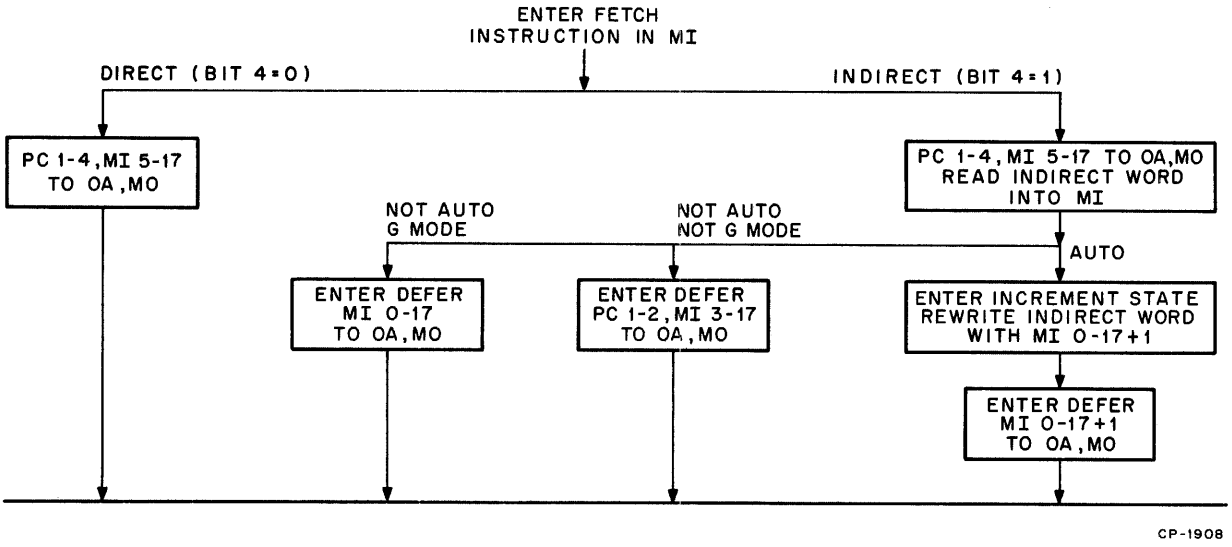


Figure 3-3 Bank Mode (PDP-9) Address Formation

2 Pass 18 bits of address through the M7175 module. CPU does 18 bit defers.

3 Pass the lower 17 bits of address through the M7175 module.

NOTE

In G Mode 1, 2, or 3, PC 0–2 will be stored during a JMS rather than L, BM, or UM bits. G1 and G0 of the MM register are used to select the mode.

3.7 MEMORY READ AND WRITE

The following paragraphs describe how a memory read or write cycle relates to CPU states. The operation of the XM15 is described in Chapter 2.

Refer to Table 3-1. Time state TS01 is used for address calculation. The information is placed on the A and B Buses, goes through the adder, and is strobed into the MO by the CLOCK signal at the end of TS01. The XM15 is then started to read from or write into this address.

On a read cycle, normal CPU operation continues until phase 3 of time state TS03 is reached. If the XM15 has not yet returned the RD RST signal, the processor stops its clock at this point and waits. When RD RST arrives, the data from XM15 is available on the MDL; it is strobed into the MI and the clock cycles are resumed.

On a write cycle, time state TS02 is used to gate the data to be written through the adder and onto the SUM Bus. The clock is stopped (if necessary) at TS02, phase 3 to await ADR ACK from memory. At this point, the data is strobed into the MO, replacing the address, and MRLS is sent to the memory, allowing it to complete the write. The normal clock cycles are resumed.

3.7.1 Processor Memory Switch

The switch (KP26) establishes the priority between the CPU and the IPU. The IPU is given the higher priority to minimize latency and prevent data loss to devices on the I/O Bus. The switch also provides the synchronizers necessary for switching between the IPU and CPU. Deskewing is provided by the port switch such that the address is put on the memory data lines 50 to 60 ns before memory request, and data is put on the lines 50 to 60 ns before memory release. The port switch also contains the drivers that send control signals to memory.

The memory interface control (KP32), which is an integral part of the port switch, generates the CPU control signals for memory and control signals for the CPU. The first stage of CPU synchronization CP MEM REQ HOLD is also shown on KP32.

When the CP is running and the IPU is inactive, the MPX flip-flop is set. As long as MPX is set, I/O ACT cannot be set, and CP ACT may be set. Each time the CP needs memory, the CP MEM REQ HOLD flip-flop is set. This occurs during TS01 PHASE 2. CP ACT is set during TS02 PHASE 0. Each event in the sequence is typically separated by one HS CLOCK or 65 ns. The HS CLOCK is used to provide the necessary deskewing of address and request. If, however, the IPU needs memory, it raises a sync (DCH SYNC or CLK SYNC) which will cause MPX to be reset. MPX (0) inhibits CP ACT from being set again. When the CP completes its present memory cycle, it is then prevented from asking for memory again until the IPU completes its use of memory. MPX is reset before the IPU is ready to use memory to provide a minimum wait when it is finally ready. When it is ready, I/O MREQ is set, then I/O ACT, and then MREQ. The IPU also uses the high-speed clock of the CPU to provide deskewing between address and request.

The control signals to memory have their drivers shown on print KP26. Each control signal may be produced by either the CPU or the IPU. The control signals are MREQ, MRLS, DATA ACK, MRD, and MWR. Read cycle and write cycle flowcharts are shown in Figures 3-4 and 3-5.

Table 3-1
CPU/XM15 Interaction

Time State	Phase	Read Cycle	Write Cycle
	0	PC 1–5 → A BUS MEM IN 6–17 → B BUS	PC 1–5 → A BUS MEM IN 6–17 → B BUS
	1	START READ, MRD	
TS01	2	1 → CP MEM REQ HOLD	START WRITE, MWR 1 → CP MEM REQ HOLD
MAJOR STATES	3	1 → CP ACT LD MO, OA MO → MDL	1 → CP ACT LD MO, OA MO → MDL
	0	M REQ	M REQ AC → C BUS
	1		
	2		
TS02	3	ADR ACK (Occurs sometime after M REQ determined by XM15) 0 → M REQ 0 → CP MEM REQ HOLD 0 → HOLD MO 0 → MO → MDL	STOP CLK (Wait for ADR ACK) ADR ACK LD MO (Change MO from address to data) 0 → HOLD MO 1 → CP MRLS MRLS
	0		
	1		
	2		MRLS ACK 0 → CP MRLS, MRLS 0 → CP ACT 0 → MO → MDL 1 → HOLD MO
TS03	3	STOP CLK (Wait for RD RST) RD RST LD MEM IN END OF CP CYCLE 0 → CP ACT 1 → HOLD MO 1 → CP MRLS MRLS, DATA ACK	
	0	MRLS ACK 0 → CP MRLS, MRLS, DATA ACK	
	1		
TS01	2		
	3		

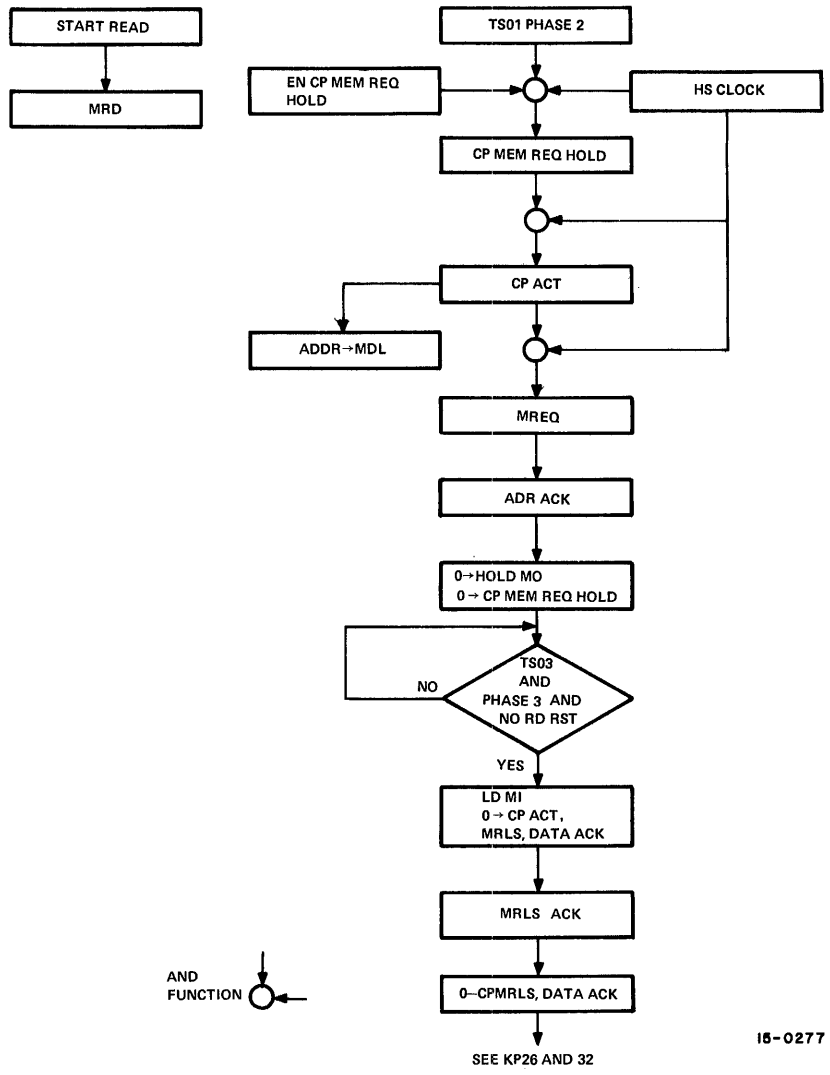


Figure 3-4 Central Processor Read Cycle

As previously explained, MRD and/or MWR, as well as the address, must be on the memory bus 50 to 60 ns before MREQ. On print KP32, Memory Interface Control, the CPU generates START READ and START WRITE. START READ is generated anytime the CPU needs to read information from memory. This will occur no later than the end of TS01 PHASE 2. It may occur as early as TS01 PHASE 0. START WRITE is generated by the CPU anytime a write into memory is to be performed. The CPU will never raise MREQ with both START READ and START WRITE, since the CPU is not capable of performing read/pause/write cycles.

For CP cycles, after MREQ is issued, the XM15 replies with ADR ACK. ADR ACK is issued to remove the address from the MDL and to clear MREQ. In the case of write cycles, it is used to produce MRLS at the TS02 PHASE 3 time. On read cycles, the next response from XM15 is RD RST. This signifies that data is present on the MDLs. The CP cannot use the data until TS03 PHASE 3, so the data is not loaded into the MI register until that time. At the same time that data is loaded into the MI, END OF CP CYCLE, MRLS, and DATA ACK are issued, signifying that the CP has completed its use of memory.

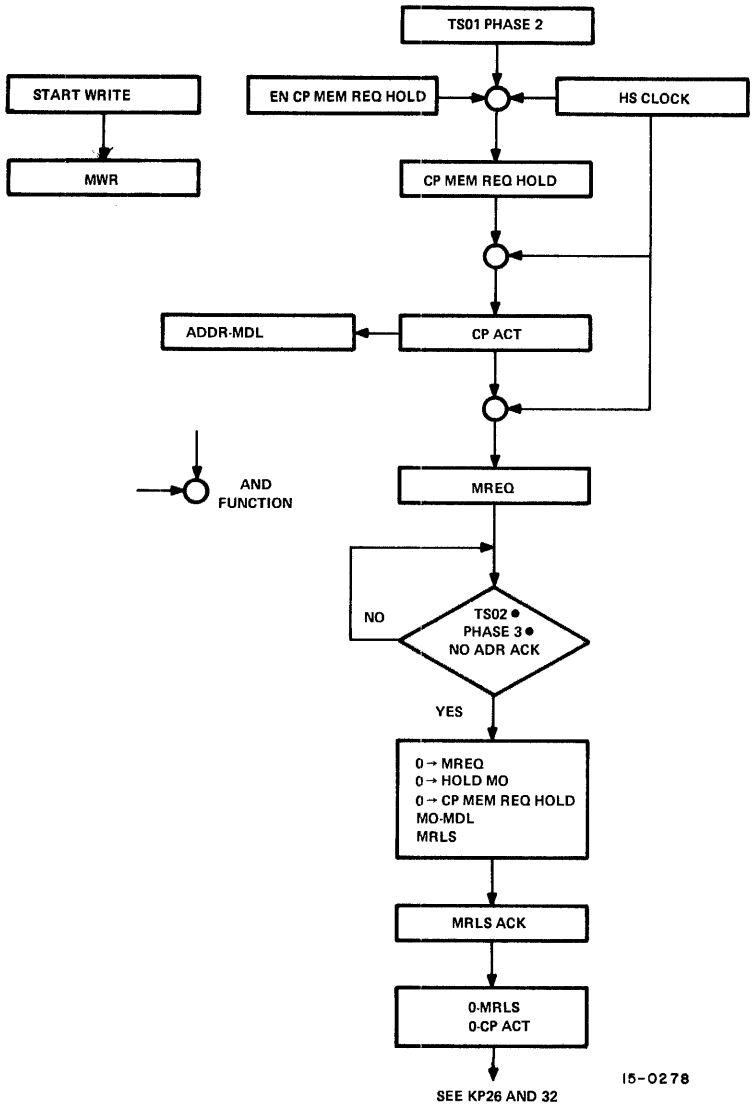


Figure 3-5 Central Processor Write Cycle

For I/O cycles, control signals from the XM15 are gated with I/O ACT to determine that they are meant for the IPU. The chain of events is similar to that of the CP, with one exception. The CP issues DATA ACK and MRLS simultaneously. The IPU issues DATA ACK first to remove memory data from the lines. Then, when the IPU has placed data on the lines to be written into memory, it issues MRLS.

3.8 INSTRUCTION FETCH

Although every instruction begins execution in the Fetch state, this is not the state in which the instruction is fetched from memory. The instruction has already been fetched during the final state (Execute, Fetch, or Defer) of the previous instruction. The Fetch state is entered with the instruction word already in the MI, and with the PC already incremented and pointing to the following instruction.

To accomplish this, the following procedure takes place during the final major state of each instruction. In time state TS01, the address of the instruction to be fetched is sent to the MO. Normally, this is done by the JAM PC TO MO signal (see Paragraph 3.2.5, Memory Output Register). If, however, the SKIP flip-flop (see KP23) is set at this time, or the SAD or OPR SKP signals are high (see KP23), the PC is incremented by sending it through the adder with a Carry Insert (see KP48) and strobed into the MO and PC. A memory read cycle is started, as above, and the new instruction is loaded into the MI at the end of the state. (See Instruction Prefetch sequence in Paragraphs 2.2 and 2.5.)

Meanwhile, during the time state TS03, the PC is incremented by gating it to the adder, causing a Carry Insert, and strobing the Sum Bus back into the PC. To provide the wrap-around mentioned in Paragraph 3.6.2, only PC bits 6–17 (5–17 in Bank Mode) are strobed. This increment occurs regardless of whether a skip was taken in time state TS01.

3.9 INSTRUCTION OPERATION DETAILS

Paragraphs 3.2 through 3.8 describe the data handling structures and basic operation necessary to implement the XVM instructions. The following paragraphs describe the sequence in which these operations occur for each instruction. Detailed information is provided in Tables 3-2 and 3-3. Supplementary explanations are included in the text.

All descriptions in this paragraph assume direct (non-deferred) addressing and Page Mode. Indirect and auto-incrementing address modes are described in Paragraph 3.10. For Bank (or PDP-9) Mode, convert all references in the text, from PC 1-5, MI 6-17 to PC 1-4, MI 5-17; *remember that no indexing is possible.*

All statements of the form "PC TO OA, MO" mean that the PC is enabled to the bus structure during the entire time state, and the output of the adder is strobed into the OA and MO at CLOCK time (end of phase 3). All incrementing uses the adder with a carry inserted (Paragraph 3.4).

3.9.1 Read Group (LAC, ADD, TAD, and XOR)

These instructions use a Fetch state, in which the operand is brought into the MI, and an Execute state, in which the next instruction is fetched. During time state TS02 of Execute, the data is sent through the adder, operated on appropriately (Paragraph 3.4), and strobed into the AC. As noted in Paragraph 3.4, ADD requires an extra time state (TS02A) to complete its end-around-carry.

3.9.2 DAC and DZM

These instructions consist of a Fetch state, in which the AC or 0 is written into memory, and an Execute state, in which the next instruction is fetched.

3.9.3 JMP

JMP uses only the Fetch state. During time state TS01, the address is formed and strobed into the PC; at the same time, it is sent to the MO and is used as the address for an instruction fetch.

3.9.4 JMS and CAL

These instructions begin with a Fetch state, in which the Link, Bank Mode, User Mode, and PC bits 3–17 are written into memory. However, if G Mode is in effect, Link, Bank Mode and User Mode are not stored and PC00–17 will be written into memory. For the JMS, the address is formed in the usual way from PC 1–5 and MI 6–17, and sent to the OA and MO. For CAL, however, a constant address of 20 must be generated. This is done by enabling the -C-A for bit 13 only, and strobing the OA and MO.

An execute state follows in which the OA + 1 is loaded into the MO and PC, and an instruction fetch is carried out from this location.

Table 3-2
Instruction Operation

Instruction	Fetch			Execute		
	TS01	TS02	TS03	TS01	TS02	TS03
LAC	PC 1–5, MI 6–17 (+XR if indexed) to OA, MO. Start Read.			PC JAM to MO. Start Read.	MI to AC	PC + 1 to PC
ADD	PC 1–5, MI 6–17, (+XR if indexed) to OA, MO. Start Read.			PC JAM to MO. Start Read.	MI + AC to AC TS02A: AC end around carry to AC	PC + 1 to PC
TAD	PC 1–5, MI 6–17 (+XR if indexed) to OA, MO. Start Read.			PC JAM to MO. Start Read.	MI + AC to AC	PC + 1 to PC
AND	PC 1–5, MI 6–17 (+XR if indexed) to OA, MO. Start Read.			PC JAM to MO. Start Read.	MI Λ AC to AC	PC + 1 to PC
EOR	PC 1–5, MI 6–17 (+XR if indexed) to OA, MO. Start Read.			PC JAM to MO. Start Read.	MI ⊻ AC to AC	PC + 1 to PC
DAC	PC 1–5, MI 6–17 (+XR if indexed) to OA, MO. Start Write.	AC to MO		PC JAM to MO.		PC + 1 to PC
DZM	PC 1–5, MI 6–17 (+XR if indexed) to OA, MO. Start Write.	0 to MO		PC JAM to MO.		PC + 1 to PC
JMP	PC 1–5, MI 6–17 (+XR if indexed) to OA, MO, PC. Start Read.		PC + 1 to PC			
JMS	PC 1–5, MI 6–17 (+XR if indexed) to OA, MO. Start Write.	L,BM,UM,PC 3–17 to MO. If G Mode, PC 0–17 to MO		OA + 1 to MO, PC Start Read.		PC + 1 to PC

Table 3-2 (Cont)
Instruction Operation

Instruction	Fetch			Execute		
	TS01	TS02	TS03	TS01	TS02	TS03
CAL	20 to OA, MO Start Write.	L,BM,UM,PC 3–17 to MO.		OA + 1 to MO, PC Start Read.		PC + 1 to PC
SAD	PC 1–5, MI 6–17 (+XR if indexed) to MO, OA Start Read.			MI XOR AC to C BUS. C = 0: JAM PC to MO C ≠ o: PC + 1 to MO, PC. Start Read.		PC + 1 to PC
OPR	OPR SKIP: PC + 1 to ____ MO, PC OPR SKIP: PC JAM to MO Start Read. (CLR AC)	(CLR LINK) Operate on AC, I	PC + 1 to PC			
LAW	PC JAM to MO Start Read.	MI to AC	PC + 1 to PC			
IOT	IOT Request 0 to AC if MI14 = 1 No memory cycle.		Stop Run Start Run on IOT	SKIP: PC + 1 to MO, ____ PC SKIP: PC JAM to MO Start Read.		
XG	No memory cycle.	Transfer, ADD to AC, LR, XR	If AXS, TEST XR = LR: 1 → SKIP or XR < LR: 0 → SKIP	SKIP: PC + 1 to MO, ____ PC SKIP: PC JAM to MO Start Read.		
PI	0 to IR (CAL) I/O Address (=0) to OA, MO Start Write.	L,BM,UM,PC 3–17 to MO		OA + 1 to MO, PC Start Read.		
API	1 to IR00 (XCT) I/O Address to OA, MO Start Read.			Execute operand as instruction		

3.9.5 ISZ

The ISZ instruction uses three major states: Fetch, Increment, and Execute (Table 3-3). The Fetch cycle reads an operand in the usual manner. The Increment cycle adds 1 and rewrites the word in memory (read/pause/write is not used). While the operand is being incremented (in time state TS02), the high-order carry output is checked, and if a carry occurs the SKIP flip-flop (KP23) is set. This implements the skip-on-zero. The Execute state is an instruction fetch, using the PC or the PC + 1, according to the state of SKIP.

Table 3-3
ISZ Instruction Operation

Major State	Time State	Operation
Fetch	TS01	PC 1–5, MI 6–17 (+XR if indexed) to MO, OA Start Read.
	TS02	
	TS03	
Increment	TS01	OA to MO Start Write
	TS02	MI + 1 to MO If carry out, set SKIP
	TS03	
Execute	TS01	$\overline{\text{SKIP}}$: PC JAM to MO SKIP: PC + 1 to MO, PC Start Read.
	TS02	
	TS03	

3.9.6 SAD

The Fetch cycle of SAD brings in an operand. This is followed by an Execute cycle in which the comparison, skipping, and instruction fetch are carried out. During time state TS01 of Execute, the XOR of the AC and the MI (operand) is gated onto the C Bus. If the C = 0 circuitry (see KP33) shows a perfect match, PC JAM to MO is used and the instruction Fetch occurs with no skip. If C $\neq$ 0, the PC is incremented before the Fetch. This incrementation is set up using the A Bus, so it does not interfere with the comparison on the C Bus.

3.9.7 XCT

This instruction goes through a Fetch state, getting an operand in the usual manner, and then enters the Fetch state a second time. The operand, now in the MI, is treated exactly as if it had been encountered in normal program flow as an instruction that was fetched into the MI by a previous instruction. All of the instruction states will occur, and the PC will be incremented or altered as usual (Table 3-4).

3.9.8 OPR

This instruction group uses a single Fetch state for its execution. In time state TS01, the OPR SKIP logic (see KP23) determines whether a skip will take place, and the Fetch for the next instruction is inititated. The actual operation on the Link and AC takes place in TS02, by setting up the appropriate buses and strobing the output into the Link and AC. The only exceptions to this are the clear operations which take place during TS01; CLOCK, for the AC; and TS02, phase 1, for the Link.

Table 3-4
XCT Instruction Operation

Major State	Time State	Operation
Fetch	TS01	PC 1–5, MI 6–17 (+XR if indexed) to MO, OA. Start Read
	TS02	
	TS03	
Fetch	TS01	Execute operand as instruction
	TS02	
	TS03	

3.9.9 LAW

LAW consists of a single Fetch state, used to fetch the following instruction. During TS02, the LAW instruction (still in the MI) is loaded into the AC.

3.9.10 IOT

The IOT begins with a Fetch state, in which no memory cycle occurs. IOT REQUEST is raised, activating the I/O Processor (Chapter 4). If bit 14 of the MI is set, the AC is cleared at Clock H time of TS01. The Fetch state continues until, at the end of TS03, phase 2, the RUN flip-flop (KP21) is dropped, stopping all CPU phase transitions. By this mechanism, the CPU waits for the IOT DONE signal (see KP55) which sets RUN. The I/O Processor, in the meantime, may have strobed the I/O Bus data lines into the AC, and may have set the SKIP flip-flop. An Execute state follows Fetch, and the next instruction is brought in, controlled by SKIP.

3.9.11 Index Group (XG)

These instructions consist of a Fetch state, with no memory operation, followed by a standard Execute state instruction fetch.

In time state TS02 of Fetch, the transfer (PAX, PAL, PXA, PXL, PLA, PLX); clear (CLX, CLR); or add (AXR, ACC, AXS) takes place. The add gates the AC or XR onto the A Bus, and MI 9–17 onto the B Bus. If MI bit 9 is a 1, the number is negative and bits 0–8 must be filled with the 1s for proper addition. This is done by activating both MI-B 0–8 and -MI-B 0–8 simultaneously, during the addition (see KP19).

Time state TS03 of Fetch is used only by the AXS, for comparing the XR to the LR. The XR is gated onto the B Bus; the 2's complement negative of the LR is added to it by gating the LR to the C Bus, -C to the A, and raising carry in. The high order carry output, along with the XR and LR signs, indicates whether SKIP should be set (see KP29). Like signs with a carry, or opposite signs with no carry, indicate that XR $\geqslant$ LR and a SKIP is called for. Skip, of course, takes effect in the following Execute state.

3.9.12 Interrupts (API and PI)

While API and PI are not proper instructions, they behave in very much the same manner once they are recognized. The recognition sequence is described in Paragraph 2.7 for API and Paragraph 4.9 for PI.

Whenever the INT ACK + ST signal is asserted and the CPU enters an instruction Fetch cycle, the interrupt begins. An instruction fetch is allowed to take place, but since the instruction will not be used at this time, the PC increment is disabled (KP24). Upon entering the Fetch state, the interrupt takes full precedence over the instruction in the MI.

If the interrupt is a PI, the 00 code (CAL) is forced into the IR. From this point, execution is identical to a CAL, except that the I/O Address Lines are used to provide the operand address, instead of the constant 20. These lines will always give a 0 on PI requests. Thus, the L, BM UM and PC 3–17 are stored in location 0 and the next instruction is fetched from location 1.

The API forces an XCT code (40) into the IR, and proceeds as an XCT would, except that the address of the operand is read from the I/O Address Lines instead of the MI. The device requesting the API must, when acknowledged, place the appropriate interrupt address on these lines. Thus, some instruction (in an address peculiar to the device) is executed. This will usually be a JMS to the interrupt handler.

3.10 DEFER AND AUTO-INCREMENT

If bit 4 of any memory reference instruction is set, that instruction is to use deferred (or indirect) addressing. Instead of the usual Fetch state, the instruction begins with Fetch and Defer states, as shown in Table 3-5. The Fetch state is always a memory read, which brings in the pointer or indirect address word. The Defer state is almost identical to the Fetch state of the same instruction in nondeferred mode; it brings in or writes out the operand, just as Fetch would have. The only difference is that MI 3–17 are used instead of MI 5–17. In the Defer state, indexing occurs after the indirect addressed word is obtained. The remaining states of the instruction proceed as though in nondeferred mode.

Table 3-5
Deferred Addressing Operation

Major State	Time State	Operation
Fetch	TS01	PC 1–5, MI 6–17 to OA, MO Start Read
	TS02	
	TS03	
Defer*	TS01	PC 1–2, MI 3–17 (+XR if indexed) to OA, MO Start Read or Write
	TS02	Identical to operation specified for non-Defer, Fetch, TS02.
	TS03	Identical to operation specified for non-Defer, Fetch, TS03.

*See Figures 3-2 and 3-3 for effects of G Mode.

If a deferred instruction has an address of $10–17_8$, regardless of the PC contents, the instruction is to use Auto-Increment mode addressing (Table 3-6). The contents of the addressed word (absolute 000010–000017) are first incremented and then used as a deferred address. This is accomplished by replacing the normal Fetch state with the Fetch, Increment, Defer sequence shown in the table. This sequence is caused by the circuitry on KP33 which sets the AUTO flip-flop during TS01. The Fetch state is used to read the indirect word from memory. Use of locations 10–17 on the lowest core page is assured by gating only MO 6–17 to the MDL. In the Increment state, the pointer is incremented and rewritten. In the Defer state, the original pointer, plus one, is used as the address and the operand is either read or written into, as it would be in the Fetch state of a normal mode instruction.

CAL can be deferred, but not auto-incremented. In deferred mode, the contents of location 20 are used as the final address. Operation is identical to that shown in Table 3-5, except that an address of 20 is forced in TS01 of Fetch. In a JMP deferred or auto, the Defer state is the final state of the instruction, and thus fetches not an operand, but the next instruction. In TS01 of Defer, the final address is strobed into the PC as well as the OA and MO.

ISZ auto uses the Increment state twice; the major state sequence is Fetch, Increment, Defer, Increment, Execute. The first increment is for rewriting the address pointer, while the second is for the normal increment of the operand. The skip-on-zero circuit can only set SKIP during the second Increment state, while AUTO is zero.

Table 3-6
Auto-Increment Operation

Major State	Time State	Operation
Fetch	TS01	PC 1–5, MI 6–17 to OA, MO 1 → AUTO Start Read (MO 6–17 to MDL)
	TS02	
	TS03	
Increment	TS01	OA to MO Start Write (MO 6–17 to MDL)
	TS02	MI + 1 to MO
	TS03	
Defer	TS01	MI 0–17 + 1 (+XR if indexed) to OA, MO Start Read or Write
	TS02	Identical to non-Defer, Fetch, TS02
	TS03	Identical to non-Defer, Fetch, TS03 0 → AUTO

All 18 bits of the auto-increment register are used as an address. This provides another method of addressing more than 32K of core memory.

3.11 CONSOLE OPERATION

3.11.1 Console Cable Multiplexer

Only two 18-conductor flexprint cables are used between the CPU and the console. These are multiplexed six ways by a free-running 36 kHz clock and a modulo -6 counter (see KP45, KP46). Three lines of the cable carry the state identification (console zero = high order), and 24 lines comprise the I Bus, which carries information to or from the console, depending on the console state. The I Bus assignments and timing are shown in KP72.

During console states 0, 1, and 2, various internal CPU signals are placed on the I Bus, and three different sets of console lights are sequentially enabled to display this information. Each light, when on, is only enabled for one sixth of each 333 μs console cycle, but brightness is maintained by using 15 volts instead of the normal 10 volts to drive the lamps. Console states 0 and 2 display permanently assigned CPU signals; state 1 displays one of 24 registers, as selected by the rotary switch on the console. (See Appendix D for indicator bit assignments.)

Console states 3, 4, and 5 are used to read the status of the various console switches into the CPU. In general, these are read into active registers so that they can be referenced by the CPU at anytime. The rotary switch status register is shown in KP44. The various key functions are stored in the flip-flops shown in KP45 and KP46. The data switch register appears with the main CPU registers in KP01 through KP18. The address switches are not stored in a register; whenever the CPU references these switches it must wait for console state 4 (CF pulse).

3.11.2 Key Functions

The control flow of the various console key functions (start, continue, execute, examine, and deposit) is shown in KP73. This paragraph provides additional explanation. Most of the associated logic appears in KP34.

The Stop switch causes the RUN flip-flop (see KP21) to drop as soon as the CPU enters phase 3, time state TS03, of the final major state of an instruction (Set Fetch is high). The CPU is effectively frozen at the end of an instruction, with the next instruction in the MI, but with the PC not yet incremented. [A]

Once the CPU is stopped, deposits and examines may be performed. These start RUN, go through a forced Fetch state, in which a memory word is read or written, then drop RUN again, under control of the STOP TS RUN flip-flop (see KP34). Executes operate similarly, using a forced Fetch to load the data switches into the MI, then executing this as an instruction. RUN is stopped after this operation by the XSW IN PROG flip-flop (see KP34).

START and CONTINUE (when stopped at TS03, Set Fetch) both use a forced Fetch state to read in the next instruction. START uses the address switches as an address, while CONTINUE uses the PC. The PC is incremented, and the CPU resumes normal operation. If CONTINUE is used and the CPU is not in TS03 of a Set Fetch state, RUN is simply raised and operation resumed.

Single Instruction, Single Step, and Single Time operate by dropping RUN at the appropriate intervals (see KP21).

3.12 READ-IN

To load binary tapes or bootstraps (Figure 3-6), the XVM uses a hardware Read-In function, which loads core from either the Teletype or the high-speed, paper-tape reader, depending on an internal jumper wire shown in KP66. Each frame of the tape carries data in bits 1-6; three consecutive frames form an 18-bit word for storage. Bit 7, if punched, causes the last word read to be executed as an instruction, terminating the read. Bit 18 is always punched. The Read-In logic is shown in KP66 and KP49; the flow diagram is in KP75.

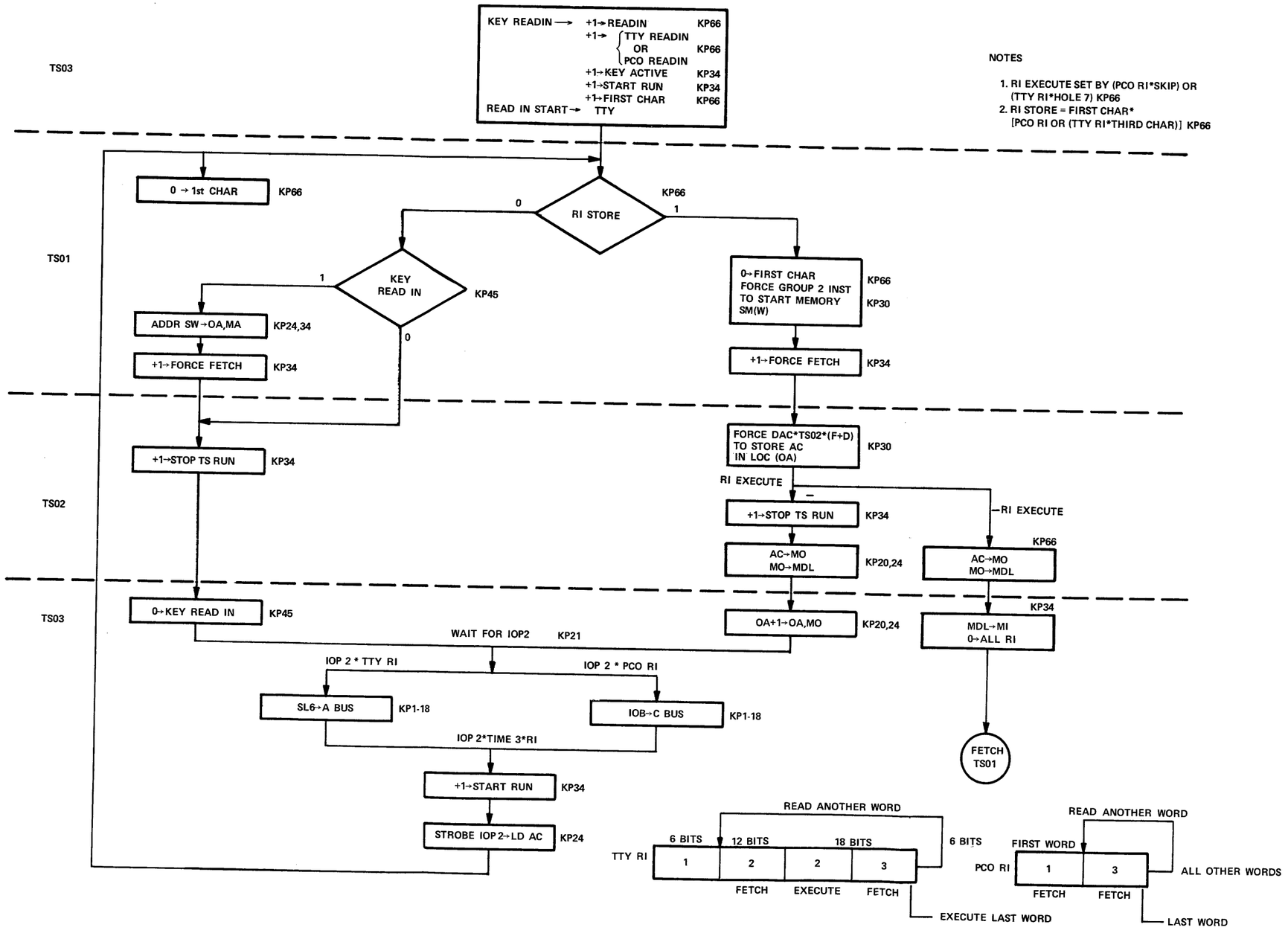


Figure 3-6 Read-In Flow Diagram

In Teletype Read-In operation, the address switches are first read into the OA and MO. These give the core location where loading is to begin. The time states are allowed to run, but are stopped by STOP TS RUN (see KP34) when TS03 is reached. Meanwhile, the Teletype reader has been started by the READ IN START signal (KP66), and eventually this returns with a character. This causes an IOP2 pulse which stores the character in the AC via SL6-A (see Paragraph 3.3.2, A Bus), restarts the time states, and increments the character counter (see KP66). When three such characters have been brought in, they are written into memory, the OA is incremented, and the process continues. When a bit-7 punch is detected, the AC is strobed into the MI instead of being written into memory, all the Read-In enables are dropped, and the MI is executed as an instruction. Usually, this will be a jump to the start of the program.

Operation using the high-speed reader is quite similar to Teletype Read-In. The principal difference is that the reader interface, instead of the CPU, packs the three 6-bit characters into a word, so each cycle after the first is a store and read cycle. The character counter and the ALS6 logic is not needed.

CHAPTER 4
KD15 I/O PROCESSOR

4.1 INTRODUCTION

The I/O Processor coordinates data transfers between the Central Processor and peripheral devices and also between the XM15 and peripheral devices. Data transfers between the CPU and peripheral devices are called program control transfers and are implemented by the input/output transfer (IOT) instructions. Data transfers between the XM15 and peripheral devices are accomplished by a request/grant priority scheme and is referred to as the data channel. Table 4-1 summarizes the XVM input/output facilities.

Program control transfers occur as a result of the IOT instruction execution. These instructions, contained in the body of the main program or in appropriate subroutines, are microcoded to effect response of a specific device interfaced to the I/O Bus System. Microcoding includes issuing a unique device selection code and appropriate processor-generated pulses to initiate device operations, such as transmitting data from the device to the Central Processor, or from the processor to the device. All program control transfers are executed through the accumulator in 18-bit words. This portion of the I/O Processor also contains facilities for skipping on device flags and interrupts which cause a break in the normal flow of Central Processor operations.

The data channel facility provides for high-speed transfer of data in blocks between peripherals and the XM15. Since the I/O Processor and Central Processor of the XVM are asynchronous, a data channel transfer request raises an I/O memory request, which is granted and transmitted to the XM15 at the conclusion of the current Central Processor memory reference in progress. These requests will continue to take priority over the Central Processor until the transfer is completed. The types of transfers available to the data channel facility are single cycle input and output transfers, multicycle input and output transfers, add to memory transfers, and increment memory transfers. The I/O Processor consists of four sections:

Timing Generator
Request Synchronizer
IOT Control Logic
Data Channel

4.2 TIMING GENERATOR

Timing for the I/O Processor is controlled by an M401 clock, located on KP51, which runs freely, with the exception of waiting for the XM15, on multi-cycle and single-cycle output transfers. This clock steps a 2-bit counter which is decoded on KP55 into four times: TIME 1, TIME 2, TIME 3 and TIME 4, as shown in Figure 4-1. TIME 1 is called I/O SYNC, and is used to synchronize devices on the I/O Bus to the I/O Processor. The frequency of the I/O clock is 4 MHz. The overall frequency of the I/O Processor is 1 MHz; therefore, the I/O clock on KP51, N21-E2, should be set so that pulses are 250 ns apart.

Table 4-1
Summary of XVM Input/Output Facilities

Facility	Remarks
Data Transfers To/From Memory	
Multi-Cycle Data Channel Input	Used to transfer 18-bit data words directly to the XM15 core memory at high-speed (170 kHz).
Multi-Cycle Data Channel Output	Used to transfer data directly from memory in 18-bit words. Maximum speed is 130 kHz.
Add to Memory	Used to add the contents of a device register to the contents of a specified core location in 18-bit words. Maximum speed is 130 kHz.
Increment Memory	This facility allows an external device to increment the content of a core location by 1. Maximum speed is 333 kHz.
Single-Cycle Data Channel Output	With this facility a device can transfer a burst of data from the XM15 core memory a 625 kHz in 18-bit words.
Single-Cycle Data Channel Input	Used to transfer a burst of data from a device to the XM15 core memory at 925 kHz per 18-bit word.
Data Transfers To/From CPU	
Addressable I/O Bus	With this facility, devices can transfer data in 18-bit words to or from the central processor. A typical rate is one transfer every 200 μs.
Command and Status Transfers	
Addressable I/O Bus	Command and status information can be transferred to or from the CPU in the same manner as ordinary data.
Read Status	This is a special facility designed to allow the user to monitor all vital flags in the system. Each device is assigned a bit for its flag(s), which is read onto the addressable I/O bus and into the CPU when the Read Status command is given. No two devices should use the same bit.
Skip	The addressable I/O bus allows the computer to test the status of a flag (typically) by issuing a pulse which will echo if the addressed flag is up. Every flag that posts a program interrupt must be identifiable by the skip facility.

Table 4-1 (Cont)
Summary of XVM Input/Output Facilities

Facility	Remarks
Interrupts	
Program Interrupt	All devices share a common program interrupt line. When a device posts an interrupt the computer is forced to location 0, bank 0, and then on to a service routine designed to identify the requesting device using the skip facility.
Automatic Priority Interrupt	This facility reduces the time to service a requesting device and establishes a priority among devices so that important interrupts can be handled quickly and without interference.
NOTE: API is contained in the XM15.	

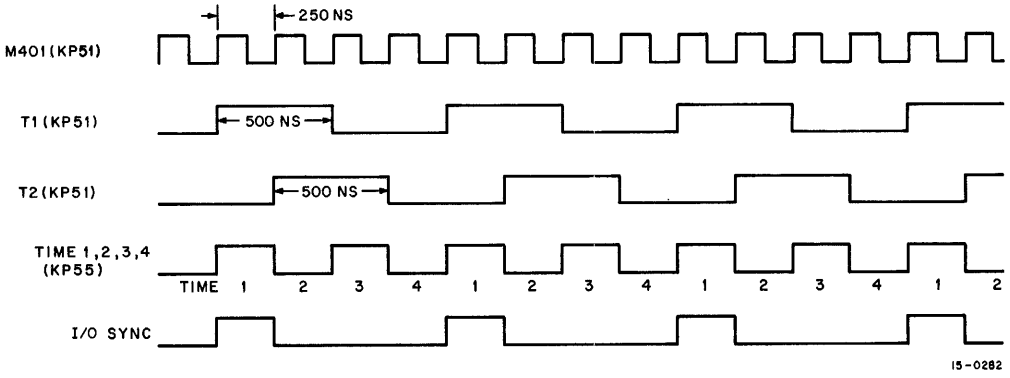


Figure 4-1 Basic I/O Timing

4.3 REQUEST SYNCHRONIZER

A priority structure is set up in the XVM as follows:

a. Data channel request
b. Clock requests
c. Automatic priority interrupt requests
d. Program interrupt request
e. IOT requests
f. Main program

In order to establish these priorities, a two-stage synchronizer is provided in the I/O Processor, as shown in KP51. Each priority contains two stages of synchronization. The first stage consists of the DCH, CLOCK, API, PI, and IOT flip-flops on KP51. The various requests for activity on the data input to these flip-flops are clocked at TIME 4. Any one or all of these flip-flops may become set at this time. 250 ns later, at TIME 1, a clock pulse is provided to the sync flip-flops immediately above each of the first stage synchronizer flip-flops, and sets one of these flip-flops. During the previous 250 ns, if a higher priority request had been set into one of the first stage flip-flops, a clear would have been transmitted to all lower request flip-flops and, therefore, only one of the second

stage synchronizer flip-flops would become set. The setting of the sync flip-flop will allow highest priority request activity to proceed. Once one of the priority sync flip-flops is set, such as in program control transfers, it will remain set until the transfer is completed.

4.4 IOT CONTROL LOGIC

The IOT instruction is a command from the Central Processor to transfer data from the Central Processor (accumulator) to the device or to read data back from the device into the accumulator of the Central Processor. The instruction format in Figure 4-2 consists of the instruction code; a 6-bit device select and a 2-bit subdevice select code, which are put onto the I/O Bus to designate the device with which the processor wishes to communicate; a clear the AC bit, which if set, will cause the clearing of the accumulator; and three I/O pulses; any one or all of which may be given in a single IOT instruction.

The general purpose of these pulses is as follows:

IOP 1 – Transmits data to the device, tests the device flag, and may cause the program to skip the next sequential instruction.

IOP 2 – Transmits data to or from the device via the accumulator.

IOP 4 – Transmits data to the device from the accumulator.

The IOT instruction requires the operation of both the Central Processor and the I/O Processor. The Central Processor, upon detecting the IOT instruction, sets the IOT request flip-flop on KP35. If MI bit 14 is set, the AC will be cleared. When the processor reaches FETCH, TS03, and CLOCK, it halts and waits for the I/O Processor to finish its execution and respond with IOT DONE.

The I/O Processor has to synchronize the IOT on KP51 with the other priority requests. Upon synchronization, the information in the accumulator is enabled to the I/O Bus lines along with the device select and subdevice select bits from MI bits 6 – 13. IOP 1 is enabled on the bus if bit 17 in the MI is set. IOP 1 in the I/O Processor lasts for 1 μs; IOP 1 on the bus is 750 ns long. At the end of IOP 1, if neither bit 15 nor 16 in the MI is set, IOT DONE is generated. Otherwise, IOP 2 in the I/O Processor is set. If bit 16 in the MI is set, IOP 2 is enabled on the I/O Bus for 750 ns. If READ REQUEST is true at this time, the AC is disabled from the I/O Bus. 750 ns after IOP 2 is placed on the bus, the AC is strobed and information that was on the I/O Bus is placed in the accumulator. At the end of IOP 2, if bit 15 of the MI is not set, an IOT DONE is generated. If it is set, IOP 4 is set. IOP 4 is enabled onto the bus for 500 ns. After this time, an IOT DONE is generated; the IOT and IOT SYNC flip-flops on KP51 are cleared out and the Central Processor is restarted. Figure 4-3 shows the IOT instruction timing, giving the synchronization time between Central Processor and I/O Processor. An IOT flow diagram is shown in Figure 4-4.

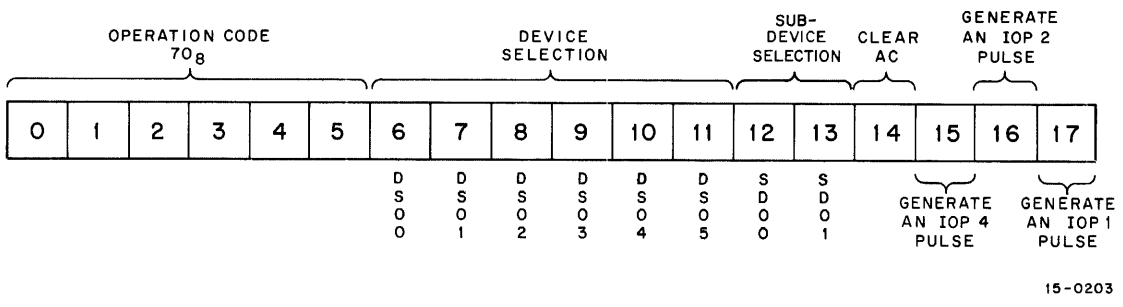


Figure 4-2 IOT Instruction Format

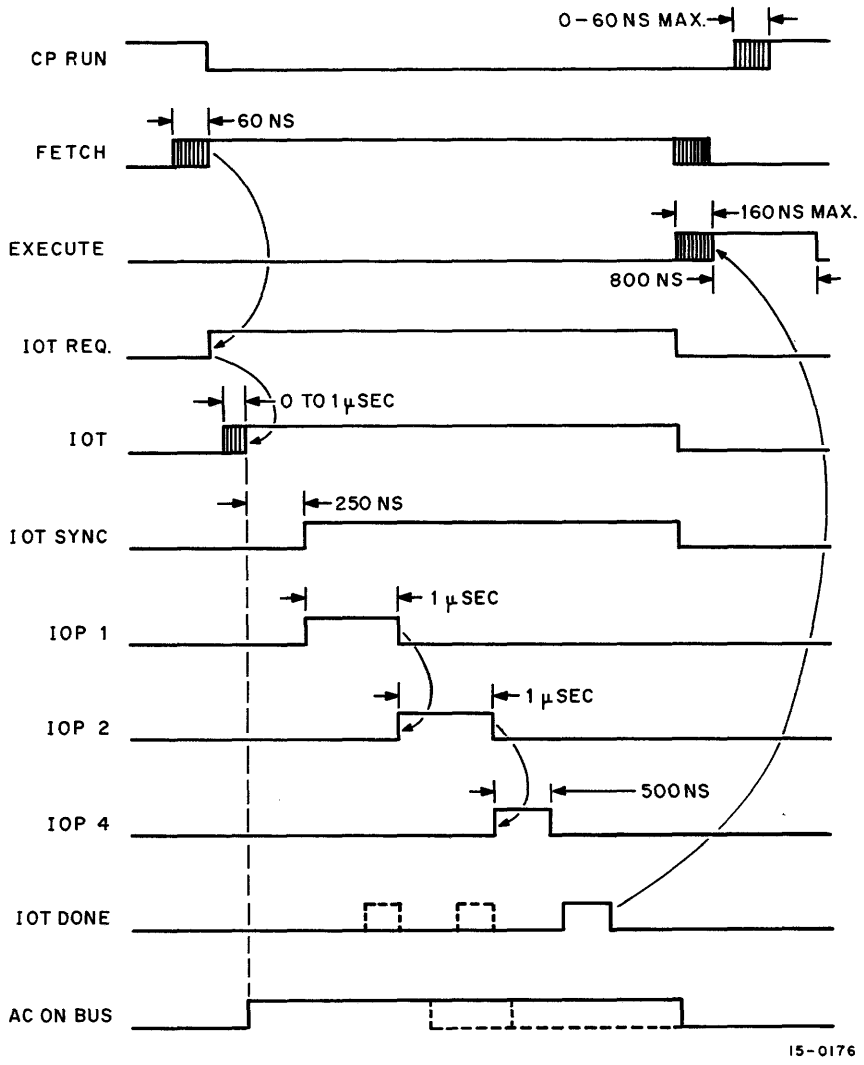


Figure 4-3 IOT Instruction Timing

4.5 I/O BUS DEVICE PRIORITY AND SYNCHRONIZATION

In DCH and API (described in Paragraph 2.7), a priority exists among the eight devices which may be placed on the DCH or API level 0, 1, 2 or 3 lines. The device closest to the I/O Processor is given highest priority. The M104 Multiplexer module is used in determining the priority by issuing the DCH or API request and controlling the device during the transfer.

An enable signal is daisy-chained from device to device on the bus. An enable signal to a device allows its request to be raised. When a device raises a request, it disables the enable transmitted to the next device on the bus, clearing or inhibiting the request of any device further down the bus. The enable is disabled until the action requested is completed.

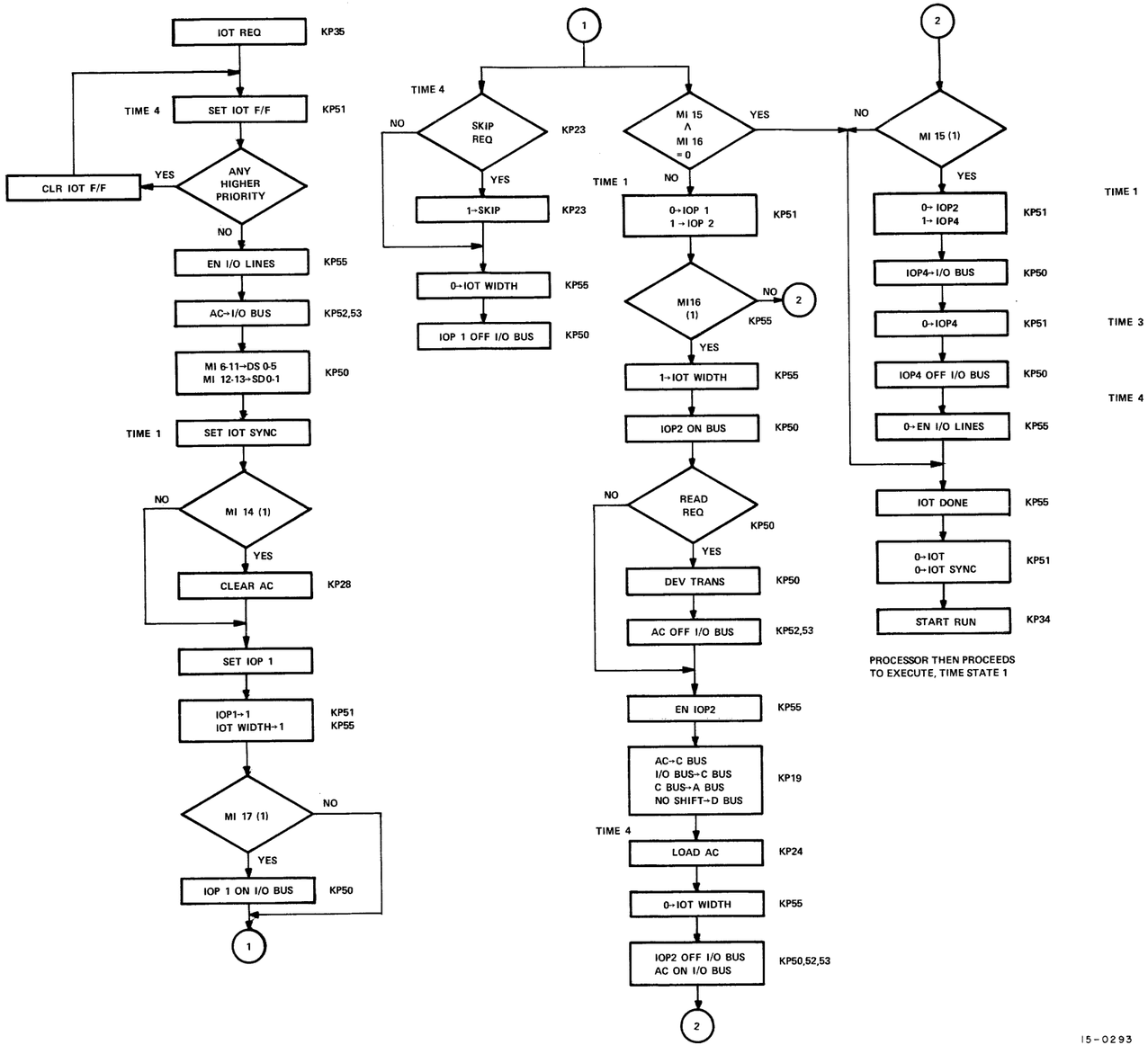


Figure 4-4 IOT Flow Diagram

The synchronization of a device starts when the device raises its device flag. If the enable (EN IN) is true, the REQ will be set at the next I/O SYNC. Approximately 1 μs later, a GRANT signal will be sent out on the I/O Bus and will load the contents of the REQ flip-flop into the ENA flip-flop. This microsecond is used to allow the EN OUT signal, that was taken away, to propagate down the bus and clear any other requests which may have been set. ENA is used to gate the address from the device onto the I/O ADDRESS lines. ENB, which is set one μs after ENA, is used in Multicycle DCH breaks to specify the data transfer. Figure 4-5 is a simplified diagram of the M104 logic. Timing is shown in Figure 4-6.

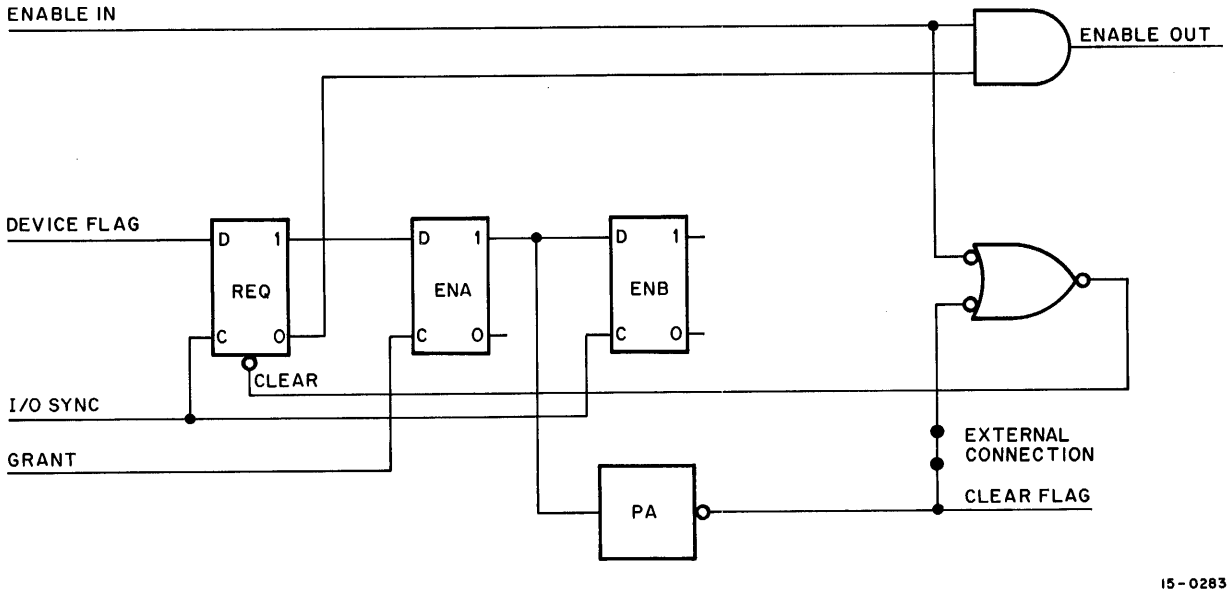


Figure 4-5 Simplified M104 Module Diagram

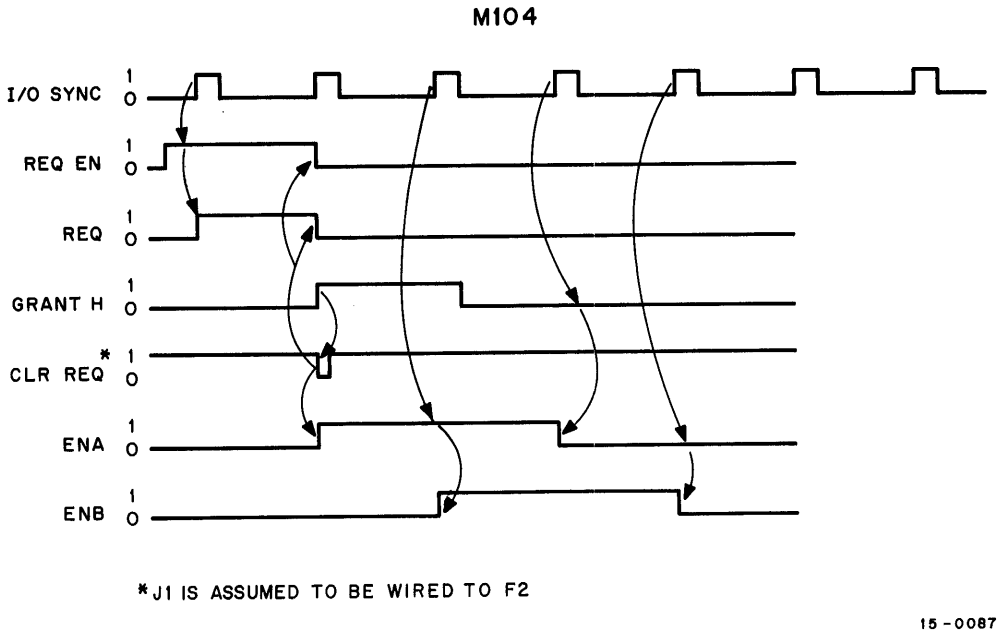


Figure 4-6 M104 Timing Diagram

4.5.1 I/O Bus Cables

The I/O Bus cables are shown in Figure 4-7. The I/O Bus signals are described in Table 4-2.

4.6 DATA CHANNEL (DCH)

Refer to Figure 4-8. The hardware to implement the XM15 to peripheral device data transfers includes: a bus buffer for temporary storage (I/O Buffer 0–17, KD04, KD05); a data storage register, an input mixer and adder used to transfer information from the devices to the XM15 memory and from the XM15 memory to the devices (DSR KD01, KD02, KD03); priority logic for the synchronization of requests (KP51) and generation of GRANT (KD06); and DCH control logic (KD04, KD05, and KD06).

Data Channel devices on the I/O Bus are initialized by IOT commands; the data transfer process is initiated also by an IOT. After initialization, when ready for a transfer, the device raises its flag which is then synchronized to the I/O Processor. The device then transfers the data through the I/O Processor to or from the XM15.

4.6.1 Data Channel Latency

Latency is defined as the amount of time which is required to transfer data after the request is made by a device. When a worst case latency time is started, it is assumed that the requesting device has priority over all other devices on the I/O Bus.

Worst case latency in the XVM occurs when a request is granted to a multicycle output device. The worst case latency for a single cycle output device is 9.9 μs.

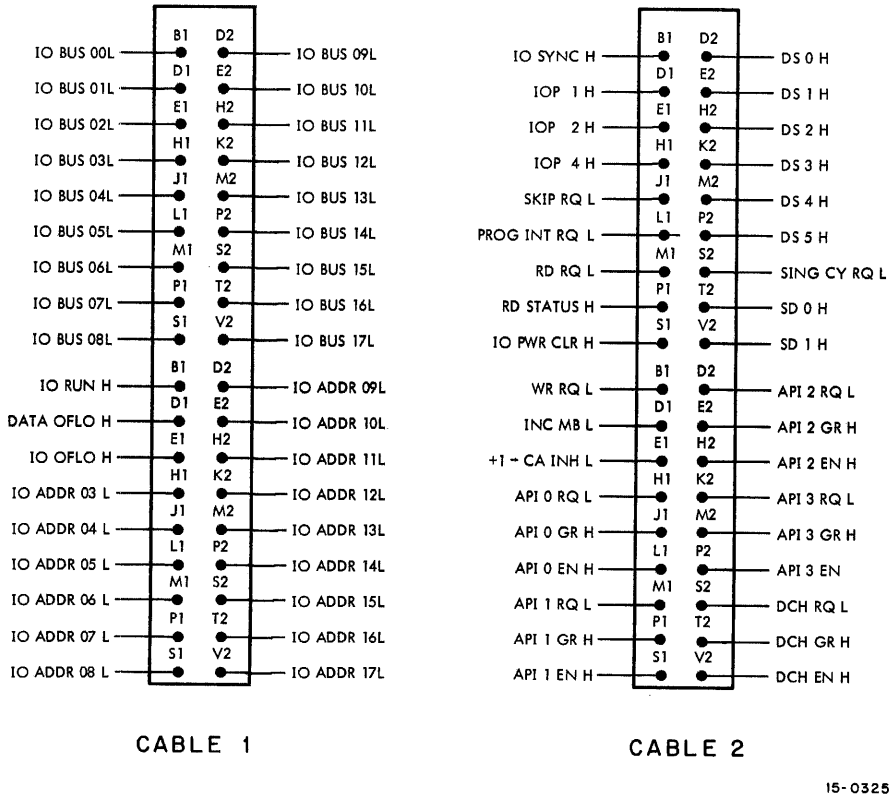


Figure 4-7 I/O Bus Cables

Table 4-2
I/O Bus Signal Functions

Signal Mnemonic	Connector Pin Number	Signal Definition	Signal Function
API 0 EN H	2BL1	This enable signal, one of four in the API system, is a dc level originating in the I/O processor and daisy chained from device to device on the same level. The M104 logic in each controller can interrupt this level, cutting the level off all devices that follow it on the bus. A device receives it as API 0 EN IN H and transmits it as API 0 EN OUT H.	Each device can post a request to its API level only if the incoming API EN level is true. By posting a request the device immediately inhibits all controllers below it on the bus. In this way priorities on each level are established when devices request simultaneously.
API 1 EN H	2BS1	Same as API 0 EN H	Same as API 0 EN H
API 2 EN H	2BH2	Same as API 0 EN H	Same as API 0 EN H
API 3 EN H	2BP2	Same as API 0 EN H	Same as API 0 EN H
API 0 GR H	2BJ1	One of four possible signals issued by the I/O processor indicating that it grants the API request at the corresponding level.	The device uses this signal to gate the address of its API entry location onto the I/O ADDR lines.
API 1 GR H	2BP1	Same as API 0 GR H	Same as API 0 GR H
API 2 GR H	2BE2	Same as API 0 GR H	Same as API 0 GR H
API 3 GR H	2BM2	Same as API 0 GR H	Same as API 0 GR H
API 0 RQ L	2BH1	One of four API request signals on channels 0–3. This signal is set by the device at I/O Sync time.	The device uses this signal to inform the I/O processor of its request for API priority level 0, the highest of the four.
API 1 RQ L	2BM1	Same as API 0 RQ L	Request API priority level 1.
API 2 RQ L	2BD2	Same as API 0 RQ L	Request API priority level 2.

Table 4-2 (Cont)
I/O Bus Signal Functions

Signal Mnemonic	Connector Pin Number	Signal Definition	Signal Function
API 3 RQ L	2BK2	Same as API 0 RQ L	Request API priority level 3.
DATA OFLO H	1BD1	This signal is gated onto the bus by the I/O processor during the third cycle of an add-to-memory operation when the sum (1's complement) of two like-signed numbers has an opposite sign.	This signal is used by the device to notify it when an incorrect sum occurs, because of overflow during an add-to-memory operation.
DCH EN H	2BV2	This enable signal is a dc level originating at the I/O processor and daisy chained from device to device. The M104 logic in each device can interrupt this level, cutting the level off all devices that follow on the bus. A device receives it as DCH EN IN H and transmits it as DCH EN OUT H.	Each device can post a DCH request only if the incoming DCH EN level is true. By posting a request, the device immediately inhibits all controllers below it on the bus. In this way priorities are established when devices request simultaneously.
DCH GR H	2BT2	Issued by the I/O processor when it acknowledges a device's DCH RQ L.	The device uses DCH GR to gate the address of its word count onto the I/O ADDR for 3-cycle transfers and gates memory address during 1-cycle transfers.
DCH RQ L	2BS2	A signed from a device to the I/O processor indicating either a request for a multicycle data channel transfer or, when posted with a single-cycle request, showing that an input transfer must be effected. The table below shows how the two functions relate. **DCH RQ L / SING CY RQ L / FUNCTION** 0 / 0 0 / 1 / Single Cycle Transfer Out 1 / 0 / Multi Cycle Transfer (In or Out) 1 / 1 / Single Cycle Transfer In	This signal is interpreted by the I/O processor in two ways: If it is present without a single-cycle request, it implies that some device wants to carry out a multicycle transfer, an increment memory, or add to memory. If a single-cycle request is also posted, then the two signals are ANDed to inform the I/O processor that a single-cycle transfer into memory is to be effected. Otherwise, the I/O processor assumes an outgoing single-cycle transfer is required.

Table 4-2 (Cont)
I/O Bus Signal Functions

Signal Mnemonic	Connector Pin Number	Signal Definition	Signal Function
DS0 H	2AD2	The first of six device select lines decoded from bit 6 of the IOT instruction.	This signal together with DS1-DS5 is decoded by the device select logic in the controller, which responds to its unique code only.
DS1 H	2AE2	The second of the six device select lines.	See DS0 H
DS2 H	2AH2	The third of the six device select lines.	See DS0 H
DS3 H	2AK2	The fourth of the six device select lines.	See DS0 H
DS4 H	2AM2	The fifth of the six device select lines.	See DS0 H
DS5 H	2AP2	The sixth of the six device select lines.	See DS0 H
INC MB L	2BD1	Forces the I/O processor to increment the contents of the memory location specified by the 15-bit address lines on the I/O bus.	This feature allows a device to increment memory locations in one cycle without disturbing the CPU.
I/O ADDR 03 L	1BH1	One of fifteen lines which constitute an input bus for devices which must deliver address data to the processor.	This address bus has two uses: a) To deliver the device's API entry location during its API break. b) To deliver the device's word count address during a multi-cycle DCH transfer, an increment memory operation, or add to memory. To deliver an absolute address during single-cycle transfers.
I/O ADDR 04 L	1BJ1	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L
I/O ADDR 05 L	1BJ1	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L
I/O ADDR 06 L	1BM1	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L

Table 4-2 (Cont)
I/O Bus Signal Functions

Signal Mnemonic	Connector Pin Number	Signal Definition	Signal Function
I/O ADDR 07 L	1BP1	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L
I/O ADDR 08 L	1BS1	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L
I/O ADDR 09 L	1BD2	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L
I/O ADDR 10 L	1BE2	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L
I/O ADDR 11 L	1BH2	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L
I/O ADDR 12 L	1BK2	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L
I/O ADDR 13 L	1BM2	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L
I/O ADDR 14 L	1BP2	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L
I/O ADDR 15 L	1BS2	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L
I/O ADDR 16 L	1BT2	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L
I/O ADDR 17 L	1BV2	Similar to I/O ADDR 03 L	Similar to I/O ADDR 03 L
I/O BUS 00 L	1AB1	The first of 18 data lines which constitute the bidirectional facility for transferring data in bytes of up to 18 bits between the device and either the CPU or memory. This is the MSB.	These data lines (I/O BUS 00 L through I/O BUS 17 L convey data between a) the AC of the CPU and a selected device information buffer register or b) the bus buffer of the I/O processor and a selected device buffer register during data channel operations.
I/O BUS 01 L	1AD1	Data line two	See I/O BUS 00 L

Table 4-2 (Cont)
I/O Bus Signal Functions

Signal Mnemonic	Connector Pin Number	Signal Definition	Signal Function
I/O BUS 02 L	1AE1	Data line three	See I/O BUS 00 L
I/O BUS 03 L	1AH1	Data line four	See I/O BUS 00 L
I/O BUS 04 L	1AJ1	Data line five	See I/O BUS 00 L
I/O BUS 05 L	1AL1	Data line six	See I/O BUS 00 L
I/O BUS 06 L	1AM1	Data line seven	See I/O BUS 00 L
I/O BUS 07 L	1AP1	Data line eight	See I/O BUS 00 L
I/O BUS 08 L	1AS1	Data line nine	See I/O BUS 00 L
I/O BUS 09 L	1AD2	Data line ten	See I/O BUS 00 L
I/O BUS 10 L	1AE2	Data line eleven	See I/O BUS 00 L
I/O BUS 11 L	1AH2	Data line twelve	See I/O BUS 00 L
I/O BUS 12 L	1AK2	Data line thirteen	See I/O BUS 00 L
I/O BUS 13 L	1AM2	Data line fourteen	See I/O BUS 00 L
I/O BUS 14 L	1AP2	Data line fifteen	See I/O BUS 00 L
I/O BUS 15 L	1AS2	Data line sixteen	See I/O BUS 00 L
I/O BUS 16 L	1AT2	Data line seventeen	See I/O BUS 00 L
I/O BUS 17 L	1AV2	Data line eighteen This is the LSB	See I/O BUS 00 L

Table 4-2 (Cont)
I/O Bus Signal Functions

Signal Mnemonic	Connector Pin Number	Signal Definition	Signal Function
I/O OFLO H	1BE1	This signal is issued during the first cycle of a multicycle data channel transfer or an increment memory cycle if the content (2's complement) of the word count assigned to the currently active data channel device becomes zero when incremented.	This signal indicates to the device that the specified number or words have been transferred at the completion of the transfer in progress. It is normally used to turn off the respective device and to initiate a program interrupt or API request.
IOP 1 H	2AD1	Microprogrammable control signal part of an IOT instruction-specified operation within a device. Decoded from bit 17 of the IOT.	Used for I/O skip instructions to test a device flag or other control functions. Cannot be used to read a device buffer register. In general, a designer should be wary of using IOP pulses for multiple purposes. Never clear and skip on a flag, with the same IOT, for example!
IOP 2H	2AE1	Same as IOP 1 H and it is also issued during a multicycle data channel transfer into memory. Decoded from bit 16 of the IOT.	Usually used to effect a transfer of data from a selected device to the processor or memory, to clear a device register, but may be used for other control functions. May not be used to determine a skip.
IOP 4 H	2AH1	Same as IOP 1 H and it is also issued during a multi- or single-cycle data channel transfer out of memory. Decoded from bit 15 of the IOT.	Usually used to effect transfer of data from the CPU or memory to the device or control. May not be used to determine a skip condition or to effect a transfer of data from a selected device to the CPU.
I/O PWR CLR H	2AS1	System clear signal generated in response to: 1) Power on or off 2) CAF instruction 3) I/O RESET key 1 mHz, 250-ns pulse width	This signal is treated as an initializing signal for all devices (controllers) attached to the I/O bus. All registers are reset to "initial" status.
I/O RUN H	2BB1	This level becomes high when the IPU is running.	Can be used to disable a device if the CPU stops.

Table 4-2 (Cont)
I/O Bus Signal Functions

Signal Mnemonic	Connector Pin Number	Signal Definition	Signal Function
I/O SYNC H	2AB1	The I/O processor clock pulse issued every microsecond; 1 mHz, 250-ns pulse width.	This signal is used to synchronize device control timing such as API RQ and DC H RQ to the I/O processor.
PROG INT RQ L	2AL1	This signal can cause the program to CAL to location 000000. The instruction resident in location 000001 is fetched and executed.	A device delivers this level to the I/O processor to request interruption of the program in progress in order that the device be serviced.
RD RQ L	2AM1	Indicates to the processor that the device is sending it a data word.	Used by the device to specify to the I/O processor an input-to-CPU data transfer is required.
RD STATUS H	2AP1	A signal issued when the CPU issues an IORS instruction or when the console switch is placed on I/O STATUS.	Used by the device to gate its status onto the I/O bus data lines (one line per status bit) which is then read into the AC of the CPU.
SD0 H	2AT2	The first of two subdevice select lines decoded from bit 12 of the IOT instruction.	This signal and DS1 H can be decoded by the device for mode selection.
SD1 H	2AV2	Same as SD0 H except it is decoded from bit 13 of the IOT instruction.	Same as SD0 H
SING CY	2AS2	Indicates when a device wants to carry out a single-cycle data transfer to memory.	This device uses this line to request from the I/O processor a single-cycle transfer. If a DCH RQ signal is sent with it, then the I/O processor responds to an input (to computer) transfer. Otherwise, it determines an output transfer.
SKIP RQ L	2AJ1	The return of the signal to the I/O processor during IOP 1 indicates that an IOT instruction test for a skip condition has been satisfied. The PC is subsequently incremented by one.	Used by a device to inform the program of the state of its interrupt flag. Also used in Single Cycle breaks as address line 01.

Table 4-2 (Cont)
I/O Bus Signal Functions

Signal Mnemonic	Connector Pin Number	Signal Definition	Signal Function
WR RQ L	2BB1	Indicates to the I/O processor that the device requires a transfer from memory during a multicycle data channel. Also used during Single Cycle breaks as address line 02.	The device uses this signal to inform the I/O processor that it wants a word from memory (during a multicycle data channel transfer). Also used during Single Cycle breaks as address line 02.
+1 → CA INH L	2BE1	If the I/O processor sees this signal during multicycle transfers, it inhibits normal incrementing of the device's assigned current address memory location.	This facility is used by such peripherals as DECtape and magnetic tape when they search for records. It is also useful during device checkout.

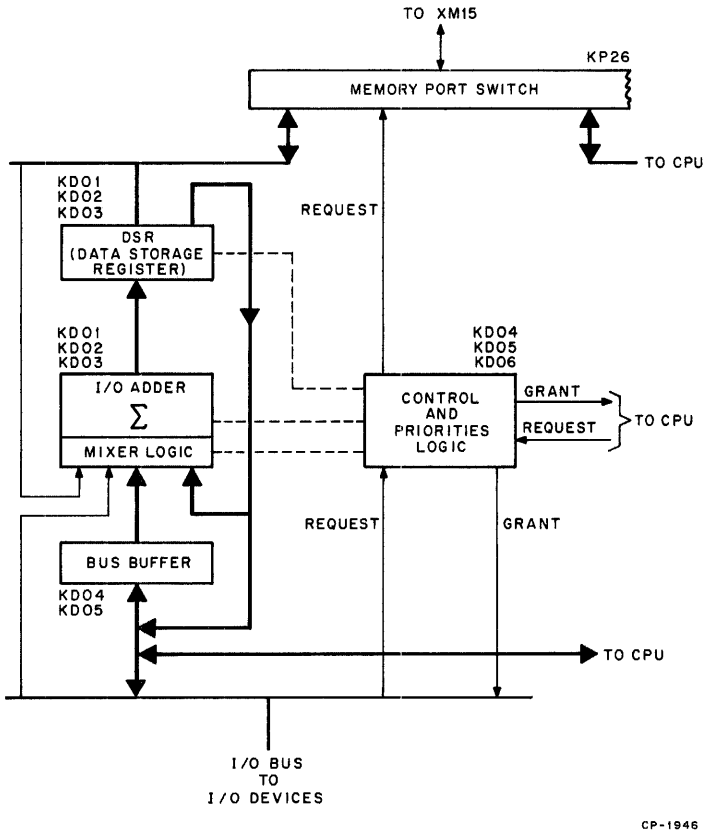


Figure 4-8 Data Channel Block Diagram

4.7 I/O TRANSFERS

4.7.1 Single Cycle Input Transfers

In utilizing this type of transfer, a device must first be synchronized to the I/O Processor, as described in Paragraph 4.3. Both address and data must then be transmitted over the I/O Bus to the I/O Processor. The processor then makes a memory request to store data.

In performing this operation (Figure 4-9), the address from the device is loaded into the DSR register and the data into the I/O buffer register. A memory write request is generated and, when the ADR ACK signal is returned from the XM15, the I/O buffer is loaded into the DSR, the DSR enabled on the MDL, the MRLS signal is sent back to the XM15 and the I/O cycle is terminated. Figure 4-10 is a flow diagram of single cycle input transfers.

If the active device maintains the request signal when the address is strobed into the DSR, a BACK to BACK transfer will be performed and another GRANT will be sent out to the device instead of terminating the cycle. The device can change its address and data when GRANT is removed from the bus, but it must have both enabled to the bus when GRANT becomes true again. Other devices are prevented from syncing because I/O SYNC is disabled from the bus.

After the device has taken all the breaks required (device word count register overflows), it may interrupt the I/O Processor through the PI or API system.

4.7.2 Single Cycle Output Transfers

For this type of transfer, a device after synchronizing with the I/O Processor, transmits its address over the I/O address lines. The I/O Processor requests the XM15 memory, reads the data from the XM15 memory, and transmits the data back out to the device.

Figure 4-11 shows a block diagram of this type of transfer in which the address is loaded into the DSR, a XM15 read request is made, the DSR is loaded with the memory data when RD RST is received and then enabled on the I/O Bus, and an IOP 4 is generated to load the data in the peripheral device.

Back-to-back transfers are detected in a similar manner as input transfers. Figure 4-12 is a detailed flow diagram of single-cycle output transfers.

4.7.3 Multicycle Input Transfers

Multicycle transfers rely on word count and current address registers located in the XM15 memory. For input transfers, the device specifies the word count location by an address on the I/O address lines and places the data on the I/O Bus. The I/O Processor increments both the word count and the current address location and writes the data into the XM15 memory location specified by the incremented current address location. This takes three I/O processor cycles and three memory cycles.

Figure 4-13 shows a block diagram of multicycle input transfers. The word count address, specified by the device on the I/O address lines, is loaded into the DSR and a memory read/pause/write cycle is requested. One is added to the data read from the XM15 memory; the result is loaded into the DSR and then rewritten into the XM15 memory. This is called the Word Count Cycle. The address on the I/O address lines is then incremented by one to point to the current address location, loaded into memory, and another read/pause/write cycle is requested. The data from the XM15 memory is incremented by one, loaded into the DSR, and written back into memory. This is the Current Address Cycle. The number now in the DSR points to the address into which data is to be written. Data from the device is loaded into the I/O buffer during the Current Address Cycle by IOP 2. A memory write request is now made, and then ADR ACK is received from the XM15, the I/O buffer is loaded into the DSR, and the data written into the XM15 memory. The I/O cycle is then terminated.

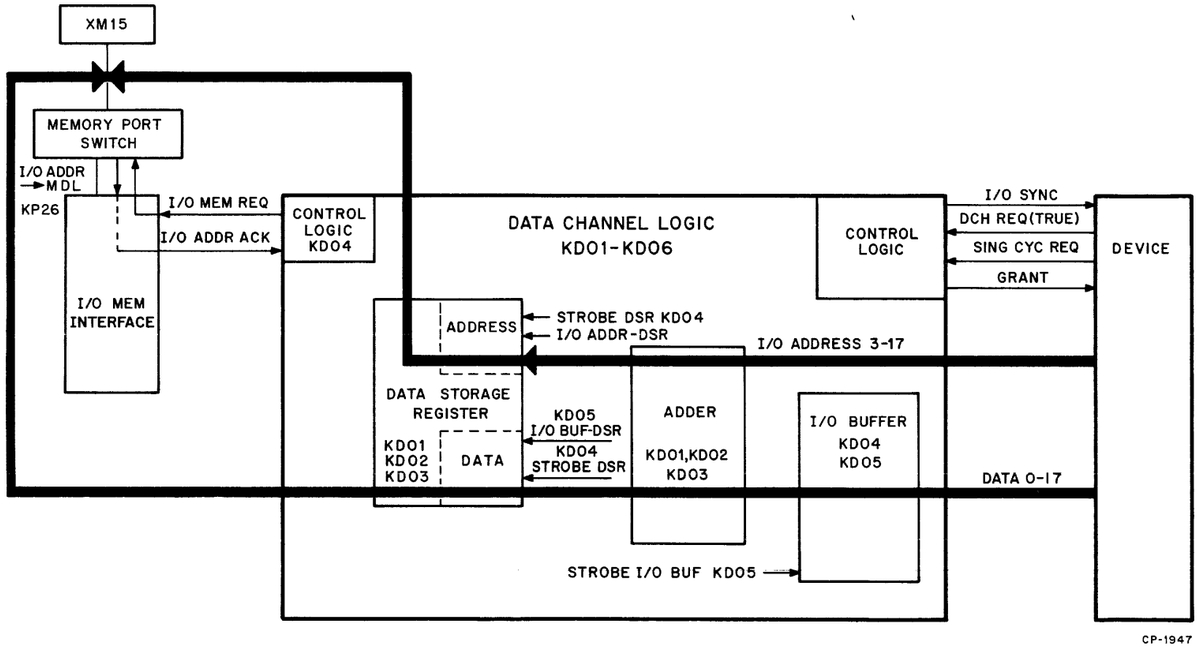
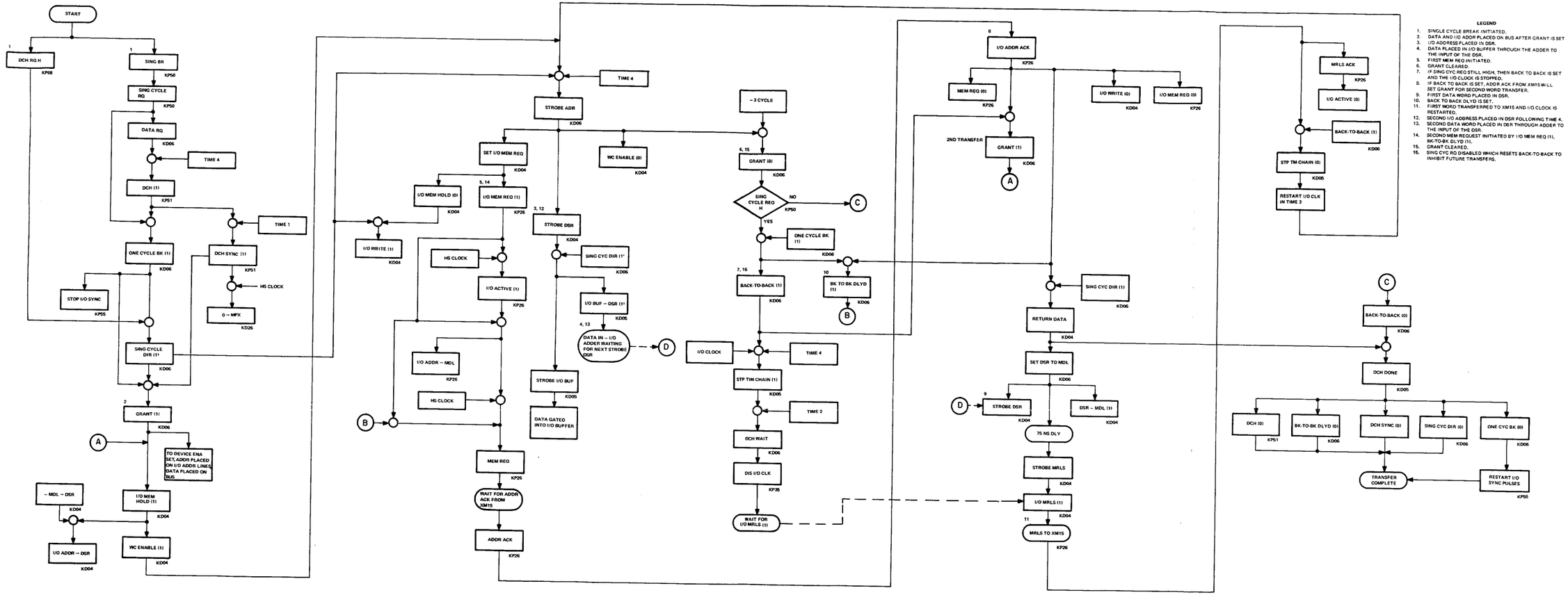


Figure 4-9 Single Cycle Data In Transfer Block Diagram



LEGEND

1. SINGLE CYCLE BREAK INITIATED.
2. DATA AND I/O ADDR PLACED ON BUS AFTER GRANT IS SET
3. I/O ADDRESS PLACED IN DSR.
4. DATA PLACED IN I/O BUFFER THROUGH THE ADDER TO THE INPUT OF THE DSR.
5. FIRST MEM REQ INITIATED.
6. GRANT CLEARED.
7. IF SING CYC REQ STILL HIGH, THEN BACK TO BACK IS SET AND THE I/O CLOCK IS STOPPED.
8. IF BACK TO BACK IS SET, ADDR ACK FROM XM15 WILL SET GRANT FOR SECOND WORD TRANSFER.
9. FIRST DATA WORD PLACED IN DSR.
10. BACK TO BACK DLYD IS SET.
11. FIRST WORD TRANSFERRED TO XM15 AND I/O CLOCK IS RESTARTED.
12. SECOND I/O ADDRESS PLACED IN DSR FOLLOWING TIME 4.
12. SECOND DATA WORD PLACED IN DSR THROUGH ADDER TO THE INPUT OF THE DSR.
14. SECOND MEM REQUEST INITIATED BY I/O MEM REQ (1), BK-TO-BK DLYD (1).
15. GRANT CLEARED.
16. SING CYC RQ DISABLED WHICH RESETS BACK-TO-BACK TO INHIBIT FUTURE TRANSFERS.

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Figure 4-10 Single Cycle Data In Transfer Detailed Flow Chart

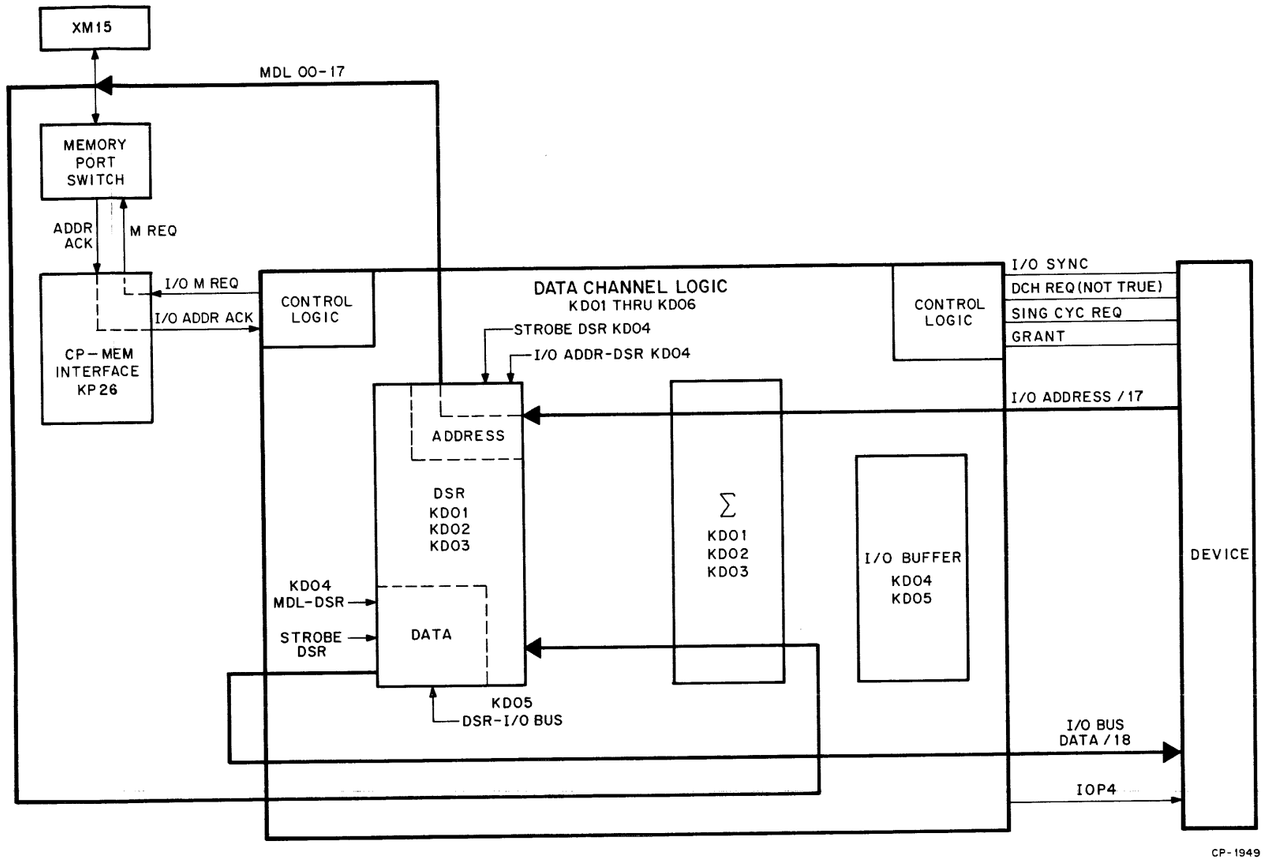
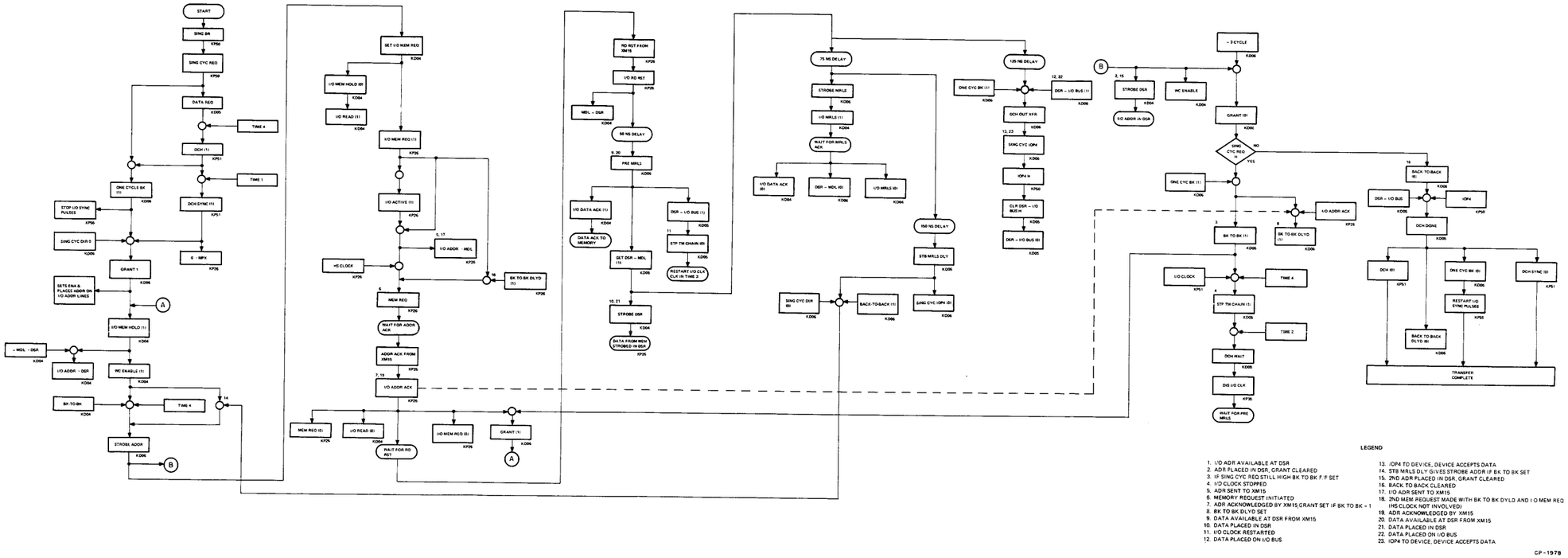


Figure 4-11 Single Cycle Data Out Transfer Block Diagram



LEGEND

1. I/O ADR AVAILABLE AT DSR
2. ADR PLACED IN DSR, GRANT CLEARED
3. IF SING CYC REQ STILL HIGH BK TO BK F/F SET
4. I/O CLOCK STOPPED
5. ADR SENT TO XM15
6. MEMORY REQUEST INITIATED
7. ADR ACKNOWLEDGED BY XM15,GRANT SET IF BK TO BK = 1
8. BK TO BK DLYD SET
9. DATA AVAILABLE AT DSR FROM XM15
10. DATA PLACED IN DSR
11. I/O CLOCK RESTARTED
12. DATA PLACED ON I/O BUS
13. IOP4 TO DEVICE, DEVICE ACCEPTS DATA
14. STB MRLS DLY GIVES STROBE ADDR IF BK TO BK SET
15. 2ND ADR PLACED IN DSR, GRANT CLEARED
16. BACK TO BACK CLEARED
17. I/O ADR SENT TO XM15
18. 2ND MEM REQUEST MADE WITH BK TO BK DYLD AND I/O MEM REQ (HS CLOCK NOT INVOLVED)
19. ADR ACKNOWLEDGED BY XM15
20. DATA AVAILABLE AT DSR FROM XM15
21. DATA PLACED IN DSR
22. DATA PLACED ON I/O BUS
23. IOP4 TO DEVICE, DEVICE ACCEPTS DATA

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Figure 4-12 Single Cycle Data Out Transfer Detailed Flow Chart

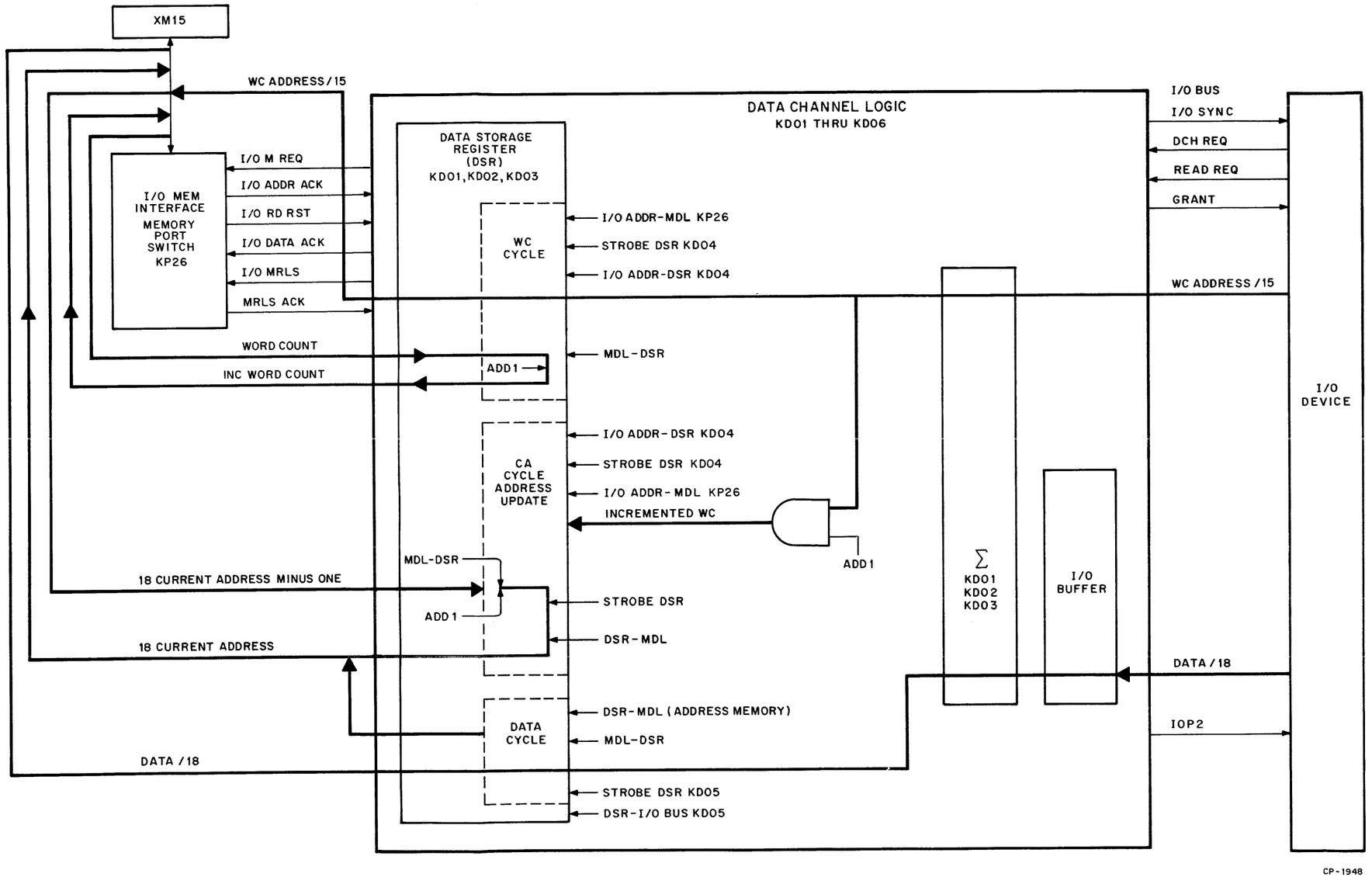


Figure 4-13 Multicycle Data In Transfer Block Diagram

If the word count register has overflowed when it was incremented (there was a carry), an I/O OFLO signal is sent to the device to prevent it from requesting another break. The current request in progress is completed. Refer to Figure 4-14 for a timing diagram and to Figure 4-15 for a detailed flow diagram.

4.7.4 Multicycle Output Transfers

Output transfers use the word count and current address location as the input transfer. The data is fetched from the XM15 memory and loaded into the device in the third cycle.

Both the word count and current address cycles are similar to the input transfers. Figure 4-16 is a block diagram of the multicycle output transfer. During the data cycle a memory read request is made and the I/O Processor is stopped. When the data is read from the XM15 memory into the DSR, the I/O Processor is restarted, data in the DSR is put onto the I/O Bus, and an IOP 4 generated to load the data into the device. Figure 4-17 is a detailed flow chart of the multicycle output transfers.

4.8 I/O AND MEMORY TRANSFERS

4.8.1 Add To Memory

This feature is similar to the multicycle transfers, but differs in that during the data cycle, data from the XM15 memory is added to data from the device and written into the XM15 memory and transmitted to the device.

A read/pause/write cycle is requested in the data cycle and, when data is available from the XM15 memory, it is enabled through one input on the DSR adder while the I/O buffer is enabled through the other and the DSR is then loaded with the result. The data is then rewritten into the XM15 memory, enabled onto the I/O Bus, and an IOP 4 is generated to load the device buffer, if desired. This type of cycle is performed by the device enabling both RD RQ and WR RQ on the I/O Bus.

4.8.2 Increment Memory

This feature increments a memory location in one I/O Processor cycle. Only the Word Count Cycle of a multicycle break is performed. The location specified by the address on the I/O address line is incremented by one. Enabling the INC MB line on the I/O Bus, along with DCH REQ, will cause this type of cycle.

4.8.3 Inhibit Increment Current Address

This line on the I/O Bus inhibits the current address from being incremented. ADD ONE is not turned on during the data portion of the current address cycle.

4.9 PROGRAM INTERRUPT

The Program Interrupt facility has two IOTs associated with it:

ION 700042 Enable the PI
IOF 700002 Disable the PI

When the PI is disabled, the computer does not respond to any Program Interrupt Requests (PROG INT RQ). However, when the PI is enabled, an interruption of normal program flow will occur. Upon receipt of a PROG INT RQ, the computer proceeds to complete its present instruction before interrupting. At clock time TS02, Phase 3 and Set Fetch of an instruction, interrupt acknowledge (INTRPT ACK – KP35) is set. This causes RUN to be cleared at TS03, Phase 3, preventing the CP from continuing. During TS03, the I/O address lines are placed on the A Bus. The lines should contain all zeros. At clock time TS03, a PI REQ is raised. PI is set at TIME 4 and PI SYNC at TIME 1. On the next TIME 4, INTERRUPT STB is issued, which loads the MO with the I/O address, sets INTERRUPT STATE, and sets START RUN allowing the CP timing to continue. The IR is cleared at TS01, forcing the CP to do a CAL. However, the CAL is to location zero because the MO was loaded with zero.

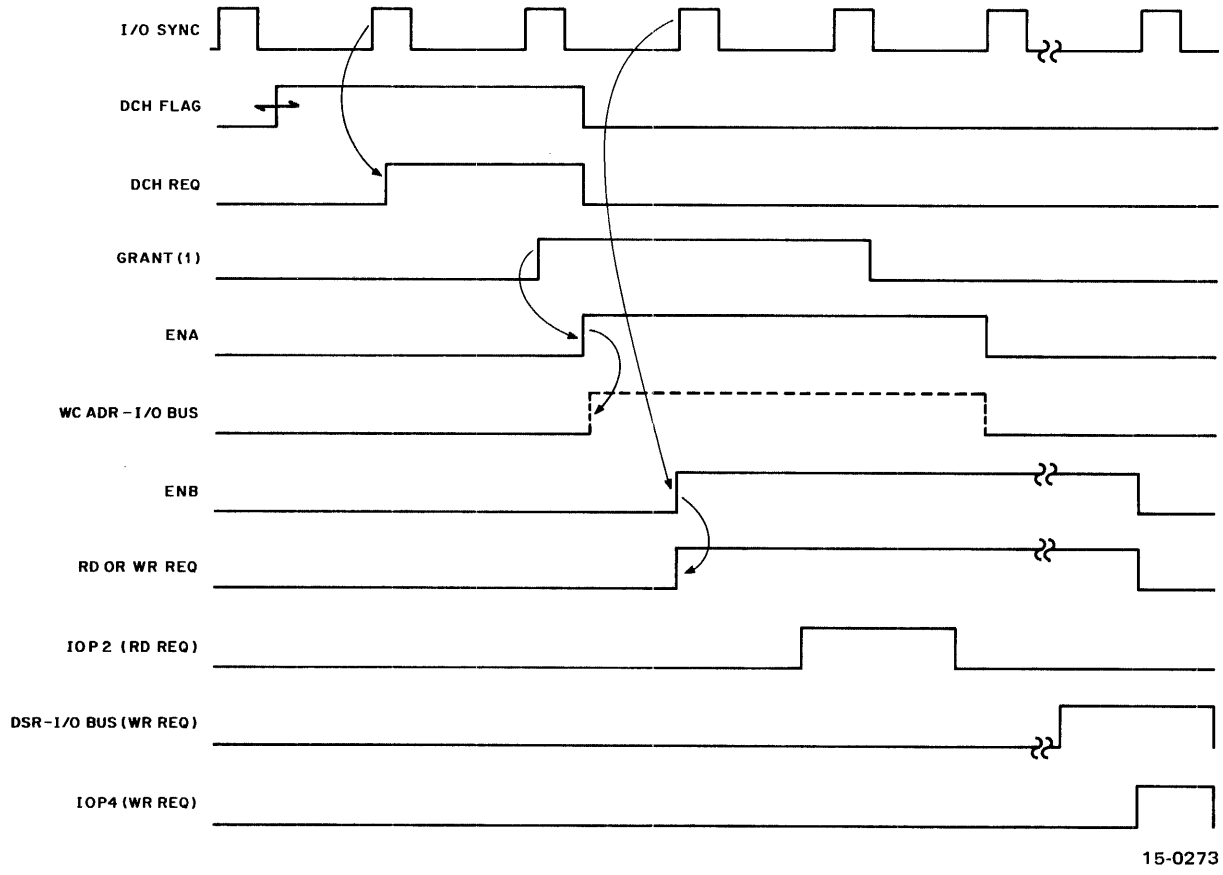
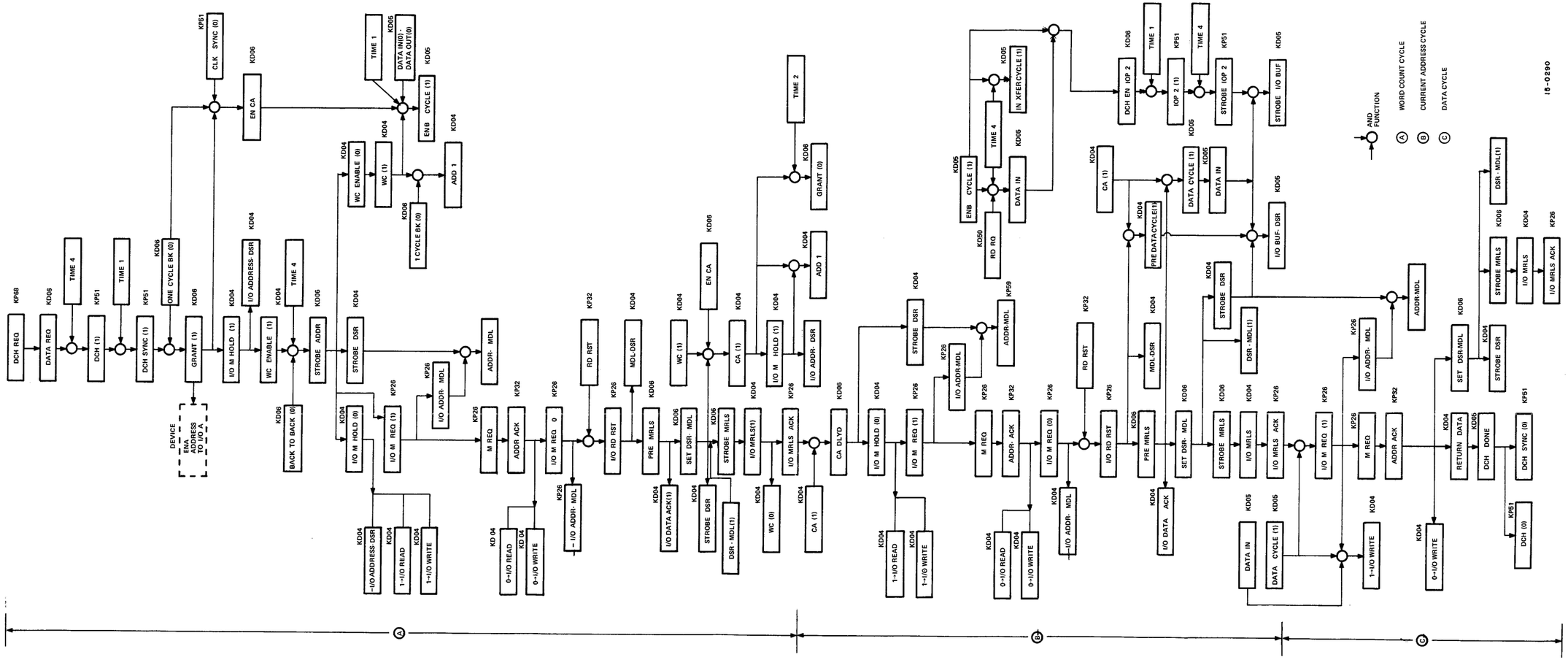


Figure 4-14 Multicycle Timing Diagram



re 4-15 Multicycle Data In Transfer Detailed Flow Chart

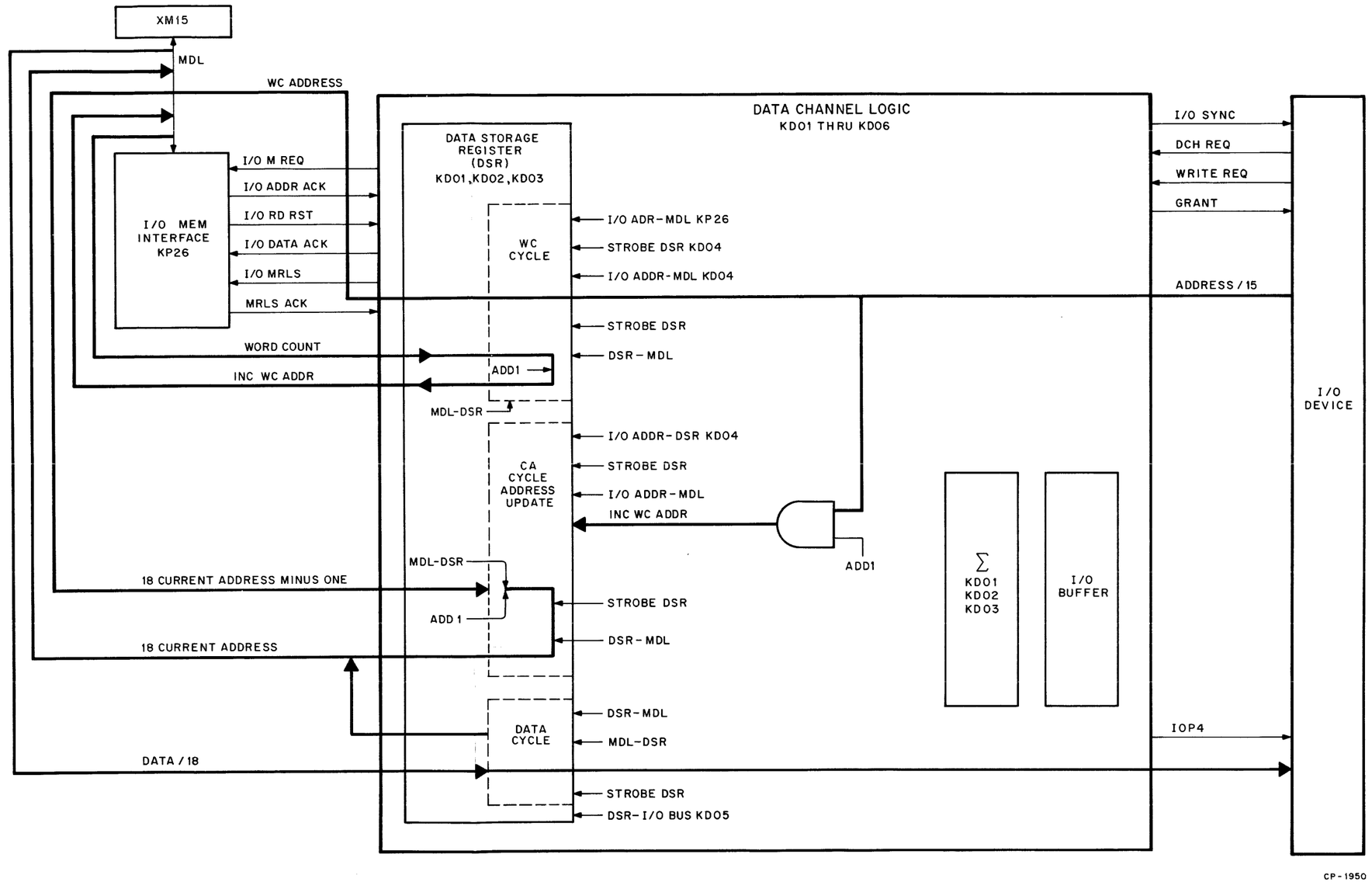


Figure 4-16 Multicycle Data Out Transfer Block Diagram

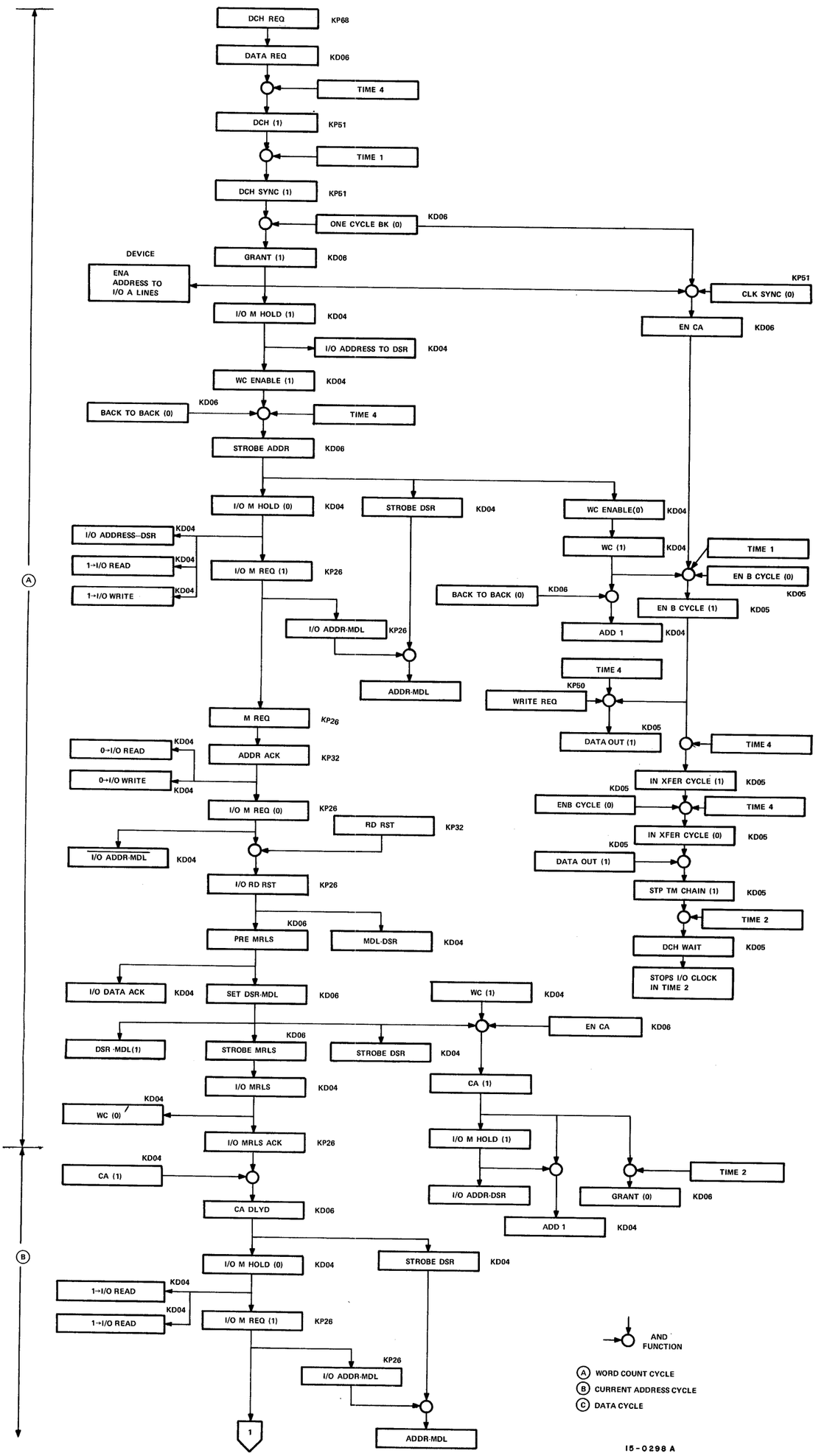


Figure 4-17 Multicycle Data Out Transfer Detailed Flow Chart (Sheet 1 of 2)

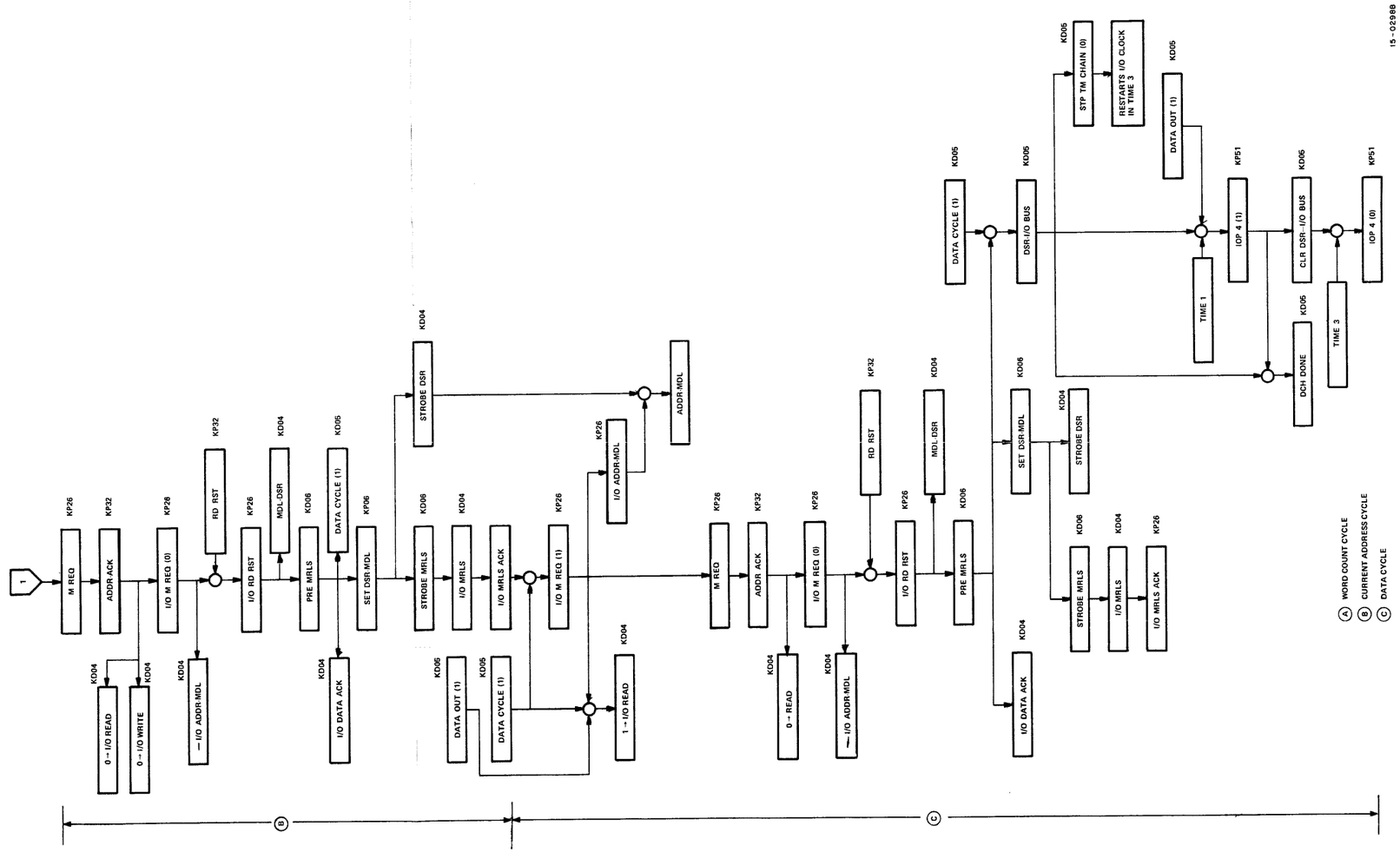


Figure 4-17 Multicycle Data Out Transfer
Detailed Flow Chart (Sheet 2 of 2)

CHAPTER 5
AUXILIARY CPU FUNCTIONS AND OPTIONS

5.1 INTRODUCTION

This chapter describes auxiliary CPU functions of the XVM System and options which may be purchased and added to the System to enhance its performance.

Auxiliary CPU functions are:

KE15-C Extended Arithmetic Element (EAE);
KW15 Real-Time Clock
KF15 Power Fail
PC15 High-Speed Paper-Tape Reader/Punch
and the Console Terminal Control.

XVM System options are:

LT15-A Teletype Interface and
VP15 Display Control.

5.2 KE15-C EXTENDED ARITHMETIC ELEMENT (EAE)

The KE15-C Extended Arithmetic Element (EAE) facilitates high-speed multiplication, division, shifting, normalizing, and register manipulation.

The EAE enables fast, flexible, hardware execution of the following signed or unsigned functions.

a. Shifting the contents of the primary arithmetic registers (AC MQ) right or left, requires 2.9 to 5.2 μs.

b. Normalizes the quantity in the primary arithmetic registers, i.e., shifts the contents left to remove leading binary zeros (or ones in the case of negative numbers) for the purpose of preserving as many significant bits as possible. The time required is 2.9 – 5.2 μs.

c. Multiplication is performed in 2.75 – 6.4 μs.

d. Division, including integer divide and fraction divide, requires 2.75 to 6.6 μs. Divide overflow indication is furnished by the link when signed division produces a quotient exceeding 377777_8 in magnitude, or unsigned in division produces a quotient exceeding 777777_8 in magnitude.

e. Basic setup instructions to manipulate the data in the registers prior to execution of the above instructions require 1.3 μs.

5.2.1 General Operation

Control logic for the KE15-C consists of a 6-bit event time counter, an instruction decoder, bus control circuitry, load signals, an instruction register, quotient detection circuitry, and other control flip-flops. In addition to this control logic, there is an 18-bit MQ/shift register.

During event time A, AC modifications occur; MQ transfers happen at time B; AC transfers occur at time C; nothing takes place at time D. All shifting occurs at time E; complementing takes place at event time F for multiply and divide operations, if necessary. For further information, refer to EAE flow drawing KE06.

There are four types of EAE instructions: SETUP, SHIFT, MULTIPLY, and DIVIDE. SETUP instructions use only four event times, while SHIFT, MULTIPLY, and DIVIDE instructions use all six event times.

Figure 5-1 is a general flow diagram for EAE instructions. Table 5-1 lists EAE instructions and Table 5-2 lists EAE microinstructions.

5.2.2 Normalize Instructions

The NORM and NORMS instructions are commonly used within a subroutine to convert an integer into a fraction and exponent for use in floating-point arithmetic. The algorithm for normalize is to shift the contents of the AC and MQ left until AC00 differs with AC01. For signed, normalize positive numbers, this results in AC00 (0) and AC01 (1). For signed, normalized numbers, the sign (AC00) is first duplicated in the link. For unsigned numbers, the link is usually initialized to 0. In both cases, the content of MQ00 enters AC17, the content shifted out of AC00 is lost, and the content of the link enters MQ17, on each shift. When shifting halts, the contents of the SC reflects the number of shifts executed to reach the normalized condition. The SC contents are available through the use of the EAE OSC or EAE LACS instruction.

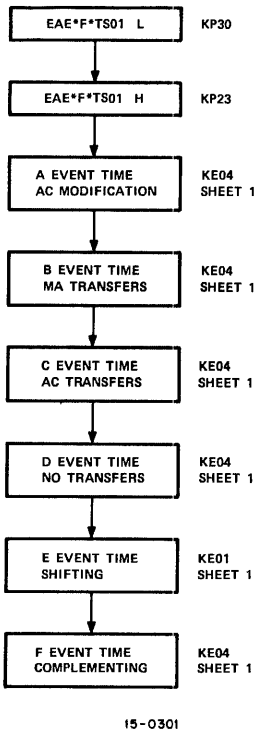


Figure 5-1 EAE General Flow Diagram

Table 5-1
EAE Instructions

Octal Code*	Mnemonic	Operation
640000	EAE	Basic EAE instruction. Acts as an NOP instruction.
640001	OSC	Inclusive-OR the SC with the AC.
640002	OMQ	Inclusive-OR the MQ with the AC.
640004	CMQ	Complement the MQ.
641001	LACS	Load AC12 through 17 with the contents of the SC.
641002	LACQ	Load the AC with the contents of the MQ.
644000	ABC	Get the absolute value of the AC.
650000	CLQ	Clear the MQ.
652000	LMQ	Load the MQ with the contents of the AC.
664000	GSM	Get the sign and magnitude of the AC.
6405XX	LRS	Long right shift.
6605XX	LRSS	Long right shift, signed.
6406XX	LLS	Long left shift.
6606XX	LLSS	Long left shift, signed.
6407XX	ALS	Accumulator left shift.
6607XX	ALSS	Accumulator left shift, signed.
640444	NORM	Normalize.
660444	NORMS	Normalize, signed.
6531XX	MUL	Multiply.
6571XX	MULS	MULTIPLY, signed.
6403XX	DIV	Divide.
6443XX	DIVS	Divide, signed.
6533XX	IDIV	Integer divide.
6573XX	IDIVS	Integer divide, signed.
6503XX	FRDIV	Fraction divide.
6543XX	FRDIVS	Fraction divide, signed.

*"XX" indicates the number to be loaded into step counter and depends upon the number of shifts required or answer precision required.

Table 5-2
EAE Microinstructions

Bit	Binary Code	Function
0, 1, 2, 3	1101	SETUP instruction.
4	1	Enters AC00 into the Link for signed operations.
5	1	Clears the MQ.
6	1	Reads AC00 into the EAE SIGN register prior to a signed multiply or divide operation.
6, 7	10	Takes the absolute value of the AC after the AC00 bit is read into the EAE SIGN register.

Table 5-2 (Cont)
EAE Microinstructions

Bit	Binary Code	Function
7	1	Inclusive-ORs the AC with the MQ and places the result in the MQ.
8	1	Clears the AC.
9, 10, 11	000	SETUP instruction code. Accompanies code in bits 15, 16, 17.
9, 10, 11	001	MUL instruction code.
9, 10, 11	010	Unused instruction code.
9, 10, 11	011	DIV instruction code.
9, 10, 11	101	LONG RIGHT SHIFT instruction code.
9, 10, 11	110	LONG LEFT SHIFT instruction code.
9, 10, 11	100	NORMALIZE instruction code.
9, 10, 11	111	ACCUMULATOR LEFT SHIFT instruction code.
12–17		Specifies the step count for all EAE codes (9–11) except SETUP.
15	1	For SETUP instruction code only, complements the MQ contents.
16	1	For SETUP instruction code only, inclusive-ORs the MQ with the AC and places the result in the AC.
17	1	For SETUP instruction code only, inclusive-ORs the AC with the SC and places the result in the AC.

For normalized numbers, the binary point is assumed to be between AC00 and AC01. The value of the exponent is in the SC. The number in the SC, after normalization, is actually the sum of the preestablished characteristic and the exponent (n) in 2's complement form. The characteristic is a number equivalent to the total number of bit positions in the AC and MQ, 36_{10} or 44_8. The NORMS instruction contains this number in bits 12–17 and loads it into the SC in 2's complement to establish the exponent in excess 44 code. This means that the exponential range of the fraction when normalized is 2^0 to 2^{35}, or $-44_8 + n$.

For example, if the integer +3 is stored in the MQ (MQ16, MQ17 are 1s) and it is desired to convert this to a fraction and exponent, the following program sequence is required.

```
NORM(S)      /NORMALIZE CONTENTS OF AC, MQ
DAC          /DEPOSIT AC IN MEMORY
LACQ         /MOVE MQ TO AC
DAC          /DEPOSIT MQ IN MEMORY
LACS         /MOVE SC TO AC
TAD (44      /SUBTRACT CHARACTERISTIC FROM STEP COUNT
DAC          /DEPOSIT RESULT (EXPONENT) IN MEMORY
```

In the process of normalization, a total of 33 shifts is required to shift MQ16(1) into AC01. This leaves the SC with a step count of:

```
011100    initialized step count
100001    plus 33 steps

111101    final step count
```

Because the step count is in 2's complement, the TAD 44_8instruction (2's complement add) in effect subtracts the characteristic from the final step count to arrive at the exponent:

```
111101    final step count
100100    TAD Characteristic

100001    exponent
```

In order to save the contents of the SC after a NORM instruction, if an interrupt occurs, an interrupt is held off for 2 cycles after a NORM instruction. This allows time to store the SC. Restoration of the step counter requires that the 2's complemented quantity, taken from the SC at the time of interrupt, be complemented, then combined with the pseudo-NORM instruction. The step count following the TAD, AND operation below is one less (1's complement) than the actual value produced by the previous normalization (2's complement). Execution of the pseudo-NORM instruction, then, 2's complements the step count into the SC, and in shifting the AC and MQ left one bit position, adds the necessary 1 to the SC to produce the correctly restored step count (the 6404XX present in the AC from TAD, AND operation shifts to become 501XXX).

Restoration Program

```
LAC SCSAVE
XOR (77          /COMPLEMENT STEP COUNT
TAD (640401)     /DEVELOP PSEUDO-NORM
AND (640477      /DELETE POSSIBLE STEP COUNT OVERFLOW
DAC .+1          /PLACE NORM IN SEQUENCE
HLT              /STEP COUNT TO SC
LAC MQSAVE
LMQ              /LOAD THE MQ
LAC ACSAVE       /LOAD THE AC
DBR              /RESTORE PC, LINK, ETC.
JMP I SUBENTR
```

5.2.3 MUL(S) Instruction

The MUL(S) instruction multiplies the contents of the AC (multiplier) by the contents of the next sequential core memory location (multiplicand) to form a product in the AC and MQ.

Bits 12–17 in the instructions are usually programmed for a step count of $22_8(18_{10})$, representing the multiplication of one 18-bit quantity (the sign bit and 17 magnitude bits for MULS) by another to produce a 36-bit product. When full precision is not required, the step count may be decreased by subtracting the appropriate number n from the instruction code. The product is always scaled 18-n from MQ17. If n is programmed in the instruction, the 18-n lower bits in the long register are meaningless.

For a MUL instruction the link must previously have been initialized to 0. During the preparatory phase, the multiplier is transferred from the AC to the MQ, the AC is cleared, and the Step Counter (SC) is set to the 2's complement of bits 12–17 of the instruction. A core memory cycle reads the multiplicand into the MI. The arithmetic phase, executed as multiplication of one unsigned quantity by another (binary point of no consequence), halts when the SC counts up to 0 (Figure 5-2).

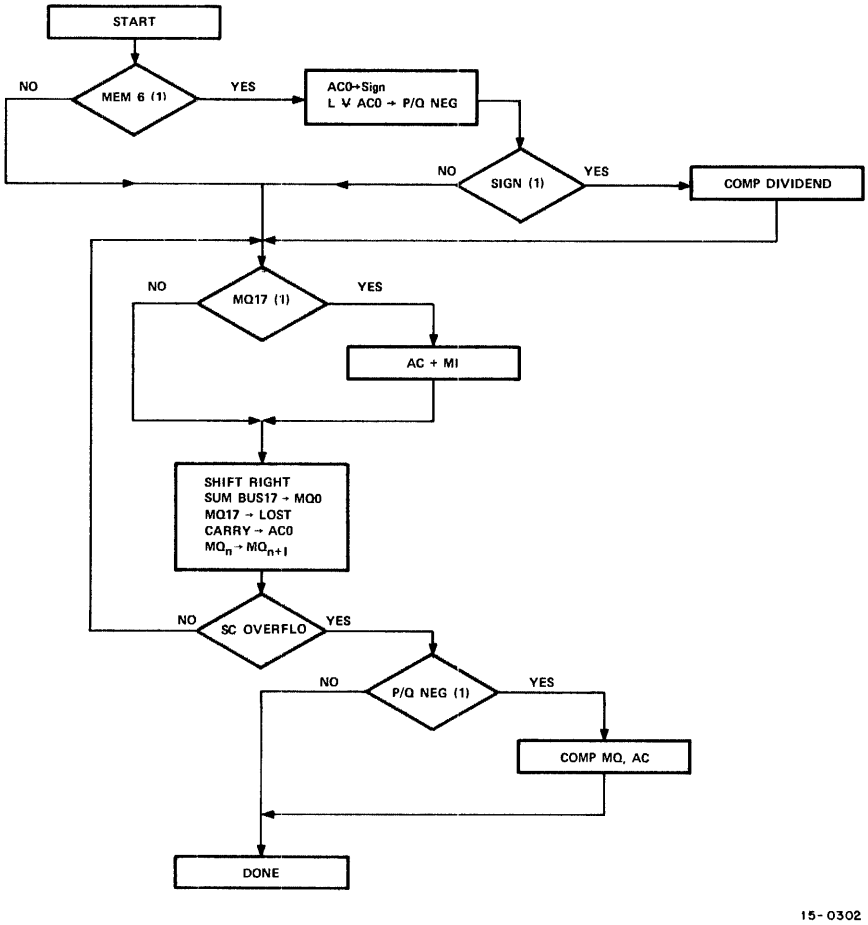


Figure 5-2 EAE Multiply Flow Diagram

For a MULS instruction, a previous LAC/GSM/DAC CAND sequence stores the absolute value of the multiplicand in memory and places the original sign of the multiplicand in the link. During the preparatory phase of MULS, a memory cycle reads the multiplicand into the MI, compares the link (sign of multiplicand) with AC00 (sign of multiplier) and sets the product quotient flip-flop if they differ and resets the link. The multiplier is transferred from the AC to the MQ and is complemented if negative, the AC is zeros, and the SC is initialized. The arithmetic phase is complete when the SC counts to 0. AC00 and AC01 each receive the sign of the product; the remaining AC and MQ bits represent the magnitude. If initially the multiplier and multiplicand had unlike signs [P/Q neg (1)], then the resulting MQ after the arithmetic operation would have been complemented.

The algorithm for multiplication using the EAE is simple: add and shift right. Each bit of the multiplier is sampled, starting with the least significant bit. If the sampled bit is a 1, the multiplicand is added to the partial product. The partial product and the multiplier are then shifted right one position for the next multiplier bit sampling. If the sampled bit is a zero, zeros are added to the partial product. With each shift the contents of the least significant bit are lost. Multiplication ends when the SC, up-counted with each shift, reaches 0.

Tables 5-3 through 5-17 illustrate the operations that take place in each instruction.

Programming Example

Multiply 2_8 x 5_8

```
START   200   200100   LAC CAND        /Load multiplicand into AC
        201   100500   JMS MPY         /Store main program address in 500
                                       /and jump to MPY subroutine
        202   200101   LAC PLIER       /Load multipler into AC
        203            /Main program re-entry
MPY     500   000202   PC              /Main program address
        501   664000   GSM             /Absolute value in AC
        502   040505   DAC .+3         /Deposit CAND in 505
        503   420500   XCT I MPY       /Load multiplier into AC
        504   657122   MULS            /Fetch I CAND I and multiply
        505   000002
        506   440500   ISZ PC          /Increment main program address
        507   620500   JMP I 500       /JMP to main program
CAND    100   000002   MULTIPLICAND
        101   000005   MULTIPLICAND
```

L	AC	MQ (multiplier)	MI (multiplicand)	SC	OPERATION
0	0000	0101	0010	1100	
	0010				ADD
	0010				
0	0001	0010	0010	1101	SHIFT
	0000				ADD
	0001				
0	0000	1001	0010	1110	SHIFT
	0010				ADD
	0010				
0	0001	0100	0010	1111	SHIFT
	0000				ADD
	0001				
0	0000	1010	0010	0000	SHIFT

ANSWER = 12_8

Table 5-3
EAE NOP 640000

CP State	Event Time	Functions	Drawings
TS02	A	---	---
TS02	B	MQ → MQ MQ1 → C L EAE LD MQ H	--- KE04, Sheet 1 KE04, Sheet 2
TS02	C	AC → AC EAE ENAB AC L EAE LD AC L	--- KE04, Sheet 2 KE04, Sheet 2
TS03	D	---	---

Table 5-4
OSC 640001

CP State	Event Time	Functions	Drawings
TS02	A	---	---
TS02	B	MQ → MQ MQ1 → C L EAE LD MQ H	--- KE04, Sheet 1 KE04, Sheet 2
TS02	C	EAE SC → C L AC → C BUS EAE LD AC	KE04, Sheet 1 KE04, Sheet 2 KE04, Sheet 2
TS03	D	---	---

Table 5-5
OMQ 640002

CP State	Event Time	Functions	Drawings
TS02	A	---	---
TS02	B	Same as NOP, Event Time B	---
TS02	C	C-MQ2L EAE ENAB AC L EAE LD AC L	KE04, Sheet 1 KE04, Sheet 2 KE04, Sheet 2
TS03	D	---	---

Table 5-6
CMQ 640004

CP State	Event Time	Functions	Drawings
TS02	A	- - -	- - -
TS02	B	MQ1 → C L EAE COMPCAL EAE LD MQ H	KE04, Sheet 1 KE04, Sheet 2 KE04, Sheet 2
TS02	C	Same as NOP, Event Time C	- - -
TS03	D	- - -	- - -

Table 5-7
LACS 641001

CP State	Event Time	Functions	Drawings
TS02	A	- - -	- - -
TS02	B	Same as NOP, Event Time B	- - -
TS02	C	EAE SC → C L EAE LD AC L	KE04, Sheet 1 KE04, Sheet 2
TS03	D	- - -	- - -

Table 5-8
LACQ 641002

CP State	Event Time	Functions	Drawings
TS02	A	- - -	- - -
TS02	B	Same as NOP, Event Time B	- - -
TS02	C	MQ2 → C L EAE LD AC L	KE04, Sheet 1 KE04, Sheet 2
TS03	D	- - -	- - -

Table 5-9
ABS 644000

CP State	Event Time	Functions	Drawings
TS02	A	EAE ENAB AC L EAE COMP ABS *A L IF AC00 EAE LD AC L	KE04, Sheet 2 KE04, Sheet 2 KE04, Sheet 1 KE04, Sheet 2
TS02	B	Same as NOP, Event Time B	---
TS02	C	Same as NOP, Event Time C	---
TS03	D	---	---

Table 5-10
CLQ 650000

CP State	Event Time	Functions	Drawings
TS02	A	---	---
TS02	B	MQ1 → C L EAE LD MQ H	KE04, Sheet 1 KE04, Sheet 2
TS02	C	Same as NOP, Event Time C	---
TS03	D	---	---

Table 5-11
LMQ 652000

CP State	Event Time	Functions	Drawings
TS02	A	---	---
TS02	B	EAE ENAB AC L EAE LD MQ H	KE04, Sheet 2 KE04, Sheet 2
TS02	C	Same as NOP, Event Time C	---
TS03	D	---	---

Table 5-12
GSM 664000

CP State	Event Time	Functions	Drawings
F*TS02	A	EAE ENAB AC L EAE COMP C → A L ABS*A L, if AC01(1) EAE LD AC L, if AC00(1), SET LINK	KE04, Sheet 2 KE04, Sheet 2 KE04, Sheet 1 KE04, Sheet 2
F*TS02	B	Same as NOP, Event Time B	---
F*TS02	C	Same as NOP, Event Time C	---
F*TS03	D	---	---

Table 5-13
LRS 6405XX and LRSS 6605XX

CP State	Event Time	Functions	Drawings
F*TS02	A	MEM4 (1) Λ AC00(1) 1 → L MI 12–17 → SC LOAD SC	 KP22 KE04, Sheet 2
F*TS02	B	Same as NOP, Event Time B	---
F*TS02	C	Same as NOP COUNT SC L (+1)	 KE05
F*TS03	D	---	---
EAE*TS01 EAE*TS02	E	LRS DECODED L → AC0, AC_n → AC_{n+1} AC 17 → MQ 00 MQ_n → MQ_{n+1} SC OVERFLO	KE04, Sheet 1 KP01–KP18 KE01 KE01, KE02 KE03, Sheet 1
EAE*TS03 EXECUTE	F	--- ---	--- ---

Table 5-14
LLS 6406XX and LLSS 6606XX

CP State	Event Time	Functions	Drawings
F*TS02	A	Same as LRS	---
F*TS02	B	Same as LRS	---
F*TS02	C	Same as LRS	---
F*TS03	D		---
EAE*TS01 EAE*TS02	E	LLS decoded L → MQ 17 $MQ_n \rightarrow MQ_{n-1}$ MQ00 → AC 17 $AC_n \rightarrow AC_{n-1}$ SC OVERFLO	KE04, Sheet 1 KE02 KE01, KE02 KP18 KP17 KE03, Sheet 1
EAE*TS03 EXECUTE	F ---	--- ---	--- ---

Table 5-15
ALS 6407XX and ALSS 6607XX

CP State	Event Time	Functions	Drawings
F*TS02	A	Same as LRS	---
F*TS02	B	Same as LRS	---
F*TS02	C	Same as LRS	---
F*TS03	D	---	---
EAE*TS01 EAE*TS02	E	ALS is decoded L → AC 17 $AC_n \rightarrow AC_{n-1}$ SC OVERFLO	KE04, Sheet 1 KP18 KP01–KP17 KE03, Sheet 1
EAE*TS03	F	---	---
EXECUTE	---	---	---

Table 5-16
NORM 640444 and NORMS 660444

CP State	Event Time	Functions	Drawings
F*TS02	A	Same as LLS	---
F*TS02	B	Same as LLS	---
F*TS02	C	Same as LLS	---
F*TS03	D	Same as LLS	---
EAE*TS01	E	NORMS decoded	KE04, Sheet 1
EAE*TS02		Same as LLS 1-F when normalized	KE03, Sheet 2
EAE*TS03	F	---	---

Table 5-17
MUL 6531XX and MULS 6571XX

CP State	Event Time	Functions	Drawings
F*TS02	A	MI 12–17-SC LD SC MI 06 (1)*AC00 (1) = 1-SIGN MI 06 (1)*L ≠ AC00 = 1-P/Q NEG	KE03, Sheet 1 KE04, Sheet 2 KE05 KE05
F*TS02	B	If SIGN (0): EAE ENAB AC EAE LD MQ H If SIGN (1): EAE ENAB AC EAE COMP C-A L EAE LD MQ H	 KE04, Sheet 2 KE04, Sheet 2 KE04, Sheet 2 KE04, Sheet 2 KE04, Sheet 2
F*TS02	C	If MI 08 (1): 0-AC	 ---
F*TS03	D	EAE ENAB AC L EAE LD AC L COUNT SC L (+1)	KE04, Sheet 2 KE04, Sheet 2 KE05

Table 5-17 (Cont)
MUL 6531XX and MULS 6571XX

CP State	Event Time	Functions	Drawings
EAE*TS01 EAE*TS02	E	EAE MUL decoded If MQ17 (1): EAE MI-B L EAE ENAB AC L EAE SHIFT RT H If MQ17 (0): EAE ENAB AC L EAE SHIFT RT L L-AC00 SUM BUS 17-MQ00 $MQ_n - MQ_{n-1}$ SUM BUS_n -AC_{n-1} EAE LD AC L EAE LD MQ H SC OVERFLO	KE04, Sheet 1 KE03, Sheet 2 KE04, Sheet 2 KE05 KE04, Sheet 2 KE05 KP01 KE01 KE01, KE02 KP02–KP18 KE04, Sheet 2 KE04, Sheet 2 KE03, Sheet 2
EAE*TS03	F	P/Q NEG (1): COMP MQ	KE04, Sheet 2

5.2.4 DIV(S) Instruction

The DIV(S) instruction (Table 5-18) divides the contents of the AC and MQ by the contents of the next sequential core memory location to form a quotient in the MQ and a remainder in the AC.

For a DIV(S) instruction, the link must previously have been set to 0 and remains 0 unless divide overflow occurs. During the preparatory phase, the step counter is set to the 2's complement of the step count in bits 12–17 of the instruction. Bits 12–17 of the instruction are usually programmed for a step count of 23_8 (19_{10}), unless full precision is not necessary. A core memory cycle takes place to read the division into the MI. The arithmetic phase, executed as the division of one unsigned quantity by another, halts when the SC counts up to zero (Figure 5-3).

For a DIVS instruction, a previous LAC/GSM/DAC/DUR sequence stores the absolute value of the divisor in memory and places the original sign of the divisor in the link. If AC00(1), the sign flip-flop is set; if L is unequal to AC00, the product quotient flip-flop is set. These flip-flops, if set, act to 1's complement the MQ and AC during the preparatory phase and to perform other complementary functions during the arithmetic phase to arrive at the correctly signed quotient, as shown on the EAE flow drawing KE15-0-06.

Table 5-18
DIV 6403XX and DIVS 6443XX

CP State	Event Time	Functions	Drawings
F*TS02	A	Same as MUL except if MI 06(1)*AC00(1)	
		COMPAC:	
		EAE ENAB AC L	KE05, Sheet 2
		EAE COMP C-A L	KE05, Sheet 2
		ABS*A L	KE04, Sheet 1
		EAE LD AC L	KE04, Sheet 2
F*TS02	B	SIGN (1): COMP MQ	
		C-MQ1L	KE04, Sheet 1
		EAE COMP, C-A L	KE04, Sheet 2
		EAE LD MQ H	KE04, Sheet 2
F*TS02	C	COUNT SC L(+1)	KE05
F*TS03	D	---	---
EAE*TS01	E	Check for divide overflow:	
EAE*TS02		carry on first or second	KE03, Sheet 2
		if DIV overflow set	
		LINK	KP22
		TEMP (0):	
		EAE-MI-B L	KE03, Sheet 2
		TEMP (1):	
		EAE MI-B L	KE03, Sheet 2
		EAE ENAB AC L	KE04, Sheet 2
		EAE SHIFT LEFT H	KE05
		SUM BUS 00-LINK	KP22
		SUM BUS_n -AC_{n-1}	KP01–KP18
		$MQ_n - MQ_{n-1}$	KE01, KE02
		Q-MQ 17	KE02
		Q-TEMP	KE05
		EAE LD AC L	KE04, Sheet 2
		EAE LD MQ H	KE04, Sheet 2
		SC OVERFLOW	KE03, Sheet 2
EAE*TS03	F	IF P/Q NEG (1):	
		COMP MQ	KE04, Sheet 2
		IF SIGN (1):	
		COMP AC	
		EAE ENAB AC L	KE04, Sheet 2
		MUL/DIV COMP H	KE04, Sheet 1
		EAE LD AC	KE04, Sheet 2

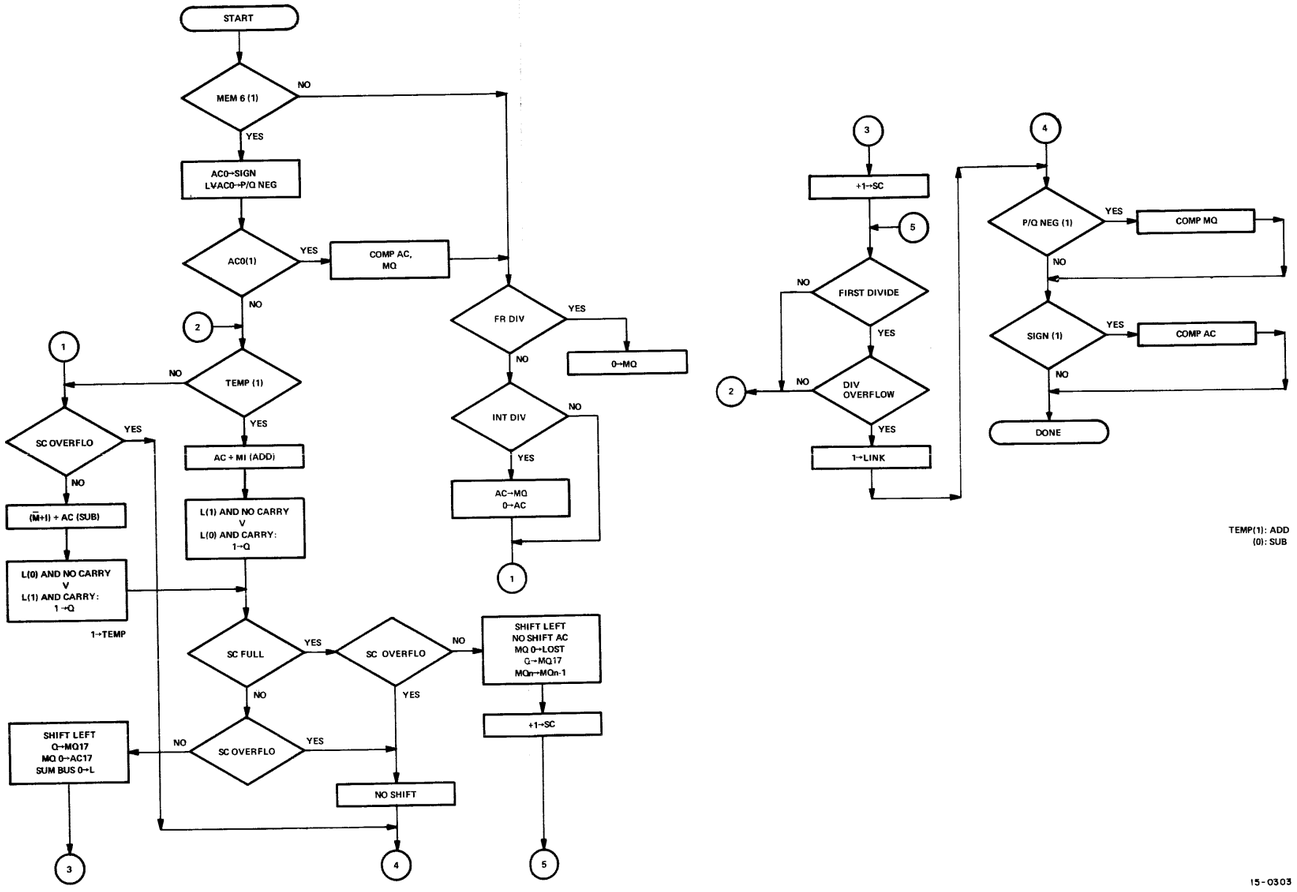


Figure 5-3 EAE Divide Flow Diagram

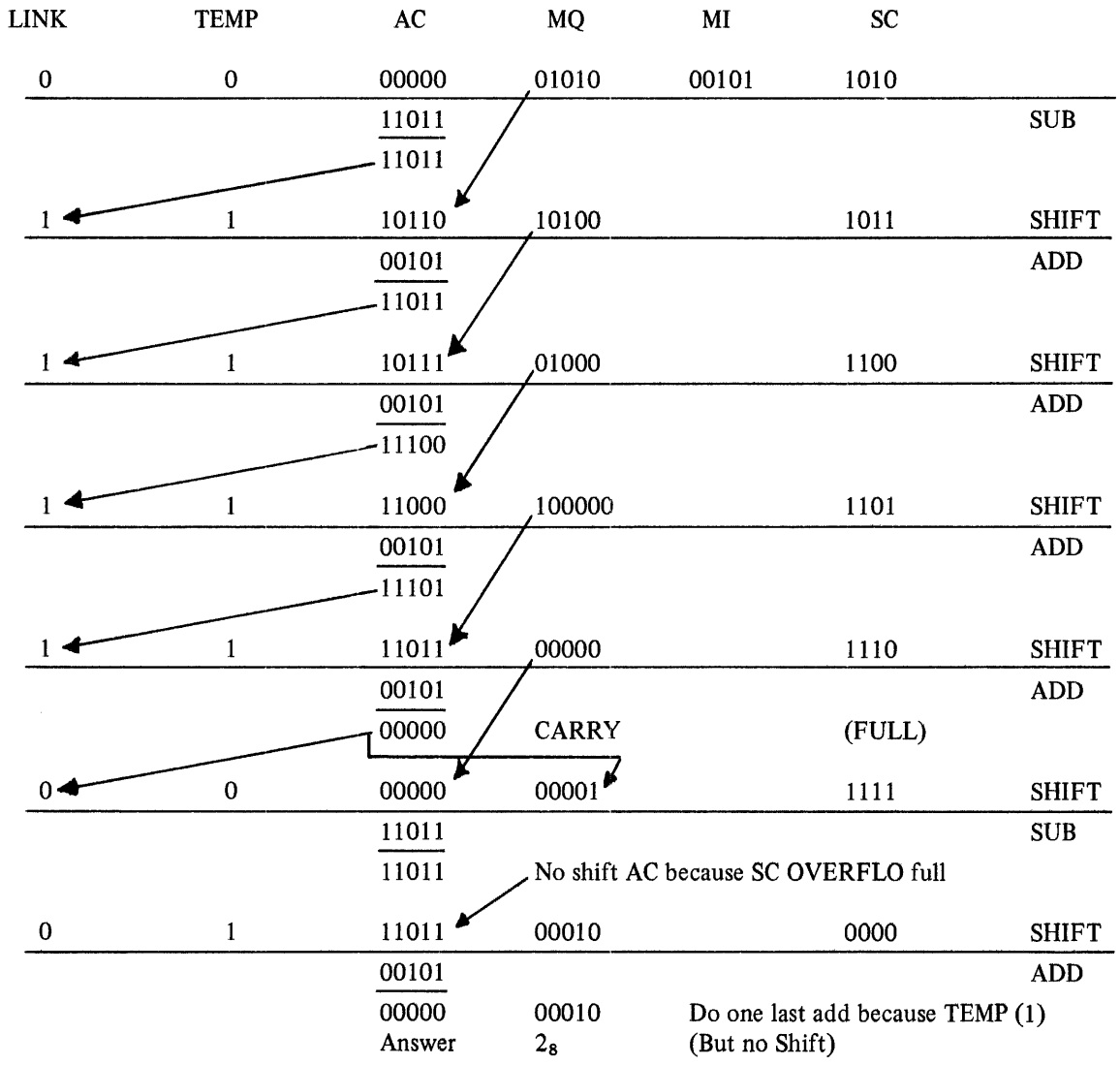
The algorithm for divide using the EAE is simple: add or subtract, and shift left. The divisor is first subtracted from the AC portion of the dividend, and the result is shifted left. If the result is a negative number [TEMP (1)], the divisor is added to the quotient; if the result is a positive number [TEMP (0)], the divisor is subtracted (2's complement add) from the quotient. The result is then shifted left one position for the next sampling. Divide overflow occurs, if in the first subtraction the divisor is not greater than the AC portion of the dividend. Divide overflow sets the link and stops the divide operation.

Programming Example

Divide $12_8 \div 5_8$

```
        500     200100  LAC DIVR        /Load divisor into AC
        501     100200  JMS DIV         /Store program address in 200 and jump
                                        /to DIV subroutine
        502                             /main program re-entry
DIV     200     502     PC              /program address
        201     664000  GSM             /Store DIVR sign in link and absolute
                                        /value in AC
        202     040207  DAC .+5         /Deposit DIVR in 207
        203     200101  LAC DIVD1       /Load half dividend into AC
        204     652000  LMQ             /Move to MQ
        205     200102  LAC DIVD2       /Load half dividend into AC
        206     644323  DIVS            /Fetch DIVR and divide
        207     000005
        210     620200  JMP I 200       /Return to main program
        100     000005  DIVR
        101     000012  DIVD1           /(Least significant)
        102     000000  DIVD2           /(Most significant)
```

Divide Example: 12 ÷ 5 = 2



5.2.5 IDIV(S) Instruction

The instruction IDIV(S) (Table 5-19) divides the contents of the AC (integer dividend) by the contents of the next sequential core memory location to form a quotient in the MQ and a remainder in the AC.

The arithmetic phase of the instruction(s) is identical to that of DIV(S). The preparatory phase transfers the contents of the AC to the MQ and clears the AC. Thereafter, the arithmetic phase, in reality, performs the division on the long register dividend first, as in DIV, with the exception that the most significant portion of the dividend (AC) is at 0.

5.2.6 FRDIV(S) Instruction

The FRDIV(S) instruction (Table 5-20) divides the contents of the AC (fraction dividend) by the contents of the next sequential core memory location and forms a quotient in the MQ and a remainder in the AC.

Table 5-19
IDIV 6533XX and IDIVS 6573XX

CP State	Event Time	Function	Drawings
F*TS02	A	Same as MUL	See MUL
F*TS02	B	Same as MUL	See MUL
F*TS02	C	Same as MUL	See MUL
F*TS03	D	---	---
EAE*TS01 EAE*TS02	E	Same as DIV	See DIV
EAE*TS03	F	Same as DIV	See DIV

Table 5-20
FRDIV 6503XX and FRDIVS 6543XX

CP State	Event Time	Function	Drawings
F*TS02	A	Same as DIV	See DIV
F*TS02	B	0-MQ: MQ1-C L EAE LD MQ H	 KE04, Sheet 1 KE04, Sheet 2
F*TS02	C	Same as DIV	See DIV
F*TS03	D	---	---
EAE*TS01 EAE*TS02	E	Same as DIV	See DIV
EAE*TS03	F	Same as DIV	See DIV

The arithmetic phase of the instruction (S) is identical to that of the DIV(S). The preparatory phase clears the MQ. The arithmetic phase is a division of the long register with the MQ at 0. For FRDIV, the binary point is assumed at the left of AC00; for FRDIVS, the binary point is assumed between AC00 and AC01.

5.2.7 Indicators

The 18-bit MQ register, 7-bit step counter (6-bits, plus overflow), and an 18-bit EAE register are all accessible from the rotary indicator switch. The EAE switch position indicates the complement of 18 control functions. Table 5-21 lists these signals and their bit.

Table 5-21
EAE Indicators

Bit	Signal
0	A (0) H
1	B (0) H
2	C (0) H
3	D (0) H
4	E (0) H
5	F (0) H
6	-SU H
7	-EAE MUL H
8	-EAE DIV SHIFT H
9	-EAE NORMS H
10	-EAE LRS H
11	-EAE LLS H
12	-EAE ACLS H
13	EAE SIGN (0) H
14	EAE P/Q NEG (0) H
15	DIV OVERFLOW (0) H
16	-EAE FULL H
17	EAE NO SHIFT H

5.2.8 EAE Execution Times

Setup	1.32 μs
Shifts	2.75 μs + 130 ns/step
MUL + DIV	2.75 μs + 260 ns/step

5.3 KW15 REAL-TIME CLOCK

The KW15 Real-Time Clock, when enabled, increments location 00007 at a rate specified by a clock in module slot L03. The M501 module, supplied with the XV100, increments every 16.7 ms in 60 Hz systems and every 20 ms in 50 Hz systems. An M401 variable clock may be used instead of the M501.

The IOTs for the Real-Time Clock are:

CLSF	700001	Skip if Clock flag is set
CLOF	700004	Clear Clock Flag and disable clock
CLON	700044	Clear Clock Flag and enable clock

When the CLON IOT is executed, the CLK EN flip-flop is set (see KP57). This enables the CLK REQ flip-flop to be set at the clock frequency if the console is locked or the CLK switch on the console is enabled (front of switch depressed). The CLK REQ is synchronized to the I/O, as described in Chapter 4, and a DCH word count cycle is used to increment location 00007.

When location 00007 increments from all 1s to all 0s, a clock overflow occurs and the CLK FLAG is set. This flag is interfaced to the PI and API whose entry address is 51. The clock will continue to count up from zero, after overflow, until location 00007 is reinitialized or the clock is turned off. Figure 5-4 is a flow diagram of the Real-Time Clock operation.

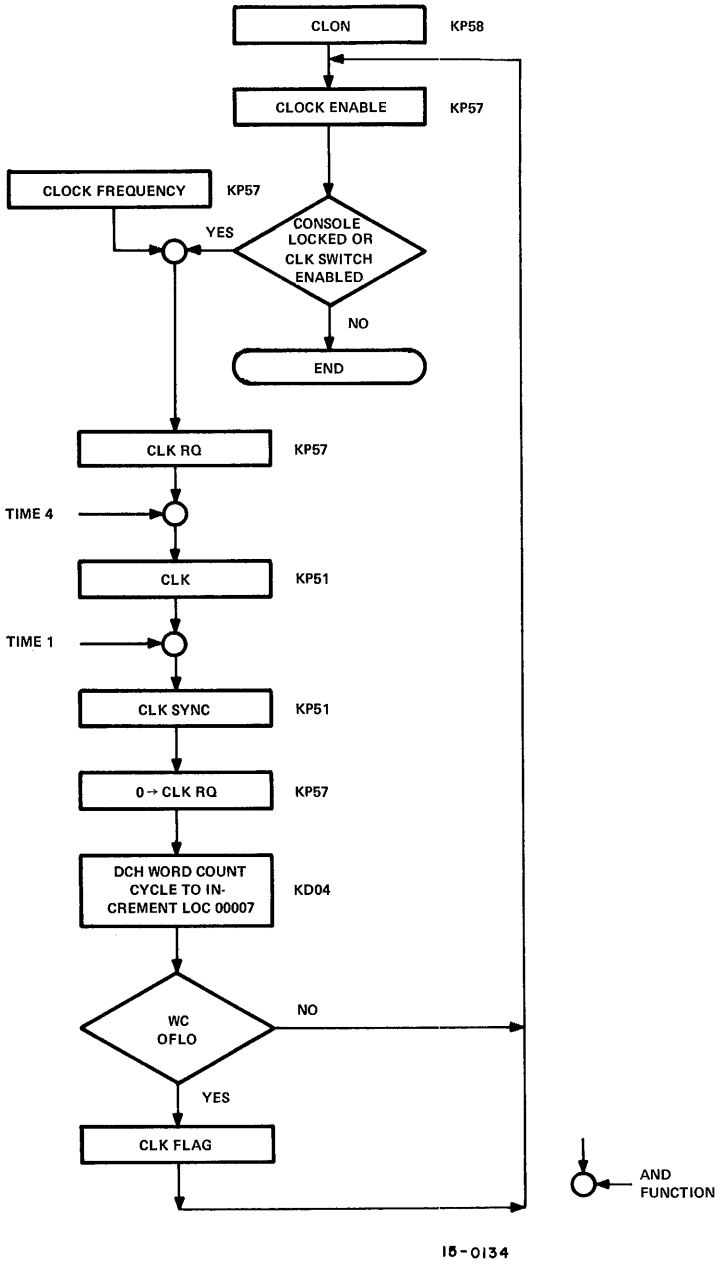


Figure 5-4 Real-Time Clock General Flow Diagram

5.4 KF15 POWER FAIL

The KF15 Power Fail protects the XVM System from loss of power by providing a means of storing important CP registers, and the subsequent restoration of these registers, and restarting of the program when power returns.

The system is always power-cleared when turned on or off. There are three ways in which power failures are handled.

If the console is not locked, the system acts exactly as though the Power Fail does not exist. A power low condition is detected by the power supplies and the CP RUN flip-flop is cleared at the end of the current instruction in progress. INT reset pulses are then generated until the logic cannot function (Figure 5-5). When power is restored, a series of INT reset pulses are produced as soon as there is enough power to supply the logic. This burst continues for 750 μs after the POWER OK line goes positive (Figure 5-6). The single power fail IOT instruction is:

SPFAL 703201 Skip on power fail flag.

The other two modes of operation (Figure 5-7) are with the console locked and the machine with PI or API enabled. When the power failure is detected as above, a power fail program interrupt request or API request is made.

In the case of API, a level zero API request is made, synchronized, and location 52 is executed. A JMS should be in this location and the subroutine should store all CPU registers in memory, place a jump to a restart routine in location zero and then halt.

In the case of PI, a program interrupt break is performed and the power fail flag is detected by the power fail skip (SPFAL). A subroutine should then store the CPU registers, place a jump to a restart routine in location zero and then halt.

When power is restored, (Figure 5-8) the machine executes the instruction which was stored in location zero, which restores the registers, and returns the machine to its previous program sequence.

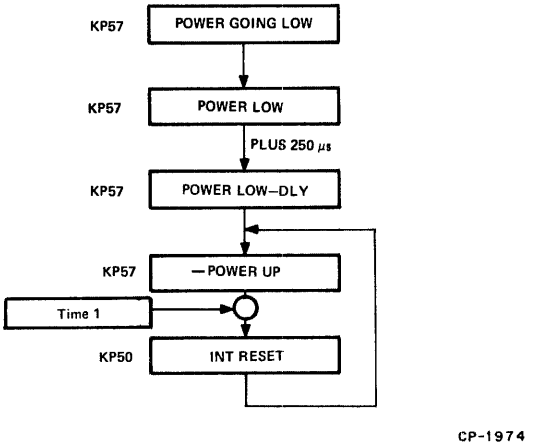


Figure 5-5 Power Fail Sequence – KF15 Disabled

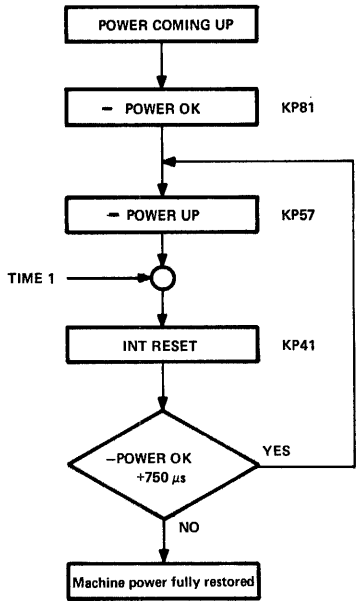


Figure 5-6 Power Restore Sequence – KF15 Disabled

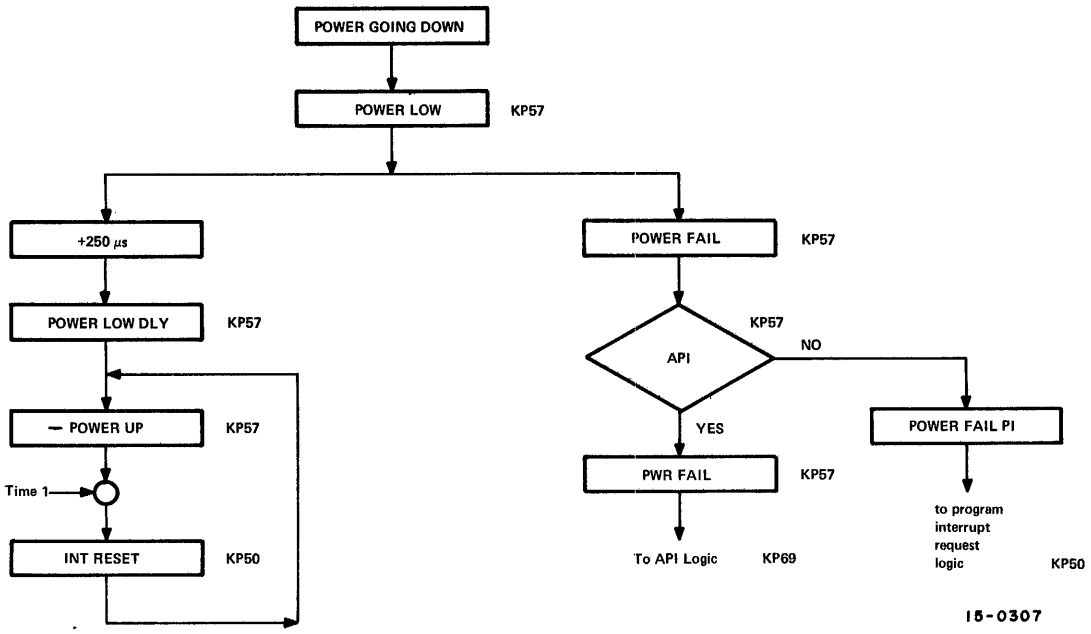


Figure 5-7 Power Fail Sequence - KF15 Disabled

5.5 PC15 HIGH-SPEED PAPER-TAPE READER/PUNCH

The PC15 High-Speed Reader/Punch consists of control logic, located in the BA15 peripheral option expander, and the PC05 Reader/Punch, which contains the reader/punch mechanics and the tape movement circuitry.

5.5.1 High-Speed Reader

The PC05 Reader has the capability of advancing and reading tape one character at a time, up to a maximum of 300 characters per second (refer to the PC05 manual for complete details). The control logic in the BA15 interfaces the PC05 to the XVM I/O Bus and also adds two features required by the XVM, i.e., character packing and hardware read-in.

The PC15 is able to read tapes in two modes: alpha and binary. A hardware read-in feature is also included. Table 5-22 lists the High-Speed Reader IOTs.

5.5.1.1 Alpha Mode - In this mode, the reader reads one 8-bit character from tape and then signals the computer that the operation is completed.

The reader control sets the ALPHA flip-flop, signals the reader to read a character, loads tape channels 7 and 8 into the 12-bit buffer in the control and then raises the reader flag (the remaining six bits are stored in the PC05 reader) (Figure 5-9).

5.5.1.2 Binary Mode - The reader advances and reads the tape and loads an 18-bit buffer with three 6-bit characters. Characters without an eight-hole punch are ignored. When the buffer is full, an 18-bit word can be transferred to the accumulator of the Central Processor.

The first two 6-bit characters are loaded into the 12-bit register in the reader control, the remaining are stored in the PC05 until read by a RRB IOT (Figure 5-10).

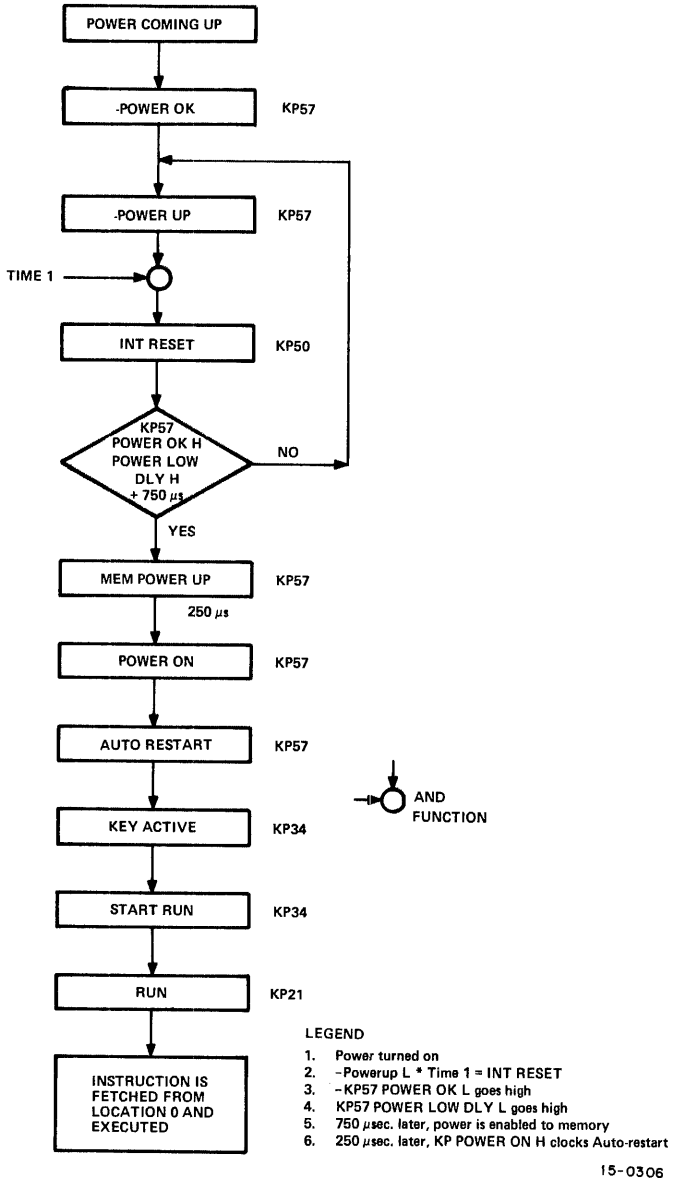


Figure 5-8 Power Restore Sequence - KF15 Disabled

Table 5-22
High-Speed Reader IOTs

Mnemonic	Octal Code	Operation Executed
RSF	700101	Skip if Reader Flag is set.
RCF	700102	Clear Reader flag, then inclusively OR the contents of the reader buffer into the AC.
RRB	700112	Clear Reader flag, and AC, then transfer contents of reader buffer into AC.
RSA	700104	Select Reader in alphanumeric mode.
RSB	700144	Select Reader in binary mode.

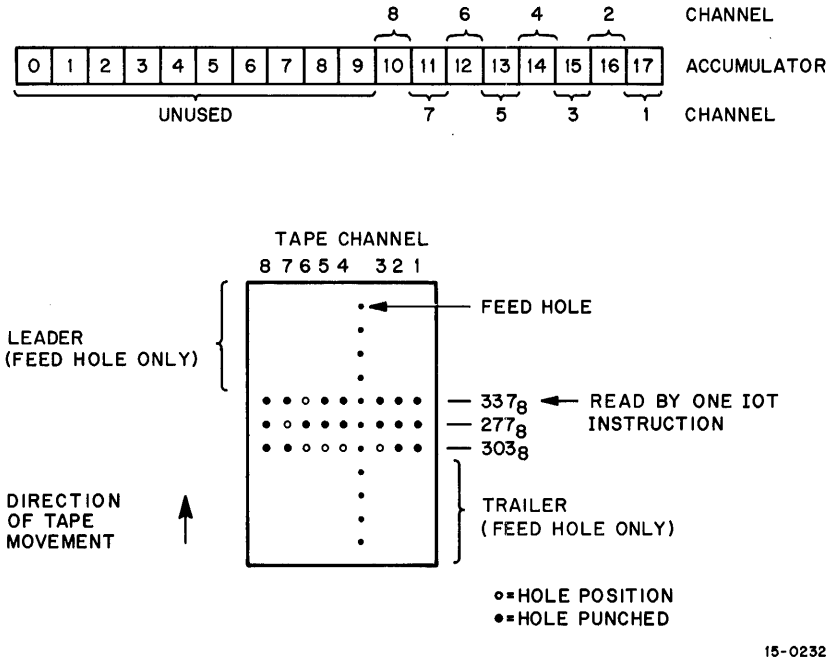


Figure 5-9 Tape Format and Accumulator Bits (ALphanumeric Mode)

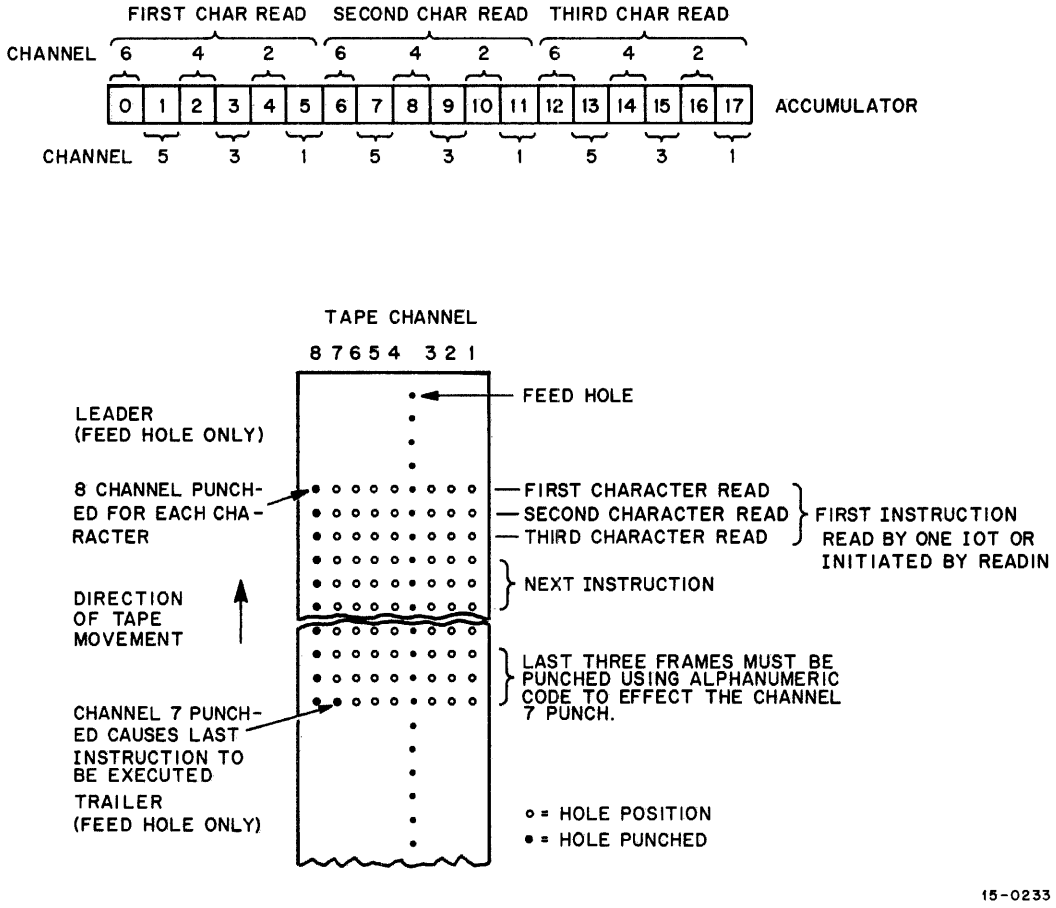
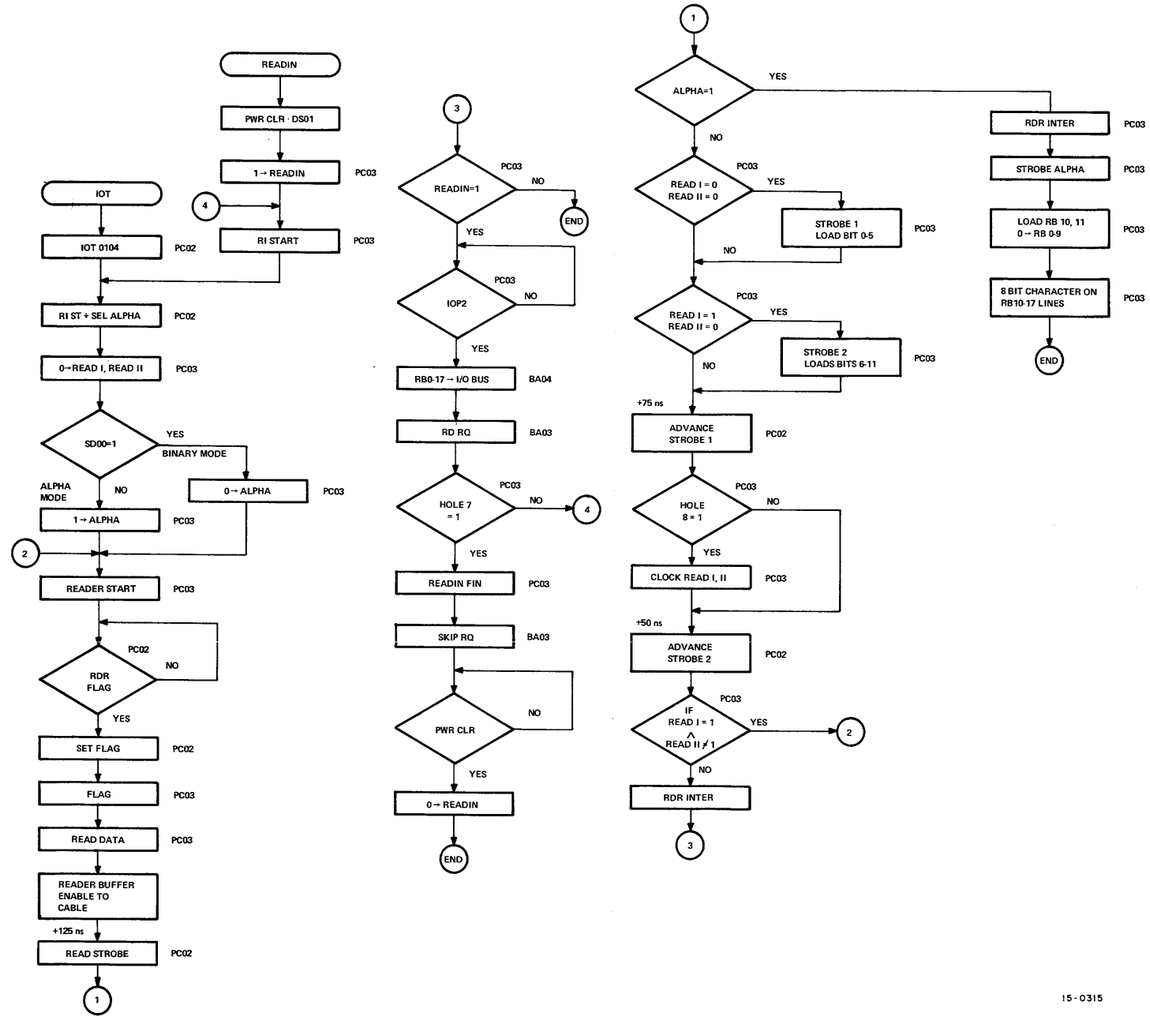


Figure 5-10 HRI Tape Format and Accumulator Bits (Binary Mode)

5.5.1.3 Read-In – When the console READ IN key is depressed and the PC15 is installed, the PC0 READ IN flip-flop KP66 is set (Figure 5-11). Refer to the read-in flow diagram (KP75). In read-in mode, 18-bit characters are assembled, as in binary mode. When the Central Processor is signaled by the character interrupt line that a character is ready, the character is transferred by IOP2 and then another character is read. The storage of the character in memory is described in Paragraph 3.12. When a hole seven punch is detected, the SKIP RQ line is enabled to signal the processor that this is the last word to be transferred and that it should be executed. A I/O PWR CLR pulse then clears out the READ IN mode.

5.5.2 High-Speed Punch

The punch receives data from the I/O Bus and punches it on paper tape. Almost all of the punch logic is located in the PC05. The punch is capable of punching in two modes: binary or alpha. In binary mode, a 6-bit character is punched onto tape, bit 7 is never punched and bit 8 is always punched. In alpha mode, 8-bit characters are punched. Figure 5-12 is a flow diagram of the high-speed punch. IOTs for the high-speed punch are listed in Table 5-23.



15-0315

Figure 5-11 High-Speed Reader Operation Flow Diagram

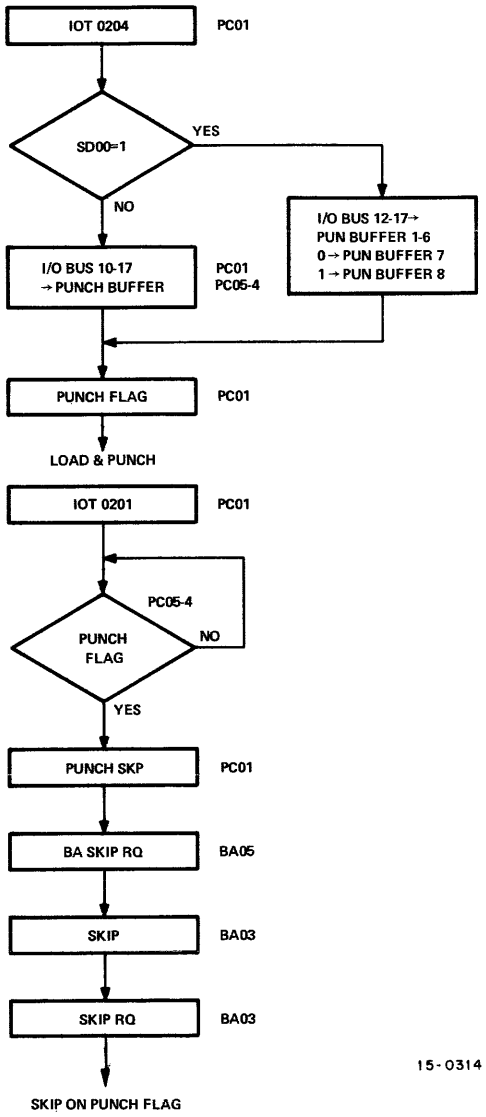


Figure 5-12 High-Speed Punch Operation Flow Diagram

Table 5-23
High-Speed Paper Tape Punch IOTs

Mnemonic	Octal Code	Operation Executed
PSF	700201	Skip if punch flag is set.
PCF	700202	Clear punch flag.
PSA	700204	Punch a line of tape in alphanumeric mode.
PSB	700244	Punch a line of tape in binary mode.

5.6 CONSOLE TERMINAL CONTROL

The interface for the first Teletype in the XVM System is included with the CPU logic (see KP64 and KP65) and is referred to as the Console Terminal Control. This logic provides control for an ASR or KSR Type 33 or 35 Teletype or an LA36 DECwriter and has no API connection. Terminals interfacad to the Console Terminal Control use priority interrupts only. Automatic printing of incoming characters is provided by connecting the input line to the output line (echo) and holding off IOT enables. Table 5-24 lists the Console Terminal Control IOTs. When executing the KSR instruction, and during read-in operations, the READER-RUN flip-flop is set. This inhibits the echo and activates the Teletype paper-tape reader. (Refer to Paragraph 5.7 for additional information, which is also applicable to the Console Terminal Control.)

5.7 LT15-A TELETYPE INTERFACE (OPTIONAL)

If a second Teletype is to be used with the XVM, the LT15-A Teletype Interface option is required. The LT15-A mounts in the BA15 panel.

The Teletype sends and receives 8-bit ASCII codes in the serial format, as shown in Figure 5-13.

The keyboard and the printer are completely separate systems, and use different serial lines for their data. The corresponding sections of the interface are also separate, but share the 880-Hz clock (LT02). Figures 5-14 and 5-15 show the keyboard and printer timing, respectively.

The receiver portion of the interface (KP64, LT02) uses a 9-bit shift register to store the start pulse and serial data bits as they come in. When the input line is raised by the start pulse, the SPIKE DETECTOR flip-flop is cleared. If the signal is still present a half cycle (4.5 ms) later, IN ACTIVE is cleared and shifting of input data begins. The CLOCK SCALE network causes a shift every 9.09 ms until the start pulse reaches the IN LAST UNIT flip-flop. At this point, the keyboard flag is raised, indicating that data is ready to be read into the XVM with an IOT. The IN STOP flip-flops prevent further operation for the full two zero cycles.

Table 5-24
Console Terminal Control IOTs

Mnemonic	Octal Code	Operation Executed
KSF	700301	Skip if keyboard flag set.
KRB	700312	Read keyboard buffer into AC10-17, clear flag.
KRS	700332	Read keyboard buffer, clear flag, select keyboard reader for next character.
TSF	700401	Skip if teleprinter flag set.
TCF	700402	Clear teleprinter flag.
TLS	700406	Load teleprinter buffer from AC10-17, start print operation.

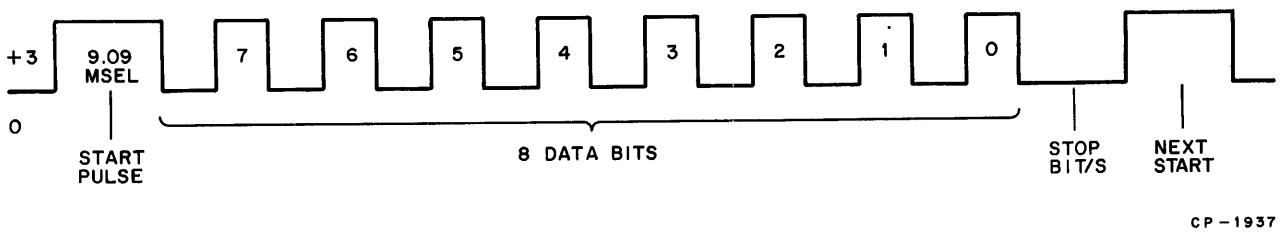


Figure 5-13 Teletype Serial ASCII Format

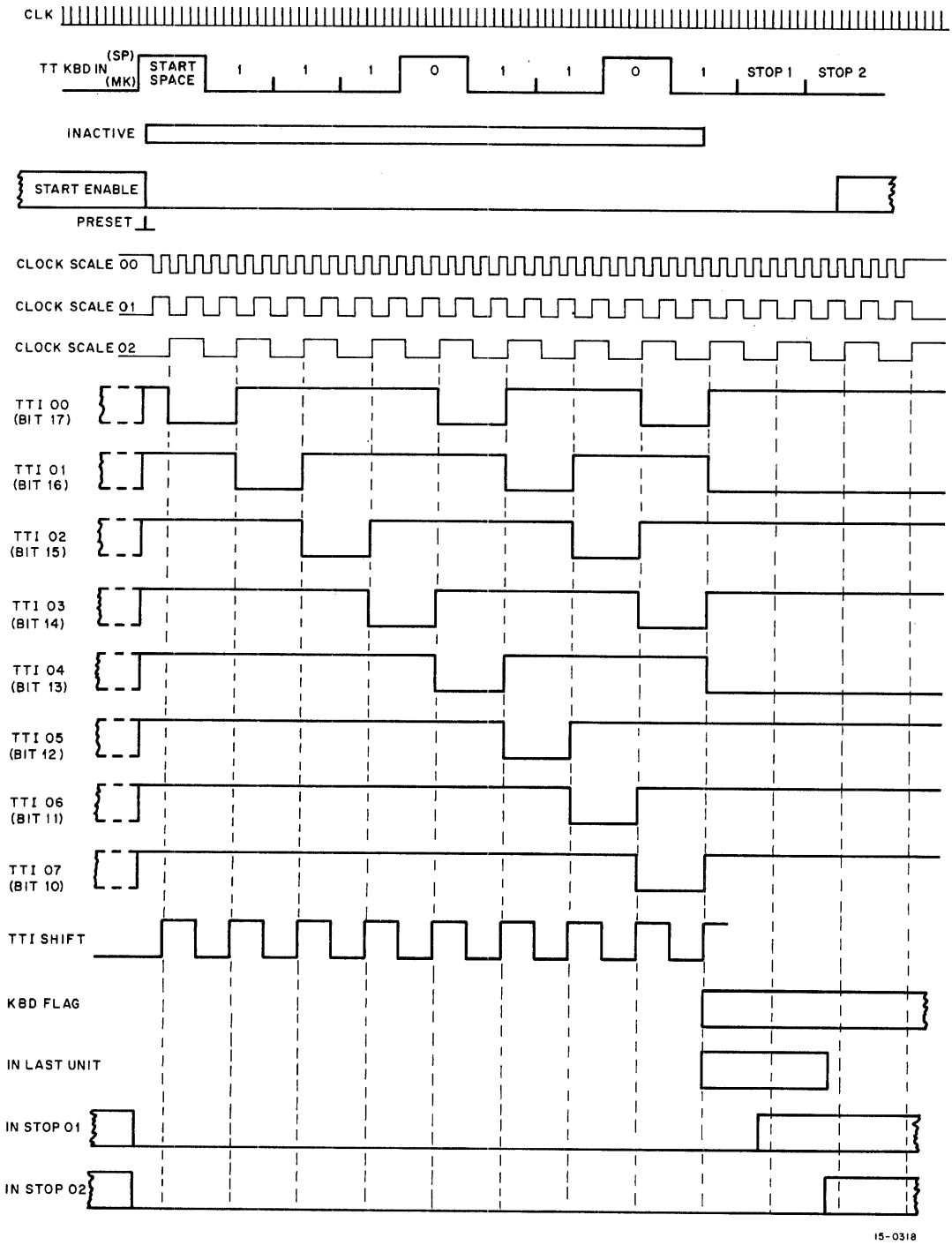


Figure 5-14 Teletype Receiver (Keyboard) Timing

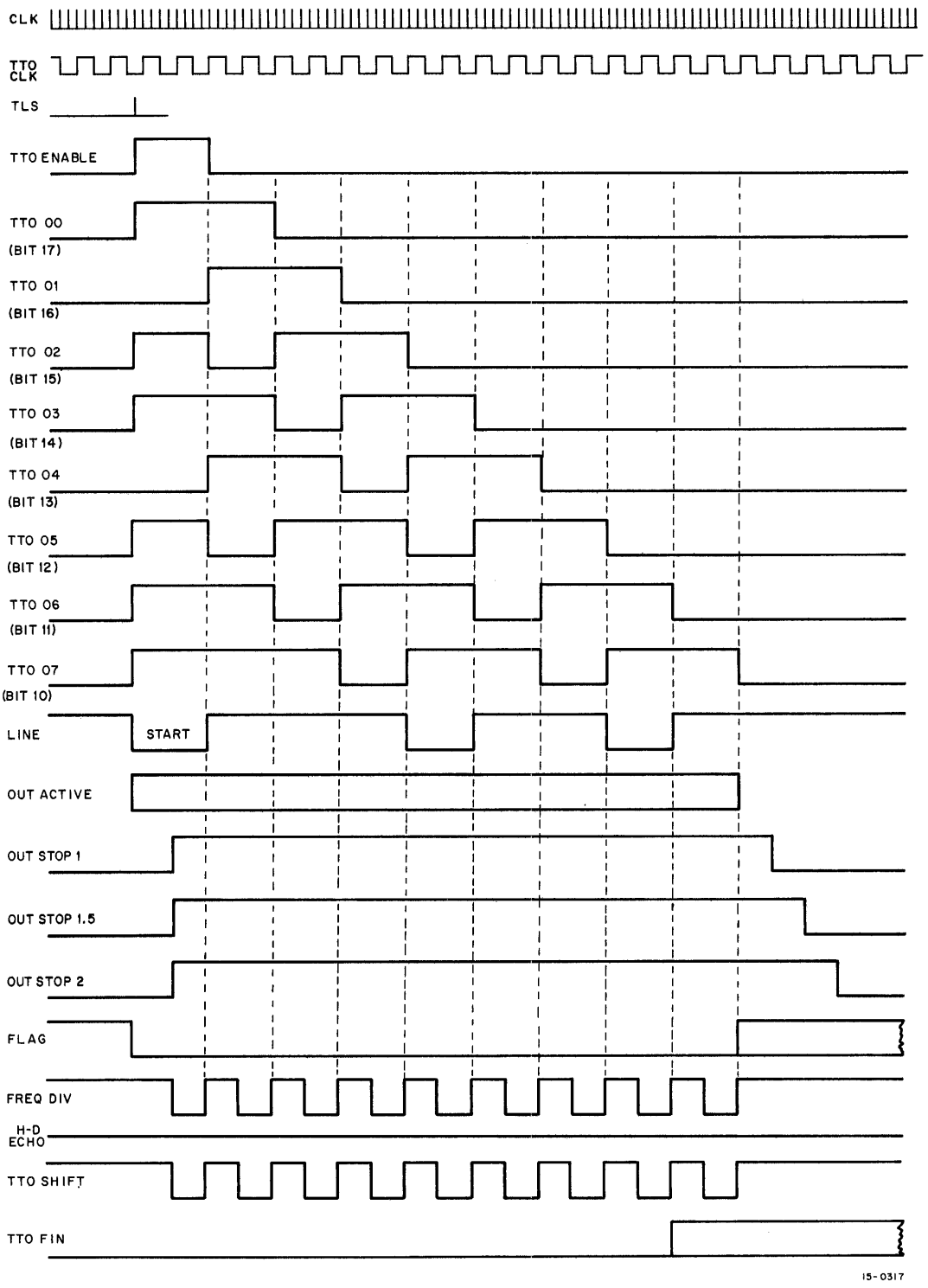


Figure 5-15 Teletype Transmitter (Printer) Timing

The transmitter (KP65, LT03) uses a 9-bit shift register to convert parallel data from the I/O Bus to serial form. The print IOT loads TTO00–TTO07 from bus bits 10–17. TTO ENABLE and OUT ACTIVE are set. LINE is also set, causing the start pulse at the output. The bits are shifted, one-by-one, into the LINE flip-flop until no 1s remain to the left of TTO07. TTO FIN detects this, stops the shifting by dropping OUT ACTIVE, and sets the TELEPRINT FLAG. The OUT STOP flip-flops produce the two cycles of 0 by preventing further enables until they clear.

The LT15-A is connected to the API system when installed.

API for keyboard – Priority level 3, Address 74.
API for teleprinter – Priority level 3, Address 75.

I/O Bus receivers and drivers for the LT15-A are provided in the BA15 option panel. LT15-A IOTs are listed in Table 5-25.

5.8 VP15 DISPLAY CONTROL (OPTIONAL)

The VP15 is a point plotting display control, which interfaces any one of three displays to an XVM:

The VP15-A uses a Tektronix* 611 storage tube (VT01)
The VP15-B uses a Tektronix RM503 oscilloscope
The VP15-C uses a DEC type VR12 X-Y Display.

Points are displayed in a 1024 bit matrix on an 8-1/4in. × 6-3/8in. display surface for the 611 tube, an 8 cm × 10 cm display surface for the RM503 scope, and a 6-3/4in. × 9in. display surface for the VR12 display.

A light pen option is available for both the RM503 and VR12 display systems (VP15 BL and VP15 CL).

The VP15A operates in two modes: Store Mode, where the point plotted is stored on the screen, and Non-Store Mode, where points displayed must be "refreshed" or replotted at least three times a second in order to remain visible. A Display Done flag is raised at the completion of the display command. The VT01 storage oscilloscope may be erased by IOT command and requires about 0.5 seconds for completion. The Display Done flag is raised at the end of this operation.

The Display flag interrupts the computer and a skip on Display flag is provided. The Non-Store Mode is designed for the display of pointers and small groups of characters. Its intensity may be significantly less than in Store Mode. It does not use the write-through feature on the VT01.

Table 5-25
LT15A IOTs

Mnemonic	Octal Code	Operation Executed
TSF1	704001	Skip on transmitter (teleprinter) flag.
TCF1	704002	Clear transmitter flag.
TLS1	704004	Load transmitter buffer and transmit.
KSF1	704101	Skip on receiver flag.
KRB1	704102	Clear receiver flag and read buffer.

*Tektronix is a registered trademark of Tektronix, Inc., Beaverton, Oregon.

The VP15-B and VP15-C are refresh displays and must have the information replotted at least 30 times per second. If a light pen is on the system, a light pen flag is raised whenever light is detected. A timer is provided to limit the occurrence of the light pen flag to about 1 kHz.

The VP15 Display Control includes the display control logic and the digital-to-analog converters.

5.8.1 Display Control

The Display Control provides the timing for point intensification and programmable erasing (VT01) of the display, and a 2-bit brightness register used on the RM503 and VR12 displays.

IOTs initiate the timing sequence for all displays. The VP15-A has two IOTs for this purpose: one for Store Mode and another for Non-Store. The VP15-B and -C have only one IOT for intensification.

In the VP15-A, a Display Done flag is raised when the display has finished plotting the point previously requested. This flag may be cleared and skipped by an IOT control.

The display may be erased manually by depressing a button on the scope or by an IOT command (VT01 storage oscilloscope only).Erase takes 0.5 seconds.

The 2-bit brightness register (BR00 and BR01) is loaded from I/0 Bus bits 16–17 by IOT control. There are four brightness levels for the RM503 and VR12.

5.8.2 Digital-to-Analog Converters (D/A)

The VP15 display contains two digital-to-analog (D/A) converters; one for the x-coordinate buffer, and one for the y-coordinate buffer. Coordinate data is loaded into these converters from the accumulator of the XVM by IOT control.

Upon IOT command, the D/A converters for each coordinate are cleared and loaded with ten bits of information from accumulator bits 08–17. The X Buffer (XB) and Y Buffer (YB) are loaded separately. These 10 bits are converted into a voltage which is used as the input to either the x- or y-deflection circuitry in the oscilloscope.

5.8.3 VP15-A Storage Tube Display IOTs

Non-Store Mode

LXDNS	700544	Load the x-coordinate buffer and display (non-stored); the point specified by XB and YB.
LYDNS	700644	Load the y-coordinate buffer and display (non-stored); the point specified by XB and YB.

Store Mode

LXBD	700564	Load the x-coordinate buffer and display (stored); the point specified by XB and YB.
LYBD	700664	Load the y-coordinate buffer and display (stored); the point specified by XB and YB.
EST	700724	Erase the storage oscilloscope.

Store and Non-Store Mode

CXB	700522	Clear x-coordinate buffer.
CYB	700622	Clear y-coordinate buffer.
LXB	700524	Load x-coordinate buffer from AC08–17.
LYB	700624	Load y-coordinate buffer from AC08–17.
EST	70724	Erase the storage tube.
SDDF	700521	Skip if Display Done flag is set.
CDDF	700722	Clear Display Done flag.
DIE	700721	Display Interrupt Enable/AC bit 16 = 1
		Disable/AC bit 16 = 0

5.8.4 VP15-C Display and VP15-B Oscilloscope IOTs

DXL	700504	Load x-coordinate buffer from AC08–I7.
DSX	70544	Load x-coordinate buffer and display point specified by XB and YB.
DYL	700604	Load y-coordinate buffer from AC08–17.
DYS	700644	Load y-coordinate buffer and display point specified by XB and YB.
DXC	700502	Clear x-coordinate buffer.
DYC	700602	Clear y-coordinate buffer.
DLB	700704	Load brightness register from bits 16–17 of AC.
DSF	700501	Skip if Display (light pen) flag is set.
DCF	700702	Clear Display (light pen) flag.

5.8.5 Principles of Operation

A simplified block diagram of the VP15 controller is given in Figure 5-16. The controller consists of three subsystems:

a. A 10-bit buffer and D/A converter for each x and y deflection circuit.

b. Z axis timing and control circuits.

c. Device decoding, I/O Bus receivers and drivers, and interrupt logic (OR API Logic).

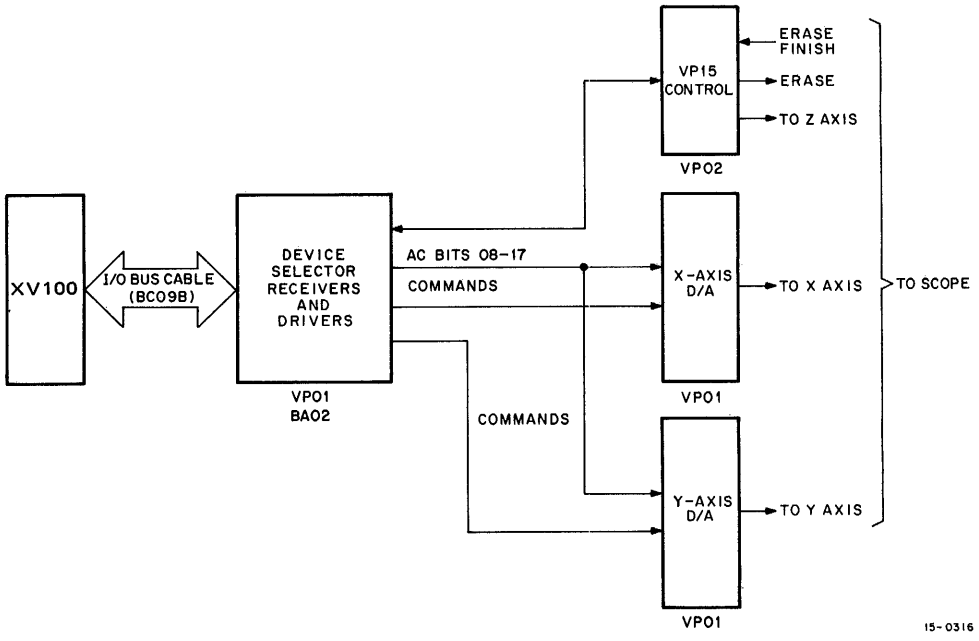


Figure 5-16 VP15 Controller Simplified Block Diagram

The receivers and drivers interface the device to the I/O Bus and to the XVM. The device selectors decode the various IOT commands. The 10-bit x and y coordinate buffers, which define a 1024 × 1024 matrix, are cleared and loaded by IOT commands. After an intensify command has been completed in the VP15-A, a Display Done flag will be set, and the computer interrupt will occur. This condition may be tested by a skip or Display Done flag.

The VT01 scope may be erased by IOT command and the display flag will be set, as above, upon the completion of the erase.

An input/output read status (IORS) instruction will read the status of the display flag into AC bit 05, and light pen flag into AC bit 05; for systems with API, the display is a priority level 2, and its I/O address is 54.

Table 5-26 lists the deflection settling and intensification times for the various VP15 options.

Table 5-26
VP15 Settling and Intensification Times

Option	Mode	Deflection Settling Time (μs)	Intensification Time (μs)
VP15A	Store Mode	80	20
	Non-Store Mode	80	1.5-2.2
VP15B	- - -	15	1.5-2.2
VP15C	- - -	3	1.5-2.2

CHAPTER 6
INSTALLATION

6.1 INTRODUCTION

This chapter contains information for installing an XM15 add-on to an existing PDP-15 System, and installation information for XV100 and XV200 XVM Systems.

Customer assistance is provided during site planning, preparation, and installation. The final layout plan should be approved by both the customer and DEC, prior to delivery of the equipment.

Planning considerations should include:

a. Shipping and access routes, e.g., door, hall passageway, elevator restrictions, etc.

b. Floor plan layout for equipment.

c. Electrical and environmental considerations.

d. Fire and safety precautions.

e. Storage facilities for accessories and supplies.

Site preparation is dictated by the customer's requirements and can range from providing the required source power, to complete construction or remodeling of the selected installation site. Therefore, it is recommended that all requirements and restrictions be considered and effected prior to shipment and installation of the equipment.

6.2 SITE PREPARATION GUIDELINES

Adequate site planning and preparation simplifies the installation process. DEC Sales and Field Service Engineers are available for consultation and planning with customer representatives regarding objectives, course of action, and progress of installation. The information in this paragraph is provided primarily to permit review of the site planning; use the *Site Preparation Handbook, DEC-00-ICSPA-A-D* and the *Site Preparation Guide, DEC-00-HSPPG-A-D* to perform initial site planning. Specific considerations for XVM Systems are given in the *XVM Systems Reference Manual, EK-15XVM-OP-001.*

6.2.1 Physical Dimensions

The overall dimensions and total weight of a particular system – the dimensions, weight of any optional cabinets, cable lengths, and the number of free-standing peripherals – should be known prior to shipment.

The route the equipment is to travel from the customer's receiving area to the installation site should be studied to facilitate delivery of the equipment. Doors, passageways, etc., should be measured and floor plans should be submitted to the DEC Sales Engineer and Field Service to ensure that the equipment is packed to suit the installation site facilities. Any restrictions (such as bends or obstructions in hallways, etc.) should be reported to DEC.

If an elevator is to be used for transferring the XVM and its related equipment to the installation site, DEC should be notified of the size and gross weight limitations of the elevator so that the equipment can be shipped accordingly.

The site space requirements are determined by the specific system configuration to be installed; when applicable, provision is made for future expansion. To determine the exact area required for a specific configuration, a machine room floor plan layout is helpful. When applicable, space should be provided in the machine room for storing tape reels, printer forms, card files, etc. The integration of the work area with the storage area should be considered in relation to the work flow requirements between areas.

In large installations where test equipment is maintained, DEC recommends that the test equipment storage area be within or adjacent to the machine room.

Operational requirements determine the specific location of the various options and free-standing peripherals of the system. Dimensions, weights, and cable lengths of free-standing peripheral equipment must be known prior to installation – preferably during site preparation and planning. The computer peripherals must not be located at distances where connecting cables exceed maximum limits.

The following points should be considered when planning the system layout:

a. Ease of visual observation of input/output devices by operating personnel.

b. Adequate work area for installing tapes, access to console, etc.

c. Space availability for contemplated future expansion.

d. Proximity of the cabinets and peripherals to any humidity-controlling or air-conditioning equipment.

e. Adequate access to equipment (e.g., rear door, etc.) for service personnel.

The final layout will be reviewed by the DEC Sales Engineer, Field Service, and in-house engineering personnel to ensure that cable limitations have not been exceeded and that proper clearances have been maintained.

6.2.2 Fire and Safety Precautions

The following fire and safety precautions are presented to aid the customer in maintaining an installation that affords adequate operational safeguards for personnel and system components.

a. If an overhead sprinkler system is used, a dry pipe system is recommended. Upon detection of a fire, this system removes source power to the room and then opens a master valve to fill the room's overhead sprinklers.

b. If the fire detection system is the type that shuts off the power to the installation, a battery-operated emergency light source should be provided.

c. If an automatic carbon dioxide fire protection system is used, an alarm should sound prior to release of the CO_2 to warn personnel within the installation.

d. If power connections are made beneath the floor of a raised-floor installation, waterproof electrical receptacles and connections should be used.

e. An adequate earth ground connection should be provided to protect operating personnel.

6.2.3 Environmental Requirements

An ideal computer room environment has an air distribution system that provides cool, well-filtered, humidified air. The room air pressure should be kept higher than that of adjacent areas to prevent dust infiltration.

6.2.3.1 Humidity and Temperature – The XVM electronics are designed to operate in a temperature range from 50°F to 110°F (10°C to 40°C) at a relative humidity of 10 to 90 percent, with no condensation. However, system configurations that use input/output devices such as magnetic tape units, card readers, etc., may require closer control of the environment. Nominal operating conditions for a typical system configuration are a temperature of 70°F (20°C) and a relative humidity of 45 percent, with no condensation.

6.2.3.2 Air Conditioning – Computer room air-conditioning equipment should conform to the requirements of the *Standard for the Installation of Air Conditioning and Ventilating Systems (non-residential),* N.F.P.A. No. 90A, as well as the requirements of the *Standard for Electronic Computer Systems,* N.F.P.A. No. 75.

6.2.3.3 Acoustical Damping – Some peripheral devices (such as line printers and magnetic tape transports) are quite noisy. In installations that use a group of high noise level devices, an acoustically damped ceiling will reduce the noise.

6.2.3.4 Lighting – If CRT peripheral devices are part of the system, the illumination surrounding these peripherals should be reduced to enable the operator to conveniently observe the display.

6.2.3.5 Static Electricity – Static electricity can be an annoyance to operating personnel and can (in extreme cases) affect the operational characteristics of the XVM and related peripheral equipments. If carpeting is installed on the computer floor, it should be of a type designed to minimize the effects of static electricity. Flooring consisting of metal panels, or flooring with metal edges, should be adequately grounded, as explained in Paragraph 3.2 of the *Site Preparation and Planning Guide, DEC-00-HSPPG-A-D.*

6.2.4 Electrical Requirements

The XVM operates from a nominal 3-phase, 115 V, 50/60 Hz or 3-phase 230 V, 50/60 Hz, ac power source. The primary ac operational voltages should be maintained within the tolerances defined in Paragraph 1.9.

For certain options that use synchronous motors, line voltage tolerance should be maintained within ±15 percent of the nominal values, and the 50/60 Hz line frequency should not vary more than ±2 Hz.

Primary power to the system should be provided on a line separate from lighting, air conditioning, etc., so that computer operation will not be affected by voltage transients. The wiring should conform to the following general guidelines:

a. All electrical wiring must conform with the National Electric Code (NEC).

b. The ground terminal on the receptacle will normally have a green colored screw; the neutral terminal will be white or silver colored; and the "hot" terminals will be brass colored.

c. Under the NEC (in the U.S. only), the color coding for the neutral wire is either white or gray, and the ground wire is solid green, green with one or more yellow stripes, or bare. There are no specified colors for the "hot" wires.

The XVM cabinet grounding point should be connected to the building power transformer ground, or to the building ground point. Direct any questions regarding power requirements and installation wiring to the local DEC Sales Engineer and/or Field Service.

Chapter 7 contains a detailed description of the AC Power System.

6.3 INSTALLATION AND INSPECTION GUIDELINES

CAUTION

Do not attempt to install the system until DEC has been notified and a DEC Field Service Representative is present.

The procedures in Paragraphs 6.3.1 through 6.3.5 are provided to assist in receipt, unpacking, inspection, and installation of XVM systems.

6.3.1 Unpacking

Before unpacking the equipment, check the shipment against the packing list provided. Check that the correct number of packages has been delivered and that each package contains all the items listed on the accompanying packing slip. Also, check that all items on the accessories list in the Customer Acceptance Procedures have been included in the shipment. Unpack the cabinets as follows:

1. Remove outer shipping container.
2. Remove the polyethylene cover from the cabinets.
3. Remove the tape or plastic shipping pins from the cabinet(s) rear access door(s).
4. Unbolt cabinet(s) from the shipping skid(s).
5. Raise the leveling feet so that they are above the level of the roll-around casters.
6. Use wood blocks and planks to form a ramp from the skid to the floor and carefully roll the cabinet onto the floor.
7. Roll the system to the proper location for installation.
8. If necessary, repeat Steps 1 through 7 for expansion cabinets. When the cabinets are properly oriented, follow the procedure of Paragraph 6.3.3 to install the cabinet(s).

6.3.2 Inspection

After removing the equipment packing material, inspect the equipment, and report any damage to the local DEC Sales Office. Inspect as follows:

1. Inspect external surface of the cabinets and related equipments for surface, bezel, switch, light damage, etc.
2. Open the rear door of the cabinet and inspect the cabinet interior for console, processor and interconnecting cable damage; loose mounting rails, loose or broken modules, blower or fan damage, any loose nuts, bolts, screws, etc.
3. Inspect the wiring side of the logic panels for bent pins, broken wires, loose external components, and foreign material.
4. Inspect the power supply for proper seating of fuses and power connections.

5. Inspect all peripheral equipment, including magnetic tape and DECtape transport heads, motors, paper-tape sprockets, etc., for internal and external damage.

CAUTION

Do not operate any peripheral device that employs motors, tape heads, sprockers, etc., if these items appear to be damaged.

6.3.3 Cabinet Installation

The cabinets are provided with roll-around casters and adjustable leveling feet so it is not necessary to bolt the cabinet to the mounting floor unless conditions indicate otherwise (e.g., shipboard installation). In multiple cabinet installations, receiving restrictions may require that cabinets be shipped individually or in pairs. In such cases, the cabinets are connected at the installation site. Cabinet installation procedures are as follows (refer to Paragraph 6.7 for H950 cabinet installation):

1. With the cabinets positioned in the room, install H952-GA filler strips between cabinet groups (filler strips are shipped attached to end of a cabinet group). Remove four bolts each from the front and rear filler strips. Butt the cabinet groups together while holding the filler strips in place and rebolt through both cabinets and the filler strips. Do not tighten the bolts securely at this time.

2. Lower the leveling feet so that the cabinets are not resting on the roll-around casters but are supported on the leveling feet.

3. Tighten the bolts that secure the cabinet groups together. Ensure that all leveling feet are planted firmly on the floor.

4. Electrical connections, including intercabinet ground strapping, are described in Paragraphs 6.3.4 and 6.3.5.

6.3.4 AC Power Connections

Paragraph 1.9 of Chapter 1 defines the electrical requirements. XM15s and XV100s are equipped with a single 861 Power Control, as shown in Figure 1-1. Most of the additional cabinets in a system include a power control and an ac connector that is similar to that supplied in the basic CPU cabinet. All ac power is distributed from the power control to the appropriate power supplies within the cabinet.

The power controls in all cabinets are connected together to provide central control of power turn-on and turn-off from the CPU console POWER switch. Before connecting any power cables to the site source power, check all building wiring. Ensure that power receptacles of the appropriate types have been provided for each cabinet and that the receptacles are positioned close enough to the cabinet positions to allow the cables to be connected without stretching or crossing the cables. In particular, check that the phase and neutral wires have been connected to the same pins in each receptacle and that the correct voltages can be measured on each phase.

6.3.5 Intercabinet Connections

When a multi-cabinet system is assembled, three types of electrical connections must be made between cabinets (refer to Paragraph 6.3.3 for mechanical connections):

a. Bus connections

   1. MDL cables (from CPU to XM15 Memory Processor).
   2. IBUS cable (Indicator Bus from CPU to XM15).
   3. API cables (from CPU to XM15).

4. IOB cables (from CPU to XM15 and from XM15 to BA15).
5. XM15 BUS cables (from XM15 to external memories, if any).
6. External Processor BUS (from the external processor to XM15 and from the external processor to the next Unibus device, if any).

b. Remote power connections – All cabinet power controls are connected to a control bus that provides for system turn-on and turn-off.

c. Ground strapping – The frame ground of the system is distributed through the cabinets by direct electrical connections between the cabinet frames.

6.3.5.1 Remote Power Connections – The power controls in all cabinets must be interconnected to ensure common power turn-on and turn-off. The cabinet-to-cabinet connections are made with cable assembly DEC-7008288, as discussed in the *861 Power Controller Maintenance Manual, EK-861AB-MM-002.*

6.3.5.2 Ground Strapping – Electrical safety is provided by connecting all cabinet frames to the ground level of the site power system. This is accomplished by connecting a wire in each power cable between the frame and the power system ground; this is not a load-carrying wire – it is intended only as an emergency ground path. The green wire in each power cable is the frame ground; the white wire is the neutral, or return wire, that carries the load current.

To improve the level of safety provided by the frame ground connections, all cabinet frames are connected by braided copper straps or #4 AWG solid wire with crimp-on lugs which are fastened to copper studs that are welded to the frames. (This also prevents the generation of ground loops between cabinets that are connected by signal-carrying cables). The studs are welded to the bottom side rails of the cabinet frame, facing inward; the stud on the left side of the cabinet is slightly forward of center while the stud on the right side is slightly to the rear.

The ground strap supplied with each cabinet is fastened to one stud, passed over the side rail of the cabinet and the side rail of the adjacent cabinet, and fastened to the stud in that cabinet. The copper studs are threaded and nuts are supplied on the studs.

6.3.5.3 Bus Connections – These connections are performed toward the end of the installation procedure. (Refer to Paragraph 6.10.)

6.4 KP15 MODIFICATIONS FOR XM15 ADD-ON

Before installing the XM15 Add-On, it is necessary to modify the KP15.

NOTE

The KP15 must be completely updated to the level of ECO-KP15-0083 before proceeding with the XM15 changes.

The modification to accept the XM15 Add-On (ECO-KP15-00084 or KP15-C00001) was designed to be installed in steps, with intermediate testing following each step. This testing ensures that errors will be detected early so as to minimize total installation time. The ECO includes wiring changes, replacement of MDL terminator modules, replacement of MDL driver modules, replacement of the power sequence module, and the installation of AC and DC LO signal wires. ECO-KP15-00084 has been inserted in the PDP-15 print set for easy access.

6.5 EQUIPMENT REPLACED BY XM15

Certain options and modules which may be present on the existing system cannot be used on an XVM System. ME15 memory, however, can be modified for use with the XM15.

The following equipment is not compatible and should be uncabled. Power connections to these equipments should be removed and be electrically and mechanically secured.

MM15 Memory.
MX15-A Memory Multiplexer(s).
MX15-B Unichannel Multiplexer.
BB15 Option Expander.

6.6 ME15 MEMORY MODIFICATIONS FOR XM15 ADD-ON

If ME15 memory is present on the existing system, the memory must be modified and reconfigured as follows:

1. Remove the M7170 module and its terminator modules and connector block.

2. Remove the G109-YA modules and determine the etch board revision (refer to print D-CS-G109YA-1).

   a. For G109-YA revision C or F, determine if ECO-G109YA-00001 is installed. This can be determined quickly by noting if there are wires on E17, pins 4, 5, or 6.

      (1) If ECO-C109YA-00001 is not installed, no further action is required.

      (2) If the ECO is installed, remove the wire from E27 (3) to E3 (6). Then, install a wire from E27 (3) to E27 (5).

   b. For revision H or later, remove jumper W14 and install jumper W15.

3. Reconfigure all ME15 memory modules according to the slot assignments given in Figure 2-19 of this manual.

4. Install shields, DEC part no. 17-00021-02, between slots 3 and 4, and also between slots 6 and 7, on each backplane.

6.7 INSTALLATION OF H950 XM15 ADD-ON CABINET

When installing the H950 cabinet (Paragraph 6.3.3) containing the XM15, position the cabinet in the Bay 1L (first position to the left of the CPU cabinet). Cable the H950 to the existing system, according to the cabling information presented in drawing A-SP-XM15-0-5.

6.8 INSTALLATION OF 859 POWER CONTROL PANEL FOR XM15 ADD-ON

Install the 859 power control panel in the existing PDP-15 central processor cabinet, according to drawing D-IC-PDP15-0-14. Drawing E-UA-PDP15-0-0 shows the physical position of the 859.

6.9 M7172, M7173, M7174, and M7175 JUMPER AND SWITCH SELECTIONS

XM15 modules M7172, M7173, M7174, and M7175 have jumpers and switches which control functions such as nonexistent memory address selection, external processor address boundary selection, memory interleaving, and Memory Management mode. Refer to Paragraph 2.8.3 for memory configuration information and to the notes accompanying each of the jumper and switch tables (Tables 6-1 through 6-9).

All switch selections for the M7173 and M7174 modules regarding port selection and memory interleaving are set up once the configuration of the XVM System is established. The equivalent switches (port selection or interleaving) for the three possible input devices (XVM, external processor, and IPF) are normally set in a similar manner. That is, once the interleaving format is established for the M7173 XVM interleaving switches, the M7174 external processor address, and IPF address interleaving switches are set to the same switch pattern. Similarly, the M7173 XVM port selection switches, the M7174 external processor, and IPF port selection switches are set to the same pattern.

Table 6-1
M7175 Memory Management Mode Selection

Jumper	In/Out	Mode Selected
W1	In	Protect Mode
W1	Out	Relocate Mode

Table 6-2
M7175 NEXM Selection

Total Memory (Words)	S1 Switch Configuration						First NEXM Address in Octal
	S1	S2	S3	S4	S7	S8	
8K	ON	ON	ON	ON	ON	OFF	020000
16K	ON	ON	ON	ON	OFF	ON	040000
24K	ON	ON	ON	OFF	ON	OFF	060000
32K	ON	ON	ON	OFF	OFF	ON	100000
40K	ON	ON	OFF	ON	ON	OFF	120000
48K	ON	ON	OFF	ON	OFF	ON	140000
56K	ON	ON	OFF	OFF	ON	OFF	160000
64K	ON	ON	OFF	OFF	OFF	ON	200000
72K	ON	OFF	ON	ON	ON	OFF	220000
80K	ON	OFF	ON	ON	OFF	ON	240000
88K	ON	OFF	ON	OFF	ON	OFF	260000
96K	ON	OFF	ON	OFF	OFF	ON	300000
104K	ON	OFF	OFF	ON	ON	OFF	320000
112K	ON	OFF	OFF	ON	OFF	ON	340000
120K	ON	OFF	OFF	OFF	ON	OFF	360000
128K	ON	OFF	OFF	OFF	OFF	ON	400000

Table 6-3
M7173 and M7174 Interleaving

Switch	Non Interleaved	4 Way Memory Must Be Interleaved		
	Memory May Be Interleaved	8K Memories	16K Memories	32K Memories
S1	ON	ON	OFF	ON
S2	OFF	OFF	ON	OFF
S3	ON	OFF	ON	ON
S4	OFF	ON	OFF	OFF
S5	ON	OFF	OFF	OFF
S6	OFF	ON	OFF	OFF
S7	OFF	OFF	ON	OFF
S8	ON	ON	ON	OFF
Jumpers	OUT	OUT	OUT	IN

NOTES

1. Interleaving must be selected on each port module with E43 S1–S8 and W11 and W12. For the external processor and IPF addresses, the selection is made on the IPF module with E8, S1–S8 and jumpers W13 and W14 and E95, S1–S8 and jumpers W11 and W12 respectively.

2. For multiprocessor configurations only, the first level XM15 will have interleaving selected for the external processor input. Higher levels are set for no interleaving.

3. All interleaving switches and jumpers must be set the same for the XVM external processor, and IPF, except as stated in #2 above.

4. Refer to Figures 2-20, 21, 22 and 23 for additional information.

5. The 32K memories column is not used.

Table 6-4
M7173 Port Msync Timing Jumpers

Jumpers	ME15	MF15 or Mix ME15/MF15
W6	IN	OUT
W7	OUT	IN
W8	IN	OUT
W9	OUT	IN

Table 6-5
M7173 and M7174 Port Selection

Switch	2 Way Bus Interleave (2 Ports Only)	8K Block Mode	16K Block Mode	32K Block Mode	64K Block Mode	128K Block Mode
S1	ON	ON	ON	ON	ON	ON
S2	OFF	OFF	OFF	OFF	OFF	OFF
S3	OFF	OFF	OFF	OFF	OFF	ON
S4	OFF	OFF	OFF	OFF	ON	OFF
S5	OFF	OFF	OFF	ON	OFF	OFF
S6	OFF	OFF	ON	OFF	OFF	OFF
S7	OFF	ON	OFF	OFF	OFF	OFF
S8	ON	OFF	OFF	OFF	OFF	OFF

NOTES

1. Port selection for XVM addressing must be set on each Port module with E65, S1–S8. For the external processor and IPF Port selection, the selection is made on the IPF module with E7, S1–S8 and E101, S1–S8 respectively.

2. If the XM15 contains a second port then its switches will be set the same except S1 will be "OFF" and S2 will be "ON".

3. Block mode assumes memory is treated as high and low blocks. The low block must be equal or greater in size than the high block. Port 1 will be the low block and Port 2 will be the high block.

4. All port selection switches must be set the same for XVM, external processor, and IPF, except as stated in #2 above.

5. With bus interleaving, memory accesses alternate between Port 1 and Port 2.

Table 6-6
M7174 IPF Word Selection

	Number of Words		
Jumper	1	2	4
W15	OUT	OUT	IN
W16	OUT	IN	OUT
W17	IN	OUT	OUT

Table 6-7
M7174 External Processor Word Upper Address Window

Word Boundary In Octal	E1 S1	E1 S2	E1 S3	E1 S4	Jumper W9	Jumper W8	Memory Size
007777	ON	ON	ON	ON	OUT	IN	4K
017777	ON	ON	ON	OFF	IN	OUT	8K
027777	ON	ON	ON	OFF	OUT	IN	12K
037777	ON	ON	OFF	ON	IN	OUT	16K
047777	ON	ON	OFF	ON	OUT	IN	20K
057777	ON	ON	OFF	OFF	IN	OUT	24K
067777	ON	ON	OFF	OFF	OUT	IN	28K
077777	ON	OFF	ON	ON	IN	OUT	32K
107777	ON	OFF	ON	ON	OUT	IN	36K
117777	ON	OFF	ON	OFF	IN	OUT	40K
127777	ON	OFF	ON	OFF	OUT	IN	44K
137777	ON	OFF	OFF	ON	IN	OUT	48K
147777	ON	OFF	OFF	ON	OUT	IN	52K
157777	ON	OFF	OFF	OFF	IN	OUT	56K
167777	ON	OFF	OFF	OFF	OUT	IN	60K
177777	OFF	ON	ON	ON	IN	OUT	64K
207777	OFF	ON	ON	ON	OUT	IN	68K
217777	OFF	ON	ON	OFF	IN	OUT	72K
227777	OFF	ON	ON	OFF	OUT	IN	76K
237777	OFF	ON	OFF	ON	IN	OUT	80K
247777	OFF	ON	OFF	ON	OUT	IN	84K
257777	OFF	ON	OFF	OFF	IN	OUT	88K
267777	OFF	ON	OFF	OFF	OUT	IN	92K
277777	OFF	OFF	ON	ON	IN	OUT	96K
307777	OFF	OFF	ON	ON	OUT	IN	100K
317777	OFF	OFF	ON	OFF	IN	OUT	104K
327777	OFF	OFF	ON	OFF	OUT	IN	108K
337777	OFF	OFF	OFF	ON	IN	OUT	112K
347777	OFF	OFF	OFF	ON	OUT	IN	116K
357777	OFF	OFF	OFF	OFF	IN	OUT	120K
367777	OFF	OFF	OFF	OFF	OUT	IN	124K
377777	UNIBUS DEVICE ADDRESSES CANNOT BE USED						

NOTE
Upper Address Boundary = Last Legal Address

Table 6-8
M7174 External Processor Word Lower Address Window

Word Boundary In Octal	Jumper W10	E1 S5	E1 S6	E1 S7	E1 S8	Memory Size
000000	OUT	OFF	OFF	OFF	OFF	0K
010000	OUT	OFF	OFF	OFF	ON	4K
020000	OUT	OFF	OFF	ON	OFF	8K
030000	OUT	OFF	OFF	ON	ON	12K
040000	OUT	OFF	ON	OFF	OFF	16K
050000	OUT	OFF	ON	OFF	ON	20K
060000	OUT	OFF	ON	ON	OFF	24K
070000	OUT	OFF	ON	ON	ON	28K
100000	OUT	ON	OFF	OFF	OFF	32K
110000	OUT	ON	OFF	OFF	ON	36K
120000	OUT	ON	OFF	ON	OFF	40K
130000	OUT	ON	OFF	ON	ON	44K
140000	OUT	ON	ON	OFF	OFF	48K
150000	OUT	ON	ON	OFF	ON	52K
160000	OUT	ON	ON	ON	OFF	56K
170000	OUT	ON	ON	ON	ON	60K
200000	IN	OFF	OFF	OFF	OFF	64K
210000	IN	OFF	OFF	OFF	ON	68K
220000	IN	OFF	OFF	ON	OFF	72K
230000	IN	OFF	OFF	ON	ON	76K
240000	IN	OFF	ON	OFF	OFF	80K
250000	IN	OFF	ON	OFF	ON	84K
260000	IN	OFF	ON	ON	OFF	88K
270000	IN	OFF	ON	ON	ON	92K
300000	IN	ON	OFF	OFF	OFF	96K
310000	IN	ON	OFF	OFF	ON	100K
320000	IN	ON	OFF	ON	OFF	104K
330000	IN	ON	OFF	ON	ON	108K
340000	IN	ON	ON	OFF	OFF	112K
350000	IN	ON	ON	OFF	ON	116K
360000	IN	ON	ON	ON	OFF	120K
370000	IN	ON	ON	ON	ON	124K

NOTE
Lower Boundary = First Legal Address

Table 6-9
M7174 External Processor Address Float

Starting Address	W3 4K	W4 8K	W5 16K	W6 32K	W7 64K
4K	OUT	IN	IN	IN	IN
8K	IN	OUT	IN	IN	IN
12K	OUT	OUT	IN	IN	IN
16K	IN	IN	OUT	IN	IN
20K	OUT	IN	OUT	IN	IN
24K	IN	OUT	OUT	IN	IN
28K	OUT	OUT	OUT	IN	IN
32K	IN	IN	IN	OUT	IN
36K	OUT	IN	IN	OUT	IN
40K	IN	OUT	IN	OUT	IN
44K	OUT	OUT	IN	OUT	IN
48K	IN	IN	OUT	OUT	IN
52K	OUT	IN	OUT	OUT	IN
56K	IN	OUT	OUT	OUT	IN
60K	OUT	OUT	OUT	OUT	IN
64K	IN	IN	IN	IN	OUT
68K	OUT	IN	IN	IN	OUT
72K	IN	OUT	IN	IN	OUT
76K	OUT	OUT	IN	IN	OUT
80K	IN	IN	OUT	IN	OUT
84K	OUT	IN	OUT	IN	OUT
88K	IN	OUT	OUT	IN	OUT
92K	OUT	OUT	OUT	IN	OUT
96K	IN	IN	IN	OUT	OUT
100K	OUT	IN	IN	OUT	OUT
104K	IN	OUT	IN	OUT	OUT
108K	OUT	OUT	IN	OUT	OUT
112K	IN	IN	OUT	OUT	OUT
116K	OUT	IN	OUT	OUT	OUT
120K	IN	OUT	OUT	OUT	OUT
124K	OUT	OUT	OUT	OUT	OUT

NOTE

The lowest #jumper removed must not represent an address value less than the upper boundary minus the low boundary. In other words, if the address bit would normally be driven true for any address within the range of the address window, its jumper must not be removed.

The following procedures may be used to confirm production systems as well as to perform initial switch selections for the XM15 Add-On. *Do not disturb the switch settings when inserting or removing modules.* Appendix E contains an XM15 switch and jumper record where changes can be recorded.

1. On the M7175 module, set the NEXM (Non Existent Memory) switches (S1, Figure 6-1) according to the data provided in Table 6-2.

2. On the M7175 module, select the Memory Management mode (normally the Relocate mode) with jumper W1 (refer to Figure 6-1 and Table 6-1).

3. Switches and jumpers on both the M7173 and M7174 modules determine memory interleaving configurations. Memory interleaving selections require some analysis and planning before attempting to set switches and select jumpers on the M7173 and M7174. The following steps are a guide to implement interleaving (refer to Paragraph 2.8.3 for additional interleaving information).

   a. Determine the total quantity and mixture of memory present in the system.

   b. On paper, assign the memory units (MF15 unit = 16K, ME15 unit = 8K) to XM15 BUS 1 (M7173 Memory Port 1) and XM15 BUS 2 (M7173 Memory Port 2). Two considerations for making these assignments are:

      (1) memory units/backplane – the backplane can be assigned to only one XM15 BUS;

      (2) the type of interleaving – refer to Figures 2-20 through 2-23.

   c. Using the interleaving information determined in step 3b (above) assign device addresses to each memory unit. This completes the configuration on paper.

   d. Begin implementing the interleaving as determined in steps 3a, b, c (above) by selecting the device address and interleaving, if required, on each memory unit according to the MF15 core *Memory Maintenance Manual, EK-MF15-MM-001* and/or the *MF15 Core Memory Maintenance Manual, EK-MF15-MM-002,* and drawing D-CS-G109-0-1.

   e. Refer to Table 6-3 and the associated notes. Select the correct column for the interleaving chosen for the system. Be sure the selection is made on both M7173 modules (Figure 6-2) and the M7174 module (Figure 6-3).

4. Set the M7173 and M7174 port selection switches (Figures 6-2 and 6-3) according to Table 6-5. Note that port selection should be consistent with the interleaving established in Paragraph 6.9 (step 3b and c).

5. On the M7173 module, cut the port timing jumper (W6, W7, W8, or W9 – Figure 6-2) according to Table 6-4.

6. On the M7174 module, select the IPF word depth according to Table 6-6 (refer to Figure 6-3 for jumper locations). Normally, the word depth is set for two.

7. If the system is configured as part of a multi-processor system (Unichannel or multiple XVM), select the external processor upper boundary, lower boundary, and address floating according to the customer's configuration requirements (refer to Tables 6-7, 6-8, and 6-9).

NOTE

If the external processor is not present, disable the inputs by installing a jumper on the XM15 backplane from B13F2 to B13C2.

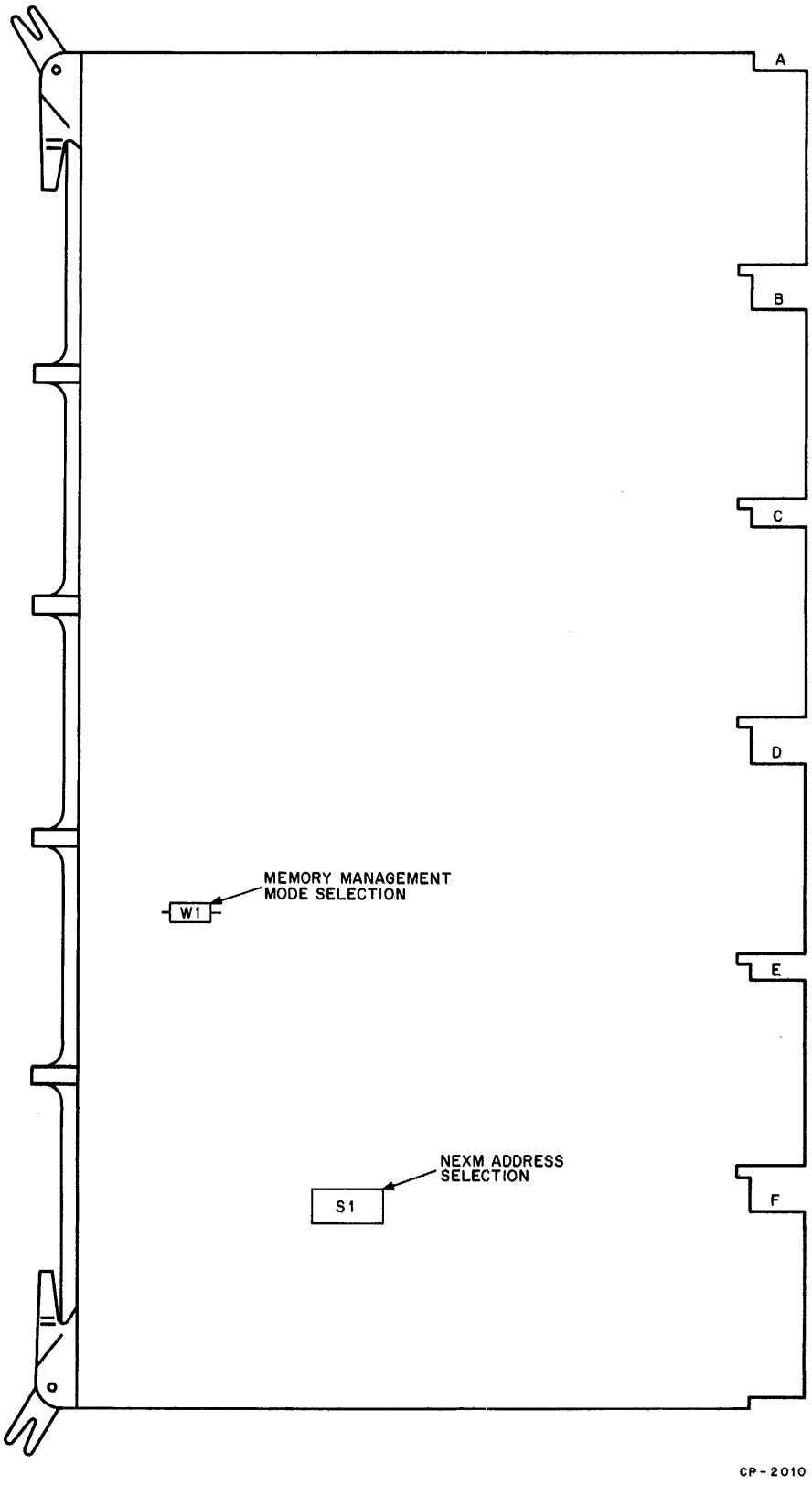


Figure 6-1 M7175 Switch and Jumper Locations

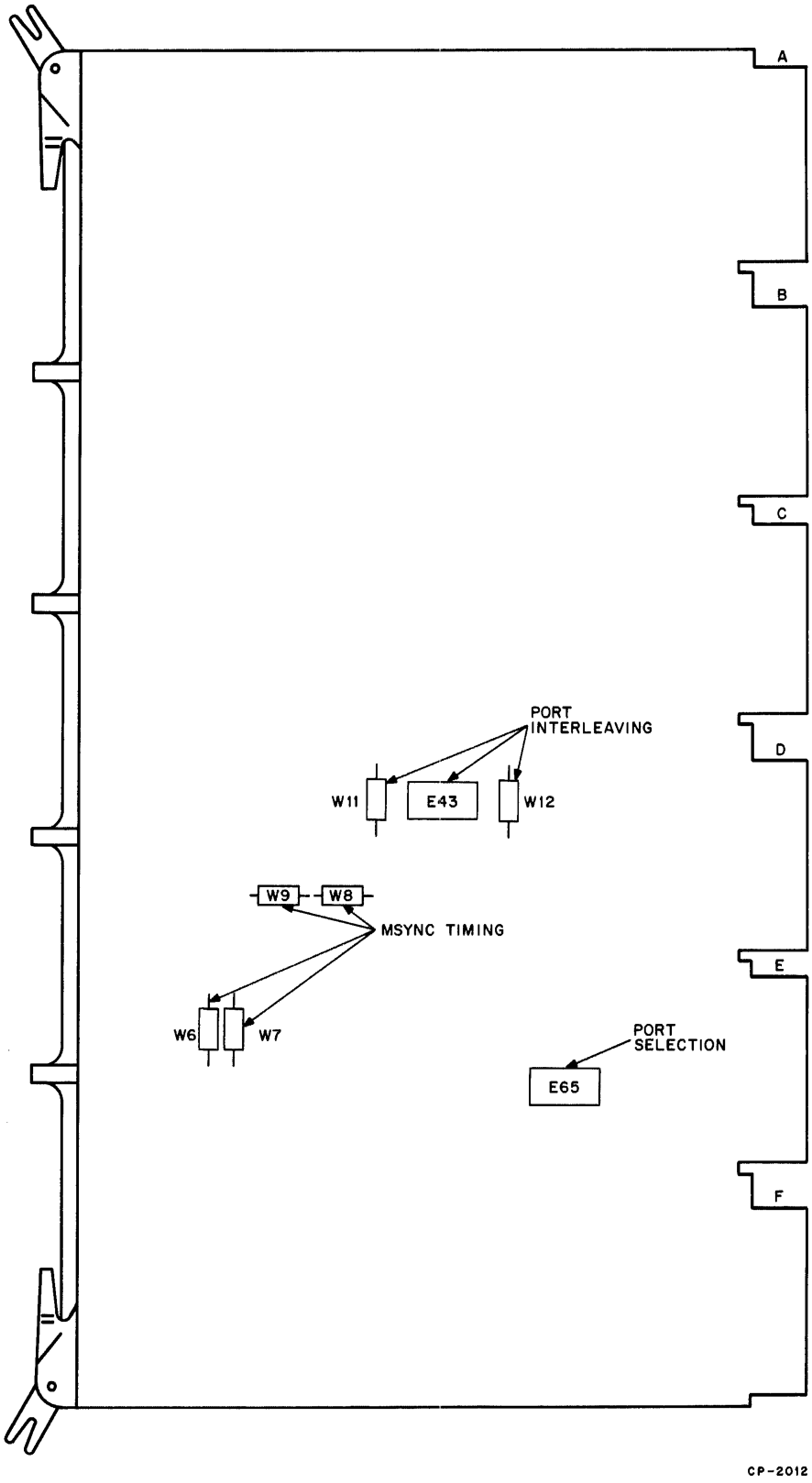


Figure 6-2 M7173 Switch and Jumper Locations

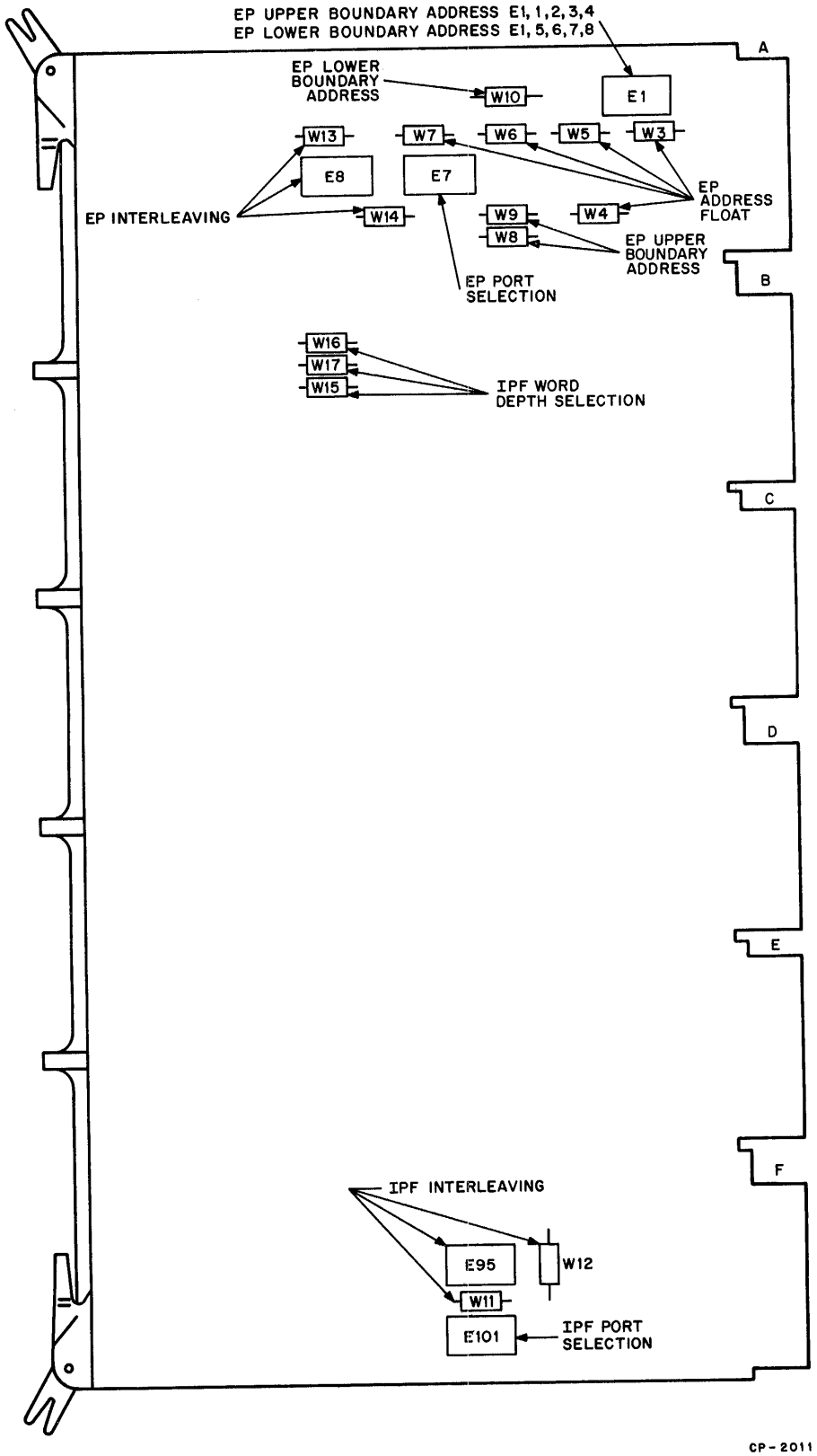


Figure 6-3 M7174 Switch and Jumper Locations

8. On the M7172 module, ensure that the address path switches (Figure 6-4) are all in the OFF position. S1, 1–8 and S2, 7–8 control 15 ADD 00–09. S2, 6 controls 15 MSYNC. S2, 5 may be used to disable the M7174 (IPF) module for maintenance purposes (refer to drawings D-CS-M7172-0-BBC1, BCC2, and BCA).

9. Install the XM15 modules per Figure 2-16.

6.10 XM15 CABLING

After installing the XM15 modules, dress and secure the cables to the XM15 (Figure 6-5) and install the BA11-K top cover. The two BC08-A cables (MDL control and data) which are mounted over each other must be positioned so that the shield is between the two cables. This applies to the shield between the API and IBUS cables as well. The BC09-B IOB cables are intertwined for trouble-free entry into the XM15. Connect the XM15 to the system according to drawing D-AR-XV100-0-2.

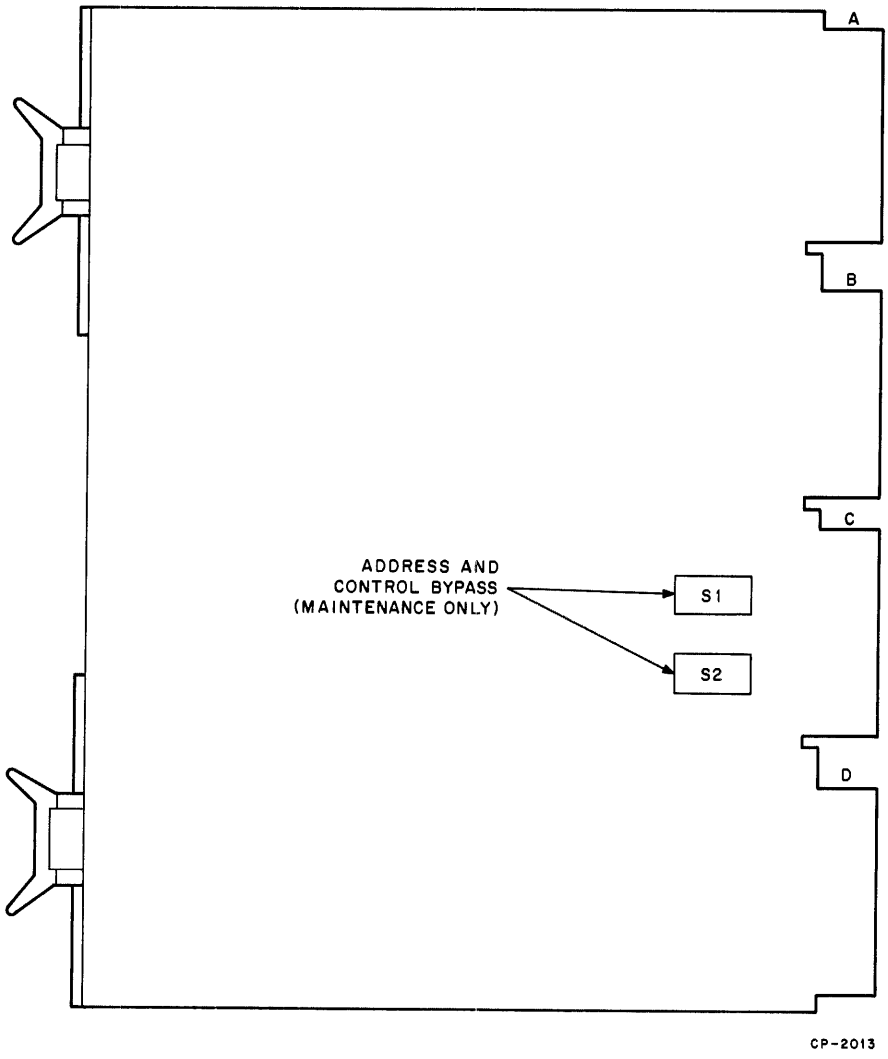


Figure 6-4 M7172 Switch Locations

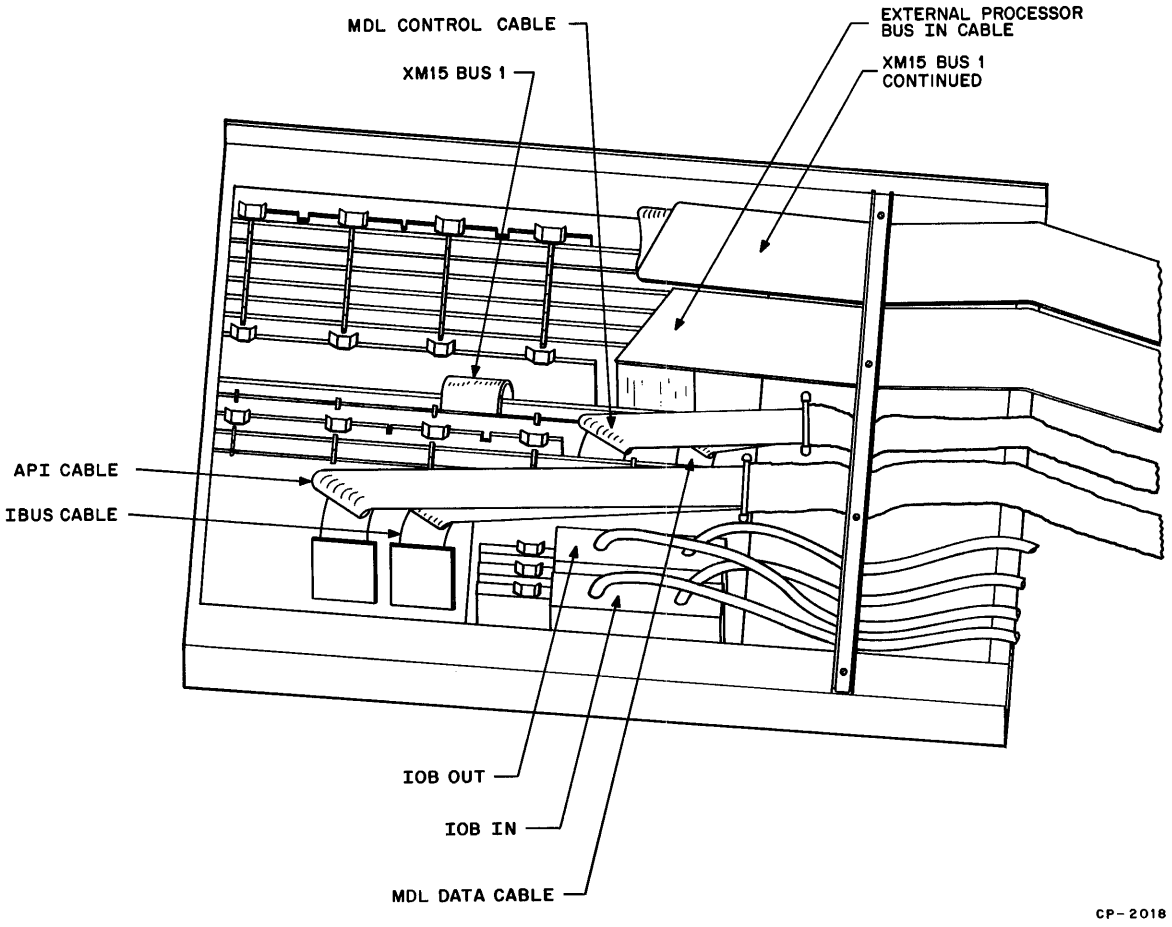


Figure 6-5 XM15 Cable Positions

6.11 INITIAL POWER TURN-ON

When the XM15 cables are installed and the BA11-K cover is secured, place the XM15 in the maintenance (titled) position, power up the system, and perform the following:

1. Perform the XVM System voltage checks and adjustments per Table 7-5 (refer to Paragraph 7.4.4).
2. Perform the console checks described in Paragraph 7.6.1.
3. Power down the system and slide the XM15 into the cabinet.
4. Install all panels and doors.
5. Repeat step 2.
6. Perform customer acceptance per drawing A-SP-XV100-0-4.

6.12 INSTALLATION OF XV100/XV200 SYSTEMS

Before installing an XV100 or an XV200 System, ensure that the site has been properly prepared, according to Paragraph 6.2; perform the installation procedure as follows:

1. Unpack and inspect the XV10 or XV200 System according to Paragraphs 6.3.1 and 6.3.2.

2. Position the cabinets of the XV100 or XV200 System according to the customer's site floor plan and perform the cabinet installation and ac power connection procedures presented in Paragraphs 6.3.3 and 6.3.4, respectively.

NOTE
Do not apply power at this time.

3. Refer to drawing D-AR-XV100-0-2 and perform the intercabinet connections, according to Paragraph 6.3.5.

4. Perform the XV100/XV200 initial power turn-on and checkout procedure (Paragraph 6.13).

6.13 XV100/XV200 INITIAL POWER TURN-ON AND CHECKOUT

1. Apply power to the XV100 or XV200 CPU cabinet and each peripheral cabinet (in turn) and perform the voltage checks listed in Table 7-5. (Refer to the individual peripheral maintenance manuals for prescribed voltage checks on system peripherals.)

2. Perform the console checks described in Paragraph 7.6.1.

3. Perform customer acceptance per drawing A-SP-XV100-0-4.

4. Perform peripheral customer acceptance per individual peripheral specifications supplied with each device.

CHAPTER 7
MAINTENANCE

7.1 INTRODUCTION

This chapter is a three-section chapter which provides maintenance data on the XVM System. Section 1 pertains to the XVM ac and dc power systems. Section 2 contains troubleshooting and timing adjustments; section 3 provides preventive and scheduled maintenance information.

WARNING

It is recommended that maintenance and repairs be performed by qualified service personnel only. Potentially dangerous voltages are present in the XVM System. Safety precautions must be observed when performing maintenance tasks.

Section 1 - Ac and Dc Power Systems

7.2 GENERAL

The XVM ac and dc power systems consist of the 861-D or -E power controller which controls and distributes ac power, and H7420, H765 and H740D dc power supplies which provide dc power.

7.3 AC POWER SYSTEM

The XVM ac power system consists of an 861-D or -E Power Controller which provides a means for controlling and distributing ac power to various units within the XVM System. The 861-D is used with XVM Systems designed for 90–132 Vac, 3-phase; the 861-E is for systems designed for 180–264 Vac, 3-phase. With the exception of the input requirements, the number of circuit breakers, and the type of ac duplex outlets, both 861 controllers operate essentially in the same manner. General theory of operation for a typical 861 controller is presented in Paragraph 7.3.1. Detailed information (including maintenance and troubleshooting) is contained in the *861-Power Controller Maintenance Manual, EK-861AB-MM-002.*

7.3.1 861 Power Controllers

There are two versions of the 861 Power Controller used in the XVM Systems:

861-D: 90–132 Vac, 3-phase, 24A, 47–63 Hz
861-E: 180–264 Vac, 3-phase, 15A, 47–63 Hz

The following paragraphs describe the operation of an 861 Power Controller in general terms. (Refer to circuit schematic D-CS-861-D-1 (861-D) or D-CS-861-E-1 (861-E)).

Power is applied to the power line filter which is an L-C filter with series RF chokes and shunt capacitors to ground. If the rated voltage is present at the indicator terminals, I1, I2 and I3 light.

All ac lines are connected to elements at circuit breaker CB1. All loads connected to the power controller (both switched and unswitched) are controlled by CB1.

If the current through any of the ac lines exceeds the rating of CB1, CB1 trips, removing power from the loads. The 861-D has separate circuit breakers for each outlet. Each outlet line from CB1 is connected to a normally open contact on relay K1. The field coil associated with K1 is energized by the output of CB1 if a relay on the pilot control board is closed.

When K1 is closed, ac power is applied across five of the outlets. The 0.1μF capacitors (C1) connected across the lines at the relay reduce the amplitude of voltage spikes at the output of the controller when switching inductive loads, thereby preventing interference to nearby electronic data processing equipment.

The Pilot Control Board contains the circuitry that allows remote turn-on and emergency turn-off of the switched power outlets in the 861 Power Controllers. These functions are accomplished by controlling the voltage applied to the field coil of relay K1 in the 861 Power Controller.

The Pilot Control Board circuit consists basically of a full-wave rectifier, loaded by the center-tapped field coil of a relay and three control lines connected to the board. Pin 3 connects to the center-tapped secondary of the full-wave rectifier transformer. Pin 2 is the disable (Emergency Shutdown) line from the signal bus, pin 1 is the enable (Power Request) line from the signal bus. Two additional lines (from the thermal switch) are connected to the lines associated with pins 3 and 2.

When the 861 LOCAL/OFF/REMOTE switch (located on the power controller panel) is in the REMOTE position, and pins 3 and 1 are connected, current flows through the lower portion of the Pilot Control Board center-tapped relay field coil to the full-wave rectifier transformer. This action closes the relay on the Pilot Control Board and causes an energizing potential to be applied across the field coil associated with K1 in the power controller, energizing the controlled outlets. When pins 3 and 2 are connected (Emergency Shutdown is true), current flows through the lower and upper halves of the center-tapped field coil in opposite directions before returning to the power supply transformer. The resultant current through the field coil is less than that required for holding the relay closed. Energizing potential therefore is not present at relay K1 and power is removed from controlled outlets.

The diode across the Pilot Control Board relay coil provides a current path in the lower section of the coil to prevent closing the relay in instances where pins 3 and 2 are connected, but pins 1 and 3 are not.

The closing of TS (thermostat) performs the same function as Emergency Shutdown (connects pins 2 and 3 together). This thermostat is exposed to the ambient air surrounding the power controller. Temperatures above 160°F close the thermostat (disabling the switched outlets). The thermostat resets automatically when the temperature drops below 120°F. Placing the 861 LOCAL/OFF/REMOTE switch in the LOCAL position provides a connection between pin 3 and the lower portion of the coil to energize K1, regardless of the state of the Power Request line on the signal bus. This switch position is normally used for maintenance purposes; operations on the Pilot Control Board are exactly the same for situations where a connection is provided between pins 3 and 1 of the signal bus connector due to closing of a circuit in an external device. A connection between pins 2 and 3 disables the switched outlets, regardless of the position of the LOCAL/OFF/REMOTE switch.

The external power supply that provides the potential for closing the Pilot Control Board relay need not be returned to ground. It can be operated in a floating configuration where a connection between pins 3 and 2 (as by the thermostat or Emergency Shutdown) disables the switched outlets and a connection between pins 1 and 3 (Power Request) enables the switched outlets.

7.4 DC POWER SYSTEM

The XVM dc power system consists of an H7420 Power Supply and H744 (+5 V), H745 (-15 V) and H754 (+20 V, -5 V) regulators to supply CPU and memory power; and an H765 Power Supply, and H744, H745, H754 regulators to supply XM15 power. An H740-D Regulated Power Supply is used to supply console +5 V and -6 V (developed from the H740-D -15 V output) and -15 V for the BA15 and KP15 TTY interfaces. General theory of operation for the H742, H765, and the above mentioned regulators is provided in the following paragraphs, along with maintenance and adjustment procedures.

7.4.1 H7420 Power Supply

The H7420 Power Supply is used with the H744, H745, and H754 regulators to supply XVM CPU and memory power. A simplified schematic diagram of the H7420 Power Supply is shown in Figure 7-1. The supply is functionally divided into two major parts:

a. A step-down transformer for providing various ac voltages required by the regulators and power control board.

b. A Power Control Board that provides +8 V (not used in the XVM), +15 V, a line clock voltage used by the KW15, and AC LO and DC LO signals for power fail warning.

Ac Input

The H7420 Power Supply operates with either a 115 Vac or 230 Vac primary power input. Jumpers on terminal strip TB1 adapt the supply to the desired voltage as shown.

Line power is applied through TB1 to the primary of transformer T1. The transformer secondaries provide 20–30 Vac and 15–24 Vac input power for the Power Control Board, and 20–30 Vac for the regulators. Power to the H7420 cooling fan and three regulator fans is taken from the transformer primary. 115 Vac is provided for external (cabinet) fan operation with either 115 or 230 Vac prime power input.

A balun (balanced to unbalanced) assembly is connected between the T1 secondary (terminals 5 and 6) and the 20–30 Vac input to the power control board (J1-1 and J1-2). The purpose of this balanced to unbalanced device is to filter out noise in the power line, thereby preventing inadvertent tripping of the power-fail circuits on the Power Control Board.

+15 V/+8 V Output

The Power Control Board (refer to circuit schematic C-CS-5409730-0-1) of the H7420 Power Supply contains a +15 V/+8 Vdc supply. This dc supply receives 15–24 Vac from the secondary of transformer T1 at J1-3 and J1-4. The ac input is full-wave rectified by diode bridge D1. The resultant dc is filtered and then applied to Darlington power amplifier Q1, through fuse F1. The bias on Q1 is controlled to provide +15 Vdc at output pins 2 and 3 with respect to output pins 4, 5, and 6 (ground). If the Q1 collector voltage starts to increase, the bias at the base of Q2 increases, and Q2 conducts slightly more current to maintain a constant output voltage. Zener diode D7 provides approximately +8 Vdc at output pin 1. (The +8 V output is not used.) When DC LO is grounded at output pin 9, Q2 conducts hard to cut off Q1 completely, thus removing the +15 V and +8 V outputs.

Clock Output

The Clock Output (refer to circuit schematic C-CS5409730-0-1) is derived from one leg of full-wave rectifier bridge D1 by voltage divider R10 and R11, and Zener diode D2. The Clock Output is a 0- to 5-V squarewave at the line frequency of the input power source (47 - 63 Hz). The Clock Output is used in the XVM to drive the KW15.

AC LO and DC LO Circuits

The AC LO and DC LO signals warn the processor when a power failure is imminent, allowing the processor time to perform a power-fail sequence. If there is an ac power failure (line power or power supply failure), AC LO is asserted on the bus, followed by DC LO. Sufficient time exists between these signals to allow storage of volatile data and the conditioning of peripherals.

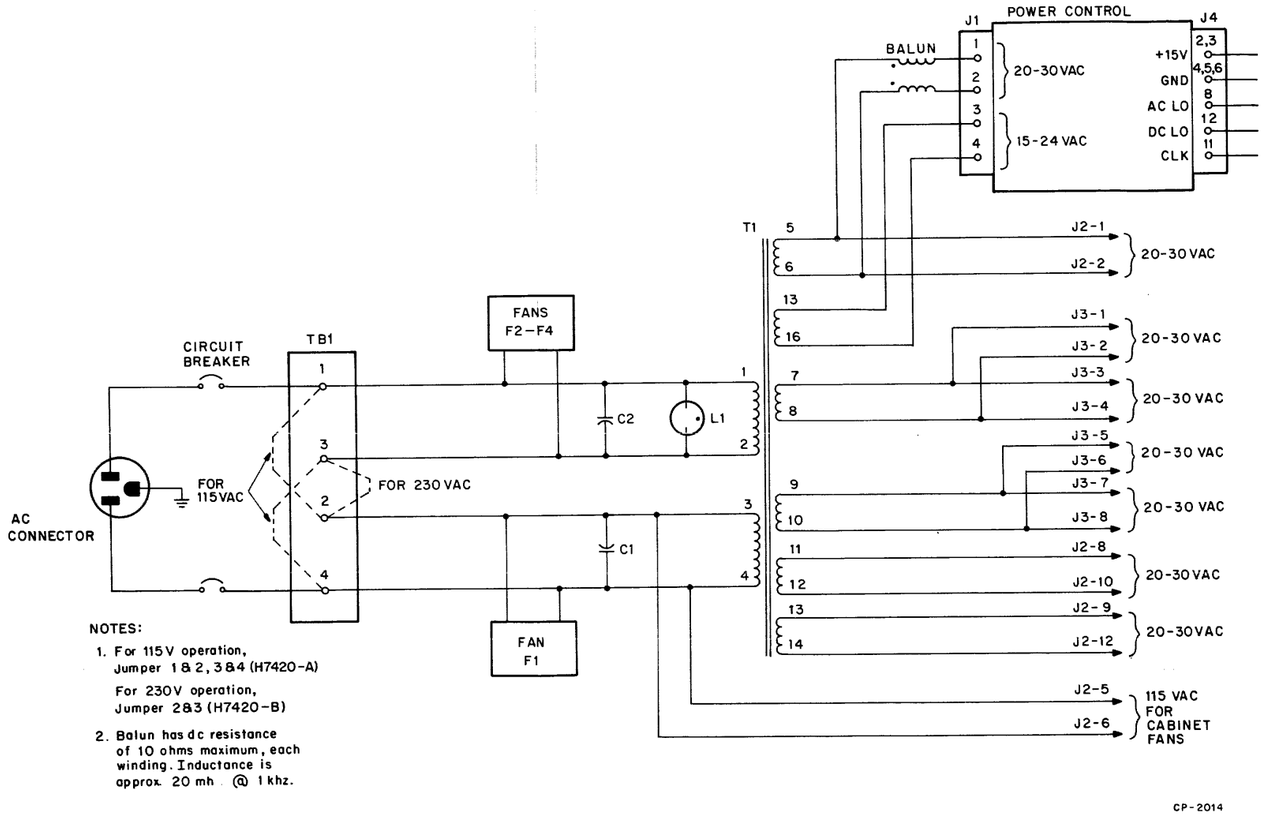


Figure 7-1 H7420 Power Supply, Simplified Schematic

Refer to circuit schematic C-CS-5409730-0-1; the 20–30 Vac input from the secondary of transformer T1 is rectified and filtered by diodes D8 - D11 and capacitor C3. A common reference voltage is derived by resistor R18 and Zener diode D12. Both sensing circuits operate in a similar manner, and each contains a differential amplifier, a transistor switch, and associated circuits. The major difference is that the base of Q6 in the AC LO differential amplifier is at a slightly lower value than that of Q9 in the DC LO differential amplifier. The operation of both sensing circuits depends upon the voltage across capacitor C3.

AC LO Sensing

When AC LO is being sensed, capacitor C3 charges and discharges at a known rate whenever ac power is switched on or off. Thus, the voltage that is applied to the emitters of differential amplifier Q6/Q7 - R17 is a rising or falling waveform of known value. For example, when power fails or is shut down, the dc voltage decays at a known rate as determined by the RC time constant. If the voltage decreases to approximately 20 V, the base of Q6 becomes negative with respect to the base of Q7. The increased forward bias on Q6 causes it to conduct more and the resultant decrease in Q7 causes it to cut off. This removal of voltage across R16 causes Q5 and Q4 to conduct, grounding the AC LO line at pin 8. The AC LO signal is applied through the cable harness and processor backplane to the processor power-fail initialize logic so that the power-fail sequence can be started.

DC LO Sensing

The DC LO sensing circuit operates in a manner similar to the AC LO sensing circuit, the prime difference being the voltage level at which they "trip". For example, if the ac input starts to decrease, as a result of a power failure or shutdown, the AC LO lines are grounded before the DC LO lines. As power is restored, the ground is removed from the DC LO lines before it is removed from the AC LO lines. The DC LO signal is also applied to the power-fail initialize logic. Figure 7-2 shows the H7420 power turn-on and turn-off sequences.

7.4.1.1 H7420 Power Supply Regulators – As mentioned previously, the H7420 Power Supply is a bulk supply which uses separate regulators to develop dc voltages for the XVM System. The regulator types are listed in Table 7-1, along with their specifications, and are described in the following paragraphs.

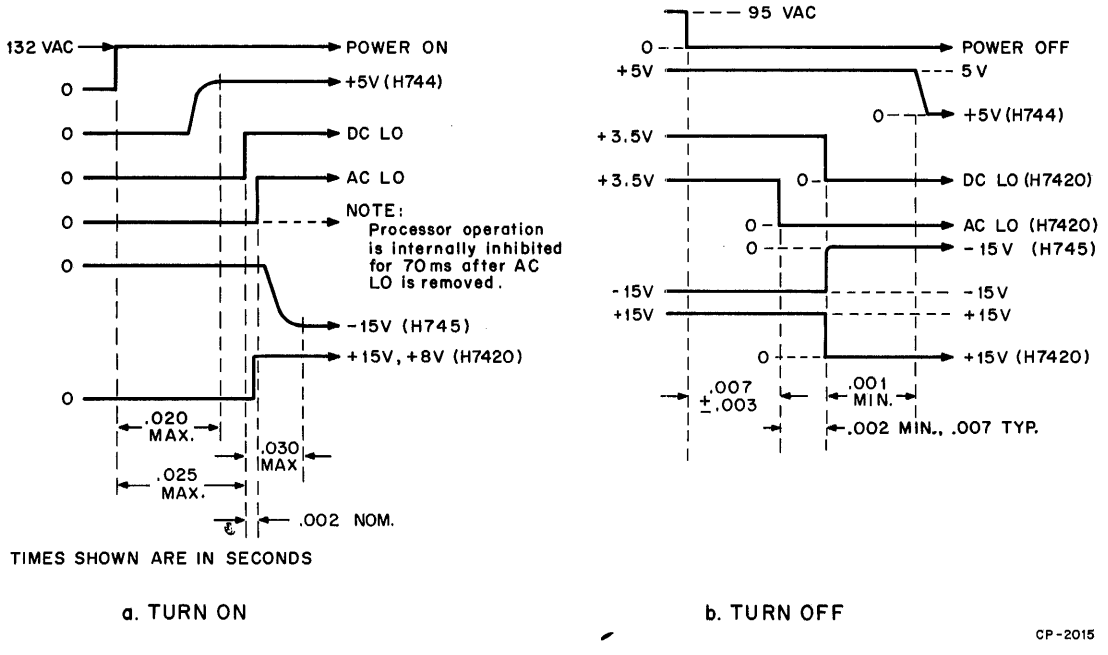


Figure 7-2 H7420 Power Up and Power Down Sequence

Table 7-1
Regulator Specifications

Regulator	Voltage and Tolerance	Output Current (max)	Peak-to-Peak Ripple (max)
H744	±5 Vdc +5% (5.5 V Max)	25 A	200 mV
H745	-15 Vdc ±5% (16 V Max)	10 A	450 mV
H754	+20 Vdc ±5% (21.5 V Max) -5 Vdc ±5% (5.5 V Max)	8 A 1 A – 8 A (Note)	5% 5%

NOTE
Maximum -5 V current is dependent upon +20 V current. It is equal to 1 A + $1_{(+20)}$ up to a total of 8 A. ($1_{(+20)}$ is the amount of +20 V current.)

7.4.1.2 H744 +5 V Regulator

The H744 Regulator circuit is shown in circuit schematic D-CSH744-0-1 and includes a regulator circuit, an overcurrent sensing circuit, and an overvoltage crowbar circuit.

20–30 Vac is applied to the regulator circuit and is full-wave rectified by bridge D1 to provide dc voltage (24 - 40 Vdc, depending on line voltage) across filter capacitor C1 and bleeder resistor R1. Operation centers on voltage regulator E1, which is configured as a positive switching regulator. E1 is a monolithic integrated circuit that is used as a voltage regulator. It consists of a temperature-compensated reference amplifier, an error amplifier, a series pass power transistor, and the output circuit required to drive the external transistors. In addition to E1, the regulator circuit includes pass transistor Q2, predrivers Q3 and Q4, and level shifter Q5. Zener diode D2 is used with Q5 and R2 to provide +15 V for E1. Q5 is used as a level shifter; most of the input voltage is absorbed across the collector-emitter of Q5. This is necessary because the raw input voltage is well above that required for E1 operation. While this +15 V input is supplied, D2, Q5, and R2 retain the ability to switch pass transistor Q2 on or off by drawing current down through the emitter of Q5.

The output circuit is standard for most switching regulators and consists of free-wheeling diode D5, choke coil L1, and output capacitors C8 and C9. These components make up the regulator output filter. Free-wheeling diode D5 is used to clamp the emitter of Q2 to ground when Q2 shuts off, providing a discharge path for L1.

In operation, Q2 is turned on and off, generating a square wave of voltage that is applied across D5 at the input of the LC filter (L1, C8 and C9). Basically, this filter is an averaging device, and the square wave of voltage appears as an average voltage at the output terminal. By varying the period of conduction of Q2, the output (average) voltage may be varied or controlled, supplying regulation (Figure 7-3). The output voltage is sensed and fed back to E1, where it is compared with a fixed reference voltage. El turns pass transistor Q2 on and off, according to whether the output voltage level decreases or increases. Defined upper and lower limits for the output are approximately +5.05 V and +4.95 V.

During one full cycle of operation, the regulator operates as follows: Q2 is turned on and a high voltage (approximately +30 V) is applied across L1. If the output is already at a +5 V level, then a constant +25 V would be present across L1. This constant dc voltage causes a linear ramp of current to build up through L1. At the same time, output capacitors C8 and C9 absorb this changing current, causing the output level (+5 V at this point) to increase. When the output, which is monitored by E1, reaches approximately +5.05 V, E1 shuts off, turning Q2 off; the emitter of Q2 is then clamped to ground. L1 discharges into capacitors C8, C9, and the load. Predrivers Q3 and Q4 are used to increase the effective gain of Q2, ensuring that Q2 can be turned on and off in a relatively short period of time.

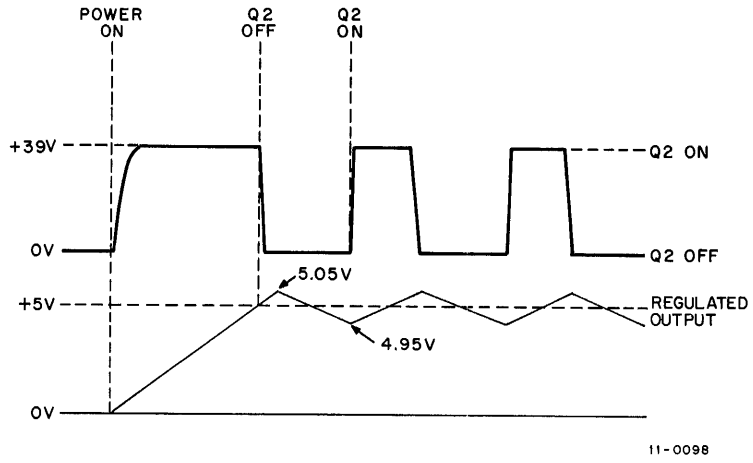


Figure 7-3 H744 Regulator Waveforms

Conversely, once Q2 is turned off and the output voltage begins to decrease, a predetermined value of approximately +4.95 V will be reached, causing E1 to turn on; E1 in turn, causes Q2 to conduct, beginning another cycle of operation.

Thus, a ripple voltage is superimposed on the output and is detected as predetermined maximum (+5.05 V) and minimum (+4.95 V) values by E1. When +5.05 V is reached, E1 turns Q2 off; when +4.95 V is reached, E1 turns Q2 on. This type of circuit action is called a ripple regulator.

The overcurrent sensing circuit consists of Q1, R3 - R6, R25, R26, programmable unijunction Q7, and C4. Transistor Q1 is normally not conducting; however, if the output exceeds 30 A, the forward voltage across R4 is sufficient to turn Q1 on, causing C4 to begin charging. When C4 reaches a value equal to the voltage on the gate of Q7, Q7 turns on and E1 will be biased off, turning the pass transistor off. Thus, the output voltage is decreased as required to ensure that the output current is maintained below 35 A (approximately) and that the regulator is short circuit protected. The regulator continues to oscillate in this new mode until the overload condition is removed. C4 then discharges until E1 is allowed to turn on again and the cycle repeats.

The following components comprise the overvoltage crowbar circuit: Zener diode D3, silicon-controlled rectifier (SCR) D7, D8, R22, R23, C7, and Q6. Under normal output voltage conditions, the trigger input to SCR D7 is at ground because the voltage across Zener diode D3 is less than 5.1 V. If the output voltage becomes dangerously high (above 6.0 V), diode D3 conducts, and the voltage drop across R23 draws gate current and triggers the SCR. The SCR fires and short circuits the +5 V output to ground.

7.4.1.3 H745 -15 V Regulator - Operation of the H745 (circuit schematic D-CS-H745-0-1) is basically the same as that of the H744 regulator. Input power (20 - 30 Vac) is taken from the transformer secondary and input to full-wave bridge D1, whose output is a variable 24 - 40 Vdc input across capacitor C1 and resistor R1.

Regulator operation is almost identical to that of the H744 regulator; however, the +15 V input that is required for E1 operation is derived externally and is input across capacitor C2 to +1, and the inverting and noninverting inputs to E1 are reversed. In addition, the polarities of the various components are reversed. For example, Q5, which is used as a "level shifter," is an NPN transistor on the H744 regulator; a PNP is required on the H745 regulator to allow the regulator to operate below ground (at -15 V).

Under normal operating conditions, regulator operation centers around linear regulator E1 and pass transistor Q2, which is controlled by E1. Predetermined output voltage limits are -14.85 V minimum and -15.15 V maximum. When the output reaches -15.15 V, E1 will shut off, turning Q2 off, and L1 discharges into C8 and C9. When the output reaches -14.85 V, E1 will conduct, causing Q2 to turn on, thereby increasing the output voltage.

The H745 regulator overcurrent sensing circuit is basically made up of the same components used in the H744 regulator, except that Q1 is an NPN transistor in the -15 V regulator. Q1 is normally not conducting; however, once the output exceeds 15 A, Q1 will turn on and C3 will charge. When C3 reaches the same value as the gate of Q7, E1 will be biased off, turning Q2 off, and thereby stopping current flow and turning the H745 regulator off. Thus, the regulator is short circuit protected.

The H745 overvoltage crowbar circuit operates as follows: when SCR D5 is fired, the -15 V output is pulled up to ground and latched to ground until input power or the +15 V input is removed. A negative slope on the +15 V line can be used to trip the crowbar for power-down sequencing, if desired.

7.4.1.4 H754 +20 V, -5 V Regulator – The H754 circuit schematic is shown in D-CS-H754-0-1 and consists of a regulator circuit, an overcurrent sensing circuit, and an overvoltage crowbar circuit.

The regulator circuit has a voltage doubler input, but the output consists of two shunt regulator circuits – one for the +20 V, the other for the -5 V. The +20 V shunt regulator consists of transistors Q4, Q10, and Q11; the -5 V shunt regulator consists of Q6 and Q9. Q10 and Q9 are the pass transistors.

The output of the basic regulator is 25 V (-5 V – +20 V). The shunt regulators are connected across this output, with a tap to ground between pass transistors Q9 and Q10. The voltage at the bases of Q6 and Q4 will vary with respect to ground, depending on the relative amount of current drawn from the +20 V and -5 V outputs of the regulator. If the +20 V current increases while the -5 V current remains constant, the output voltage at the +20 V output will tend to go more negative with respect to ground; this will also cause the -5 V output to go more negative, since the output of the basic regulator is a fixed 25 V. This change is sensed at the bases of Q6 and Q4: Q6 will conduct, causing Q9 to conduct, increasing the current between -5 V and ground until the balance between the +20 V and the -5 V is restored. At this time, neither Q6 nor Q4 will be conducting. If the -5 V current increases, Q4 and Q10 will conduct to balance the outputs.

The overcurrent sensing circuit comprises Q1, Q8, Q13, Q14, and associated circuitry. The total peak current is sampled through R4. When the peak current reaches approximately 14 A, Q1 turns on sufficiently to establish a voltage across R7 and R38, firing Q8. This pulls the voltage on pin 4 of the 723 above the reference voltage on pin 5, shutting off Q2. D6 now conducts, and the current through R37 turns on Q14, which turns on Q13. This keeps Q8 on for a time which is determined by the output voltage and L1. This action, in turn, allows the off-time to increase as the overload current increases, thereby changing the duty cycle in proportion to the load. The output current is thus limited to approximately 10 A.

There are two crowbar circuits in the H754: Q7 and its associated circuitry for the +20 V, and Q12 and its circuitry for the -50 V. Either one will trigger SCR D9.

7.4.1.5 H7420 Regulators – Fuse Replacement – When an XVM dc power system fault has been isolated to a voltage regulator (H744, H745, or H754), examine the fuse (F1) internal to the regulator. Remove the regulator from the H7420 power supply and measure the fuse continuity with a VOM. Figure 7-4 shows the locations of the H7420 regulators. Fuse ratings and DEC part numbers are listed below.

Regulator	Fuse Amperage	Part No
H744	15 A	9007226
H745	15 A	9007226
H754	10 A	9008838

7.4.1.6 H7420 Regulators – Troubleshooting – In the event that the internal regulator fuse requires replacement, or there is no output from a regulator, perform the checks in Table 7-2. Regulator adjustments are presented in Paragraph 7.4.4.

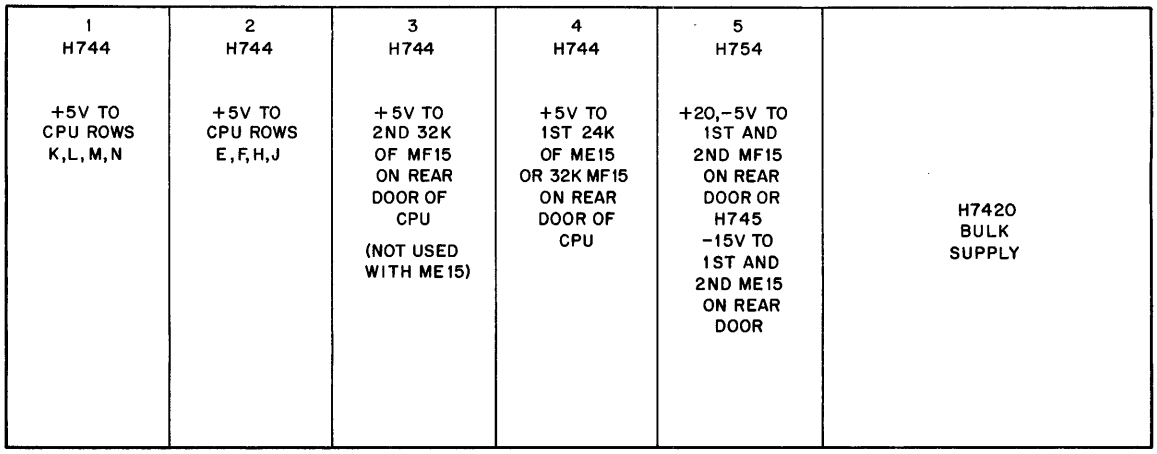


Figure 7-4 H7420 Regulator Slot Assignments

Table 7-2
H744, H745, H754 Voltage Regulator Troubleshooting Chart

Fault Indication	Most Probable Cause	Corrective Action
No output voltage	1. D1 (bottom of D1 will appear burnt).	Replace regulator or D1.
	2. E1 (DEC 723, IC voltage regulator).	Replace regulator or E1.
	3. Misadjusted output voltage.	Shut power off and turn voltage adjust fully ccw (below crowbar voltage). Turn power on and slowly increase voltage, per Table 7-5, until correct value is obtained.
Blown Fuse	1. Q2 (pass transistor).	Replace voltage regulator or pass transistor and associated components.
	2. Excessive loading of voltage regulator.	Replace fuse (Paragraph 7.4.1.5) and check loads.

7.4.2 H765 Power Supply

The H765 Power Supply is used with H744, H745, and H754 regulators to supply XVM, XM15 Memory Processor, and expansion memory (mounted in BA11-K mounting boxes) power. Paragraphs 7.4.1.2 and 7.4.1.3 provide maintenance data on the H744, H745, and H754 regulators. The paragraphs which follow provide maintenance data on the H765 Power Supply. Detailed information on the H765 Power Supply (including maintenance and troubleshooting) is contained in the *BA11-K Mounting Box Manual, EK-BA11K-MM-002.*

7.4.2.1 Mechanical Description – The H765 Power Supply consists of two H744 regulators (+5 V), an H745 regulator (-15 V), an H754 regulator (+20 V, -5 V), a 5411086 regulator (+15 V), a 7010014 transformer assembly, a 7009811-1, -2 ac input box, a 5410864 power distribution board, and two 1211714 fans. The contents of the H765 power system are primarily housed in a welded steel chassis.

The chassis is rectangular and measures approximately 7-3/4 in. long by 10-1/2 in. high by 17 in. wide. The H765 power system top cover is held in place by seven screws. The main structural member contains cutouts and drill holes which enable screws to be inserted for securing the regulators, ac distribution box, transformer assembly, and fans. Cutouts for the regulators allow the regulator ON indicators to be monitored and the regulator output voltages to be adjusted.

The H744, H745, and H754 regulators are secured to the H765 power supply chassis with three Phillips head screws. The mounting screws pass through the H765 chassis holes and screw into the regulator. A plastic (Lexon) shield is installed on the component side of each regulator. This permits visual inspection of the regulator components once the regulator is removed from the H765 chassis. The fuse, which is located on the component side, is accessed by removing the plastic shield. Each regulator contains one potentiometer, except the H754, which contains two potentiometers. An output indicator lamp is located next to the potentiometer. The output of the regulators is terminated in a Mate-N-Lok connector.

The 5411086 regulator is contained on a printed circuit board mounted within the ac input box. It is secured in place when the ac input box is installed in the H765 Power Supply. The inputs and outputs of the regulator are terminated in two Mate-N-Lok connectors.

The 7010014 transformer assembly is located in the center of the H765 chassis. Two capacitors, two varistors, and two terminal strips are mounted directly on the transformer. The transformer baseplate is used to bolt the transformer to the chassis. The area around the transformer is open, enabling ample air flow from the two fans across the transformer frame, providing over-temperature monitoring. Output leads from the transformer, which go to other modules, are terminated in Mate-N-Lok connectors. A cable clamp is used to secure these leads to the chassis.

The 7009811-1-2 ac input box is mounted in the center of the power supply chassis with three Phillips head screws. This enables easy access to the ac line cord, circuit breaker, and remote power control Mate-N-Lok. The 5410993 power control is physically mounted in the ac control box.

The 5410864 power distribution board is a multilayer, printed circuit board containing 12 Mate-N-Lok connectors, connected directly to the board, and four Mate-N-Loks connected to flying leads. The power distribution board is grounded using a ground tab which is connected to a flying lead. The power distribution board is mounted on the rear of the BA11-K chassis; four screws are used to fasten it in place.

Two 1211714 six-inch ball bearing fans, mounted in the chassis between the module boards and regulators, are utilized in the H765 Power Supply. Each fan is secured to the chassis with two screws. The screws of each fan are tightened to 10 in./lb maximum.

7.4.2.2 Functional Description

A functional block diagram of the power system is shown in Figure 7-5. Assume that the line cord is plugged in and the circuit breaker is on; line voltage is applied to the ac input box. The ac input box contains a circuit breaker, relay, power control circuit, and regulator. The regulator, which is physically mounted in the ac input box, is functionally a separate assembly with its own part number. The circuit breaker can be used as an on/off switch (only if pins 1 and 3 are shorted on the 3-pin connector) as well as an overcurrent protection device. The relay and power control circuit allows remote control of ac power to the transformer assembly by means of a key switch or thermal switch. The 7010014 transformer assembly steps down the voltage from the ac input box to approximately 28 Vdc and routes it to H744, H745, H754, and 5411086 regulators. In addition, the transformer assembly routes 115 Vdc to box fans 1 and 2. The regulated dc outputs of the regulators are applied to the power distribution board, where they are distributed to the various backplane connections.

7.4.2.3 Circuit Description – The paragraphs which follow describe the ac input box, the transformer assembly, the 5411086 regulator, and the power distribution board. Refer to unit assembly drawing E-UA-H765-0-0 for the interconnection of the above mentioned components.

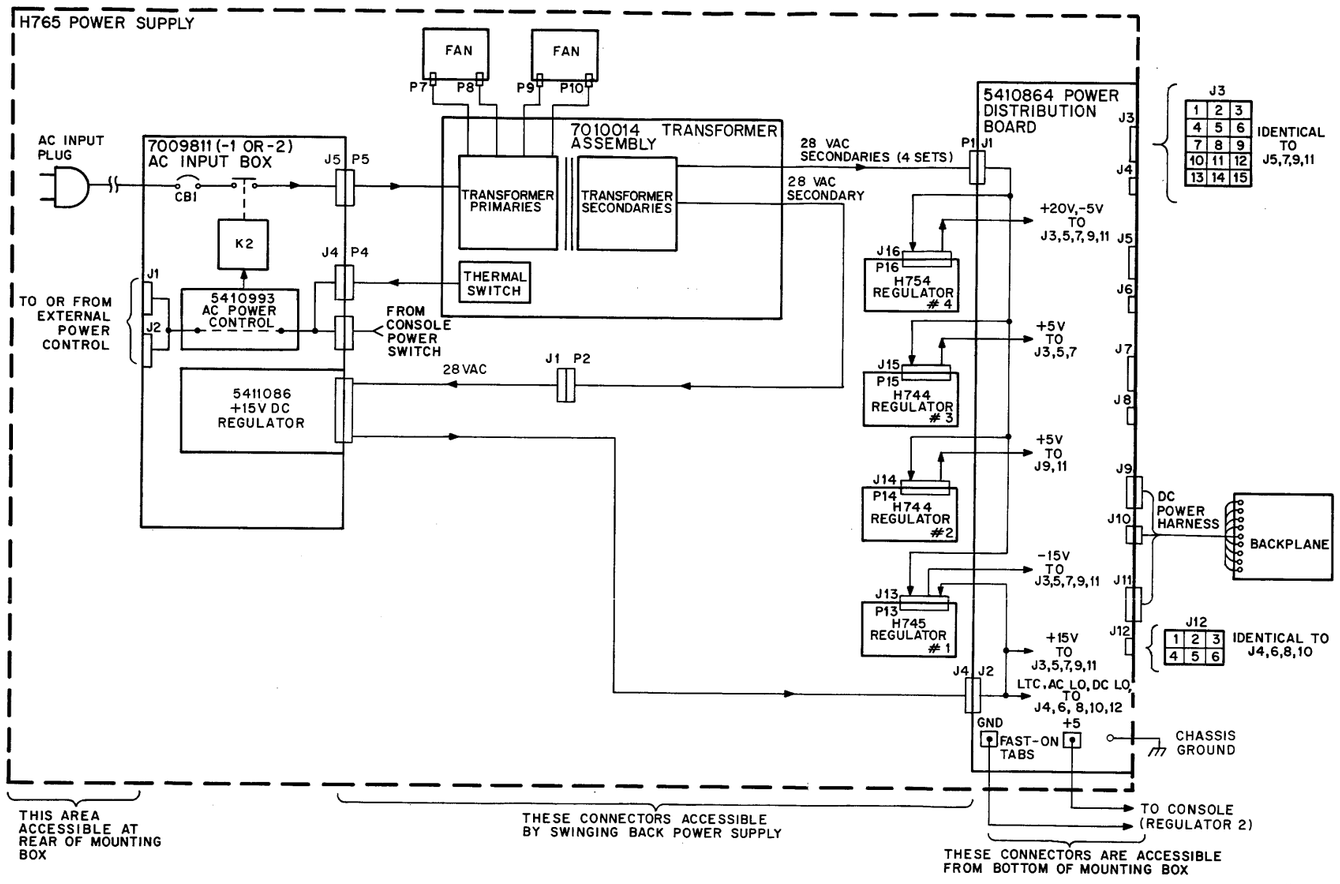


Figure 7-5 H765 Power Supply
Functional Block Diagram

AC Input Box

The 115 V (7009811-1) and 230 V (7009811-2) ac input boxes are functionally identical. They differ physically in their components and in the way they are connected to the transformer assembly. Figure 7-6 is a simplified schematic of the 115 Vac power configuration. In this configuration, the power transformer windings are connected in parallel.

In the 230 Vac power configuration (Figure 7-7), the power transformer windings are connected in series.

Utilizing the 115 Vac input box (7009811-1), the input line voltage is applied via a 20 A circuit breaker (E-UA-H765-0-0) to relay K2, and transfer T1 on the power control board. Transformer T1 steps down the voltage to 24 Vac. The 24 Vac is rectified and applied to relay K1. To energize K1 (Figure 7-8), the optional remote power switch contacts must be closed. Energizing K1 completes the path to K2, switching the 115 Vac to the transformer assembly. The normally open thermal switch (TS1), located in the transformer assembly, closes when an over-temperature condition is sensed. Closing TS1 applies 24 Vdc to half of the K1 relay coil. This creates two opposing fields, causing K2 to deenergize. Deenergizing K1 interrupts the ac power to the transformer assembly. The varistor (D6 or D7) across the coil (E-UA-H765-0-0) of K2 suppresses voltage spikes in excess of 150 Vac for ac input box 7009811-1, and 275 Vac for ac input box 7009811-1.

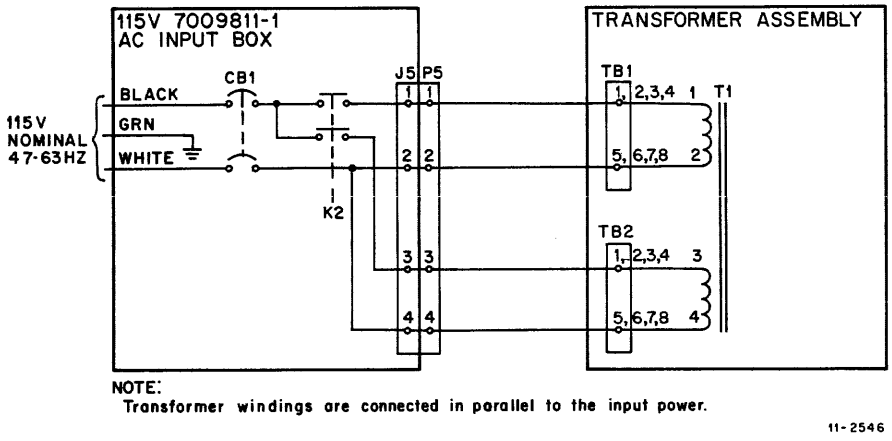


Figure 7-6 H765 Power Supply 115 V Power Configuration

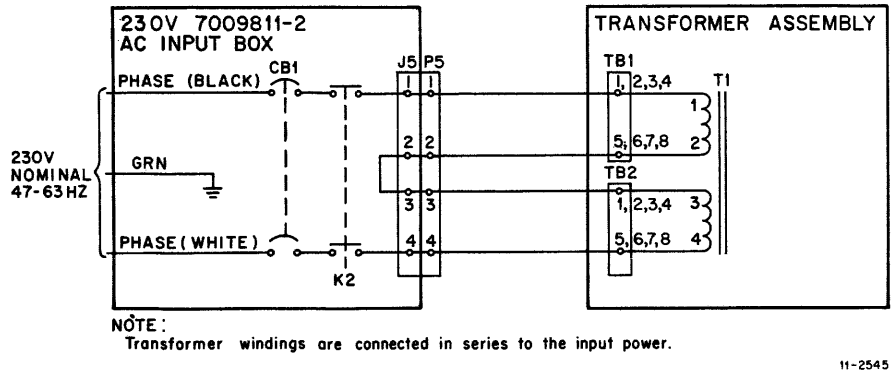


Figure 7-7 H765 Power Supply 230 V Power Configuration

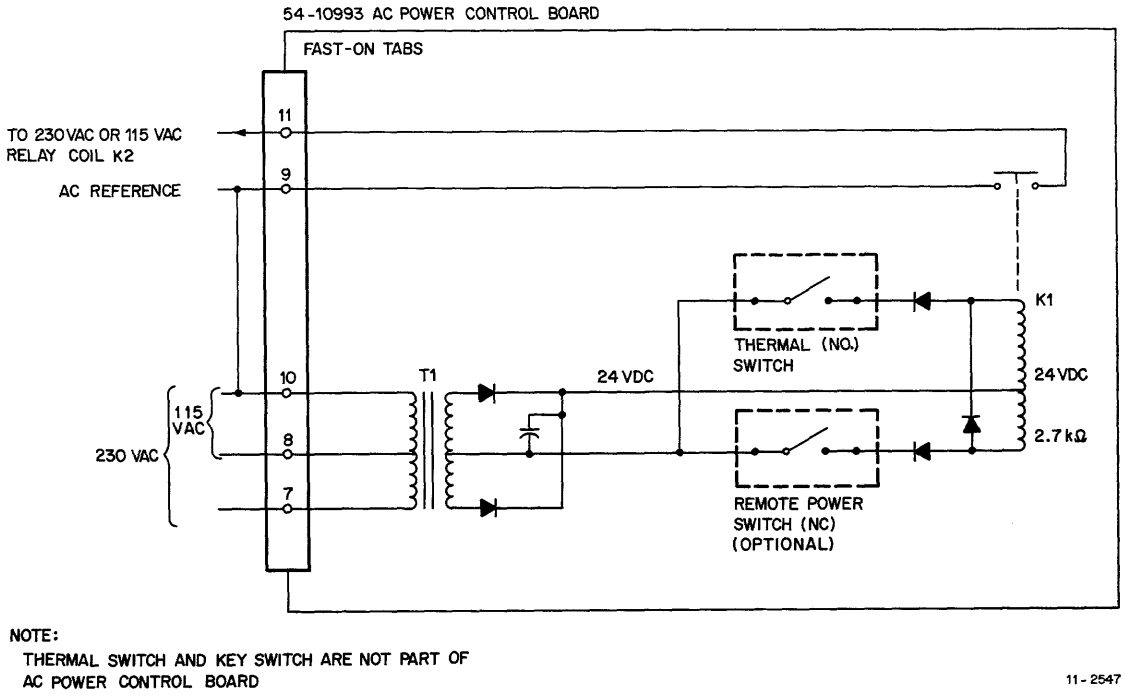


Figure 7-8 H765 Power Control Simplified Diagram

Transformer Assembly
The primary function of the transformer assembly is to step down the 115 Vac or 230 Vac input voltage, (E-UA-H765-0-0) to 28 Vac. There are five separate secondary transformer windings, one for each regulator.

Capacitors and varistors are connected across the primary of T1. The capacitors (C1, C2) are input line filters. The varistors (D1, D2) suppress voltage spikes in excess of 150 Vac. In addition, the transformer assembly routes 115 Vac from TB1 and TB2 to box fans 1 and 2, respectively.

5411086 Regulator
The +15 V output from the 5411086 regulator, internal to the H765 Power Supply, is not used by the XM15; only the AC LO and DC LO sensing circuits are used. These circuits are similar to those used in the H7420 Power Supply and are discussed in Paragraph 7.4.1.

Power Distribution Board
The Power Distribution Board (Figure 7-9) performs two primary functions: it routes the transformer assembly secondary output voltages to the regulators and routes the dc outputs of the regulators to the backplane.

Routing voltage to the regulators is accomplished via Mate-N-Lok J1/P1 and an etch on the Power Distribution Board. Mate-N-Lok P1/J1 routes 28 Vdc from four separate transformer secondaries to H745, H754, and both H744 regulators. The etch routes +15 Vdc from 5411086 regulator to the H745 regulator.

MATE-N-LOKS J11, J9, J7, J5, J3

PIN DESIGNATIONS

13	10	7	4	1
14	11	8	5	2
15	12	9	6	3

PIN	SIGNAL
1.	+5V
2.	+15V
3.	+20V
4.	+5V
5.	GROUND
6.	Not Used
7.	GROUND
8.	GROUND
9.	GROUND
10.	Not Used
11.	GROUND
12.	Not Used
13.	−15V
14.	−5V
15.	Not Used

MATE-N-LOKS J12, J10, J8, J6, J4

PIN DESIGNATIONS

4	1
5	2
6	3

PIN	SIGNAL
1.	GND
2.	LTC (Line Clock)
3.	DC LO
4.	AC LO
5.	Not Used
6.	Not Used

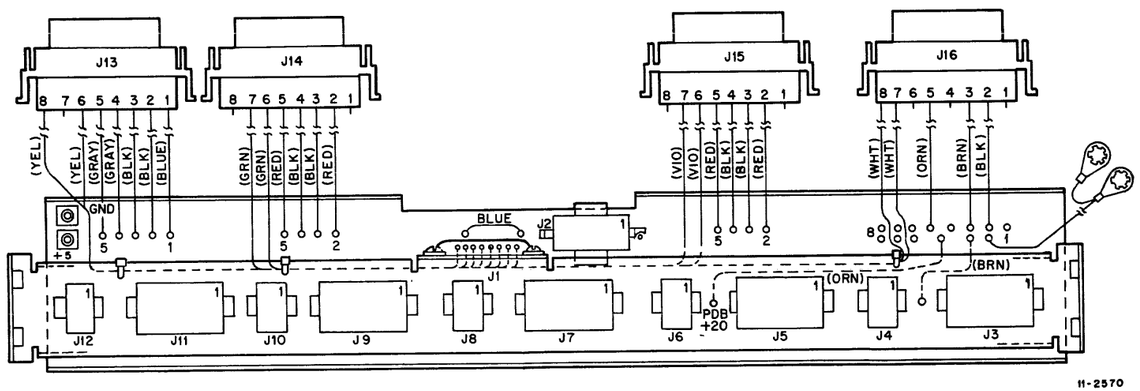


Figure 7-9 H765 Power Distribution Board

The regulator outputs are routed as follows:

H745 Regulator 1– –15 Vdc output is routed via the power distribution board etch to 15-pin Mate-N-Loks J3, J5, J7, and J11.

H744 Regulators 2 and 3 – Regulator 2, +5 Vdc output is routed via the power distribution board etch to 15-pin Mate-N-Loks J9 and J11. H744 regulator 3, +5 Vdc output is routed via the power distribution board etch to 15-pin Mate-N-Loks J3, J5, and J7. A unique configuration of the power supply is that two H744 regulators cannot be connected in parallel. Figure 7-10 is a simplified diagram illustrating the correct H744 to power distribution board configuration.

H754 Regulator 4 – +20 Vdc and –5 Vdc outputs are routed via the power distribution board etch to 15-pin Mate-N-Loks J3, J5, J7, J9, and J11.

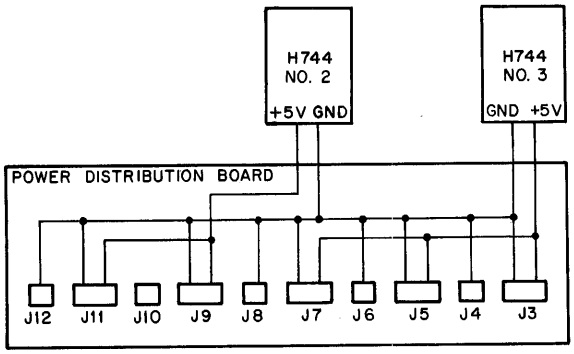
5411086 Regulator – +15 Vdc output is routed via the power distribution board etch to H745. The +15 Vdc is also routed via the etch to 15-pin Mate-N-Loks J3, J5, J7, J9, and J11. 5411086 LTX, AC LO L, and DC LO, L outputs are routed via the etch to 6-pin Mate-N-Loks J4, J6, J8, J10, and J12. Only the AC LO and DC LO outputs are used in the XM15.

The dc and signal outputs of Mate-N-Loks J3 – J12 are routed to the backplane via a power harness.

7.4.2.4 H765 Power Supply Regulators – The H765 Power Supply is a bulk supply which uses separate regulators to develop dc voltages for the XM15 Memory Processor and expansion memory units housed in BA11-K mounting boxes. H744, H745, and H754 are the separate regulators used with the H765 supply. Specifications and descriptions for these regulators are given in Paragraph 7.4.1.1.

7.4.2.5 Fuse Replacement – The only fuses in the H765 power supply are those internal to the H744, H745, or H754 regulators. Fuse replacement is apparent upon removal of a regulator (refer to Paragraph 7.4.2.8 for H765 regulator removal). Figure 7-11 shows the locations of the H765 regulators. Fuse ratings and DEC part numbers are given in Paragraph 7.4.1.5.

7.4.2.6 Troubleshooting – Regulator troubleshooting for the H765 power supply is the same as that for the H7420 power supply – refer to Paragraph 7.4.1.6.



NOTE:
Regulators H745, H754, and 5411086 output voltages are common to MATE-N-LOKS J3, J5, J7, J9, and J11.

11-2565

Figure 7-10 H744 Connection Diagram

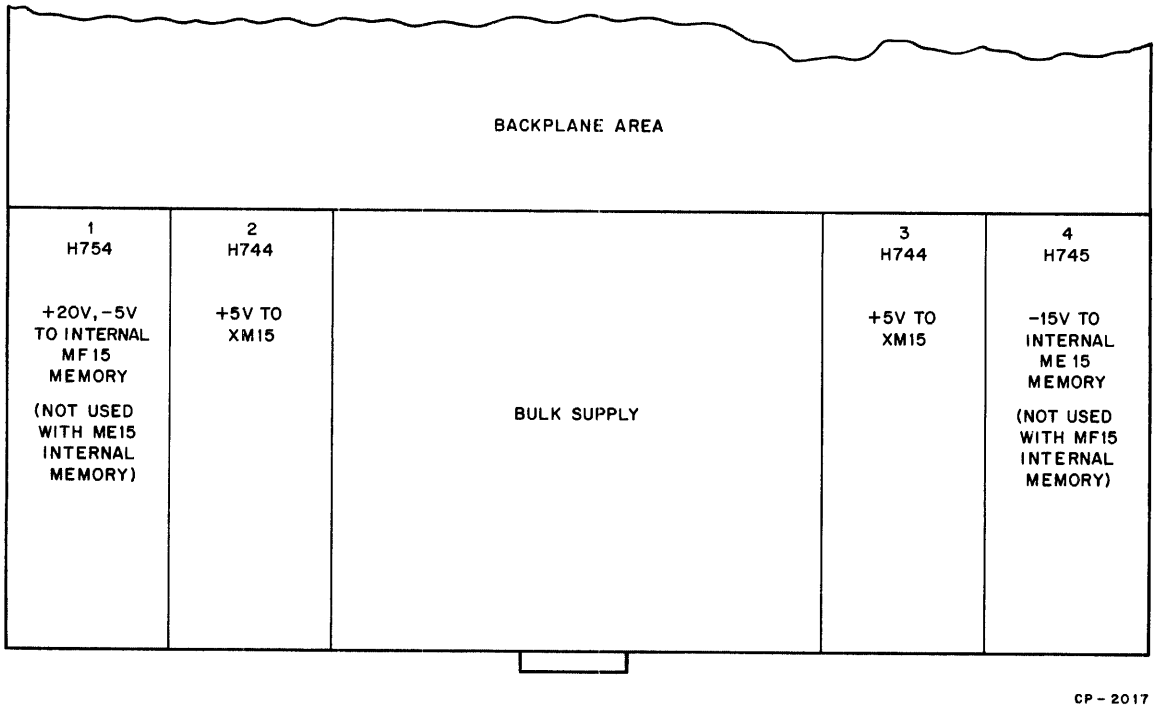


Figure 7-11 H765 Regulator Slot Assignments - Bottom View

7.4.2.7 Access Procedure - The H765 access procedure enables the H765 to be accessed for adjustments and subassembly removal. Refer to Figure 7-12 and perform the following steps:

1. Remove ac power by disconnecting the ac line cord from the ac power source.
2. Fully extend the BA11-K from the rack, ensuring that cables do not bind.
3. Remove the BA11-K top cover by removing six screws.
4. Remove the cable clamps by removing four screws.
5. To remove the H765 top cover, loosen the top three screws and remove the back four screws.

7.4.2.8 Regulator Removal - To remove the H744, H745, and H754 regulators from the H765 power supply, refer to Figure 7-13 and perform the following steps:

1. Perform the H765 power supply access procedure (Paragraph 7.4.2.7).
2. Rotate the BA11-K 90 degrees.

CAUTION
Hold H765 in place while removing screws.

3. Tilt the H765 power supply by removing two H765 power supply screws on each side of the H765 (Figure 7-12).

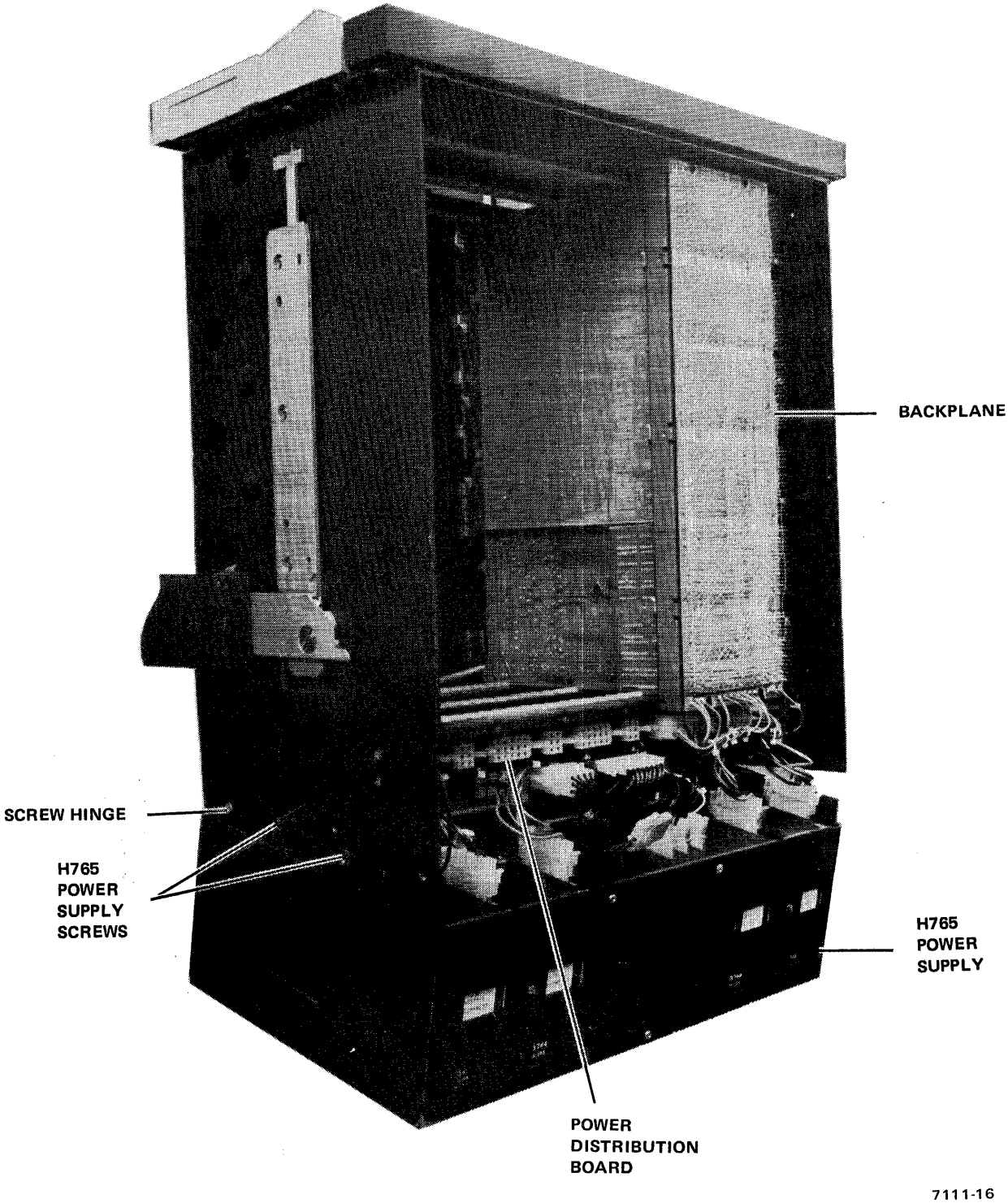


Figure 7-12 H765 Power Supply Access (Maintenance Position)

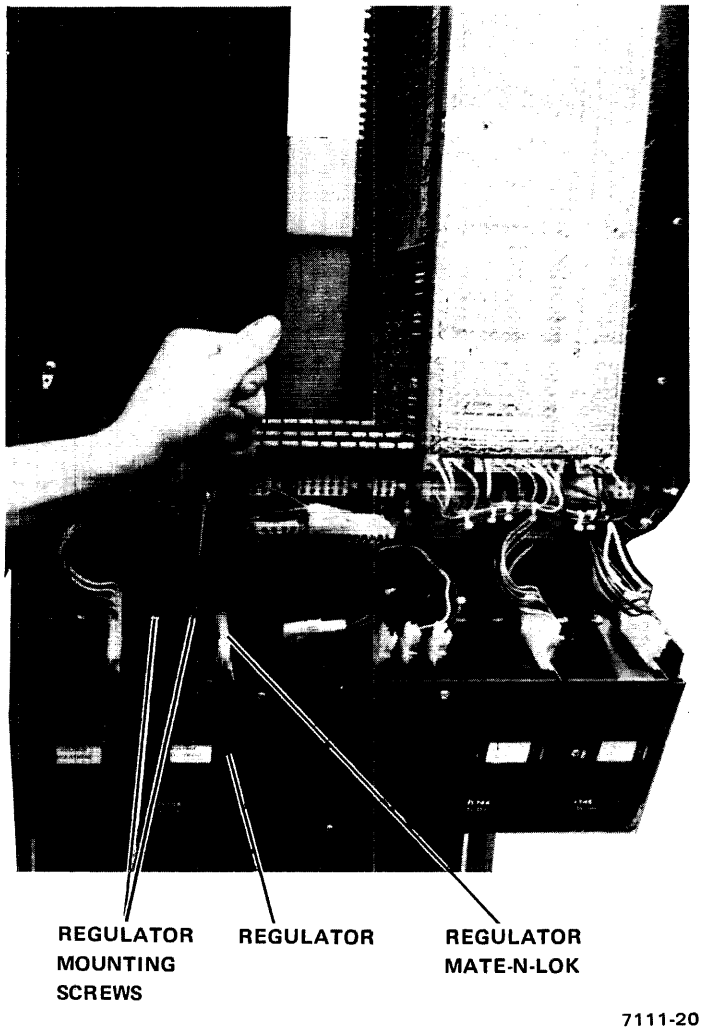


Figure 7-13 H765 Power Supply – Regulator Removal

4. Remove the bottom cover of the BA11-K.

WARNING
Power must be removed prior to removing regulators.

5. Disconnect the Mate-N-Lok from the regulator to be removed.
6. Remove three screws, two on the top and one on the bottom of the regulator (Figure 7-13).
7. Rotate the BA11-K 90 degrees to the horizontal position.
8. To remove regulator, slide it out.
9. Install new regulator per Paragraph 7.4.2.9.

7.4.2.9 Regulator Installation – To install an H744, H745, or H754 regulator in the H765 power supply, refer to Figure 7-13 and perform the following steps:

WARNING
Power must be removed prior to installing regulators.

1. Slide regulator into H765.

CAUTION
Use the correct length screws when installing regulator.

2. Install three screws, two on top and one on the bottom of the regulator (Figure 7-13).
3. Connect Mate-N-Lok to regulator.
4. Remove load from regulator by disconnecting Mate-N-Loks J3, J5, J7, J9, and J11 on the H765 power distribution board.
5. Connect H765 ac line cord to power source and apply power.

NOTE
If regulator crowbars, turn power off and rotate regulator voltage adjustment. Adjust fully ccw (below crowbar voltage). Turn on power.

6. Using a DVM, measure voltage at power distribution board to ensure that voltage is within limits specified in Table 7-5. Adjust voltage if necessary.
7. Turn off power and reconnect Mate-N-Loks J3, J5, J7, J9, and J11 on power distribution board.
8. Turn on power and check regulator voltage at backplane per Table 7-5. Adjust voltage if necessary.
9. Perform H765 access procedure (Paragraph 7.4.2.7) in reverse order.

7.4.2.10 H765 Power Supply – Fan Removal/Installation – To remove an H765 power supply fan, refer to Figure 7-14 and perform the steps below. Reverse the removal procedure to install a fan.

1. Perform the H765 power supply access procedure (Paragraph 7.4.2.7).

WARNING
The BA11-K should be in a horizontal position when removing fans.

Ensure that ac power is removed prior to replacing fans.

2. Remove all modules.
3. On the module side of the fan, remove the two screws holding the fan (Figure 7-14).
4. Slide the fan up and out of the H765; disconnect the jack from the fan (1-1/2 in. fan).

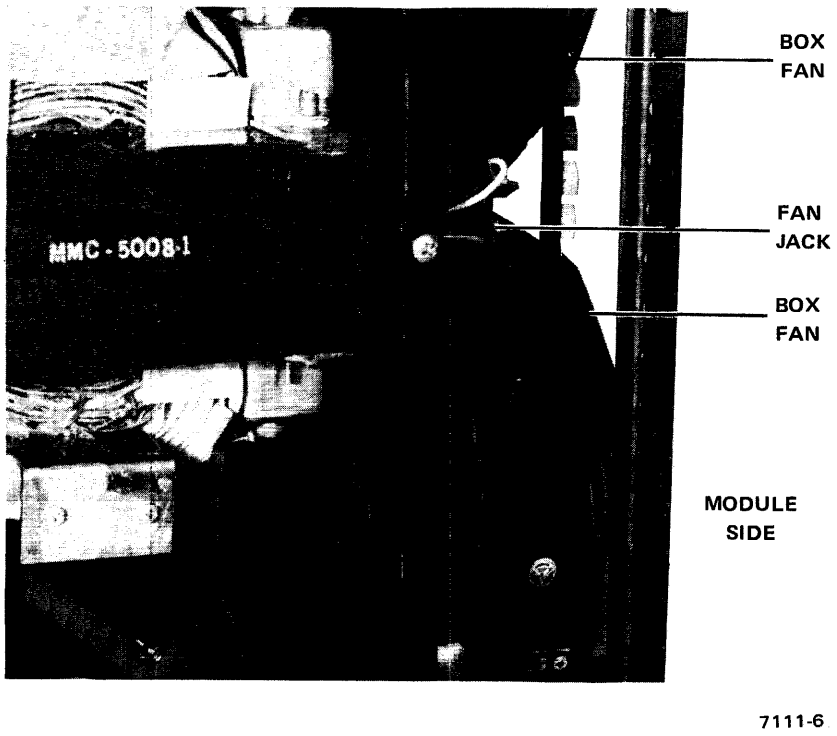


Figure 7-14 H765 Power Supply – Fan Removal

5. For boxes with 2 in. fans, remove the power distribution board and slide the fan from the bottom of the box chassis.

CAUTION

When installing the fan, do not tighten the screws beyond 10 in./lb. Tightening screws beyond 10 in./lb. may cause the fan to bind.

7.4.3 H740-D Power Supply

The H740-D power supply is used to supply console +5 V, -6 V (developed from H740-D -15 V output) and -15 V for the BA15 and KP15 TTY interfaces in the XVM System. The H740-D is a forced air-cooled unit operating from single-phase 115 V or 230 V (nominal), 47–63 Hz line voltage and develops three (+15 V, +5 V, -15 V) regulated output voltages. The output voltages and their characteristics are:

Voltage	Characteristics
+15 V (not used)*	Series regulated and overcurrent protected.
+5 V	Switching regulated and overvoltage and overcurrent protected.
-15 V	Switching regulated and overvoltage and overcurrent protected.

*The +15 V output is not used in the XVM System.

In addition, the H740-D generates the following control signals:

power fail early warning signals (AC LO L and DC LO L)
alternate AC LO L signal (PWR OK L)
clock signal (LTC L).

The power supply is completely contained in the H740-D chassis with one 3-wire input power cord (with plug) and one 15-socket Mate-N-Lok output connector, both accessible from the rear of the chassis.

The unit is equipped with overload and overtemperature protection devices. An input power circuit breaker removes power if input current is excessive (7 A @ 115 V, 4 A @ 230 V). A thermostat, mounted on the power supply heat sink, shuts down the power supply whenever heat sink temperature becomes excessive (100°C).

Figure 7-15 shows the H740-D, which is mounted in the XVM CPU cabinet, behind the H7420 power supply. Detailed information on the H740-D power supply (including maintenance and troubleshooting) is contained in the *H740-D Power Supply Maintenance Manual, DEC-11-H740A-A-D.*

7.4.3.1 H740-D Power Supply Specifications – Tables 7-3 and 7-4 list the power supply input and output specifications.

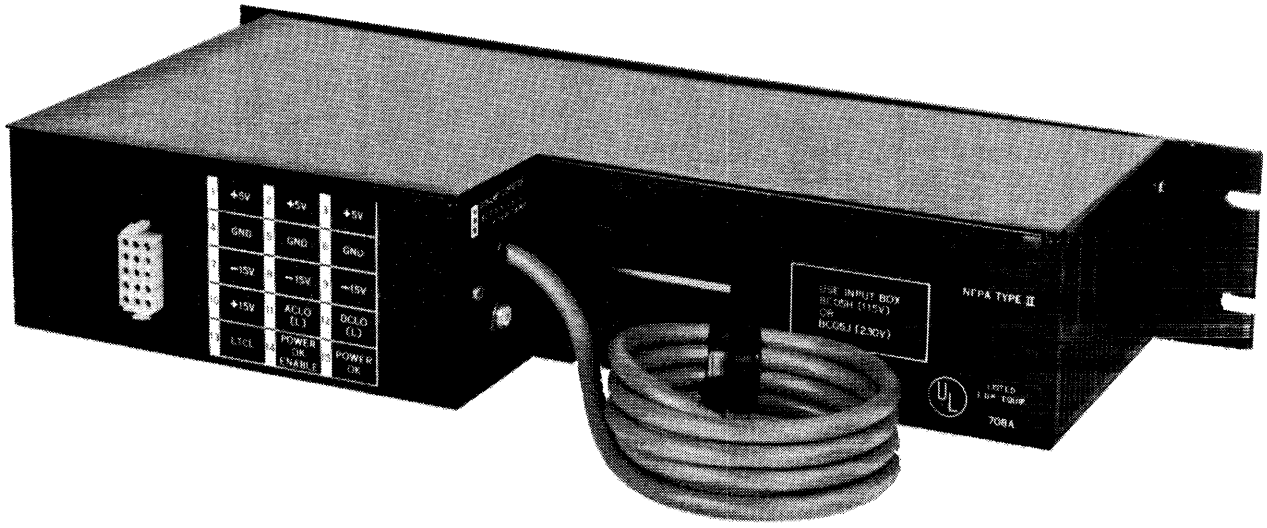


Figure 7-15 H740D Power Supply

Table 7-3
H740D Power Supply Input Specifications

Parameters	Specifications
*Input Voltage (1 phase, 2 wires, and ground)	95-135/190-270 V
Input Frequency	47-63 Hz
Input Current	5/2.5 A rms nominal
Input Power	325 W at full load
Inrush	80/40 A peak, 1 cycle
Input Breaker (part of BC05 Line Set)	7 A/4 A single-pole, manually reset, thermal

*Input voltage selection, 115 V or 230 V, is made by specifying the appropriate Digital Model BC05. All specifications are with respect to the BC05 input.

Table 7-4
H740D Power Supply Output Specifications

Parameter	Specifications
+15 V (NOT USED IN XVM)	
Load Range	
Static	0-1 A
Dynamic	0-1 A
Current Limit @ 25° C	1.3-1.7 A (-6.2 mA/ ° C)
Regulation (all causes including line, load, ripple, noise, drift, ambient temperature)	±5%
+5 V	
Load Range	
Static	0-20 A
Dynamic # 1	±5 A (within 0-20 A load range)
Dynamic # 2	No load – full load
Current Limit @ 25° C	24-29.4 A (-0.1 A/ ° C)
+5 V	
Regulation	
Line	±0.5%
Static Load	3%
Dynamic Load # 1	±2%
Dynamic Load # 2	±10%
Ripple and Noise	4% peak-to-peak
1000 Hour Drift	±0.25%
Temperature (0-50° C)	±1%
-15 V	
Load Range	
Static	0-7 A
Dynamic # 1	△ I = 5 A (0.5 A/ s)
Dynamic # 2	No load – full load (0.5 A/ s)
Current Limit at 25° C	10-13.3 A (-0.03 A/° C)

Table 7-4 (Cont)
H740D Power Supply Output Specifications

Parameter	Specifications
Regulation	
Line and Static Load	±1%
Dynamic Load # 1	±2.5%
Dynamic Load # 2	±3%
Ripple and Noise	3% peak-to peak
1000 Hour Drift	±0.25%
Temperature (0-50° C)	±1%
BUS DC LO L and BUS AC LO L Static Performance at Full Load (for 230 V Connection, Double Voltages Below)	
BUS DC LO L goes to high	74-80 Vac line voltage
BUS AC LO L goes high	8-11 Vac above voltage at which BUS DC LO L goes to high
BUS AC LO L drops to low	80-86 Vac line voltage
BUS DC LO L drops to low	7-10 Vac below voltage at which BUS AC LO drops to low
Hysteresis (contained in above specifications)	3-4 Vac
Output voltages still good	70 Vac line voltage

7.4.4 Voltage Checks and Adjustments

Correct XVM power system operating voltages are required for a properly operating XVM System. System voltages are measured with a DVM under normal load conditions at the load (usually backplane). Table 7-5 lists the XVM device (CPU, console, memory, etc.) and the power supply/regulator which supplies the operating voltages to the device. Test points and the loaded voltage level (as well as the accepted tolerance) for the test points are also given. Adjustment procedures for each power supply are presented in the following paragraphs.

7.4.4.1 H7420 Power Supply Voltage Adjustments – The H7420 power supply develops +5 V for the CPU (KP15), +15 V for the console, +5 V, -15 V for ME15 memory on the rear door of the CPU cabinet, or in the case of MF15 on the rear door, +5 V, +10 V, -5 V. CPU +5 V is supplied by H744 regulators 1 and 2 of the H7420 power supply (refer to Figure 7-4). +15 V for the console is supplied by the H744 regulator 4 and -15 V is supplied by H745 regulator 5 (Figure 7-4). If MF15 is on the rear door rather than ME15, +15 V is supplied by H744 regulators 3 and 4 and regulator 5 is now an H754, which supplies +20 V, -5 V (Figure 7-4).

Table 7-5
XVM Voltage Checks and Adjustments

Device	P. S. & Regulator	Test Points	Voltage & Tolerance	Comments
CPU (+5 V)	H7420 H744 regulator 1	KP15 K, L, M, N1A2	+5 ±0.25 Vdc	
CPU (+5 V)	H7420 H744 regulator 2	KP15 E, F, H, J1A2	+5 ±0.25 Vdc	
BA15 (+5 V) Console (+5 V)	H740D	BA15 A1A2	+5 ±0.25 Vdc	
Console (+15 V)	H7420 Internal regulator	856A TB1-8	+15 ±0.75 Vdc	Not adjustable.
Console (-6 V)	H740D	856A TB1-4	-6 ±0.5 Vdc	Not adjustable. Developed from H740D – 15 V.
MF Memory on CPU rear door (+5 V)	H7420 H744 regulator 3	+5 V TAB on 2nd backplane on rear door	+5 ±0.25 Vdc	Used only for second 32K of MF memory on rear door of CPU cabinet.
ME or MF Memory on CPU rear door (+5 V)	H7420 H744 regulator 4	+5 V TAB on 1st backplane on rear door	+5 ±0.25 Vdc	Used only for first 24K of ME or 32K of MF on rear door of CPU cabinet.
MF Memory on CPU rear door (+20 V, -5 V)	H7420 H754 regulator 5	+20 V TAB and -5 V TAB on both rear door back-planes	+20 ±1.0 Vdc -5.5 ±0.25 Vdc	Regulator 5 will be an H745 if ME memory is on rear door of CPU cabinet. (Refer to note on page 7-25 when adjusting H754.)
ME Memory on CPU rear door (-15 V)	H7420 H745 regulator 5	-15 V TAB on both rear door backplanes	-15 ±0.75 Vdc	Regulator 5 will be an H754 if MF memory is on rear door of CPU cabinet.
BA15 (-15 V) KP15 (-15 V)	H740D	BA15 K03U2	-15 ±0.75 Vdc	
MF internal memory (+20 V, -5 V)	H765 H754 regulator 1	+20 V TAB and -5 V TAB on MF backplane	+20 ±1.0 Vdc -5 ±0.25 Vdc	Regulator 1 will be an H745 if internal (XM15) memory is an ME memory. (Refer to note on page 7-25 when adjusting H754.)

Table 7-5 (Cont)
XVM Voltage Checks and Adjustments

Device	P. S. & Regulator	Test Points	Voltage & Tolerance	Comments
XM15 (+5 V)	H765 H744 regulator 2	Upper & lower left +5 V TABS on XM15 backplane for regulator 2	+5 ±0.25 Vdc	
	H744 regulator 3	Upper & lower right +5 V TABS On XM15 backplane for regulator 3.		
ME internal memory (-15V)	H765 H745 regulator 4	-15 V TAB on ME backplane	-15 ±0.75 Vdc	Regulator 4 will be an H754 if internal memory is an MF memory.

The H744, H745, and H754 regulators are all adjusted in the same manner. Adjustment potentiometers are located next to the output lamp on each regulator. Perform the following steps to ensure that the voltages are within the tolerances specified in Table 7-5. If a voltage regulator cannot be adjusted within tolerance, check for a bad regulator (Paragraph 7.4.1.6), faulty wiring, or a higher than normal load.

1. Using a DVM, measure the output voltages under normal load conditions at the backplane (Table 7-5).

2. Adjust voltages at the backplane to the tolerances specified in Table 7-5, as required.

3. Using a DVM, measure the voltage at the regulator (or power distribution board). Ensure that the maximum voltages at the regulator (Table 7-1) are not exceeded. These voltages represent the maximum regulator voltage prior to crowbar. (Do not adjust the regulator to these voltages.)

4. Using an oscilloscope, measure the peak-to-peak ripple content on all dc outputs (Table 7-1).

NOTE
H754 Voltage Adjustment

The +20 V adjustment is located on the side of the H754; the -5 V potentiometer is on the top, next to the connector. To set the output voltages, power down, disconnect the load, power up, and adjust for a 25 V reading between the +20 and -5 V outputs with the 20 V potentiometer. Then set the -5 V between its output and ground. Power down, reconnect the load, power up, and then check and adjust the outputs again. This procedure is necessary because the +20 V potentiometer (R17) actually sets the overall output of the regulator (25 V from +20 V to -5 V), while the -5 V adjustment (R21) controls the -5 V to ground output. (Refer to schematic drawing D-CS-H754-0-1.)

7.4.4.2 H765 Power Supply Voltage Adjustments – The H765 power supply develops +5 V for the XM15 Memory Processor logic and -15 V for the internal ME15 memory, or +20 V, -15 V for the internal MF15 memory. XM15 logic receives +5 V from H744 regulators 2 and 3 (refer to Figure 7-11) of the H765. If internal memory is an ME15, -15 V is supplied by H744 regulator 4. If internal memory is an MF15, +20 V, -5 V is supplied by the H754 regulator 1.

The adjustment procedure for the H744, H745, and H754 regulators used in the H765 power supply is the same as that used for the H7420 power supply. Refer to Paragraph 7.4.4.1 for the regulator adjustment procedure and to Figure 7-16 for H765 regulator adjustment locations.

7.4.4.3 H740-D Power Supply Voltage Adjustments – The H740-D power supply develops +5 V and -6 V (developed from the H740-D -15 V output) for the console, and -15 V for the BA15 and the KP15.

There are only three adjustments to the power supply. These adjust the three dc output voltages: +15 V, +5 V, and -15 V. A small screwdriver is all that is required. Clockwise adjustment of any of the potentiometers increases voltage. The potentiometers are located on the top side of the dc regulator module (Figure 7-17). Potentiometer designations are:

R35 (+15 V) – Not used on XVM
R50 (+5 V)
R26 (-15 V)

CAUTION

Do not adjust voltages beyond their 105 percent rating. Adjust slowly to avoid overvoltage crowbar, which will blow dc output fuses.

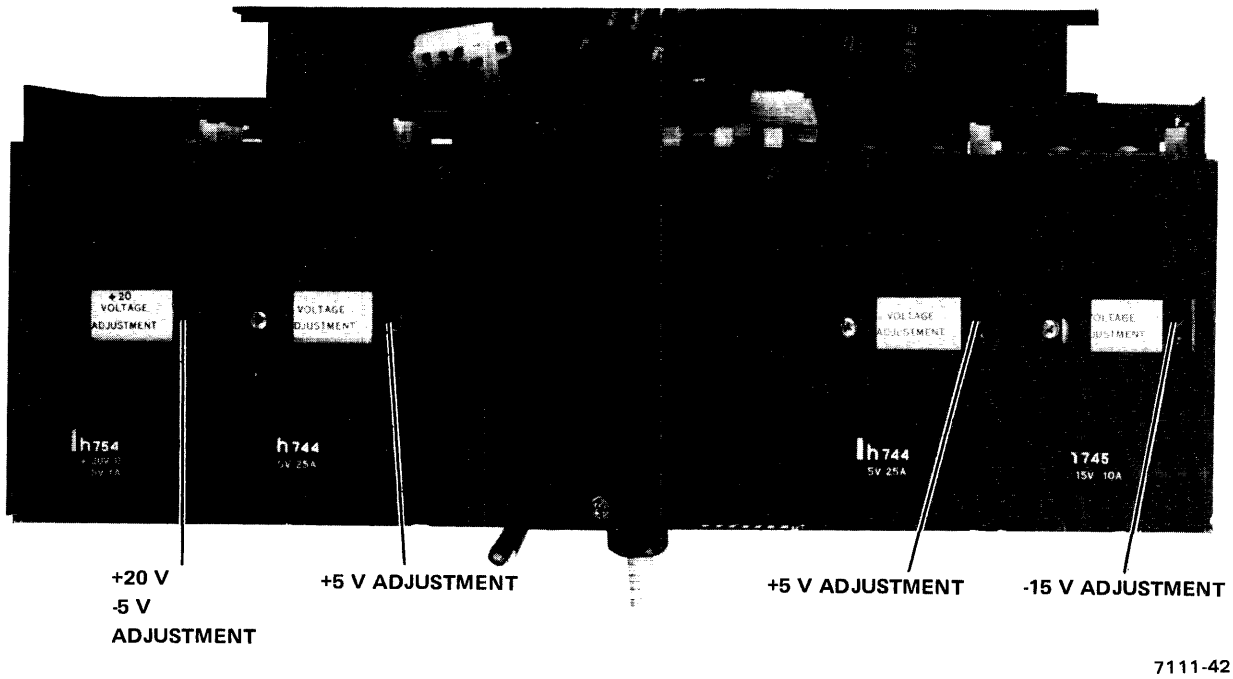


Figure 7-16 H765 Regulator Adjustment Locations

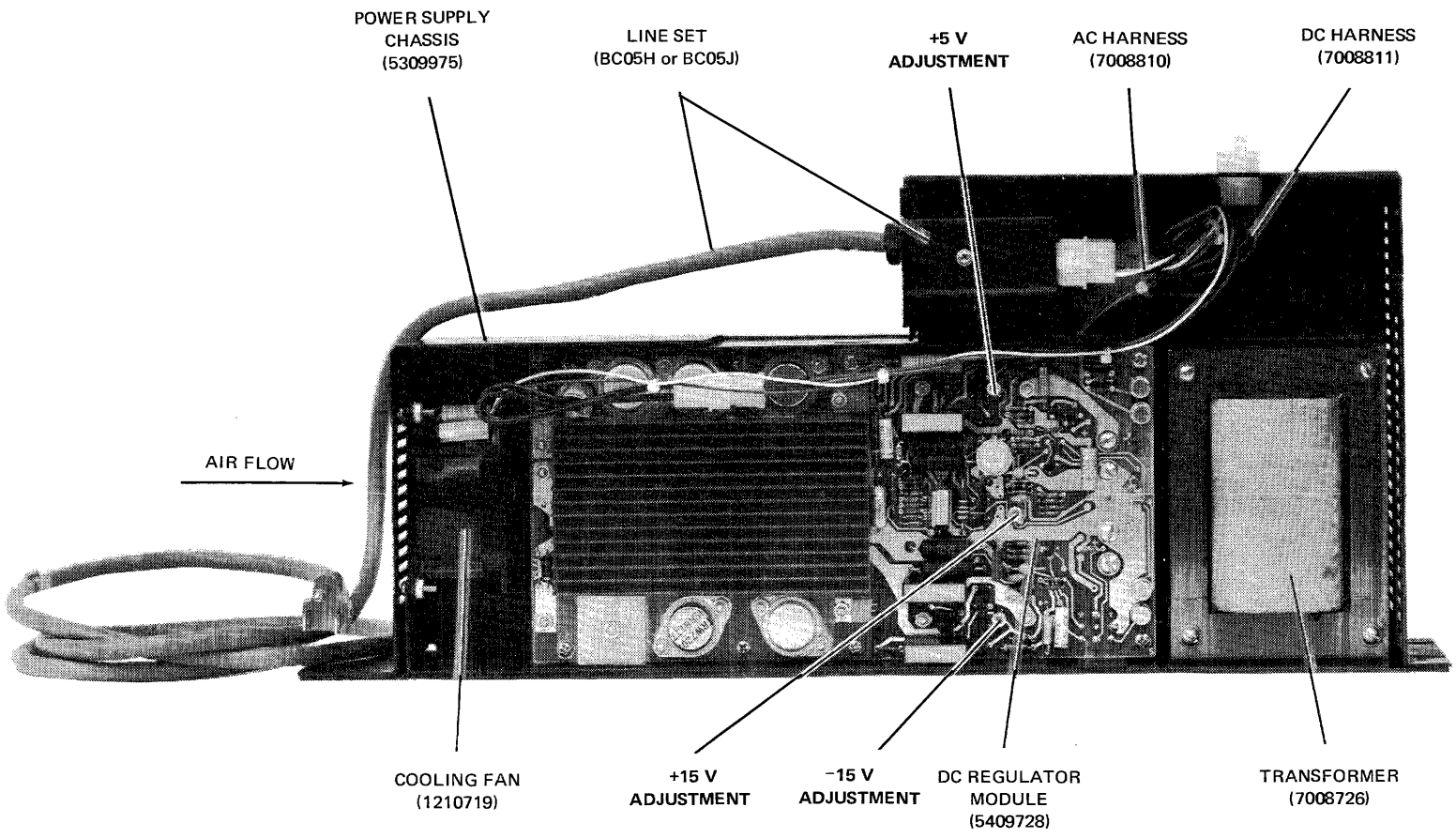


Figure 7-17 H740D Power Supply Component Locations

Section 2 – Troubleshooting and Timing Adjustments

7.5 GENERAL

The XVM is constructed of reliable TTL M-series modules. Proven reliability of this circuitry ensures relatively little equipment downtime due to logic failure. If a malfunction occurs, maintenance personnel should analyze the condition and correct it as indicated in the following procedures. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Personnel responsible for maintenance should be familiar with the system concept, the logic drawings, the theory of operation of the specific module circuits, and location of mechanical and electrical components.

The first step in repairing a reported malfunction is to isolate the problem. In a hardware-software system environment such as the XVM, the first step is to determine whether the problem lies in the hardware, the software, or both. The most practical way of doing this is by maintaining good communication between the operator, the programmer, and maintenance personnel.

Until the problem is isolated to either hardware or software, the cooperation of all parties concerned is essential. A step-by-step procedure should be used to trace the problem until a point is reached where all the inputs (conditions) to an element (of the hardware) are correct, but the output is not correct. The faulty element thus located should be repaired. Where necessary, the element itself may be subjected to step-by-step fault location (from output to input) until the source of the problem is found.

It is virtually impossible to outline all specific procedures for locating faults within digital systems such as the XVM. However, diagnosis and remedial action for a faulty condition can be undertaken logically and systematically in the following phases:

Preliminary investigation
System troubleshooting
Logic troubleshooting
Circuit troubleshooting
Repairs and replacement
Validation tests
Recording in log book

Before beginning troubleshooting procedures, explore every possible source of information. Gather all available information from those users who have encountered the same problem and check the system log book for any previous references to the problem or to a similar one.

Do not attempt to troubleshoot by using only complex system programs. Run the MAINDEC programs and select the shortest, simplest program available which exhibits the error conditions. MAINDEC programs are carefully written to include program loops for assistance in system and logic troubleshooting.

Once the problem is understood and the proper program is selected, the logical section of the system at fault should be determined. Obviously, the program which has been selected gives a reasonable idea of what section of the system is failing. However, faults in equipment which transmit or receive information, or improper connection of the system, frequently gives indications similar to those caused by computer malfunctions.

Reduce the program to its simplest scope loop and duplicate this loop in a dissimilar portion of memory to verify, for instance, that an operation failure is not dependent upon memory location. This process can aid in distinguishing memory failures from processor failures. Use of this technique often pinpoints the problem to a few modules.

7.6 SYSTEM TROUBLESHOOTING

System troubleshooting is the first step toward isolating and repairing a machine malfunction. If the machine cannot be started, refer to the section on console checks (Paragraph 7.6.1). If the machine is running, determine that hardware, not software, is causing the problem. If the problem is occurring with DEC software (compact, system monitor, etc.), obtain a certified copy of the program that is in good condition and attempt to repeat the malfunction. Generally, a recurring problem indicates a logic failure. If the problem occurs only with the user's software, an analysis of the failing program must be made. Use of the single time and single step is recommended. Some other items to check in the user's software are special bit assignments and functions.

Are Bank Mode, Page Mode, etc., being used properly?

Are memory fields being used properly?

Is the program making unwarranted assumptions; i.e., assuming that the accumulator will be clear on start-up, etc?

In general, attempt to isolate the problem to a major system; then exercise that system with the MAINDEC diagnostics. Then, if necessary, proceed to logic troubleshooting and repair.

7.6.1 Console Checks

Assuming that the problem is not clearly defined, the following checks should be made in an attempt to isolate basic machine faults. Any malfunctions observed at this time should be remedied before going further.

a. Power On – Does the power indicator on the console come on? Is the power up to specification?

b. Reset – Does the exec major state lamp light as well as the time state 3 lamp? Are the IR, MB, AC, PC, LINK and MO Registers cleared?

c. Deposit – Do the data switches transfer to the MO and MB? Do the address switches transfer to the OA? Are the fetch and time state 3 lamps on?

d. Examine – Do the address switches transfer to the OA and MO register? Do the contents of the location addressed appear in the MB register?

e. Deposit Next – Do the data switches transfer to the MO and MB? Do the contents of the OA register increment properly?

f. Examine Next – Do the OA and MO registers increment? Do the contents of each sequential memory location appear in the MB?

g. Deposit all 1s through memory using the repeat deposit next feature. Does the OA increment through to the final available memory address +1? When the first nonexistent memory address is accessed, does the computer stop in the fetch state at time state 3? Is the run light on and the nonexistent address in the OA and MO? Is the MB cleared? Does the repeat speed vary with the on/off speed switch? With the machine hung with the run light on, the stop and reset keys should have to be depressed together to clear this condition. Either one by itself should have no effect.

h. Examine all of memory for bit loss.

i. With the address switches equal to 0, and with all 1s in memory, depress reset and start. Does the run liqht come on? Do the PC and MO registers increment up through 17777? Does the AC equal all 1s? Do the time states 1, 2, and 3 lamps light?

j. Depress stop – Does the run light go out? Does the computer stop in fetch, time state 3?

k. Depress continue – Are the indications as in step i?

l. Deposit a Lac 100 in location zero, a jump to zero in location 1, and a 525252 in location 100. Depress start key. Does the machine cycle properly between the fetch and execute states? Does 525252 appear in the AC?

m. The reset performed in step b will force the instruction pre-fetch to an enabled condition. An IPF (M7174) malfunction may remain undetected for the tests in steps b through l. This may be prevented by grounding pin L17V2 in the KP15. The key functions DEPOSIT, EXAMINE, DEPOSIT NEXT and EXAMINE NEXT will now operate through IPF as follows:

1. EXAMINE – Causes the IPF to START and fill the instruction file with the memory locations following the address in the console address switches.

2. EXAMINE NEXT – If step 1 was performed, the data should be retrieved from the IPF File, not memory.

3. DEPOSIT – Will cause an abort in the IPF if the address specified is already contained in the IPF file.

4. DEPOSIT NEXT - Same as step 3.

The console keys are very useful when troubleshooting the IPF with pin L17V2 grounded. Be sure the ground is removed before normal operations are resumed.

n. Using the execute switch, try performing several instruction sets in the data switches. Does the processor react properly to each instruction? Can the instructions be repeated by the use of the repeat function?

If the computer performs the above operations successfully, the timing of the CPU, memory, console and I/O are approximately correct and troubleshooting at a processor level can commence.

7.6.2 Processor Troubleshooting

XM15, I/O and CPU processor troubleshooting is best achieved through the use of the MAINDEC diagnostic programs listed in Table 7-6. They provide the most rapid method of exercising these system areas.

Since the use of MAINDECs requires the Readin function of the Teletype or high-speed reader to be operational, this section of the processor must be checked first.

If the Readin section of the computer is not working, the operation of the reader IOTs should be checked by use of the execute repeat function of the console or by toggling in small read routines and comparing the processor operation against the appropriate timing and flowcharts.

The extensive use of indicators (including two maintenance positions on the console indicator switch) in the XVM and its peripheral devices was purposely included in the design. These indicators can (and should be) used as aids in troubleshooting problems. You will probably find that many problems can be found and repaired through the use of these indicators without the need of any other test equipment. Refer to Appendix D for indicator details.

Since the three main sections of the XVM System rely upon a request-grant system of operation, most basic problems should be fairly easy to locate. As an example, the CPU requests memory and waits for the XM15 to acknowledge with an address acknowledge signal. If the XM15 fails to answer, the processor will hang up, almost immediately pointing out the source of the trouble.

More subtle problems should be investigated through the use of the appropriate diagnostic program. Timing margins and module vibration often will point up intermittent problems more rapidly, although care should be exercised in the use of module vibrating, so as not to introduce more problems.

When troubleshooting peripheral devices, a check of the signals on the I/O Bus should be performed first, i.e., IOP pulses, device and subdevice select lines, etc., for proper levels and timing. Then, the appropriate peripheral diagnostic should be run and the problem investigated by use of the diagnostic writeup.

If the diagnostic will not run, check the operation of the individual IOTs for the peripheral. Can the command register be loaded? Can data be transferred to and from the devices data register? Can the status registers of the device be transferred to the processor? In the case of a 3-cycle device, a small routine to transfer blocks of data with +1 CA inhibit set will prevent wiping out core memory if there is a word count or current address problem. Once the fault has been isolated to a particular section, the next logical step is logic troubleshooting.

7.6.3 Logic Troubleshooting

Logic troubleshooting in XVM is best accomplished using the technique of reverse signal tracing. When a malfunction has been isolated to a section of logic, some type of failure loop, using either the reset-start switch combination, a small program, or a scope loop option in a diagnostic MAINDEC, should be used. Then, by comparing the logic engineering drawings with the machine status, that portion of logic which is causing the failure becomes evident. When troubleshooting the XM15 Memory Processor, the Signal Glossary in Appendix A should be consulted for signal functions.

NOTE

An unconnected input to a gate, if not tied to a +3 V pullup high, floats at approximately +1.9 V and three-state outputs used in the XM15 will be +2.2 – 2.4 V when in the high-impedance state.

Before attempting to troubleshoot the logic, make sure that proper and calibrated test equipment is available. Always calibrate the vertical preamplifier and probes of the oscilloscope before using. Make certain that the oscilloscope has a good ac ground, and keep the dc ground from the probe as short as possible.

Use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep can be synchronized by control pulses or by level transitions, which are available at individual module terminals on the wiring side of the logic. Care should be exercised when probing the logic to avoid shorting between pins. Shorting of signal pins to power supply pins can result in damaged components. Within modules, unused gate inputs are held at +3 V.

WARNING

Standard safety practices should be observed when working with energized equipment. Remember that peripherals are not always connected to the mainframe power control and may be energized when the XVM is off.

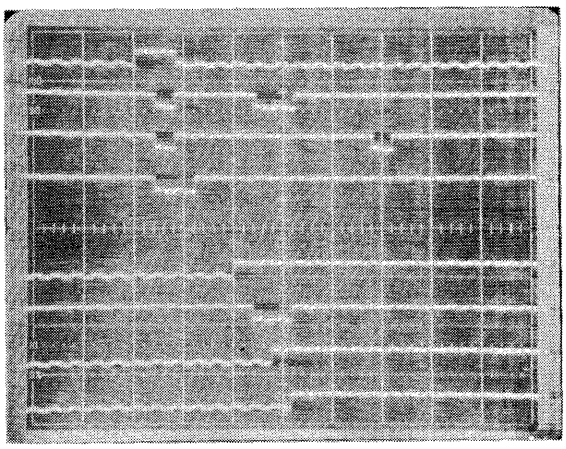
7.6.4 XM15 Memory Processor Troubleshooting

When a system fault has been isolated to the XM15, observing waveforms at the XM15 modules will aid in isolating the fault to a particular module. Figures 7-18 through 7-28 show key waveforms for the M7174, M7172, and M7173 modules. Each waveform is supported by the signal name and the test point at which the signal can be observed with an oscilloscope. The waveform figures are to be used as a means of comparison when viewing with an oscilloscope. It is suggested that the Signal Glossary in Appendix A be consulted for a description of the signal functions. A description of each waveform figure is presented in the following paragraphs.

7.6.4.1 M7174 Waveforms

SIGNAL	T. P.
START (1) H	(E26-9)
RD CLK L	(E73-6)
WRT CLK L	(E24-6)
RESET L	(E13-12)
INC ENB (1) H	(E43-5)
INIT INC L	(E13-8)
*ENB WPC (1) H	(E12-9)
ENB (1) H	(E43-9)

*Signal is no longer used



≈ 50 ns/div

Figure 7-18 M7174 IPF START Sequence Waveforms

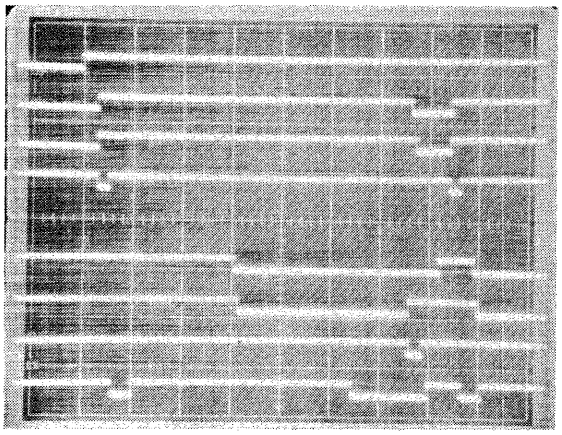
Figure 7-18 shows the key events during initial start of the M7174 IPF START sequence. When START sets, it causes the read and write program counters (RPC and WPC) to be loaded by RD CLK and WRT CLK, respectively. This action saves the current CPU address which is used to direct the IPF to the proper memory locations for retrieving instructions. RESET is generated to initialize the remainder of the IPF control circuits.

A few nanoseconds later, INC ENB sets and allows INIT INC to increment the RDPC. ENB WPC allows incrementing the WPC whenever the IPF posts a request for memory access. When ENB sets, the IPF is ready to process instruction requests from the CPU and to automatically fetch future instructions from memory.

The instruction sequence for Figure 7-18 is as follows:

```
LOC  200 IOT NOP (START begins here)
     201 NOP
     202 NOP
     203 JUMP 200
```

SIGNAL	T. P.
ENB (1) H	(E43-9)
BUSY (1) H	(E26-5)
IPF MSYNC H	(E77-10)
INC WPC L	(E25-6)
IPF CYC L	(E58-9)
LD (1) L	(E55-6)
DONE L	(E62-12)
WAIT L	(E14-2)



≈ 200 ns/div

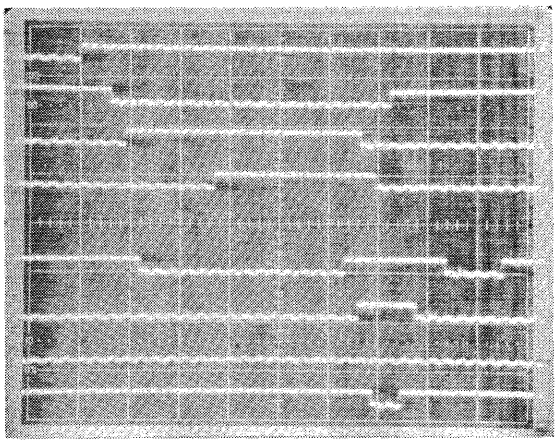
Note: IPF is held off by Port until IPF CYC goes true.

Figure 7-19 M7174 IPF WRITE (MEM READ) Waveforms

IPF writes (Figure 7-19) can begin following START (Figure 7-18). When ENB (Figure 7-19) sets, the IPF write circuits (write refers to memory reads followed by writing data into the IPF file registers) will begin a memory reference by asserting BUSY and IPF MSYNC while the WPC is incremented by INC WPC. The M7173 Memory Port module responds with IPF CYC, which places the IPF file in a condition to receive new data (LD sets). When the data has been deskewed by the M7173 module, DONE is asserted and causes the new data to be latched into the IPF file registers. The signal WAIT will be asserted whenever the instruction being requested by the CPU is being fetched from memory, but has not yet been latched into the IPF file registers.

The instruction sequence for Figure 7-18 is also applicable to Figure 7-19.

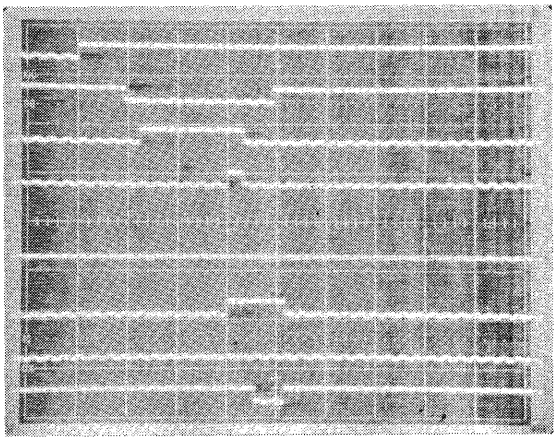
SIGNAL	T. P.
IPF H	E93-8
15 MSYNC L	E81-5
REQ (1) H	E31-5
CK H	E61-12
WAIT L	E14-2
15 SSYNC (1) H	E55-8
MISS (1) H	E74-5
INC RPC	E25-11



≈65 ns/div

Figure 7-20 M7174 IPF REQ (HIT with WAIT) Waveforms

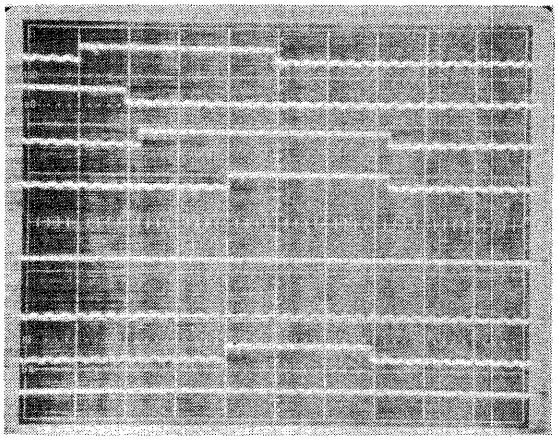
SIGNAL	T. P.
IPF H	E93-8
15 MSYNC L	E81-5
REQ (1) H	E31-5
CK H	E61-12
WAIT L	E14-2
15 SSYNC (1) H	E55-8
MISS (1) H	E74-5
INC RPC	E25-11



≈65 ns/div

Figure 7-21 M7174 IPF REQ (HIT without WAIT) Waveforms

SIGNAL	T. P.
IPF H	E93-8
15 MSYNC L	E81-5
REQ (1) H	E31-5
CK H	E61-12
WAIT L	E14-2
15 SSYNC (1) H	E55-8
MISS (1) H	E74-5
INC RPC	E25-11



≈65 ns/div

Figure 7-22 M7174 IPF REQ (MISS) Waveforms

Three M7174 IPF REQuests are shown in Figures 7-20, 7-21, and 7-22. If the current memory reference is determined to be an instruction fetch (IPF asserted) and 15 MSYNC is asserted, the M7174 IPF module begins a request sequence by setting REQ. After the delay time required for address verification, CK is asserted. At CK time, 15 SSYNC will set for a "HIT" (data is in the M7174 IPF file registers - Figures 7-20 and 7-21) or a "MISS" (data is not in the file registers - Figure 7-22) will set. For a "HIT", data is gated to the CPU from the file. For a "MISS", the CPU memory request is allowed to proceed through the M7173 Memory Port module directly to memory.

The instruction sequences for Figures 7-20, 7-21, and 7-22 are as follows:

Figure 7-20

```
200  NOP
201  NOP        WAIT occurs
202  NOP
203  JMP 200
```

Figure 7-21

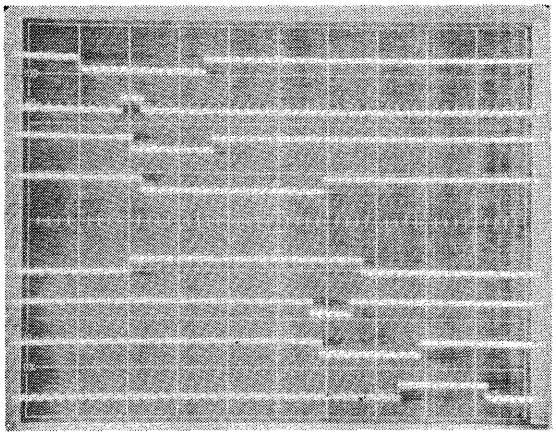
```
200  IOT NOP
201  NOP        WAIT does not occur
202  NOP
203  JMP 200
```

Figure 7-22

```
200  SKP
201  SKP        MISS occurs
202  JMP
```

7.6.4.2 M7172 Waveforms

SIGNAL	T. P.
MREQ L	E4-4
LD ADD H	E26-8
ADD ACK L	E3-5
MSYNC L	E32-3
BUSY (1) H	E16-9
15 DLY SSYNC L	E14-1
RD RST L	E3-3
DATA ACK H	E11-2



≈ 100 ns/div

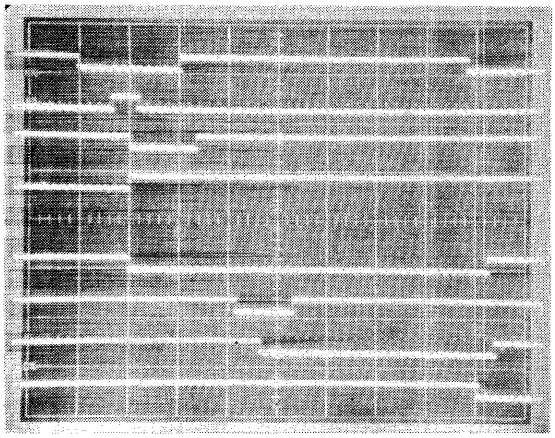
Figure 7-23 M7172 Read Cycle (From IPF) Waveforms

Figure 7-23 shows the standard control "handshaking" that occurs between the M7172 Interface module and the CPU, and between the M7172 and the M7173 Memory Port module. MREQ from the CPU causes LD ADD to clock the address on the MDLs into the address register and to assert MSYNC to the M7173 Memory Port module. BUSY also sets, indicating that the M7172 Interface module is processing a memory request. When the memory responds, the M7173 module deskews the data and posts 15 DLY SSYNC which loads the data into a holding register and releases the M7173 module. Next, RD RST is sent to the CPU where the data is received and DATA ACK is issued, completing the cycle.

The instruction sequence for Figure 7-23 is as follows:

```
200  NOP
201  NOP
202  NOP
203  JMP 200
```

SIGNAL	T. P.
MREQ L	E4-4
LD ADD H	E25-8
ADD ACK L	E3-5
MDL – 15 DATA H	E37-6
KT MSYNC L	E37-8
MRLS L	E4-6
MSYNC L	E32-3
15 DLY SSYNC	E14-1



≈ 120 ns/div

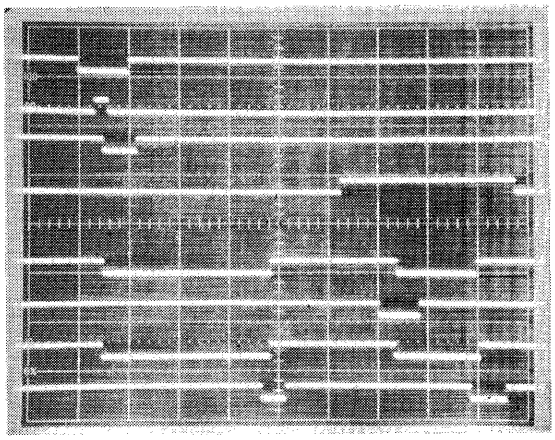
Figure 7-24 M7172 Write Cycle Waveforms

The M7173 write cycle (Figure 7-24) is similar to the read cycle (Figure 7-23) except that at ADD ACK time, the CPU places DATA on the MDLs and asserts MRLS. In addition, KT MSYNC is sent to the M7175 Memory Management module to allow address modification while the write data is being received and passed to the M7173 Memory Port module.

The instruction sequence for Figure 7-24 is as follows:

```
200  IOT NOP
201  DAC 200
202  NOP
203  JMP 200
```

SIGNAL	T. P.
MREQ L	E-4
LD ADD H	E25-8
ADD ACK L	E3-5
MDL – 15 DATA H	E37-6
KT MSYNC L	E37-8
MRLS L	E4-6
MSYNC L	E32-3
15 DLY SSYNC	E14-1



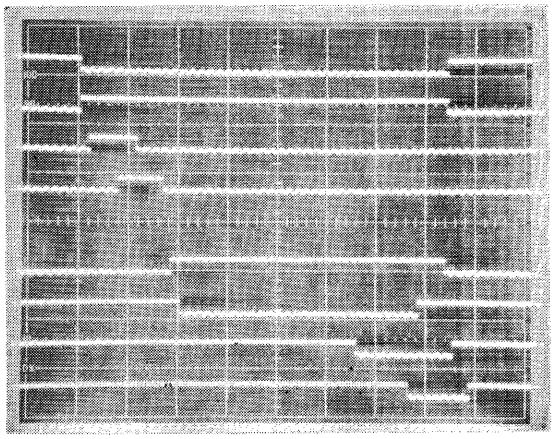
≈250 ns/div

Figure 7-25 M7172 Read/Pause/Write Waveforms

The read/pause/write sequence (Figure 7-25) was produced by the Real Time Clock which was started by executing the IOT-CLKON 700044 while the CPU was stopped.

7.6.4.3 M7173 Waveforms

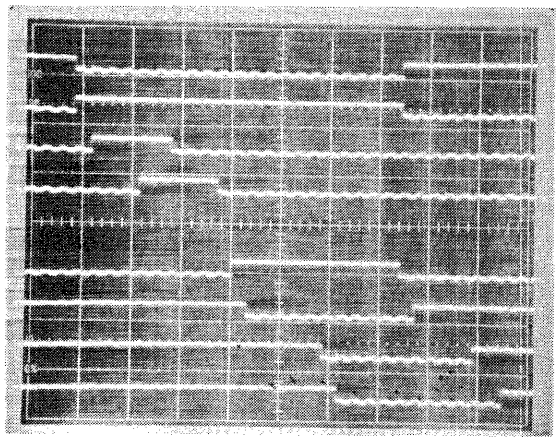
SIGNAL	T. P.
15 REQ L	E76-6
PORT REQ H	E76-8
REQ STB H	E67-6
CYC STB H	E67-10
PORT 15 MSYNC (1) H	E82-5
MEM MSYNC L	E46-3
MEM SSYNC L	E41-4
15 DLY SSYNC L	E63-6



≈120 ns/div

Figure 7-26 M7173 Read Cycle (CPU) Waveforms

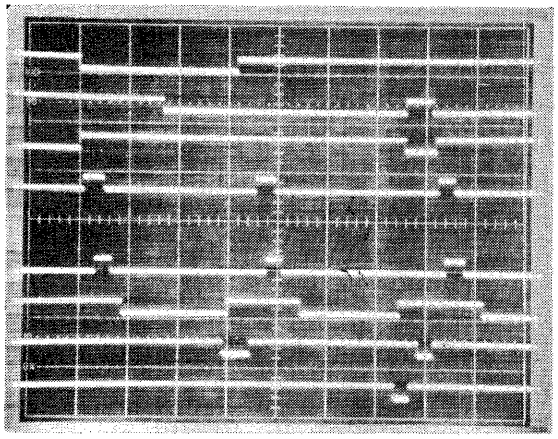
SIGNAL	T. P.
15 REQ L	E76-6
PORT REQ H	E76-8
REQ STB H	E76-6
CYC STB H	E67-10
PORT 15 MSYNC (1) H	E82-5
MEM MSYNC L	E46-3
MEM SSYNC L	E41-4
15 DLY SSYNC L	E63-6



≈ 75 ns/div

Figure 7-27 M7173 Write Cycle (CPU) Waveforms

SIGNAL	T. P.
15 REQ L	E76-6
IPF REQ L	E52-6
PORT REQ H	E76-8
REQ STB H	E67-6
CYC STB H	E67-10
MEM MSYNC L	E46-3
15 DLY SSYNC L	E63-6
IPF DLY SSYNC L	E47-6



≈ 220 ns/div

Figure 7-28 M7173 Read Cycle (CPU followed by two IPF) Waveforms

Figures 7-26, 7-27, and 7-28 show the key events in the selected M7173 Memory Port module when doing a read, write, and an operand read (by CPU), followed by the IPF read of an instruction. The first portion of each sequence shows the M7173 arbitration signals. For example, when 15 REQ is asserted, PORT REQ is generated and causes the timed sequence, where REQ STB loads all current requests into a holding flip-flop. REQ STB is followed by CYC STB which sets only the highest priority cycle flip-flop. With arbitration now complete, the M7173 begins the memory request by asserting PORT 15 MSYNC, which drives MEM MSYNC. Following the access time of the memory, MEM SSYNC is received by the M7173 and is delayed (for data deskew) before driving 15 DLY SSYNC.

The instruction sequence for Figures 7-26, 7-27, and 7-28 is as follows:

```
200 LAC 200
201 DAC210
202 NOP
203 JMP 200
```

7.6.5 Troubleshooting An Intermittent System

Intermittent problems within an XVM System should be isolated to a functional area (XM15, CPU, etc.). Then, checks should be performed on system cables, power, and timing. If these checks do not uncover the problem, the problem most likely exists in the logic (assuming that the software is not at fault). Logic troubleshooting is outlined in Paragraphs 7.6.3 and 7.6.4. Before troubleshooting any logic, perform the following checks:

Cables

a. Check all I/O cables for tightness.

b. Ensure that the I/O cables are inserted in the correct input and output locations.

c. RP02 Disk systems – check disk control and data cables. Look for pushed in pins at the end of the cable connected to the disk.

Power

a. Perform the dc voltage check and adjustment procedures (refer to Paragraph 7.4.4).

b. Check all Mate-N-Lok connectors on the XVM power supplies. These connectors should be lightly vibrated while running system exerciser diagnostics.

Timing

a. Check CP cycle time by doing a JMP SELF and looking at the duration of TS01 H (E30K2). Adjust potentiometer on M775 in location E30 for 250 ns.

b. Check I/O clock (N21D2) for 250 ns min.

c. Check console clock (N28D2) for 27.5μs. In many cases, erratic console clock operation can cause system halts with all registers reset.

NOTE
Refer to Paragraph 7.7 for timing adjustments.

d. Check IOP pulses for correct width on the I/O Bus. IOP1 + IOP2 should be 750 ns, IOP4 should be 500 ns for IOTs and 3-cycle devices; IOP4 should be 100 ns for single-cycle devices.

e. Check data pulses on the I/O Bus. The pulse should be +2.5 V to GND.

7.6.6 Module (Circuit) Troubleshooting

Engineering schematic diagrams of each module are supplied with each XVM System in the Module Manual and in the XM15 circuit schematics. They should be referred to for detailed circuit information. Engineering block schematic diagrams are contained in the *XVM Systems Maintenance Manual, Volume 2*. When troubleshooting the XM15 modules, refer to the Signal Glossary, Appendix A, for a description of module signals.

Visually inspect the module on both the component side and the printed-wiring side to check for overheated or broken components, etc. If this inspection fails to reveal any signs of trouble, or fails to confirm a fault condition observed, use the multimeter to measure resistance.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistance of diodes. Diodes should measure approximately 20 ohms forward and more than 1000 ohms reverse. (Front-to-back ratio should always be greater than 10 to 1.) If readings in each direction are the same, and no parallel circuit paths exist, replace the diode.

Measure in both directions the emitter-collector, collector-base, and emitter-base resistances of transistors. Short circuits between collector and emitter or an open circuit in the base-emitter path cause most failures. A good transistor indicates an open circuit in both directions between collector and emitter. Normally, 50 to 100 ohms exist between the emitter and the base, or between the collector and the base in the forward direction; an open circuit exists in the reverse direction. To determine forward and reverse directions, consider a transistor as two diodes connected back-to-back. In this analogy, PNP transistors would have cathodes connected together to form the base, and both the emitter and collector would assume the function of an anode. In NPN transistors, the base would be a common-anode connection; both the emitter and collector would be the cathode.

Multimeter polarity must be checked before measuring resistance, because many meters apply a positive voltage to the common lead when in the resistance mode.

Since integrated circuits contain complex circuits with only the input, output, and power terminals available, static multimeter testing is limited to continuity checks for shorts between terminals. Integrated circuit checking is best done under dynamic conditions and using a module extender to make terminals readily accessible. Using XVM engineering drawings and the M-series module schematics, an integrated circuit may be located on a circuit board in the following ways:

a. Hold the module with the handle in your left hand (the component side facing you).

b. Integrated circuits are numbered starting at the contact end of the board in the upper right corner.

c. The numbers increase toward the handle.

d. When a row is complete, the next integrated circuit is located in the next row at the contact end of the board (Refer to Figure 7-29).

e. The pins on each integrated circuit are located as shown in Figure 7-30.

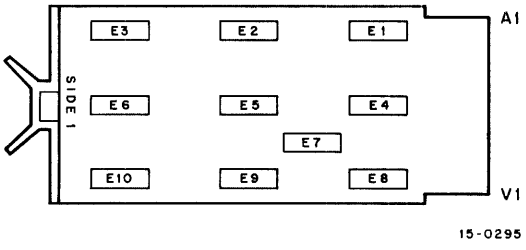
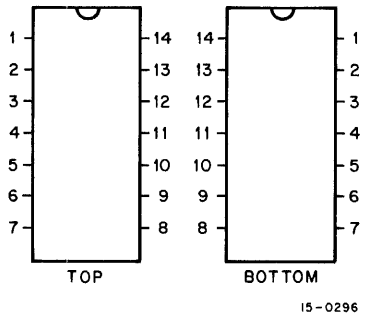


Figure 7-29 Integrated Circuit Location



NOTE
Refer to Appendix C for exceptions to the standard pining for V_{CC} and GND.

Figure 7-30 Integrated Circuit Pin Location

7.6.6.1 Module Repairs and Replacement

DEC recommends replacing defective modules with modules of known quality on a one-for-one basis and returning the suspect module to a DEC field office for subsequent repair and/or replacement. If, for expediency, field repairs must be performed, *it is imperative that the following procedure for the repair of M-series modules be strictly adhered to.* Procedures for repairing the multilayer modules used in the XM15 are detailed in Appendix B.

When soldering semiconductor devices (transistors, diodes, rectifiers, or integrated circuits, any of which may be damaged easily by heat, physical shock, or excessive electrical current), take the following special precautions:

a. Ensure that the equipment is turned off.

b. Use a heat sink, such as a pair of pliers, to grip the lead between the nearest joint and device soldered.

c. Use the smallest 6 V iron with an isolation transformer. Using an iron without an isolation transformer may result in excessive voltages present at the iron tip.

d. Perform the soldering operation in the shortest possible time to prevent damage to the component and delamination of the module-etched wiring.

e. Integrated circuits may be removed by using a solder puller to remove all excessive solder from contacts. Then, by straightening the leads, lift the integrated circuit from its terminal points. If it is not desirable to save the defective integrated circuit for test purposes, the terminals may be cut at the integrated body and each terminal removed from the board individually.

CAUTION

Never attempt to remove solder from terminal points by heating or rapping modules against another surface; this results in module or component damage. Always remove solder with a solder-sucking tool.

When removing any part of the equipment for repair and replacement, ensure that all leads or wires which are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals. Replace defective components with parts of equal or better quality and tolerance.

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When the repair has been completed, remove all excess flux by washing junctions with a solvent such as trichlorethylene. *Do not expose painted or plastic surfaces to this solvent.*

7.6.7 Validation Tests

Always return repaired modules to the location from which they were taken. If a defective module is replaced by a new one during a repair period, tag the defective module, noting the location from which it was taken, and the nature of the failure. When repairs are complete, return the repaired module to its original location and determine whether or not the repairs have corrected the problem.

To confirm the fact that repairs have been completed, run all tests which originally determined the problem. If modules were moved during the troubleshooting period, return them to their original positions before running the validation tests.

Anytime that a module is replaced by one from spares, return the module to its original location to confirm its defectiveness before initiating a repair procedure.

7.6.8 Recording In Log Book

A log book is supplied with each XVM System. Corrective maintenance is not complete until all activities are recorded in the log book. Record all data, indicating the symptoms displayed by the fault, the method of fault detection, the component at fault, and any comments which would be helpful in maintaining the equipment in the future. The log should be maintained on a daily basis, recording all operator usage and preventive maintenance results.

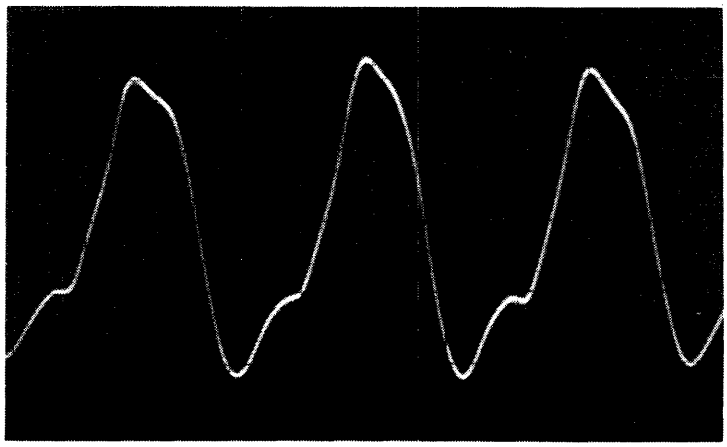
7.7 TIMING ADJUSTMENTS

The XVM System has been purposely designed to eliminate numerous delay and timing adjustments which have proved to be frequent sources of trouble in other machines. The aim of this design is to aid the serviceman in troubleshooting and maintaining the XVM System by eliminating time wasted in the adjustment of a large number of delays and timing chains. The XM15 Memory Processor logic has no timing adjustment. Timing adjustments for the ME15 Memory are detailed in the *ME15 Core Memory Maintenance Manual, EK-ME15-MM-001.* MF15 timing adjustments are in the *MF15 Core Memory Maintenance Manual, EK-MF15-MM-001.* CPU and I/O timing adjustments are covered in the following paragraphs.

NOTE
The CPU and I/O timing adjustments are taken at the +1.5 V point on the appropriate waveform.

7.7.1 CPU Timing Adjustment

7.7.1.1 CPU Clock - With probe #1, sync on and look at pin E30F2 in the CPU (HS clock H), adjust the potentiometer on E30 to give approximately a 62.5 ns cycle time (refer to Figure 7-31).



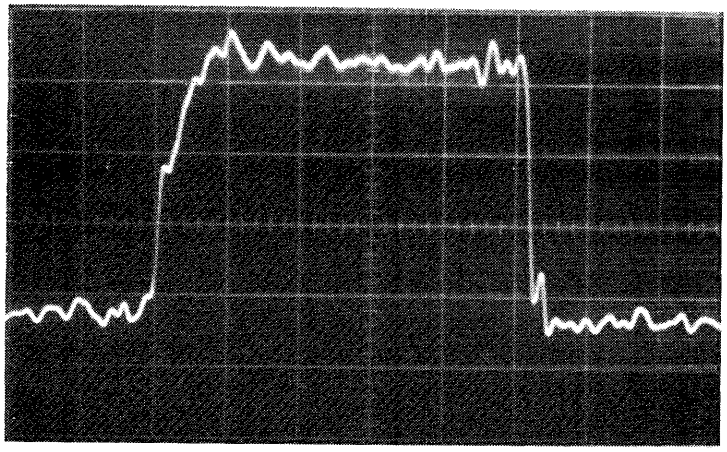
CLK: 62.5 ns
VOLTAGE: 1 V/CM

Figure 7-31 CPU Clock

Deposit the following program in memory and loop on it.

LOC	100/	1SZ	103	440103
	101/	JMP	100	600100
	102/	JMP	100	600100

With probe #1, sync on and look at E30K2 (TS01 H) (refer to Figure 7-32). Readjust the potentiometer on E30 to give a 250 ns duration.

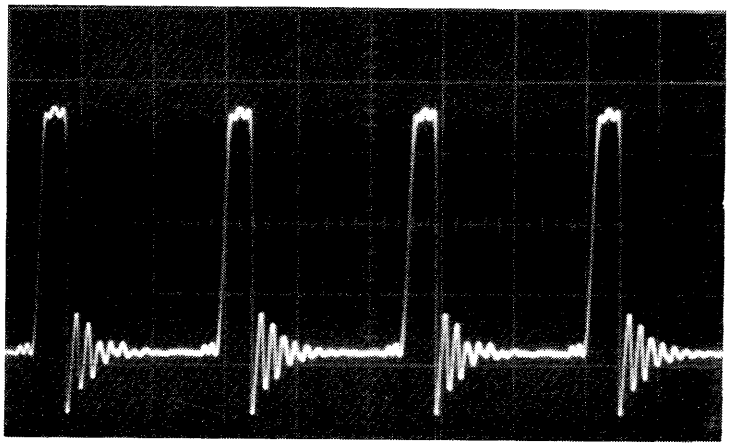


TS01: 250 ns
VOLTAGE: 1 V/CM

Figure 7-32 TS01 Duration

7.7.2 I/O Timing Adjustments

7.7.2.1 I/O Clock - The I/O clock is adjusted by observing with probe #1 pin N21D2 (I/O Clock) (refer to Figure 7-33). Adjust the pototentiometer on N21 so that the pulses occur every 250 ns.

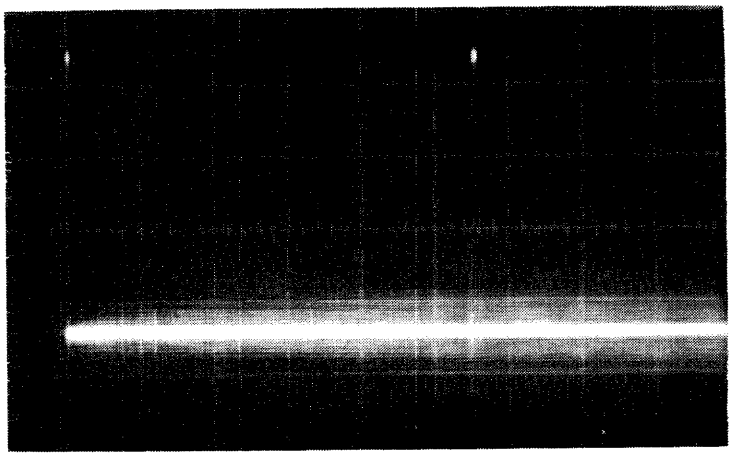


TIME: 100 ns/CM
VOLTAGE: 1V/CM

Figure 7-33 I/O Clock

7.7.2.2 I/O Read-Restart Tap – The XV100 System, unlike the PDP-15 and PDP-15C, does not require different delay tap selection for each of its various configurations, but is always wired from M18N1 to L18A1. (Refer to drawing D-BS-KD15-C-06.)

7.7.2.3 Console Clock – With probe #1, sync on and look at pin N28D2, CLK IN H (refer to Figure 7-34). Adjust the potentiometer on N28 so that the pulses occur every 27.5 μs.



TIME: 5 us/CM
VOLTAGE: 1V/CM

Figure 7-34 Console Clock

Section 3 - Scheduled and Preventive Maintenance

7.8 GENERAL

XVM scheduled and preventive maintenance are presented in this section. Scheduled maintenance uses the MAINDEC diagnostic programs supplied with the XVM System to verify System operation on a weekly basis. Preventive maintenance consists of tasks which are performed at least once every three months to keep the System operating at its peak. These tasks include such items as cleaning air filters, lubricating slide mechanisms, and checking timing, etc.

7.9 SCHEDULED MAINTENANCE

The XVM System must receive certain routine maintenance attention to ensure maximum life and reliability of the computer system. DEC recommends the following schedule:

1000 hrs: Electrical Inspection
500 hrs: Mechanical Inspection (or at least once every 3 months).

7.9.1 Weekly Maintenance

Time should be scheduled each week to run the MAINDEC Programs listed in Table 7-6. Each program should be run for a minimum of five minutes or one pass, whichever is greater. Take any corrective action needed at this time and log the results. The external cleanliness of the system should also be maintained on a weekly basis.

System downtime can be minimized by a rigid adherence to a preventive maintenance schedule. A dirty, clogged air filter can lead to machine failure due to overheating. All filters should be cleaned periodically. The procedure for cleaning filters is described under Preventive Maintenance Tasks.

7.9.2 Maintenance Test Programs

Table 7-6 lists the diagnostic programs designated MAINDEC. Altogether these programs provide a complete check of the system logic.

These programs are written in such a manner as to check certain circuits or functions of the machine, from a go/no-go situation to isolate basic logic faults, through the use of random number generation. This helps to isolate the more difficult random failures that may occur. Programs are designed to test the operability of the system under the interaction of various tests, coupled with peripheral requests and interrupts.

When an error or failure is detected by the diagnostic, it will either halt or produce an error typeout. The reason for the halt or typeout may then be determined through investigation of the console indicators and controls, or by use of a scope loop in the diagnostic if one is provided. The diagnostic writeups and listings should be consulted for the type of error failure and for the use of console controls and/or switch settings that will aid in isolating the machine fault.

7.10 PREVENTIVE MAINTENANCE

Preventive maintenance consists of procedures that are performed prior to the initial operation of the computer and periodically during its operating life. These procedures include visual inspections, cleaning, mechanical checks, and operational testing. A log should be kept for recording specific data which indicates the performance history and rate of deterioration. This information can then be used to determine the need and time for performing corrective maintenance on the system.

Table 7-6
MAINDEC Diagnostic Programs

Identification Number	Program Name
Basic Central Processor, Memory and Teletype	
MAINDEC-15-DOBO-D	Instruction Test - Document
1-PH	Part 1
2-PH	Part 1A
MAINDEC-15-DOBD-PB	Instruction Test - Part 2
MAINDEC-15-DOAC-PB	Hardware Index Register Test
MAINDEC-15-DODA-PH	JMP - Self Test
MAINDEC-15-DOEA-PH	JMP - Y Interrupt Test
MAINDEC-15-DAKAA	JMS - Y Interrupt Test
MAINDEC-15-DOKA-PH	ISZ TEST
MAINDEC-15-D1A0-D	Basic Memory Checkerboard Document
1-PB	Low
2-PB	High
MAINDEC-15-D1BC	Extended Memory Checkerboard
MAINDEC-15-D0CA	Memory Address Test
MAINDEC-15-D1CD	Extended Memory Test
MAINDEC-15-D1FA	Extended Memory Address Test
MAINDEC-15-D1GA	Memory Address Timing Test
MAINDEC-15-D7AA	4 K Basic Exerciser
MAINDEC-15-D7BC	8 K Basic Exerciser (if 8K of core)
MAINDEC-15-DALAA	LA36 Terminal Diagnostic
MAINDEC-00-D2G3	Binary Count Pattern Test Tape (for above)
MAINDEC-15-DAMXA	ME15 Extended Memory Checkerboard
MAINDEC-15-D0GB	EAE Test - Part 1
MAINDEC-15-D0HA	EAE Test - Part 2
MAINDEC-15-D2C0	High Speed Punch Test
MAINDEC-15-D2CC	High Speed Reader Test
MAINDEC-15-D2C0	Reader Test Tape (for above)
MAINDEC-15-DAAPA	I/O Test (API)
MAINDEC-15-D1EC	Memory Protect Test
MAINDEC-XV-DAKXA	XM15 Memory Management Diagnostic
MAINDEC-XV-DAKXB	XM15 Memory Management (IPF Diagnostic)
MAINDEC-15-DOJB	Power Fail Test
Peripherals	
MAINDEC-15-DAQAA	DECtape Basic Exerciser
MAINDEC-15-D3RA	DECtape Random Exerciser
MAINDEC-15-D8CB	LT09/LT19 Teletype Control Test
MAINDCE-15-ARFA	RF15 Disk Data Test
MAINDEC-15-D5BB	RF15 Multi-Disk Test
MAINDEC-15-D5CC	DISKLESS (not required during scheduled maintenance)
MAINDEC-15-D2UA	CR03B GDI Card Reader Test
MAINDEC-15-D1B2	Binary Cards (for above)
MAINDEC-15-D6BB	Display Diagnostic
MAINDEC-15-D4CC	Magnetic Tape Control Drive Function Timer
MAINDEC-15-D4DB	7 Track Data Reliability
MAINDEC-15-D4EB	9 Track Data Reliability

Table 7-6 (Cont)
MAINDEC Diagnostic Programs

Identification Number	Programs
Peripherals	
MAINDEC-15-D4GC	Random Exerciser
MAINDEC-15-DAKTA	Memory Relocate Test

Scheduling of computer usage should always include time for scheduled preventive maintenance checks. Careful testing during this scheduled time may turn up faults that occur intermittently during normal operation, or catch problems before they result in costly failure.

The following tasks should be performed at least once every three months.

a. Clean both the exterior and interior of the computer cabinet, using a vacuum cleaner and/or clean cloth moistened in a non-flammable solvent.

b. Clean all air filters. Use a vacuum cleaner to remove the dirt and dust, or wash the filters in clean warm water.

c. Lubricate all slide mechanisms, door pins and castors with a light machine oil. Wipe off any excess oil.

d. Inspect all wiring, cables and harnesses for cuts, breaks, fraying, wear, deterioration, kinks, strains and mechanical security. Replace or repair any defects found.

e. Inspect the following for both proper operation and/or mechanical security. Repair, replace, or tighten as required all lamps, switches, knobs, connectors, fuses, fans and covers. Ensure that all System fans are operating.

f. Inspect all module mounting panels to ensure that all modules are firmly seated in their sockets. Remove and clean any modules that may have collected excess dirt or dust.

g. Inspect the power supplies for leaky capacitors, overheated resistors, relay operation, etc.; replace or repair any defective items found.

h. Check the voltage outputs of all voltage regulators and make any necessary adjustments to bring the voltages into specification. If the voltage cannot be adjusted to meet the specification, the corrective maintenance must be performed.

i. Run all MAINDEC programs to verify proper machine operation. Each program should be run for a minimum of five minutes, or one pass, whichever is greater.

j. Perform all preventive maintenance procedures for each peripheral device connected to the XVM System, as directed by the individual instructions supplied with each option.

k. Check for circuit deterioration by varying the machine timing in accordance with the XVM engineering specifications.

l. Enter the results of the preventive maintenance in the log book.

7.11 MAINTENANCE EQUIPMENT

Special tools and test equipment required for maintenance are listed in Table 7-7. Except for DEC equipment, suggested commercial brands are given for purposes of specification only; their being mentioned does not constitute exclusive endorsement.

Table 7-7
Maintenance Equipment

Equipment	Specification	Model or Type
Multimeter	10 Kohms/V – 20 Kohms/V	Triplett model 310 or 630-NA
Oscilloscope		Tektronix type 454, 547
Probes	X10 with response characteristics matched to oscilloscope	Tektronix type P6010, P6047
Clip-on current probe	2 mA/mV or 10 mA/mV	Tektronix type P6022 with passive terminator
Recessed probe tip (2 each)		Tektronix
Unwrapping tool	30 gauge	Gardner Denver 505-244-475
Wire-wrap tool	30 gauge	Gardner Denver A-20557-29
30-gauge bit for wire-wrap tool		Gardner Denver 504221
Sleeve for 30-gauge bit		Gardner Denver 500350
Module extender (1)		DEC no. W984
Module extender (1)		DEC no. W982
Module extender (1)		DEC no. W987
Jumper wires		Assorted lengths affixed with 30-gauge Termi-Points
Screw driver	6-in non-conductive shaft	
Field service kit		DEC type 142
Diagnostic programs	(Supplied with system)	
Chip Clip	16-pin test clip	DEC no. 29-10246

APPENDIX A
SIGNAL GLOSSARY

A.1 INTRODUCTION

This signal glossary describes the functions of key signals used in the XM15 Memory Processor. Signals are listed for the M7172, M7173, M7174, M7175, and M7176 modules. Each signal name is followed by a circuit schematic reference for locating the source of the signal. Refer to the KP15 or KP15-C Print Set for the CP and IOP Signal glossary.

M7172

ABORT CLR (BCC2)
This signal is generated by the IPF, API, or Memory Management module. For the IPF, it indicates either that the IPF was not enabled, or that an abort was caused by a "MISS" "HALT", OR "WRT IN". The API module contains the IPF on/off IOT circuit and will stop the IPF by driving ABORT CLR. The Memory Management generates Abort Clear during an XCT instruction.

ADD 00 - 09 (BCA)
These address bits are driven by the Interface to the Memory Management module and may or may not be modified by that module before being driven out as 15 ADD 00–09.

ADD ACK (BCC1)
Generated by the Bus Interface and indicates to the CPU that the address has been loaded in the Bus Interface.

C1 CO (BCC1)
These two flip-flops are loaded from the 15s MRD and MWR lines and indicate whether a DATI, DATO or DATIP will be performed on memory. These lines are set as follows:

MRD	MWR	CO	C1	
F	T	F	F	= DATO
T	F	F	T	= DATI
T	T	T	T	= DATIP

CP ACT (BCC2)
This signal originates in the 15 and indicates whether the Central Processor is active or the I/O Processor is active.

DATA ACK (BCC1)
This signal originates in the 15 and indicates during a memory read, that the data has been accepted by the 15. During a read/pause/write, it indicates to the Bus Interface that the data may be strobed off the MDLs.

DCH SYNC (BCC2)
Generated by the I/O Processor to indicate that the next memory cycle is I/O, not CP.

IPF (BCC2)
This flip-flop, when set, indicates to the IPF (M7174) that the current memory access is an instruction fetch. It temporarily inhibits the request to the Memory Ports.

KT MSYNC (BCC1)
Generated by the Bus Interface for all memory references and initiates the operation of the Memory Management module.

BUSY (BCC1)
This signal inhibits any further memory requests from being accepted by the Bus Interface.

MRD (BCC1)
MRD is true when the CPU is requesting a memory read or read/pause/write.

MREQ L (BCC1)
This signal originates in the 15 and indicates that a memory access is being requested.

MRLS (BCC1)
Generated by the CPU. For memory reads, it terminates the memory cycle. For memory writes or read/pause/write, indicates that write data is on the MDLs.

MRLS ACK (BCC1)
Acknowledges the end of a memory reference and if the reference was a write, that the data has been loaded in the Memory Port.

MSYNC (BCC1)
Generated by the Bus Interface to load write data into the selected Memory Port and to condition the Memory Management module to produce 15 MSYNC. If switch-selected, this signal becomes 15 MSYNC.

MWR (BCC1)
MWR is true when the CPU is requesting a memory write or read/pause/ write.

PWR CLR (BCC1)
This signal originates in the 15 as a result of power going off or coming on, or depressing the RESET key. It generates clear for the Bus Interface, the Memory Management module, the IPF, the API, and if the external processor is not accessing memory, the Memory Port is cleared.

RD RST (BCC2)
This signal occurs during a read or read/pause/write to indicate to the 15 that the requested data is on the MDLs or that data should be sent to the memory in the case of a read/pause/write.

WRT MSYNC (BCC1)
This flip-flop when set, indicates that the current memory cycle is a write data cycle. It is also used for read/pause/write.

15 ADD 00–17 (BCA)
15 ADD 00–09 are driven by the Memory Management module or, if switch-selected, by the Interface. 15 ADD 10–17 are always driven by the Interface. All 18 bits are received by the IPF and Memory Port modules.

15 DC LOW (BCC1)
A DC Low condition in any XVM power supply will generate this signal. As a result, the Bus Interface, the IPF, and the Memory Ports are cleared.

15 DLY SSYNC (BCC2)
Generated by the Memory Ports or the IPF to indicate completion of the current memory reference.

15 MSYNC (BCC1)
Originates in the Memory Management module, or if switch-selected, in the Bus Interface and signals the start of memory references to the IPF and the Memory Ports.

M7173

BUS MSYNC (PRS)
When asserted, indicates that a request for memory access is being made on the external processor input.

CLR (PMPS)
This is the primary clear signal for the Memory Port. It occurs when:

Current cycle is terminated
MEM DC Low is asserted
DCH CLR is asserted
As a result of a time-out
When the XVM asserts PWR CLR.

CLR 11 MSYNC (PMPS)
This signal clears 11 MSYNC, sets 11 HOLD (and thus generates Bus SSYNC).

CYC STB (PMPS)
This signal is generated 60 ns after a Port request has been asserted. It is used to clock one of the four CYC flip-flops, according to which request line is true, and the priority the Port has established.

DATA →MEM (PMC)
This signal, generated by the Port control logic, is used to gate data from the XVM processor or the external processor through the memory data drives.

DCH ACT (PMC)
This signal is true during DCH cycle breaks. It is used to ensure that memory access will be quaranteed for each of the required 1, 2, or 3 cycles possible.

DCH ACT (B) (PMC)
This signal originates in the M7172 module and is used to condition the Memory Port modules for an XVM DCH memory request. The next 15 MSYNC following the assertion of DCH ACT (B) generates DCH REQ to the Port. These events occur simultaneously in both Memory Port modules. This ensures that their cycle and single-cycle, back-to-back memory requests will have control of both Memory Ports during each of the multiple requests for memory.

DCH CLR (PMC)
This signal is generated by the Port logic during XVM IPU 1, 2, or 3 cycle breaks, or whenever a false request is made. It is used to clear certain control flip-flops in the case of false requests, and it is used to clear pending requests during DCH cycles.

DCH CYC (PRS)
This signal, when accompanied by 15 REQ, indicates that the XVM IPU request has been granted a DCH memory cycle. It is used to start the memory bus dialogue.

DCH REQ (PMC) (This signal is no longer used.)
This flip-flop is set when the XVM I/O requires memory access for DCH cycles. See also DCH ACT.

DIS PC (PMC)
Disable power clear is generated by the Port logic to inhibit power clear from the XVM, which generates memory INIT, during an external processor memory cycle.

DIS REQ (PMPS)
This flip-flop is set whenever a Port cycle has been committed. It is used to block out any further Port requests and specifies the pulse width of CYC STB.

ENB 15 DATA (PMC)
During XVM memory reads, this enable drives memory data from the Memory Port module to the Bus Interface module.

ENB 15 →MEM (PMC)
When true, generates the signal DATA MEM and thus enables the data multiplexer output to be driven to memory.

ENB BUS →MEM (PMC)
This signal is generated during memory write cycles to gate the external processor data to the memory drivers. When true, the external processor data is gated through the Port MUX. When false, XVM data is gated through the MUX.

ENB LINES 1, 2 (PMC)
These two signals, generated by the Port logic, are used to gate the 15 address lines to memory during an XVM memory access. They are also generated by default as soon as the 15 REQ is asserted, provided no other cycle is pending.

IPF CYC (PRS)
This signal indicates that the IPF module has been granted memory access. It is used to start the memory bus dialogue and enables data to the IPF data bus.

NOTE
Data flow is only from the port to the IPF module.

IPF MSYNC (PMPS)
When asserted, initiates a memory read request to the Port.

IPF PORT SEL (PRS)
This signal is generated in the M7174 module and is used to enable IPF requests in the Memory Port. See also 15 PORT SEL.

IPF REQ (PRS)
This signal is generated in the Port logic whenever the IPF is attempting to access memory. It is used to start the Port priority arbitration if a previous memory cycle is not pending.

LD 11 DATA (PMC)
During external processor memory reads, the memory data is loaded into a holding register by this signal.

LD 15 DATA (PRS)
During XVM memory writes, this signal loads data into a holding register. The loading occurs independent of current Port activity.

MEM DC LOW (PMC)
This signal is generated by any one of the XVM power supplies and is driven on the XM15 bus where it causes the Memory Ports to be cleared, due to power supply failure.

MEM DLY SSYNC (PMPS)
This is the 70 ns delayed version of MEM SSYNC. It is used to generate either 15 DLY SSYNC, IPF DLY SSYNC, or CLR 11 MSYNC.

MEM INIT (PMC)
Initialization of memory is allowed whenever the external processor is not accessing the Memory Port. MEM INIT is generated by 15 PWR CLR. (See DIS P.C.)

MEM MSYNC (PMPS)
This signal, generated by the Port logic, is asserted whenever a Port request has been granted. It is used to signal the memory to start a memory cycle.

MEM SSYNC (PMPS)
This signal, generated by the memory, is asserted whenever the Port has been granted memory access. It is used to generate slave sync to whichever one of the three processors has its CYC flip-flop set.

MSYNC (PRS)
For XVM memory writes, this undelayed MSYNC will load 15 data into its holding register.

PORT 11 MSYNC (PMPS)
This signal is generated during the external processor access cycle. It is used to generate master sync to the memory.

PORT 15 MSYNC (PMPS)
This signal is generated during an XVM CPU access cycle whenever the Port grants priority. It is used to generate master sync to the memory.

PORT IPF MSYNC (PMPS)
This signal is generated during an access by the IPF module. It is used to generate master sync to the memory.

PORT REQ (PRS)
This signal is generated by the Port logic whenever a request for memory access has been made and the requesting device has asserted its address lines. It is used to start the Port arbitration timing.

REQ + 100, 150, 200 (PMPS)
These are the key timing pulses generated by the Port to arbitrate current requests from memory. The end result will be setting one of these MSYNC flip-flops.

REQ STB (PMPS)
This signal is generated by the Port logic whenever a memory access is required. It is used along with the REQ from the device to start the priority arbitration.

TIMEOUT (PMC)
This condition will occur whenever Port MSYNC goes false without memory SSYNC asserted. It will cause the port module to be cleared by CLR.

11 CYC (PRS)
This signal indicates that the External Processor has been granted memory access. It is used to start the memory bus dialogue, enable the data to pass from the external processor data bus to the memory data drivers, and gate the memory data receivers through the bus data drivers.

11 DATIP (PMC)
This flip-flop sets for read/pause/write cycles. It presents IPF REQ or XVM requests from gaining control of the Memory Port between read and write portions of the DATIP.

11 HOLD (PMPS)
This signal is generated by the Port control logic during external processor cycles. It is used to generate slave sync, to be sent back to the external processor and to gate memory data to the external bus data drivers. When this flip-flop is set, the Port is released to service other requests as the data has been latched up.

11 INH (PRS)
Generated by 11 DATIP or 15 DC LOW, it prevents 15 or IPF REQ from gaining control of the Memory Port.

11 PORT SEL (PRS)
This signal is generated in the M7174 module and is used to enable 11 requests in the Memory Port. (See also 15 PORT SEL.)

11 REQ (PRS)
This signal is generated in the Port logic whenever the external processor is attempting to access memory. It is used to start the Port priority arbitration if a previous memory cycle is not pending.

15 ADD 00–17 (MPA)
These address bits are held and driven by the Bus Interface (M7172). They are presented to the Memory Ports and the IPF for XVM CPU or I/O requests.

15 CYC (PRS)
This signal indicates that the XVM CPU has been granted memory access. It is used to start the memory bus dialogue, enable data to pass from the Bus Interface data lines to the memory data drivers, and gate the memory data receivers through the 15 data drivers.

15 DATIP (PMC)
This flip-flop sets for read/pause/write cycles. It prevents IPF REQ or 11 REQ from gaining control of the Memory Port between the read and write portions of the DATIP.

15 DLY SSYNC (PMPS)
This signal is generated by the Port control logic during XVM memory read or write operations. It indicates to the Bus Interface that the requested data is on the data lines.

15 MSYNC (PRS)
This signal is asserted by the M7175 Memory Management module following any address modification specified and is used to generate 15 REQ.

15 PORT SEL (PRS)
A selectable single-bit address is used to enable 15 requests in the Memory Port. The selected bit becomes 15 PORT SEL. One of two modes of Port addressing results from this selection: block mode, where all memory below the address specified by the selected bit will be on one Port and an equal amount above that address on the other Port, and LSB mode, where all even addresses are on one Port while odd addresses are on the other.

15 REQ (PRS)
This signal is generated by the Port whenever the 15 is attempting to access memory and the IPF signal is not asserted. It is used to start the Port priority arbitration if a previous memory cycle is not pending.

15 WAIT (PMC)
This signal is generated by the Port logic whenever the XVM is making a request for memory access and instruction prefetch is not specified. Because the address lines are enabled as soon as an XVM request is made, this signal is used to hold off the address lines if an IPF or external processor cycle is in progress.

ABORT (IPCI)
A flip-flop which stops the current operation for one of several reasons:

Because a WRT IN has occurred.
A MISS has occurred.
An instruction has been fetched which breaks sequence, i.e., JMP, JMS, or CAL.

ABOVE (IPCM)
This signal, which is the output of the WCMP, establishes the upper boundary of the file. When true, it indicates that the current access is above the upper boundary.

BELOW (IPCM)
This signal, which is the output of the RCMP, establishes the lower boundary of the file. When true, it indicates that the current access is below the lower boundary.

BUSY (IPC2)
A flip-flop which indicates that the IPF is currently fetching an instruction from memory.

CCMP (IPPC)
The CCMP is a comparator which compares bits 0–5 of the 15 address and bits 0–5 of the CPC to determine if the current access is within the current 4K segment.

CK H (IPC1)
A signal which indicates that the comparators are stable and may be used. It is used to clock Slave Sync (SSYNC) and MISS.

CLR ENB (IPC1)
Causes the IPF to be restarted. It is asserted when the current 15 address is out of bounds, a request has been made to modify data within the IPF file, or the program has broken sequences.

CPC (IPPC)
The Common Program Counter is loaded from bits 0–5 of the 15 address. The contents of the CPC are used along with the WPC to provide an address to the Memory Port. It is also used in conjunction with the WPC and the RPC to determine the upper and lower boundaries of the current contents of the register file.

DEFER (IPC2)
Asserted when the current instruction in the file is a GRP3 indirect instruction. This will set the PAUSE 2 flip-flop, causing the IPF to wait 2 memory cycles while the 15 gets the indirect address and operand from memory.

DONE (IPC2)
When asserted, indicates that the memory request to the Port has finished.

ENB (IPC1)
A flip-flop which indicates that the IPF has been enabled and that subsequent IPF accesses will be honored.

EQUAL (IPCM)
Indicates that the 15 address and the WPC are equal. Therefore, the IPF is presently fetching the instruction from memory. It is used to generate WAIT.

FULL (IPC2)
This signal indicates that the file has been filled. Further memory requests will be inhibited until the 15 makes an IPF access.

GRP 3 H (IPC2)
This signal is true if the file output is decoded as a JMP, JMS, CAL, or any operand read instruction. It will cause either PAUSE 1 or 2 to be set at the end of the current reference.

GRP 3 L (IPC2)
Indicates that the instruction being read out of the file is a DAC or DZM indirect, or a GRP 3 H. It causes the IPF to pause one memory cycle.

HALT (IPC2)
This flip-flop indicates that the instruction currently being read out of the file breaks program sequence. HALT will cause an abort sequence to be initiated.

IN (IPCM)
Indicates that the 15 address is within the limits of the WPC and RPC. Therefore, the file contains the requested data.

IN ENB (IPC1)
IN is true and the IPF is ENBabled.

INC RPC (IPC2)
This signal down-counts the FULL counter and generates an RD CLK.

INC WPC (IPC2)
This signal up-counts the WPC when the IPF begins its memory reference. This is not allowed when the WPC is at a 4K boundary, when register file is FULL, or when the IPF is pausing.

INIT INC (IPC1)
Increments the RPC following a START, enables INC WPC and sets the ENB flip-flop during the start sequence so that subsequent IPF requests will be enabled.

INT A XX, INT B XX (IPEP)
These are address bits at the output of the interleaving selection switches. INT A XX are IPF address bits. INT B XX are external processor address bits (i.e., PDP-11).

IPF CYC 1, 2 (IPAM)
Indicates that the Memory Port (1, 2) has selected the IPF for the next memory reference. In the IPF, it enables the appropriate memory address lines and selects the address MUX to drive the IPF address.

IPF MSYNC (IPC2)
Asserted when BUSY is set. It is sent to the Port to request data from memory.

IPF WAIT (IPC1)
This signal is generated by any abort and ensures that the Bus Interface module holds off new requests so that the IPF may sync on the new 15 address.

JMP & JMS & CAL (IPC2)
This signal is asserted when the output of the file bits 0, 1, 2, 3 are decoded as a 60, 10, or 00. It is the enable for setting the ALT flip-flop, which causes an abort. It also generates GRP 3 H, which prevents further IPF memory requests.

LD (1) L (IPC2)
This signal is generated during an IPF memory cycle and loads the resultant data into the register file.

LD L (IPC1)
Generated during the start-up sequence, it sets INC ENB following the loading of CPC, WPC and RPC.

LESS (IPPC)
See MORE.

LOWER OK (IPEP)
Indicates that the current external processor address bus has not exceeded the lower limit of the selected address window.

LSB (IPPC)
This flip-flop is used to select Port 1 or Port 2. If set, Port 2 will be selected; if clear, Port 1 will be selected. It is initially loaded with the contents of 15 Addr bit 17, and complemented at the end on subsequent IPF memory accesses.

MISS (IPC1)
Indicates that the current requested instruction is not contained in the register file.

MORE, LESS (IPPC)
These are outputs of the CCMP which, along with the RCMP and the WCMP, generate the signals ABOVE, BELOW, and EQUAL.

PAUSE 1, 2 (IPC2)
Two flip-flops, which when set, cause the IPF to wait 1 or 2 memory cycles.

1. LAC - set PAUSE 1
   Wait 1 memory cycle MEM AC

2. LAC indirect - set PAUSE 2
   Wait 2 memory cycles.

PORT 1, 2 SEL (IPPC)
Selects the appropriate Memory Port by examining the incoming 15 address.

PORT 1, 2, 11 CYC (IPAM)
Indicates that the Memory Port (1, 2) has selected the external processor for the next memory reference. In the IPF, it enables the appropriate memory address lines and selects the address MUX to drive the external processor address.

RCMP (IPCM)
The RCMP compares the contents of bits 6–17 of the 15 address with bits 6–17 of the RPC and is used with WCMP to determine if the current access is in the file.

REQ (IPC1)
A flip-flop which indicates that instruction pre-fetch (IPF) has been asserted by the bus interface and Master Sync (MSYNC) has been generated.

The 15 is requesting an instruction.

RD CLK (IPC2)
This signal is asserted when the RPC is to be loaded with the 15 address lines.

It also occurs when the RPC is incremented.

RPC (IPPC)
The Read Program Counter is a 12-bit register, loaded from 15 address lines 6–17, and indicates the lower boundary of the current contents of the register file.

START (IPC1)
A flip-flop that initiates the IPF start-up sequence. This may be the result of an abort or the first start-up following the enable IPF IOT.

STOP (IPC2)
Generated following the last increment of the RPC to clear the UP flip-flop.

UC (IPC2)
When set, this flip-flop indicates that a request to memory has started, and at this time, an up-count may be performed on the FULL counter.

UP (IPC2)
Enables incrementing the RPC following the reading of an instruction from the IPF register file.

UPPER OK (IPEP)
Indicates that the current external processor address has not exceeded the upper limit of the selected address window.

WAIT (IPCM)
A flip-flop, which when set, delays setting 15 SSYNC whenever the current instruction is being retrieved from memory but is not yet loaded in the register file.

WCAR (IPPC)
This is the WPC carry bit and is used to generate 4K L.

WCMP (IPCM)
The WCMP compares the contents of bits 6–17 of the 15 address with bits 6–17 of the WPC, and is used with RCMP to determine if the current access is in the file.

WPC (IPPC)
The Write Program Counter is a 12-bit register, loaded from the 15 address lines. Bits 16, 17 are used to indicate which word in the file is being written. Bits 6–17, along with Bits 0–5 of the CPC, are sent to the Port to address memory.

WRT CK H (IPC1)
A signal which indicates that a request has been made by the 15, but it is a write request. If the requested address is in the file, an abort sequence will be executed.

WRT CLK (IPC2)
This signal is asserted when the WPC is loaded with the 15 address lines or when the WPC is incremented.

4 K L (IPC1)
As long as this signal is low, the current address in the WPC is at the 4K boundary. It prevents further memory references.

4 BITS EQ (IPCM)
When true, this signal terminates the INC RPC pulses when the RPC is one greater than the current 15 address. This ensures that the proper lower boundary is contained in the RPC.

11 ADD XX (IPAM)
These are external processor address bits, after they have been relocated by the lower boundary adder and/or the address FLOAT jumpers.

11 PORT, 1, 2 SEL (IPEP)
Selects the appropriate Memory Port by examining the incoming external processor address.

11A, 11B, SEL A, SEL B (IPAM)
The selects and strobes for the IPF address MUXs. SEL A enables addresses to memory Bus 1; SELB enables addresses to memory Bus 2. When true, 11A and 11B select the external processor address to be driven to the appropriate memory. When false, the IPF address is driven to memory.

BR 00–09 (MMBR)
This is the contents of the boundary register and is used to determine the limit of the user's core space.

DEFER (MMC1)
Used to enable traps during protect mode, when indirect references violate the user's boundary.

GM0, 1 (MMC1)
These two bits of the MM register select the address width to be used while in User Mode. The selection will also determine the virtual position of the SHARE ADDRESS space.

G MODE (MMC1)
This mode allows program selection of the address width through the Memory Management module. The selection is accomplished by loading GM0 GM1 in the MM register with the appropriate width code. Further, the Memory Management must be in the User Mode. The G MODE signal is also driven to the CPU to control the contents of the upper defer address bits.

I BUS 00–17 (MMII)
These information bits allow selected control and data to be displayed on the 15 console.

INT & API ST (MMC2)
A signal from the processor which indicates that an interrupt, trap, or API break is about to occur.

IOB 00–17 (MMII)
The 15 I/O Bus provides 18 bits of data for loading and reading various data and control registers in the MEM MGR module.

IOT ENB (MMC1)
This bit of the MM register will permit execution of IOTs, while in User Mode, if set.

KM CRY (MMBR)
This is the carry bit which indicates that the address is outside the user's address space. It is used only in Protect Mode and will cause a trap. (See KT CRY.)

KT CRY (MMBR)
This is the carry bit which indicates that the address is outside the user's address space. It is used only in Relocate Mode and will cause a trap. (See KM CRY.)

LDMM (MMIO)
This is an IOT decode which will load the 18 bits of MM register from the IOB.

NEXM (MMC2)
This flip-flop is set whenever the nonexistent memory comparators indicate that the address referenced does not exist, or when the share or relocation address overflows to a nonexistent address. When set, this flip-flop causes a trap.

P MODE (MMC1) (See R MODE)
This is one of two basic modes that the Memory Management performs. In this mode, the boundary register is used to divide memory into two working areas. The lower area is protected from the upper area through the use of TRAPs. Relocation does not occur.

PRE (MMC1)
The PRE flip-flop sets the Memory Management in a condition to enter User Mode on the next instruction executed.

FETCH (MMC3)
A signal from the processor which indicates that the processor is entering the instruction fetch cycle.

RA 00–09 (MMBR)
Relocated address – the address produced by normal relocation mode.

R DIS (MMC1)
This bit in the MM register disables relocation and protect functions. This allows the use of G MODE, which requires User Mode, without enabling the other User Mode functions.

REL (MMAR)
This signal enables the three possible types of relocated address:

Share address
Relocate address
The contents of the Relocation register

R MODE (MMC1) (See P MODE)
This is one of two basic modes that the Memory Management performs. In this mode, the Relocation register contains the base address of the user's address space. The Boundary register contains the upper limit of the user's address space. When this mode is accompanied by User Mode, the user's address will be relocated and TRAP will be enabled.

RST UM (MMC1)
Restore User Mode – this is an IOT decode which causes Memory Management to immediately enter User Mode.

SA 00–09 (MMSM)
Share Address – the relocated address produced by Share Mode references.

SEL A, SEL B (MMSM)
These selection signals determine which of four addresses are driven to the Memory Ports. The selected address becomes 15 ADD 00–09. The four possible addresses are SA, RR, RA, or ADD, all of which contain bits 00–09.

SH (MMC1)
This bit of the MM register enables share addressing.

SHARE (MMC1)
This is an enable for the share address decodes and relocation.

SL ENB (MMAR)
Segment Length – this enable determines the upper limit of the shared address space. When the limit is reached, the enable will be false.

SLR 0, 1 (MMC1)
These two bits of the MM register select the length of the shared segment.

STB XCT (MMC3)
Strobe Execute – this signal clocks the execute flip-flops in order to detect illegal XCT or XCT instructions.

TRAP (MMC2)
This flip-flop sets when any one of several illegal events occurs:

A nonexistent memory reference.
An attempt to execute a privileged instruction.
An address space violation.
An attempt to write in a write-protected location.

TRAP P (MMC2)
This is a clear pulse sent to the Bus Interface whenever a write trap or nonexistent memory reference occurs.

UM (MMC1)
When the MEM MGR is in the User Mode, relocation and protection are normally in effect. It has an enabling effect on G-, R-, and P-Modes. User Mode is entered by the execution of an IOT and is exited as a result of an interrupt TRAP or CAL.

WRT P (MMC1)
This bit of the MM register enables write protection of the External Shared Address Space.

WRT TRAP (MMC2)
This signal causes a trap when a reference attempts to write into a write-protected shared address.

24K, 56K, 120K, 248K, >400 (MMAR)
These are address decodes which determine whether the requested address is in the shared address space.

1701, 1702, 1704, 1741, 1742, 1744, 1724, 0022, 0024 (MMIO)

1701 - SKP PV IOT; skip if protect violation.
1702 - CLR PV IOT; clear protect violation flag.
1704 - LD BR IOT; load boundary register.
1741 - SKP NEXM IOT; skip on nonexistent memory.
1742 - MPEU IOT; enter User Mode.
1744 - CLR NEXM IOT; clear NEXM flag.
1724 - LD RR IOT; load Relocation register
0022 - RD MM IOT; read Memory Management register.
0024 - LD MM IOT; load Memory Management register.

M7176

ABORT CLR (APIC)
This signal, when driven by the API module, causes the IPF module to be inhibited. The state of the signal is controlled by the IPF IOT, 701724, which causes ABORT CLR to assume the state of the CPU's AC bit 17; that is, AC 17 on a one (true) will cause ABORT CLR to be true.

API CAL (APIC)
This signal is generated by the CPU and is used to set PL 04 whenever API is enabled and a CAL instruction is executed. This will disable software requests of a lower priority until the PL04 level is released.

API I/O A 12-17 (BAPI)
These are I/O address bits generated by the API module. Each of 10 possible conditions generates a unique API I/O address and is driven to the I/O Bus address lines. The conditions are: Test Requests 0-7, PF API RQ, and RTC API RQ.

API 0–3 EN (XM15 BS)
These enable signals, one of four in the API system, are dc levels originating in the I/O Processor; they are daisy-chained from device to device on the same level. The M104 logic in each controller can interrupt these levels, cutting the level off to all devices that follow it on the bus. A device receives a level as API X EN IN H and transmits it as API X EN OUT H.

API 0–3 GR (APIR)
One of four possible signals issued by the API module, indicating that it grants the API request at the corresponding level.

API 0–3 RQ (IOBR)
One of four API request signals on channels 0–3. A request is set by the device at I/O Sync time. It is received by the API module and initiates the API sequence.

API SKIP REQUEST – See SPI

API STROBE (APIC)
This strobe, generated by T4 and API SYNC, strobes the current state of the request flip-flops into the priority level flip-flops. This action is conditioned by the priority level enables so that only priority levels above the highest current level will be set.

CLK 00–17 (CLKM)
This is the Task Accounting Clock register outputs which may be read by IOT, RD CLK, 701712.

CLK (1) H (CLKM)
This is the buffered output of a 1 MHz free-running oscillator which is divided by 10, yielding an output frequency of 100 KHz. At this frequency, the CLK register capacity is 2.62 seconds.

CLR CLK (CLKM)
This pulse clears the Task Accounting Clock register immediately following RD CLK IOT.

DBK – See DBR (PL03)

DBR (PL03)
This signal is IOT-decoded and driven by the CPU, which in the API module, causes the highest priority level flip-flop currently set to clear, thus enabling the next highest priority level to be serviced. DBK performs the same function.

DIS BRK (TR0)
This flip-flop is set by an IOT DBI (705522) and cleared by EBI (705521). It is used to temporarily disable all requests for API breaks to the CPU. It does not, however, prevent receipt of new requests by the API module.

DS0–5 (IOBR)
These are six device select lines. These signals are decoded by the device select logic in the controller, which responds to its unique code only.

I/O BUS 00–17 (IOBR)
These are the 18 data bits of the I/O Bus which are received and used by the API module to test for various conditions within the API circuits. These bits are driven whenever the IOT RPL or RD CLK is received by the module.

ISA (APIC)
This IOT, Initiate Selected Activities, is used to load the API ENB, TRQ00–03, API RQ04–07, and PL 00–07 flip-flops from the CPU's AC.

PF API RQ A, B. - See RTC API RQ A, B (TR0)

PL 00–07 EN (PL03, PL47)
When true, these signals indicate that their associated priority level flip-flops and any higher level flip-flop are not set. The enables are used along with their corresponding request flip-flop to set the corresponding priority level flip-flop at API strobe time.

RD CLK - See CLK 00–17 and CLR CLK (APIC)

RPL (APIC)
This IOT, Read the Priority Levels, causes the current state of the API enable flip-flop, API 00–07 RQs and PL 00–07 to be driven to the I/O Bus, and then to be loaded in the CPU's AC.

RTC API RQ A, B (TR0)
These flip-flops will post an API request for a power fail or real time clock flag condition. Power fail will cause API level 00 request. An RTC FLG will cause API level 03 request. The B flip-flop of each pair is used to generate the appropriate API I/O address.

RQ 00–07 (APIR)
These flip-flops store the pending API requests at T4 whenever API is enabled. This is the first step in processing any API break.

RQ SYNC 00–07 (PL03, PL47)
These levels indicate that an API request has been received and is in process of causing an API break. Any RQ SYNC will generate CP API RQ when API is enabled.

SPI (APIC)
This is the IOT Skip on Priorities Inactive. If all eight priority levels are enabled (inactive) this IOT will cause the CPU to skip the next instruction by generating API SKIP REQUEST.

TIME 03, 04 (APIC)
These two time signals originate in the I/O Processor and are used to synchronize API requests on the I/O Bus with the request arbitration circuitry of the API module.

APPENDIX B
MULTI-LAYER BOARD TECHNIQUES

B.1 GENERAL

The XM15 modules are multi-layer etched circuit boards. The four layers consist of one power and one ground internal plane and two external signal layers (Figure B-1).

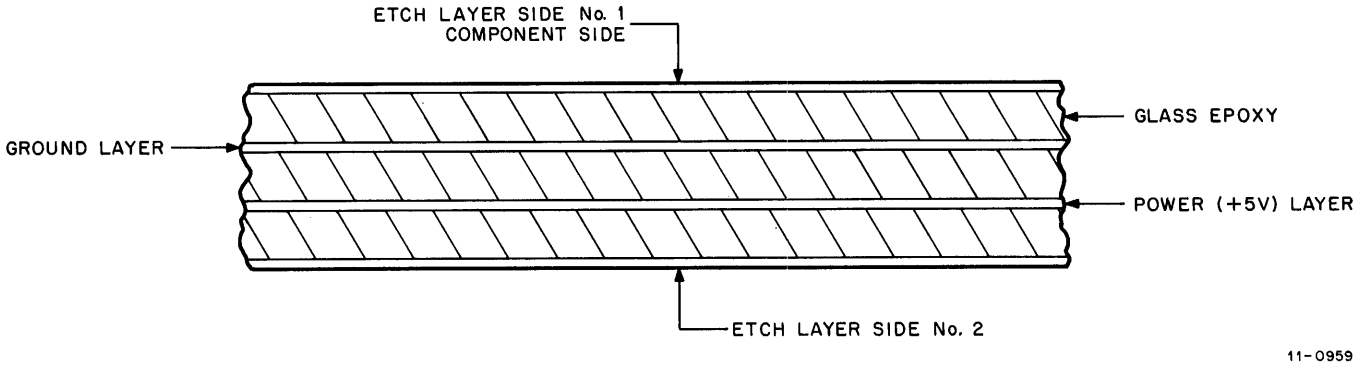


Figure B-1 Cross Section of Multilayer Board

B.2 IC CONNECTIONS

On each module, which uses a DEC standard inner layer, three types of plated-through holes are made in the board.

1. A feed-through hole which makes no connections to V_{CC} ground inner layers and only connects the outer signal surfaces.

2. A plated-through hole which connects both signal surfaces to the ground inner layer and does not contact the V_{CC} inner layer.

3. A plated-through hole which connects both signal surfaces inner layer and does not contact the ground to the V_{CC} inner layer. See Figure B-2 for examples.

B.3 IC AND COMPONENT REMOVAL AND REPLACEMENT

Because the etch is small and plated-through holes are delicate, extra care should be taken during the maintenance and repair of the multi-layer modules, expecially when soldering and unsoldering components. Certain tools, listed in Table B-1, (or their equivalent) are recommended for use during removal and replacement of ICs on the multi-layer modules. The manufacturer and type or part number of each tool is indicated in parentheses at its first occurrence in the procedure.

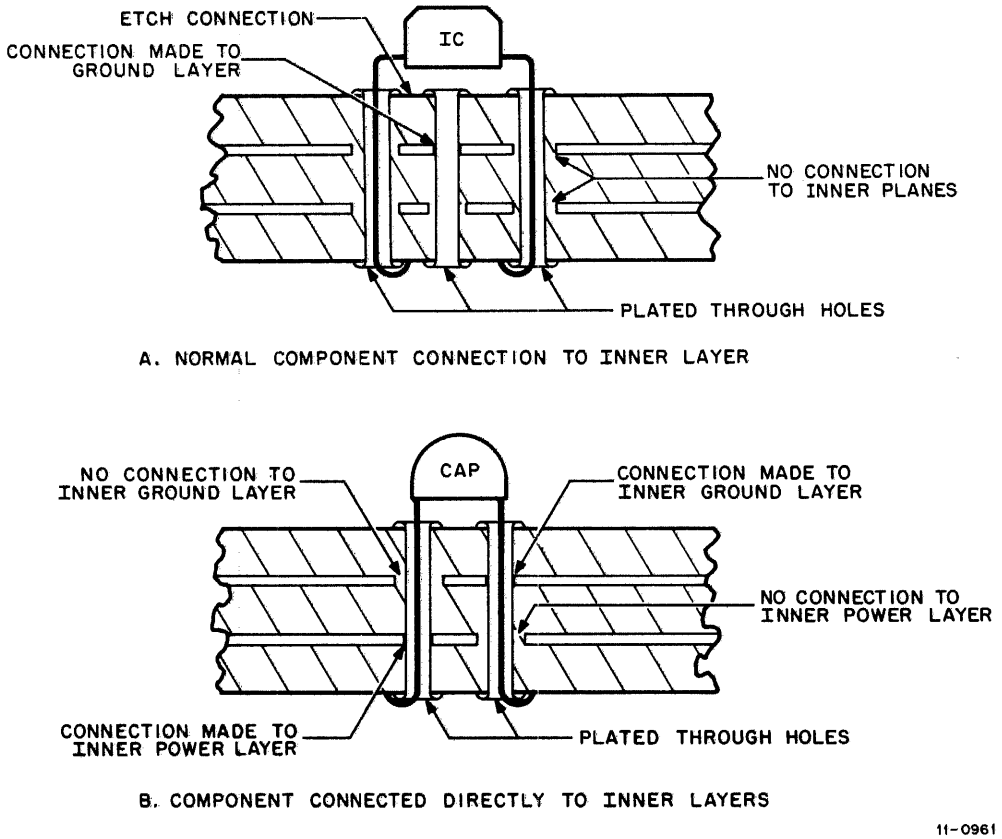


Figure B-2 Component Connections to Inner Layers

Table B-1
Repair Tools Required

Equipment or Tool	Manufacturer	Model, Type or Part No.	DEC Part No.
Diagonal Cutters	Utica	47-4	29-13460
Diagonal Cutters	Utica	466-4 (modified)	29-12551
Miniature Needle Nose Pliers	Utica	23-4-½	29-13462
Solder Extractor	Solder Pullit	Standard	29-13451
Soldering Iron (30 W)	Paragon	615	29-13452
Soldering Iron Tip	Paragon	605	29-19333
16-pin IC Clip	AP Incorporated	AP923700	29-10246
24-pin IC Clip	AP Incorporated	AP923714	29-19556

B.3.1 Removal and Replacement of Plastic Case ICs

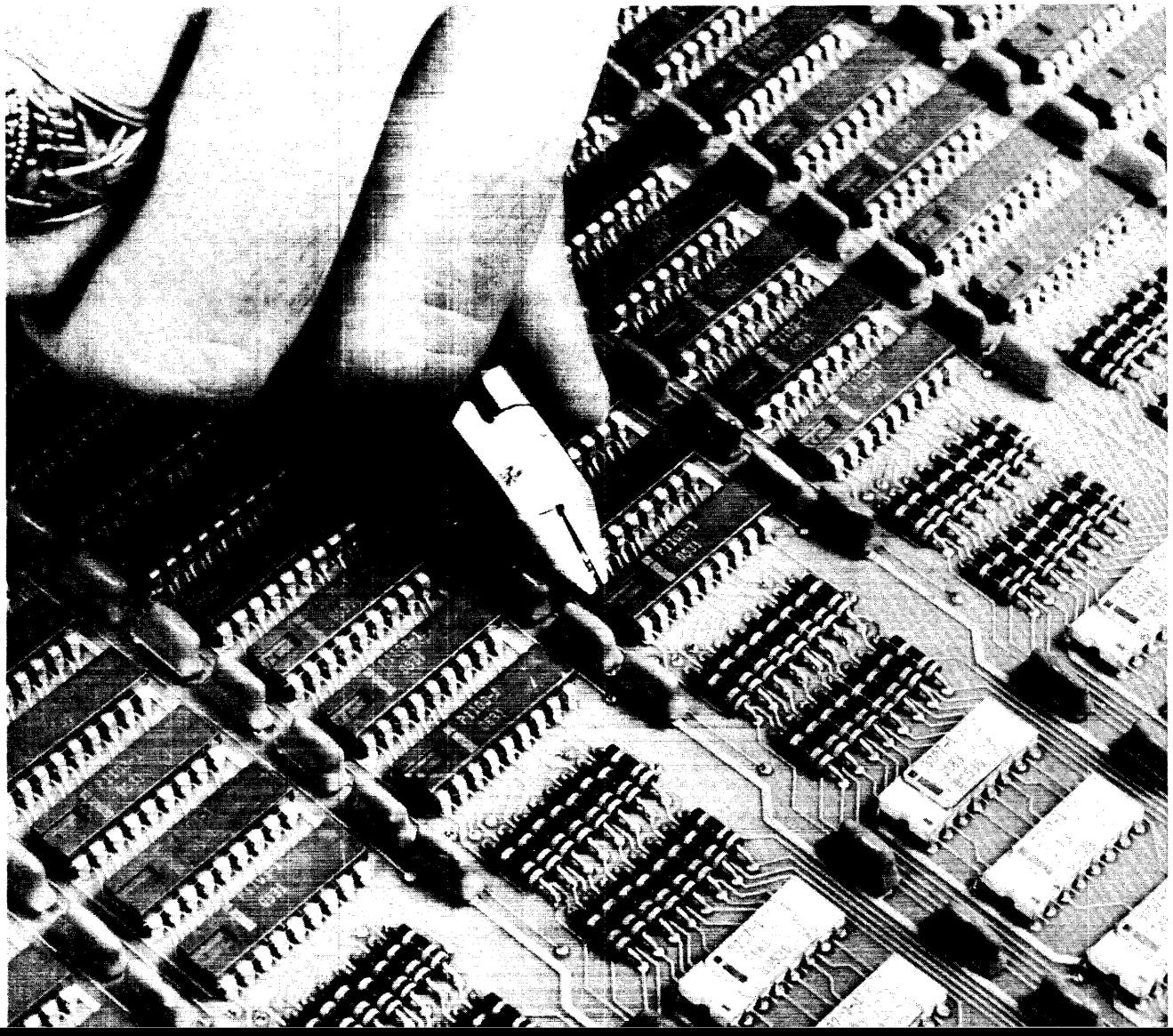
To remove and replace a plastic case IC and to prevent damage to the multi-layer board, the following procedure should be strictly adhered to.

To remove and replace plastic case ICs, proceed as follows:

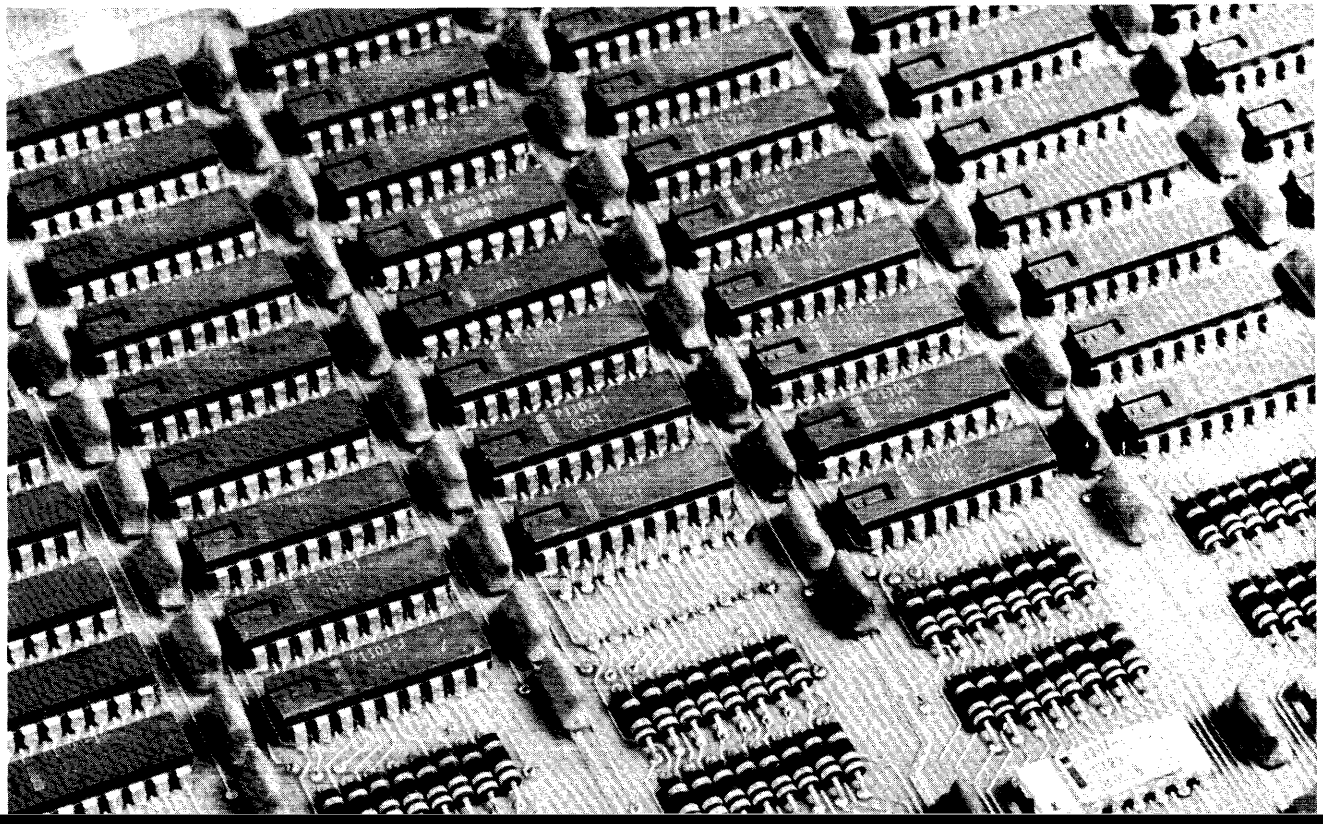
1. Figure B-3 shows the module to be repaired and the required tools. The sample module is a G401 MOS Memory Matrix module (not used in the XM15, but it is used here to illustrate the principles which apply).

Figure B-3 Module to be repaired and Tools Required

2. Figure B-4 shows leads of the defective IC being clipped, using small diagonal cutters (Utica, Part No. 47-4).



3. Figure B-5 shows the IC location after the IC has been removed, with the IC leads still in the board. Locate the IC leads just removed on the soldered (back) side of the board; cut all leads to avoid difficultY during the removal.



4. Figure B-6 shows the IC leads being removed from side 1 of the board. Apply heat to the lead with the soldering iron (Paragon, Part No. 615) until the lead becomes loose. Then, remove the lead with pliers (Utica, Part No. 23-4).

CAUTION

Leads that are connected to an inner layer require more heat because much of the heat is absorbed by the inner layer. It is helpful to add solder to the lead first, which causes more heat to be conducted to the solder in the eyelet around the lead.

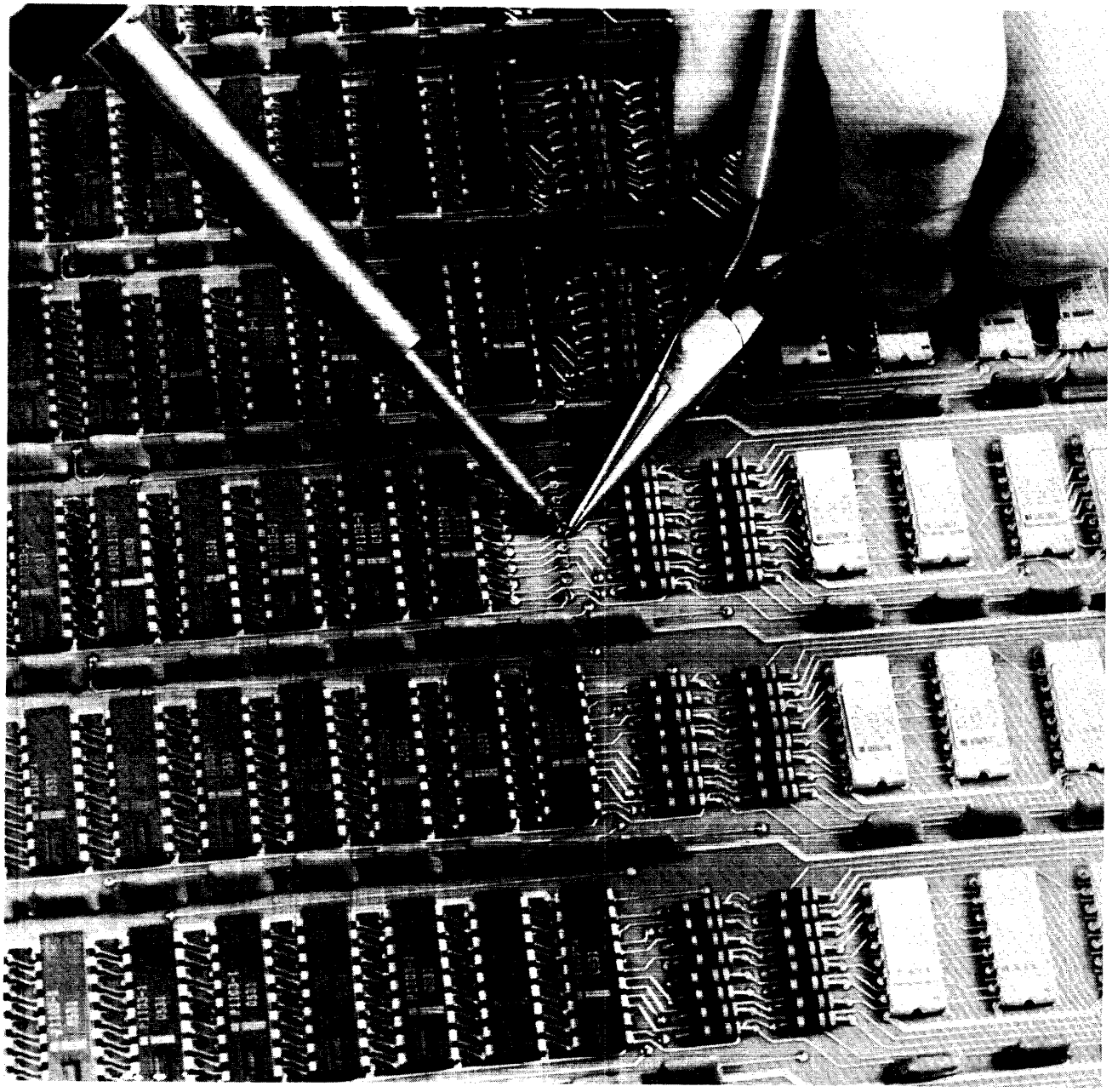
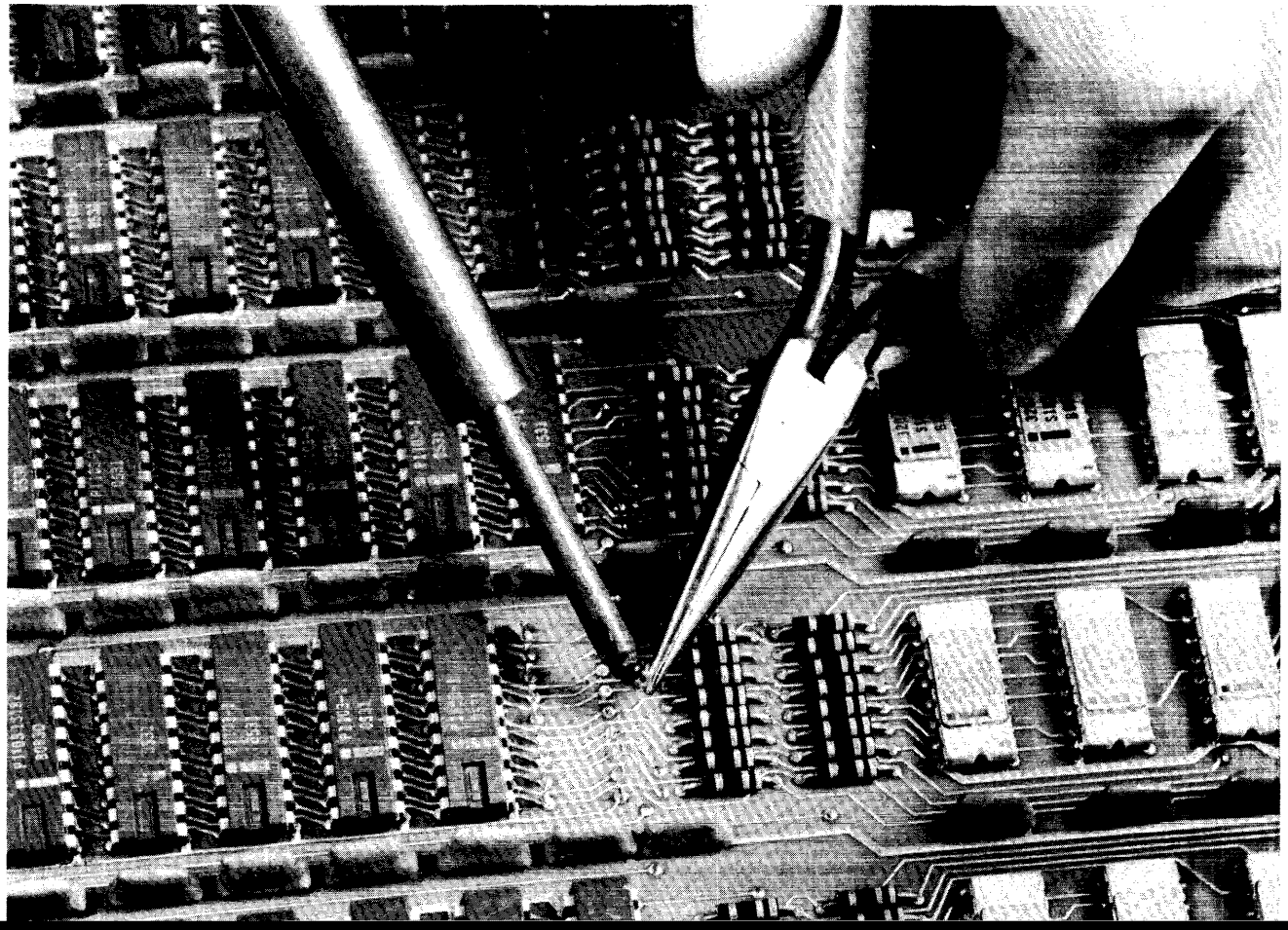
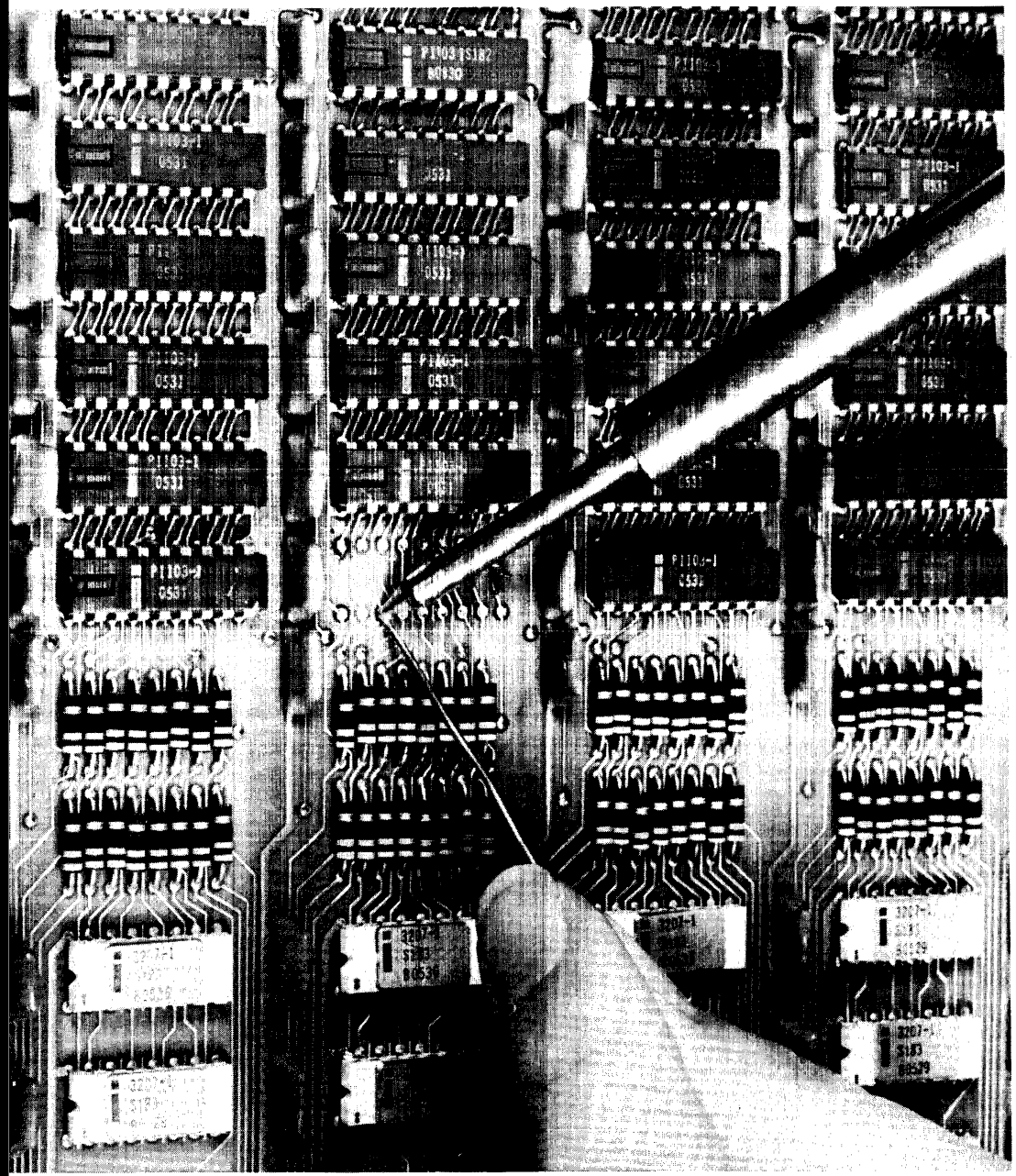


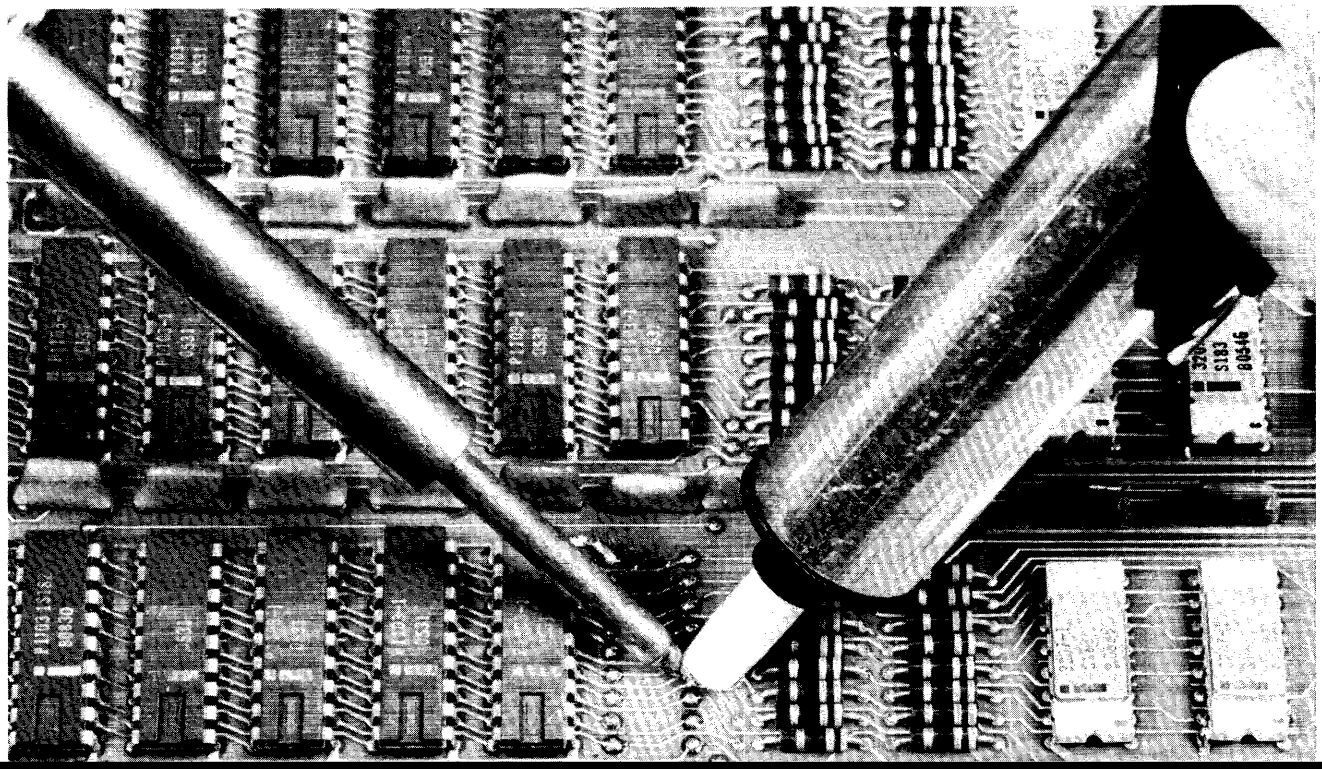
Figure B-6 removing IC Leads

5. Figure B-7 shows a lead immediately after removal from the eyelet. After all of the IC leads have been removed, carefully apply a small amount of solder to each of the eyelets (Figure B-8). The extra solder distributes heat evenly and makes Step 6 (cleaning the holes) easier and more effective.





6. Once the eyelets have been refilled with solder, (Step 5), remove the solder using the soldering iron and solder extractor, as shown in Figure B-9. In Figure B-9, the eyelet has no connection to the board inner layers; the solder can be extracted from the same side of the module to which the heat is applied. However, in cases where direct connections to the inner layer are made, heat must be applied to one side of the module and the solder must be extracted from the opposite side, due to the heat sinking properties of the inner layers. In this case, the module should be in a vertical position to allow access to both sides of the module simultaneously.



7. Figure B-10 shows the IC location after all of the eyelets have been cleared of solder. Inspect the eyelets to ensure that no excess solder remains. If all of the solder is not removed, refill the hole as described in Step 5 and again remove the solder as described in Step 6. Carefully continue this procedure, as required, until all of the eyelets are cleared of excess solder.

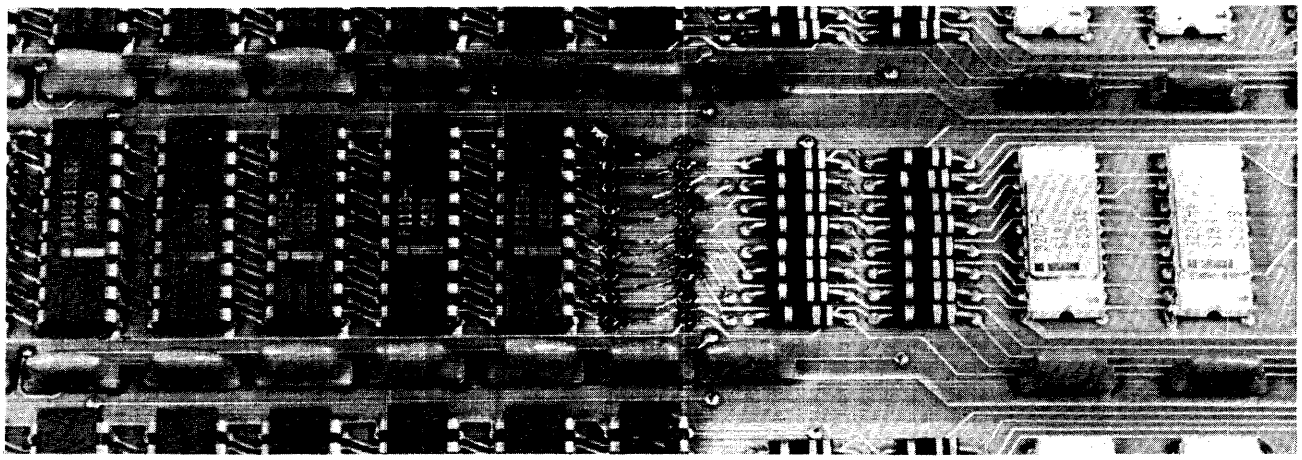


Figure B-10 IC Location Ready for Insertion of New IC

8. Use a cleaning solvent and a brush to clean the IC location of any excess solder flux.

9. Thoroughly inspect the IC location and the surrounding areas for solder splash and damage to etch lines and plated-through holes.

10. Ensure that none of the leads on the replacement IC are bent; insert the replacement IC in the holes. Avoid bending the leads on side 2 of the module to make any future removal of the ICs easier.

CAUTION

If the leads must be bent to hold the IC in position for soldering, avoid bending the leads more than 45 degrees, using only one lead at each end and on opposite sides of the IC.

11. Solder the new IC from side 2 of the module. Use enough solder to fill the holes and make a good connection. Avoid using an excess of solder to prevent an overflow on the top side of the board, which could cause a short under the body of the IC.

12. Once all of the solder connections are made, clean and inspect the area for any damage. Take the necessary corrective action for any defects that are found.

CAUTION

After installing an ECO, or replacing a faulty IC on a module, ensure that no short circuit exists between the power and ground of the module. Do this before replacing the module in the equipment.

APPENDIX C
IC DESCRIPTIONS

C.1 INTRODUCTION

This appendix describes unusual Intergrated Circuits (IC) which are used in the XVM System. The descriptions are supported by circuit diagrams and, in most cases, truth tables. The following types of IC are covered:

Type No.	Description
8097	Hex Buffers
8234	Digital Multiplexer
8266	Digital Multiplexer
8641	Quad Bus Transceiver
7483A	Full Adder
74123	Multivibrator
74S85	Magnitude Comparators
74S153	Data Line Selector/Multiplexer
74S157	Quadruple Multiplexer
74161	Binary Counter
74170	Register File
74S174	Hex D-Type Flip-Flops
74S175	Quad D-Type Flip-Flops
74193	Binary Counter
74S257	Quadruple Multiplexers

C.2 8097 HEX BUFFERS WITH THREE-STATE OUTPUTS

The 8097 converts standard TTL or DTL outputs to three-state outputs. Each 8097 non-inverting buffer can drive 20 TTL unit loads with a typical propagation delay of 14 ns (not in the high impedance state). The buffers have common enable/disable inputs for each of two groups. Two buffers are controlled by the disable on pin 15 and four buffers are controlled by the disable on pin 1. When disabled, the buffer outputs are in a high impedance state (the outputs will measure approximately 2.5 Vdc). The high impedance state allows several buffers to be connected on a common bus, provided no more than one set is enabled at the same time. Figure C-1 shows the 8097 circuitry.

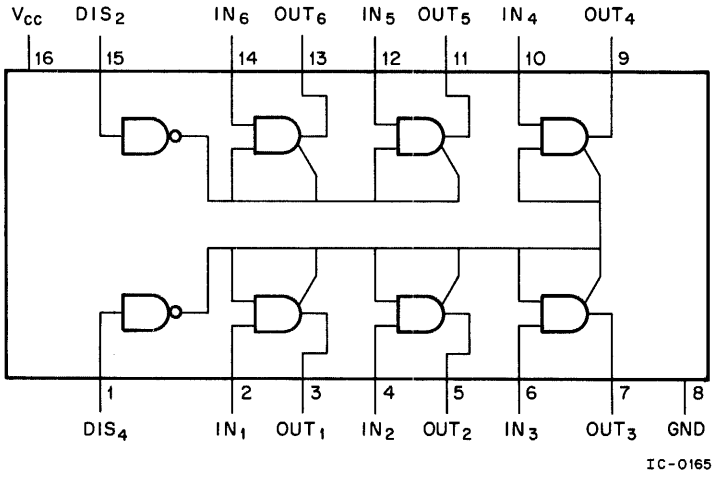
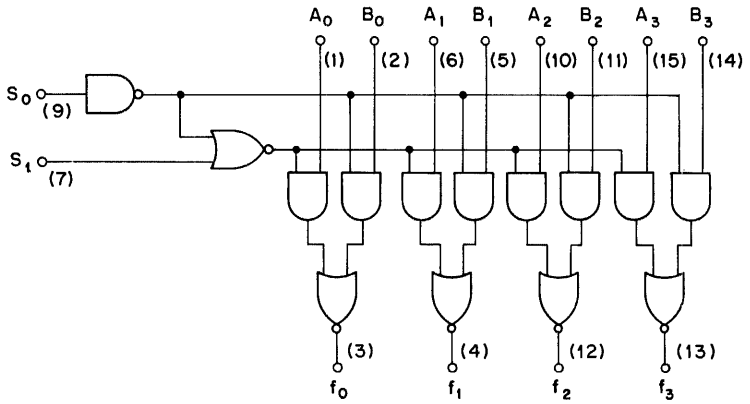


Figure C-1 8097 Hex Buffers

C.3 8234 2-INPUT, 4-BIT DIGITAL MULTIPLEXER

The 8234 IC is designed for general-purpose, data selection applications and features inverting data paths. The design has open-collector outputs which permit direct wiring to other open-collector outputs (collector logic). Figure C-2 shows the 8234 circuitry.



S_0	S_1	f_n
0	0	$\overline{B}$
1	0	$\overline{A}$
0	1	$\overline{B}$
1	1	1

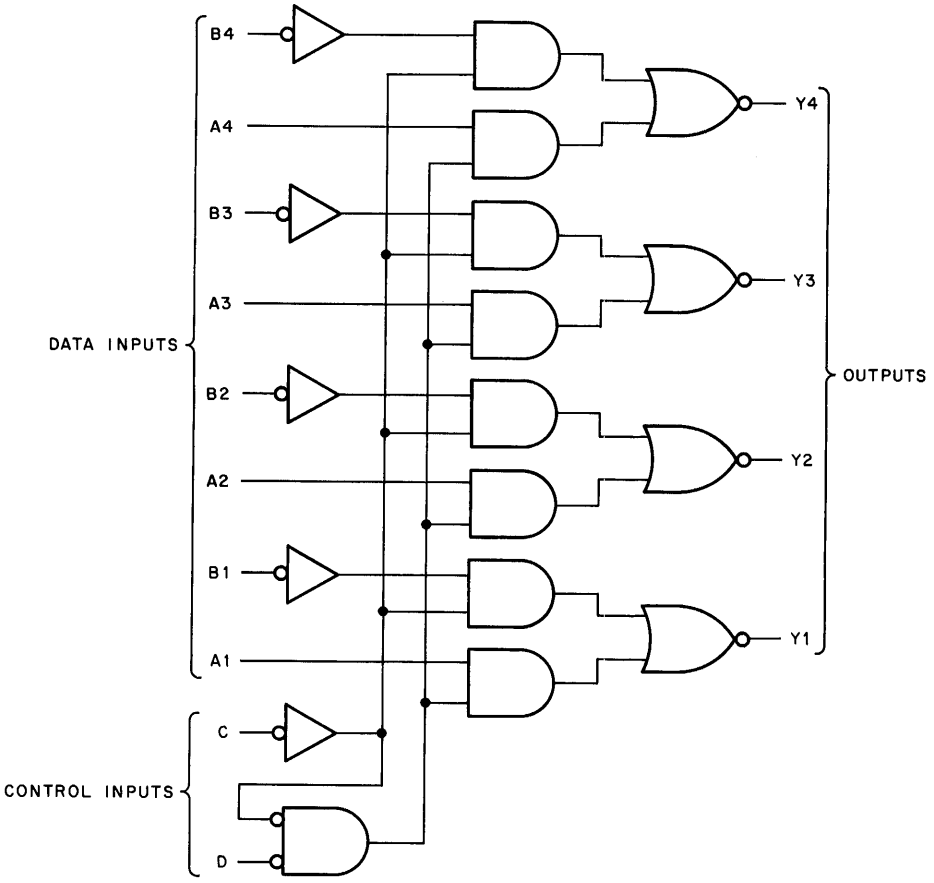
V_{CC} = (16)
GND = (8)
( ) = DENOTES PIN NUMBERS

IC-0154

Figure C-2 8234 Digital Multiplexer

C.4 8266 2-INPUT, 4-BIT MULTIPLEXER

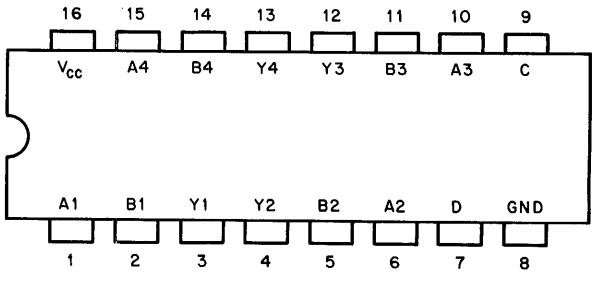
The 8266 has the capability of choosing between two different 4-bit input sources, as controlled by one selection input, while the other input is held to 0. Figure C-3 shows the 8266 circuitry.



LOGIC DIAGRAM

CONTROL INPUT		OUTPUT
C	D	Yn
LOW	LOW	Bn
LOW	HIGH	Bn
HIGH	LOW	$\overline{An}$
HIGH	HIGH	HIGH

TRUTH TABLE



PIN LOCATOR
(TOP VIEW OF IC)

IC-0099

Figure C-3 8266 2-Input 4-Bit Multiplexer

C.5 8641 QUAD BUS TRANSCEIVER

The 8641 consists of four identical receiver/driver combinations in one package. Data on DATA IN 1, e.g., appearing on pin 2 will be driven out of pin 1 (BUS 1) to the bus (if enabled). A BUS 1 signal received from the bus on pin 1 will be fed out of pin 3 (DATA OUT 1) to the equipment. Figure C-4 shows the 8641 circuitry.

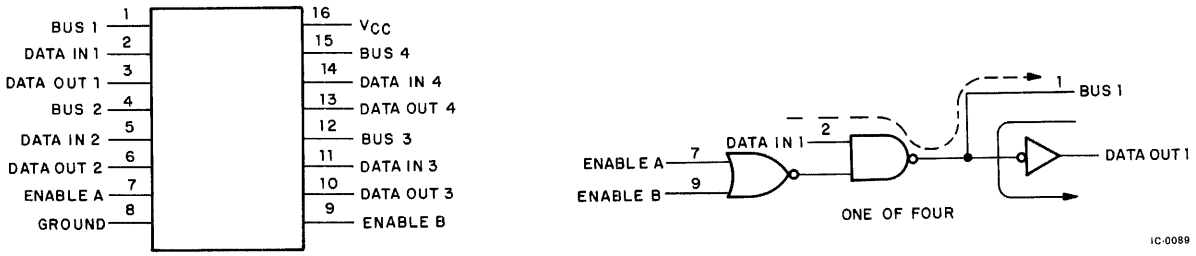
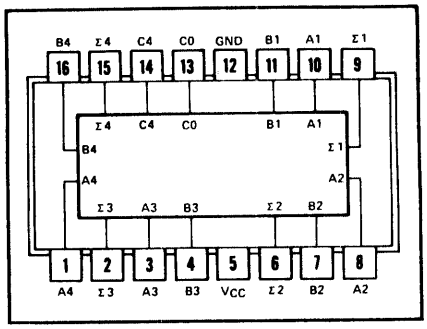


Figure C-4 8641 Quad Bus Transceiver

C.6 7483A 4-BIT FULL ADDER

The 7483A Binary Adder performs the addition of two 4-bit binary numbers and provides for carry IN and carry OUT functions. Figure C-5 shows the 7483A circuitry.



FUNCTION TABLE

INPUT				OUTPUT: WHEN C0 = L				OUTPUT: WHEN C0 = H			
								WHEN C2 = L			WHEN C2 = H
A1 / A2	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4		Σ1 / Σ3	Σ2 / Σ4	C2 / C4	
L	L	L	L	L	L	L		H	L	L	
H	L	L	L	H	L	L		L	H	L	
L	H	L	L	H	L	L		L	H	L	
H	H	L	L	L	H	L		H	H	L	
L	L	H	L	L	H	L		H	H	L	
H	L	H	L	H	H	L		L	L	H	
L	H	H	L	H	H	L		L	L	H	
H	H	H	L	L	L	H		H	L	H	
L	L	L	H	L	H	L		H	H	L	
H	L	L	H	H	H	L		L	L	H	
L	H	L	H	H	H	L		L	L	H	
H	H	L	H	L	L	H		H	L	H	
L	L	H	H	L	L	H		H	L	H	
H	L	H	H	H	L	H		L	H	H	
L	H	H	H	H	L	H		L	H	H	
H	H	H	H	L	H	H		H	H	H	

H = high level, L = low level

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

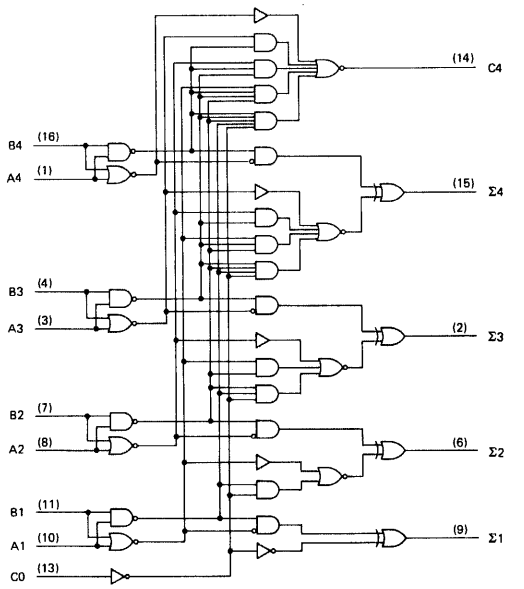


Figure C-5 7483A Full Adder

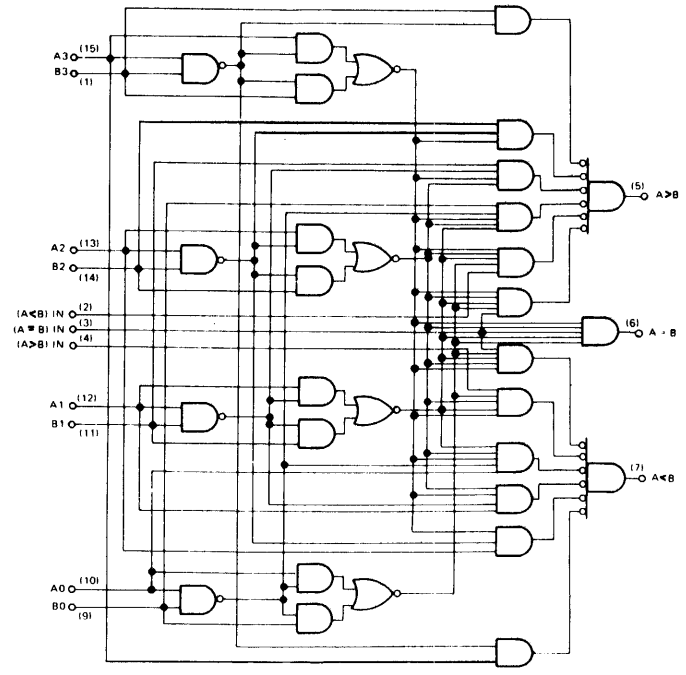
C.7 74S85 4-BIT MAGNITUDE COMPARATORS

The 74S85 performs magnitude comparison of straight binary and straight BCD (8421) codes. Three fully-decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. Figure C-6 shows the 74S85 circuitry.

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = high level, L = low level, X = irrelevant



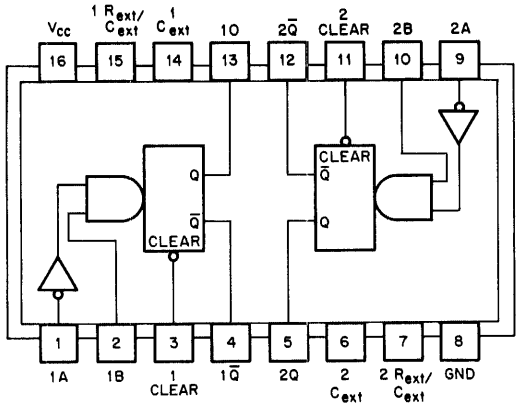
Pin (16) = V_{CC}, Pin (8) = GND

IC-0159

Figure C-6 74S85 Magnitude Comparators

C.8 74123 RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

The 74123 Multivibrator provides dc triggering from gated low level active (A) and high level active (B) inputs. It also provides overriding direct clear inputs and complementary outputs. The retriggering capability simplifies generation of extremely long duration output pulses. If the input is triggered before the output pulse is terminated, the output pulse is extended. An overriding clear feature allows any output pulse to be terminated at a predetermined time, independent of timing components. Figure C-7 shows the 74123 circuitry.



FUNCTIONAL LOGIC / PIN LOCATOR

TRUTH TABLE

INPUTS		OUTPUTS	
A	B	Q	$\bar{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎴
↓	H	⎍	⎴

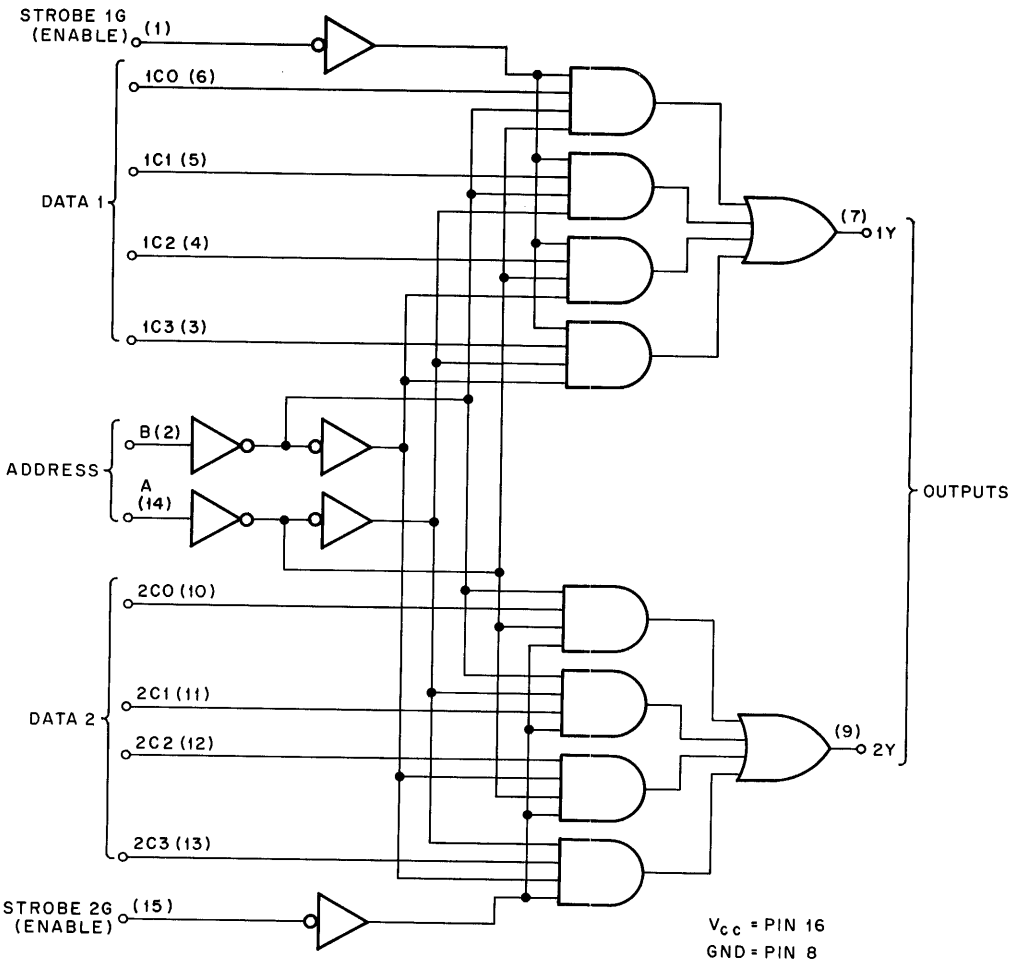
NOTE: H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎴ = one low-level pulse, X = irrelevant (any input, including transitions).

IC-0156

Figure C-7 74123 Retriggerable Monostable Multivibrator with Clear

C.9 74S153 DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

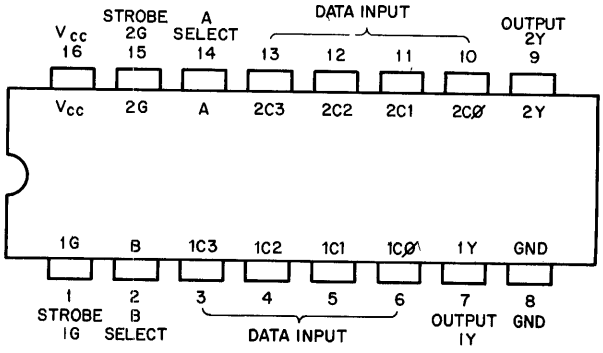
The 74S153 is a multiplexer with separate strobe lines applied to each section. It can be used for data multiplexing, parallel-to-serial conversion, pulse pattern generation, and as a Boolean function generation. Figure C-8 shows the 74S153 circuitry.



LOGIC DIAGRAM

CONTROL INPUT		STROBE	OUTPUT
E	F	G	Y
LOW	LOW	LOW	A
HIGH	LOW	LOW	B
LOW	HIGH	LOW	C
HIGH	HIGH	LOW	D
DON'T CARE		HIGH	LOW

TRUTH TABLE (EACH HALF)



IC-0096

Figure C-8 74S153 Dual 4-Line to 1-Line Data Selector Multiplexer

C.10 74S157 QUADRUPLE 2-LINE TO 1-LINE MULTIPLEXER

The 74S157 multiplexer features buffered inputs and outputs. All outputs are low when disabled (enable high). The truth table and logic diagram are shown below.

INPUTS			OUTPUT Y	OUTPUT W
ENABLE	SELECT	A B	SN54/74157, SN54S/74S157	SN54S/74S158
H	X	X X	L	H
L	L	L X	L	H
L	L	H X	H	L
L	H	X L	L	H
L	H	X H	H	L

H = high level, L = low level, X = irrelevant

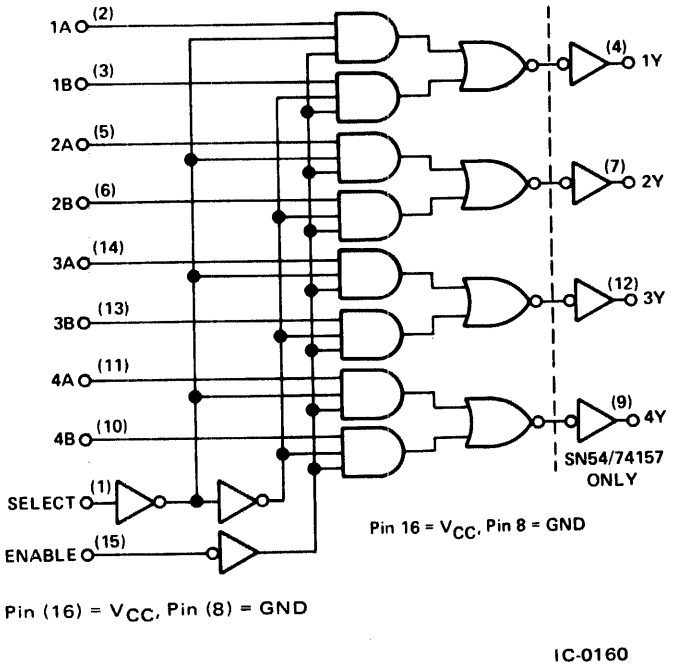


Figure C-9 74S157 Quadruple 2-Line to 1-Line Multiplexer

C.11 74161 4-BIT BINARY COUNTER

The 74161 binary counter has internal look ahead for fast counting and a carry output for n bit cascading. Figure C-10 shows the 74161 circuitry.

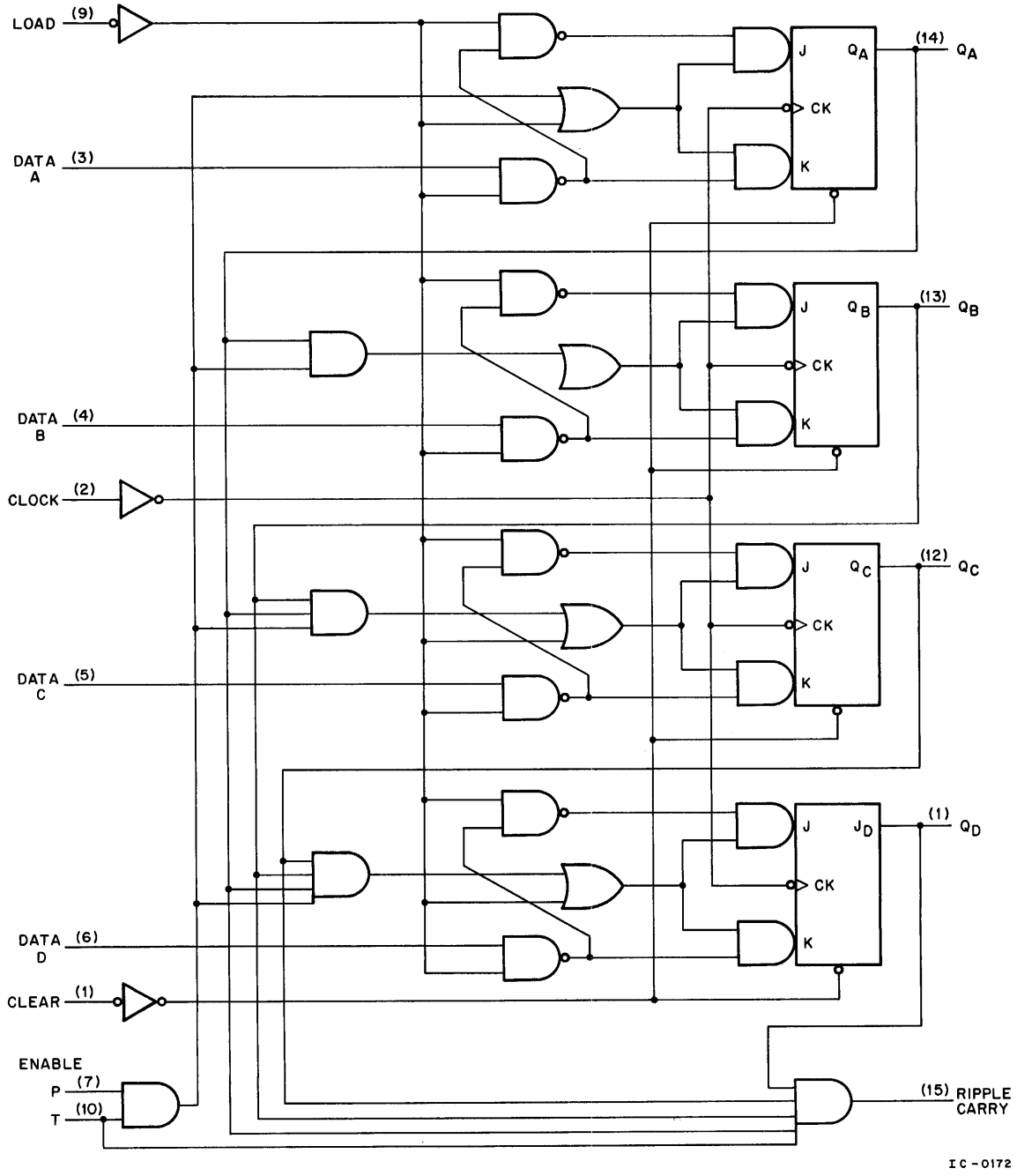


Figure C-10 74161 4-Bit Binary Counter

C.12 74170 4-BY-4 REGISTER FILE

The 74170 file is organized as four words of four bits each and contains separate address decoding for the write in and read out of data. Data is stored in latches, read out is nondestructive and simultaneous reading and writing is permitted, provided that the settling time for new data (25 ns) is observed. Figure C-11 shows the 74170 circuitry.

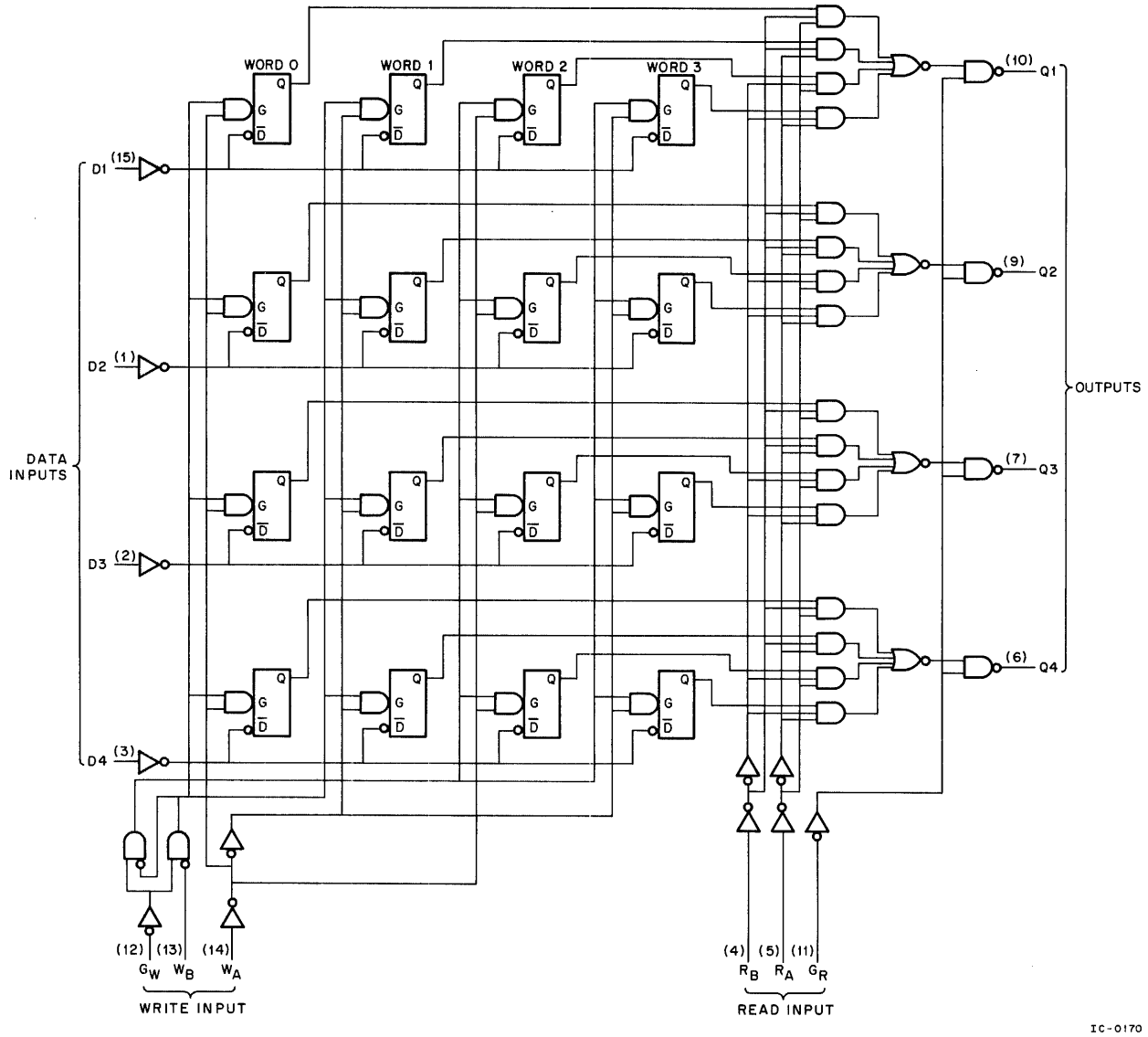


Figure C-11 74170 Four-By-Four Register File

C.13 74S174 HEX D-TYPE FLIP-FLOPS

The 74S174 contains six flip-flops with single outputs. The flip-flops contain direct-clear inputs and buffered clock inputs. Figure C-12 shows the 74S174 circuitry.

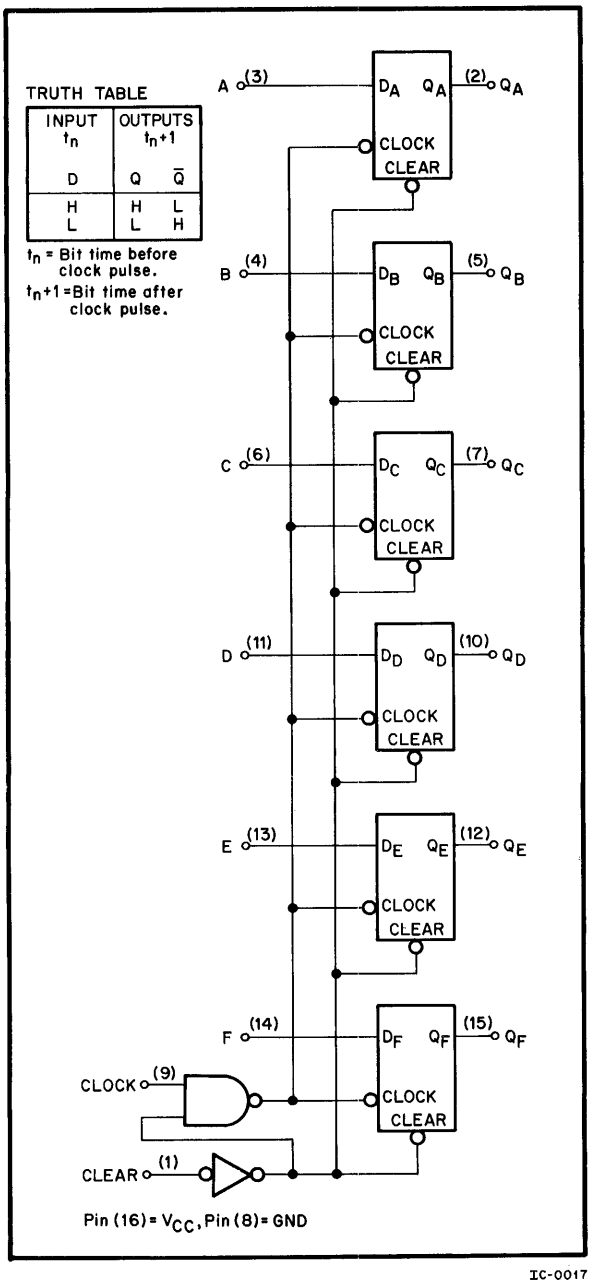


Figure C-12 74S174 Hex D-Type Flip-Flops

C.14 74S175 QUAD D-TYPE FLIP-FLOPS

The 74S175 contains four D-type flip-flops with dual outputs. Each flip-flop has direct-clear and buffered clock inputs. Figure C-13 shows the 74S175 circuitry.

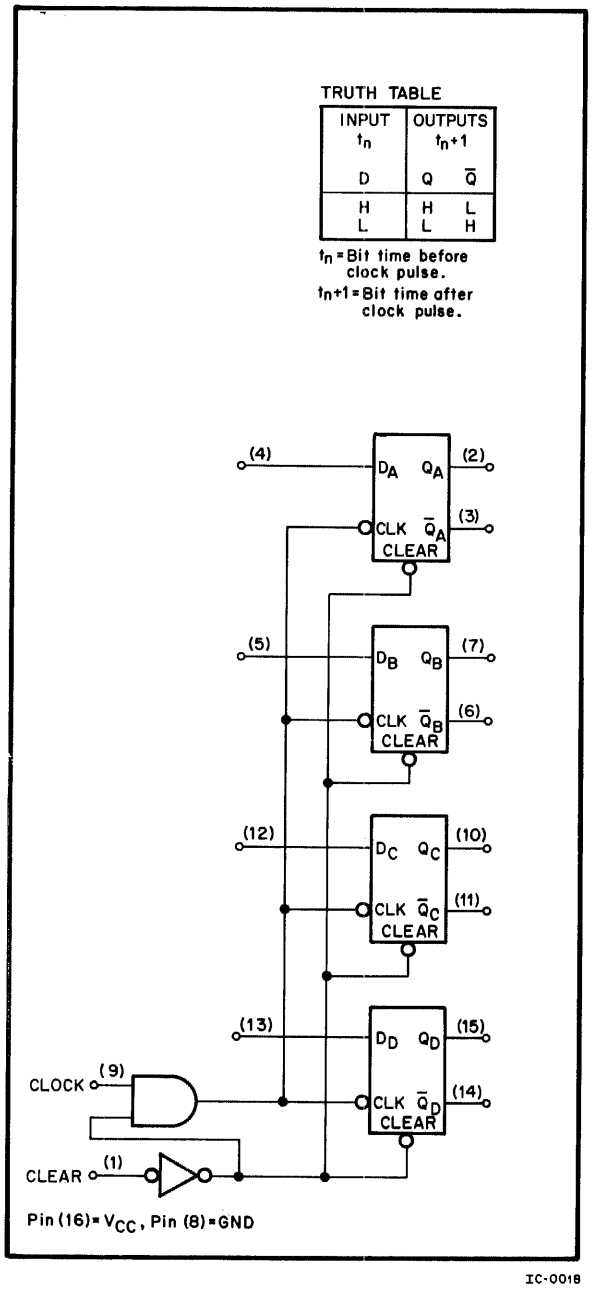


Figure C-13 74S175 Quad D-Type Flip-Flops

C.15 74193 4-BIT BINARY COUNTER

The 74193 binary counter has an individual asynchronous preset to each flip-flop, a fully independent clear input, internal cascading circuitry, and provides synchronous counting operations. The truth table is shown below. Figure C-14 shows the 74193 circuitry.

Count Up	Count Down	Load	Mode
X	X	L	Parallel Load
CLOCK	H	H	Count Up
H	CLOCK	H	Count Down

H = high level, L = low level, X = irrelevant

Signal/Pin Designation

Signal Name	Pin Designation
DATA INPUT A	15
DATA INPUT B	1
DATA INPUT C	10
DATA INPUT D	9
CLEAR	14
LOAD	11
DOWN COUNT	4
BORROW OUTPUT	13
CARRY OUTPUT	12
UP COUNT	5
OUTPUT Q_A	3
OUTPUT Q_B	2
OUTPUT Q_C	6
OUTPUT Q_D	7

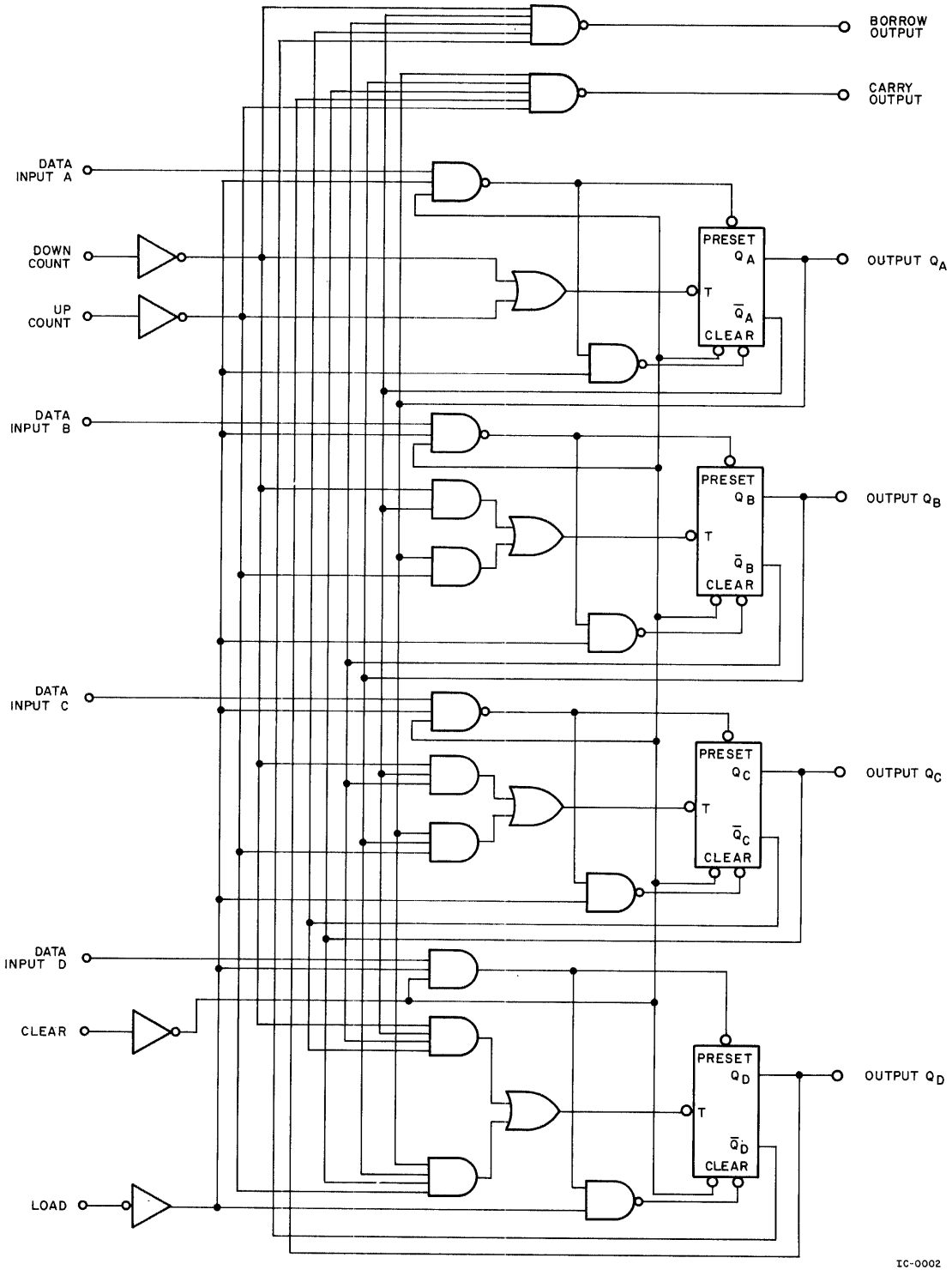


Figure C-14 74193 4-Bit Binary Counter

C.16 74S257 QUADRUPLE 2-LINE TO 1-LINE MULTIPLEXERS WITH THREE-STATE OUTPUTS

The 74S257 features buffered inputs and outputs. All outputs are in the high impedance state when disabled (enable high). Figure C-15 shows the 74S257 circuitry.

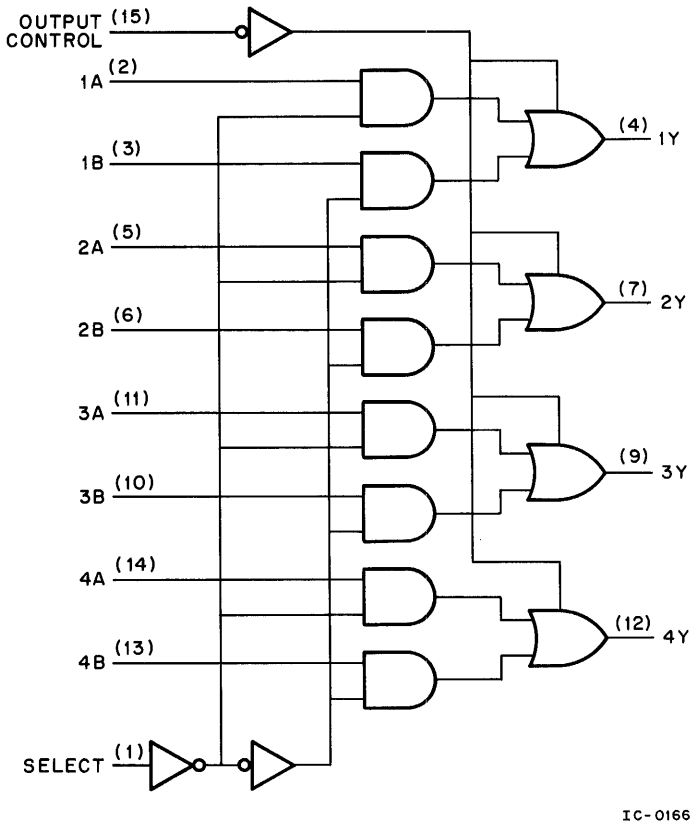


Figure C-15 74S257 Quadruple 2-Line to 1-Line Multiplexers

APPENDIX D
CONSOLE CONTROLS AND INDICATORS

D.1 INTRODUCTION

The XVM console provides the switches and indicators required for operator initiation, control, monitoring, and maintenance of the system. Any of 24 18-bit registers can be displayed at one time to provide the operator with visual indications of all registers and buses. Console controls are described in Table D-1; indicators are described in Tables D-2 and D-3. The two rows of key-type switches are identified by corresponding rows of labels, located just below the indicator portion of the console. The upper row of labels identify the rear switches; the lower row of labels identify the front switches. Unless otherwise indicated, a switch function is active when the rear half of the switch is depressed or, in the case of momentary contact switches, when the elevated half of the switch is momentarily depressed.

Table D-1
Console Controls

Control	Type	Function
Repeat Speed/System Power	Potentiometer/switch	Controls the rate of repeat activity when the system is in repeat mode. The repeat rate is continuously variable from 1 Hz to 10 kHz. When rotated beyond detent at full counterclockwise position, removes all power to system.
DATA	Eighteen two-position rocker switches	Word length (bits 00-17) register switches to provide binary data that can be read either into the accumulator by execution of an OAS (OR the switch content with the accumulator content) instruction, or into memory under control of the DEPOSIT or executed by the EXEC switch.
ADDRESS	Fifteen two-position rocker switches	Specifies a memory location. These switches are used in conjunction with the START, DEPOSIT and EXAMINE switches.
START	Spring-loaded momentary-contact switch	Initiates program execution at the memory location specified by the setting of the ADDRESS switches.

Table D-1 (Cont)
Console Controls

Control	Type	Function
CONT	Spring-loaded momentary-contact switch	a. Resumes program execution at the point that it was halted, determined by the contents of the program counter (PC). b. In conjunction with other control switches (SING TIME, SING STEP, SING INST), steps the program sequentially through the desired time states (SING TIME), major states states (SING STEP), or instruction (SING INST).
DEPOSIT THIS	Spring-loaded momentary-contact rocker switch	Places the contents of the DATA switches in the memory location designated by the ADDRESS switches.
DEPOSIT NEXT	Spring-loaded momentary-contact rocker switch	Places the contents of the DATA switches in succeeding memory locations; the location is specified by the ADDRESS switches plus the number of times the NEXT switch is depressed.
EXAMINE THIS	Spring loaded momentary-contact rocker switch	Places the contents of memory location specified by the ADDRESS switches in the memory buffer (MB) register.
EXAMINE NEXT	Spring-loaded momentary-contact rocker switch	Places the contents of the memory location specified by the ADDRESS switches plus the number of times the NEXT switch is depressed into the memory buffer (MB) register. **NOTE** **Operation of the DEPOSIT THIS/NEXT and EXAMINE THIS/NEXT switches does not affect the AC, LINK, XR, LR and PC registers.**
STOP	Spring-loaded momentary-contact	Terminates program execution when the instruction that is in progress has been executed. **NOTE** **Operation of the STOP switch does not inhibit I/O data channel activity.**
EXEC	Spring-loaded momentary-contact rocker switch	Causes the instruction specified by the contents of the DATA switches to be executed. Program will stop following execution of the one instruction.

Table D-1 (Cont)
Console Controls

Control	Type	Function
RESET	Spring loaded momentary-contact rocker switch	Clears major registers (MB, AC, LINK, PC, IR, XR, LR) and control flip-flops (flags, option select). The clearing prevents any overlap of previous operations from interfering with new operations. Typically RESET is activated prior to reading in programs from paper tape. **NOTE** **STOP is the only switch active while the machine is running. If, at any time, machine must be reset while the RUN light is on, RESET and STOP switches should be depressed simultaneously. This is an unconditional reset procedure that should be used with caution, because data can be lost.**
READIN	Spring-loaded momentary-contact rocker switch	Initiates the hardware read-in process when transferring information from paper tape into memory. The data is read into memory starting at the location specified by the ADDRESS switches.
REG GROUP	Two-position rocker switch	Determines which group of registers the Register Select switch can access for display in the REGISTER indicators. When the front of the REG GROUP switch is depressed, the contents of the register specified in the left-hand window of the Register Select switch are displayed in the REGISTER indicators. When the rear of the REG GROUP switch is depressed, the register, bus, or status information specified in the right-hand window of the Register Select switch are displayed on the REGISTER indicators; typically this second group is used for maintenance purposes.
Register Select	Twelve-position rotary switch	In conjunction with the REG GROUP switch, selects the register, bus, or status data and control signals to be displayed in the REGISTER indicators (see TABLE D-2).
SING TIME	Two-position rocker switch	In conjunction with the Continue (CONT) switch, permits the manual stepping of the program through individual time states of each major state.
SING STEP	Two-position rocker switch	In conjunction with the Continue (CONT) switch, permits the manual stepping of the program through individual major states of each instruction.

Table D-1 (Cont)
Console Controls

Control	Type	Function
SING INST	Two-position rocker switch	In conjunction with the Continue (CONT) switch, permits the manual stepping of the program through one instruction at a time.
REPT	Two-position rocker switch	With this switch in the ON position, the processor will repeat the key function depressed by the operator at the rate specified by the repeat speed setting. START – program execution will restart at a repeat rate of from 1 Hz to 3 kHz after the machine halts. EXECUTE – the instruction in the data switches will be executed at the repeat clock rate (1 Hz to 10 kHz). CONTINUE – program execution will continue at the repeat clock rate (1Hz to 10 kHz) after halting. DEPOSIT: THIS, NEXT EXAMINE: THIS, NEXT – the Deposit This; Deposit Next or Examine This; Examine Next function will be repeated at the rate of from 1 Hz to 3 kHz. Depressing STOP or turning off the Repeat (REPT) switch will halt the repeat action.
USER	Two-position rocker switch	When set (back half of switch depressed) depressing START causes the system to start in User Mode.
BANK MODE	Two-position rocker switch	When set (back half of switch depressed) depressing START causes the system to start in bank mode permitting direct addressing of 8, 192 (17777_8) words of core memory. When switch is not set (front half depressed) depressing START causes the system to start in page mode permitting direct addressing of 4,096 (7777_8) words of core memory.
CLOCK	Two-position rocker switch	Inhibits program control of the real-time clock. Program control of the real-time clock resumes when the CLOCK switch is OFF.

Table D-2
Console Register Indicators

Register Select Switch	Register Bits	Function
REGISTER SELECT switch in position		The following summarizes the REGISTER display contents for each position of the REGISTER SELECT and REG GROUP switches. With REG GROUP switch down (lefthand REGISTER SELECT switch window determines REGISTER Display) the REGISTER indicators display the contents of:
AC	00-17	Accumulator register
PC	00-17	Program Counter register
OA	00-17	Operand Address register
MQ	00-17	Multiplier Quotient register
PL/SC	PLO-7, S0 11-17	Priority Level/Step counter
XR	00-17	Index register
LR	00-17	Limit register
EAE	00-07 STATES 08-17 OPERATION	Extended Arithmetic Element Discrete States (EAE option) and operations.
DSR	00-17	Data Storage register (IPU)
I/OB	00-17	Input/Output Bus
STA	00-17 FLAGS	Input/Output Status (indicates only when the processor is stopped).
MO	00-17	Memory Output register
REGISTER SELECT switch in position:		With REG GROUP switch up (righthand REGISTER SELECT switch window determines REGISTER display) the REGISTER indicators display contents of:
ABU	00-17	A Bus
BBU	00-17	B Bus
CBU	00-17	C Bus
SFT	00-17	Shift Bus
IOA	00-17	Input/Output address

Table D-2 (Cont)
Console Register Indicators

Register Select Switch	Register Bits	Function
SUM	00-17	Sum Bus **NOTE** **The EAE, A Bus, B Bus, C Bus, and Shift Bus output indications are complementary. Therefore, when these functions are selected for display, a lamp is off to indicate a logic 1 (assertion) and lighted to indicate a logic 0 (negation).**
M1	00-03	Control Discretes Group 1 Bit 00-Division shift to the D Bus 01-Multiply shift to the D Bus 02-Single left rotate (RAL) to the D Bus 03-Single right rotate (RAR) to the D Bus
	04-12	Bit 04-Double left rotate (RTL) to the D Bus 05-Double right rotate (RTL) to the D Bus 06-No shift to the D Bus 07-Console switches to the D Bus 08-C Bus to the A Bus 09-A Bus to the C Bus inverted 10-Index register to the A Bus 11-Read-in 12-Shift left 6 to the A Bus
	13-17	13-I/O address to the A Bus 14-ADDRESS switches to the A Bus 15-Operand address register (OA) to the A Bus 16-Data in 17-Data out
M2	00-17	Control Discretes Group 2 Bit 00-SKIP (1) H 01-Memory Input register (MI) inverted to the B Bus 02-Limit Register (LR) to the C Bus 03-AND to the B Bus 04-Load the Accumulator (AC) 05-Load the Memory Output register (MO) 06-Load the Program Counter (PC) 07-Load the Operand Address register (OA) 08-Load the Limit Register (LR) 09-Load the Index Register (XR) 10-Buffered AC to the C Bus 11-Index Register (XR) to the B Bus 12-I/O Bus to the C Bus 13-Exclusive OR to the C Bus

Table D-2 (Cont)
Console Register Indicators

Register Select Switch	Register Bits	Function
M2 (Cont)		14-Central Processor Memory Request CP MEM REQ (1) H 15-Start READ 16-Start WRITE 17-Request Central Processor Memory Release REQ CP MRLS (1) H
MMA	00-04	ADD 00-04
	05	ADD 16
	06	NEXM
	07	MSYNC
	08-17	Relocation Register 00-09
MMB	00	User Mode (in M7175)
	01-05	Memory Management register
	06	Protection Violation
	08-17	Boundary Register 00-09
MST	00-12	Memory States

Table D-3
Miscellaneous Console Indicators

Indicator	Function
POWER	Indicates that the power supply voltages are at operation levels.
RUN	Indicates that the program execution is in progress.
G MODE	Indicates G Mode has been selected in memory management (M7175).
CLOCK	Indicates that the real-time clock facility is enabled.
IOT D	Indicates that IOTs are permitted.
USER MODE	Indicates that the memory management User Mode is enabled.
DCH ACTIVE	Lights when the data channel is being serviced, i.e., data is being transferred between core memory and a device via the I/O Bus.
API ENABLE	Lights when the automatic priority interrupt system is activated.
API STATES ACTIVE 0-3 4-7	Indicates API level(s) active. Hardware levels. Software levels.
MAJOR STATES	
FETCH	Indicates that the processor is in the fetch state.
INC	Indicates that the processor is in the increment state.
DEFER	Indicates that the processor is in the defer state.
EAE	Indicates that the processor is in the EAE (extended arithmetic element) instruction state.
EXEC	Indicates that the processor is in the execute state.
TIME STATES 1,2,3	Indicates the processor time states. When all time states are off machine is in time state 2A of the ADD instruction.
PI ACTIVE	Indicates that a program interrupt is pending service.
PI ENABLE	Indicates that the program interrupt system is enabled (under program control).
MODE INDEX	Indicates that the processor is operating in page mode and therefore indexing can be accomplished.
LINK	Displays state of the Link bit.

Table D-3 (Cont)
Miscellaneous Console Indicators

Indicator	Function
INSTRUCTION	Displays contents of the 6-bit program word instruction field.
0-3	Displays the instruction operation code.
DEFER	Indicates that the operand is indirectly addressed.
INDEX	Indicates that the operand address is indexed when in page mode or that the upper 4K (of an 8K bank) is addressed when in bank mode.
MEMORY BUFFER 00-17	Displays the contents of the currently accessed memory address.
REGISTER 00-17	In conjunction with the setting of the REG GROUP and Register Select switches, displays: a. data in a register. b. data on a Bus. c. control signal levels.

APPENDIX E
XM15 SWITCH AND JUMPER RECORD

E.1 INTRODUCTION

Table E-1 is a switch and jumper record for the XM15 M7172, M7173, M7174, and M7175 modules. The table contains entries for the XM15 serial number and production settings which were entered at the time of manufacture on the date specified in the Date entry. Change columns are provided and are to be used when switch and/or jumper settings are changed in the field. Table E-1 is arranged by increasing module designations. Each module designation is subdivided into functions which are controlled by switches and/or jumpers on the modules.

Table E-1
XM15 Switch and Jumper Settings

XM15 Serial No.	Prod. Settings	Change 1	Change 2	Change 3	Change 4	Change 5
Date						
M7172 Addressing S1 1-8						
S2 7-8						
IPF Disable S2 5						
15 MSYNC S2 6						
No. 1 M7173 MSYNC TIMING W6						
W7						
W8						
W9						
Port Selection E65 S1						
S2						
S3						
S4						
S5						
S6						
S7						
S8						

Table E-1 (Cont)
XM15 Switch and Jumper Settings

XM15 Serial No.	Prod. Settings	Change 1	Change 2	Change 3	Change 4	Change 5
Date						
Selection Mode						
Port Interleaving E43 S1						
S2						
S3						
S4						
S5						
S6						
S7						
S8						
W11						
W12						
Interleaving Mode						
No.2 M7173 MSYNC TIMING W6						
W7						
W8						
W9						
Port Selection E65 S1						
S2						
S3						
S4						

Table E-1 (Cont)
XM15 Switch and Jumper Settings

XM15 Serial No	Prod. Settings	Change 1	Change 2	Change 3	Change 4	Change 5
Date						
No. 2 M7173 (Cont)						
S5						
S6						
S7						
S8						
Selection Mode						
Port Interleaving E43 S1						
S2						
S3						
S4						
S5						
S6						
S7						
S8						
W11						
W12						
Interleaving Mode						
M7174 EP Upper Boundary Address E1 S1						
S2						
S3						

Table E-1 (Cont)
XM15 Switch and Jumper Settings

XM15 Serial No.	Prod. Settings	Change 1	Change 2	Change 3	Change 4	Change 5
Date						
M7174 (Cont)						
S4						
W8						
W9						
Upper Boundary Address Octal						
EP Lower Boundary Address E1 S5						
S6						
S7						
S8						
W10						
Lower Boundary Address Octal						
EP Address Float W3						
W4						
W5						
W6						
W7						
Float Factor						
EP Interleaving E8 S1						
S2						

Table E-1 (Cont)
XM15 Switch and Jumper Settings

XM15 Serial No.	Prod. Settings	Change 1	Change 2	Change 3	Change 4	Change 5
Date						
M7174 (Cont)						
S3						
S4						
S5						
S6						
S7						
S8						
W13						
W14						
EP Interleaving Mode						
EP Port Selection E7 S1						
S2						
S3						
S4						
S5						
S6						
S7						
S8						
EP Port Selection Mode						
IPF Interleaving E95 S1						
S2						

Table E-1 (Cont)
XM15 Switch and Jumper Settings

XM15 Serial No.	Prod. Settings	Change 1	Change 2	Change 3	Change 4	Change 5
Date						
M7174 (Cont)						
S3						
S4						
S5						
S6						
S7						
S8						
W11						
W12						
IPF Interleaving Mode						
IPF Port Selection E101 S1						
S2						
S3						
S4						
S5						
S6						
S7						
S8						
IPF Port Selection Mode						
IPF Word Depth W15						

Table E-1 (Cont)
XM15 Switch and Jumper Settings

XM15 Serial No.	Prod. Settings	Change 1	Change 2	Change 3	Change 4	Change 5
Date						
M7174 (Cont)						
W16						
W17						
Word Depth						
M7175 Memory Management Mode W1						
Mode Selected						
NEXM Address S1 1						
2						
3						
4						
7						
8						
NEXM Address Octal						

NOTES:
1. Selection Mode = 8K, 16K, 32K, 64K, LSB.
2. Interleaving Mode = Non, 2X, 4X, LSB.
3. Float Factor = Positive relocation caused by use of the "float" jumpers.
4. Switch settings are either ON or OFF.
5. Jumpers are either IN or OUT.

Reader's Comments

XVM SYSTEMS MAINTENANCE MANUAL
EK-15XVM-MM-001

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults do you find with the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

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_____

Would you please indicate any factual errors you have found. _____

_____

_____

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