PDP-11 Diagnostic Handbook 1988

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PDP11 DIAGNOSTIC HANDBOOK
1988

This handbook is the result of the personal initiative and effort of Hanspeter Steinegger, System Support Engineer in the Swiss TSSC. He used every spare minute to complete this booklet.

This handbook is meant to be a tool for Field Engineers.
It is the second edition of the "FIELD ENGINEERING DIAGNOSTIC HANDBOOK" which was produced 5 years ago by the GER Product Support Organisation. This new handbook replaces the orange paperback which was published in 1982.

My compliments to Hanspeter, who demonstrated what an individual can achieve and in which direction we should go to be even more efficient as a Support Organisation.

Rolf Gnannt

FOREWORD

This diagnostic handbook will help you to maintain and repair PDP11 systems and their options. Even if you are not trained or are not familiar with an option, with the help of this book, you should be able to find and run the correct diagnostic test

Some information regarding the layout of this book

Each diagnostic test had to fit on one page, and one page is not much. Due to that limited space, I was not able to include error information. In case you get errors and you are unsure what the meaning is, your local Telephone Support Center can give you further error information (this is not valid for non Digital employees).

I wrote the diagnostic name with the newest revision level in this book (example : EQKCE1 , "E1" is the REV. level as of September 1987). The XXDP monitor will accept "??" in place of an revision level (example : .R EQKC??). In this case it will run any revision it finds on the diagnostic media. This can help you to determine if your diagnostic test is at the newest revision. In time newer revision will exist therefore I would advise you to note them in your book.

At the end of this book you find a index of all the valid PDP11 diagnostic programs available today. Together with the DEC-X11 modules there are over a thousand tests.

Zuerich 30 - September 1987

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11/40

FP11-C

11/70 CPU,CACHE

11/70 MMU,UNIBUS MAP

11/70 MJ11 CORE MEMORY

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11/34 CPU, FPP, CACHE

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11/23/24 CPU, FPP, CIS

11/44 FPP, CPU, CACHE

11/21 CPU

11/84/83/73

11/60 FPP, CPU, CACHE

11/03 LSI

MSV11-J

MSV11-L/D/P

11/73 LSI CPU

11/60 MEMORY MF11S-K

MEMORY MS11/L/M/P

PDP11 INSTR./ I/O EXER

11/45 CPU TRAP TEST

ABSTRACT :

This program checks that on all trap operations register 6 is decremented the correct amount, that the correct PC is saved on the stack, that the old condition codes and priority are placed on the stack and that the new status and condition codes are correct. Both the TRAP and EMT trap instructions are tested to see that all combinations will trap. Checked also is that all reserved instructions will trap. Verification of the TRAP instruction 000003 which is used for software debug routines like ODT DDT is done. Also the trace bit is tested. Stack overflow, the RTI and RTT instructions are checked.

OPERATING PROCEDURES :

.R CKBME0

the test will ring the bell on pass completion

If an error is detected, there will be a program halt. In this case register 6 (the stackpointer) should be examined to determine its contens. Memory as specified by R6 contains the PC + 2 of the failing instruction which caused the faulty trap or interrupt.

SWITCH SETTINGS :

no switch settings

11/45 MEMORY MANAGEMENT TEST

ABSTRACT :

This program is designed using a "BOTTOM UP" approach starting with the smallest segment of MEMORY MANAGEMENT logic and building up to cover all the logic. The program begins by testing some of the internal CPU data and address path and address detection logic, then works outward through the MEM. MANAGEMENT registers. It is assumed that the CPU has been tested, or are known to be good. This test is able to map and exercising I/O devices like TC11, LP11, KW11-L and RF11 disks.

OPERATING PROCEDURES :

.R CKTGE0
The program will immediatly halt.
Set the desired switch settings.
Press continue.

The program will print a $ at the end off each Memory bank (4KW).
and a asterisk will be typed at the end of a full pass thru all memory.

SWITCH SETTINGS :

Switch settings before the program start

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit all error typeouts
SW12 = 1 inhibit trace trapping
SW11 = 1 inhibit iterations
SW10 = 1 inhibit processor test
SW09 = 1 inhibit cycling supervisor mapping
SW08 = 1 inhibit cycling supervisor page 7 access key

Switch settings to be set after the program halt.

SW07 = 1 inhibit TC11 dectape
SW06 = 1 inhibit RF11 disk
SW05 = 1 inhibit line printer
SW04 = 1 inhibit line clock
SW00 = 1 inhibit TTY output

11/40/45 INSTRUCTION EXERCISER

ABSTRACT :

This is a overall test of the 11/40/45 CPU, Memory Management in User and Kernel mode and all of the memory. In particular it tests the CPU and executes each instruction in all address modes and includes tests for traps, interrupts, the Unibus and the Massbus. If not deselected, the program relocates the test codes throughout memory. Also, if selected, the program will relocate using available disks, RF, RK, RP04, RS04 and RK06. Precautions must be taken to ensure the PROTECTION OF USER DISKS. Writers comment: this is a very good program use it as mutch as possible.

OPERATING PROCEDURES :

.R CQKCG0

The test will print after a pass:
"DCQKC DONE"

CONTROL SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current subtest
SW13= 1 inhibit error typeout
SW12= 1 inhibit relocation (run only first 8K of memory)
SW11= 1 inhibit subtest iteration
SW10= 1 ring bell on error
SW09= 1 inhibit relocation (above 28K)
SW08= 1 load PDP 11/45 micro-break register with SWR <07:00>
SW07= 1 print end of pass typeout "THE QUICK BROWN FOX..."
SW06= 1 inhibit clock interrupts
SW05= 1 enable relocation via all available disks
SW04= 1 enable random disk address selection for relocation
SW03= 1 enable relocation via I/O device

SW02= 1 device codes--;this switches when set cause the program
SW01= 1 device codes--;to relocate the test code using the device
SW00= 1 device codes--;specified below:

0 = CPU
1 = RK11
2 = RF11
3 = RP11
4 = RC
5 = RP04
6 = RS04
7 = RK06

11/45/55/70 FP11-C FLOATING POINT TEST 1

ABSTRACT :

This is the Floating point processor diagnostic FP11-C and consists of two programs designed to detect and report logic faults in the FPP of the 11/45/55 and 70 system. This part 1 is the basic FPP instruction test. After this test run also part 2 "EFPBA1".

OPERATING PROCEDURES :

.R EFPAA0

SWITCH SETTINGS :

SW15= 1 halt on error
SW13= 1 loop on current test
SW12= 1 inhibit all error type outs
SW11= 1 not used
SW10= 1 inhibit iterations
SW09= 1 ring bell on error
SW08= 1 loop on error
SW07= 1 loop on subtest specified in SW <07:00>
SW07= 0 load micro-break register with SW <07:00>
SW06= 1 selects subtest / micro-break reg.
SW05= 1 selects subtest / micro-break reg.
SW04= 1 selects subtest / micro-break reg.
SW03= 1 selects subtest / micro-break reg.

11/45/55/70 FP11-C FLOATING POINT TEST 2

ABSTRACT :

This is the Floating point processor diagnostic FP11-C and consists of two programs designed to detect and report logic faults in the FPP of the 11/45/55 and 70 system. This part 2 is the multiply - divide and ROM test.

OPERATING PROCEDURES :

.R EFPBA1

SWITCH SETTINGS :

SW15= 1 halt on error
SW13= 1 loop on current test
SW12= 1 inhibit all error type outs
SW11= 1 skip memory management tests
SW10= 1 inhibit iterations
SW09= 1 ring bell on error
SW08= 1 loop on error
SW07= 1 loop on subtest specified in SW <07:00>
SW07= 0 load micro-break register with SW <07:00>
SW06= 1 selects subtest / micro-break reg.
SW05= 1 selects subtest / micro-break reg.
SW04= 1 selects subtest / micro-break reg.
SW03= 1 selects subtest / micro-break reg.
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11/70 CPU EKBAD0

11/70 CPU DIAGNOSTIC PART 1

ABSTRACT :

This diagnostic is the first part of the 11/70 CPU, it designed to detect and report logic faults in the CPU. Any fault detected in this program causes the program to "HALT". After this, run the second part of the CPU test, EKBBF0.

OPERATING PROCEDURES :

set the switch register by <CONTROL P> (RD console)

CON= xxxxxxWZ

(W = deposit xxxxxx into console switch register)
(R = read and type console switch settings)
(Z = switch console terminal back to program)

.R EKBAD0

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on test
SW13= 1 inhibit error typeouts
SW12= 1 inhibit T-bit trapping
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test in SWR <07:00>
SW07= 1 not used
SW06= 1 skip bus request 6 test
SW05= 1 skip bus request 5 test
SW04= 1 skip bus request 4 test
SW00= 1 skip operator intervention testing

11/70 CPU DIAGNOSTIC PART 2

ABSTRACT :

This diagnostic is the second part of the 11/70 CPU, it tests advanced instructions and miscellaneous logic.

OPERATING PROCEDURES :

set the switch register by <CONTROL P> (RD console)

CON= xxxxxxWZ

(W = deposit xxxxxx into console switch register)

(R = read and type console switch settings)

(Z = switch console terminal back to program)

.R EKBBF0

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on test
SW13= 1 inhibit error typeouts
SW12= 1 inhibit T-bit trapping
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test in SWR <07:00>
SW07= 1 not used
SW06= 1 skip bus request 6 test
SW05= 1 skip bus request 5 test
SW04= 1 skip bus request 4 test
SW02= 1 test selector (with switch 8)
SW01= 1 test selector (with switch 8)
SW00= 1 skip operator intervention testing

11/70 CACHE TEST 1

ABSTRACT :

The programs EKBC and EKBD are repair and and test programs of the cache memory system in the 11/70 system. The failures (if any) are typically identified with a failing circuit when the report is made, but the overal diagnostic philosophy has been to locate the failing module out of four.

M8142	*CCB CACHE CONTROL BOARD*
M8143	*ADM CACHE ADDRESS MEMORY BOARD*
M8144	*DTM CACHE DATA MEMORY BOARD*
M8145	*CDP CACHE DATA PATHS BOARD*

The program EKBC is designed to test the boards M8142 and M8145, while EKBD is designed to test M8143 and M8144.

OPERATING PROCEDURES :

set the switch register by <CONTROL P> (RD console)

CON= xxxxxx**WZ**

(W = deposit xxxxxx into console switch register)

(R = read and type console switch settings /

(Z = switch console terminal back to program)

.R EKBCD1

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on test
SW13= 1 inhibit error printout
SW12= 1 not used
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test in SWR <06:00>
SW07= 1 skip execution of tests which use memory management
SW06= 1 selects the subtest in case SW 08 is on
SW05= 1 selects the subtest in case SW 08 is on
SW04= 1 selects the subtest in case SW 08 is on
SW03= 1 selects the subtest in case SW 08 is on
SW02= 1 selects the subtest in case SW 08 is on
SW01= 1 selects the subtest in case SW 08 is on
SW00= 1 selects the subtest in case SW 08 is on

11/70 CACHE TEST 2

ABSTRACT :

The programs EKBC and EKBD are repair and and test programs of the cache memory system in the 11/70 system. The failures (if any) are typically identified with a failing circuit when the report is made, but the overal diagnostic philosophy has been to locate the failing module out of four.

M8142	*CCB CACHE CONTROL BOARD*
M8143	*ADM CACHE ADDRESS MEMORY BOARD*
M8144	*DTM CACHE DATA MEMORY BOARD*
M8145	*CDP CACHE DATA PATHS BOARD*

The program EKBC is designed to test the boards M8142 and M8145, while EKBD (this test) is designed to test M8143 and M8144.

OPERATING PROCEDURES :

set the switch register by <CONTROL P> (RD console)

CON= xxxxxxWZ

(W = deposit xxxxxx into console switch register)

(R = read and type console switch settings /

(Z = switch console terminal back to program)

.R EKBDE1

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on test
SW13= 1 inhibit error printout
SW12= 1 not used
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test in SWR <06:00>
SW07= 1 skip execution of tests which use memory management
SW06= 1 selects the subtest in case SW 08 is on
SW05= 1 selects the subtest in case SW 08 is on
SW04= 1 selects the subtest in case SW 08 is on
SW03= 1 selects the subtest in case SW 08 is on
SW02= 1 selects the subtest in case SW 08 is on
SW01= 1 selects the subtest in case SW 08 is on
SW00= 1 selects the subtest in case SW 08 is on

11/70 MEMORY MANAGEMENT TEST

ABSTRACT :

This program was designed using a "BOTTOM UP" approach starting with the smallest segment of MEMORY MANAGEMENT logic and building up to cover all the logic. The program begins by testing some of the internal CPU data and address path and address detection logic, then works outward through the MEM. MANAGEMENT registers. It is assumed that both the CPU and the CACHE have been tested, or are known to be good.

OPERATING PROCEDURES :

set the switch register by <CONTROL P>

CON= xxxxxxWZ

(W = deposit xxxxxx into console switch register)

(R = read and type console switch settings / CON= R)

(Z = switch console terminal back to program)

.R EKBEE1

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit all error typeouts
SW12= 1 inhibit trace trapping
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test in SWR <06:00>
SW07= 1 inhibit multiple error typeouts
SW06= 1 selects subtest
SW05= 1 selects subtest
SW04= 1 selects subtest

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11/70 (M8141) UNIBUS MAP TEST

ABSTRACT :

This program assumes the CPU, cache and mem-management to be OK. It tests that all map registers can be addressed, tests all map registers with data patterns, addressing main memory through the UNIBUS by relocating to top 128K and MAP disabled, and tests relocation via UNIBUS - UNIBUS-MAP - MEMORY. If the program catches an error in a early test and is allowed to continue running through the later test the error indications from those later tests may be invalid. This is due to the structure of the program, which assumes that all areas tested prior to the current test are functioning properly. The test is giving you even chip level error descriptions.

OPERATING PROCEDURES :

set the switch register by <CONTROL P>

CON= xxxxxxWZ

(W = deposit into console switch register)
(R = read and type console switch settings / CON= R)
(Z = switch console terminal back to program)
(C = continue out from a halt state)
(H = CPU halt)
(I = initialize CPU and Unibus, clear all error ergister)
(N = execute next instruction in the program and halt)

.R EKBFD1

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error printout
SW12= 1 inhibit trace trapping
SW11= 1 inhibit iterations
SW10= 1 bell on error
SW09= 1 loop on error
SW08= 1 loop on test in SWR <06:00>
SW07= 1 inhibit multiple error typeouts
SW06= 1 selects the subtest in case SW 08 is on
SW05= 1 selects the subtest in case SW 08 is on
SW04= 1 selects the subtest in case SW 08 is on
SW03= 1 selects the subtest in case SW 08 is on
SW02= 1 selects the subtest in case SW 08 is on
SW01= 1 selects the subtest in case SW 08 is on
SW00= 1 selects the subtest in case SW 08 is on

11/70 POWER FAIL TEST

ABSTRACT :

This test is made of 2 sections section 1 and section 2. Section 1 serves as a test of CPU logic validity during a power fail sequence and consists of 16 subtests. This are simple power fail tests that guarantee that the proper machine states are entered on power fail and power up. This section can be run on a standard unmodified 11/70 processor. Section 2 is for 11/74 multi processor systems. This gets enabled by setting bit 6 of the SWR. All standard 11/70 CPU diagnostics should first be run to insure proper operation under normal stable power condition. The bootstrap has to be in the normal mode, obtaining a new PC from memory location 24 (not "POWER UP REBOOT"). Test 25 is an overal System power fail and recovery test.

OPERATING PROCEDURES :

.R EKBGC0

It prints :
CEKBG-C 11/70 POWER FAIL
[UNIPROCESSOR MODE IS IN EFFECT]

ENTERING SECTION 1

INTERRUPT THE POWER AFTER THE TEST NUMBER APPEARS IN THE DISPLAY.
IF YOU HAVE A RD CONSOLE, INTERRUPT THE POWER
AT THE END OF THIS MESSAGE.

Manualy power down, then up again for each subtest (15 octal times) until the "END PASS" message is printed.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on test
SW08= 1 enable system power fail test (subtest 25)
SW07= 1 disable section 1 (test multiprocessor mode only)

11/70 MJ11 PARITY MEMORY DIAGNOSTIC

ABSTRACT :

This program has the ability to test memory from address 000000 to address 17757777. It does so using unique address techniques, worst case noise patterns and instruction execution throughout memory. This program may be used to adjust and margin memory.

If there are parity errors in the lower area of core memory then you have to clear this first before booting with the following routine :
DEPOSIT A 14747 OCTAL INTO LOCATION 157776
LOAD ADDRESS 157776, RUN, WAIT A SECOND, HALT

OPERATING PROCEDURES :

set the desired switches
If the RD console is installed use <CONTROL P>, xxxxxxWZ
to set the swich register

.R EMJAD0

An asterisk "" will be printed after each pass.*
"CEMJA DONE" will be printed after each pass.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 inhibit relocation/ use of memory management
SW11 = 1 inhibit subtest iteration
SW10 = 1 ring bell on error
SW09 = 1 display error count in display
SW08 = 1 halt program (unrelocated)
SW07 = 1
SW06 = 1 use 18 bit unibus mapping only
SW05 = 1 not used
SW04 = 1 not used

11/70-MK11 EMKAB0

11/70 MK11 ECC (also mixed MJ/MK) MEMORY DIAG.

ABSTRACT :

This program has the ability to test memory from address 000000 to address 17757777. It does so using unique address techniques, worst case noise patterns and instruction execution throughout memory. The intention of this program is to test as comprehensively as possible MOS memories used on the 11/70 system. The test is also for MOS/CORE mixed configurations. In case you have a intermittend problem and you can have the system for a longer time run the test in "KAMIKAZE" mode, this causes all patterns to be run but takes very long for one pass. Be carfull with setting bit 0 in the SWR, in the maindec listing is the note : "FOR FIELD SERVICE THIS SWITCH SHOULD ALWAYS BE OFF". My comment : for one or two passes you can set this switch for a quick verify but if you leave it on for a longer time (4-24h) it will report errors or crash even with a good memory. This test has a special maintenance mode (field service mode) to provide specific functional capabilities.

Put a 000400 into SWR to stop the test (<CONTROL P> 000400WZ)
Use <CONTROL T> to see whats happening
Use <CONTROL F> to enter field service mode

FS mode 0 = exit field service mode
FS mode 1 = type out mem CSR register / 2 = load CSR register
FS mode 3 = examine memory / 4 = write memory loc. with xxx
FS mode 5 = select bank test
FS mode 10= type error summary
FS mode 13= enter kamikaze mode / 14= exit kamikaze mode
FS mode 15= turn cache off / 16= turn cache on

FS mode 99= type "field service mode" help text

OPERATING PROCEDURES :

R EMKAB0

it prints a memory map

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on test
SW13= 1 inhibit error typeout
SW12= 1 inhibit relocation
SW11= 1 inhibit subtest iteration
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 halt program (unrelocated)
SW07= 1 detailed error reports
SW06= 1 print configuration MAP
SW05= 1 limit max errors per bank
SW04= 1 FAT terminal (132 col. or better)
SW03= 1 test mode (banks forward/rev., patterns for./rev)
SW02= 1 test mode
SW01= 1 test mode
SW00= 1 detect single bit errors

11/70 INSTRUCTION / I/O EXERCISER

ABSTRACT :

This is a overall test of the 11/70 CPU, Memory Management in User and Kernel mode and all of the memory. It executes each instruction in all address modes and includes tests for traps, interrupts, the Unibus and the massbus. If not deselected, the program relocates the test codes throughout memory. Also, if selected, the program will relocate using available disks, RP03, RK05, RP04, RS03/04. Precautions must be taken to ensure the PROTECTION OF USER DISKS.

Writers comment: this is one of the 2 best and most importend 11/70 test, the other is EMKAB0 memory test.

OPERATING PROCEDURES :

.R EQKCE1

It will print a help text.
You can set the optional switch register
(with RD console <CONTROL P> xxxxxxWZ)
Type a character to start the test.

The test will print after a subpass:
!THE QUICK BROWN FOX JUMPED OVER THE LAZY DOGS BACK 0123456789
Execution time depends on the memory size.

CONTROL SWITCH SETTINGS :

set the SWR as the help text has typed.

11/70 RH70 CONTROLLER TEST

ABSTRACT :

This program tests the RH70 in the PDP 11/70 subsystem. It uses any working RH70 peripheral connected to the RH70 under test. It can test up to four RH70 connected to the subsystem. Although the peripheral connected is used, the peripheral is not tested by this program. The drive on the RH70 must have a scratch pack installed. A tape drive must have a scratch tape mounted.

OPERATING PROCEDURES :

.R ERHAE1

Set switch register before starting.
The test prints :

CERHAE0 RH70 CTRLR DIAG
ON RH NO 1 BASE 176700 FOUND RM03 SINGLE PORT
AT UNIT NUMBER 0 VECTOR 000254

TESTING RH NO 1 USING BASE 176700 RM SINGLE PORT
AT UNIT NUMBER 0 VECTOR 000254

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit all error typeouts
SW12 = 1 not used
SW11 = 1 inhibit iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on subtest specified in SW <07:00>
SW07 = 1 selects subtest
SW06 = 1 selects subtest
SW05 = 1 selects subtest
SW04 = 1 selects subtest
SW03 = 1 selects subtest
SW02 = 1 selects subtest
....

11/34 FLOATING POINT TEST 1

ABSTRACT :

This is the Floating point processor diagnostic of the 11/34 FP11-A (M8267). To test the entire FP11-A, run part 1,2 and 3. Run the tests in sequence (first part 1 then 2 and 3). Each other pass will exercise the T-BIT trapping starting with pass 3 then 5,7,9... unless SW 12 is on. This diagnostic tests the following instructions: LDFPS, STFPS, CFCC, SETF, SETD, SETI, SETL, STST, LDF, LDD, STD, ADDF, ADDD, SUBF, SUBD.

OPERATING PROCEDURES :

.R FFPAA1

Set switch register before starting.
If there isn't any SWR it will print :

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit all error typeouts
SW12 = 1 inhibit T-bit trapping
SW11 = 1 inhibit iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on subtest specified in SW <06:00>
SW07 = 1 print error summary
SW06 = 1 selects subtest
SW05 = 1 selects subtest
SW04 = 1 selects subtest
SW03 = 1 selects subtest

11/34 FPP FFPBA0

11/34 FLOATING POINT TEST 2

ABSTRACT :

This is the Floating point processor diagnostic of the 11/34, the FP11-A (M8267). To test the entire FP11-A, run part 1,2 and 3. Run the tests in sequence (first part 1 then 2 and 3). This diagnostic tests the following instructions: ADDF, ADDD, SUBD, CMPD, CMPF, DIVD, DIVF, MULD, MULF, MODD, MODF. Some long floating-point instructions can be interrupted (by Unibus-Interrupt) and started again (as if that instruction had never been started). This function can not be tested in the field.

OPERATING PROCEDURES :

.R FFPBA0

Set switch register before starting.
If there isn't any SWR it will print

SWR = 00000 NEW =

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit all error typeouts
SW12 = 1 inhibit T-bit trapping
SW11 = 1 inhibit iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on subtest specified in SW <06:00>
SW07 = 1 print error summary
SW06 = 1 selects subtest
SW05 = 1 selects subtest
SW04 = 1 selects subtest
SW03 = 1 selects subtest
.....

11/34 FLOATING POINT TEST 3

ABSTRACT :

This is the Floating point processor diagnostic of the 11/34, the FP11-A (M8267). To test the entire FP11-A, run part 1,2 and 3. Run the tests in sequence (first part 1 then 2 and 3). Part 3 tests a lot of different floating point instructions, some of them with all possible source and destination modes. the results of the hardware floating point module is compared against the correct results written into the diagnostic. Some long floating point instructions can be interrupted (by Unibus-Interrupt)and started again (as if it that instruction had never been started). This function can not be tested in the field.

OPERATING PROCEDURES :

.R FFPCB0

Set switch register before starting.
If there isn't any it will print

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit all error typeouts
SW12 = 1 inhibit T-bit trapping
SW11 = 1 inhibit iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on subtest specified in SW <06:00>
SW07 = 1 print error summary
SW06 = 1 selects subtest
SW05 = 1 selects subtest
SW04 = 1 selects subtest
.....

11/34 BASIC CPU TEST

ABSTRACT :

This test checks all of the processor logic and microcode for all basic 11/34 instructions except the TRAP's and memory management instructions. In particular it tests:

-all branches on the condition codes
-intenal data path with different data patterns
-all scratch pad registers (GPR's)
-the PSW, write into and read it back
-all possible address modes

To test the full 11/34 CPU, run after:

FKABD0 trap test
FKACA0 EIS test
FKTGC0 Memory management test 1
FKTHB0 Memory management test 2

OPERATING PROCEDURES :

.R FKAAC0

The diagnostic will print a end of pass message after a sucessfull run.

The diagnostic responds to the detection of all errors by storing certain information in memory and halting the processor.

SWITCH SETTINGS :

No switch settings available

11/34 CPU TRAP TEST

ABSTRACT :

This program checks that on all trap operations register 6 is decremented the correct amount, that the correct PC is saved on the stack, that the old condition codes and priority are placed on the stack and that the new status and condition codes are correct. Both the TRAP and EMT trap instructions are tested to see that all combinations will trap. Checked also is that all reserved instructions will trap. Verification of the TRAP instruction 000003 which is used for software debug routines like ODT DDT is done. Also the trace bit is tested. Stack overflow, the RTI and RTT instructions are checked.

OPERATING PROCEDURES :

.R FKABD0

the test will print the title :
"CFKABD0 11/34 TRAPS TST"

After one pass it prints :
"CFKABD0 11/34 TRAP TST DONE"

If an error is detected, there will be a program halt. In this case register 6 (the stackpointer) should be examined to determine its contens. Memory as specified by R6 contains the PC + 2 of the failing instruction which caused the faulty trap or interrupt.

SWITCH SETTINGS :

no switch settings

11/34 EIS - EXTENDED INSTRUCTION SET TEST

ABSTRACT :

This diagnostic tests the ASH, ASHC, MUL and DIV instructions. This instructions are integrated into the basic CPU and is not an option for the 11/34.

OPERATING PROCEDURES :

.R FKACA0

The test will print only :

"END PASS"

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 not used
SW13= 1 inhibit error typeouts
use memory loc 176 if no SWR is available.

11/34 CACHE DIAGNOSTIC

ABSTRACT :

This is the 11/34 cache diagnostic (M8268). It uses the line clock (50, 60 Hz) for time messurement (memory loc 176 = 000 for 60 Hz and 001 for 50 Hz). 124KW of memory is needed for complete checkout of the TAG section in the cache. For the DMA test you need a UNIBUS exerciser box or board. It tests :

-that all 4 cache control registers can be written and read,
-all hit bits to be set after a hit
-the datapath and RAM chips with a data pattern (rotateing a 1 in 0's)
-the cache flush feature
-the cache parity error logic
-that the I/O page is not cached
-the address path and TAG field with patterns
-the cache bypass mode
-that all DMA write invalidates cache (need UNIBUS exer)
-and so on.....

OPERATING PROCEDURES :

.R FKKAB0

The program prints its name and expected run time and enters the command mode by prompting : "CACHE= >"

Valid commands are:

RUN	*starts the test*
<CONTROL C>	*stops the test and returns to command mode*
LOT	*loop on test in error*
CLOT	*cancel LOT*
LOE	*loop on error*
CLOE	*cancel LOE*
HOE	*halt on error*
CHOE	*cancel HOE*
IER	*inhibit error print out*
CIER	*cancel IER*
LST xxx	*loop on selected test, xxx = test number*
CLST	*cancel LST*

Example : LST 121 will execute all tests before 121 and will loop on this test after.

11/34 INSTRUCTION / I/O EXERCISER

ABSTRACT :

This is a overall test of the 11/34 CPU, Memory Management in User and Kernel mode and up to 124K words of memory. It executes each instruction in all address modes and includes tests for Traps, interrupts and Unibus. It is using peripherals like a RK11-RK05 and TC11, writes data to the entire disk and verifies it by a write check.

OPERATING PROCEDURES :

.L FKTGC0
set the CSR in loc 174 and SWR in 176 and start test at 200 or

.R FKTGC0 for a default run.

CONTROL SWITCH SETTINGS :

set the desired memory management option switches in loc 174
SW05= 1 inhibit variable memory expansion
SW02= 1 inhibit test the 4K bank as 32K virtual
SW01= 1 inhibit use of USER MODE
SW00= 1 disable MEMORY MANAGEMENT

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit all error typeout
SW12= 1 inhibit trace trapping
SW11= 1 inhibit iterations
SW10= 1 inhibit processor test

This switches are only read at start of the test
SW07= 1 use line printer
SW06= 1 test TC11 DECTAPE
SW05= 1 test RF11 DISK
SW04= 1 test LINE CLOCK
SW03= 1 test RK11 disk
SW00= 1 inhibit TTY output

11/34 MEM.MANAG. FKTHB0

11/34 MEMORY MANAGEMENT TEST

ABSTRACT :

This program was designed using a "BOTTOM UP" approach starting with the smallest segment of MEMORY MANAGEMENT logic and building up to cover all the logic. The program begins by testing some of the internal CPU data and address path and address detection logic, then works outward through the MEM. MANAGEMENT registers.

OPERATING PROCEDURES :

.R FKTHB0

The test will print:

CFKTHB0 11/34 MEMORY MGMT. DIAG.

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit all error typeouts
SW12 = 1 inhibit trace trapping
SW11 = 1 inhibit iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR <07:00>
SW07 = 1

use <CONTROL G> to change SWR in loc 176

ADDRESS/VECTOR FLOAT

UNIBUS/Q-BUS ADDRESS AND VECTOR ASSIGNMENTS

ABSTRACT :

This program helps you to assign addresses and vectors to options on the Q-BUS or UNIBUS. It prints a help text, then you have to enter the options you like to connect and configure on the bus. The program will print you then the address and vector for each interface.

OPERATING PROCEDURES :

.R FLOAT

the test will prints :

CZFLA FLOAT UTILITY PROG - VERSION: C0

CONTROL C TO RESTART PROGRAM
CONTROL Z TO PRINT SELECTED LIST
CONTROL S TO STOP PRINTING
CONTROL Q TO CONTINUE PRINTING
CONTROL A TO BACK UP DEVICE LIST

TERMINAL TYPES:
A = LA36 NO FILL
L = LA120 100 FILL CHARACTER
V = VT52 OR VT100 50 FILL CHARACTER
ENTER TERMINAL TYPE.(A,L,V)? L

POSSIBLE OPTIONS ARE
FA-FLOATING ADDRESSES, (DJ,DH,DQ,ETC.)
VA-FLOATING ADDRESSES AND VECTORS.
HE-HELP
EX-EXIT
ENTER OPTION:

11/04 BASIC CPU TEST

ABSTRACT :

This test checks all of the processor logic and microcode for all basic 11/04 instructions except the TRAP's and memory management instructions. In particular it tests:
-all branches on the condition codes
-internal data path with different data patterns
-all scratch pad registers (GPR's)
-the PSW, write into and read it back
-all possible address modes
-all instructions specified above

OPERATING PROCEDURES :

.R GKAAA0

the test will prints :
"END OF DGKAA"

The diagnostic responds to the detection of all errors by storing certain information in memory and halting the processor.

SWITCH SETTINGS :

No switch settings available

KEF11-B CIS DIAGNOSTIC

ABSTRACT :

This program verifies the KEF11-BA (CIS commercial instruction set) option with both memory management enabled and disabled. It allows the user to check out any combination of CIS chips. In virtually all cases, fault isolation is to the CIS chip level. The CIS option consists of six MOS-LSI control chips contained in three 40-pin hybrid carriers. All CIS instructions are chip partitioned, i.e. all the code for a particular instruction is contained on a particular control chip. The exception is that all CIS instructions must pass throug the first CIS chip (control chip DC303-004) before reaching their destination chip. To run this test the first CIS chip (DC303-004) must be installed. I have never seen the 3 40-pin hybrid chips separat, rather I have seen all 6 chips on one big ceramic hybrid.

OPERATING PROCEDURES :

.R JKDHB0

The test print :

CJKDHB0 KEF11 B CIS DIAGNOSTIC

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 scope loop
SW13= 1 inhibit error typeout
SW12= 1 not used
SW11= 1 inhibit subtest iteration
SW10= 1 not used
SW09= 1 not used
SW08= 1 not used
SW07= 1 Mem. Management always disabled
SW06= 1 Mem. Management always disabled
SW05= 1 test CIS control chip 9 (DC303-009)
SW04= 1 test CIS control chip 8 (DC303-008)
SW03= 1 test CIS control chip 7 (DC303-007)
SW02= 1 test CIS control chip 6 (DC303-006)
SW01= 1 test CIS control chip 5 (DC303-005)
SW00= 1 test CIS control chip 4 (DC303-004)

if SW <05:00> are all zero (default mode) then the diagnostic will test all six CIS chips.

11/04 CPU TRAP TEST

ABSTRACT :

This program checks that on all trap operations register 6 is decremented the correct amount, that the correct PC is saved on the stack, that the old condition codes and priority are placed on the stack and that the new status and condition codes are correct. Both the TRAP and EMT trap instructions are tested to see that all combinations will trap. Checked also is that all reserved instructions will trap. Verification of the TRAP instruction 000003 which is used for software debug routines like ODT DDT is done. Also the trace bit is tested. Stack overflow, the RTI and RTT instructions are checked.

OPERATING PROCEDURES :

.R GKABC0

the test will print : "END OF DGKAB"

If an error is detected, there will be a program halt. In this case register 6 (the stackpointer) should be examined to determine its contens. Memory as specified by R6 contains the PC + 2 of the failing instruction which caused the faulty trap or interrupt.

SWITCH SETTINGS :

no switch settings

In case you run this test without a DL11 - Console, you can set the bit 0 in memory location 322 to a 1. This makes the test running without a TTY console, but disables testing the WAIT instruction and the interrupt operation.

11/23 FPP (M8188) FLOATING POINT TEST 1

ABSTRACT :

This is the Floating point processor diagnostic FPF11 and consists of two programs designed to detect and report logic faults in the LSI 11/23 FPF11 floating point processor module (M8188).

OPERATING PROCEDURES :

.R JFPAA1

The test prints:
CJFPAA FPF11 DIAGNOSTIC, PART 1

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15 = 1 halt on error
SW13 = 1 loop on current test
SW12 = 1 inhibit all error typeouts
SW11 = 1 print test numbers
SW10 = 1 inhibit iterations
SW09 = 1 ring bell on error
SW08 = 1 loop on error
SW07 = 1 loop on subtest specified in SW <06:00>
SW06 = 1 reserved for logic analyzer
SW05 = 1 selects subtest
SW04 = 1 selects subtest
SW03 = 1 selects subtest
.....

use <CONTROL G> to modify the SWR at loc 176

11/23 FPP (M8188) FLOATING POINT TEST 2

ABSTRACT :

This is the Floating point processor diagnostic FPF11 and consists of two programs designed to detect and report logic faults in the LSI 11/23 FPF11 floating point processor module (M8188).

OPERATING PROCEDURES :

.R JFPBA0

The test prints:

CJFPBA FPF11 DIAGNOSTIC, PART 1

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15= 1 halt on error
SW13= 1 loop on current test
SW12= 1 inhibit all error typeout
SW11= 1 print test numbers
SW10= 1 inhibit iterations
SW09= 1 ring bell on error
SW08= 1 loop on error
SW07= 1 loop on subtest specified in SW <06:00>
SW06= 1 reserved for logic analyzer
SW05= 1 selects subtest
SW04= 1 selects subtest
SW03= 1 selects subtest

.....

use <CONTROL G> to modify the SWR at loc 176

11/23/24 MEMORY MANAGEMENT TEST

ABSTRACT :

This program was designed using a "BOTTOM UP" approach starting with the smallest segment of MEMORY MANAGEMENT logic and building up to cover all the logic. The program begins by testing some of the internal CPU data and address path and address detection logic, then works outwards through the MEM. MANAGEMENT registers. Then 18-bit and 22-bit mode relocation is tested.

OPERATING PROCEDURES :

.R JKDAD1

The test will print:

CJKDAD0 KTF11-AA MMU DIAG.

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit all error typeouts
SW12= 1 inhibit trace trapping
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test in SWR <07:00>
SW07= 1

11/23/24 CPU JKDBD0

11/23/24 BASIC CPU TEST

ABSTRACT :

This test checks the DCF11-AA processor logic and microcode. It consists of three parts: basic CPU instruction tests, TRAP tests and EIS instructions tests. In the first and second part, the program will halt on error, in part three, the EIS tests, when a error is detected, the error PC and test number will be typed and the program will continue execution.

CPU test: checks out the basic PDP11 instructions in every addressing mode with various data patterns.

TRAP test: tests all trap instructions, trap overflow conditions R6 (stack pointer), interrupts, the reset and wait instruction.

EIS test: tests ASH, ASHC, MUL and DIV instructions.

OPERATING PROCEDURES :

.R JKDBD0

This is the normal start at 200
the program will print :

CJKDBD0 DCF11 AA CPU DIAGNOSTIC

END PASS # 1
END PASS #15

The initial contens of loc 176 is 000000, the user may halt the program (normaly by the "BREAK" key on the console) open location 176 and change it, then restart the diagnostic at 200.

SWITCH SETTINGS :

SW15= 1 halt on error (part 3 only)
SW14= 1 inhibit error typeout (part 3 only)
SW01= 1 CIS chip set present
SW00= 1 skip trap test

11/23/24 KEF11 FLOATING POINT CHIP TEST 1

ABSTRACT :

The two programs JKDCB0 & JKDDB0 are desined to detect and report logic faults in the F-11 MMU and FPP chip set (because part of the FP microcode is in the MMU chip). The program prints the total number of passes completed. The test assumes that the basic CPU is faultless, to make sure run JKDBD0 CPU test.

OPERATING PROCEDURES :

.R JKDCB0

The program prints its name, and

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit all error type outs
SW12= 1 inhibit T-bit trapping
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on subtest specified in SW <06:00>
SW06= 1 selects subtest
SW05= 1 selects subtest
SW04= 1 selects subtest
SW03= 1 selects subtest
SW02= 1 selects subtest
.....

11/23/24 KEF11 FLOATING POINT CHIP TEST 2

ABSTRACT :

The two programs JKDCB0 & JKDDB0 are desined to detect and report logic faults in the F-11 MMU and FPP chip set (because part of the FP microcode is in the MMU chip). The program prints the total number of passes completed. The test assumes that the basic CPU is faultless, to make sure run JKDBD0 CPU test.

OPERATING PROCEDURES :

.R JKDDB0

The program prints its name, and

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit all error type outs
SW12= 1 inhibit T-bit trapping
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on subtest specified in SW <06:00>
SW06= 1 selects subtest
SW05= 1 selects subtest
SW04= 1 selects subtest
SW03= 1 selects subtest
SW02= 1 selects subtest
.....

11/24 CPU-BOARD M7133 GO-NOGO TEST

ABSTRACT :

This program is a GO-NOGO test for the PDP 11/24 CPU board. It tests the CPU including EIS, the MMU, the FPP, the LTC and both SLU's. It does not contain the capabilities of scope looping, error recovery or printing of error information. Error halts do indicate which device failed to allow the technician to determine which diagnostic to use to fix the board or what field replaceable unit may fix the board. The second SLU must have TURN-AROUND connector installed.

OPERATING PROCEDURES :

.R JKDEB0

If you want to change SWITCHES -
halt CPU, change loc 176, restart like @200G.

The program just halts in case of an error!
First pass runtime (worst case) 45 seconds

SWITCH SETTINGS :

SW15 = 1 not used
SW07 = 1 not used
SW06 = 1 not used
SW05 = 1 program reserved - program will set if CIS chip present
SW04 = 1 inhibit testing of SLU2
SW03 = 1 inhibit testing of LTC
SW02 = 1 inhibit testing of SLU1
SW01 = 1 inhibit testing FPP instruction set
SW00 = 1 inhibit testing of memory management unit

11/24 SLU & LTC (M7133) DIAGNOSTIC

ABSTRACT :

This program tests both serial line units (SLU's) and the line time clock (LTC) on the CPU (M7133) module. Its main purpose is to provide scope looping for repair personnel. Error type-outs identify a function being done and failed and to what logical portion of the board it failed on. The test needs a TURN-AROUND connector installed on SLU2.

OPERATING PROCEDURES :

.R JKDFB0

This will start the test at 200 (normal start)

Start address 204 will execute the ECHO test
An "" is printed at the beginning of the test. The ECHO test reads a character from the terminal ,writes that character to the terminal and reports any error.*

Start address 210 is the terminal output test. Depressing any character at the terminal halts the test.

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 scope loop
SW13= 1 inhibit error typeout
SW12=
SW11= 1 not used
SW10= 1 inhibit error flags test
SW09= 1 loop on error
SW08= 1 not used
SW07= 1 disable SLU2 data test
SW06= 1 inhibit LTC tests
SW05= 1 inhibit all SLU tests (both SLUS)
SW04= 1 inhibit SLU1 testing
SW03= 1 inhibit SLU2 testing

KEF11-B CIS DIAGNOSTIC

ABSTRACT :

This program verifies the KEF11-BA (CIS commercial instruction set) option with both memory management enabled and disabled. It allows the user to check out any combination of CIS chips. In virtually all cases, fault isolation is to the CIS chip level. The CIS option consists of six MOS-LSI control chips contained in three 40-pin hybrid carriers. All CIS instructions are chip partitioned, i.e. all the code for a particular instruction is contained on a particular control chip. The exception is that all CIS instructions must pass throug the first CIS chip (control chip DC303-004) before reaching their destination chip. To run this test the first CIS chip (DC303-004) must be installed. I have never seen the 3 40-pin hybrid chips separat, rather I have seen all 6 chips on one big ceramic hybrid.

OPERATING PROCEDURES :

.R JKDHB0

The test print :

CJKDHB0 KEF11 B CIS DIAGNOSTIC

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 scope loop
SW13 = 1 inhibit error typeout
SW12 = 1 not used
SW11 = 1 inhibit subtest iteration
SW10 = 1 not used
SW09 = 1 not used
SW08 = 1 not used
SW07 = 1 Mem. Management always disabled
SW06 = 1 Mem. Management always disabled
SW05 = 1 test CIS control chip 9 (DC303-009)
SW04 = 1 test CIS control chip 8 (DC303-008)
SW03 = 1 test CIS control chip 7 (DC303-007)
SW02 = 1 test CIS control chip 6 (DC303-006)
SW01 = 1 test CIS control chip 5 (DC303-005)
SW00 = 1 test CIS control chip 4 (DC303-004)

if SW <05:00> are all zero (default mode) then the diagnostic will test all six CIS chips.

KDF11-B SLU & LTC (M8189) DIAGNOSTIC

ABSTRACT :

This program tests both serial line units (SLU's) and the line time clock (LTC) on the CPU (M8189) module. Its main purpose is to provide scope looping for repair personnel. Error type-outs identify a function being done and failed and to what logical portion of the board it failed on. The test needs a TURN-AROUND connector installed on SLU2.

OPERATING PROCEDURES :

.R JKDIB0

This will start the test at 200 (normal start)

Start address 204 will execute the ECHO test
An "" is printed at the beginning of the test. The ECHO test reads a character from the terminal ,writes that character to the terminal and reports any error.*

Start address 210 is the terminal output test. Depressing any character at the terminal halts the test.

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 scope loop
SW13 = 1 inhibit error typeout
SW12 =
SW11 = 1 not used
SW10 = 1 inhibit error flags test
SW09 = 1 loop on error
SW08 = 1 not used
SW07 = 1 disable SLU2 data test
SW06 = 1 inhibit LTC tests
SW05 = 1 inhibit all SLU tests (both SLUS)
SW04 = 1 inhibit SLU1 testing
SW03 = 1 inhibit SLU2 testing

KDF11-B CPU-BOARD M8189 GO-NOGO TEST

ABSTRACT :

This program is a go-nogo test for the MICRO PDP11 CPU board. It tests the CPU including EIS, the MMU, the FPP, the LTC and both SLU's. It does not contain the capabilities of scope looping, error recovery or printing of error information. Error halts do indicate which device failed to allow the technician to determine which diagnostic to use to fix the board or what field replaceable unit may fix the board. The second SLU must have turn around connector installed. This program is set to do minimum testing unless action is taken via the Software switch register (memory loc. 176). Bits 1, 6, 7-10 have been set up such that the program will bypass certain tests unless the switch register bit is set.

OPERATING PROCEDURES :

.R JKDJB0

If you want to change SWITCHES -
halt CPU,(Break if enabled)
change loc 176, restart like @200G.

START TESTING

error reporting looks like :
"FAILED DURING CPU TESTS"

SWITCH SETTINGS :

SW15= 1 not used
SW11= 1 not used
SW10= 1 test E102 switches
SW09= 1 test parity error detection
SW08= 1 use the Q22-BUSEXER
SW07= 1 test the upper 5 address bits for time out
SW06= 1 test using a Q-BUS exerciser
SW05= 1 program reserved - program will set if CIS chip present
SW04= 1 inhibit testing of SLU2
SW03= 1 inhibit testing of LTC
SW02= 1 inhibit testing of SLU1
SW01= 1 test FPP instruction set
SW00= 1 inhibit testing of memory management unit

KDF11-BE CPU-BOARD M8189 GO-NOGO TEST

ABSTRACT :

This program is a go-nogo test for the MICRO PDP11 CPU board. It tests the CPU including EIS, the MMU, the FPP, the LTC and both SLU's. It does not contain the capabilities of scope looping, error recovery or printing of error information. Error halts do indicate which device failed to allow the technician to determine which diagnostic to use to fix the board or what field replaceable unit may fix the board. The second SLU must have turn around connector installed. This program is set to do minimum testing unless action is taken via the Software switch register (memory loc. 176). Bits 1, 6, 7-10 have been set up such that the program will bypass certain tests unless the switch register bit is set.

OPERATING PROCEDURES :

.R JKL5B0

If you want to change SWITCHES -
halt CPU, (Break if enabled)
change loc 176, restart like @200G.

START TESTING

error reporting looks like :
"FAILED DURING CPU TESTS"

SWITCH SETTINGS :

SW15 = 1 not used
SW11 = 1 not used
SW10 = 1 test E102 switches
SW09 = 1 test parity error detection
SW08 = 1 use the Q22-BUSEXER
SW07 = 1 test the upper 5 address bits for time out
SW06 = 1 test using a Q-BUS exerciser
SW05 = 1 program reserved - program will set if CIS chip present
SW04 = 1 inhibit testing of SLU2
SW03 = 1 inhibit testing of LTC
SW02 = 1 inhibit testing of SLU1
SW01 = 1 test FPP instruction set
SW00 = 1 inhibit testing of memory management unit

11/44 FLOATING POINT (M7093) TEST 1

ABSTRACT :

This is the Floating point processor diagnostic of the 11/44, it is almost identical to the 11/34 FP11-A test. To test the entire FP11-F, run part 1,2 and 3. Run the tests in sequence (first part 1 then 2 and 3). Each other pass will exercise the T-BIT trapping starting with pass 3 then 5, 7, 9 ... unless SW 12 is 1. This diagnostic tests the following instructions: LDFPS, STFPS, CFCC, SETF, SETD, SETI, SETL, STST, LDF, LDD, STD, ADDF, ADDD, SUBF, SUBD.

OPERATING PROCEDURES :

.R KFPAD0

Set switch register by <CONTROL P>
>>>D SW xxxxxx<CR>
>>>C<CR> - back to program mode

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit all error type outs
SW12= 1 inhibit T-bit trapping
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on subtest specified in SW <06:00>
SW07= 1 print error summary
SW06= 1 selects subtest
SW05= 1 selects subtest
SW04= 1 selects subtest
SW03= 1 selects subtest
SW02= 1 selects subtest
SW01= 1 selects subtest
SW00= 1 selects subtest

11/44 FLOATING POINT (M7093) TEST 2

ABSTRACT :

This is the Floating point processor diagnostic of the 11/44, it is almost identical to the 11/34 FP11-A test. To test the entire FP11-F, run part 1,2 and 3. Run the tests in sequence (first part 1 then 2 and 3). This diagnostic tests the following instructions: ADDF, ADDD, SUBD, CMPD, CMPF, DIVD, DIVF, MULD, MULF, MODD, MODF. Some long floating-point instructions can be interrupted (by Unibus-Interrupt) and started again (as if that instruction had never been started). This function can not be tested in the field.

OPERATING PROCEDURES :

.R KFPBC0

Set switch register by <CONTROL P>
>>>D SW xxxxxx <CR>
>>>C<CR> - back to program mode

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit all error type outs
SW12 = 1 inhibit T-bit trapping
SW11 = 1 inhibit iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on subtest specified in SW <06:00>
SW07 = 1 print error summary
SW06 = 1 selects subtest
SW05 = 1 selects subtest
SW04 = 1 selects subtest
SW03 = 1 selects subtest
SW02 = 1 selects subtest
SW01 = 1 selects subtest
SW00 = 1 selects subtest

11/44 FLOATING POINT (M7093) TEST 3

ABSTRACT :

This is the Floating point processor diagnostic of the 11/44, it is almost identical to the 11/34 FP11-A test. To test the entire FP11-F, run part 1,2 and 3. Run the tests in sequence (first part 1 then 2 and 3). Part 3 tests a lot of different floating point instructions, some of them with all possible source and destination modes. The results of the hardware floating point module is compared against the correct results written into the diagnostic. Some long floating-point instructions can be interrupted (by Unibus-Interrupt) and started again (as if that instruction had never been started). This function can not be tested in the field.

OPERATING PROCEDURES :

.R KFPCD0

Set switch register by <CONTROL P>
>>>D SW xxxxxx <CR>
>>>C<CR> - back to program mode

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit all error type outs
SW12 = 1 inhibit T-bit trapping
SW11 = 1 inhibit iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on subtest specified in SW <06:00>
SW07 = 1 print error summary
SW06 = 1 selects subtest
SW05 = 1 selects subtest
SW04 = 1 selects subtest
SW03 = 1 selects subtest
SW02 = 1 selects subtest
SW01 = 1 selects subtest
SW00 = 1 selects subtest

11/44 BASIC CPU TEST

ABSTRACT :

This tests checks all of the processor logic and microcode for all basic 11/44 instructions except the TRAP's and memory management instructions. In particular it tests:
-all branches on the condition codes
-intenal data path with different data patterns
-all scratch pad registers (GPR's)
-the PSW, write into and read it back
-all possible address modes
-all instructions specified above,
-the EIS instructions ASH, ASHC, MUL, DIV

OPERATING PROCEDURES :

.R KKAAB0

the test will print :
END OF CKKAAB0 11/44 CPU/EIS

The diagnostic responds to the detection of all errors by storing certain information in memory and halting the processor.

SWITCH SETTINGS :

no switch settings

11/44 CPU TRAP TEST

ABSTRACT :

This program checks that on all trap operations register 6 is decremented the correct amount, that the correct PC is saved on the stack, that the old condition codes and priority are placed on the stack and that the new status and condition codes are correct. Both the TRAP and EMT trap instructions are tested to see that all combinations will trap. Checked also is that all reserved instructions will trap. Verification of the TRAP instruction 000003 which is used for software debug routines like ODT DDT is done. Also the trace bit is tested. Stack overflow, the RTI and RTT instructions are checked.

OPERATING PROCEDURES :

.R KKABD1

the test will print :
END OF CKKABD0 11/44 TRAPS

If an error is detected, there will be a program halt. In this case register 6 (the stackpointer) should be examined to determine its contens. Memory as specified by R6 contains the PC + 2 of the failing instruction which caused the faulty trap or interrupt.

SWITCH SETTINGS :

no switch settings

11/44 POWER FAIL TEST

ABSTRACT :

This test is made of 11 subtests. The 2 milisecond power down and power up time is checked on each power fail. The subtests check the following:
-01 simple power down/up test in kernel
-02 power fail with branch instruction
-03 power fail with EMT trap
-04 power fail with odd address
-05 power fail with time-out in kernel
-06 power fail with stack overflow
-07 power fail with reset
-10 power fail with memory management abort
-11 will use memory management to run the volatility test for all memory available

It is assumed that CPU, traps, memory management and Unibus MAP diagnostic have been run successfully.

OPERATING PROCEDURES :

.R KKACC0

It prints :
CKKACC0 11/44 POWER FAIL TEST
BOOT ENABLE SWITCH MUST BE OFF

Then it prints the size of memory and operating instruction. The subtest number will be printed at the beginning of each test. Manualy power down, then up again for each subtest until the "END PASS" message is printed.

For MOS memory with no battery-backup use the STD BY (stand by) mode.

SWITCH SETTINGS :

SW14= 1 loop on test

This bit must be set to a 1 after error halt every time the test is to be repeated.

11/44 (M7096) MFM-8085 TEST

ABSTRACT :

The Multi Function Module (MFM) self test is desined to test hardware assosiated with the 8085 Front-End CPU, handling the concole functions on the 11/44. The T test checks the 8085 subsystem (CPU, ROM's and RAM's). This test does not interfere with the state of the big CPU and memory. After a successful pass it prints "CONSOLE". In addition, a LED on the MFM module will be turned on at the beginning of "T" and extinguished at the successful completion of "T" test. It tests:

The "T" sequence :	*ROM checksum test*
	RAM data test
	RAM address test
The "T/E sequence :	*all "T" basic tests*
	halt and continue test
	PAX data line test
	PAX address line test
	Console switch register test

THIS DIAGNOSTIC IS IN ROM's AND NOT ON DISK OR TAPE

OPERATING PROCEDURES :

>>>T<CR> *this starts the console self test*
>>>T/E<CR> *this starts the console extensive test*

The tests resides in the Console ROM's

"CONSOLE TEST" is a progress message and some letters indicate the start of a new subtest.

C	*0-2K ROM test*
O	*2-4K ROM test*
NSO	*console RAM data test*
LE	*testing done*
T	*data bus test*
E	*PAX address test*
S	*switch register test*
T	*test complete*

11/44 (M7097) CACHE TEST

ABSTRACT :

The diagnostic is a logic test of the 11/44 cache. The maintenance features offered by the 11/44 cache allows information to be read in key areas of the cache allowing the diagnostic to isolate failures to data paths, and in some cases IC's. At the start of the diagnostic, a small area of write control logic and the maintenance features are assumed to be working. The cache is completly turned off and not turned on until 90 percent of the diagnostic is complete The test is using Mem. Management and Unibus-MAP. The following is tested:

-cache registers, address select logic, AMR register,
-that the I/O page is not cached
-the address path and TAG field with patterns
-the cache bypass mode
-that a DMA-write invalidates cache (the Unibus-Exerciser board is needed to perform DMA's)
.... and so on .....

OPERATING PROCEDURES :

set the switch register by <CONTROL P>
>>>D SW xxxxxx<CR>
>>>C (back to program mode)

.R KKKAC0

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test specified in SW <07:00>
SW13 = 1 inhibit error printout
SW12 = 1 inhibit iterations
SW09 = 1 loop on error
SW08 = 1 diag. will verify that invalidation will occure due to a read hit bypass condition. Test assumes physical strap W2 is in.
SW07 = 1 selects the subtest in case SW 08 is on
SW06 = 1 selects the subtest in case SW 08 is on
SW05 = 1 selects the subtest in case SW 08 is on
SW04 = 1 selects the subtest in case SW 08 is on
SW03 = 1 selects the subtest in case SW 06 is on
SW02 = 1 selects the subtest in case SW 08 is on
SW01 = 1 selects the subtest in case SW 08 is on
SW00 = 1 selects the subtest in case SW 08 is on

11/44 MEMORY MANAGEMENT TEST 1

ABSTRACT :

This program is the memory management logic test part 1,using a "bottom up" approach starting with the smallest segment and building up to cover all of the logic. Every other pass starting with the third one (3,5,7..) will exercise T-bit trapping unless inhibitted. The test is able to handle power fails, but only R0 to R6 are saved. It tests :

-the PSW, all PAR's and PDR's in Kernel mode,
-the Supervisor and User mode in I and D space,
-the MMR0, MMR1, MMR2 and MMR3 registers by using different data patterns,
-the Mem. Management in maintenance mode,
-18 bit mapping, 22 bit mapping,
-the W-bit (written into page bit)

OPERATING PROCEDURES :

set the switch register by <CONTROL P>
>>>D SW xxxxxx<CR>
>>>C (back to program mode)

.R KKTAB1

<CONTROL C> will cause the program to type the present test and pass number, requests a new value for the switch register and starts with subtest 1 again.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error printout
SW12= 1 inhibit trace trapping
SW10= 1 bell on error
SW09= 1 loop on error
SW08= 1 loop on test in SWR <07:00>
SW07= 1 selects the subtest in case SW 08 is on
SW06= 1 selects the subtest in case SW 08 is on
SW05= 1 selects the subtest in case SW 08 is on
SW04= 1 selects the subtest in case SW 08 is on
SW03= 1 selects the subtest in case SW 08 is on
SW02= 1 selects the subtest in case SW 08 is on
SW01= 1 selects the subtest in case SW 08 is on
SW00= 1 selects the subtest in case SW 08 is on

11/44 MEMORY MANAGEMENT TEST 2

ABSTRACT :

This program is the memory management logic test part 2, complementing part 1. It tests the special abort sequences, MFPI, MTPI and CSM instruction. Run KKTAB0 before this one. Every other pass starting with the third one (3,5,7) will exercise T-bit trapping unless inhibitted. The test is able to handle power fails. It tests :

-the non resident abort sequence,
-the read only abort sequence
-the page lengh abort sequence
-the abort sequence in super/user mode
-the instruction/data space abort
-tests the Move From/To Previous Instruction (MFPI, MTPI)
-tests the CSM (call supervisor mode) instruction

OPERATING PROCEDURES :

set the switch register by <CONTROL P>
>>>D SW xxxxxx <CR>
>>>C (back to program mode)

.R KKTBD0

<CONTROL C> will cause the program to type the present test and pass number, requests a new value for the switch register and starts with subtest 1 again.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error printout
SW12= 1 inhibit trace trapping
SW10= 1 bell on error
SW09= 1 loop on error
SW08= 1 loop on test in SWR <07:00>
SW07= 1 selects the subtest in case SW 08 is on
SW06= 1 selects the subtest in case SW 08 is on
SW05= 1 selects the subtest in case SW 08 is on
SW04= 1 selects the subtest in case SW 08 is on
SW03= 1 selects the subtest in case SW 08 is on
SW02= 1 selects the subtest in case SW 08 is on
SW01= 1 selects the subtest in case SW 08 is on
SW00= 1 selects the subtest in case SW 08 is on

11/44 (M7098), 11/24 (M7134) UNIBUS MAP TEST

ABSTRACT :

This program assumes the CPU, cache and mem-management to be OK. It tests that all map registers can be addressed, tests all map registers with data patterns, addressing main memory through the UNIBUS by relocating to top 128K and MAP disabled, tests relocation via UNIBUS - UNIBUS-MAP - MEMORY, tests the LMA register (last mapped address reg.) and tests the UNIBUS memory when optionaly selected by SW 05 = 1. There may be some cases where a bad cache module can interfere into this test and prohibits close isolation of an error. In this case you can run with the cache disabled. Simply load the cach CSR register (17777746) with 001000 then S 200 (start 0200). If CPU is an 11/24 program will prompt for a switch register input.

OPERATING PROCEDURES :

set the switch register by <CONTROL P>
>>>D SW xxxxxx <CR>
>>>C (back to program mode)

.R KKUAE0

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error printout
SW12 = 1 inhibit trace trapping
SW11 = 1 set when running on 11/24 and UNIBUS memory
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR <05:00>
SW07 = 1 inhibit multiple error typeouts
SW06 = 1 select Cache tests
SW05 = 1 select UNIBUS memory test
SW04 = 1 selects the subtest in case SW 08 is on
SW03 = 1 selects the subtest in case SW 08 is on
SW02 = 1 selects the subtest in case SW 08 is on
SW01 = 1 selects the subtest in case SW 08 is on
SW00 = 1 selects the subtest in case SW 08 is on

11/21-KXT-11 CPU NKXAB0

KXT-11 (M8063/M7676) SBC TEST

ABSTRACT :

The KXT11 is a T11-based single board computer (SBC-11). It includes a T11 CPU, up to 12 KW RAM, sockets for optional ROM's, two 8 bit serial I/O ports and one 8 bit parallel I/O port. This program has 147 (octal) tests designed to verify the integrity of those components. It tests in the following sequence:

1. *T11 CPU instruction tests*
2. *T11 CPU traps and interrupt tests*
3. *local RAM tests*
4. *local ROM address test*
5. *serial line unit 1 tests*
6. *serial line unit 2 tests*
7. *parallel I/O port tests*

The program has the following default parameters:

start address	*172000 (power up start)*
restart address	*172004 (time-out restart)*
local ROM address	*170000 (1KW macro-ODT for 11/21) or*
local ROM address	*164000 (2KW macro-ODT for 11/21+)*
local RAM address	*160000 (2KW for 11/21) or*
local RAM address	*100000 (12KW for 11/21+) or*
local RAM address	*140000 (4KW for 11/21+)*
BEVNT vector	*100 PRI6*
BHALT vector	*140 PRI7*
serial line unit 1 add.	*177560 console terminal*
serial line unit 1 vec.	*60*
serial line unit 2 add.	*177540 with loop-back connector*
serial line unit 2 vec.	*120*
parallel port address	*176200 with loo-back connector*
parallel port out-vec.	*130*
parallel port in-vec.	*134*
Q-BUS RAM address	*000000 16KW*

OPERATING PROCEDURES :

RUN NKXAB0 *put the loop-back connector H3275 on.*

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15= 1 halt on error
SW13= 1 inhibit error typeouts
SW12= 1 print error summary at END-PASS
SW09= 1 loop on error
use "CONTROL G" to enter software SWR in loc. 176

11/84/83/73 (M8190) EEPROM LOADER

ABSTRACT :

The KDJ11-B has two on-board ROM's. One contains the self-test and the boot code. The other contains the base area with hardware selection parameters, optional bootstraps, optional UFD (user friendly diagn.) system descriptrion area, and optional forein language text. The purpose of this program is to load the local language into the EEPROM. For each language is a particular program.

UK ENGLISH	*OEEAA0*
DUTCH	*OEEBA0*
FRENCH	*OEECA0*
GERMAN	*OEEDA0*
ITALIAN	*OEEEA0*
SPANISH	*OEEFA0*
SWEDISH	*OEEGB0*
US ENGLISH	*OEEHA0*

OPERATING PROCEDURES :

RUN OEE???

wait until the program types the prompt (.) again.

KDJ11-B CPU OKDAG0

11/84/83/73 (M8190) CPU/CACHE/MMU/SLU TEST

ABSTRACT :

This diagnostic tests the KDJ11-B CPU board, including the J11 chip set, on board cache, on board ROM's, including 16 bit and the 8 bit EEPROM, serial line unit, and line time clock. Some of the functionality of the cache is hidden inside the J11 and the rest of the functions is implemented in two on board GATE-ARRAYS. The storage capacity of the cache is 4 k bytes of RAM, called data-RAM's.It is a quad height Q22 bus module.

OPERATING PROCEDURES :

RUN OKDAG0

** KDJ11-B CPU DIAGNOSTIC - COKDAD0 **

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error typeouts
SW12 = 1 EEPROM subtest run switch
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR <05:00>
SW07 = 1 do extensive cache data RAM test
SW06 = 1 do extensive cache TAG RAM test
SW05 = 1 subtest number
SW04 = 1 subtest number
SW03 = 1 subtesr number

use "CONTROL G" to enter software SWR in loc. 176

KDJ11-D CLUSTER (CPU + MEMORY + ..) M7554 DIAGNOSTIC

ABSTRACT :

This diagnostic tests the 11/53 CPU board including the J11 chip set, on-board memory on-board ROM's, serial line unit, line time clock and the bus arbitration. The memory is 512 K byte with parity detection and has a CSR to determine parity errors. It has also 2 SLU (serial line units) with internal loop back mode for diagnostic and has a user selectable baud rate of 300 to 38400 baud.

.There is a CPU part of the test where it tests

CPU instuctions,
Memory Management Unit
Floating Point instructions

.On board memory tests

memory data path
memory accessability
memory error register
data shorts and stuck at bits
quick verify data and addressing test
parity detect logic and RAM's

.On board ROM code tests

the 16 bit checksum in the ROM's

.Line time clock tests

LTC bit 7
LKS interrupt priority

.Serial line unit tests
.and so on

OPERATING PROCEDURES :

.R OKDD??

** KDJ11-DA CPU DIAGNOSTIC - COKDDC0*

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error printouts
SW12= 1 enable test tracing
SW11= 1 inhibit subtest iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test specified in SW <05:00>
SW07= 1 inhibit the check parity test
SW06= 1 not used

11/84 UNIBUS ADAPTER TEST M8191

ABSTRACT :

This diagnostic tests the UNIBUS-ADAPTER (UBA) module M8191. The functionality of the module is : Unibus - PMI bus adapter (where PMI is a faster version of a Q22-BUS), M9312 compatible boot facility, and the Unibus-MAP logic. The module also has a DMA cache store, utilised for doing DMA transfers from memory to Unibus devices. The UBA can be programmed to do diagnostic cycles to verify some of the funtionality without requiring any of the peripherals to be actually connected to the unibus. There are 54 (decimal) subtests.

OPERATING PROCEDURES :

.R OKTAC0

COKTAC0 KTJ11-B DIAGNOSTIC

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error printouts
SW12= 1
SW11= 1 inhibit subtest iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test specified in SW <05:00>
SW07= 1 not used
SW06= 1 not used
SW05= 1 selects subtest number if SW08 is on
SW04= 1 selects subtest number if SW08 is on

11/60 FLOATING POINT TEST 1

ABSTRACT :

This is the Floating point processor diagnostic, for the "WARM FPP" which is standard in the 11/60 CPU and the "HOT FPP", that one is an option (4 modules M7878, M7879, M7880 and M7881). When the program is started a message is printed indicating the presence or absence of the optional FP11-E hot floating point unit (based upon the "WHAMI-REG" bit 4). The program selects and tests HOT or WARM-FP by setting and clearing bit 12 of the LOG-FLAG-INTERRUPT reg. (select HOT-FP = 1, select WARM-FP = 0). This test supports power fail, but none of the FP11 registers are saved. This can result in a error message typed after power is restored. This test assumes CPU, CACHE, and MEMORY are OK.

OPERATING PROCEDURES :

.R QFPAB0

The program prints its name and starts testing
In case of an error you can see in the first line of the error message weher the error happend in the HOT or WARM FP11.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit all error typeout
SW12= 1 inhibit "END PASS" typeouts
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test specified in mem loc. 01150
SW07= 1 not used
SW01= 1 test only unit (WARM- or HOT FP) specified in SW <00>
SW01= 0 select alternately HOT-FP then WARM-FP
SW00= 1 select "WARM FP" only
SW00= 0 select "HOT FP" only

11/60 FLOATING POINT TEST 2

ABSTRACT :

This is the Floating point processor diagnostic, for the "WARM FPP" which is standard in the 11/60 CPU and the "HOT FPP", that one is an option (4 modules M7878, M7879, M7880 and M7881). When the program is started a message is printed indicating the presence or absence of the optional FP11-E hot floating point unit (based upon the "WHAMI-REG" bit 4). The program selects and tests HOT or WARM-FP by setting and clearing bit 12 of the LOG-FLAG-INTERRUPT reg. (select HOT-FP = 1, select WARM-FP = 0). This test supports power fail, but none of the FP11 registers are saved. This can result in a error message typed after power is restored. This test assumes CPU, CACHE, and MEMORY are OK.

OPERATING PROCEDURES :

.R QFPBB0

The program prints its name and starts testing
In case of an error you can see in the first line of the error message weher the error happend in the HOT or WARM FP11.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit all error typeouts
SW12= 1 inhibit "END PASS" typeouts
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test specified in mem. loc 1150
SW07= 1 not used
SW01= 1 test only unit (WARM- or HOT FP) specified in SW <00>
SW01= 0 select alternately HOT-FP then WARM-FP
SW00= 1 select "WARM FP" only
SW00= 0 select "HOT FP" only

11/60 FLOATING POINT TEST 3

ABSTRACT :

This is the Floating point processor diagnostic, for the "WARM FPP" which is standard in the 11/60 CPU and the "HOT FPP", that one is an option (4 modules M7878, M7879, M7880 and M7881). When the program is started a message is printed indicating the presence or absence of the optional FP11-E hot floating point unit (based upon the "WHAMI-REG" bit 4). The program selects and tests HOT or WARM-FP by setting and clearing bit 12 of the LOG-FLAG-INTERRUPT reg. (select HOT-FP = 1, select WARM-FP = 0). The test is using the DL11-W line clock to provide I/O interrupts during execution. If present the KW11-P programmable clock will also be utilized. This test supports power fail, but none of the FP11 registers are saved. This can result in a error message typed after power is restored. This test assumes CPU, CACHE, and MEMORY are OK.

OPERATING PROCEDURES :

.R QFPCB0

The program prints its name and starts testing
In case of an error you can see in the first line of the error message weher the error happend in the HOT or WARM FP11.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit all error typeouts
SW12= 1 inhibit "END PASS" typeouts
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test specified in mem. loc. 1150
SW07= 1 not used
SW01= 1 test only unit (WARM- or HOT FP) specified in SW <00>
SW01= 0 select alternately HOT-FP then WARM-FP
SW00= 1 select "WARM FP" only
SW00= 0 select "HOT FP" only

11/60 FLOATING POINT TEST 4

ABSTRACT :

This is the Floating point processor exerciser, doing randomly ADD, SUB, MUL and DEV instructions in the "WARM FPP" which is standard in the 11/60 CPU and the "HOT FPP", that one is an option (4 modules M7878, M7879, M7880 and M7881). When the program is started a message is printed indicating the presence or absence of the optional FP11-E hot floating point unit (based upon the "WHAMI-REG" bit 4). The program selects and tests HOT or WARM-FP by setting and clearing bit 12 of the LOG-FLAG-INTERRUPT reg. (select HOT-FP = 1, select WARM-FP = 0). The test is using the DL11-W line clock to provide I/O interrupts during execution. If present the KW11-P programmable clock will also be utilized. This test supports power fail, but none of the FP11 registers are saved. This can result in a error message typed after power is restored. This test assumes CPU, CACHE, and MEMORY are OK.

OPERATING PROCEDURES :

.R QFPDB0

The program prints its name and starts testing
In case of an error you can see in the first line of the error message weher the error happend in the HOT or WARM FP11.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit all error type outs
SW12= 1 inhibit "END PASS" typeouts
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test specified in mem. loc. 01150
SW07= 1 not used
SW01= 1 test only unit (WARM- or HOT FP) specified in SW <00>
SW01= 0 select alternately HOT-FP then WARM-FP
SW00= 1 select "WARM FP" only
SW00= 0 select "HOT FP" only

11/60 FLOATING POINT TEST 5

ABSTRACT :

This program is a hardware oriented macro diagnostic for the FP11-E "HOT" FP processor option of the 11/60 CPU ("HOT FPP" is an option (4 modules M7878, M7879, M7880 and M7881). This test supports power fail, but none of the FP11 registers are saved. This can result in a error message typed after power is restored. This test assumes CPU, CACHE, and MEMORY are OK.

OPERATING PROCEDURES :

.R QFPEA0

The program prints its name and starts testing

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit all error type outs
SW12= 1 inhibit "END PASS" typeouts
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test specified in mem. loc 01150
SW07= 1 not used
SW06= 1 16. BIT FP data typeouts
SW06= 0 SIGN/EXP/FRAC FP data typeouts
SW05= 1 summary only error printouts
SW05= 0 detailed error printouts
SW04= 1 if error occures and loop-on error (SW09) is set force a tight loop on error to occur.

11/60 BASIC CPU TEST

ABSTRACT :

This tests are partitioned into four sections: 1. basic CPU test to verify the "Hardcore". Any fault causes the program to halt. 2. basic instruction test, any error cause a halt. 3. Comprehensive instruction test (main program) tests all instructions and reports any error. 4. Tests instructions in various combinations, manipulating variable data patterns. It also tests the MED and error logging features of the CPU.

OPERATING PROCEDURES :

.R QKDAE0

the test will print a "END PASS # 1 TOTAL ERRORS SINCE.." message

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit normal error printouts
SW12= 1 inhibit all error printouts
SW11= 1 inhibit subtest iterations
SW10= 1 loop on test in SWR <08:00
SW09= 1 loop on error
SW08= 1 not used
SW07= 1 not used

11/60 CPU TRAP TEST

ABSTRACT :

This program checks that on all trap operations register 6 is decremented the correct amount, that the correct PC is saved on the stack, that the old condition codes and priority are placed on the stack and that the new status and condition codes are correct. Both the TRAP and EMT trap instructions are tested to see that all combinations will trap. Checked also is that all restricted instructions will trap. Verification of the TRAP instruction 000003 which is used for software debug routines like ODT DDT is done. Also the trace bit is tested. Stack overflow, yellow and red zone violation are checked.

OPERATING PROCEDURES :

.R QKDBA0

the test will print a "END PASS # 1 TOTAL ERRORS SINCE.." message

If an error is detected, there will be a program halt. In this case register 6 (the stackpointer) should be examined to determine its contens. Memory as specified by R6 contains the PC + 2 of the failing instruction which caused the faulty trap or interrupt.

SWITCH SETTINGS :

no switch settings

11/60 INSTRUCTION / I/O EXERCISER

ABSTRACT :

This is a overall test of the 11/60 CPU, Memory Management in User and Kernel mode and up to 124K words of memory. It executes each instruction in all address modes and includes tests for Traps, Interrupts, Floating point, the Unibus and the Massbus. It is using peripherals like a RK11-RK05 for relocating the program. The low byte of the display register contains the current test #, the upper byte displays bits 11:4 of Kernel PAR0 (correspond to bits 17:10 physical address). Power fail is supported.

OPERATING PROCEDURES :

**** TAKE CARE TEST WRITES ONTO THE DISK ****

.R QKDCA0

The test will write the disk and unit # which will be used for relocation and waits for the operator to type a character · it gives you time to writeprotect a customer or diagnostic disk.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test that you are in
SW13= 1 inhibit all error type outs
SW12= 1 inhibit use of Unibus Exerciser if present
SW11= 1 inhibit iterations
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 relocate with CPU (no disk needed)
SW07= 1 inhibit system size typeout
SW06= 1 inhibit relocation
SW05= 1 inhibit round robin (use only selected disk rather all
SW04= 1 inhibit random disk addressing
SW03= 1 inhibit use of Massbus tester (if present)

SWR <0:2> along with SW 05 selects a disk

SW02= 1	*0 = RP11 / RP03*
SW01= 1	*1 = RK11 / RK05*
SW00= 1	*4 = RH11 / RP04*
	5 = RH11 / RS03/04

11/60 CACHE DIAGNOSTIC

ABSTRACT :

This program is a 13KW program, but 124 K words are needed for complete check of the cache TAG field. Also needed is a NPR device for testing invalidation of cache locations during NPR's DATO's (SW 08 = 1). The choise is: Unibus Exer. RK05, RP03 or TU10. When SW 08 is set the test will request you to select one of this devices. Before any device is choosen, it should be powered up, write enabled (scratch media loaded) and in the ready state. The program will then ask you device specific questions. The diagnostic checks the cache data path as well as the cache RAM chips with several data patterns. When SW 07 is set the program will ask you to switch of the machine and on again. This test will check the initialisation (clear) of the cache (only with core memory or battery back up).

OPERATING PROCEDURES :

.R QKKAA0

the test will print a "END PASS # 1 TOTAL ERRORS SINCE.." message

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test that you are in
SW13 = 1 inhibit all error type outs
SW12 = 1 bypass tests using Memory Management
SW11 = 1 inhibit iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 enable NPR device tests
SW07 = 1 enable power up test

11/60 MEMORY MANAGEMENT TEST

ABSTRACT :

This program will test all of the memory management logic, including the stack limit register logic, and enables the operator to isolate the detected failures to a replacable module. It is assumed that the CPU has been tested, or is known to be functioning correctly. This test is started from address 200. The 11/60 cache is turned off for the first pass of the program and is turned back on for the second and subsequent passes.

OPERATING PROCEDURES :

.R QKTAB0

the test will print a "END PASS # 1 TOTAL ERRORS SINCE.." message

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on the test that you are in
SW13= 1 inhibit all error type outs
SW12= 1 inhibit trace trap
SW11= 1 inhibit iterations after first pass
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test in SWR <06:00>
SW07= 1 inhibit multiple error type outs

LSI-11 BASIC ISTRUCTION TEST

ABSTRACT :

This program tests the LSI-11 BASIC instruction set in all modes. Trap type instructions are not tested. This test needs at least 4KW of memory. Place the LTC switch in off position. This test can be power failed with no error.

OPERATING PROCEDURES :

R VKAAC0

the test will print a "END PASS" message

First pass will take about 1 second
Other passes less than 20 seconds

SWITCH SETTINGS :

no swich settings available

LSI-11 EIS ISTRUCTION TEST

ABSTRACT :

This program tests the LSI-11 EIS instruction set <ASH, ASHC, MUL and DIV> option using registers 0-5 at least once with each instruction. It is also checked that extended instructions can be interrupted (by the console teletype). The program should be run for at least 2 passes with all switches low.

OPERATING PROCEDURES :

.R VKABB0

set optional switches in mem. loc 422
restart program.

the test will print a "END PASS" message

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 not used
SW13 = 1 inhibit printout
SW12 = 1 not used
SW11 = 1 not used

LSI-11 FIS ISTRUCTION TEST

ABSTRACT :

This program tests the LSI-11 floating instruction set <FADD, FSUB, FMUL and FDIV> option with fixed number patterns, using each register at least once as the stack pointer. The LINE-CLOCK LTC switch must be in the off position.

OPERATING PROCEDURES :

.R VKACC1

set optional switches in mem. loc 422
restart program

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 scope loop
SW13= 1 inhibit printout
SW12= 1 inhibit trace trapping
SW11= 1 enable iterations of subroutines
SW10= 1 bell on error
SW09= 1 loop on error
SW08= 1 loop on test in SWR <07:00>

LSI-11 TRAP TEST

ABSTRACT :

This is a test of all operations and instructions that causes traps, oddities of register 6, interrupts, the reset and wait instructions. It runs in LSI-11 or PDT-11 with a SLU and 4k word of memory. The clock must be disabled.

OPERATING PROCEDURES :

.R VKADC1

set optional switches in mem. loc 422
restart program

SWITCH SETTINGS :

SW06= 1 inhibit testing EIS/FIS opcodes 070000 - 075037
SW05= 1 inhibit "END OF PASS" typeouts
SW04= 1 inhibit testing opcodes 75400-76777 for reserved. instr. traps
SW03= 1 do not allow opcodes 170000-177777 to do res. inst. traps
SW02= 1 do not allow opcodec 76030-76057 (DIS reserved)
SW01= 1 test I/O address space 160000 - 167776
SW00= 1 not used

LSI-11 4K SYSTEM (INTERRUPT) EXERCISER

ABSTRACT :

This is an LSI-11 4k systems exerciser. It is a test of the processors ability to operate peripherals in interrupt mode. It is not a complete test of the peripherals themselves. The test occupies less than 4k of memory but does run a memory address test of all available memory above 4k. A processor instruction test is run while allowing the peripherals to interrupt at random. If relocation is enabled the processor instruction test is run in each 4k memory bank. If you test the DRV11, insure test cable (BC08R) is installed.

OPERATING PROCEDURES :

.R VKAHA1

set optional switches in mem. loc 176
restart program

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on subtest
SW13 = 1 inhibit error printouts
SW12 = 1 inhibit T bit trapping
SW11 = 1 inhibit subtest iteration
SW10 = 1 inhibit processor instruction test
SW09 = 1 inhibit instruction test relocation
SW08 = 1 restart program on error
SW07 = 1 inhibit end of pass printout
static switch settings
SW06 = 1 inhibit ASR33 low speed reader test
SW05 = 1 inhibit line printer test
SW04 = 1 inhibit DRV11 parallel line unit test
SW03 = 1 inhibit EIS/FIS test
SW02 = 1 inhibit console output test
SW01 = 1 inhibit floppy unit 1 test
SW00 = 1 inhibit floppy unit 0 test

static switch settings can only be modified if the test is to be restarted at 200

LSI-11 DIBOL INSTR. SET PART 1

ABSTRACT :

This program verifies the operation of the dibol move and string instructions of the LSI-11. The program checks that each instruction is interruptable using the console SLU interface and runs alternate passes with the trace trap enabled. You need a LSI-11 with Dibol chip installed.

OPERATING PROCEDURES :

.R VKAIB0

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 scope loop
SW13= 1 inhibit error typeout
SW12= 1 inhibit trace trap
SW11= 1 not used
SW10= 1 not used
SW09= 1 loop on error
SW08= 1 loop on test on SWR <05:00>
SW07= 1 inhibit interruptability tests
SW06= 1 not used

use "CONTROL G" to enter software SWR in loc. 176

LSI-11 DIBOL INSTR. SET PART 2

ABSTRACT :

This program verifies the operation of the dibol decimal instructions of the LSI-11. The program checks that each instruction is interruptable using the console SLU interface and runs alternate passes with the trace trap enabled. You need a LSI-11 with Dibol chip installed.

OPERATING PROCEDURES :

.R VKAJB0

There are 53 (octal) subtests in this diagnostic program

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 scope loop
SW13= 1 inhibit error typeout
SW12= 1 inhibit trace trap
SW11= 1 not used
SW10= 1 not used
SW09= 1 loop on error
SW08= 1 loop on test on SWR <05:00>
SW07= 1 inhibit interruptability tests
SW06= 1 not used
use "CONTROL G" to enter software SWR in loc. 176

LSI-11 TRAP TEST (30KW MEMORY + FIS)

ABSTRACT :

This program is a copy of VKAD?? with minor changes. The changes enable the the program to run with 30 KW of memory on the system. The program also defaults to running with "FIS" options. This is a test of all operations and instructions that causes traps, oddities of register 6, interrupts, the reset and wait instructions.

OPERATING PROCEDURES :

.R VKALA1

set optional switches in mem. loc 422
restart program

SWITCH SETTINGS :

SW15 = 1 not used
SW14 = 1 not used
SW06 = 1 inhibit EIS/FIS option tests
SW05 = 1 do not print "END OF PASS"
SW04 = 1 do not allow opcodes 75400-76777 to do res. instr. traps
SW03 = 1 do not allow opcodes 170000-177777 to do res. inst. traps
SW02 = 1 do not allow opcodec 76030-76057 (DIS reserved)
SW01 = 1 not used
SW00 = 1 not used

MSV11-J MEMORY VMJAB0

MSV11-J ECC (also mixed L/J/P TYPE) MEMORY DIAG.

ABSTRACT :

This program has the ability to test memory from address 000000 to address 17757777. It does so using unique address techniques, worst case noise patterns and instruction execution throughout memory. The intention of this program is to test as comprehensively as possible MOS memories used on the LSI-bus without concentrating on any one system. On the other side, this test is also not intended to be a total 100 % test of the memory. Other tests (DEC-X11) that to I/O may find memory problems that this test is unable to. This test has a special maintenance mode (field service mode) to provide specific functional capabilities. The first pass is a "QV" - quick verify pass.

Use <CONTROL C> to stop the program.

Use <CONTROL T> to see whats happening

Use <CONTROL F> to enter field service mode

FS mode 0 = exit field service mode

FS mode 1 = typeout CSR register / 2 = load CSR register

FS mode 3 = examine memory / 4 = write memory loc. with xxx

FS mode 5 = select bank test

FS mode 8 = type out error summary

FS mode 11 = enter kamikaze mode / 12 = exit kamikaze mode

FS mode 13 = turn cache off / 14 = turn cache on

FS mode 17 = test all banks and typeout the bank and pattern

FS mode 99 = type "field service mode" help text

OPERATING PROCEDURES :

.R VMJAB0

SWR = 000000 NEW =

it prints a memory map

SWITCH SETTINGS :

SW15 = 1 halt on error

SW14 = 1 loop on test

SW13 = 1 inhibit error typeout

SW12 = 1 inhibit relocation

SW11 = 1 inhibit subtest iteration

SW10 = 1 ring bell on error

SW09 = 1 loop on error

SW08 = 1 halt program (unrelocated)

SW07 = 1 detailed error reports

SW06 = 1 inhibit configuration MAP

SW05 = 1 limit max errors per bank

SW04 = 1 FAT terminal (132 col. or better)

SW03 = 1

SW00 = 1 detect single bit errors

Q-BUS MEMORY VMSAC0

0-4 MEGABYTE MEMORY EXER. (mixed D/L/P)

ABSTRACT :

This program has the ability to test memory from address 000000 to address 17757777. It does so using unique address techniques, worst case noise patterns and instruction execution throughout memory. The intention of this program is to test as comprehensively as possible all MOS memories used on the LSI-bus without concentrating on any one system. On the other side, this test is also not intended to be a total 100 % test of the memory. Other tests (DEC-X11) that to I/O may find memory problems that this test is unable to. This test does not run if you have MSV11-J (M8037) memory installed, use VMJAB0. Execution time for parity memory is 5 min. for 124 Kbyte, 20 min for 512 Kbyte, 120 min for 2560 Kbyte.

OPERATING PROCEDURES :

.R VMSA??

SWR = 000000 NEW =

KT11 (MEMORY MANAGEMENT) AVAILABLE
22 BIT ADR AVAIL

MEMORY MAP:
FROM 000000 TO 3777777

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on test
SW13= 1 inhibit error typeout
SW12= 1 inhibit memory management (initialy only)
SW11= 1 inhibit subtest iteration
SW10= 1 ring bell on error
SW09= 1 loop on error
SW08= 1 loop on test in SWR <4:0>
SW07= 1 inhibit program relocation
SW06= 1 inhibit parity error detection
SW05= 1 inhibit exercising vector area

Q-BUS MEMORY VMSBD0

0-4 MEGABYTE MEMORY QUICK VERIFY

ABSTRACT :

This program was created to do a quick verify test of Q-BUS memory. This was needed especially for testing the memory of a MICRO PDP-11. The program is designed to give the user friendly messages. There must be more than 64 KW of memory. It will tell you how long one pass will approximately take.

OPERATING PROCEDURES :

.R VMSB??

VMSBC0
-MEMORY 1024K bytes. Test time - 6 minutes, 44 seconds.....OK
-MEMORY 1024K bytes. test time - 6 minutes, 44 seconds.....OK

KDJ11-A (M8192) BASIC INSTR. /EIS/TRAP TEST

ABSTRACT :

This diagnostic tests the KDJ11 basic instruction set including EIS, TRAPS, and the alternate register set. Ensure that halt trap option is disabled (jumper W9 installed).

OPERATING PROCEDURES :

.R ZKDJ??

SWR = 000000 NEW =

At the end of each pass the diagnostic name and pass count are printed.

SWITCH SETTINGS :

SW12= 1 not used
SW11= 1 not used
SW10= 1 do not test BEVENT
SW09= 1 extended cache test
SW08= 1 18 bit address only
use "CONTROL G" to enter software SWR in loc. 176

New revision of DCJ11 (J11 CPU Chip) chip has a change to fix a problem found with ASH and ASHC instructions. The old diagnostic (REV B1) will fail with the new DCJ11 chip set installed.
You need a patch.

KDJ11-A (M8192) MEMORY MANAGEMENT DIAG.

ABSTRACT :

This diagnostic focuses on testing the MEMORY MANAGEMENT UNIT functionality. The test requires 4 megabytes of Q-BUS memory to fully test the MMU adder. A subset of the adder is tested if less than 4 megabyte of memory is available. In addition, for testing in Q-BUS systems with only 18 address bits, set bit 08 in the software switch register (loc. 176) to skip all tests which require 22 bit addressing.

OPERATING PROCEDURES :

.R ZKDKB0

SWR = 000000 NEW =

At the end of each pass the diagnostic name and pass count are printed.

SWITCH SETTINGS :

SW12 = 1 not used
SW11 = 1 not used
SW10 = 1 do not test BEVENT
SW09 = 1 extended cache test
SW08 = 1 18 bit address only
use "CONTROL G" to enter software SWR in loc. 176

KDJ11-A FP ZKDLB0

KDJ11-A (M8192) FLOATING POINT DIAGNOSTIC

ABSTRACT :

This diagnostic focuses on testing the floating point instruction functionality. Ensure that halt trap option is disabled (jumper W9 installed). You need 32 KW of memory. Keep in mind that each KDJ-11 chip has a floating point processor implemented, optional is a floating poit accelerator chip.

OPERATING PROCEDURES :

.R ZKDLB0

SWR = 000000 NEW =

At the end of each pass the diagnostic name and pass count are printed.

SWITCH SETTINGS :

SW12= 1 not used
SW11= 1 not used
SW10= 1 do not test BEVENT
SW09= 1 extended cache test
SW08= 1 18 bit address only
use "CONTROL G" to enter software SWR in loc. 176

KDJ11-A CACHE ZKDMB0

KDJ11-A (M8192) CACHE MEMORY DIAGNOSTIC

ABSTRACT :

This diagnostic focuses on testing the functionality of the cache memory system. A switch is provided in the software switch register to disable 22 bit address generation in 18 bit Q-BUS systems. This is implemented by setting bit 08 to a one. In addition, a switch is provided to enable the execution of the cache data, cache TAG RAM data reliability tests. This tests are very long and may not be desired in all cases. This tests are enabled by setting bit 09 in the software switch register (loc. 176) to one. The longest test is the TAG RAM DATA reliability test which takes approx. 25 minutes to execute. For this reason the data reliability tests are normaly deselected.

OPERATING PROCEDURES :

```
.R ZKDMB0

SWR = 000000 NEW =
```

SWITCH SETTINGS :

SW12= 1 not used
SW11= 1 not used
SW10= 1 do not test BEVENT
SW09= 1 extended cache tests
SW08= 1 18 bit address only
use "CONTROL G" to enter software SWR in loc. 176

CIS COMMERCIAL INSTRUCTION SET TEST

ABSTRACT :

This diagnostic is not directed at any specific CIS hardware (11/44, 11/24...) implementation but rather is intended to provide a exerciser for all PDP11 CIS processors. Therefor it can run on a 11/23, 11/24, 11/44 having CIS option. It tests all CIS instructions in register and inline mode by using all combinations of operands and data types, in USER, SUPER and KERNEL mode, memory management enabled and disabled, D-SPACE enabled and disabled and interrupts. Operands for each test case are either extracted from input tables or generated using a random number generater. Expected results are computed in the loop by emulating CIS instructions using basic PDP11 instructions.

OPERATING PROCEDURES :

.R ZKEEC0

SWR = 000000 NEW =
set optional switches

SA = Start address
SA = 204 enter parameters manualy
SA = 210 run quick verify mode only

Starting at 200 will do a quick verify pass, then a normal pass (about 30 minutes) followed by a random exerciser until the operator stops it.

Starting at 204 will get you into a dialog mode :
TEST INTERRUPS IN CIS INSTR. (KW11 REQUIRED) Y OR N ?
INTR SOURCE (R = LTC, N = KW11-P 100KHZ, C = KW11-P 10KHZ..
RANDOM EXERCISE MODE (Y OR N) ?
ENTER INSTRUCTION TO TEST <ALL>

CONTROL CHARACTERS:
"CONTR T" display test number and instruction under test
"CONTR C" restart exerciser (only when started at 204)
"CONTR D" display all operands and results, continue
"CONTR E" same as "CONTR D" but query for continue
"CONTR O" print progress report ON/OFF toggle.

SWITCH SETTINGS :

SW00 = 1 program will query for test # (in decimal) to stop and display
use "CONTROL G" to enter software SWR in loc. 176

0-28K (124K) WORD MEMORY TEST

ABSTRACT :

This diagnostic will test 0-28K, with switch 12=1 0-124kW of MOS or CORE memoryon a PDP (LSI) family computer. Some tests are worst case for MOS and some for core, but all tests are always run. The test occupies less than 2K of memory so it can be used to test a system with only 4kW of memory. This test is not intended to be a 100 % test of the memory. Other tests that do I/O may find memory problems that this test is unable to find.

OPERATING PROCEDURES :

.R ZKMAF0

SWR = 000000 NEW =
Set optional switches

To halt the test, type CONTROL-C, this will insure the program is relocated back to lower memory. Be patient, the CONTROL-C is only recognized at the end
of the current subtest.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on subtest defined by bits <3:0>
SW13= 1 inhibit error typeout
SW12= 1 enable testing above 28K (with memory management)
SW11= 1 enable parity testing
SW10= 1 halt after each subtest
SW09= 1 inhibit program relocation
SW08= 1 type first failing bit error per 4kW
SW07= 1 enable long galloping test
SW06= 1 inhibit memory sizing
SW05= 1 inhibit "PASS #xx" printout
SW04= 1 inhibit printouts
SW03= 1 test number
SW02= 1 test number
SW01= 1 test number
SW00= 1 test number
use "CONTROL G" to enter software SWR in loc. 176

11/60 MOS MEMORY ZMMLC0

11/60 MEMORY DIAGNOSTIC

ABSTRACT :

This diagnostic program runs on PDP11/60 with MF11S-K ECC memory installed. It tests memory from 0 - 124k. There are a lot of 11/60 with MS11-L installed, on which this test does not run error free.

OPERATING PROCEDURES :

.R ZMMLC0

The test prints the CSR address and memory limit
The first pass is a quick one
Wait for the second "END PASS" message

Halt test only by <control C> to be sure no DOUBLE ERROR forced during test is left in the memory.

If there is, and you have battery back up option installed then switch off all (machine and battery circuit breaker) to clear the double bit error.

Set operating switches

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on subtest by SW <3:0>
SW13= 1 inhibit error typeout
SW12= 1 inhibit relocation (testing above 28K)
SW11= 1 enable printouts of single errors (disable ECC)
SW10= 1 halt after each subtest
SW09= 1 inhibit program relocation
SW08= 1 type first uncorrectable error only
SW07= 1 enable XOR printout for array test
SW06= 1 inhibit memory sizing
SW05= 1 inhibit "END PASS #xx" and relocation printouts
SW04= 1 scan memory with ECC disable, no test run
SW03= 1 test #
SW02= 1 test #
SW01= 1 test #
SW00= 1 test #

MOS MEMORY ZMSDD0

MS11-L/M MEMORY TEST

ABSTRACT :

This diagnostic program runs on all PDP11 with memory management and MS11-L and/or MS11-M memory (also mixed). It has special maintenance mode (field service mode) to provide special functional capabilities. It must be on 16K words boundaries starting at 000.

OPERATING PROCEDURES :

.R ZMSDD0

SA = 202 restart address

SWR = 000000 NEW =
Set operating switches

Control "K" = kill error print out and skip pattern
Control "T" = tell me what's happening
Control "F" = enter field service mode
in command mode :99 will print you a help message

0 = EXIT
1 = READ CSR
2 = LOAD CSR
3 = EXAMINE MEMORY
4 = MODIFY MEMORY
5 = SELECT BANK & TEST
6 = TYPE CONFIG MAP
.....

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on subtest
SW13 = 1 inhibit error typeout
SW12 = 1 inhibit relocation
SW11 = 1 inhibit subtest iteration (quick verify)
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 halt program (restore loaders)
SW07 = 1 detailed error reports
SW06 = 1 inhibit configuration map
SW05 = 1 limit max errors per bank
SW04 = 1 fat terminal (132 columns or better)
SW03 = 1 test mode
SW02 = 1 test mode
SW01 = 1 test mode
SW00 = 1 detect single bit errors

MOS MEMORY ZMSPB0

MS11-L/M/P MEMORY TEST

ABSTRACT :

This diagnostic program runs on all 11/24/44's with MS11-L/M/P MOS memory. It has special maintenance mode (field service mode) to provide special functional capabilities. It must be on 16 K words boundaries starting at 000.

OPERATING PROCEDURES :

.R ZMSPB0

SA = 202 restart address

SWR = 000000 NEW =
Set operating switches

Control "K" = kill error print out and skip pattern
Control "T" = tell me what's happening
Control "F" = enter field service mode
in command mode :99 will print you a help message

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on subtest
SW13 = 1 inhibit error typeout
SW12 = 1 inhibit relocation
SW11 = 1 inhibit subtest iteration (quick verify)
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 halt program (restore loaders)
SW07 = 1 detailed error reports
SW06 = 1 inhibit configuration map
SW05 = 1 limit max errors per bank
SW04 = 1 fat terminal (132 columns or better)
SW03 = 1 test mode
SW02 = 1 test mode
SW01 = 1 test mode
SW00 = 1 detect single bit errors

PDP11 CPU ZQKCF0

PDP11 FAMILY INSTRUCTION EXERCISER

ABSTRACT :

This diagnostic program is designed to be a comprehensive check of the PDP11 CPU's (no memory management is tested). The program executes each instruction in all address modes and includes tests for traps and the console interrupt sequence. The program does not test instructions not common to the 11/20 or 11/05. The program relocates the test code throughout memory 0-28k.

OPERATING PROCEDURES :

.R ZQKCF0

Set operating switches
Pass count is printed after each pass
"DZQKC DONE" is printed when done.

SWITCH SETTINGS

SW15= 1 halt on error
SW14= 1 loop on subtest
SW13= 1 inhibit error typeout
SW12= 1 inhibit relocation
SW11= 1 inhibit subtest iteration
SW10= 1 ring bell on error
SW09= 1 not used
SW08= 1 not used
SW07= 1 inhibit end of pass printout

MEMORY ZQMCG3

0-124K WORD MEMORY (not ECC) TEST

ABSTRACT :

This diagnostic program has the ability to test memory from address 000 000 to address 757 777. It does so by using : unique addressing techniques, worse case noise patterns, and instruction execution throughout memory. The smallest unit of memory this program will recognize is 4 kw.There is also a special routine to typeout all unibus address ranges which do not timeout. Core memory as well as MOS memory is tested with or without parity check (for ECC memory use an other test). This test is also not intended to be a 100% test of the memory. Other tests that do I/O may find memory problems that this test is unable to. Optional is : Memory management and parity memory control modules.

OPERATING PROCEDURES :

.R ZQMCG3

SA = 204 conversation mode (enter first and last address)
SA = 210 restart address
SA = 214 restore loader and halt
SA = 220 memory map typeout routine

SWR = 000000 NEW =
Set operating switches

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on subtest
SW13 = 1 inhibit error typeout
SW12 = 1 inhibit memory management (initial start only)
SW11 = 1 inhibit subtest iteration
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR<4:0>
SW07 = 1 inhibit program relocation
SW06 = 1 inhibit parity error detection
SW05 = 1 inhibit exercising vector area (loc 0-1000)

COMMUNICATION, PRINTERS BOOT MODULES, TERMINALS REALTIME CLK, SLAVE CPU's

DHV11	DLV11-J
DMV11	DPV11
DLV11-E	DZV11
DZQ11	DLV11
MXV11-A	MXV11-B
DEQNA	DMP11
DUP11	DH11
DM11	DHU11
DMC11	DL11
KMC11	DMR11
DR11-B	DUP11
DZ11	DR11-C
KMC11-B	KMC11-A
KXJ11-CA	KW11-P
DECSA	LA36
LP11 2310	LN01
LP25/26/27	LP05/11/14
LS11	LP07
DEQNA	M9312
DELUA	DEUNA

DHV-11 M3104 FUNCTIONAL TEST PART 1 OF 3

ABSTRACT :

This is a part of the DHV11 functional verification test. This part of the test verifies that the reset, register access, and interrupt functions of the board are functioning correctly. Normaly it tests all available lines, but if you want only a particular line to be tested then use the active line bit map question (set bit 3 to a one for line 3 in octal to be tested).

OPERATING PROCEDURES :

```
.R VDHAE0

        This program is running under the supervisory program
        This supervisory program will first talk to you
CVDHA-E-0
DHV11-M FUNC TST PART 1
UNIT IS DHV11-M
RSTRT ADR 142060
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
CSR ADDRESS : (O) 160460 ?
INTERRUPT VECTOR ADDRESS : (O) 300 ?
ACTIVE LINE BIT MAP : (O) 377 ?
INTERRUPT BR LEVEL (O) 4 ?

CHANGE SW (L) ? Y

REPORT UNIT NUMBER AS EACH UNIT IS TESTED: (L) Y ?
NUMBER OF INDIVIDUAL DATA ERRORS TO REPORT ON A LINE: (D) 0 ?
ROM VERSION PRINTOUT ON THE FIRST PASS (L) Y ?

ROM VERSION NUMBERS : PROC 1 = 2 (D) PROC 2 = 2 (D)
```

DHV-11 M3104 FUNCTIONAL TEST PART 2 OF 3

ABSTRACT :

This is a part of the DHV11 functional verification test. This part of the test verifies that the major communication functions of the board are functioning correctly. Normaly it tests all available lines, but if you want only a particular line to be tested then use the active line bit map question (set bit 3 to a one for line 3 in octal to be tested).

OPERATING PROCEDURES :

```
.R VDHBE0

        This program is running under the supervisory program
        This supervisory program will first talk to you

CVDHB-E-0
DHV11-M FUNC TST PART 2
UNIT IS DHV11-M
RSTRT ADR 142060
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
CSR ADDRESS : (O) 160460 ?
INTERRUPT VECTOR ADDRESS : (O) 300 ?
ACTIVE LINE BIT MAP : (O) 377 ?
TYPE OF LOOPBACK        1 = INTERNAL
                        2 = H3277
                        3 = H325
                        4 = H3101
                        5 = H3103
                        6 = 70-22629
                        7 = H315B : (O) 2 ?

INTERRUPT BR LEVEL (O) 4 ?

CHANGE SW (L) ? Y

REPORT UNIT NUMBER AS EACH UNIT IS TESTED: (L) Y ?
NUMBER OF INDIVIDUAL DATA ERRORS TO REPORT ON A LINE: (O) ?
```

DHV-11 M3104 FUNCTIONAL TEST PART 3 OF 3

ABSTRACT :

This is a part of the DHV11 functional verification test. This part of the test verifies that the major communication functions of the board are functioning correctly. Normaly it tests all available lines, but if you want only a particular line to be tested then use the active line bit map question (set bit 3 to a one for line 3 in octal to be tested).

OPERATING PROCEDURES :

.R VDHCE0

This program is running under the supervisory program
This supervisory program will first talk to you

CVDHC-E-0
DHV11-M FUNC TST PART 3
UNIT IS DHV11-M
RSTRT ADR 142060
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
CSR ADDRESS : (O) 160460 ?
INTERRUPT VECTOR ADDRESS : (O) 300 ?
ACTIVE LINE BIT MAP : (O) 377 ?
TYPE OF LOOPBACK 1 = INTERNAL
2 = H3277
3 = H325
4 = H3101
5 = H3103
6 = 70-22629
7 = H315B : (O) 2 ?

INTERRUPT BR LEVEL (O) 4 ?

CHANGE SW (L) ? Y

REPORT UNIT NUMBER AS EACH UNIT IS TESTED: (L) Y ?
NUMBER OF INDIVIDUAL DATA ERRORS TO REPORT ON A LINE: (O) ?

DHV-11 M3104 QUICK FUNCTIONAL USER FRIENDLY

ABSTRACT :

This is a function verification test for the DHV11-M, 8 line asynchronous multiplexer. This program has been created for inclusion within the 11/84 User Friendly Diagnostic (UFD). This is a merged program of the following tests: VDHAxx, VDHBxx and VDHCxx. Some code from this three tests got removed which required external loopback or other operator intervention.

OPERATING PROCEDURES :

.R VDHEC0

This program is running under the supervisory program
This supervisory program will first talk to you

CVDHE-C-0
DHV11-M TEST, ORION UFD
UNIT IS DHV11-M
RSTRT ADR 142060
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
CSR ADDRESS : (O) 160460 ?
INTERRUPT VECTOR ADDRESS : (O) 300 ?
INTERRUPT BR LEVEL : (O) 4 ?

DLV11-J LOGIC TEST

ABSTRACT :

This diagnostic program is a logic test to verify the operation of the DLV11-J. Testing is done in two distinct phases: all selected channels per DLV11-J module are tested individually, and secondly the DLV11-J module is tested as a whole for channel interaction problems. This test operates up to 2 DLV11-J serial line interfaces configured at consecutive base addresses. The program will do auto sizing if the device MAP "$DEVM" = 0. The operator must install data wrap around connectors (H3270-A) to do data testing. This diagnostic assumes that the operator has initialized location "$USWR" (user switch register memory loc 001220) and "$DEVM" (device map memory loc. 1252) to the proper values.
Default address 176560 vector 60 for the console
default address 176500 vector 300 for the first serial channel
If your configuration is not standard, write the first RCSR address into memory loc. 1250 (176500 is default) and the vector into memory loc. 1244 (300 is default).

$USWR - memory loc. 1220 - bit interpretation

bit 11-9 console device	*1 = yes console on mod. 1 chan 3* *0 = console not on DLV11-J* *2 = console on module 2*
bit 04 run data wrap around tests	*1 = yes*
bit 03 breake detection enabled	*1 = yes*
bit 02 even or odd parity	*0 = odd*
bit 01 parity enabled	*0 = no*
bit 00 number of data bits transmitted	*1 = 8 bit*

OPERATING PROCEDURES :

.R VDLAB0

This starts the test att address 200 (normal start).

CVDLAB0 DLV11-J TEST

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error print out
SW12 = 1 enable performance reports
SW11 = 1 inhibit iteration
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR <7:0>
SW07 = 1
SW06 = 1
use "CONTROL G" to enter software SWR at loc 176.

DMV-11 MICRO CONTROLLER STATIC DIAG. PART 1

ABSTRACT :

The M8053 and M8064 are single-line synchronous, micro-processor based communications interfaces which can support both character oriented (DDCMP, BSC, ETC) and bit-oriented protocols. This program tests the CSRS, RAM, and basic micro-processor logic on these boards. The M8064 has integral modem.

OPERATING PROCEDURES :

.R VDMAC1

This program is running under the supervisory program
This supervisory program will first talk to you

CVDMA-C-1
DMV-11 U-CONTROL LOGIC DIAG - PART 1 OF 2
UNIT IS M8053 OR M8064
RSTRT ADR 142060
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
DEVICE CSR ADDRESS : (O) 160020 ?
DEVICE VECTOR ADDRESS : (O) 300 ?
DEVICE PRIORITY LEVEL : (O) 4 ?

No software parameters available

DMV-11 MICRO CONTROLLER STATIC DIAG. PART 2

ABSTRACT :

The M8053 and M8064 are single-line synchronous, micro-processor based communications interfaces which can support both character oriented (DDCMP, BSC, ETC) and bit-oriented protocols. This program tests the CSRS, RAM, and basic micro-processor logic on these boards. The M8064 has integral modem.

OPERATING PROCEDURES :

```
.R VDMBC0

        This program is running under the supervisory program
        This supervisory program will first talk to you

CVDMB-C-0
DMV-11 U-CONTROL LOGIC DIAG - PART 2 OF 2
UNIT IS M8053 OR M8064
RSTRT ADR 142060
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
DEVICE CSR ADDRESS : (O) 160020 ?
DEVICE VECTOR ADDRESS : (O) 300 ?
DEVICE PRIORITY LEVEL : (O) 4 ?

IS THE PROCESSOR STRAPPED TO MODE 0 ON POWER-UP (L) Y ?
BOARD TYPE (0=M8064, 1=M8053-EIA) : (O) 0 ?
IS THIS A MANUFACTURING TEST STAND ? (L) N ?

No software parameters available
```

DMV-11 LINE UNIT STATIC DIAG. PART 1

ABSTRACT :

The M8053 and M8064 are single-line synchronous, micro-processor based communications interfaces which can support both character oriented (DDCMP, BSC, ETC) and bit-oriented protocols. This program tests the VIA, FIFO and basic USYRT logic on these boards. The M8064 has integral modem. The line unit is integrated on the same board as the micro-processor is. There are 3 tests to run just for the line-unit part.

OPERATING PROCEDURES :

.R VDMCC1

This program is running under the supervisory program
This supervisory program will first talk to you

CVDMC-C-1
DMV-11 LINE UNIT TESTS - PART 1 OF 3
UNIT IS M8053 OR M8064
RSTRT ADR 142060
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
DEVICE CSR ADDRESS : (O) 160020 ?
DEVICE VECTOR ADDRESS : (O) 300 ?
DEVICE PRIORITY LEVEL : (O) 4 ?

SWITCH PACK #1 (BOOT ADDRESS) : (O) 0 ?
SWITCH PACK #2 ((DDCMP ADDRESS) : (O) 0 ?
BOARD TYPE (0=M8064, 1=M8053-V.35
2=M8053-EIA) : (O) 0 ?
BAUD RATE (0=LOW (19.2) 1=HIGH (56K)) : (O) 1 ?

No software parameters available

DMV-11 LINE UNIT STATIC DIAG. PART 2

ABSTRACT :

The M8053 and/or M8064 are single-line synchronous, micro-processor based communications interfaces which can support both character oriented (DDCMP, BSC, ETC) and bit-oriented protocols. This program tests the line oriented logic on these board. The M8064 has integral modem. The line unit is integrated on the same board as the micro-processor is. There are 3 tests to run just for the line-unit part.

OPERATING PROCEDURES :

.R VDMDC0

This program is running under the supervisory program
This supervisory program will first talk to you

CVDMD-C-0
DMV-11 LINE UNIT TESTS - PART 2 OF 3
UNIT IS M8053 OR M8064
RSTRT ADR 142060
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
DEVICE CSR ADDRESS : (O) 160020 ?
DEVICE VECTOR ADDRESS : (O) 300 ?
DEVICE PRIORITY LEVEL : (O) 4 ?

No software parameters available

DMV-11 LINE UNIT STATIC DIAG. PART 3 OF 3

ABSTRACT :

The M8053 and/or M8064 are single-line synchronous, micro-processor based communications interfaces which can support both character oriented (DDCMP, BSC, ETC) and bit-oriented protocols. This program tests the integral modem and associated logic on these boards. The M8064 has integral modem. The line unit is integrated on the same board as the micro-processor is. There are 3 tests to run just for the line-unit part.

OPERATING PROCEDURES :

```
.R VDMEC0

        This program is running under the supervisory program
        This supervisory program will first talk to you

CVDME-C-0
DMV-11 LINE UNIT TESTS - PART 3 OF 3
UNIT IS M8053 OR M8064
RSTRT ADR 142060
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
DEVICE CSR ADDRESS : (O) 160020 ?
DEVICE VECTOR ADDRESS : (O) 300 ?
DEVICE PRIORITY LEVEL : (O) 4 ?

BOARD TYPE (0=M8064, 1=M8053-V.35,
                    2=M8053-EIA) : (O) 0 ?
TURNAROUND CONNECTOR TYPE-
0=H3254 & H3255, 1=INTEGRAL MODEM CABLE, 2=EIA CABLE
3=V.35 CABLE, 4=NONE : (O) 0 ?

No software parameters available
```

DPV11 M8020 SERIAL SYNCHRONOUS FUNCTIONAL TEST

ABSTRACT :

This program is running under the run-time supervisor. This test can run in 4 different modes, internal loop-back (no loop-back connector needed), RS423 loopback, RS422 loopback, local modem loop and remote modem loop. Internal loopback runs the diagnostic through the USYNRT maintenance mode loopback, the drivers will not be tested. RS423 requires a H3260 onboard connector or the BC05C cable and the H3259 connector.

OPERATING PROCEDURES :

.R VDPVC1

This program is running under the supervisory program.
This supervisory program will first talk to you.

CVDPV-C-1
DIAGNOSTIC TESTS
UNIT IS DPV11
RESTART ADDRESS 142060
DR>STA

CHANGE HW (L) ?

#UNITS (D) ? 1<CR>

UNIT 0
ADDRESS : (O) ? 160010 ?<CR>
VECTOR (O) ? 300<CR>
LOOPBACK-
0 = INTERNAL,
1 = RS423,
2 = RS422,
3 = LOCAL MODEM LOOP,
4 = REMOTE MODEM LOOP (O): 1 ?<CR>

DLV11-E OFF-LINE DIAGNOSTIC

ABSTRACT :

This diagnostic program is a logic test to verify the operation of the DLV11-E. The program has set initialy defaults to all options, except programmable baude rate. This test operates up to 16 identically configured DLV11-E interfaces. The default address of the first interface is 175610, vector 300. If the address is not standard, then the program has to be modified $BASE (175610) is mem. loc. 1250, $VECT1 (300) is mem loc. 1244. The loc $USWR is mem. loc. 1220 and contains all the user selectable options. The default value is (071110).

bit 14 (-FR) and (-FD) jumpers in	*1 = yes*
bit 13 cable terminated (H315)	*1 = yes*
bit 12 breake generation enabled	*1 = yes*
bit 11-8 baud rate offset	*05 = 110 baud*
bit 07 programmable baud rate	*0 = no*
bit 06 common speed	*1 = yes*
bit 05 even or odd parity	*0 = odd*
bit 04 parity enabled	*0 = no*
bit 03-0 #of data bits	*10 = 8*

OPERATING PROCEDURES :

.R VDVAD1

This starts the test att address 200 (normal start).

CVDVA-D DLV11-E OFFLINE TEST

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 scope loop
SW13= 1 inhibit error print out
SW12= 1 not used
SW11= 1 inhibit iteration
SW10= 1 bell on error
SW09= 1 loop on error
SW08= 1 loop on test in SWR <7:0>
SW07= 1
SW06= 1
use "CONTROL G" to enter software SWR at loc 176.

DZV11 M7957 / DZQ11 M3106 DIAG. TEST 1 OF 2

ABSTRACT :

This test verifies the DZV11/DZQ11 operates according to specifications. Parameters may be supplied to the program by either "AUTO SIZING" or input from the user on the console by having SW00 = 1 at start time. Auto sizing will be done the first time the program is started and SW07 = 0, SW00 = 0 and SW03 = 0. For a normal run (auto sizing, all SW = 000 000) no TURN-AROUND connector is needed, it uses the internal maintenance loop. The cables and line drivers can not be tested in this mode.

OPERATING PROCEDURES :

.R VDZAD3

(SWR) = /000000/ = /01 manual mode
normaly you run the auto mode (easy to run) but
I explane here the manual mode

CVDZAD3
FOUR LINE ASYNC MUX TESTS, PART 1 OF 2

1ST CSR ADDRESS-(160000:167770):
VECTOR ADDRESS-(300:770):
MAINTENANCE MODE
[EXTERNAL <H325> (E)]:
[INTERNAL <DZVCSR03 = 1 (I)]:
[STAGGERED <H329> (S)]:

 # OF DZV11'S IN OCTAL (1:20):

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error print out
SW12 = 1 bell on error
SW11 = 1 inhibit iterations
SW10 = 1 escape to next test
SW09 = 1 loop with current data
SW08 = 1 catch error and loop on it
SW07 = 1 no auto size
SW06 = 1 reselect DZV11's desired active
SW04 = 1 select delay parameter
SW03 = 1 extra parameter input
SW02 = 1 lock on selected test
SW01 = 1 restart program at selected test
SW00 = 1 get users parameters from console

DZV11 M7957 / DZQ11 M3106 DIAG. TEST 2 OF 2

ABSTRACT :

This test verifies the DZV11/DZQ11 operates according to specs. Parameters may be supplied to the program by either "AUTO SIZING" or input from the user on the console by having SW00 = 1 at start time. Auto sizing will be done the first time the program is started and SW07 = 0, SW00 = 0 and SW03 = 0. For a normal run (auto sizing, all SW = 000 000) no TURN-AROUND connector is needed, it uses the internal maintenance loop. The cables and line drivers can not be tested in this mode.

OPERATING PROCEDURES :

.R VDZBD0

(SWR) = /000000/ = /01 manual mode
normaly you run the auto mode (easy to run) but
I explane here the manual mode

CVDZBD0
FOUR LINE ASYNC MUX TESTS, PART 2 OF 2

1ST CSR ADDRESS-(160000:167770):
VECTOR ADDRESS-(300:770):
MAINTENANCE MODE
[EXTERNAL <H325> (E)]
[INTERNAL <DZVCSR03 = 1 (I)]
[STAGGERED <H329> (S)]:

 # OF DZV11'S IN OCTAL (1:20):

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error print out
SW12 = 1 bell on error
SW11 = 1 inhibit iterations
SW10 = 1 escape to next test
SW09 = 1 loop with current data
SW08 = 1 catch error and loop on it
SW07 = 1 no auto size
SW06 = 1 reselect DZV11's desired active
SW04 = 1 select delay parameter
SW03 = 1 extra parameter input
SW02 = 1 lock on selected test
SW01 = 1 restart program at selected test
SW00 = 1 get users parameters from console

DZV11 M7957 / DZQ11 M3106 EIA CABLE/ECHO TEST

ABSTRACT :

This test is designed as a non-chainable standalone diagnostic providing the operator with direct control over the testing of all DZV11 EIA cables. Connect a terminal to any line on the DZV11/DZQ11 and type line number on the console and you will get a printout on the connected terminal. After you can type any character on the terminal and the computer via DZV11 will give you the ECHO to test the input circuit. If you do the cable test put a H325 TURN-AROUND connector on a line and select the line number on the console.

OPERATING PROCEDURES :

.R VDZCB1

(SWR) = /000000/ = /
CVDZCB
DZV11 ECHO AND CABLE TESTS

CONTROL REG ADDRESS-160100<CR>
VECTOR ADDRESS-310<CR>
WHICH TEST ECHO OR CABLE (E or C) E<CR>
BAUD RATE-50/75/110/135/150/300/600/1200/18002400/4800/7200 or 9600<CR>
LINE-00<CR>

At this point the message:

THE QUICK BROWN FOX JUMPED OVER THE LAZY DOGS BACK 0123456789

should be printed on the terminal.
The program will then print on the console terminal:

TYPE A CHAR. ON DZV11 terminal

Any printable character which is typed on the DZV11 terminal will be ECHOED back on the terminal.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 not used
SW13 = 1 inhibit error print out
SW12 = 1 bell on error
SW11 = 1 not used
SW10 = 1 escape to the end of pass after an error
SW09 = 1 not used
SW08 = 1 restart the test after an error

DLV11 (M7940) LOGIC TEST

ABSTRACT :

This is a logic test of the DLV11 serial line unit for the LSI-11 computer. This test will operate on the DLV11 without any special test devices by default. However a special wrap module can be used and tested by option. This is a multiple device test which will operate on the console DLV11 addressed at 177560, and up to 8 additional DLV11's with specified addresses. Default address for console : 177560 next 176500.

Remember for 110 baude use 2 stop bits, all other baude rates only 1 stop bit.

OPERATING PROCEDURES :

.R VKAEB2

Set bits in the Software switch reg. in loc. 422
restart program at 200

SWITCH SETTINGS :

SW15= 1 continue on error
SW14= 1 scope loop
SW13= 1 not used
SW12= 1 not used
SW11= 1 not used
SW10= 1 loop on current test
SW09= 1 run wrap test
SW08= 1 set device map manualy
SW07= 1 not used
SW06= 1 not used

MXV11-A LOGIC TEST (2 SLU,ROM's,CLOCK,RAM's)

ABSTRACT :

This diagnostic is a logic test to verify the operation of the 2 Serial Line Units, ROM and clock options, the PCR register and the DDR register and the RAM on the MXV11-A. The program will test to whatever options the device MAP is set to. The program prints the contens of the device MAP for verification. Each of the 2 SLU channels are tested individually. The operator must install data wrap around connectors to do data testing. To bypass data tests, the operator must modify the device MAP.

The default Address and Vectors are as follows:

Channel 0 (SLU) address 776500	*(memory loc. 001254)*
vector 300	*(mem loc. 001256)*
Channel 1 (SLU) address 777560	*(memory loc. 001260)*
vector 60	*(memory loc. 001262)*

OPERATING PROCEDURES :

.R VMXAA0

SWR = 000000 NEW =

DEVM = 000000 NEW = (device map)

bit 15 = 1 (100000) bypass channel 0 test
bit 14 = 1 (040000) 7 bits/word with parity
bit 12 = 1 (010000) even parity (bit = 0 odd parity)
bit 11 = 1 (004000) Break detection enabled channel 0
bit 10 = 1 (002000) bypass data wrap tests channel 0
bit 08 = 1 (000400) test channel 1
bit 07 = 1 (000200) 7 bits/word with parity channel 1
bit 05 = 1 (000040) even parity (bit = 0 odd parity)
bit 04 = 1 (000020) breake detection enabled channel 1
bit 03 = 1 (000010) bypass data wrap tests channel 1
bit 02 = 1 (000004) bypass RAM tests
bit 01 = 1 (000002) bypass ROM testing
bit 00 = 1 (000001) clock option enabled test

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error print out
SW12 = 1 enable performance reports
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR <7:0>
SW07 = 1 test number to loop on
SW00 = 1 test number to loop on
change loc 176 (software SWR) to enter new switches

MXV11-B LOGIC TEST (2 SLU,ROM's,CLOCK,RAM's)

ABSTRACT :

This diagnostic is a logic test to verify the operation of the 2 Serial Line Units, ROM and clock options, the PCR register and the DDR register and the RAM on the MXV11-B. The program will test to whatever options the device MAP is set to. The program prints the contens of the device MAP for verification. Each of the 2 SLU channels are tested individually. The operator must install data wrap around connectors to do data testing. To bypass data tests, the operator must modify the device MAP.

The default Address and Vectors are as follows:

Channel 0 (SLU) address 776500	*(memory loc. 001254)*
vector 300	*(mem loc. 001256)*
Channel 1 (SLU) address 777560	*(memory loc. 001260)*
vector 60	*(memory loc. 001262)*

OPERATING PROCEDURES :

.R VMXBA0

SWR = 000000 *NEW =*

DEVM = 000000 *NEW =* *(device map)*

bit 15 = 1 (100000) bypass channel 0 test
bit 13 = 1 (020000) 2 MXV11B modules for test
bit 12 = 1 (010000) CPU has no Memory Management
bit 11 = 1 (004000) Break detection enabled channel 0
bit 10 = 1 (002000) bypass data wrap tests channel 0
bit 09 = 1 (001000) do data internal-wrap tests
bit 08 = 1 (000400) test channel 1
bit 07 = 1 (000200) bypass PCR register test
bit 06 = 1 (000100) bypass use of LED's
bit 04 = 1 (000020) breake detection enabled channel 1
bit 03 = 1 (000010) do data internal-wrap tests channel 1
bit 02 = 1 (000004) bypass RAM tests
bit 01 = 1 (000002) ROM present, do test
bit 00 = 1 (000001) clock option enabled test

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error print out
SW12 = 1 enable performance reports
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR <7:0>
SW07 - 1 test number to loop on
SW00 = 1 test number to loop on
change loc 176 (software SWR) to enter new switches

DEQNA (M7504) NI EXERCISER DIAGNOSTIC
DELQA (M7516) NI EXERCISER DIAGNOSTIC

ABSTRACT :

The network interconnect exerciser (NIE) program is meant to provide field service with a tool for determining the connectivity of nodes on the network interconnect (NI). The NIE program will determine the ability of nodes on the NI to communicate with each other and provide node installation verification and problem isolation. The NIE uses the low level maintenance features of the DEQNA/DELQA to provide testing without interrupting normal operation of the NI. The VAX version of the NIE can also be run conncurrently on another node, with each version running independently of each other.

OPERATING PROCEDURES :

.R VNIA??

This program is running under the supervisory program.
This supervisory program will first talk to you.

CVNIA-D-0
CVNIAD0 DEQNA, DELQA NI EXERCISER
UNIT IS DEQNA
RSTRT ADR 142060
DR>START

CHANGE HW (L) ? Y

#UNITS (D) ? 1<CR>
UNIT 0
DEVICE CSR ADDRESS? (O) ? 174440<CR>
INTERRUPT VECTOR ADDRESS? (O) ? 700<CR>
INTERRUPT PRIORITY LEVEL ? (O) 5 ?
this is a standard address and vector.

NIE>
now you are in a command mode, you can type
NIE> (A) ? HELP
with this command you will get the help text
below is a example of usefull commands
NIE> (A) CLEAR NODE/ALL
NIE> (A) BUILD
NIE> (A) SHOW NODES
NIE> (A) RUN TEST/PASS=nn *TEST=DIRECT, LOOPPAIR or PATTERN*
NIE> (A) SHOW COUNTERS
NIE> (A) SUMMARY

DMP11, DMV11 DATA COMMUNICATION LINK TEST

ABSTRACT :

This DCLT (data com link test) is meant to provide field service with a tool to maintain DMP11, DMV11 to DDCMP multipoint communication links. This program will provide the coverage necessary to detect failures to the computer equipment, the communication link, or the modem.

OPERATING PROCEDURES :

This program is running under the supervisory program.
This supervisory program will first talk to you.

```
.R ZCLMC0

CZCLM-C-0
CZLMC0 DMP DMV-11 DATA COMM. LINK TEST
UNIT IS DMP OR DMV 11
RSTRT ADR 145702
DR>START

CHANGE HW (L) ? Y

#UNITS (D) ? 1<CR>
UNIT 0
FULL DUPLEX OPERATION: (L) Y ?
DEVICE CSR ADDRESS : (O) 160170
INTERRUPT VECTOR ADDRESS: (O) 300 ?
INTERRUPT PRIORITY : (O) 5 ?
OPTION TYPE 0=DMP, 1=DMV : (O) 1
IS THIS MULTIPOINT NETWORK: (L) N ?
IS THIS A CONTROL STATION: (L) N ?

THIS IS DCLT. TYPE "H" OR "?" FOR DETAILS
        MODE=ACTIVE/PASS=0001
             /NOSTATUS/CHECK/NOECHO/NOMODEM/NOPROTOCOL

DCLT> (A) ?              now you are in command mode, you can type
DCLT> (A) ? H<CR>        this will print a help text
                         below is a example of usefull commands
DCLT> (A) CLEAR EXPECTLIST
DCLT> (A) SET EXPECTMSG=1ALT
DCLT> (A) SHOW EXPECTLIST
DCLT> (A) SHOW TRANSMITLIST

DCLT> (A) RUN MODE=ACTIVE
                  MODE=RECEIVE
                  MODE=TRANSMIT
                  MODE=TALK
                  MODE=LISTEN
DCLT> (A) PRINT          gets you to report level prompt RPT>
RPT> H                   get help
```

DUP11 DATA COMMUNICATION LINK TEST

ABSTRACT :

This DCLT (data com link test) is meant to provide field service with a tool to maintain DUP11 communication links. This program allows the DUP11 to communicate with other synchronous (including DDCMP) devices on point to point or multidrop networks. This DCLT program will provide the coverage necessary to detect failures to the computer equipment, the communication link, or the modem.

OPERATING PROCEDURES :

This program is running under the supervisory program.
This supervisory program will first talk to you.

```
R ZDCLB0

CZDCL-B-0
DUP-11 DATA COMM LINK TEST
UNIT IS DUP-11
RSTRT ADR 145702
DR>START

CHANGE HW (L) ? Y

#UNITS (D) ? 1<CR>
UNIT 0
FULL DUPLEX OPERATION: (L) Y ?
DEVICE CSR ADDRESS : (O) 160170 ?
INTERRUPT VECTOR ADDRESS: (O) 300 ?
REMOTE NODE "ITEP": (L) N ?
IS THIS A MULTIPOINT NETWORK: (L) N ?
ADDRESS THIS STATION: (D) 1 ?

THIS IS DCLT. TYPE "H" OR "?" FOR DETAILS
      MODE=ACTIVE/PASS=0001
           /NOSTATUS/CHECK/NOECHO/NOMODEM/NOPROTOCOL

DCLT> (A) ?              now you are in command mode, you can type
DCLT> (A) ? H<CR>        this will print a help text
                         below is a example of usefull commands
DCLT> (A) CLEAR EXPECTLIST
DCLT> (A) SET EXPECTMSG=1ALT
DCLT> (A) SHOW EXPECTLIST
DCLT> (A) SHOW TRANSMITLIST
DCLT> (A) RUN MODE=ACTIVE
                 MODE=RECEIVE
                 MODE=TRANSMIT
                 MODE=TALK
                 MODE=LISTEN
DCLT> (A) PRINT          gets you to report level prompt RPT>
RPT> H                   get help
```

DH11 STATIC LOGIC TEST

ABSTRACT :

The DH11 static logic test is designed to provide a means for testing the correct function of all read/write bits in the following DH11 registers: DH11 system control register, DH11 line parameter register, DH11 break control register, DH11 silo status register. In addition, tests are provided to check the function of those bits that are read only in maintenance mode. This test does not need a TURN-AROUND connector.

OPERATING PROCEDURES :

.R ZDHAD0

This starts the test at address 200 (normal start).

The program will type:

DH11 STATIC LOGIC TEST
VECTOR ADDRESS-
CONTROL REGISTER ADDRESS-

R *indicating run state*

CZDHA-D0 *is end of pass message*

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 scope loop
SW13 = 1 inhibit error print out
SW12 = 1
SW11 = 1 inhibit iteration
SW10 = 1 escape to next test on error
SW09 = 1 freeze variable parameter in current test
SW08 = 1
SW01 = 1 start program at selected test
SW00 = 1 change parameters at program restart

DH11 MEMORY TEST

ABSTRACT :

The DH11 memory test is a test of the byte count and bus address memories of the DH11. Each memory is tested for addressability and data read/write capability. No TURN-AROUND connector is needed.

OPERATING PROCEDURES :

.R ZDHBC0

This starts the test at address 200 (normal start).
The program will type:

DH11 MEMORY TEST

VECTOR ADDRESS-
CONTROL REGISTER ADDRESS-

R — *indicate run state*

CZDHB-C0 — *is end of pass message*

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 scope loop
SW13 = 1 inhibit error print out
SW12 = 1
SW11 = 1 inhibit iteration
SW10 = 1 escape to next test on error
SW09 = 1 freeze variable parameter in current test
SW08 = 1
SW01 = 1 start program at selected test
SW00 = 1 change parameters at program restart

DH11 TRANSMITTER AND RECEIVER TEST

ABSTRACT :

The DH11 transmitter and receiver logic test checks the basic transmitter and receiver functions. Functions tested include interrupts, operation of transmitter NPR logic, and operation of receiver silo logic. NO TURN-AROUND connector is needed.

OPERATING PROCEDURES :

.R ZDHCC0

This starts the test at address 200 (normal start).

The program will type:

DH11 TRANSMITTER AND RECEIVER LOGIC TEST

VECTOR ADDRESS-
CONTROL REGISTER ADDRESS-

R	*indicate run state*
CZDHC-C0	*is end of pass message*

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 scope loop
SW13 = 1 inhibit error print out
SW12 = 1
SW11 = 1 inhibit iteration
SW10 = 1 escape to next test on error
SW09 = 1 freeze variable parameter in current test
SW08 = 1
SW01 = 1 start program at selected test
SW00 = 1 change parameters at program restart

DH11 SPEED SELECTION LOGIC TEST

ABSTRACT :

The DH11 speed selection logic test verifies that the speed selection functions of the line parameter register operate properly for each transmitter and receiver line. Transmitter timing is checked first, and then receiver timing is tested. The program uses a relative timing comparison to determine if line speed selection is correct. No TURN-AROUND connector is needed.

OPERATING PROCEDURES :

.R ZDHDD0

This starts the test at address 200 (normal start).
The program will type:

DH11 SPEED SELECTION LOGIC TEST

VECTOR ADDRESS- *enter vector*
CONTROL REGISTER ADDRESS- *enter CSR addree*
R indicates run state
006222 NO CLOCK
LINE SPEED
00 01
00 02
..
01 01
01 02
01 03

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 scope loop
SW13 = 1 inhibit error print out
SW12 = 1
SW11 = 1 inhibit iteration
SW10 = 1 escape to next test on error
SW09 = 1 freeze variable parameter in current test
SW08 = 1
SW01 = 1 start program at selected test
SW00 = 1 change parameters at program restart

DM11 MODEM CONTROL MULTIPL. TEST

ABSTRACT :

The DM11 diagnostic tests the modem control multiplexer used with the DH11 (and others) and consists of 4 groups of tests.
GROUP 0 - all line scaner and line mux functions are tested (no test connector)
GROUP 1 - a single line is tested using modem cable and a H315 test connector.
GROUP 2 - connect-disconnect test for 103A modems
GROUP 3 - connect-disconnect test for 202C modems

OPERATING PROCEDURES :

.R ZDHKF0

This starts the test at address 200 (normal start).
The program will type:

CZDHK MODEM CONTROL DIAGNOSTIC

SWR = 000000 NEW = 000001

type 001 to enter vector and address

VECTOR ADDRESS :
CONTROL REGISTER ADDRESS :

LINE SELECT PARAMETER :
select line (modem) 001 = line 0, 002 = line 1, 004 = line 2
010 = line 3, 1000 = line 9 (each bit represents a line)
177777 = select all lines
TEST : type test-group (0-3)

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error print out
SW12 = 1
SW11 = 1 inhibit iteration
SW10 = 1 escape to next test on error
SW09 = 1 freeze data
SW01 = 1 start program at selected test
SW00 = 1 change parameters at program restart

DH11 COMPREHENSIVE DIAGN. TEST

ABSTRACT :

The DH11 comprehensive diagnostig test is replacing the older ZDHAxx... to ZDHKxx. It consists of 48 logically sequenced tests. The program is configurable by the autosizer or by console dialogue to test all 16 lines. Individual lines within a DH11 may be selected or deselected for testing. Whenever an error is detected a comprehensive error report is typed that allows the user to isolate the fault to a functional area of logic. Test 101 and 105 through 107 (test group 1) of the modem control diagn. ZDHKxx have been included in this program. In this way all the level converters and cables can be checked with just one program using the H315 turnaround connector.

OPERATING PROCEDURES :

.R ZDHMD2

This starts the test at address 200 (normal start).
set the SWR = 000000 worst case testing
set the SWR = 000002 to type the device map
set the SWR = 004000 for a quick pass
set the SWR = 002000 to skip modem control test

The program will type:

CZDHM-D-0 DH11 DIAGNOSTIC
with SWR = 000001 it will ask you :
TYPE NO. OF ADDRESSES (OCTAL) BETWEEN VECTORS (10 OR 20)
TYPE SCR ADDRESS FOR FIRST DH11 160020
TYPE VECTOR ADDRESS FOR FIRST DH11 330
TYPE DH11 DEVICE SELECTION PARAMETER (which DH11)
TYPE LINE SELECTION PARAMETER (which line)

TESTING DH11 #00

Without TURN-AROUND-CONNECTOR test 42 and futher will fail

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 scope loop
SW13 = 1 inhibit error print out
SW12 = 1
SW11 = 1 inhibit iteration
SW10 = 1 inhibit modem control tests
SW09 = 1 lock on hard error
SW08 = 1 run test in SWR <07:00>
SW01 = 1 type device map generated by the autosizer
SW00 = 1 manual parameter entry

DH11 DATA RELIABILITY TEST

ABSTRACT :

This DH11 diagnostic consists of three sub-programs. Sub-program 1 is the data reliability test. It can test up to 16 DH11 one after the other, using all combinations of line parameters (baude rate, character length, parity etc.). All errors detected are reported on the console device as they occure and also logged in error statistics tables. Sub-program 2 is a single line echo test, able to test any line by using an terminal connected to this line and Sub-program 3 is a data pattern/cable test using an H315 test connector on the line under test.

OPERATING PROCEDURES :

.R ZDHND0

This starts the test at address 200 (normal start).

This will run Sub-program 1 and will test all lines on all DH11 found
set the SWR = 000200 worst case testing
set the SWR = 000002 to type the device map

To run the Sub-prgram 2 start program at address 214
If you start the program with SWR = 000001 you get into console dialog.
enter number of addresses between vectors, device address, vector,
enter which DH11 to select (in binary, 001 = DH11 #00)
enter which line to select (in binary, 005 = line #0 and 2

To run the Sub-program 3 start program at address 220

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on currently selected DH11
SW13 = 1 inhibit printout
SW09 = 1 halts after configuration to permit printing preconfig. map
SW08 = 1 perform a standard pass (with iterations)
SW01 = 1 type device map
SW00 = 1 allow user to input parameters

FUNCTIONAL VERIFICATION TEST 1

ABSTRACT :

This diagnostic is part one of the DHU11 functional verification test. This tests the reset, selftest, register address, BMP code and interrupt functions of the board. This test does not need a TURN-AROUND connector.

OPERATING PROCEDURES :

```
.R ZDHUB0
        This program is running under the supervisory program
        This supervisory program will first talk to you
CZDHU-B-0
DHU-11 FUNC TST PART1
UNIT IS DHU-11
RSTRT ADR 145702
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
CSR ADDRESS : (0) 160460 ?
INTERRUPT VECTOR ADDRESS: (O) 310 ?
ACTIVE LINE BIT MAP: (O) 177777 ?
INTERRUPT BR LEVEL: (O) 5 ?

CHANGE SW (L) ? Y

REPORT UNIT NUMBER AS EACH UNIT IS TESTED: (L) Y ?
ROM VERSION PRINTOUT ON THE FIRST PASS: (L) Y ?
EXTENDED ERROR REPORTING: (L) N ?
NUMBER OF INDIVIDUAL DATA ERRORS TO REPORT ON A LINE: (D) 0 ?
```

FUNCTIONAL VERIFICATION TEST 2

ABSTRACT :

This diagnostic is part two of the DHU functional verification test. This tests the basic and major comunication functions of the board. This program does not perform extensive data transmitssion and reception tests.

OPERATING PROCEDURES :

```
.R ZDHVB0
                This program is running under the supervisory program
                This supervisory program will first talk to you
CZDHV-B-0
DHU-11 FUNC TST PART 2
UNIT IS DHU-11
RSTRT ADR 145702
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
CSR ADDRESS : (0) 160460 ?
INTERRUPT VECTOR ADDRESS: (O) 310 ?
ACTIVE LINE BIT MAP: (O) 177777 ?
TYPE OF LOOPBACK (1=INTERNAL, 2=H3029 or H3277): (O) 2 ?

CHANGE SW (L) ? Y

REPORT UNIT NUMBER AS EACH UNIT IS TESTED: (L) Y ?
EXTENDED ERROR REPORTING: (L) N ?
```

FUNCTIONAL VERIFICATION TEST 3

ABSTRACT :

This diagnostic is part three of the DHU functional verification test. This tests the modem control signals of the board. This program does not perform extensive data transmitssion and reception tests.

OPERATING PROCEDURES :

```
.R ZDHWB0
        This program is running under the supervisory program
        This supervisory program will first talk to you
CZDHW-B-0
DHU-11 FUNC TST PART 3
UNIT IS DHU-11
RSTRT ADR 145702
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
CSR ADDRESS : (0) 160460 ?
ACTIVE LINE BIT MAP: (O) 177777 ?
TYPE OF LOOPBACK (1=INTERNAL, 2=H3029 or H3277): (O) 2 ?

CHANGE SW (L) ? Y

REPORT UNIT NUMBER AS EACH UNIT IS TESTED: (L) Y ?
EXTENDED ERROR REPORTING: (L) N ?
NUMBER OF INDIVIDUAL DATA ERRORS TO REPORT ON A LINE: (D) 0 ?
```

FUNCTIONAL VERIFICATION TEST 4

ABSTRACT :

This diagnostic is part four of the DHU functional verification test. This tests extensively data transmition and reception. This program also includes a keyboard echo and modem loopback test.

OPERATING PROCEDURES :

.R ZDHXA1

This program is running under the supervisory program
This supervisory program will first talk to you

CZDHX-A-0
DHU-11 FUNC TST PART 4
UNIT IS DHU-11
RSTRT ADR 145702
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
CSR ADDRESS : (0) 160460 ?
INTERRUPT VECTOR ADDRESS: (O) 310 ?
ACTIVE LINE BIT MAP: (O) 177777 ?
TYPE OF LOOPBACK (1=INTERNAL, 2=H3029 or H3277), 3=H325
4=MODEM, 5=KEYBOARD ECHO): (O) 2 ?

CHANGE SW (L) ? Y

REPORT UNIT NUMBER AS EACH UNIT IS TESTED: (L) Y ?
REPORT NUMBER OF BITS TESTED IN DMA ADDR TEST: (L) N ?
EXTENDED ERROR REPORTING: (L) N ?
NUMBER OF INDIVIDUAL DATA ERRORS TO REPORT ON A LINE: (D) 0 ?

DL11-E, C/D OFF-LINE DIAGNOSTIC

ABSTRACT :

Two separate diagnostic programs are provided for the DL11-E, ZDLA?? DL11-E off line tests and ZDLB?? DL11-E on-line tests. The off line tests test all DL11-E logic and may be used to individually test up to 31 DL11-E's. The off line tests do not require a modem, however a special jumper connector is required (H325). For the on-line test you need a modem and a suitable terminal device. The DL11-C and DL11-D can also be tested with this offline test. This are both tested in maintenance mode (no turn-around). There are five DL11's : A,B,C,D and E.

DL11-A is 20 mA current loop	*M7800 YA*
DL11-B is EIA RS232C	*M7800*
DL11-C is a more flexible DL11-A (20mA)	*M7800*
DL11-D is a more flexible DL11-B (EIA)	*M7800*
DL11-E is with full modem control (EIA)	*M7800*

OPERATING PROCEDURES :

.R ZDLAH0

This starts the test att address 200 (normal start).
Restart address is 204.

TYPE PROGRAM NUMBER = 0

0 = input/ouput logic tests
1 = transmitter scope loop
2 = receiver scope loop
3 = single character maint. mode data test
4 = special binary count maint. mode data test

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 scope loop
SW13 = 1 inhibit error print out
SW12 = 1 select line number and lock on it
SW11 = 1 inhibit iteration
SW10 = 1 halt at end of current test
SW09 = 1 loop on selected routine
SW08 = 1
SW07 = 1 disable stall mode
SW06 = 1 routine to be run (if enabled by SW 09)
SW05 = 1 routine to be run (if enabled by SW 09)
SW04 = 1 routine to be run (if enabled by SW 09)
SW03 = 1 routine to be run (if enabled by SW 09)
SW02 = 1 routine to be run (if enabled by SW 09)
SW01 = 1 routine to be run (if enabled by SW 09)
SW00 = 1 routine to be run (if enabled by SW 09)

use "CONTROL G" to enter software SWR at loc 176.

DL11-W / 11/44 MFU-SLU TEST

ABSTRACT :

This is a logic test for the DL11-W as well as the 11/44 MFU-SLU (serial line unit). The test can optionaly check transmit and receive signals with a H325 turnaround connector (SW 07= 1). This test is mainly for the console serial line and line clock interface, but can test up to 15 additional identically configured DL11 interfaces. Console address 177560 vector 60, line-clock address 177546 vector 100, additional DL11 address 176500 vector 300. The test is able to handle power fails. The ECHO test (start at 204) reads a character from terminal and writes it back and reports any error. Type "CONTROL C" to stop the ECHO test.

OPERATING PROCEDURES :

.R ZDLDI0

This starts the test att address 200 (normal start).
Start address 204 will execute the ECHO test.
Start address 210 will execute the terminal output test.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error print out
SW12= 1 not used
SW11= 1 not used
SW10= 1 enable error flags tests
SW09= 1 loop on error
SW08= 1 enable BREAK function tests
SW07= 1 run datatest through loop-back connector
SW06= 1 halt in ROMCLK routine before clocking micro-proc.
SW05= 1 inhibit lineclock test
SW04= 1 allow manual setting of DEVICE MAP
SW03= 1 inhibit SLU test (test only line clock)
SW02= 1 for 11/44 enable BREAK and ERROE FLAG test (SW 8 & 10 on)
SW01= 1 11/44 select auto initiation of T/A test via turn around cable
SW00= 1

use "CONTROL G" to enter software SWR at loc 176.

ZDLDC0 this test needs modification for the 11/44
ZDLDD0 does not alow vectors greater then 376
ZDLDE0 has several timing problems on 11/44
ZDLDG0 needs correction for 11/24
ZDLDH0 the terminal output test did not check for XON - XOFF

DMC11 BASIC R/W and MICRO-PROC. TEST

ABSTRACT :

This program tests the DMC11 micro-processor (M8200-YA or M8200-YB). It performs write/read tests on the DMC Unibus registers, checks the micro-processor operation and its memory, exercises NPR's into main memory. It does not require a line-unit. This test runs on a KMC11 (M8204) however it is not advised that this diagnostic be used to check a KMC11, rather you should check a KMC11 with the KMC11 diagnostic package. There are five off line diagnostics that are to be run in sequence to insure that if an error should occure it will be detected at an early stage : ZDMC??, ZDME??, ZDMF??, ZDMG?? and ZDMH??.

OPERATING PROCEDURES :

.R ZDMCD0

this, with all switches down, will do a "AUTO SIZING"
with SWR bit 0=1 will do manual input (questions)
with SWR bit 7=1 will use existing parameters from previous DMC11 diagnostic runs.

in manual mode it will ask:

HOW MANY DMC11's TO BE TESTED ? 1<CR>
01
CSR ADDRESS ? 160010<CR>
VECTOR ADDRESS? 310<CR>
BR PRIORITY LEVEL ? (4,5,6,7) ? 5<CR>
DOES MICRO-PROCESSOR HAVE CRAM? (Y OR N) N<CR>
WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1",
IF M8202 TYPE "2" ? 1<CR>
IS THE LOOP BACK CONNECTOR ON ? Y<CR>
SWITCH PAC#1 (DDCMP LINE#) ? 377<CR>
SWITCH PAC#2 (BM873 BOOT ADD) ? 377<CR>

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error print out
SW12= 1 bell on error
SW11= 1 inhibit iterations
SW10= 1 escape to next test on error
SW09= 1 loop with current data
SW08= 1 catch error and loop on it
SW07= 1 use previous parameter table
SW06= 1 halt in ROMCLK routine before clocking micro-proc.
SW05= 1
SW04= 1
SW03= 1 reselect DMC11's desired active
SW02= 1 lock on selected test
SW01= 1 restart program at selected test
SW00= 1 build new status table from questiuons

DMC11 LINE UNIT TEST (M8201/M8202) 1

ABSTRACT :

This program tests the DMC11-AR and DMC11-AL line unit. It performs write/read tests on the DMC line unit registers. It checks for proper transmitter, receiver, and BCC operation in DDCMP mode. The modem signals are also checked. This test requires a DMC micro-processor (M8200 or M8204) to run. For best diagnosis a turn-around connector should be installed, however the diagnostic will run without it (some tests are skipped). There are five off line diagnostics that are to be run in sequence to insure that if an error should occure it will be detected at an early stage : ZDMC??, ZDME??, ZDMF??, ZDMG?? and ZDMH??.

OPERATING PROCEDURES :

.R ZDMED2

this, with all switches down, will do a "AUTO SIZING"
with SWR bit 0=1 will do manual input (questions)
with SWR bit 7=1 will use existing parameters from previous DMC11 diagnostic runs.

in manual mode it will ask:

HOW MANY DMC11's TO BE TESTED ? 1<CR>
01
CSR ADDRESS ? 160010<CR>
VECTOR ADDRESS? 310<CR>
BR PRIORITY LEVEL ? (4,5,6,7) ? 5<CR>
DOES MICRO-PROCESSOR HAVE CRAM? (Y OR N) N<CR>
WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1",
IF M8202 TYPE "2" ? 1<CR>
IS THE LOOP BACK CONNECTOR ON ? Y<CR>
if the answer was "Y" and M8201, you have to enter modem type
SWITCH PAC#1 (DDCMP LINE#) ? 377<CR>
SWITCH PAC#2 (BM873 BOOT ADD) ? 377<CR>

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error print out
SW12 = 1 bell on error
SW11 = 1 inhibit iterations
SW10 = 1 escape to next test on error
SW09 = 1 loop with current data
SW08 = 1 catch error and loop on it
SW07 = 1 use previous parameter table
SW06 = 1 halt in ROMCLK routine before clocking micro-proc.
SW05 = 1
SW04 = 1
SW03 = 1 reselect DMC11's desired active
SW02 = 1 lock on selected test
SW01 = 1 restart program at selected test
SW00 = 1 build new status table from questions

DMC11 LINE UNIT TEST (M8201/M8202) 2

ABSTRACT :

This program tests the DMC11-AR and DMC11-AL line unit. It performs write/read tests on the DMC line unit registers. It checks for proper transmitter, receiver, and BCC operation in bit stuff mode. The modem signals are also checked. This test requires a DMC micro-processor (M8200 or M8204) to run. For best diagnosis a turn-around connector should be installed, however the diagnostic will run without it (some tests are skipped). There are five off line diagnostics that are to be run in sequence to insure that if an error should occure it will be detected at an early stage : ZDMC??, ZDME??, ZDMF??, ZDMG?? and ZDMH??.

OPERATING PROCEDURES :

.R ZDMFC2

this, with all switches down, will do a "AUTO SIZING"
with SWR bit 0=1 will do manual input (questions)
with SWR bit 7=1 will use existing parameters from previous DMC11 diagnostic runs.

in manual mode it will ask:
HOW MANY DMC11's TO BE TESTED ? 1<CR>
01
CSR ADDRESS ? 160010<CR>
VECTOR ADDRESS? 310<CR>
BR PRIORITY LEVEL ? (4,5,6,7) ? 5<CR>
DOES MICRO-PROCESSOR HAVE CRAM? (Y OR N) N<CR>
WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1",
IF M8202 TYPE "2" ? 1<CR>
IS THE LOOP BACK CONNECTOR ON ? Y<CR>
if the answer was "Y" and M8201, you have to enter modem type
SWITCH PAC#1 (DDCMP LINE#) ? 377<CR>
SWITCH PAC#2 (BM873 BOOT ADD) ? 377<CR>

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error print out
SW12= 1 bell on error
SW11= 1 inhibit iterations
SW10= 1 escape to next test on error
SW09= 1 loop with current data
SW08= 1 catch error and loop on it
SW07= 1 use previous parameter table
SW06= 1 halt in ROMCLK routine before clocking micro-proc.
SW05= 1
SW04= 1
SW03= 1 reselect DMC11's desired active
SW02= 1 lock on selected test
SW01= 1 restart program at selected test
SW00= 1 build new status table from questiuons

DMC11-AR/AL ZDMGD0

DMC11 CROM & JUMP TST

ABSTRACT :

This program tests the DMC11-AR and DMC11-AL micro-processors (M8200-YA, M8200-YB). It performs jump tests on the micro-processor and verifies the control ROM of the M8200. This diagnostic will not run on a KMC11 (M8204), however it is possible to load the KMC CRAM with the DMC micro-code. See test 2 for details. There are five off line diagnostics that are to be run in sequence to insure that if an error should occure it will be detected at an early stage: ZDMC??, ZDME??, ZDMF??, ZDMG?? and ZDMH??. Parameters must be set up to alert the diagnostics to the DMC11 configuration.

OPERATING PROCEDURES :

.R ZDMGD0

this, with all switches down, will do a "AUTO SIZING"
with SWR bit 0=1 will do manual input (questions)
with SWR bit 7=1 will use existing parameters from previous DMC11 diagnostic runs.

in manual mode it will ask:

HOW MANY DMC11's TO BE TESTED ? 1<CR>
01
CSR ADDRESS ? 160010<CR>
VECTOR ADDRESS? 310<CR>
BR PRIORITY LEVEL ? (4,5,6,7) ? 5<CR>
DOES MICRO-PROCESSOR HAVE CRAM? (Y OR N) N<CR>
WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1",
IF M8202 TYPE "2" ? 1<CR>
IS THE LOOP BACK CONNECTOR ON ? Y<CR>
SWITCH PAC#1 (DDCMP LINE#) ? 377<CR>
SWITCH PAC#2 (BM873 BOOT ADD) ? 377<CR>

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error print out
SW12 = 1 bell on error
SW11 = 1 inhibit iterations
SW10 = 1 escape to next test on error
SW09 = 1 loop with current data
SW08 = 1 catch error and loop on it
SW07 = 1 use previous parameter table
SW06 = 1 halt in ROMCLK routine before clocking micro-proc.
SW05 = 1
SW04 = 1
SW03 = 1 reselect DMC11's desired active
SW02 = 1 lock on selected test
SW01 = 1 restart program at selected test
SW00 = 1 build new status table from questiuons

DMC11 FREE RUNNING TESTS

ABSTRACT :

This program tests the DMC11-AR (M8200-YA) and DMC11-AL (M8200-YB) or the KMC11 micro-processor (M8204). A line unit (M8201 or M8202) must be installed. Currently there are five off line diagnostics that are to be run in sequence to insure that if an error should occure it will be detected at an early stage: ZDMC??, ZDME??, ZDMF??, ZDMG?? and ZDMH??. Parameters must be set up to alert the diagnostics to the DMC11 configuration. These parameters are contained in the status table and are generated in two ways: 1. manual input - the operator answers questions. 2. autosizing - the program determines the parameters automaticaly.

OPERATING PROCEDURES :

.R ZDMHC1

this, with all switches down, will do a "AUTO SIZING"
with SWR bit 0=1 will do manual input dialog (questions)
with SWR bit 7=1 will use existing parameters from previous DMC11 diagnostic runs.

in manual mode it will ask:

HOW MANY DMC11's TO BE TESTED ?
CSR ADDRESS ?
VECTOR ADDRESS ?
BR PRIORITY LEVEL? (4,5,6,7) ?
IF DMC HAS CRAM (8204) TYPE "Y", IF CROM (M8200) TYPE "N" ?
DMC11-AR(REMOTE,L.SPEED)OR DMC11-AL(LOCAL,H.SPEED)TYPE "R" or "L"?
WHICH LU? IF NONE TYPE "N", IF M8201 TYPE "1", IF M8202 TYPE "2" ?
IS THE LOOP BACK CONNECTOR ON ?
SWITCH PAC#1 (DDCMP LINE #) ? (0-377)
SWITCH PAC#2 (BM873 BOOT ADD) ? (0-377)

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error print out
SW12 = 1 bell on error
SW11 = 1 inhibit iterations (quick pass)
SW10 = 1 escape to next test on error
SW09 = 1 loop with current data
SW08 = 1 cach error and loop on it
SW07 = 1 use previous status table
SW06 = 1 halt in ROMCLK routine before clocking micro-proc.
SW03 = 1 reselect DMC11's desired active
SW02 = 1 lock on selected test
SW01 = 1 restart program at selected test
SW00 = 1 build new status table from questions.

DMR11 FUNCTIONAL DIAGNOSTIC

ABSTRACT :

It is advised that the static diagnostic be run before these functional diagnostics. It is assumed that the processor is in proper working condition. Ensure that the swich 1 at location E-85 on the M8207 is on. If this switch is off, the maintenance bits in BSEL1 can't be used and certain tests will not be correctly run. When choosing a cable test connection, ensure that the switch pack E-39 on the M8203 is properly set up for the desired interface. If chosing test configuration option 1-4, it is not necessary to select the interface; however the baud rate must be correct. For example to run config. 3 (H3255-EIA) it is nessary to have the baud rate to be within the EIA range.

OPERATING PROCEDURES :

```
.R ZDMID3
                This program is running under the supervisory program
                This supervisory program will first talk to you
CZDMI-D-0
DMR 11 FUNCTIONAL TESTS
UNIT IS DMR11
RSTRT ADR 145702
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
CSR ADDRESS: (O) 160170 ?
VECTOR ADDRESS: (O) 300 ?
TEST CONFIGURATION
0 = INTERNAL (NO CONNECTOR)
1 = H3254 V.35                  (NOTE: MODE 1-4 ALLOWS
2 = H3254 - INTEGRAL            PROGRAM INTERFACE SELECTION)
3 = H3255 - RS232C/423
4 = H3255 - RS422
5 = CABLE AND SW PACK INTERFACE SELECTED
        (V.35-H3250, RS232C-H325, RS423/422-H3251)
        INTEGRAL-BC55A-10,

* SELECT THE FOLLOWING ONLY IF THE MODEM SUPPORTS LOOPBACK *
6 = LOCAL LOOP
7 = REMOTE LOOP
(O) 5 ?

CHANGE SOFTWARE (L) ? N
```

DMP/DMR/DMC/KMC11 M8200/04/07 MICROPROCESSOR TEST 1

ABSTRACT :

This program tests M8200, M8204 or M8207 microprocessor. It is the first of two diagnostics for these options. The M820x microprocessor uses an eight bit data path with a sixteen bit instruction memory. The instruction memory and data memory are two separate memories. The microprocessor is designed for moving data at high rates to work as a high speed link between processors when used with a line unit. The M8200 and M8207 have PROM instruction memories. The M8204 has writable control store. The memory size between all three processors vary also.

OPERATING PROCEDURES :

```
.R ZDMPD0
        This program is running under the supervisory program
        This supervisory program will first talk to you
CZDMP-D-0
M8207 DIAG. #1 OF 2
UNIT IS M8200,M8204,OR M8207
RSTRT ADR 145702
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
WHICH MICRO-CPU? (0=M8200, 4=M8204, 7=M8207 (O) 7 ?
MICRO-CPU CSR ADDRESS : (O) 160170 ?
MICRO-PROCESSOR VECTOR ADDRESS : (O) 300 ?
MICRO-PROCESSOR PRIORITY LEVEL : (O) 5 ?

No software parameters available
```

DMP/DMR/DMC/KMC11 M8200/04/07 MICROPROCESSOR TEST 2

ABSTRACT :

This program tests M8200, M8204 or M8207 microprocessor. It is the second of two diagnostics for these options. The M820x microprocessor uses an eight bit data path with a sixteen bit instruction memory. The instruction memory and data memory are two separate memories. The microprocessor is designed for moving data at high rates to work as a high speed link between processors when used with a line unit. The M8200 and M8207 have PROM instruction memories. The M8204 has writable control store. The memory size between all three processors vary also.

OPERATING PROCEDURES :

```
.R ZDMQE0
                This program is running under the supervisory program
                This supervisory program will first talk to you
CZDMQ-E-0
M8207 DIAG. #2 OF 2
UNIT IS M8200,M8204,OR M8207
RSTRT ADR 145702
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
WHICH MICRO-CPU? (0=M8200, 4=M8204, 7=M8207 (O) 7 ?
MICRO-CPU CSR ADDRESS : (O) 160170 ?
MICRO-PROCESSOR RUN SWITCH TYPE 0 IF OFF, 1 IF ON : (O) 1 ?

No software parameters available
```

DMC11/DMR11/KMC11 M8203 LINE UNIT STATIC TEST 1

ABSTRACT :

This program tests M8203 synchronus line unit module which supports both character-oriented (DDCMP, BSC...) and bit oriented (SDLC, HDLC...) protocols. The purpose of this program is to perform diagnostc testing of all M8203 logic in a relatively static manner. The following functions will be performed: line unit register addressing, USYRT addressing, static bit interaction and read/write logic test. Put H3254 and H3255 , H325, H3250 or H3251 test connector in (if not present, some tests will be skipped).

OPERATING PROCEDURES :

```
.R ZDMRF0
        This program is running under the supervisory program
        This supervisory program will first talk to you
CZDMR-F-0
M8203 STATIC LOGIC TESTS - PART 1 OF 2
UNIT IS M8203
RSTRT ADR 145702
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
DEVICE CSR ADDRESS : (0) 160170 ?
M8207 RUN SWITCH (E28 SW7) - TYPE 0 IF OFF, 1 IF ON : (O) 1 ?

CHANGE SW (L) ? N

No software parameters available
```

DMC11/DMR11/KMC11 M8203 LINE UNIT STATIC TEST 2

ABSTRACT :

This program tests M8203 synchronus line unit module which supports both character-oriented (DDCMP, BSC...) and bit oriented (SDLC, HDLC...) protocols. The purpose of this program is to perform diagnostc testing of all M8203 logic in a relatively static manner. The following functions will be performed: line unit register addressing, USYRT addressing, static bit interaction and read/write logic test. Put H3254 and H3255 , H325, H3250 or H3251 test connector in (if not present, some tests will be skipped).

OPERATING PROCEDURES :

```
.R ZDMSF0
                This program is running under the supervisory program
                This supervisory program will first talk to you
CZDMS-F-0
M8203 STATIC LOGIC TESTS - PART 2 OF 2
UNIT IS M8203
RSTRT ADR 145702
DR>STA

CHANGE HW (L) ? Y

#UNITS (D) ? 1
UNIT 0
DEVICE CSR ADDRESS : (0) 160170 ?
M8203 REG 11 (E134 SW10,9 , E121 SW9,10 : (O) 0 ?
M8203 REG 15 (E134 SW8-1) : (O) 0 ?
M8203 REG 16 (E121 SW8-1) : (O) 0 ?
SELECT TURNAROUND TYPE; 0=H3254&H3255, 1=H325,
2=H3250, 3=H3251, 4=INTEGRAL MODEM HDX SWITCH,
5=MOD LOC, 6=MOD REM, 7=NONE : (O) 0 ?
SELECT BAUDE RATE; TYPE '0' FOR 2.4K; '1' FOR 4.8K;
'2' FOR 9.6K; '3' FOR 19.2K; '4' FOR 56K; '5' FOR 250K;
'6' FOR 500K; '7' FOR 1 MEG BAUD : (O)

CHANGE SW (L) ? N
```

DUP11 (M7867) OFLINE SDLC XMTR

ABSTRACT :

The function of this program is to verify that the option operates according to specifications. Parameters may be set to alert diagnostics as to the DUP11 configuration by answering the parameter dialog. All questions should be answered and then each diagnostic will overlay these parameters which are stored in the memory (in the status table). The diagnostic will run up to eight consecutively addressed and consecutively vectored DUP11's in a chain mode. This program tests the control and status registers. In addition, the transmitter SDLC functions are checked in maintenance internal mode.

OPERATING PROCEDURES :

.R ZDPBC0

This will start the DUP11 test at address 200
with switch-reg 000000 it will use default parameters
CSR = 160050 VECTOR 770
With switch-reg = "000001" before starting at 200 ,new parameters are requested.
With switch-reg = "000200" before starting at 200 ,it will use parameters from previous DUP11 tests run before.
If you enter new parameters, it will ask you:

REC CSR ADDRS
VEC ADRS
PRIORITY (4 TO 7)
 # OF DUP's (IN OCTAL)
IS THE OPTIONAL CLR JMPR IN? (Y OR N)
IS THE H325 CONNECTOR ON? (Y OR N)

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error print out
SW12 = 1 bell on error
SW11 = 1 inhibit iterations
SW10 = 1 escape to next test on error
SW09 = 1 loop with current data
SW08 = 1 catch error and loop on it
SW07 = 1 use previous status table
SW06 = 1 not used
SW03 = 1 select DUP11's desired active
SW02 = 1 lock on selected test
SW01 = 1 restart program at selected test
SW00 = 1 enter parameters using manual dialog

if the CPU has no switch register it will use memory loc. 176
use "CONTROL G" to enter software SWR at loc 176.

DUP11 (M7867) OFLINE SDLC RCVR

ABSTRACT :

The function of this program is to verify that the option operates according to specifications. Parameters may be set to alert diagnostics as to the DUP11 configuration by answering the parameter dialog. All questions should be answered and then each diagnostic will overlay these parameters which are stored in the memory (in the status table). The diagnostic will run up to eight consecutively addressed and consecutively vectored DUP11's in a chain mode. ZDPDxx tests the receiver SDLC functions in maintenance internal mode, that is, clocking of the device is done by the program.

OPERATING PROCEDURES :

.R ZDPC??

This will start the DUP11 test at address 200
with switch-reg 000000 it will use default parameters
CSR = 160050 VECTOR 770
With switch-reg = "000001" before starting at 200 ,new parameters are requested.
With switch-reg = "000200" before starting at 200 ,it will use parameters from previous DUP11 tests run before.
If you enter new parameters, it will ask you:

REC CSR ADDRS
VEC ADRS
PRIORITY (4 TO 7)
 # OF DUP's (IN OCTAL)
IS THE OPTIONAL CLR JMPR IN? (Y OR N)
IS THE H325 CONNECTOR ON? (Y OR N)

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error print out
SW12= 1 bell on error
SW11= 1 inhibit iterations
SW10= 1 escape to next test on error
SW09= 1 loop with current data
SW08= 1 catch error and loop on it
SW07= 1 use previous status table
SW06= 1 not used
SW03= 1 select DUP11's desired active
SW02= 1 lock on selected test
SW01= 1 restart program at selected test
SW00= 1 enter parameters using manual dialog

if the CPU has no switch register it will use memory loc. 176
use "CONTROL G" to enter software SWR at loc 176.

DUP11 (M7867) SDLC TEST

ABSTRACT :

The function of this program is to verify that the option operates according to specifications. Parameters may be set to alert diagnostics as to the DUP11 configuration by answering the parameter dialog. All questions should be answered and then each diagnostic will overlay these parameters which are stored in the memory (in the status table). The diagnostic will run up to eight consecutively addressed and consecutively vectored DUP11's in a chain mode. ZDPDxx tests the DUP11 to run a limited SDLC protocoll and long data patterns. Specific data patterns are run to prove bit-stuff capability. The EIA data gates are proven and the priority logic functions are checked.

OPERATING PROCEDURES :

.R ZDPD??

This will start the DUP11 test at address 200
with switch-reg 000000 it will use default parameters
CSR = 160050 VECTOR 770
With switch-reg = "000001" before starting at 200 ,new parameters are requested.
With switch-reg = "000200" before starting at 200 ,it will use parameters from previous DUP11 tests run before.
If you enter new parameters, it will ask you:

REC CSR ADDRS
VEC ADRS
PRIORITY (4 TO 7)
IS THE OPTIONAL CLR JMPR IN? (Y OR N)
IS THE H325 CONNECTOR ON? (Y OR N)

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error print out
SW12 = 1 bell on error
SW11 = 1 inhibit iterations
SW10 = 1 escape to next test on error
SW09 = 1 loop with current data
SW08 = 1 catch error and loop on it
SW07 = 1 use previous status table
SW06 = 1 not used
SW03 = 1 select DUP11's desired active
SW02 = 1 lock on selected test
SW01 = 1 restart program at selected test
SW00 = 1 enter parameters using manual dialog

if the CPU has no switch register it will use memory loc. 176
use "CONTROL G" to enter software SWR at loc 176.

DUP11 (M7867) CONFIDENCE TEST

ABSTRACT :

The function of this program is to provide a level of confidence in the operation of the DUP11 without changing jumpers or switches from customer configuration. The option is tested in SDLC mode, then in DEC mode using a simulated DDCMP-line protocol with an imbedded CRC character. Both of this modes will be tested over a cable if a turnaround is possible. The modem control lines will also be tested if the H325 turnaround connector is used. The determination of what will be tested is done by answering a "parameter dialog". Additionaly the modem data leads may be tested if a modem has the analog loopback feature enabled.

OPERATING PROCEDURES :

.R ZDPE??

This will start the DUP11 test at address 200
with switch 7 = "0" new parameters are needed.
with switch 7 = "1" before starting at 200 old parameters
from previous tests are used.
if you enter new parameters, it will ask you:

REC CSR ADDRS
VEC ADRS
IS A MODEM WITH ANALOG LOOPBACK ENABLED CONNECTED? Y OR N)
IS THE H325 CONNECTOR ON? (Y OR N)
ARE THE DEFAULT JUMPERS ALL IN? (Y OR N)
IS THE OPTIONAL CLR JUMPER IN? (Y OR N)
SEC TX JUMPER IN? (Y OR N)
SEC RX JUMPER IN? (Y OR N)
ARE DSC 1 AND 2 BOTH IN? (Y OR N)

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error print out
SW12= 1 bell on error
SW11= 1 inhibit iterations
SW10= 1 escape to next test on error
SW09= 1 not used
SW08= 1 catch error and loop on it
SW07= 1 use previous status table
SW02= 1 lock on selected test
SW01= 1 restart program at selected test
SW00= 1 not used

if the CPU has no switch register it will use memory loc. 176
use "CONTROL G" to enter software SWR at loc 176.

DR11-B (four slot backplane) NPR DIAG.

ABSTRACT :

This is a logic test of the "NPR GENERAL INTERFACE" DR11-B. There is a special maintenance feature that allows testing of NPR's without a customers device attached. There is a second test included for exercising the DA11-B interprocessor link. The DR11-B test should be run in each computer before testing the DA11-B. DA11-B consisting of 2 M7229 modules and 2 BC08R cables.

OPERATING PROCEDURES :

.R ZDRB??

This will start the DR11-B test at address 200

Starting for the DA11-B
load address 1006 for the slave computer press start.
computer will halt.
load address 1000 for the master computer press start.
computer will halt.
press continue on the slave
press continue on the master

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error print out
SW12= 1 inhibit trace trap
SW11= 1 inhibit iterations
SW10= 1 not used
SW09= 1 not used
SW02= binary BR level of DR11-B (4,5 or 6)
SW01= binary BR level of DR11-B (4,5,or 6)
SW00= binary BR level of DR11-B (4,5,or 6)
if SW02-SW00 = 0 the BR level of the DR11-B is assumed = 5

if the CPU has no switch register it will use memory loc. 176
use "CONTROL G" to enter software SWR at loc 176.

DR11-C (M7860) with Testcable BC08R

ABSTRACT :

This is a logic test of the DR11-C. For this test to operate a special maintenance cable must be connected (BC08R). This test will check up to 32 sequentional DR11-C's.

OPERATING PROCEDURES :

.R ZDRC??

This will start the test at address 200
use 204 for special entrance - for testing unique DR11-C
use 210 for restart

For start address 204 :
1st halt - set switches to CSR address of DR11-C - press continue
2nd halt - set switches to Vector address of DR11-C - press cont.
set switch 10 to "1" to inhibit sequencing to next DR11-C

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error print out
SW12= 1 not used
SW11= 1 inhibit iterations
SW10= 1 do not advance to next DR11-C
SW09= 1 inhibit printout of device tested

if the CPU has no switch register it will use memory loc. 176
use "CONTROL G" to enter software SWR at loc 176.

DZ11 (M7819 EIA and M7814 20m)

ABSTRACT :

Parameters may be supplied to the program by either "auto sizing" or input from the user on the console by having SW00=1 at start time. Auto sizing will be done only the first time the program is started and SW00,03,07=00. The autosizer detects DZ11 address and vectors and determine wether it is a EIA or 20mA board. A turnaround connector is needed in order to test the parity and break logic. Test with SWR = 000 does not need a TURN-AROUND connector.

H3271 = Turnaround connector for EIA module, · H3190 for 20mA module
H325 = Turnaround and dispatch pannel testing for EIA module.

OPERATING PROCEDURES :

.R ZDZAI0

with SWR =000, will do a "AUTO SIZING", with SWR =001 manual input in manual mode it will ask:
1ST CSR ADDRESS (160000:163700):
1ST VECTOR ADDRESS (300:770):
BR LEVEL (4:6):
TYPE "A" FOR EIA MODULE OR "B" FOR 20 MA (A:B):
maintenance mode
[EXTERNAL <H325>-EIA ONLY (E)]
[INTERNAL <DZCSR03=1> (I)]
[STAGGERED <H3271>-EIA ONLY (S)]
[STAGGERED <H3190>-20MA ONLY (S)]
 # OF DZ11's <IN OCTAL> (1:20):
It will print "END PASS CZDZA-I CSR: 160100 VEC: 310....
Starting at address 210 with SWR = 002 calles the CABLE/ECHO - TERMINAL TEST
to verify the cables and distribution pannel. Put a terminal on any line, select the baude rate and line on the console terminal. The program prints on the console: TERMINAL ECHO TEST, and on the terminal connected to the DZ: THE QUICK BROWN FOX JUMPED.....

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error print out
SW12= 1 bell on error
SW11= 1 inhibit iterations
SW10= 1 escape to next test on error
SW09= 1 loop with current data
SW08= 1 catch error and loop on it
SW07= 1 use previous parameter table
SW06= 1 reselect DZ11's desired active
SW04= 1 select delay parameter
SW03= 1 extra parameter inputs (speed....)
SW02= 1 lock on selected test
SW01= 1 restart program at selected test
SW00= 1 build new status table from questiuons

KMC11-A IOP M8204 MICRO DIAGNOSTIC

ABSTRACT :

This program tests the KMC micro-processor. It performs write / read tests on the KMC unibus registers, checks the micro processor operation, checks out main memory, scratch pad memory, the ALU functions as well as interrupts and NPR operation. It does not require a line-unit to run.

OPERATING PROCEDURES :

.R ZKCAA0

this, with all switches down, will do a "AUTO SIZING"
with SWR bit 0=1 will do manual input (questions)
with SWR bit 7=1 will use existing parameters from previous KMC11 diagnostic runs.

in manual mode it will ask:

HOW MANY KMC11's TO BE TESTED ? 1<CR>
01
CSR ADDRESS ? 160010<CR>
VECTOR ADDRESS? 310<CR>
BR PRIORITY LEVEL ? (4,5,6,7) ? 5<CR>
WHICH LINE UNIT ? IF NONE TYPE "N", IF M8201 TYPE "1",
IF M8202 TYPE "2" ? 1<CR>
IS THE LOOP BACK CONNECTOR ON ? Y<CR>
SWITCH PAC#1 (DDCMP LINE#) ? 377<CR>
SWITCH PAC#2 (BM873 BOOT ADD) ? 377<CR>

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current test
SW13= 1 inhibit error print out
SW12= 1 bell on error
SW11= 1 inhibit iterations
SW10= 1 escape to next test on error
SW09= 1 loop with current data
SW08= 1 catch error and loop on it
SW07= 1 use previous parameter table
SW06= 1 halt in ROMCLK routine before clocking micro-proc.
SW05= 1
SW04= 1
SW03= 1 reselect KMC11's desired active
SW02= 1 lock on selected test
SW01= 1 restart program at selected test
SW00= 1 build new status table from questiuons

KMC11-A M8204 READ/WRITE MICRO-PROC. TEST

ABSTRACT :

This program tests the KMC micro-processor. It performs write / read tests on the KMC unibus registers, checks the micro processor operation, checks out main memory, scratch pad memory, the ALU functions as well as interrupts and NPR operation. It does not require a line-unit to run.

OPERATING PROCEDURES :

.R ZKCCA1

this, with all switches down, will do a "AUTO SIZING"
with SWR bit 0=1 will do manual input (questions)
with SWR bit 7=1 will use existing parameters from previous KMC11 diagnostic runs.

in manual mode it will ask:

HOW MANY KMC11's TO BE TESTED ? 1<CR>
01
CSR ADDRESS ? 160010<CR>
VECTOR ADDRESS? 310<CR>
BR PRIORITY LEVEL ? (4,5,6,7) ? 5<CR>
WHICH LINE UNIT ? IF NONE TYPE "N", IF M8201 TYPE "1",
IF M8202 TYPE "2" ? 1<CR>
IS THE LOOP BACK CONNECTOR ON ? Y<CR>
SWITCH PAC#1 (DDCMP LINE#) ? 377<CR>
SWITCH PAC#2 (BM873 BOOT ADD) ? 377<CR>

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error print out
SW12 = 1 bell on error
SW11 = 1 inhibit iterations
SW10 = 1 escape to next test on error
SW09 = 1 loop with current data
SW08 = 1 catch error and loop on it
SW07 = 1 use previous parameter table
SW06 = 1 halt in ROMCLK routine before clocking micro-proc.
SW05 = 1
SW04 = 1
SW03 = 1 reselect KMC11's desired active
SW02 = 1 lock on selected test
SW01 = 1 restart program at selected test
SW00 = 1 build new status table from questiuons

MAIN MEMORY, JUMP AND CRAM TESTS ON MICRO-PROC. KMC11-A or -AR (M8204/M8200-YA) with KMC11-DA/FA

ABSTRACT :

This program tests the KMC micro-processor. Parameters must be set up for the diagnostic to the KMC11 configuration. They are generated in two ways . manual input or autosizing. This program tests the KMC11-AR micro processor (M8204-YA) with low speed cram, or the KMC11 (M8204). It performs jump tests on the micro-processor, and tests the CRAM and other unique functions of the M8204. If a KMC11-AR (M8200-YA) and line unit (M8201) are present, free-running tests are performed. These tests are skipper if a KMC (M8204) or no line-unit is present.

OPERATING PROCEDURES :

.R ZKCDA0

this, with all switches down, will do a "AUTO SIZING"
with SWR bit 0=1 will do manual input (questions)
with SWR bit 7=1 will use existing parameters from previous KMC11 diagnostic runs.

in manual mode it will ask:

HOW MANY KMC11's TO BE TESTED ? 1<CR>
01
CSR ADDRESS ? 160010<CR>
VECTOR ADDRESS? 310<CR>
BR PRIORITY LEVEL ? (4,5,6,7) ? 5<CR>
WHICH LINE UNIT ? IF NONE TYPE "N", IF M8201 TYPE "1",
IF M8202 TYPE "2" ? 1<CR>
IS THE LOOP BACK CONNECTOR ON ? Y<CR>
SWITCH PAC#1 (DDCMP LINE#) ? 377<CR>
SWITCH PAC#2 (BM873 BOOT ADD) ? 377<CR>

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error print out
SW12 = 1 bell on error
SW11 = 1 inhibit iterations
SW10 = 1 escape to next test on error
SW09 = 1 loop with current data
SW08 = 1 catch error and loop on it
SW07 = 1 use previous parameter table
SW06 = 1 halt in ROMCLK routine before clocking micro-proc.
SW05 = 1
SW04 = 1
SW03 = 1 reselect KMC11's desired active
SW02 = 1 lock on selected test
SW01 = 1 restart program at selected test
SW00 1 build new status table from questiuons

FUNCTIONAL TEST PART 3

ABSTRACT :

This program continues from part 2 and tests extensively write read and write check operations using different data patterns. Select the 'TYPE HELP TEXT (L) N ? to list all tests performed. Each unit to be tested must be loaded with a scratch pack.

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal startaddress (address = 176700, vector = 254)

SA = 204 to change address and vector of the RH/RM

The program will print:

CZRMOBO - RM05/3/2 FUNCTIONAL TEST, PT 3

SWR = 000000 NEW =

you can change the switch register now.
If you have a switch register on the CPU change it there.

TYPE HELP TEXT (L) N ?

you can answer with 'Y' and it will print the list of all tests and the meaning of the switch settings.

You have to select a drive or type 'A' for all drives.

To ensure that no bad headers are left on the disk pack, this program should be halted by typing a CONTROL C. As a resolt, the program will be halted when the drive under test has completed testing.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeouts
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on specific error
SW08 = 1 loop on test as per SW<07-00>
SW07 = 1 TN 128
SW06 = 1 TN 64
SW05 = 1 TN 32
SW04 = 1 TN 16
SW03 = 1 TN 08
SW02 = 1 TN 04
SW01 = 1 TN 02
SW00 = 1 TN 01

KMC11-B M8206 STATIC TEST PART 1

ABSTRACT :

This program tests 1 to 64 KMC11-B modules. It consists of a set of sequential logic tests used to verify the logic of the KMC11-B. It is run before, and in conjunction with ZKMBxx to fully check the KMC11-B logic.

OPERATING PROCEDURES :

```
.R ZKMBA0

        This program is running under the supervisory program.
        This supervisory program will first talk to you.
CZKMB-A-0
CZKMBA0 KMC11-B STATIC PART 1
UNIT IS M8206
RSTRT ADR 145702
DR>STA/FLAG:PNT

CHANGE HW (L) ? Y

# UNITS (D) ? 1

UNIT 0.,
CSR ADDRESS : (O) 174100 ?<CR>
VECTOR ADDRESS : (O) 300 ?<CR>
PRIORITY LEVEL : (O) 5 ?<CR>
```

KMC11-B M8206 STATIC TEST PART 2

ABSTRACT :

This program tests 1 to 64 KMC11-B modules. It consists of a set of sequential logic tests used to verify the logic of the KMC11-B. It is run after, and in conjunction with ZKMBxx to fully check the KMC11-B logic.

OPERATING PROCEDURES :

```
.R ZKMCA0

        This program is running under the supervisory program.
        This supervisory program will first talk to you.
CZKMC-A-0
CZKMCA0 KMC11-B STATIC PART2
UNIT IS M8206
RSTRT ADR 145702
DR>STA/FLAG:PNT

CHANGE HW (L) ? Y

# UNITS (D) ? 1

UNIT 0
CSR ADDRESS : (O) 174100 ?<CR>
RUN REMOTE POWERFAIL TEST ? 0=NO, 1=YES : (O) 0<CR>
```

KW11-P PROGRAM. REAL TIME CLOCKL TEST

ABSTRACT :

This diagnostic verifies proper operation of the KW11-P. It contains a series of incremental routines that test the control and status register, count set buffer, counter, and interrupt vector address using 100 KHz, 10KHz line and external frequencies.

OPERATING PROCEDURES :

R ZKWB??

START ADDRESS

SA = 200 normal start
SA = 204 restart address (primarily used by XOR tester
SA = 210 timing test
SA = 214 double or single real time clock test 100 KHz
SA = 220 double or single real time clock test 10 KHz
SA = 224 double or single real time clock test 60 Hz
SA = 230 double or single real time clock test 50 Hz

If no hardware switch register is available the program will automatically use the contens of loc 176 as the software switch register.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop after error is detected
SW13 = 1 inhibit error reports
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1
SW04 = 1 enable synchronisation tests (2 KW11-P interf. needed)
SW03 = 1 adjusts delays for 11/60, 11/70 or 11/45 with MOS
SW02 = 1 CLK2 present-execute repeatability tests

KXJ11-CA SLAVE CPU ZKXAB0

KXJ11-CA I/O SLAVE CPU TEST

ABSTRACT :

This diagnostic is a functional test of the entire module. It consists of two major sections : the KXJ11-CA test code and the support routines which reside in the arbiter's memory. The suppor routines include routines to: size arbiter memory, determine what type of processor the arbitter cpu is (KDJ11, KDF11 ect.) and communicate between the arbitter and the slave CPU. This diagnostic can run in three modes : SBC mode tests the KXJ11-CA as a single board computer (to enter this mode bit 11 in the software switch register 176 must be set to = 1 and the IOP ID swich on the KXJ11-CA to be tested must be set to 0 or 1), single IOP mode tests the KXJ11-CA as the only I/O processor in an arbitter system, or multiple IOP mode can test up to 14 KXJ11-CA modules on the arbiter's Q-BUS.

To run this test your system needs DLV11 (DLV11-J...)compatible serial line ports for each KXJ11-CA to be tested plus one for the arbter's console port.

OPERATING PROCEDURES :

The diagnostic is loaded via a mass storrage device connected to the arbiter
RUN ZKXAB0

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 inhibit error summary
SW13 = 1 inhibits error reports
SW12 = 1 IOP ID# is known good for testing
SW11 = 1 test stand alone IOP
SW10 = 1 execute extanded memory test
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR<6:0>
SW07 = 1 inhibit test number/title

LA36 TERMINAL ZLAFA1

LA36 TERMINAL ON DL11 TEST

ABSTRACT :

This diagnostic verifies proper operation of the LA36 terminal on DL11, DLV11 type interface. Up to 48 terminals, including the console device, can be tested at a time. Control of this diagnostic may be through a switch register, or via interactive console terminal commands. The diagnostic self sizes the system as far as the interfaces, and ther interrupt vectors.

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal start

SA = 1372 restart address

The diagnostic will ask if console control is desired. Answer "Y" if you want to use interactive commands, otherwise type "N" for switch register control. If "Y" is typed a menu of available commands is printed on the console, and the program will wait for command input.

When switch register control is selected the program will halt. Set the switches , then press continue.

SWITCH SETTINGS :

SW15 = 1 halt on error

SW14 = 1 loop after error is detected

SW13 = 1 inhibit error reports

SW12 = 1 print interface table

SW11 = 1 inhibit iterations

SW10 = 1

SW06 = 1 run all tests in sequence

SW05 = 1 run all available lines

DECSA ZLDIA0

DECSA REPAIR LEVEL DIAGNOSTIC

ABSTRACT :

The program is called the LOADABEL DIAGNOSTIC IMAGE. The communication server can request the loading and running of the loadable diagnostic image "LDI" after successful completion of the self-tests.

OPERATING PROCEDURES :

press START button
wait for 88.88 to blink
press TEST button to "IN" position
display shows ethernet address, then L 30.....50 - this is loading image
take TEST button out (by pressing in again)

Connect a local terminal onto the DECSA behind the pannel (1200 baude)
This should display PLU>
PLU>H (help) prints you a help message
RUN CIDSAA, or CIDSBA, or SYSEXE

Currently there are five diagnostics and a system exerciser that can be executed separately in manual mode.

This program is running under the supervisory program.
This supervisory program will first talk to you.

CIDSA-B-0
CIDSAB PAM REPAIR DIAGNOSTIC #1
UNIT IS M3110 M3111
DR>START/PASS:1/FLAG:PNT<CR> *start, 1 pass, print test NR*
CHANGE HW ? Y

UNIBUS ADDRESS OF PAM 171200 ?<CR>
HARD ERROR INTERRUPT VECTOR (O) 130 ?<CR>
SOFT ERROR INTERRUPT VECTOR (O) 134 ?<CR>
DO YOU WISH TO CHANGE MARGIN CONDITION (L) ?<CR>

The display on the DECSA shows you the subtest number executed.

LN01 LASER PRINTER ZLNAD0

LN01 LASER PRINTER TEST

ABSTRACT :

This diagnostic verifies proper operation of the LN01 laser printer and its associated M7258 control unit which interfaces to the PDP-11 CPU. There are 20 subtests which assures a comprehensive checkout of the functional capability of the printer.

Test 1 interface logic test
Test 2 data transfer paths test
Test 3 printable characters test
Test 4 non-printable characters test
Test 5 print control test
Test 6 muliple line advance test
Test 7 overstrike test
Test 8 interlock test
Test 9 absolule and relative positioning test
Test 10 line feed new line mode test
Test 11 power-up default test
Test 12 tabs test
Test 13 margins test
Test 14 underline test
Test 15 partial line up, partial line down test
Test 16 drawn vectors test
Test 17 justify test
Test 18 portrait test
Test 19 font test
Test 20 miscelaneous control functions test

OPERATING PROCEDURES :

.R ZLNAD0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZLNA-D-0
CZLNAD0 LINE PRINTER DIAGNOSTIC
UNIT IS LN01
RSTRT ADR 147642
DR>START/FLAG:PNT

CHANGE HW (L) ? Y

 # UNITS (D) ? 1

UNIT 0
LP11 ADDRESS (O) 177514 ?<CR>
INTERRUPT VECTOR (O) 200 ?<CR>

CHANGE SW (L) ? N

RUN MANUAL INTERVENTION TESTS (L) N ?
AUTODROP ERROR COUNT (D) 5 ?

LP11 2310 PRINTER ZLPAB1

LP11-CONTR. AND DATA PROD.2310 PRINTER

ABSTRACT :

The LP11 line printer diagnostic test program is designed to provide a thorough check-out of the printer control interface electronics as well as the electronic and mecanical portions of the line printer itself. The program consists of a series of seven tests and drive routines, each of which can be selected and operated independently of the others using special entry points. The first test (test 1) is composed of several tests designed to check-out the processor interface control electronics and intercommunications data paths. Test 2, 3, and 4 use worst case patterns to test printer performance and endurance while test 5 and 6 provide drive for printer hammer allignment and intensity adjustment procedures and test of the paper slew and clutch operations.

OPERATING PROCEDURES :

.R ZLPAB1

SA = START ADDRESS

SA = 600 control test	*test 1 section 1*
SA = 610 test data paths	*test 1 section 2*
SA = 614 test character gen.	*test 1 setion 3*
SA = 620 test test zone and format	*test 1 section 4*
SA = 624 test hammer worst case	*test 2*
SA = 630 rotating pattern	*test 3*
SA = 634 double wedge pattern	*test 4*
SA = 640 hammer alignment test	*test 5*
SA = 644 slew test	*test 6*
SA = 650 scope loop test	*test 7*

SWITCH SETTINGS :

SW15= 1 halt after error printout (in static test only)
SW14= 1 132 col. line printer
SW13= 1 96 character set
SW12= 1 loop on test

LP05/11/14/ PRINTER ZLPKH0

LP05/11/14 PRINTER TEST

ABSTRACT :

This diagnostic verifies proper operation of the LP05, LP11, LP14 line printer and its associated M7258 control unit which interfaces to the PDP-11 CPU. There are 12 subtests, and 3 parts, part one checks out the processor interface and the printers inter-communication data paths and manual intervention test. Part two is a printing test designed to test the line printers mecanism itself. The last part is a scope driver routine for trouble shooting the line printer.

OPERATING PROCEDURES :

.R ZLPKH0

SA = Start Address
SA = 600 skip operator intervention test
SA = 700 run special scope driver routine
SA = 404 print speed test using line time clock
50 Hz patch loc 3212 from 7020 to 5670

SWITCH SETTINGS :

SW15 = 1 loop on error (in test 1 only)
SW14 = 1 optional DA VFU available
SW13 = 1 96 character set
SW12 = 1 loop on test
SW11 = 1 send only one character to line printer in scope mode
SW10 = 1 LP14 printer 0 = LP05/LP14
SW09 = 1 inhibit error reports
SW08 = 1
SW00 = 1 used for print speed manual timing

LP25/26/27/07 PRINTER ZLPLG0

LP25/26/27/07/LGxx PRINTER TEST

ABSTRACT :

This diagnostic verifies proper operation of the LP25, LP26, LP27, LGxx or LP07 line printer and its associated M7258 control unit which interfaces to the PDP-11 CPU. LG series printers will be tested as an LP26, due to the good LGxx internal self-test. There are 12 subtests. Any mix of printer types (LP.../LG...) can be tested up to a total of sixteen units.

OPERATING PROCEDURES :

.R ZLPLG0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZLPL-F-0
CLPLF0 LINE PRINTER DIAGNOSTIC
UNIT IS LP25,LP26,LP27,LP07,LG01
RSTRT ADR 147642
DR>START/FLAG:PNT

CHANGE HW (L) ? Y

 # UNITS (D) ? 1

UNIT 0
LP11 ADDRESS (O) 177514 ?<CR>
INTERRUPT VECTOR (O) 200 ?<CR>
ENTER 0 IF LP25, 1 IF LP26/LGxx, 2 IF LP07, 3 IF LP27 (O) ? 0
96 CHARACTER BAND (L) N ?<CR>

CHANGE SW (L) ? N

RUN MANUAL INTERVENTION TESTS (L) N ?
PERFORM MANUAL PRINTING SPEED MEASUREMENT (L) N ?
DESIRED TIME INTERVAL FOR PRINTING SPEED CALCULATION (D) 60 ?
TESTING IN U.S.A. (L) Y ?
AUTODROP ERROR COUNT (D) 5 ?

LS11 CENTRONICS PRINTER TEST

ABSTRACT :

This diagnostic verifies proper operation of the centronics line printer and assosiated control unit. It consists of a manual intervention check test, format control characters test, timing tests.....

OPERATING PROCEDURES :

.R ZLSAB0

SA = Start Address
SA = 600 restart address after appropriate swich settings

1 pass takes approx. 11 minutes.

Set operating switches

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 scope loop
SW13 = 1 inhibit error typeout
SW12 = 1 select "print time free" puls generater
SW11 = 1
SW10 = 1 elongation on SWR input test
SW09 = 1 selection of a particular test
SW08 = 1 select manual intervention test
SW07 = 1 test number selection
SW06 = 1 test number selection
SW05 = 1 test munber selection
SW04 = 1 test number selection
SW03 = 1 test number selection
SW02 = 1 test number selection
SW01 = 1 test number selection
SW00 = 1 test number selection

M9312 BOOT MODULE ZM9BE0

M9312 11/24/44 BOOT STRAP TEST

ABSTRACT :

This diagnostic verifies the ROM information on the M9312 bootstrap terminator or 11/44 /24 UBI terminator. If 11/44 CPU, the M9312 is not needed for this test (the M9312 module is integrated in the UBI module). This test reads all bytes in the ROM, calculates the checksum and compares it with the checksum written in the ROM.

OPERATING PROCEDURES :

.R ZM9BE0

SA = Start Address
SA = 204 restart address

Set operating switches

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1
SW13 = 1 inhibit error typeout
SW12 = 1
SW11 = 1
SW10 = 1 bell on error

DEQNA (M7504) (ETHERNET) FUNCTIONAL DIAGNOSTIC
DELQA (M7516) (ETHERNET) FUNCTIONAL DIAGNOSTIC

ABSTRACT :

The program tests the functionality of the DEQNA / DELQA in a 18 or 22 bit Q-bus environment. This ZQNA test attempts to isolate faults to the following field replacable units : DEQNA, DELQA bulkhead assembly, transceiver cable, circuit breaker (fuse in bulkhead assembly), and transceiver. A configuration of up to two units will be accepted for test. The internal and internal/ extended loopback mode tests do not require the transceiver or the loopback connector to be unplugged. The external loopback mode may be used with a terminated transceiver that has no network cable attached.

OPERATING PROCEDURES :

.R ZQNA??

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZQNA-I-0
DEQNA/DELQA FUNCTIONAL TEST
UNIT IS DEQNA/M7504
RSTRT ADR 142060
DR>STA/FLAG:PNT<CR> *start, print test NR*
#UNITS (D) ? 1<CR>

UNIT 0
DEQNA I/0 PAGE ADR (O) 174440 ?<CR>
INTERRUPT VECTOR ADR (O) ? 700<CR>
this is a standard address and vector.

CHANGE SW (L) ? Y

DO YOU WANT TO TEST SANITY TIMER (L) N ?
EXTERNAL LOOPBACK MODE (L) N ?
SYSTEM HAS BLOCK-MODE MEMORY (L) Y ?
IS LOOPBACK CONNECTOR IN DEQNA (L) N ?
NXM TEST ? MUST HAVE < 4MB MEMORY (L) N ?

DEUNA (M7792/M7793) REPAIR LEVEL DIAGNOSTIC

ABSTRACT :

The program tests the functionality of the DEUNA. This diagnostic was designed to detect static and dinamic hardware failures in the DEUNA boardset. It will only run in a standalone, offline environment. The DEUNA is logicaly removed from the 'wire' by the diagnostic, so no messages from other nodes on the network, to the DEUNA under test, will disturbe the test. However, because this diagnostic runs the DEUNA self-test in test 9, and the self-test performs an external loopback as part of its testing procedure, it is recommended that the DEUNA transceiver cable be removed from the H4000 transceiver and plugged into a field service external loopback connector. There are 46 subtests in this program.

OPERATING PROCEDURES :

.R ZUAAB0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZUAA-B-0
DEUNA REPAIR DIAGNOSTIC
UNIT IS DEUNA
RSTRT ADR 142060
DR>STA/FLAG:PNT<CR> *start, print test NR*
#UNITS (D) ? 1<CR>

UNIT 0
WHAT IS THE PCSR0 ADDRESS? (O) ? 174510<CR>
WHAT IS THE VECTOR ADDRESS? (O) ? 120<CR>
this is a standard address and vector.

DEUNA (M7792/M7793) FUNCTIONAL DIAGNOSTIC

ABSTRACT :

The program tests the functionality of the DEUNA. A configuration of up to eight units will be accepted for test. This diagnostic will only operate in a stand alone, offline environment using the operational microcode. This test needs a DEUNA with an external loopback connector or transceiver cable connected to coaxial cable. There are 28 subtests.

OPERATING PROCEDURES :

```
.R ZUABC0

        This program is running under the supervisory program.
        This supervisory program will first talk to you.
CZUAB-C-0
DEUNA PDP11 FUNCTIONAL DIAGNOSTIC
UNIT IS DEUNA
RSTRT ADR 142060
DR>STA/FLAG:PNT<CR>     start, print test NR
#UNITS (D) ? 1<CR>

UNIT 0
WHAT IS THE PCSR0 ADDRESS? (O) ? 174510<CR>
WHAT IS THE VECTOR ADDRESS? (O) ? 120<CR>
        this is a standard address and vector.

CHANGE SW (L) ? Y

RUN TEST 20 IN EXTERNAL LOOPBACK MODE ? (L) N ?
        to do that you need the loop-back connector.
```

DEUNA / DELUA NIE EXERCISER DIAGNOSTIC

ABSTRACT :

The network interconnect exerciser (NIE) program is meant to provide field service with a tool for determining the connectivity of nodes on the network interconnect (NI). The NIE program will determine the ability of nodes on the NI to communicate with each other and provide node installation verification and problem isolation. The NIE uses the low level maintenance features of the DEUNA to provide testing without interrupting normal operation of the NI. The VAX version of the NIE can also be run conncurrently on another node, with each version running independently of each other.

OPERATING PROCEDURES :

.R ZUACD0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZUAC-D-0
CZUAC DEUNA, DELUA NI EXERCISER
UNIT IS DEUNA, DELUA
RSTRT ADR 142060
DR>START

CHANGE HW (L) ? Y

#UNITS (D) ? 1<CR>
UNIT 0
WHAT IS THE PCSR0 ADDRESS? (O) ? 174510<CR>
WHAT IS THE VECTOR ADDRESS? (O) ? 120<CR>
WHAT IS THE PRIORITY LEVEL ? (O) 5 ?
this is a standard address and vector.

ETHERNET DEFAULT ADDRESS (HEX): 08-00-2B-03-2D-40
.....

NIE>
now you are in a command mode, you can type
NIE> (A) ? HELP
with this command you will get the help text
below is a example of usefull commands
NIE> (A) CLEAR NODE/ALL
NIE> (A) BUILD
NIE> (A) SHOW NODES
NIE> (A) RUN PATTERN
NIE> (A) SHOW COUNTERS
NIE> (A) SUMMARY

DELUA (M7521) FUNCTIONAL DIAGNOSTIC

ABSTRACT :

The program tests the functionality of the DELUA. A configuration of up to eight units will be accepted for test. This diagnostic will only operate in a stand alone, offline environment using the operational microcode. This test needs a DELUA with an external loopback connector or transceiver cable connected to coaxial cable. There are 27 subtests.

OPERATING PROCEDURES :

```
.R ZUADB0

        This program is running under the supervisory program.
        This supervisory program will first talk to you.
CZUAD-B-0
DELUA PDP11 FUNCTIONAL DIAGNOSTIC
UNIT IS DELUA
RSTRT ADR 142060
DR>STA/FLAG:PNT<CR>     start, print test NR
#UNITS (D) ? 1<CR>

UNIT 0
WHAT IS THE PCSR0 ADDRESS? (O) ? 174510<CR>
WHAT IS THE VECTOR ADDRESS? (O) ? 120<CR>
        this is a standard address and vector.

CHANGE SW (L) ? Y

RUN EXTERNAL LOOPBACK MODE TEST (REQ. H4080 OR EQUIV. LOOPBACK ?
Y/N (L) N ?
TO AVIOD MAN. INTERVENTION INSTALL H4080 OR EQUIV. LOOPBACK NOW
Y/N (L) N ?
```

DISK's DISK's DISK's DISK's

RC25
RK611
RK06/07
RP04/05/06
RP07
RK11/05
RLV11/12
RL11
RL01/02
RM02/03/05
RM80
RQDX1/2/3
RX50/RUX50
RD51/52
RD53/54
RX33
RD31
RS03/04
RX01/02
RA80/81/82
RA60
UDA/KDA50

M8739/M7740/RC25 PERFORMANCE EXER

ABSTRACT :

This exerciser is designed to verify the integrity of the drive(s) and to detect faults at the functional level only. This test tries to simulate a stressful operating system. These conditions are created by issuing a heavy load of MSCP I/O commands to all online units. You can select write-only, read-only, writes and reads, write-compares and read-compares. This exerciser can test up to 4 controllers, each controller having up to 2 drives. All RC25 drives to be tested by this program must have been successfully verified by the RC25 AZTEC front-end / host diagnostic (ZRCFC0)

OPERATING PROCEDURES :

```
.R ZRCDB0

        This program is running under the supervisory program.
        This supervisory program will first talk to you.
CZRCD-B-0
RC25 DISK EXERCISER
UNIT IS SINGLE RC25 PLATTER
RSTRT ADR 145702
DR>START

CHANGE HW (L) ? Y
#UNITS (D) ? 1<CR>          disk drives

UNIT 0
IP ADDRESS (O) 172150 ?<CR>
VECTOR (O) 154 ?<CR>
BR LEVEL (O) 5 ?<CR>
PLATTER ADDRESS (UNIT PLUG) (D) 0 ?<CR>
                            even number = removable cardridge
                            odd number = fixed disk
ALLOW WRITES TO CUSTOMER DATA AREA ON THIS PLATTER (L) ? N

CHANGE SW (L) ? Y

ERROR LIMIT (0 FOR NO LIMIT) (D) 32 ?
TRANSFER LIMIT IN MEGABYTES (0 FOR NO LIMIT) (D) 2 ? 10
SUPPRESS PRINTING ERROR LOG MESSAGES (L) Y ?
RUN DM EXERCISER INSTEAD OF MULTI DRIVE SUBTEST (L) N ?
RANDOM SEEK MODE (L) Y ?
STARTING TRACK (D) 0 ?
ENDING TRACK (D) 1641 ?
.....
```

M8739/M7740/RC25 FRONT END TEST

ABSTRACT :

This test is a basic functional test of the RC25 subsystem. It verifies: that the CPU can communicate correctly with the RC25 disk through the adapter, that the RC25 can seek and select the heads properly, that the RC25 conforms to the specified seek and rotational times, and that it can perform all functions in response to MSCP commands.

OPERATING PROCEDURES :

.R ZRCFC0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZRCF-C-0
RC25 FRONT END/HOST DIAGNOSTIC
UNIT IS AZTEC RC25 PLATTER
RSTRT ADR 145702
DR>START

CHANGE HW (L) ? Y
#UNITS (D) ? 1<CR> *(unit = 1 single patter)*

UNIT 0
IP ADDRESS (O) 172150 ?<CR>
VECTOR (O) 154 ?<CR>
BR LEVEL (O) 5 ?<CR>
PLATTER ADDRESS (UNIT PLUG) (D) ?<CR>
even number = removable cardridge
odd number = fixed disk

CHANGE SW (L) ? Y

USE TOP SURFACE FOR SINGLE SURFACE TEST (L) Y ?
DO YOU WISH TO LIMIT AREA TESTED IN TESTS 15-18 (L) N ?
NUMBER OF RETRIES FOR TEST IF EHROR OCCURED (D) 0 ?
DO YOU WISH TO CONTINUE TESTING AFTER RETRIES? (L) N ?
DO YOU WISH TO DO THE MANUAL INTERVENTION TEST? (L) N /
DO YOU WISH TRACE MODE ? (L) Y ?

RC25 DISK PACK FORMATTER

ABSTRACT :

This program will prepare RC25 media for use as addressable storage by providing headers and replacing of bad blocks. There are three modes of formatter operations: 1. REFORMAT: this mode is used to format a medium which has been previously formatted, and is being reformatted to clear existing data. It assumes that the FCT is still intact. 2. RESTORE: only for manufacturing. 3. RECONSTRUCT: this mode is used when none of the other modes is possible. It detects bad blocks by performing repetitive read checks of each sector. For this reason, a reconstruct run takes considerably longer than the other modes.

OPERATING PROCEDURES :

.R ZRCHB0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZRCH-B-0
RC25 DISK FORMATTER
UNIT IS RC25 DISK DRIVE SUBSYSTEM
RSTRT ADR 145702
DR>START

CHANGE HW (L) ? Y
#UNITS (D) ? 1<CR> *(unit = 1 single patter)*

UNIT 0
RC25 IP REGISTER ADDRESS (O) 172150 ?<CR>
RC25 INTERRUPT VECTOR ADD.(O) 154 ?<CR>
RC25 BUS REQUEST LEVEL (O) 5 ?<CR>
UNIT NUMBER TO BRING ONLINE (UNIT PLUG) (D) ?<CR>
even number = removable cardridge
odd number = fixed disk

CHANGE SW (L) ? Y

FORMAT IN UNATTENDED REFORMAT MODE (L) Y ?

ENTER DATE <MM-DD-YYYY> (A)

RK611 CONTROLLER TEST, PART 1

ABSTRACT :

The RK611 diskless controller diagnostic part 1 reads and writes every RK611 register, tests the interrupt mechanism, and tests the silo loading logic. No RK06/07 drive is required for program execution.

OPERATING PROCEDURES :

.R ZR6AD0

START ADDRESSES:
SA = 200 normal starting
SA = 204 restart program
SA = 214 request bus address, vector address and priority modification

first pass : 7 seconds
subsequent : 2 minutes

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 abort after 20 errors
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR (7-0)

use "CONTROL G" to enter software SWR at loc. 176

RK611 CONTROLLER TEST, PART 2

ABSTRACT :

The RK611 diskless controller diagnostic part 2 tests the loading of the drive bus messages by executing class A commands. Some tests execute commands partialy in maintenance mode and partially at normal speed to fool the controller and force errors. No RK06/07 drive is required for program execution, deselect all drives (port A and B out).

OPERATING PROCEDURES :

.R ZR6BD0

START ADDRESSES:
SA = 200 normal starting
SA = 204 restart program
SA = 214 request bus address, vector address and priority modification normal RKCS1 address 177440, vector 210.

first pass : 7 seconds
subsequent : 2 minutes

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 abort after 20 errors
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR (7-0)

use "CONTROL G" to enter software SWR at loc. 176

RK611 CONTROLLER TEST, PART 3

ABSTRACT :

The RK611 diskless controller diagnostic part 3 tests the loading of the drive bus messages shift register by executing class B commands, tests index and sector pulse detection, tests silo and NPR transfers from memory in 16 and 18 bit mode, tests non-existent memory and unibus parity error detection, tests read and write MFM loopback, and tests class B instruction errors. Most tests execute commands in maintenance mode. No RK06/07 drive is required for program execution, deselect all drives (port A and B out).

OPERATING PROCEDURES :

.R ZR6CE0

START ADDRESSES:
SA = 200 normal starting
SA = 204 restart program
SA = 214 request bus address, vector address and priority modification
normal RKCS1 address 177440, vector 210.

first pass : 30 seconds
subsequent : 8 minutes

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 abort after 20 errors
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR (7-0)

use "CONTROL G" to enter software SWR at loc. 176

RK611 CONTROLLER TEST, PART 4

ABSTRACT :

The RK611 diskless controller diagnostic part 4 tests the loading of the drive bus message shift register by executing class C commands, tests header generation for search operations, tests write data NPR transfers to silo, tests header recognition, tests cylinder, track and sector increments after successful header search, tests detection of all header type errors, tests ECC generation and writing, tests partial sector write (zero fill), tests 18 bit format ECC generation and data writes. No RK06/07 drive is required for program execution, deselect all drives (port A and B out).

OPERATING PROCEDURES :

.R ZR6DD0

START ADDRESSES:
SA = 200 normal starting
SA = 204 restart program
SA = 214 request bus address, vector address and priority modification normal RKCS1 address 177440, vector 210.

first pass : 25 seconds
subsequent : 3 minutes

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 abort after 20 errors
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR (7-0)

use "CONTROL G" to enter software SWR at loc. 176

RK611 CONTROLLER TEST, PART 5

ABSTRACT :

The RK611 diskless controller diagnostic part 5 tests multi-sector data transfers, tests mid-transfer seeks, tests cylinder overflow checking, tests NPR transfers to memory, tests ECC error detection and correction, tests write check both 16 and 18 bit mode and forces write check errors. No RK06/07 drive is required for program execution, deselect all drives (port A and B out).

OPERATING PROCEDURES :

.R ZR6EC0

START ADDRESSES:
SA = 200 normal starting
SA = 204 restart program
SA = 214 request bus address, vector address and priority modification normal RKCS1 address 177440, vector 210.

first pass : 60 seconds
subsequent : 3 minutes

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 abort after 20 errors
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR (7-0)

use "CONTROL G" to enter software SWR at loc. 176

RK06/07 DUAL PORT DIAGNOSTIC

ABSTRACT :

The RK06/07 dual port logic test performs a series of tests which verify that the dual port option is functioning properly. Both ports of the disk are cabled to the same controller by a standard cable and the dual port test switch is enabled on the dual port module. The effect of this is that one drive appeares as two units one on port A and one on port B. The bit 0 of the unit select number on port B is complemented. This arrangement allows the dual port logic to be tested from one CPU/Controller to a maximum of 4 drives. The test needs a pack installed and the drive ready.

OPERATING PROCEDURES :

.R ZR6GC0

START ADDRESSES:
SA = 200 normal starting
SA = 220 request bus address, vector address and priority modification normal RKCS1 address 177440, vector 210.

one pass : 2.5 minutes

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 bypass drive after 20 errors
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR (7-0)

use "CONTROL G" to enter software SWR at loc. 176

RK06/07 DISK DRIVE DIAGNOSTIC TEST 1

ABSTRACT :

The RK06/07 test 1 checks that the drive is capable of performing all static tests, insures that the drive can write and read headers, insures that the drive can perform seeks, formats the pack and checks error detection. Install a good diskpack and spin it up, wait for ready then run the test.

OPERATING PROCEDURES :

.R ZR6HF0

START ADDRESSES:
SA = 200 normal starting
SA = 204 same as 200 but bypass test 16 (N square)
SA = 220 request bus address, vector address and priority modification normal RKCS1 address 177440, vector 210.
SA = 230 same as 220 but bypass test 16 (N square)

one pass : RK06 7 minutes
one pass : RK07 14 minutes

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 bypass drive after 20 errors
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR (7-0)

use "CONTROL G" to enter software SWR at loc. 176

RK06/07 DISK DRIVE DIAGNOSTIC TEST 2

ABSTRACT :

The RK06/07 test 2 checks that the drive is capable of performing read and write data operations, worst case pattern, spiral writing and reading and all offset operations are performed.

OPERATING PROCEDURES :

.R ZR6IF0

START ADDRESSES:
SA = 200 normal starting
SA = 220 request bus address, vector address and priority modification normal RKCS1 address 177440, vector 210.

Load program, scratch pack installed and drive ready, drives not to be tested must have both ports deselected.

one pass : 1.5 minutes

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 bypass drive after 20 errors
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR (7-0)

use "CONTROL G" to enter software SWR at loc. 176

RK06/07 DISK DRIVE DIAGNOSTIC TEST 3

ABSTRACT :

The RK06/07 test 3 is the manual intervention test. You have to open and close the door, pull ou the unit select plug, push the port switch and so one.....

OPERATING PROCEDURES :

.R ZR6JF0

SA = 220 request bus address, vector address and priority modification normal RKCS1 address 177440, vector 210.

Load program, scratch pack installed and drive ready, drives not to be tested must have both ports deselected.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 bypass drive after 20 errors
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error

use "CONTROL G" to change software SWR at loc. 176

RK611 CONTROLLER FUNCTIONAL TEST

ABSTRACT :

The RK611 functional controller diagnostic completes the testing of an RK611 controller. This program tests those areas in the controller that could not be tested in a diskless environment.

OPERATING PROCEDURES :

.R ZR6KG0

SA = 204 restart address
SA = 214 request bus address, vector address and priority modification
SA = 220 is the phase locked loop clock adjustment start.
normal RKCS1 address 177440, vector 210.

Load program, scratch pack installed and drive ready, drives not to be tested must have both ports deselected.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 bypass drive after 20 errors
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 execute test number specified in SW <7-0>

use "CONTROL G" to change software SWR at loc. 176

RK06/RK07 PACK FORMATTER

ABSTRACT :

This utility can write, read and verify headers and data on a pack, reports the pack serial number, you can verify a pack with data on in a read-only mode and it formats a pack and all sectors found bad will be added to the "BAD SECTOR FILE". If this file is corrupted you will not be able to format this pack, you can fix this problem with the "ZR6R?? utility, RSX (BAD) or RSTS.

OPERATING PROCEDURES :

START ADDRESSES:
SA = 200 normal starting
SA = 204 restart address
This test has the standard address and vector in it.
To change this patch loc 2570 for RKBAS (normal 177440) and loc 2572 for RKVEC (normaly 210).

Load program, pack installed and drive ready,

You can get a help info with this diagnostic
Below is a example to format a pack in drice 0 (RK07)

DRIVE TYPE (6 OR 7) 7
DRIVE NUM = 0
SECTOR/TRACK = <CR>
MODE = <CR>
EVEN CYLINDER PATTERN = <CR>
ODD CYLINDER PATTERN = <CR>
TRACK LIMITS = <CR>
OFFSET = <CR>
ANY SECTOR TO BE FLAGED BAD? (TYPE Y OR N)N<CR>
PRESERVE SOFTWARE BAD SECTOR FILES? (TYPE T OR N)Y<CR>
SOFTWARE DETECTED BAD SECTOR FILES PRESERVED

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current cylinder and track operation
SW13 = 1 inhibit error typeout
SW12 = 1
SW11 = 1
SW10 = 1 ring bell on error
SW09 = 1
SW08 = 1
SW07 = 1 report summary of all bad sectors
SW01 = 1 report all data in error

use "CONTROL G" to change software SWR at loc 176

RK06/07 DYNAMIC TEST PART 1

ABSTRACT :

This RK06/07 test provides a functional shakedown of the entire subsystem, including the unibus interface and access to main memory. The testing in part 1 employs worst-case situations involving mecanical positioning, disk addressing and data transfers. In addition, measurements are made pertaining to drive operational timing.

OPERATING PROCEDURES :

.R ZR6ME1

SA = 204 request bus address, vector address and priority modification normal RKCS1 address 177440, vector 210.
SA = 220 dual-access data test 22

Load program, scratch pack installed and drive ready, drives not to be tested must have both ports deselected.

Runtime first pass : 14 minutes
Runtime subsequent : 21 minutes

Patch location 166 from 000000 to 000001 for 50 Hz timing.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 report description only, on error
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 apply random stall between operations
SW07 = 1 do explicit seeks in tests 1-12
SW06 = 1 report one error per transfer in tests 17,21
SW05 = 1 inhibit writes in test 21
SW04 = 1 inhibit write checks in test 21
SW03 = 1 inhibit reads and software compares in test 21
SW02 = 1 inhibit software compares in test 21
SW01 = 1 read after a write check error in test 21
SW00 = 1 report all software compare errors in tests 17,21

use "CONTROL G" to change software SWR at loc. 176

RK06/07 DYNAMIC TEST PART 2

ABSTRACT :

This RK06/07 test provides a functional shakedown of the entire subsystem, including the unibus interface and access to main memory. The testing in part 2 employs worst-case situations involving head offseting, memory addressing and data transfers, unibus cycle contention and muliple drive operations. In addition, an RK06/07 head alignment aid is provided to do ON-LINE alignment of drive heads.

OPERATING PROCEDURES :

.R ZR6NE3

SA = 204 request bus address, vector address and priority modification normal RKCS1 address 177440, vector 210.
SA = 224 head alignment aid program start

Load program, scratch pack installed and drive ready, drives not to be tested must have both ports deselected.

Runtime first pass : 2 minutes
Runtime subsequent : 3 minutes

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 report description only, on error
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 apply random stall between operations
SW07 = 1
SW06 = 1 report one error per transfer in tests 2-4
SW02 = 1
SW01 = 1 inhibit writes in test 1
SW00 = 1 report all software compare errors in tests 2-4

use "CONTROL G" to change software SWR at loc. 176

RK06/07 PERFORMANCE EXERCISER

ABSTRACT :

This RK06/07 performance exerciser will exercise in a random overlapped manner 1 to 8 RK06 or RK07 disk drives attached to the same controller. Drives under test can be added to or dropped from the test by operator command. It executes reads, writes and writes followed by a write check at random blocks on the disk. Any time you can get a error statistic.

OPERATING PROCEDURES :

.R ZR6PD0

SA = 204 restart address
SA = 214 request bus address, vector address and priority modification normal RKCS1 address 177440, vector 210.

Load program, scratch pack installed and drives ready, drives not to be tested must have both ports deselected.

The following commands are available in command mode :
(<CONTROL C> gets you into the command mode).

Tn	*initiate testing on drive n (number)*
Dn	*drop drive n (number)*
Pn	*change parameters on drive n (number)*
Sn	*print statistics of drive n (number)*
Wn	*write and verify the pack on drive n (number)*

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current operations
SW13 = 1 inhibit error typeout
SW12 = 1
SW10 = 1 ring bell on error
SW09 = 1
SW07 = 1
SW06 = 1 inhibit dropping drives on clearable errors
SW05 = 1 inhibit dropping drives if op count threshold is exceeded
SW04 = 1 inhibit dropping drives if error threshold exceeded
SW03 = 1 display entire sector read before retry sequence
SW02 = 1
SW01 = 1 inhibit software data comparisons
SW00 = 1

use "CONTROL G" to change software SWR at loc. 176

RK06/RK07 DRIVE COMPATIBILITY TEST

ABSTRACT :

This utility helps to verify the compatibility of up to 16 RK06 or RK07 drives. Compatibility is defined here as the ability of a drive to write data which can be read successfully by all other drives, and additionaly the ability of a drive to completely over-write data written by all other drives. The testing is done in two passes. For the entire test you need only one pack but you have to move that one around into all drives.

OPERATING PROCEDURES :

START ADDRESSES:

SA = 200 start program for one subsystem only
SA = 204 start pass 1 for more than one subsystem
SA = 220 start pass 2 for more than one subsystem

Follow as the program instructs you !

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error typeout
SW12 = 1 report description only, on errors
SW11 = 1 unused
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 apply random stall between operations
SW07 = 1 type bad sector files at start
SW01 = 1 unused

use "CONTROL G" to change software SWR at loc. 176

RK06/07 USER DEFINED TEST

ABSTRACT :

This RK06/07 test provides the capability of entering, editing, saving, recalling and executing test programs designed by the user. It operates interactively to allow the user to develop a specific test made of subsystem commands, checking and reporting in any sequence. A function the field service uses often is the formatting and creation of the BAD SECTOR FILE of which you find a description below.

OPERATING PROCEDURES :

.R ZR6RC1

You get into the command mode
TYPE HP TO PRINT HELP FILE
**HP*

below you find the example which formats and creates a empty BAD SECTOR FILE on a RK07 drive 0

	SF = set function
**SF,CC<CR>*	*SF,CC = set function, controller clear*
**SF,DC,0<CR>*	*SF,DC = drive clear, drive# 0*
**DT,7*	*DT = drive type is RK07*
**SF,PA,0<CR>*	*SF,PA = pack acknowledge, drive# 0*
**SF,WH,0,1456,2,0,102<CR>*	*WH = write header drive 0 cylinder 1456, track 2, sector 0,*
**DP,X,pack serial number<CR>*	*6 digits*
000000<CR>	
000000<CR>	
000000<CR>	
177777<CR>	
177777<CR><CR>	
**SF,WD,0,1456,2,0,12000,X<CR>*	
**CO<CR>*	

COMPILE OK
**RU<CR>*

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW02 = 1 inhibit all data compare error reports
SW01 = 1 report all data compare error
SW00 = 1 short error report

use "CONTROL G" to change software SWR at loc. 176

MECHANICAL AND READ/WRITE TEST

ABSTRACT :

This program will check seeks, access times, read and write, track and sector addressing. Each drive to be tested has to have a formatted disk pack. programmable (dual port) drives may be tested.

OPERATING PROCEDURES :

START ADDRESSES:

SA = 200 normal starting (inhibit dual ported drives)
SA = 204 select operating parameters (inhibit dual ported drives)
SA = 210 select RH11/RH70 addresses (do not inhibit dual ported drives)
SA = 214 combination of 204/210 (do not inhibit dual ported drives)
SA = 220 same as 200 but no inhibitions
SA = 224 same as 204 but no inhibitions

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error type out
SW11 = 1 inhibit iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 print error message on line printer
SW07 = 1 read control switch settings from TTY
SW06 = 1 inhibit time reports (tests 12-15)
SW05 = 1 report one error per sector (test 16 & 17)
SW04 = 1 inhibit writes (test 20)
SW03 = 1 inhibit write checks (test 20)
SW02 = 1 inhibit read and software compares (test 20)
SW01 = 1 inhibit software compares (test 20)
SW00 = 1 perform read after write check (test 20)
use "CONTROL G" to enter software SWR at loc. 176

CONTROL SWITCH SETTINGS :

SW00 = 1 = 20 sector (18 bit) / 0 = 22 sector mode (16 bit)
SW05 = 1 inhibit software timeouts (disable watchdog timer)
SW06 = 1 50Hz power source
SW07 = 1 do explicit seeks before data transfers
SW07 = 0 do read header and data commands in tests 0-6
SW08 = 1 do explicit seeks before data transfers
SW12 = 1 incrementing stalls in test 4
SW13 = 1 use random stall times
SW14 = 1 stall after every drive function
SW15 = 1 inhibit write pack before testing (test 16)
Default condition of CSW (15 = 00) = 0
To enter control switch from TTY, following are used:
<.> CR (period): a statement terminator
<. > CR (period period): end of modification and start of test
<,> CR (comma): seperator between drive No. and test No.
</> CR (slash): test NO. followed by slash, opens that test for modification
RUBOUT. delete last character

RP04/5/6 FORMATTER PROGRAM

ABSTRACT :

This program formats disk packs in either 16 or 18 bit mode and performs a check of the pack's surface by reading back the written bit pattern. You can select a read only mode ('C' = check mode).

NOTE: This program is not intended to be a entire sector verification test, for doing that you need more and different data patterns.

OPERATING PROCEDURES :

START ADDRESSES:

SA = 200 normal starting (inhibit dual ported drives)
SA = 204 non-standard RH11 or RH70 address/vector (enable dual ported drives)
SA = 210 select RH11/RH70 addresses (do not inhibit dual ported drives)
SA = 220 same as 200 but no inhibitions

PROGRAM DIALOG:

PROGRAM MODE (C or F) : C = check, F = format & check, default <CR> = F
OPERATE IN 22 SECTOR (16 bit mode) (Y or N)
DRIVE :
ENTER ADDRESS LIMITS: <CR> = default
SELECT DATA PATTERN : 0 = zeros
1 = ones
2 = worst case <CR> = default, worst case

"Control C" will print you the current cylinder and track address. By typing "control C" during typing the current cylinder and track address, the program will abort. This is the proper way to halt the program. If not done this way, a sector may be improperly formatted.

RUN TIME:	*FORMAT*	*VERIFICATION*	*TOTAL*
RP04/05	*8 min.*	*4 min.*	*12 min.*
RP06	*16 min.*	*8 min.*	*24 min.*

SWITCH SETTINGS :

SW15 = 1 halt on error
SW13 = 1 inhibit error typeout
SW10 = 1 bell on error
SW09 = 1 loop on error
SW07 = 1 print soft errors as they occur
SW02 = 1 don't display system status after initial start
SW01 = 1 loop on the current track
SW00 = 1 loop the program on selected drive

use "CONTROL G" to enter software SWR at loc. 176

RP04/5/6 HEAD ALIGNMENT PROGRAM

ABSTRACT :

A program to check out head alignment of RP04/05/06, or used as a tool to align head with the appropriate drive test box.
The program also contains a utility routine which performs 5000 random seeks without data transfers. The random seek utility allows the operator to exercise the drive with the alignment pack in place and then re-verify head alignment.

OPERATING PROCEDURES :

START ADDRESSES:
SA = 200 normal starting (RH11 / RH70 has standard address and vector)
SA = 204 to change non-standard addresses of RH11 / RH70.

Connect the test box and mount the alignment pack.
Select the drive to be aligned in response to the typeout on the console.
Answer the mode of operation : A / V or E
A = alignment V = verify E = exerciser (5000 seeks)

If an A is selected, the program will position the heads over the alignment cylinder and then ask for a head. The head entered will be selected and the program will ask for a new head. Until the new head is entered, the last one will remain selected.

HEAD ALIGNMENT:

on RP04/05 the program checks for each head being within
+/-150 microinches of track centerline of CYL 245 and
+/-350 microinches of track centerline of CYL 004 and 400.

on RP06 the program checks for each head being within
+/- 75 microinches of track centerline of CYL 496 and
+/-175 microinches of track centerline of CYL 008 and 800.

If not within these limits, the program will type an error message for that particular head. If SW 00 = 1, the actual value of the offset will be typed out. Heads out of tolerance will not be identified.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW13 = 1 inhibit error typeout
SW09 = 1 loop on error
SW02 = 1 check alignment of the specified head
SW01 = 1 loop on the current head
SW00 = 1 type all track center values

use "CONTROL G" to enter software SWR at loc. 176

RP04/5/6 RP MULTI-DRIVE LOGIC TEST

ABSTRACT :

Performs interactive tests on RP04/5/6 connected to a massbus with RH11 or RH70. Single or dual port testing is possible. Uses overlapped operations between the drives. All data transfer commands are used, selected randomly. Uses formatted disk packs.

OPERATING PROCEDURES :

START ADDRESSES:

SA = 200 normal starting (RH11 / RH70 has standard addr.176700 vec. 254)
SA = 204 to change non-standard addresses of RH11 / RH70.
SA = 220 same as 200 but dual ported drives are not inhibited.

KEYBOARD COMMANDS: *(after a CONTR. C)*

T = assign drives for test
R = performs a sequential read of a pack
W = write and check data pack with a datapattern
S = request a drive performance summary
D = deassign a drive under test

T, W, R require address limits, drive ID and bad block info to be entered or use defaults, a "period" is defining default values for the remaining entries and starts execution.

Maximum 16 bad sectors may be entered on a pack in the format
C,T,S *EXAMPLE : 145,04,12*

Examples : T1 = ass.drive 1 for test *TA = all drives*
R5 = read pack on drive 5 *RA = all packs*
D3 = deassign drive 3 *DA = all drives*

RUNTIME : 1 drive = 2,5 hrs. *8 drives = 11 hrs.(data transfer mode)*
1 drive = 25 hrs. *8 drives = 40 hrs.(seek verify mode)*

SWITCH SETTINGS :

SW15 = 1 halt on error
SW13 = 1 inhibit error typeout
SW10 = 1 ring the bell on error
SW07 = 1 display all data compare errors
SW06 = 1 do not alter the current operation parameters
SW05 = 1 partial register display
SW04 = 1 do not deassign drives
SW03 = 1 display the sector in error if 'DCK' 'DTE' or 'WCE'
SW02 = 1 inhibit subsystem status typeout during startup
SW01 = 1 inhibit data comparison after read orders
SW00 = 1 read only mode

use "CONTROL G" to enter software SWR at loc. 176

DUAL CONTROLLER TEST, PART 1

ABSTRACT :

This is a series of tests which verify that the RP04/5/6 dual controller logic is funtioning properly. Only the control logic is tested by this program, data handling in the dual controller mode is not tested.

Both ports of the drive are cabled to the same massbus by a special adapter cable (P/N 7010507-02). This arrangement allows the dual controller logic to be tested from one PDP-11 computer. With this cable, the drive appears as two units on the massbus. Each port of the drive will respond to a different massbus address. The address of each port will depend upon the drive's "DP" board - module M7775 for RP04's, or by the address plug for RP05/6's

****

Any other drive on the massbus which has an address in conflict with either of the test addresses must be powered down.

****

OPERATING PROCEDURES :

Switch the "controller select" switch on the drive to be tested to the A/B position. Cycle the drive up.
Start the program.
Enter the drive number.
Enter the test number to be run. Carriage return will run all tests.

START ADDRESSES:
SA = 200 normal starting (RH11 / RH70 has standard addr.176700 vec. 254)
SA = 204 to change non-standard addresses of RH11 / RH70.

SWITCH SETTINGS .

SW15= 1 halt on error
SW14= 1 loop on test
SW13= 1 inhibit error typeout
SW11= 1 inhibit test iterations
SW10= 1 ring bell on error
SW09= 1 loop on error

use "CONTROL G" to enter software SWR at loc. 176

DUAL CONTROLLER TEST. PART 2

ABSTRACT :

This is a series of tests which verify that the RP04/5/6 dual controller logic is funtioning properly. Only the control logic is tested by this program, data handling in the dual controller mode is not tested.

Both ports of the drive are cabled to the same massbus by a special adapter cable (P/N 7010507-02). This arrangement allows the dual controller logic to be tested from one PDP-11 computer. With this cable, the drive appears as two units on the massbus. Each port of the drive will respond to a different massbus address. The address of each port will depend upon the drive's "DP" board - module M7775 for RP04's, or by the address plug for RP05/6's

****

Any other drive on the massbus which has an address in conflict with either of the test addresses must be powered down.

****

OPERATING PROCEDURES :

Switch the "controller select" switch on the drive to be tested to the A/B position. Cycle the drive up.
Start the program.
Enter the drive number.
Enter the test number to be run. Carriage return will run all tests.
There are 14 tests

START ADDRESSES:
SA = 200 normal starting (RH11 / RH70 has standard addr.176700 vec. 254)
SA = 210 to change non-standard addresses of RH11 / RH70.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error

use "CONTROL G" to enter software SWR at loc. 176

DISKLESS TEST, PART 1

ABSTRACT :

This test is used to test the device control logic connected to either an RH11 or RH70 disk drive controller. The DCL is mainly tested. If the disk is powered up, it is required to get the disk to the "heads unloaded" position. After a successful run of this test it can be assumed that the DCL part, which handels data, is working properly. All data commands use the maintenance register in the wraparound mode. This test assumes that the RH70 specific test (ERHAE1) has been successfully run.

OPERATING PROCEDURES :

START ADDRESSES:

**Switch 12 must be set when this program is to be run using an RH70*

SA = 200 normal starting (RH11 / RH70 has standard addr.176700 vec. 254)
SA = 204 to change non-standard addresses of RH11 / RH70.
SA = 210 unit selection (program asks for unit number)

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 RH70 controller select
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR (7-0)
SW07 = 1 stop further data misscompare printout
SW06 = 1 ECC test - compare end result only

use "CONTROL G" to enter software SWR at loc. 176

DISKLESS TEST, PART 2

ABSTRACT :

This test is used to test the device control logic connected to either an RH11 or RH70 disk drive controller. The DCL is mainly tested. If the disk is powered up, it is required to get the disk to the "heads unloaded" position. After a successful run of this test it can be assumed that the DCL part, which handels data, is working properly. All data commands use the maintenance register in the wraparound mode. This test assumes that the RH70 specific test (ERHAE1) has been successfully run.

OPERATING PROCEDURES :

START ADDRESSES:

**Switch 12 must be set when this program is to be run using an RH70*

SA = 200 normal starting (RH11 / RH70 has standard addr.176700 vec. 254)
SA = 204 to change non-standard addresses of RH11 / RH70.
SA = 210 unit selection (program asks for unit number)

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 RH70 controller select
SW11 = 1 inhibit test iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR (7-0)
SW07 = 1 stop further data misscompare printout
SW06 = 1 ECC test - compare end result only

use "CONTROL G" to enter software SWR at loc. 176

FUNCTIONAL CONTROLLER (DCL) TEST, PART 1

ABSTRACT :

This tests the rest of the "DCL" (together with ZRJGxx and ZRJHxx). After this one run ZRJJD0. If all this 4 tests run without error, it can be assumed that the "DCL" works OK. It uses the disk surface and the drive mechanics. It does not need a formatted disk pack. The test assumes a good scratch pack (not to many bad sectors).

OPERATING PROCEDURES :

START ADDRESSES:

SA = 200 normal starting (RH11 / RH70 has standard addr.176700 vec. 254)
It will test all drives available one after an other.

SA = 204 to change non-standard addresses of RH11 / RH70.

SA = 210 for unit selection

SA = 220 same as 200 but will not run tests needing manual intervention.

SWITCH SETTINGS :

*Use switch 12 = 1 if run on a 11/70

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 RH70 controller selected
SW11 = 1 inhibit iterations
SW10 = 1 ring the bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR <7-0>
SW07 = 1 stop futher data compares if SW08 is low
SW06 = 1 type all error registers if SW08 is low
SW05 = 1 multy address plug test if SW08 is low

use 'CONTROL G" to enter software SWR at loc. 176

FUNCTIONAL CONTROLLER (DCL) TEST, PART 2

ABSTRACT :

This tests the rest of the "DCL" (together with ZRJGxx, ZRJHxx and ZRJIxx). If all this 4 tests run without error, it can be assumed that the "DCL" works OK. It uses the disk surface and the drive mechanics. It does not need a formatted disk pack. The test assumes a good scratch pack (not to many bad sectors).

OPERATING PROCEDURES :

START ADDRESSES:

SA = 200 normal starting (RH11 / RH70 has standard addr.176700 vec. 254)
It will test all drives available one after an other.
SA = 204 to change non-standard addresses of RH11 / RH70.
SA = 210 for unit selection

SWITCH SETTINGS :

**Use switch 12 = 1 if run on a 11/70*

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 RH70 controller selected
SW11 = 1 inhibit iterations
SW10 = 1 ring the bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SWR <7-0>
SW07 = 1 stop futher data compares if SW08 is low
SW06 = 1 type all error registers if SW08 is low

use "CONTROL G" to enter software SWR at loc. 176

RP07 FORMATTER/SCANNER

ABSTRACT :

This is the 16 bit formatter/scanner program. The format process uses media "DEFECT SKIPS" in addition to bad sector flagging. This program has basicaly 6 functions: format, verify, scan, list, modify and write FE2. This program is running under the Supervisor.

OPERATING PROCEDURES :

To be used only by RP07 trained field engineers !

.R ZRJKB0

DR>START <CR>

Answer the hardware questions of the Supervisor

Then you have to enter the option:

0 = format headers and data on the disk pack
1 = verify headers and track descriptors
2 = scan the disk pack for new defects and record them
3 = list the defective tracks and the headers of defective sectors
4 = modify the track descriptor
5 = write the second field service cylinder only

If your answer was a 0, 2 or a 4 then the program will ask you:
"Do yoy want to write anywhere on media (L) N ?"
A "N" (no) will force the program to use the field service cylinder only.
A "Y" will destroy all customer data on the pack.

Now you can change the drive parameters
"MIN CYL (D) 0 ? "
"MAX CYL (D) 630 ? "
"MIN TRK (D) 0 ? "
"MAX TRK (D) 31 ? "

RP07 FUNCTIONAL TEST

ABSTRACT :

This test will verify that the disk is capable of performing seeks, that the seeks and access times are within tolerance, that the addressing circuitry operates properly, and that write and read data capabilities are functional. This program is running under the supervisory program. If a KW11-P system clock is not installed on the system, the timing tests will not be executed.

OPERATING PROCEDURES :

.R ZRJLB0

DR>START

Answer the hardware questions of the Supervisor
Then you will be prompted by :

CHANGE SW (L) ?

normal run is default <CR>
if you answer "YES" to this question you can change the following drive parameters:

STARTING CYL (D) 0 ?
ENDING CYL (D) 629 ?
INCREMENT CYL (D) 1 ?
STARTING TRK (D) 0 ?
ENDING TRK (D) 31 ?
INCREMENT TRK (D) 1 ?
STARTING SEC (D) 0 ?
ENDING SEC (D) 49 ?
DATA PATTERN (O) 030221 ?

DO YOU want TO WRITE ANYWHERE ON MEDIA (L) N ?

A "N" (no) will force the program to use the field service cylinder only.
A "Y" will destroy all customer data on the pack.
It will print a warning message :

! CUSTOMER DATA WILL BE OVERWRITTEN ! (test 17 & 18)

CONTINUE (L) ?

This test 17 and 18 (writing test) will only be run when the "WRITE DATA ANYWHERE ON THE MEDIA" option is selected by the operator.

RP07 FRONT-END / ISOLATOR TEST

ABSTRACT :

This is a program which partially automates the pathfinder document to allow computerized sequential diagnosis of an RP07. The program initially demonstrates hardware integrity between the RHxx controller, associated cabling and the disk control logic (DCL). Satisfactory completion of this phase of testing then permits "HOST" invocation of the RP07 resident microdiagnostics, those specifically allowing remote execution, to ascertain a reasonable level of confidence in the disk drive. This program is running under the supervisory program.

OPERATING PROCEDURES :

.R ZRJMB0

DR>START

Answer the hardware questions of the Supervisor
Then you will be prompted by :

CHANGE SW (L) ?

normal run is default <CR>
if you answer "YES" to this question you can change the following drive parameters:

"EXECUTE TEST 25., MASSBUS INTERFACE SWITCH TEST (L) Y ?"
The test 25 requires manual intervention.
"FOR DRIVE N, WILL YOU PLACE THE MASSBUS DISABLE SWITCH J12-S01 IN THE DISABLED (DOWN) POSITION?"

"EXECUTE TEST 52., PRINT CONTENS OF INTERNAL ERROR LOG (L) Y ?
The error log in the RP07 may be useful as a troubleshooting tool, and as such may be printed.

"SELECT A TRACK FOR THE RP07 INTERNAL RD-WRT TESTS (L) N ?"

"EXECUTE TEST 60, SELECT A MICRO-DIAGNOCTIC FOR EXEC. (L) N ?"

RP07 DUAL PORT TEST

ABSTRACT :

This test performs a series of tests which verify that the RP07 dual port logic is functioning properly. Only the control logic is tested by this program, data handling in the dual port mode is not tested by this program. Both ports of the drive are cabled to the same massbus by a special cable. This arrangement allows the dual port logic to be tested from one PDP11 / RH11 or RH70. Power down all massbus disks except the one to test because you can get an disk address conflict. This program is running under the supervisory program.

OPERATING PROCEDURES :

.R ZRJNA0

DR>START <CR>

Answer the hardware questions of the Supervisor

UNIT 1
RPCS1 ADRS (O) 176700 ?
VECTOR (O) 254 ?
BR LEVEL (O) 5 ?
DRIVE # (O) 0 ?

Supervisory commands are:

START
RESTART
CONTINUE
PROCEED
EXIT
ADD
DROP
PRINT
DISPLAY
FLAGS
ZFLAGS

There are 32 subtests.

RP07 PERFORMANCE EXERCISER

ABSTRACT :

This program is designed to perform an interactive test on RP07 disk drives connected to a massbus subsystem. The drives may be controlled by an RH70 controller. You can verify that the drives under test are performing to their data error rate and seek error rate. The program will exercise drives connected as either single or dual port units. Dual port drives are tested by loading and running the program from both controlling systems. Operations on the multi-drive configurations are overlapped (other drives are performing seek/search operations while one drive is performing a data transfer).

OPERATING PROCEDURES :

.R ZRJOB0

Start address 204 allows to change the default RP/RH address or any drive parameters.

writes first datapattern, then goes into a testing mode.

KEYBOARD COMMANDS: *(after a CONTR.C)*

T = assign a drive for test
R = performs a sequential read of a pack
W = write and check data pack with a datapattern
S = request a drive performance summary
D = deassign a drive under test

End of pass occures when the drive has read 2.58 x 1000 million words
If SW09 = 1 the end of pass occures at 0.645 x 1000 million words read.

SWITCH SETTINGS :

SW15 = halt on error
SW13 = inhibit error type out
SW10 = ring bell on error
SW09 = change end of pass to 1/4 of normal
SW08 = inhibit end of pass messages
SW07 = display all data compare errors
SW06 = do not alter the current operation parameters
SW05 = partial register display if error (no ECC reg.)
SW04 = do not drop drives at end of test or max. error count
SW03 = display the sector in error if 'DCK', 'DTE' or 'WCF'
SW02 = do not type drive status at program start / no perform. report
SW01 = inhibit data compare after read w/o 'DCK' error
SW00 = read only mode

RK05 PERFORMANCE EXERCISER

ABSTRACT :

This program simulates a operating system running on RK05's and checks for errors that arise in such an environment. It uses overlapped seeks with polling the drives etc. This test expects a good formatted scratch pack on all drives to be tested. It can test up to 8 drives all together. One pass can take from 30 to 90 minutes.

Before running this test make sure ZRKJ??, ZRKK??, ZRKL?? and ZRKI?? (utility package / pack formatter) run with no error.

OPERATING PROCEDURES :

.R ZRKHG0

SA = 200 normal starting (writing first data pattern)
SA = 210 restart address, go straight to exerciser and skips test 1-7

SWITCH SETTINGS :

SW15 = 1 halt on error
SW13 = 1 inhibit error typeout
SW12 = 1 type out the error history
SW11 = 1 dump out all RK11 registers
SW10 = 1 ring the bell on error
SW09 = 1 loop on specific error
SW08 = 1 dump out transfer data and error statistics
SW06 = 1 select bus address limits for data transfers
SW05 = 1 halt before doing the next set of commands
SW04 = 1 do not rewrite the disk on 210 restart
SW03 = 1 type out elapsed time at error
SW02 = 1 drop drive after maximum errors
SW01 = 1 type serial number of erroring drive
SW00 = 1 type only elapsed time if SW08 and SW03 = 1

use "CONTROL G" to enter software SWR at loc. 176

RK05 UTILITY PACKAGE

ABSTRACT :

This program is not a diagnostic, rather it helps to make adjustments, and provides some utility programs needed to maintain RK05 disks.

OPERATING PROCEDURES :

START ADDRESSES:

SA = 200 normal starting

The RK11 utility package is divided into eight sections.
It will print a menue:

SECTION	*NAME*
0	*INDEX*
1	*COMPATIBILITY TEST*
2	*OSCILLATING SEEK PACKAGE*
3	*FORMATTER SURFACE VERIFIER*
4	*FRONT PANNEL TEST*
5	*RK05 CONTROL PANNEL TEST 2*
6	*HEAD ALIGNMENT ROUTINE*
7	*POWER FAILURE (DURING WRITE) TEST*

TYPE = x

0= to adjust the index/sector timing to 70 us (+-12us).
To do that you need an alignment pack.

1= to confirm the fact that a group of drives are truly compatible.

2= to perform servo adjustments and/or seek logic checkout by performing seeks between user specified address.
The program requests to enter drive number and halts.
Enter drive number in SW (drive 0 = SW0=1).
press continue.
The program requests to enter seek address and halts.
Enter seek address in SW reg. (4 cylinder seek = 2000)
(max cylinder seek 0-202 cylinders seek = 145000 in SW reg.)
press continue.

The rest should be strait forward.

SWITCH SETTINGS :

Section 2 oscillating seek pachage is using the switches to tell the program how big seeks to perform

Use "CONTROL G" to enter software SWR at loc. 176

RK11 BASIC LOGIC TEST #1

ABSTRACT :

This program is part-1 of 2 and it checks ony the drive-independent logic of the RK11 controller, no drive is needed. After this test run part 2 (ZRKKxx).

OPERATING PROCEDURES :

.R ZRKJE0

The program will print:

END PASS # 1
END PASS # 2 ....

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on test
SW13= 1 inhibit error typeout
SW12= 1 loop on error
SW11= 1 inhibit iterations
SW10= 1 testing on simulator
SW09= 1 loop on specific error
SW08= 1 loop on test as per SW<07-00>

use "CONTROL G" to enter software SWR at loc. 176

RK11 BASIC LOGIC TEST #2

ABSTRACT :

This program is part-2 of 2 and it checks the rest of the controller logic. Make sure that the drives to be tested are loaded with disks and are in 'RUN' and 'WRT' enabled. Put drives that are not to be tested on 'LOAD' mode. This test is also capable of detecting faults in the drive.

OPERATING PROCEDURES :

.R ZRKKF2

The program will print:

RK11 BASIC LOGIC TEST 2
MAINDEC-11 CZRKKF
TO TEST DRIVE 'N' HALT PROGRAM.....

DRIVES TO BE TESTED?
you enter the drive # like : 0,1,2 <CR>

DRIVE 0
DRIVE 1
DRIVE 2
END PASS # 1

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on test
SW13= 1 inhibit error typeout
SW12= 1 loop on error
SW11= 1 inhibit iterations
SW10= 1 testing on simulator
SW09= 1 loop on specific error
SW08= 1 loop on test as per SW<07-00>
SW06= 1 drop the drive after maximum number of errors occur

use "CONTROL G" to enter software SWR at loc. 176

RK05 DINAMIC TEST

ABSTRACT :

This program demonstrates the electromechanical integrity of the RK05 (RK05F) drive. It checks linear positioner control and speed control, verifies read-write logic integrity and provides a timer for the seek function. Before real testing starts, the program formats and then checks the pack for correct format.

OPERATING PROCEDURES :

.R ZRKLE0

SA = 210 conversational mode

If any particular drive is to be selected for testing, put that drive into "RUN" and "WRITE ENABLE" mode. Put the rest of the drives on "LOAD" and "WRITE LOCK". Then start as usual.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1 loop on error
SW11 = 1 dump all RK11 registers on error
SW10 = 1 ring bell on error
SW09 = 1 loop on specific error
SW08 = 1 loop on test as per SW<07-00>
SW07 = 1
SW06 = 1 type seek timer
SW05 = 1 type the small graph
SW04 = 1 print the complete graph
SW03 = 1 terminate function selected by user
SW02 = 1 drop the drive after max. allowable errors
SW01 = 1
SW00 = 1 ask for data pattern

use "CONTROL G" to enter software SWR at loc. 176

RLV11 DISKLESS CONTROLLER TEST

ABSTRACT :

This program tests only the controller, tests registers read/write function, test the reset function, the NO-OP function, interrupts and the maintenance function. This test runs only on the RLV11 controller (M8013, M8014).

OPERATING PROCEDURES :

```
.R VRLAC0
```

This program is running under the supervisory program.
This supervisory program will first talk to you.

```
CVRLA-C-0
CVRLAC0 RLV11 RL01 DISKLESS DIAGNOSTIC
UNIT IS RLV11
RESTART ADDRESS 145702
DR>START <CR>
```

You have to answer the hardware questions.
This is a (mostly used) example :

```
CHANGE HW (L) ? Y<CR>
# UNITS (D) ? 1<CR>
UNIT 0
11/23 PROCESSOR (L) Y ?
BUS ADDRESS (O) 174400 ? <CR>
VECTOR (O) 160 ? <CR>
DRIVE (O) 0 ? <CR>
BR LEVEL (O) 5 ? <CR>

CHANGE SW (L) ? Y<CR>

DROP ON ERROR LIMIT (L) N ?
AUTOSIZE (L) N ?

CVRLA EOP 1
0 Cumulative errors
```

RLV12 DISKLESS CONTROLLER TEST

ABSTRACT :

This program tests the RLV12, RLV11 and/or RL11 disk controllers with or without a drive attached. This test is a modified VRLAB0 test, retaining all previous tests and got upgraded to include additional testing for the RLV12. In RLV12 mode, the program tests the basic interface logic, control register manipulation and functionality. The RLV12 maintenance mode function is executed to test controller write/read data paths without a drive present. The extended addressing capability is tested in 18 or 22 bit mode depending on the type and ammount of memory installed in the test system.

OPERATING PROCEDURES :

.R VRLB??

This program is running under the supervisory program.
This supervisory program will first talk to you.

CVRLB-C-0
RLV12 DISKLESS
UNIT IS RLV12, RLV11, OR RL11
RESTART ADDRESS 145702
DR>START <CR>

You have to answer the hardware questions.
This is a (mostly used) example :

CHANGE HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
RLV12 (L) Y ?
RLV11 (L) Y ?
CSR ADDRESS (O) 174400 ?
VECTOR (O) 160 ?
BR LEVEL (O) 4 ? <CR>

CHANGE SW (L) ? Y<CR>

ERROR LIMIT FOR AUTO-DROP (D) 0 ?

ALL REMAINING QUERIES ARE FOR OPTIONAL (MANUFACTORING)
G5388 TEST-LOOP-MODULE SET-UP. USE <^Z> TO BYPASS.

G5388 TLM INSTALLED (L) N ? N
MMU AVAILABLE
MEMORY SIZE 384 KW
22 BIT ADDRESSING

CVRLB EOP 1
0 Cumulative errors

RL11/RLV11/RLV12 ZRLGE0

RL11/RLV11/RLV12 CONTROLLER TEST 1

ABSTRACT :

This program is part 1 of 2. It starts by checking basic interface logic with register manipulation. Then interrupts are tested with the corresponding BR level, NOOP, get status, read headers, head select, extensively checks the CRC logic and seek operations. It tests the full controller but by default also exercises the drive. This test does not write onto the disk but it is strongly recommended not to use a customer disk. If you want you can put the drive into "WRITE PROTECT" mode.

OPERATING PROCEDURES :

.R ZRLGE0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZRLG-E-0
CZRLG TESTS CONTR. FUNCTIONS, INTERFACE LOGIC, REG. OPERATIONS
UNIT IS RL01,RL02
RESTART ADDRESS 142060
DR>START <CR>

You have to answer the hardware questions.
This is a (mostly used) example :

CHANGE HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0<CR>
RL11 = 1, RLV11 = 2, RLV12 = 3 (O) ? 1<CR>
BUS ADDRESS (O) 174400 ? <CR>
VECTOR (O) 160 ? <CR>
DRIVE (O) 0 ? <CR>
DRIVE TYPE = RL01 (L) Y ? N<CR> (no for RL02)
BR LEVEL (O) 5 ? <CR>

CHANGE SW (L) ? N<CR>

NEXT TEST MAY ZERO LOAD UNIT. DO IT ANYWAY ? Y

It will type (if no errors)

CZRLG EOP 1
0 Cumulative errors

RL11/RLV11/RLV12 CONTROLLER TEST 2

ABSTRACT :

This program is part 2 of 2. It continues testing of the RL controller. It tests the write function in different ways, proper increment of RLBA reg., header not found with write, multiple sector transfers, read function in different ways, chechs the SILO in the controller, the write-check function, read without header-compare. This test writes onto the disk.

OPERATING PROCEDURES :

.R ZRLHB1

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZRLH-B-0
CZRLH TESTS WRITE DATA, READ DATA, AND WRITE CHECK OPERATIONS
UNIT IS RL01,RL02
RESTART ADDRESS 145702
DR>START <CR>

You have to answer the hardware questions.
This is a (mostly used) example :

CHANGE HW (L) ? Y<CR>

 # UNITS (D) ? 1<CR>

UNIT 0<CR>
RL11 (L) Y ?<CR>
BUS ADDRESS (O) 174400 ? <CR>
DRIVE TYPE = RL01 (L) Y ? N
VECTOR (O) 160 ? <CR>
BR LEVEL (O) 5 ? <CR>
DRIVE (O) 0 ? 1<CR>

CHANGE SW (L) ? N<CR>

It will type (if no errors)

CZRLH EOP 1
0 TOTAL ERRS

RL01/02 DRIVE TEST 1

ABSTRACT :

This program is part 1 of 2. The program runs on the first drive before starting on the second. It tests : get status from drive with reset, get status, seek, and read header. Only seeks with 0 difference are used so no head movement is required. Optional : operator intervention test, head load and unload test, drive select test, head alignment support routine.

OPERATING PROCEDURES :

.R ZRLID1

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZRLI-D-0
CZRLI TESTS THE RL01-02 INTERFACE AND BASIC DRIVE LOGIC
UNIT IS RL01,RL02
RESTART ADDRESS 145702
DR>START <CR>

You have to answer the hardware questions.
This is a (mostly used) example :

Change HW (L) ? Y<CR>

 # UNITS (D) ? 1<CR>

UNIT 0<CR>
RL11 (L) Y ?<CR>
BUS ADDRESS (O) 174400 ? <CR>
VECTOR (O) 160 ? <CR>
DRIVE (O) 0 ? 1<CR>
DRIVE TYPE = RL01 (L) Y ? N
BR LEVEL (O) 5 ? <CR>

CHANGE SW (L) ? N<CR>

It will type (if no errors)

CZRLI EOP 1
0 TOTAL ERRS

If you answer Y to the question :
CHANGE SW (L) ? Y <CR>

EXECUTE DRIVE SELECT TESTS (L) N ?
EXECUTE HEAD ALIGNMENT SUPPORT (L) N ?
DO MANUAL INTERVENTION TESTS (L) N ?
INPUT ERROR LIMIT (D) 20 ?

RL01/02 DRIVE TEST 2 (SEEK)

ABSTRACT :

This program is part 2 of 2. The test starts detecting outer and inner guard band. Seek operations undergo a broad range of testing using single differences, proceeding to seeks of greater differences. This test does not write onto the disk, you can put it into the "WRITE- PROTECT" mode.

OPERATING PROCEDURES :

.R ZRLJB2

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZRLJ-B-0
CZRLJ TESTS OUTER & INNER GUARD BAND DETECTION AND SEEK OPERATIONS
UNIT IS RL01,RL02
RESTART ADDRESS 145702
DR>START <CR>

You have to answer the hardware questions.
This is a (mostly used) example :

Change HW (L) ? Y<CR>

 # UNITS (D) ? 1<CR>

UNIT 0<CR>
RL11 (L) Y ?<CR>
BUS ADDRESS (O) 174400 ? <CR>
VECTOR (O) 160 ? <CR>
DRIVE (O) 0 ? 1<CR>
DRIVE TYPE = RL01 (L) Y ? N
BR LEVEL (O) 5 ? <CR>

Change SW (L) ? N<CR>

It will type (if no errors)

CZRLJ EOP 1
0 TOTAL ERRS

If you answer Y to the question :

CHANGE SW (L) ? Y <CR>

you can change the following parameters:

USE ALL CYL (L) N ?
USE ALL SECT (L) N ?
LOW SEEK LIMIT (L) N ?
UPPER SEEK LIMIT (L) N ?
USE ONLY ONE SURF (L) N ?
INPUT ERROR LIMIT (D) 20 ?
DATA CMP ERR LMT (D) 10 ?

11/21 - RL01/02 PERFORMANCE EXERCISER

ABSTRACT :

The program tries to simulate a user environment. It will randomly exercise up to 2 controllers and 8 drives. Initialy the bad sector file is read from each drive and stored in memory, then each pack is written with one of eight data patterns. The drives are randomly picked and given a random string function of:

1. seek, write, write-check
2. seek, read data, compare data
3. seek, read headers, read 1 sector with no header compare, get status
4. seek, read, read

OPERATING PROCEDURES :

.R NRLKA0

This program is running under the supervisory program.
This supervisory program will first talk to you.

.....

DR>START <CR>

You have to answer the hardware questions.
This is a (mostly used) example :

Change HW (L) ? Y<CR>

 # UNITS (D) ? 2<CR> (this is the number of drives)

UNIT 0<CR>
RL11 (L) Y ?<CR>
BUS ADDRESS (O) 174400 ? <CR>
VECTOR (O) 160 ? <CR>
DRIVE (O) 0 ? 1<CR>
DRIVE TYPE = RL01 (L) Y ? N
BR LEVEL (O) 5 ? <CR>

UNIT 1

.....

Change SW (L) ? N<CR>

to get a summary type <CONTR C>

DR>PRI

after the summary, to continue type

DR>CON

If you answer Y to the question

CHANGE SW (L) ? Y <CR>

you can change a lot of parameters like:

RETRY LMT (D) 1 ?
TIME BETWEEN REPORTS (MIN) (D) 240 ?

RL01/02 PERFORMANCE EXERCISER

ABSTRACT :

The program tries to simulate a user environment. It will randomly exercise up to 2 controllers and 8 drives. Initialy the bad sector file is read from each drive and stored in memory, then each pack is written with one of eight data patterns. The drives are randomly picked and given a random string function of:

1. *seek, write, write-check*
2. *seek, read data, compare data*
3. *seek, read headers, read 1 sector with no header compare, get status*
4. *seek, read, read*

OPERATING PROCEDURES :

.R ZRLKB3

This program is running under the supervisory program.
This supervisory program will first talk to you.

.....

DR>START <CR>

You have to answer the hardware questions.
This is a (mostly used) example :

CHANGE HW (L) ? Y<CR>

 # UNITS (D) ? 2<CR> (this is the number of drives)

UNIT 0<CR>
RL11 (L) Y ?<CR>
BUS ADDRESS (O) 174400 ? <CR>
VECTOR (O) 160 ? <CR>
DRIVE (O) 0 ? 1<CR>
DRIVE TYPE = RL01 (L) Y ? N
BR LEVEL (O) 5 ? <CR>

UNIT 1
.....

CHANGE SW (L) ? N<CR>

to get a summary type <CONTR C>

DR>PRI

after the summary, to continue type

DR>CON

If you answer Y to the question :

CHANGE SW (L) ? Y <CR>

you can change a lot of parameters like:

RETRY LMT (D) 1 ?
TIME BETWEEN REPORTS (MIN) (D) 240 ?

RL01/02 DRIVE COMPATIBILITY TEST

ABSTRACT :

This program checks that all drives on a computerside are compatible with each other i.e. a drive can read the data written on a other drive. The program attempts to find ten sets of tracks at predetermined spots that contain no bad sectors. The ten sectors are on both surfaces, inner outer and middle cylinders. As the pack is moved between drives the following checks are made:

1. each drive can overwrite each other drive.

2. each drive can read each othes data.

3. each drive can write to the nearby cylinders (written by other drives) without disturbing the others data.

OPERATING PROCEDURES :

.R ZRLLC1

This program is running under the supervisory program.
This supervisory program will first talk to you.

.....

DR>START <CR>

You have to answer the hardware questions.
This is a (mostly used) example :

Change HW (L) ? Y<CR>

 # UNITS (D) ? 2<CR> (this is the number of drives on the System)

UNIT 0<CR>
RL11 (L) Y ?<CR>
BUS ADDRESS (O) 174400 ? <CR>
VECTOR (O) 160 ? <CR>
DRIVE (O) 0 ? 1<CR>
DRIVE TYPE = RL01 (L) Y ? N
BR LEVEL (O) 5 ? <CR>

UNIT 1

.....

You have to unload the drive and move the same pack to the next drive as the program instructs you.

RL01/02 BAD SECTOR FILE UTILITY

ABSTRACT :

This program has the following utilities

1. REPORT CONTENS OF THE BAD SECTOR FILE
2. ADD A SECTOR TO THE 'FIELD' BAD SECTOR FILE
3. DELETE A SECTOR FROM THE 'FIELD' BAD SECTOR FILE
4. VERIFY PACK - READ ONLY
5. WRITE PACK WITH WORST CASE DATA PATTERN AND VERIFY
6. MAKE A BAD SECTOR FILE
7. PRINT HELP MESSAGE

ENTER COMMAND (1 - 7) - (D) ?

Make sure you have a known good drive before using this utility.

The utility 4 is very usefull to verify any data pack with data on. It will report if any data on the pack cannot be read or the CRC on the end is bad. In this case put the drive into write protect mode.
The utility 5 is a good program to test a pack, but this one will read and write

OPERATING PROCEDURES :

.R ZRLMB1

This program is running under the supervisory program.
This supervisory program will first talk to you.

.....

DR>START <CR>
You have to answer the hardware questions.
This is a (mostly used) example :

Change HW (L) ? Y<CR>

 # UNITS (D) ? 1<CR>

UNIT 0<CR>
RL11 (L) Y ?<CR>
BUS ADDRESS (O) 174400 ? <CR>
VECTOR (O) 160 ? <CR>
DRIVE (O) 0 ? 1<CR>
DRIVE TYPE = RL01 (L) Y ? N
BR LEVEL (O) 5 ? <CR>

Then you get the menue, from that you have to select the utility.

RL01/02 DRIVE TEST 3 (SEEK/READ)

ABSTRACT :

This program exercises RL01/02 disk drives on RL11/RLV11 controllers. It starts by testing the simplest functions first using the logic tested in earlier tests to test more complex functions. First it tests seeks then data transfers. It reads the bad sector files into memory and will use this later to prevent testing on bad sectors.

It has 8 subtests:

1. *seek timing*
2. *basic read data test*
3. *write / read data test part 1(with 8 patters)*
4. *rotational timing test*
5. *write /read data test part 2*
6. *write lock error and data protection test*
7. *adjacent cylinder interference test*
8. *overwrite test*

OPERATING PROCEDURES :

.R ZRLNC0

This program is running under the supervisory program.
This supervisory program will first talk to you.

.....

DR>START <CR>

You have to answer the hardware questions.
This is a (mostly used) example :

Change HW (L) ? Y<CR>

 # UNITS (D) ? 2<CR> (this is the number of drives)

UNIT 0<CR>
RL11 (L) Y ?<CR>
BUS ADDRESS (O) 174400 ? <CR>
VECTOR (O) 160 ? <CR>
DRIVE (O) 0 ? 1<CR>
DRIVE TYPE = RL01 (L) Y ? N
BR LEVEL (O) 5 ? <CR>

UNIT 1

. . .

If you answer Y to the question :

CHANGE SW (L) ? Y <CR>

you can change a lot of parameters like:

USE ALL CYL (L) N ?
USE ALL SECT (L) N ?
DO MANUAL INTERVENTION TEST (L) N ?

. . .

if no error found it will print

CZRLN EOP 1
0 TOTAL ERRS

RM02/03/05 PACK FORMATTER PROGRAM

ABSTRACT :

This program formats disk packs either in 16 bit or 18 bit mode and / or performs a check of the pack's surface by reading back the written headers and data bit pattern.
You can select a verify mode only.

NOTE: This program is not intended to be a entire sector verification test, for doing that you need more and different data patterns.

OPERATING PROCEDURES :

START ADDRESSES:
SA = 200 normal starting address (address 176700, vector 254).
SA = 204 non-standard RH11 or RH70 address/vector and to use the bad sector file utility routines.
After start the program prints the UNIT STATUS table

0	*LOAD DEVICE*
1	*ONLINE RM03*
2	*NOT PRESENT*

.....

Now you have to answer the questions printed.

DO YOU WANT TO FORMAT (L) Y ? (<CR> for yes, N for verify only)
DO YOU WANT 16. BIT MODE (L) Y ? (<CR> for yes)

DRIVE :1

CHANGE DRIVE PARAMETERS (L) N ?
If you answer with Y (yes) you can enter address limits and you get the menue of the bad sector file utility.
ENTER ADDRESS LIMITS:

MINCYL	*0 /*
MAXCYL	*822 /*
MINTRK	*0 /*
MAXTRK	*4 /*

FORMAT & HEADER VERIFY, OPERATE IN 16. BIT MODE

SELECT ONE OF THE FOLLOWING FUNCTIONS
you get 5 subprograms to select from.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW13 = 1 inhibit error typeout
SW10 = 1 bell on error
SW09 = 1 loop on error
SW02 = 1 don't display system status after initial start
SW01 = 1 loop on the current track
SW00 = 1 loop the program on selected drive
use "CONTROL G" to enter software SWR at loc. 176

FUNCTIONAL TEST PART 1

ABSTRACT :

This test starts with simple functions like error clear test, diagnostic mode test, pack acknowledge test, recalibrate test, offset test, interrupt test, return to centerline test, seek test look ahead test and so one. Each unit to test must be loaded with a scratch pack.

OPERATING PROCEDURES :

START ADDRESS
SA = 200 normal startaddress (address = 176700, vector = 254)
SA = 204 to change address and vector of the RH/RM
The program will print:

CZRMMB0 - RM05/3/2 FUNCTIONAL TEST, PT 1

SWR = 000000 NEW =
you can change the switch register now.
If you have a switch register on the CPU change it there.

TYPE HELP TEXT (L) N ?

you can answer with 'Y' and it will print the list of all tests and the meaning of the switch settings.

You have to select a drive or type 'A' for all drives.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on specific error
SW08 = 1 loop on test as per SW<07-00>
SW07 = 1 TN 128
SW06 = 1 TN 64
SW05 = 1 TN 32
SW04 = 1 TN 16
SW03 = 1 TN 08
SW02 = 1 TN 04
SW01 = 1 TN 02
SW00 = 1 TN 01

FUNCTIONAL TEST PART 2

ABSTRACT :

This program continues from part 1 and tests mainly write, read and write check operations using headers and data. Select the 'TYPE HELP TEXT (L) N ? to list all tests performed.

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal startaddress (address = 176700, vector = 254)

SA = 204 to change address and vector of the RH/RM

The program will print:

CZRMNBO - RM05/3/2 FUNCTIONAL TEST, PT 2

SWR = 000000 NEW =

you can change the switch register now.
If you have a switch register on the CPU change it there.

TYPE HELP TEXT (L) N ?

you can answer with 'Y' and it will print the list of all tests and the meaning of the switch settings.

You have to select a drive or type 'A' for all drives.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeouts
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on specific error
SW08 = 1 loop on test as per SW<07-00>
SW07 = 1 TN 128
SW06 = 1 TN 64
SW05 = 1 TN 32
SW04 = 1 TN 16
SW03 = 1 TN 08
SW02 = 1 TN 04
SW01 = 1 TN 02
SW00 = 1 TN 01

DISKLESS DCL/RH DIAGNOSTIC PART 1

ABSTRACT :

This program detects failures in the RH massbus controller as well as in the massbus RM adapter. There are 120 (octal) subtests. Select the 'TYPE HELP TEXT (L) N ?' to get the discription of all test.

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal startaddress (address = 176700, vector = 254)

SA = 204 to change address and vector of the RH/RM

The program will print:

CZRMPBO - RM05/3/2 DISKLESS TEST, PT 1

SWR = 000000 NEW =

you can change the switch register now.
If you have a switch register on the CPU change it there.

TYPE HELP TEXT (L) N ?

you can answer with 'Y' and it will print the list of all tests and the meaning of the switch settings.

You have to select a drive or type 'A' for all drives.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeouts
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test as per SW<07-00>
SW07 = 1 TN 128
SW06 = 1 TN 64
SW05 = 1 TN 32
SW04 = 1 TN 16
SW03 = 1 TN 08
SW02 = 1 TN 04
SW01 = 1 TN 02
SW00 = 1 TN 01

DISKLESS DCL/RH DIAGNOSTIC PART 2

ABSTRACT :

This program detects failures in the RH massbus controller as well as in the massbus RM adapter. It continues testing from part 1. There are 24 (octal) subtests. This program is using the maintenance mode of the RM adapter a lot. Answer yes (Y) to: 'TYPE HELP TEXT (L) N ?' to get the discription of all test.

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal startaddress (address = 176700, vector = 254)
SA = 204 to change address and vector of the RH/RM
The program will print:

CZRMQBO - RM05/3/2 DISKLESS TEST, PT 2

SWR = 000000 NEW =

you can change the switch register now.
If you have a switch register on the CPU change it there.

TYPE HELP TEXT (L) N ?

you can answer with 'Y' and it will print the list of all tests and the meaning of the switch settings.

You have to select a drive or type 'A' for all drives.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeouts
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test as per SW<07-00>
SW07 = 1 TN 128
SW06 = 1 TN 64
SW05 = 1 TN 32
SW04 = 1 TN 16
SW03 = 1 TN 08
SW02 = 1 TN 04
SW01 = 1 TN 02
SW00 = 1 TN 01

RM DUAL PORT TEST PART 1

ABSTRACT :

This test performs a series of tests which verify that the RM02/03/05 dual port logic is functioning properly. Only the control logic is tested by this program, data handling in the dual port mode is not tested by this program. Both ports of the drive are cabled to the same massbus by a special cable. This arrangement allows the dual port logic to be tested from one PDP11 / RH11 or RH70. The part 2 performs manual intervention tests.

OPERATING PROCEDURES :

Connect the dual port test cable (P/N: 7010507-02).
Any other drive on the massbus which has an address in conflict with either of the test addresses must be powered down.
I recommend to power down all drives except the one to test.

START ADDRESS
SA = 200 normal startaddress (controller address = 176700, vector = 254)
SA = 204 restart address, the program will use the current drive address.
SA = 210 to allow the address of the RH11 / RH70 to be changed.
The program will print:

CZRMRB0 - RM05/3/2 DUAL PORT LOGIC TEST, PT 1

SWR = 000000 NEW =
you can change the switch register now
or <CR> for no change.
If you have switches on the CPU, change it there.

Enter the drive number.
Enter the test number (<CR> will run all tests).

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error

RM DUAL PORT TEST PART 2

ABSTRACT :

This is part 2 of 2 and is used to test the "DUAL PORT SELECT" switch. This part is the manual intervention part.

OPERATING PROCEDURES :

Connect the dual port test cable (P/N: 7010507-02).
Any other drive on the massbus which has an address in conflict with either of the test addresses must be powered down.
I recommend to power down all drives except the two under test.

START ADDRESS
SA = 200 normal startaddress (controller address = 176700, vector = 254)
SA = 204 restart address, the program will use the current drive address.
SA = 210 to allow the address of the RH11 / RH70 to be changed.
The program will print:

CZRMSB0 - RM05/3/2 DUAL PORT LOGIC TEST, PT 2

SWR = 000000 NEW =
you can change the switch register now
or <CR> for no change.
If you have switches on the CPU, change it there.

Enter the drive number.
Enter the test number (<CR> will run all tests).

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error

RM DRIVE COMPATIBILITY TEST

ABSTRACT :

This program verifies the compatibility of up to 16 RM drives which may reside on 1 or more RH/RM subsystems. Compatibility is defined here as the ability of a drive to write data which can be read successfully by all other drives, and additionally the ability of a drive to completely over-write data written by all other drives. It test specialy :

1. Head mis-alignment
2. Positioner lateral misalignment
3. Spindle-Cartridge interface runout
4. Improper levels of write current
5. incorrect addressing of read/write heads

Testing is done in two passes. In pass 1, compatibility data patterns are written by all the drives upon the same disk pack. In pass 2, the data from all drives is read by each drive, with head offset.

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal startaddress (controller address = 176700, vector = 254)
Here the program assumes that all drives are on this system.
SA = 204 to change RH/RM address and vector and to run pass 1.
SA = 210 to change RH/RM address and vector and to run pass 2.
The program will print:

CZRMTB0 - RM05/3 2 DRIVE COMPATIBILITY TST

SWR = 000000 NEW =
you can change the switch register now
or <CR> for no change.
If you have switches on the CPU, change it there.

SUBSYS "A" DRIVES(S):
Enter how many drives you have on sys A (2,3,5,7<CR>)
Follow all instructions typed by the program.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error typeout
SW12 = 1 inhibit trace trap
SW11 = 1
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 apply random staa between operations
SW07 = 1 type bad sector files at start

RM DRIVE PERFORMANCE EXERCISER

ABSTRACT :

This program is designed to perform an interactive test on RM02/03/05 disk drives connected to a massbus subsystem. You can verify that the drives under test are performing to their data error rate and seek error rate. The program will exercise drives connected as either single or dual port units. Dual port drives are tested by loading and running the program from both controlling systems. Operations on the multi-drive configurations are overlapped (other drives are performing seek/search operations while one drive is performing a data transfer).

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal startaddress (controller address = 176700, vector = 254)
Data patterns will be written to all on-line drives first before the
test goes into testing mode

SA = 204 to change RH/RM address and vector.

The program will print:

CZRMUB0 - RM05/3/2 PERFORMANCE EXERCISER

SWR = 000000 NEW =
you can change the switch register now
or <CR> for no change.
If you have switches on the CPU, change it there.

CHANGE PARAMETERS (L) N ?

KEYBOARD COMMANDS:

Tn = assign drive number "n" for test
Dn = drop drive "n"
Rn = performs a sequential read of a pack in drive "n"
Sn = print performance summary of drive "n"
Wn = write and check data pack with a data pattern in drive "n"
WTn = write and test after drive "n"

SWITCH SETTINGS :

SW15 = 1 halt on error
SW13 = 1 inhibit error typeout
SW10 = 1 bell on error
SW08 = 1 inhibit end of pass message
SW07 = 1 display all data compare errors
SW06 = 1 do not alter the current operation parameters
SW05 = 1 do not display ECC registers in case of errors
SW04 = 1 do not drop drives at end of test / max error count reached
SW03 = 1 display sectors in error
SW02 = 1 inhibit subsystem status report during startup
SW01 = 1 inhibit data compare after read command
SW00 = 1 read only mode

EXTENDED DRIVE TEST

ABSTRACT :

This program tests extensively seek functions, seek timing, track/sector addressing, and that the data storage and retrieval capabilities are functioning properly.

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal startaddress (address = 176700, vector = 254)
SA = 204 select operating parameters
SA = 210 select RH11 / RH70 address and vector
SA = 214 combination of 204 and 210

The program will print:

CZRMVBO - RM05/3/2 EXTENDED DRIVE TEST

SWR = 000000 NEW =
you can change the switch register now.
If you have a switch register on the CPU change it there.

When the program is started from location 200 or 210, tests 0-10, 12, 13, 15-20 will be run using all available online drives. If the operator wishes to select the drives to be tested, the tests to be performed, or the parameters to be used, the conversation mode may be entered by typing a
CONTROL C or by starting the program from either location 204 or 214.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeouts
SW12 = 1 type out test number
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 print error messages on line printer
SW07 = 1 read "C. SWR" settings from TTY
SW06 = 1 inhibit time reports
SW05 = 1 report one error per sector
SW04 = 1 inhibit writes in test 20
SW03 = 1 inhibit writechecks in test 20
SW02 = 1 inhibit read and software compare in test 20
SW01 = 1 inhibit software compare in test 20
SW00 = 1 perform read after write check in test 20

RM80 PERFORMANCE EXERCISER

ABSTRACT :

This program is designed to perform an interactive test on RM80 disk drives connected to a massbus subsystem. You can verify that the drives under test are performing to their data error rate and seek error rate. The program will exercise drives connected as either single or dual port units. Dual port drives are tested by loading and running the program from both controlling systems. Operations on the multi-drive configurations are overlapped (other drives are performing seek/search operations while one drive is performing a data transfer).

OPERATING PROCEDURES :

.R ZRNAA0

START ADDRESS

SA = 200 normal startaddress (controller address = 176700, vector = 254)
Data patterns will be written to all on-line drives first before the test goes into testing mode

SA = 204 to change RH/RM80 address and vector.
The program will print:

CZRNAA0 - RM80 PERFORMANCE EXERCISER

SWR = 000000 NEW =
you can change the SWR now or <CR> for no change.
If you have switches on the CPU, change it there.

DO YOU WISH TO EXERCISE ONLY FE CYLINDERS (L) Y ?
CHANGE PARAMETERS (L) N ?
KEYBOARD COMMANDS:
To get into command mode during testing, type a "CONTROL C"

Tn = assign drive number "n" for test
Dn = drop drive "n"
Rn = performs a sequential read of a pack in drive "n"
Sn = print performance summary of drive "n"
Wn = write and check data pack with a data pattern in drive "n"
WTn = write and test after drive "n"

SWITCH SETTINGS :

SW15 = 1 halt on error
SW13 = 1 inhibit error typeout
SW10 = 1 bell on error
SW08 = 1 inhibit end of pass message
SW07 = 1 display all data compare errors
SW06 = 1 do not alter the current operation parameters
SW05 = 1 do not display ECC registers in case of errors
SW04 = 1 do not drop drives at end of test / max error count reached
SW03 = 1 display sectors in error
SW02 = 1 inhibit subsystem status report during startup
SW01 = 1 inhibit data compare after read command
SW00 = 1 read only mode

DISKLESS RM-ADAPTER / RH DIAGNOSTIC PART 1

ABSTRACT :

This program detects failures in the RH massbus controller as well as in the massbus RM adapter. There are 120 (octal) subtests. Select the 'TYPE HELP TEXT (L) N ?' to get the discription of all test.

OPERATING PROCEDURES :

.R ZRNBA0

START ADDRESS
SA = 200 normal startaddress (address = 176700, vector = 254)
SA = 204 to change address and vector of the RH/RM
The program will print:

CZRNBAO - RM80 DISKLESS TEST, PT 1

SWR = 000000 NEW =
you can change the switch register now.
If you have a switch register on the CPU change it there.

TYPE HELP TEXT (L) N ?

you can answer with 'Y' and it will print the list of all tests and the meaning of the switch settings.

You have to select a drive or type 'A' for all drives.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeouts
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SW<07-00>
SW07 = 1 TN 128
SW06 = 1 TN 64
SW05 = 1 TN 32
SW04 = 1 TN 16
SW03 = 1 TN 08
SW02 = 1 TN 04
SW01 = 1 TN 02
SW00 = 1 TN 01

DISKLESS RM-ADAPTER / RH DIAGNOSTIC PART 2

ABSTRACT :

This program detects failures in the RH massbus controller as well as in the massbus RM adapter. It continues testing from part 1. There are 24 (octal) subtests. This program is using the maintenance mode of the RM adapter a lot. Answer yes (Y) to: 'TYPE HELP TEXT (L) N ?' to get the discription of all test.

OPERATING PROCEDURES :

.R ZRNCA0

START ADDRESS
SA = 200 normal startaddress (address = 176700, vector = 254)
SA = 204 to change address and vector of the RH/RM
The program will print:

CZRNCA0 - RM80 DISKLESS TEST, PT 2

SWR = 000000 NEW =
you can change the switch register now
If you have a switch register on the CPU change it there.

TYPE HELP TEXT (L) N ?

you can answer with 'Y' and it will print the list of all tests and the meaning of the switch settings.

You have to select a drive or type 'A' for all drives.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeouts
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test as per SW<07-00>
SW07 = 1 TN 128
SW06 = 1 TN 64
SW05 = 1 TN 32
SW04 = 1 TN 16
SW03 = 1 TN 08
SW02 = 1 TN 04
SW01 = 1 TN 02
SW00 = 1 TN 01

RM80 FUNCTIONAL TEST PART 1

ABSTRACT :

This is the first of 4 programs, which would normaly be run in sequence, starting with part 1. Briefly, part 1 tests housekeeping and mecanical positioning operations like controller clear test, pack acknowledge test, recalibrate test, offset test, return to centerline test, seek test, search test and so on. There are 67 (octal) subtests in part 1.

OPERATING PROCEDURES :

.R ZRNDA0

START ADDRESS
SA = 200 normal startaddress (address = 176700, vector = 254)
SA = 204 to change address and vector of the RH/RM
The program will print:

CZRNDA0 - RM80 FUNCTIONAL TEST, PT 1

SWR = 000000 NEW =
you can change the switch register now.
If you have a switch register on the CPU change it there.

TYPE HELP TEXT (L) N ?

you can answer with 'Y' and it will print the list of all tests and the meaning of the switch settings.

You have to select a drive or type 'A' for all drives.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeouts
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test as per SW<07-00>
SW07 = 1 TN 128
SW06 = 1 TN 64
SW05 = 1 TN 32
SW04 = 1 TN 16
SW03 = 1 TN 08
SW02 = 1 TN 04
SW01 = 1 TN 02
SW00 = 1 TN 01

RM80 FUNCTIONAL TEST PART 2

ABSTRACT :

This is the second of 4 programs, which would normaly be run in sequence, starting with part 1. Briefly, part 2 tests write, read and write check operations like format test, read header test, read invalid sector test, format FE cylinder test and so on. There are 31 (octal) subtests in part 2.
This test does not overwrite customer data.

OPERATING PROCEDURES :

.R ZRNEA0

START ADDRESS
SA = 200 normal startaddress (address = 176700, vector = 254)
SA = 204 to change address and vector of the RH/RM
The program will print:

CZRNEA0 - RM80 FUNCTIONAL TEST, PT 2

SWR = 000000 NEW =
you can change the switch register now.
If you have a switch register on the CPU change it there.

TYPE HELP TEXT (L) N ?
you can answer with 'Y' and it will print the list of all tests and the meaning of the switch settings.

You have to select a drive or type 'A' for all drives.

The program must be halted only by typing "CONTROL C" on the console, otherwise bad header information may be left on the disk.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeouts
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test as per SW<07-00>
SW07 = 1 TN 128
SW06 = 1 TN 64
SW05 = 1 TN 32
SW04 = 1 TN 16
SW03 = 1 TN 08
SW02 = 1 TN 04
SW01 = 1 TN 02
SW00 = 1 TN 01

RM80 FUNCTIONAL TEST PART 3

ABSTRACT :

This is the third of 4 programs, which would normaly be run in sequence, starting with part 1. Briefly, part 3 tests write, read and write check operations using data pattrens, and forcing different error conditions. There are 23 (octal) subtests in part 3.
This test does not overwrite customer data. All data transfers will be performed on the FE cylinders only.

OPERATING PROCEDURES :

.R ZRNFA0

START ADDRESS
SA = 200 normal startaddress (address = 176700, vector = 254)
SA = 204 to change address and vector of the RH/RM
The program will print:

CZRNFA0 - RM80 FUNCTIONAL TEST, PT 3

SWR = 000000 NEW =
you can change the switch register now.
If you have a switch register on the CPU change it there.

TYPE HELP TEXT (L) N ?
you can answer with 'Y' and it will print the list of all tests and the meaning of the switch settings.

You have to select a drive or type 'A' for all drives.

The program must be halted only by typing "CONTROL C" on the console, othervise bad header information may be left on the disk.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeouts
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test as per SW<07-00>
SW07 = 1 TN 128
SW06 = 1 TN 64
SW05 = 1 TN 32
SW04 = 1 TN 16
SW03 = 1 TN 08
SW02 = 1 TN 04
SW01 = 1 TN 02
SW00 = 1 TN 01

RM80 FUNCTIONAL TEST PART 4

ABSTRACT :

This is the last of 4 programs, which would normaly be run in sequence, starting with part 1. Briefly, part 4 tests seeks, checks that seek times are within tolerance and that the track/sector addressing circuitry operates properly. There is absolutely no writting of data involved in this program. There are 15 (octal) subtests in part 4.
This test does not overwrite customer data.

OPERATING PROCEDURES :

.R ZRNGA0

START ADDRESS
SA = 200 normal startaddress (address = 176700, vector = 254)
SA = 204 select operating parameters
SA = 210 select RH controller addresses
SA = 214 combination of 204 and 210

The program will print:

CZRNGA0 - RM80 FUNCTIONAL TEST, PT 4

SWR = 000000 NEW =
you can change the switch register now.
If you have a switch register on the CPU change it there.

You have to select a drive or type 'A' for all drives.

SWITCH SETTINGS :
SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeouts
SW12 = 1 type test number
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 print error message on line printer
SW07 = 1 read "C.SWR" settings from TTY
SW06 = 1 inhibit time reports (test 11-15)

CONTROL SWITCH SETTINGS :
SW06 = 1 50 Hz power source (for seek timing)
SW06 = 0 60 Hz power source (for seek timing)

RM80 DUAL PORT TEST PART 1

ABSTRACT :

This test performs a series of tests which verify that the RM80 dual port logic is functioning properly. Only the control logic is tested by this program, data handling in the dual port mode is not tested by this program. Both ports of the drive are cabled to the same massbus by a special cable. This arrangement allows the dual port logic to be tested from one PDP11 / RH11 or RH70. The part 2 performs manual intervention tests.

OPERATING PROCEDURES :

Connect the dual port test cable. (P/N: 7010507-02).
Any other drive on the massbus which has an address in conflict with either of the test addresses must be powered down.
I recommend to power down all drives except the one to test.

.R ZRNHA0

START ADDRESS
SA = 200 normal startaddress (controller address = 176700, vector = 254)
SA = 204 restart address, the program will use the current drive address.
SA = 210 to allow the address of the RH11 / RH70 to be changed.
The program will print:

CZRNHA0 - RM80 DUAL PORT LOGIC TEST, PT 1

SWR = 000000 NEW =
you can change the switch register now
or <CR> for no change.
If you have switches on the CPU, change it there.

Enter the drive number.
Enter the test number (<CR> will run all tests).

SWITCH SETTINGS :
SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error

RM80 DUAL PORT TEST PART 2

ABSTRACT :

This is part 2 of 2 and is used to test the "DUAL PORT SELECT" switch. This part is the manual intervention part.

OPERATING PROCEDURES :

Connect the dual port test cable (P/N: 7010507-02).
Any other drive on the massbus which has an address in conflict with either of the test addresses must be powered down.
I recommend to power down all drives except the one to test.

.R ZRNIA0

START ADDRESS
SA = 200 normal startaddress (controller address = 176700, vector = 254)
SA = 204 restart address, the program will use the current drive address.
SA = 210 to allow the address of the RH11 / RH70 to be changed.
The program will print:

CZRNIA0 - RM80 DUAL PORT LOGIC TEST, PT 2

SWR = 000000 NEW =
you can change the switch register now
or <CR> for no change.
If you have switches on the CPU, change it there.

Enter the drive number.
Enter the test number (<CR> will run all tests).

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeout
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error

RM80 HDA FORMATTER PROGRAM

ABSTRACT :

This program is a reconstruction process for 16 bit applications that re-establishes the factory format of a HDA. This is not a troubleshooting tool, also HDA's should not be formatted unless the existing format has been damaged by hardware or software failures. Manufacturing has much better methods and equipment to scan a HDA for bad or marginal sectors (which can be sometimes be read and sometimes not) than we in the field. So always remember, do not format any HDA unless you realy have a good reason to do so.

NOTE: This program is not intended to be a entire sector verification test, for doing that you need more and different data patterns.

OPERATING PROCEDURES :

.R ZENJB0

After start the program prints:

CZRNJB0 - RM80 FORMATTER UTILITY

DRIVE #:
enter the drive number address followed by a <CR>

OPTIONS:
the following commands are available:

IN	*initialize the bad sector file. This will destroy the contens of all the bad sector files.*
FO	*format the disk (all cylinders 0-560)*
FO:F	*format the FE cylinders only (cyl. 559 trk.2 - cyl 560 trk 13)*
LI	*list the physical addresses of the defects in all bad sector files.*
LI:L	*list the logical addresses of the defects in all bad sector files.*
VFL=N	*verify / how many times to read the data in verify mode.*
ERL=N	*error limit count before the format is aborted.*
CSR=N	*RM base address (default is 176700)*
VEC=N	*RM vector address (default is 254)*

EXAMPLE :

OPTION: FO/CSR=176000/VEC=260/VFL=3/ERL=10<CR>

RQDX/RUX50/RX/RD ZRQAH0

RQDX1/2/3, RUX50, RX50, RD51, RD52 EXERCISER

ABSTRACT :

This program is a subsystem performance exerciser testing the RQDX1/2/3 or RUX50 controller with RD51, RD52 and/or RX50 connected. It tries to simulate a user environment. It will test up to 4 units (drives) For the winchester drives you can specify not to overwrite customer data.

OPERATING PROCEDURES :

.R ZRQAH0

This program is running under the supervisory program.
This supervisory program will first talk to you.

DRSSM-G1
CZRQA-H-0
RD/RX EXERCISER
UNIT IS RQDX or RUX50
RESTART ADDRESS 145702
DR>

You have to answer the hardware questions.
For each drive to test you have to answer the 7 questions.

DR>START<CR>

Change HW (L) ? Y<CR>

 # UNITS (D) ? 3<CR> *drives to test (RX50 is 2 units)*
IP ADDRESS (0) 172150 ? <CR>
VECTOR ADDRESS (0) 154 ? <CR>
BR LEVEL [USUALLY 4-RQDX 5-RUX50] (D) 4 <CR>
DRIVE NUMBER (D) 0 ?

RDxx usually 0 / RX50 usally 1 and 2

TEST ENTIRE CUSTOMER DATA AREA OF THIS DISK (L) ? N

if you answer with "Y" yes then it will overwrite the entire disk, if you answer "N" no, then you can enter limits (LBN's)

WRITE ON CUSTOMER DATA AREA ON THIS DISK UNIT (L) ?

answer with "N" if customer data have to be retained.

Change SW (L)

Here you can enter time, error limits, transfer limits, halt on bad blocks hard errors and so on.

It will print a nice statistic every aprox. 15 seconds.

RQDX1/2 RD51/52 FORMATTER

ABSTRACT :

This program is the front end which invokes the formatter for the RD51/52 in the RQDX1/2. It interfaces with the actual formatter which is in the controller. This program in the RQDX will prompt for any information it needs, and then begins running. A run consists of marking the disk as unformatted, formatting it running three passes of a surface analysis, saving the FCT and RCT, and marking the disk as formatted.

OPERATING PROCEDURES :

.R ZRQBC1

This program is running under the supervisory program.
This supervisory program will first talk to you.

ZRQB-C-1
RD51/52 DISK FORMATTER
UNIT IS RQDX1 DISK DRIVE SUBSYSTEM
RESTART ADDRESS 145702
DR>STA<CR>

You have to answer the hardware questions.

Change HW (L) ? Y<CR>

Answer no to use the pre-built answers for all hardware questions.
This program is pre-build to format unit 0 with default answers.

** UNITS (D) ? 1<CR>*
UNIT 0
IP REGISTER ADDRESS (0) 172150 ? <CR>
INTERRUPT VECTOR ADDRESS (0) 154 ? <CR>
BUS REQUEST LEVEL (O) 4 <CR>

CHANGE SW (L) N

For fieldservice use a "N" for no.
Now the formatter of the RQDX will talk to you (not supervisor)

The questions asked depend on the version of the controller microcode in the RQDX. When the controller is first initialized, the host determines which version (8 or 9) is running.

ENTER DATE <MM-DD-YYYY> (A) ? 03-13-1987
ENTER UNIT NUMBER TO FORMAT <0> : (D) 0 ? 0
USE EXISTING BAD BLOCK INFORMATION <N>: (L) Y ?

trie first with "Y" if error then trie "N"

USE DOWN-LINE LOAD <N>: (L) N ?
CONTINUE IF BAD BLOCK INFORMATION IS INACCESSABLE <N>: (L) N ?
ENTER NON ZERO SERIAL NUMBER : 533885

FORMAT BEGUN
FORMAT COMPLETE

RQDX3 RD51/52/53/54 ZRQCF0

RQDX3 RD31/51/52/53/54/RX33 FORMATTER

ABSTRACT :

This program is the front end which invokes the formatter in the RQDX3. This formatter is different from the RQDX1/2 one. Also a disk on a RQDX1/2 has an other format structure then one on a RQDX3, it needs reformatting if you change the controller from RQDX1/2 to RQDX3. The RQDX3 controller has more functionality in it like getting the UIT (UNIT IDENTIFICATION TABLE) from a disk into the controller. This program in the RQDX3 will prompt for any information it needs, and then begins running. A run consists of marking the disk as unformatted, formatting it, running several passes of a surface analysis, saving the FCT (factory control table)(except RD51 which has no FCT) and RCT (replacement control table), and marking the disk as formatted. There is a lot more to know about this formatter but due to lack of space can not be explaned here.

OPERATING PROCEDURES :

This program is running under the supervisory program.
This supervisory program will first talk to you.

ZRQC-F-0
RQDX3 DISK FORMAT/PARK DISK UTILITY
UNIT IS RD51, RD52, RD53, RD31, RD54, RX33
RESTART ADDRESS 145702
DR>STA<CR>

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
IP REGISTER ADDRESS (0) 172150 ? <CR>
INTERRUPT VECTOR ADDRESS (0) 154 ? <CR>
JUST PARK THE HEADS (L) N ? N

for shipping the drive place the heads in the park position.

AUTO FORMAT MODE (L) Y ? Y

You can run the "AUTOSIZER". This will give you a nice list what disktype he found on the RQDX3.

LOGICAL DRIVE (0-255) (D) 0 ?
DRIVE SERIAL NUMBER (1-32000) (D) ?
AUTOSIZER FOUND:

Types a nice table

WARNING ALL DATA ON DISK WILL BE DESTROYED, CONTINUE ? N ? Y
MSCP CONTROLLER MODEL #: 19
MICROCODE VERSION #: 2

FORMAT BEGUN
PASS 00003 BEG

If you get the message: no progress shown after a cmd timeout leave it running for some minutes.

PASS 00005 BEG
FORMAT COMPLETE

Finaly you get the table about the bad LBNs, RBNs, DBNs.
LBN = logical block number, RBN = replacement bn, DBN = diagnostic bn.

RQDX1/2 RUX50 ZRQDA0

RQDX1/2 RUX50 RD51/52/53/RX50 SUBSYSTEM EXERCISER

ABSTRACT :

This program consists of two parts. The initialization test is running first. This first checks out the controller,

OPERATING PROCEDURES :

.R ZRQDA0

This program is running under the supervisory program.
This supervisory program will first talk to you.

ZRQD-A-0
RD/RX EXERCISER
UNIT IS RD51, RD52, RD53, RD31, RD54, RX33
RESTART ADDRESS 145702
DR>STA<CR>

You have to answer the hardware questions.

Change HW (L) ? N<CR>

answer N to run the pre-build configuration of 4 drives.
this does not write on customer data area.

 # UNITS (D) ? 2<CR>

answer how many disk to test.

UNIT 0
IP REGISTER ADDRESS (0) 172150 ? <CR>
VECTOR ADDRESS (0) 154 ? <CR>
BR LEVEL [usually 4-RQDX 5-RUX50] (O) 4 ?
DRIVE NUMBER (D) 0 ?
ALSO RUN DUP EXERCISER (L) Y ?

Only the DUP exer. uses DBNs (diagnostic blocks) for writes.
to Tests writes without deleting customer data.

WRITE ON DIAGNOSTIC AREA (L) Y ?
TEST ENTIRE CUSTOMER DATA AREA OF THIS DISK (L) Y ?

if you say no you can specify a area (start LBN, end LBN)

WRITE ON CUSTOMER DATA AREA ON THIS DISK UNIT (L) ?
***WARNING - CUSTOMER DATA WILL BE OVERWRITTEN...CONFIRM (L) ?*

CHANGE SW (L) N

Every 20 second you will get a nice summary
The upper table is from the normal MSCP test
The lower one is from the DUP test.

There are 4 types of errors:

System fatal errors detected by the diagn. supervisor
Drive fatal errors
Hard error (non recoverable softerror)
Softerrors (normaly media related) reported by MSCP

RX33 FORMATTER

ABSTRACT :

This program is the front end which invokes the formatter for the RX33 in the RQDX3. This program will never work on the RQDX1/2. This formatter uses the DUP protocol to answer questions asked by the format program in the controller microcode. This program in the RQDX will prompt for any information it needs, and then begins running. Once online, all available blocks on the diskette are tested by a series of MSCP read and write commands. If any bad blocks are found, the diskette should be disgarded.

OPERATING PROCEDURES :

```
.R ZRQFC0

                This program is running under the supervisory program.
                This supervisory program will first talk to you.
ZRQF-C-0
RQDX3 RX33 FORMAT UTILITY
UNIT IS RX33
RESTART ADDRESS 145702
DR>-STA<CR>
                You have to answer the hardware questions.

CHANGE HW (L) ? Y<CR>

# UNITS (D) ? 1<CR>
UNIT 0
IP REGISTER ADDRESS (0) 172150 ? <CR>
INTERRUPT VECTOR ADDRESS (0) 154 ? <CR>
LOGICAL DRIVE (0-255) (D) 1 ?

WARNING - REMOVE BOOT DISKETTE IF IN DRIVE....
INSERT DISKETTE TO BE FORMATTED.

MSCP CONTROLLER MODEL #: 19
MICROCODE VERSION #: 2

FORMAT BEGUN

FORMAT COMPLETE
```

RH11 RS03/04 BASIC FUNCTION TEST

ABSTRACT :

This program verifies that the RH11 controller and the RS03, RS04 disks are operating correctly. This is not a reliability diagnostic. It can test up to 8 drives mixed RS03 and RS04.

OPERATING PROCEDURES :

.R ZRSBH0

all switches down or zero for worst case
The program will run and bell will ring once every pass.

SA = 220 write lock test

Starting addresses for testing the RH11-RS03/04 registers using the switch register.

250	*word count register test*
254	*bus address register test*
260	*disk address register test*
264	*drive status register test*
270	*error register test*
274	*look ahead register test*
300	*RSCS2 register test*
304	*attention register test*
310	*maintenance register test*
314	*RSCS1 register test*

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit typeouts
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test as per SW<07-00>r

use "CONTROL G" to enter software SWR at loc. 176

RH11 RS03/04 DATA RELIABILITY TEST

ABSTRACT :

This program verifies that the RH11 controller and the RS03, RS04 disk are operating correctly. This is a reliability diagnostic with a series of disk address and data pattern tests. If there is a power fail while the diagnostic is running, the program will wait for approx. 5 minutes, to give all the drives time to come back up to speed, before restarting the test sequence. With the swich 10 up you will get into the conversational mode where you can change program parameters, like MULTI DRIVE MODE ?, UNIT # ?, WD CT ?, PATTERN, ...

OPERATING PROCEDURES :

.R ZRSCG0

all switches down or zero for worst case

The program will now map the data buffers in 4k segments up to 124k. It will then type out the parameters of the data buffers.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on function
SW13= 1 inhibit typeouts
SW12= 1 inhibit comparison in memory
SW11= 1 halt on completion of transfer
SW10= 1 enter conversational mode
SW09= 1 loop on error
SW08= 1 data reliability mode
SW07= 1 wait in wait mode for interrupt (waitinstruction)
SW06= 1 optional typeout of retry errors
SW05= 1 inhibit pass count
SW04= 1 allow 8 errors typeout in the compare routine
SW03= 1 typeout # of errors
SW02= 1 inhibit memory management
SW01= 1 data test only
SW00= 1 drop drive after 20 errors

use "CONTROL G" to enter software SWR at loc. 176

RH11 RS04 MAINTENANCE MODE DIAGNOSTIC

ABSTRACT :

This program has two modes. The operator may select which drive he wants tested or he can let the program sequence through all the drives on the system. The first part of this diagnostic will test the drive registers associated with the drive under test. The program will also test the HH controller registers to confirm that the controller is working correctly. The second part of this diagnostic will test the drive in maintenance mode. This "MAINTENANCE MODE" test capability isolates the digital electronics from the analog and allows independent testing of the digital logic.

OPERATING PROCEDURES :

.R ZRSDC0

The program will type :
TEST ALL DRIVES ? (Y or N)
If the operator types "Y" it will test all drives
If the operator types "N" the program will type
TYPE UNIT #
Tests only that drive ; program prints
ALL ERROR LIGHTS ON SELECTED UNIT SHOULD BE ON
-CHECK- THEN HIT CONTINUE

SA = 220
The program will then test all RS04 drives on the system.

SWITCH SETTINGS : /

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit typeouts
SW12 = 1 typeout all errors in data compare routine
SW11 = 1 run maintenance mode verify test
SW10 = 1 bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test in SW <7:0>

use "CONTROL G" to enter software SWR at loc. 176

RX11/RX01 SYSTEM RELIABILITY TEST

ABSTRACT :

This program checks the RX11 system by writing, reading and verifying various data patterns under various head movements. It can transfer data and checks for errors over the entire diskette, tracks and sectors. A diskette must be inserted in each drive to test.

OPERATING PROCEDURES :

START ADDRESSES:

SA = 200 normal starting
SA = 202 restart address
SA = 204 dump all errors collected

Standard address RXCS = 177170, RXDB = 177172, Vector = 264
If you have non standard address modify memory location
loc 1204 for new vector
loc 1206 for new address RXCS
loc 1210 for new address RXDB

loc 1212 contains parameter bits
bit 15 (1) 1000000 select drive unit 1
bit 14 (1) 400000 select drive unit 0

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 halt at end of pass
SW13 = 1 inhibit typeouts
SW12 = 1 typeout only 10 data errors
SW11 = 1 no retry on error, log hard error
SW08 = 1 no recalibr. on seek errors

use "CONTROL G" to enter software SWR at loc. 176

RX11 INTERFACE TEST

ABSTRACT :

This program checks the RX11 interface M7846. It tests the done flag, interrupt address and level, initialization, read status register, fill and empty data buffer with data patterns. A diskette must be inserted in each drive to test.

OPERATING PROCEDURES :

.R ZRXBF0

SA = 202 restart address

Standard address RXCS = 177170, RXDB = 177172, Vector = 264
If you have non standard address modify memory location
loc 1204 for new vector
loc 1206 for new address RXCS
(RXDB is calculated from RXCS)

loc 1212 contains parameter bits (a 0= test both units)
bit 15 (1) 1000000 select drive unit 1
bit 14 (1) 400000 select drive unit 0

End of pass message is a "D" and the bell rings.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 halt at end of pass
SW13 = 1 inhibit typeouts
SW12 = 1 loop on test
SW11 = 1 lock on error
SW10 = 1 halt at end of test
SW09 = 1 limit data error printout
SW08 = 1 inhibit recalibration
SW00 = 1 inhibit bell on error

use "CONTROL G" to enter software SWR at loc. 176

11/21 - RX02 PERFORMANCE EXERCISER

ABSTRACT :

This program exercises up to 4 RX02 drives, maintains drive statistics and provides run summaries. It will give the user confidence, after successfully running, that the subsystem is performing within specification.

OPERATING PROCEDURES :

This program is running under the supervisory program.
This supervisory program will first talk to you.

```
.R NRXDA0

DRSSM-G1
CNRXDA0-0
RX02 SS PERF EXER
UNIT IS RX02
RSTRT ADR 145702
DR>
```

You have to answer the hardware questions.
This is a (mostly used) example :

```
DR>STA<CR>
CHANGE HW (L) ? Y<CR>
# UNITS (D) 2<CR>              (how many drives ?)

UNIT 0
RX BUS ADR (O) 177170 ?<CR>
VECTOR ADR (O) 264 ?<CR>
DRIVE # (O) 0 ? 0<CR>
EXP WRD-CR (O) 0 ? <CR>        (for future expansion)

UNIT 1
RX BUS ADR (O) 177170 ?<CR>
VECTOR ADR (O) 264 ?<CR>
DRIVE # (O) 0 ? 1<CR>
EXP WRD-CR (O) 0 ? <CR>        (for future expansion)

CHANGE SW (L) ? N<CR>
```

After about 30 minutes (CPU depend.) it will print a statistical report.
To get one any time, type <CONTR. C>

```
DR>PRI<CR>
```

The test starts with Unit 0 (drive 0) and changes after about 15 min. to Unit 1 (drive 1).

11/21 - RXV21/RX02 FUNCTIONAL / LOGIC TEST

ABSTRACT :

This program consists of a function test and a logic test. The user can select to run either or both: The diagnostic defaults to run the logic test. It exercises up to 4 RX02 drives.

OPERATING PROCEDURES :

This program is running under the supervisory program.
This supervisory program will first talk to you.

```
.R NRXFA0

DRSSM-G1
CNRXFA0-0
RX02 FUNCTION-LOGIC TEST
UNIT IS RX02
RSTRT ADR 145702
DR>
```

You have to answer the hardware questions.
This is a (mostly used) example :

```
DR>STA<CR>
CHANGE HW (L) ? Y<CR>
# UNITS (D) 2<CR>          (how many drives ?)

UNIT 0
RX BUS ADR (O) 177170 ?<CR>
VECTOR ADR (O) 264 ?<CR>
DRIVE # (O) 0 ? 0<CR>
EXP WRD-CR (O) 0 ? <CR>  (for future expansion)
BR-LEVEL (O) 5 ? <CR>

UNIT 1
RX BUS ADR (O) 177170 ?<CR>
VECTOR ADR (O) 264 ?<CR>
DRIVE # (O) 0 ? 1<CR>
EXP WRD-CR (O) 0 ? <CR>  (for future expansion)
BR-LEVEL (O) 5 ? <CR>

CHANGE SW (L) ? N<CR>    here you have the following options:

TEST HELP ?
LOGIC TEST MODE ?
FUNCTION TEST MODE ?
DEVICE FATAL THRESHOLD LEVEL ?
.....
```

The test starts with Unit 0 (drive 0) and changes after about 15 min. to Unit 1 (drive 1).

RX02 PERFORMANCE EXERCISER

ABSTRACT :

This program exercises up to 4 RX02 drives, maintains drive statistics and provides run summaries. It will give the user confidence, after successfully running, that the subsystem is performing within specification.

OPERATING PROCEDURES :

This program is running under the supervisory program.
This supervisory program will first talk to you.

```
DRSSM-G1
CZRXDC0-0
RX02 SS PERF EXER
UNIT IS RX02
RSTRT ADR 145702
DR>
```

You have to answer the hardware questions.
This is a (mostly used) example :

```
DR>STA<CR>
CHANGE HW (L) ? Y<CR>
# UNITS (D) 2<CR>              (how many drives ?)

UNIT 0
RX BUS ADR (O) 177170 ?<CR>
VECTOR ADR (O) 264 ?<CR>
DRIVE #  (O) 0 ? 0<CR>
EXP WRD-CR (O) 0 ? <CR>        (for future expansion)

UNIT 1
RX BUS ADR (O) 177170 ?<CR>
VECTOR ADR (O) 264 ?<CR>
DRIVE # (O) 0 ? 1<CR>
EXP WRD-CR (O) 0 ? <CR>        (for future expansion)

CHANGE SW (L) ? N<CR>
```

After about 30 minutes (CPU depend.) it will print a statistical report.
To get one any time, type <CONTR. C>

```
DR>PRI<CR>
```

The test starts with Unit 0 (drive 0) and changes after about 15 min. to Unit 1 (drive 1).

RX02 FORMAT CHANGE UTILITY

ABSTRACT :

This program is a utility to change a single density diskette to doube density (default) or vis versa on both drives. After, it verifies the diskette. This is not a real formatting (writing headers).

OPERATING PROCEDURES :

.R ZRXEA2

Start address 210 = restart address
Start address 220 = debug mode

It will type "HELP ? (Y or N)
It will type a nice help text if you answer with Y

SET DISKETTE TO SINGLE DENSITY ? (Y OR N) N<CR>
VERIFY DISKETTE CRC (ALL TRACKS)? (Y OR N) Y<CR>
FLOPPY DISK SYSTEM: 0 ADDRESS CHANGE? (Y OR N) N<CR>

FORMAT DONE ON FOLLOWING
SYSTEM:0 DRIVE:0 DRIVE:1

FORMAT COMPLETED
DO YOU WANT TO FORMAT MORE DISKETTES? (Y OR N) N Y<CR>

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 extended error reports
SW13 = 1 inhibit error reports
SW12 = 1 bus init on error if loop
SW11 = 1 not used
SW09 = 1 loop on error

RXV21/RX211 RX02 FUNCTIONAL / LOGIC TEST

ABSTRACT :

This program consists of a function test and a logic test. The user can select to run either or both. The diagnostic defaults to run the logic test. It exercises up to 4 RX02 drives.

OPERATING PROCEDURES :

This program is running under the supervisory program.
This supervisory program will first talk to you.

DRSSM-G1
CZRXFB0-0
RX02 FUNCTION-LOGIC TEST
UNIT IS RX02
RSTRT ADR 145702
DR>

You have to answer the hardware questions.
This is a (mostly used) example :

DR>STA<CR>
CHANGE HW (L) ? Y<CR>
 # UNITS (D) 2<CR> *(how many drives ?)*

UNIT 0
RX BUS ADR (O) 177170 ?<CR>
VECTOR ADR (O) 264 ?<CR>
DRIVE # (O) 0 ? 0<CR>
EXP WRD-CR (O) 0 ? <CR> *(for future expansion)*
BR-LEVEL (O) 5 ? <CR>

UNIT 1
RX BUS ADR (O) 177170 ?<CR>
VECTOR ADR (O) 264 ?<CR>
DRIVE # (O) 0 ? 1<CR>
EXP WRD-CR (O) 0 ? <CR> *(for future expansion)*
BR-LEVEL (O) 5 ? <CR>

CHANGE SW (L) ? N<CR> here you have the following options:

TEST HELP ?
LOGIC TEST MODE ?
FUNCTION TEST MODE ?
DEVICE FATAL THRESHOLD LEVEL ?
.....

The test starts with Unit 0 (drive 0) and changes after about 15 min. to Unit 1 (drive 1).

UDA50/KDA50/RAxx BASIC SUBSYSTEM DIAGNOSTIC

ABSTRACT :

This diagnostic is testing the UDA50A or the KDA50-Q disk controller and the associated disk drives. There are three tests within this diagnostic :

Test 1 : Buss addressing test. Runs the UDA50 or KDA50 ROM resident diagnostic, then further tests the bus address interface and controller memory.

Test 2 : Disk resident diagnostic test, executes the diagnostic in each disk drive.

Test 3 : Disk function test. Functionaly tests each disk drive to ensure the drive can seek, read, write and format.

OPERATING PROCEDURES :

```
.R ZUDHA1

        This program is running under the supervisory program.
        This supervisory program will first talk to you.
CZUDH-A-1
CZUDHA0 UDA50A,KDA50-Q BASIC SUBSY
UNIT IS LOGICAL DISK DRIVE
RSTRT ADR 145702
DR>STA/FLAG:PNT<CR>     start, print test NR

CHANGE HW (L) ? Y
#UNITS (D) ? 1<CR>      disk drives

UNIT 0
CSR ADDRESS OF CONTROLLER (O) 172150 ?<CR>
VECTOR (O) 154 ?<CR>
BR LEVEL (D) 5 ?<CR>
DRIVE # (D) 0 ?<CR>

CHANGE SW (L) ? Y

ENTER MANUAL INTERVENTION MODE IN TEST 2 (L) N ?
```

UDA50/KDA50/RAxx ZUDIA0

UDA50/KDA50/RAxx DISK EXERCISER

ABSTRACT :

This diagnostic is testing the UDA50A or the KDA50-Q disk controller and the associated disk drives. There is only one test within this diagnostic :

Test 1 : Exercises the disk drives in a manner similar to normal operating systems. This test should be used to gain confidence in the reliability of the disk drive.

OPERATING PROCEDURES :

.R ZUDIA0

This program is running under the supervisory program. This supervisory program will first talk to you.

CZUDI-A-0
CZUDIA0 UDA50A,KDA50-Q DRIVE EXER
UNIT IS LOGICAL DISK DRIVE
RSTRT ADR 145702
DR>STA/FLAG:PNT<CR> *start, print test NR*

CHANGE HW (L) ? Y
#UNITS (D) ? 1<CR> *disk drives*

UNIT 0
CSR ADDRESS OF CONTROLLER (O) 172150 ?<CR>
DRIVE # (D) 0 ?<CR>
EXERCISE ON CUSTOMER DATA AREA (L) N ?<CR>

CHANGE SW (L) ? Y

ENTER MANUAL INTERVENTION MODE FOR SPECIAL DIAGNOSIS (L) N ?
ERROR LIMIT (D) 32 ?
READ TRANSFER LIMIT IN MEGABYTES - 0 FOR NO LINIT (D) 0 ?
SUPRESS PRINTING SOFT ERRORS (L) Y ?
DO INITIAL WRITE ON START (L) Y ?
ENABLE ERROR LOG (L) N ?

THE FOLLOWING QUESTION REFER TO UNIT 0 CONTR. AT 172150 DRIVE 0

NUMBER OF BAD BLOCKS (D) 0 ? 2
BAD BLOCK (A) 0 ? xxxx
BAD BLOCK (A) 0 ? 2345

The program will allow writes and reads to these blocks but no errors will be printed for this blocks.

CHANGE TESTING PARAMETERS FOR THIS DRIVE (L) N ?

UDA50/KDA50/RAxx MSCP SUBSYSTEM EXERCISER

ABSTRACT :

This diagnostic is using the MSCP interface to the UDA50A or the KDA50-Q disk controllers to perform extensive input/output operations on all selected SDI (standard disk interface) compatible disk drives and selected controllers. This test supports up to 2 controllers with each up to four drives. There are three tests within this diagnostic :

Test 1 : controller verification test, initialize test, self test, controller memory and data path test, set characteristics test.

Test 2 : subsysten verification test, initialize controllers and drives, set drives online and available, reads, seek, writes and data compare tests.

Test 3 : subsystem exerciser.

OPERATING PROCEDURES :

```
.R ZUDJC0

        This program is running under the supervisory program.
        This supervisory program will first talk to you.
CZUDJ-C-0
CZUDJC0 UDA50A,KDA50-Q DISK SUBSYSTEM EXERCISER
UNIT IS DSA DISK DRIVE
RSTRT ADR 145702
DR>STA/FLAG:PNT<CR>     start, print test NR

CHANGE HW (L) ? Y
#UNITS (D) ? 1<CR>      disk drives

UNIT 0
CSR ADDRESS OF CONTROLLER (O) 172150 ?<CR>
DRIVE # (D) 0 ?<CR>
WRITE ON CUSTOMER DATA AREA (L) N ?<CR>

CHANGE SW (L) ? Y

THE FOLLOWING QUESTIONS APPLY ONLY TO TEST 3:

ENTER MANUAL INTERVENTION MODE (L) N ?
HARD ERROR LIMIT (D) 1 ?
EXERCISER TIME LIMIT IN MINUTES (D) 60 ?
MINUTES BETWEEN STATISTICAL REPORTS (D) 15 ?
PRINT SOFT ERROR MESSAGES (L) N ?
DO DATA PATTERN VERIFICATION ON READS (L) Y ?
DO DATA PATTERN VERIFICATION ON WRITES (L) N ?
USE VARIABLE LENGTH TRANSFERS (L) Y ?
MAXIMUM TRANSFER SIZE IN BLOCKS (D) 8 ?
.....
```

UDA50/KDA50/RAxx ZUDKC0

RA80, RA81, RA82, RA60 FORMATTER

ABSTRACT :

This program formats any disk drive connected to a UDA50A, KDA50-Q disk controller. No changes to this program will be needed to format new disk drives as they become available. Reformat - format the disk with the bad sector information that was written onto the disk at the factory. This is the normal way to format a disk. Do not reformat any disk if you do not have a good reason (just undefined errors on a disk is not a good reason).

OPERATING PROCEDURES :

.R ZUDKC0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZUDK-C-0
CZUDKC0 UDA50A,KDA50-Q FORMATTER
UNIT IS RA SERIES DISK DRIVE
RSTRT ADR 145702
DR>START

CHANGE HW (L) ? Y
#UNITS (D) ? 1<CR> disk drives

UNIT 0
CSR ADDRESS (O) 172150 ?<CR>
DRIVE # (D) 0 ?<CR>

At the end the formatter should print "FCT sucessfully used".
If not inform support.

RA80/81/82, RA60 BAD BLOCK REPL. UTILITY

ABSTRACT :

This program is normaly not on the distribution disk or tape, it is on a separat tape (contact your support group in case you want it). You need to know exactly what you want to do with this program, otherwise do not use this program. This is not a diagnostic test any way. If you want to study this program, print out the help text file (about 30 pages) study this carefully and if every thing is clear then you are a candidate to use this program. In short, what you can do with this program is: read a pack (HDA) with data on (read/only, check every block to be readable), replace a bad block if one exists (BBR), print all replaced LBN's.

OPERATING PROCEDURES :

.R ZUDLA0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZUDL-A-0
Bad Block Replacement Utility
UNIT IS Local disk drive
RSTRT ADR 145702
DR>START

CHANGE HW (L) ? Y
#UNITS (D) ? 1<CR> *number ofdisk drives*

UNIT 0
CSR ADDRESS (O) 172150 ?<CR>
VECTOR (O) 154 ?<CR>
BR LEVEL (D) 5 ?<CR>
UNIBUS BURST RATE (D) 63 ?<CR>
DRIVE # (D) 0 ?<CR>

BAD BLOCK REPLACEMENT UTILITY.

WARNING: All drives configured for test
MUST have customer data backed-up.
Have you backed-up customer data (L) N ? Y <CR>

It is recommended that you read the operator help
information before proceeding.
Display operator Help (L) N ?

to read-only the HDA, give the following answers:
Automatic or Manual replacement (A/M) A ? <CR>
Automatic crash recovery (L) Y ? <CR>
Display replacements as they occure (L) Y ? <CR>
Display RCT replacement descriptors (L) N ? Y <CR>
Enable replacements (L) Y ? N <CR>
Enable write with Forced Error Flag (L) Y ? N <CR>

TAPE's TAPE's TAPE's TAPE's

TSV05
TA11
TM03
TE16
TU77
TK50
TK25
TS03
TE10
TU10
TM11
TMA11
TMB11
TSU05
TS11
TS04
TU81
TM02
TU16
TU45
TU58
TU80

TSV05 (Q-BUS) DIAGNOSTIC PART 1

ABSTRACT :

The TSV05 diagnostics are intended to provide confidence in the basic functionality of this subsystem. As such, this should be the first host level diagnostic run on the TSV05 to verify installation or for troubleshooting. this progran consists of 11 subtests which are executed in sequence.

1 initialize #1
2 wrap data high byte test
3 wrap data low byte test
4 RAM test
5 second initialization test
6 command reject test
7 write characteristics test
8 volume check
9 completion interrupt
10 basic packet protocol test
11 non-tape motion command tests

After test 1 run test 2,3 and 4.

OPERATING PROCEDURES :

This program is running under the supervisory program.
This supervisory program will first talk to you.

R VTSA??

CVTSA-C-0
***** TSV05 LOGIC DIAGNOSTIC - REPLACE M7196 IF ERROR *****
UNIT IS TSV05
RESTART ADR 145702
DR>START/FLA:PNT<CR> *(print each test number)*

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
DEVICE ADDRESS (TSBA/TSDB) (D) 172520 ? <CR>
INTERRUPT VECTOR (0) 224 ? <CR>

CHANGE SW (L)

INHIBIT ITERATIONS (L) N ?

TSV05 (Q-BUS) DIAGNOSTIC PART 2

ABSTRACT :

The TSV05 diagnostics are intended to provide confidence in the basic functionality of this subsystem. As such, this should be the second host level diagnostic run on the TSV05 to verify installation or for troubleshooting. This progran consists of 12 subtests, 1-9 are executed in sequence, 10-12 are standalone and have to be selected specialy (START/TEST:11)

1 initialize after write characteristics
2 basic write subsystem memory command
3 DMA memory addressing
4 RAM exerciser test
5 FIFO exerciser
6 static transport bus interface test
7 transport bus interface loopback test
8 read/write data parity check test
9 miscellaneous logic checks test
10 manual intervention
11 configuration type out
12 scope loops

After test 2 run test 3 and 4.

OPERATING PROCEDURES :

This program is running under the supervisory program.
This supervisory program will first talk to you.

R VTSB??

CVTSB-E-0
***** TSV05 LOGIC DIAGNOSTIC - REPLACE M7196 IF ERROR *****
UNIT IS TSV05
RESTART ADR 145702
DR>START/FLA:PNT<CR> *(print each test number)*

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
DEVICE ADDRESS (TSBA/TSDB) (D) 172520 ? <CR>
INTERRUPT VECTOR (0) 224 ? <CR>

CHANGE SW (L)

INHIBIT ITERATIONS (L) N ?

TSV05 (Q-BUS) DIAGNOSTIC PART 3

ABSTRACT :

The TSV05 diagnostics are intended to provide confidence in the basic functionality of this subsystem. As such, this should be the third host level diagnostic run on the TSV05 to verify installation or for troubleshooting. This progran consists of 8 subtests which are executed in sequence.

1 initialize #4 test
2 off-line and reject rewind
3 basic write data
4 basic read data (forward and reverse)
5 space records
6 rereads
7 write data retry
8 write read tape mark

After test 3 run test 4.

OPERATING PROCEDURES :

This program is running under the supervisory program.
This supervisory program will first talk to you.

R VTSC??

CVTSC-D-0
***** TSV05 LOGIC DIAGNOSTIC - CHK CABLES - TRANSPORT IF ERROR *****
UNIT IS TSV05
RESTART ADR 145702
DR>START/FLA:PNT<CR> *(print each test number)*

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
DEVICE ADDRESS (TSBA/TSDB) (D) 172520 ? <CR>
INTERRUPT VECTOR (0) 224 ? <CR>

CHANGE SW (L)

INHIBIT ITERATIONS (L) N ?

TSV05 (Q-BUS) DIAGNOSTIC PART 4

ABSTRACT :

The TSV05 diagnostics are intended to provide confidence in the basic functionality of this subsystem. As such, this should be the fourth host level diagnostic run on the TSV05 to verify installation or for troubleshooting. This program consists of 8 subtests which are executed in sequence.

1 skip tape marks test
2 no-op and initialize test
3 erase and operation incomplete test
4 data parity test
5 test operations at EOT
6 extended mode features
7 record buffering
8 function timing

This is the last of 4 tests to run

OPERATING PROCEDURES :

This program is running under the supervisory program.
This supervisory program will first talk to you.

R VTSD??

CVTSD-E-0
***** TSV05 LOGIC DIAGNOSTIC - CHECK TRANSPORT IF ERROR *****
UNIT IS TSV05
RESTART ADR 145702
DR>START/FLA:PNT<CR> *(print each test number)*

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
DEVICE ADDRESS (TSBA/TSDB) (D) 172520 ? <CR>
INTERRUPT VECTOR (0) 224 ? <CR>

CHANGE SW (L)

INHIBIT ITERATIONS (L) N ?

TSV05 DATA RELIABILITY TEST

ABSTRACT :

This program can be used as a basic function test, data reliability test or compatibility test. This diagnostic can test one controller and up to 2 drives. This program mainly verifies that the tape drives under test are performing to there data error rate specified. It consists of 5 parts :

Test 1 basic functions
Test 2 data reliability
Test 3 write compatibility write utility
Test 4 read compatibility read utility
Test 5 operator selected sequence utility

OPERATING PROCEDURES :

.R VTSE??

This program is running under the supervisory program.
This supervisory program will first talk to you.

CVTSE-D-0
DATA RELIABILITY TEST
UNIT IS TSV05
RSTRT ADR 145702
DR>START *answer the hardware questions*

CHANGE HW (L) ? Y<CR>
UNITS (D) ? 1<CR>
TSDB ADDRESS (0) 172520 ?<CR>
VECTOR (0) 224 ?<CR>

CHANGE SW (L) ? N<CR>

here you can change some software parameters like:
CLEAR COUNTERS (L) Y ?
RESET RANDOM VARIABLES (L) N ?
HALT AFTER EACH CMD (L) N ?
INHIBIT RECOVERY (L) Y ?
DISABLE INTERRUPTS (L) N ?
INHIBIT RFC ERROR REPORT (L) ?
CHANGE COMMAND SEQUENCE (L) ?

Tape Unit must be online a tape loaded at BOT
and a write enable ring in.

TA11 CASSETTE BASIC LOGIC TEST #1

ABSTRACT :

This program is part-1 of 2 and contains a series of basic logic tests that check the TA11 for proper operation.

OPERATING PROCEDURES :

START ADDRESSES:
SA = 200 normal starting
SA = 204 select drive(s) before starting test
SA = 210 select drive(s) and addresses before starting test
SA = 214 setup for manual looping
SA = 220 write file gap from BOT to EOT
SA = 224 write continous blocks of data
SA = 230 read continues blocks of data
SA = 234 write file gap and a block of data
SA = 240 read block of data and a file gap
SA = 244 space fwd file gap from BOT to EOT
SA = 250 back space file gap
SA = 500 load switch register into the TACS (control/status)
SA = 600 write switch register on tape from BOT to EOT
SA = 700 read from BOT to EOT

load a write enabled cassette in both drives
rewind both drives
start test
the program will ring every pass

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on test
SW13 = 1 inhibit error typeouts
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 ring bell on error
SW09 = 1 loop on error
SW08 = 1 loop on test as per SW<07-00>

use "CONTROL G" to enter software SWR at loc. 176

TC11 BASIC LOGIC TEST #1

ABSTRACT :

This program is part-1 of 3 and contains a series of basic logic tests that checks that each of the controller registers can be referenced without causing bus error traps and all bits can be set and cleared. A special routine (test 0) is available in the program as a maintenance aid in adjusting the TC11 control delays.

OPERATING PROCEDURES :

.R ZTCAA0

SA = 1000 restart address

The program identifies itself, types setup instructions, SR options message, and halts.
Perform setup (all transports must be off, set WRTM switch and WALL switch to off position) and set SW if any.
Press continue.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 enter scope mode
SW13 = 1 inhibit error typeouts
SW12 = 1
SW11 = 1 inhibit iterations
SW10 = 1 halt at end of test currently executing
SW09 = 1 loop on test as per SW<07-00>

To get to the adjustment maintenance routine, load address 1000, set SW9 = 1 and SW07 to SW00 = 0 and press start.

TM03 FUNCTIONAL TEST PART 1

ABSTRACT :

This program is designed to sequentially test all control logic functionality of the TM03. Each test will attempt to isolate failures to the module level and provide printout information which will identify the failing module. It will use the maintenance mode of the TM03. There are 51 (octal) tests.

OPERATING PROCEDURES :

.R ZTEAE0

SA = 200 normal startaddress
SA = 210 restart address (no header printed)

Tape Unit must be online and a tape loaded at BOT

Answer the following questions:

REGISTER START: 172440
VECTOR ADDRESS: 224
IS CONTROLLER JUMPERED IN NON-STANDARD MODE, ?
TYPE 2 FOR NON = STANDARD OR CR FOR STANDARD ?
TM03 DRIVE: 0 *controller select number*
TE16/TU77 SLAVE: 0 *tape drive select number*
STATIC TESTS ONLY: 0 *(0 = no, 1 = yes)*
SLAVE TYPE (0 = TE16, 1 = TU77): 0
SWR = 000000 NEW =

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on errors
SW13 = 1 inhibit error typeout
SW12 = 1 halt at end of pass
SW11 = 1 inhibit iterations
SW10 = 1 halt after current test
SW09 = 1 do manual intervention tests
SW08 = 1
SW07 = 1
SW06 = 1
SW05 = 1 selects individual test
SW04 = 1 selects individual test
SW03 = 1 selects individual test
SW02 = 1 selects individual test
SW01 = 1 selects individual test
SW00 = 1 selects individual test

use "CONTROL G" to enter software SWR at loc. 176

TM03 FUNCTIONAL TEST PART 2

ABSTRACT :

This program is designed to sequentially test the data formatting functionality of the TM03. Each test will attempt to isolate failures to the module level and provide printout information which will identify the failing module. It will use the maintenance mode of the TM03. There are 20 (octal) tests.

OPERATING PROCEDURES :

.R ZTEBC0

SA = 210 restart address (no header printed)

Tape Unit must be online and a tape loaded at BOT

Answer the following questions:

REGISTER START: 172440
VECTOR ADDRESS: 224
TM03 DRIVE: 0 *controller select number*
TE16/TU77 SLAVE: 0 *tape drive select number*
SLAVE TYPE (0 = TE16, 1 = TU77): 0
SWR = 000000 NEW =

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on errors
SW13 = 1 inhibit error typeout
SW12 = 1 halt at end of pass
SW11 = 1 inhibit iterations
SW10 = 1 halt after current test
SW09 = 1
SW08 = 1 inhibit wrap data check
SW07 = 1 inhibit wrap status check
SW06 = 1 selectable wrap data pattern (in single test)
SW05 = 1 selects individual test
SW04 = 1 selects individual test
SW03 = 1 selects individual test
SW02 = 1 selects individual test
SW01 = 1 selects individual test
SW00 = 1 selects individual test

use "CONTROL G" to enter software SWR at loc. 176

TM03/TE16/TU77 BASIC FUNCTION TEST

ABSTRACT :

This program is intended to test all of the basic operations of the TM03/TE16/TU77 Subsystem, write, read, space, erase, rewind, ect. There are 27 (octal) tests.

OPERATING PROCEDURES :

.R ZTECF0

SA = 210 restart address (no header printed)

Tape Unit must be online and a tape loaded at BOT with a write enable ring installed.

Answer the following questions:

REGISTER START: 172440
VECTOR ADDRESS: 224
IS CONTROLLER JUMPERED IN NON-STANDARD MODE
TYPE 2 FOR NON-STANDARD OR <CR> FOR STANDARD:
DRIVE NUMBER: 0 *controller select number*
SLAVE NUMBER: 0 *tape drive select numbe*
SERIAL NO: 12345
RH ONLY (NO = 0, YES = 1): (0) ?

SWR = 000000 NEW =

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on error
SW13 = 1 inhibit error typeout
SW12 = 1 do not halt at end of pass
SW11 = 1 inhibit iterations
SW10 = 1 halt after current test
SW09 = 1
SW05 = 1
SW04 = 1 selects individual test
SW03 = 1 selects individual test
SW02 = 1 selects individual test
SW01 = 1 selects individual test
SW00 = 1 selects individual test

use "CONTROL G" to enter software SWR at loc. 176

TM03/TE16/TU77 DATA RELIABILITY PROGRAM

ABSTRACT :

With this program you can verify that the tape drives under test are performing to there data error rate specified. Up to 8 drives can be tested by a single execution of the program. The program tests writs, reads, rewinds, tape positioning, EOT-BOT sensing.

OPERATING PROCEDURES :

START ADDRESS
SA = 200 normal startaddress
SA = 204 restart address (keep parameters)
SA = 240 all default except RH address and vector.
Tape Unit : ONLINE, TAPE LOADED at BOT, WRITE ENABLED
Answer the following questions:

REGISTER START: 172440	
VECTOR ADDRESS: 224	
DRIVE NUMBER: 0	*controller select number*
SLAVE NUMBER: 0	*tape drive select number*
DENSITY (3 or 4):	*3 = 800, 4 = 1600 BPI*
PARITY (0 or 1):	*0 = ODD, 1 = EVEN*
FORMAT (14,15 or 16):	*14 = normal, 15 = core dump*
	16 = PDP15 or IBM compatible
SLAVE NUMBER: 1	*<CR> if no more drives*
RECORD COUNT: 100	*1-177777 gives blocking factor*
CHARACTER COUNT: 200	*20-10000 characters per record*
PATTERN NUMBER : 1	*0-15 different data patterns*
TAPE MARK: 0	*1 = one tape mark after each data block*
INTERCHANGE READ: 0	*0 = normal 1 = interchange*
SINGLE PASS:0	*1 = stop after one pass*
STALLS:	*1-177777 (time delay between functions)*

SWITCH SETTINGS :

RECOMMENDED SWITCH SETTING : 000720

SW15 = 1 halt on error
SW14 = 1 print read/write statistics
SW13 = 1 do not check data errors
SW12 = 1 do not check write status errors
SW11 = 1 do not check read status errors
SW10 = 1 do not print any error
SW09 = 1 rewind all available tapes
SW08 = 1 generate random data
SW07 = 1 generate random character count
SW06 = 1 generate random record count
SW05 = 1 yozzle on current record
SW04 = 1 do write/read retries
SW03 = 1 do not read forward
SW02 = 1 do not read reverse
SW01 = 1 read forward first
SW00 = 1 do not write
use "CONTROL G" to enter software SWR at loc. 176

TM03/TE16/TU77 DRIVE FUNCTION TIMER

ABSTRACT :

This program will check both the logic generated time delays as well as the distances traveled by the tape. Actual tape speed may also be checked by using the speed tests with an 800 BPI SKEW tape.

OPERATING PROCEDURES :

.R ZTEEE0

SA = 210 restart address (use parameters from the previous run)

Tape Unit must be online and a tape loaded at BOT with a write enable ring in.

Answer the questions:
FIRST ADDRESS OF CONTROLLER: 172440
TM03 DRIVE #'s TO BE TESTED: ALL (or 0-7)
FOR TM03 DRIVE X TYPE SLAVE #'s TO BE TESTED: ALL (or 0-7)
SPEED TESTS (YES/NO) : NO

The program will start testing timing functions.
On completetion the program will halt the CPU.
To repeat test press continue.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current test
SW13 = 1 inhibit error typeout
SW12 = 1
SW11 = 1 inhibit subtest iterations
SW10 = 1 dont print function times
SW09 = 1 bell on error
SW08 = 1
SW06 = 1 do not halt after one pass
SW05 = 1 selects individual test
SW04 = 1 selects individual test
SW03 = 1 selects individual test
SW02 = 1 selects individual test
SW01 = 1 selects individual test
SW00 = 1 selects individual test

use "CONTROL G" to enter software SWR at loc. 176

TK50/TK70 FRONT END FUNCTIONAL TEST

ABSTRACT :

The TK50/70 functional diagnostic is intended to provide confidence in the basic functionality of this subsystem. As such, this should be the first host level diagnostic run on the TK50/70 subsystem to verify installation or for troubleshooting. Emphasis is placed on isolating faults to the field replaceable unit (FRU). Up to four TK50/70 units can be tested sequentialy. One pass will take about 20 minutes. This is not a data reliability test. There are 9 subtests performed by the diagnostic code ; subtest 10 invokes the controller resident level 2 microdiagnostics.

OPERATING PROCEDURES :

.R ZTKA??

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTKA-E-0
CZTKAE0 TK50/70 FUNCTIONAL
UNIT IS TK50
RSTRT ADR 145702
DR>STA<CR>

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
TKIP ADDRESS (0) 174500 ? <CR>
TK VECTOR (0) 260 ? <CR>
T/MSCP UNIT NUMBER (O) 0 <CR>

TESTING UNIT 0

On the end you will get a nice summary table

BLOCKS WRITTEN CHANNEL 1 : 2290
BLOCKS WRITTEN CHANNEL 2 : 2290
BLOCKS READ CHANNEL 1 : 2190
.....

(there are physicaly 2 read/write heads/channels)

TK50/TK70 DATA RELIABILITY TEST

ABSTRACT :

This program will exercise the TK50/70 and establish the performance quality of each unit through accumulation of statistics. Predetermined sequences of operations will permit read and write compatibility (media interchange testing) and data reliability testing. This test accepts up to 4 units. This test is not a fault isolation tool.

OPERATING PROCEDURES :

.R ZTKB??

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTKB-C-0
CZTKBC0 DATA RELIABILITY
UNIT IS TK50
RSTRT ADR 145702
DR>STA<CR>

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
TKIP ADDRESS (0) 174500 ? <CR>
T/MSCP UNIT NUMBER (O) 0 <CR>

CHANGE SW (L) ? N<CR>
here you can select time of day clock,
change controller parameters,
change printing parameters,
change test parameters.

One end of pass will require approximately 1 hour and 10 minutes for each unit to test.

Any unrecoverable write, read or hardware error means that this unit did not pass the test.

TK25 FRONT END FUNCTIONAL TEST 1

ABSTRACT :

The TK25 functional diagnostics are intended to provide confidence in the basic functionality of the TK25 subsystem. As such, this should be the first host level diagnostic run on the TK25 to verify installation or for troubleshooting. One pass will take about 1 minutes. This is not a data reliability test.
There are 11 subtests :

1 Initialization test, build in microdiagnostics (FRU is TK25 controller)
2 Controller RAM test (FRU is TK25 controller)
3 Command reject test (FRU is TK25 controller)
4 Write characteristics command (FRU is TK25 controller)
5 Volume check (FRU is TK25 controller)
6 Completion interrupt (FRU is TK25 controller)
7 Basic packet protocol test (FRU is TK25 controller)
8 Non tape motion commands test (FRU is TK25 controller)
9 Memory addressing test (FRU is TK25 controller)
10 Initialize after write characteristics (FRU is TK25 controller)
11 Basic write subsystem memory command test (FRU is TK25 controller)

After test 1 run test 2,3 and 4.

OPERATING PROCEDURES :

.R ZTKEB0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTKE-B-0
CZTKEA0 TK-25 FRT END FUNC #1
UNIT IS TK-25
RSTRT ADR 145702
DH>STA<CR>

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
DEVICE ADDRESS (TSSR) (0) 172522 ? <CR>
INTERRUPT VECTOR (0) 224 ? <CR>

CHANGE SW (L)

ENABLE CONTROLLER RAM DUMP ON ERROR (L) N ?

INHIBIT ITERATIONS (L) N ?

TK25 FRONT END FUNCTIONAL TEST 2

ABSTRACT :

The TK25 functional diagnostics are intended to provide confidence in the basic functionality of the TK25 subsystem. This should be the second host level diagnostics to run on the TK25 to verify installation or for troubleshooting. One pass will take about 1 minutes.
There are 7 subtests :

1 Initialization test #2
2 Off line reject and rewind test.
3 Basic write test.
4 Basic read data test (forward and reverse).
5 Manual intervention test
6 Configuration type out
7 Scope loop

After test 2 run test 3 and 4.

OPERATING PROCEDURES :

.R ZTKFA0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTKF-A-0
CZTKFA0 TK-25 FRT END FUNC #2
UNIT IS TK-25
RSTRT ADR 145702
DR>STA<CR> *if you want manual intervention test*
type START/FLAG:PNT/TEST:5/PASS:1<CR>
if you want configuration type out
type START/FLAG:PNT/TEST:6/PASS:1<CR>
if you want scope loop
type START/FLAG:PNT/TEST:7PASS:1<CR>

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
DEVICE ADDRESS (TSSR) (0) 172522 ? <CR>
INTERRUPT VECTOR (0) 224 ? <CR>
INTERRUPT PRIORITY (0) 5 ?<CR>

CHANGE SW (L)
if you type "Y" it will ask

ENABLE CONTROLLER RAM DUMP ON ERROR (L) N ?

INHIBIT ITERATIONS (L) N ?

TK25 FRONT END FUNCTIONAL TEST 3

ABSTRACT :

The TK25 functional diagnostics are intended to provide confidence in the basic functionality of the TK25 subsystem. This should be the third host level diagnostics to run on the TK25 to verify installation or for troubleshooting. One pass will take about 6 minutes.
There are 4 subtests :

1 Space records test
2 Rereads test
3 Write data retry test
4 write/read tape mark

After test 3 run test 4.

OPERATING PROCEDURES :

.R ZTKGA0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTKG-A-0
CZTKGA0 TK-25 FRT END FUNC #3
UNIT IS TK-25
RSTRT ADR 145702
DR>STA<CR>

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
DEVICE ADDRESS (TSSR) (0) 172522 ? <CR>
INTERRUPT VECTOR (0) 224 ? <CR>
INTERRUPT PRIORITY (0) 5 ?<CR>

CHANGE SW (L)
if you type "Y" it will ask

ENABLE CONTROLLER RAM DUMP ON ERROR (L) N ?

INHIBIT ITERATIONS (L) N ?

TK25 FRONT END FUNCTIONAL TEST 4

ABSTRACT :

The TK25 functional diagnostics are intended to provide confidence in the basic functionality of the TK25 subsystem. This should be the fourth host level diagnostics to run on the TK25 to verify installation or for troubleshooting. One pass will take about 30 minutes.
There are 5 subtests :

1 Write tape mark retry test
2 Skip tape marks
3 No-op and initialize test
4 Erase and operation incomplete test
5 Operations at EOT

This is the last functional test.

OPERATING PROCEDURES :

.R ZTKHB0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTKH-B-0
CZTKHB0 TK-25 FRT END FUNC #4
UNIT IS TK-25
RSTRT ADR 145702
DR>STA/FLAG:PNT<CR> *(print test numbers)*

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
DEVICE ADDRESS (TSSR) (0) 172522 ? <CR>
INTERRUPT VECTOR (0) 224 ? <CR>
INTERRUPT PRIORITY (0) 5 ?<CR>

CHANGE SW (L)
if you type "Y" it will ask

ENABLE CONTROLLER RAM DUMP ON ERROR (L) N ?
INHIBIT ITERATIONS (L) N ?
INHIBIT EOT CHECKING (REDUCES RUN TIME BY 22 MINUTES) (L) N ?

TK25 DATA RELABILITY TEST

ABSTRACT :

This program can be used as a basic function test, a data reliability test, a compatability test, or to execute a sequence of operater selected commands. This diagnostic can test up to 4 units in a round robin fashion. There are 6 tests in this program :

1 Basic functions
2 Data reliability
3 Write and read streaming test
4 Write compatibility utility
5 Read compatibility utility
6 Operator selected sequenced utility

OPERATING PROCEDURES :

.R ZTKIB0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTKI-B-0
CZTKIB0 TK-25 DATA RELIABILITY TEST
UNIT IS TK-25
RSTRT ADR 145702
DR>STA

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
TSSR ADDRESS (0) 172522 ? <CR>
VECTOR (0) 224 ? <CR>

CHANGE SW (L)
if you type "Y" it will ask

CLEAR COUNTERS (L) Y ?
RESET RANDOM VARIABLES (L) N ?
HALT AFTER EACH COMMAND (L) ?
PRINT SOFT ERRORS (L) N ?
INHIBIT RECOVERY (L) N ?
BAD TAPE SPOT DETECT (L) Y ?
DISABLE INTERRUPTS (L) N ?
INHIBIT REC ERROR REPORTS (L) N ?
CONTROLLER RAM DUMP (L) N ?
ENABLE EARLY WARNING MESSAGES (L) N ?
CHANGE COMMAND SEQUENCE (L) N ?

One full pass takes about (11/23+) 2,5 hours

TS03/TE10/TU10 BASIC FUNCTION TEST

ABSTRACT :

This program is intended to test all of the basic operations of the TS03/TE10/TU10 Subsystem, write, read, space, erase, rewind, and if selected manual intervention.

OPERATING PROCEDURES :

.R ZTMAI0

Tape Unit must be online and a tape loaded at BOT and write enabled.

The program will type : SET SW0 = 1 IF 7 CHANNEL

If appropriate set SW0 and then press continue

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on error
SW13= 1 inhibit error typeout
SW12= 1 inhibit subtest iteration
SW11= 1 single pass
SW10= 1 inhibit manual intervention test
SW09= 1 TS03 tape drive
SW01= 1
SW00= 1 test 7 channel tape drive

use "CONTROL G" to enter software SWR at loc. 176

TM11/TS03/TE10/TU10 DATA RELIABILITY PROGRAM

ABSTRACT :

With this program you can verify that the tape drives under test are performing to there data error rate specified. Up to 8 drives (9 channel only) can be tested by a single execution of the program. The program tests writs, reads, rewinds, tape positioning, EOT-BOT sensing. There are 6 subtests available for selection if started at 204 or 210. There are also 8 data patterns to select.

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal startaddress all parameters are default.
SA = 204 operator controlled parameter and unit selection
SA = 210 same as above but instead 4k - 8k memory available

Tape Units to test must be online and a tape loaded at BOT and a write enable ring in.

If you start at 204 or 210 the program will type

"SELECT UNITS" (like 0,1,2,3<CR>)

SWITCH SETTINGS :

SW15 = 1
SW14 = 1
SW13 = 1 print errors only at end of tape
SW12 = 1
SW09 = 1
SW08 = 1 print error statistics
SW07 = 1
SW06 = 1 write statistical recovery
SW05 = 1 delete write xirg
SW04 = 1 delete read re-trys
SW03 = 1 print after parity errors
SW02 = 1
SW01 = 1
SW00 = 1 change data pattern (to next one)

use "CONTROL G" to enter software SWR at loc. 176

TM11/TU10 (7 CHANNEL) DATA RELIABILITY PROGRAM

ABSTRACT :

With this program you can verify that the tape drives under test are performing to there data error rate specified. Up to 8 drives (7 channel only) can be tested by a single execution of the program. The program tests writs, reads, rewinds, tape positioning, EOT-BOT sensing. There are 6 subtests available for selection if started at 204 or 210. There are also 8 data patterns to select.

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal startaddress all parameters are default.
SA = 204 operator controlled parameter and unit selection
SA = 210 same as above but instead 4k - 8k memory available

Tape Units to test must be online a tape loaded at BOT and a write enable ring in.

If you start at 204 or 210 the program will type

"SELECT UNITS" (like 0,1,2,3<CR>)

SWITCH SETTINGS :

SW15 = 1
SW14 = 1
SW13 = 1 print errors only at end of tape
SW12 = 1
SW09 = 1
SW08 = 1 print error statistics
SW07 = 1
SW06 = 1 write statistical recovery
SW05 = 1 delete write xirg
SW04 = 1 delete read re-trys
SW03 = 1 print after parity errors
SW02 = 1
SW01 = 1
SW00 = 1 change data pattern (to next one)

use "CONTROL G" to enter software SWR at loc. 176

TM11/TU10 (7 or 9 CHANNEL) DRIVE FUNCTION TIMER

ABSTRACT :

The TM11 drive function timer assists in testing of the TM11 controller and TU10 tape unit, selected operations are executed, timed and the times are printed (in miliseconds) there is no limit or error testing facilities in the program, the decision on the validity of times measured must be made by the operator.

OPERATING PROCEDURES :

.R ZTMDE0

Tape Units to test must be online a tape loaded at BOT and a write enable ring in.

Before starting set control switches in memory location 176 to select a Tape-Unit (if no front pannel switches).
On completion of all tests "END OF TIMING" will be printed and the processor will halt. To repeat test, simply press continue.

CONTROL SWITCH SETTINGS :

SW15 = 1 unit 0, 7 channel
SW14 = 1 unit 1, 7 channel
SW13 = 1 unit 2, 7 channel
SW12 = 1 unit 3, 7 channel
SW11 = 1 unit 4, 7 channel
SW10 = 1 unit 5, 7 channel
SW09 = 1 unit 6, 7 channel
SW08 = 1 unit 7, 7 channel
SW07 = 1 unit 0, 9 channel
SW06 = 1 unit 1, 9 channel
SW05 = 1 unit 2, 9 channel
SW04 = 1 unit 3, 9 channel
SW03 = 1 unit 4, 9 channel
SW02 = 1 unit 5, 9 channel
SW01 = 1 unit 6, 9 channel
SW00 = 1 unit 7, 9 channel

use "CONTROL G" to enter software SWR at loc. 176

TMA11/TMB11/TU10/TE10 (7/9 CHANNEL) DRIVE FUNCTION TIMER

ABSTRACT :

The TM11/TMA11/TMB11 drive function timer assists in testing of the controller and tape units, selected operations are executed, timed and the times are printed (in miliseconds) there is no limit or error testing facilities in the program, the decision on the validity of times measured must be made by the operator.

OPERATING PROCEDURES :

.R ZTMEE0

Tape Units to test must be online and a tape loaded at BOT and a write enable ring in.

Before starting set control switches in memory location 176 to select a Tape-Unit (if no front pannel switches).
On completion of all tests "END OF TIMING" will be printed and the processor will halt. To repeat test, simply press continue.

CONTROL SWITCH SETTINGS :

SW15= 1 unit 0, 7 channel
SW14= 1 unit 1, 7 channel
SW13= 1 unit 2, 7 channel
SW12= 1 unit 3, 7 channel
SW11= 1 unit 4, 7 channel
SW10= 1 unit 5, 7 channel
SW09= 1 unit 6, 7 channel
SW08= 1 unit 7, 7 channel
SW07= 1 unit 0, 9 channel
SW06= 1 unit 1, 9 channel
SW05= 1 unit 2, 9 channel
SW04= 1 unit 3, 9 channel
SW03= 1 unit 4, 9 channel
SW02= 1 unit 5, 9 channel
SW01= 1 unit 6, 9 channel
SW00= 1 unit 7, 9 channel

use "CONTROL G" to enter software SWR at loc. 176

TMA-TMB11/TE10/TU10 SUPPL. INSTRUCTION TEST

ABSTRACT :

This program is intended to be used in addition to the ZTMAI0 test to complete testing of the mag tape controller. The program consists of only four tests which check only the TMA,B-11 features of data transfer at odd byte starting address and operation incomplete time out.

OPERATING PROCEDURES :

.R ZTMFF0

SA = 210 restart address (no header printed)

Tape Unit must be online and a tape loaded at BOT and write enabled.

When started at 200 the program will print a identification header and requests the unit number to be typed on the concole.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on error
SW13 = 1 inhibit error typeout
SW12 = 1 inhibit subtest iteration
SW11 = 1 do not halt at end of pass
SW10 = 1 halt at end of current test
SW09 = 1
*SW02 = 1 select individual test **
*SW01 = 1 select individual test **
*SW00 = 1 select individual test * (0 = all tests)*

use "CONTROL G" to enter software SWR at loc. 176

TM.A.B11/TS03/TU10/TE10 DATA RELIABILITY TEST

ABSTRACT :

With this program you can verify that the tape drives under test are performing to there data error rate specified. Up to 8 drives (7 or 9 channel) can be tested by a single execution of the program. The program tests writing, reading, rewinding, tape positioning, EOT-BOT sensing.

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal startaddress enter all parameters

SA = 204 restart address (keep parameters, continue data pattern sequence)

SA = 210 same as above but reset data pattern like start at 200

SA = 240 special start, special sequence of testing

Tape Unit must be online and a tape loaded at BOT and a write enable ring in.

Answer the following questions:

REGISTER START: 172520	
VECTOR ADDRESS: 224	
UNIT NUMBER: 0	*drive select number*
DENSITY (0 - 3):	*0 = 200, 1 = 556, 2 = 800BPI 7ch, 3 = 800BPI 9ch*
PARITY (0 or 1):	*0 = ODD, 1 = EVEN*
UNIT NUMBER: <CR>	*<CR> if no more units*
RECORD COUNT: 100	*1-177777 gives blocking factor*
CHARACTER COUNT: 200	*4-4000 characters per record*
PATTERN NUMBER : 1	*0-20 different data patterns*
TAPE MARK: 0	*1 = one tape mark after each data block*
SINGLE PASS:0	*1 = stop after one pass*
STALLS:	*1-177777 (time delay between functions)*

SWITCH SETTINGS :

RECOMMENDED SWITCH SETTING : 000700

SW15 = 1 halt on error

SW14 = 1 yozzle on current block

SW13 = 1 do not check data errors

SW12 = 1 do not check write status errors

SW11 = 1 do not check read status errors

SW10 = 1 do not print any error

SW09 = 1 rewind all available tapes

SW08 = 1 generate random data

SW07 = 1 generate random character count

SW06 = 1 generate random record count

SW05 = 1 yozzle on current record

SW04 = 1 print statistics

SW03 = 1 do not read

SW02 = 1

SW01 = 1 disable retries

SW00 = 1 do not write

use "CONTROL G" to enter software SWR at loc. 176

TSU05 DIAGNOSTIC PART 1

ABSTRACT :

The TSU05 diagnostics are intended to provide confidence in the basic functionality of this subsystem. As such, this should be the first host level diagnostic run on the TSU05 to verify installation or for troubleshooting. this progran consists of 11 subtests which are executed in sequence.

1 bus reset test
2 wrap data high byte
3 wrap data low byte
4 M7455 RAM test
5 second initialization test
6 command reject test
7 write characteristics test
8 volume check test
9 completion interrupt test
10 basic packet protocol test
11 non-tape motion command tests

After test 1 run test 2,3 and 4.

OPERATING PROCEDURES :

.R ZTSAA0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTSA-A-0
***** TSU05 DIAGNOSTIC PART 1 REPLACE M7455 IF ERROR *****
UNIT IS TSU05
RESTART ADR 142060
DR>START/FLA:PNT<CR> *(print each test number)*

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
DEVICE ADDRESS (TSBA/TSDB) (D) 172520 ? <CR>
INTERRUPT VECTOR (0) 224 ? <CR>

CHANGE SW (L)

INHIBIT ITERATIONS (L) N ?

TSU05 DIAGNOSTIC PART 2

ABSTRACT :

The TSU05 diagnostics are intended to provide confidence in the basic functionality of this subsystem. As such, this should be the second host level diagnostic run on the TSU05 to verify installation or for troubleshooting. This program consists of 12 subtests, 1-9 are executed in sequence, 10-12 are standalone and have to be selected specialy (START/TEST:11)

1 initialize after write characteristics
2 basic write subsystem memory command
3 DMA memory addressing
4 M7455 RAM exerciser test
5 extended features switch and timer A and B
6 FIFO exerciser
7 static transport bus interface test
8 transport bus interface loopback test
9 read/write data parity test
10 manual intervention
11 configuration type out
12 scope loops

After test 2 run test 3 and 4.

OPERATING PROCEDURES :

```
.R ZTSBA0

                    This program is running under the supervisory program.
                    This supervisory program will first talk to you
CZTSB-A-0
**** TSU05 DIAG PART 2 REPLACE M7455 IF ERROR ****
UNIT IS TSU05
RESTART ADR 145702
DR>START/FLA:PNT<CR>          print each test number

                    You have to answer the hardware questions.

Change HW (L) ? Y<CR>
# UNITS (D) ? 1<CR>
UNIT 0
DEVICE ADDRESS (TSBA/TSDB) (D) 172520 ? <CR>
INTERRUPT VECTOR (0) 224 ? <CR>

CHANGE SW (L)

INHIBIT ITERATIONS (L) N ?
```

TSU05 DIAGNOSTIC PART 3

ABSTRACT :

The TSU05 diagnostics are intended to provide confidence in the basic functionality of this subsystem. As such, this should be the third host level diagnostic run on the TSU05 to verify installation or for troubleshooting. This program consists of 8 subtests which are executed in sequence.

1 initialize #4 test
2 off-line and reject rewind
3 basic write data
4 basic read data (forward and reverse)
5 space records
6 rereads
7 write data retry
8 write/read tape mark

After test 3 run test 4.

OPERATING PROCEDURES :

.R ZTSCA0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTSC-A-0
***** TSU05 DIAG PART 3 CHK CABLES - TRANSPORT IF ERROR *****
UNIT IS TSU05
RESTART ADR 145702
DR>START/FLA:PNT<CR> (print each test number)

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
DEVICE ADDRESS (TSBA/TSDB) (D) 172520 ? <CR>
INTERRUPT VECTOR (0) 224 ? <CR>

CHANGE SW (L)

INHIBIT ITERATIONS (L) N ?

TSU05 DIAGNOSTIC PART 4

ABSTRACT :

The TSU05 diagnostics are intended to provide confidence in the basic functionality of this subsystem. As such, this should be the fourth host level diagnostic run on the TSU05 to verify installation or for troubleshooting. This program consists of 9 subtests which are executed in sequence.

1 write tape mark retry
2 skip tape marks
3 no-op "clean tape" and initialize
4 erase and operation incomplete
5 data parity test
6 operations at EOT
7 extended mode features
8 record buffering
9 function timing

This is the last of 4 tests to run

OPERATING PROCEDURES :

.R ZTSDA0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTSD-A-0
***** TSU05 DIAG PART 4 CHECK TRANSPORT IF ERROR *****
UNIT IS TSU05
RESTART ADR 145702
DR>START/FLA:PNT<CR> *(print each test number)*

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
DEVICE ADDRESS (TSBA/TSDB) (D) 172520 ? <CR>
INTERRUPT VECTOR (0) 224 ? <CR>

CHANGE SW (L)

INHIBIT ITERATIONS (L) N ?

TMA11/TMB11 TS03 DRIVE FUNCTION TIMER

ABSTRACT :

The TMA/TMB11 drive function timer assists in testing of the tape controller and TS03 tape unit, selected operations are executed, timed and the times are printed (in miliseconds) there is no limit or error testing facilities in the program, the decision on the validity of times measured must be made by the operator. Ether 1 or 2 TS03 units may be selected.

OPERATING PROCEDURES :

.R ZTSEB0

Tape Units to test must be online and a tape loaded at BOT and a write enable ring in.

Enter starting register address
If speed test only, enter a one (1).
If all others, enter a zero (0).
If speed test, mount a 800 BPI skew tape and type <CR>
The program will automaticaly find the available TS03 tape unit.
The program will begin timing functions.
On completion of all tests it prints "END OF TIMING" and halts.
To repeat test: press continue.

SWITCH SETTINGS :

no switch settings

TMA.B11/TS03 ZTSFD0

TMA-TMB11 TS03 SUPPL. INSTRUCTION TEST

ABSTRACT :

This program is intended to be used in addition to the ZTMAI0 test to complete testing of the mag tape controller. The program consists of only four tests which check only the TMA,B-11 features of data transfer at odd byte starting address and operation incomplete time out.

OPERATING PROCEDURES :

.R ZTSFD0

SA = 210 restart address (no header printed)

Tape Unit must be online, a tape loaded at BOT and write enabled.

When started at 200 the program will print a identification header and requests the unit number to be typed on the concole.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on error
SW13 = 1 inhibit error typeout
SW12 = 1 inhibit subtest iteration
SW11 = 1 do not halt at end of pass
SW10 = 1 halt at end of current test
SW09 = 1
*SW02 = 1 select individual test **
*SW01 = 1 select individual test **
*SW00 = 1 select individual test * (0 = all tests)*

use "CONTROL G" to enter software SWR at loc. 176

TS11 TS04 DATA RELIABILITY TEST

ABSTRACT :

This program can be used as a basic function test, data reliability test, compatibility test or to execute a sequence of operator selected commands. This program mainly verifies that the tape drives under test are performing to there data error rate specified. It consists of 5 parts :

Test 1 basic functions
Test 2 data reliability
Test 3 compatibility write-utility
Test 4 compatibility read-utility
Test 5 operator selected sequence utility

OPERATING PROCEDURES :

.R ZTSHD0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTSH-D-0
DATA RELIABILITY TEST
UNIT IS TS11
RSTRT ADR 145702
DR>START

answer the hardware questions

CHANGE HW (L) ? Y<CR>
UNITS (D) ? 1<CR>
TSSR ADDRESS (0) 172522 ? <CR>
VECTOR (0) 244 ? <CR>

CHANGE SW (L) ? N<CR>

here you can change some softwate parameters like :

CLEAR COUNTERS (L) Y ?
RESET RANDOM VARIABLES (L) N ?
HALT AFTER EACH CMD (L) N ?
PRINT RECOVERABLE ERRORS (L) N ?
INHIBIT RECOVERY (L) Y ?
DISABLE INTERRUPTS (L) N ?
INHIBIT RFC ERROR REPORT (L) ?
CHANGE COMMAND SEQUENCE (L) ?

Tape Unit must be online and a tape loaded at BOT and a write enable ring in.

TS11 TS04 CONTROL LOGIC TEST

ABSTRACT :

This diagnostic tests one unit at the time, but will sequentialy test up to 4 units. The units do not have to be on line and a tape does not have to be loaded to run this diagnostic. This program executes TS11 and TS04 commands in the diagnostic wraparound mode to identify failing modules.
It consists of 10 subtest :
Test 1 PDP11-TS11 wrap test
Test 2 PDP11-TS04 wrap test
Test 3 set TS04 characteristc test
Test 4 perform data wrap on the P.E. read formatter
Test 5 wrap a data pattern to check each track
Test 6 skew the data on a track by one byte
Test 7 check the dead track logic by rippling a dead track thru
Test 8 lookup table test
Test 9 inline micro diagnostic test
Test 10 init micro diagnostic test

OPERATING PROCEDURES :

.R ZTSIC0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTSI-C-0
CONTROL LOGIC TEST
UNIT IS TS11
RSTRT ADR 145702
DH> START

answer the hardware questions

CHANGE HW (L) ? Y<CR>
UNITS (D) ? 1<CR>
TSSR ADDRESS (0) 172522 ?<CR>
VECTOR (0) 224 ?<CR>

CHANGE SW (L) ? N<CR>

here you can change some software parameters like:
ENABLE DATA COMPARE ERROR PRINTS FOR TESTS 4-7 (L) N ?

TU81 DATA RELIABILITY TEST

ABSTRACT :

This program will exercise the TU81 and establish the performance quality of each unit through the accumulation of statistics. Predetermined sequences of operations will permit read and write compatibility (media interchange testing) and data reliability testing. The data reliability program will detect functional faults, but will not provide diagnostic isolation to the field replaceable unit. One pass with default parameters will take about 1 hour and 10 minutes (twice BOT to EOT).

This program consists of 7 parts :

Test 1 basic functions
Test 2 quick verify read/write test
Test 3 complex read/write test
Test 4 write interchange test
Test 5 read unknown tape
Test 6 start/stop write/read test
Test 7 conversation test

OPERATING PROCEDURES :

.R ZTU1A0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTU1-A-0
CZTU1A0 TU81 DATA RELIAB TEST
UNIT IS TU81
RSTRT ADR 145702
DR>START

answer the hardware questions

CHANGE HW (L) ? Y<CR>
UNITS (D) ? 1<CR>
UNIT 0
TKIP ADDRESS (0) 174500 ?<CR>
T/MSCP UNIT NUMBER (O) 0 ?<CR>

CHANGE SW (L) ? N<CR>

here you can change some software parameters like:

ENABLE TIME OF DAY CLOCK (L) N ?
CHANGE CONTROLLER PARAMETERS (L) ?
INITIAL DENSITY OF EACH TEST IS GCR (L) ?
CHANGE PRINTING PARAMETERS (L) N ?
CHANGE TEST PARAMERERS (L) N ?

Tape Unit must be online and a tape loaded at BOT and a write enable ring in.

TU81 FRONT END FUNCTION TEST

ABSTRACT :

This program should be the first host level diagnostic run on the TU81 to verify installation, or for troubleshooting. This diagnostic tests one unit at the time, but will sequentialy test up to 4 units. In addition to host level testing the program will implicitly invoke the TU81's controller resident level 1 self-test microdiagnostics as well as explicitly invoking the controllers level 2 microdiagnostics. To run a full pass of the program, a scratch tape must be mounted on the unit.

OPERATING PROCEDURES :

This program is running under the supervisory program.
This supervisory program will first talk to you.

```
.R ZTU2D0

CZTU2-D-0
CZTU2D0 TU81 FUNCTIONAL DIAGNOSTIC
UNIT IS TU81
RSTRT ADR 145702
DR>START
                answer the hardware questions

CHANGE HW (L) ? Y<CR>
UNITS (D) ? 1<CR>
TUIP ADDRESS (0) 174500 ?<CR>
VECTOR (0) 260 ?<CR>
T/MSCP UNIT NUMBER (O) 0 ?<CR>
```

First pass will take about 20 minutes, others 24 minutes.

TM02/TU16/TE16 DATA RELIABILITY TEST

ABSTRACT :

The program is exercising any tape drive that can be operated through the TM02 controller (NRZI, 7 or 9 Track, PE). Up to 8 drives may be tested by a single run of the program. It exercises writes, reads, rewinds, tape positioning, EOT - BOT sensing and assumes a good RH and TM02.

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal startaddress - enter parameters
SA = 204 restart address - keep parameters
SA = 210 same as 204 except data pattern is returned to fixed one
SA = 240 special test sequence / enter only RH addr. and vector
SA = 300 restart - short parameter entry.

Put Tape Units online, at BOT and write ring in.
Answer the following questions:

REGISTER START = 172440<CR>
VECTOR = 224<CR>

DRIVE NUMBER	*controller number*
SLAVE NUMBER	*tape unit number*
DENSITY =	*3 = 800, 4 = 1600BPI*
PARITY =	*0 = even, 1 = odd*
FORMAT =	*14 = normal, 15 = core dump*
SLAVE NUMBER	*next tape unit or <CR> for no more*
RECORD COUNT = 100	*(1 - 177777) blocking factor*
CHARACTER COUNT = 200	*(20-4000) characters per record*
PATTERN NUMBER = 1	*(0-15) different data patterns*
TAPE MARKS = 0	*1 = one tape mark after each data block*
INTERCHANGE READ = 0	*0 = normal, 1 = interchange read*
SINGLE PASS = 0	*0 = stop after one pass*
STALLS = 1	*1-177777 (time delay between functions)*

SWITCH SETTINGS :

RECOMMENDED SWITCH SETTING : 000720

SW15 = 1 stop on error
SW14 = 1 print read/write statistics
SW13 = 1 do not check data errors
SW12 = 1 do not check write status errors
SW11 = 1 do not check read status errors
SW10 = 1 do not print any errors
SW09 = 1 rewind all available tapes
SW08 = 1 generate random data
SW07 = 1 generate random character count
SW06 = 1 generate random record count
SW05 = 1 yozzle on current record
SW04 = 1 do write/read retries
SW03 = 1 do not read forward
SW02 = 1 do not read reverse
SW01 = 1 read forward first
SW00 = 1 do not write

"CONTROL G" to enter software SWR at loc. 176

TM02/TU16/TE16 ZTUBH0

TM02/TU16/TE16 BASIC FUNCTION TEST

ABSTRACT :

This program is intended to test all of the basic functional level operations of the TM02-TU16/TE16 mag. tape system. All functions, write, read, space, erase, rewind, ect. will be tested. In addition to the TM02-TU16/TE16 tests, the RH will be tested separately in so far as it is possible to separate the RH from the TM02-TU16/TE16 itself.

OPERATING PROCEDURES :

.R ZTUBH0

Start address 210 = restart address - keep parameters

Put Tape Units online, tape loaded at BOT and write ring in.
Answer the following questions:

REGISTER START = 172440<CR>	
VECTOR = 224<CR>	
DRIVE NUMBER=	*controller number*
SLAVE NUMBER=	*tape unit number*
RH11 OR RH70=	*0= RH11, 1= RH70*
RH ONLY=	*1= test only RH*
NRZ ONLY=	*0= no 1= yes*

SWITCH SETTINGS :

SW15= 1 stop on error
SW14= 1 loop on error
SW13= 1 do not print errors
SW12= 1 inhibit iterations
SW11= 1 do not stop after one pass
SW10= 1 halt after current test
SW09= 1
SW08= 1
*SW04= 1 select subtest**
*SW03= 1 select subtest**
*SW02= 1 select subtest**
*SW01= 1 select subtest**
*SW00= 1 select subtest**

** all zero = all tests*
use "CONTROL G" to enter software SWR at loc 176

TM02/TU16/TE16 CONTROL LOGIC TEST

ABSTRACT :

This program tests all control logic and data formatting functions within the TM02 formatter. Each test will attempt to isolate failures to the module level and prints the failing module number. There are two major areas of testing :control logic (test 1-41/57-64) and data formatting (test 42-56).

OPERATING PROCEDURES :

.R ZTUCG0

START ADDRESS
SA = 200 normal startaddress - enter parameters
SA = 210 restart address - keep parameters

Put Tape Units online, tape loaded at BOT and write ring in.
Answer the following questions:

REGISTER START = 172440<CR>
VECTOR = 224<CR>

DRIVE NUMBER =	*controller number*
DRIVE NUMBER =	*<CR> if only one*
SLAVE NUMBER =	*tape unit number*
NRZ ONLY =	*0 = no 1 = yes*
STATIC TEST ONLY:	*0 = no, 1 = yes*

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on error
SW13 = 1 do not print errors
SW12 = 1 inhibit iterations
SW11 = 1 do not stop after one pass
SW10 = 1 halt after current test
SW09 = 1 do manual intervention test
SW08 = 1 inhibit wrap around data check
SW07 = 1 inhibit wrap around status check
SW06 = 1 selectable wrap data pattern
*SW05 = 1 select subtest**
*SW04 = 1 select subtest**
*SW03 = 1 select subtest**
*SW02 = 1 select subtest**
*SW01 = 1 select subtest**
*SW00 = 1 select subtest**

** all zero = all tests*
use "CONTROL G" to enter software SWR at loc. 176

TM02/TU16 DRIVE FUNCTION TIMER

ABSTRACT :

This program measures the time required and gap size produced by the TM02/TU16 Mag. tape. The test will check both the logic generated time delays, and the distances travled by the tape in response. Actual tape speed may also be checked by using the speed tests with an 800 BPI skew tape.

OPERATING PROCEDURES :

.R ZTUDD0

SWR= 000000 NEW=

Put Tape Units online, tape loaded at BOT and write ring in.
Answer the following questions:

TYPE FIRST ADDRESS OF CONTROLLER : 172440	*(standard)*
TYPE TM02 DRIVE #'s TO BE TESTED : 0	*(0= FIRST TM02)*
FOR TM02 DRIVE 0 TYPE SLAVE #'s TO BE TESTED:0	*(normaly slave 0)*
TAPE SPEED TESTS ONLY ? :	*(0=no, 1=yes)*
NRZ ONLY ? :	*(0=no, 1=yes)*

The program halts after one pass, press continue to do one more pass.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current subtest
SW13= 1 do not print errors
SW11= 1 inhibit iterations
SW10= 1 inhibit printing of function times
SW09= 1 bell on error
SW07= 1 halt after selected test
SW06= 1 do not halt after one pass
*SW05= 1 select subtest**
*SW04= 1 select subtest**
*SW03= 1 select subtest**
*SW02= 1 select subtest**
*SW01= 1 select subtest**
*SW00= 1 select subtest**

** all zero = all tests*
use "CONTROL G" to enter software SWR at loc. 176

TM02/TE16 DRIVE FUNCTION TIMER

ABSTRACT :

This program measures the time required and gap size produced by the TM02/TE16 Mag. tape. The test will check both the logic generated time delays, and the distances traveled by the tape in response. Actual tape speed may also be checked by using the speed tests with an 800 BPI skew tape.

OPERATING PROCEDURES :

.R ZTUGC1

SWR= 000000 NEW=

Put Tape Units online, tape loaded at BOT and write ring in.
Answer the following questions:

TYPE FIRST ADDRESS OF CONTROLLER : 172440	*(standard)*
TYPE TM02 DRIVE #'s TO BE TESTED : 0	*(0= FIRST TM02)*
FOR TM02 DRIVE 0 TYPE SLAVE #'s TO BE TESTED:	*(normaly slave 0)*
TAPE SPEED TESTS ONLY ? :	*(0=no, 1=yes)*
NRZ ONLY ? :	*(0=no, 1=yes)*

The program halts after one pass, press continue to do one more pass.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current subtest
SW13= 1 do not print errors
SW11= 1 inhibit iterations
SW10= 1 inhibit printing of function times
SW09= 1 bell on error
SW07= 1 halt after selected test
SW06= 1 do not halt after one pass
*SW05= 1 select subtest**
*SW04= 1 select subtest**
*SW03= 1 select subtest**
*SW02= 1 select subtest**
*SW01= 1 select subtest**
*SW00= 1 select subtest**

** all zero = all tests*
use "CONTROL G" to enter software SWR at loc. 176

TM02/TU45 DATA RELIABILITY TEST

ABSTRACT :

The program is exercising the TU45 drive on the TM02 controller. Up to 8 drives may be tested by a single run of the program. It exercises writes, reads, rewinds, tape positioning, EOT - BOT sensing and assumes a good RH and TM02.

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal startaddress - enter parameters

SA = 204 restart address - keep parameters

SA = 210 same as 204 except data pattern is returned to fixed one

SA = 240 special test sequence / enter only RH addr. and vector

SA = 300 restart - short parameter entry.

Put Tape Units online, at BOT and write ring in.

Answer the following questions:

REGISTER START: 172440 <CR>

VECTOR: 224 <CR>

DRIVE NUMBER:0	*controller number*
SLAVE NUMBER:0	*tape unit number*
DENSITY:4	*3 = 800, 4 = 1600BPI*
PARITY:	*0 = even, 1 = odd*
FORMAT:	*14 = normal, 15 = core dump*
SLAVE NUMBER: <CR>	*next tape unit or <CR> for no more*
RECORD COUNT: 100	*(1 - 177777) blocking factor*
CHARACTER COUNT: 200	*(20-4000) characters per record*
PATTERN NUMBER: 1	*(0-15) different data patterns*
TAPE MARKS: 0	*1 = one tape mark after each data block*
INTERCHANGE READ: 0	*0 = normal, 1 = interchange read*
SINGLE PASS: 0	*0 = stop after one pass*
STALLS: 1	*1-177777 (time delay between functions)*

SWITCH SETTINGS :

REROMMENDED SWITCH SETTING : 000720

SW15 = 1 stop on error

SW14 = 1 print read/write statistics

SW13 = 1 do not check data errors

SW12 = 1 do not check write status errors

SW11 = 1 do not check read status errors

SW10 = 1 do not print any errors

SW09 = 1 rewind all available tapes

SW08 = 1 generate random data

SW07 = 1 generate random character count

SW06 = 1 generate random record count

SW05 = 1 yozzle on current record

SW04 = 1 do write/read retries

SW03 = 1 do not read forward

SW02 = 1 do not read reverse

SW01 = 1 read forward first

SW00 = 1 do not write

"CONTROL G" to enter software SWR at loc. 176

TM02/TU45 BASIC FUNCTION TEST

ABSTRACT :

This program is intended to test all of the basic functional level operations of the TM02-TU45 Mag. Tape system. All functions, write, read, space, erase, rewind, ect. will be tested. In addition to the TM02-TU45 tests, the RH will be tested separately in so far as it is possible to separate the RH from the TM02-TU45 itself.

OPERATING PROCEDURES :

.R ZTUJA0

START ADDRESS
SA = 200 normal startaddress - enter parameters
SA = 210 restart address - keep parameters

Put Tape Units online, tape loaded at BOT and write ring in.
Answer the following questions:

REGISTER START = 172440<CR>	
VECTOR = 224<CR>	
DRIVE NUMBER=	*controller number*
SLAVE NUMBER=	*tape unit number*
RH11 OR RH70=	*0= RH11, 1= RH70*
RH ONLY=	*1= test only RH*
NRZ ONLY=	*0= no 1= yes*

SWITCH SETTINGS :

SW15= 1 stop on error
SW14= 1 loop on error
SW13= 1 do not print errors
SW12= 1 inhibit iterations
SW11= 1 do not stop after one pass
SW10= 1 halt after current test
SW09= 1
SW08= 1
*SW04= 1 select subtest**
*SW03= 1 select subtest**
*SW02= 1 select subtest**
*SW01= 1 select subtest**
*SW00= 1 select subtest**

** all zero = all tests*
use "CONTROL G" to enter software SWR at loc. 176

TM02/TU45 CONTROL LOGIC TEST

ABSTRACT :

This program tests all control logic and data formatting functions within the TM02 formatter. Each test will attempt to isolate failures to the module level and prints the failing module number. There are two major areas of testing :control logic (test 1-41/57-64) and data formatting (test 42-56).

OPERATING PROCEDURES :

START ADDRESS
SA = 200 normal startaddress - enter parameters
SA = 210 restart address - keep parameters

Put Tape Units online, tape loaded at BOT and write ring in.
Answer the following questions:

REGISTER START = 172440<CR>
VECTOR = 224<CR>
DRIVE NUMBER = controller number
DRIVE NUMBER = <CR> if only one
SLAVE NUMBER = tape unit number
NRZ ONLY = 0 = no 1 = yes
STATIC TEST ONLY: 0 = no, 1 = yes

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on error
SW13 = 1 do not print errors
SW12 = 1 inhibit iterations
SW11 = 1 do not stop after one pass
SW10 = 1 halt after current test
SW09 = 1 do manual intervention test
SW08 = 1 inhibit wrap around data check
SW07 = 1 inhibit wrap around status check
SW06 = 1 selectable wrap data pattern
*SW05 = 1 select subtest**
*SW04 = 1 select subtest**
*SW03 = 1 select subtest**
*SW02 = 1 select subtest**
*SW01 = 1 select subtest**
*SW00 = 1 select subtest**

* *all zero = all tests*
use "CONTROL G" to enter software SWR at loc. 176

TM02/TU45 DRIVE FUNCTION TIMER

ABSTRACT :

This program measures the time required and gap size produced by the TM02/TU45 Mag. tape. The test will check both the logic generated time delays, and the distances traveled by the tape in response. Actual tape speed may also be checked by using the speed tests with an 800 BPI skew tape.

OPERATING PROCEDURES :

.R ZTULA0

START ADDRESS
SA = 200 normal startaddress - enter parameters

SWR = 000000 NEW =

Put Tape Units online, tape loaded at BOT and write ring in.
Answer the following questions:

TYPE FIRST ADDRESS OF CONTROLLER : 172440	*(standard)*
TYPE TM02 DRIVE #'s TO BE TESTED : 0	*(0= FIRST TM02)*
FOR TM02 DRIVE 0 TYPE SLAVE #'s TO BE TESTED:0	*(normaly slave 0)*
TAPE SPEED TESTS ONLY ? :	*(0=no, 1=yes)*
NRZ ONLY ? :	*(0=no, 1=yes)*

The program halts after one pass, press continue to do one more pass.

SWITCH SETTINGS :

SW15 = 1 halt on error
SW14 = 1 loop on current subtest
SW13 = 1 do not print errors
SW11 = 1 inhibit iterations
SW10 = 1 inhibit printing of function times
SW09 = 1 bell on error
SW07 = 1 halt after selected test
SW06 = 1 do not halt after one pass
*SW05 = 1 select subtest**
*SW04 = 1 select subtest**
*SW03 = 1 select subtest**
*SW02 = 1 select subtest**
*SW01 = 1 select subtest**
*SW00 = 1 select subtest**

** all zero = all tests*
use "CONTROL G" to enter software SWR at loc. 176

TM03/TU45 CONTROL LOGIC TEST 1

ABSTRACT :

This program is intended to test all control logic functionality of the TM03 controller. Each test will attempt to isolate failures to the module level and provide printout information which will identify the failing module. The level of fault isolation is possible because of the TM03 structure and its maintenance mode.

OPERATING PROCEDURES :

.R ZTUOB0

START ADDRESS
SA = 200 normal startaddress - enter parameters
SA = 210 restart address - keep parameters

Put Tape Units online, tape loaded at BOT and write ring in.
Answer the following questions:

REGISTER START: 172440<CR>
VECTOR: 224<CR>
TM03 DRIVE: controller number
TU45 SLAVE: tape unit number
STATIC TEST ONLY: 0= no 1= yes

SWITCH SETTINGS :

SW15= 1 stop on error
SW14= 1 loop on error
SW13= 1 do not print errors
SW12= 1 do not stop after one pass
SW11= 1 inhibit iterations
SW10= 1 halt after current test
SW09= 1 do manual intervention tests
SW08= 1
*SW05= 1 select subtest**
*SW04= 1 select subtest**
*SW03= 1 select subtest**
*SW02= 1 select subtest**
*SW01= 1 select subtest**
*SW00= 1 select subtest**

* all zero = all tests
use "CONTROL G" to enter software SWR at loc. 176

TM03/TU45 CONTROL LOGIC TEST 2

ABSTRACT :

This program is intended to test all data formatting functionality of the TM03 controller. Each test will attempt to isolate failures to the module level and provide printout information which will identify the failing module. The level of fault isolation is possible because of the TM03 structure and its maintenance mode.

OPERATING PROCEDURES :

.R ZTUPB0

START ADDRESS
SA = 200 normal startaddress - enter parameters
SA = 210 restart address - keep parameters

Put Tape Units online, tape loaded at BOT and write ring in.
Answer the following questions:

REGISTER START: 172440<CR>
VECTOR: 224<CR>
TM03 DRIVE: *controller number*
TU45 SLAVE: *tape unit number*

SWITCH SETTINGS :

SW15 = 1 stop on error
SW14 = 1 loop on error
SW13 = 1 do not print errors
SW12 = 1 do not stop after one pass
SW11 = 1 inhibit iterations
SW10 = 1 halt after current test
SW09 = 1
SW08 = 1 inhibit wrap around data check
SW07 = 1 inhibit wrap around status check
SW06 = 1 selectable wrap data pattern (in single test)
*SW05 = 1 select subtest**
*SW04 = 1 select subtest**
*SW03 = 1 select subtest**
*SW02 = 1 select subtest**
*SW01 = 1 select subtest**
*SW00 = 1 select subtest**

** all zero = all tests*
use "CONTROL G" to enter software SWR at loc. 176

TM03/TU45 BASIC FUNCTION TEST

ABSTRACT :

This program is intended to test all of the basic functional level operations of the TM03/TU45 Mag. Tape system. All functions, write, read, space, erase, rewind ect. will be tested. In addition to the TM03/TU45 tests, the RH will be tested separately in so far as it is possible to separate the RH from the TM03/TU45 itself.

OPERATING PROCEDURES :

START ADDRESS
SA = 200 normal startaddress - enter parameters
SA = 210 restart address - keep parameters

Put Tape Units online, tape loaded at BOT and write ring in.
Answer the following questions:

REGISTER START: 172440 < CR >	
VECTOR: 224 < CR >	
DRIVE NUMBER:0	*controller number*
SLAVE NUMBER:	*TAPE UNIT NUMBER*
SERIAL NUMBER:	*printed by the program*
RH ONLY:	*1 = test only RH*

SWITCH SETTINGS :

SW15 = 1 stop on error
SW14 = 1 loop on error
SW13 = 1 do not print errors
SW12 = 1 do not stop after one pass
SW11 = 1 inhibit iterations
SW10 = 1 halt after current test
SW09 = 1
SW08 = 1
*SW04 = 1 select subtest**
*SW03 = 1 select subtest**
*SW02 = 1 select subtest**
*SW01 = 1 select subtest**
*SW00 = 1 select subtest**

** all zero = all tests*
use "CONTROL G" to enter software SWR at loc. 176

TM03/TU45 DATA RELIABILITY TEST

ABSTRACT :

The program is exercising the TU45 drive that can be operated through the TM03 controller. Up to 8 drives may be tested by a single run of the program. It exercises writes, reads, rewind, tape positioning, EOT - BOT sensing and assumes a good RH and TM03.

OPERATING PROCEDURES :

START ADDRESS

SA = 200 normal startaddress - enter parameters
SA = 204 restart address - keep parameters
SA = 210 same as 204 except data pattern is returned to fixed one
SA = 240 special test sequence / enter only RH addr. and vector
SA = 300 restart - short parameter entry.

Put Tape Units online, at BOT and write ring in.
Answer the following questions:

REGISTER START: 172440<CR>
VECTOR: 224<CR>

DRIVE NUMBER:0	*controller number*
SLAVE NUMBER:0	*tape unit number*
DENSITY:4	*3 = 800, 4 = 1600BPI*
PARITY:	*0 = even, 1 = odd*
FORMAT:	*14 = normal, 15 = core dump*
SLAVE NUMBER:<CR>	*next tape unit or <CR> for no more*
RECORD COUNT: 100	*(1 - 177777) blocking factor*
CHARACTER COUNT: 200	*(20-4000) characters per record*
PATTERN NUMBER: 1	*(0-15) different data patterns*
TAPE MARKS: 0	*1 = one tape mark after each data block*
INTERCHANGE READ: 0	*0 = normal, 1 = interchange read*
SINGLE PASS: 0	*0 = stop after one pass*
STALLS: 1	*1-177777 (time delay between functions)*

SWITCH SETTINGS :

RECOMMENDED SWITCH SETTING : 000720

SW15 = 1 stop on error
SW14 = 1 print read/write statistics
SW13 = 1 do not check for data errors
SW12 = 1 do not check for write status errors
SW11 = 1 do not check for read status errors
SW10 = 1 do not print any errors
SW09 = 1 rewind all available tapes
SW08 = 1 generate random data
SW07 = 1 generate random character count
SW06 = 1 generate random record count
SW05 = 1 yozzle on current record
SW04 = 1 do write/read retries
SW03 = 1 do not read forward
SW02 = 1 do not read reverse
SW01 = 1 read forward first
SW00 = 1 do not write

"CONTROL G" to enter software SWR at loc. 176

TM03/TU45 DRIVE FUNCTION TIMER

ABSTRACT :

This program measures the time required and gap size produced by the TM03/TU45 Mag. tape. The test will check both the logic generated time delays, and the distances traveled by the tape in response. Actual tape speed may also be checked by using the speed tests with an 800 BPI skew tape.

OPERATING PROCEDURES :

.R ZTUSB0

SWR= 000000 NEW=

Put Tape Units online, tape loaded at BOT and write ring in.
Answer the following questions:

TYPE FIRST ADDRESS OF CONTROLLER : 172440	*(standard)*
TYPE TM03 DRIVE #'s TO BE TESTED : 0	*(0= FIRST TM03)*
FOR TM03 DRIVE 0 TYPE SLAVE #'s TO BE TESTED:0	*(normaly slave 0)*
TAPE SPEED TESTS ONLY ? :	*(0=no, 1=yes)*

The program halts after one pass. press continue to do one more pass.

SWITCH SETTINGS :

SW15= 1 halt on error
SW14= 1 loop on current subtest
SW13= 1 do not print errors
SW12= 1
SW11= 1 inhibit iterations
SW10= 1 inhibit printing of function times
SW09= 1 ring bell on error
SW08= 1 type line item after each iteration
SW07= 1
SW06= 1 do not halt after one pass
*SW05= 1 select subtest**
*SW04= 1 select subtest**
*SW03= 1 select subtest**
*SW02= 1 select subtest**
*SW01= 1 select subtest**
*SW00= 1 select subtest**

** all zero = all tests*
use "CONTROL G" to enter software SWR at loc 176

11/21 - TU58 PERFORMANCE EXERCISER

ABSTRACT :

This program will exercise from 1 to 8 TU58 controller boards, each of which supports 1 or 2 drives. The program implements the "maintenance mode" switch within all packet commands. Statistical summaries are provided for all units tested. The program consists of 9 subtests:
Test 1 initiates self test
Test 2 seek test, seeks to BOT then to EOT on both tracks
Test 3 writes, then reads in 512 byte/block mode
Test 4 writes, then reads in 128 byte/block mode
Test 5 write tape
Test 6 read tape
Test 7 write verify tape
Test 8 read modified threshold tape
Test 9 tests modified radial serial protocol

OPERATING PROCEDURES :

This program is running under the supervisory program. This supervisory program will first talk to you.

```
.R NTUUA0

CNTUU-A-0
TU58 PERF EXER
UNIT IS TU58 CONTROLLER
RSTRT ADR 145702
DR>STA<CR>
```

You have to answer the hardware questions.

```
Change HW (L) ? Y<CR>
# UNITS (D) ? 1<CR>
UNIT 0
TU58 CSR (0) 176500 ? <CR>
VECTOR ADDR. (O) 300 ? <CR>
PDT INTERFACE (L) N ? N<CR>
TEST DRIVE 0 (L) Y ? <CR>
TEST DRIVE 1 (L) Y ? <CR>

CHANGE SW (L) ? Y<CR>,

NUMBER OF BLOCKS: TEST 5-8 (8 TO 512) (D) 8 ?
ADD DR # TO DATA PATTERN:TEST 5-8 (L) Y ?
STATISTICS PRINTED AT EOP (L) Y ?
COMPARE DATA ON READ (L) Y ?
PRINT PACKET ON ERROR (L) Y ?
.....
```

To get the summary any time, type <control C> and then PRI<CR>

TU58 PERFORMANCE EXERCISER

ABSTRACT :

This program will exercise from 1 to 8 TU58 controller boards, each of which supports 1 or 2 drives. The program implements the "maintenance mode" switch within all packet commands. Statistical summaries are provided for all units tested. The program consists of 9 subtests:

Test 1 initiates self test
Test 2 seek test, seeks to BOT then to EOT on both tracks
Test 3 writes, then reads in 512 byte/block mode
Test 4 writes, then reads in 128 byte/block mode
Test 5 write tape
Test 6 read tape
Test 7 write verify tape
Test 8 read modified threshold tape
Test 9 tests modified radial serial protocol

OPERATING PROCEDURES :

.R ZTUUF0

This program is running under the supervisory program.
This supervisory program will first talk to you.

CZTUU-F-0
TU58 PERF EXER
UNIT IS TU58 CONTROLLER
RSTRT ADR 145702
DR>STA<CR>

You have to answer the hardware questions.

Change HW (L) ? Y<CR>
 # UNITS (D) ? 1<CR>
UNIT 0
TU58 CSR (0) 176500 ? <CR>
VECTOR ADDR. (O) 300 ? <CR>
PDT INTERFACE (L) N ? N<CR>
TEST DRIVE 0 (L) Y ? <CR>
TEST DRIVE 1 (L) Y ? <CR>

CHANGE SW (L) ? Y<CR>,

NUMBER OF BLOCKS: TEST 5-8 (8 TO 512) (D) 8 ?
ADD DR # TO DATA PATTERN:TEST 5-8 (L) Y ?
STATISTICS PRINTED AT EOP (L) Y ?
COMPARE DATA ON READ (L) Y ?
PRINT PACKET ON ERROR (L) Y ?

To get the summary any time, type <control C> and then PRI<CR>

TU80 DATA RELIABILITY TEST

ABSTRACT :

This program is exercising the TU80 drive and can be used as a basic function test, a data reliability test or a compatibility test. It can test up to 4 units simuntaneously.
There are 6 tests in this program:
Test 1 basic functions
Test 2 data reliability
Test 3 write and read streaming test
Test 4 write compatibility/ write utility
Test 5 read compatibility/ read utility
Test 6 operator selected sequence utility

OPERATING PROCEDURES :

Put Tape Units online, tape loaded at BOT and write ring in.

This program is running under the supervisory program.
This supervisory program will first talk to you.

```
.R ZTUVB0

CZTUV-B-0
DATA RELIABILITY TEST
UNIT IS TU80
RSTRT ADR 145702
DR>STA/FLAG:PNT<CR>          (start, print test NR)
#UNITS (D) ? 1<CR>

UNIT 0
TSSR ADDRESS (0) 172522 ?<CR>
VECTOR (0) 224 ?<CR>

CHANGE SW (L) N<CR>

                        if you type "Y" you can change:
CLEAR COUNTERS (L) Y ?
RESET RANDOM VARIABLES (L) N ?
HALT AFTER EACH CMD (L) N ?
PRINT SOFT ERRORS (L) N ?
INHIBIT RECOVERY (L) N ?
BAD TAPE SPOT DETECT (L) Y ?
DISABLE INTERRUPTS (L) N ?
INHIBIT RFC ERROR REPORT (L) N ?
M7454 RAM DUNP (L) N ?
CHANGE CMD SEQ (L) N ?
```

Test 2 will print a summary table

TU80 FRONT END DIAGNOSTIC PART 1

ABSTRACT :

This program is testing the functionality of the TU80 drive, provides error messages which identify failing functions and aids in the repair of the device.
This is the first test out of four.
There are 11 tests in this program:
Test 01 initialization test
Test 02 ram test
Test 03 command reject test
Test 04 write characteristic test
Test 05 volume check test
Test 06 completion interrupt test
Test 07 basic packet protocol test
Test 08 non-tape motion commands test
Test 09 DMA mempry addressing test
Test 10 initialization after write characteristics test
Test 11 basic write subsystem memory command test

OPERATING PROCEDURES :

Put Tape Units online, tape loaded at BOT .

This program is running under the supervisory program
This supervisory program will first talk to you

```
.R ZTUWA0

CZTUW-A-0
CZTUWA0 TU80 FRONT END PRT A
UNIT IS TU80
RSTRT ADR 145702
DR>STA/FLAG:PNT<CR>                    (start, print test NR)
#UNITS (D) ? 1<CR>

UNIT 0
DEVICE ADDRESS (TSSR) (0) 172522 ?<CR>
INTERRUPT VECTOR (0) 224 ?<CR>
INTERRUPT PRIORITY (0) 5 ?

CHANGE SW (L) N<CR>

                              if you type "Y" you can change:
ENABLE M7454 RAM DUMP ON ERROR (L) N ?
INHIBIT ITERATIONS (L) N ?
```

TU80 FRONT END DIAGNOSTIC PART 2

ABSTRACT :

This program is testing the functionality of the TU80 drive, provides error messages which identify failing functions and aids in the repair of the device. This is the second test out of four. Run test ZTUYA0 and ZTUZA0 after this one.

There are 8 tests in this program:
Test 01 FIFO exerciser test
Test 02 initialize #4 test
Test 03 off-line reject and rewind test
Test 04 basic write data test
Test 05 basic read data (forward and reverse) test
Test 06 manual intervention test
Test 07 configuration typeout test
Test 08 scope loops test

OPERATING PROCEDURES :

Put Tape Units online, tape loaded at BOT and write enabled.

This program is running under the supervisory program.
This supervisory program will first talk to you.

```
.R ZTUXA0

CZTUX-A-0
CZTUXA0 TU80 FRONT END PRT B
UNIT IS TU80
RSTRT ADR 145702
DR>STA/FLAG:PNT<CR>            (start, print test NR)
#UNITS (D) ? 1<CR>

UNIT 0
DEVICE ADDRESS (TSSR) (0) 172522 ?<CR>
INTERRUPT VECTOR (0) 224 ?<CR>
INTERRUPT PRIORITY (0) 5 ?

CHANGE SW (L) N<CR>

                        if you type "Y" you can change:
ENABLE M7454 RAM DUMP ON ERROR (L) N ?
INHIBIT ITERATIONS (L) N ?
```

TU80 FRONT END DIAGNOSTIC PART 3

ABSTRACT :

This program is testing the functionality of the TU80 drive, provides error messages which identify failing functions and aids in the repair of the device.
This is the third test out of four. Run test ZTUZA0 after this one.
There are 4 tests in this program:
Test 01 space records test
Test 02 reread tests
Test 03 write data retry test
Test 04 write tape mark test

OPERATING PROCEDURES :

Put Tape Units online, tape loaded at BOT and write enabled.

This program is running under the supervisory program.
This supervisory program will first talk to you.

```
.R ZTUYA0

CZTUY-A-0
CZTUYA0 TU80 FRONT END PRT C
UNIT IS TU80
RSTRT ADR 145702
DR>STA/FLAG:PNT<CR>                    (start, print test NR)
#UNITS (D) ? 1<CR>

UNIT 0
DEVICE ADDRESS (TSSR) (0) 172522 ?<CR>
INTERRUPT VECTOR (0) 224 ?<CR>
INTERRUPT PRIORITY (0) 5 ?

CHANGE SW (L) N<CR>

                              if you type "Y" you can change:
ENABLE M7454 RAM DUMP ON ERROR (L) N ?
INHIBIT ITERATIONS (L) N ?
```

TU80 FRONT END DIAGNOSTIC PART 4

ABSTRACT :

This program is testing the functionality of the TU80 drive, provides error messages which identify failing functions and aids in the repair of the device.
This is the last one out of four tests.
There are 6 tests in this program:
Test 01 write tape mark retry test
Test 02 skip tape marks test
Test 03 no-op ("clean tape") and initialize test
Test 04 erase and operation incomplete test
Test 05 operations at EOT test
Test 06 function timing test

OPERATING PROCEDURES :

Put Tape Units online, tape loaded at BOT and write enabled.

This program is running under the supervisory program.
This supervisory program will first talk to you.

```
.R ZTUZA0

CZTUZ-A-0
CZTUZA0 TU80 FRONT END PRT D
UNIT IS TU80
RSTRT ADR 145702
DR>STA/FLAG:PNT<CR>          (start, print test NR)
#UNITS (D) ? 1<CR>

UNIT 0
DEVICE ADDRESS (TSSR) (0) 172522 ?<CR>
INTERRUPT VECTOR (0) 224 ?<CR>
INTERRUPT PRIORITY (0) 5 ?

CHANGE SW (L) N<CR>

                    if you type "Y" you can change:
ENABLE M7454 RAM DUMP ON ERROR (L) N ?
INHIBIT ITERATIONS (L) N ?
```

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44	BKTGD1.BIC	11/35/40 MEMORY MANAGEMENT EXER.
45	BQAAA0.BIN	WATCHDOG TIMER WITH CLOCK TEST
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73	CKBHB0.BIC	11/45 REGISTER TEST
74	CKBIB0.BIC	11/45 ASH (ARITHMETIC SHIFT) INSTR. TEST
75	CKBJA0.BIC	11/45 ASHC (ARITHM SHIFT COMB) INSTR. TEST
76	CKBKA0.BIC	11/45 MULTIPLY INSTRUCTION TEST
77	CKBLA0.BIC	11/45 DIVIDE INSTRUCTION TEST
78	CKBME0.BIC	*11/45 TRAP TEST
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80	CKBOA0.BIC	11/45 STATES (USER, KERNEL) TEST
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099	D0EA0 .BIC	PDP11 INSTR. (ROTATE & SHIFT) TEST 5
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107	D6BA0 .BIN	AA11 CALIBRATION
108	D6DB0 .BIN	VT06 DIAGNOSTIC
109	D6FC0 .BIN	LAB11 DIAGNOSTIC
110	DGTAD2.BIC	GT40/GT44 INSTRUCTION TEST 1
111	DGTBD0.BIC	GT40/GT44 INSTRUCTION TEST 2
112	DGTCC0.BIC	GT40/GT44 VISUAL DISPLAY TEST (VR14)
113	DGTDD0.BIC	GT40 ROM VERIFY
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122	EKBAD0.BIC	*11/70 CPU DIAGN. PART 1 (BASIC INSTR)
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130	EMJAD0.BIC	*11/70 MJ11 CORE MEMORY EXERCISER
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133	ERHAE1.BIC	*11/70 RH70 TEST (WITH DISK OR TAPE ON)
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136	ERSCB0.BIC	11/70 RH70 RS03 MAINTENANCE MODE DIAG.
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138	FFPAA1.BIN	*11/34 FP11-A (M8267) DIAGNOSTIC PART 1
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141	FKAAC0.BIC	*11/34 CPU DIAGNOSTIC
142	FKABD0.BIC	*11/34 TRAP TEST
143	FKACA1.BIC	*11/34 EIS INSTRUCTION TEST
144	FKKAB0.BIN	*11/34 CACHE (M8268) DIAGNOSTIC
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146	FKTHB0.BIN	*11/34 MEMORY MANAGEMENT DIAGN.
147	FLOAT .BIN	*PRINTS VECTORS AND ADDRESS ASSIGNMENTS
148	GKAAA0.BIC	*11/04 CPU (M7263) DIAGNOSTIC
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150	JDLAA0.BIC	11/23B SLU/DLV11-J DIAGNOSTIC
151	JFPAA1.BIC	*11/23 WITH FPF11 (M8188 MODULE) PART 1
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153	JKDAD1.BIC	*11/23/24 (KDF11) MEMORY MANAGEM. DIAGN.
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155	JKDCB0.BIC	*11/23/24 KEF11 FLOATING POINT TEST 1
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157	JKDEB0.BIN	*11/24 CPU BOARD (M7133) DIAG.(EIS,MMU,FPP..)
158	JKDFB0.BIN	*11/24 SLU & LTC TEST (M7133)
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160	JKDIB0.BIC	*11/23-B (M8189) SLU & LTC DIAGNOSTIC
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163	JM9AB0.BIN	11/24 ROM M9312 TEST
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167	KKAAB0.BIC	*11/44 CPU & EIS INSTR. EXER.
168	KKABD1.BIC	*11/44 TRAP TEST
169	KKACC0.BIC	*11/44 POWER FAIL TEST
170	KKFAA0.---	11/44 BOOT STRAP ROM DIAGN. -NOT ON DISK-
171	KKFBA0.---	*11/44 CONSOLE ROM DIAGN. -NOT ON DISK-
172	KKKAC0.BIC	*11/44 CACHE (M7097) DIAGNOSTIC
173	KKTAB1.BIC	*11/44 MEMORY MANAGEMENT TEST PART 1
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176	NAAAA0.BIN	AAV11 (A6001 & FALCON) (LOG./FUNCT. TEST
177	NAXAA0.BIN	AXV11-C / ADV11-C (FALCON) FUNCT. TEST.
178	NDLAA0.BIN	DLV11-J (M8043 & FALCON) LOGIC TEST

179	NDMAA0.BIC	DMV11 (M8053/M8064)(FALCON) MP TEST 1
180	NDMBA0.BIC	DMV11 (M8053/M8064)(FALCON) MP TEST 2
181	NDMCA0.BIC	DMV11 (M8053/M8064)(FALCON) LU TEST 1
182	NDMDA0.BIC	DMV11 (M8053/M8064)(FALCON) LU TEST 2
183	NDMEA0.BIC	DMV11 (M8053/M8064)(FALCON) LU TEST 3
184	NDPVA0.BIN	DPV11 (FALCON) FUNCTIONAL TEST
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191	NDUTA0.BIN	DUV11 (FALCON) OFFLINE TRANSMITTER TEST
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193	NDUVA0.BIN	DUV11 (FALCON) OFFLINE COMBINED TEST
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195	NDVCA0.BIN	DLV11-F (FALCON) OFFLINE TEST
196	NDZAA0.BIN	DZV11 (FALCON) DIAGNOSTIC PART 1
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198	NDZCA0.BIN	DZV11 (FALCON) CABLE/ECHO TEST
199	NIBAA0.BIN	IBV11-A (FALCON) DIAGNOSTIC
200	NKAFA0.BIN	DRV11 (FALCON) LOGIC TEST
201	NKMAA0.BIC	LSI MOS/CORE MEMORY 0-124K EXER.
202	NKMBB0.BIC	KMV11-A (FALCON) LINE CONTR. TEST
203	NKMCA0.BIN	KMV11-A (FALCON) FIRMWARE TEST
204	NKMDA0.BIC	KMV11-A/B (M7500/M7501) (FALCON) TEST
205	NKMEA0.BIC	KMV11-B (FALCON) LINE CONTR. TEST
206	NKTCA0.BIC	KXT11-CA (M8377) BUS TEST
207	NKWAA0.BIC	KWV11-A (FALCON) DIAGNOSTIC
208	NKXAB0.BIC	*KXT11 SBC 11/21,11/21+ CPU TEST
209	NMXAA0.BIC	MXV11-A (FALCON) TEST
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231	OEEBA0.BIC	KDJ11-B EEPROM DUTCH LOADER
232	OEECA0.BIC	KDJ11-B EEPROM FRENCH LOADER
233	OEEDA0.BIC	KDJ11-B EEPROM GERMAN LOADER
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259	RLPDA0.BIN	LPA/AR11 LOGIC TEST 2
260	RLPEA0.BIN	LPA/AR11 LOGIC TEST 3
261	RLPFC0.BIN	LPA/DR11-K INPUT OUTPUT LOGIC TEST
262	RLPGC0.BIN	LPA/KW11-K DUAL REAL TIME CLOCK TEST
263	RLPHA0.BIN	LPA/LPS DIAGNOSTIC TEST 1
264	RLPIA0.BIN	LPA/LPS DIAGNOSTIC TEST 2
265	RLPJA0.BIN	LPA/LPS DIAGNOSTIC TEST 3
266	RLPKC0.BIN	LPA/AD11-K TEST (WITH/WITHOUT WRAPAR.)
267	RLPLA0.BIC	LPA/DMC11 (M8200-YC) DIAGNOSTIC TEST 1
268	RLPMB0.BIN	LPA/DMC11 (M8200-YC) DIAGNOSTIC TEST 2
269	RLPNA1.BIC	LPA/IPBM (M8254) FIELD DIAGNOSTIC
270	TDHAB0.MPG	DH11 DEVICE ROUTINE FOR MPG

271	TDJAB0.MPG	DJ11 DEVICE ROUTINE FOR MPG
272	TDLAB0.MPG	DL11 DEVICE ROUTINE FOR MPG
273	TDQAB0.MPG	DQ11 DEVICE ROUTINE FOR MPG
274	TDUAA0.MPG	DU11 DEVICE ROUTINE FOR MPG
275	TLPAB0.MPG	LP11/LS11 DEVICE ROUTINE FOR MPG
276	TMGAC0.MPG	MAINTENANCE PROGRAM GENERATOR
277	TMMAB0.MPG	MEMORY MANAGEMENT FOR MPG
278	TMSAA0.MPG	MINIMUM SUPPORT DEV ROUTINE
279	TPCAB0.MPG	PC11/PR11 DEVICE ROUTINE FOR MPG
280	TR3AA0.MPG	RP02/03 DEVICE ROUTINE FOR MPG
281	TR6AA0.MPG	RK06 DEVICE ROUTINE FOR MPG
282	TRKAB0.MPG	RK05 DEVICE ROUTINE FOR MPG
283	TRPAB0.MPG	RP04/05/06 DEVICE ROUTINE FOR MPG
284	TRSAA0.MPG	RS03/04 DEVICE ROUTINE FOR MPG
285	TTCAB0.MPG	TC11 DEVICE ROUTINE FOR MPG
286	TTMAB0.MPG	TM11 DEVICE ROUTINE FOR MPG
287	TVDAB0.MPG	VALID DEVICE TABLES FOR MPG
288	TCMPG .BIN	TC11 MPG MONITOR
289	RKMPG .BIN	RK11 MPG MONITOR
290	TMMPG .BIN	TM11/TU10 MPG MONITOR
291	THMPG .BIN	TM02/TU16 MPG MONITOR
292	RXMPG .BIN	RX11/RX01 MPG MONITOR
293	RBMPG .BIN	RP04/05/06 MPG MONITOR
294	VAAAA1.BIC	AAV11 4 CHANNEL D/A CONVERTER TEST
295	VADAC0.BIC	ADV11 A/D CONVERTER PERFORMANCE TEST
296	VAXAB0.BIC	ADV11-C/AXV11-C A/D CONVERTER TEST
297	VCDAB0.BIC	MDE MICRO DEVEL. ENVIRONM. M8740 TEST
298	VCDBB0.BIC	MDE STATE ANALYZER (M8741) TEST
299	VCDCB0.BIC	MDE TARGET EMULATOR (M8742) TEST
300	VCDDB0.BIC	MDE SYSTEM BUS DIAGNOSTIC
301	VCLHC0.BIN	DPV11/DA/DB (M8020) DATA COM LINK TEST
302	VCMAA0.BIC	CMQ11-K CSS OPTION CARD RD DIAGN.
303	VDHAE0.BIC	*DHV11 (M3104) FUNCTIONAL TEST 1
304	VDHBE0.BIC	*DHV11 (M3104) FUNCTIONAL TEST 2
305	VDHCE1.BIC	*DHV11 (M3104) FUNCTIONAL TEST 3
306	VDHEC0.BIC	*DHV11 (M3104) TEST ORION
307	VDLAB0.BIC	*DLV11-J LOGIC TEST
308	VDMAC1.BIN	*DMV11 MICRO CONTR. STATIC TEST 1
309	VDMBC0.BIN	*DMV11 (M8053 OR M8064) STATIC TEST 2
310	VDMCC1.BIN	*DMV11 LINE UNIT STATIC TEST 1
311	VDMDC0.BIN	*DMV11 LINE UNIT STATIC TEST 2
312	VDMEC0.BIN	*DMV11 LINE UNIT STATIC TEST 3
313	VDPVC1.BIN	*DPV11 (M8020) FUNCTIONAL DIAGNOSTIC
314	VDRAC0.BIC	DRV11-B DMA AND LOGIC TEST
315	VDRBA0.BIN	DRV11-B (M7950) INTERPROCESSOR EXERCISER
316	VDRCC0.BIC	DRV11-J (M8049) DIAGNOSTIC TEST 1

317	VDRDB0.BIC	DRV11-J (M8049) DIAGNOSTIC TEST 2
318	VDVAD1.BIN	*DLV11-E OFFLINE TEST
319	VDVCC1.BIN	DLV11-F OFFLINE TEST
320	VDZAD3.BIC	*DZV11/DZQ11 DIAGN. TEST 1
321	VDZBD0.BIC	*DZV11/DZQ11 DIAGN. TEST 2
322	VDZCB1.BIN	*DZV11/DZQ11 CABLE/ECHO TEST
323	VDZDA0.BIN	DZV11 OVERLAY FOR INTERPROC. PROG.
324	VHQAD0.BIN	DHV11/DHQ11 CXA16/CXY08 FUNCT. TEST
325	VIBAB0.BIC	IBV11-A DIAGNOSTIC (ADDRESS 760150)
326	VIBBA1.BIC	IBV11-A DIAGNOSTIC (ADDRESS 771420)
327	VKAAC0.BIC	*11/03 CPU BASIC INSTRUCTION TEST
328	VKABB0.BIC	*11/03 CPU EIS INSTRUCTION TEST
329	VKACC1.BIC	*11/03 FIS INSTRUCTION TEST
330	VKADC1.BIC	*11/03 TRAP TEST
331	VKAEB2.BIC	*DLV11 WITH LSI TEST
332	VKAFE0.BIN	DRV11 LOGIC TEST
333	VKAHA1.BIC	*LSI 4K SYSTEM (INTERR.) EXER.
334	VKAIB0.BIN	*11/03 DIS (DIBOL INSTR. SET) TEST 1
335	VKAJB0.BIN	*11/03 DIS (DIBOL INSTR. SET) TEST 2
336	VKALA1.BIC	*11/03 (30K MEMORY & FIS) TRAP TEST
337	VKDAD0.BIN	PDT 11/150 SYSTEM EXERCISER
338	VKDBA0.BIC	PDT 11/130 SYSTEM EXERCISER
339	VKMAB1.BIN	KMV11-A/B (M7500/M7501) LOGIC TEST
340	VKMBB1.BIN	KMV11-A LINE CONTROLLER TEST
341	VKMCA1.BIN	KMV11-A (FIRMWARE) FUNCTIONAL TEST
342	VKMEB1.BIN	KMV11-B (M7501) LINE CONTR. TEST
343	VKMHA0.BIN	KMV11-C LOGIC DIAGNOSTIC
344	VKMJA0.BIN	KMV11-C (FIRMWARE) FUNTIONAL TEST
345	VKPAA0.BIC	KPV11-A DIAGNOSTIC
346	VKUAA0.BIN	KUV11 (LSI WCS) DIAGNOSTIC
347	VKWAC0.BIC	KWV11-A PROGR. REAL-TIME CLOCK TEST
348	VM8AF0.BIC	*BDV11/KDF11 BOOTSTRAP/ROM DIAGN. TEST
349	VMEMA0.BIC	LSI NON-VOLATILE MEMORY(CORE,BBU-MOS)TEST
350	VMJAB0.BIC	*MSV11-J (MIXED L-J-P) MEMORY DIAGNOSTIC
351	VMNAC1.BIC	MINC-11 ANALOG/DIGITAL PERFORMANCE TEST
352	VMNBB0.BIC	MINC-11 DIGITAL-IN DIAGNOSTIC
353	VMNCB1.BIC	MINC-11 CLOCK TEST
354	VMNDA1.BIC	MINC-11 DIGITAL/ANALOG TEST
355	VMNEA1.BIC	MINC-11 DIGITAL-OUT TEST
356	VMNFC0.BIC	MINC-11 STARTUP/SIZER DIAGN.
357	VMNGA0.BIC	MINC-11 CHAIN TERMINATOR PROGRAM
358	VMRAA0.BIC	LSI11 UVPROM-RAM TEST
359	VMSAC0.BIC	*0-4 MEGABYTE MEMORY EXER. (MIXED D,L,P)
360	VMSBD0.BIC	*0-4 MEGABYTE MEMORY QUICK VERIFY
361	VMXAA0.BIC	*MXV11-A LOGIC TEST (2 SLU,ROM,CLOCK,RAM)
362	VMXBA0.BIN	*MXV11-B LOGIC TEST (2 SLU,ROM,CLOCK,RAM)

363	VNIAD0.BIC	*DEQNA NETWORK INTERCONNECT EXERCISER
364	VPCAH0.BIC	PCS (PROCESS CONTROL SS) TEST
365	VRLAC0.BIN	*RLV11 CONTROLLER TEST
366	VRLBC0.BIC	*RLV12 OR RLV11 CONTROLLER TEST
367	VTSAC0.BIC	*TSV05 SUBSYSTEM FUNCTIONAL TEST 1
368	VTSBE0.BIC	*TSV05 SUBSYSTEM FUNCTIONAL TEST 2
369	VTSCD0.BIC	*TSV05 SUBSYSTEM FUNCTIONAL TEST 3
370	VTSDE0.BIC	*TSV05 SUBSYSTEM FUNCTIONAL TEST 4
371	VTSED0.BIC	*TSV05 DATA RELIABILITY TEST
372	VVSAB1.BIC	VSV11/VS11 (CSS) DIAGNOSTIC
373	VVTAA1.BIN	VTV30-J/H VT30-H LOGIC TEST
374	VVTBA0.BIN	VTV30-J/H VT30-H DISPLAY TEST
375	VVTCA0.BIN	VTV30-K LOGIC TEST
376	WQAAB0.BIN	11W03 LSI SYSTEM TEST
377	XAAAD0.OBJ	DEC-X M. AA11/VT01-A EXER
378	XAABC0.OBJ	DEC-X M. AA11-K SCOPE CONTR. EXER
379	XAACB0.OBJ	DEC-X M. AAV11 EXER
380	XAAVA0.OBJ	DEC-X M. AAV11-D EXER
381	XADAE0.OBJ	DEC-X M. AD01-D A/D CONV. EXER
382	XADBB0.OBJ	DEC-X M. AD11-K EXER
383	XADCB0.OBJ	DEC-X M. ADV11 EXER
384	XADVA0.OBJ	DEC-X M. ADV11-D EXER
385	XAFAE0.OBJ	DEC-X M. AFC11 CONVERTER EXER
386	XARAC0.OBJ	DEC-X M. AR11 A/D CONVERTER EXER
387	XBBAB0.OBJ	DEC-X M. KIT11-D EXER
388	XBEAC0.OBJ	DEC-X M. M7855 BUS-TESTER EXER
389	XBMCN0.OBJ	DEC-X M. DIVERS. BOOTSTRAP EXER
390	XBMDE0.OBJ	DEC-X M. BDV11 ROMS EXER MODULE
391	XBMEB0.OBJ	DEC-X M. BM873-YF BOOTSTRAP EXER
392	XBMFB0.OBJ	DEC-X M. BM873-YH BOOTSTRAP EXER
393	XBMGB0.OBJ	DEC-X M. BM873-YJ BOOTSTRAP EXER
394	XBMHB0.OBJ	DEC-X M. M9312 BOOTSTRAP EXER
395	XBMIB0.OBJ	DEC-X M. M9301/M9311 BOOTSTRAP EXER
396	XBTAB0.OBJ	DEC-X M. BUS TESTER A EXER
397	XBTBB0.OBJ	DEC-X M. BUS TESTER B EXER
398	XBTCC0.OBJ	DEC-X M. Q22BE Q-BUS EXER
399	XCBAE0.OBJ	DEC-X M. CB11 SCAN EXER
400	XCBBE0.OBJ	DEC-X M. CB11 DISTRIBUTE EXER
401	XCBCF0.OBJ	DEC-X M. CB11-HA EXER
402	XCDAG0.OBJ	DEC-X M. CD11 EXER
403	XCIAB0.OBJ	DEC-X M. CISP EXER
404	XCMAC0.OBJ	DEC-X M. CSS CMS11K EXER
405	XCMJB0.OBJ	DEC-X M. CMR11 EXER
406	XCPAG0.OBJ	DEC-X M. PDP11 CPU EXER
407	XCPBK0.OBJ	DEC-X M. CPU EIS EXER

408	XCRAG0.OBJ	DEC-X M. CR11 EXER
409	XCSTA0.OBJ	DEC-X M. CAST CONTROL EXER
410	XDCAG0.OBJ	DEC-X M. DC11 EXER
411	XDFAB0.OBJ	DEC-X M. DFA01
412	XDHAL0.OBJ	DEC-X M. DH11 16 LINE EXER
413	XDHUA0.OBJ	DEC-X M. DHU11 EXER
414	XDHVH0.OBJ	DEC-X M. DHV11 EXER
415	XDJAL0.OBJ	DEC-X M. DJ11 EXER
416	XDLAL0.OBJ	DEC-X M. DL11-W/DLV11-J EXER
417	XDLBD0.OBJ	DEC-X M. DL11-E/DLV11-E EXER
418	XDMBJ0.OBJ	DEC-X M. DM11-BB 16 LINE EXER
419	XDMCC0.OBJ	DEC-X M. DMC-11 EXER
420	XDMDF0.OBJ	DEC-X M. DMP11/DMV11 EXER
421	XDMEC0.OBJ	DEC-X M. DMP11/DMV11 SLV
422	XDMRC0.OBJ	DEC-X M. DMR-11 EXER
423	XDMSA0.OBJ	DEC-X M. DM11-BA 9 LINE EXER
424	XDNAH0.OBJ	DEC-X M. DN11 EXER
425	XDPAE0.OBJ	DEC-X M. DP11 EXER
426	XDPBB0.OBJ	DEC-X M. DUP11 EXER
427	XDPVC0.OBJ	DEC-X M. DPV11 EXER
428	XDQAI0.OBJ	DEC-X M. DQ11 EXER
429	XDRAD0.OBJ	DEC-X M. DR11-A EXER
430	XDRBJ0.OBJ	DEC-X M. DR11-B EXER
431	XDRCI0.OBJ	DEC-X M. DR11-C EXER
432	XDRDC0.OBJ	DEC-X M. DR11-K EXER
433	XDREC0.OBJ	DEC-X M. DR11-L EXER
434	XDRFE0.OBJ	DEC-X M. DRV11-B EXER
435	XDRJC0.OBJ	DEC-X M. DRV11-J EXER
436	XDRKA0.OBJ	DEC-X M. CSS DR70 EXER
437	XDRQA0.OBJ	DEC-X M. DRQ3B INTERFACE M7549
438	XDRUA0.OBJ	DEC-X-M. DRU11 EXER
439	XDRVB0.OBJ	DEC-X M. DRV11-WA EXER
440	XDRWD0.OBJ	DEC-X M. DR11-W EXER
441	XDTAD0.OBJ	DEC-X M. DTE20 EXER
442	XDUAI0.OBJ	DEC-X M. DU11 EXER
443	XDUBE0.OBJ	DEC-X M. UDA50/KDA50 EXER
444	XDVAB1.OBJ	DEC-X M. DV11 EXER
445	XDXAG0.OBJ	DEC-X M. DX11 EXER
446	XDZAG0.OBJ	DEC-X M. DZ11 EXER
447	XDZBC0.OBJ	DEC-X M. DZV11/DZQ11 EXER
448	XDZMA0.OBJ	DEC-X M. DZM11 EXER
449	XFPAG0.OBJ	DEC-X M. FP11 (11/40,45) EXER
450	XFPBF0.OBJ	DEC-X M. FP11/A/B/C EXER
451	XFPCA0.OBJ	DEC-X M. CTRL BRIDGE EXER
452	XGTAE0.OBJ	DEC-X M. GT40 EXER
453	XIBAD0.OBJ	DEC-X M. IBV11-A EXER

454	XICAD0.OBJ	DEC-X M. ICS11 EXER
455	XICBC0.OBJ	DEC-X M. ICR11 EXER
456	XIEAA0.OBJ	DEC-X M. IEU11/IEQ11 EXER
457	XIEBA0.OBJ	DEC-X M. IEC11-A EXER
458	XIECA0.OBJ	DEC-X M. IEC11-B EXER
459	XKCTA0.OBJ	DEC-X M. KCT32 EXER
460	XKEAD0.OBJ	DEC-X M. KE11 EXER
461	XKGAD0.OBJ	DEC-X M. KG11 EXER
462	XKLAE0.OBJ	DEC-X M. KL11 EXER
463	XKMAA0.OBJ	DEC-X M. KMC11-B EXER
464	XKMCD0.OBJ	DEC-X M. KMC11 EXER
465	XKMDB0.OBJ	DEC-X M. KMV11-A/B EXER
466	XKMKA0.OBJ	DEC-X M. KMV11-C EXER
467	XKMSA0.OBJ	DEC-X M. KMS11-K EXER
468	XKUAB0.OBJ	DEC-X M. KUV11-AA EXER
469	XKWAH0.OBJ	DEC-X M. KW11-L EXER
470	XKWBL0.OBJ	DEC-X M. KW11-P EXER
471	XKWCB0.OBJ	DEC-X M. KW11-W EXER
472	XKWDB0.OBJ	DEC-X M. KW11-K EXER
473	XKWEB0.OBJ	DEC-X M. KWV11-K EXER
474	XKWFB0.OBJ	DEC-X M. GROSS TMNG EXER
475	XKWGB0.OBJ	DEC-X M. KW11-C EXER
476	XLKAB0.OBJ	DEC-X M. LK11 EXER
477	XLPAF0.OBJ	DEC-X M. LP11 PRINTER EXER
478	XLPBF0.OBJ	DEC-X M. LPS-KW EXER
479	XLPCE0.OBJ	DEC-X M. LPS11/LPS-VC EXER
480	XLPDF0.OBJ	DEC-X M. LPS-AD,NP EXER
481	XLPED0.OBJ	DEC-X M. LPD11 EXER
482	XLPFB0.OBJ	DEC-X M. LP20 EXER
483	XLPHE0.OBJ	DEC-X M. LPA11-XX EXER
484	XLPJB0.OBJ	DEC-X M. LPV11 EXER
485	XMLAA0.OBJ	DEC-X M. ML11 EXER
486	XMNAB0.OBJ	DEC-X M. MNCAD (A/D) EXER
487	XMNBB0.OBJ	DEC-X M. MNCDI EXER
488	XMNCB0.OBJ	DEC-X M. MNCKW EXER
489	XMNDB0.OBJ	DEC-X M. MNCDA EXER
490	XMNEB0.OBJ	DEC-X M. MNCDO EXER
491	XMRAA0.OBJ	DEC-X M. M7765 MIRA MODULE EXER
492	XMRBA0.OBJ	DEC-X M. M7763 MIRA MODULE EXER
493	XNCAD0.OBJ	DEC-X M. NC11-A EXER
494	XNCBB0.OBJ	DEC-X M. NCV11-A EXER
495	XPAAF0.OBJ	DEC-X M. PA611 READER EXER
496	XPABG0.OBJ	DEC-X M. PA611 PUNCH EXER
497	XPCCE0.OBJ	DEC-X M. PC11 EXER
498	XPCSC0.OBJ	DEC-X M. PCS11 I/O EXER
499	XPLAC0.OBJ	DEC-X M. PCL EXER

500	XQNAD0.OBJ	DEC-X M. DEQNA EXER
501	XRCAD0.OBJ	DEC-X M. RC11 EXER
502	XRCFC0.OBJ	DEC-X M. RC25 EXER
503	XRFAG0.OBJ	DEC-X M. RF11 EXER
504	XRHAA0.OBJ	DEC-X M. CSS RH01 EXER
505	XRKAG0.OBJ	DEC-X M. RK11/RK05 EXER
506	XRKBH1.OBJ	DEC-X M. RK611 RK06/07 EXER
507	XRLAK0.OBJ	DEC-X M. RL11/RLV11/RLV12 EXER
508	XRMBC0.OBJ	DEC-X M. RM02/03 WITH RH11 EXER
509	XRMDB0.OBJ	DEC-X M. RP04/5/6 RM02/3 EXER
510	XRNAB0.OBJ	DEC-X M. RP07/RM02/3/5/80 EXER
511	XRQAI0.OBJ	DEC-X M. RQDX1/2/3 RUX50 EXER
512	XRXAE0.OBJ	DEC-X M. RX01 EXER
513	XRXBC0.OBJ	DEC-X M. RX02 EXER
514	XTAAD0.OBJ	DEC-X M. TA11 EXER
515	XTCAG0.OBJ	DEC-X M. TC11 EXER
516	XTKAC0.OBJ	DEC-X M. TK50 EXER
517	XTKBB0.OBJ	DEC-X M. TK25 EXER
518	XTMAJ0.OBJ	DEC-X M. TM11 EXER
519	XTMBM0.OBJ	DEC-X M. TM02/03 TU/TE16 EXER
520	XTMDB0.OBJ	DEC-X M. TM78 EXER
521	XTRAD0.OBJ	DEC-X M. TR79F EXER
522	XTSAC0.OBJ	DEC-X M. TS11/TS04/TU80 EXER
523	XTSVA0.OBJ	DEC-X M. TSV05 EXER
524	XTUAD0.OBJ	DEC-X M. TU58 EXER
525	XTUCB0.OBJ	DEC-X M. TU81 (E) EXER
526	XUACB0.OBJ	DEC-X M. DEUNA EXER
527	XUADB0.OBJ	DEC-X M. DELUA EXER
528	XUDAD0.OBJ	DEC-X M. UDC11 EXER
529	XVSAC0.OBJ	DEC-X M. VS60 EXER
530	XVSBB0.OBJ	DEC-X M. VSV01 EXER
531	XVSCB0.OBJ	DEC-X M. VSV11 CSS EXER
532	XVSVA0.OBJ	DEC-X M. VSV21 EXER
533	XVTAB0.OBJ	DEC-X M. VT20 EXER
534	XVTBB0.OBJ	DEC-X M. DH11/VT20 EXER
535	XVTCB0.OBJ	DEC-X M. VTV30 CSS EXER
536	XVTVB0.OBJ	DEC-X M. VTV30H/J VT30H EXER
537	XXYAD0.OBJ	DEC-X M. XY11 PLOTTER EXER
538	XXYBB0.OBJ	DEC-X M. CSS XY311 EXER
539	ZAABA0.BIN	AA11-A/B/C SCOPE CONTROL TEST
540	ZAACB0.BIC	AA11-K ANALOG CIRCUITRY TEST
541	ZAAFA0.BIN	AAF01-A WITH DRU11-C/DR11-C TEST
542	ZAAVA0.BIN	AAV11-D DRS LOGIC TEST
543	ZADAC0.BIN	AD02/AD11 DIAGNOSTIC
544	ZADBB0.BIN	AD01-D DIAGNOSTIC TEST
545	ZADFA0.BIN	ADF11 CONVERSION TEST

546	ZADGA0.BIN	ADF11 LOGIC DIAGNOSTIC TEST 1
547	ZADHA0.BIN	ADF11 ANALOG TESTS 2
548	ZADIA0.BIN	ADF11 EXERCISER FOR 1024 CANNEL
549	ZADJA0.BIN	AD02 SPECIAL 1024 CH. LOGIC TEST
550	ZADKA0.BIN	ADF11 MULTI CH. SAMPLE & HOLD TEST
551	ZADLB3.BIC	AD11-K PERFORMANCE TEST
552	ZADVA0.BIN	ADV11-D DRS LOGIC TEST
553	ZAFAC0.BIC	AFC11 ANALOG MULTIPLEXER DIAGNOSTIC
554	ZARAB0.BIC	AR11 DIAGNOSTIC TEST 1
555	ZARBB0.BIC	AR11 DIAGNOSTIC TEST 2
556	ZARCB1.BIC	AR11 DIAGNOSTIC TEST 3
557	ZBMAE0.BIC	BM792YA-H/K/L BOOTSTRAP LOADER TEST
558	ZBMBA0.BIN	BM792-YB DIAGNOSTIC TEST
559	ZBMCA0.BIN	BM792-YC DIAGNOSTIC TEST
560	ZBMDJ0.BIC	BM873 UNIVERSAL RESTART ROM TEST
561	ZBMHA0.BIC	BM792-YH BOOTSTRAP LOADER TEST
562	ZBMKB0.BIC	BM792-YK BOOTSTRAP LOADER TEST
563	ZCBAC0.BIN	CB11 LOGIC TEST
564	ZCBHB0.BIN	CB11-HA (M7291) LOGIC TEST
565	ZCDAD0.BIN	CD11 CARD READER DIAGNOSTIC
566	ZCDBB0.BIN	CD11/CD20 CARD READER DIAGNOSTIC
567	ZCLKC0.BIN	*DMR11,DMC11 DATA COMM. LINK TEST
568	ZCLMC0.BIN	*DMP11,DMV11 DATA COMM. LINK TEST
569	ZCMBB1.BIN	CM11-F CARD READER DIAGNOSTIC TEST
570	ZCMJC0.BIN	CMR11 (COMPACT MICRO REMOTE) TEST
571	ZCRAC0.BIN	CR11 CARD READER TEST
572	ZCRBC0.BIC	CR11/CM11-F DIAGNOSTIC TEST
573	ZCTAA0.BIN	CTS11-JC WITH 8035/8045 (ASCII) TEST
574	ZCTBA0.BIN	CTS11-JC WITH 8035/8045 (HOLLO) TEST
575	ZDAAA0.BIN	DA11-F BUS WINDOW STATIC TEST
576	ZDABA0.BIN	DA11-F BUS WINDOW EXERCISER
577	ZDAVA0.BIN	DAV11 (CSS) INTERPROCESSOR EXERCISER
578	ZDCAD0.BIN	DC11 (ASYNC. MODEM INTERF.) OFFLINE TEST
579	ZDCBB0.BIN	DC11 (ASYNC. MODEM INTERF.) ONLINE TEST
580	ZDCLB0.BIC	*DUP11 DATA COMM. LINK TEST
581	ZDCOC0.BIN	DC11 OVERLAY FOR INTERPROC. TEST
582	ZDFAC0.BIN	DU11/DFC11 & DP11/DFC11 OFFLINE EXER
583	ZDFBB0.BIN	DFA01 FUNCTIONAL DIAGN.
584	ZDHAD0.BIN	*DH11 STATIC LOGIC TEST
585	ZDHBC0.BIN	*DH11 MEMORY TEST
586	ZDHCC0.BIN	*DH11 TRANSM. RECEIVER LOGIC TEST
587	ZDHDD0.BIN	*DH11 SPEED SELECTION LOGIC TEST
588	ZDHEC0.BIN	DH11 CHARACTER LENGTH AND DATA TEST
589	ZDHFC0.BIN	DH11 SINGLE LINE DATA TEST
590	ZDHGC0.BIN	DH11 SINGLE LINE PARITY & MULTI L. DATA
591	ZDHHC0.BIN	DH11 AUTO-ECHO TEST

592	ZDHID0.BIN	DH11 BREAK AND HALF-DUPLEX TEST
593	ZDHJC0.BIC	DH11 ECHO / CABLE TEST
594	ZDHKF0.BIN	*DH11 MODEM CONTROL MULTIPLEXER TEST
595	ZDHLC0.BIN	DH11 OVERLAY FOR INTERPROC. TEST
596	ZDHMD2.BIC	*DH11 COMPREHENSIVE DIAG. TEST
597	ZDHND0.BIC	*DH11 DATA RELIABILITY TEST
598	ZDHUB0.BIN	*DHU11 FUNCTIONAL VERIFIC. TEST 1
599	ZDHVB0.BIN	*DHU11 FUNCTIONAL VERIFIC. TEST 2
600	ZDHWB0.BIN	*DHU11 FUNCTIONAL VERIFIC. TEST 3
601	ZDHXA1.BIN	*DHU11 FUNCTIONAL VERIFIC. TEST 4
602	ZDJAF0.BIC	DJ11 LOGIC TEST
603	ZDJBG0.BIC	DJ11 ON LINE/OFF LINE EXER.
604	ZDJDB0.BIN	DJ11 OVERLAY FOR INTERPROC. TEST
605	ZDLAH0.BIN	*DL11-E,C,D OFF LINE TEST
606	ZDLBC0.BIN	DL11-E ON LINE TEST
607	ZDLCD0.BIN	DL11-C,D E OFF LINE TEST
608	ZDLDI0.BIN	*DL11-W / 11/44 MFM SLU TEST
609	ZDLOD0.BIN	DL11 OVERLAY FOR INTERPROC. TEST
610	ZDMAD0.BIN	DM11 (ASYNC. DATA MUX) LOGIC TEST
611	ZDMBD0.BIC	DM11 (ASYNC. DATA MUX) DATA TEST
612	ZDMCD0.BIN	*DMC11 (M8200-YA/YB)FUNCTIONAL TEST
613	ZDMED2.BIC	*DMC11 (M8201 OR M8202)LINE UNIT TEST 1
614	ZDMFC2.BIC	*DMC11 (M8201 OR M8202)LINE UNIT TEST 2
615	ZDMGD0.BIC	*DMC11-AR/AL ((M8200-YA/YB) CROM & JUMP TEST
616	ZDMHC1.BIC	*DMC11 FREE RUNNING TEST
617	ZDMID3.BIC	*DMR11 FUNCTIONAL DIAGNOSTIC
618	ZDMOA0.BIN	DMC11 OVERLAY FOR INTERPROC. TEST
619	ZDMPD0.BIC	*DMR11 MICROPROC. M8200/04/07 TEST 1
620	ZDMQE0.BIC	*DMR11 MICROPROC. M8200/04/07 TEST 2
621	ZDMRF0.BIC	*DMC/KMC/DMR11 (M8203) LINE UNIT TEST 1
622	ZDMSF0.BIC	*DMC/KMC/DMR11 (M8203) LINE UNIT TEST 2
623	ZDMTF0.BIC	DMP/DMV11 MULTIDROP INTERF. TEST
624	ZDNAD0.BIN	DN11 DIALEX STATIC AND ONLINE TEST
625	ZDPAD0.BIN	DP11 EXERCISER
626	ZDPBC0.BIC	*DUP11 OFF LINE DIAGN. TEST 1
627	ZDPCD0.BIC	*DUP11 OFF LINE DIAGN. TEST 2
628	ZDPDD0.BIN	*DUP11 DIAGNOSTIC TEST 3
629	ZDPEC0.BIN	*DUP11 CONFIDENCE TEST
630	ZDPFB0.BIN	DUP11 OVERLAY FOR INTERPROC. TEST
631	ZDPGB0.BIN	VT62/DUP11 DIAGNOSTIC
632	ZDPOC0.BIN	DP11 OVERLAY FOR INTERPROC. TEST
633	ZDQAD0.BIC	DQ11 BASIC R/W TEST 1
634	ZDQBD0.BIC	DQ11 BASIC R/W TEST 2
635	ZDQCE0.BIC	DQ11 BASIC NPR AND INTERRUPT TEST
636	ZDQDE0.BIC	DQ11 RECEIVER TRANSMITTER EXER.
637	ZDQEE0.BIC	DQ11 MISC. RX AND TX TESTS

638	ZDQFF0.BIC	DQ11 CHARACTER DETECT TESTS
639	ZDQGB0.BIC	DQ11 STARTER PROG. (BUILD A PARAM.)
640	ZDQHE0.BIC	DQ11 CHARACTER LENGTH AND INTERR. TEST
641	ZDQOD0.BIN	DQ11 OVERLAY FOR INTERPROC. TEST
642	ZDRBI0.BIN	*DR11-B/DA11-B NPR LOGIC TEST
643	ZDRCH1.BIC	*DR11-C LOGIC TEST (MAITEN. CABLE)
644	ZDRDA0.BIN	DR11-A DUAL INTERFACE MASTER TEST
645	ZDREA0.BIN	DR11-A DUAL INTERFACE SLAVE TEST
646	ZDRFA0.BIN	DR11-A DUAL INTERFACE EXERCISER
647	ZDRGE0.BIC	DR11-K LOGIC TEST (MAINT. CABLE)
648	ZDRHA1.BIN	DR11-L/M EXER (WITH MAINT. CABLE)
649	ZDRIB0.BIC	DR11-A LOGIC TEST (MAINT. CABLE)
650	ZDRKB0.BIN	DR11-W INTERPROC. EXER (2 COMPUTER)
651	ZDRLD0.BIC	DR11-W NPR TEST IN DR11-W AND B MODE
652	ZDRMA0.BIN	DR70 MASSBUS CHANNEL INTERF. DIAG.
653	ZDRQA0.BIN	DRQ3B PARALLEL DMA I/O MOD. FUNCT. T
654	ZDRUA0.BIN	DRU11-C/DRQ11-C PROCESSOR LINK TEST
655	ZDRVC0.BIN	DRV11-WA DMA INTERFACE TEST
656	ZDTAB0.BIC	DT11 DIAGNOSTIC
657	ZDUAE0.BIC	DU11 OFF LINE LOGIC TEST
658	ZDUBD0.BIC	DU11 OFF LINE RECEIVER TEST
659	ZDUCD0.BIC	DU11 OFF LINE RECEIVER TIMING TEST
660	ZDUDD0.BIC	DU11 OFF LINE TRANSMITTER TEST
661	ZDUED0.BIC	DU11 OFF LINE TIMING AND INTERR. TEST
662	ZDUFD0.BIC	DU11 OFF LINE MULTI DU11 EXERCISER
663	ZDUOB0.BIN	DU11 OVERLAY FOR INTERPROC. TEST
664	ZDUQC1.BIN	DUV11 OFF LINE LOGIC TEST
665	ZDURB1.BIC	DUV11 OFF LINE RECEIVER TEST
666	ZDUSB1.BIC	DUV11 OFF LINE RECEIVER TIMING TESTS
667	ZDUTB1.BIC	DUV11 OFF LINE TRANSMITTER TESTS
668	ZDUUB1.BIC	DUV11 OFF LINE TIMING & INTERR.TEST
669	ZDUVB1.BIC	DUV11 OFF LINE MULTIPLE DUV11 EXER.
670	ZDVAC0.BIC	DV11 BASIC REGISTER R/W TEST
671	ZDVBC0.BIC	DV11 STATIC LINE CARDS TEST
672	ZDVCD0.BIC	DV11 ROM TEST PART 1
673	ZDVDD1.BIC	DV11 ROM TEST PART 2
674	ZDVEC1.BIC	DV11 MODEM CONTROL AND CABLE TEST
675	ZDVFA0.BIC	DV11 ASYNCHRONOUS LINE CARDS TEST
676	ZDVOB0.BIC	DV11 OVERLAY FOR INTERPROC. TEST
677	ZDVZA0.BIN	DV11 16 LINE SYNCHR. MULTI TEST
678	ZDXAD3.BIC	DX11-B (DEC-IBM INTERF.) TEST 1
679	ZDXDA0.BIN	DX11-B / 2848 DIAGNOSTIC
680	ZDXEA0.BIN	DX11 FRIEND
681	ZDXFD0.BIN	DX11-B (DEC-IBM INTERF.) TEST 2
682	ZDXGC0.BIN	DX11-B OFF LINE DIAGN. EXER.
683	ZDXHD0.BIC	DX11-B ONLINE MAINTEN. CABLE EXER.

684	ZDXIC0.BIC	DX11-B RESPONDER PROGRAM
685	ZDXJC0.BIC	DX11-B OFFLINE MEMORY ADDRESSING TEST
686	ZDXKA0.BIN	DX11-B ON LINE OS EXER.
687	ZDZAI0.BIN	*DZ11 ASYNC. LINE MUX TEST
688	ZDZBC0.BIN	DZ11 OVERLAY FOR INTERPROC. TEST
689	ZDZCB0.BIN	VT62 / DZ11 DIAGNOSTIC TEST
690	ZDZGA0.BIN	GS03 / DZ11 LOGIC TEST
691	ZDZHA0.BIN	DZM11 FUNCTIONAL TEST
692	ZFLAC0.BIN	FLOATING ADDRESS/VECTOR UTILITY
693	ZFPAA0.BIC	VAX FRONT END PROC. BRIDGE LOG.TEST
694	ZFPBA0.BIC	VAX FRONT END PROC. BRIDGE LINK TEST
695	ZFPCA0.BIC	I/O PAGE ADDRESS FINDER
696	ZFPDA0.BIC	PROM CHECKSUM CALCULATOR/CHECKER
697	ZGSAA0.BIN	GS03-WD LINE SWITCH CONTROLED BY DZQ11
698	ZGSBA0.BIN	GS03-WD LINE SWITCH CONTROLED BY DHV11
699	ZICAD0.BIN	ICS11 CONTROLLER TEST
700	ZIDVA0.BIN	IDV11-D (CSS) FIVE CHANNEL COUNTER TEST
701	ZIEAC0.BIN	IEU/IEQ11 (CSS) FUNCTIONAL TEST
702	ZIEBA0.BIN	IEC11-A (CSS) IEC-BUS CONTR. TEST
703	ZIECA0.BIN	IEC11-B WITH IEC11-A (CSS) TEST
704	ZIRAA0.BIN	ICR11 (M8094,M8098,M8096) TEST
705	ZIRBA1.BIN	ICR11 (INDUSTR. CONTR. REMOTE) TEST
706	ZITAD0.BIN	INTERPROCESSOR TEST PROGRAM (ITEP)
707	ZIXVB0.BIN	IDV/IAV11 FUNCTIONAL TEST
708	ZKAQH0.BIC	PDP11 (11/35,40,45,34...)POWER FAIL TEST
709	ZKARB0.BIC	PDP11 TRAP TEST
710	ZKCAA0.BIC	*KMC11 MICRO-PROC.(M8204) TEST
711	ZKCCA1.BIC	*KMC11 MICRO-PROC. READ/WRITE TEST
712	ZKCDA0.BIC	*KMC11 MICRO-PROC. JUMP, CRAM TEST
713	ZKCEB0.BIC	KMC11 DDCMP LINE UNIT (M8201/8202) TEST
714	ZKCFB0.BIC	KMC11 BITSTUFF LINE UNIT R/W TEST
715	ZKCGA0.BIC	KMC11 MICRO-PROC. FREE RUNNING TEST
716	ZKCHA0.BIC	ISB11-A SERIAL BUS EXERCISER
717	ZKCIB0.BIN	RMT DIAGNOSTIC EXERCISER
718	ZKCTA0.BIN	KCT32 DIAGNOSTC
719	ZKDAA0.BIN	BB1-D DMA INTERFACE DIAGN.
720	ZKDJB2.BIC	*KDJ11-A BASIC INSTR. SET,EIS & TRAP TEST
721	ZKDKB0.BIC	*KDJ11-A MEMORY MANAGEMENT DIAGNOSTIC
722	ZKDLB0.BIC	*KDJ11-A FLOATING POINT DIAGN.
723	ZKDMB0.BIC	*KDJ11-A CACHE MEMORY DIAGNOSTIC
724	ZKEBB0.BIC	EAE11 LOGIC TEST
725	ZKECA0.BIN	EAE11 RANDOM EXERCISER
726	ZKEDA0.BIC	KE11-B DIAGNOSTC PACKAGE
727	ZKEEC0.BIC	*CIS (COMMERCIAL INSTR. SET) PROC. TEST
728	ZKGAB0.BIC	KG11-A CRC (CYCLIC REDUNDANCY CHECK) TEST
729	ZKHAB0.BIC	KIT11-H (UNIBUS INPUT/OUTP.) TEST

730	ZKLAE0.BIC	KL11 / DL11-A TELETYPE TEST
731	ZKMAF0.BIC	*PDP11 0-124K MOS OR CORE MEMORY TEST
732	ZKMBA0.BIN	*KMC11-B (M8206) STATIC TEST 1
733	ZKMCA0.BIN	*KMC11-B (M8206) STATIC TEST 2
734	ZKMDA0.BIN	KMC11-DMS11-DA LINE UNIT STAT. TEST
735	ZKMEA0.BIN	KMC11-DMS11-DA LINE UNIT DYNAM. TEST
736	ZKMFA0.BIN	KMS11-BD-DM11-BA (MODEM CONTR.) TEST
737	ZKMGA0.BIN	DM11-BA MODEM CONTROL TEST
738	ZKMOA0.BIN	KMC11 OVERLAY FOR INTERPROC. TEST
739	ZKMSA0.BIN	KMS11-BD/BE (DDCMP) DATA COM.LINK TEST
740	ZKMUA0.BIN	KMS11-BL/BM (DDCMP) DATA COM.LINK TEST
741	ZKMVA0.BIN	KMS11-K FUNCTIONAL (CPU & LU MOD) TEST
742	ZKTCA0.BIN	KXT11-CA SINGLE BOARD COMP. DIAG.
743	ZKUAE0.BIN	UNIBUS SYSTEM EXER (WITH M7855) DIAGN.
744	ZKUBC0.BIN	M7855 MODULE TEST PROGRAM
745	ZKVAB0.BIN	VT71 KEYBOARD DIAGNOSTIC
746	ZKVBB0.BIN	VT71 CONTROL & VIDEO TEST
747	ZKVCA0.BIN	VT71 TERMINAL DIAGNOSTIC
748	ZKWAG0.BIC	KW11-L LINE FREQUENCY CLOCK TEST
749	ZKWBJ1.BIC	*KW11-P PROGRAMABLE REAL TIME CLOCK TEST
750	ZKWCC2.BIN	KW11-W WATCH DOG TIMER TEST
751	ZKWKA2.BIC	KW11-K LOGIC TEST
752	ZKWLA0.BIN	KW11-C LOGIC TEST
753	ZKXAB0.BIN	*KXJ11-CA DIAGNOSTIC
754	ZKXCA0.BIN	KXJ11-CA DIAGNOSTIC (Q-BUS)
755	ZLABA1.BIC	LA30 TERMINAL TEST
756	ZLACF0.BIN	LA36 TERMINAL TEST ON DL11 OR KL11
757	ZLADD0.BIN	LA36 TERMINAL TEST ON DH11 OR DJ11
758	ZLAEB0.BIN	LA180 PRINTER DIAGNOSTIC
759	ZLAFA1.BIN	*LA36 (1-48 TERMINAL) ON DL11/DLV11
760	ZLAIB0.BIN	LA34/LA38 ON DZ11 FUNCTIONAL TEST
761	ZLCAC0.BIN	LC11/LA30 TERMINAL TEST
762	ZLCPA0.BIN	LCP01 (CSS) COLOR PRINTER DIAGNOSTIC
763	ZLDIA0.BIN	*DECSA (DEC ETHER. COM. SERV.) REPAIR T
764	ZLKAA0.BIN	LK11-A PUSH BUTTON MODULE TEST
765	ZLNAD0.BIN	*LN01 LASER PRINTER DIAGNOSTIC
766	ZLPAB1.BIN	*LP11/LP01 PRINTER DIAGNOSTIC
767	ZLPBB0.BIN	LPC11 INTERFACE DIAGNOSTIC TEST
768	ZLPCC0.BIC	LPS11 (LAB. PERIPHERAL SYS.) TEST 1
769	ZLPDC0.BIC	LPS11 (LAB. PERIPHERAL SYS.) TEST 2
770	ZLPIB0.BIC	LPS11 DRA OPTION I/O TEST
771	ZLPJB0.BIN	LPD11 INTERFACE DIAG. TEST
772	ZLPKH0.BIN	*LP05/LP11/LP14 LINE PRINTER TEST
773	ZLPLG0.BIN	*LP25/LP26/LP27/LP07 LINE PRINTER TEST
774	ZLQPB0.BIN	LQPSE-F ON DZ11,DL11-W,DLV11-F/J TEST
775	ZLSAB0.BIC	*LS11 CENTRONICS PRINTER TEST

776	ZLVAB0.BIC	LV11 PRINTER PLOTTER (LV01-AX/BX)TEST
777	ZLXAC0.BIN	LXY11/LXY21 OR LXV11 DIAGNOSTIC
778	ZM9AE0.BIC	M9301, M9400 BOOTSTRAP MODULE TEST
779	ZM9BE0.BIN	*M9312 / 11/44 UBI BOOT MODULE TEST
780	ZMDSA0.BIN	11MDS-A CUS TEST
781	ZMLAD0.BIN	ML11 SOLID STATE DISK LOGIC TEST
782	ZMLBB0.BIN	ML11 SOLID STATE DISK PERFORMANCE EXER
783	ZMLCB0.BIN	ML11 SOLID STATE DISK MAINT. PROGRAM
784	ZMMJA0.BIC	PDP11 MEMORY TEST 8K SPECIAL
785	ZMMLC0.BIC	*MF11S-K MEMORY DIAGNOSTIC
786	ZMRAA0.BIC	MIRA DUAL MICRO 11/83 OR 11/83 TEST
787	ZMSDD0.BIN	*MS11-L/M MEMORY DIAGNOSTIC
788	ZMSPC0.BIN	*MS11-L/M/P MOS MEMORY DIAGNOSTIC
789	ZNCAC1.BIC	NC11-A LOGIC (GAMMA CAMERA INTERF.) T
790	ZNCBC0.BIN	NC11-A GAMMA 11 EXERCISER
791	ZNCCC0.BIN	NCV11 LOGIC TEST
792	ZNCDB0.BIN	NCV11 PERFORMANCE EXERCISER
793	ZNIAA0.---	DEUNA RSX NI EXERCISER
794	ZNWAA0.BIN	NW11 MATCHDOG DIAGNOSTIC
795	ZPAAC0.BIN	TYP-11 RDR/PUNCH DIAGNOSTC
796	ZPABA0.BIN	MULTI READER/PUNCHER EXERCISER
797	ZPCAE0.BIN	PC11 READER PUNCHER TEST
798	ZPLAC0.BIN	PCL11 (PARALLEL COM. LINK) EXERCISER
799	ZPLBC0.BIN	PCL11 STAND ALONE TEST
800	ZPMAC0.BIN	PDM-70 DIAGNOSTIC TEST
801	ZPRBA0.BIN	PRS01 TOGGLE IN TEST PROGRAM
802	ZQBBA0.BIN	M9312 ROM BLASTER UTILITY
803	ZQKBH0.BIC	PDP11 4K SYSTEM EXERCISER (0-28KW) (old)
804	ZQKCF0.BIC	*PDP11 FAMILY INSTRUCTION EXERCISER
805	ZQMAB1.BIN	PDP11 MEMORY I/O EXERCISER
806	ZQMBH0.BIN	0-128K MEMORY EXERCISER (OLD)
807	ZQMCH0.BIC	*PDP11 MEMORY TEST (0-124KW)
808	ZQNAI0.BIN	*DEQNA (ETHERNET) FUNCTIONAL TEST
809	ZR6AD0.BIN	*RK611 DISKLESS CONTROLLER TEST 1
810	ZR6BD0.BIN	*RK611 DISKLESS CONTROLLER TEST 2
811	ZR6CE0.BIN	*RK611 DISKLESS CONTROLLER TEST 3
812	ZR6DD0.BIN	*RK611 DISKLESS CONTROLLER TEST 4
813	ZR6EC0.BIN	*RK611 DISKLESS CONTROLLER TEST 5
814	ZR6GC0.BIC	*RK611/RK06/07 DUAL PORT DIAGNOSTIC
815	ZR6HF0.BIC	*RK06/07 DISK DRIVE DIAGNOSTIC TEST 1
816	ZR6IF0.BIC	*RK06/07 DISK DRIVE DIAGNOSTIC TEST 2
817	ZR6JF0.BIN	*RK06/07 DISK DRIVE DIAGNOSTIC TEST 3
818	ZR6KG0.BIN	*RK611 FUNCTIONAL CONTROLLER TEST
819	ZR6LD0.BIN	*RK06/07 FORMATTER PROGRAM
820	ZR6ME1.BIC	*RK06/07 DYNAMIC TEST PART 1
821	ZR6NE3.BIC	*RK06/07 DYNAMIC TEST PART 2

822	ZR6PD0.BIN	*RK06/07 PERFORMANCE EXERCISER
823	ZR6QC0.BIN	*RK06/07 COMPATIBILITY TEST
824	ZR6RC1.BIN	*RK06/07 USER DEFINED TEST
825	ZRCAB0.BIC	RC11 (RS64) FIXED HEAD DISK STATIC TEST
826	ZRCBB0.BIC	RC11 (RS64) FIXED HEAD DISK DATA TEST
827	ZRCCB0.BIC	RC11 MULTI DISK EXERCISER
828	ZRCDB0.BIN	*RC25 DISK DRIVE FUNCTIONAL EXER
829	ZRCFC0.BIN	*RC25 DISK DRIVE BASIC FUNCTIONAL TEST
830	ZRCHB0.BIN	*RC25 DISK PACK FORMATTER
831	ZRFAB0.BIC	RF11 FIXED HEAD DISK STATIC TEST
832	ZRFBB1.BIC	RF11 FIXED HEAD DISK DATA TEST
833	ZRFCB0.BIC	RF11 FIXED HEAD DISK MULTI DISK TEST
834	ZRHBF0.BIC	RH11 MASSBUS I/O CONTROLLER TEST
835	ZRJAD0.BIC	*RP04/05/06 MECANICAL AND READ/WRITE TEST
836	ZRJBD0.BIC	*RP04/05/06 FORMATTER PROGRAM
837	ZRJCB0.BIC	*RP04/05/06 HEAD ALIGNMENT PROGRAM
838	ZRJDE0.BIC	*RP04/05/06 MULTI-DRIVE LOGIC TEST
839	ZRJED0.BIN	*RP04/05/06 DUAL-PORT LOGIC TEST PART 1
840	ZRJFA0.BIN	*RP04/05/06 DUAL-PORT LOGIC TEST PART 2
841	ZRJGE0.BIC	*RP04/05/06 DISKLESS TEST PART 1
842	ZRJHE0.BIC	*RP04/05/06 DISKLESS TEST PART 2
843	ZRJID0.BIC	*RP04/05/06 FUNCTIONAL CONTROLLER TEST 1
844	ZRJJD0.BIC	*RP04/05/06 FUNCTIONAL CONTROLLER TEST 2
845	ZRJKB0.BIC	*RP07 HDA FORMATTER / SCANER UTILITY
846	ZRJLB0.BIC	*RP07 FUNCTIONAL TEST
847	ZRJMB0.BIC	*RP07 FRONT-END (CONTROLLER) ISOLATOR TEST
848	ZRJNA0.BIC	*RP07 DUAL PORT TEST
849	ZRJOB0.BIC	*RP07 PERFORMANCE EXERCISER
850	ZRKHG0.BIC	*RK11/RK05-J/F PERFORMANCE EXERCISER
851	ZRKIF0.BIN	*RK11/RK05-J/F UTILITY PROGRAMS
852	ZRKJE0.BIC	*RK11/RK05-J/F BASIC LOGIC TEST 1
853	ZRKKF2.BIC	*RK11/RK05-J/F BASIC LOGIC TEST 2
854	ZRKLE0.BIC	*RK11/RK05-J/F DINAMIC TEST
855	ZRLGE0.BIC	*RL11/RLV11 CONTROLLER TEST 1
856	ZRLHB1.BIC	*RL11/RLV11 CONTROLLER TEST 2
857	ZRLID1.BIN	*RL01/02 DRIVE TEST 1
858	ZRLJC0.BIC	*RL01/02 DRIVE TEST 2 (SEEK TEST)
859	ZRLKB3.BIC	*RL01/02 PERFORMANCE EXERCISER
860	ZRLLC1.BIN	*RL01/02 COMPATIBILITY TEST PROGRAM
861	ZRLMB1.BIN	*RL01/02 BAD SECTOR FILE UTILITY
862	ZRLNC0.BIC	*RL01/02 DRIVE TEST 3 (SEEK/READ/WRITE TEST)
863	ZRMLB1.BIC	*RM02/03/05 DISK PACK FORMATTER
864	ZRMMB2.BIC	*RM02/03/05 SUBSYSTEM FUNCTIONAL TEST 1
865	ZRMNB1.BIC	*RM02/03/05 SUBSYSTEM FUNCTIONAL TEST 2
866	ZRMOB1.BIC	*RM02/03/05 SUBSYSTEM FUNCTIONAL TEST 3
867	ZRMPB3.BIC	*RM02/03/05 DISKLESS CONTR. DIAG. PART 1

868	ZRMQB1.BIC	*RM02/03/05 DISKLESS CONTR. DIAG. PART 2
869	ZRMRB0.BIN	*RM02/03/05 DUAL PORT TEST 1
870	ZRMSB0.BIN	*RM02/03/05 DUAL PORT TEST 2
871	ZRMTB0.BIN	*RM02/03/05 DRIVE COMPATIBILITY TEST
872	ZRMUB1.BIC	*RM02/03/05 PERFORMANCE EXERCISER
873	ZRMVB1.BIC	*RM02/03/05 EXTENDED DRIVE TEST
874	ZRNAA0.BIC	*RM80 PERFORMANCE EXERCISER
875	ZRNBA0.BIC	*RM80 DISKLESS TEST 1
876	ZRNCA0.BIC	*RM80 DISKLESS TEST 2
877	ZRNDA0.BIC	*RM80 FUNCTIONAL TEST 1
878	ZRNEA0.BIC	*RM80 FUNCTIONAL TEST 2
879	ZRNFA0.BIC	*RM80 FUNCTIONAL TEST 3
880	ZRNGA0.BIC	*RM80 FUNCTIONAL TEST 4
881	ZRNHA0.BIC	*RM80 DUAL PORT TEST 1
882	ZRNIA0.BIC	*RM80 DUAL PORT TEST 2
883	ZRNJB0.BIC	*RM80 HDA FORMATTER UTILITY
884	ZRP1C0.BIC	RP11-E/RP02/03 MULTI DRIVE EXER.
885	ZRP2B0.BIN	RP11-E/RP02/03 DISK PACK FORMATTER
886	ZRPAD1.BIN	RP11-C/RP03 DISKLESS DIAGNOSTIC
887	ZRPBE0.BIN	PR11-C/RP03 DATA RELIABILITY TEST
888	ZRPCD0.BIC	RP11-C/RP02/03 MULTI DRIVE DIAGN.
889	ZRPDB0.BIN	RP11-C/RP03 DISK PACK FORMATTER
890	ZRPEA0.BIN	RP11 /RP02 DISKLESS DIAGNOSTIC
891	ZRPFB0.BIC	RP11 /RP02 DATA RELIABILITY TEST
892	ZRPGB0.BIC	RP11 /RP02 MULTI DRIVE DIAGNOSTIC
893	ZRPHA0.BIN	RP11 /RP02 DISK PACK FORMATTER
894	ZRPWC0.BIC	RP11-E /RP02/03 DISKLESS LOGIC TEST
895	ZRPYD1.BIC	RP11-E /RP02/3 FUNCT. LOGIC R/W TEST
896	ZRPZC0.BIC	RP11-E /RP02/3 POSITIONING TEST
897	ZRQAH0.BIC	*RQDX1/2/3 /RX50 RUX50/RD51/52 EXER.
898	ZRQBC1.BIN	*RQDX1/2 /RD51/52 FORMATTER
899	ZRQCF0.BIC	*RQDX3/RD31/51/52/53/54/RX33 FORMATTER
900	ZRQDA0.BIN	*RQDX1/2/3 DUP EXERCISER
901	ZRQEB0.BIC	RQDX3 RD51/52/53/54, RX50, RX33 EXER.
902	ZRQFC0.BIC	*RQDX3 RX33 HIGH DENSITY FLOPPY FORMATTER
903	ZRQGA0.BIN	RQDX1/2/3 UTILITY, CONTROLLER/DRIVE INFO.
904	ZRSBH0.BIN	*RH11 RS03/04 BASIC FUNCTION DIAGNOSTIC
905	ZRSCG0.BIC	*RH11 RS03/04 DATA RELIABILITY TEST
906	ZRSDC0.BIN	*RH11 RS04 MAINTENANCE MODE DIAGNOSTIC
907	ZRSEC0.BIN	RH11 RS03 MAINTENANCE MODE DIAGNOSTIC
908	ZRTAC0.BIN	RT01/RT02 TERMINAL TEST
909	ZRXAF0.BIC	*RX11/RX01 SYSTEM RELIABILITY TEST
910	ZRXBF0.BIC	*RX11 INTERFACE (M7846) DIAGNOSTIC
911	ZRXCA0.BIN	RX11/RXV11/RXV211/RXV21 RX02 UTIL. DRIVER
912	ZRXDC0.BIC	*RX02 (up to 4 drives) SUBSYS. PERFORM. EXER.
913	ZRXEA2.BIC	*RX02 DISKETTE FORMATTER (sing./double chang.)

914	ZRXFB0.BIC	*RX02 FUNCTIONAL LOGIC TEST
915	ZTAAC0.BIN	*TA11 CASSETTE BASIC LOGIC TEST 1
916	ZTABC0.BIN	TA11 CASSETTE BASIC LOGIC TEST 2
917	ZTACC0.BIN	TA11 CASSETTE MANUAL INTERVENTION TEST
918	ZTADD0.BIN	TA11 CASSETTE MOTION TEST
919	ZTAEC0.BIC	TA11 CASSETTE DATA RELIABILITY TEST
920	ZTAFC0.BIN	TA11 CASSETTE ABSOLUTE LOADER
921	ZTAHA0.BIN	TA11 CASSETTE COPY PROGRAM
922	ZTCAA0.BIC	*TC11 BASIC LOGIC TEST 1
923	ZTCBE0.BIC	TC11 BASIC LOGIC TEST 2
924	ZTCCA0.BIC	TC11 BASIC LOGIC TEST 3
925	ZTCDC0.BIC	TC11 READ AND WRITE ALL
926	ZTCED0.BIC	TC11 DEC TAPE EXERCISER
927	ZTEAE0.BIN	*TM03-TE16/TU77 CONTROL LOGIC TEST 1
928	ZTEBC0.BIN	*TM03-TE16/TU77 CONTROL LOGIC TEST 2
929	ZTECF0.BIN	*TM03-TE16/TU77 BASIC FUNCTION TEST
930	ZTEDE0.BIN	*TM03-TE16/TU77 DATA RELIABILITY TEST
931	ZTEEE0.BIN	*TM03-TE16/TU77 DRIVE FUNCTION TIMER
932	ZTEFB0.BIN	TM02/03-TU16/TE16/TU77 UTILITY DRIVER
933	ZTKAE0.BIN	*TK50/TK70 FRONT END FUNCTION TEST
934	ZTKBC0.BIN	*TK50/TK70 DATA RELIABILITY TEST
935	ZTKEB0.BIC	*TK25 FRONT END FUNCTION TEST 1
936	ZTKFA0.BIC	*TK25 FRONT END FUNCTION TEST 2
937	ZTKGA0.BIC	*TK25 FRONT END FUNCTION TEST 3
938	ZTKHB0.BIN	*TK25 FRONT END FUNCTION TEST 4
939	ZTKIB0.BIN	*TK25 DATA RELIABILITY TEST
940	ZTMAI0.BIC	*TM11/TMA11/TMB11 TS03/TU10 BASIC TEST
941	ZTMBG0.BIN	*TM11/TU10 DATA RELIABILITY TEST 9TRK
942	ZTMCD0.BIC	*TM11/TU10 DATA RELIABILITY TEST 7TRK
943	ZTMDE0.BIN	*TM11/TU10 DRIVE FUNCTION TIMER
944	ZTMEE0.BIC	*TMA11/TMB11/TU10 DRIVE FUNCTION TIMER
945	ZTMFF1.BIC	*TMA11/TMB11/TU10 SUPPLEMENT INSTR. TEST
946	ZTMGC0.BIN	TMA11/TMB11/TU10 UTILITY DRIVER
947	ZTMHF1.BIC	*TM11/TMA11/TMB11/TS03/TU10 MULTIDR. DATA
948	ZTMIC0.BIN	TM78 CONTROLER/LOGIC TEST
949	ZTRAC0.BIC	TR79F TAPE DIAGNOSTIC
950	ZTRBD0.BIC	TR79F UTILITY PROGRAM
951	ZTSAA0.BIC	*TSU05 DIAGNOSTIC PART 1
952	ZTSBA0.BIC	*TSU05 DIAGNOSTIC PART 2
953	ZTSCA0.BIC	*TSU05 DIAGNOSTIC PART 3
954	ZTSDA0.BIC	*TSU05 DIAGNOSTIC PART 4
955	ZTSEB0.BIC	*TS03 DRIVE FUNCTION TIMER
956	ZTSFD0.BIC	*TS03 SUPPLEMENTAL TEST
957	ZTSGB0.BIN	TS03 UTILITY DRIVER
958	ZTSHD0.BIN	*TS11/TS04 DATA RELIABILITY TEST
959	ZTSIC0.BIN	*TS11/TS04 CONTROL LOGIC TEST

960	ZTU1A0.BIN	*TU81 DATA RELIABILITY TEST
961	ZTU2D0.BIN	*TU81 FRONT END FUNCTION TEST
962	ZTUAJ0.BIN	*TM02/TU16/TE16/ RELIABILITY TEST
963	ZTUBH0.BIN	*TM02/TU16/TE16/TU77 BASIC FUNCTION TEST
964	ZTUCG0.BIN	*TM02/TU16 CONTROL LOGIC TEST
965	ZTUDD0.BIN	*TM02/TU16 DRIVE FUNCTION TIMER TEST
966	ZTUED0.BIN	TM02/TU16 UTILITY DRIVER
967	ZTUFA0.BIN	DATA ON PAPER TAPE CREATE PROGRAM
968	ZTUGC1.BIC	*TM02/TE16 DRIVE FUNCTION TIMER
969	ZTUIA0.BIN	*TM02/TU45 DATA RELIABILITY TEST
970	ZTUJA0.BIN	*TM02/TU45 BASIC FUNCTION TEST
971	ZTUKA0.BIN	*TM02/TU45 CONTROL LOGIC TEST
972	ZTULA0.BIN	*TM02/TU45 DRIVE FUNCTION TIMER TEST
973	ZTUMA0.BIN	TM02/TU45 UTILITY DRIVER
974	ZTUNA0.BIN	TM02/TU45 DATA TP CRT
975	ZTUOB0.BIC	*TM03/TU45 CONTROL LOGIC TEST PART 1
976	ZTUPB0.BIC	*TM03/TU45 CONTROL LOGIC TEST PART 2
977	ZTUQB0.BIC	*TM03/TU45 BASIC FUNCTION TEST
978	ZTURB0.BIC	*TM03/TU45 DATA RELIABILITY TEST
979	ZTUSB0.BIN	*TM03/TU45 DRIVE FUNCTION TIMER TEST
980	ZTUTA0.BIN	TM03/TU45 UTILITY DRIVER
981	ZTUUF0.BIN	*TU58 PERFORMANCE EXERCISER
982	ZTUVB0.BIN	*TU80 DATA RELIABILITY TEST
983	ZTUWA0.BIC	*TU80 FRONT END DIAGNOSTIC PART 1
984	ZTUXA0.BIC	*TU80 FRONT END DIAGNOSTIC PART 2
985	ZTUYA0.BIC	*TU80 FRONT END DIAGNOSTIC PART 3
986	ZTUZA0.BIC	*TU80 FRONT END DIAGNOSTIC PART 4
987	ZUAAB0.BIN	*DEUNA (M7792/M7793) REPAIR LEVEL DIAGN.
988	ZUABC0.BIC	*DEUNA (M7792/M7793) FUNCTIONAL DIAGN.
989	ZUACD0.BIN	*DEUNA (M7792/M7793) NI EXERCISER
990	ZUADB1.BIC	*DELUA FUNCTIONAL DIAGNOSTIC
991	ZUDAD0.BIN	UDC11 SYSTEM FUNCTIONAL EXERCISER
992	ZUDBB0.BIC	UDC11 CONTROL TEST
993	ZUDHA1.BIC	*UDA50/KDA50/RAxx BASIC SUBSYSTEM DIAGN.
994	ZUDIA0.BIC	*UDA50/KDA50/RAxx DISK EXERCISER
995	ZUDJC0.BIC	*UDA50/KDA50/RAxx SUBSYSTEM EXERCISER
996	ZUDKC0.BIN	*UDA50/KDA50/RAxx FORMATTER
997	ZUDLA0.BIN	*UDA50/KDA50/RAxx HDA (BAD BLOCKS) SCRUBBER
998	ZUDMA0.BIN	UDA/KDA ERROR LOG UTILITY
999	ZUF1E0.BIN	MICRO-11 USER TEST #1
1000	ZUF2E0.BIN	MICRO-11 USER TEST #2
1001	ZUF3A0.BIN	MICRO-11 USER TEST #3
1002	ZUF4A0.BIN	MICRO-11 USER TEST #4
1003	ZURCD0.BIN	MICRO-11 RC25 USER TEST
1004	ZUTKE0.BIN	MICRO-11 TK25 USER TEST
1005	ZVSAB0.BIC	VS60 INSTRUCTION TEST PART 1

1006	ZVSBB0.BIC	VS60 INSTRUCTION TEST PART 2
1007	ZVSCC0.BIC	VS60 INSTRUCTION TEST PART 3
1008	ZVSDC0.BIC	VS60 VISUAL DISPLAY TEST
1009	ZVSEA0.BIC	VSV01 DIAGNOSTIC TEST
1010	ZVSFA0.BIC	VS60 VISUAL WITH X-Y PONT CORRELATION
1011	ZVSVA0.BIN	VSV11/VS11 COLOUR LOOKUP OPTION TEST
1012	ZVSWB0.BIN	VSV21 DIAGNOSTC TEST
1013	ZVTAA0.BIC	VT36 DIAGNOSTIC PART 2
1014	ZVTBD0.BIC	VT05 TERMINAL DISPLAY TEST
1015	ZVTCF0.BIN	VT50A,B,H/52 TERMINAL ACCEPTANCE TEST
1016	ZVTDB1.BIC	VT55 ACCEPTANCE TEST
1017	ZVTEB0.BIN	VT20 HOST COMPUTER PROGRAM
1018	ZVTGA0.BIN	DH11/VT20 HOST COMPUTER PROGRAM
1019	ZVTHC0.BIC	DL11 / VT61 EXERCISER
1020	ZVTJB0.BIN	DJ11/VT61 EXERCISER
1021	ZVTKA0.BIN	VT INPUT LINE LOOPBACK PROGRAM
1022	ZVTLA0.BIN	VT61-T/V71-T MULTI LINE LOOP TEST
1023	ZVTMA0.BIN	VT61 ACCEPTANCE TEST
1024	ZVTNA0.BIC	VT105 ACCEPTANCE TEST
1025	ZVTOA0.BIC	M7142 CRT CONTROL LOGIC, ASCII ACCEPT. TEST
1026	ZVTVA0.BIN	VTV31-K VIDEO INTERFACE DIAGNOSTIC (CSS)
1027	ZVTZA0.BIN	VT36 DIAGNOSTIC PART 3

* = OPERATING DESCRIPTION IN THIS BOOK