Professional™ 300 series

Technical Manual

digital

Professional™ 300 series

Technical Manual

digital

1st Edition, December 1982

Printed in U.S.A.

CONTENTS

CHAPTER 6 LK201 KEYBOARD DESCRIPTION

CHAPTER 10 RX50 DUAL DISKETTE DRIVE

CHAPTER 11 RD50 HARD DISK CONTROLLER MODULE

CHAPTER 12 RD50 HARD DISK DRIVE

CHAPTER 13 POWER SUPPLY

FIGURES

TABLES

INTRODUCTION

This manual documents hardware functions for the Professional 350 computer. Any discussions about operation and/or programming are summarized. This manual provides the following objectives.

- Documents system concepts and design information for field engineers and personnel trained by Digital Equipment Corporation.
- Provides Field Service with the technical information needed to repair systems effectively and cost-efficiently.
- Provides information that is not duplicated in any other hardware manual.

MANUAL ORGANIZATION

The first four chapters provide an introduction to the Professional 350 system. They describe the system concepts and are necessary to understand before proceeding with the rest of the manual. The following is a brief description of Chapters 1-4.

- **Chapter 1 – System Introduction** – provides a brief introduction to the Professional 350 system.
- **Chapter 2 – System Installation** – provides the information needed to prepare the site and install the Professional 350. Information on cleaning the equipment and handling diskettes is also included.
- **Chapter 3 – Controls and Indicators** – describes all controls and indicators and their functions.
- **Chapter 4 – System Overview** – describes how each system component interacts.

Chapters 5-13 make up the rest of the manual. Each of these chapters describes a system component and the following is a brief description of Chapters 5-13.

- **Chapter 5 – System Microprocessor and Memory** – describes the system module and support devices. This chapter contains functional and detailed descriptions of each circuit, programming information for system module devices, and descriptions of the Octal Debugging Technique (ODT) commands.
- **Chapter 6 – Keyboard** – provides a functional and detailed description of the keyboard and its circuitry.
- **Chapter 7 – Bit Map Video Controller/Extended Bit Map Modules** – provides a functional and detailed description of the bit map video controller module and the extended bit map module. Programming information is provided for the bit map video controller.

- **Chapter 8 – Video Monitor** – provides functional and detailed descriptions of the monochrome monitor.

- **Chapter 9 – RX50 Controller Module** – provides functional and detailed descriptions of each circuit of the RX50 controller. Programming information is also supplied.

- **Chapter 10 – RX50 Dual Diskette Drive** – discusses the operation of the RX50 dual diskette drive. A functional and detailed description of each circuit is provided.

- **Chapter 11 – RD50 Hard Disk Controller Module** – describes the RD50 hard disk controller module. A functional and detailed description of each circuit is provided. Programming information is also provided in this chapter.

- **Chapter 12 – RD50 Hard Disk Drive** – discusses the operation of the RD50 hard disk drive. A detailed description of each drive and read/write (R/W) module circuit is provided. Removal/replacement procedures for the R/W module are also provided.

- **Chapter 13 – System Unit Power Supply** – provides functional and detailed descriptions of the power supply.

RELATED DOCUMENTATION

The following is a list of related documents for the Professional 350.

Professional 350 Pocket Service Guide – EK-PC350-PS

Professional 350 Illustrated Parts Breakdown – EK-PC350-IP

Professional 300 Series Owner Manual – AA-N587A-TH

Professional 350 Installation Guide – AZ-N626A-TH

Professional 350 User Guide for Hard Disk System – AA-N603A-TH

Professional 350 Field Maintenance Print Set – MP-01394-00

VR201 Field Maintenance Print Set – MP-01410-00

LK201 Field Maintenance Print Set – MP-01395-00

KEF11 Field Maintenance Print Set – MP-01473-00

CHAPTER 1
SYSTEM INTRODUCTION

1.1 SYSTEM DESCRIPTION

The following Paragraphs provide a physical description of the Professional 350 system. The Professional 350 consists of the following three hardware assemblies (Figure 1-1).

- System Unit
- Video Monitor
- Keyboard

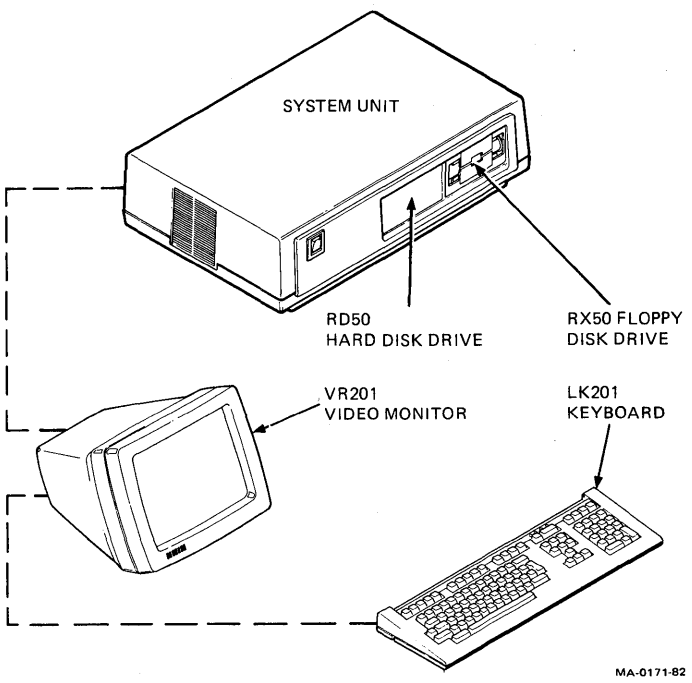


Figure 1-1 The Professional 350 Computer System

1.1.1 System Unit

The system unit contains the following components.

- **System Module** – The system module is central to the entire computer system. It is a printed circuit board mounted on a metal plate that slides in and out of the bottom of the Professional 350 enclosure. The system module contains all the control and interface electronics needed to support the F-11 microprocessor chip set, which is mounted on the system module.

- **RD50 Hard Disk Drive** – The system unit contains the RD50 hard disk drive. It is a winchester-based hard disk drive that provides 5 megabytes of formatted storage.

- **RX50 Dual Diskette Drive** – The system unit also contains the RX50 dual diskette drive. This is a dual diskette storage unit that provides 819 kilobytes of formatted storage on removable diskettes.

1.1.2 Video Monitor

The video monitor provides the system display. It is a 12 inch diagonal monochrome monitor. The video monitor has an adjustable tilt for operator viewing comfort and has two display controls on the monitor rear panel to adjust brightness and contrast.

1.1.3 Keyboard

The operator uses the keyboard to enter data into the system. The keyboard contains three keypads (main, editing, and numeric) and a series of special function keys.

1.2 SYSTEM SPECIFICATIONS

The general system specifications for the Professional 350 are listed below. Additional specifications for each component or module are supplied in the appropriate chapters.

SYSTEM UNIT

Functional

Microprocessor	Digital F-11 chip set (CPU)
Diagnostics	Built-in power-up self-test
Memory	Capable of addressing up to 3 megabytes
Video output	RS170-compatible, monochrome, bit map graphics
Communications port	RS423 asynchronous/byte, up to 19.2 Kilobaud with modem control
Printer port	Serial, RS423
Removable storage	Dual diskette drive, 5.25 in (13.3 cm) diskettes, 819 kilobytes total
Fixed storage (optional)	5 megabytes, 5.25 in (13.3 cm) hard disk drive
System expansion	4 option slots, user installable

Power

Power supply type	Transistor, switch type ac to dc converter
Vac input	Switch selectable
115 V nominal	Single-phase, 3-wire 90 to 128 V rms, 47 to 63 Hz line frequency
230 V nominal	Single-phase, 3-wire, 174 to 256 V rms, 47 to 63 Hz line frequency
Line current	6A @ 115 Vac 4A @ 230 Vac
Power consumption	320 watts maximum
Circuit protection	Circuit breaker, externally accessible

Physical

Height	16.5 cm (6.5 in)
Length	55.8 cm (22 in)
Width	34.3 cm (14.3 in)
Maximum Weight	15.9 kg (35 lb)

KEYBOARD

Functional

Electronics	8-bit microprocessor, 4 kilobytes of ROM, 256 bytes of RAM, 4 Indicators, transducer
Diagnostics	Power-up self-test

Keypads

Main keypad	57 keys
Numeric keypad	18 keys
Special function keys	20 keys
Editing keypad	10 keys

Physical

Height	5 cm (2.0 in) at highest point
Length	53.3 cm (21 in)
Width	17.1 cm (6.75 in)
Weight	2 Kg (4.5 lb)
Home row key height	30 mm above desktop

MONOCHROME MONITOR

Functional

Character format	24 lines × 80/132 characters per line software driven
Video format	Monochrome composite

Physical

Height	24.38 cm (9.75 in)
Width	29.33 cm (11.73 in)
Depth	30.57 cm (12.23 in)
Diagonal	305 cm (12 in) diagonally measured CRT
Weight	6.6 kg (14.5 lb)
Adjustable tilt	+5 to −25 degrees

RX50 DUAL DISKETTE DRIVE SUBSYSTEM

Performance

Formatted capacity	819 kilobytes
Diskettes per drive	2
Transfer rate	250 kilobits/sec
Average access time	290 msec

Functional

Density	96 tracks per inch

Physical

Height	8.4 cm (3.25 in)
Width	14.7 cm (5.75 in)
Depth	21.6 cm (8.5 in)
Weight	2.17 kg (4.8 lb)

RD50 HARD DISK DRIVE SUBSYSTEM

Performance

Formatted capacity	5 megabytes
Transfer rate	5 megabits/sec
Average access time	170 msec

Functional	
Density	255 tracks per inch
Physical	
Height	8.6 cm (3.2 in)
Width	14.9 cm (5.75 in)
Depth	20.3 cm (8 in)
Weight	2.3 kg (5 lb)

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION
The Professional 350 is a customer-installable system. Chapter 2 contains the following information.

- Site preparation
- Installation
- System upkeep

2.2 SITE PREPARATION
Before installing the computer system check the spacing, lighting, power, and environmental requirements.

2.2.1 Space
When positioning the Professional 350 use the following guidelines.

- Allow six inches on all sides of the computer for adequate airflow.
- Keep all ventilation ports clear.
- Allow room for the placement of peripheral devices.
- Place all cables away from traffic areas.

2.2.2 Lighting
Place the system unit and the video monitor away from direct sunlight. This minimizes heat build-up and glare.

2.2.3 Power
The following are the power requirements for the Professional 350.

- Input voltage – 115 or 230 Vac
- Line frequency – 47 to 63 Hz
- Power consumption – 320 watts maximum

2.2.4 Environment
The following are environmental requirements for the Professional 350.

- Temperature – 10° to 40° C (50° to 104° F)
- Humidity – 20% to 80% relative humidity
- Maximum wet bulb of 25° C
  Minimum dew point of 2° C

2.3 SYSTEM INSTALLATION

This section describes how to install the Professional 350 system and its options.

NOTE

The following procedures summarize the instructions in the Professional 350 Installation Guide (AZ-N626A-TH). Refer to the Installation Guide for complete installation procedures and illustrations.

2.3.1 Packaging

The Professional 350 system is shipped in four containers. Each container contains one of the following elements.

- System unit
- Software – including the Professional 350 Installation Guide
- Video monitor – including monitor cable
- Keyboard – including keyoard cable

2.3.2 Installing the Professional 350

The following procedure describes how to install the Professional 350.

1. Unpack the system and place each component on the work area surface.
2. Connect the video monitor cable to the back of the system unit (Figure 2-1) and to the back of the video monitor (Figure 2-2).
3. Connect the keyboard to the back of the monitor (Figure 2-2).
4. Set the voltage select switch on the back of the system unit to the correct operating voltage (115 or 230/240 Vac).
5. Remove the shipping card from the diskette drive. To do this open the door and slide the card out.
6. Make sure that the system unit power switch is set to the OFF position ("0"). Connect the power cord to the system unit and plug it into the nearest wall outlet.

2.3.3 Additional Equipment

The following are the options/modules for the Professional 350.

- Printed circuit board (PCB) modules
- Mass storage options
- Floating point adapter

2.3.3.1 Top Cover Removal – The following procedure describes how to remove the top cover.

1. Set the system unit power switch to OFF ("0").
2. Unplug the power cord and disconnect all cables from the rear of the system unit.
3. Slide the top cover release tabs forward and out and lift the cover straight up (Figure 2-3).

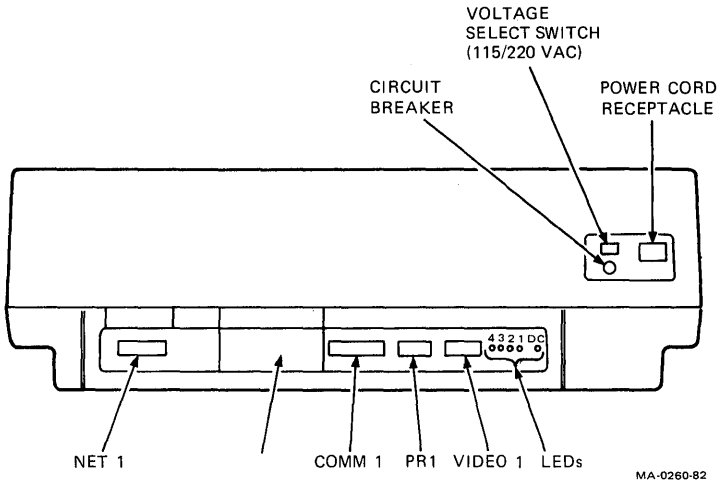


Figure 2-1 System Unit Rear Panel

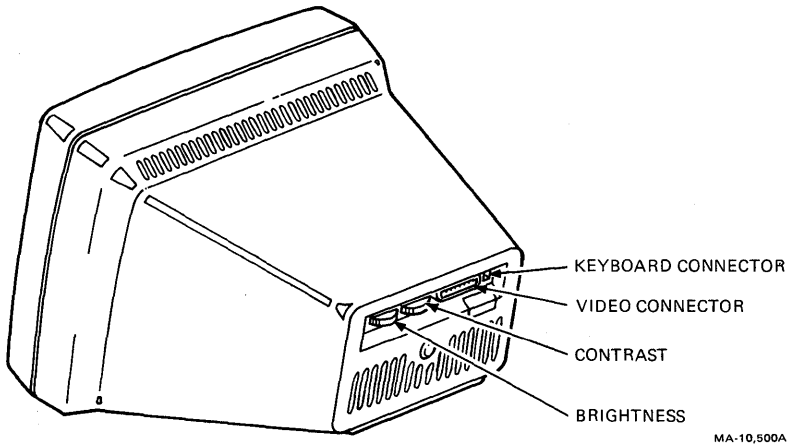


Figure 2-2 Monitor Rear Panel

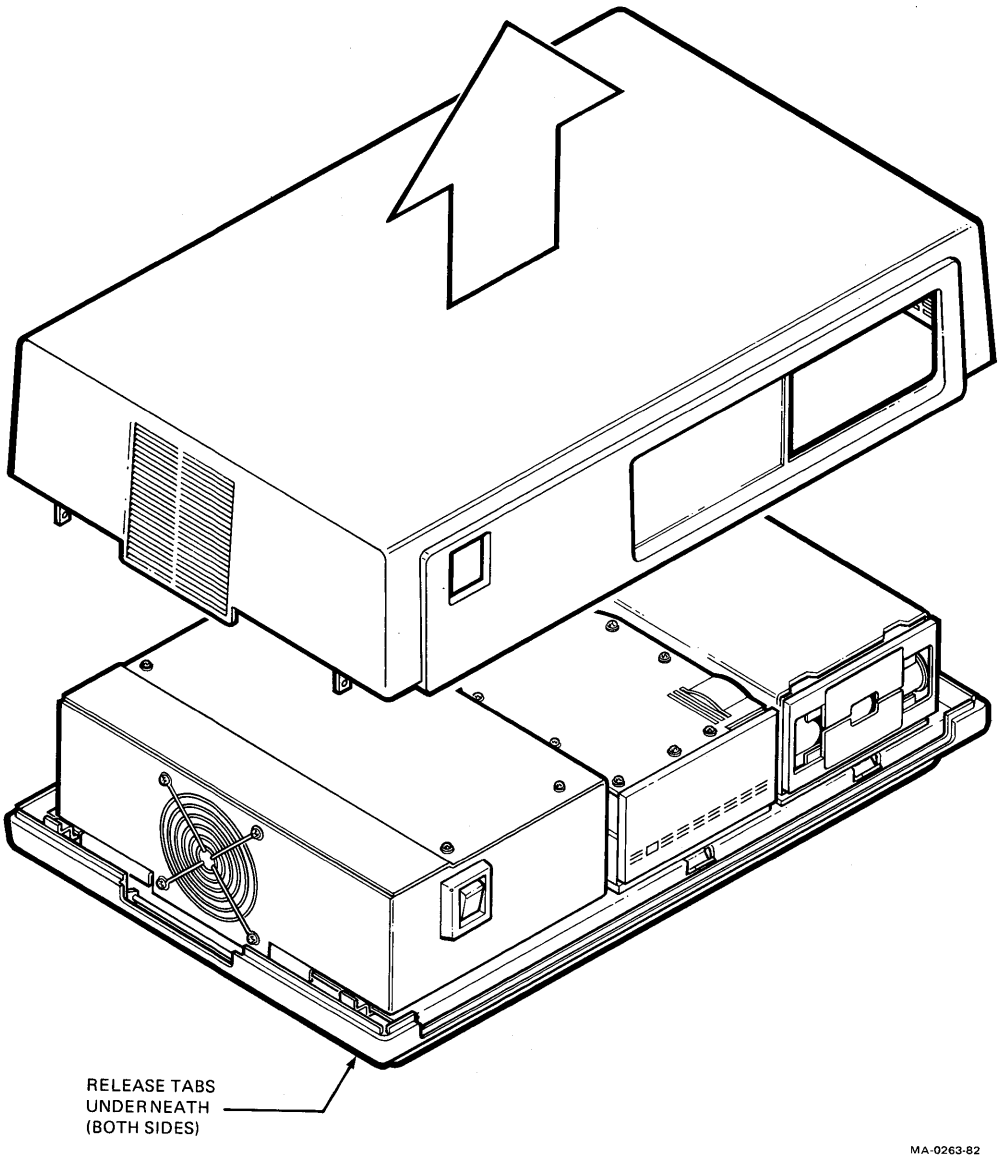


Figure 2-3 Top Cover Removal

2.3.3.2 Printed Circuit Board (PCB) Module Installation – The following describes how to install PCB modules in the system unit card cage.

1. Remove the top cover (Section 2.3.3.1).

2. Remove the screw securing the card cage door in place and open the card cage door (Figure 2-4).

3. Hold the module by the zero insertion force (ZIF) connector and pull the handle out turning it 90° clockwise.

4. Slide the module into the slot in the card cage. Turn the handle straight up and push it in toward the module.

5. If there are any cables to be connected to the PCBs, remove the cable cover screws and then remove the cable cover.

NOTE

Install the extended bit map module into the slot next to the bit map video controller module. Connect the flat cable provided to the extended bit map module and the bit map video controller module as shown in Figure 2-5. Cable restrictions require that the RD50 hard disk drive controller be in slot 1.

6. Close the card cage door. Replace the cable cover if it was removed. Replace the top cover and reconnect all cables to the rear of the system unit.

7. Reconnect the system unit power cord to the nearest wall outlet after the last module is installed.

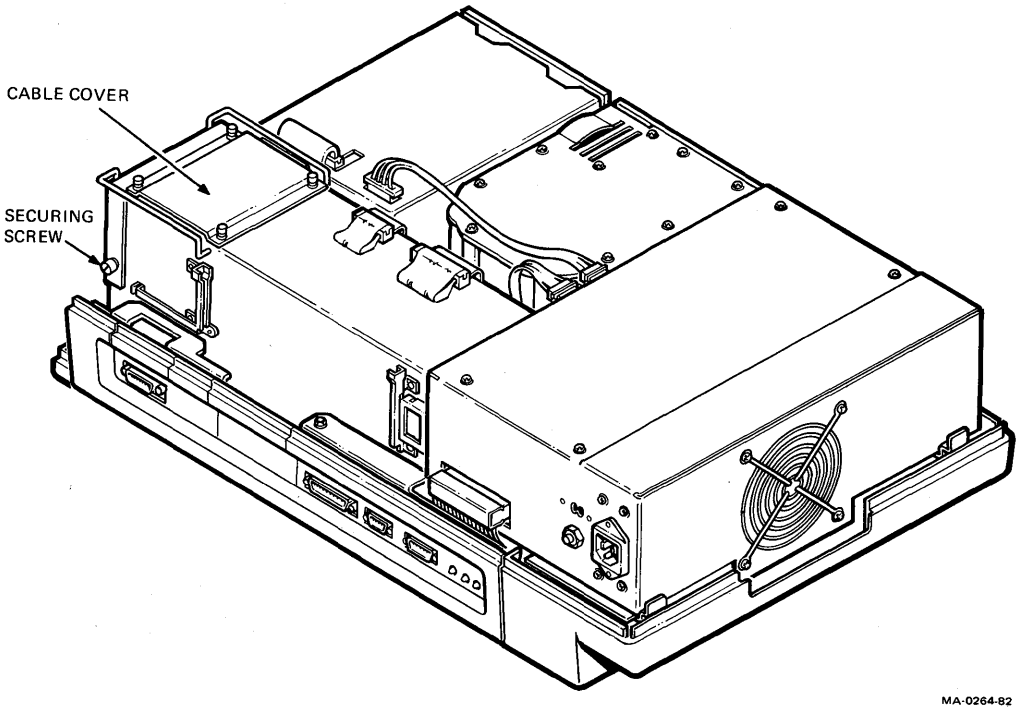


Figure 2-4 Card Cage Door Securing Screw

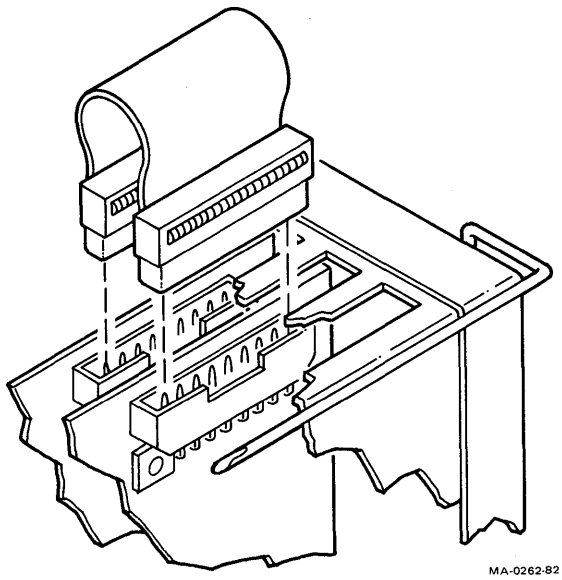


Figure 2-5 Bit Map Video Controller to Extended Bit Map Module Connector

2.3.3.3 RD50 Mass Storage Device Installation – The RD50 hard disk drive is the only mass storage device available as an option. Perform the following procedure to install the RD50 device option in the Professional 350.

1. Remove the top cover.
2. Remove the screw securing the card cage door in place and open the card cage door (Figure 2-4).
3. Install the RD50 hard drive controller into the card cage.

NOTE
Cable restrictions require that the RD50 hard disk drive controller be in slot 1.

4. Connect the signal cables and the power cable to the RD50 hard disk drive (Figure 2-6).
5. Slide the RD50 into the system unit until it clicks into place (Figure 2-6).

CAUTION
Use extreme caution when installing the RD50 hard disk drive. Sudden physical shocks to the RD50 (such as dropping it onto a hard surface) will destroy the drive.

6. Connect the drive cables to the RD50 hard drive controller and the power supply (Figure 2-6).
7. Replace the top cover.
8. Reconnect all cables to the rear of the system unit and plug the power cord into the nearest wall outlet.

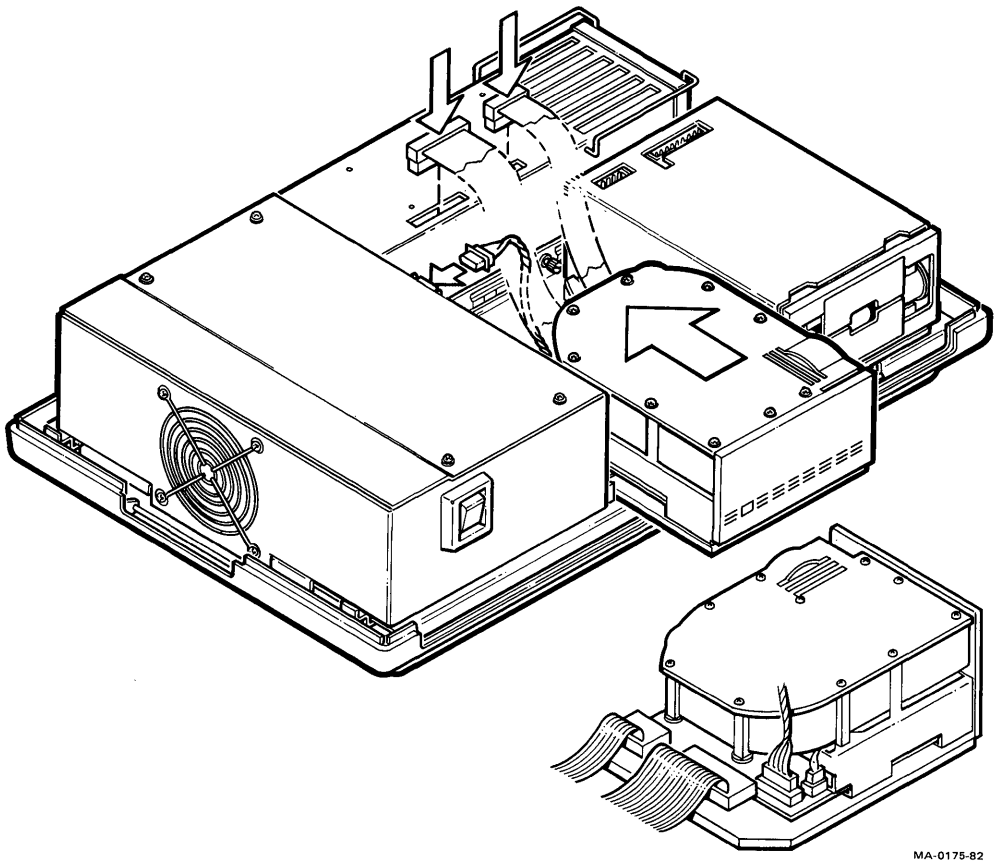


Figure 2-6 RD50 Hard Disk Drive Installation

2.3.3.4 Floating Point Adapter – The following describes how to install the floating point adapter.

CAUTION
The floating point adapter (FPA) is a static-sensitive device. Do not remove the FPA from its container until you are ready to install it or damage can result.

1. Remove the top cover.
2. Disconnect all cables from the card cage, power supply, and the rear of the system unit (Figure 2-7).
3. Using a ball point pen, or other long thin tool, press down on the two drive release snaps and slide both disk drives half way out of the system unit (Figure 2-8).
4. Release the three captive thumb screws at the bottom of the card cage (Figure 2-9).

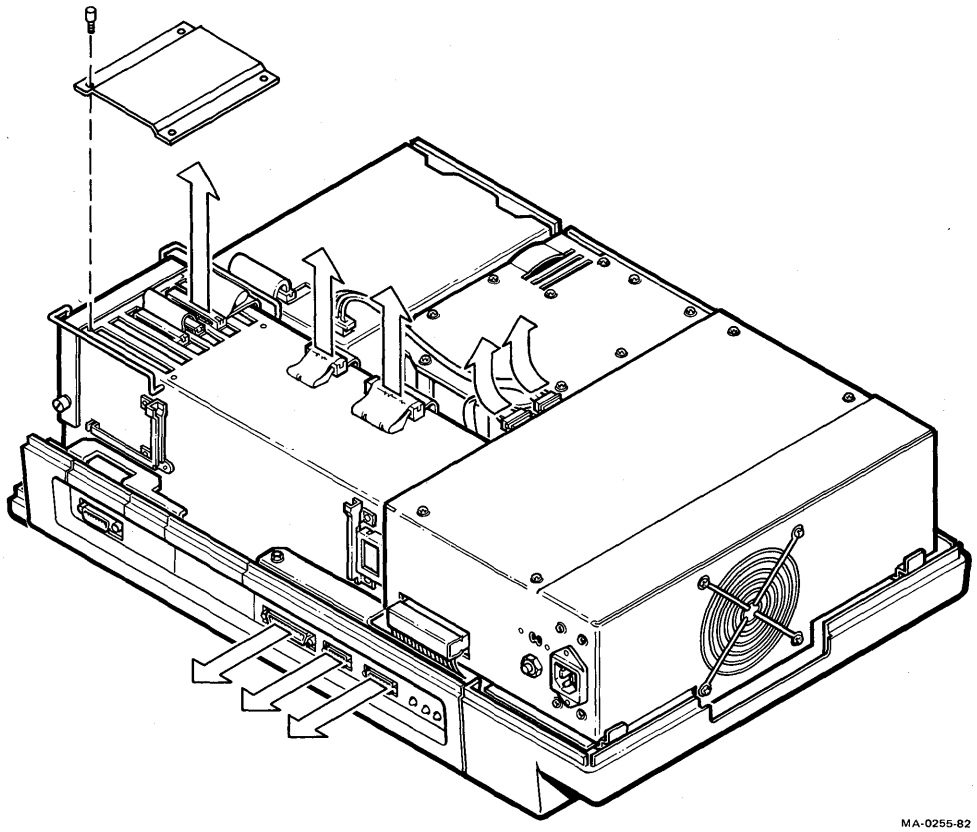


Figure 2-7 Removing the Cables

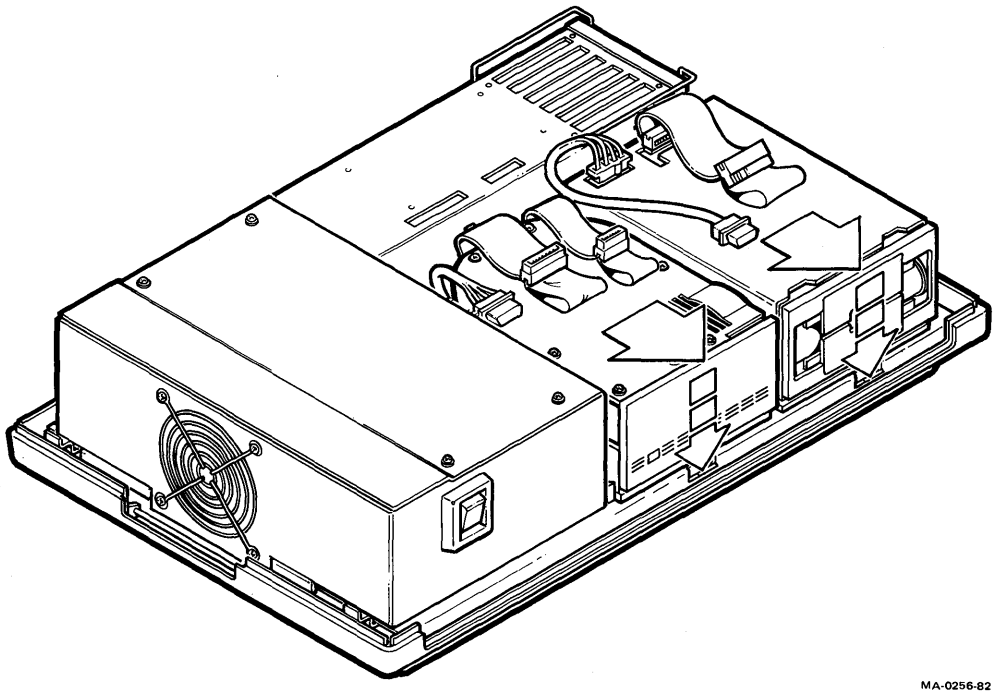


Figure 2-8 Slide Out Drives

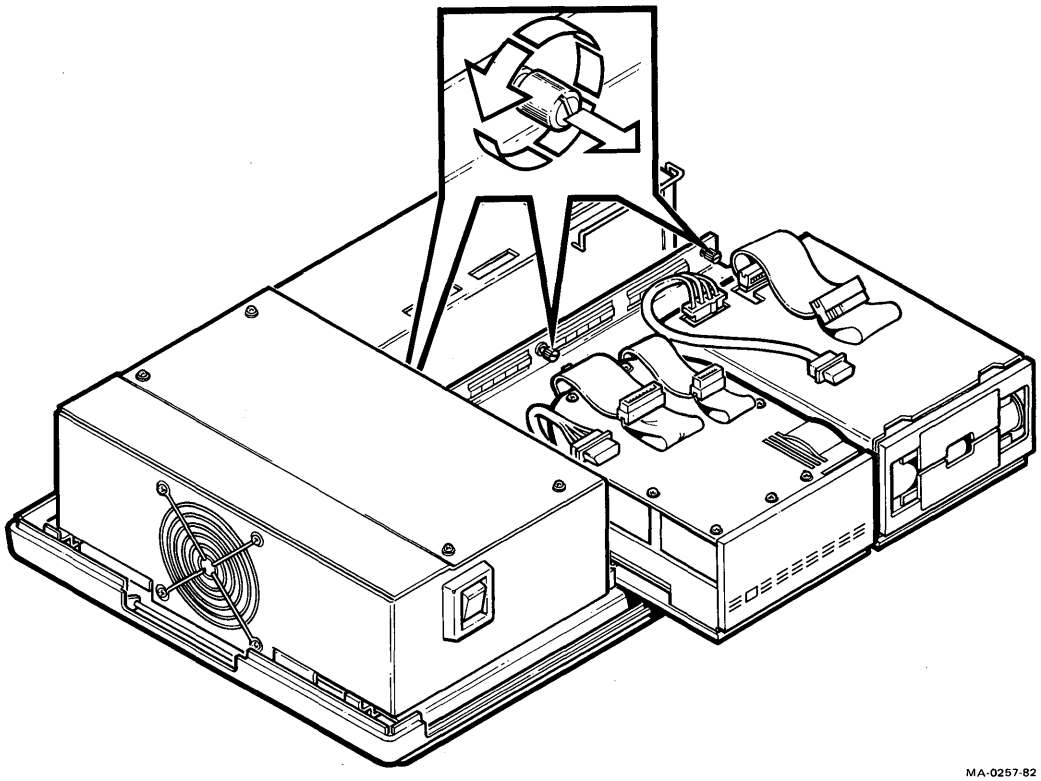


Figure 2-9 Release Thumb Screws

5. Disconnect the power cable from the system module and slide the system module out of the system unit (Figure 2-10).

6. Remove the cap from the floating point adapter socket (Figure 2-11).

7. Using the plastic ends on both sides, lift the floating point adapter from its shipping container.

8. Place the FPA in the socket. Make sure that the two-hole tab faces toward the power supply (Figure 2-11).

9. Secure the FPA by pressing down on each tab (Figure 2-11). When secured, the black FPA cover comes off leaving the FPA in its socket. Save the FPA cover.

10. Slide the system module back onto the system unit and secure it with the three captive screws.

11. Slide both disk drives back into the system unit until they both click into place.

12. Reconnect all cables to the card cage, system module, power supply, and the rear of the system unit.

13. Replace the top cover.

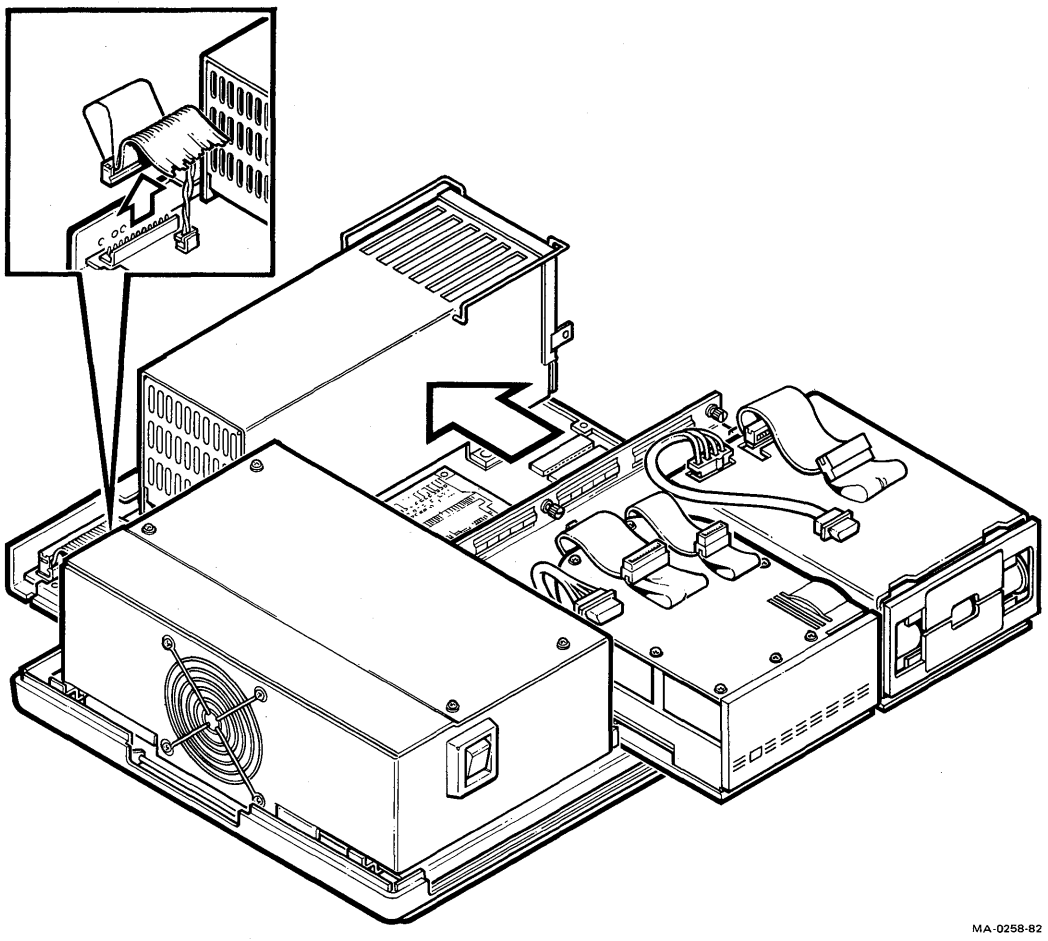


Figure 2-10 Removing the System Module

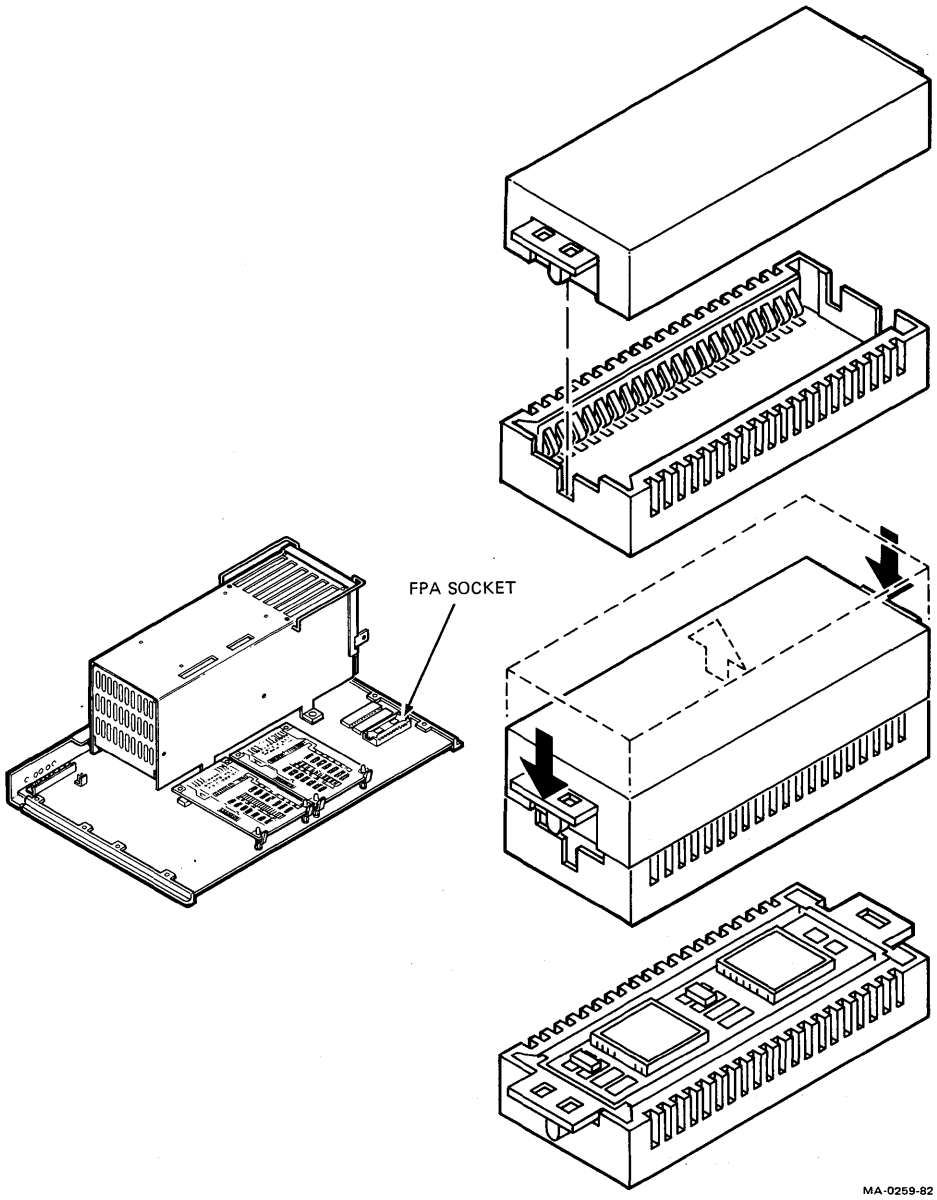


Figure 2-11 Installing the Floating Point Adapter

2.4 SYSTEM UPKEEP

The following sections describe system cleaning and floppy diskette handling.

2.4.1 System Cleaning

To clean the system unit, video monitor and keyboard covers, use a cloth dampened with a mild solution of soap and water.

To clean the monitor screen, use a cloth dampened with a mild solution of isopropyl alcohol and water.

2.4.2 Diskette Handling and Storage

Improper handling or storage of diskettes destroys recorded data and damages the read/write (R/W) heads in the RX50 dual diskette drive. The following are some suggestions for diskette handling.

- Return the diskette to its protective envelope when it is not being used.
- Store diskettes vertically and loosely to avoid warping the jackets.

CAUTION

Never store or place the diskette near any strong magnetic fields (such as on top of a motor, on top of the system unit, or on top of the monitor). This could damage the data on the disk.

- Use a felt tip pen to mark the diskette jacket. Do not use a pencil or ballpoint pen. These can crease the jacket and damage the media inside.
- Insert the diskette into the drive carefully. Never force the door closed; you could crush the diskette.
- Never remove or insert a diskette if either indicator on the RX50 drive is lit.

CAUTION

Do not open an access door if either drive is busy (drive indicator is lit). This damages the data stored on either diskette.

- Never touch the recording surface where the jacket is cut away for the R/W heads. Fingerprints damage recorded data and the R/W heads.
- Never store diskettes in direct sunlight or near heaters where temperatures go above 52° C (125° F). High temperatures warp the jackets.
- Never bend or fold the diskette jacket.

CHAPTER 3
CONTROLS AND INDICATORS

3.1 INTRODUCTION
The Professional 350 system consists of three major components: the system unit, video monitor, and the keyboard. Each component has controls and indicators that direct and monitor the system's operation.

3.2 SYSTEM UNIT CONTROLS AND INDICATORS
The following sections describe the controls and indicators for the Professional 350 system unit.

3.2.1 Controls
The system unit contains the following three controls.

- System power switch
- Voltage select switch
- System circuit breaker

3.2.1.1 System Power Switch – The system power switch is on the front of the system unit (Figure 3-1). It controls the input power for the system and is labeled with the numbers 1 for ON and 0 for OFF.

3.2.1.2 Voltage Selection Switch – The voltage selection switch is on the rear of the system unit (Figure 3-2). It selects either 110 Vac or 220 Vac and must be set before the system is turned on.

3.2.2 Indicators
The system unit contains two groups of indicator and one circuit breaker. The first group is located on the front of the system unit (Figure 3-1). This group indicates whether the diskette drives are busy or inactive.

The second group is located on the rear of the system unit (Figure 3-2). This group consists of 4 red and one green indicators and indicates the status of the system unit's internal power and self-test.

3.2.2.1 Diskette Drive Busy Indicators – Two indicators on the front of the system unit indicate if the diskette drive is busy. The upper indicator lights if the upper drive is busy and the lower indicator lights if the lower drive is busy.

3.2.2.2 Indicators 1, 2, 3, and 4 – These indicators, on the rear of the system unit, monitor the system's self-test. The self-test runs whenever the system power switch is turned on. At the end of the test, all four indicators turn off and the DIGITAL logo appears on the screen.

3.2.2.3 DC Indicator – The dc indicator monitors the power supplied to the system module. If this light is off when the power switch is on, then no dc is being applied to the system.

3.2.2.4 System Circuit Breaker – The system circuit breaker is located on the rear of the system unit (Figure 3-2). The circuit breaker pops out when an electrical fault occurs within the system.

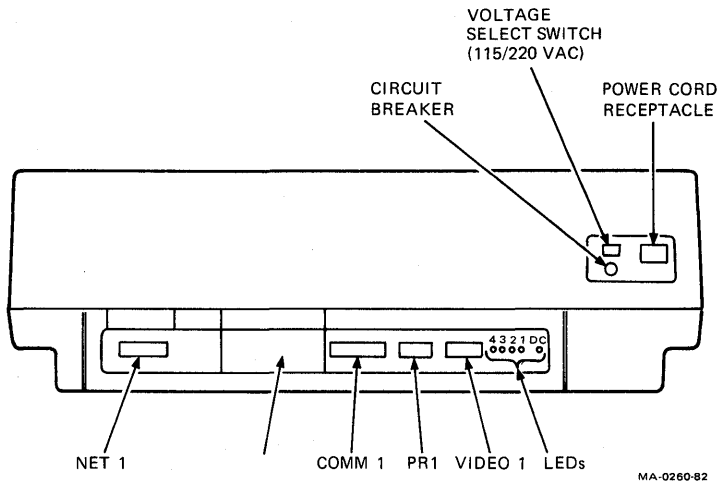


Figure 3-1 System Unit Front Panel

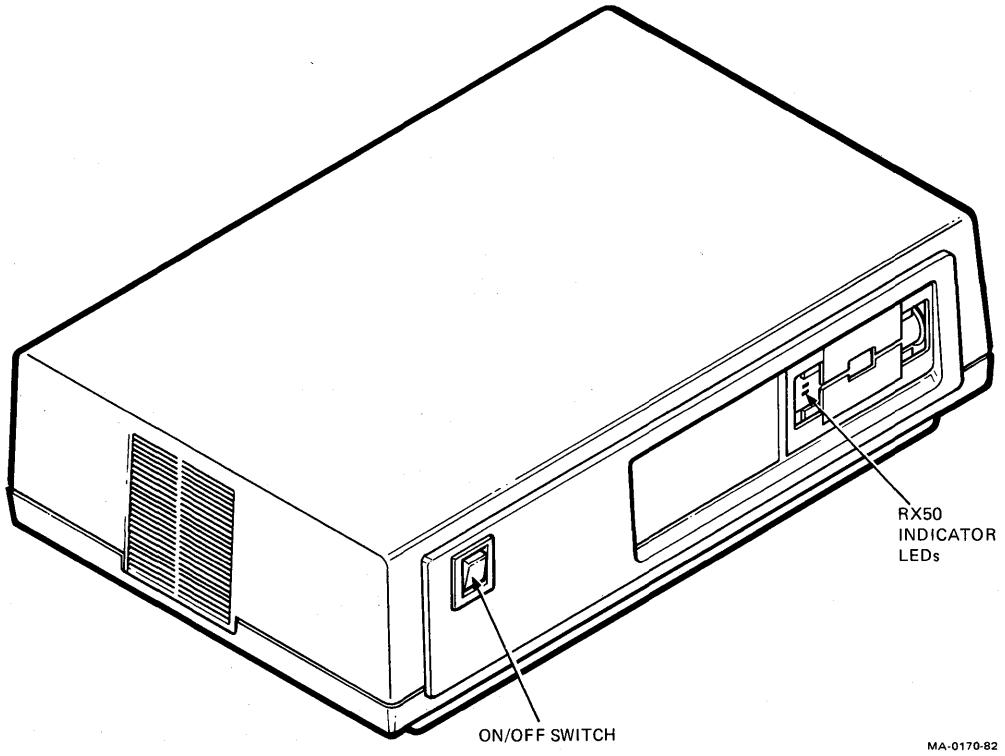


Figure 3-2 System Unit Rear Panel

3.3 VIDEO MONITOR CONTROLS

The following sections describe the controls for the Professional 350 video monitor. Since the monitor is the indicator for the entire system, there is no indicator section in this description.

The monitor has two controls (Figure 3-3).

- Brightness
- Contrast

3.3.1 Brightness – The brightness control is located on the rear of the monitor. This control determines the brightness of the display background.

3.3.2 Contrast – The contrast control is located on the rear of the monitor next to the brightness control. This control determines how bright the characters on the screen are compared to the background of the screen.

3.4 KEYBOARD CONTROLS AND INDICATORS

The following sections describe the keyboard controls and indicators (Figure 3-4).

3.4.1 Controls

The Professional 350 keyboard contains a series of special function keys and three keypads: the main keypad, the editing keypad, and the numeric keypad. These keys generate electrical codes which are processed by the internal CPU and then sent to the system module.

3.4.1.1 Main Keypad – The main keypad operates like a standard typewriter keyboard.

3.4.1.2 Editing Keypad – The editing keypad is used to edit or change data that has already been entered into the system.

3.4.1.3 Numeric Keypad – The numeric keypad is used to enter numeric data. The number, minus, comma, and period keys generate the same characters as the corresponding keys on the main keypad.

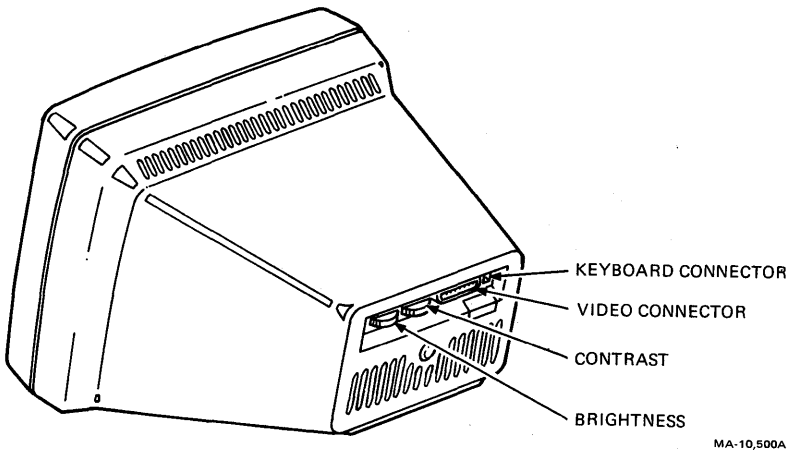


Figure 3-3 Monitor Rear Panel

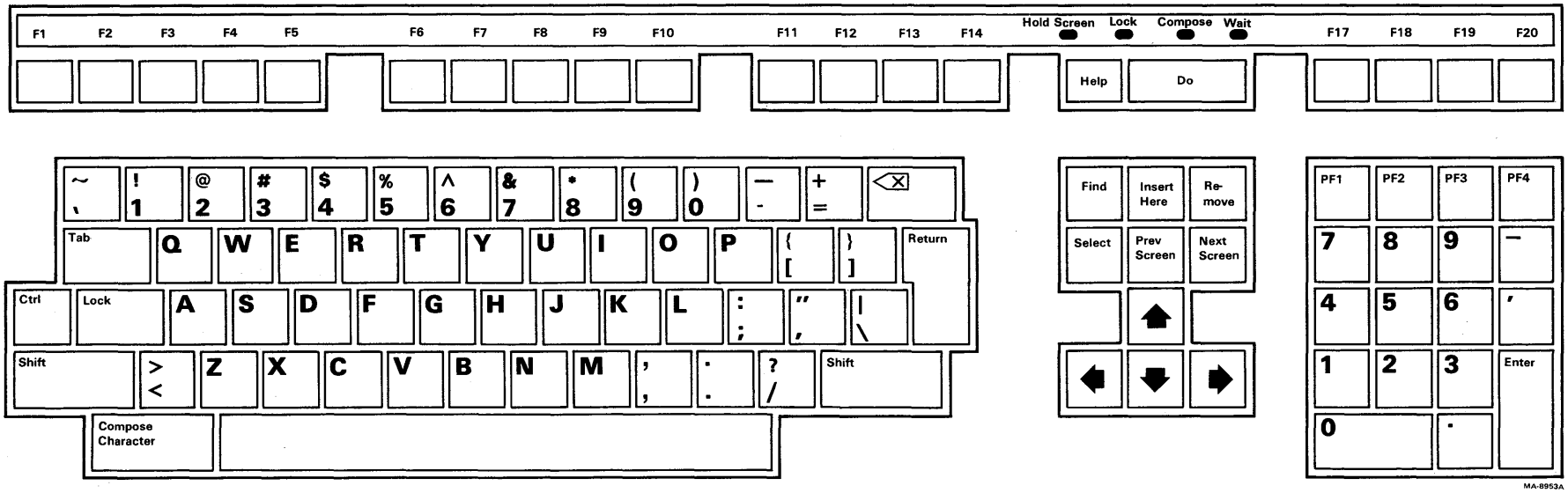


Figure 3-4 Keyboard Layout

3.4.1.4 Special Function Keys – The top row of the keyboard contains 20 keys. Two of these keys are marked HELP and DO. The remaining keys are blank. These blank keys are called special function keys. The operation that each key performs can change with the software application.

3.4.2 Indicators

The keyboard has four indicator and two indicator sounds. The indicators are located just above the HELP and DO keys. The indicator sounds generate a signal sound when an action occurs.

3.4.2.1 HOLD SCREEN Indicator – The HOLD SCREEN Indicator indicates when the system can display new data. If the indicator is turned off, the system can display new data. If the indicator is turned on, the data displayed on the screen is on hold and does not change.

3.4.2.2 LOCK Indicator – The LOCK indicator indicates whether the LOCK key has been pressed. If the LOCK indicator is turned off, all the alphabetic keys send lowercase characters. If the LOCK indicator is turned on, all the alphabetic keys send uppercase characters.

3.4.2.3 COMPOSE Indicator – The COMPOSE indicator indicates when the COMPOSE CHARACTER key is pressed. When this indicator is turned on, the system combines the next key pressed with the last key pressed and creates a special character.

3.4.2.4 WAIT Indicator – The WAIT indicator indicates when the system is performing a specific function or sequence of functions. When the WAIT indicator is turned on the keyboard is inactive. The operator must wait before entering any more data or commands on the keyboard.

3.4.2.5 CLICK – The click is one of two indicator sounds. A circuit in the keyboard generates this sound when a key is pressed.

3.4.2.6 TONE – The tone is an indicator sound generated by the keyboard under software control. When the tone sounds it indicates either something was performed wrong or a specific sequence of events is needed.

CHAPTER 4
SYSTEM OVERVIEW

4.1 INTRODUCTION

This chapter describes the function of each component in the Professional 350 system and how they interact. Detailed descriptions for each component are provided in the following chapters.

Figure 4-1 is a physical block diagram showing how each component fits together. Refer to this figure for the following discussion.

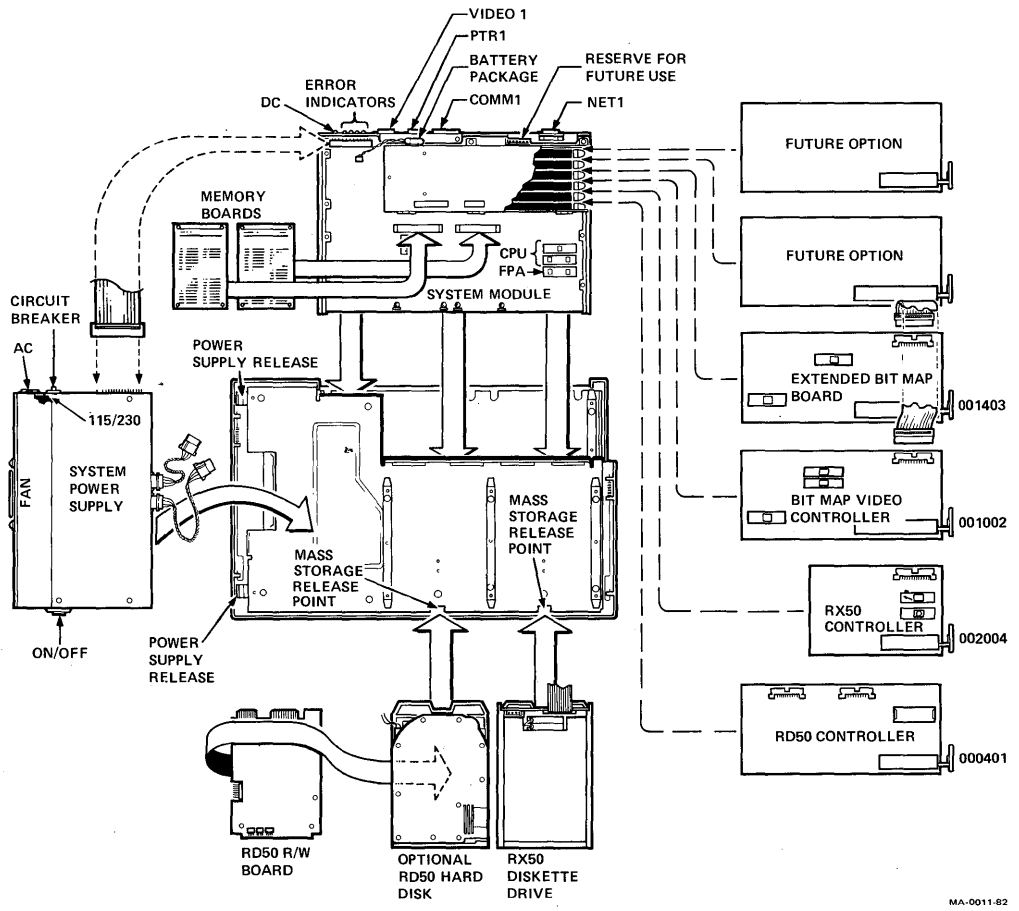


Figure 4-1 Physical Component Block Diagram

4.2 FUNCTIONAL DESCRIPTION

The following sections provide a functional description of the Professional 350 system components.

4.2.1 System Module

The system module is a 26.7 cm (10.5 in) × 40.6 cm (16 in) printed circuit board. It mounts on a metal plate that slides in and out of the bottom of the Professional 350 enclosure.

The system module consists of the F-11 chip set and support circuits. The F-11 is the central processing unit (CPU) for the Professional 350. The chip set consists of two integrated circuit chips: the data/control chip, and the memory management unit. Refer to Chapter 5 for a detailed description of the F-11 chip set.

The following is a list of the system module electronics.

- CPU – data/control chip and memory management unit.
- 16 kilobytes of boot/diagnostic ROM.
- A video/keyboard port that supports RS170-compatible color, monochromatic signals and the keyboard interface. The keyboard interface electronics are located on the system module. The video interface electronics are located on the video controller.
- A serial printer port that supports serial printers and acts as a terminal connector for maintenance purposes.
- A modem communications port that supports asynchronous, byte-synchronous, and bit-synchronous communications.
- A time-of-day clock with battery backup.
- Two connectors that support two 128K RAM daughter modules.
- A six-slot card cage that supports the Computing Terminal Interconnect (CTI) BUS. These also allow access to a general purpose I/O connector and two dedicated I/O connectors.
- A networking port.

4.2.1.1 Computing Terminal Interconnect (CTI) BUS – The CTI BUS is the interconnect path for the CPU and other option modules. It is a six-slot backplane mounted on the system module.

Each slot in the card cage has a 90-pin "T" rail connector. All modules inserted into the card cage must use a 60- or 90-pin zero insertion force (ZIF) connector.

The first 60 pins of the bus are used for all CTI BUS signals. This portion of the CTI BUS is referred to as the general section. The last 30 pins route signals from the option modules to connectors on the rear of the system module. These pins are referred to as the private section of the CTI BUS.

4.2.1.2 RAM Daughter Board (128K) – The system module supports two 128K RAM daughter boards. The RAM boards mount directly onto the system module. Each RAM board contains sixteen 64K × 1 dynamic RAM chips.

4.2.1.3 Floating Point Adapter (FPA) – The floating point adapter is an option for the F-11 chip set. It is a 40-pin IC mounted on the system module next to the memory management unit (MMU). The FPA contains the floating point instructions that supplement the arithmetic instructions of the data/control chip set.

4.2.2 Keyboard Subsystem

The keyboard subsystem consists of the LK201 keyboard and the keyboard interface electronics. Refer to Chapter 6 for a detailed description of the LK201 keyboard.

The keyboard connects to the system module by a cable from the monitor. It is also detachable. The keyboard contains an 8051 microprocessor to process all data entered through the keyboard. The interface USART for the keyboard is on the system module. Refer to Chapter 5 for a detailed description of the keyboard interface electronics.

4.2.3 Video Monitor Subsystem

The video monitor subsystem consists of the VR201 video monitor and the bit map video controller module. An extended bit map module is optional. Refer to Chapter 7 for a detailed description of the video controller and the extended bit map modules. Refer to Chapter 8 for a detailed description of the VR201 video monitor.

4.2.3.1 VR201 Video Monitor – The display screen is a 30.5 cm (12 in) diagonal monochrome monitor. The monitor housing contains the CRT, yoke assembly and the video monitor board. Two external controls adjust brightness and contrast. A cable in the rear of the system unit connects the monitor to the rest of the system. The monitor also contains a telephone-type connector for keyboard connection.

4.2.3.2 Bit Map Video Controller Module – The bit map video controller module is a 12.7 cm (5 in) × 30.5 cm (12 in) circuit board that plugs into one of the six slots in the CTI BUS card cage. The module contains bit map graphics with a single display memory plane of 1024 × 256 bits. The controller uses register-based control logic to help the system module access correct bit locations for screen display.

4.2.3.3 Extended Bit Map Module – The extended bit map module (EBM) is a 12.7 cm (5 in) × 30.5 cm (12 in) circuit board which plugs into a slot next to the bit map video controller module in the CTI BUS card cage. This module adds two more bit map memory planes (1024 × 256/plane) to the monitor subsystem. When used with a monochrome system, it provides enhanced graphics and additional levels of gray scale. When used with a color system, the bit map video controller provides support for the blue scale. The red and green scales are supported by the extended bit map module.

4.2.4 RX50 Dual Diskette Drive Subsystem

The RX50 dual diskette drive subsystem consists of the drive controller and the drive unit. Refer to Chapter 9 for a detailed description of the RX50 controller module and Chapter 10 for a detailed description of the RX50 dual diskette drive.

4.2.4.1 RX50 Controller Module – The RX50 controller module is a 12.7 cm (5 in) × 20.3 cm (8 in) circuit board that plugs into slot 2 of the CTI BUS card cage.

NOTE

The RX50 controller can only be inserted into slots 1 or 2 of the card cage. If the system has an RD50 hard disk drive subsystem, the RX50 controller can only be inserted into slot 2.

All subsystem activity is performed under program control. The RX50 controller module can perform implied seeks, reading, and writing to specified sectors and tracks on the diskette.

4.2.4.2 RX50 Dual Diskette Drive – The RX50 is a diskette drive which mounts in the system box. Each RX50 unit contains two physical drives.

NOTE
The RX50 unit is only capable of single-sided reading/writing per drive.

Each drive within a single drive unit provides 409,600 8-bit bytes (formatted) per diskette for a total of 819,200 bytes of storage. A signal cable connects the drive to the RX50 controller. A dc power cable connects the drive directly to the power supply.

4.2.5 RD50 Hard Disk Drive Subsystem

The RD50 hard disk drive subsystem consists of the controller and drive unit. Refer to Chapter 11 for a detailed description of the RD50 hard disk controller and Chapter 12 for a detailed description of the RD50 hard disk drive.

4.2.5.1 RD50 Hard Disk Controller – The RD50 hard disk controller is a 12.7 cm (5 in) × 30.5 cm (12 in) circuit board which plugs into slot 1 of the CTI BUS card cage. The system module controls all drive activity. Data transfers to the storage media are performed in two steps.

- The system module controls a data transfer from main memory to the sector data buffer on the RD50 controller.
- The RD50 controller then channels this data to the RD50 drive.

Two cables connect the controller to the drive: a disk data I/O cable and a control status cable. A power cable supplies power directly to the drive unit.

4.2.5.2 **RD50 Hard Disk Drive** – The RD50 is a 13.3 cm (5.25 in), nonremovable, sealed media, hard disk drive. Two nonremovable 5.25 in hard disks are used as the storage media. Each disk surface uses one R/W head. The total storage capacity (formatted) is five megabytes.

The RD50 hard disk drive consists of two subassemblies: the head/disk assembly (HDA) and a R/W module. The disk drive contains the storage media and supporting mechanical assemblies and cannot operate without the R/W module. The R/W module is assembled in the drive unit. Both slide into the system unit (Figure 4-1). Two connectors on the R/W module connect the drive to the RD50 hard disk controller. A third connector on the R/W module connects the drive to the power supply.

4.2.6 Power Supply

The power supply is a 210 watt, switch type, ac/dc voltage converter circuit. It operates at a constant frequency using pulse width modulation to regulate voltage to the system. Voltage to the supply is single-phase/three-wire and user-selectable at 115 or 230 Vac. Maximum input power required is 320 watts.

The supply mounts on the left side of the system unit. The power supply contains the system power switch, power supply circuit breaker, and voltage selection switch. It also contains circuits to protect the system against overvoltage, start-up undervoltage, and overcurrent conditions. Refer to Chapter 13 for a detailed description of the power supply.

4.3 FUNCTIONAL OPERATION DESCRIPTION

The following is a functional operation description. Figure 4-2 is a functional block diagram that shows how the components interact in the Professional 350. Refer to this figure for the following discussion.

The operating system of the Professional 350 can execute several simultaneous tasks. This is accomplished by using dedicated interrupts from microprocessor-based components to the CPU.

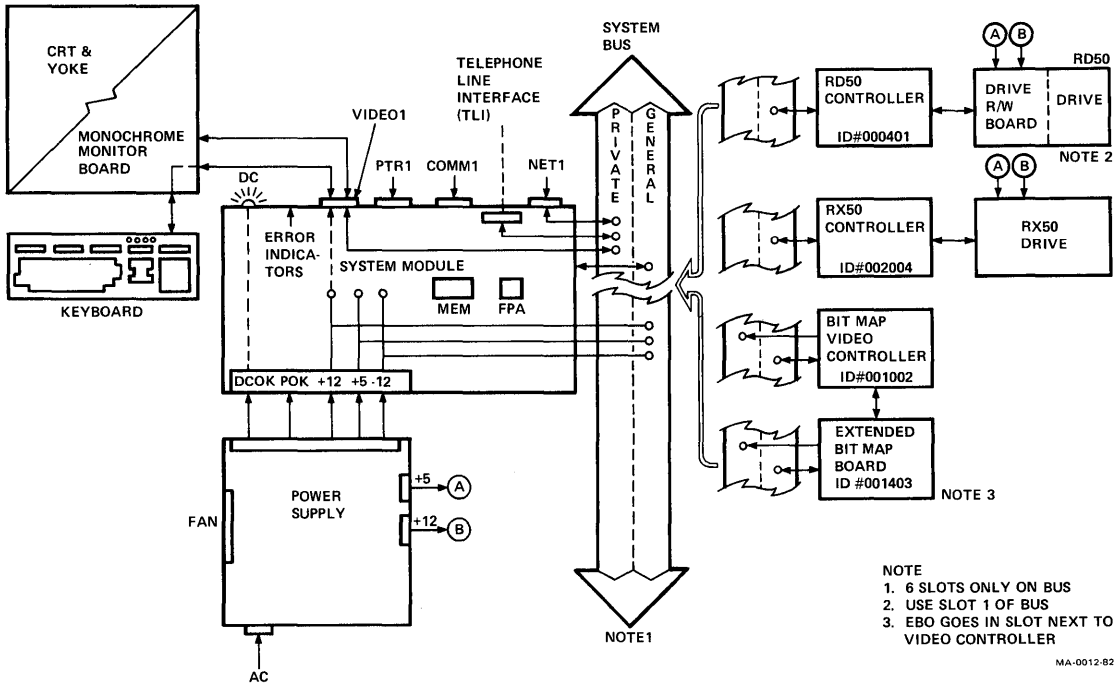


Figure 4-2 Functional System Block Diagram

4.3.1 Initialization Sequence

At power up, the CPU accesses all available components to determine the system configuration. It then assembles an I/O map in main memory. This corrolates each device with its appropriate handling routine.

4.3.2 Hardware Interaction Example

The following example is presented as an aid in understanding how the Professional 350 operates. It may not follow the specific CPU execution cycles.

In the example, the Professional 350 retrieves a file from the RX50, updates the video display and prints a file to an attached printer. Each task is concurrently executed and supervised.

- To retrieve a file, the host processor specifies the necessary address and executes a READ command to the RX50 controller. When the data is ready, the controller responds with a command completion interrupt to indicate the data is available.

- To update the CRT display, the host processor calculates the data and address for the display. It then loads this information into the video bit map memory space.

- To print a file, the host processor first addresses memory. It then addresses the printer USART. The USART assumes control and transfers the data, one character at a time, to the printer. As each transfer is completed, the USART interrupts the CPU and waits for the next character to be loaded.

Each task requires several host processor cycles. Dedicated interrupts received from each device inform the host processor of completed commands or device readiness. Most microprocessor-based devices for the Professional 350 do not require sequential command and data accesses. This leaves the host processor free to select, according to its priority scheme, which device to serviced during each processor cycle.

CHAPTER 5
SYSTEM MODULE

5.1 INTRODUCTION

This chapter describes the Professional 350 system module, which is represented by the shaded part of Figure 5-1. The system module contains the central processor unit (CPU) and circuits that support its operation. These circuits permit the CPU to communicate with devices mounted on the system module and with devices mounted on the CTI BUS or peripheral devices that are attached through the connectors on the rear panel of the system box. Figure 5-2 shows the system module.

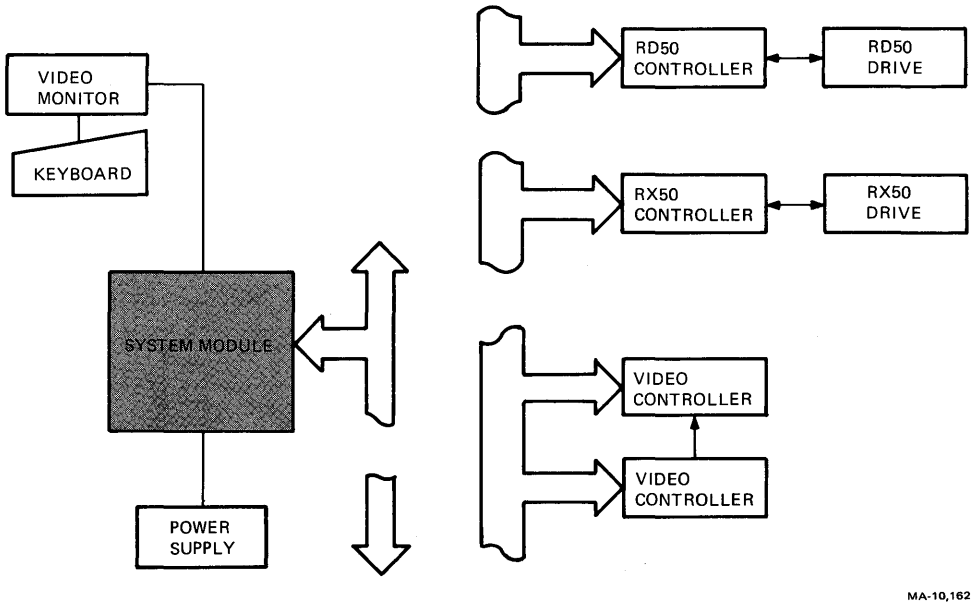


Figure 5-1 System Block Diagram

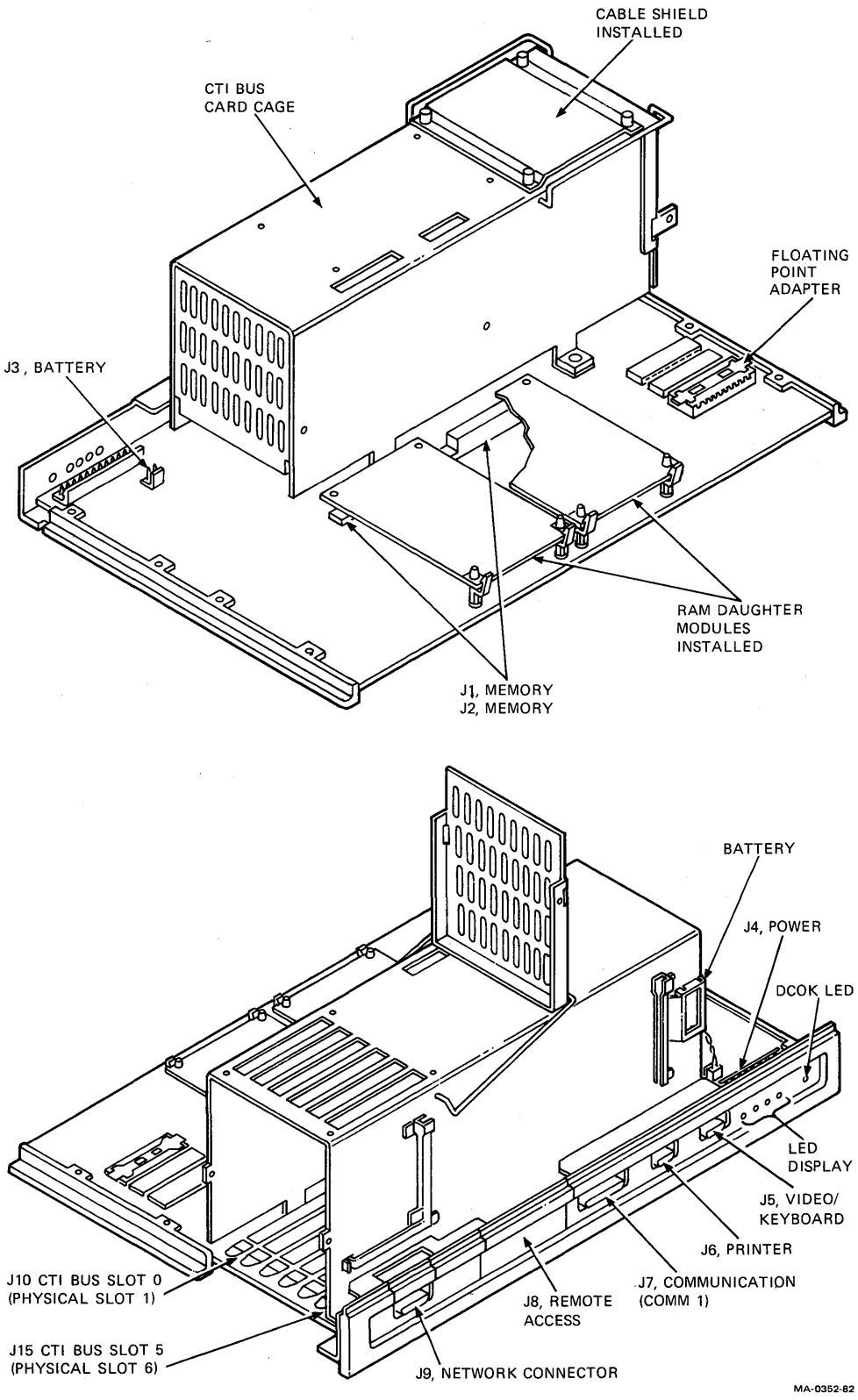


Figure 5-2 System Module

5.1.1 Chapter Organization

This chapter is divided into five sections.

- Section 5.2 provides a general description of the functions performed by the system module.
- Section 5.3 provides a detailed description of the circuits and components that perform the module's functions. It also provides the theory of operation.
- Section 5.4 provides information about programming the devices that make up the system module. Programming information is given in machine language, not high level application language.
- Section 5.5 provides the pin-out for the connectors on the system module itself and the back panel of the system module box.
- Section 5.6 provides the specifications for the unit.

Sections 5.2, 5.3, and 5.4 follow approximately the same format. The sub-sections follow the same sequence so material presented in Section 5.2.6, for example, corresponds to material in Sections 5.3.6 and 5.4.6. This relationship is followed most closely for Sections 5.2.6, 5.3.6, and 5.4.6.

5.1.2 Related Documentation

Title	Document No.
KEF11 Field Maintenance Print Set	MP-01473-00

5.2 GENERAL DESCRIPTION

The following paragraphs provide a general description of the basic functions performed by the devices and circuits that are on the Professional 350 system module.

5.2.1 System Module General Description

The CPU/memory module provides the basic centrol processor unit (CPU) functions (F-11 CPU chip set and memory management unit) for the computer and also supplies the I/O module expansion backplane for up to six options. All input and output connectors (printer, keyboard, communications, network, and remote access lines) reside on this module. This module supports the Computer Terminal Interconnect CTI) BUS structure.

The system module supports random access memory (RAM) on optional plug-in printed circuit modules (daughterboards). Each daughterboard has 128 Kb of RAM. Up to two daughterboards can be used, although the system module's addressing and decoding logic provides for addressing one megabyte. These modules are not connected through the option area.

The system module has a 22-bit address space to access up to four megabytes, although this system's memory range has been limited to three megabytes. The top eight kilobytes are reserved as the I/O page.

All interrupt for devices on the system module and devices on option modules are handled by controllers on the system module. The system module supports DMA to the RAM memory and arbitrates all the DMA requests.

5.2.1.1 Subsystem Characteristics – The CPU/memory board provides the following functions.

- PDP-11/23 instruction set
- 16-bit word or 8-bit byte addressing
- Eight internal registers
- Stack processing
- Programmable vectored interrupts
- Direct memory access (DMA)
- 16-bit ODT console emulater
- Support for one megabyte of RAM (on system module daughterboards)
- 22-bit addressing (three megabyte addressing capability)
- Kernel and user modes only (no supervisor mode)
- Optional floating point instruction set
- Power-up self-test and bootstrap (ROM based)
- Indicator (LED) display
- Battery backed-up time and date clock
- Battery backed-up RAM (50 bytes)
- Printer/console interface
- Video/keyboard interface
- Communications interface
- Full modem controls
- ID PROM
- Six slot CTI backplane

5.2.2 Physical Description

The system module is 26.0 × 40.0 cm (10.4 × 16 inches) and has the CPU and support circuits on it. The CTI BUS is located in an aluminum card cage that has six bus slots inside. A hinged door covers the opening. Access slots for option modules are on top. The rear panel has most of the connectors on it and forms the rear of the system module.

5.2.3 System Module Features

The system module consists of a CPU which, under software control, can perform several tasks concurrently. This is called interlacing operations. Since a single operation may require more than one processor cycle, the CPU can perform another task while completing the first. When the first is done, an interrupt informs the CPU. The CPU can then find the status of that operation, begin its next step, and repeat the process for the second step.

The CPU directs, controls, and monitors operations on the system module. Interrupts, printer, keyboard, and communications interfaces are programmable. These devices perform their own functions and through interrupts, permit interlacing operations to take place in a foreground and background mode.

5.2.3.1 Central Processor – The central processor consists of a 2 die 40-pin hybrid integrated circuit. The data chip contains the PDP-11 general registers, the processor status word (PSW), working registers, the arithmetic logic unit (ALU) and conditional branching logic. It performs arithmetic and logical functions, handles all data and address (except relocation) transfers with the external BUS, and operates most of the signals used for interchip communication and external system control.

The control chip contains microprogram (internally programmed sequences) logic and local microprogram storage in programmable logic array (PLA) and ROM arrays. This chip accesses the appropriate microinstruction in PLA or ROM, sends it along the microinstruction bus (MIB) to other control and MMU chips, and generates the next microinstruction (microprogram instruction) address. The control chip accesses only its local storage but additional control chips can be added externally to provide additional microprogram storage (for example, for floating point processing).

5.2.3.2 Memory Management – The memory management unit provides 22-bit memory addressing capability of four megabytes (two megabytes). It also allows memory protection in a multi-tasking operating system environment. The maximum allowable system memory is three megabytes.

The memory management function is implemented in one 40-pin package. The floating point registers are located in the MMU chip.

5.2.3.3 Floating Point Adapter (FPA) Option – The floating point instruction set (FP11) is an option. Both single and double precision floating point capability are available. Other features available include floating-to-integer and integer-to-floating conversion.

The FP11 microprogram resides in two MOS/LSI chips contained in one 40-pin package the FPA. The FPA requires both the MMU chip and the base MOS/LSI chips because all the floating point accumulators and status registers reside in the MMU.

5.2.3.4 Power-Up Self-Tests – The power-up self-tests in ROM verify system configuration and available memory space. The self-test is executed at every system power up. Verification is the identification of devices and their statuses.

The self-tests include the following three parts.

- System core
- Base options
- Add-on options

After these three parts are finished, the system executes a bootstrap loading routine.

The system core self-test verifies the CPU, all available memory space, the self-test ROM, and the full addressing range of the MMU chip. The power-up self-test does not continue testing if the system core self-test is not successful.

The base option part of the self-test continues after successful completion of the system core self-test. This part tests all options available on the system module. The options include the communications port, system clock, FPA (if installed), the printer port, battery check, battery backed up RAM check, and video/keyboard port.

The final part of the self-test is the add-on options self-test. This test is performed on all options connected to the CTI BUS. The self-test is loaded from a ROM located on each option module. This does not include the RD50 hard disk drive subsystem, the RX50 dual diskette drive subsystem, and the video subsystem. The system's ROMs contain the diagnostics for these components. All other option modules contain their own self-test diagnostics. All option modules have an option identification number. This number allows the system self-test to determine which devices are installed in the system and store this information in a configuration table for use by the operating system.

The primary indicator of an error during self-test is a picture of the system displayed on the monitor with the failing option highlighted. Also displayed are an error code and the identification number (ID) of the error type. The secondary error indicator is the four indicators (LED) display on the rear of the system box which can be used if the monitor display is either not attached or not working.

5.2.3.5 Boot Sequence – If the power-up self-tests are completed without error, the system enters a bootstrap routine and the DIGITAL logo appears on the monitor. This causes a search to first determine the boot device and then to load the boot program.

The following is the three phase boot sequence.

- Primary Boot Sequence – At the end of the power-up self-test, the diagnostic boot ROM determines if there are any removable media devices on the system. If there are, each device is read and tested for a bootable volume. If there are no removable media devices on the system or there is no bootable volume loaded, the secondary boot sequence is executed.

- Secondary Boot Sequence – The second phase consists of reading the battery backed up RAM for customer-selected boot devices. The first selectable device boot routine in battery backed up RAM is loaded and executed. If this boot fails, the diagnostic boot ROM selects the next device. Once all devices in the battery backed up RAM have been tried without success, the tertiary boot sequence is started.

- Tertiary Boot Sequence – The third step uses the boot priorities predetermined by the ID number of the devices. The diagnostic boot ROM starts with the highest priority, loads the appropriate boot program, and starts execution. If the boot fails, the next device in the priority chain is selected and an error is displayed on the monitor, indicating the boot process failed. The display is a picture of a diskette with a question mark.

- Bootstrap Failure – After the bootstrap error is displayed, the self-test ROM loops back to the primary boot sequence and stays in this loop until a valid boot is executed or power is reduced.

5.2.4 CTI BUS Option Connectors

The CTI BUS backplane is part of the system module. The backplane accepts option modules using a zero insertion force (ZIF) connector. There are six option module slots.

Each option slot has a 90-pin connector on the system module. The first 60 pins (referred to as the general section of the bus) are used for the CTI BUS signals. The last 30 pins, 61 through 90 (referred to as the private section of the bus), to route signals from the option modules to connectors on the rear of the system module. An option module that only requires the CTI BUS signals can use a 60-pin ZIF connector. An option module that requires using the rear connectors on the system module must use a 90-pin ZIF connector.

All signals, except six signals, are bused through all six slots. The six non-bussed signals provide slot dependent signals to the system module for handling address decoding, interrupts, and DMA.

5.2.5 System Registers

The system module contains registers that store information about the overall system status. The CPU reads these regularly and performs the appropriate service routine whenever a status change occurs.

5.2.5.1 Indicator (LED) Register and Display – This register is the only one visible to the user. It shows the system status after the power-up self-test (Section 5.2.3.4).

There are five LEDs on the rear of the system module, one green and four red LEDs. The green one turns on when the DCOK signal from the power supply is asserted. This indicates all dc power is within tolerance. The four red LEDs indicate errors found during the power-up self-test. At power up, all four red LEDs turn on then turn off if no errors are found. If the LEDs remain on, it indicates a system module error. The decoded indicator error codes are found in Table 5-6.

5.2.6 Interrupts

The system module uses three interrupt controller chips to handle all the system interrupts.

- The first controller handles all the interrupts generated by devices on the system module.
- The second controller handles all the A interrupts from the option modules.
- The third controller handles all the B interrupts from the option modules.

The interrupt controllers do the following.

- Latch the interrupt requests
- Provide the interrupt enable for each
- Prioritize the pending interrupts
- Generate the proper vectors

The controllers interrupt the CPU at processor status level 4.

5.2.7 ROM Memory

The system module also contains 16 kilobytes of ROM. It contains the power-up self-test code, configuration and initialization code, and the boot code. Some of the ROM is in the I/O page and some is in the memory address space.

Address	Size	Location
17730000–17757776	12 KB	memory space
17760000–17767776	4 KB	I/O page

Any attempt to write to the ROM locations results in a non-existent memory trap to location 4.

5.2.7.1 ID PROM – Each system module board contains a PROM with a unique 32-byte ID. The ID PROM contains information to verify the system module integrity.

5.2.8 RAM Memory

The system module contains support circuitry for two memory option modules (daughterboards). There are two 40-pin connectors on the system module that accept the memory modules. The memory option modules provide 128 Kilobytes of RAM with 16 64K × 1 dynamic RAM chips. The system module can address up to 512 kilobytes at each RAM daughter module slot.

With this scheme, backplane slots are not used for memory. However, additional memory can be installed in the backplane if required. Memory added in the backplane requires its own support circuitry (address and decode logic).

5.2.9 Video/Keyboard Port

The system module provides a serial keyboard port as part of the video/keyboard port. Video signals for black and white and color CRT monitors use other pins in the same port.

The video controller, mounted on the CTI BUS, generates the video signals. Refer to Chapter 7 for information about the bit map video controller module.

The keyboard uses a 2661 USART and performs asynchronous serial communications at programmable baud rates up to 19.2 kilobaud. The port uses EIA RS-423 signal levels. Connection is made on the rear of the unit via a 15-pin male D-subminiature connector, J5. Section 5.5 shows the pinning and position of J5 on the system module.

The keyboard part of the port communicates with the computer's keyboard. However, it is a general serial port that can be used to communicate with any serial device. The mode of operation is programmable (Section 5.4). When using the port with the computer's keyboard, the mode must be set to the following.

- 8-bit character length
- No parity
- One stop bit
- 4800 baud clock rate

5.2.10 Printer Port

The system module provides a serial printer port. It can perform asynchronous serial communications at programmable baud rates up to 19.2 kilobaud. The port uses EIA RS-423 signal levels. Connection is made on the rear of the unit via a 9-pin male D-subminiature connector, J6.

5.2.10.1 Console Serial Line Port – The console DL is included as a maintenance feature. Physically it is the same port as the printer port. The printer port can be made to simulate a standard console interface. When a terminal is connected to the port instead of a printer, the address decoder recognizes the console addresses 17777560–17777566. In this mode, the port programs like a DL serial device with a receiver CSR, a receiver data buffer, a transmitter CSR, and a transmitter data buffer. Accesses to these registers when a terminal is not connected to the port result in reads of all zeros and writes with no effect. All the printer port registers, 17773400–17773406, are always accessible.

Interrupts are not handled like a standard console DL. There are no interrupt enable bits in the CSR registers at locations 17777560 and 17777564. Interrupts must be enabled/disabled and handled through interrupt controller 0 like the printer port interrupts. The vectors can be changed from the printer port vectors of 220 and 224 to the console vectors of 60 and 64 by reprogramming the response memory in interrupt controller 0 (Refer to Sections 5.2.6, 5.3.6, and 5.4.6 for details).

Hardware break detection can be enabled when a terminal is connected to the port. This allows the processor to halt into micro-ODT (Octal Debugging Technique) when the break key is depressed on the terminal. The hardware break detection has no effect if a printer is connected to the port.

When pins 8 and 9 of the printer port connector J6 short, the hardware determines that a terminal is connected to the port. When using the port for a printer, a printer port cable (PN BCC05) should be used (the cable does not short pins 8 and 9). When using the port as a console, a terminal port cable (PN BCC08) should be used (the cable shorts pins 8 and 9).

5.2.11 Communication Port

The system module has a communication port that can operate in asynchronous and bit or byte synchronous protocols. In asynchronous mode, it runs at split programmable baud rates up to 19.2 kilobaud. In synchronous mode, it runs up to 740 kilobaud. The transmitter is double buffered and the receiver is quad buffered. A full set of modem controls is also present. All the port signals are EIA RS-423 levels. Connection is made on the rear of the unit via a 25-pin male D-subminiature connector, J7.

There are two interrupts associated with the communications port. The first interrupts the CPU if the 7201 USART chip requires service, receiver or transmitter. The second interrupt can indicate that a state change has occurred on one of four modem control signals. These four modem control signals are Ring Indicator, Data Set Ready, Clear To Send, and Carrier Detect.

5.2.12 Battery Backed up System Clock and RAM

The battery backed up system clock and RAM keeps track of time and date. It stores 50 bytes of data even when the system is turned off. The clock is an MC146818 CMOS chip. The backup is achieved using of a rechargeable nickel cadmium (NiCD) battery. The battery power is supplied to the system module via connector J3.

The clock accuracy is better than one minute per month.

The battery continuously charges when the system is powered on. When the power is shut off, the battery supplies power to the clock which continues to update the time and date. A completely charged battery maintains clock operation for a minimum of 10 days while the system is turned off. The battery is completely charged after 48 hours of continuous system power on time.

The system clock and RAM contains a bit which indicates if the clock power goes too low and that the time and date may be invalid. The bit, called a valid RAM and time (VRT) bit, is located in the CSR3 register. See Section 5.4.13.1 for details of the VRT bit.

The chip can also be programmed to interrupt the CPU at a specified alarm time or at a periodic rate. The periodic rate can be programmed to one of 13 frequencies ranging from 2 Hz to 8.192 kHz. There is no line time clock.

5.3 DETAILED DESCRIPTION

This section provides functional and detailed descriptions of the functions performed by the microprocessor and support circuits of the KDF11-CA system module. It describes the system logic used for making decisions. It only describes computer operations, electronic processes, or complicated timing sequences when necessary.

To understand the central processor's functions refer to the following books.

Microcomputers and Memories
Microcomputer Processor Handbook
KDF11 Field Maintenance Print Set (MP-01473-00)

All illustrations in this section functional block diagrams. Logic symbols indicate function and may not represent actual circuitry. Figure 5-3 shows this section's map and module block diagram. For quick reference, each block on the diagram has a number or numbers by it. These numbers refer to the subsection(s) in this section that describe the block.

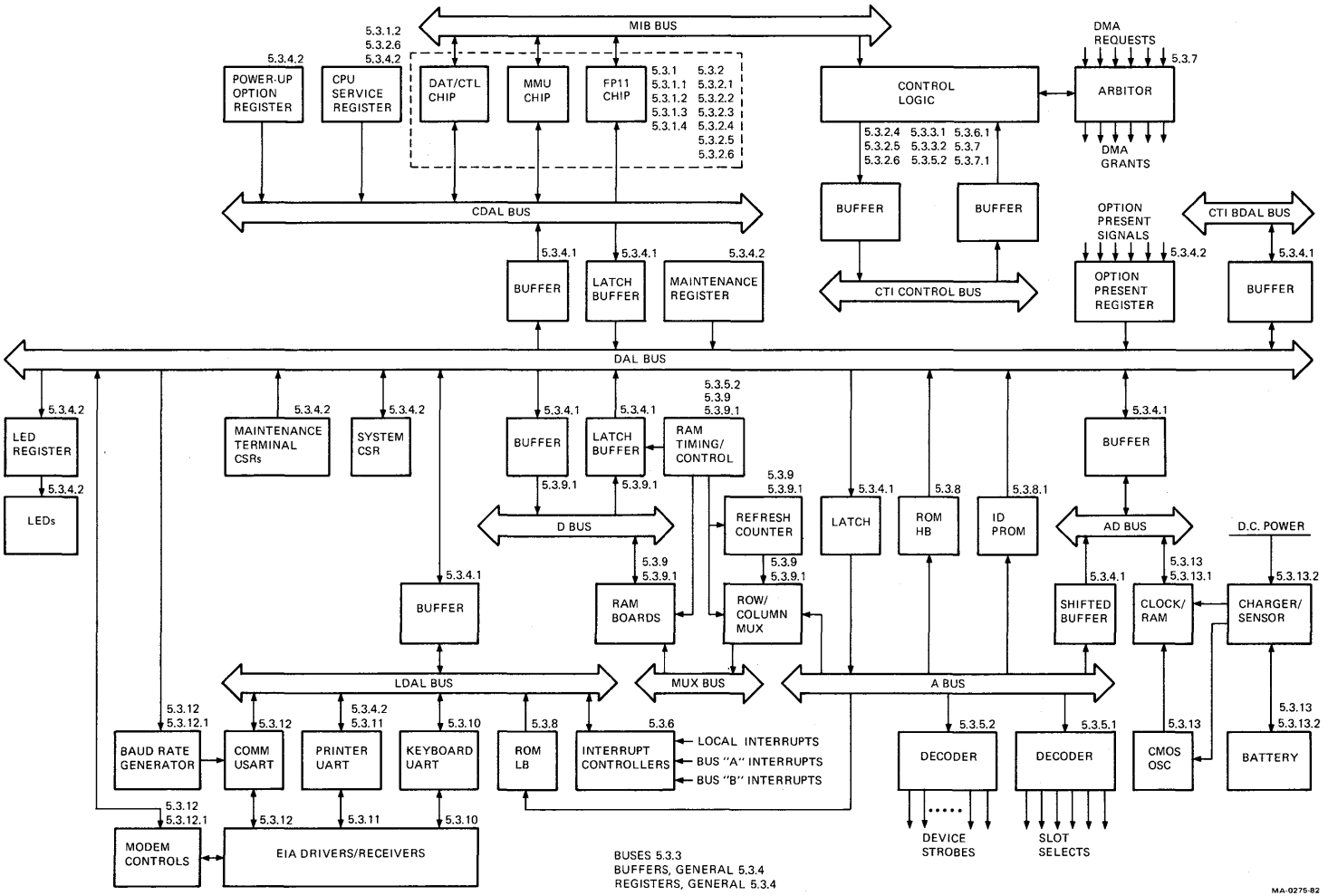


Figure 5-3 Section 5.3 Map

5.3.1 Microprocessor Overview

The Professional 350 CPU chip set consists of three integrated circuit chips: the data chip, the control chip, and the memory management unit (MMU) chip. The chip set is a 16-bit LSI microprocessor with PDP-11/23 capabilities. It also implements a subset of PDP-11/70 memory management. The chip set can also execute floating point arithmetic instructions when an FP11 option, the Floating Point Adapter (FPA), is installed.

The chips are installed on 40-pin ceramic dual in-line packages (DIP). The basic configuration is a hybrid combination of a data chip and a base control chip on a single DIP, the central processor chip. The memory management unit (MMU) is mounted by itself on a DIP.

The data chip contains PDP-11 registers, scratchpad registers, and the arithmetic logic unit (ALU). The control chip contains (in internal memory) instructions to supervise CPU operations. These instructions, called microinstructions, emulate the instructions performed in full size PDP-11 processors. The CPU's logic telling it how to use microinstructions are called the microprogram. The PDP-11 instructions are called here macroinstructions. Therefore the Professional's CPU, which is not actually a PDP-11 itself, performs microinstructions which emulate PDP-11 macroinstructions. Several microcycles (periods to perform microinstructions) may be required for each macrocycle (period to complete a macroinstruction).

The memory management chip contains the necessary registers and relocation logic to implement 18 and 22-bit addressing. It also contains the floating point register file.

- Data chip
  The data chip contains PDP-11 registers, scratchpad registers, the processor status word (PS), the arithmetic logic unit (ALU), and the conditional branching logic (i.e., microinstructions). This chip performs all arithmetic and logical functions, handles data and address transfers with the rest of the system (except relocated addresses), and coordinates most interchip communication.

- Control chip
  The control chip contains the microprogram logic and the required storage areas to supervise CPU operations. The control chip implements microinstruction sets, emulating the basic PDP-11 instruction set. These instruction sets include the extended instruction set (EIS) and provides console debugging capabilities.

- Memory management unit (MMU) chip
  The memory management unit (MMU) performs two activities. It provides the memory management and contains the necessary registers for floating point execution.

  As a memory management unit, the chip provides dual mode capability (user instruction space – normal operation) and kernel (CPU instruction space – internal operation) for relocation of a 16-bit virtual address to an 18-or-22 bit physical address. The MMU chip contains the error detection logic to provide memory protection features such as R/W access control and page length limits. In addition, all necessary memory management data registers are in this chip.

  As an aid to floating precision, the MMU chip provides the 36 16-bit registers needed for operand storage, status information storage, and scratchpad areas during floating point operations.

- Floating Point Adapter (FPA) Option
  The floating point precision option (FP11) provides 46 additional instructions to the integer arithmetic instructions in the basic instruction set. This option executes floating point operations 5 to 10 times faster than equivalent software routines and provides for both single precision (32-bit) and double precision (64-bit) operands. This is equivalent to 7 and 17 decimal digit accuracy respectively. This option also conserves memory space since the FP11's internal logic executes floating point routines instead of programmed routines. FP11 operation requires the MMU for operation because the MMU contains eight 64-bit floating point registers.

5.3.1.1 Chip System Architecture – These are three categories of signals used for communicating between the chips and with external logic: Microinstruction Bus (MIB), Data Address Lines Bus (DAL), and discrete signals (Figure 5-4).

The MIB is time-multiplexed. During clock-low time, a new microinstruction travels along the MIB from the active control chip to the data chip and all other control chips. During the next clock-high time, the data chip generates control information based on this microinstruction and transmits control information on the MIB.

The CDAL bus is a bi-directional connection between the logic circuits. It is time-multiplexed and has two independent definitions during the clock cycle. During the first half of a cycle, clock-high time, the chips use the CDALs to transfer data in or out. This data is a PDP-11 macroinstruction, a 16-bit physical or virtual address, or some form of numerical data. During the last half of a cycle, clock-low time, a relocated address or service information can be transferred on the CDALs. The relocated address is the 18 or 22-bit translation of the 16-bit virtual address driven by the data chip during the preceding clock-high time. The MMU chip must be installed (normal operation in the Professional 350) for 22-bit addressing. Synchronous and asynchronous status information, service, also use the CDAL bus. Service information consists of interrupt requests, error conditions, power conditions and the halt line. This information is latched in the control chip where it directs microprogram flow.

The discrete signals are dedicated lines each with specific meanings; they are not time-multiplexed. These signals are discussed later.

Table 5-1 summarizes the buses just presented.

5.3.1.2 Data/Base Control Chip Interaction – The data chip/base control chip combination is a multichip PDP-11 microprocessor with expandable internal storage for microprogram processing. The data chip/control chip relationship is that of arithmetic logic unit (ALU) and sequencer; the data chip is an ALU and controller, the control chip directs the microprogram sequence and storage. The following sequence provides an overview of their operation. This sequence considers just the base control chip. However, all control chips interact with the data chip in the same manner. They differ only in what macro-level information they can decode.

1. Fetch macroinstruction: both the data and control chips receive and latch a macroinstruction.

2. Execute macroinstruction: the control chip transmits a specific sequence of microinstructions to emulate the latched macroinstruction. Simultaneously, the data chip receives the microinstructions and performs the appropriate arithmetic, logical, and control functions.

3. Load service information: the control chip latches service information. If service is pending (Section 5.3.2.6), the chip set goes to step 4. If no service is pending, the chip set goes to step 1.

4. Execute service routine: the control chip transmits a specific sequence of microinstructions to execute the required service routine. Simultaneously, the data chip receives the microinstructions and performs the appropriate arithmetic, logical, and control functions.

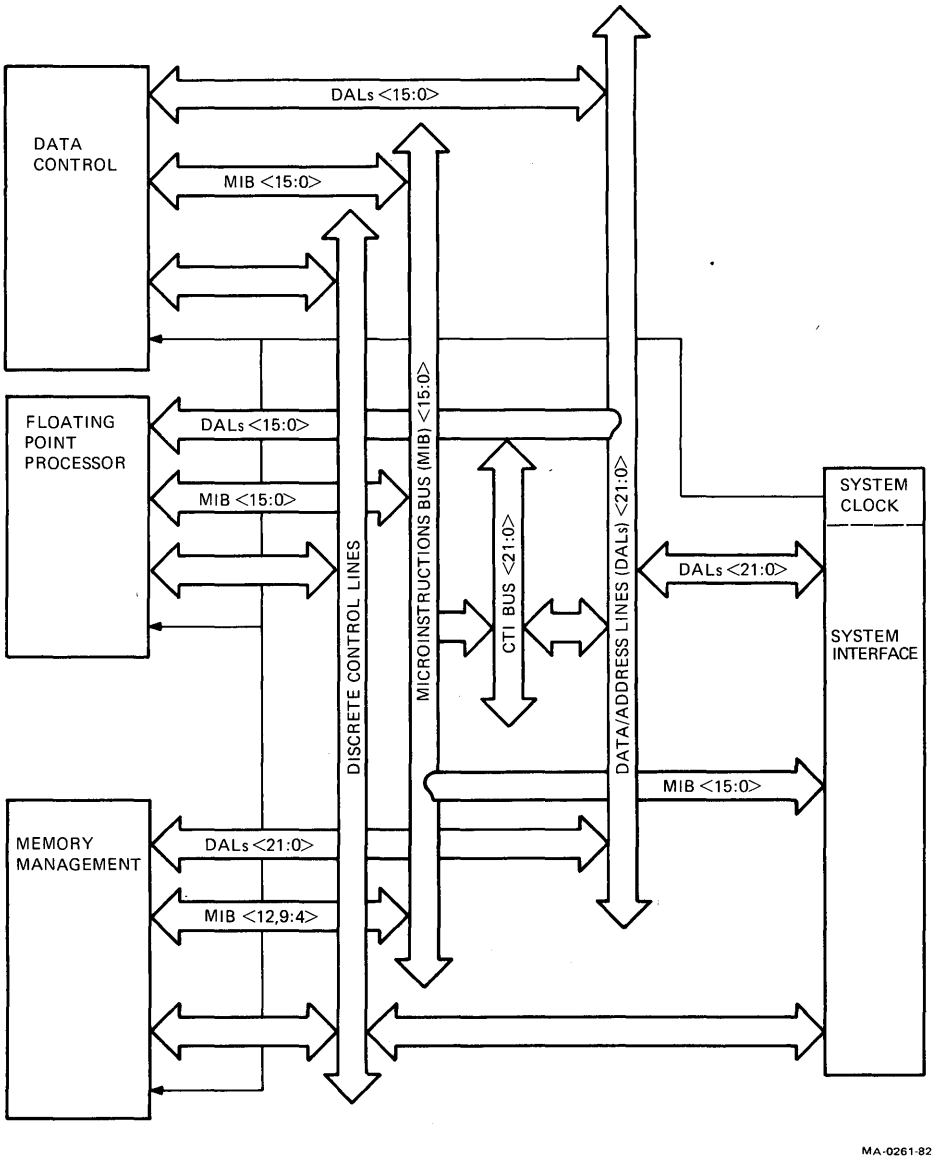


Figure 5-4 CPU Chip Set Communication

Table 5-1 Functional Summary of CPU Communication Buses

Clock-high Time		Clock-low Time
CDALs:	a macroinstruction, a 16-bit physical or virtual address, or numerical data	A relocated address, or service data
MIB:	control information	A microinstruction

To help clarify the preceding process, the following provides a detailed emulation of the CLR R0 macroinstruction.

PART I: MACROINSTRUCTION FETCH

Clk*	Data Chip	Control Chip
Low		Transmit ADR2 PC microinstruction on the MIB, (this instruction causes the value in the PC to address memory and increments the PC by 2.
↑	Latch ADR2 PC microinstruction from the MIB	
High	Execute address ADR2; put PC on the DALs, increment PC by 2, output discrete control signals	
↓		Latch control information from the MIB
Low		Transmit instruction input microinstruction on the MIB
↑	Latch instruction input microinstruction from the MIB	
High	Execute the microinstruction just brought in; input the CLR R0 macroinstruction from the DALs and output discrete control signals	
↓	Latch macroinstruction from the DALs	Latch macroinstruction from the DALs and control information from the MIB

* The terms in this column define the state of the clock line: low = clock voltage at a low, high = clock voltage at a high, ↑ = a rising edge, ↓ = a falling edge.

Low		Transmit CLR microinstruction on the MIB
↑	Latch CLR microinstruction from the MIB	
High	Execute CLR microinstructions; clear the register which is specified in the latched macroinstruction and transmit discrete control signals	
↓		Latch the control information from the MIB

The chip set now goes to service. On the next rising edge, the macro-level service data is clocked into the control chip from the CDALs. If no service is requested, the machine falls through to the macroinstruction fetch sequence. If service is requested, the appropriate service routine is begins.

If the CPU cycle is not an address relocation, the CDAL address bits 16–21 are pulled low.

5.3.1.3 Memory Management Interaction – When the MMU is used for memory management, it supplies the resources for 18 and 22-bit addressing. When added to the data chip/control chip system, it creates an additional communication situation. This occurs when an address needs to be relocated. The following sequence shows the address relocation.

Relocation Address Interchip Communication

Clk	Data Chip	MMU Chip
High (during execution of an address microinstruction)	Outputs the address on the CDALs and BSIO (a discrete control signal), outputs the the proper AIO codes (specific combinations of MIB lines) on the MIB.	Detects an address cycle by looking at the AIO codes, asserts a specific MIB line to indicate a relocated address cycle and inputs the address from the CDALs and BSIO.
	Latches the MIB line data for MMU chip; this tells the data chip that the MMU is relocating an address.	

Relocation Address Interchip Communication (Cont)

Clk	Data Chip	MMU Chip
low		Generates the relocated address and transmits it on the CDALs and BSIO.
↑	Latches the relocated address from the CDALs and BSIO to check for reference to the PSW.	Latches the internally relocated address to check for reference to any of the processor's registers.

If memory management is disabled, address cycles (a macrocycle) proceed as all other microcycles. If enabled, it adds three changes to the address cycles of the basic chip interaction. First, it changes when the address on the CDALs is valid. Instead of being valid towards the end of clock-high time, the address must be examined towards the end of clock-low time. Second, clock-low time must be lengthened from the minimum specified value for nonrelocated cycles. This allows the MMU time to operate. Third, to prevent a bus conflict, service cannot be on the DALs at the same time as a relocated address. The microprogramming prevents the chip set from loading service data during an address relocation. In addition, the system interface will not drive the DALs with service data at this time.

5.3.1.4 Floating Point Interaction – Floating point instruction capability is an option in the Professional 350 computer. The FP11 requires the MMU chip's floating point registers. These registers are indirectly addressed by the control field of the I/O microinstructions. The timing of the data transfers to and from these registers is the same as for any other I/O microinstruction. These transfers are transparent to the system user. Adding the floating point chips does not change the internal interaction of the system from earlier descriptions, for example, with and without memory management.

The microprogram handles control chip selection. A control chip deselects itself by executing an unconditional jump to another control chip. The target control chip decodes the jump microinstruction and selects itself. This executes the microprogram in a different part of the internal instruction set.

5.3.2 Instruction Cycles and Timing

The following paragraphs describe concepts of instruction and timing cycles used in the Professional 350. It does not explain the PDP-11 instruction set.

- Section 5.3.2.1 explains micro- and macroinstruction cycles.
- Section 5.3.2.2 explains the base system timing logic.
- Section 5.3.2.3 explains how teh system creates the needed timing signals.
- Section 5.3.2.4 explains how the MIB lines are decoded to start a cycle.
- Section 5.3.2.5 explains the CPU reset function.
- Section 5.3.2.6 explains the service register's timing between cycles.

5.3.2.1 Instruction Cycles – The chip set emulates PDP-11 macroinstructions with microprograms. This may require several microinstructions to do a single macroinstruction. Microinstructions use the system clock for synchronization. Macroinstructions require longer periods to execute that depend on the instruction performed. Macroinstructions use another internal clock, based on the first, for timing. The chip set tells its support circuits how much time is required and sets up the circuits to synchronize properly.

- Microinstruction Cycles
  The basic microinstruction cycle (Figure 5-5) shows common operations which occur every microcycle. The conditional latching of service data during a microinstruction cycle is controlled by the Next Address Field of the microinstruction being executed. As far as the system interface is concerned, it should place service data on the CDALs every clock-low time, except during address relocation cycles.

  During certain microinstructions, internal data is placed on the CDALs. This happens because the CDAL drivers are enabled every clock-high time unless an input microinstruction is being executed. During certain microinstructions this data is meaningful; for others the data is not used. As one microinstruction executed the next is accessed. This results in a faster execution of instructions.

  Microinstructions are not included in this manual because they are proprietary and confidential to Digital Equipment Corporation.

- Macroinstruction Cycles
  If service is pending, the appropriate service sequence is initiated. If no service is pending, a macroinstruction is fetched.

  Once a macroinstruction is fetched, the appropriate emulation microprogram is selected. After the completion of the emulation microprogram, the cycle begins again by first determining if service is pending.

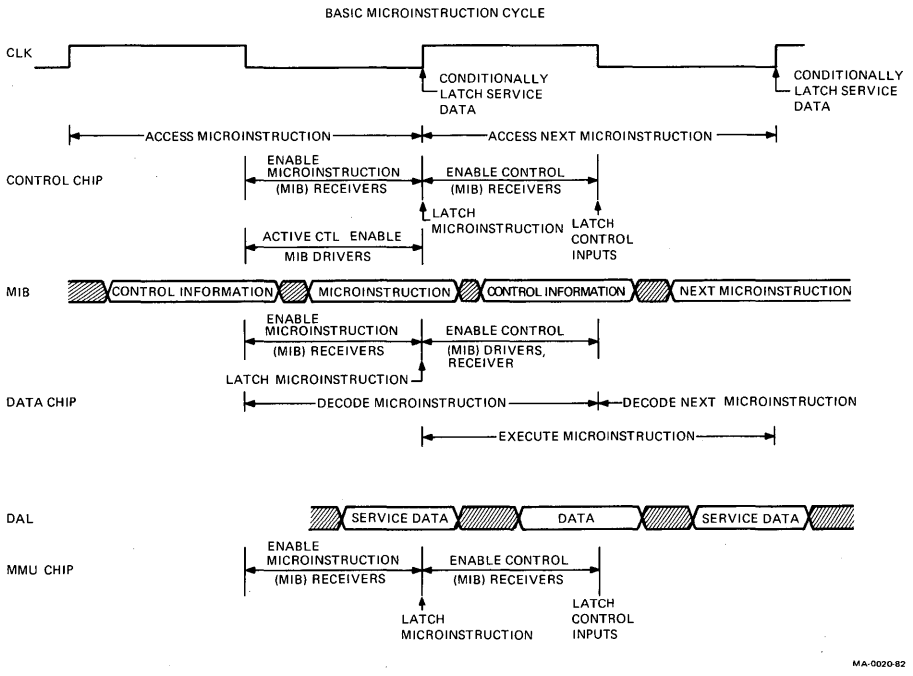


Figure 5-5 Basic Microinstruction Cycle

5.3.2.2 Basic Timing Logic – The microprocessor operates on microprogram data and instructions during the high and low periods of its clock. This section describes the system clock. The clock uses two signals, oscillator output (OSC H) and PHASE H, to synchronize the CPU and supporting logic. OSC is the system clock. PHASE is the CPU chip set clock.

The oscillator output (OSC H) is the system clock. It regularly sets certain circuits to allow data transfer. During CPU clock high time (PHASE H asserted), the data chip generates control information based on the current microinstruction and transmits this on the MIB. The microinstructions travel along the MIB during CPU clock low time (PHASE H not asserted). The control information on the MIB sets other circuits and determines the duration of PHASE. Depending upon the macrocycle, PHASE H and PHASE L remain high or low for specific multiples of OSC. These two clocks, along with other control information, direct the path and timing for data flow.

Three MIB lines states indicate the present type of CPU cycle. See Table 5-2. The control circuitry reads the MIB lines and sets timing circuits for PHASE. PHASE's duration, then, varies depending upon the status of the MIB lines.

Each microcycle may be an address cycle, a data write, or other operations shown in the table. A read-modify-write cycle to memory requires several different PHASE periods. PHASE stays high depending upon which devices are communicating. It may be kept high for two, three, five, or more clock cycles depending on the kind of microcycle. PHASE may be kept high while waiting for a reply from any addressed device and may be kept high indefinitely waiting for DMA. PHASE can be low for two, five, or six clock cycles, again depending on the type of microcycle. If PHASE is kept low longer than six clock cycles, the CPU chips may lose data from lack of refresh. Table 5-3 describes the three basic microcycles.

By coordinating PHASE with OSC, the latches and buffer chips are ready to load address or data information. It is necessary to synchronize times for set up, hold, and release because of buffer chip parameters and bus specifications.

Example – MIB control information and OSC H produce a sequence of timing signals (including PHASE). The number of signals depends on the type of cycle to be run. Figure 5-6 shows a timing diagram for an address relocation cycle. This operation requires three clock periods high and five low. Note the system clock, OSC, is a periodic signal.

1. PHASE goes high at OSC H rising edge. As PHASE H goes high, its complementary output, PHASE L, goes low. This starts the following timing signal sequence and clears a second timing sequence.

2. At the next OSC H rising edge, Phase Time 2 (PT 2) goes high.

3. At the next OSC H, PT 3 goes high.

4. At the next OSC H, PHASE goes low and PHASE-BAR goes high. PT 2 and PT 3 go low. However, PT 4 was clocked in just as the input signals went low so that PT 4 H appears as a spike impulse.

5. As PHASE L goes high, it starts a similar sequence of timing signals during PHASE-BAR.

Table 5-2 System Set Up for Instruction Cycle

MIB AIO 12 2	9 1	8 0	Name	Microinstruction Invoked by	Meaning
0	0	0	AWO	Address	During this cycle, the data chip transmits an address. A data write only operation.
0	0	1	ARW	Address	During this cycle, the data chip transmits an address. A data read modify write operation.
0	1	0	–	Unused	
0	1	1	ARO	Address	During this cycle, the data chip transmits an address. A data read only operation.
1	0	0	WRITE BYTE	Output	The data chip performs a byte output operation. During this cycle, the data chip transmits a data byte. If the address is even, the data is be on the low byte of the DALs. If the address is odd, the data is on the high byte. In both cases the non-data byte is unpredictable.
1	0	1	WRITE	Output	The data chip performs a word output operation. During this cycle, the data chip transmits a word of data.
1	1	0	READ	Input	The data chip performs an input operation. During this cycle, the data chip reads a word of data.
1	1	1	NOP	All except Address, Input, or Output	Data chip not performing an I/O operation (neither data in nor data out operation).

* These control signals are forced to NOP (AIO = 7_8) if an input or output microinstruction is executed when the explicit PS address mode is active (for example, if the PS is referenced by its I/O address, the input and output AIO codes are overridden to the NOP AIO code). This information is needed by the control and MMU chips.

Table 5-3 Microcycles

Cycle Description	Cycle Steps
Read Only	ARO, READ
Write	AWO, NOP, WRITE* or WRITE BYTE*
Read-Modify-Write	ARW, READ, NOP, WRITE* or WRITE BYTE*

* The AIO code determines if this is a byte or word operation. Address A00 determines the high or low byte if it is a byte operation.

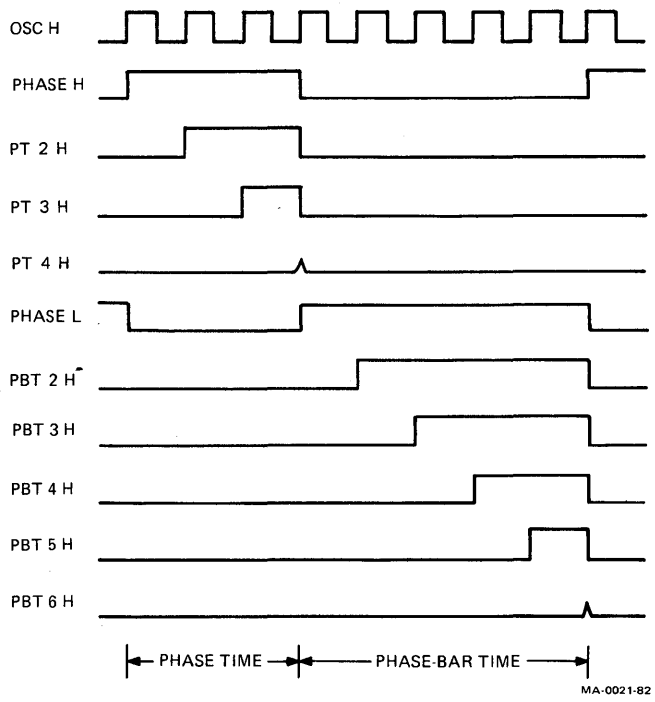


Figure 5-6 Address Relocator Cycle

6. At the next OSC H, PHASE-BAR TIME 2 (PBT 2 H) goes high.
7. At each of the next three OSC H signals, PBT 3 H, PBT 4 H, and PBT 5 H go high respectively.
8. At the sixth OSC H, PHASE-BAR goes low as PBT 6 H appears as a spike impulse.
9. The signals now are PHASE H and PHASE-BAR L.
10. PT 4, PT 5, PT 6, and PBT 6 are not generated during this cycle.

The next section describes how these signals are generated.

5.3.2.3 Detailed Timing Logic – A 26.666 MHz crystal oscillator output is divided by two and buffered to drive the timing logic for the CPU, the CTI BUS control logic, and the DAL Bus control logic. This signal, OSC H, has a period of 75 ns. Figure 5-7 shows the signals used for system timing.

The clock driver uses the PHASE H flip-flop output to produce the +12 V CPU chip set clock signals (CHIP CLKA H and CHIP CLKB H). Each chip set clock cycle consists of a PHASE time (PHASE H set) and a PHASE-BAR time (PHASE H clear). The CPU chip set is semi-static and loses information if it remains in PHASE-BAR time longer than 500 ns. However, it can remain in PHASE time indefinitely. PHASE and PHASE-BAR are complementary.

Two shift registers (PT 2 H through PT 5 H and PBT 2 H through PBT 6 H) operate as clock signal timers during PHASE time (PT) and PHASE-BAR time (PBT) respectively. PT means PHASE TIME and PBT means PHASE-BAR-TIME. If PHASE H is set, but PT 2 through PT 5 are clear, the logic is in phase time one. If PHASE H and PT 2 are set, but PT 3 H through PT 5 H are clear, then the logic is in phase time two. Similarly, if PHASE H is clear and PBT 2 H through PBT 5 H are clear, the logic is in phase-bar time one. If PBT 2 H through PBT 4 H are set, but PHASE H and PBT 5 are clear, then the logic is in phase-bar time four.

The PHASE H flip-flop and the two shift registers are clocked on the leading edge of OSC H. When PHASE H is set, the logic advances from one phase time to the next in sequence. However, there is one exception: the logic pauses in phase time one if DMA is in process.

When PHASE H is clear, the logic advances from one phase-bar time to the next. Usually it advances from PBT 2 to PT 1. However, there are two exceptions:

- During address relocation cycles, the logic enters PHASE after PBT 5.
- During a reset of the CPU chip cycle, the logic enters PHASE after PBT 6.

A clearing signal clears the flip-flops, which gate data onto the CDAL lines during PHASE time. That data must remain there for one-half OSC period into PHASE-BAR time. The phase time clearing signal clears the flip-flops, which gate data onto the CDAL lines during PHASE-BAR time. That data must remain there for one-half OSC period into PHASE time.

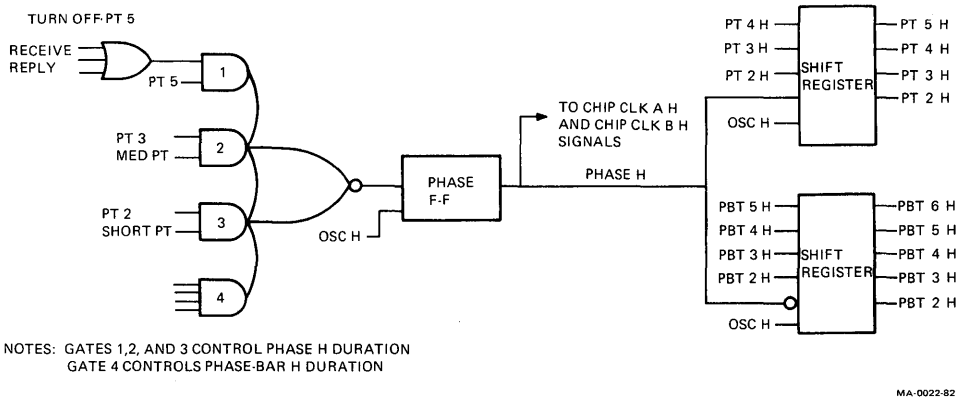


Figure 5-7 Phase Signal Duration Functional Diagram

5.3.2.4 MIB Decode Logic – During PHASE-BAR time, the MIB lines contain the current microinstruction provided by one of the CPU control chips (Table 5-2). During PHASE H time, the MIB lines contain control information provided by the CPU data chip. The system logic monitors some MIB lines during PHASE time and some at the end of PHASE time.

During PHASE Time, the MIB lines 12, 9, and 8 contain the address input/output signals (AIO 2, 1, and 0). The AIO codes are decoded to determine whether the current cycle is an address cycle, a bus type data in cycle, or a bus type data out cycle. The AIO lines are signals which determine whether the logic enters PHASE-BAR time after PT 2 (SHORT PT H), after PT 3 (MED PT H), or after PT 5 (SHORT PT H and MED PT H both clear).

At the end of PHASE time, PHASE H clocks the following MIB lines into flip-flops.

- MIB 15 H to REL CYC H if a memory relocation cycle is indicated.
- MIB 12 H inverted to LAD CYC L for an address cycle.
- MIB 07 H inverted (SYNCF H) to LSYNCF L to synchronize the address on the bus.
- MIB 14 H to INIT H to initialize the system whenever a reset instruction occurs or at power up.

5.3.2.5 CPU Chip Reset – The CPU can remain in PHASE H time indefinitely; PHASE L can remain no longer than 6 clock cycles before data may be lost. Table 5-4 shows error conditions which could cause the CPU to be reset. If one of these errors occur, the system logic generates a reset signal which extends PHASE-BAR time to 6 clock cycles. Reset enables the CPU service register so the CPU can determine which error condition caused the reset.

Table 5-4 Reset Conditions

Signal	Meaning
DCOKC 3 L	DC voltage is OK and present for at least 3 clock cycles. This is a normal condition that causes reset on power up.
BUS ERROR H	The processor put out an address on the bus but there is no response from the device.
NO CSEL H	Neither control chip (CPU nor FPP) is active.
MER H	Bus memory error.
ABORT L	MMU chip tried to address an invalid address.

5.3.2.6 Service Register – Service information is system status information. The CPU uses this to monitor the conditions shown in Table 5-5. The service information is enabled on the CDAL lines when not doing address relocation when PHASE H is low or during a chip reset. Logic circuits turn on the drivers that place the service data on the CDAL bus for the CPU to read directly.

5.3.3 Buses

Both 16-bit addresses and 8-bit data bytes or 16-bit data words are multiplexed over bus data/address lines. During a programmed data transfer, the processor asserts an address on the bus for a fixed time. After the address time is completed, the processor initiates the programmed input or output data transfer. The actual data transfer is asynchronous and requires a reply from the addressed device. The bus synchronization and control signals provide this function.

The bidirectional and asynchronous communications on the buses allow the devices to send, receive, and exchange data at their own rates. The bidirectional nature of the bus allows use of the common bus interfaces for different devices.

Communication between two devices on the bus is a master-slave relationship. At any point in time, there is one device that controls the bus. This device is the bus master. The master device controls the bus when communicating with another device on the bus, the slave. An example of this relationship is the processor, as master, fetching an instruction from memory (which is always a slave). Another example is a DMA device interface, as master, transferring data to memory, as slave. Bus master control is dynamic. The bus arbitrator is the processor module.

Since the CTI BUS is used by the processor and all I/O devices, a hardware priority structure determines which device becomes bus master when more than one device requests control of the bus. Every device on the CTI BUS which is capable of becoming bus master is assigned a priority according to its function or type. If two devices of the same priority level each request the bus at the same time, the device in the lower slot number becomes the bus master.

Table 5-5 Service Register

Signal	Meaning
DCOKC 3 L	DC voltage is OK and present for at least 3 clock cycles. This is a normal condition that causes reset on power up.
TIME OUT H	No response received after putting an address on the bus
MER L	Bus memory error
ABORT L	MMU chip tried to address an invalid address
CTL ERR L	Neither control chip (CPU nor FPP) is active
HALT H	Octal debugging technique signal to start or stop single step operation
PWRFL H	Power failing
IRQ 4 H	Interrupt request

Data transfers on the CTI BUS are asynchronous; communication is independent of the physical bus length and the response time of the slave device. The asynchronous operation between bus master and slave devices depends upon synchronizing the bus transactions with clock signals. This allows each device to operate at the maximum possible speed.

Full 16-bit words or 8-bit bytes of information can be transferred on the bus between a master and a slave. The information can be instructions, addresses, or data. For example, this type of information transfer occurs when the processor, as master, fetches instructions and operands and transfers data to and from memory.

Refer to Figure 5-4 for a simplified diagram of the buses and Figure 5-8 for a complete system block diagram showing interfaces. Figure 5-9 shows the buses without other functions. The following paragraphs describe each major bus.

Microinstruction Bus (MIB)
The 16-bit MIB is common to all data and control chips. The MMU receives a subset of the MIB because it does not need access to all MIB control signals. A different subset of the MIB controls the processor support logic.

The MIB is time multiplexed and is used for different functions during clock high and low times. During clock high time, the MIB transfers control information from the data chip to all control chips, the MMU, and the board logic. During clock low time, the MIB transfers microinstructions from the active control chip to other control chips and the data chip.

Data/Address Line Bus (DAL)
The DAL interconnects all the MOS chips and buffers on the processor board. The 22-bit DAL bus is time multiplexed. Of the 22, the CPU uses six lines for addressing only. During clock high time, the data chip transfers information to or receives information from the other chips along the DAL. During clock low time, the board transfers service data (such as interrupt requests) along the CDAL bus to the control chip. The control chip receives service information and determines whether to trap or fetch the next instruction. During clock low time or during address relocation, the relocated address from the MMU transfers to the DAL bus.

Computer Terminal Interconnect Bus (CTI)
The CTI BUS is the control path for the CPU and all options modules. It is also the Professional 350 backplane. The six option slots mounted on the system module connect to the 90-signal bus. All signals are bused to all six slots with the exception of six signals. These six slot dependent signals are on the system module for address decoding, interrupts, and DMA. These signals are as follows.

- Option present indicator
- Slot select from the I/O page address decoder
- Two interrupt request lines (A, B) from each option
- DMA request from the option
- DMA grant from DMA arbitration circuits

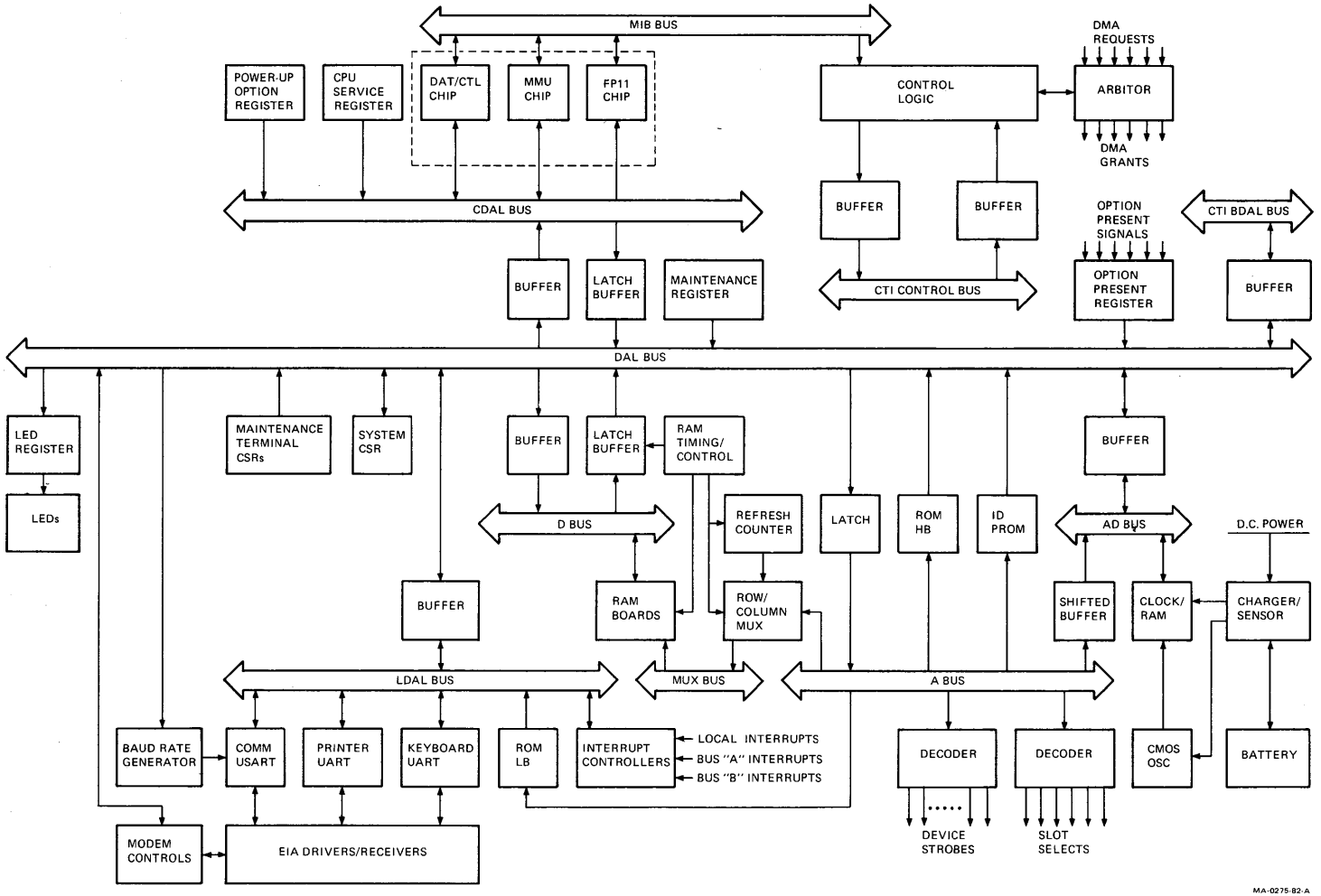


Figure 5-8 System Module Block Diagram

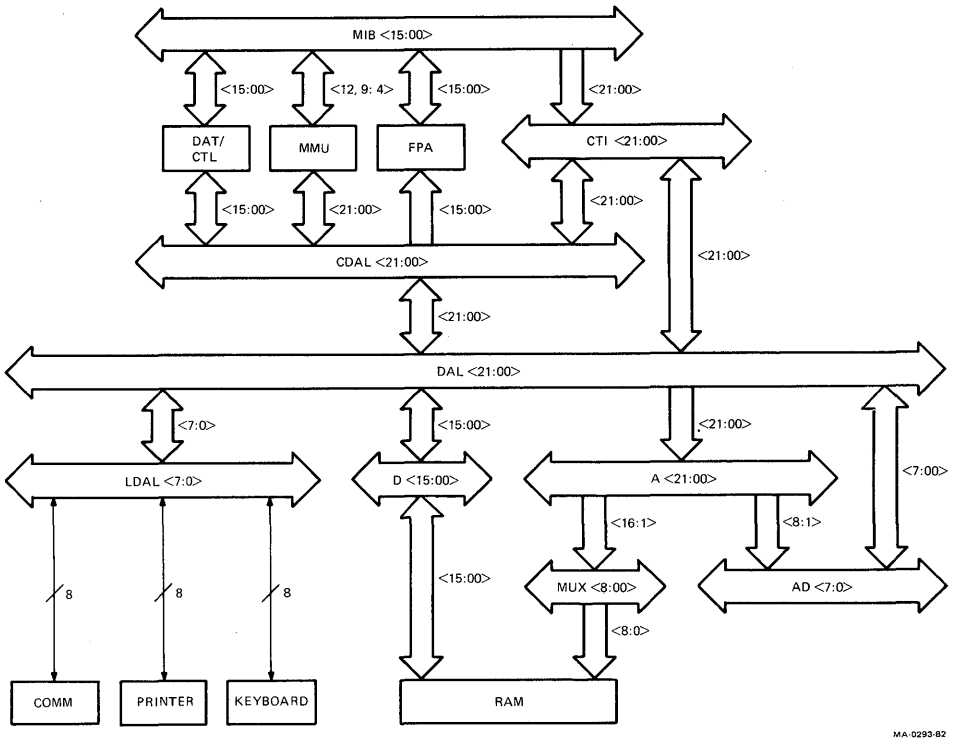


Figure 5-9 Professional 350 System Module Bus Scheme

Each option slot has a 90-pin connector on the system module. The first 60 pins are used for the CTI BUS signals. These are referred to as the general section of the bus. This section of the bus is control lines and bused data/address lines (CTI/BDAL). The last 30 pins, 61 through 90, route signals from the option modules to connectors on the rear of the system module. These are referred to as the private section of the bus. An option module that only needs the CTI BUS signals can use a 60-pin Zero Insertion Force (ZIF) connector. An option module that uses the rear connectors on the system module must use a 90-pin ZIF connector. Section 5.3.5.2 describes the bus timing relationships. Refer to Section 5.5 and Table 5-30 for the CTI BUS signal definitions.

D Bus

The D bus is the data path to and from the externally mounted RAM daughterboards. Data from the DAL bus can be written to RAM via the D bus when the WRITE signal is asserted and then written directly to the daughterboards. A RAM read causes data to be latched from the D Bus into three-state latches for release to the DAL bus. The RAM modules are addressed via the A Bus.

A Bus

The CPU and DMA devices use the A Bus to address all I/O devices and memory. Addresses are latched from the DAL bus and held until the bus cycle is completed. Logic uses the A Bus to activate device strobes, slot selects, ROM, registers, and RAM addressing.

AD Bus

This bus accesses the battery backed up clock chip. It also permits battery backed up RAM addressing and data transfer. This is a low byte only bus. Refer to Section 5.3.4.1 for further information.

LDAL Bus
This bus is the low driver data/address bus. It is the system's interface to devices with low drive outputs: the keyboard, printer, and communications ports. It also carries interrupt vectors to the CPU from the interrupt controller chips. It carries low drive signals to a TTL buffer which drives the DAL bus. It is a low byte only bus.

CDAL Bus
The CDAL bus is an interface bus between the CPU chips and the DAL bus. The CPU chips have low output drive and would be loaded down by the DAL bus and its interface logic.

MUX Bus
The MUX bus carries address data from the A Bus to the RAM daughterboards. Quad 2:1 multiplexers transmit first the low, then the high bytes of address data to the RAMs. Refresh address for the RAM also uses the MUX bus. The system module can support up to 512 kilobyte per daughterboard slot using a ninth address line.

5.3.3.1 Bus Reply – All bus cycles require the enabled device to reply, whether it is a local (system module) or CTI BUS device. The CPU stops in PHASE time and waits for a reply. The reply ends PHASE time. Figure 5-10 shows the reply signals and the signals that enable them. Each device needs a different time to reply which depends on its speed. Therefore the device determines when PHASE ends via its reply time.

If PT 4 H is asserted, the CPU is on the bus and a DMA device cannot use the bus. If PT 4 H is sent, there are 6.5 μs for a device to reply. If no reply comes, a timer times out and asserts the reply signal. The reply ends PHASE time but indicates a timeout error to the CPU.

5.3.3.2 Other Bus Control Signals – Other signals which control data flow on the CTI BUS and internal buses are the following.

- ADDRESS STROBE – Occurs on OSC L. Refer to Figure 5-11.
- DATA STROBE – Occurs on OSC H. Refer to Figure 5-11.
- MDEN – Master Drive Enable indicates that the master is placing an address or data on the bus. Refer to Figure 5-12.
- SDEN – Slave Drive Enable indicates that a slave should drive data on the bus. Refer to Figure 5-12.

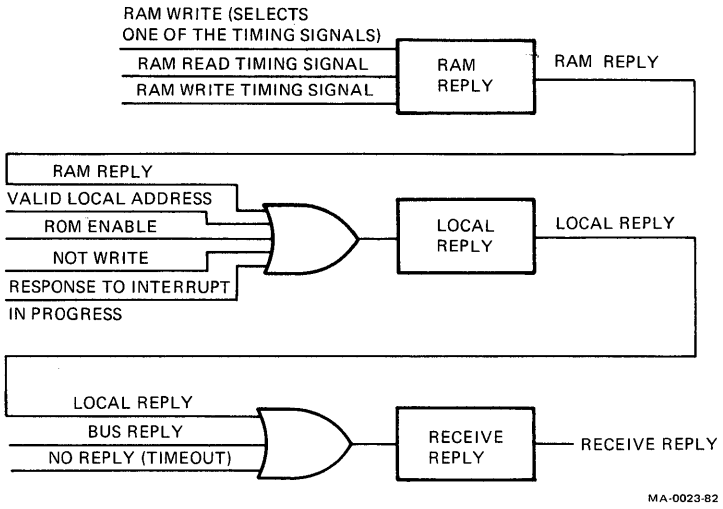


Figure 5-10 Reply

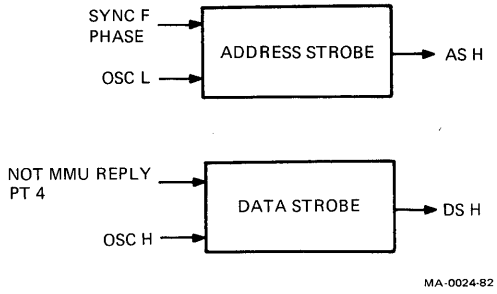


Figure 5-11 Address and Data Strobe

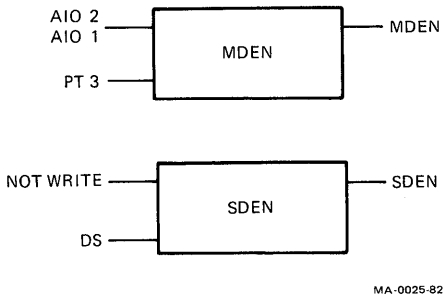


Figure 5-12 Master and Slave Drive Enable

5.3.4 Bus Interfaces

Bus interfaces in the Professional 350 fall into two categories, buffers and registers. Buffers isolate electrical circuits from each other. For example, a buffer permits passage of data on one bus to another to meet device drive or timing requirements (Section 5.3.4.1).

Registers hold status information for the CPU to read. They transfer their data directly to the appropriate bus when addressed and enabled (Section 5.3.4.2).

5.3.4.1 Buffers – There is an interfacing buffer between each pair of buses. These buffers switch a data path to and from different circuits according to CPU instructions and the timing requirements of different circuits.

Although buffers switch signals, they can also change drive level requirements depending on the requirements of the devices they serve.

Figure 5-13 shows the system block diagram with only buses and buffers. Each buffer on the figure has a number which corresponds to the following numbered paragraphs. These paragraphs describe buffer's function. Figure 5-13 also shows the enabling signals and the transceivers that change the buffers' direction.

1. CDAL – DAL Buffers – Signals from the CPU on the CDAL bus are always passed as 16 bits. They are clocked into latch buffers at the first OSC L rising edge during PT 3 H or at the rising edge of PBT 4. The CPU enables output to the DAL bus when it becomes bus master. This places either an address or data on the bus.

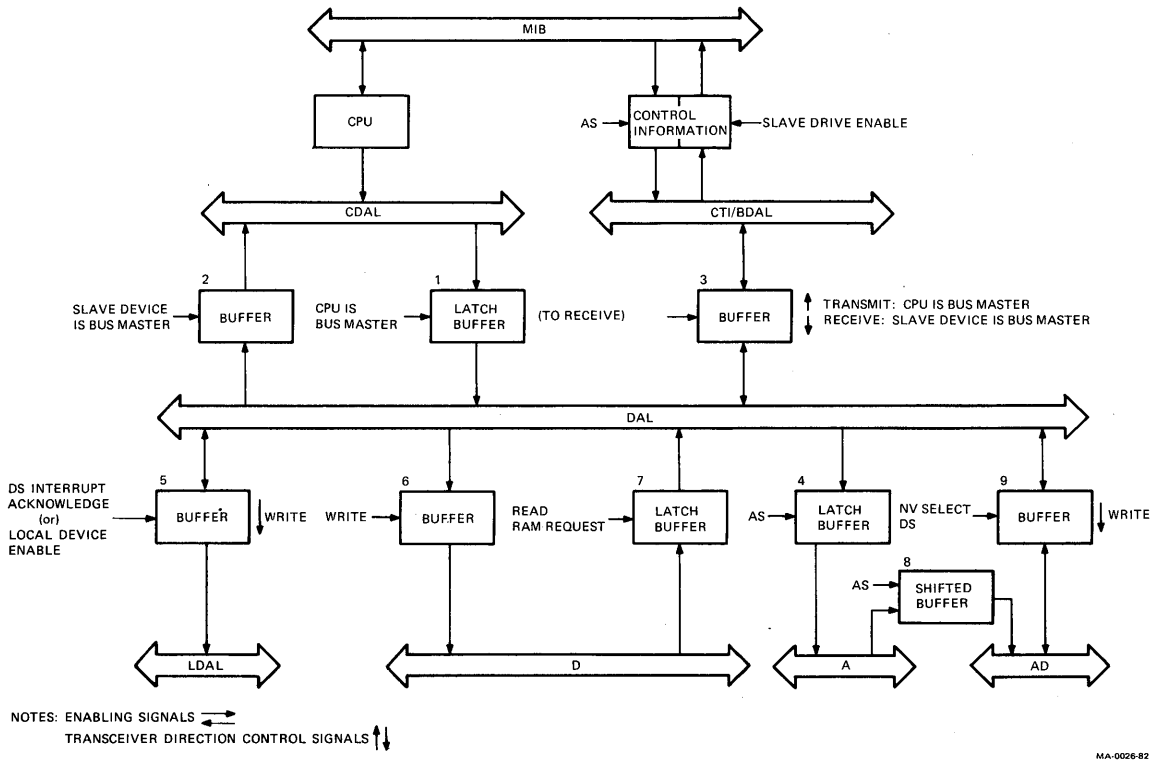


Figure 5-13 System Block Diagram with Bus Interfaces

2. DAL – CDAL Buffers – This buffer permits data from the DAL bus to be gated onto the CDAL bus and to the CPU chip set. The signals are clocked in on the falling edge of the PHASE H signal.

3. DAL – CTI/BDAL Buffer – This buffer consists of three octal bus transceivers between the DAL and CTI/BDAL buses. The CTI/BDAL bus connects the DAL bus to all slots on the CTI BUS. The CPU transmits address to the DAL bus in 22-bit words. Data to or from the CTI/BDAL bus is transferred in 16-bit words (BDAL 15:00)

4. DAL – A Bus Address Latches – Latch buffers transfer addresses on the DAL bus to the A Bus. All DAL lines and BSIO in DMA devices must assert 22-bit addresses and BSIO. The master also uses 22-bits at address strobe time. The chips in this circuit require set up time for the addresses to stabilize on the bus before latching them.

5. DAL – LDAL Buffer – This buffer uses an octal transceiver to transmit eight bits of data. The LDAL, a low drive bus, connects to devices that provide low drive. The buffer amplifies these devices; signals and puts the signals directly on the DAL bus.

6. DAL – D Buffer – Data for RAM on the DAL bus is written to the D Bus during write operations. The data is then transmitted directly to the RAM chips.

7. D – DAL Buffer – Data in RAM is available after addressing. The data is latched in tri-state latch buffers when a valid RAM request is made. A RAM read signal enables the output. This places the data on the DAL bus.

8. A – AD Buffer – This shifted buffer passes address data (A08 – 01) to access RAM and registers in the battery backed up clock/RAM circuit. A08 – 01 are used because the address bit A00 normally selects high or low byte data. Since this circuit is a low byte device, A00 is not used by the chip. Therefore the address is shifted one bit to A08 – A01 instead of A07 – 00. The address is valid at the address strobe signal.

9. DAL – AD Buffer – This octal bus transceiver permits data transfer to and from the battery backed up clock/RAM circuit. It is enabled by the address decoder and data strobe signals.

5.3.4.2 Registers – Registers hold status information or other information needed for data processing. Certain interrupt data, power level data, and system configuration data are examples of the kinds of data stored in registers.

Figure 5-14 shows the system block diagram. Each register on the figure has a number which corresponds to the following numbered paragraphs. These paragraphs describe each register's function.

1. Power Up Option Register
   This register, on the CDAL lines, is an octal tri-state buffer. It is read at power up to make the CPU go to an address in the system ROM (17760000) and begin executing the code there to start the power-up self-test.

2. CPU Service Register
   This register stores information about power, errors, and interrupts. Refer to Section 5.3.2.6 for a list of service register functions.

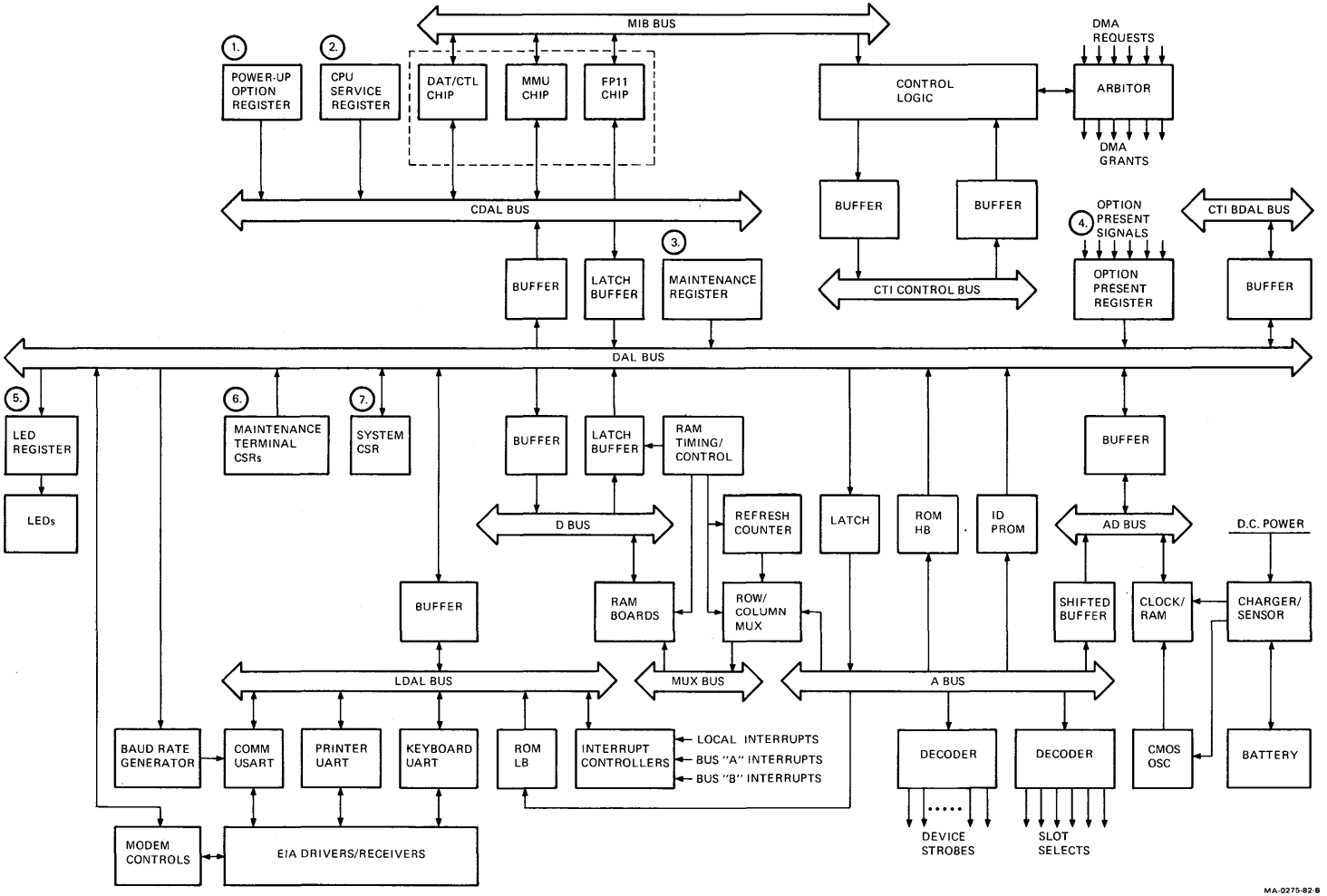


Figure 5-14 System Block Diagram with Register

3. Maintenance Register (Address 17777750)
This register tells system software the type of CPU and hardware configuration. The software can then configure itself to the hardware configuration.

When the computer is booted, the operating software asserts address 17777750. The address decoder asserts the signal LREPLY H and the CPU waits for a response. Since 17777750 is an invalid address, there is no response. This means that no device is driving the bus. The software then reads the bus (which is all low) and interprets this to mean a Professional 350 computer.

4. Option Present Register (Address 17773702)
A hardwire in each option module pulls a line low when it is inserted in its slot. These assert the signals OPRES 0 through 5 L.

When the CPU needs to determine which slots are used (to determine address ranges), it puts this register's address on the A lines. When decoded, it asserts RD OPRES L. RD OPRES L enables the register and puts the data on the DAL lines. The buffer control signal SDEN L permits the buffers to transfer the data to the CDAL lines which connect directly to the CPU data chips.

5. Indicator (LED) Register (Address 17773704)
This LED register is a system status indicator. There are five LEDs on the back of the system module (one green and four red LEDs). The green LED lights when the power supply asserts the DCOK signal. The four red are error indicators used by the power-up self-test. Table 5-6 indicates the error condition for each LED code.

The LED display register uses only the first four bits of the low byte. It controls the state of the four red LEDs on the rear of the unit. The register is reset at power up. (At power up, all four red LEDs are on.) The first error is latched and held and the LED display indicates the error found. Otherwise the register is always read as all zeros. All writes to the high byte have no effect.

Figure 5-15 shows the positions of the LEDs if viewed from the back of the unit.

6. Maintenance Terminal Control and Status Register (Address 17777560–17777566)
A console terminal can be connected to the system through the printer port for maintenance debugging and testing. The console terminal interface is made of four registers at addresses 17777560–177777566. The microcode Octal Debugging Technique (Micro-ODT) accepts 16-bit addresses which permits addressing 56 kilobytes of memory plus the 8 kilobytes I/O page.

7. System Control and Status Register (CSR) (Address 17773700)
This register tells the CPU which memory module(s) is (are) present (0 and/or 1) and the size (128 kilobytes). It also tells if a monitor cable is connected to the system. The register also enables or disables the break detect from the printer interface.

The CPU puts this register's address on the A lines, which when decoded asserts RD STATUS L. RD STATUS L enables the register and puts the data on the DAL lines. The buffer control signal, SDEN L, allows the buffers to transfer the data to the CDAL lines which connect directly to the CPU data chips.

Table 5-6 Indicator (LED) Error Codes

LED 3	LED 2	LED 1	LED 0	Error Condition
off	off	off	off	None – self-test found no errors
off	off	off	on	Bus slot 0 error detected (physical slot 1)
off	off	on	off	Bus slot 1 error detected (physical slot 2)
off	off	on	on	Bus slot 2 error detected (physical slot 3)
off	on	off	off	Bus slot 3 error detected (physical slot 4)
off	on	off	on	Bus slot 4 error detected (physical slot 5)
off	on	on	off	Bus slot 5 error detected (physical slot 6)
off	on	on	on	Invalid – reserved
on	off	off	off	Invalid – reserved
on	off	off	on	Keyboard failed
on	off	on	off	No boot found
on	off	on	on	Monitor cable not present
on	on	off	off	Memory in slots 0 and 1 both failed
on	on	off	on	Memory in slot 1 failed (low bank)
on	on	on	off	Memory in slot 0 failed (low bank)
on	on	on	on	System module failed*

* All the LEDs are lit at power up (lamp test). If they all remain lit, a system module error is indicated.

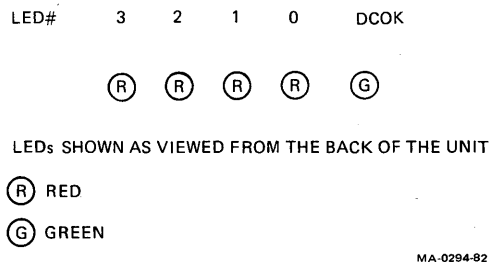


Figure 5-15 Indicator (LED) Display

5.3.5 Other Control Logic

This section describes the control logic used to select or enable devices on the system module or on the CTI BUS.

5.3.5.1 Slot Select Decoder – The slot select decoder uses addresses and selection signals to enable different slots on the CTI BUS. It asserts a slot select signal (SS n L).

During clock high time of a memory management address relocation cycle, the MMU chip determines if the address the CPU control chip puts out is in the I/O page range (17760000–17777776). During clock low time, if it is in the range, the MMU chip puts out a relocated address on the CDAL bus and enables BSIO H. BSIO H is asserted as BIOSEL L on the CTI BUS and is latched with BSIO and the A Bus address. Latched BSIO H is LBSIO H which, along with A bus signals A 12:10, enables the slot select decoder. The decoder uses address lines A 9:7 to assert the slot number selection. Table 5-7 provides each slot's address assignments. Address assignments depend on slot number, not device type.

5.3.5.2 I/O Page Address Decoder – The I/O Page Address Decoder is a local device address decoder. It is a programmable logic array (PLA) that recognizes device addresses and enables the corresponding circuit. For example, if an address for battery backed up RAM is on the bus, the decoder asserts a battery backed up RAM enable.

When an address is on the bus, all devices read the address but only the enabled devices can react to it. The decoder decodes addresses and enables devices for data transfer. System logic coordinates the data flow on the buses. It opens the appropriate buffers at the right times to permit reading addresses and data and holds buffers and latches for specified times. System logic uses the system clock and timing signals generated by PHASE time.

The following are examples of data flow. Refer to Figure 5-13 for each of the examples. This figure shows the system block diagram with bus interfaces only. In addition, each example refers to an illustration that shows the system block diagram and the address and data flow. Table 5-8 shows the system memory map with addresses.

Table 5-7 Slot Select and Address Ranges

Slot	Address Range
0	17774000–17774177
1	17774200–17774377
2	17774400–17774577
3	17774600–17774777
4	17775000–17775177
5	17775200–17775377

Table 5-8 System Module Memory Map

00000000-????????*	RAM – main memory
17730000-17767776	16Kb ROM – diagnostic/boot
17772300-17772316	MMU – kernel PDRs
17772340-17772356	MMU – kernel PARs
-17772516	MMU – SR3
17773000-17773032	Clock registers
17773034-17773176	Battery Backed-up RAM – 50 bytes
17773200-17773212	Interrupt controller registers
17773300-17773314	Communication port registers
17773400-17773406	Printer port registers
17773500-17773506	Keyboard registers
17773600-17773676	ID PROM
-17773700	System CSR
-17773702	Option module present register
-17773704	Indicator (LED) display register
17774000-17774176	Option module slot 0
17774200-17774376	Option module slot 1
17774400-17774576	Option module slot 2
17774600-17774776	Option module slot 3
17775000-17775176	Option module slot 4
17775200-17775376	Option module slot 5
17777560-17777566	Maintenance terminal registers
17777572-17777576	MMU – SR0, SR1, SR2
17777600-17777616	MMU – user PDRs
17777640-17777656	MMU – user PARs
-17777750	Processor maintenance register
-17777776	Processor PSW

* Upper address limit depends upon the amount of RAM the system is configured with. All addresses are 22-bit octal format. The system module supports addressing up to 1 megabytes; the system supports up to 3 megabytes.

Example 1 – CPU Writing to I/O Device (Refer to Figure 5-16).

- The CPU indicates it is to be bus master and latches the address into the CDAL-DAL latch buffer. This puts the address on the DAL bus. Address strobe also transfers the address to the A bus. System control logic decodes microinstructions on the MIB bus to generate necessary control signals.

- The address decoder decodes the address and, if valid, enables the device (here the printer USART). The ROM, RAM, and slot address decoders also read the address but do not enable because the address is invalid for their devices.

- On data strobe, the DAL-LDAL buffer transfers data to the LDAL bus and to the printer USART.

  Although Example 1 shows writing to an I/O device, the signals are also asserted on the CTI BUS. Since no device on the bus was addressed (slot select), the bus devices do not respond. The address decoder responded to the address, enabling the printer USART. Figure 5-17 shows a simplified bus timing relationship for signals on the CTI BUS.

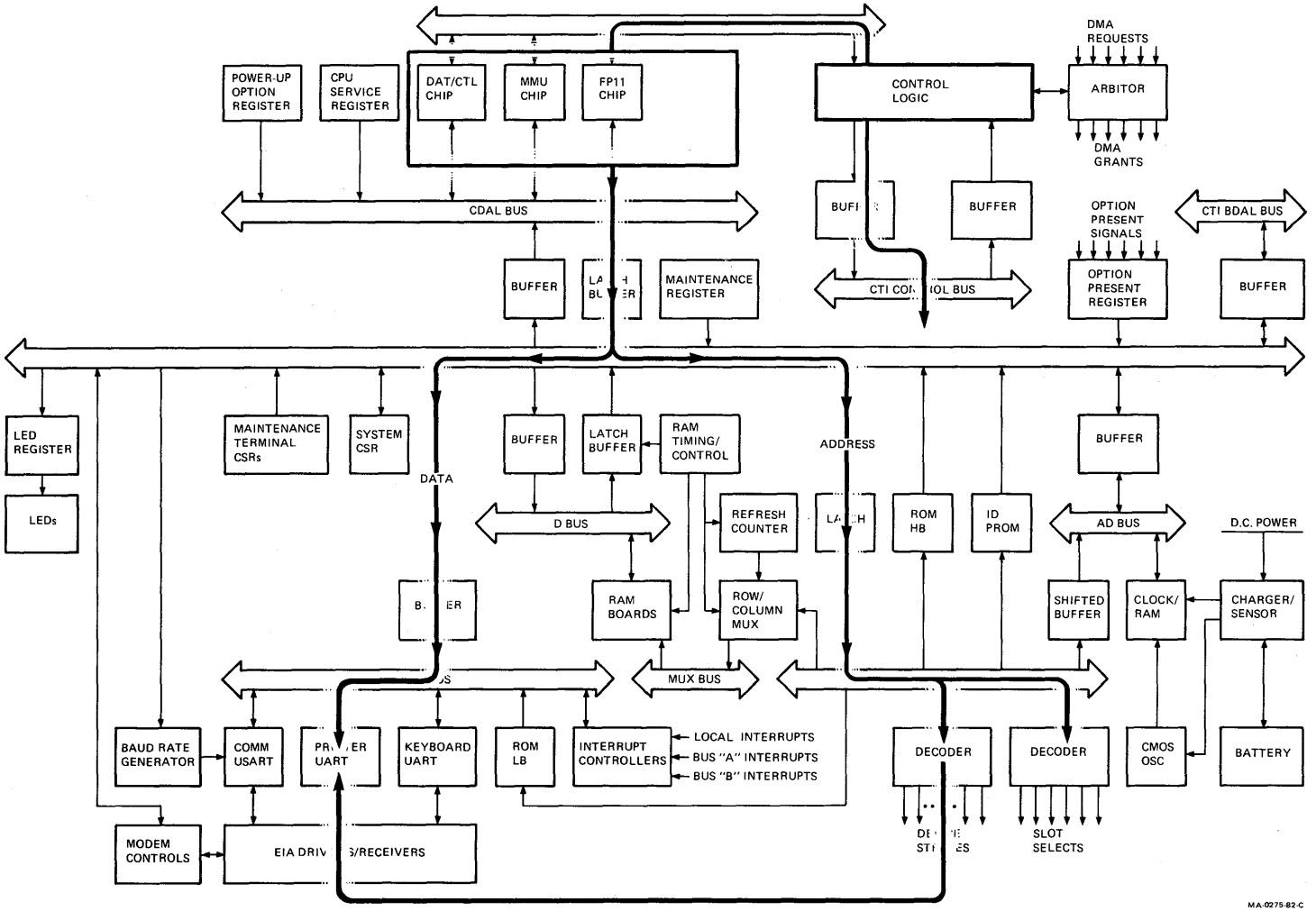


Figure 5-16 CPU Writing to I/O Device

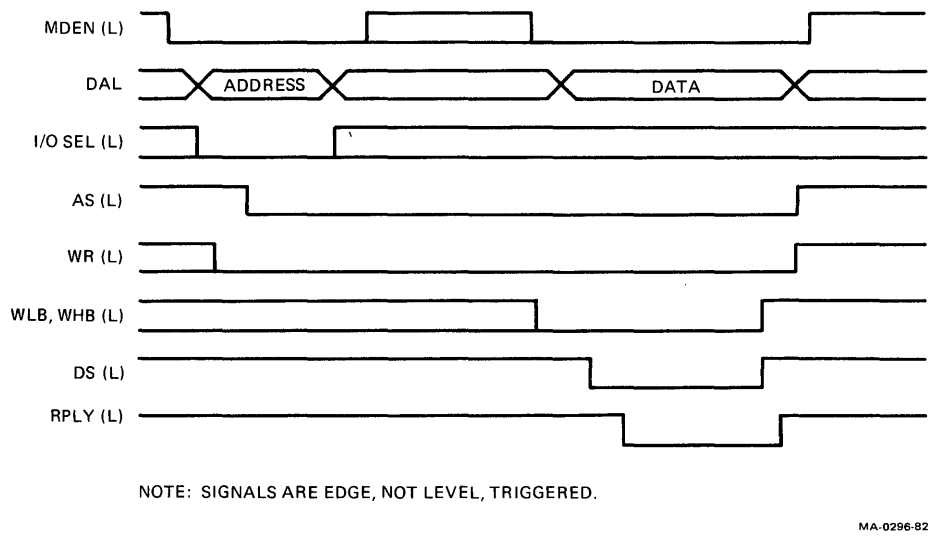


Figure 5-17 Simplified CTI BUS Timing Relationships During Write Cycle

Example 2 – CPU Read from RAM (Refer to Figure 5-18.)

- The CPU indicates it needs to read from RAM. It signals it is to be bus master and latches the address into the CDAL-DAL latch buffer. This puts the address on the DAL bus. Address Strobe also transfers the address to the A Bus.

- The RAM address decoder decodes the address, recognizes that it is a valid RAM address, and asserts a RAM enable. This decoder is a 256 × 4 PROM decoder which enables the appropriate RAM daughterboard module. (There are two possible).

- The address is now on the A Bus. A delayed address strobe signal and the system RAM enable assert signals that transfer the address to a multiplexer driver which, in turn, puts the address on the RAM chips. Note that the address is also on the CTI BUS but external RAM does not respond because the address is not decoded in their ranges.

- Once addressed, the data in RAM is available for reading. Additional system timing signals open the latch buffers, putting the RAM data on the DAL bus. The CPU has finished addressing and enables the slave drive enable signal. This allows a slave device to drive the bus. This signal enables the DAL-CDAL latch buffer and gates the data to the CDAL bus which connects directly to the CPU chip set.

- If the CPU requires backplane RAM, the system board RAM enable is not generated and the appropriate device on the CTI BUS decodes the address and would reply from the bus.

  Although Example 2 shows reading from RAM, the signals are also asserted on the CTI BUS. Since no device on the bus was addressed (slot select), the bus devices do not respond. The address decoder responded to the address, enabling RAM. Figure 5-19 shows a simplified CTI BUS timing relationship during a read cycle.

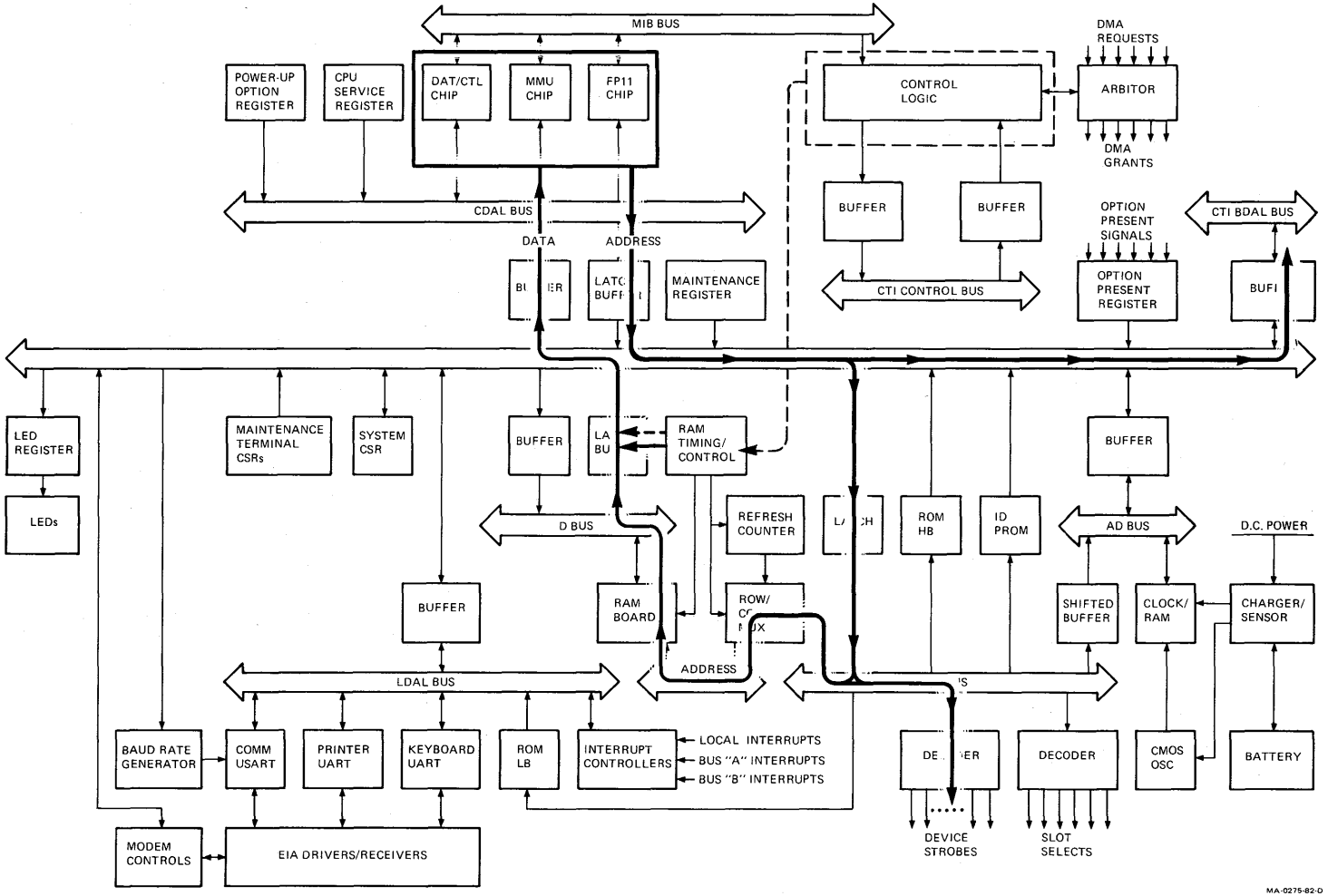


Figure 5-18 CPU Read from RAM

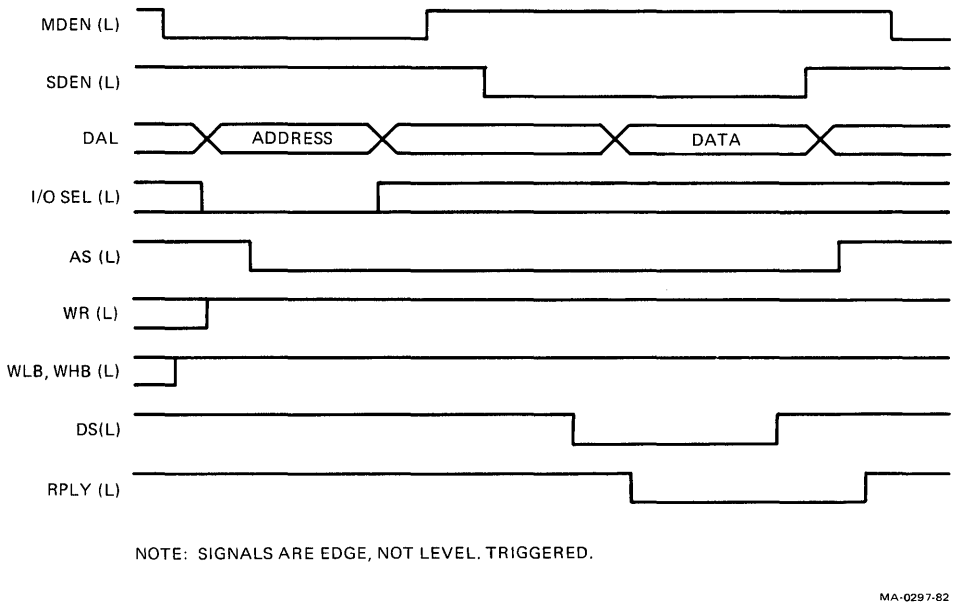


Figure 5-19 Simplified CTI BUS Timing Relationship During a Read Cycle

Example 3 – DMA Request and Grant (Refer to Figure 5-20. Also refer to Section 5.3.7 for a description of DMA).

- A device on the CTI BUS signals a request for DMA. A hardwire circuit chooses which DMA request is first.
- The DMA selection circuit gives a DMA grant to the first device requesting DMA.
- The device asserts it is bus master and puts an address on the DAL bus and then address strobe.
- Address strobe latches the address to the A Bus and then it is decoded. The appropriate memory (either RAM daughterboard or RAM in the backplane) is enabled. If the required operation is a write to memory, the DMA device asserts the write signal.
- On data strobe, data transfers to or from the bus master (the device). The direction depends upon the state of the WRITE signal. If the bus master writes to the RAM daughterboards, the DAL-D buffer transfers the data.

Figure 5-21 shows a simplified CTI BUS timing relationship for a DMA request and grant cycle.

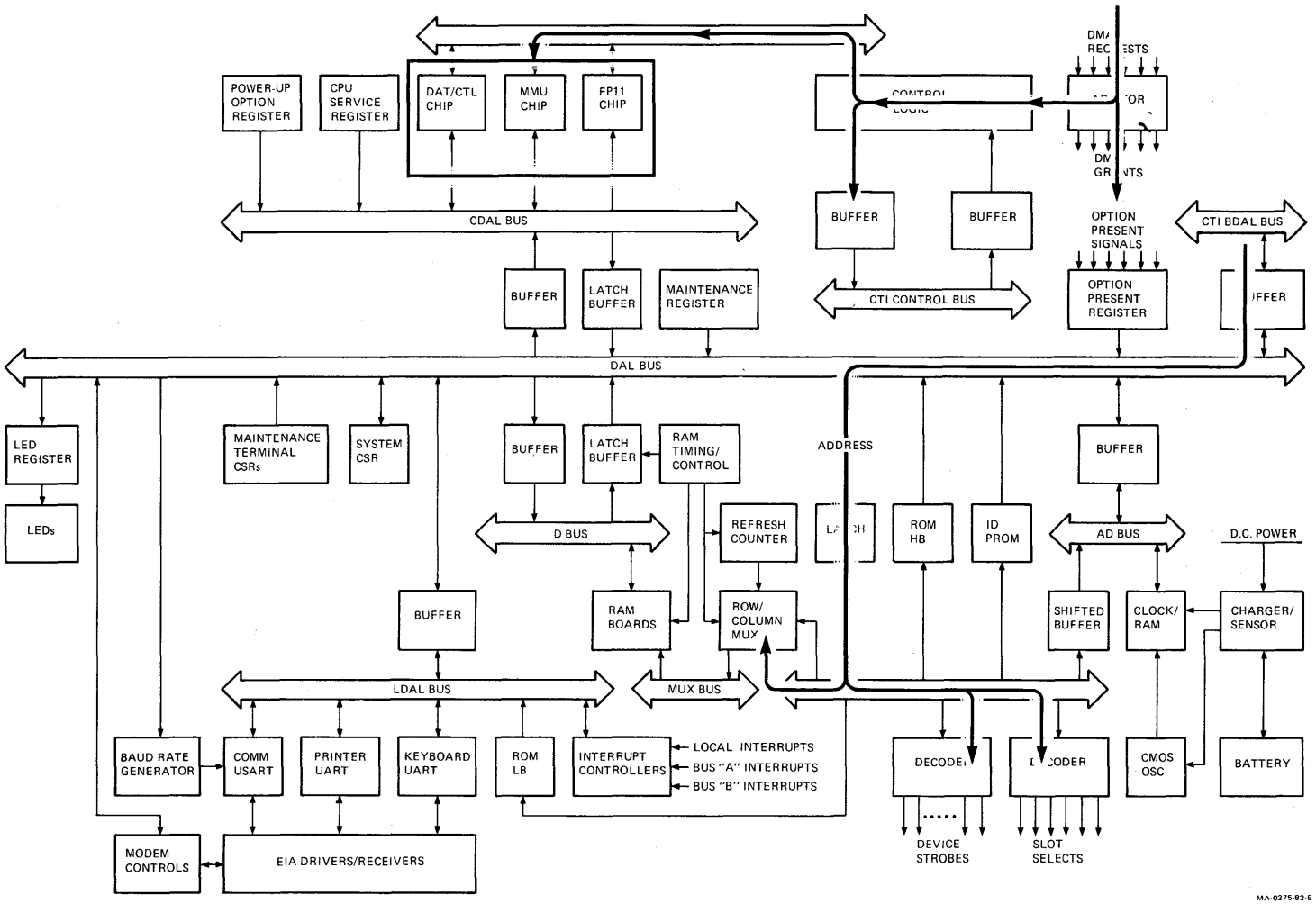


Figure 5-20 DMA Request and Grant

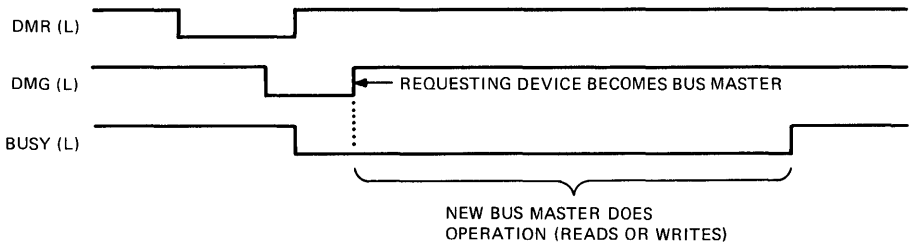


Figure 5-21 Simplified CTI BUS Timing Relationship During a DMA Request/Grant Cycle

Example 4 – CPU Writing Out to RAM (Refer to Figure 5-22).

- The system mounted RAM modules are addressed as in Example 1.
- A clock signal enables the data transfer from CPU to DAL bus, then to the DAL-D buffer. The CPU asserts a write signal. The WRITE signal enables the buffer, putting the data on the D Bus. The WRITE signal also enables RAM to write.
- Since the RAM chips were enabled once addressed, data strobe clocks the data into RAM.
- If the CPU required backplane RAM, the system RAM enable is not generated and the appropriate device on the CTI BUS decodes the address and would reply from the bus.

5.3.6 Interrupt Vector Circuit

The system module uses three interrupt controller chips (9519A) to handle all the system interrupts. The first controller handles all the interrupts generated by devices on the system module. The second controller handles all the A interrupts from the option modules and the third controller handles all the B interrupts from the option modules. The interrupt controllers latch the interrupt requests, provide the interrupt enable for each, prioritize the pending interrupts, and generate the proper vectors (Figure 5-23). Firmware programs the controller chips to prioritize pending interrupts and generate their vectors. The controllers interrupt the CPU at processor status level 4.

After acknowledgement, the device interrupt request line must be unasserted and then reasserted to generate a new CPU interrupt request.

Refer to Table 5-9 for the interrupt controller assignments.

Each of the interrupt controllers has a set of registers which control the specific features of operation. These registers are accessed via the CSR and data registers. Refer to Section 5.4 for details on these registers.

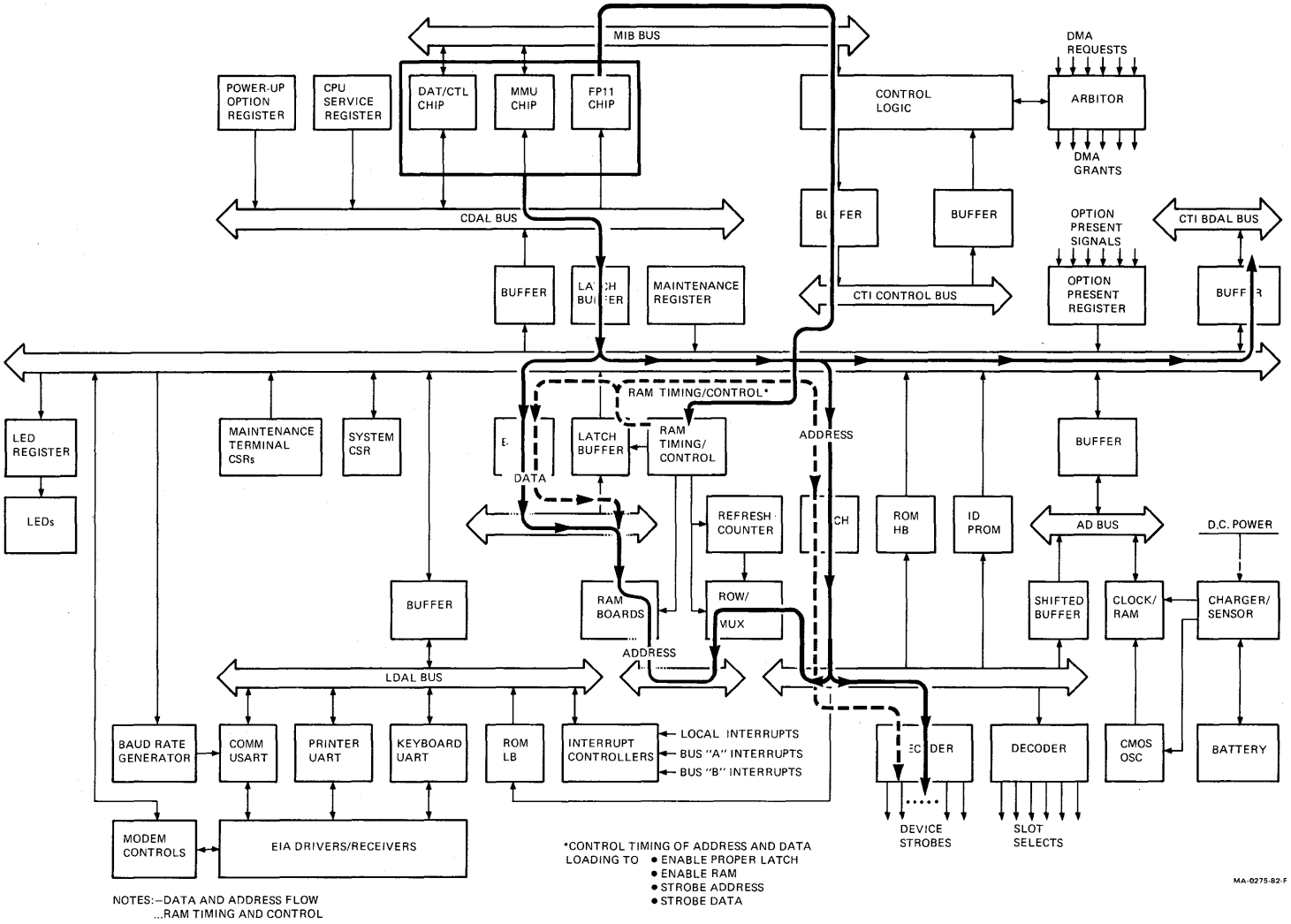


Figure 5-22 CPU Writing Out to RAM

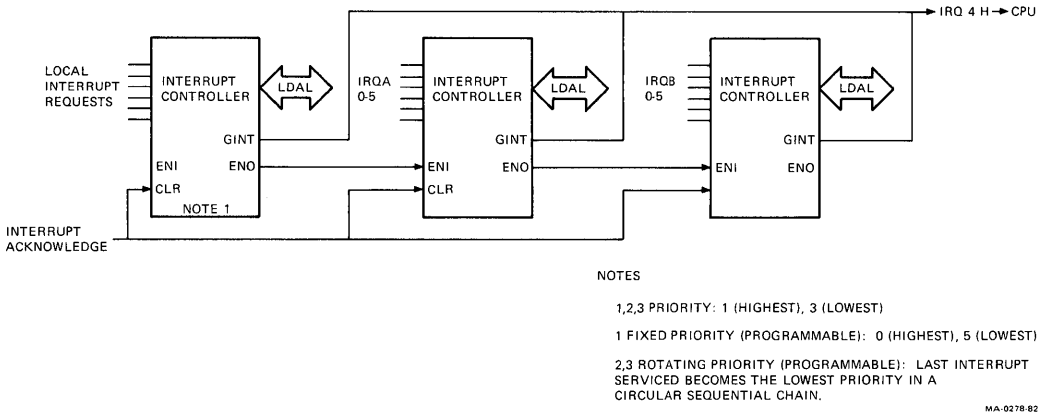


Figure 5-23 Functional Interrupt Control Circuit

Table 5-9 Interrupt Controller Assignment

Controller	Request Level	Vector*	Interrupt Description
0	0	—	Not used
	1	200	Keyboard receiver interrupts
	2	204	Keyboard transmitter interrupt
	3	210	Communication port interrupt
	4	214	Modem controls change interrupt
	5	220	Printer receiver interrupt
	6	224	Printer transmitter interrupt
	7	230	Clock interrupt
1	0	300	Option module 0 interrupt request A
	1	310	Option module 1 interrupt request A
	2	320	Option module 2 interrupt request A
	3	330	Option module 3 interrupt request A
	4	340	Option module 4 interrupt request A
	5	350	Option module 5 interrupt request A
	6	—	Not used
	7	—	Not used
2	0	304	Option module 0 interrupt request B
	1	314	Option module 1 interrupt request B
	2	324	Option module 2 interrupt request B
	3	334	Option module 3 interrupt request B
	4	344	Option module 4 interrupt request B
	5	354	Option module 5 interrupt request B
	6	—	Not used
	7	—	Not used

* Firmware establishes these vectors at power up.

5.3.6.1 Interrupt Service – A device interrupt can be generated at any time. The CPU, by reading the service register, knows when PHASE H is low. When the CPU receives an interrupt, the CPU stops processing, stores its current location and function internally, and changes to an interrupt handling routine. when the CPU asserts an interrupt acknowledgement signal (Figure 5-24), it is ready to read the vector of the highest interrupting device.

This signal begins the interrupt vector operation. The system I/O controllers determine the highest priority interrupt. Once determined, the appropriate controller places the vector on the LDAL bus.

The interrupt acknowledge signal performing the following.

- Enables the LDAL-DAL buffer, putting the interrupt vector on the DAL bus when PHASE H is asserted.
- Turns off the control line buffer to the CTI BUS, keeping AS H and all control signals from the CTI BUS.
- Initiates the interrupt controllers to generate the vector for the highest pending interrupt.

A response in process signal from the interrupt controller (RIP L) asserts a reply signal. This changes PHASE to PHASE-BAR and clocks the vector into the CPU.

5.3.7 Direct Memory Access (DMA)

When a DMA type device on the CTI BUS requires access to memory to read or write data, it requests a direct memory access (DMA). If a DMA device requests the bus, the CPU gets off the bus and allows the device to become bus master and access memory directly.

If two or more devices require DMA at the same time, an arbitration determines which device receives the grant first. There are two priority schemes in the Professional 350.

Each option controller module has a circuit to transmit its own priority level and monitor the priority of any device currently using the bus. If a low priority device is on the bus and a higher priority device requests DMA, the lower priority one un-asserts its DMA request line.

There are three priority levels in the Professional 350. If the requesting devices are at the same priority level, then the one in the lowest slot number wins the decision.

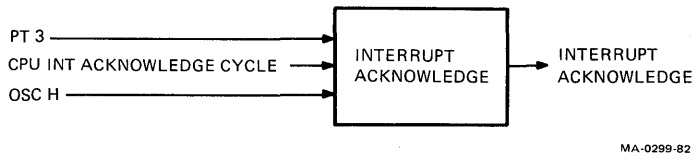


Figure 5-24 Interrupt Acknowledge Signal

5.3.7.1 DMA Detailed Description – Each slot on the CTI BUS has a DMA request line. An option controller module pulls the line low to assert a DMA request. A clock circuit samples the DMA requests and an 8:3 priority encoder drives a latch (Figure 5-25) which holds the winner of the arbitration. Once the winner is latched, the priority encoder can latch for the next arbitration. A decoder then enables the DMA grant to the slot of the winner.

When the device receives the grant, it drops its request and asserts a bus busy (BBUSY) signal. This signal sets up timing circuits that prevent asserting a new DMA grant until the busy signal clears. The DMA arbitor circuit stops the system clock in PHASE time and disables the CPU until DMA is finished. If a second DMA request follows the first, the CPU remains idle.

The DMA arbitor also arbitrates between devices on the bus and CPU bus cycles. If the CPU is using the bus, it prevents a DMA grant until it is finished with the bus.

5.3.8 (Read Only Memory) ROM

The system ROM contains power-up self-test code, configuration and initialization code, and the boot code. Some ROM is in the I/O page and some is in the memory address space. After addressing, the data in ROM is put out on the bus. Attempts to write to ROM result in non-existent memory traps to location 4.

The power-up self-test is described in Section 5.2.3.4.

The following is the address and data read sequence. Refer to Figure 5-26 for ROM addressing and reading.

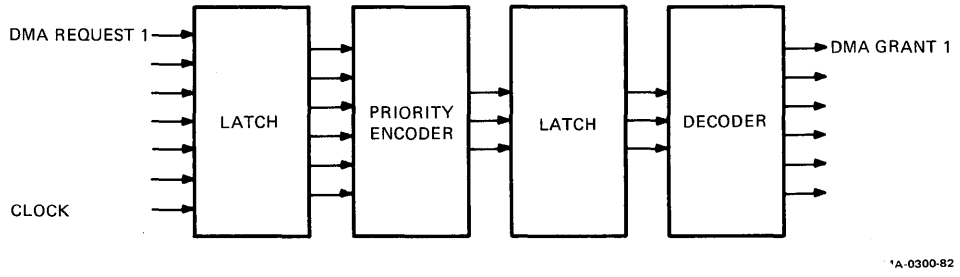


Figure 5-25 DMA Arbitor

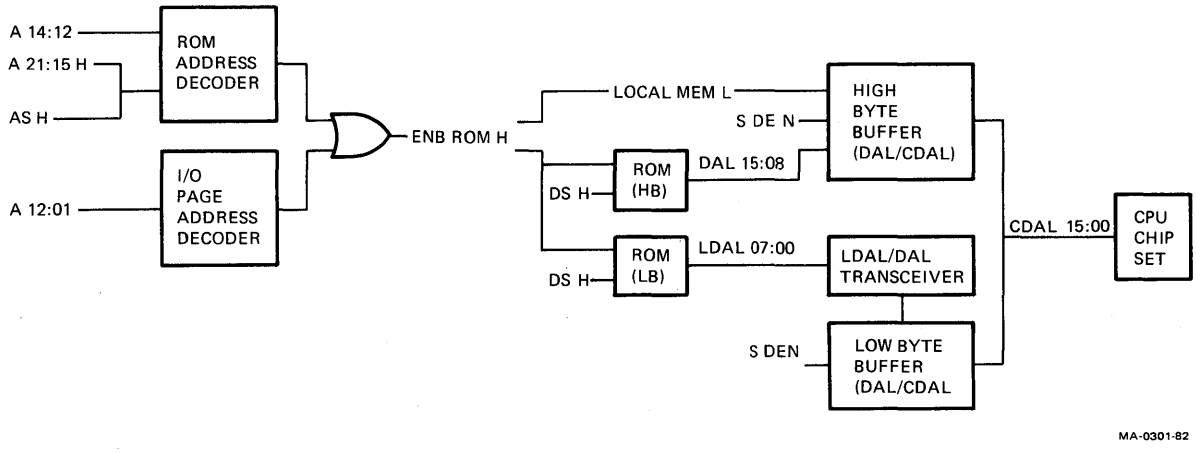


Figure 5-26 ROM Addressing and Reading

Addressing ROM
If ROM is in the memory space, the following occurs.

- If A 21:15 are high, at Address Strobe (AS H), the ROM address decoder decodes A 14:12. This asserts ENB ROM H (valid ROM address) and LOCAL MEM L.

- ENB ROM H and Data Strobe (DS H) put addressed ROM data on the bus. High byte data is on the DAL bus (DAL 15:08), low byte data is on the LDAL bus (LDAL 07:00).

- LOCAL MEM L indicates the CPU is talking to either local ROM or RAM.

I/O Page Address Decoder
If ROM is in the I/O page range, the following occurs.

- A 12 and LBSIO are decoded and assert ENB ROM L if the address is a valid ROM address in this range.

Reading Data from ROM

High Byte

- At Data Strobe (DS H), the DAL-CDAL buffer passes the data (DAL 15:08) from the DAL to the CDAL bus.

Low Byte

- LDAL 07:00 transfers data from the LDAL to DAL bus at DS H, and since the DAL-CDAL buffer is on at this time, the data (DAL 07:00) passes to the CDAL bus.

Both Bytes

- Data on the CDAL bus is read directly by the CPU chip set.

- ENB ROM H also asserted LOCAL REPLY H five clock cycles later. One cycle after that, it asserts RREPLY 3 L. This ends PHASE time and the data transfer on the DAL bus.

5.3.8.1 ID PROM – Each Professional 300 Series computer module has a unique ID PROM containing a unique identifying number. When the CPU places an address in this PROM's range (17773600 – 17773676), the address is decoded, the PROM enabled, and the data asserted on the DAL bus.

5.3.9 Random Access Memory (RAM)
This section describes RAM on the Professional 350 system module. RAM is mounted on two daughter modules. Battery backed up RAM, internal to the battery backed up clock chip, is discussed in Section 5.3.13.

Each RAM daughterboard consists of 16 (64K × 1) dynamic MOS memory chips which provide capacity for 128 kilobytes of memory. The system can address up to 512 kilobytes per daughterboard slot. Inserting either module in either slot informs the CPU of available address space. Bank 0 is the slot physically farther from the CPU chip set, bank 1 is the closer.

RAM requires support timing circuits. Address and data come to RAM via the DAL bus. The DAL bus is multiplexed for address and data, but RAM requires two separate buses so an address can be held while data is read or loaded. The A Bus accepts address data from the DAL bus and the D bus accepts data, each at its respective time.

Refresh Cycles
Data in RAM requires periodic refreshes. The system generates a refresh signal every 12.7 μs (refresh clock). The memory chips used here only require a row address strobe for refresh. At the refresh signal, a counter and driver clock each row to refresh data. The refresh signal also enables a row address strobe signal described next. Refresh cycles occur after each instruction fetch or when the refresh clock times out at 12.7 μs. These time outs occur while executing long instructions, during DMA transfers (with no fetching), or when halted into ODT.

Read/Write Cycles
Reading from or writing to RAM requires loading an address into RAM. An address to the RAM chips is 16 or 18 bits wide. Since the RAM chips have only eight or nine address lines, row and column data are entered separately. First, the low bits are loaded as row address. Then the high bits are loaded as column address. Row address strobe and column address strobe clock in the row and column addresses.

- A RAM address multiplexer takes the 16 or 18 address lines from the A Bus and first transfers the low half and then the high half to the MUX bus.
- Row and column address strobes load the low and high parts of the address from the MUX bus to the RAM chips.

If a DMA device is reading from RAM, it places the RAM address on the bus. This enables the address on the chips and asserts the data on the D Bus. RAM outputs the full 16-bit data word. The device then reads whichever byte(s) it wants.

For a DMA device to write to RAM, it places the RAM address on the bus. This enables the address on the chips. A write signal is necessary. RAM writes may be low byte only, high byte only, or a full 16-bit data word.

Refresh Read/Write Arbitration
Because refresh is a periodic event and memory cycles occur only on demand, the system must arbitrate between refresh and read/write (R/W) signals. A refresh signal is needed to keep the refresh counter counting to address all memory address rows. Since refresh is periodic, arbitration begins when a R/W signal clocks its respective flip-flop. (Figure 5-27). Refresh wins the arbitration if the refresh clock gates the refresh flip-flop before delayed address strobe. If the R/W signal and delayed address strobe win, there is a memory cycle. If R/W wins, other circuits are also enabled for data transfer.

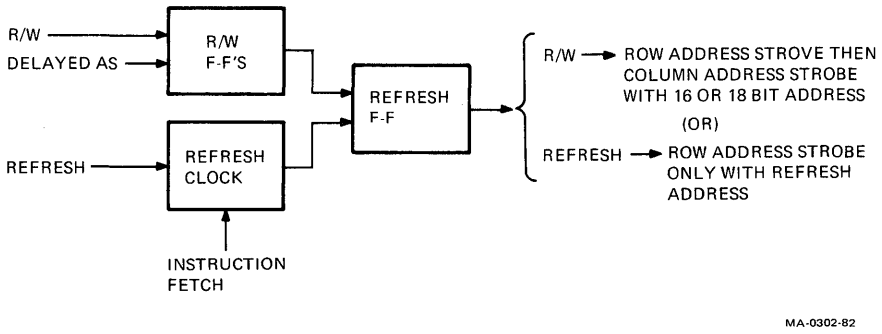


Figure 5-27 Refresh-R/W Arbitration

5.3.9.1 RAM Timing and Control (Refresh Cycles) – When power is applied to the Professional 350, a one-shot timer asserts a refresh clock signal (Figure 5-27). This signal clocks a flip-flop which generates the refresh signal. The following occurs when refresh is asserted.

- Clocks a 8-bit binary counter which addresses all RAM address rows.
- Enables an octal tri-state buffer driver to put the refresh address on the MUX bus.
- Asserts row address strobe.
- Disables the D-DAL latch buffer.
- Disables column address strobe to the RAM chips.

The following occurs when refresh is not asserted.

- Starts the one-shot timer to clock the next refresh cycle.
- Allows normal RAM operations.

Read/Write Cycles – If the CPU asserts a memory cycle, the MIB bus indicates the kind of cycle to take place. Control circuits set up other logic to carry it through. The signal LBSIO plus two bits on the A bus (A21 and A20) must all be asserted to enable the RAM address decoder. The address decoder asserts the memory row select signal for the RAM daughter module(s). The decoder plus a read or write signal enables circuitry that begins timing used for refresh R/W arbitration. If the CPU wants to read, a whole word is asserted on the D Bus. If it wants a byte, it ignores the undesired byte. When writing, the CPU can signal a write or write-byte. If it signals a write-byte, then it asserts a write-high-byte or write-low-byte. The undesired RAM byte is unaffected. If writing a word, then both write-byte signals are asserted.

Read and write are the inputs to their respective flip-flops. A delayed address strobe clocks each flip-flop. The delay assures the address decode is completed. Read is triggered at address time and there is no need to wait for data strobe. The outputs of either flip-flop combines with timing signals as the entry to refresh R/W arbitration.

If the R/W signal wins the arbitration, it does the following.

- Blocks the refresh signal.
- Asserts timing signals.
- Allows reading from or writing to RAM.

The timing signals perform the following.

- Control the period of the refresh versus R/W cycle.
- Switch the RAM address multiplexer (Figure 5-26).
- Enable the column address strobe.
- Clear the refresh and R/W flip-flop to be ready for the next arbitration.
- Enable the D-DAL latch buffer.

Reading the RAM uses the D-DAL buffer. This buffer latches if there is a valid RAM request at delayed address strobe. As explained, RAM data is put out on the D Bus directly when addressed.

Writing to memory uses the DAL-D buffer which goes directly to the RAM chips. Writing requires the write command to enable this buffer. The write command also goes out to the CTI BUS.

Refresh R/W Arbitration – When there is no R/W signal, refresh occurs at regular intervals (12.7 μs). When a R/W signal occurs, RAM timing logic arbitrates between the refresh and R/W signals.

The RAM Address Decoder cannot assert an enable for system RAM until the address is stable on the A Bus. When clocked, the read and write provides an input to the refresh flip-flop. Arbitration begins when the R/W signals compare timing with the self-generated refresh signal (Figure 5-28). If the refresh signal arrives at an R-C timing circuit first, it provides a slower discharge time and a longer period. If R/W arrives at the R-C circuit, then it provides a faster discharge and holds the refresh flip-flop clear until the next arbitration begins.

Whichever signal wins begins a new timing cycle. The cycle enables a buffered delay line to provide pulses for RAM timing logic. The signal that starts this delay line holds itself on until the end of the cycle, ensuring that the cycle is the correct period.

Timing signals for both daughter modules enable the RAM chips. If it is a refresh cycle, the RAM column address strobe is blocked and the row address strobe only is sent to both modules (while the counter refreshes each address row). If it is a R/W cycle, a module select signal enables the RAM row address strobe for the module selected by the RAM address decoder. The timing signals then enable the column address strobe and switch the RAM address multiplexer for the high byte.

The refresh flip-flops clear at the end of the refresh cycle timing chain. This permits a new arbitration.

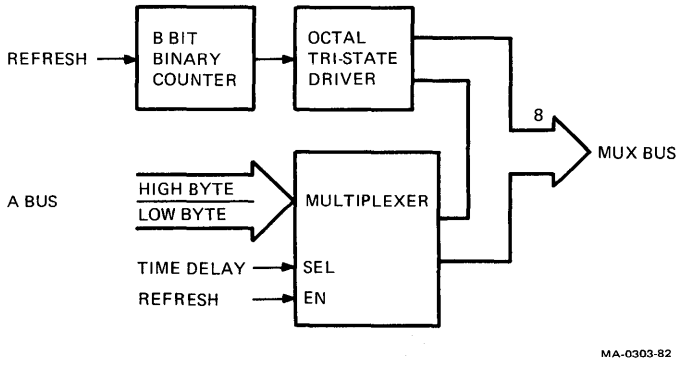


Figure 5-28 RAM Address Multiplexer

5.3.10 Keyboard I/O

The keyboard I/O is a serial port on the system module. It performs asynchronous serial communication to and from the keyboard. The keyboard interface uses a 2661 enhanced programmable communication interface (EPCI). The EPCI is an enhanced USART containing its own I/O buffers and shift registers for controlling asynchronous character protocol. This chip converts parallel data characters from the LDAL bus into serial data for transmission to the keyboard. Simultaneously it converts serial data from the keyboard into parallel data for CPU processing. The keyboard, discussed in Chapter 6, has its own microprocessor to coordinate keyboard I/O at that level.

The EPCI requires standard EIA RS-423 signal levels and uses appropriate receivers and drivers for input and output. Keyboard connection to the system board is via a 15-pin male D-subminiature connector, J5 (see Section 5.5). The I/O signals to the keyboard are sent and received through the video/keyboard connector, J5. Signals are physically passed through the video monitor by the monitor's keyboard connector. Data to and from the keyboard is via the signals KBD XDATA and KBD RDATA. When a character is transmitted or received, the EPCI generates an interrupt (KBD XIRQ L or KDB RIRQ L). Refer to the sections on interrupts (Sections 5.3.6 and 5.4.6).

The EPCI uses a 5.0688 MHz clock for baud rate generation. The transmit and receive baud rates are programmable by the CPU. The keyboard runs at 4800 baud (the firmware programs the keyboard USART to 4800 baud). Refer to Figure 5-29.

Refer to Section 5.4 for a complete description of the registers and their interpretation.

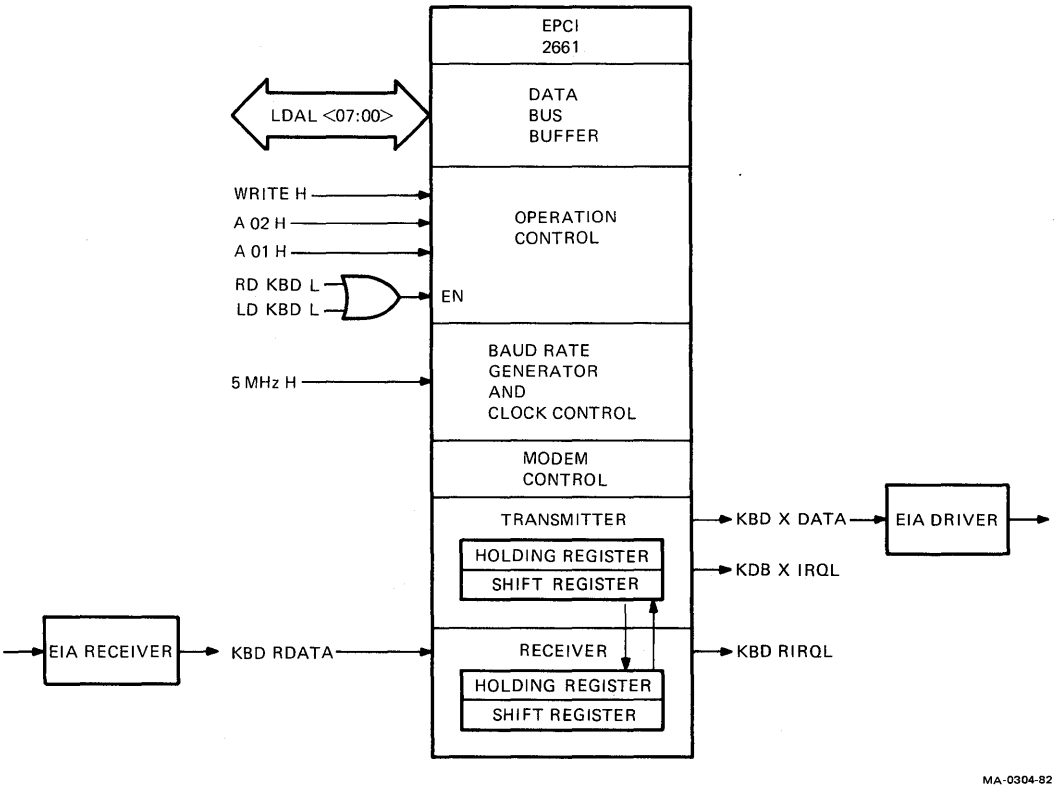


Figure 5-29 Keyboard Interface

5.3.11 Printer I/O

The printer I/O is a port on the system module that performs asynchronous serial communication to and from a serial printer. The printer interface uses a 2661 EPCI. This chip converts parallel data characters from the LDAL bus into serial data for transmission to the printer. Simultaneously, it converts serial data from the printer into parallel data for CPU processing (Figure 5-30).

The EPCI requires standard EIA RS-423 signal levels and uses appropriate receivers and drivers for input and output. Connection to the unit is via a 9-pin male D-subminiature connector, J6 (see Section 5.5).

The EPCI uses a 5.0688 MHz clock for baud rate generation. The transmit and receive baud rates are programmable by the CPU. The firmware programs the printer port to 4800 or 9600 baud depending upon the cable, printer (PN BCC05), or console (PN BCC08).

It is necessary to connect a printer before the EPCI permits data output.

The EPCI generates an interrupt to the CPU when characters are transmitted or received. Refer Sections 5.3.6 and 5.4.6.

Shorting pins 8 and 9 of the printer connector together tells the CPU a terminal DL console is connected for maintenance. The normal printer cable connector does not short these pins. The short pulls the line low, enabling break detection by the CPU. A received break asserts the CPU halt line (HALT H) to the CPU via the service register. This makes the CPU enter micro-ODT (Octal Debugging Technique) for maintenance and system level troubleshooting.

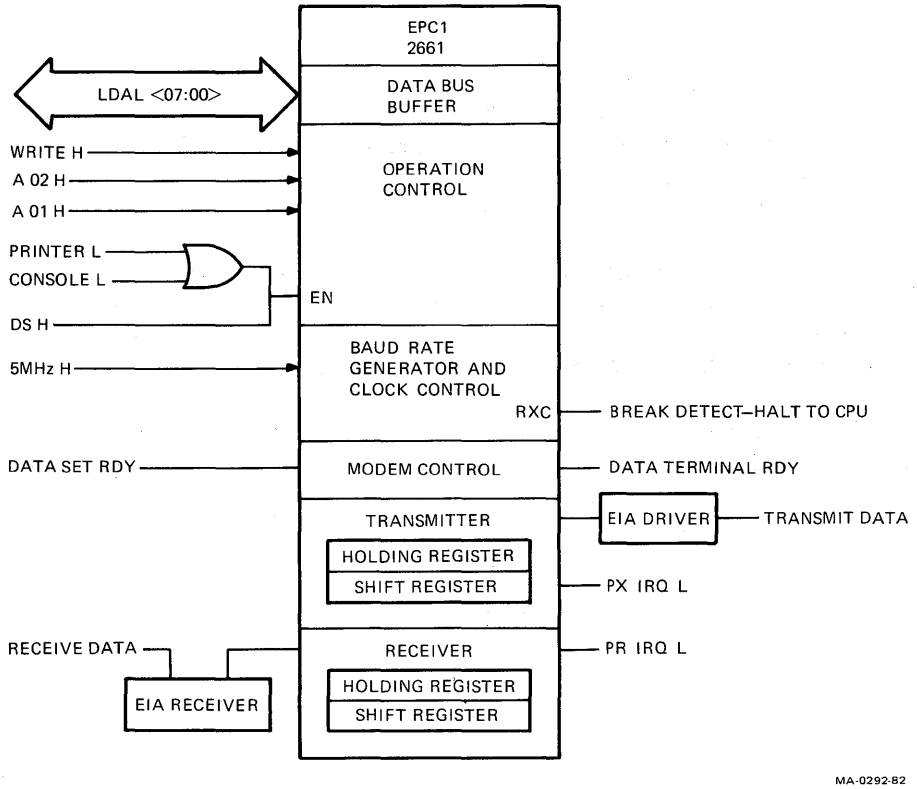


Figure 5-30 Printer Interface

This micro-ODT function allows the conventional front panel on a processor to be replaced by any terminal generating ASCII code. If a conventional printer cable is used (pins 8 and 9 open), BREAK does not halt the CPU. The cable for this function is the console cable (PN BCC08).

The EPCI is enabled on DS H and received data is placed on the LDAL bus. The CPU then reads the data. Refer to Sections 5.4.14 and 5.4.15 for a description of addressing and register interpretation.

5.3.12 Communication I/O

The system module has a communication port capable of operating with asynchronous and bit or byte synchronous protocols. It uses a 7201 USART containing its own I/O buffers and shift registers. In asynchronous mode, it can run at split programmable baud rates up to 19.2K baud. In synchronous mode, it can run up to 740K baud. The transmitter is double buffered and the receiver is quad buffered. A full set of modem controls is also present for asynchronous communication. All the port signals are EIA RS-423 levels. Connection is made on the rear of the unit via a 25-pin male D-subminiature connector, J7 (see Section 5.5).

The communications port can assert two interrupts.

- The first can interrupt the CPU if the USART chip requires receiver or transmitter service.
- The second interrupt can indicate that a state change has occurred on one of four modem control signals.

These four modem control signals are Ring Indicator, Data Set Ready, Clear To Send, and Carrier Detect.

Communication I/O requires support circuits. A baud rate generator selects the clock speed for the USART. Modem controls monitor modem status signals.

- Modem Controls – EIA level buffers receive the modem signals mentioned above. These signals connect directly to the DAL bus through a buffer which is enabled via the I/O page address decoder. A exclusive-or circuit compares the modem signals' states clocked in on PHASE time with their status on the previous PHASE time. If any of the states changes, the exclusive-or circuit generates an interrupt (see Sections 5.3.6 and 5.4.6).
- Baud Rate Generator – A programmable baud rate generator (BRG) creates the clock signal for the USART. The I/O page address decoder selects the BRG. Section 5.4.13 provides a table of selectable baud rates for programming the BRG. Refer to Figure 5-31. Transmit and receive baud rates for the USART can be selected independently.
- USART – The communications USART is a parallel-to-serial, serial-to-parallel converter. It is programmable to check transmitted and received data integrity. It can generate an interrupt to the interrupt controller chips (see Sections 5.3.6 and 5.4.6).

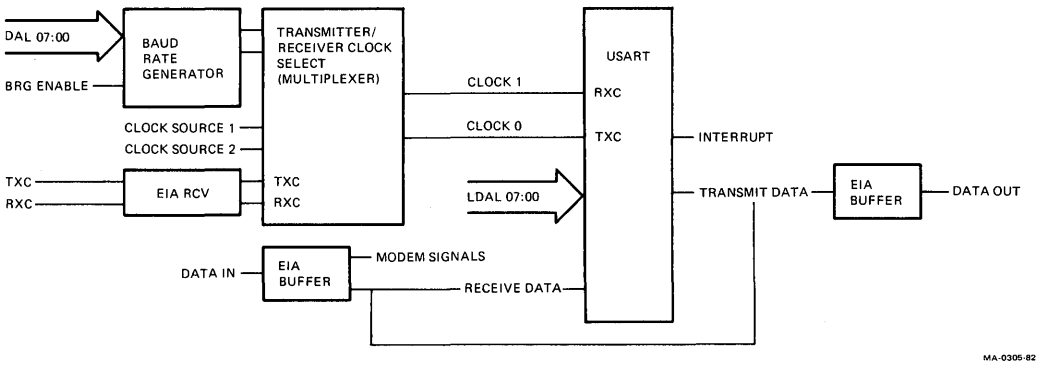


Figure 5-31 Communications Interface

5.3.12.1 Communications I/O Detailed Description – The following paragraphs provide a detailed description of the communications I/O features.

- Modem Controls – The modem interface uses standard EIA 423 level signals for input and output. Four modem control signals are modem status indicators: Ring Indicator (RI), Data Set Ready (DSR), Clear to Send (CTS), and Carrier Detect (CD). At the beginning of each PHASE period, these signals are latched into a holding buffer. Each signal then provides input to exclusive NOR gates. If there is a change in state from the beginning of one PHASE time to the next, the NOR gates assert an interrupt to the interrupt controller chips. The CPU can read modem signals from the DAL bus by addressing the modem control registers (enabled via the I/O page address decoder).

- Baud Rate Generator – The baud rate generator uses the same 5 MHz clock as the printer EPCI (Figure 5-31).

  The BRG generates clock signals for the USART. Table 5-10 shows the selection scheme for the transmit and receive clocks.

- USART – The communications USART uses another clock oscillator. The CPU selects transmit and receive baud rate clocks as described above. Transmit data feeds back into the received data line (Figure 5-31) but is ignored except when in maintenance mode. When this happens, received data is ignored until the modem control register is cleared (at power up or by a reset instruction) or written with new data.

Table 5-10 Baud Rate Generator TX/RX Clock Selection

Clock Source	Baud Rate Generator Clock
01	Asynchronous; determined by BRG
01	Modem supplies synchronous receive and transmit signals
10	Modem supplies receiver clock, transmit clock source is transmitter stage of BRG
11	Maintenance mode; transmit stage of BRG is the clock for transmit and receive

5.3.13 Battery Backed-Up Clock and RAM

The following paragraphs describe the battery backed-up clock and RAM.

- Clock – This system clock maintains date and time even when the system is turned off. The clock is a 146818 CMOS chip. The power off back up uses a rechargeable nickel cadmium (NiCd) battery. The battery connector, J3, is on the system module (Section 5.5). The battery is mounted inside on the rear of the card cage. The clock uses its own 32.768 kHz oscillator as a time base.

- RAM – The clock chip has 50 bytes of RAM which are also backed up by battery. The battery power maintains data in the chip when system power is turned off.

- Battery – When the system is turned on, the power supply trickle charges the battery and powers an oscillator for the clock. When turned off, the battery powers the oscillator and clock. Fully charged (power on for 48 continuous hours minimum), the battery maintains clock operation for 10 days minimum if system power is turned off.

5.3.13.1 Clock and RAM Circuit – The clock chip is programmable for date and time functions. Alarm and interrupts also are programmable by writing to the clock's registers. Reads and writes to the clock require assertion of NV L (from the I/O Page Address decoder) and DS L. Reads require the signal WRITE L to be high (not asserted). The clock can assert an interrupt request (CLK IRQ L).

The clock chip power line is filtered to minimize spurious noise from the oscillator.

Addresses and data to and from the clock chip are multiplexed on the AD bus and are low byte only.

Refer to Section 5.4.13 for programming and register descriptions for both the clock and RAM.

5.3.13.2 Battery Charger and Voltage Sensor – The battery charging circuit supplies 10 mA to the battery when the system power is turned on. The charging circuit is a voltage divider that uses +12 Vdc in reference to +5 Vdc. When the system is turned off, the battery powers the oscillator and clock.

The clock/RAM has an internal bit which can be cleared (VRT in Status register 3) if power goes low. When set, this bit indicates clock and RAM data may not be valid. If there is insufficient battery power, the input pin for this circuit is pulled low when the system is first turned on (Figure 5-32). Table 5-11 shows the power sense when power is on and off.

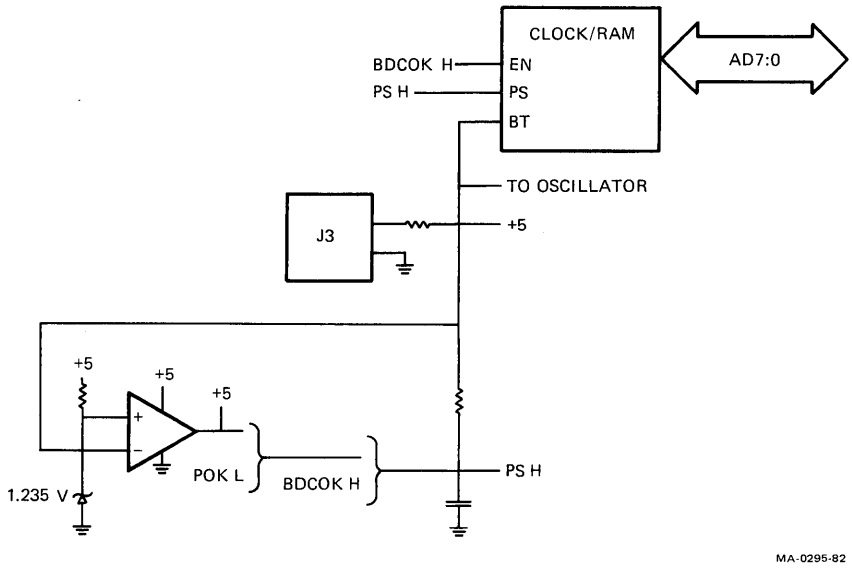


Figure 5-32 Functional Battery Charger and Voltage Sensor

Table 5-11 Power Sense

Battery Installed and Charged
Power Off:
Battery holds PS H
VRT bit stays set

Power On:
No change

Battery Not Present or Discharged
Power Off:
PS is low
VRT bit clear

Power On:
RC circuit holds PS low until BDCOK H
(which sets chip enable)
then POK goes L, asserting PS H.

5.4 PROGRAMMING INFORMATION

5.4.1 Introduction

This section describes the machine level programming for the Professional 350 system module. It contains information about how to access internally programmed functions for the CPU and support devices on the system module. It does not contain information about applications programming in high level languages.

Each subsection gives a short description of the device and its function. Some sections provide a brief theory of operation for the devices. Also included are a description of the buffer or register, diagrams showing the bit names and arrangements, and definitions of each bit or groups of bits. Tables are included in the bit descriptions to show the effects of the bit combinations.

The de-bugging subsections provide examples that show how the maintenance commands can be used.

5.4.2 General Programming Information

The system module contains the CPU and other devices that need instructions to operate. The instructions must be entered at the beginning of each operating session or whenever a change in operating instructions is needed. This section contains the instructions for the CPU and all the supporting devices on the system module.

This section contains two types of programming information: information to change the program and information that tells what is happening. Depending on what is happening, the program might change the operating instructions.

Operating instructions are written to buffers. Information is read from registers. The CPU chip set, interrupt controllers, RAM, system clock, keyboard and printer USARTs, and communications controller all have buffers into which data can be written. They also all have registers which can be read (ROM can only be read).

User programs (in machine language) enter instructions to make the Professional 350 perform as needed. For example, to restructure the interrupt scheme, the priority of the preferred device can be raised. The necessary instructions must be entered to the interrupt controllers using their instruction set. If it is necessary to read the status of certain registers, these can be accessed by addressing the register and reading its current status.

Buffer contents can be entered and registers read via the printer port. This is described in Sections 5.4.14 and 5.4.15. Simple maintenance and diagnostic routines (in machine language) can be run through this port.

Refer to Table 5-8 for address ranges.

5.4.3 Central Processor

The following paragraphs provide information about the central processor.

Processor Chip Description

The central processor is a 2 die 40-pin hybrid integrated circuit. The data chip contains the PDP-11 general registers, the processor status word (PSW), working registers, the arithmetic logic unit (ALU), and conditional branching logic. It performs arithmetic and logical functions, handles all data and address (except relocation) transfers with the external bus, and operates most of the signals used for interchip communication and external system control.

The control chip contains microprogram logic and 552 words of local microprogram storage in PLA and ROM arrays. This chip accesses the appropriate microinstruction in PLA or ROM, sends it along the micro-instruction bus (MIB) to other control and MMU chips, and generates the next microinstruction address. The control chip accesses only its local storage. However, additional control chips, like the floating point adapter (FPA), can be added externally to provide additional microstorage.

Instruction Set

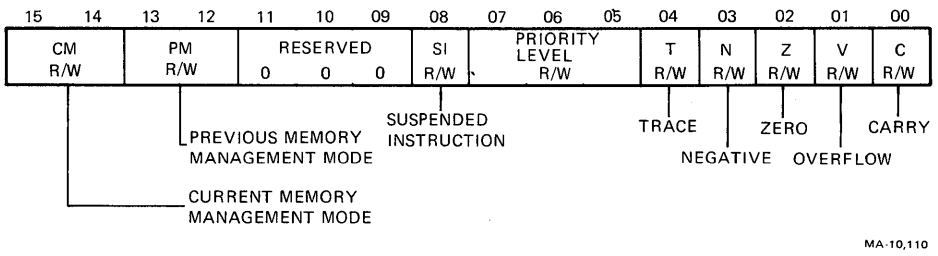
The instruction set is the standard PDP-11 instruction set plus the Extended Instruction Set (EIS). This provides hardware fixed point arithmetic in double precision mode. The HALT instruction is executed differently in kernel mode and user mode. In user mode, a trap through location 10 occurs. In kernel mode, the CPU halts and enters micro-ODT (Sections 5.4.14 and 5.4.15). The floating point adapter option adds additional instructions.

Processor Registers

Addresses:

17777750	Processor maintenance register
(R0)	General register 0
(R1)	General register 1
(R2)	General register 2
(R3)	General register 3
(R4)	General register 4
(R5)	General register 5
(R6 or SP)	General register 6 or stack pointer
(R7 or PC)	General register 7 or program counter
17777776	processor status word

Processor Status Word



The processor status word (PSW) contains the following information on the current status of the PDP-11.

- The current processor priority
- The current and previous operational modes
- The condition codes describing the results of the last instruction
- An indicator for detecting the execution of an instruction to be trapped during program debugging
- And an indicator for detecting the presence of a suspended instruction.

General Registers 0–7
The eight internal general registers (R0–R7) are used as accumulators and for operand addressing. Access to these registers is via software reference using the appropriate addressing mode or via the $ and R commands in ODT.

Stack Pointer – General register R6 is the hardware stack pointer (SP). This register saves and restores processor status word (PSW) information during hardware traps and interrupts. There are two stack pointer registers: one for kernel mode and one for user mode. For more information, refer to Section 5.4.3.2.

Program Counter – General register R7 is the program counter (PC). It contains the address of the next instruction to be executed. It is used for addressing purpose and not as an accumulator for arithmetic operations.

Processor Maintenance Register – The processor maintenance register is a 16-bit register that identifies the system architecture. It is always read as all zeros. All zeros in bits <7:4> indicate a Professional 300 series architecture product. Writes to the register have no effect but do not cause a non-existent memory trap.

Processor Traps
Several instructions and conditions cause the processor to trap through vectors to service routines. The following list indicates the processor trap vectors and conditions.

Vectors	Conditions
004	Bus timeout trap or stack overflow trap
010	Illegal and reserved instruction traps
014	Breakpoint and trace trap
020	IOT Instruction trap
024	Power fail trap
030	Emulator trap
034	Trap instruction trap
114	Memory error (parity, ECC, etc.)
244	Floating point error
250	Memory management abort

Bus Timeout – A bus timeout prevents hanging the bus when attempting to address non-existent memory location. A timeout occurs if the processor does not receive a REPLY signal from a slave device within approximately 6.5 μs from the start of the bus cycle. The timeout causes the bus cycle to terminate and the processor to trap through location 4.

5.4.3.1 Power Fail Trap – A power fail trap allows the processor to power down in an orderly way when ac power is lost. When the ac power loss is detected, the power supply clears the POK signal. The processor then traps through location 24 to allow the execution of a power fail routine.

5.4.3.2 Memory Management – The memory management unit (MMU) provides full 22-bit memory addressing capability of 2 megawords (4 megabytes). It also allows memory protection in a multi-tasking operating system environment.

A single die in one 40-pin package contains the MMU. Some of the floating point registers are in the MMU chip.

Memory Management Registers

Addresses:

17772300–17772316	Kernel page descriptor registers
17772340–17772356	Kernel page address registers
17777600–17777616	User page descriptor registers
17777640–17777656	User page address registers
17777572	Status register 0
17777574	Status register 1
17777576	Status register 2
17772516	Status register 3

Vector:

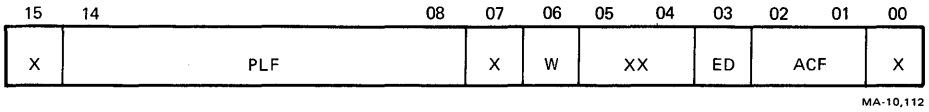
250	MMU abort

Page Address and Page Descriptor Registers

Kernel Active Page Registers			User Active Page Registers		
NO.	**PAR**	**PDR**	**NO.**	**PAR**	**PDR**
0	17772340	17772300	0	17777640	17777600
1	17772342	17772302	1	17777642	17777602
2	17772344	17772304	2	17777644	17777604
3	17772346	17772306	3	17777646	17777606
4	17772350	17772310	4	17777650	17777610
5	17772352	17772312	5	17777652	17777612
6	17772354	17772314	6	17777654	17777614
7	17772356	17772316	7	17777656	17777616

Page Address Register (PAR) – The page address register (PAR) contains the 16-bit page address field (PAF) that specifies the base address of the page. The page address register is a relocation constant or a base register containing a base address. Either explanation indicates the basic function of the page address register (PAR) in the relocation scheme.

Page Descriptor Register (PDR) – The page descriptor register (PDR) contains information relative to page expansion, page length, and access control.



Bit 15 — Not used. Always read as zero.

Bits 14-08 — PLF – Page Length Field. This 7-bit field specifies the block number which defines the boundary of that page. The block number of the virtual address is compared against the PLF to detect length errors. An error occurs if the block number is higher than the PLF when expanding upwards or if the block number is less than the PLF when expanding downwards.

R/W bits.

Bit 07 — Not used. Always read as zero.

Bit 06 — W – Write Access Bit. This bit indicates this page was modified (written into) after either the PAR or PDR was loaded (W = 1 is affirmative). The W bit is useful in applications which include disk swapping and memory overlays. It is used to determine which pages were modified and must be saved in their new form and which pages were not modified and can be overlaid. Note that the W bit is reset to 0 when either the PAR or PDR is modified (written into).

Read-only bit.

Bits 05-04 — Not used. Always read as zeros.

Bit 03 — ED – Expansion Direction. This bit specifies in which direction the page expands. If ED = 0, the page expands upwards from block number 0 to include blocks with higher addresses. If ED = 1, the page expands downwards from block number 127 to include blocks with lower addresses. Upward expansion is usually used for program space while downward expansion is used for stack space.

R/W bit.

Bits 02-01 — ACF – Access Control Field. This 2-bit field describes the access rights of this specific page. The access codes or keys specify the way in which a page may be accessed and whether or not a given access results in an abort of the current operation. A memory reference that causes an abort is not completed, but terminated immediately.

Aborts are caused by attempts to access non-resident pages by page length errors or by access violations, such as attempting to write into a read-only page. Traps are used as an aid in collecting memory management information.

Table 5-12 lists the ACF keys and their functions. The ACF is written into the PDR under program control.

Bit 00 — Not used. Always read as zero.

Table 5-12 Access Control Field Keys

ACF	Key	Description	Function
00	0	Non-resident	Aborts any attempt to access this non-resident page.
01	2	Resident read-only	Aborts any attempt to write into this page.
10	4	(not used)	Aborts all accesses
11	6	Resident read/write	Read or write allowed No trap or abort. Read/write bits.

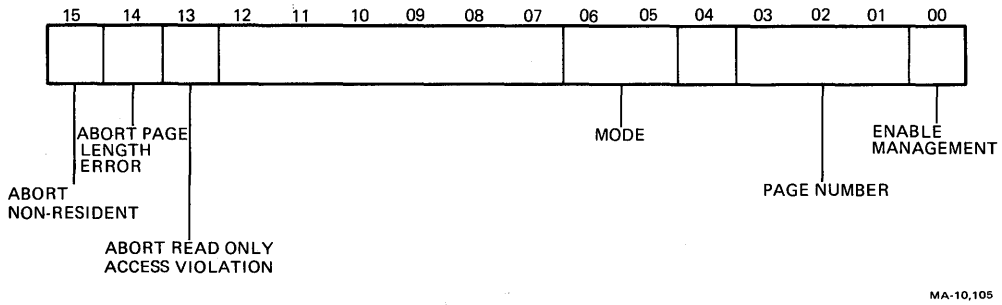
Status Register 0 (SR0)

SR0 contains abort error flags, memory management enable, plus other information needed to recover from an abort or to service a memory management trap. The following paragraphs describe the SR0 format.

Bits 15–13 are the abort flags. Abort bits can be set simultaneously by the same access attempt. They are in priority order; flags to the right are less significant and should be ignored. For example, a non-resident abort service routine ignores page length and access control flags. A page length abort service routine ignores an access control fault.

NOTE

When set (abort conditions), bits 15–13 cause the logic to hold the contents of SR0 bits 1 through 6 and status register SR2. This makes recovery from the abort easier.



Bit 15

Abort Non-Resident – This bit is automatically set by trying to access a page with an access control field (ACF) key equal to 0 or 4, or by enabling relocation with an illegal mode in the PS. When this occurs, the processor traps through vector 250. This bit can also be written under program control. However, only that information which is automatically written into this bit because of hardware action is useful as a monitor of the MMU status. Setting this bit under program control does not cause a trap to occur. The program should reset this bit to 0 after an abort or trap has occurred to continue monitoring memory management.

R/W bit.

Bit 14

Abort Page Length – This bit is automatically set by accessing a location in a page with a block number (virtual address bits 12–6) not authorized by the PLF for that page. When this occurs, the processor traps through vector 250. This bit can also be written under program control. However, only that information which is automatically written into this bit because of hardware action is useful as a monitor of the MMU status. Setting this bit under program control does not cause a trap to occur. The program should reset this bit to 0 after an abort or trap has occurred to continue monitoring memory management.

R/W bit.

Bit 13

Abort Read Only – This bit is automatically set by writing into a read-only page. When this occurs, the processor traps through vector 250. This bit can also be written under program control. However, only that information which is automatically written into this bit because of hardware action is useful as a monitor of the MMU status. Setting this bit under program control does not cause a trap to occur. The program should reset this bit to 0 after an abort or trap has occurred to continue monitoring memory management.

R/W bit.

Bits 12–07

Not used.

Bits 06–05

Mode of Operation – These bits indicate the CPU mode (user or kernel) associated with the page causing the abort (kernel = 00, user = 11). They are automatically written at the time of the abort. These bits can also be written under program control. However, only that information which is automatically written in these bits as a result of hardware action is useful as a monitor of the MMU status.

R/W bits.

Bit 04

Not used.

Bits 03–01

Page Number – These bits identify the page being accessed when an abort occurs. They are automatically written at the time of the abort. Pages, like blocks, are numbered from 0 upwards. These bits can also be written under program control. However, only that information which is automatically written in these bits as a result of hardware action is useful as a monitor of the MMU status.

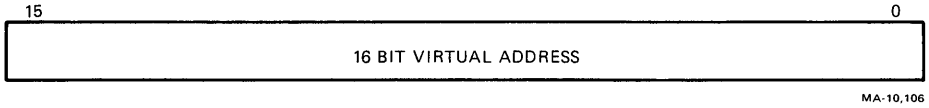
R/W bits.

Bit 00 — Enable relocation and protection – This bit is the memory management enable bit. It is set and cleared under program control. When it is set to 1, all addresses are relocated and protected by the MMU. When cleared to 0, the MMU is disabled and addresses are neither relocated nor protected.

R/W bit.

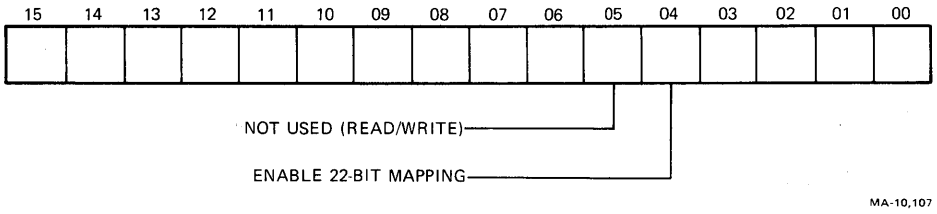
Status Register 1 (SR1)
SR1 is a read-only register which is always read as zero.

Status Register 2 (SR2)



SR2 is loaded with the 16-bit virtual address (VA) at the beginning of each instruction fetch. It is not updated if the instruction fetch fails. SR2 is read-only; a write attempt does not modify its contents. SR2 is the virtual address program counter. On an abort, setting SR0 bit 15, 14, or 13 holds SR2 until the SR0 abort flags are cleared.

Status Register 3 (SR3)



Bits 15–06 — Not used.

Bit 05 — Reserved – This bit is a R/W bit that has no effect on system module operation.

R/W bit.

Bit 04 — Enable 22-bit mapping – This bit enables or disables the memory management 22-bit mapping. If memory management is not enabled (SR0 bit 0 is clear), this bit is ignored and the 16-bit address is not relocated. If memory management is enabled (SR0 bit 0 is set) and this bit is clear, the computer uses 18-bit mapping. If memory management is enabled and this bit is set, the computer uses 22-bit mapping.

R/W bit.

NOTE

The 22-bit mapping should always be used. If 18-bit mapping is used, address bits <21:18> are always zeros and the I/O page is selected when bits <17:13> are all ones. In 18-bit mode, 12 of the 16 kilobytes of ROM are not accessible (along with any other memory devices above the 18-bit address range).

Bits 03–00 — Not used.

5.4.3.3 Memory Management Relocation – Figure 5-33 shows how the MMU relocates 16-bit virtual addresses into 22-bit physical addresses.

Refer to *Microcomputers and Memories* for a detailed description of the memory relocation process.

5.4.3.4 Default State After Power-Up – At the completion of the power-up self-test, clearing bit 00 in SR0 disables the MMU. Bit 04 in SR3 is also cleared so 22-bit mapping is not selected.

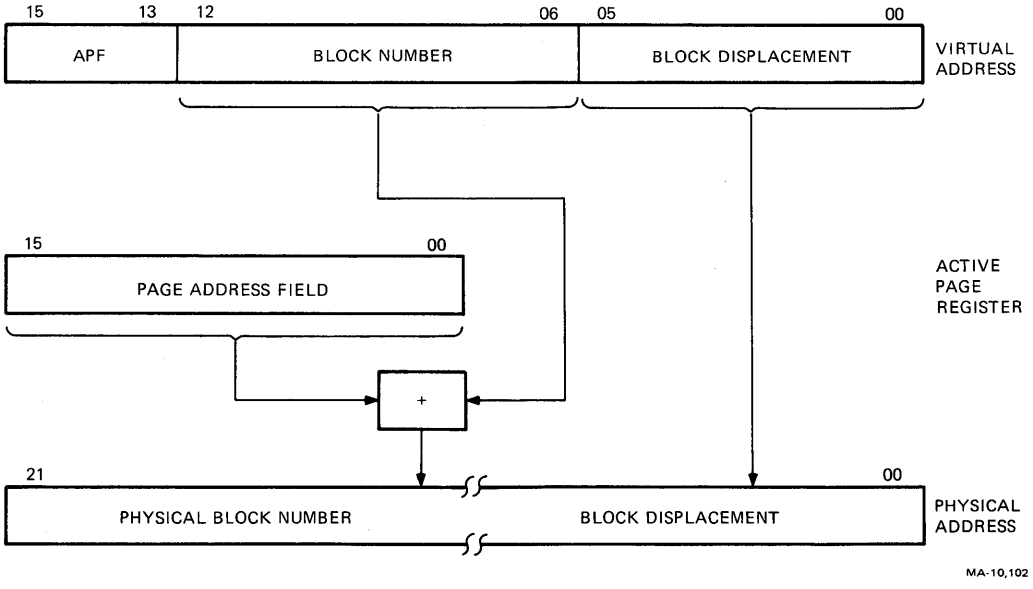


Figure 5-33 Memory Management Relocation

5.4.3.5 Floating Point Precision – The floating point instruction set (FP11) is a microcode option and is contained in the floating point adapter (FPA). Both single and double precision floating point capability are available together with other features including floating-to-integer and integer-to-floating conversion.

The microcode resides in two MOS/LSI chips contained in one 40-pin package (FPA). The FP11 needs the MMU chip and the base MOS/LSI chips because all the floating point accumulators and status registers are in the MMU. The 40-pin FP11 chip is added to the system module by inserting it into the special user-installable IC socket. The chip is mounted on a special carrier which is keyed so that it only fits into the socket in the correct way. This makes adding the option easier than with the usual 40-pin IC socket. It removes the dangers of bending the IC pins during insertion and installing the chip backwards. Figure 5-34 shows the location of the floating point adapter socket on the system board.

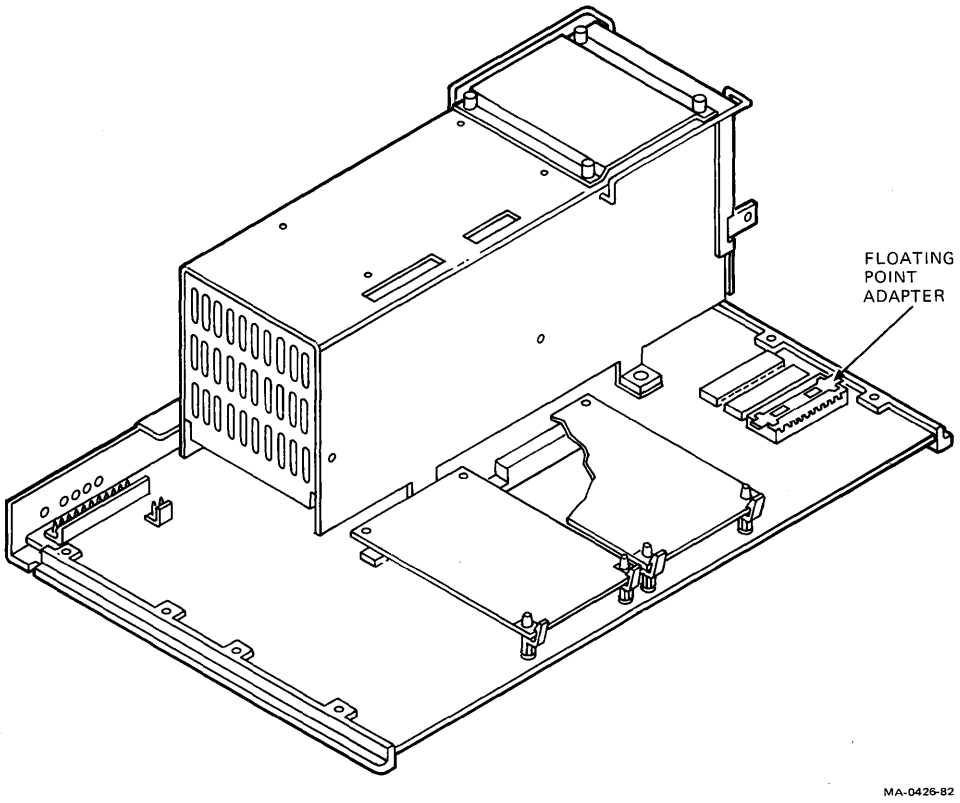


Figure 5-34 Floating Point Adapter Socket Location

5.4.4 Computing Terminal Interconnect (CTI) BUS

The CTI BUS backplane is part of the system module. The backplane is designed to accept option modules using a zero insertion force (ZIF) connector. Six option module slots are provided. Figure 5-35 shows the position of the option slots on the system.

Each option slot has a 90-pin connector on the system module. The first 60 pins are used for the general section of the CTI BUS signals. The last 30 pins; 61 through 90, route signals from the option modules to connectors on the rear of the system module. These are referred to as the private section of the bus. An option module that only needs the CTI BUS signals can use a 60-pin ZIF connector. An option module that uses the rear connectors on the system module can use a 90-pin ZIF connector.

Bus signal timing is discussed in Sections 5.3.3 through 5.3.5. The bus signal descriptions and pin-out are in Section 5.6.

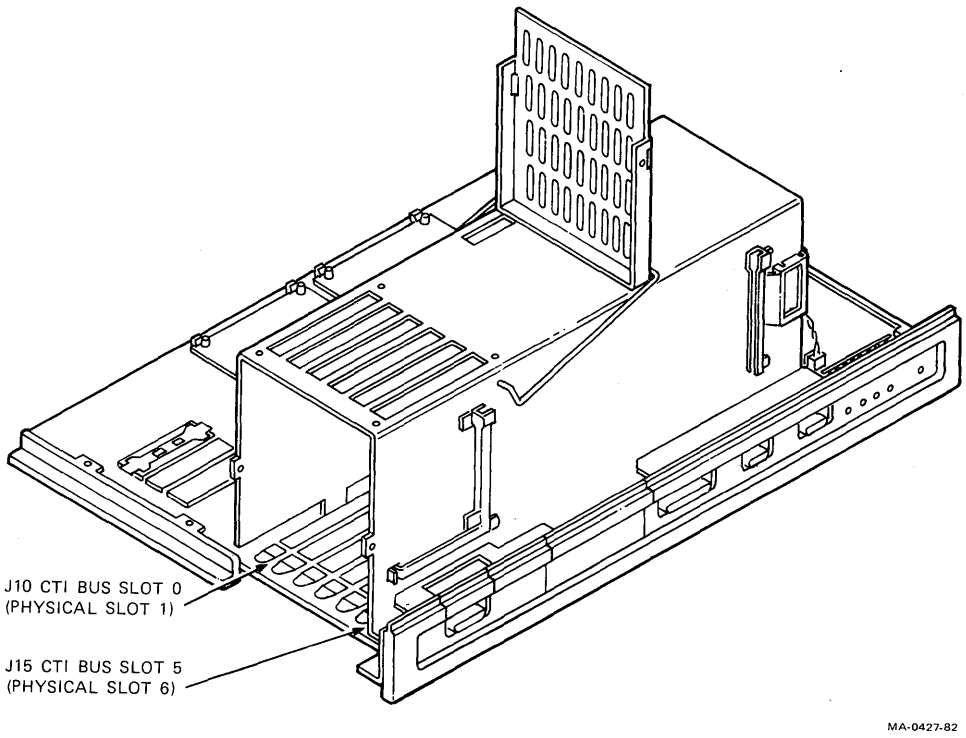


Figure 5-35 CTI BUS Option Slots

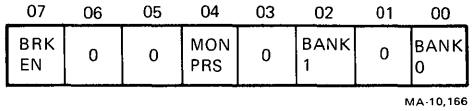
5.4.5 System Control and Status Register (SCSR)

REGISTER OPERATION

Address:

17773700 Control and status register

This register uses only the low byte. The high byte is always read as all zeros and writes to the high byte have no effect. The system control and status register provides certain configuration information and allows the selection of certain modes of operation. The bits in the register function are described in the following paragraphs.



Bit 07 BRK EN – Break Enable. This bit enables hardware break detect on the printer port when that port is used with a terminal. Mode register 1 of the printer port must be initialized before this bit is set. When BRK EN is set, hardware break detection is enabled. When cleared, break detection is disabled. If a printer is connected to the port, break detection is disabled regardless of the state of the BRK EN bit. BRK EN is cleared at power up.

R/W bit.

Bits 06-05 Not used. Always read as zeros.

Read-only bits.

Bit 04 MON PRS – Monitor Present. This is a status bit to indicate that a video monitor is connected to the video interface. MON PRS asserted indicates a monitor is present and cleared indicates no monitor present.

Read-only bit.

Bit 03 Reserved; clear.

Read-only bit.

Bit 02 BANK1. This is a status bit that indicates if a memory module is present in memory option slot 1. It is set when a memory module is present and cleared when no memory module is present.

Read-only bit.

Bit 01 Reserved; clear.

Read-only bit.

Bit 00 BANK0. This is a status bit that indicates if a memory module is present in memory option slot 0. It is set when a memory module is present and cleared when no memory module is present.

Read-only bit.

5.4.5.1 Default State After Power-Up – When the power-up self-test is completed, the firmware sets the break enable bit in the system CS, bit 07. The other bits in the system CSR are read-only and depend upon the memory installed.

5.4.5.2 Indicator (LED) Display – There are five LEDs on the back of the system module. The green one lights when the DCOK signal from the power supply is asserted. The four red ones are error indicators controlled by the power-up self-test. At power up, all four red LEDs are lit. Table 5-13 indicates the error condition for each LED code.

Table 5-13 Indicator (LED) Error Codes

LED 3	LED 2	LED 1	LED 0	Error Condition
off	off	off	off	None – self-test found no errors
off	off	off	on	Bus slot 0 error detected (physical slot 1)
off	off	on	off	Bus slot 1 error detected (physical slot 2)
off	off	on	on	Bus slot 2 error detected (physical slot 3)
off	on	off	off	Bus slot 3 error detected (physical slot 4)
off	on	off	on	Bus slot 4 error detected (physical slot 5)
off	on	on	off	Bus slot 5 error detected (physical slot 6)
off	on	on	on	Invalid – reserved
on	off	off	off	Invalid – reserved
on	off	off	on	Keyboard failed
on	off	on	off	No boot found
on	off	on	on	Monitor cable not present
on	on	off	off	Memory in slots 0 and 1 both failed
on	on	off	on	Memory in slot 1 failed (high bank)
on	on	on	off	Memory in slot 0 failed (low bank)
on	on	on	on	System module failed*

* All the indicators (LEDs) are lit at power-up (lamp test). If they all stay lit, a system module error is indicated.

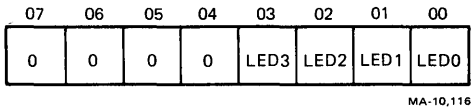
INDICATOR (LED) DISPLAY REGISTER

Address:

17773704 Indicator (LED) Display Register

The LED display register uses only the low byte. The register is always read as all zeros and writes to the high byte have no effect.

The register controls the state of the four red LEDs on the rear of the unit.



Bits 07-04 Not used. Always read as zeros.

Bits 03-00 LED3-LED0. These bits control the state of the four red LEDs on the rear of the unit. Setting one of these bits causes the corresponding LED to be turned off. Clearing a bit causes the corresponding LED to light. All four bits are cleared (lit) at power up. The bits are always read as zeros.

Write-only bits.

5.4.5.3 Indicator Display Default State After Power-Up – The power-up self-test firmware uses the display to indicate any detected errors. At the completion of the self-test, the indicator display contains the code for the first error detected. If no errors were found, the LED display is turned off.

5.4.6 Interrupt Controllers

Each interrupt controller can handle up to eight interrupt requests. Every interrupt in the system is handled by one of the three interrupt controllers. Table 5-14 shows the interrupts that are handled by each controller. Interrupt controller 0 has a higher priority than controller 1 and controller 1 has a higher priority than controller 2.

Within a given controller, the interrupt requests are received at a request level from 0 to 7. Request level 0 is the highest if the controller is programmed for fixed priority arbitration. The eight request levels have basically equal priority if the controller is programmed for rotating arbitration. See bit 00 of the mode register for more detail. Note that bits within certain internal registers correspond to certain request levels. For example, there is an 8-bit interrupt mask register which enables or disables the eight interrupts. Setting bit 02 in the mask register, disables the interrupt at request level 2. Clearing bit 05 in the mask register, enables the interrupt at request level 5. In the Professional 350 system, all interrupts occur at request level 4.

Addresses:

17773200	Interrupt controller 0 data register
17773202	Interrupt controller 0 CSR register
17773204	Interrupt controller 1 data register
17773206	Interrupt controller 1 CSR register
17773210	Interrupt controller 2 data register
17773212	Interrupt controller 2 CSR register

Table 5-14 Interrupt Controller Use

Controller	Request Level		Vector*	Interrupt Description
	0	0	—	Not used
	0	1	200	Keyboard receiver interrupt
highest	0	2	204	Keyboard transmitter interrupt
priority	0	3	210	Communication port interrupt
controller	0	4	214	Modem controls change interrupt
	0	5	220	Printer receiver interrupt
	0	6	224	Printer transmitter interrupt
	0	7	230	Clock interrupt
	1	0	300	Option module 0 interrupt request A
	1	1	310	Option module 1 interrupt request A
	1	2	320	Option module 2 interrupt request A
	1	3	330	Option module 3 interrupt request A
	1	4	340	Option module 4 interrupt request A
	1	5	350	Option module 5 interrupt request A
	1	6	—	Not used
	1	7	—	Not used
	2	0	304	Option module 0 interrupt request B
	2	1	314	Option module 1 interrupt request B
lowest	2	2	324	Option module 2 interrupt request B
priority	2	3	334	Option module 3 interrupt request B
controller	2	4	344	Option module 4 interrupt request B
	2	5	354	Option module 5 interrupt request B
	2	6	—	Not used
	2	7	—	Not used

* These vectors are established at power up by the firmware. The firmware programs the interrupt controllers to contain these vectors. It is highly recommended that these vectors not be changed.

All interrupt controller registers use only the low byte. The high bytes are always read as all zeros and writes to high bytes have no effect.

The remainder of this section describes how these interrupt controllers function. The detail is important at the firmware level to understand the full module operation. However, at higher levels, only a part of the information is necessary and the rest may be scanned. The necessary paragraphs are indicated by an asterisk (*).

Each of the interrupt controllers has a set of registers which controls the specific features of operation. These registers are accessed via the CSR and data registers. The following are the set of registers.

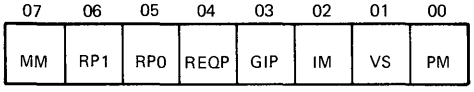
Interrupt Request Register (IRR)* – The IRR is 8-bits long and stores the active transitions on the eight interrupt request lines. A bit in the IRR is set when the corresponding interrupt request line makes the appropriate transition. An IRR bit is cleared when the processor acknowledges its interrupt. The processor can clear or set the IRR bits by writing special commands into the controller CSR. The IRR contents may be read from the controller data register by preselecting it in the mode register (see mode register). The IRR bits are cleared by a Reset.

Interrupt Service Register (ISR) – The ISR is 8-bits long and stores the acknowledge status of the IRR bits. When acknowledged, the controller selects the highest priority request pending, clears the associated IRR bit, and sets the associated ISR bit. When the ISR bit is programmed for automatic clearing (see auto clear register), it is cleared at the end of the acknowledge cycle. If auto clear is not selected, the processor must clear the ISR bit by writing the appropriate command into the controller CSR. The ISR contents may be read from the controller data register by preselecting it in the mode register (see mode register). A RESET clears the ISR bits.

Interrupt Mask Register (IMR) – The IMR is 8-bits long and enables or disables each of the individual interrupt requests. Setting an IMR bit disables the corresponding interrupt request, while clearing an IMR bit enables the corresponding request. Only unmasked IRR bits cause a group interrupt. The state of an IMR bit has no effect on the operation of its IRR bit. The processor can clear or set the IMR bits by writing special commands into the controller CSR. The IMR contents may be read from the controller data register by preselecting it in the mode register (see mode register). The processor loads the IMR by writing a PRESELECT IMR command (see command definition in next section) into the controller CSR followed by a write to the data register. A RESET sets all the IMR bits.

Auto Clear Register (ACR) – The ACR is 8-bits long and specifies the automatic clearing option for each ISR bit. When an ACR bit is set, the corresponding ISR bit is automatically cleared at the end of the acknowledge cycle. When an ACR bit is cleared, the corresponding ISR bit is not cleared at the end of the acknowledge cycle. The processor must clear it by writing a command to the controller CSR. The processor loads the ACR by writing a PRESELECT ACR command (see command definition in next section) into the controller CSR followed by a write to the data register. The ACR contents may be read from the controller data register by preselecting it in the mode register (see mode register). A RESET clears all the ACR bits.

Mode Register – The mode register is 8-bits long and controls many of the controller options. It is loaded by writing commands into the controller CSR (see command definitions in next section). The mode register can not be read. Bits 00, 02, and 07 are available in the controller CSR during read operations. A RESET clears the mode register. The mode register bit functions are as follows.



Bit 07* — MM – Master Mask. When set, it enables group interrupts to the processor. When cleared, it disables group interrupts to the processor.

Bit 06-05* — RP1-RP0 – Register Preselect. These bits determine which internal register will be read when the processor reads the controller data register. The internal register is selected as follows.

RP1	RP0	Register
0	0	Interrupt service register
0	1	Interrupt mask register
1	0	Interrupt request register
1	1	Auto clear register

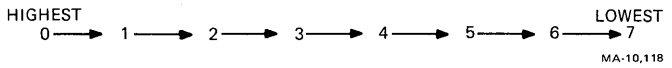
Bit 04 — REQP – Interrupt Request Polarity. This bit determines the active transition for setting IRR bits. When set, an IRR bit is set when the corresponding interrupt request line makes a low to high transition. When cleared, a high to low transition on the interrupt request line sets the IRR bit. This bit should always be cleared because the system hardware provides high to low transitions for all interrupts to all three controllers.

Bit 03 — GIP – Group Interrupt Polarity. This bit determines the polarity of the group interrupt output to the processor. When set, the group interrupt output is asserted high. When cleared, the group interrupt output is asserted low. This bit should always be cleared because the system hardware recognizes active low group interrupts from all three controllers.

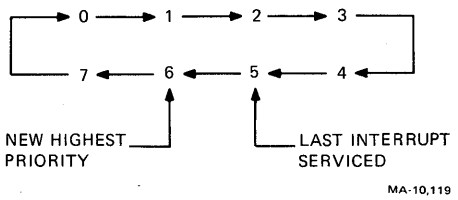
Bit 02 — IM – Interrupt Mode. This bit determines whether the controller is operating in interrupt mode or polled mode. When IM is cleared, interrupt mode is selected and the group interrupt output functions normally. When IM is set, the polled mode is selected and the group interrupt output is disabled so the controller goes not interrupt the processor. In polled mode, the processor can read the controller CSR to see if any interrupt requests are pending. See section on status register.

Bit 01 — VS – Vector Selection. This bit determines whether the controller generates a common vector for all the interrupt requests or an individual vector for each request. The response memory contains eight vectors, one for each request level (see response memory section). When VS is cleared, each interrupt level is associated with its own unique vector in the response memory. When VS is set, all interrupt levels are associated with the vector in the request level 0 response memory location. In this mode, the controller generates the same vector regardless of the interrupt request being acknowledged.

Bit 00 — PM – Priority Mode. This bit determines whether a fixed priority or rotating priority selects the highest pending interrupt request. When cleared, fixed priority is selected. In fixed priority mode, interrupt request line 0 is always the highest level and request line 7 is always the lowest level.



When PM is set, rotating priority is selected. In rotating mode, a circular chain determines the priorities.



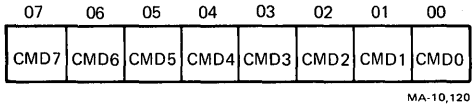
The last interrupt level serviced becomes the lowest priority in the circular chain.

Response Memory – The response memory stores the vectors for each of the eight interrupt requests. The response memory contains eight bytes, one for each vector. The controller, using the response memory, determines which vector to generate in response to a processor interrupt acknowledge. The processor loads the response memory can not be read. The processor loads the response memory by writing a PRESELECT RESPONSE MEMORY command (see command definition in next section) into the controller CSR followed by a write to the data register. The response memory is not effected by a RESET.

All three interrupt controllers program in the same way. The programming and data transfers are all done with two addressable registers: the data register and the CSR register. These two registers are described in the following paragraphs.

5.4.6.1 Control/Status Register (CSR) – The CSR operates as a command register on writes and as a status register on reads. Commands are written into the CSR to select specific controller operation. The CSR can be read to determine specific controller status.

Command Register (CSR – write operations)



Bits 07-00* CMD7-CMD0 – Command. These bits determine the command to the controller. The available commands are given in the following paragraphs.

Write-only bits.

The following commands are available.

* RESET – 0 0 0 0 0 0 0 0
The reset command establishes a known state in the controller. The response memory and byte count registers are not effected. The interrupt mask register is set to all ones. The interrupt request register, interrupt service register, auto clear register, and the mode register are cleared to all zeros.

* CLEAR IRR AND IMR – 0 0 0 1 0 X X X
All bits in the interrupt request register and the interrupt mask register are cleared.

* CLEAR SINGLE IRR AND IMR BIT – 0 0 0 1 1 B2 B1 B0

The bit specified by B2-B0 is cleared in both the interrupt request register and the interrupt mask register.

* CLEAR IMR - 0 0 1 0 0 X X X
The interrupt mask register is cleared to all zeros.

* CLEAR SINGLE IMR BIT - 0 0 1 0 1 B2 B1 B0
The bit specified by B2-B0 is cleared in the interrupt mask register.

* SET IMR - 0 0 1 1 0 X X X
The interrupt mask register is set to all ones.

* SET SINGLE IMR BIT - 0 0 1 1 1 B2 B1 B0
The bit specified by B2-B0 is set in the interrupt mask register.

* CLEAR IRR - 0 1 0 0 0 X X X
The interrupt request register is cleared to all zeros.

* CLEAR SINGLE IRR BIT - 0 1 0 0 1 B2 B1 B0
The bit specified by B2-B0 is cleared in the interrupt request register.

* SET IRR - 0 1 0 1 0 X X X
The interrupt request register is set to all ones.

* SET SINGLE IRR BIT - 0 1 0 1 1 B2 B1 B0
The bit specified by B2-B0 is set in the interrupt request register.

CLEAR HIGHEST PRIORITY ISR BIT - 0 1 1 0 X X X X
The highest priority bit in the interrupt service register is cleared.

CLEAR ISR - 0 1 1 1 0 X X X
The interrupt service register is cleared to all zeros.

CLEAR SINGLE ISR BIT - 0 1 1 1 1 B2 B1 B0
The bit specified by B2-B0 is cleared in the interrupt service register.

LOAD MODE BITS M0 THRU M4 - 1 0 0 M4 M3 M2 M1 M0
The five low order bits of the command are transferred to the five low order bits of the mode register.

* CONTROL MODE BITS M5 THRU M7 - 1 0 1 0 M6 M5 N1 N0
The M5 and M6 bits of the command are transferred to bits 05 and 06 of the mode register. The N0 and N1 bits of the command control bit 07 of the mode register are as follows.

N1	**N0**	
0	0	No change to bit 07 in mode register
0	1	Set bit 07 in mode register
1	0	Clear bit 07 in mode register
1	1	Illegal

*

PRESELECT IMR FOR WRITING – 1 0 1 1 X X X X

Following this command, all write operations to the controller data register load the data into the interrupt mask register. This condition continues until a different preselect command is entered.

PRESELECT ACR FOR WRITING – 1 1 0 0 X X X X

Following this command, all write operations to the controller data register load the data into the auto clear register. This condition continues until a different preselect command is entered.

PRESELECT RESPONSE MEMORY FOR WRITING – 1 1 1 0 0 L2 L1 L0

Following this command, all write operations to the controller data register load the data into a response memory location. L2 through L0 specify which interrupt request level response memory location is loaded as follows.

L2	L1	L0	Level
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

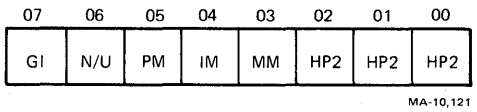
This condition continues until a different preselect command is entered.

NOTE

For the above commands that use B2-B0, the bit specified is as follows.

B2	B1	B0	Bit	
0	**0**	**0**	**0**	**LSB**
0	**0**	**1**	**1**	
0	**1**	**0**	**2**	
0	**1**	**1**	**3**	
1	**0**	**0**	**4**	
1	**0**	**1**	**5**	
1	**1**	**0**	**6**	
1	**1**	**1**	**7**	**MSB**

Status Register (CSR – read operations)



Bit 07

GI – Group Interrupt. When set, it indicates that no unmasked bits are set in the interrupt request register. When cleared, it indicates that at least one unmasked bit is set in the interrupt request register. This bit is valid even when polled mode operation is selected.

Read-only bit.

Bit 06

N/U – Not used.

Read-only bit.

Bit 05

PM – Priority Mode. PM indicates the state of mode register bit 00. When cleared, it indicates fixed priority operation. When set, it indicates rotating priority operation.

Read-only bit.

Bit 04

IM – Interrupt Mode. IM indicates the state of mode register bit 02. When cleared, it indicates that interrupt mode is selected. When set, it indicates that polled mode is selected.

Read-only bit.

Bit 03

MM – Master Mask. MM indicates the state of mode register bit 07. When cleared, it indicates that the controller is disarmed and will not generate a group interrupt to the processor. When set, the controller is armed and group interrupts to the processor can occur.

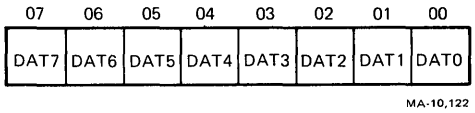
Read-only bit.

Bits 02-00

HP2-HP0 – Highest Pending Interrupt. These bits indicate the highest unmasked request level bit that is set in the interrupt request register. These bits should only be considered valid when the GI bit is cleared. This indicates that at least one unmasked interrupt request is present. The highest pending interrupt is determined by the bits set in the interrupt request register and the priority mode.

Read-only bits.

5.4.6.2 Data Register



Bits 07-00* DAT7-DAT0 – Data. During write operations, the data in this register is transfered to the internal register specified by the last PRESELECT command. The data can be transferred to the interrupt mask register, the auto clear register, or the response memory. During read operations, the contents of one of the internal registers is transferred to the data register. The internal register transferred is determined by the preselect bits in the mode register (bits 06 and 05). The interrupt request register, interrupt service register, interrupt mask register, or the auto clear register may be preselected.

R/W bits.

5.4.6.3 Interrupt Controller Default State After Power Up – The three interrupt controller chips are initialized by the firmware at power up. The state of each controller is programmed as follows.

- Interrupt Controller 0

  IRR = 000 (interrupt request register)
  IMR = 377 (interrupt mask register)
  ACR = 377 (auto-clear register)

  Vector 0 = 234
  Vector 1 = 200
  Vector 2 = 204
  Vector 3 = 210 (response memory)
  Vector 4 = 214
  Vector 5 = 220
  Vector 6 = 224
  Vector 7 = 230

  IMR preselected for reads from data register.
  IMR preselected for writes to data register.
  Fixed priority mode selected.
  Master mask bit set (enabled).

- Interrupt Controller 1

  IRR = 000 (interrupt request register)
  IMR = 377 (interrupt mask register)
  ACR = 377 (auto-clear register)

  Vector 0 = 300
  Vector 1 = 310
  Vector 2 = 320
  Vector 3 = 330 (response memory)
  Vector 4 = 340
  Vector 5 = 350
  Vector 6 = 360
  Vector 7 = 370

  IMR preselected for reads from data register.
  IMR preselected for writes to data register.
  Rotating priority mode selected.
  Master mask bit set (enabled).

- Interrupt Controller 2

  IRR = 000 (interrupt request register)
  IMR = 377 (interrupt mask register)
  ACR = 377 (auto-clear register)

  Vector 0 = 304
  Vector 1 = 314
  Vector 2 = 324
  Vector 3 = 334 (response memory)
  Vector 4 = 344
  Vector 5 = 354
  Vector 6 = 364
  Vector 7 = 374

  IMR preselected for reads from data register.
  IMR preselected for writes to data register.
  Rotating priority mode selected.
  Master mask bit set (enabled).

5.4.7 Direct Memory Access (DMA)

The bus and the system module permit direct memory access by the option modules. A DMA device requests the bus from the CPU by asserting its DMA request line, DMR n L. The DMA device becomes the bus master when it receives a grant from the CPU on its DMA grant line, DMG n L. The DMA devices and the system module each perform part of the DMA arbitration. DMA devices monitor the bus DMA priority lines, BP 0 L and BP 1 L, and only request the bus if they are at the current DMA priority level or higher. The system module arbitrates between the DMA devices that are requesting the bus and the CPU. DMA devices always have priority over the CPU and are granted the bus when the processor completes any bus cycle already in progress. When multiple DMA devices at a specific DMA priority level request the bus at the same time, the arbitor grants the bus to the one in the lowest numbered slot, for example, slot 0 is selected before slot 3. If a DMA device does not assert the BUS BUSY signal in response to its grant within the permitted time (see Section 5.6), the system module removes the grant and continues.

All the signals are bused through all six slots with the exception of six signals. The six non-bused signals provide slot dependent signals to the system module for handling address decoding, interrupts, and DMA. These signals are as follows.

OPRES n L	Option present indicator
SS n L	Slot select from address decoder
IRQA n L	Interrupt request A from option
IRQB n L	Interrupt request B from option
DMR n L	DMA request from option
DMG n L	DMA grant from arbiter

where n = slot number (0-5)

5.4.7.1 Option Module Addresses – Each option module is allocated 128 bytes in the I/O page. The system module decodes the addresses and asserts a slot select (SS) to the appropriate option module if an option module address is detected. Table 5-15 shows the byte addresses for each option module.

NOTE

DMA devices may address the option modules. In this condition, the system module decodes the address output by the DMA device and asserts a slot select to the appropriate option module if an option module address is detected.

5.4.7.2 Option Module Vectors – Each option module has two interrupt request lines so each slot needs two vectors. Table 5-16 shows the vectors for the option module interrupts.

All interrupt vectors are soft because they can be programmed to any 8-bit number in the interrupt controller chips (see Section 5.4.6). However, the vectors given are established at power up by the firmware. It is highly recommended that the vectors not be changed.

Table 5-15 Option Slot Addresses

Slot	I/O Page Addresses
0	17774000–17774177
1	17774200–17774377
2	17774400–17774577
3	17774600–17774777
4	17775000–17775177
5	17775200–17775377

Table 5-16 Option Slot Vectors

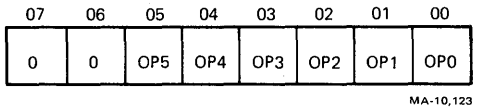
Slot	Interrupt Request Vector A	Interrupt Request Vector B
0	300	304
1	310	314
2	320	324
3	330	334
4	340	344
5	350	354

5.4.7.3 Option Module Present Register (OMPR)

Address:

17773702 Data buffer

The option module present register indicates which of the six option module slots contains a module. It is a read only register which uses only the low byte. The high byte is read as all zeros and all writes to the register have no effect.



Bits 07-06 Not used. Always read as zeros.

Read-only bits.

Bits 05-00 OP5-OP0 – Option Present. A one in an OP bit indicates that a module is present in the corresponding option module slot. For example, if OP1 is set, a module is present in option module slot 1. A zero in an OP bit indicates no module is present in the corresponding slot.

Read-only bits.

5.4.8 ROM

The system module contains 16 kilobytes of ROM. It contains the power-up self-test code, configuration and initialization code, and the boot code. Table 5-16 shows that some of the ROM is in the I/O page and some is in the memory address space. Any attempt to write to the ROM locations results in a nonexistent memory trap to location 4.

Refer to Section 5.2.3.4 for a description of the system power-up self-test.

5.4.8.1 ID PROM – Each system module board contains a PROM with a unique 32-byte ID.

Addresses:

17773600–17773676 32 bytes PROM

All 32 word locations use only the low byte. The high bytes are always read as all zeros. Any attempt to write to the ID PROM locations results in a non-existent memory trap to location 4.

The ID code is a 12-BCD digit (6-byte) random number. The ID PROM should be blasted with the ID as shown in Table 5-17.

Table 5-17 ROM Address Space

Address	Size	Location
17730000–17757777	12 kilobytes	memory space
17760000–17767777	4 kilobytes	I/O page

OCTAL PROM ADDRESS	PROM CONTENTS	22-BIT SYSTEM ADDRESS
00	RANDOM ID BYTE 1	17773600
01	RANDOM ID BYTE 2	17773602
02	RANDOM ID BYTE 3	17773604
03	RANDOM ID BYTE 4	17773606
04	RANDOM ID BYTE 5	17773610
05	RANDOM ID BYTE 6	17773612
06	ERROR CHK BYTE 1*	17773614
07	ERROR CHK BYTE 2*	17773616
10	RANDOM ID BYTE 1	17773620
11	RANDOM ID BYTE 2	17773622
12	RANDOM ID BYTE 3	17773624
13	RANDOM ID BYTE 4	17773626
14	RANDOM ID BYTE 5	17773630
15	RANDOM ID BYTE 6	17773632
16	ERROR CHK BYTE 1*	17773634
17	ERROR CHK BYTE 2*	17773636
20	RANDOM ID BYTE 1	17773640
21	RANDOM ID BYTE 2	17773642
22	RANDOM ID BYTE 3	17773644
23	RANDOM ID BYTE 4	17773646
24	RANDOM ID BYTE 5	17773650
25	RANDOM ID BYTE 6	17773652
26	ERROR CHK BYTE 1*	17773654
27	ERROR CHK BYTE 2*	17773656
30	00000000	17773660
31	11111111	17773662
32	01010101	17773664
33	10101010	17773666
34	11111111	17773670
35	00000000	17773672
36	ERROR CHK BYTE 3†	17773674
37	ERROR CHK BYTE 4†	17773676

* CHECK BYTES 1 AND 2 FORM A WORD CHECK ON THE PREVIOUS 6 BYTES

† CHECK BYTES 3 AND 4 FORM A WORD CHECK ON THE ENTIRE PROM

MA-10,163

5.4.9 RAM

The module contains support circuitry for two memory option modules. There are two 40-pin connectors on the system module to accept the memory modules. Figure 5-36 shows the position of the memory option modules. Refer to Table 5-22 for the memory connects pinning.

Additional memory can be installed in the backplane if needed. Memory added in the backplane requires its own support circuitry. The memory option module is a 128 kilobyte module containing 16 64K × 1 dynamic RAMs.

When both slots contain memory boards, the memory in slot 0 always starts at address 00000000 and the memory in slot 1 starts where the first one ends (Table 5-18).

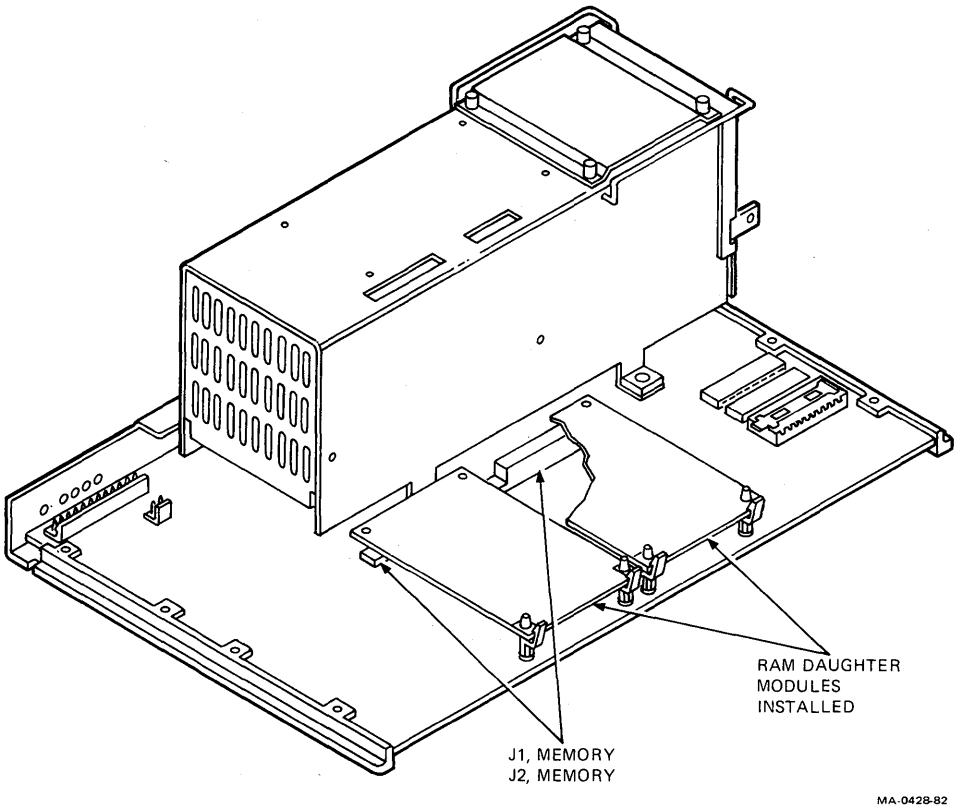


Figure 5-36 Memory Option Sets

Table 5-18 Memory Configurations

Slot 0	Slot 1	Memory	Address Range
128 kilobytes	0	128 kilobytes	00000000–00377777
0	128 kilobytes	128 kilobytes	00000000–00377777
128 kilobytes	128 kilobytes	256 kilobytes	00000000–00777777

The system control and status register (at 17773700) can be read to determine the memory configuration. Bits 03-00 should be interpreted as follows.

Bit	State	Meaning
00	0	No memory module present in memory slot 0.
00	1	Memory slot 0 contains a memory module.
01	0	The memory module in slot 0 is 128 kilobytes.
01		Reserved
02	0	No memory module present in memory slot 1.
02	1	Memory slot 1 contains a memory module.
03	0	The memory module in slot 1 is 128 kilobytes.
03		Reserved

The system module has circuits for address decoding and multiplexing, for timing, and for cycle-stealing refresh.

5.4.10 Keyboard

There is a serial keyboard port on the system module. It can perform asynchronous serial communications at programmable baud rates up to 19.2 kilobaud. The port uses EIA RS-423 signal levels and connection is made on the rear of the unit via a 15-pin male D-subminiature connector, J5. Section 5.6 shows the pinning of J5 on the system module.

This port is included primarily to communicate with the Professional 300 series keyboard. However, it is a general serial port that can be used to communicate with any serial device. The mode of operation is completely programmable as described in the following paragraphs. When using the port with the Professional 300 series keyboard, the mode must be set to the following.

- 8-bit character length
- No parity
- One stop bit
- 4800 baud clock rate

5.4.10.1 Keyboard Interface

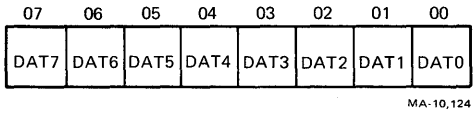
Addresses:

17773500	Data buffer register
17773502	Status register
17773504	Mode registers
17773506	Command register

Vectors:

200	Receiver
204	Transmitter

All the keyboard port registers use only the low byte. The high bytes are always read as all zeros and writes to high bytes have no effects. This port is not a standard DL type interface.

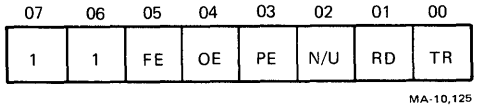


Bits 07-00

DAT7-DAT0 – Data. On read operations, this register operates as the receiver holding register and contains the last received character. The character is right justified if the character length is less than eight bits. On write operations, this register serves as the transmitter holding register and should be loaded with the next character to be transmitted.

R/W bits.

Status Register (STAT)



Bits 07-06

Not used. Always read as ones.

Read-only bits.

Bit 05

FE – Framing Error. When set, it indicates that the received character was not framed by the programmed number of stop bits. If the received character is all zeros and FE is set, a break condition was detected. When cleared, FE indicates that the received character was correctly framed. FE is cleared by disabling the receiver or by a Reset Error command in the command register (see section on command register).

Read-only bit.

Bit 04

OE – Overrun Error. When set, it indicates that the previous character loaded into the receiver holding register was not read by the processor by the time that a new received character was loaded into it. When cleared, no overrun condition occurred. OE is cleared by disabling the receiver or by a Reset Error command in the command register (see section on command register).

Read-only bit.

Bit 03

PE – Parity Error. When set, it indicates that the received character had a parity error. When cleared, no parity error was detected. This bit only functions when parity is enabled (see section on mode register). PE is cleared by disabling the receiver or by a Reset Error command in the command register (see section on command register).

Read-only bit.

Bit 02 — N/U – Not used.

Read-only bit.

Bit 01 — RD – Receiver Done. When set, it indicates that a character was received and loaded into the receiver holding register for the processor to read. When cleared, it indicates that no new character was loaded into the receiver holding register. RD is cleared by reading the receiver holding register or by disabling the receiver in the command register (see section on command register). RD is not set when characters are received if remote loopback mode is enabled in the command register (see section on command register).

Read-only bit.

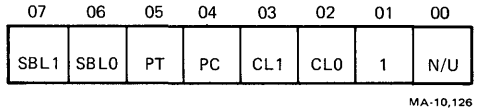
Bit 00 — TR – Transmitter Ready. TR is only valid when the transmitter is enabled in the command register (see section on command register). When TR is cleared, it indicates that the transmitter holding register is not ready to receive another character for transmission from the processor. When set, it indicates that the processor may load the next character for transmission into the transmitter holding register. TR is cleared when operating in auto echo or remote loopback modes (see section on command register).

Read-only bit

Mode Registers (MR1 AND MR2)

There are two mode registers that select the operating mode of the keyboard port. Both registers reside at the same address. Operations (read or write) to a mode register cause an internal pointer to point to the other mode register for the next operation. Reading the command register always causes the internal pointer to point to mode register 1. Both mode registers are cleared when system power is turned on. The processor has to initialize both registers to the specified mode of operation. The two mode registers are in the following paragraphs.

Mode Register 1 (MR1)



Bits 07-06 — SBL1-SBL0 – Stop Bit Length. These bits select character framing of 1, 1.5, or 2 stop bits for both the transmitter and the receiver. The stop bits are selected as follows.

SBL1	SBL0	Stop	Bit Length
0	0	0	Invalid
0	1	1	Stop bit
1	0	1.5	Stop bits
1	1	2	Stop bits

R/W bits.

Bit 05

PT – Parity Type. When set, PT selects even parity. When cleared, PT selects odd parity. Parity type is the same for the transmitter and the receiver. This bit has no effect if parity is not enabled (see PC bit).

R/W bit.

Bit 04

PC – Parity Control. When cleared, parity is disabled for the transmitter and the receiver. When set, the transmitter adds a parity bit to the transmitted character and the receiver performs a parity check on incoming characters. The PT bit selects odd or even parity.

R/W bit.

Bits 03-02

CL1-CL0 – Character Length. These bits select the number of data bits per character for the transmitter and the receiver. The character length does not include the parity bit (if any), the start bit, or the stop bits. Character length is selected as follows.

CL1	CL0	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

R/W bits.

Bit 01

1. – This bit must always be set to a one for correct operation. When the system power is turned on, this bit is cleared. The processor must set it to a one before using the keyboard port.

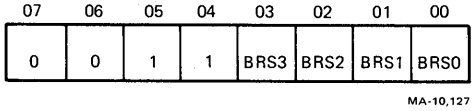
R/W bit.

Bit 00

N/U – Not used.

R/W bit.

Mode Register 2 (MR2)



Bits 07-04

0011 – These bits must always be programmed to 0011 for correct operation. When the system power is turned on, these bits are cleared. The processor must program them before using the keyboard port.

R/W bit.

Bits 03-00

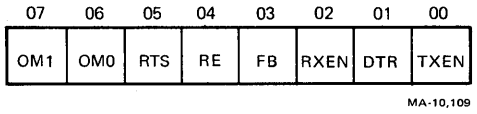
BRS3-BRS0 – Baud Rate Select. These bits determine the frequency of the internal baud rate generator. The frequency is 16 times the selected baud rate. These bits select the clock for both the transmitter and receiver. The accuracy of the input frequency to the baud rate generator is ± 0.01 %. The baud rate is selected as follows.

BRS3	BRS2	BRS1	BRS0	Baud Rate	Baud Rate Generator Percent Error
0	0	0	0	50	–
0	0	0	1	75	–
0	0	1	0	110	–
0	0	1	1	134.5	+0.016
0	1	0	0	150	–
0	1	0	1	300	–
0	1	1	0	600	–
0	1	1	1	1200	–
1	0	0	0	1800	–
1	0	0	1	2000	+0.253
1	0	1	0	2400	–
1	0	1	1	3600	–
1	1	0	0	4800	–
1	1	0	1	7200	–
1	1	1	0	9600	–
1	1	1	1	19200	+3.125

R/W bits.

Command Register (CMD)

The command register also controls the keyboard port operator. The command register is cleared when system power is turned on. The processor has to initialize the register to the specified mode of operation. The command register is described in the following paragraphs.



Bits 07-06

OM1-OM0 – Operating Mode. These bits select the operating mode of the port as follows.

OM1	OM0	Operating Mode
0	0	Normal operation
0	1	Automatic echo mode
1	0	Local loopback
1	1	Remote loopback

These modes are described in the following paragraphs.

Normal – The transmitter and receiver operate independently according to the mode and status registers.

Automatic Echo – Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver continues to assert Receiver Done each time a character is received but the transmitter no longer asserts Transmitter Ready. Only the first character of a break condition is echoed. The transmitter goes to the mark state until the next valid start is detected.

Local Loopback – In this mode, the transmitter output is internally connected to the receiver input. The external transmitter output is held in the mark state. The transmitter must be enabled but the receiver need not be enabled (see RxEN and TxEN bits). The DTR and RTS bits must both be set for local loopback to function correctly.

Remote Loopback – Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver no longer asserts Receiver Done each time a character is received and the transmitter no longer asserts Transmitter Ready. Only the first character of a break condition is echoed. The transmitter goes to the mark state until the next valid start is detected. The error status bits, PE, OE, and FE still function in this mode.

R/W bits.

Bit 05 RTS – Request To Send. There is no external hardware support for this signal. However, it must be set for local loopback mode to function correctly (see OM1-OM0 bits).

R/W bit.

Bit 04 RE – Reset Error. Setting RE causes the error bits, PE, OE, and FE in the status register to be cleared. It is always read as a zero. Write-once bit.

Bit 03 FB – Force Break. When cleared, normal transmitter operation occurs. When set, the transmitter output signal enters and holds the space condition at the end of the current transmitted character.

R/W bit.

Bit 02 RxEN – Receiver Enable. When set, the receiver is enabled for normal operation. When cleared, the receiver immediately terminates operation and clears Receiver Done. Disabling the receiver, clears the error bits PE, OE, and FE in the status register.

R/W bit.

Bit 01 DTR – Data Terminal Ready. There is no external hardware support for this signal. However, it must be set for local loopback mode to function correctly (see OM1-OM0 bits).

R/W bit.

Bit 00	TxEN – Transmitter Enable. When set, the transmitter is enabled for normal operation. When cleared, the transmitter is disabled. If the transmitter is disabled, it completes transmitting any character that was already begun before terminating operation (not a character pending in the transmitter holding register). When disabled, the transmitter output stays in the mark state and the transmitter ready bit is cleared. R/W bit.

5.4.10.2 Keyboard Default State After Power-Up – After the power-up self-test is completed, the firmware initializes the keyboard port as follows.

Mode Register 1

1 stop bit
Parity disabled
8-bits per character

Mode Register 2

4800 baud

Command Register

Normal operation
RTS enabled
Force break disabled
Receiver enabled
DTR enabled
Transmitter enabled

5.4.11 Printer

There is a serial printer port on the system module. It can perform asynchronous serial communications at programmable baud rates up to 19.2 kilobaud. The port uses EIA RS-423 signal levels and connection is made on the rear of the unit via a 9-pin male D-subminiature connector, J6. Section 5.6 shows the pinning and position of J6 on the system module. The printer cable part number is PN BCC05.

5.4.11.1 Printer Port Interface –

Addresses:

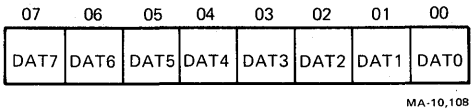
17773400	Data buffer register
17773402	Status register
17773404	Mode registers
17773406	Command register

Vectors:

220	Receiver
224	Transmitter

All the printer port registers use only the low byte. The high bytes are always read as all zeros and writes to high bytes have no effects. This port is not a standard DL type interface. It can be made to look like a standard DL interface without the interrupt enable bits at the terminal address of 17777560. See Section 5.4.15 on maintenance terminal registers.

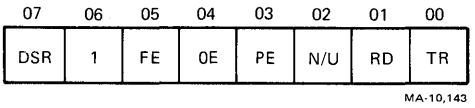
Data Buffer Register (DBUF)



Bits 07-00 DAT7-DAT0 – Data. On read operations, this register operates as the receiver holding register and contains the last received character. The character is right justified if the character length is less than eight bits. On write operations, this register operates as the transmitter holding register and should be loaded with the next character to be transmitted.

R/W bits.

Status Register (STAT)



Bit 07 DSR – Data Set Ready. This bit shows the state of the DSR signal input and can be used to determine that the printer is connected and ready. When DSR is set, it indicates that the DSR signal input is asserted and the printer is present and ready. When DSR is cleared, it indicates that the DSR signal input is not asserted and the printer is either not present or not ready.

Read-only bit.

Bit 06 Not used. Always read as a one.

Read-only bit.

Bit 05 FE – Framing Error. When set, it indicates that the received character was not framed by the programmed number of stop bits. If the received character is all zeros and FE is set, a break condition was detected. When cleared, FE indicates that the received character was correctly framed. FE can be cleared by disabling the receiver or by a Reset Error command in the command register. See section on command register.

Read-only bit.

Bit 04 OE – Overrun Error. When set, it indicates that the previous character loaded into the receiver holding register was not read by the processor by the time that a new received character was loaded into it. When cleared, no overrun condition occurred. OE can be cleared by disabling the receiver or by a Reset Error command in the command register. See the section on command register.

Read-only bit.

Bit 03 — PE – Parity Error. When set, it indicates that the received character had a parity error. When cleared, no parity error was detected. This bit functions when parity is enabled. See section on mode register. PE can be cleared by disabling the receiver or by a Reset Error command in the command register. See the section on command register.

Read-only bit.

Bit 02 — N/U – Not used.

Read-only bit.

Bit 01 — RD – Receiver Done. When set, it indicates that a character was received and loaded into the receiver holding register for the processor to read. When cleared, it indicates that no new character was loaded into the receiver holding register. RD can be cleared by reading the receiver holding register or by disabling the receiver in the command register. See the section on command register. If remote loopback mode is enabled in the command register, RD is not set when characters are received. See the section on command register.

Read-only bit.

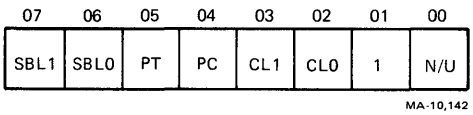
Bit 00 — TR – Transmitter Ready. TR is only valid when the transmitter is enabled in the command register. See the section on command register. When TR is cleared, it indicates that the transmitter holding register is not ready to receive another character for transmission from the processor. When set, it indicates that the processor may load the next character for transmission into the transmitter holding register. TR is cleared when operating in auto echo or remote loopback modes. See the section on command register.

Read-only bit.

Mode Registers (MR1 AND MR2)

There are two mode registers that select the operating mode of the printer port. Both registers reside at the same address. Operations (read or write) to a mode register cause an internal pointer to point to the other mode register for the next operation. Reading the command register always causes the internal pointer to point to mode register 1. Both mode registers are cleared when system power is turned on. The processor has to initialize both registers to the specified mode of operation. The two mode registers are described in the following paragraphs.

Mode Register 1 (MR1)



Bits 07-06

SBL1-SBL0 – Stop Bit Length. These bits select character framing of 1, 1.5, or 2 stop bits for both the transmitter and the receiver. The stop bits are selected as follows.

SBL1	SBL0	STOP	Bit Length
0	0		Invalid
0	1	1	Stop bit
1	0	1.5	Stop bits
1	1	2	Stop bits

R/W bits.

Bit 05

PT – Parity Type. When set, PT selects even parity. When cleared, PT selects odd parity. Parity type is the same for the transmitter and the receiver. This bit has no effect if parity is not enabled (see PC bit).

R/W bit.

Bit 04

PC – Parity Control. When cleared, parity is disabled for the transmitter and the receiver. When set, the transmitter adds a parity bit to the transmitted character and the receiver performs a parity check on incoming characters. The PT bit selects odd or even parity.

R/W bit.

Bits 03-02

CL1-CL0 – Character Length. These bits select the number of data bits per character for the transmitter and the receiver. The character length does not include the parity bit if any, the start bit, or the stop bits. Character length is selected as follows.

CL1	CL0	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

R/W bits.

Bit 01

1 – This bit must always be set to a one for correct operation. When the system power is turned on, this bit is cleared. The processor must set it to a one before attempting to use the printer port.

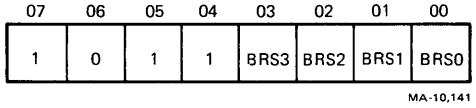
R/W bit.

Bit 00

N/U – Not used.

R/W bit.

Mode Register 2 (MR2)



Bits 07-04

1011 – These bits must always be programmed to 1011 for correct operation. When the system power is turned on, these bits are cleared. The processor must program them before attempting to use the printer port.

R/W bit.

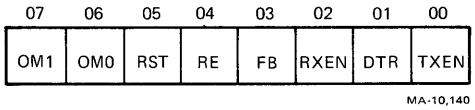
Bits 03-00

BRS3-BRS0 – Baud Rate Select. These bits determine the frequency of the internal baud rate generator. The frequency is 16 times the selected baud rate. These bits select the clock for both the transmitter and receiver. The accuracy of the input frequency to the baud rate generator is ± 0.01 %. The baud rate is selected as follows.

BRS3	BRS2	BRS1	BRS0	Baud Rate	Baud Rate Generator Percent Error
0	0	0	0	50	–
0	0	0	1	75	–
0	0	1	0	110	–
0	0	1	1	134.5	+0.016
0	1	0	0	150	–
0	1	0	1	300	–
0	1	1	0	600	–
0	1	1	1	1200	–
1	0	0	0	1800	–
1	0	0	1	2000	+0.253
1	0	1	0	2400	–
1	0	1	1	3600	–
1	1	0	0	4800	–
1	1	0	1	7200	–
1	1	1	0	9600	–
1	1	1	1	19200	+3.125

R/W bits.

Command Register (CMD)
The command register also controls the printer port operator. The command register is cleared when system power is turned on. The processor has to initialize the register to the specified mode of operation. The command register is described in the following paragraphs.



Bits 07-06 OM1-OM0 – Operating Mode. These bits select the operating mode of the port as follows.

OM1	OM0	Operating Mode
0	0	Normal operation
0	1	Automatic echo mode
1	0	Local loopback
1	1	Remote loopback

These modes are described in the following paragraphs.

Normal – The transmitter and receiver operate independently according to the mode and status registers.

Automatic Echo – Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver continues to assert Receiver Done each time a character is received but the transmitter no longer asserts Transmitter Ready. Only the first character of a break condition is echoed. The transmitter goes to the mark state until the next valid start is detected.

Local Loopback – In this mode, the transmitter output is connected to the receiver input internally. The external transmitter output is held in the mark state. The transmitter must be enabled but the receiver need not be enabled (see RxEN and TxEN bits). The DTR and RTS bits must both be set for local loopback to function correctly.

Remote Loopback – Characters received in the receiver holding register are automatically loaded into the transmitter holding register and transmitted. The receiver must be enabled but the transmitter need not be enabled (see RxEN and TxEN bits). The receiver no longer asserts Receiver Done each time a character is received and the transmitter no longer asserts Transmitter Ready. Only the first character of a break condition is echoed. The transmitter goes to the mark state until the next valid start is detected. The error status bits, PE, OE, and FE still function in this mode.

R/W bits.

Bit 05

RTS – Request To Send. There is no external hardware support for this signal. However, it must be set for local loopback mode to function correctly (see OM1-OM0 bits).

R/W bit.

Bit 04

RE – Reset Error. Setting RE clears the error bits, PE, OE, and FE in the status register. It is always read as a zero. Write-once bit.

Bit 03

FB – Force Break. When cleared, normal transmitter operation occurs. When set, the transmitter output signal enters and holds the space condition at the end of the current transmitted character.

R/W bit.

Bit 02

RxEN – Receiver Enable. When set, the receiver is enabled for normal operation. When cleared, the receiver immediately terminates operation and clears Receiver Done. Disabling the receiver clears the error bits, PE, OE, and FE in the status register.

R/W bit.

Bit 01

DTR – Data Terminal Ready. When set, the Data Terminal Ready signal is asserted on the printer port connector. When cleared, the DTR signal is not asserted on the printer connector. This bit must be set for local loopback mode to function correctly (see OM1-OM0 bits).

R/W bit.

Bit 00

TxEN – Transmitter Enable. When set, the transmitter is enabled for normal operation. When cleared, the transmitter is disabled. If the transmitter is disabled, it completes the transmitting any character that was already begun before terminating operation (not a character pending in the transmitter holding register). When disabled, the transmitter output stays in the mark state and the transmitter ready bit is not asserted.

R/W bit.

5.4.11.2 Printer Default State After Power-Up – After the power-up self-test has completed, the firmware initializes the printer port as follows.

Mode Register 1

1 stop bit
Parity disabled
8-bits per character

Mode Register 2

4800 baud (9600 baud if terminal cable is attached)

Command Register

Normal operation
RTS enabled
Force break disabled
Receiver enabled
DTR enabled
Transmitter enabled

5.4.12 Communications

A communication port on the system module operates in asynchronous and bit or byte synchronous protocols. In asynchronous mode, it can be run at split programmable baud rates up to 19.2 kilobaud. In synchronous mode, it can run up to 740 kilobaud. The transmitter is double buffered and the receiver is quad buffered. A full set of modem controls is also present. All the port signals are EIA RS-423 levels. Connection is made on the rear of the unit via a 25-pin male D-subminiature connector, J7. Section 5.6 shows the pinning and position of J7 on the system module.

There are two interrupts associated with the communications port. The first interrupts the CPU if the USART chip needs service for the receiver or transmitter. The second interrupt indicates that a state change has occurred on one of four modem control signals. These four modem control signals are Ring Indicator (RI), Data Set Ready (DSR), Clear To Send (CTS), and Carrier Detect (CD).

5.4.12.1 Communication Port Interface –

Addresses:

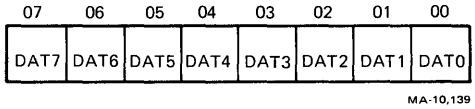
17773300	Data buffer register
17773302	Control/status register A
17773304	Reserved
17773306	Control/status register B
17773310	Modem Control register 0
17773312	Modem control register 1
17773314	Baud rate register

Vectors:

210	Receive/transmit
214	Modem change

All the communication port registers use only the low byte. The high bytes are always read as all zeros and writes to the high bytes have no effects. The reserved register (17773304) responds to read and write accesses but reads always produce all zeros and writes have no effect. The other registers are described in the following paragraphs.

Data Buffer Register



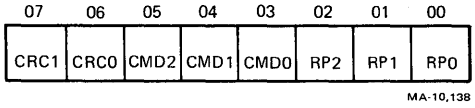
Bits 07–00 DAT7-DAT0 – Data. On read operations, this register contains data bytes received by the communication port. The receiver has a three byte buffer for holding received characters. On write operations, this register operates as a transmitter holding register and should be loaded with the next character to be transmitted.

R/W bits.

Control/Status Register A

This register operates as a window to 11 internal registers. The internal registers are eight write registers and three read registers. The write registers are labeled WR0-WR7 and control the different operating modes of the communication port. The read registers are labeled RR0-RR2 and provide status information. An internal pointer register selects which command or status registers to be read or written during an access to control/status register A. After reset, the pointer register contents are zero. The first write to the control/status register loads the data into WR0. The three least significant bits of WR0 operate as the pointer register. The next access to the control/status register accesses the internal register selected by the pointer register. The pointer is reset after the read or write operation is completed.

Write Register 0 (WR0)



Bits 07–06 CRC1-CRC0 – CRC Reset Code. When written, these bits have the following effect.

CRC1	CRC0	Effect
0	0	Null – no effect.
0	1	Resets receive CRC checker – resets the CRC checker to zeros. If in SDLC mode the CRC checker is set to all ones.
1	0	Resets transmit CRC generator – resets the CRC generator to zeros. If in SDLC mode, the CRC generator is set to all ones.
1	1	Resets Transmitter Underrun/End of Message Latch.

Write-only bits.

Bits 05–03

CMD2-CMD0 – Command Bits. These bits determine which of seven commands to perform.

Command (octal)	Effect
0	Null – no effect.
1	Send Abort – generates eight to thirteen ones when in SDLC mode.
2	Reset External/Status Interrupts – resets the latched status bits of RR0 and reenables them, allowing interrupts to occur again.
3	Channel Reset – resets the latched status bits of RR0, the interrupt priority logic, and all control registers in the channel. Allow two microseconds for the channel reset time before any additional commands or controls are written into the channel.
4	Enable Interrupt on Next Receive Character – if the interrupt on first receive character mode is selected, this command reactivates that mode again after each complete message is received to prepare for the next message.
5	Reset Transmitter Interrupt Pending – if the transmit interrupt enable mode is selected, the channel automatically interrupts when the transmit buffer becomes empty. When there are no more characters to be sent, issuing this command prevents additional transmitter interrupts until the next character has been completely sent.
6	Error Reset – error latches, parity, and overrun errors in RR1 are reset.
7	End of Interrupt – resets the interrupt-in-service latch of the highest priority internal device under service and allows lower priority devices to interrupt.

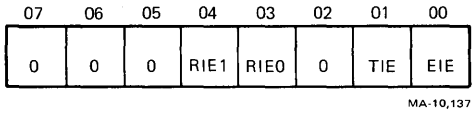
Write-only bits.

Bits 02–00

RP2-RP0 – Register Pointer bits. These bits determine which write register the next byte is written into or which read register the next byte is read from. After reset, the first byte written goes into WR0. Following a read or a write to any register (except WR0) the pointer points to WR0.

Write-only bits.

Write Register 1 (WR1)



Bits 07–05 N/U – Not used. Must always be written as zeros.

Write-only bits.

Bits 04–03 RIE1-RIE0 – Receiver Interrupt Enable bits. These bits enable receiver interrupts in the following modes.

RIE1	RIE0	Function
0	0	Disables receiver and special condition interrupts.
0	1	Enables interrupt on first received character only or special condition.
1	0	Enables interrupt on all receive characters or special condition (parity error is a special receive condition).
1	1	Enables interrupt on all receive characters or special condition (parity error is not a special receive condition).

Write-only bits.

Bit 02 N/U – Not used. Must always be written as zero.

Write-only bit.

Bit 01 TIE – Transmitter Interrupt Enable. When set, it allows transmitter interrupts to occur when the transmitter buffer is empty. When cleared, no transmitter interrupts occur.

Write-only bit.

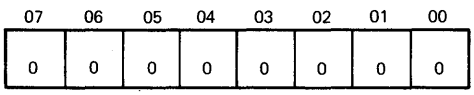
Bit 00 EIE – External Interrupt Enable. When set, it allows interrupts when one of the following occur.

Entering or leaving synchronous hunt phase
Break detection or termination
SDLC abort detection or termination
Idle/CRC latch becoming set (CRC being sent)

When cleared, no such interrupt occurs.

Write-only bit.

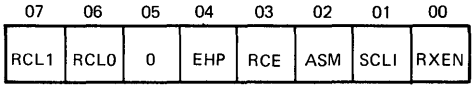
Write Register 2 (WR2)



Bits 07–00 N/U – Not used. If this register is written, it must be written with all zeros.

Write-only bits.

Write Register 3 (WR3)



Bits 07–06 RCL1-RCL0 – Receiver Character Length. These bits determine the receiver character length as follows.

RCL1	RCL0	Data Bits/Character
0	0	5
0	1	7
1	0	6
1	1	8

Write-only bits.

Bit 05 N/U – Not used. Must be written as zero.

Write-only bit.

Bit 04 EHP – Enter Hunt Phase. After initialization, the channel automatically enters the hunt mode. If synchronization is lost, the hunt phase may be reentered by writing a one to this bit.

Write-only bit.

Bit 03 RCE – Receiver CRC Enable. Writing a one to this bit enables (or reenables) CRC calculation. CRC calculation starts with the last character placed in the receiver buffer. Writing a zero to this bit disables but does not reset the receiver CRC generator.

Write-only bit.

Bit 02

ASM – Address Search Mode. In SDLC mode, all frames are received if this bit is zero. If this bit is a one, frames are only received with address bytes that match the global address (11111111) or the value loaded into WR6. This bit must be zero in non-SDLC modes.

Write-only bit.

Bit 01

SCLH – Sync Character Load Inhibit. Setting this bit prevents the receiver from loading sync characters into the receive buffer.

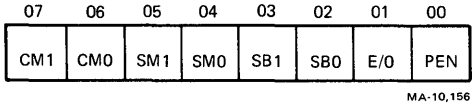
Write-only bit.

Bit 00

RXEN – Receiver Enable. Setting this bit enables the receiver to start. It should be set only after the receiver is initialized.

Write-only bit.

Write Register 4 (WR4)



Bits 07-06

CM1-CM0 – Clock Mode. These bits select the clock rate multiplier for both the receiver and transmitter as follows.

CM1	CM0	Clock Rate
0	0	1 x
0	1	16 x
1	0	32 x
1	1	64 x

In synchronous modes, 1 x must be selected.

Write-only bits.

Bits 05-04

SM1-SMO – Synchronous Mode. These bits select the synchronous protocol when synchronous operation is selected. They are ignored when asynchronous operation is selected.

SM1	SM0	Mode
0	0	8-bit internal sync character (monosync)
0	1	16-bit internal sync character (bisync)
1	0	SDLC
1	1	Invalid

Write-only bits.

Bits 03-02

SB1-SB0 – Stop Bits. These bits select the number of stop bits for asynchronous operation. They also select whether the mode of operation is asynchronous or synchronous.

SB1	SB0	Mode
0	0	Select synchronous operation
0	1	1 stop bit – asynchronous operation
1	0	1.5 stop bits – asynchronous operation
1	1	2 stop bits – asynchronous operation

Write-only bits.

Bit 01

E/O – Even/Odd Parity. This bit selects even or odd parity for both the receiver and transmitter when parity is enabled. A one selects even parity and a zero selects odd parity.

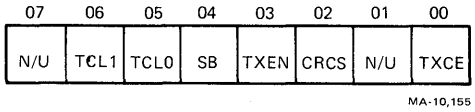
Write-only bit.

Bit 00

PEN – Parity Enable. When cleared, parity is disabled. When set, parity is enabled for both the receiver and transmitter. If the receiver character length is programmed to 8 data bits, the parity bit is not transferred to the processor. With other receiver character lengths, the parity bit is transferred to the processor.

Write-only bit.

Write Register 5 (WR5)



Bit 07

N/U – Not used.

Bit 06-05

TCL1-TCL0 – Transmitter Character Length. These bits determine the transmitter character length as follows.

TCL1	TCL0	Data Bits/Character
0	0	5 or less
0	1	7
1	0	6
1	1	8

Normally each character is sent to the transmitter right-justified and the unused bits are ignored. However, when sending 5 or less bits per character, the data should be formatted as follows.

D7	D6	D5	D4	D3	D2	D1	D0	Bits/Character
0	0	0	D4	D3	D2	D1	D0	5
1	0	0	0	D3	D2	D1	D0	4
1	1	0	0	0	D2	D1	D0	3
1	1	1	0	0	0	D1	D0	2
1	1	1	1	0	0	0	D0	1

Write-only bits.

Bit 04 SB – Send Break. Writing a one to this bit causes the transmit data line to immediately go to the space condition. Writing a zero to the bit allows normal transmitter operation.

Write-only bit.

Bit 03 TXEN – Transmitter Enable. Writing a one to this bit enables the transmitter and should only be done after the transmitter is initialized. Writing a zero to this bit disables the transmitter and enters either the idle or mark state.

Bit 02 CRCS – CRC Select. This bit selects which CRC polynomial to be used by both the receiver and transmitter.

CRCS	Mode	Polynomial
0	CRC-CCITT	$X^{16} + X^{15} + X^5 + 1$
1	CRC-16	$X^{16} + X^{15} + X^2 + 1$

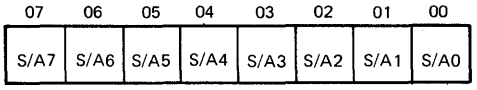
Write-only bit.

Bit 01 N/U – Not used.

Bit 00 TXCE – Transmitter CRC Enable. Writing a one to this bit enables the transmitter CRC generator. Writing a zero to this bit disables the transmitter CRC generator.

Write-only bit.

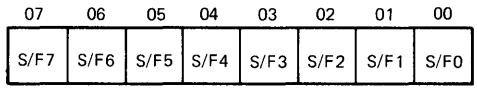
Write Register 6 (WR6)



Bits 07-00 S/A7-S/A0 – Sync/Address Register. This register should be loaded with the transmit sync character in monosync mode, the low order 8 sync bits in bisync mode, or the address byte in SDLC mode.

Write-only bits.

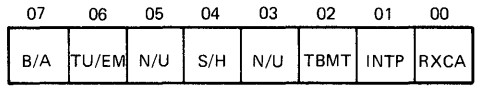
Write Register 7 (WR7)



Bits 07-00 S/F7-S/F0 – Sync/Flag Register. This register should be loaded with the receive sync character in monosync mode, the high order 8 sync bits in bisync mode, or the flag character (01111110) in SDLC mode.

Write-only bits.

Read Register 0 (RR0)



Bit 07 B/A – Break/Abort. When this bit is a one in asynchronous mode, it indicates the detection of a break (a null character plus a framing error which occurs when the receive input line is held in the space state for more than one character time). The B/A bit resets to a zero when the line returns to the mark state. In SDLC mode, a one indicates the detection of an abort sequence (7 or more ones received in sequence). The B/A bit resets when a zero is received. Any transition of the Break/Abort bit causes an external/status interrupt.

Read-only bit.

Bit 06 — TU/EM – Transmitter Underrun/End of Message. This bit is set following a reset. It can only be reset by writing a Reset Transmitter Underrun/End of Message Latch command into WR0. When the transmit underrun condition occurs, this bit is set and an external/status interrupt is generated.

Read-only bit.

Bit 05 — N/U – Not used.

Read-only bit.

Bit 04 — S/H – Sync/Hunt. The meaning of this bit depends on the mode of operation. In asynchronous mode, the bit is read as a zero. In monosync, bisync, or SDLC modes, this bit indicates whether the receiver is in the sync hunt or receive data operation phase. A zero indicates the receive data phase and a one indicates the sync hunt phase. A transition of this bit causes an external/status interrupt.

Read-only bit.

Bit 03 — N/U – Not used.

Read-only bit.

Bit 02 — TBMT – Transmit Buffer Empty. This bit is set when the transmitter buffer is empty except during the transmission of CRC.

Read-only bit.

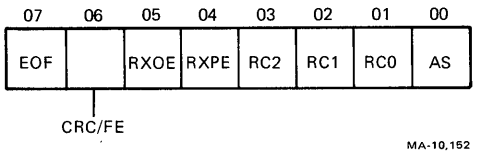
Bit 01 — INTP – Interrupt Pending. This bit is set when the vector of a pending interrupt is read from control/status register B. It is reset when an End of Interrupt command is issued in WR0 and no other interrupt is pending at the time.

Read-only bit.

Bit 00 — RXCA – Receive Character Available. This bit is set when the receiver buffer contains data and is reset when the buffer is empty.

Read-only bit.

Read Register 1 (RR1)



Bit 07 — EOF – End of Frame. This bit is valid only in SDLC mode. A one indicates that a valid ending flag is received. EOF is reset by either an Error Reset command (in WR0) or on receipt of the first character of the next frame.

Read-only bit.

Bit 06 — CRC/FE – CRC/Framing Error. In asynchronous mode, a one indicates a receiver framing error. In synchronous modes, a one indicates that the calculated CRC value does not match the last two bytes received. CRC/FE is reset by issuing an error reset command in WR0.

Read-only bit.

Bit 05 — RXOE – Receiver Overrun Error. When set, this bit indicates that the receiver buffer is overloaded by the receiver. The last character in the buffer (the third character) is overwritten and flagged with this error. Once the overwritten character is read, this error is latched until reset by the Error Reset command in WR0.

Read-only bit.

Bit 04 — RXPE – Receiver Parity Error. If parity is enabled, this bit is set for received characters whose parity does not match the programmed sense (odd/even). This bit is latched until it is reset by issuing a Error reset command in WR0.

Read-only bit.

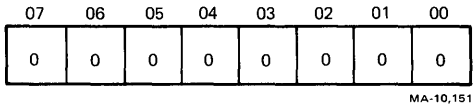
Bit 03-01 — RC2-RC0 – Residue Codes. Bit synchronous protocols allow I-fields that are not an integral number of characters. Because transfers from the communications port to the CPU are character oriented, the residue codes provide the capability of receiving leftover bits. Residue bits are right justified in the last two data bytes received.

Read-only bits.

Bit 00 — AS – All Sent. In asynchronous mode, this bit is set when the transmitter is empty and reset when a character is present in either the transmitter buffer or the transmitter shift register. In synchronous mode, this bit is always a one.

Read-only bit.

Read Register 2 (RR2)



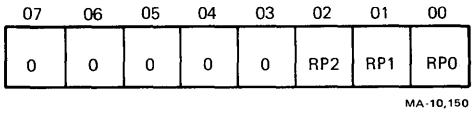
Bits 07-00 N/U – Not used. always read as zeros.

Read-only bit.

Control/Status Register B

This register operates as a window to 11 internal registers as did control/status register A. The internal registers consist of eight write registers and three read registers. The write registers are labeled WR0-WR7 and the read registers are labeled RR0-RR2. An internal pointer register selects which WR or RR registers to be read or written during an access to control/status register B. After reset, the pointer register contents are zero. The first write to the control/status register loads the data into WR0. The three least significant bits of WR0 are the pointer register. The next access to the control/status register accesses the internal register selected by the pointer register. The pointer is reset after the read or write operation is completed. In control/status register B, only WR0, WR1, WR2, and RR2 should be accessed. These four registers are described in the following paragraphs.

Write Register 0 (WR0)



Bits 07-06 N/U – Not used. Must always be written as zeros.

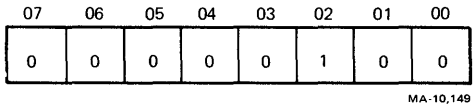
Write-only bits.

Bits 02-00 RP2-RP0 – Register Pointer bits. These bits determine which write register the next byte is written into or which read register the next byte is read from. After reset, the first byte written goes into WR0.

Following a read or a write to any register (except WR0) the pointer points to WR0. The pointer should only be used to access WR0, WR1, WR2, and RR2.

Write-only bits.

Write Register 1 (WR1)

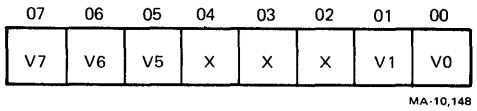


Bits 07-00

This register must be loaded with 00000100 for correct vector information when servicing interrupts from the communication port. No other data should ever be written into this register.

Write-only bits.

Write Register 2 (WR2)

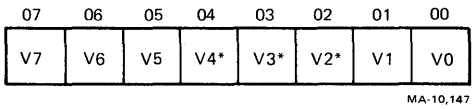


Bits 07-00

V7-V0 – Vector bits. This register should be written with a base vector for the channel interrupts (receiver, special receive, transmitter, and external/status interrupts). It is used when reading RR2 to get the vector. It does not matter what bits 04-02 are because they are modified to identify the four channel interrupts. Refer to the next section on RR2 for more details.

Write-only bits.

Read Register 2 (RR2)



Bits 07-00

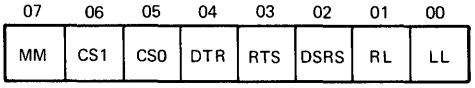
V7-V0 – Vector. This register is used to get the vector of the highest priority interrupt pending in the communication channel. The vector is the same as the contents that were written into WR2. Bits V4-V2 are modified to identify which condition caused the interrupt. After a receive/transmit interrupt causes the CPU to vector through location 210, the interrupt service routine should read RR2 to get the secondary vector that identifies which condition caused the interrupt.

V4	V3	V2	Condition Causing Interrupt
0	0	0	Transmitter buffer empty
1	0	1	External/status change
1	1	0	Receiver character available
1	1	1	Special receiver condition

If RR2 is read when no interrupt is pending, the vector is read with the variable bits V4-V2 set to all ones.

R/W bits.

Modem Control Register 0



Bit 07

MM – Maintenance Mode. When set, this bit loops the communications channel transmit data line onto the receiver data line. The transmit data signal to the modem is held in the mark state and the receive data from the modem is ignored. It is cleared at power up or by a Reset instruction.

R/W bit.

Bit 06-05

CS1-CS0 – Clock Source. These bits select the source of the transmit and receive baud rate clocks to the communications channel. The clock sources can be either the baud rate generator or the modem. The communication port can also provide the transmit clock to the modem. The following indicates how the selection is made.

Sources for Clocks

CS1	CS0	RXC	TXC	TXC/DTE
0	0	RBRG	TBRG	None
0	1	RXC/DCE	TXC/DCE	None
1	0	RXC/DCE	TBRG	TBRG
1	1	TBRG	TBRG	None

RBRG – clock is from receiver baud rate generator.

TBRG – clock is from transmitter baud rate generator.

RXC/DCE – clock is the receive clock line from modem.

TXC/DCE – clock is the transmit clock line from modem.

NONE – no clock signal is sent to modem.

The RXC column gives the source of the receiver baud rate clock to the channel. The TXC column gives the source of the transmitter baud rate clock. The TXC/DTE column indicates the clock that the communications port sends to the modem. It is cleared at power up or by a RESET instruction.

R/W bits.

Bit 04

DTR – Data Terminal Ready. When set, this signal is asserted to the modem. When cleared, the DTR signal is removed from the modem. It is cleared at power up or by a RESET instruction.

R/W bit.

Bit 03 RTS – Request To Send. When set, this signal is asserted to the modem. When cleared, the RTS signal is removed from the modem. It is cleared at power up or by a RESET instruction.

R/W bit.

Bit 02 DSRS – Data Signaling Rate Select. When set, this Rate Select signal is asserted to the modem. When cleared, the DSRS signal is removed from the modem. It is cleared at power up or by a RESET instruction.

R/W bit.

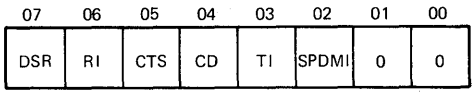
Bit 01 RL – Remote Loopback. When set, this signal is asserted to the modem. When cleared, the RL signal is removed from the modem. It is cleared at power up or by a RESET instruction.

R/W bit.

Bit 00 LL – Local Loopback. When set, this signal is asserted to the modem. When cleared, the LL signal is removed from the modem. It is cleared at power up or by a RESET instruction.

R/W bit.

Modem Control Register 1



Bit 07 DSR – Data Set Ready. This bit indicates the state of the DSR signal from the modem. A one indicates that DSR is asserted and a zero indicates that it is not asserted. A transition of this signal generates a modem change interrupt.

Read-only bit.

Bit 06 RI – Ring Indicator. This bit indicates the state of the RI signal from the modem. A one indicates that RI is asserted and a zero indicates that it is not asserted. A transition of this signal generates a modem change interrupt.

Read-only bit.

Bit 05 CTS – Clear To Send. This bit indicates the state of the CTS signal from the modem. A one indicates that CTS is asserted and a zero indicates that it is not asserted. A transition of this signal generates a modem change interrupt.

Read-only bit.

Bit 04

CD – Carrier Detect. This bit indicates the state of the CD signal from the modem. A one indicates that CD is asserted and a zero indicates that it is not asserted. A transition of this signal generates a modem change interrupt.

Read-only bit.

Bit 03

TI – Test Indicator. This bit indicates the state of the TI signal from the modem. A one indicates that TI is asserted and a zero indicates that it is not asserted.

Read-only bit.

Bit 02

SPDMI – Speed Mode Indicator. This bit indicates the state of the SPMI signal from the modem. A one indicates that SPDMI is asserted and a zero indicates that it is not asserted.

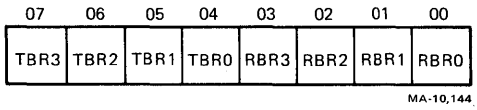
Read-only bit.

Bits 01-00

N/U – Not used. Always read as zeros.

Read-only bits.

Baud Rate Register



Bits 07-04

TBR3-TBR0 – Transmitter Baud Rate select. These bits program the transmitter baud rate generator. The accuracy of the input frequency to the baud rate generator is ± 0.01 %.

TBR3	TBR2	TBR1	TBR0	ASYNC 16 × Clock Baud Rate	SYNC 1 × Clock Baud Rate	Baud Rate Generator Percent Error
0	0	0	0	50		
0	0	0	1	75	1200	
0	0	1	0	110		
0	0	1	1	134.5		+0.016
0	1	0	0	150	2400	
0	1	0	1	300	4800	
0	1	1	0	600	9600	
0	1	1	1	1200	19200	
1	0	0	0	1800		
1	0	0	1	2000		+0.253
1	0	1	0	2400		
1	0	1	1	3600		
1	1	0	0	4800		
1	1	0	1	7200		
1	1	1	0	9600		
1	1	1	1	19200		+3.125

Write-only bits.

Bits 03-00 RBR3-RBR0 – Receiver Baud Rate select. These bits program the receiver baud rate generator. The accuracy of the input frequency to the baud rate generator is ± 0.01 %.

RBR3	RBR2	RBR1	RBR0	ASYNC 16 × Clock Baud Rate	Baud Rate Generator Percent Error
0	0	0	0	50	
0	0	0	1	75	
0	0	1	0	110	
0	0	1	1	134.5	+0.016
0	1	0	0	150	
0	1	0	1	300	
0	1	1	0	600	
0	1	1	1	1200	
1	0	0	0	1800	
1	0	0	1	2000	+0.253
1	0	1	0	2400	
1	0	1	1	3600	
1	1	0	0	4800	
1	1	0	1	7200	
1	1	1	0	9600	
1	1	1	1	19200	+3.125

5.4.12.2 Communications Port Default State After Power-Up – When the power-up self-test is completed, the firmware initializes the communications port. The firmware issues a Channel Reset command to both control/status register A and control/status register B. This clears all the internal control registers in the communications USART. In addition, the firmware loads the modem and baud rate registers as follows.

Modem Control Register 0	= 000
Baud Rate Register	= 356

5.4.13 Battery Backed Up System Clock and RAM

The battery backed up system clock and RAM are part of the same chip. A battery, charged when the system is turned on, maintains the clock and RAM.

The clock's internal system contains a bit to indicate if the clock power gets too low and the time and date may no longer be valid. The bit is in the CSR3 register and is called the VRT (valid RAM and time) bit. See section on CSR3 for details of the VRT bit.

The chip can also be programmed to interrupt the CPU at a specified alarm time or at a periodic rate. The periodic rate can be programmed to one of 13 frequencies from 2 Hz to 8.192 KHz. There is no line time clock.

The clock keeps time accurate to within 1 minute per month. This assumes that the system module is installed in the Professional 300 series system box and operates within the specified temperature limits for the system. See Section 5.6 for accuracy and temperature specifications.

5.4.13.1 Clock Interface

Addresses:

17773000	Seconds
17773002	Seconds alarm
17773004	Minutes
17773006	Minutes alarm
17773010	Hours
17773012	Hours alarm
17773014	Day of week
17773016	Date of month
17773020	Month
17773022	Year
17773024	CSR0
17773026	CSR1
17773030	CSR2
17773032	CSR3

Vector:

230

All 14 registers use only the low byte. The high bytes are always read as all zeros and writes to high bytes have no effect.

Time, Date, Alarm Registers
The first 10 registers (17773000–17773022) handle the time, date, and alarm functions. Refer to Table 5-19. The contents of these 10 registers can be programmed to be in either binary or BCD format. All of the registers must be the same format. Bit 02 in CSR1 determines the data format. The hours and hours alarm registers can be programmed to be in either 12 or 24 hour format. Both registers must be the same format. When the 12 hour format is selected, bit 07 of the two registers indicates AM (when cleared) or PM (when set). The day of week register counts cyclicly from 1 to 7 where 1 represents Sunday. The year register counts cyclicly from 00 to 99. The three alarm registers can generate an interrupt to the processor at the specified time if the alarm interrupt enable bit is set in CSR1. Each of the alarm registers can be programmed to a "don't care" state by setting bits 06 and 07. This allows alarm interrupts to occur every hour, every minute, or every second if specified. All 10 time, date, and alarm registers can be read or written to but must be done according to the procedures described in the following paragraphs.

A time and date update cycle starts once each second. The time and date increment by one second and the time is compared to the alarm registers during the update cycle. The update cycle continues for 1984 μs, during which the 10 time, date, and alarm registers are not accessible. Undefined data results if any of these registers are read during an update cycle. There are two methods of assuring correct data:

1. Bit 07 in CSR0 is the update-in-progress bit (UIP). The UIP bit pulses once per second. After the UIP bit goes high, the update cycle begins 244 μs later. If the UIP bit is read as a low, the program has at least 244 μs to read the time and date before the update cycle begins and makes the information inaccessible. If the UIP bit is read as a high, the time and date may not be available.

CAUTION
If this method is used, the program should avoid interrupts with service routines that would cause the time needed to read the time and date to exceed 244 μs.

Table 5-19 Time, Date, and Alarm Modes

Address Mode	Function	Decimal Range	Binary Mode in Binary	BCD in Hex
17773000	Seconds	00–59	000–073	00–59
17773002	Seconds alarm	00–59	000–073	00–59
17773004	Minutes	00–59	000–073	00–59
17773006	Minutes alarm	00–59	000–073	00–59
17773010	Hours–12 hour mode			
	AM	01–12	001–014	01–12
	PM	01–12	201–214	81–92
	Hours–24 hour mode	00–23	000–027	00–23
17773012	Hours alarm–12 mode			
	AM	01–12	001–014	01–12
	PM	01–12	201–214	81–92
	Hours alarm–24 mode	00–23	000–027	00–23
17773014	Day of week	01–07	001–007	01–07
17773016	Date of month	01–31	001–037	01–31
17773020	Month	01–12	001–014	01–12
17773022	Year	00–99	000–143	00–99

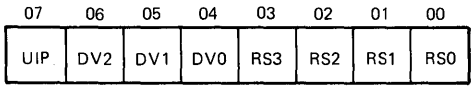
2. An update ended interrupt is provided to indicate that the update cycle is completed. This interrupt occurs at the end of the update cycle if the update interrupt enable bit is set in CSR1. This method gives the program almost a full second to read the time and date before the next update cycle. The interrupt service routine must clear the update ended flag bit in CSR2 for correct operation. See the section on CSR2 for more details.

Care must also be taken when writing to the 10 time, date, and alarm registers. Setting the time and date or programming the alarm must not be done during an update cycle. The following procedures should be used.

1. Setting the time and date is done by using the SET bit in CSR1. Setting the SET bit inhibits update cycles. If an update is in progress when the program sets the SET bit, the update is completed. With updates halted, the program should select the specified formats in CSR1, initialize the time and date registers with the appropriate information, and initialize the alarm registers if used. The SET bit can then be cleared to enable update cycles to occur normally.

2. The alarm registers can be initialized when the time and date are set or when an update cycle is not in progress (using one of the two previously described methods).

Control/Status Register 0 (CSR0)



Bit 07

UIP – Update in Progress. The UIP bit is a status flag that may be monitored by the program. It is set 244 μs before an update cycle starts and is cleared immediately after the update cycle is complete. UIP is not effected by a RESET.

Read-only bit.

Bits 06–04

DV2-DV0 – Divider Control. These bits should be initialized to the following.

DV2	DV1	DV0
0	1	0

Any other state of these three bits cause incorrect clock operation. These bits are not affected by RESET.

R/W bits.

Bits 03–00

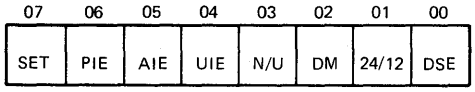
RS3-RS0 – Rate Select. These four bits select one of 13 periodic rates to generate an interrupt. These bits are not affected by RESET. The periodic rates are selected as follows.

RS3	RS2	RS1	RS0	Periodic Rate	Frequency
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 μs	8192 Hz
0	1	0	0	244.141 μs	4096 Hz
0	1	0	1	488.281 μs	2048 Hz
0	1	1	0	976.562 μs	1024 Hz
0	1	1	1	1.95313 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125.0 ms	8 Hz
1	1	1	0	250.0 ms	4 Hz
1	1	1	1	500.0 ms	2 Hz

The accuracy of these rates is ± 0.0025 %.

R/W bits.

Control/Status Register 1 (CSR1)



Bit 07 — SET – The SET bit halts update cycles to initialize the time and date registers. When set, update cycles are inhibited. If the bit is set during an update, the update cycle is completed. When cleared, normal update cycles occur. SET is not effected by RESET.

R/W bit.

Bit 06 — PIE – Periodic Interrupt Enable. When set, it enables periodic interrupts at the rate selected by bits RS3-RS0 in CSR0. When cleared, no periodic interrupts occur. PIE is cleared by RESET.

R/W bit.

Bit 05 — AIE – Alarm Interrupt Enable. When set, it enables alarm interrupts to occur at the time specified in the alarm registers. When cleared, no alarm interrupts occurs. AIE is cleared by RESET.

R/W bit.

Bit 04 — UIE – Update ended Interrupt Enable. When set, it enables an interrupt to occur at the end of each update cycle. When cleared, no update interrupts occur. UIE is cleared by RESET.

R/W bit.

Bit 03 — N/U – Not Used. Cleared by RESET.

R/W bit.

Bit 02 — DM – Data Mode. When set, it indicates that the time, date, and alarm registers are in binary format. When cleared, BCD format is selected. DM is not effected by RESET. DM should only be changed when initializing all the time and date registers.

R/W bit.

Bit 01 — 24/12 – 24 Hour Mode/12 Hour Mode. When set, it selects 24 hour clock format. When cleared, it selects 12 hour clock format. AM or PM is indicated by bit 07 in the hours register. 24/12 is not effected by RESET. 24/12 should only be changed when initializing all the time and date registers.

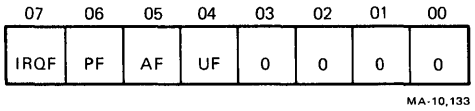
R/W bit.

Bit 00

DSE – Daylight Savings Enable. When set, two special updates are enabled. On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time reaches 1:59:59 AM for the first time, it changes to 1:00:00 AM. When DSE is cleared, these special updates do not occur. DSE is not effected by RESET. DSE should not be changed during an update cycle.

R/W bit.

Control/Status Register 2 (CSR2)



Bit 07

IRQF – Interrupt Request Flag. When set, it indicates that the clock is generating an interrupt to the processor. IRQF is set when one or more of the following conditions occur.

- The PIE and PF bits are both set
- The AIE and AF bits are both set
- The UIE and UF bits are both set

Read-only bit.

Bit 06

PF – Periodic Interrupt Flag. PF is set at the end of each period time. The period time is determined by the periodic rate bits RS3-RS0. PF is set independently from the state of the PIE bit. PF set generates a clock interrupt to the processor and causes a one to appear in the IRQF bit if the PIE bit is also set. PF is cleared by Reset or by reading CSR2.

Read-once bit.

Bit 05

AF – Alarm Interrupt Flag. AF is set when the time matches the alarm time. AF is set independently from the state of the AIE bit. AF set generates a clock interrupt to the processor and causes a one to appear in the IRQF bit if the AIE bit is also set. AF is cleared by RESET or by reading CSR2.

Read-once bit.

Bit 04

UF – Update-ended Interrupt Flag. UF is set after each update cycle has completed. UF operates independently from the state of the UIE bit. UF set generates an interrupt to the processor and causes a one to appear in the IRQF bit if UIE is also set. UF is cleared by RESET or by reading CSR2.

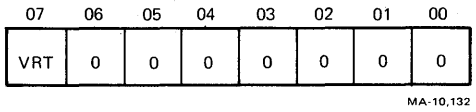
Read-once bit.

Bits 03-00

Not used. Always read as zeros.

Read-only bits.

Control/Status Register 3 (CSR3)



Bit 07 — VRT – Valid RAM and Time. When set, it indicates that the clock has not lost power and that the time and date have been updated correctly since last initialized. If cleared, it indicates that the power to the clock got too low and the time and date may not be valid. The processor should set the VRT bit when it initializes the clock. Reading CSR3 sets the VRT bit. VRT is not effected by RESET. This bit also indicates the validity of the battery backed-up RAM.

Read-once bit.

Bits 06-00 — Not used. Always read as zeros.

Read-only bits.

5.4.13.2 System Clock Default State After Power-Up – The firmware initializes the clock after the power-up self-test is completed. This default state follows.

CSR 0:

bits <06:04> = 0 1 0 (divider control)
bits <03:00> = 0 0 0 0 (no periodic rate)

CSR 1:

bit 07 (the set bit) is cleared if the battery power got too low and is not effected otherwise
bits <06:04> = 0 0 0 (interrupt enables cleared)
bits <03:00> are not effected

CSR 2:

read-only register not initialized by firmware

CSR 3:

bit 07 = 1 (VRT bit always set)

5.4.13.3 Battery Backed Up RAM

Addresses:

17773034–17773176 50 bytes RAM

All 50 RAM locations use only the low byte. The high bytes are always read as all zeros and writes to high bytes have no effect.

5.4.14 Maintenance ODT

A part of the microcode in the processor emulates the capability found on a "lights and switches" console. However the Professional 350 computer does not have a "lights and switches" console or a console switch register at bus address 17777570. Therefore, a terminal at the standard bus address of 17777560 can perform console functions. Communication between the processor and the user is through a series of ASCII characters which the processor interprets as console commands. The terminal addresses, 17777560 through 17777566 are generated in microcode and can not be changed.

This feature is called microcode on-line debugging technique (Micro-ODT). Micro-ODT accepts 16-bit addresses, allowing it to access 56 kilobytes of memory plus the 8 kilobyte I/O page.

5.4.14.1 Terminal Interface – The hardware interface for a terminal (serial line) to communicate with ODT is the printer port. A terminal cable (PB BCC08) must be used instead of the printer cable (PN BCC05). If the terminal cable is not used, read accesses of the terminal CSRs (addresses 17777560 and 17777564) results in all zeros indicating that the transmitter and the receiver are not ready. See Section 5.4.15 for details about these cables and the maintenance terminal.

5.4.14.2 Entry Conditions – The ODT console mode can be entered as follows.

1. Execution of a HALT instruction in kernel mode.
   or
2. From the maintenance terminal by pressing the BREAK key on the keyboard. The BREAK ENABLE bit in the system CSR must be set and the terminal cable must be used or BREAK is ignored.

On entry, ODT causes the following initialization.

1. Prints a <CR> and <LF>.

2. Prints the PC (program counter contents) in 6 digits (16-bit octal).

3. Performs a read from RBUF (input data buffer at 17777562) and then ignores the character present in the buffer. This prevents ODT interpreting false characters or user program characters as a command.

4. Prints a <CR> and <LF>.

5. Prints the prompt character "@".

6. Enters a wait loop for terminal input. The DONE flag (bit 7) in RCSR at 17777560 is continuously tested via a read by the processor for a 1. If it is a 0, the processor keeps testing.

5.4.14.3 ODT Operation of Serial Line Interface – The processor's microcode operates the serial interface in half-duplex mode by using program I/O techniques instead of interrupts. This means that when the ODT microcode is busy printing characters using the output side of the interface, the microcode is not monitoring the input side for incoming characters. In this condition, all incoming characters are lost. Although the USART chip may post overrun errors, the microcode does not check any error bits in the serial interface.

NOTE

Do not try to type ahead to ODT because those characters will not be recognized. More importantly, if another processor is at the end of the serial line, it must use half duplex operation. No input characters should be sent until ODT's output is completed.

The input sequence for ODT is on entry to ODT, the RBUF register is read and the character ignored to eliminate a possible false command ODT then continues with the input sequence.

1. Read RCSR bit 7 (Done Flag). If a zero, continue testing.

2. If RCSR bit 7 is a 1, read low byte of RBUF.

The following is the output sequence of ODT.

1. Read XCSR bit 7 (Done Flag). If a zero, continue testing.

2. If XCSR bit 7 is a 1, write the character into the low byte of XBUF.

5.4.14.4 Command Set – This section describes the ODT command set. When examples are used, the user's entry is not bolded but the processor's response is. The commands are a subset of ODT-11 and use the same command characters. ODT has 10 internal states. Each state recognizes certain characters as valid input and responds with a "?" to all others. Table 5-20 describes these states.

The parity bit (bit 7) on all input characters is ignored not stripped) by ODT. If the input character is echoed, the state of the parity bit is copied to the output buffer (XBUF). Output characters internally generated by ODT (for example, <CR>) have the parity bit equal to zero. All commands are echoed except for <LF>.

To describe the use of a command, some commands are referred to before they are defined. This section should be scanned first for familiarity and then re-read for detail. The word location refers to a bus address, processor register, or processor status word (PSW).

/ (ASCII 057) Slash

This command opens a bus address, processor register, or PSW and is normally preceded by other characters which specify a location. In response to /, ODT prints the location contents (for example, six characters) and then a space (ASCII 40). After printing is complete, ODT waits for either new data for that location or a valid close command. The space character is issued so that the location's contents and possible new contents entered by the user can be seen on the terminal.

Example: @001000/**012525 <SPACE>**

where:	@	=	ODT prompt character
001000		=	octal location in the address space specified by the user (leading zeros are not needed).
	/	=	command to open and print contents of location
012525		=	contents of octal location 1000
<SPACE>		=	space character generated by ODT

The / command can be used without a location specifier to verify the data just entered into a previously opened location. The / produces this result only if it is entered immediately after a prompt character. A / issued immediately after the processor enters ODT mode prints a ? <CR> <LF> because a location has not yet been opened.

Table 5-20 ODT States

State	Example of Terminal	Valid Output	Input	Comments
1	@ R, $ G P CTL-SHIFT-S H	0–7	Octal digits	
2	@R OR @$ S	0–7		
3	@1000/123456	0–7	 CR LF	
4	@R1/123456	0–7	 CR LF	
5	@1000 /	0–7	 G	
6	@R1 OR @RS S /	0–7		
7	@1000/123456 1000	0–7	 CR LF	
8	@R1/123456 1000	0–7	 CR LF	
9	@ /			Previous location was opened
10	@ CTL-SHIFT-S			2 binary bytes

Example: @1000/**012525 <SPACE>** 1234 **<CR> <CR> <LF>**

@/001234 <SPACE>

where:

first line	=	new data of 1234 entered into location 1000 and location closed with <CR>.
second line	=	a / was entered without a specified location and the previous location was opened to show that the new contents were correctly entered.

<CR> (ASCII 15) Carriage Return
This command closes an open location. If a location's contents are to be changed, precede the <CR> with the new data. If no change is specified, <CR> closes the location without changing its contents.

Example: @R1/**004321 <SPACE>** <CR> **<CR> <LF>**

@

Processor register R1 was opened and no change was specified so the user issued <CR>. In response to the <CR>, ODT printed <CR> <LF> and @.

Example: @R1/**004321 <SPACE>** 1234 <CR> **<CR> <LF>**

@

In this condition, the user wanted to change R1 and the new data, 1234, was entered before issuing the <CR>. ODT deposited the new data in the open location and then printed <CR> <LF> and @.

ODT echoes the <CR> entered by the user and then prints <CR> <LF> @.

<LF> (ASCII 12) Line Feed

This command closes an open location and then opens the next contiguous location. Bus addresses and processor registers are incremented by two and one respectively. If the PSW is open when a <LF> is issued, it closes and prints a <CR> <LF> @; no new location is opened. If the open location's contents are to be changed, the new data should precede the <LF>. If no data is entered, the location is closed without being modified.

Example: @R2/**123456 <SPACE>** <LF> **<CR> <LF>**

@R3/054321 <SPACE>

In this example, the user entered <LF> with no data preceding it. In response, ODT closed R2 and then opened R3. When a user has the last register, R7, open and issues <LF>, ODT returns to the beginning register, R0.

Example: @R7/**000000 <SPACE>** <LF> **<CR> <LF>**

@R0/123456 <SPACE>

Unlike other commands, ODT does not echo the <LF>. Instead it prints <CR> then <LF> so that teletype printers operate correctly. In order to make this easier to decode, ODT also does not echo ASCII 0, 2 or 10, but responds to these 3 characters with ? <CR> <LF> @.

$ (ASCII 044) or R (ASCII 122) Internal Register Designator

Either character, when followed by a register number up to 7, or PSW designator, S, opens that specific processor register.

The $ character is compatible with ODT-11. The R character provides an easy one key stroke and is representative of what it does (R = Register).

Example: **@$0/000123 <SPACE>**

Example: **@R7/000123 <SPACE>**

If more than one character (digit or S) after the $ or R is typed, ODT uses the last character as the register designator. An exception: If the last 3 digits equal 077 or 477, ODT opens the PSW instead of R7.

S (ASCII 123) Processor Status Word

This designator opens the PSW (processor status word) and must be used after the user enters an $ or R register designator.

Example: **@RS/100377 <SPACE>** 0 <CR> **<CR> <LF>**

@/000010 <SPACE>

Note that the trace bit (bit 4) of the PSW can not be modified by the user. This is so that PDP-11 program debug utilities (for example, ODT-11) which use the T bit for single stepping are not accidentally damaged by the user. If the user issues a <LF> while the PSW is open, the PSW closes and ODT prints a <CR> <LF> @. No new location is opened in this example.

G (ASCII 107) GO

This command starts program execution at a location entered immediately before the G. This function is equivalent to the LOAD ADDRESS and START switch sequence on other PDP-11 consoles.

Example: **@200G <NULL> <NULL>**

The following is the ODT sequence for a G.

1. Prints two nulls (ASCII 0) so the bus initialize which follows does not purge the G character from the double buffered USART chip in the serial line interface.

2. Loads R7 (PC) with the entered data. If no data is entered, 0 is used. In the above example, R7 equals 200 and this is where program execution will start.

3. The PSW and FPS (floating point status) registers are cleared to 0.

P (ASCII 120) Proceed

This command continues execution of a program and corresponds to the CONTINUE switch on other PDP-11 consoles. No programmer visible machine state is modified using this command.

Example: @P

Program execution continues at the place pointed to by R7. After the P is echoed, the ODT state is left and the processor immediately enters the state to fetch the next micro-instruction. If a HALT request is asserted, it is recognized at the end (during the service state) of the instruction and the processor enters the ODT state. On entry, the PC (R7) contents are printed. A user can single instruction step through a program and get a PC "trace" displayed on the terminal, a HALT request can be asserted by using the H command.

H (ASCII 110) Halt

The H command asserts a HALT request to the processor and corresponds to the HALT switch on other PDP-11 consoles. Each time the H command is typed, an internal halt request flip-flop is toggled. On entering ODT, the halt request flip-flop is cleared (not asserting a halt request). Typing the H toggles the flip-flop and asserts a halt request. Typing the H again resets the flip-flop and clears the halt request. This allows the user to single step through this code. To single step, the H command should be used to assert a halt request to the processor. Then, each time the P command is typed, one instruction is executed. When single stepping is no longer wanted, type the H command followed by one more P command.

Example: @H <CR> <LF>

@

<CONTROL-SHIFT-S> (ASCII 23) Binary Dump

This command is for manufacturing test purposes and is not a normal user command. It displays a part of memory more efficiently than using the / and <LF> commands. The protocol is as follows.

1. After a prompt character, ODT receives a control-shift S command and echoes it.

2. The host system at the other end of the serial line must send two 8-bit bytes which ODT interprets as a starting address. These two bytes are not echoed.

   The first byte specifies starting address bits <15:8> and the second byte specifies starting address bits <7:0>. Bus address bits <21:16> are always forced to zero; the dump command is limited to the first 64 Kbytes of address space.

3. After the second address byte has been received, ODT outputs to the serial line 12 octal bytes starting at the address specified previously. When the output is done, ODT prints <CR> <LF> @.

   To exit from the command, if accidentally entered, enter two @ characters (ASCII 100) as a starting address. After the binary dump, the user will receive a prompt character, @.

5.4.14.5 Address Specification – The Professional 300 series Micro-ODT accepts 16-bit addresses, allowing it to access 56 kilobytes of memory plus the 8 kilobyte I/O Page. Addresses 000000 through 157776 correspond to the first 56 Kilobytes of physical memory. Addresses 160000 through 177776 correspond to the I/O page (physical locations 17760000 through 17777776). If an address with more than 16 bits is specified, only the 16 least significant bits are used.

Processor I/O Addresses
Certain processor and MMU registers have I/O addresses assigned to them for programming purposes. If referenced in ODT, the PSW responds to its bus address, 177776. Processor registers R0 through R7 do not respond (time out occurs) to bus addresses 177700 through 177707 if referenced in ODT.

The MMU contains status registers and PAR/PDR pairs. These registers can be accessed from ODT by entering their bus address.

Example: @177572/**000001 <SPACE>**

In this example, memory management status register 0 was opened and the memory management enable bit is set.

The floating point accumulators, which are also in the MMU chip, cannot be accessed from ODT. Only floating point instructions can access these registers.

Stack Pointer Selection
Accessing kernel and user stack pointer registers is done as follows. When R6 is referenced in ODT, it accesses the stack pointer specified by the PS current mode bits (PS<15:14>). This is done for convenience only. If a program operating in kernel mode (PS<15:14> = 00) is halted and R6 is opened, the kernel stack pointer is accessed.

Similarly, if a program is operating in user mode (PS<15:14> = 11), R6 accesses the user stack pointer. If a different stack pointer is wanted, the user must change PS<15:14> to the appropriate value and then the R6 command can be used. If an operating program is halted, the original value of PS<15:14> must be restored to continue execution.

Example:
PS = 140000
@R6/**123456 <SPACE>**
The user mode stack pointer has been opened.
@RS/**140000 <SPACE>** <CR> 0 <CR> **<CR> <LF>**
@R6/**001000 <SPACE>** <CR> **<CR> <LF>**
@RS/**000000 <SPACE>** 140000 <CR> **<CR> <LF>**
@P

In this example, the kernel mode stack pointer was specified. The PS was opened and PS<15:14> was set to 00 (kernel mode). Then R6 was examined and closed. The original value of PS<15:14> was restored and then the program was continued using the P command.

If PS<15:14> are set to 01, another unique register within the processor is accessed. This register is reserved for future DIGITAL use.

Entering Octal Digits
In general, when specifying an address or data, ODT uses the last six octal digits if more than six have been entered. The user need not enter leading zeros for either address or data; ODT forces zeros as the default. If an odd address is entered, the low order bit is ignored and a full 16-bit word is displayed.

ODT Timeout
If the user specifies a non-existent address, ODT responds to the bus timeout by printing ? <CR> <LF> @. The bus timeout is approximately 6.5 μs.

5.4.14.6 Invalid Characters – In general, any character which ODT does not recognize during a specific sequence is echoed (except the ASCII codes 0, 2, 10, or 12) and ODT prints a ? <CR> <LF> @.

ODT has 10 internal states and each state has its own set of valid input characters. Some commands are only allowed when in certain states or sequences. This lowers the chance of a user accidentally destroying data by pressing the wrong key. Table 5-20 defines the states and valid input characters.

5.4.15 Maintenance Terminal

The maintenance terminal is included as a debugging and testing feature. Physically, it is the same port as the printer port. The printer port can be made to simulate a standard PDP-11 DL interface. When a terminal is connected to the port instead of a printer, accesses to the maintenance terminal addresses 17777560–17777566 function like the standard DL interface. In this mode, the port programs like a DL serial device with a receiver CSR, a receiver data buffer, a transmitter CSR, and a transmitter data buffer. Accesses to these registers when a terminal is not connected to the port result in reads of all zeros and writes that have no effect. Accesses to the printer port registers, 17773400–17773406 operate normally regardless of the device connected to the port.

Interrupts are not handled like a standard terminal DL. There are no interrupt enable bits in the CSR registers at locations 17777560 and 17777564. Interrupts must be enabled, disabled, and handled through interrupt controller 0 like the printer port interrupts. The vectors can be changed from the printer port vectors of 220 and 224 to the terminal vectors of 60 and 64 by reprogramming the response memory in interrupt controller 0 (see Section 5.4.6).

Hardware break detection can be enabled when a terminal is connected to the port. This allows the processor to halt into micro-ODT when the break key is depressed on the terminal. The hardware break detection has no effect if a printer is connected to the port.

The hardware determines that a terminal is connected to the port when pins 8 and 9 of the printer port connector, J6, are shorted. When using the port for a printer, a printer port cable (PN BCC05) should be used. The cable does not short pins 8 and 9. When using the port for a terminal, a terminal port cable (PN BCC08) should be used; the cable shorts pins 8 and 9.

5.4.15.1 Maintenance Terminal Interface

Addresses:

17777560	Receiver CSR
17777562	Receiver data buffer
17777564	Transmitter CSR
17777566	Transmitter data buffer

Vectors:

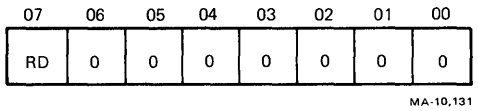
220*	Receiver
224*	Transmitter

All four registers use only the low byte. Writes to high bytes have no effect and high bytes are read as all zeros. The operation of each terminal register is given below.

---

* Vectors of 60 and 64 can be obtained by programming interrupt controller 0. Interrupts on this port are not handled like a standard PDP11 DL (see description above).

Receiver Control and Status Register (RCSR)



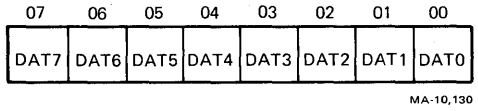
Bit 07 — RD – Receiver Done. This bit indicates that a character was received by the interface receiver. Each time a new character is received, the RD bit is set. RD is cleared by reading the receiver data buffer register or by a RESET.

Read-only bit.

Bits 06-00 — Not used. Always read as zeros.

Read-only bits.

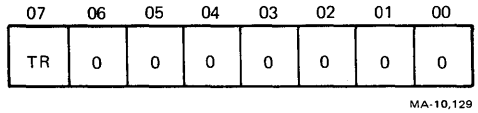
Receiver Data Buffer Register (RBUF)



Bits 07-00 — DAT7-DAT0 – Data. This register contains the last received character. Reading the register clears RD. Writes to the register have no effect on the data in the register nor the RD bit.

Read-only bits.

Transmitter Control and Status Register (XCSR)



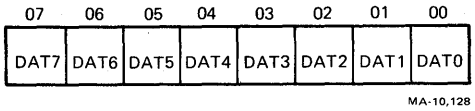
Bit 07 — TR – Transmitter Ready. This bit indicates that the transmitter data buffer register is ready to be loaded with another character. Each time the transmitter data buffer is loaded, the TR bit is cleared. TR is set by a RESET or when the transmitter data buffer becomes ready.

Read-only bit.

Bits 06-00 — Not used. Always read as zeros.

Read-only bits.

Transmitter Data Buffer Register (XBUF)



Bits 07-00 DAT7-DAT0 – Data. This register should be loaded with characters to be transmitted. Writing to the register clears TR. Reading the register returns unpredictable data and has no effect on the TR bit.

Write-only bits.

5.5 CONNECTORS

There are 15 connectors on the Professional 350 system module (Table 5-21). Tables 5-22–5-29 show the pin connections for all but the CTI BUS connectors. Table 5-30 shows the connectors for jacks 10–15, the CTI BUS.

Table 5-21 System Module Connectors

Connector	Function
J1, J2	Memory boards
J3	Battery
J4	DC power
J5	Video/keyboard
J6	Printer
J7	Communication
J8	Remote access
J9	Network
J10–J15	CTI BUS options

Table 5-22 J1, J2 RAM Module Pin-out

Pin	Signal
1	+5.0 V
2	MUXA 1 L
3	+5.0 V
4	MUXA 2 L
5	GND
6	MUXA 0 L
7	GND
8	MUXA 4 L
9	GND
10	MUXA 7 L
11	GND
12	MUXA 3 L
13	D03 H
14	D04 H
15	D02 H
16	D05 H
17	D01 H
18	D06 H
19	D00 H
20	D07 H
21	D08 H
22	D15 H
23	D09 H
24	D14 H
25	D10 H
26	D13 H
27	D11 H
28	MUXA 6 L
29	D12 H
30	MUXA 5 L
31	GND
32	MUXA 8 L
33	GND
34	RCV WLB H
35	GND
36	RAS n L
37	BANK n L
38	CAS H
39	Reserved
40	RCV WHB H

Table 5-23 J3, Battery Back-up

Pin	Signal
1	+3.6 V
2	GND

Table 5-24 J4,DC Power

Pin	Signal
1	BDCOK H
2	KEY
3	BPOK H
4	−12.0 V
5	+12.0 V
6	+5.0 V
7	+5.0 V
8	+5.0 V
9	+5.0 V
10	GND
11	GND
12	GND
13	GND
14	GND
15	GND
16	GND

Table 5-25 J5, Video/Keyboard

Pin	Signal
1	BLUE RETURN
2	GREEN RETURN
3	RED RETURN
4	MONO RETURN
5	GND
6	GND
7	+12.0 V
8	+12.0 V
9	BLUE VIDEO
10	GREEN VIDEO
11	RED VIDEO
12	MONO VIDEO
13	MON PRES L
14	KBD RDATA
15	KBD XDATA

Table 5-26 J6, Printer Port

Pin	Signal	CCITT V.24	EIA RS-232-C
1	PROTECTIVE GND	101	AA
2	TRANSMIT DATA	103	BA
3	RECEIVE DATA	104	BB
4			
5	DATA TERMINAL READY	108/2	CD
6	DATA SET READY	107	CC
7	SIGNAL GND	102	AB
8	GND		
9	TERMINAL L		

Table 5-27 J7, Modem Communications

Pin	Signal	CCITT V.24	EIA RS-232-C
1	PROTECTIVE GND	101	AA
2	TRANSMIT DATA	103	BA
3	RECEIVE DATA	104	BB
4	REQUEST TO SEND	105	CA
5	CLEAR TO SEND	106	CB
6	DATA SET READY	107	CC
7	SIGNAL GND	102	AB
8	CARRIER DETECT	109	CF
9			
10			
11			
12	SPEED MODE INDICATION	112	CI
13			
14			
15	TRANSMIT CLOCK (DCE)	114	DB
16			
17	RECEIVE CLOCK (DCE)	115	DD
18	LOCAL LOOPBACK	141	
19			
20	DATA TERMINAL READY	108/2	CD
21	REMOTE LOOPBACK	140	
22	RING INDICATOR	125	CE
23	DATA SIGNAL RATE SELECT	111	CH
24	TRANSMIT CLOCK (DTE)	113	DA
25	TEST INDICATOR	142	

Table 5-28 J8, Remote Access Connector

Pin	Signal
1	RAL 01
2	RAL 02
3	RAL 03
4	GND
5	RAL 04
6	RAL 05
7	+12.0 V*
8	RAL 06
9	RAL 07
10	GND
11	RAL 08
12	RAL 09
13	+5.0 V #
14	RAL 10
15	RAL 11
16	GND
17	RAL 12
18	RAL 13
19	−12.0 V*
20	RAL 14
21	RAL 15
22	RAL 16

* Line fused with 0.25A
# Line fused with 0.50A

Table 5-29 J9, Network (NET1)

Pin	Signal
1	SHIELD
2	COLLISION PRESENCE +
3	TRANSMIT +
4	
5	RECEIVE +
6	POWER RETURN (GND)
7	
8	
9	COLLISION PRESENCE −
10	TRANSMIT −
11	
12	RECEIVE −
13	POWER (+12.0 V)*
14	
15	

* Line fused with 0.50A

Table 5-30 CTI BUS Pin-Out and Signal Descriptions

General Section of the CTI BUS

Pin No.	Signal Name and Active State*	Transmit/ Receive †	Description
1	BDCOK H	R	DC voltage level OK; (Section 5.3.2.5)
2	+5.0 V		
3	BPOK H	R	Sufficient voltage in power supply to run emergency power loss program
4	GND		
5	BINIT L	T	Initialize system on power up (Section 5.3.2.4)
6	−12.0V		
7	BDAL 15 L	T/R	Buffered data/address line (Section 5.3.3)
8	BDAL 13 L	T/R	Buffered data/address line (Section 5.3.3)
9	BDAL 14 L	T/R	Buffered data/address line (Section 5.3.3)
10	BDAL 12 L	T/R	Buffered data/address line (Section 5.3.3)
11	BSPARE 0		Reserved
12	BDAL 11 L	T/R	Buffered data/address line (Section 5.3.3)
13	BRPLY L	R	Reply (Section 5.3.3.1)
14	BDAL 10 L	T/R	Buffered data/address line (Section 5.3.3)
15	GND		
16	BDAL 09 L	T/R	Buffered data/address line (Section 5.3.3)

* B at beginning of signal name indicates a bused signal
† Transmit/receive with reference to the system module

Table 5-30 CTI BUS Pin-Out and Signal Descriptions (Cont)

General Section of the CTI BUS

Pin No.	Signal Name and Active State*	Transmit/ Receive†	Description
17	BMDEN L	T	Master drive enable (CPU puts data or address on bus (Section 5.3.3.1)
18	BDAL 08 L	T/R	Buffered data/address line (Section 5.3.3)
19	BWRITE L	T	Write (Section 5.3.9.1)
20	BDAL 07 L	T/R	Buffered data/address line (Section 5.3.3)
21	BWLB L	T	Write low byte (Section 5.3.9.1)
22	BDAL 06 L	T/R	Buffered data/address line (Section 5.3.3)
23	BWHB L	T	Write high byte (Section 5.3.9.1)
24	BDAL 05 L	T/R	Buffered data/address line (Section 5.3.3)
25	BSDEN L	T	Slave drive enable (slave device should put data on bus) (Section 5.3.3.1)
26	BDAL 04 L	T/R	Buffered data/address line (Section 5.3.3)
27	GND		
28	BDAL 03 L	T/R	Buffered data/address line (Section 5.3.3)
29	SS n L	T	Slot select (n = slot number) (Section 5.3.5.1)
30	BDAL 02 L	T/R	Buffered data/address line (Section 5.3.3)
31	IRQB n L	R	Interrupt request B from slot n (Section 5.3.6)
32	BDAL 01 L	T/R	Buffered data/address line (Section 5.3.6)

Table 5-30 CTI BUS Pin-Out and Signal Descriptions (Cont)

General Section of the CTI BUS

Pin No.	Signal Name and Active State*	Transmit/ Receive†	Description
34	BDAL 00 L	T/R	Buffered data/address line (Section 5.3.3)
35	OPRES n L	R	Option present in slot n (Section 5.3.4.2)
36	GND		
37	BDS L	T	Data strobe (Section 5.3.3.1)
38	+5.0 V		
39	BAS L	T	Address strobe (Section 5.3.3.1)
40	+12.0 V		
41	BSPARE 2		Reserved
42	BSPARE 3		Reserved
43	BIOSEL L	T	I/O select (Section 5.3.5.1)
44	BDAL 21 L	T/R	Buffered data/address line (Section 5.3.3)
45	BP 0 L	T/R	Bus priority level (Section 5.3.7)
46	BDAL 20 L	T/R	Buffered data/address line (Section 5.3.3)
47	BP 1 L	T/R	Bus priority level (Section 5.3.7)
48	BDAL 19 L	T/R	Buffered data/address line (Section 5.3.3)
49	BSPARE 1		Reserved
50	BDAL 18 L	T/R	Buffered data/address line (Section 5.3.3)

* B at beginning of signal name indicates a bused signal

† Transmit/receive with reference to the system module

Table 5-30 CTI BUS Pin-Out and Signal Descriptions (Cont)

General Section of the CTI BUS

Pin No.	Signal Name and Active State*	Transmit/ Receive†	Description
51	GND		
52	BDAL 17 L	T/R	Buffered data/address line (Section 5.3.3)
53	BMER L	R	Bus memory error (Section 5.3.2.5)
54	BDAL 16 L	T/R	Buffered data/address line (Section 5.3.3)
55	DMR n L	R	DMA request from slot n (Section 5.3.7)
56	DMG n L	T	DMA grant to slot n (Section 5.3.7)
57	BBUSY L	T/R	Bus busy (Section 5.3.7.1)
58	+5.0V		
59	BSPARE 4		Reserved
60	GND		

Private Section of the CTI BUS

The following connect to J8, remote access connector
61-76RAL 01-RAL 16

The following connect to J9, Network Connector (NET1)

77	TRANSMIT +	(J9 pin 3)
78	TRANSMIT –	(J9 pin 10)
79	RECEIVE +	(J9 pin 5)
80	RECEIVE –	(J9 pin 12)
81	COLLISION PRESENCE +	(J9 pin 2)
82	COLLISION PRESENCE –	(J9 pin 9)

Table 5-30 CTI BUS Pin-Out and Signal Descriptions (Cont)

General Section of the CTI BUS

Pin No.	Signal Name and Active State*	Transmit/ Receive†	Description
The following connect to J5, Video/Keyboard Connector			
83	RED RETURN		(J5 pin 3)
84	RED VIDEO		(J5 pin 11)
85	GREEN RETURN		(J5 pin 2)
86	GREEN VIDEO		(J5 pin 10)
87	BLUE RETURN		(J5 pin 1)
88	BLUE VIDEO		(J5 pin 9)
89	MONO RETURN		(J5 pin 4)
90	MONO VIDEO		(J5 pin 12)

* B at beginning of signal name indicates a bused signal

† Transmit/receive with reference to the system module

5.6 SPECIFICATIONS

The following paragraphs provide the specifications for the system module.

5.6.1 Physical Specifications

5.6.1.1 Dimensions and Weight

Length	40.0 cm (16 in)
Width	26.0 cm (10.4 in)
Height	2.25 cm (0.9 in) (without back panel and card cage) 15.25 cm (6.1 in) (with back panel and card cage)
Weight	1.12K Kg (2.5 lb) (with 2 memory boards installed) (approximate)

5.6.1.2 Module Interconnects – Figure 5-37 shows the position of all the connectors on the Professional 350 system module. Table 5-31 indicates the type and function of each connector. The pinning for each connector is listed in Section 5.5.

5.6.2 Power Requirements

The following paragraphs provide the power requirements.

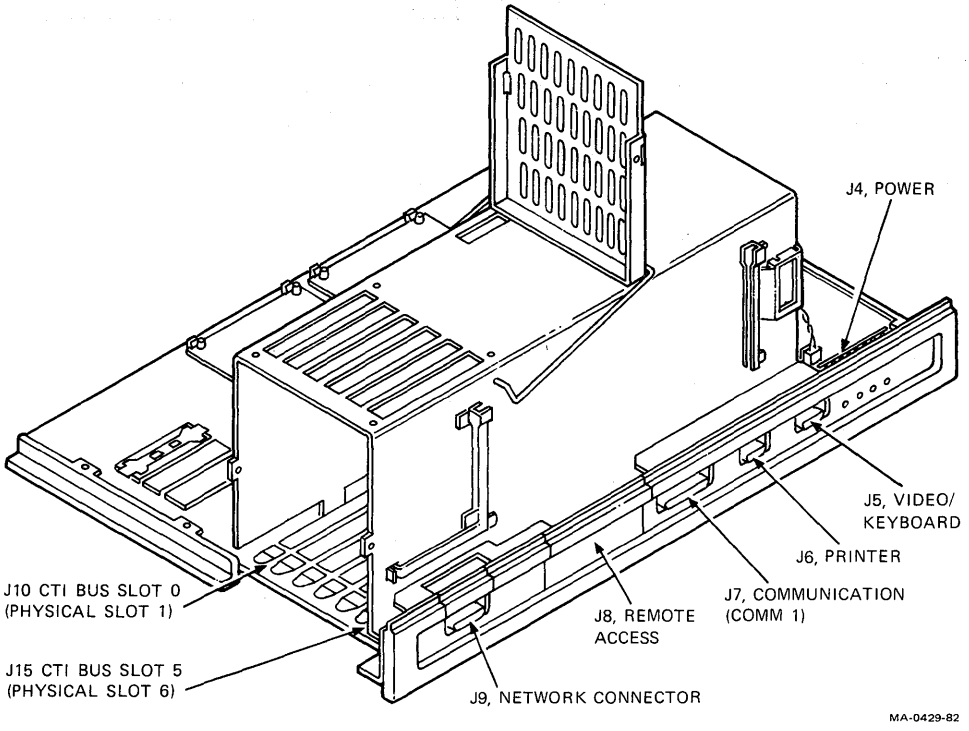


Figure 5-37 Connector Placement

Table 5-31 Connector Types

Connector	Function	Type
J1,J2	Memory boards	40-pin male
J3	Battery	2-pin male
J4	DC power	16-pin male
J5	Video/keyboard	15-pin male D-subminiature
J6	Printer	9-pin male D-subminiature
J7	Communication	25-pin male D-subminiature
J8	Remote access	22-pin finger receptacle
J9	Network	15-pin female D-subminiature
J10-J15	CTI BUS options	90-pin ZIF T-rail

5.6.2.1 DC Power Requirements – The dc power requirements are as follows.

Voltage	Current Tolerance	Typical	Maximum
+12.0 V	+5%, −5%	320 mA	500 mA
+5.0 V	+5%, −5%	5.0 A	6.0 A
−12.0 V	+5%, −5%	60 mA	100 mA

(This data includes two 128 kilobyte memory modules but has no devices connected to any of the I/O ports.)

5.6.3 Environmental Specifications

The following paragraphs provide the environmental specifications.

5.6.3.1 Temperature

Operating

5° C (41° F) min
60° C (140° F) max

The temperature limits are specified as the free air ambient temperature around the module. See Section 5.6.3.4 for airflow and temperature requirements when the module is enclosed in the system box.

The maximum allowable operating temperature is reduced by 1.8° C per 1000 meters (1° F per 1000 feet) above sea level.

NOTE
The accuracy of the real time clock oscillator is ± 0.002 % over the temperature range of +10° C to +50° C (50° F to 122° F). Beyond these limits the clock still functions but the accuracy is degraded.

Storage

−40° C (−40° F) min
66° C (151° F) max

Before operating a module which is at a temperature beyond the operating range, that module must first be brought to an environment within the operating range and then must be allowed to stabilize for a reasonable length of time. (Five or more minutes depending on the air circulation.)

5.6.3.2 Relative Humidity

Operating

10% min
95% max

The wet bulb temperature must not exceed 32° C (90° F) and the dew point must not be less than 2° C (36° F).

Storage

10% min
95% max

5.6.3.3 Altitude

Operating

50,000 ft (90 mm mercury) max

The maximum operating temperature must be derated at high altitudes (Section 5.6.3.1).

Storage

50,000 ft (90 mm mercury) max

The module is not mechanically or electrically damaged at altitudes up to 50,000 feet.

5.6.3.4 Airflow – Operating

Adequate airflow must be provided to limit the inlet to outlet temperature rise across the module. When operating above 55° C (131° F), the outlet temperature must not exceed 65° C (149° F). When operating below 55° C (131° F), the inlet to outlet temperature rise must not exceed 10° C (18° F).

CHAPTER 6
LK201 KEYBOARD DESCRIPTION

6.1 INTRODUCTION

This chapter describes the LK201 keyboard used on the Professional 300 Series of personal computers. The shaded part of Figure 6-1 shows its relationship in the system block diagram.

The keyboard is the user interface to the system. It detects keystrokes, encodes them, and transmits the information to the central processor. The keyboard also receives information from the central processor.

Communication between the keyboard and the central processor in the system box is full duplex, serial asynchronous at a speed of 4800 baud. The communication lines conform to EIA Standard RS-423 which applies to unbalanced voltage interfaces.

6.1.1 Related Documentation

Refer to the following related documentation while reading this chapter.

Title	Documentation No.
LK201 Maintenance Print Set	MP-01395-00

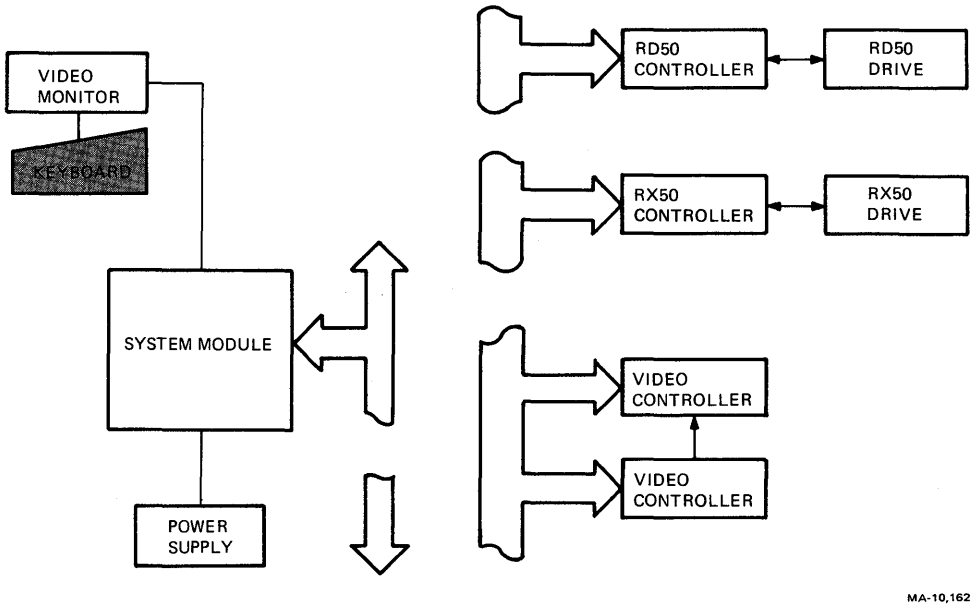


Figure 6-1 System Block Diagram

6.2 PHYSICAL DESCRIPTION

The keyboard used in the Professional 300 Series has 105 keys arranged in the following four groups Figure 6-2.

- Main keypad (57 keys)
- Numeric keypad (18 keys)
- Special function keypad (20 keys)
- Editing keypad (10 keys)

The keycaps can be installed manually, but require a special tool for removal.

The keyboard circuitry is contained in a low profile cabinet that has a 30 mm nominal height from table top to home row. The keyboard case is made of two plastic shells that can be separated with a screwdriver. Non-slip plastic strips along the bottom prevent the keyboard from sliding on a table top. Two feet can be manually inserted in holes to raise the back edge of the keyboard.

A plastic window along the top edge above the special function keys can be lifted to insert a user function label. The label, a thin paper strip, fits into the indented space and varies according to the application program.

A coiled cable (PN BCC01), with a 4-pin modular connector on each end, connects the keyboard to the video monitor. The keyboard transmits four signals to the monitor which pass unchanged to the system box via the video cable (Figure 6-3). The four signals are as follows.

- +12 V power to keyboard
- ground to keyboard
- SERIAL OUT (transmit line from keyboard)
- SERIAL IN (receive line to keyboard)

The cable can be placed in a channel in the bottom case and the modular type telephone connector fits into the jack, J4. The cable can be inserted in the channel to either side of the keyboard. Section 6.6 provides the specifications for the keyboard.

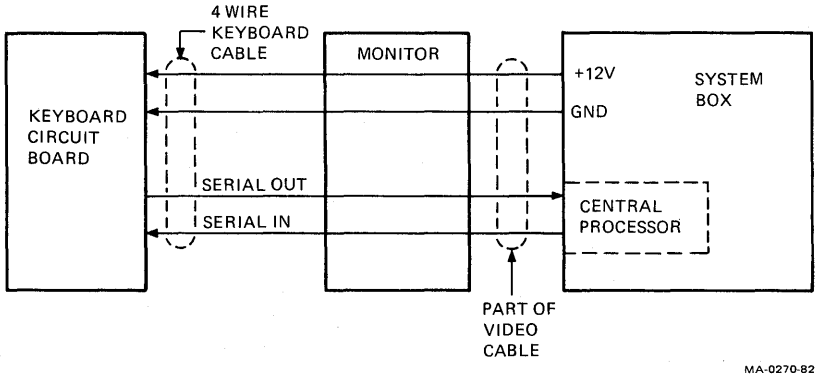


Figure 6-2 Keyboard Cable Connections

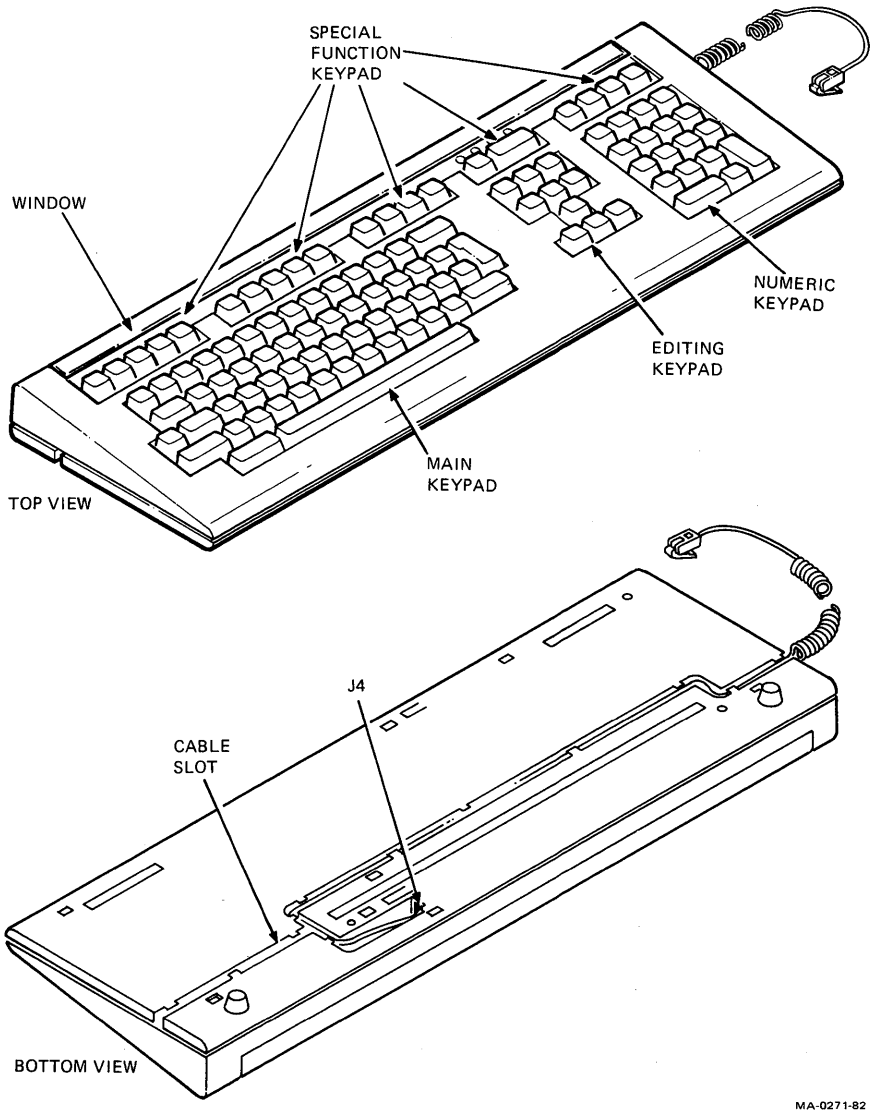


Figure 6-3 LK201 Keyboard

6.3 FUNCTIONAL DESCRIPTION

The following sections provide a functional description of the LK201 keyboard.

6.3.1 Overview of Keyboard Operation

Figure 6-4 shows a simplified block diagram of the keyboard circuitry. Everything except the block marked KEYBOARD SWITCH MATRIX is on the printed circuit board. This block represents the connections between the keyboard switches and the signals from the 8051 microprocessor.

The firmware in the 8051 8-bit microprocessor controls three major keyboard operations at the same time.

1. Scans the keyboard to detect changes in the keyboard matrix.
2. Transmits the results of the keyboard scan to the system central processor.
3. Receives information from the system central processor.

6.3.1.1 Keyboard Scanning – The keyboard switches are connected at the intersections of an 18 × 8 line matrix. This provides a fixed position identifier for each key.

The firmware scans the 18-line axis and detects a depressed or newly released key by reading the 8-line axis. The firmware then verifies the detected keystroke and changes this positional information into an 8-bit code that is unique to that key.

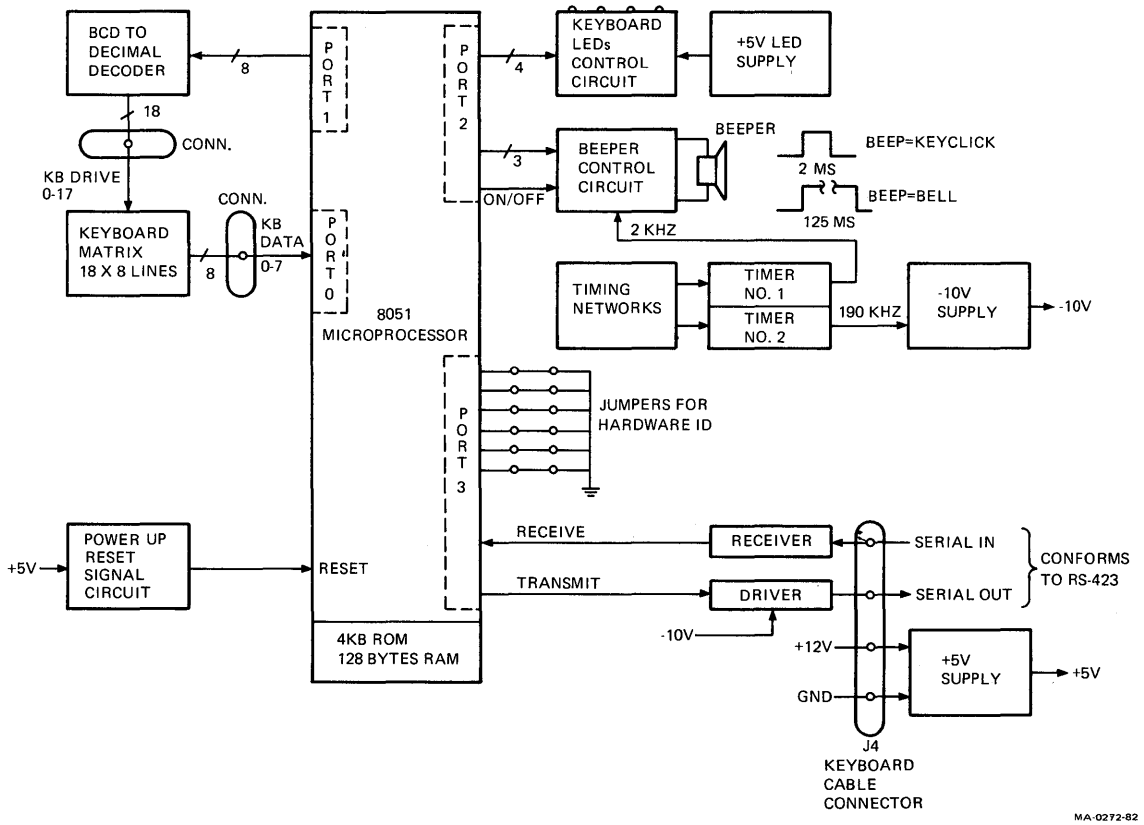


Figure 6-4 Simplified Block Diagram of LK201 Keyboard Circuitry

6.3.1.2 Control of Audio Transducer and Indicators – Two circuits control the audio transducer and the indicators. One circuit receives its inputs from the 8051 and controls the transducer (beeper). A long beep represents the bell and a short beep represents the keyclick.

A separate circuit, controlled by a signal from the 8051, controls each of the four indicators. The firmware, responding to commands received from the system central processor, turns the indicators on or off.

6.3.2 Keyboard Firmware Functions

This section describes the keyboard firmware functions. The functions are divided into two categories: those that cannot be changed by instructions from the system central processor and those that can be changed by instructions from the system central processor.

6.3.2.1 Functions Not Changed by System Central Processor Instructions – The following functions cannot be changed by instructions from the system central processor.

- Power-up test
- Keycodes
- Special codes

Power-Up Test

Upon power up, the firmware performs a self-test in less than 70 ms. The test results are transmitted to the system central processor in four bytes.

The keyboard indicators are lit during self-test. The indicators blink once during the self-test routine. The indicators remain lit if the test fails but go off if the test is passed. The system module can also request self-test at any time.

Keycodes

The keycodes represent fixed positions in the key switch matrix. The key associated with a particular matrix position is always represented by the same keycode.

Special Codes

There are 13 special codes transmitted by the keyboard. Four codes transmit the results of the power-up self-test. The other nine codes are status indicators or command acknowledgements.

6.3.2.2 Functions Changed by System Central Processor Instructions – The system central processor can issue instructions to change some keyboard transmission characteristics and to control the keyboard indicators and beeper.

Upon completion of a successful power-up self-test, the firmware sets certain functions to predetermined conditions. They are referred to as default conditions. The conditions can be changed but they always come up to the default condition after a successful power-up self-test.

6.3.2.3 Firmware Functions That Can be Changed – Certain firmware functions can be changed by commands (instructions) from the system central processor. These commands are categorized as transmission commands and peripheral commands. Transmission commands contain a mode set command and an auto-repeat rate set command. Peripheral commands contain a variety of commands. Refer to Section 6.5.5.3 for more information on peripheral commands.

6.4 Detailed Keyboard Circuit Description

The following section describes the keyboard circuit. Figure 6-4 shows the LK201 keyboard block diagram.

6.4.1 Keyboard Matrix Scanning

The key locations are arranged in an 18 × 8 line matrix. Each key switch is connected across a matrix intersection. This gives a fixed position for each key connected in the matrix. This matrix accommodates all 105 keys in the LK201 keyboard.

Figure 6-5 is a simplified block diagram of the matrix scanning circuit. Eight lines from PORT 1 of the 8051 microprocessor go to the binary coded decimal (BCD) inputs of two 74LS145 BCD-to-decimal decoders. Ten outputs from one decoder and eight outputs from the other decoder provide the drive lines for the matrix. These 18 lines are called KB DRIVE 0–17.

The other axis of the matrix consists of eight lines tied to +5 V through pull-up resistors. These lines go to PORT 0 of the 8051 microprocessor and are called KB DATA 0–7.

The 8051 scans the 18 drive lines. Key closures are detected by reading the eight data lines. The complete matrix is scanned every 8.33 ms.

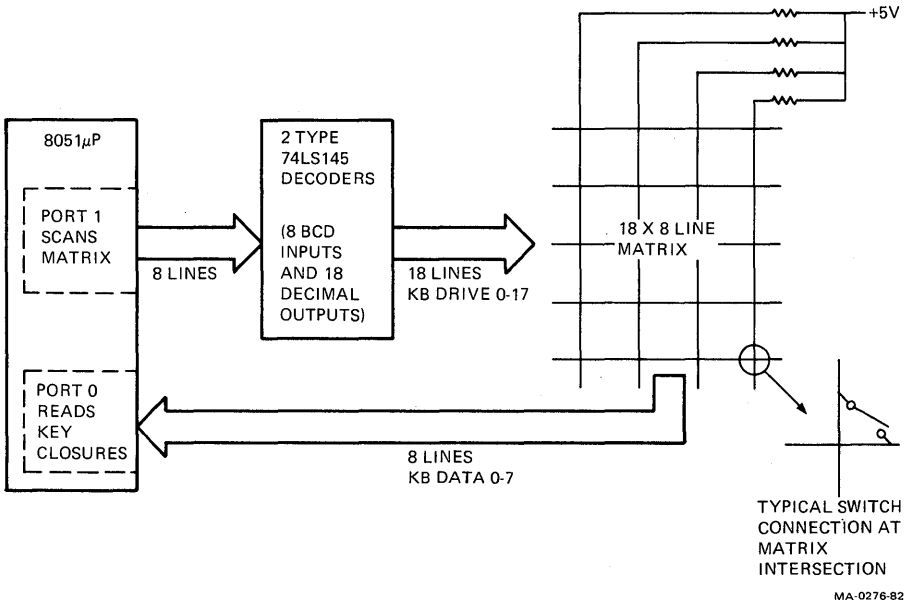


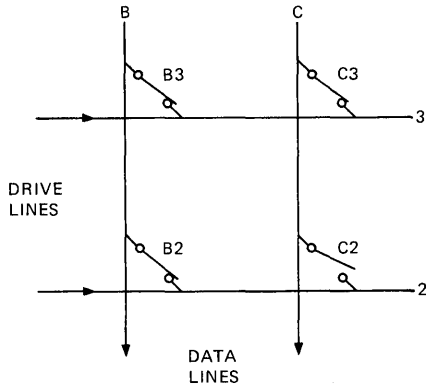
Figure 6-5 Simplified Block Diagram of Matrix Scanning Circuit

When a key closure is detected, it is scanned again to verify that it is really a key closure and not electrical noise.

Once the key closure is verified, the 8051 firmware translates the position information into a key code and transmits it to the system central processor. Transmission is handled by the Universal Asynchronous Receiver Transmitter (UART) in the 8051.

A sneak path or ghost key indication can occur when three of the four corners of a matrix rectangle are closed (Figure 6-6). The key positions in the matrix are arranged to avoid sneak paths. However, if a sneak path does occur, the firmware prevents the keycode for the key (which caused the sneak path) to be transmitted until one of the involved keys is released. This prevents transmission of ghost keys entirely.

Table 6-1 shows the keyboard matrix on the LK201-AA (American) keyboard. Keycap designations are shown for reference only and can be compared to Figure 6-7.



1. CONDITIONS ARE: SWITCHES B2, B3, AND C3 CLOSED, SWITCH C2 OPEN; LINE 2 IS BEING DRIVEN AND LINE C IS BEING READ.

2. INTERSECTION C2 IS BEING LOOKED AT. IT SHOULD NOT SHOW A KEY CLOSURE BECAUSE SWITCH C2 IS OPEN.

3. HOWEVER A SNEAK PATH IS PRESENT FROM LINE 2 THROUGH SWITCHES B2, B3, AND C3 TO LINE C. A GHOST KEY IS READ AT INTERSECTION C2.

MA-0273-82

Figure 6-6 Example of Ghost Key Generation

Table 6-1 Keyboard Matrix

Refer to Figures 6-7A and 6-7B. They show the international matrix for the LK201 keyboard. The legends provided are from the LK201-AA keyboard and are provided for convenience only.

KB DRIVE	KB DATA 7	6	5	4	3	2	1	0
17	Reserved	F19	Reserved	F20	PF4	N__ (Note 1)	N,	ENTER
		G22		G23	E23	D23	C23	A23
16	F18	PF3	Reserved	N9	↓	N6	N3	N.
	G21	E22		D22	B17	C22	B22	A22
15	F17	PF2	Reserved	N8	N5	→	N2	N0 (See
	G20	E21		D21	C21	B18	B21	Note 2)
14	PF1	NEXT SCREEN	REMOVE	↑	N7	N4	N1	N0
	E20	D18	E18	C17	D20	C20	B20	A20
13	INSERT HERE	_ -	D0	PREV SCREEN	{ [	" '	Reserved	Reserved
	E17	E11	G16	D17	D11	C11		
12	FIND	+ =	HELP	SELECT	}]	RETURN	←	
	E16	E12	G15	D16	D12	C13	B16	C12
11	ADDTNL OPTIONS	X (delete)	Reserved	) 0	P	See Note 3	: ;	? /
	G14	E13		E10	D10		C10	B10
10	Reserved	F12	Reserved	F13	(9	O	L	. .
		G12		G13	E09	D09	C09	B09
9	Reserved	F11	Reserved	Reserved	* 8	I	K	, ,
		G11			E08	D08	C08	B08
8	Reserved	MAIN SCREEN	Reserved	EXIT	& 7	U	J	M
		G08		G09	E07	D07	C07	B07

Table 6-1 Keyboard Matrix (Cont)

KB DRIVE	KB DATA 7	6	5	4	3	2	1	0
7	Reserved	CANCEL	Reserved	RESUME	^ 6	Y	H	N
		G07		G06	E06	D06	C06	B06
6	Reserved	Reserved	Reserved	INTER-RUPT	% 5	T	G	B
				G05	E05	D05	C05	B05
5	SETUP	F5	Reserved	$ 4	R	F	V	SPACE
	G02	G03		E04	D04	C04	B04	A01–A09
4	Reserved	PRINT SCREEN	Reserved	BREAK	# 3	E	D	C
		G00		G01	E03	D03	C03	B03
3	HOLD SCREEN	@ 2	Reserved	TAB	W	S	X	> <
	G99	E02		D00	D02	C02	B02	B00
2	Reserved	Reserved	Reserved	~	! 1	Q	A	Z
				E00	E01	D01	C01	B01
1	CTRL	LOCK	COMPOSE	Reserved				
	C99	C00	A99					
0	SHIFT							
	B99,B11							

NOTES

1. Note that N0 – N9, N__, N,, and N. refer to the numeric keypad.
2. N0 of the numeric keypad can be divided into two keys. Normally only the N0 keyswitch is implemented as a double size key.
3. The RETURN key also can be divided into two keys. The one which is decoded as return is the RETURN (C13) key.

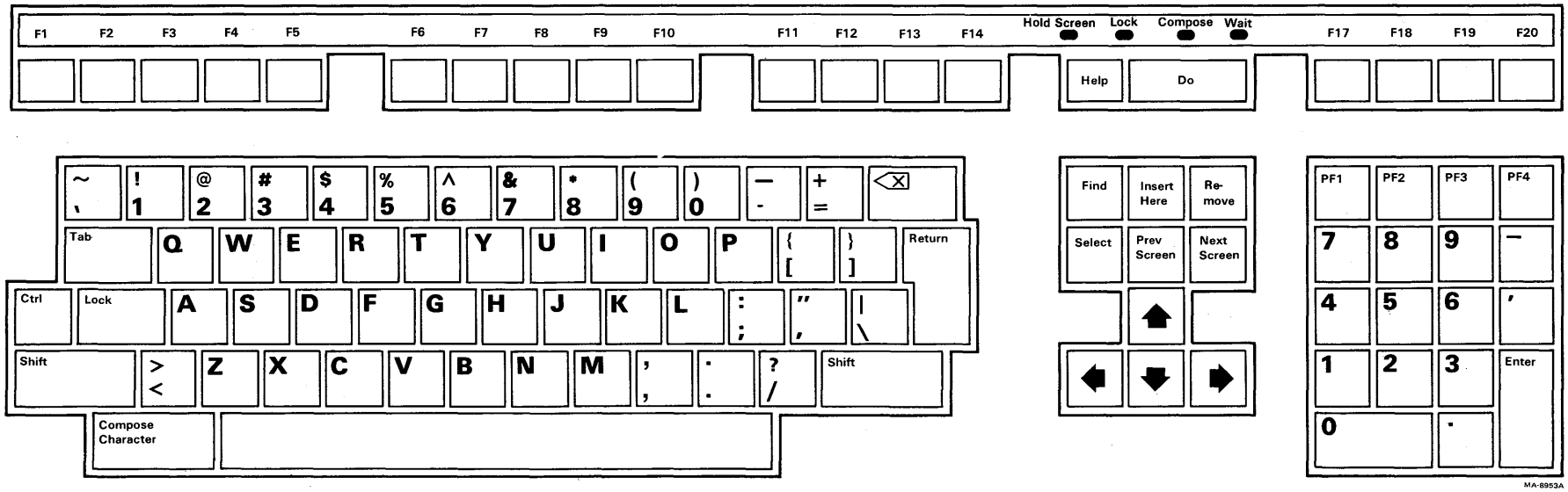
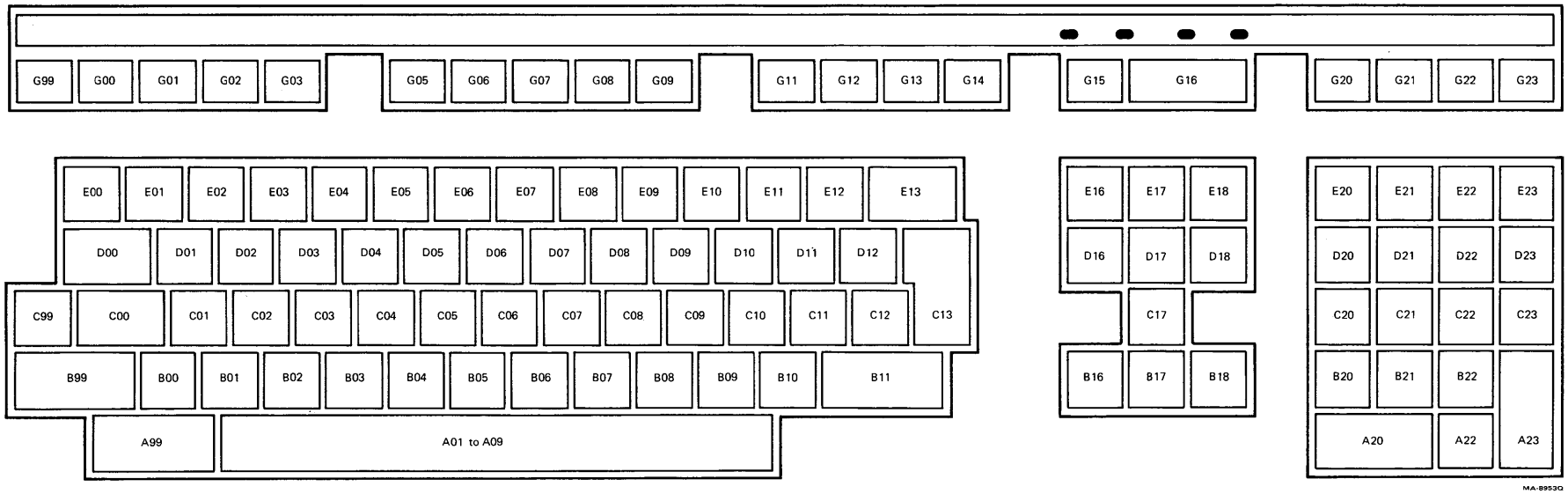


Figure 6-7A LK201-AA Keyboard Layout



NOTE: THE GRAPHIC CHARACTERS ARE SHOWN FOR ILLUSTRATION PURPOSES ONLY AND ARE NOT MEANT TO ASSIGN KEYCAP USAGE OR LEGENDS.

Figure 6-7B LK201-AA Keyboard Layout

6.4.2 Audio Transducer Control Circuit

Figure 6-8 shows the audio transducer or beeper control circuit. The beeper is driven by a transistor whose base is connected to a 2 kHz square wave from a 556 timer IC. This signal is biased by a network of four type 74LS05 open collector inverters. The 8051 microprocessor controls all four inverters via the firmware. The ON/OFF inverter connects directly to the transistor base. When the 8051 puts a high on the ON/OFF inverter input, its output goes low and removes the 2 kHz square wave from the transistor base. This cuts off the transistor and disables the beeper.

To turn on the beeper, the 8051 puts a low on the ON/OFF inverter input. Its output goes high and allows the 2 kHz signal to reach the transistor base. This turns on the beeper. The firmware generates a keyclick (on for 2 ms) or a bell tone (on for 125 ms).
The 8051 sets up the three level control inverters by putting one of eight binary combinations on the inverter inputs. All highs give the softest sound and all lows give the loudest sound.

The firmware controls the keyclick and the bell tone independently. The bell tone is sounded only upon request from the system control processor. The keyclick is sounded (unless disabled) under the following conditions.

- When a key is depressed
- When a metronome code is sent
- When a command to sound the keyclick is received from the system control processor

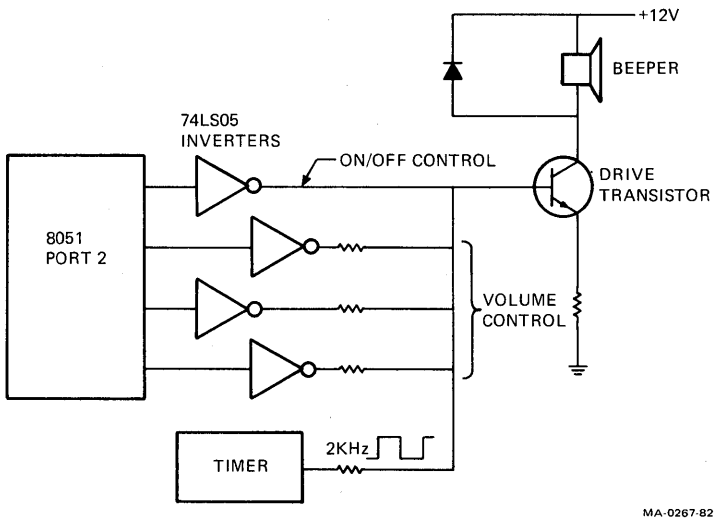


Figure 6-8 Beeper Control Circuit

6.4.3 Indicator (LED) Control Circuit

Figure 6-9 shows the LED indicator control circuit.

The control signal for each LED comes from PORT 2 of the 8051 to the input of a type 74LS05 open collector inverter. The inverter output goes to the LED cathode; its anode is connected to +5 V. A separate +5 V source relieves the LEDs load on the main +5 V supply.

A low signal from the 8051 drives the inverter output high which cuts off the LED. A high signal from the 8051 drives the inverter output low. This provides a path to ground from the +5 V through the LED. The LED then turns on.

6.4.4 Keyboard Communication

The following sections describe the keyboard communication.

6.4.4.1 Keyboard Transmit Mode – The keyboard codes and a few other special codes are transmitted via a serial line output in PORT 3 of the 8051. The transmitted signal goes from the 8051 to a driver, through the keyboard cable, monitor, and video cable to the system central processor. A UART within the 8051 controls the transmission.

Transmitted characters conform to a specific format. Each character is 10 bits long. The first bit is the START bit. It is always a logical 0 (space). The next eight bits represent the encoded data. The last bit is the STOP bit. It is always a logical 1 (mark). Figure 6-10 shows the character format.

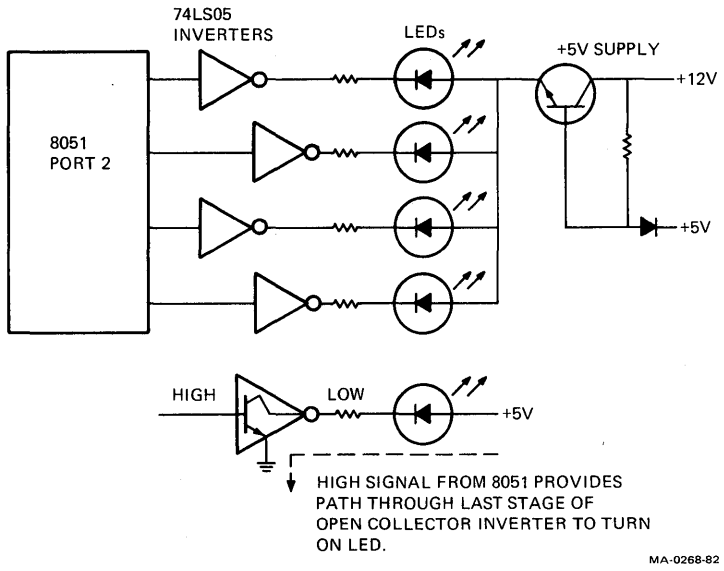


Figure 6-9 Indicator (LED) Control Circuit

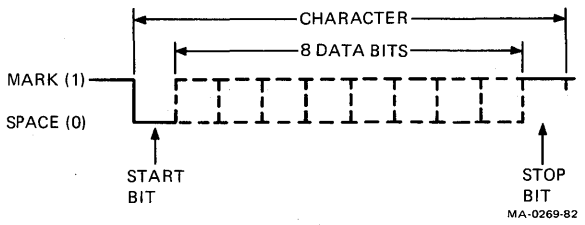


Figure 6-10 Keyboard Transmit and Receive Character Format

6.4.4.2 Keyboard Receive Mode – The firmware contains features that can be enabled by commands from the system central processor. There are two categories of features: one sets keyboard transmission characteristics and the other controls the keyboard peripherals. A peripheral command covers indicator control, bell and keyclick loudness, keyboard ID code, and reinstate keyboard. The commands come from the system central processor, through the video cable, monitor, and keyboard cable to the receiver and into the 8051 via PORT 3. They go to the UART in the 8051.

Received characters conform to the same 10-bit format used for transmitted characters. The eight data bits are arranged in a specified protocol depending on the command type.

6.4.5 Reset Signal for 8051 Microprocessor
Whenever the system is turned on, the 8051 microprocessor in the keyboard must be reset. This allows the 8051 to start operating.

The reset signal generator is active only during powerup. The input is +5 V. The output is connected to the RESET input of the 8051. When power is turned on, the +5 voltage starts to rise from zero. The reset signal circuit output follows it and drops off when a steady state of +5 V is reached. This circuit holds the 8051 RESET input high (+3.5 V to +5 V) long enough to enable the reset action in the 8051. This action occurs only during powerup.

6.4.6 Hardware Keyboard Identification (ID)
At power up, the keyboard performs a self-test and sends the results to the system central processor. One piece of information to be sent is the keyboard hardware ID which is read from hardwired jumpers.

There are six jumpers. Each jumper line goes from an input in PORT 3 of the 8051 to ground. All jumpers are installed so the keyboard hardware ID is zero.

6.4.7 Voltage Supplies
The only voltage sent to the keyboard is +12 V. However, +5 V and −10 V are also required. These voltages are derived from the +12 V.

There is a +5 V supply that handles most of the requirements for this voltage. The four keyboard LEDs have their own +5 V supply. A −10 V supply provides voltage for the driver in the SERIAL OUT line.

6.5 KEYBOARD PROGRAMMING

This section describes the functions that the keyboard performs under system central processor control. It also describes keyboard programming machine language. High level user programming is not described here.

6.5.1 Keyboard Layout and Key Identification

Each keyboard key has a unique location. Each location is scanned, and when closure or release is detected, the location is verified. This is then decoded to an 8-bit keycode. Figure 6-7 shows the keyswitch locations. Table 6-2 shows the 14 functional divisions of the keyboard. Table 6-3 shows the divisions, keycaps, and keycodes.

Table 6-2 Keyboard Functional Divisions

Division	Description	Representation
1	48 graphic keys, Spacebar	0001
2	Numeric keypad	0010
3	Delete Character (E12)	0011
4	Return (C13) Tab (D00)	0100
5	Lock (C00) Compose (A99)	0101
6	Shift (B99 and B11), CTRL (C99)	0110
7	Horizontal cursors (B16 and B18)	0111
8	Vertical cursors (B17 and C17)	1000
9	Six keys directly above the cursor keys (D16-D18 and E16-E18)	1001
10	Function keys (G99-G03)	1010
11	Function keys (G05-GO9)	1011
12	Function keys (G11-G14)	1100
13	Function keys (G15-G16)	1101
14	Function keys (G20-G23)	1110

Table 6-3 Keycode Translation Table

Division	Position	Keycap	Keycode (dec)	Keycode (hex)
Function Keys				
10	G99	Hold screen	086	56
	G00	Print screen	087	57
	G01	Break	088	58
	G02	Setup	089	59
	G03	F5	090	5A
		Reserved	091–098	5B–62
11		Reserved	099	63
	G05	Interrupt	100	64
	G06	Resume	101	65
	G07	Cancel	102	66
	G08	Main screen	103	67
	G09	Exit	104	68
		Reserved	105–110	69–6E
12			111	6F
		Reserved	112	70
	G11	F11 (ESC)	113	71
	G12	F12 (BS)	114	72
	G13	F13 (LF)	115	73
	G14	Addtnl opt's	116	74
		Reserved	117–122	75–7A
13		Reserved	123	7B
	G15	Help	124	7C
	G16	D0	125	7D
14		Reserved	126–127	7E–7F
	G20	F17	128	80
	G21	F18	129	81
	G22	F19	130	82
	G23	F20	131	83
		Reserved	132–135	84–87
6 Basic Editing Keys				
9		Reserved	136–137	88–89
	E16	Find	138	8A
	E17	Insert here	139	8B
	E18	remove	140	8C
	D16	Select	141	8D
	D17	Prev screen	142	8E
	D18	Next screen	143	8F
		Reserved	144	90

Table 6-3 Keycode Translation Table (Cont)

Division	Position	Keycap	Keycode (dec)	Keycode (hex)
Keypad				
2		Reserved	145	91
	A20	0	146	92
		Reserved	147	93
	A22	.	148	94
	A23	Enter	149	95
	B20	1	150	96
	B21	2	151	97
	B22	3	152	98
	C20	4	153	99
	C21	5	154	9A
	C22	6	155	9B
	C23	,	156	9C
	D20	7	157	9D
	D21	8	158	9E
	D22	9	159	9F
	D23	-	160	A0
	E20	PF1	161	A1
	E21	PF2	162	A2
	E22	PF3	163	A3
	E23	PF4	164	A4
		Reserved	165	A5
Cursor Keys				
7		Reserved	166	A6
	B16	Left	167	A7
	B18	Right	168	A8
8	B17	Down	169	A9
	C17	Up	170	AA
		Reserved	171–172	AB–AC
Shift, Lock CTRL, A99 and A10				
6		Reserved	173	AD
	B99,B11	Shift	174	AE
	C99	CTRL	175	AF
5	C00	Lock	176	B0
	A99	Compose	177	B1
		Reserved	178	B2

Table 6-3 Keycode Translation Table (Cont)

Division	Position	Keycap	Keycode (dec)	Keycode (hex)
Special Codes				
		All Ups	179	B3
		Metronome	180	B4
		Output error	181	B5
		Input error	182	B6
		KBD LOCKED acknowledge	183	B7
		TEST MODE acknowledge	184	B8
		PREFIX to keys down	185	B9
		MODE CHANGE acknowledge	186	BA
		Reserved	187	BB
Delete				
3	E13	Delete (X)	188	BC
Return and Tab				
4	C13	Return	189	BD
	D00	Tab	190	BE
48 Graphics Keys and Space Bar				
1	E00	Tilde	191	BF
	E01	!1	192	D0
	D01	Q	193	C1
	C01	A	194	C2
	B01	Z	195	C3
		Reserved	196	C4
	E02	@2	197	C5
	D02	W	198	C6
	C02	S	199	C7
	B02	X	200	C8
	B00	><	201	C9
		Reserved	202	CA
	E03	#3	203	CB
	D03	E	204	CC
	C03	D	205	CD
	B03	C	206	CE
		Reserved	207	CF
	E04	$4	208	D0
	D04	R	209	D1
	C04	F	210	D2
	C04	V	211	D3

Table 6-3 Keycode Translation Table (Cont)

Division	Position	Keycap	Keycode (dec)	Keycode (hex)
	A01–A09	Space	212	D4
		Reserved	213	D5
	E05	%5	214	D6
	D05	T	215	D7
	C05	G	216	D8
	B05	B	217	D9
		Reserved	218	DA
	E06	^6	219	DB
	D06	Y	220	DC
	C06	H	221	DD
	B06	N	222	DE
1		Reserved	223	DF
	E07	&7	224	E0
	D07	U	225	E1
	C07	J	226	E2
	B07	M	227	E3
		Reserved	228	E4
	C08	*8	229	E5
	D08	I	230	E6
	C08	K	231	E7
	B08	‘‘	232	E8
		Reserved	233	E9
	E09	(9	234	EA
	D09	0	235	EB
	C09	L	236	EC
	B09	. .	237	ED
		Reserved	238	EE
	E10	)0	239	EF
	D10	P	240	F0
		Reserved	241	F1
	C10	: ;	242	F2
	B10	? /	243	F3
		Reserved	244	F4
	E12	+ =	245	F5
	D12	}]	246	F6
	C12	| \	247	F7
		Reserved	248	F8
	E11	_ -	249	F9
	D11	[	250	FA
	C11	. ,	251	FB
		Reserved	252-255	FC-FF

NOTE
The legends under “keycap” are taken from the keycap legends of the LK201-AA (American).

Keycodes 00 through 64 are reserved. Keycodes 65 through 85 are unused.

6.5.2 Modes

This section describes the function of the keycode transmission modes. The mode set command allows any one of the 14 keyboard divisions to be set to any one of the following three modes. (Refer to Section 6.5.7 for division defaults.)

- **Down Only Mode** – The keyboard transmits a keycode when the key is depressed.
- **Autorepeat Down** – The keyboard transmits a keycode when the key is first depressed. If the key is held down past the specified timeout period (usually 300 to 500 ms), a fixed metronome code is sent at the specified rate until the key is released.
- **Down/up** – The keyboard transmits a keycode when the key is depressed and an "up code" when the key is released. If any other **DOWN/UP** keys are depressed, the "up code" is a repeat of the "down code." If no other **DOWN/UP** keys are depressed, the keyboard sends an ALL UPS code.

6.5.2.1 Special Considerations Regarding Autorepeat – The Autorepeat Rate Set command allows the following changes in the autorepeat mode.

- Autorepeat rate buffer association – The buffer association can be changed for the selected keyboard division.
- The timeout and interval values can be changed in any one of the four autorepeat rate buffers.
- If multiple autorepeating keys are held down, metronome codes are still generated. The metronome codes apply to the keycode transmitted most recently. If the last key pressed down is released, and other key(s) is(are) still down, the keycode(s) of the key(s) still down is (are) retransmitted.

Example: The **a** key is held down.

This produces the following transmission.

a metronome metronome

Now the **b** key is depressed. This produces the following transmission.

a metronome metronome b metronome metronome

Now the **b** key is released. This produces the following transmission.

a metronome metronome b metronome metronome a metronome met. . .

While metronome codes are being generated for an autorepeating key, a non-autorepeating keycode or special code may be transmitted. The keyboard transmits this special code instead of the next metronome code and then returns to the autorepeated code. The keycode to be autorepeated is always the last byte transmitted.

Example: The **a** key is held down.

This produces the following transmission.

a metronome metronome

Now the **SHIFT** key is depressed. This produces the following transmission.

a metronome metronome shift a metronome

Now the **SHIFT** key is released. This produces the following transmission.

a metronome metronome shift a metronome ALL UPS a metronome. . .

- If an autorepeating key is not to autorepeat (for example, **CNTL C**), the system module must issue a Temporary Inhibit Autorepeat command. This halts the transmission of any metronome codes or keyclicks for that key only. Metronome codes continue when another key is depressed. The command must be issued after the keycode for the autorepeating key is received.

- Autorepeat can be enabled and disabled independently of the division settings by using the Enable/Disable Autorepeat commands. These commands apply to all keys on the keyboard. When autorepeat is disabled, internally the keyboard continues to autorepeat characters. However, it does not transmit metronome codes or keyclicks. When autorepeat is enabled, the keyboard transmits the metronome codes from the point they were before autorepeat was disabled. This may be within either the timeout or interval period, depending upon the time elapsed since key depression.

- If the keyboard receives a request to change a division mode to autorepeat while a key is depressed, the keyboard makes the change immediately. After the specified timeout period, the keyboard transmits metronome codes for the depressed key. In place of the first metronome code, the keyboard transmits the keycode of the autorepeating key.

All autorepeating division modes can be changed to down only with one command. This and other autorepeat commands are grouped with the peripheral commands (Section 6.5.5.3).

6.5.2.2 Special Considerations Regarding Down/Up Mode – If two **DOWN/UP** keys are released simultaneously (within the same scan), and there are no other **DOWN/UP** keys down on the keyboard, only one ALL UPS code is generated.

6.5.2.3 Autorepeat Rates – There are four buffers in the keyboard to store autorepeat rates. They are numbered 0 through 3. Each buffer stores the following two values. These values can be changed by the system module.

- The timeout value
- The interval value

The timeout value is the amount of time between the detection of a down key and the transmission of the first metronome code (defaults range from 300 to 500 ms). The interval value is the number of metronome codes per second (defaults to 30).

Each division is associated with one of the four buffers. Rates are taken from the associated buffer each time the autorepeat timers are loaded. This buffer-to-division association can be changed by the system module or left to default.

6.5.3 Keyboard Peripherals

This section describes the peripherals available on the keyboard. The keyclick, bell, and LEDs are all considered keyboard peripherals. Refer to Section 6.5.5.3 for information on system module control of these peripherals.

6.5.3.1 Audio – The keyclick is a 2 ms beep and the bell is a 125 ms beep. The bell is sounded only upon request from the system module. The keyclick (if not disabled by the system module) is sounded under the following three conditions.

- When a key is depressed
- When a metronome code is sent
- When the system module receives a sound keyclick command.

If either the **B11** or **B99** keys (the left and right **SHIFT** keys on the LK201) or the **C99** key (the **CNTL** key on the LK201) are depressed, the keyclick is not generated. However, if a command is sent from the system module to enable the keyclick on the **C99** key, the keyclick is generated (Section 6.5.5.3). Figure 6-7 shows the positions of these keys.

The keyclick or bell (or both) may be disabled. When the keyclick or bell is disabled, it does not sound. If the system module requests sound (Section 6.5.5.3), the keyclick or the bell does not sound.

Both the keyclick and bell may be set independently to one of the following eight volume levels.

000 – highest
001
010 – default
011
100
101
110
111 – lowest

6.5.3.2 Indicators (LEDs) – The system module normally transmits indicator control commands. However the following are exceptions.

- Upon power up, the keyboard turns all LEDs off.

- After receiving the Inhibit Transmission command, the keyboard turns on the keyboard locked LED. The LED is turned off after the keyboard receives a Resume Transmission command.

6.5.4 Keyboard-to-System Module Protocol

The following paragraphs describe the keyboard-to-system module protocol.

6.5.4.1 Keycode Transmission – The keyboard transmits single byte keycodes that reflect the keyboard matrix status. The 8-bit codes above 64_{10} are used for keycodes. Every key is identified by a unique keycode. There are no special codes for shifted or control keys.

Refer to Figure 6-7 and Tables 6-1 and 6-2 for the complete keycode matrix translation table.

6.5.4.2 Special Code Transmission – There are 13 special codes: nine codes with values above 64_{10} and four codes below.

The following are the nine special codes above 64_{10} (keycode value range).

- ALL UPS — Keycode 179 (dec), B3 (hex)
- METRONOME CODE — Keycode 180 (dec), B4 (hex)
- OUTPUT ERROR — keycode 181 (dec), B5 (hex)
- INPUT ERROR — Keycode 182 (dec), B6 (hex)
- KBD LOCKED ACK — Keycode 183 (dec), B7 (hex)
- TEST MODE ACK — Keycode 184 (dec), B8 (hex)
- PREFIX TO KEYS DOWN — Keycode 185 (dec), B9 (hex)
- MODE CHANGE ACK — Keycode 186 (dec), BA (hex)
- RESERVED — Keycode 127 (dec), 7F (hex)

ALL UPS – indicates to the system module that a **DOWN/UP MODE** key was just released and no other **DOWN/UP** keys are depressed.

METRONOME CODE – indicates to the system module that an interval has passed, a keyclick has been generated, and the last key received by the system module is still depressed.

OUTPUT ERROR – indicates an output buffer overflow to the system module. The overflow occurred after receiving a Keyboard Inhibit command from the system module and some keystrokes may be lost.

INPUT ERROR CODE – indicates to the system module that the keyboard received a meaningless command, too many, or too few parameters.

KEYBOARD LOCKED CONFIRMATION – indicates to the system module that the keyboard received an Inhibit Transmission command (Section 6.5.5.3).

TEST MODE ACKNOWLEDGE – indicates that the keyboard has entered test mode. This is a special mode used during the production test. If the system module receives this acknowledge, it sends 80 hex. This terminates the test mode and jumps to power up.

PREFIX TO KEYS DOWN – indicates that the next byte is a keycode for a key already down in a division which has been changed to DOWN/UP (Section 6.5.5.4).

MODE CHANGE ACKNOWLEDGE – indicates that the keyboard has received and processed a mode change command (Section 6.5.5.4).

RESERVED – Keycode 7F is reserved for internal use.

The following four special codes are below 64_{10} value range.

- KEYBOARD ID – FIRMWARE — Keycode 01 (dec), 01 (hex)
- KEYBOARD ID – HARDWARE — Keycode 00 (dec), 00 (hex)
- KEY DOWN ON POWER UP ERROR CODE — Keycode 61 (dec), 3D (hex)
- POWER UP SELF-TEST ERROR CODE — Keycode 62 (dec), 3E (hex)

KEYBOARD ID – This is a two byte identification code, transmitted after the power-up self-test (Section 6.5.4.3). It is also sent on request from the system module (Section 6.5.5.3).

KEY DOWN ON POWER UP ERROR CODE – indicates that a key was depressed on power up.

POWER UP SELF-TEST ERROR CODE – indicates to the system module that the ROM or RAM self-test of the system module failed (Section 6.5.4.3).

6.5.4.3 Power Up Transmission – Upon power up, the keyboard performs a self-test in less than 70 ms. It transmits the self-test results to the system module in 4 bytes.

Byte 1: KBID (firmware) – This is the keyboard identification (ID) that is stored in the firmware

Byte 2: KBID (hardware) – This is the keyboard ID that is read from hardware jumpers

Byte 3: ERROR – Two error codes indicate either failure of the ROM or RAM self-test within the processor (3E hex), or keydown on power up (3D hex). No error is indicated by 00.

Byte 4: KEYCODE – This byte contains the first keycode detected if there was a key down on power up. No error is indicated by 00.

If the ROM self-test (CHECKSUM) fails and the error is critical, the keyboard is unable to transmit. Non-critical errors permit the keyboard to continue operation.

If the keyboard finds a key down on the first scan, it continues to look for an ALL UP condition. The keyboard sends the corrected 4-byte power-up sequence when the depressed key is released. This avoids a fatal error condition if a key is pressed by mistake while powering up.

The keyboard LEDs are lit during the power-up self-test. If the self-test passes, the keyboard turns the LEDs off. If a bell is selected on power up, the system module can transmit a Sound Bell command to the keyboard. However, this should not be done until the system module receives the last byte of the 4-byte sequence. The request for self-test tests the serial line and system module connection. The power-up self-test takes 70 ms or less.

The system module can request a jump to power up at any time. This causes the LEDs on the keyboard to blink on and off (for the power-up self-test).

6.5.5 System Module to Keyboard Protocol

The system module controls both the peripherals associated with the keyboard and the keyboard transmit characteristics. Figure 6-11 shows the protocol for the transmission of commands and parameters from the system module to the keyboard.

6.5.5.1 Commands – There are two kinds of commands – those that control keyboard transmission characteristics and those that control keyboard peripherals. The low bit of the command is the TYPE flag. It is clear if the command is a Transmission command. It is set if the command is a Peripheral command.

Transmission Commands	**Peripheral Commands**
Mode set	Flow control
Autorepeat rate set	Indicator
	Audio
	Keyboard ID
	Reinitiate keyboard
	Some autorepeat control
	Jump to test mode
	Reinstate defaults

ERROR - RIGHT COLUMN INDENT REQUESTED - ILLEGAL IN STYLE 0
The high order bit of every command is the PARAMS flag. If there are any parameters to follow, this flag is clear. If there are no parameters, this flag is set.

6.5.5.2 Parameters – The high order bit of every parameter is the PARAMS flag. It is clear if there are parameters to follow. It is set on the last parameter. The remaining seven bits of the parameter are for data.

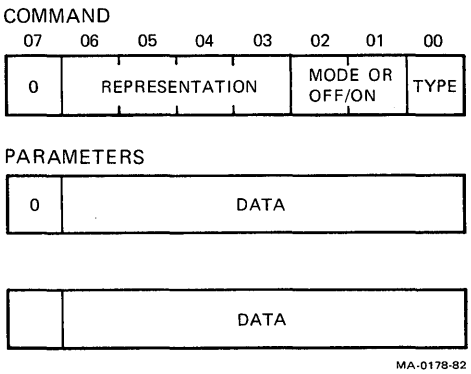


Figure 6-11 System Module to Keyboard Protocol

6.5.5.3 Peripheral Commands – Two commands can turn the data flow from the keyboard off and on.

- **Inhibit Keyboard Transmission** – This command shuts off or locks the keyboard and turns on the Keyboard Locked LED. After receiving the Inhibit command, the keyboard sends a special command to the system central processor. If the system central processor receives this code without requesting it, this indicates that noise on the line was interpreted as the inhibit command. The central processor then responds immediately with the Resume Keyboard Transmission command.

- **Resume Keyboard Transmission** – This command turns on or unlocks the keyboard and turns off the Keyboard Locked LED. If any keystrokes are lost, the keyboard responds with an error code.

Each keyboard LED can be turned on and off.

The following are the eight commands that control the keyclick and bell sounds.

- Disable Keyclick
- Enable Keyclick and Set Volume
- Disable CNTL Keyclick
- Enable CNTL Keyclick
- Sound Keyclick
- Disable Bell
- Enable Bell and Set Volume
- Sound Bell

The following four commands are related to the control of the autorepeat mode.

- **Temporary Autorepeat Inhibit** – Autorepeat is stopped for a specific key only. It resumes automatically when another key is depressed.

- **Enable Autorepeat Across the Board** – Starts transmission of metronome codes without affecting autorepeat timing or keyboard division.

- **Disable Autorepeat Across the Board** – Stops transmission of metronome codes without affecting autorepeat timing or keyboard division.

- **Change All Autorepeat to Down Only** – Changes all keyboard autorepeating divisions to down only mode.

The following are three other miscellaneous commands.

- **Request Keyboard ID** – The keyboard sends the two byte ID (firmware and hardware). The keyboard does not jump to the power-up sequence.

- **Reinitiate Keyboard** – The keyboard jumps to the power-up sequence. Transmission to the keyboard should be held until the host processor receives the last byte of the power-up self-test.

- **Reinstate Defaults** – Sets the following functions back to the default settings after a successful completion of the power-up self-test.

  Division mode settings
  Autorepeat interval and timeout rates
  Autorepeat buffer selections
  Audio volume
  Control key keyclick

To send a peripheral command, set the TYPE flag (low order bit). Bits 6–3 contain a COMMAND representation from the chart below. Bits 2 and 1 specify on (01), off (00), or sound (11). Bit 7 should be set if there are no parameters to follow.

See Table 6-4 for the peripheral commands (in hex).

Command	**Representation**
Flow Control	0001
Indicator (LEDs)	0010
Keyclick	0011
Bell	0100
Keyboard ID	0101
Keyclick For CNTL Key	0111
Temporarily Inhibit Autorepeat	1000
Jump to Test Mode	1001
Change All Autorepeat Characters To Down Only	1010
Enable/Disable Autorepeat	1100

The Jump To Power-Up command is FD hex.

The following are some of the peripheral commands.

- **Flow Control** – The system module can lock the keyboard with the Inhibit Keyboard Transmission command. When the keyboard is unlocked, it responds with an error code if any keystrokes were missed (Section 6.5.6.2).

- **Indicators (LEDs)** – Figure 6-12 shows the LED parameter.
  Figure 6-13 shows the LED layout on the LK201 keyboard.

- **Audio** – Figure 6-14 shows the audio volume parameter.

Table 6-4 Peripheral Commands in Hex

Function	Hex	Parameters
Flow control		
Resume keyboard transmission	8B	None
Inhibit keyboard transmission	89	None
Indicators		
Light LEDs	13	Bit pattern
Turn off LEDs	11	Bit pattern
Audio		
Disable keyclick	99	None
Enable click, set volume	1B	Volume
Disable CNTL keyclock	B9	None
Enable CNTL keyclick	BB	None
Sound keyclick	9F	None
Disable bell	A1	None
Enable bell, set volume	23	Volume
Sound bell	A7	None
Autorepeat		
Temporary autorepeat inhibit	C1	None
Enable autorepeat across keyboard	E3	None
Disable autorepeat across keyboard	E1	None
Change all autorepeat to down only	D9	None
Other		
Request keyboard ID	AB	None
Jump to power up	FD	None
Jump to test mode	CB	None
Reinstate defaults	D3	None

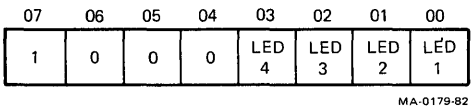


Figure 6-12 Indicator (LED) Parameter

Figure 6-13 Indicator (LED) Layout

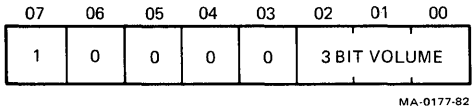


Figure 6-14 Audio Volume Parameter

The volume levels for the audio are as follows.

000 – highest
001
010
011
100
101
110
111 – lowest

Either keyclick or bell (or both) can be disabled. When the keyclick or bell is disabled, it does not sound, even if the system module requests it.

The following are additional peripheral commands.

- **Temporary Autorepeat Inhibit** – Stops autorepeat for this key only. Autorepeat automatically continues when another key is depressed.

- **Disable/enable Autorepeat Across Keyboard** – Stop(s)/start(s) transmission of metronome codes without affecting autorepeat timing or division settings

- **Change All Autorepeat To Down Only** – Changes division settings for all autorepeating divisions to down only

- **Request Keyboard ID** – Keyboard sends a 2-byte keyboard ID. Keyboard does not jump to power up.

- **Reinitiate Keyboard** – Keyboard jumps to its power up routine. The system module should not try to transmit anything to the keyboard until the last byte of the power-up sequence is received.

- **Jump To Test Mode** – Special test mode for production test

- **Reinstate Defaults** – Set the following functions back to the default settings after a successful completion of the power-up self-test.

  Division mode settings
  Autorepeat interval and timeout rates
  Autorepeat buffer selections
  Audio volume
  Control key keyclick

6.5.5.4 Mode Set Commands – The following describe the mode set commands.

- **Division mode settings** – Refer to Section 6.5.2 for an explanation of transmission modes and rates.

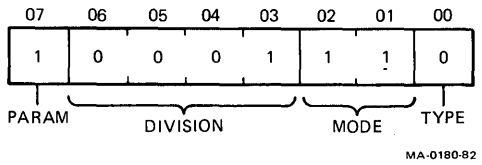
- Each division on the keyboard has a unique 4-bit representation (Section 6.5.1). Table 6-2 describes these representations.

- Each mode has a unique 2-bit code.

Modes	Representation
Down only	00
Autorepeat down	01
Down up	11

To set the key transmission mode on a particular keyboard division, the system module must send the PARAMS flag, then the keyboard division representation with the mode code, and then followed by the TYPE flag (cleared).

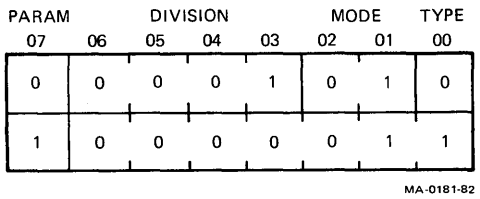
Example: Set main array to down/up



The PARAMS flag is set to 1 if there are no parameters. The PARAMS flag is clear if there are parameters.

Autorepeat Rate Buffer Association – If the autorepeat mode is selected, the system module can transmit a parameter to change the buffer association of the selected division. Refer to Section 6.5.2.3 for autorepeat rates and Section 6.5.7 for default values.

Example: Set main array to autorepeat, change buffer association to buffer 3

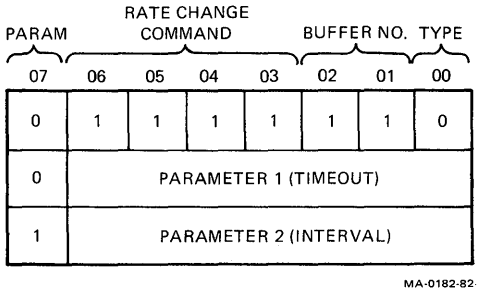


Autorepeat Rate Buffer Values – At keyboard power-up time, the four autorepeat rate buffers contain default values (see Section 6.5.2.3 for autorepeat rates and Section 6.5.7 for defaults). The system module may change these values.

In the command byte, bit 7 (PARAMS flag) should be clear, bits 6–3 are 1111 (to indicate that this is a Rate Set command), bits 2 and 1 should be the buffer number (0 to 3), bit 0 (TYPE flag) is clear.

There should be two parameters carrying the rate set data.

Example: Change rates in buffer 3



The first parameter specifies the timeout to the store in the selected buffer. The second parameter specifies the interval. Refer to Section 6.5.2.1 for definitions of these parameters.

For example, to set the autorepeat rate in buffer 1, the system module firmware transmits 00000011 followed by two bytes of numeric parameters.

The autorepeat timeout is the transmitted number times 5 ms. To specify a rate of 5 ms delay, the first parameter received is 00000001. The maximum allowable time is 630 ms (01111110). The system module must not send 635 (01111111).

NOTE
This code is reserved for internal keyboard use. 00 is an illegal value.

Autorepeat timeout is implemented as a multiple of 8.33 ms, the keyboard's internal scan rate. Timeout rates can vary ± 4.15 ms.

The Autorepeat Interval is the number of metronome codes per second. In order to specify a speed of 16 Hz, the second parameter received is 10010000. Note that the high order bit is set because it is the last parameter. The highest value which may be sent is 124 (11111100).

The lowest rate which can be implemented by the keyboard is 12 Hz. Values as low as 1 can be transmitted, but are translated to 12 Hz.

NOTE
The system module must not send 125 – or 11111101. This code is the Powerup command.

6.5.6 Special Considerations

The following paragraphs describe the special codes and their considerations.

6.5.6.1 Error Handling – There are four error codes. The first two are sent at power up if the self-test fails (Section 6.5.4.3). The other two codes are the INPUT ERROR code and the OUTPUT ERROR code.

The OUTPUT ERROR (B5 hex) is sent after the keyboard receives a Resume Transmission command, if the output buffer overflowed while the keyboard was locked.

The INPUT ERROR (B6 hex) is sent when the keyboard detects noise (unidentified command or parameter) on the line. B6 is also sent if the keyboard detects a delay of more than 100 ms when expecting a parameter.

6.5.6.2 Keyboard Locked Condition – When the keyboard receives an Inhibit Transmission command, it lights the LOCKED LED and transmits one more byte. This is a special code indicating that the keyboard is locked (KEYBOARD LOCKED ACKNOWLEDGE). If the system module receives this code without a request, it indicates that noise on the line was interpreted as an Inhibit Transmission command. The system module should immediately send the Resume Transmission command to unlock the keyboard.

The output first in first out (FIFO) buffer in RAM is four bytes. When the keyboard is locked it attempts to store characters received from the keyboard. The keyboard stops scanning its matrix. When the keyboard is unlocked by the system module, it transmits all four bytes in the output buffer. If any keystrokes have been missed due to buffer overflow, the keyboard transmits an error code as the fifth byte (OUTPUT ERROR). Any keys which were not transmitted and are being held down when the keyboard is unlocked are processed as new keys. An error code upon unlocking the keyboard indicates a possible loss of keystrokes to the system module.

The keyboard stops scanning its matrix when its buffer is full. However, it processes all incoming commands.

6.5.6.3 Reserved Code – The number 7F (hex) is reserved for the internal keyboard input and output buffers handling routines.

6.5.6.4 Test Mode – The keyboard jumps into a test mode by command during production test. It transmits a special code to the system module to confirm the test mode. If the system module receives this code, it should send the byte 80 (hex) to continue. This causes a jump to power-up.

6.5.6.5 Future Expansion – Some keycodes are reserved for future use as special codes or keycodes. Table 6-5 lists these reserved codes.

6.5.7 Default Conditions

- Certain keyboard divisions have specific default modes. Some divisions default to the autorepeat mode; therefore, they have an associated buffer that contains the default values for timeout and interval. Timeout is the amount of time that the keyboard waits before starting to autorepeat a character. The rate of autorepeating a character is called the interval. Table 6-5 shows the default modes and Table 6-6 shows the default rates in the four keyboard division autorepeat rate buffers.

- The volume level for the keyclick and bell has an eight step range. The default volume level for the keyclick and bell is the third loudest.

- For the LK201 keyboard, the **CNTRL** (control) key defaults to the no keyclick state.

6.5.7.1 Audio Volume – Both keyclick and bell volumes are 2 decimal (010 binary) by default. The key in position C99 of the keyboard (the **CNTL** key in the LK201) does not generate a click unless enabled by the system module. The keys in position B99 and B11 (**SHIFT** keys on the LK201) never generate a keyclick.

Table 6-5 Keyboard Division Default Modes

Keyboard Division	Mode	AR Buffer
Main array	autorepeat	0
Keypad	autorepeat	0
Delete	autorepeat	1
Cursor keys	autorepeat	1
Return and Tab	down only	
Lock and Compose	down only	
Shift and Control	down/up	
Six basic editing keys	down/up	

Table 6-6 Default Rates in Autorepeat Buffers

Buffer No.	Timeout (ms)	Internal (Hz)
0	500	30
1	300	30
2	500	40
3	300	40

6.6 SPECIFICATIONS

Functional

Electronics	8-bit microprocessor, 4 kilobytes of ROM 256 bytes of RAM, 4 LEDs, transducer
Cord	1.9 m (6 ft), coiled, 4-pin telephone-type modular connectors, plugs into display monitor (PN BCC01)
Keypad	Sculptured key array
Home row key height	30 mm above desk top
Keys	105 matte textured-finish keys
Main keypad	57 keys
Numeric keypad	18 keys
Special function keypad	20 keys; firmware and software driven
Editing keypad	10 keys
Spacing	1.9 cm (0.75 in) center to center (single width keys)
Wobble	Less than 0.5 cm (0.020 in)
Diagnostics	Power-up self-test, generates identification upon passing test

Physical

Height	5 cm (2.0 in) at highest point
Length	53.3 cm (21 in)
Width	17.1 cm (6.75 in)
Weight	2 Kg (4.5 lb)

CHAPTER 7
BIT MAP VIDEO CONTROLLER AND EXTENDED BIT MAP MODULES

7.1 INTRODUCTION

The bit map video controller and extended bit map are the display control components of the video subsystem for the Professional 350 system. Figure 7-1 shows the bit map video controller and extended bit map modules relationship to the other components which make up the Professional 350 system.

7.1.1 Related Documentation

Refer to the following related documentation while reading this chapter.

Title	Document No.
VC241 Extended Bit Option Field Maintenance Print Set	MP-01471-00

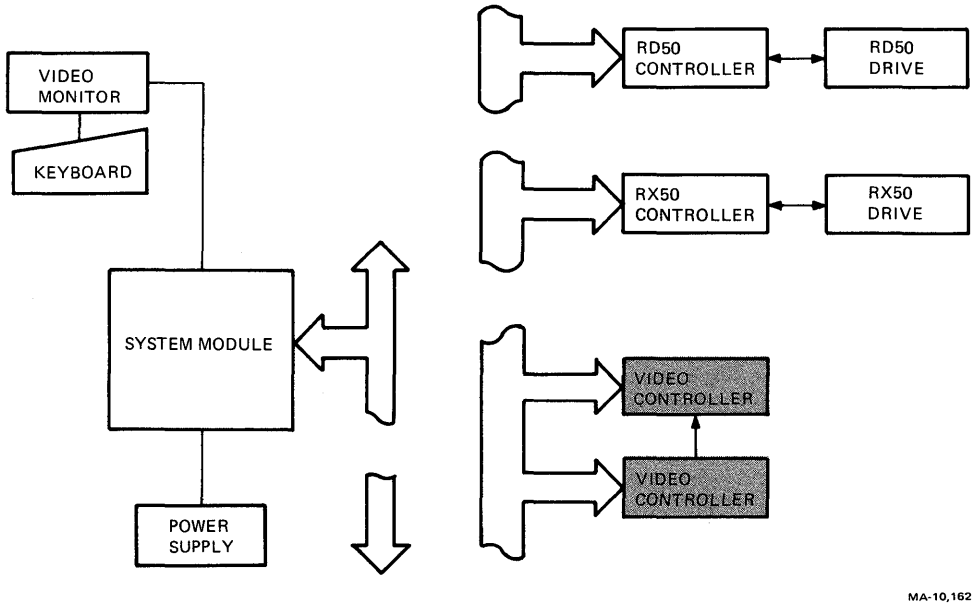


Figure 7-1 System Block Diagram

7.1.2 General Information

The bit map video controller and extended bit map modules generate video drive signals for a monochrome or color monitor (Figure 7-2). Both modules are 5.2 × 12-inch field replaceable units (FRU). The bit map video controller (FRU PN 54-15138) occupies one slot of the CTI BUS option space in the Professional 350 card cage. This module is a required component for a video subsystem of the Professional 350 system. The extended bit map (FRU PN 54-15146) occupies the slot on the CTI BUS following the bit map video controller.

The extended bit map module is optional for a video subsystem that supports only monochrome monitors. For this application, the module provides two additional planes of video display storage.

The extended bit map module is required for a video subsystem that supports both color and monochrome monitors. For a color monitor the module supplies data storage and video generation for green and red video signals (nonmapped mode) or data storage and color mapped video generation.

A zero insertion force (ZIF) connector (J1) at the bottom of each module makes the module compatible to the CTI BUS. This connector allows the host processor to control the operations of the controller from the CTI BUS.

One cable (PN 17-00303) connects the bit map video controller module to the extended bit map module, at connectors (J2) at the top of each module. The bit map video controller is the master of the extended bit map. It directs the operations of the extended bit map performs via signals passed over this cable. Each module can be accessed directly. For data transfers between the host processor and the extended bit map, the host processor accesses the bit map video controller to control receiving or sending data over the CTI BUS to the extended bit map.

Refer to Chapter 5 for the connector description and signal definitions for J1. Refer to Section 11.4 for the connector descriptions and signal definitions for J2.

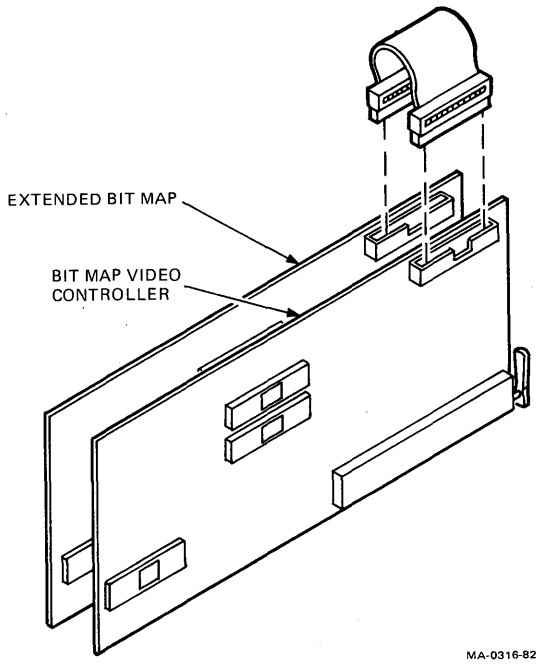


Figure 7-2 Bit Map Video Controller and Extended Bit Map Modules

7.2 FUNCTIONAL COMPONENTS

The following sections describe the functional components of the bit map video controller and the extended bit map modules of the Professional 350 system.

7.2.1 Bit Map Video Controller Circuit Components

To the host processor, the bit map video controller appears as a set of registers and 16K words (32K bytes) of video memory that is accessible from the CTI BUS. The host processor reads and writes to the registers to issue video memory data modification commands to the controller and to select video display characteristics. The host processor directly accesses the video memory (16K word video bit maps) for read-modify-write operations. Refer to the register definitions in Section 11.5 for more information.

Data transfers between the video memory and the host processor are program controlled by the host processor. Under this program, the host processor reads and writes to the video memory on the bit map video controller. The video memory appears as a 16K word (32K byte) page in the host processor address space. The controller sequentially reads the video memory and converts the data to a video drive signal. This signal contains the necessary vertical and horizontal synchronization pulses and equalization pulses to drive a display monitor.

The bit map video controller module contains one bit map (video memory) to provide one plane of displayable data. This plane is displayed in one of three register-selectable horizontal resolution modes: 1024, 512, and 256 pixel resolution. In the 1024 pixel resolution mode, each bit in memory controls one screen pixel; the pixel can be on or off. In the 512 pixel resolution mode, two memory bits control each screen pixel; the pixels are twice as big as in the 1024 pixel mode and have one of four intensity levels. In the 256 pixel resolution mode, four memory bits control one screen pixel; the pixels are four times as big as in the 1024 pixel mode and have one of 16 intensity levels.

Figure 7-3 is a simple block diagram of the bit map video controller module. This module contains circuits that access commands and controls the data flow on the bit map video controller and the extended bit map modules. These circuits are the video memory control circuits, CTI BUS to memory access circuits and register access control circuits.

The bit map video controller consists of the following circuits (Figure 7-3).

- CTI BUS interface
- CTI BUS register access
- Registers
- CTI BUS video memory access
- Video memory control and update
- Video memory
- Clock generator
- Video generator

7.2.1.1 CTI BUS Interface Circuits – The host processor gains access to the video subsystem through these circuits by reading and writing to the bit map video controller and extended bit map registers and video memories. For the host processor to access video subsystem, the CTI BUS interface circuits perform the following functions.

- Acknowledge accesses to the bit map video controller or the extended bit map registers and video memories by the host processor.
- Pass data between the host processor and Bit Map Video Controller registers and video memory.
- Pass interrupts to the host processsor to indicate vertical retrace and the completion of a command.

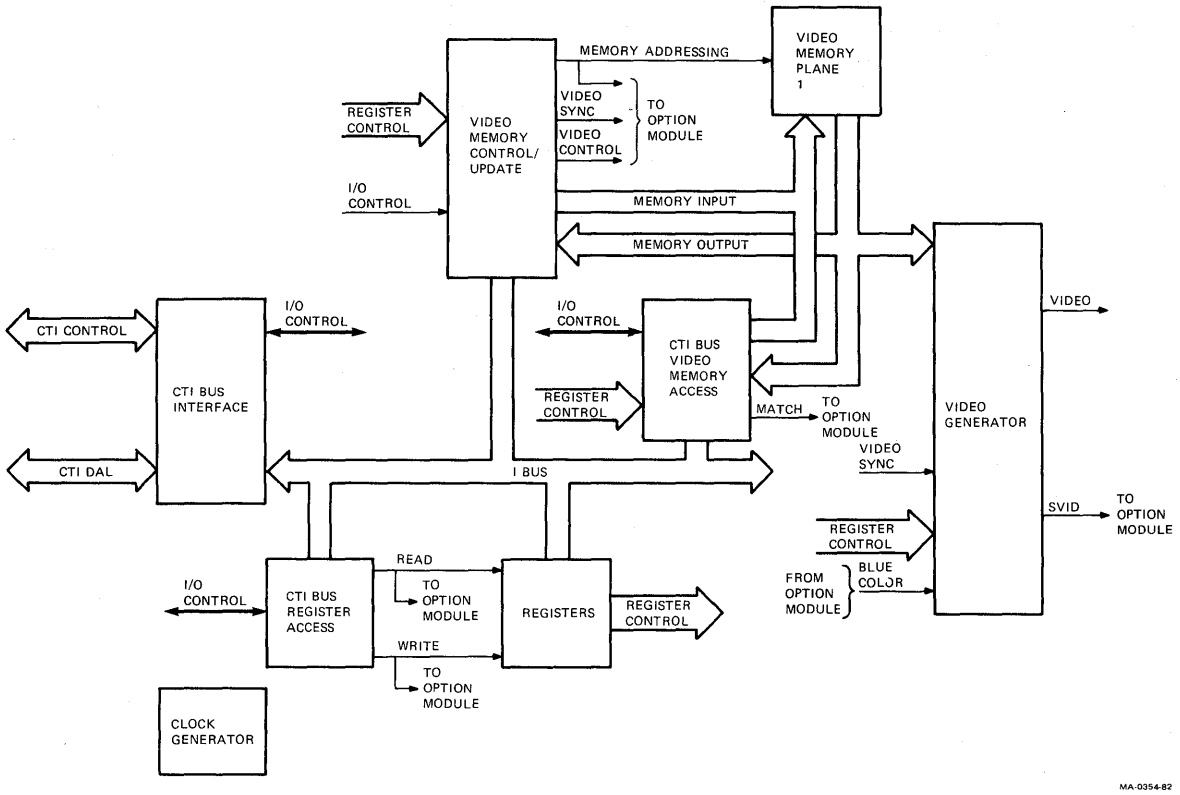


Figure 7-3 Bit Map Video Controller Block Diagram

7.2.1.2 CTI BUS Register Access Circuits – When the host processor accesses a register in the bit map video controller or the extended bit map, the CTI BUS interface circuits pass the address and I/O control signals to the CTI BUS register access circuits. These circuits decode the address and I/O control signals to generate register read and write signals for registers on the bit map video controller and the extended bit map modules.

7.2.1.3 Registers – The bit map video controller contains nine registers which can be read or written to by the host processor. Access to these registers allows the host processor to control the bit map video controller and the extended bit map modules and access status data. These registers provide register control signals for the video memory control/update circuits, video generator, and the extended bit map. Refer to Section 7.5 for detailed information on each register.

7.2.1.4 CTI BUS Video Memory Access – The bit map video controller contains one bit map memory plane (video memory). The host processor can read or write to this memory through the CTI BUS interface circuits and the CTI BUS video memory access circuits. For the host processor to access the video memory, these circuits perform the following operations.

- Determines if an address on the CTI BUS from the host processor is in the video memory address page.
- Passes data between the video memory and the CTI BUS interface circuits for the host processor.

7.2.1.5 Video Memory Control and Update Circuits – These circuits synchronize the bit map video controller and the extended bit map modules operations. During most operations the video memory is accessed. These circuits control read-modify-write operations and read only accesses to the video memory. The read-modify-write operations occur during host processor accesses and video memory update modification operations to the video memory. The read only operations sequentially pass the video memory data to the video generator to refresh the screen.

To perform these operations, the video memory control and update circuits perform the following operations.

- Generate video memory addresses for read-modify-write and read only operations.
- Generate video sync signals for the video generator.
- Perform logical operations on data stored in the bit map video controller video memory.
- Pass video timing and video memory address signals to the extended bit map module.

7.2.1.6 Video Memory – The video memory is a 16K by 16-bit word memory and is addressed by the video memory control and update circuits. During read-modify-write cycles, addressed data passes between the video memory, the video memory control and update circuits, and the CTI BUS video memory access curcuits. During read only cycles, sequentialy addressed data passes from the video memory to the video generator circuits.

This memory is mapped such that each bit (or group of bits) directly controls a video screen pixel (Figure 7-4). The bit map arrangement provides a greater horizontal resolution than vertical resolution. For vertical resolution, up to 255 lines of data are available, however, the line spacing is fixed. For horizontal resolution, each line is controlled by 1024 bits of information. This allows for the selection of three different pixel lengths and up to 16 different pixel intensities.

7.2.1.7 Video Generator Circuit – The video generator circuit generates a composite video drive signal for a monochrome or color monitor. This signal is generated from data stored in the video memory and video sync signals from the video memory control and update circuits.

The video generator circuit can operate in one of three monochrome resolution modes selected by the register control signals (nonmapped). For mapped operation, the video generator serializes data from the video memory and passes it to the extended bit map module. The extended bit map then returns color map control signals to the video generator. This generates a blue video drive signal and a monochrome video drive signal. The generated video drive signal is passed to the CTI Private BUS and then routed to the connector on the system box.

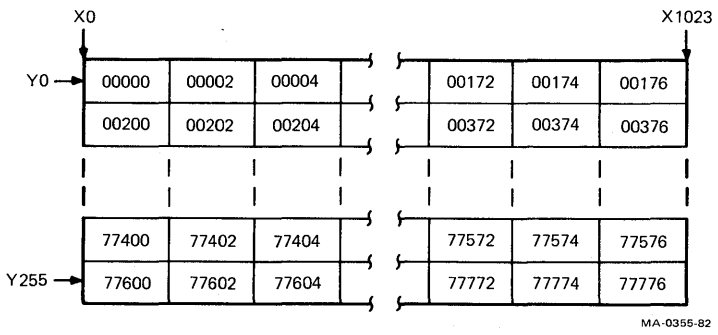


Figure 7-4 Video Memory Bit Map Layout

7.2.2 Extended Bit Map Module Circuit Components

With the exception of the color map register, the circuits on the extended bit map module operate like the circuits on the bit map video controller module. The extended bit map module is optional when the video subsystem supports a monochrome monitor. It provides two additional 16K word video memory planes for the video subsystem. the extended bit map module is required when the video subsystem supports a color monitor.

When the module is used for color video signal generation it can operate in two modes, nonmapped or mapped. For mapped modes, video memory plane 1 on the bit map video controller module contains the display data for generating a primary blue video. The extended bit map Module video memory planes 2 and 3 store data for generating primary green and red video.

When the subsystem operates in the mapped mode, the video memory planes store addresses for an eight word color map register (CMR). The CMR provides data control signals to the three video generators for blue, green, and red signals. The simultaneously addressed video memory planes each provide serial data to the CMR. One bit from each plane provides a 3-bit address to the CMR. The host processor preloads each of the CMR locations with a data word to select one of 256 possible colors.

When a CMR location is addressed by the three data bits formed from each of the three planes, color map signals are sent to each video generator. These signals control each video generator to set the intensity level for each primary color pixel in a color cluster to show one of eight colors.

For monochrome monitors, all three video memory planes operate in either mapped or nonmapped modes. Refer to Section 7.2.1 for the resolution modes the video memory planes can operate in while the subsystem is in nonmapped operation. Each plane can also be turned on or off under program control. This allows for any combination of displayed planes.

Figure 7-5 is a simple block diagram of the extended bit map module circuit. This module requires control, timing, and video memory addressing signals from the bit map video controller module to perform its operations. When this module is accessed directly by the host processor, it returns an identification byte to the host processor. Host processor accesses to the bit map video controller module provide accesses to the extended bit map module's registers and its video memory planes.

The extended bit map module contains the following circuits.

- CTI BUS interface
- Plane and color map registers
- Two CTI BUS video memory access circuits
- Two video memory update circuits
- Two video memories
- Two video generator circuits

7.2.2.1 CTI BUS Interface Circuit – The CTI BUS interface circuits can be accessed in two modes, direct and indirect host processor accesses. For direct host processor accesses to the extended bit map modules register address space, these circuits place a module identification code on the CTI BUS. For an indirect access to the extended bit map module, the host processor accesses the bit map video controller module which generates control signals for the CTI BUS interface circuit. These control signals enable the circuits to pass I/O control signals and data between the CTI BUS and the module's internal bus.

7.2.2.2 Plane and Color Map Registers – The bit map video controller module enables these registers for writing and reading. Data is passed between the registers and the CTI BUS through the CTI BUS interface circuits. The plane register allows the host processor to control each planes resolution and update modification mode, and enables each plane for operation. The color map register selects eight displayable colors during the video subsystems mapped operation.

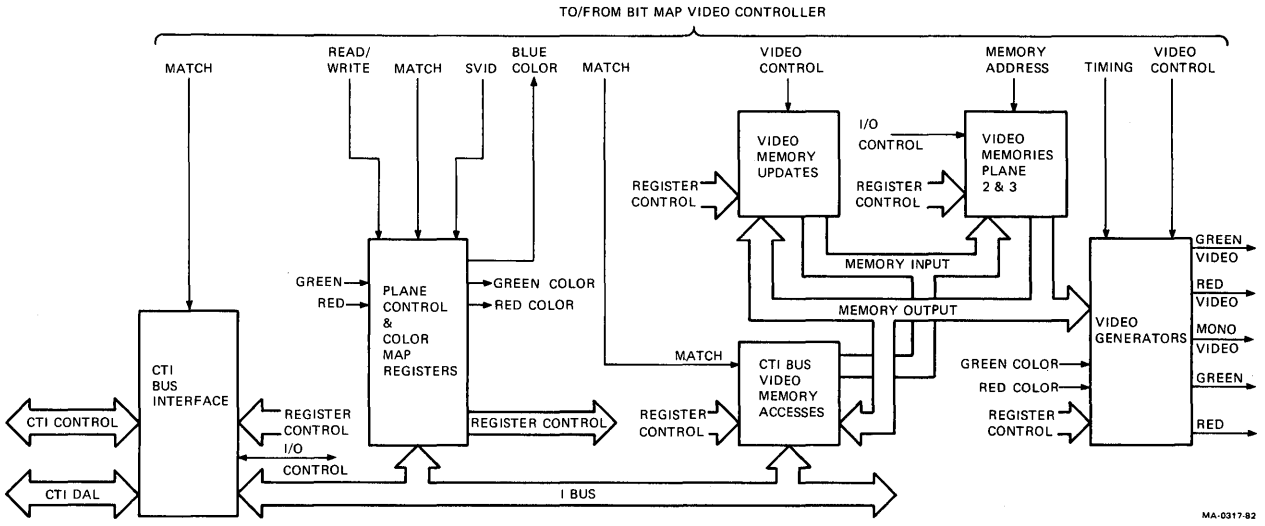


Figure 7-5 Extended Bit Map Block Diagram

7.2.2.3 CTI BUS to Video Memory Access Circuits – The extended bit map contains two CTI BUS video memory access circuits, one for each video memory plane, plane 2 (green plane) and plane 3 (red plane). These circuits are controlled by the bit map video controller and the extended bit map plane 2 and 3 control register. These circuits allow data to pass between these respective video memory and the host processor through the CTI BUS interface circuits.

7.2.2.4 Video Memory Update Circuits – The extended bit map contains two video memory update circuits, one for each video memory plane, plane 2 (green plane) and plane 3 (red plane). These circuits are controlled by the bit map video controller and the extended bit map plane 2 and 3 control register. These circuits allow logical operations to be performed on data stored in there respective video memory plane.

7.2.2.5 Video Memory – The extended bit map contains two video memory planes, plane 2 (green plane) and plane 3 (red plane). Each video memory plane is a 16K by 16-bit word memory plane and is mapped like plane 1 (blue plane) on the bit map video controller (Section 7.2.1.6).

Both video memory planes are addressed by the bit map video controller for read-modify-write and read only cycles. The CTI BUS interface circuits provide additional I/O control signals to the video memories during read-modify-write cycles. The plane 2 and 3 control register provides control signals to select each plane during read-modify-write cycles.

During read-modify-write cycles, addressed data passes between the video memory, the video memory update circuits, and the CTI BUS video memory access circuits. For read only cycles, sequentialy addressed data passes from the video memory to its respective video generator circuits during nonmapped operation, or to the color map during mapped operation.

7.2.2.6 Video Generator – The extended bit map contains two video generator circuits, one for each respective video memory plane, plane 2 (green plane) and plane 3 (red plane). The video generator circuits are controlled by the bit map video controller and the extended bit map plane 2 and 3 control register. Each video generator generates a video signal to drive a monochrome or color monitor. The video signal is generated from data stored in the video memory for nonmapped operations or by the color map for mapped operations. The plane 2 (green) video generator also receives and passes video synchronization signals from the bit map video controller.

For nonmapped operations, each video generator circuit can operate in one of three resolution modes. For mapped operations, each video generator serializes data from its video memory and passes it to the color map register (CMR). The CMR then returns color map control signals to each video generator for controlling its video drive signals generation. Each video drive signal is passed to the CTI Private Bus and routed to the connector on the system box.

7.3 THEORY OF OPERATION

The following section describes the theory of operation of the bit map video controller and the extended bit map modules of the Professional 350 system.

7.3.1 Bit Map Video Controller Detailed Operation

The bit map video controller is a required module for generating composite video signals for the Professional 350 system. To perform this function, the module contains the following circuits.

- CTI BUS interface
- CTI BUS register access
- Registers
- CTI BUS video memory access
- Video memory control and update
- Video memory
- Clock generator
- Video generator

7.3.1.1 CTI BUS Interface Detailed Operation – The CTI BUS interface circuit passes CTI BUS control signals, data, and addresses between the host processor and the bit map video controller (Figure 7-6). To perform this function, this circuit uses the following components.

- CTI BUS control signal buffer
- CTI BUS high byte data address buffer
- CTI BUS data address transceiver
- Transmit decoder

CTI BUS I/O Control Signal Buffering

All control signals passed between the bit map video controller and the CTI BUS are buffered to isolate the current drain of the module from the CTI BUS. Table 7-1 lists the CTI BUS control signals and their functions on the module.

Refer to Chapter 5 for further information on CTI BUS control signal timing sequences.

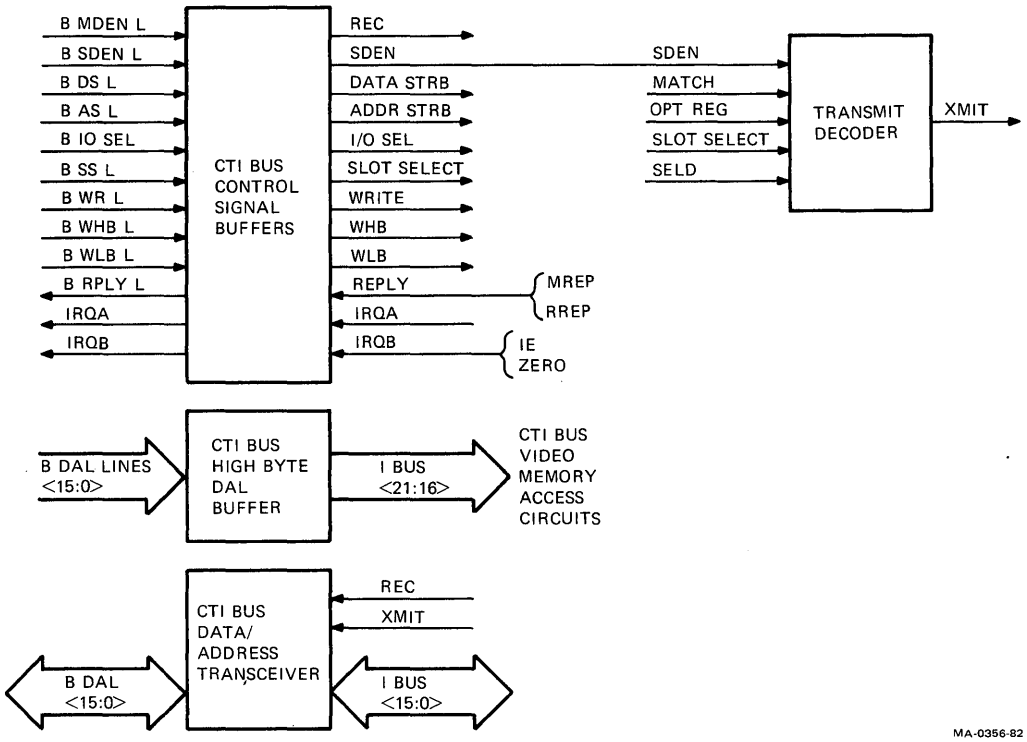


Figure 7-6 CTI BUS Interface Circuit Operation

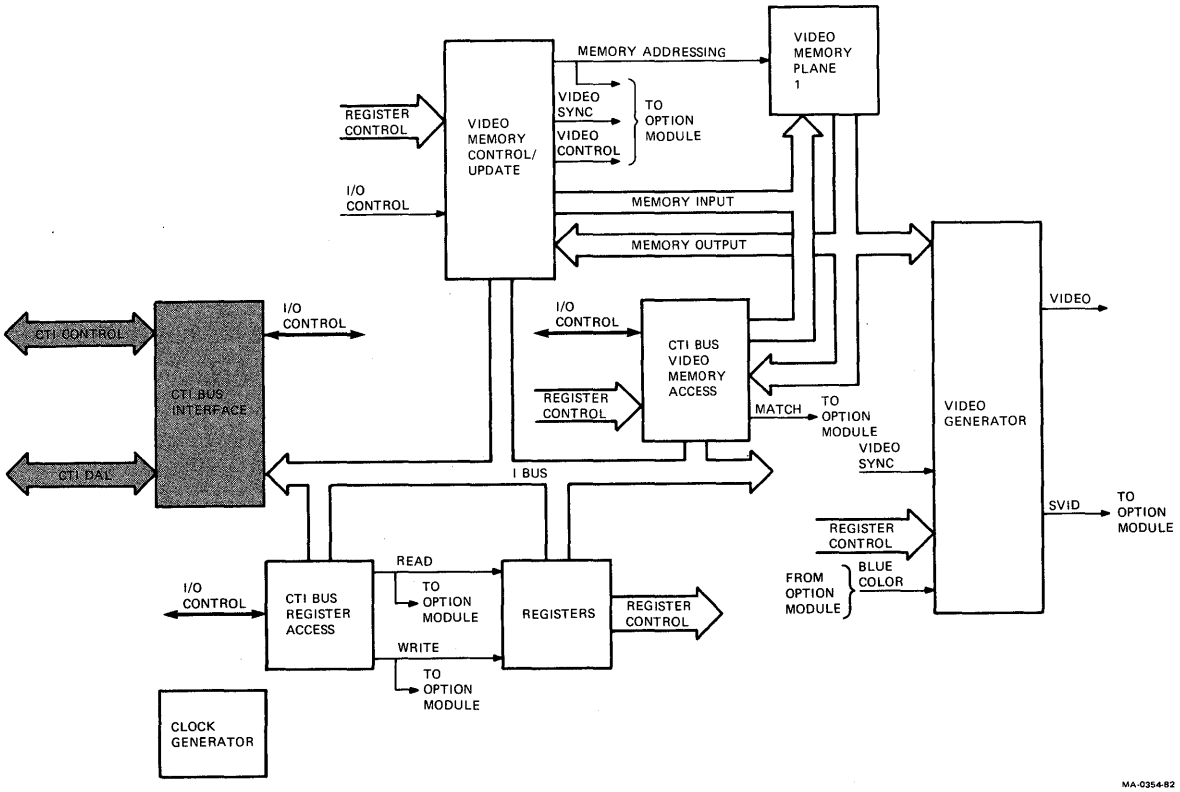


Table 7-1 CTI BUS Control Signal Functions

CTI BUS Signal	Module Signal	Function
B MDEN L	REC	Controls module to accept addresses or data from the CTI BUS.
B SDEN L	SDEN	Enables transmit decoder.
B AS L	ADDR STRB	Enables the module to latch the address on the CTI BUS into the register access control, CTI BUS to video memory access, and video memory control/update circuits.
B DS L	DATA STRB	Enables the module to pass data between its registers or video memory and the CTI BUS.
B IOSEL L	I/O SEL	Enables the CTI BUS to video memory access circuits.
B SS L	SLOT SELECT	Enables host processor access to the modules registers.
B WR L	WRITE	Enables the host processor to write words to the module (accept data from the CTI BUS) or read words from the module (pass data to the CTI BUS).
B WHB L	WHB	Enables the host processor to write high bytes to the module (accept data from the CTI BUS) or read high bytes from the module (pass data to the CTI BUS).
B WLB L	WLB	Enables the host processor to write low bytes to the module (accept data from the CTI BUS) or read low bytes from the module (pass data to the CTI BUS).
B RPLY L	REPLY	An acknowledgement signal from the module to the host processor. It indicates the host processor properly accessed a register or a video memory plane on either the bit map video controller or the extended bit map.
B IRQA L	IRQA	An interrupt signal from the module to the host processor. It indicates the module is performing a verticle retrace.
B IRQB L	IRQB	An interrupt signal from the module to the host processor. It indicates the counter register is empty.

CTI BUS To/From Internal Bus Address and Data
All addresses and data passed between the host processor and the bit map video controller occur over the CTI BUS B DAL lines. A CTI BUS high byte DAL buffer isolates the B DAL <21:16> lines from the modules internal bus, (I BUS <21:16>). These lines are used only during video memory addressing sequences (Section 7.3.1.4). The CTI BUS data/address transceivers isolates the B DAL <15:00> lines from the modules internal bus, (I BUS <15:00>). The receive (REC) signal from the CTI BUS control signal buffers enables these transceivers to pass data or addresses on the CTI BUS to the internal bus. The transmit (XMIT) signal from the transmit decoder enables these transceivers to pass data on the internal bus to the CTI BUS.

The host processor controls the module to receive addresses and data with the CTI BUS signal B MDEN L (REC). When the module transfers data to the CTI BUS, the CTI BUS signal B SDEN L enables a transmit decoder. This decoder generates a transmit signal for the transceiver for two conditions, video memory access or bit map video controller register access.

For video memory accesses, the SDEN signal enables the transmit decoder. The decoder looks for a MATCH and a SELD signal. The MATCH signal, from the CTI BUS to video memory circuit, indicates a host processor access to the video memory Address range. The SELD signal, from the plane 1 control register, indicates that the video memory plane is enabled.

For bit map video controller register access, the transmit decoder is enabled by SDEN, OPT REG, and SLOT SELECT. The XMIT signal is enabled, if the SLOT SELECT signal indicates that the module is selected and the OPT REG signal indicates that the accessed register is on the bit map video controller.

7.3.1.2 CTI BUS Register Access Detailed Operation – The CTI BUS register access circuit decodes register addresses from the host processor and generates register read and write strobes (Figure 7-7). The strobes are generated for registers on the bit map video controller and the extended bit map. To perform this function, this circuit uses the following components.

- Address latch
- Register access decoder

When the CTI BUS interface circuits pass a video subsystem register address to the I BUS, they also pass an ADRS STRB signal to the address latch. Six address bits are loaded into the latch for decoding (I BUS <6:1> to ADDRESS<6:1>). These bits allow access to 64 registers on word boundaries between address 0 and 176 (HEX).

The register access decoder generates register read and write strobes only to existing registers. If a nonexisting register is addressed, the decoder does not generate a read or write strobe. If SLOT SELECT is asserted during a DATA STRB, the decoder generates an RREP register reply (RREP) for the CTI BUS interface circuits. This occurs regardless of the address register.

The CTI BUS I/O control signals from the CTI BUS interface circuit enable and clock the decoder. The generation of a read or write strobe from the decoded address is direct. If REC and SLOT SELECT are asserted during a data strobe, an address of 20 (HEX) with the WRITE, WHB, and WLB unasserted generates an RD20 strobe.

If an extended bit map register is addressed (RD10, WR10, RD12, or WR12), the OPT REG signal is asserted. This disables the CTI BUS interface circuits and enables circuits on the extended bit map module.

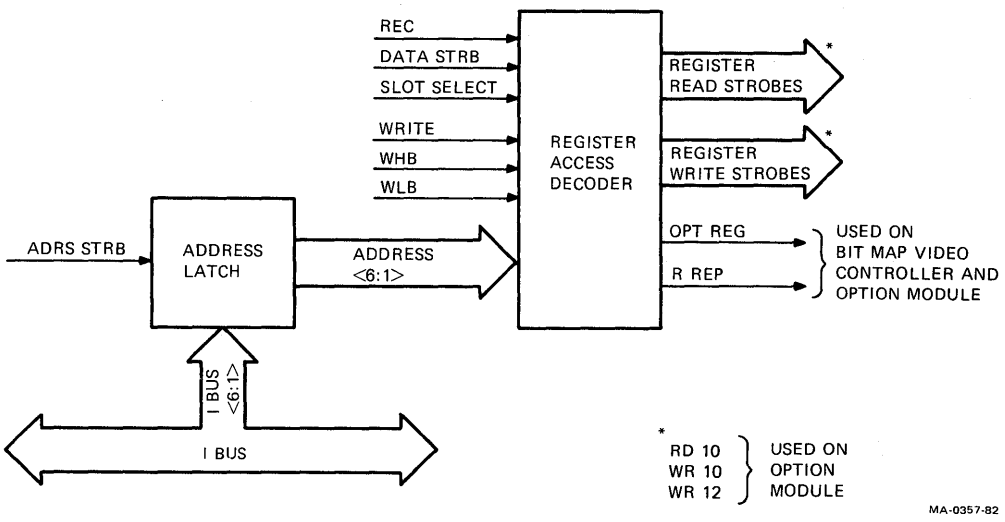
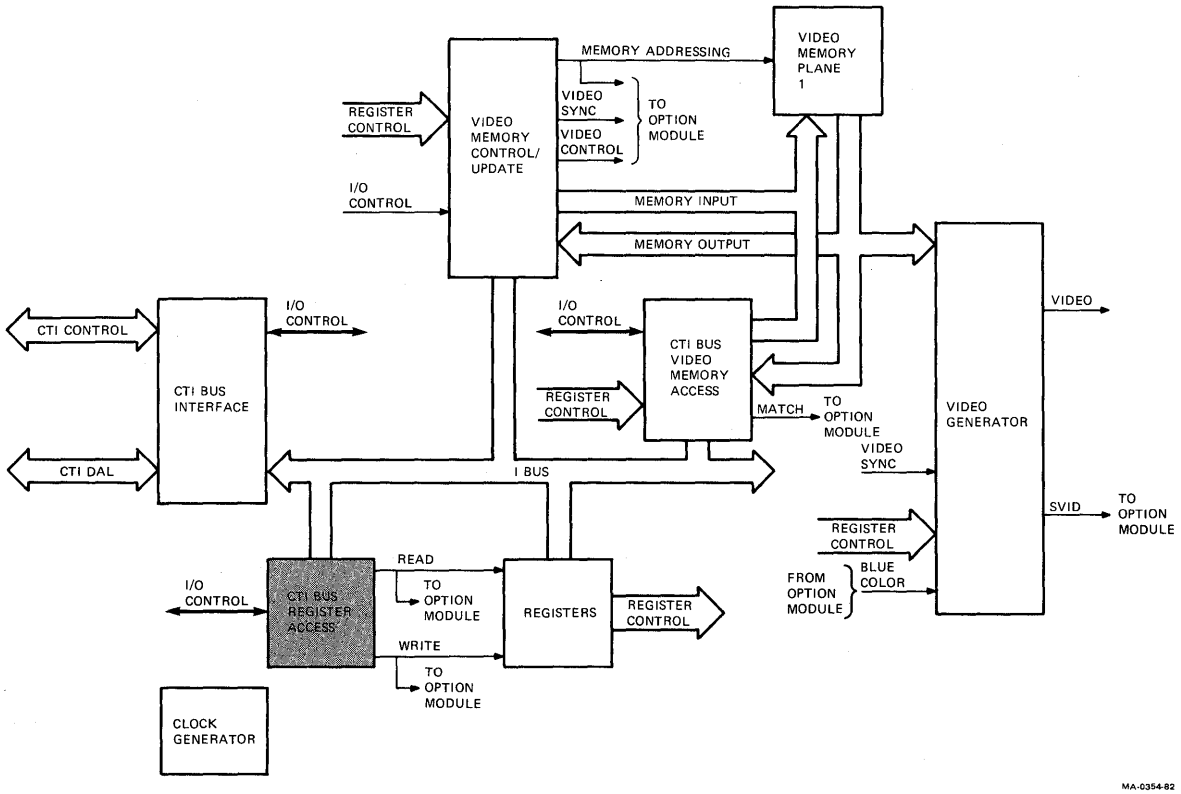


Figure 7-7 CTI BUS Register Access Circuit Operation



7.3.1.3 Registers – The bit map video controller contains nine registers. The host processor uses these registers to identify, control, and acquire status information from the controller. registers are accessed through the CTI BUS register access circuits. Table 7-2 lists the addresses, access, and operation of each register. Figures 7-8 through 7-15 show the operation and location of each register. They also show the control and status signal interfacing the registers to the remaining bit map video controller circuits. Refer to Section 7.5 for further information about the registers.

Table 7-2 Controller Register Access Functions

Address	Access	Operation
XXXXXX00	Read only	Provides the identification code of the bit map video controller to the host processor.
XXXXXX04	R/W	The control and status register of the bit map video controller. It is cleared upon initialization of the module. The low byte of this register is in the video controller chip (DC715), the high byte is a discrete register. The high and low bytes can be written to independently. A read operation provides both high and low byte information.
XXXXXX06	R/W	The plane register which selects the operational mode of the video data chip (DC716) and the video generator on the bit map video controller.
XXXXXX14	R/W	The scroll register contained in the video controller chip (DC715) on the bit map video controller.
XXXXXX16	R/W	The X coordinate register contained in the video processor chip (DC717) used during video memory update operations.
XXXXXX20	R/W	The Y coordinate register contained in the video processor chip (DC717) and used during video memory update operations.
XXXXXX22	Write only	The counter register indicates the number of read-modify-write cycles the host processor performs to the video memory.
XXXXXX24	Write only	The pattern register used as the LSB data during read-modify-write cycles to the video memory. This register must be loaded befor the counter register.
XXXXXX26	Write only	The memory base register sets the 16K page location of the video memory for host processor access.

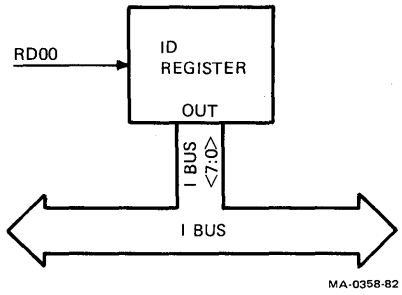
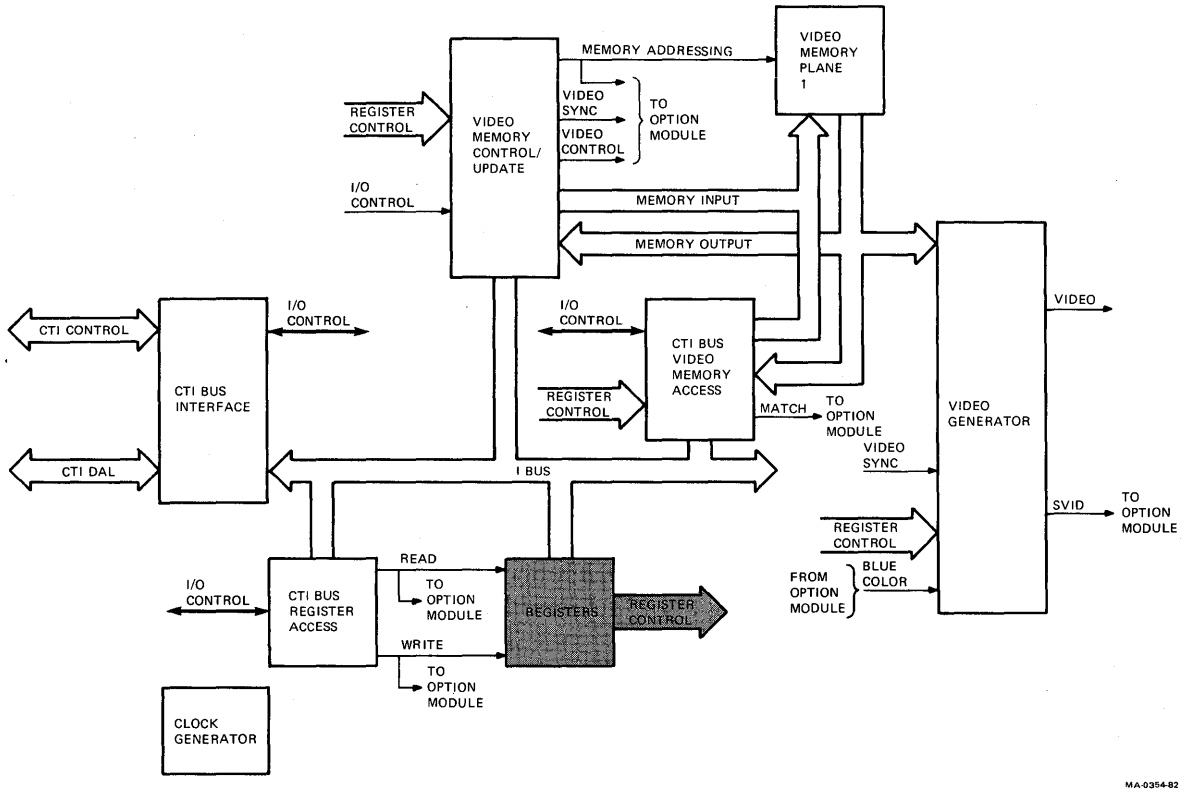


Figure 7-8 ID Register Operation



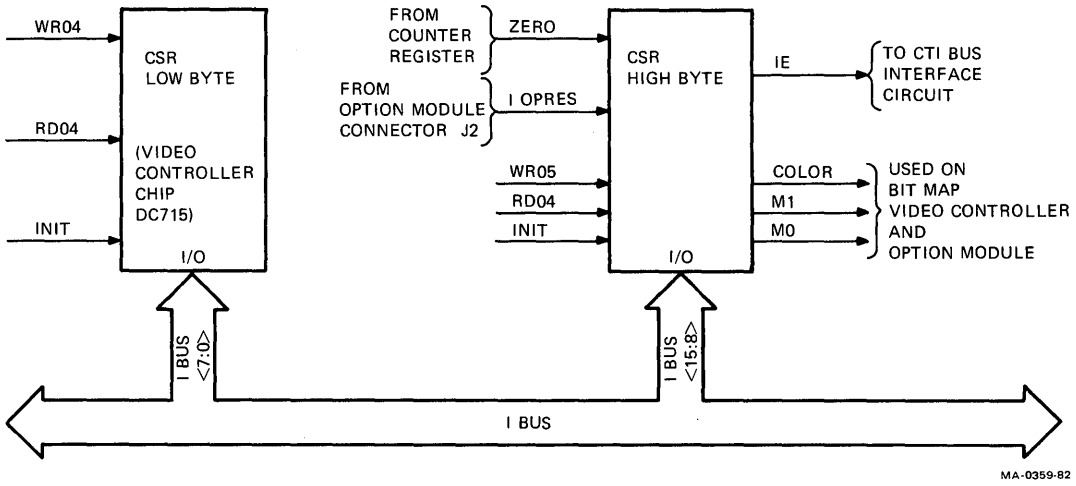
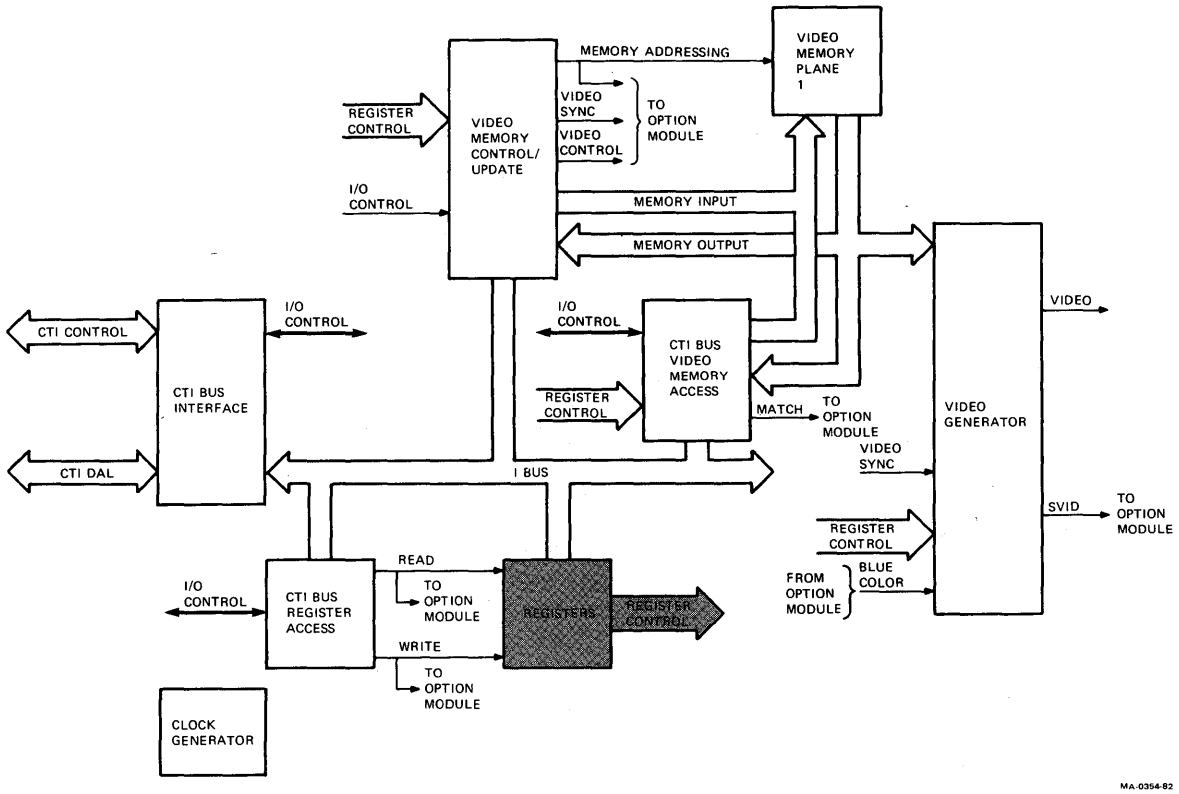


Figure 7-9 CSR Register Operation



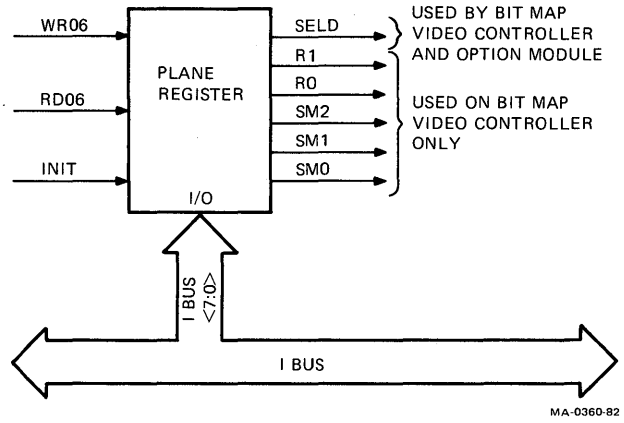
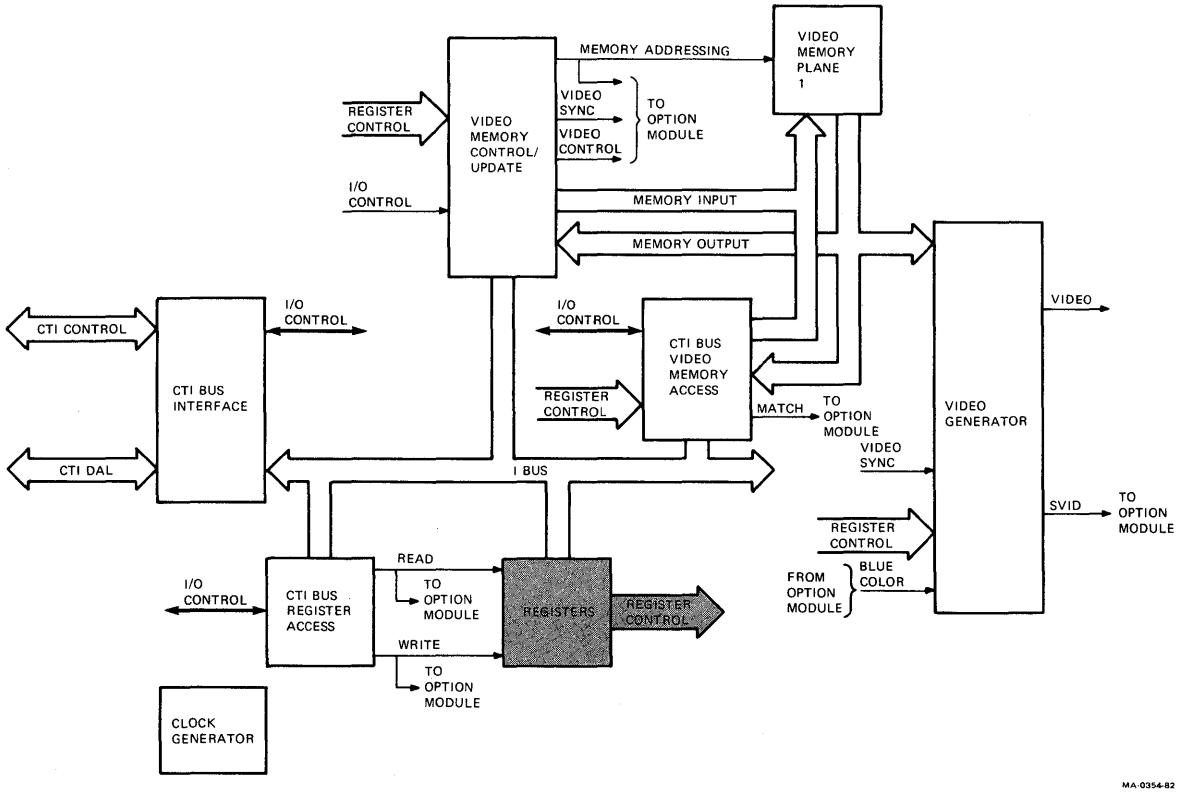


Figure 7-10 Plane Register Operation



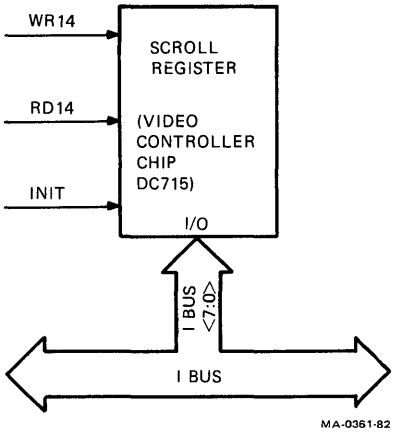
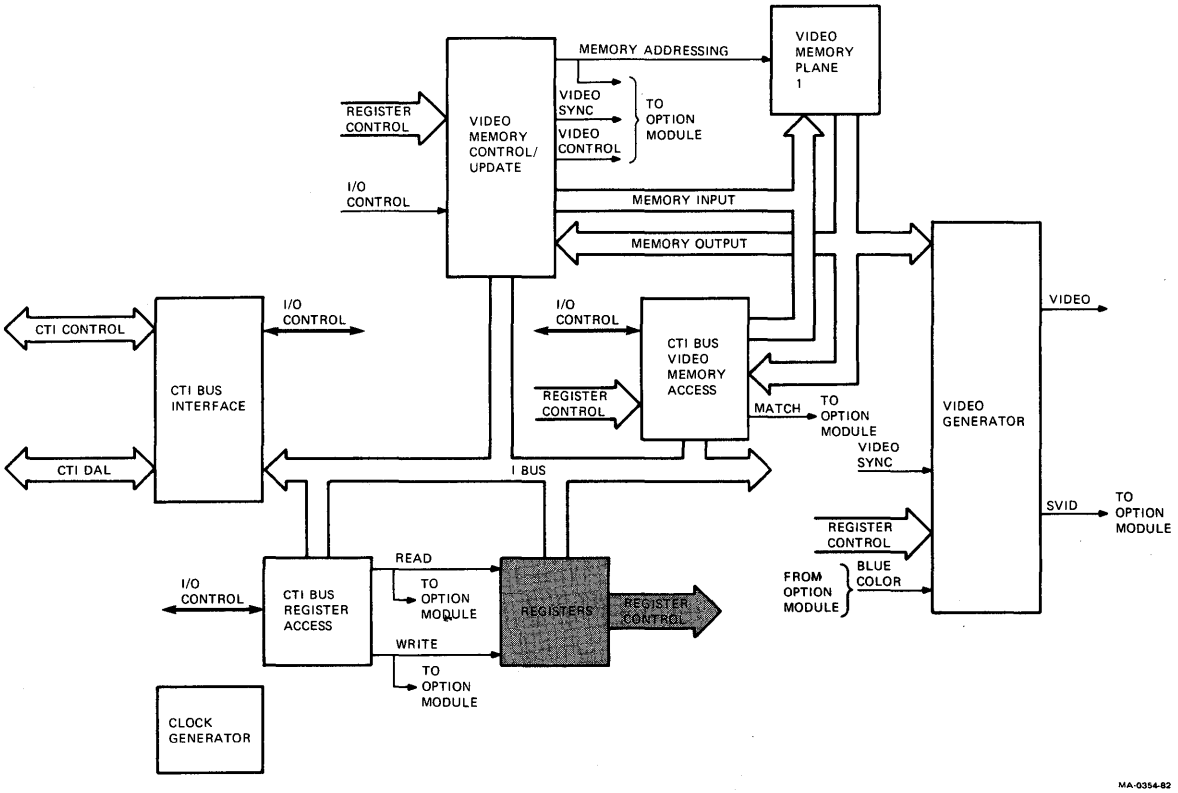


Figure 7-11 Scroll Register Operation



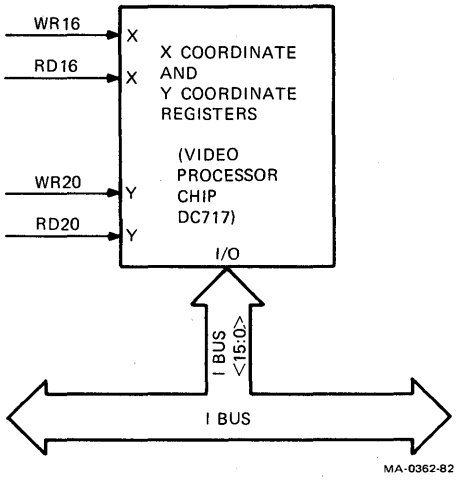
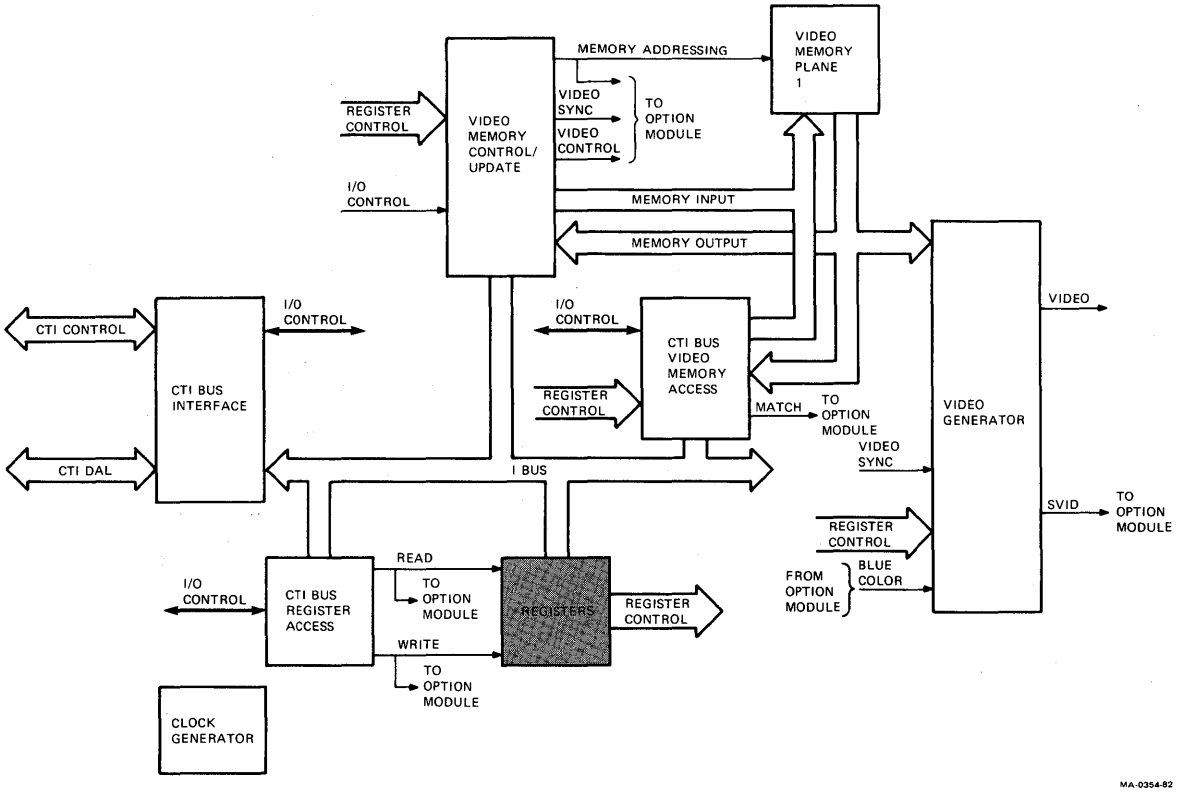


Figure 7-12 X and Y Coordinate Register Operation



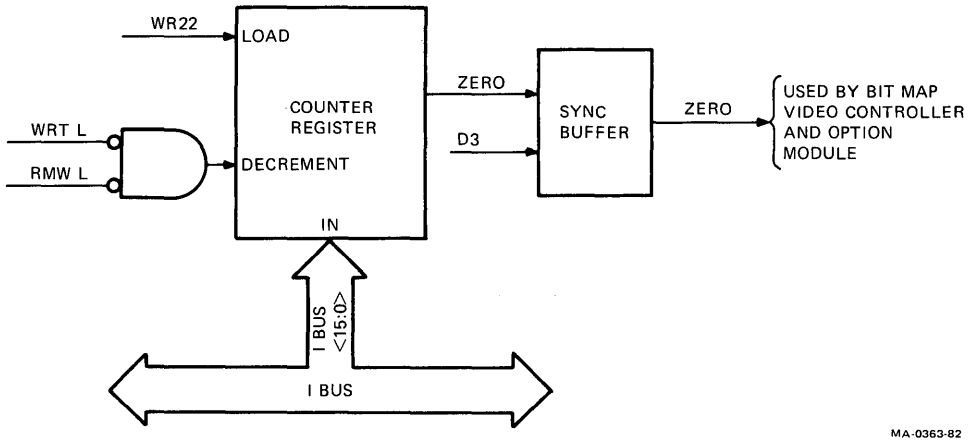
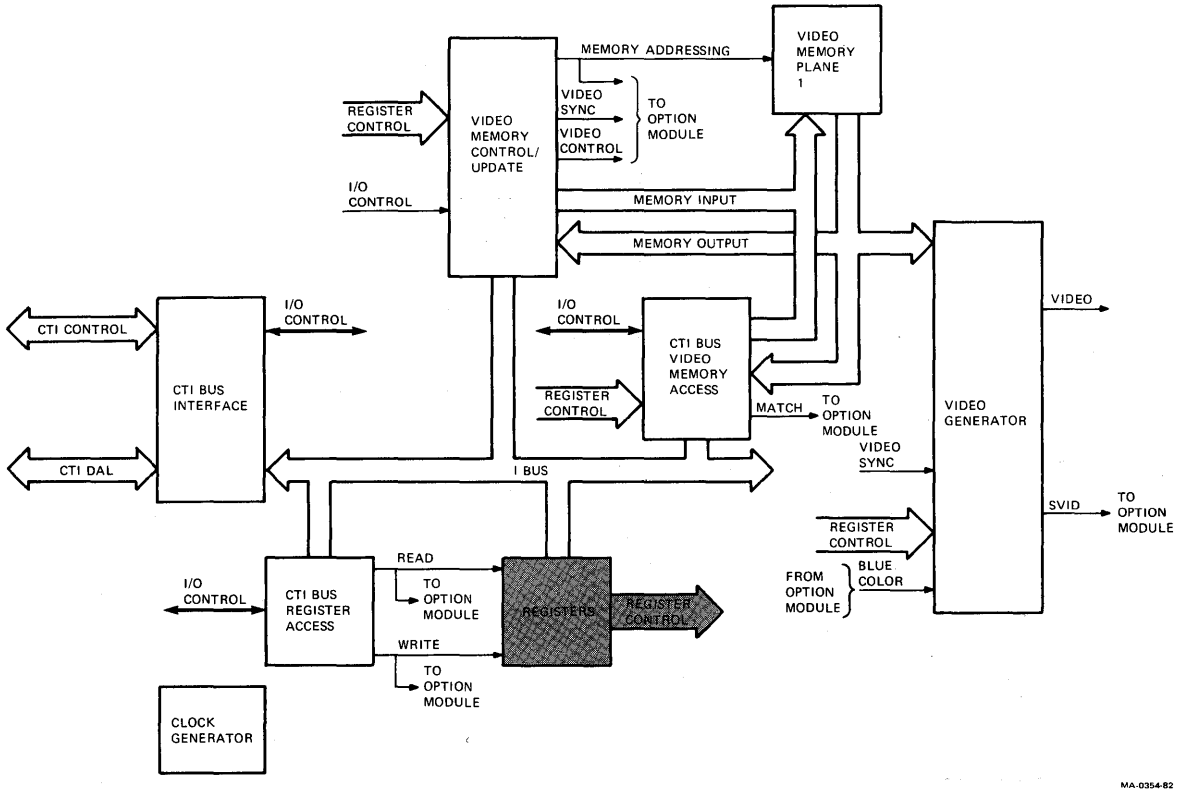


Figure 7-13 Counter Register Operation



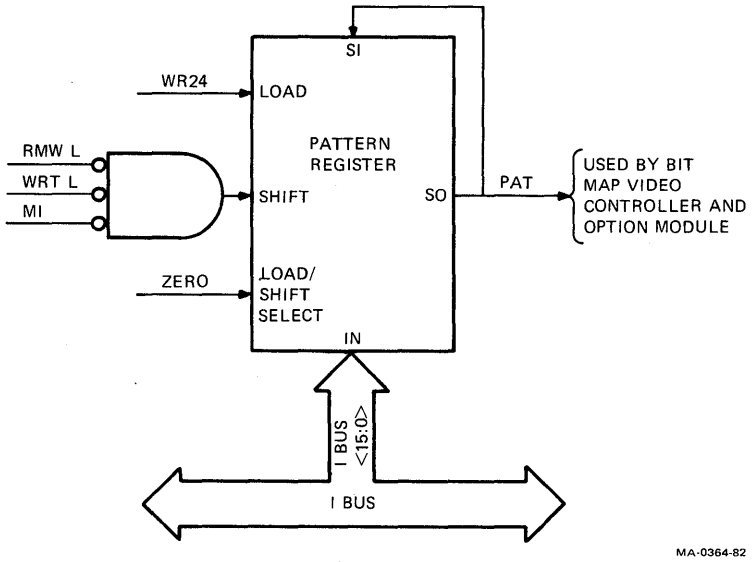
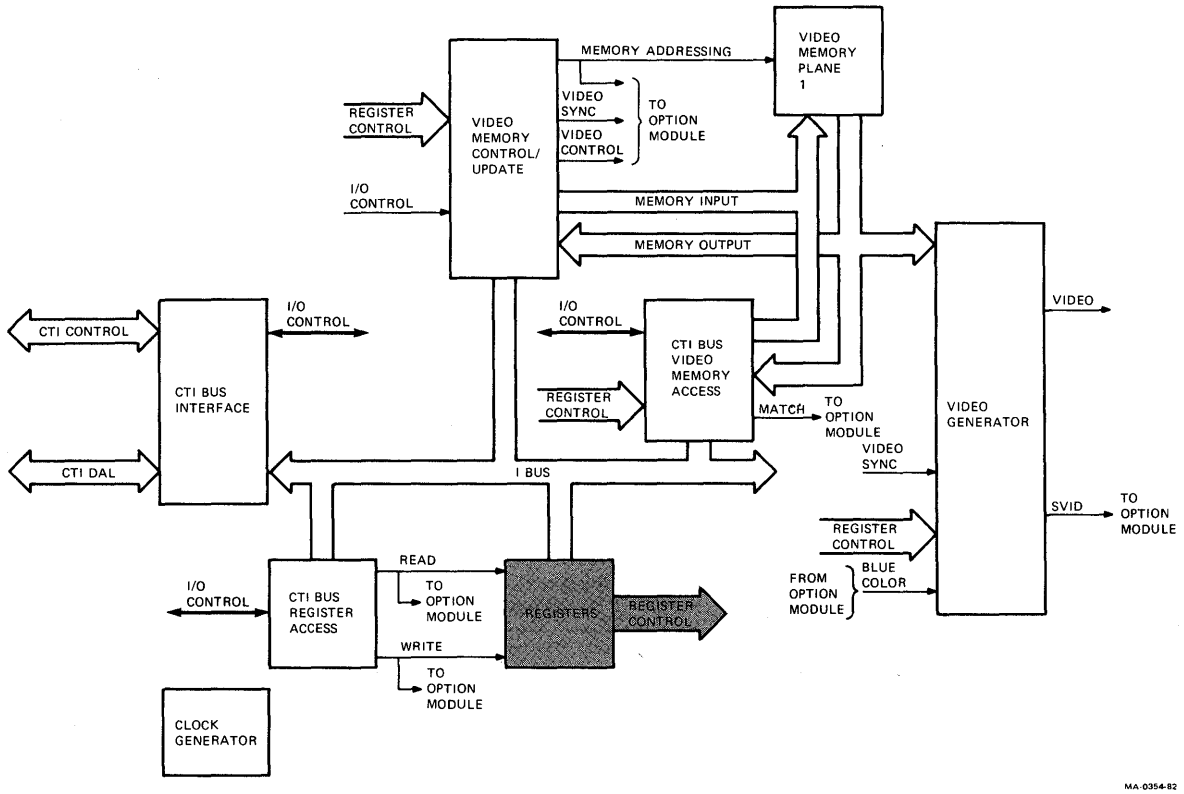


Figure 7-14 Pattern Register Operation



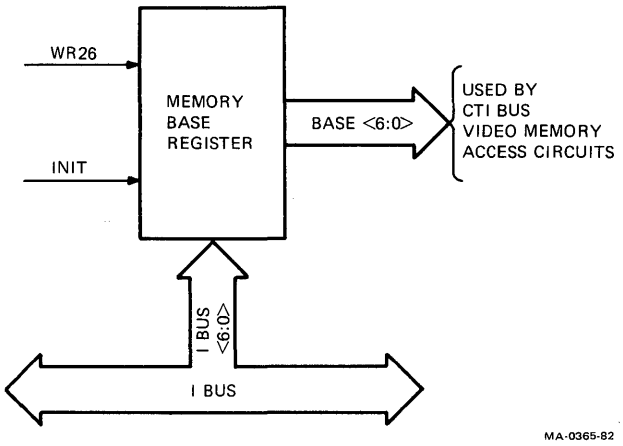
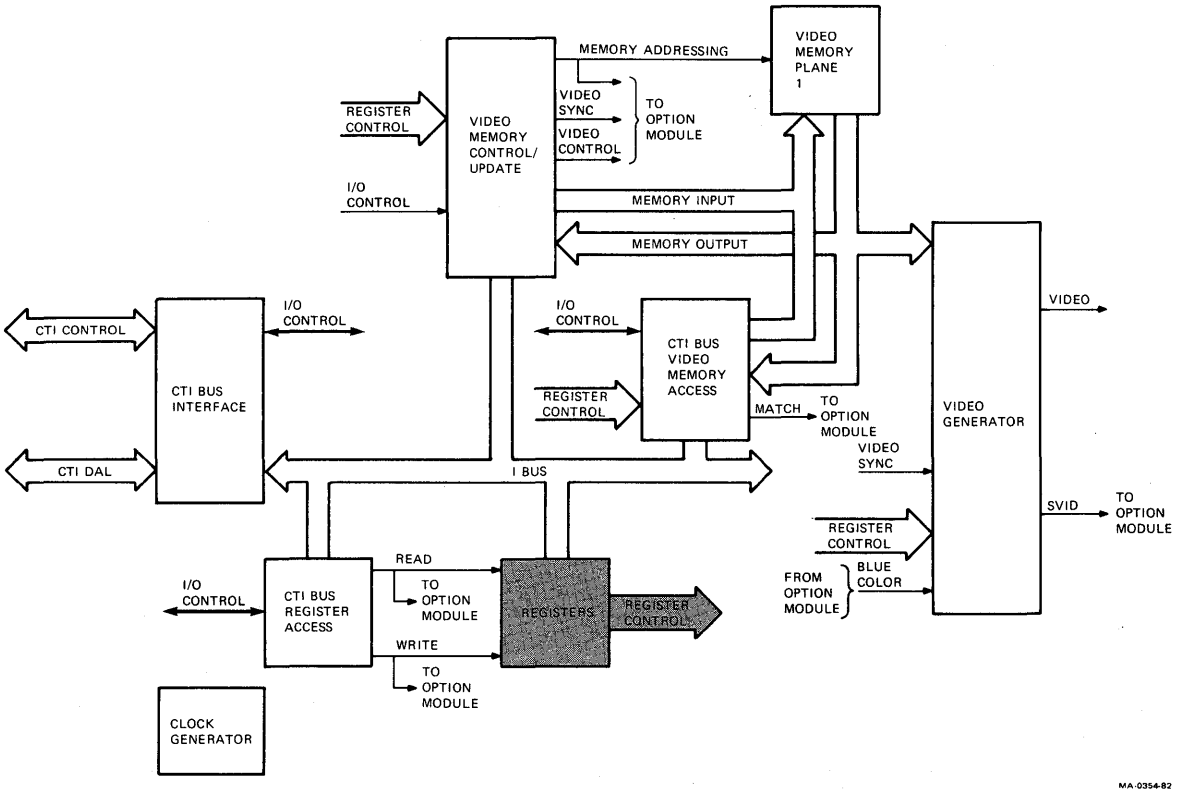


Figure 7-15 Memory Base Register Operation



7.3.1.4 CTI BUS Video Memory Access Circuits – The CTI BUS video memory access circuit (Figure 7-16) passes data between the internal bus and the video memory during host processor accesses to the video memory. To perform this function, this circuit uses the following components.

- Video memory address comparator
- CTI BUS video memory enable and reply buffer
- CTI BUS to video memory port
- Video memory to CTI BUS port

Video Memory Address Matching
To access the video memory, the host processor selects the video memory plane by accessing the plane 1 control register and setting the enable bit. Refer to Section 7.5 for the plane 1 control register definition. The video memory address comparator senses an enable video memory plane through the SELF and NO MEM signals.

The host processor then places a video memory address on the CTI BUS and asserts the I/O SEL signal. The I/O SEL enables the video memory address comparator to compare the 7-bit address in the base register to the 7-MSB of the CTI BUS (I BUS <21:15>) on the module. If a match occurs, the ADRS STRB (generated by the host processor) latches the comparator to generate a MATCH signal. This signal indicates that host processor is accessing a video memory plane address.

Video Memory Data Transfers
After a video memory MATCH is established, the DATA STRB from the host processor clocks the CTI BUS video memory enable and reply buffer. This generates a memory enable signal (MEM). During a DATA STRB, a clock signal (D3) which synchronizes read-modify-write video memory accesses, asserts a memory reply signal (MREP) for the CTI BUS interface circuits.

During a host processor read cycle, the WRITE signal from the CTI BUS interface circuit and a video memory write enable signal (WRT) from the video memory control and update circuits remain unasserted. This enables the video memory to CTI BUS port when MREP, MEM, and SELF are asserted. When enabled the addressed memory location data (MDO<15:0>) passes to the I BUS for the host processor.

During write cycles, the CTI BUS to video memory port passes data from the I BUS to the video memory data inputs (MDI>15:0>) when the memory enable signal (MEM) and the read-modify-write enable signal (D3) are asserted.

7.3.1.5 Clock Generator – The clock generator circuit (Figure 7-17) generates the required clock signals to synchronize all internal operations on the bit map video controller and the extended bit map modules. To perform this function, this circuit uses the following components.

- 20 MHz clock generator
- Clock divider
- High resolution clock generator

The 20 MHz clock generator provides three 20 MHz signals: CLKL, CLK1, and CLK2. Signal CLKL is sent to the extended bit map. Signals CLK1 and CLK2 are used by the bit map video controller.

The CLK1 signal is divided into a 10 MHz (D0), a 5 MHz (D1), and a 1.25 MHz (D3) signal. Signals D0, D1,and D3, are synchronized to the parallel enable (PE) signal from the video memory control and update circuits. This allows the clock signals to clock circuits at the desired intervals for every read-modify-write and read only cycle.

The CLKL, CLK1, CLK2, D0, D1, and D3, are all 50% duty cycle clocks. The high resolution clock generator produces a 5 MHz clock (DX) with a 25% duty cycle for the video generator circuits on the bit map video controller and the extended bit map.

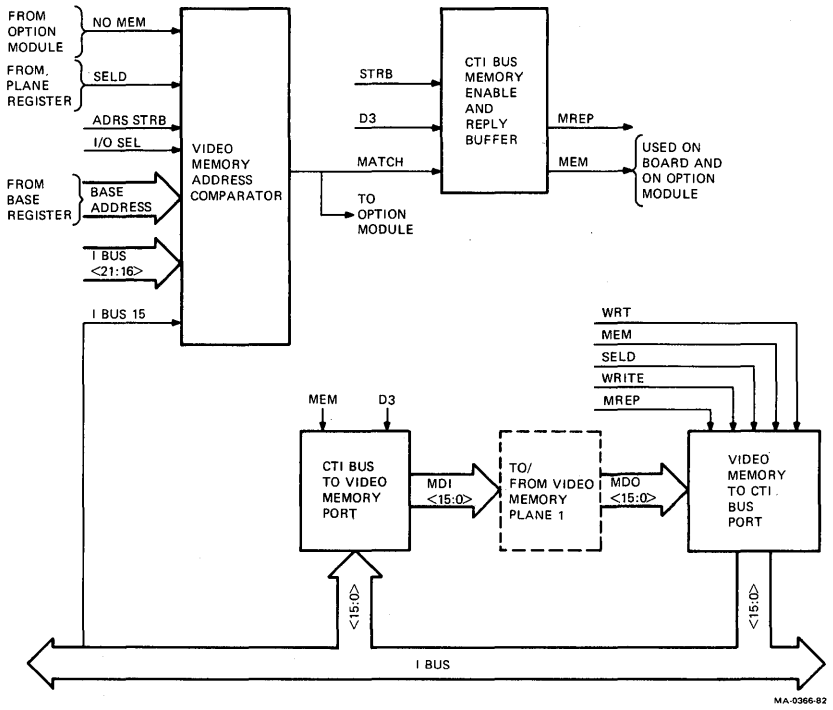
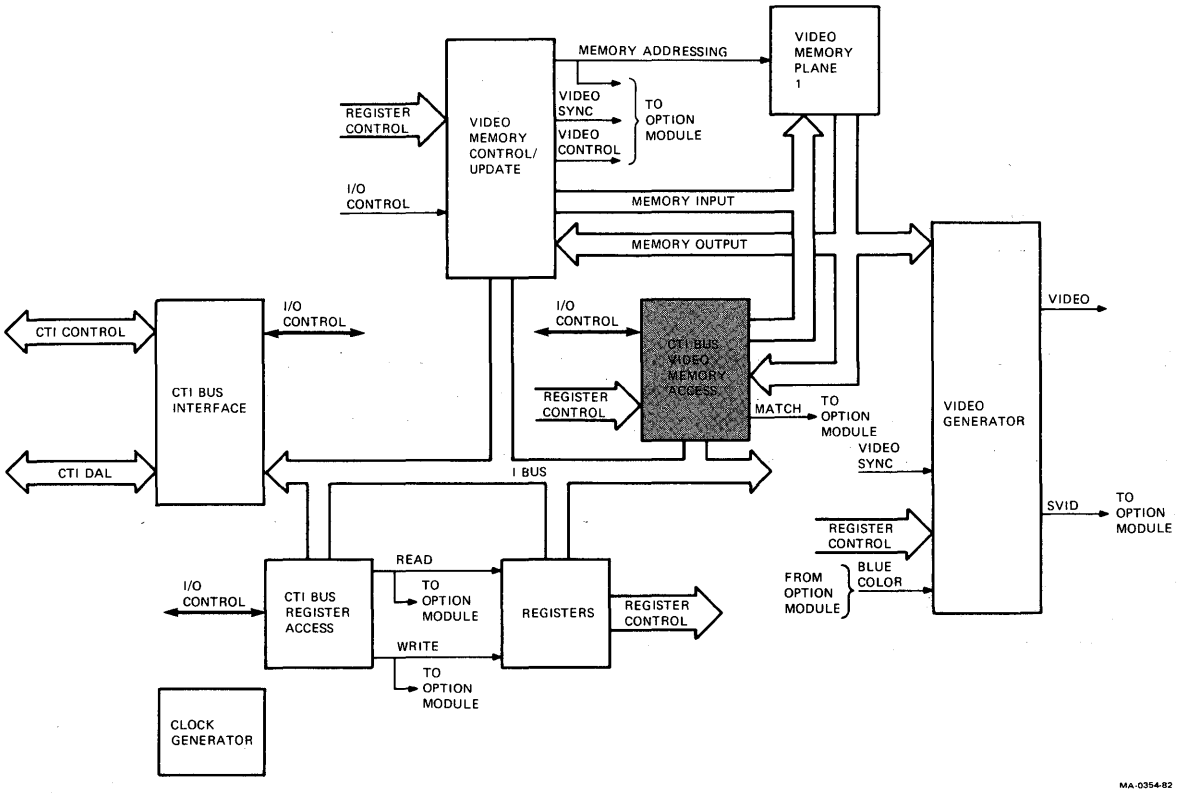


Figure 7-16 CTI BUS Video Memory Access Circuit Operation



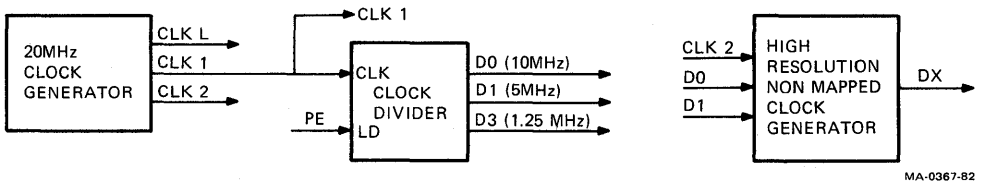
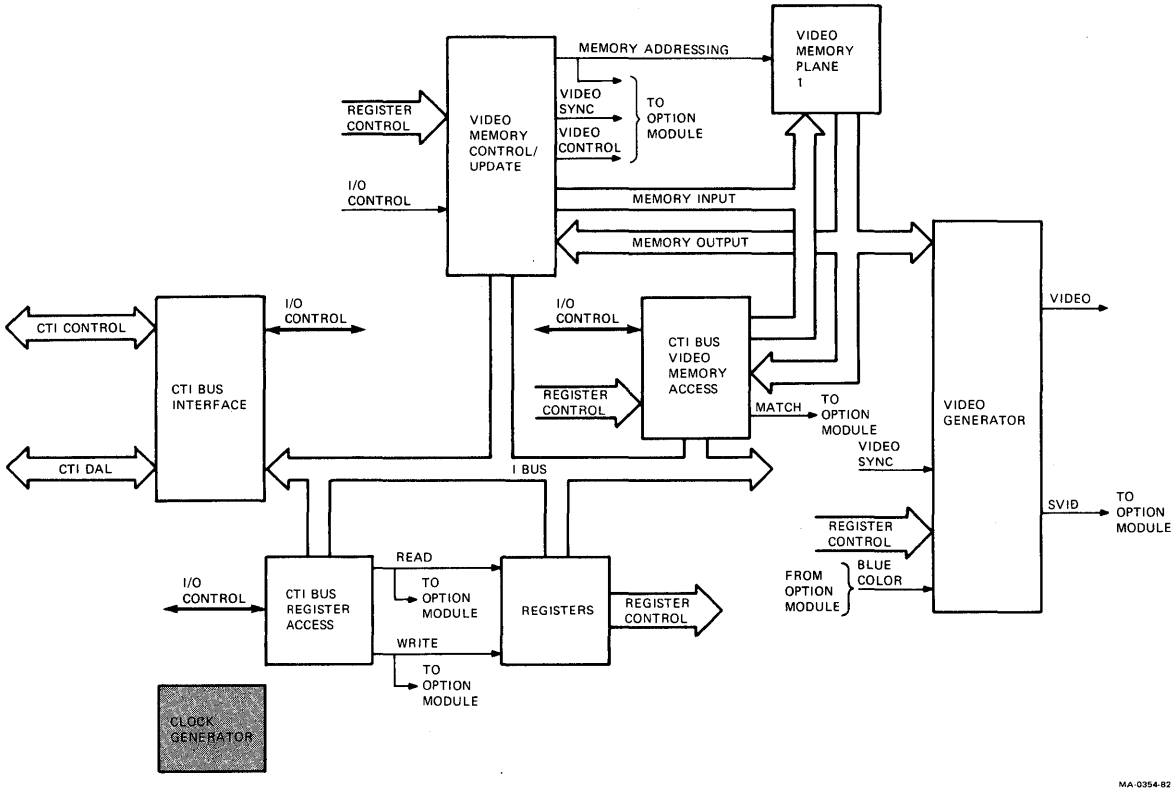


Figure 7-17 Clock Generator Circuit Operation



7.3.1.6 Video Memory Control And Update Circuit Operation – The video memory control and update circuits process commands from the host processor for both modules, control the generation of video signals for both modules, and update the video memory on the bit map video controller (Figure 7-18). To perform this function this circuit uses the following components.

- Video processor chip (DC717)
- Video controller chip (DC715)
- Synchronization buffer
- Memory write enable buffer
- Video data modification chip (DC716)

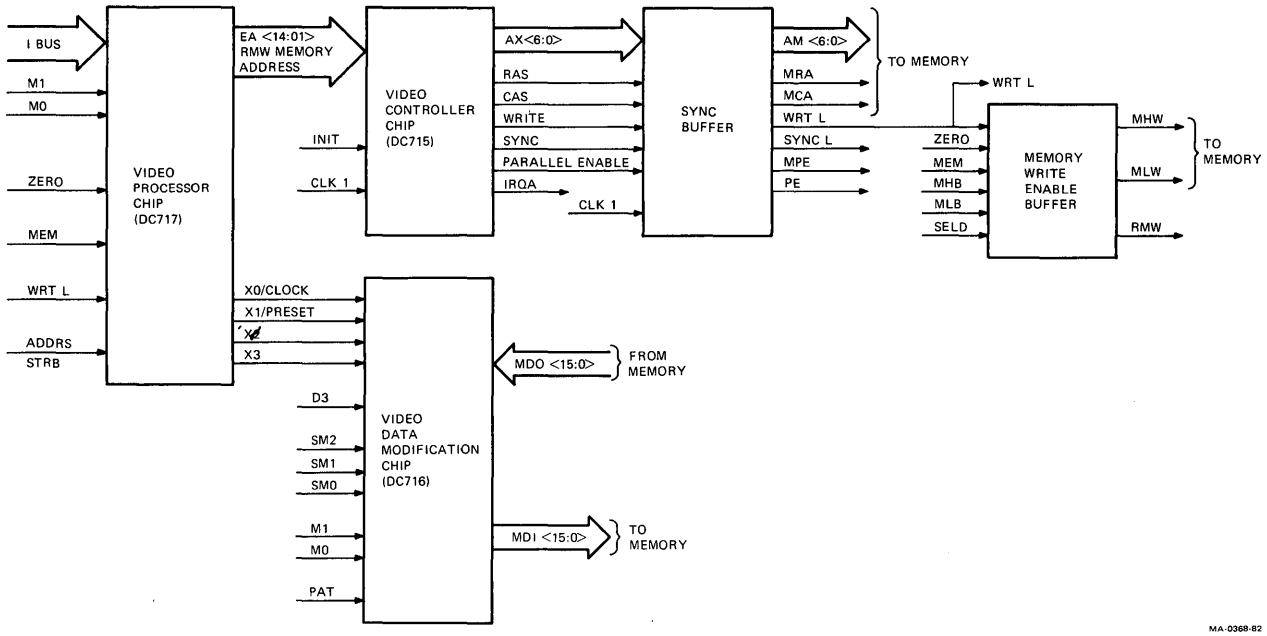
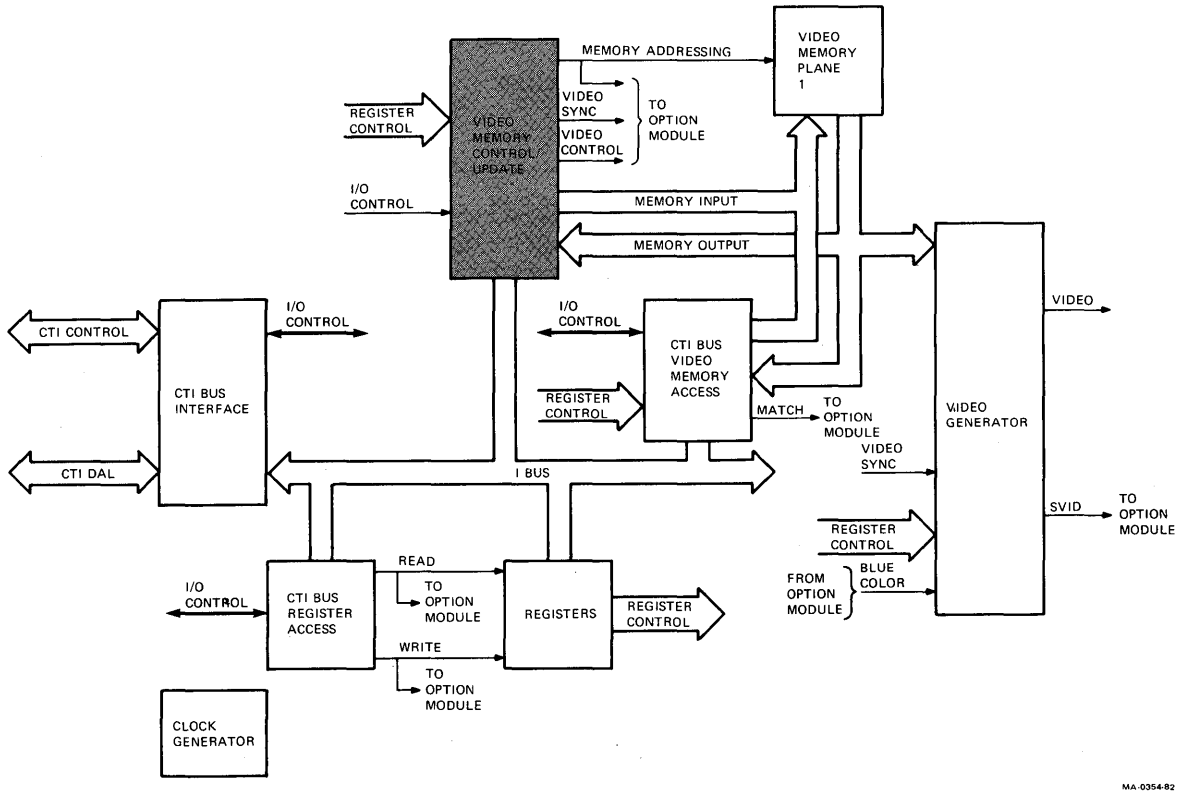


Figure 7-18 Video Memory Control and Update Circuit Operation



Video Processor Chip (DC717) Operation

The video processor chip is a 48-pin-low power schottky type gate array integrated circuit, manufactured by DIGITAL. This chip controls all read-modify-write cycles for the video memories. Two types of read-modify-write cycles can occur for the video memories, a host processor access read-modify-write cycle or a video processor read-modify-write cycle.

For a host processor read-modify-write cycle, a 14-bit address of the desired memory location is loaded into the video processor chip from the I BUS by an asserted ADDR STRB signal. The memory enable signal (MEM) from the CTI BUS video memory access circuits cause the chip to send the address to the video controller chip on the EA<14:01>lines.

For a video processor read-modify-write cycle, the X coordinate register, Y coordinate register, CSR, and counter register control the 14-bit address the chip provides to the video controller. The X and Y coordinate registers are internal to the video processor chip and the CSR and Counter registers are discrete. See Section 7.3.1.3 for further information about registers.

The four LSBs of the X coordinate register define the bit to be modified within the word and are sent to the video data modification chip. These same lines are multiplexed with the timing signals, CLOCK and PRESET, for the video data modification chip.

The video processor chip also contains control logic. The control logic controls the X and Y coordinate registers, the multiplexing of the read-modify-write address, and multiplexing of the bit in the word with the timing signals. This control logic receives M0, M1, ZERO, MEM, and WRT. Table 7-3 lists the operations the video processor chip performs when these signals are enabled.

In bit mode (M1 low), the X0 through X3 bits are the X coordinate registers least significant bit outputs to the video data modification chip. In word mode (M1 high), CLOCK is the WRT L buffered, and PRESET indicates an underflow or overflow of the most significant bit from the X coordinate register.

Table 7-3 Video Processor Chip Operation Mode Selection

Signal	Description
MEM	If present, this signal selects a host processor read- modify-write cycle for the video memory and disables the X and Y coordinate registers. If not present, a video processor read-modify-write cycle is selected and the X and Y coordinate registers are selected.
ZERO	Counter register ZERO disables the X and Y coordinate registers to count and enables the registers to be loaded.
WRT L	The clock signal for the X and Y cooordinate registers to increment or decrement.
M1 and M0	These 2 bits from the CSR indicate a X and Y coordinate register mode as follows.

M1	M0	Operations
0	0	Bits shifted left to right
0	1	Bits shifted top to bottom
1	0	Words shifted left to right
1	1	Words shifted right to left

Video Controller Chip (DC715) Operation

The video controller chip is a 48-pin low power schottky type gate array integrated circuit manufactured by DIGITAL. The chip controls all memory and video timing, generates screen refresh addresses, and controls vertical scroll.

For memory timing, this chip divides the 20 MHz system clock (CLK1) by 16 (800 ns). The 800 ns clock represents two memory cycles, one read-modify-write cycle for modifying memory data and one read only cycle for screen refresh. The chip also generates the RAS and CAS signals and time multiplexes the 14-bit video memory address for both memory cycles into 7-bit multiplexed address bus (AX<6:0>) for the synchronization buffer.

For video timing, the CSR controls this chip to generate horizontal, vertical, and video sync signals. The CSR programs horizontal and vertical counters internal to the chip to provide 50 or 60 Hz operation and interlaced or noninterlaced operation. These counters also coordinate the video memories addressing for the screen refresh cycles.

The six least significant bits of the horizontal counter form the six least significant bits of the screen refresh address (word within line). The eight least significant bits of the vertical counter form the eight most significant bits of the screen refresh address.

The chip contains a multiplexer to switch between the external address (EA01-EA14) for read-modify-write cycles generated by the video processor chip, and the internally generated read only addresses for screen refresh cycles. The memory timing clock controls this multiplexer. During the first half of every 800 ns display cycle, the multiplexer selects the external address. During the second half of the cycle the multiplexer selects the internal address.

The video controller chip contains the scroll register. This register's are always added to the eight most significant bits of the selected memory address. This operation modifies all addresses to the video memory. This moves all information in memory and causes a vertical scroll.

Table 7-4 describes the signals generated by the video controller chip for the synchronization buffer.

Table 7-4 Video Controller Chip Output Signal Definitions

Signal	Description
AX<6:0>	The time multiplexed RAS/CAS address bus for dynamic RAM devices.
RAS	Row address select for video memory control
CAS	Column address select for video memory control
WRITE	WRITE pulse for video memory control
PE	A parallel enable signal is generated to parallel load the video shift register in the video generator with memory data. It is only generated during the active portion of the video timing (64 times per line during 256 lines in 625 line mode or 240 lines in 525 line mode).
SYNC	This signal contains the complete video sync signal with horizontal sync, vertical sync and equalization pulses.
IRQA	When enabled by the CSR, this signal is the vertical retrace interrupt request for the host processor.

Video Memory Address and Video Control Synchronization
The video control chip generates the video memory address and video control signals. These signals are synchronized by the synchronization buffer and the memory write enable buffer. This allows all signals to switch on the 20 MHz system clock edges. The video memory address AX<6:0> becomes AM<6:0>. The row and column address strobes RAS and CAS become MRA and MCA. The write strobe for video processor cycles becomes WRT L. The video sync signal for the video generator circuits becomes SYNC L. The parallel enable signal goes to the video generator circuits as MPE and to the clock generator circuits as PE.

Two more signals are provided for write operations to the video memory, the memory high byte write (MHW) and memory write low byte (MLW). These signals are generated for both host processor to video memory accesses and video processor to video memory accesses. For a host processor cycle, the ZERO, MEM, and SELD enable the buffer while the CTI BUS interface circuit signals WHB and WLB select MHW and MLW respectively. For a video processor cycle, the synchronized WRT L signal generates both MHW and MLW and a RMW signal to indicate a video processor read-modify-write cycle.

Video Data Modification Chip (DC716) Operation
The video data modification chip is a 48-pin low power schottky type gate array integrated circuit, manufactured by DIGITAL. This chip performs the data modification to the bit map video controllers video memory during video processor controlled read-modify-write cycles.

This chip receives control signals from the video processor chip and register control signals from the CSR, plane control, and pattern registers. These signals control the video data modification chip to modify the data stored in the video memory. Table 7-5 describes the video data modification chip operation selection.

Refer to Section 7.5 for further information on video processor logical operations.

Table 7-5 Video Data Modification Chip Operation Selection

Signal	Function
X3-X0	In bit mode, these four inputs specify the bit to be modified within the addressed word.
CLOCK\ PRESET	In word mode, these two signals control shift operations.
M1-M0	These signals specify the bit and word operation modes.
SM2-SM0	These submode signals specify the logical operation to be performed by the chip.
PAT	The least significant bit of the pattern register can be used as data for the logical operations.
D3	A timing signal that controls the memory data inputs and outputs.
RMW	This read-modify-write signal enables the chip to perform a logical operation.

7.3.1.7 Video Memory Circuit Operation – The video memory is an array of 16 (16K by 1-bit) dynamic RAMs (Figure 7-19). The video memory control and update circuit address these RAMs for all read-modify-write operations and read only operations. Memory input data (MDI<15:0>) comes from the video memory control and update circuits or the CTI BUS to video memory access circuits. Memory output data (MDO<15:0>) goes to the video memory control and update circuits, the CTI BUS to video memory access circuits or the video generator circuits.

7.3.1.8 Video Generator Circuit Operation – The video generator circuit (Figure 7-20) assembles the video data and sync pulses, then amplfies them for transmission over the CTI Private Bus to the monitor. To perform this function this circuit uses the following components.

- Parallel-to-serial converter
- Serial serial shift buffer
- Nonmapped resolution decoder
- Nonmapped video sync buffer
- Mapped video sync buffer
- Video drivers

The video generator operates in two modes nonmapped or mapped. The COLOR signal, from the plane register, selects the operation for either mode. All circuits necessary for single plane nonmapped mode video signal generation (monochrome monitor only) are on the bit map video controller. For mapped mode operation, these circuits serialize the video memory data and pass it to the extended bit map module. The external bit map returns blue video data (CM1 and CM0) and generates a BLUE VIDEO signal and a MONO VIDEO signal.

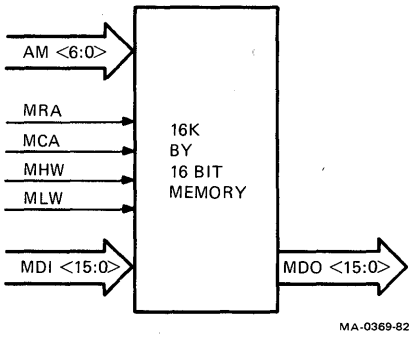
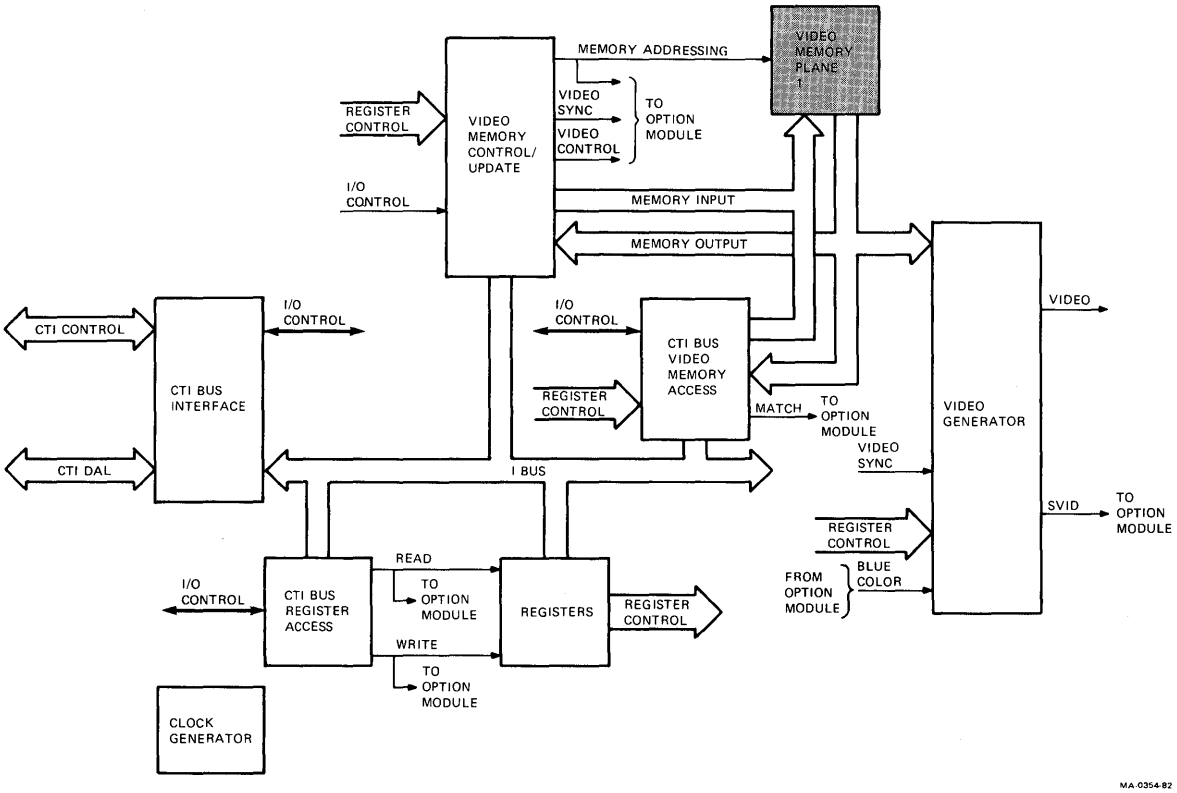


Figure 7-19 Video Memory Circuit Operation



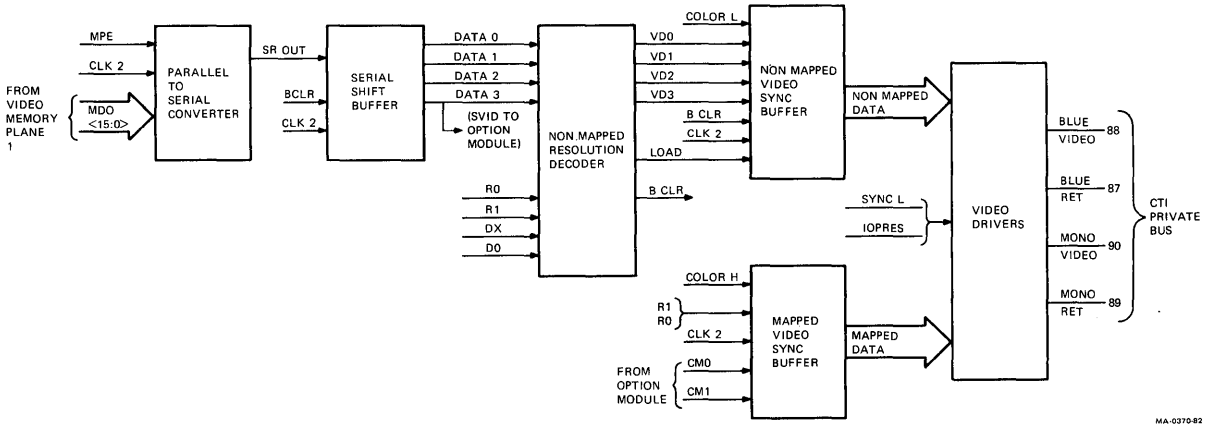
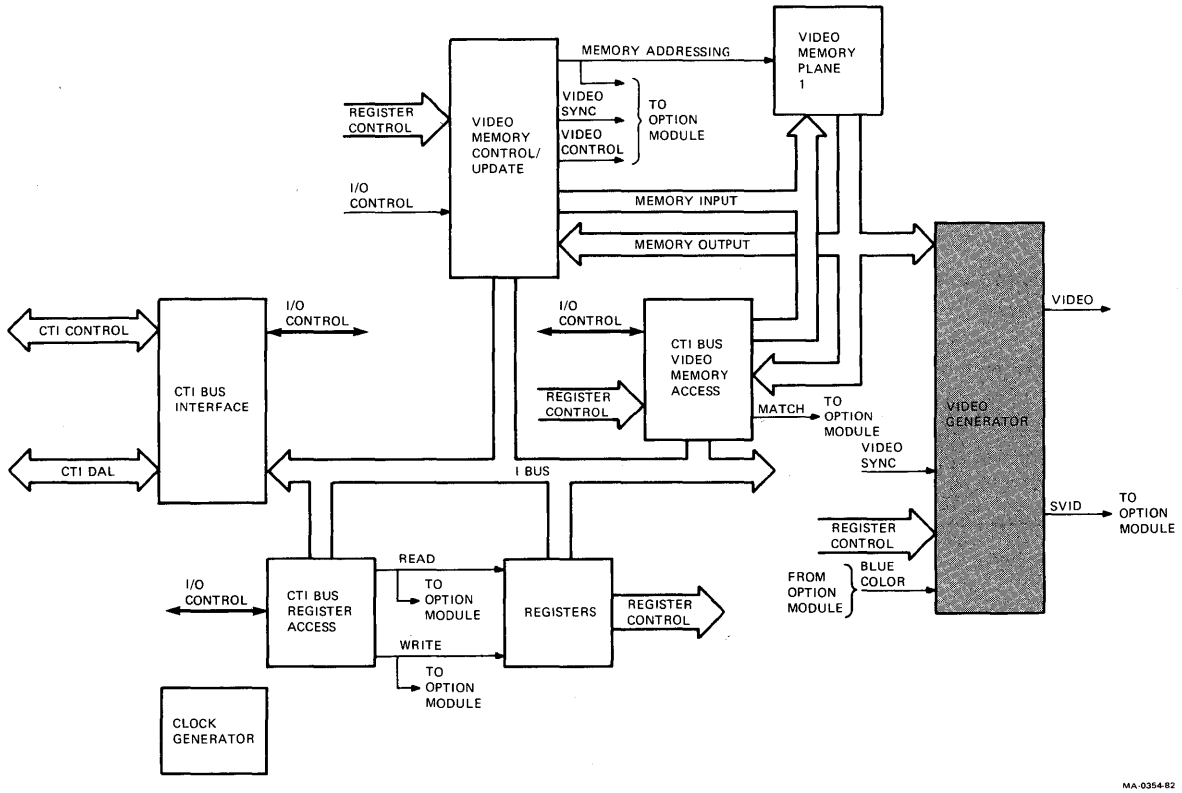


Figure 7-20 Video Generator Circuit Operation



Nonmapped Video Signal Generation
During a read only operation, the parallel enable signal (MPE) from the video memory control and update circuit enables the parallel to serial converter to load a data word from the video memory. The 20 MHz clock (CLK2) shifts the data (SROUT) to the serial shift buffer. The video memory control and update circuits have complete control over the converter. These circuits control the loading and shifting of the data to a serial format for lines and disable data loading during vertical and horizontal retraces.

The serial shift buffer provides the serial data to the nonmapped resolution decoder in three forms: single bits at a 20 MHz rate (D0), two bits at a time at 10 MHz rate (D0 and D1), and four bits at a time at a 5 MHz rate (DATA 0 through DATA 3).

The nonmapped resolution decoder receives the resolution selection signals (R1 and R0) from the plane 1 control register and clock signals (D0 and DX) from the clock generator. The R1 and R0 signals selects one of four modes of operation: single-bit resolution, dual-bit resolution, quad-bit resolution, or a blank screen. Table 7-6 shows which data bits are provided to the nonmapped video sync buffer as video data and how the different resolution modes are selected.

The video data is synchronized with the CLK2 signal by the nonmapped video sync buffer and passed to the video drivers. The drivers amplify the video data and the sync pulse from the video memory control and update circuits and pass the composite video signal to the CTI Private Bus as MONO VIDEO. Figure 7-21 shows the three types of composite video signals the video generator produces during nonmapped operation.

Mapped Video Signal Generation
During a read only operation, the parallel enable signal (MPE) from the video memory control and update circuit enables the parallel-to-serial converter to load a data word from the video memory. The 20 MHz clock (CLK2) shifts the data (SROUT) to the serial shift buffer. The video memory control and update circuits have complete control over the converter. These circuits control the loading and shifting of the data to a serial format. The converter is not loaded during vertical and horizontal retraces.

Table 7-6 Nonmapped Resolution Mode Operation

R1	R0	Load	VD3	VD2	VD1	VD0	DUTY	BCLR L
0	0	0	Data 0	Data 0	0	0	50 ns	1
0	1	DO	Data 1	Data 0	0	0	100 ns	1
1	0	DX	Data 3	Data 2	Data 1	Data 0	200 ns	1
1	1	0	0	0	0	0	none	0

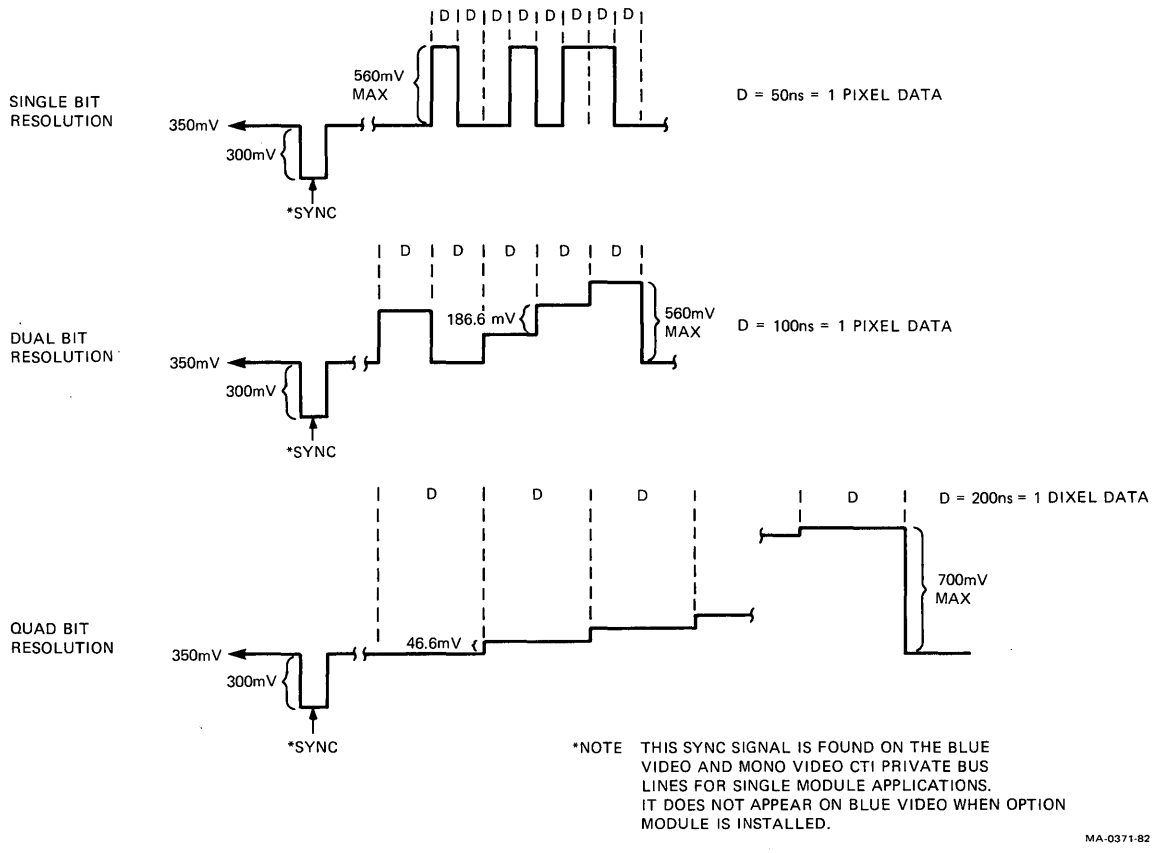


Figure 7-21 Nonmapped Video Signal Characteristics

The serial shift buffer delays the serial data by 200 ns and then sends it to the extended bit map (DATA 3 – SVID). The extended bit map returns two serial data bits (CM1 and CM0) to the mapped video sync buffer. This buffer is clocked by the 20 MHz system clock (CLK2) to synchronize the data at the video drivers inputs. If one of the resolution bits (R1 and R0) is a 0, the mapped video sync buffer is enabled. If both resolution bits are a 1, the mapped video sync buffer is disabled.

The video drivers amplify the color video data from the video memory control and update circuits. The drivers then pass BLUE VIDEO and MONO VIDEO signals to the CTI Private Bus. Figure 7-22 shows the video signal the video generator produces the video signal during mapped operations.

NOTE

When the extended bit map module is not in the video subsystem, the plane 1 video generator amplifies the SYNC signal. The signal appears on the BLUE VIDEO line and the MONO VIDEO line. When the extended bit map module is in the video subsystem, the plane 2 video generator on the extended bit map amplifies the SYNC signal. This signal appears on the GREEN VIDEO line and the MONO VIDEO line.

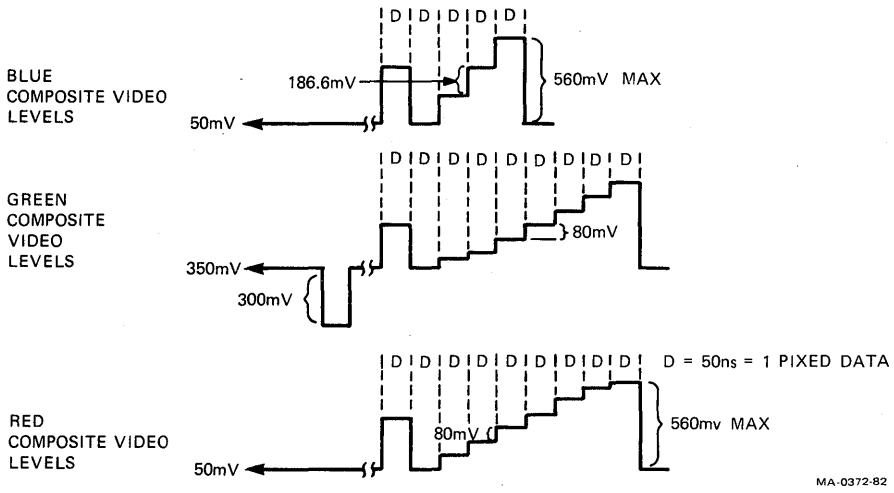


Figure 7-22 Mapped Video Signal Characteristics

7.3.2 Extended Bit Map Module Detailed Operation

The extended bit map is an optional module when used as alternate display planes for monochrome monitors. It is required for color monitors for to provide the required data storage and red and green video signals. To perform these functions, the module contains the following circuits.

- CTI BUS interface
- Plane and color map registers
- Two CTI BUS video memory access circuits
- Two video memory update circuits
- Two video memory planes
- Two video generators

7.3.2.1 CTI BUS Interface Circuit Operation – The CTI BUS interface circuit for the extended bit map module (Figure 7-23) passes data between the CTI BUS and the internal bus (I Bus) for direct and indirect accesses. To perform this function, this circuit uses the following components.

- CTI BUS control signal buffer
- Memory plane access decoder
- CTI BUS data/address transceivers
- Identification buffer

Direct Extended Bit Map Module Accessing

The extended bit map module responds to direct host processor read accesses with the module identification code. Host processor write accesses to the module have no affect on the module operation. For direct accesses to the module, the host processor asserts the slave device enable signal (B SDEN L) and the slot select signal (BSS L) to the CTI BUS control signal buffer. These signals generate a module transmit signal (XMIT) and an enable identification buffer signal (ENAID). These signals simultaneously enable the identification buffer and CTI BUS data/address transceivers. This allows the buffer to pass the modules identification code over the I Bus to the CTI BUS BDAL lines to the host processor.

The module also generates an acknowledgement signal (REPLY) for the host processor. It is generated when the CTI BUS DATA STRB is asserted with the SLOT SELECT signal.

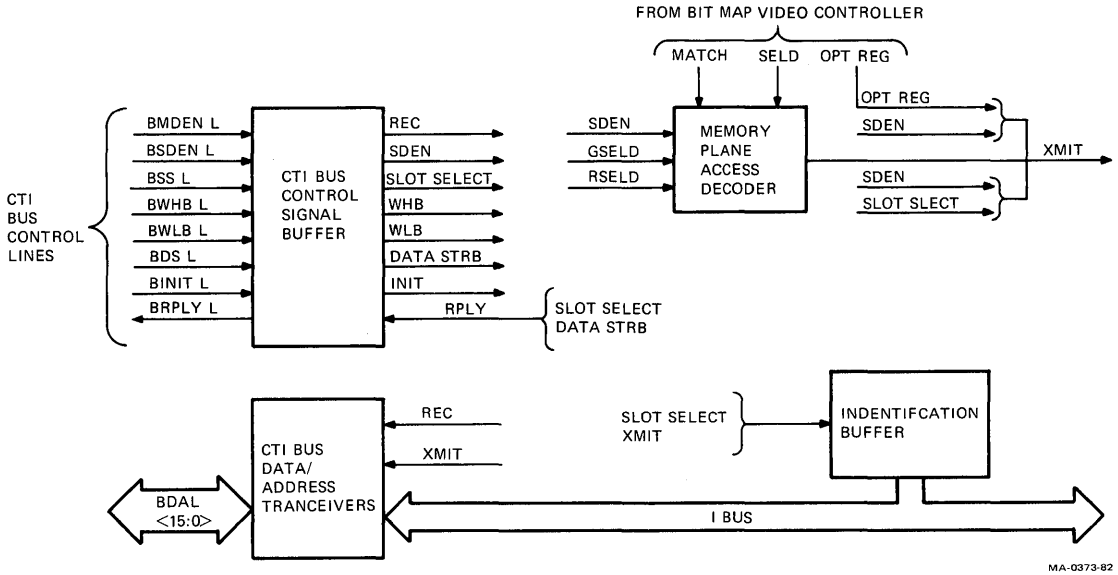
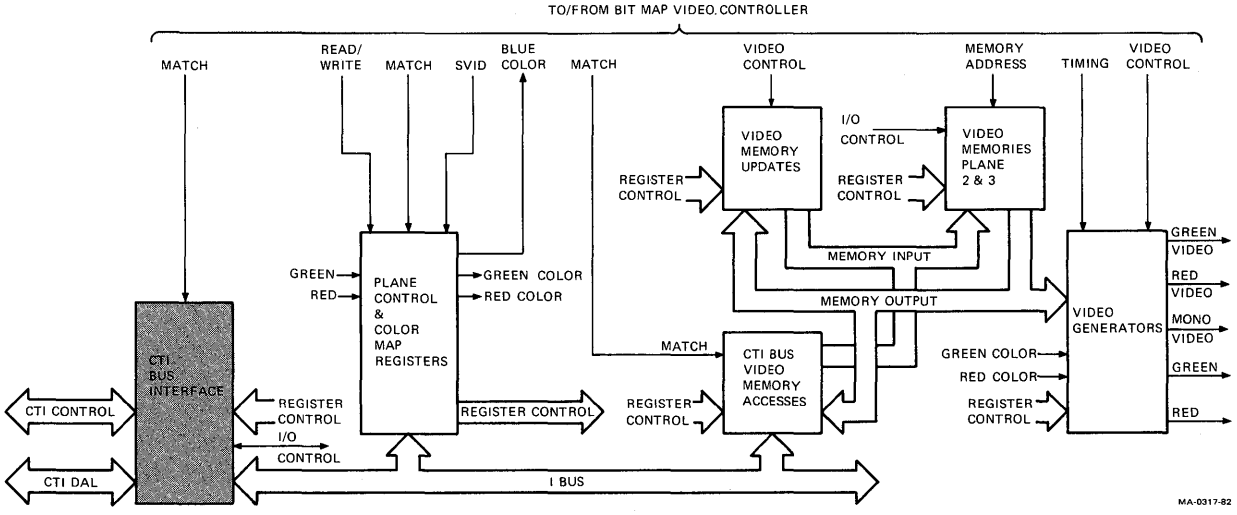


Figure 7-23 CTI BUS Interfaced Circuit Operation (Option Module)



Indirect Extended Bit Map Module Accessing
For indirect extended bit map module accessing, the host processor does not assert the SLOT SELECT signal. A buffered B MDEN L signal (REC) passes data from the host processor to the modules internal bus (I Bus). This signal enables the CTI BUS data/address transceivers to pass data on the BDAL lines to the internal bus (I Bus). Data is passed from the internal bus to the host processor in two modes: register access or video memory access.

During a read access to the extended bit map module registers, a transmit (XMIT) signal is generated for the CTI BUS data/address transceivers. An option register access signal (OPT REG) from the bit map video controller enables the slave device enable signal (SDEN) to generate a XMIT signal. The data is then passed over the I Bus from the registers to the CTI BUS.

During a read access to the extended bit maps video memory, the memory plane access decoder generates the XMIT signal for the CTI BUS data/address transceivers. A MATCH signal from the bit map video controller enables the decoder. This indicates that the host processor accessed an address in the assigned 16K word (32K byte) video memory plane range. The slave device enable signal generates an XMIT signal during the following conditions.

- The video memory plane on the bit map video controller is not enabled (SELD unasserted).
- One of the video memory planes on the extended bit map is enabled (GSELD or RSELD is asserted).

7.3.2.2 Plane 2 and 3 Control and Color Map Register Operation – The plane 2 and 3 control and color map registers (Figure 7-24) are written or read to with data from the modules internal bus, under control of the bit map video controller. The plane 2 and 3 control register selects the operational mode of the video memory update circuits for the plane 2 (green) and plane 3 (red) video memories, and the plane 2 (green) and plane 3 (red) video generators on the extended bit map. The color map register controls the generation of the color composite video signals during mapped operations.

Plane 2 and 3 Control Register
The plane 2 and 3 control register is read or written to under control of the bit map video controller. A write strobe (WR10) loads data from the internal bus (I Bus) into the register. A read strobe (RD10) places the register contents on the internal bus. Refer to Section 7.3.2.1 for further information on host processor to module and module to host processor transfers.

A CTI BUS initialization signal (INIT), passed to the module by the CTI BUS interface circuits, resets the plane 2 and 3 control register contents. This ensures that no video memory plane is selected or enabled after an initialization.

Color Map Register Operation
During mapped operations, the color map register (CMR) provides data for the generation of composite video signals. This register is an eight word by 8-bit memory. Each word is preloaded with a value which controls each of the three video generators on both modules to generate a composite video signal. There are eight (out of 256) preselected combinations that the video subsystem can generate on a color or monochrome monitor.

The bit map video controller loads the CMR (WR12 asserted) from the internal bus (I Bus). The low byte on the I Bus (I<7:0>) is the data word. The upper three bits (I<10:8>) define the address the data word is loaded into. This procedure is performed to define the eight combinations the subsystem will generate for an application.

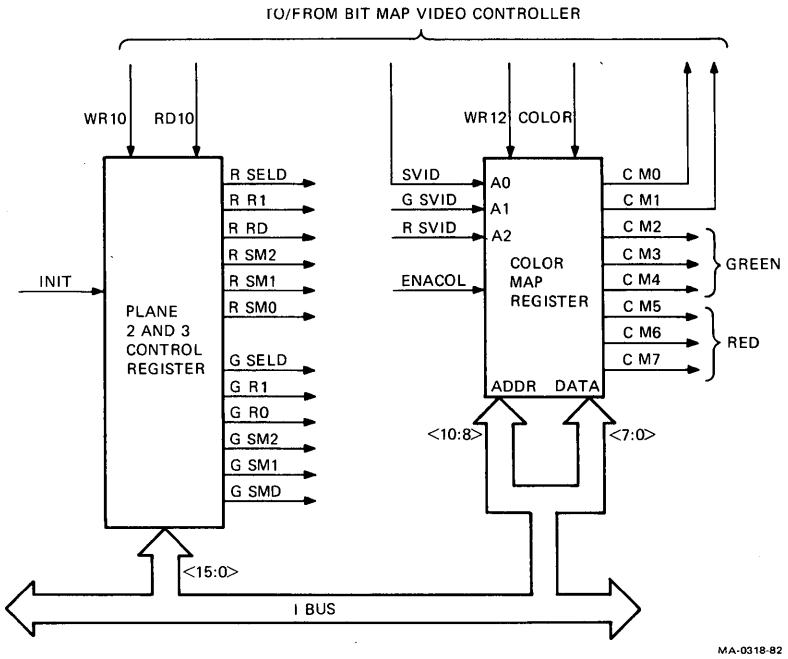
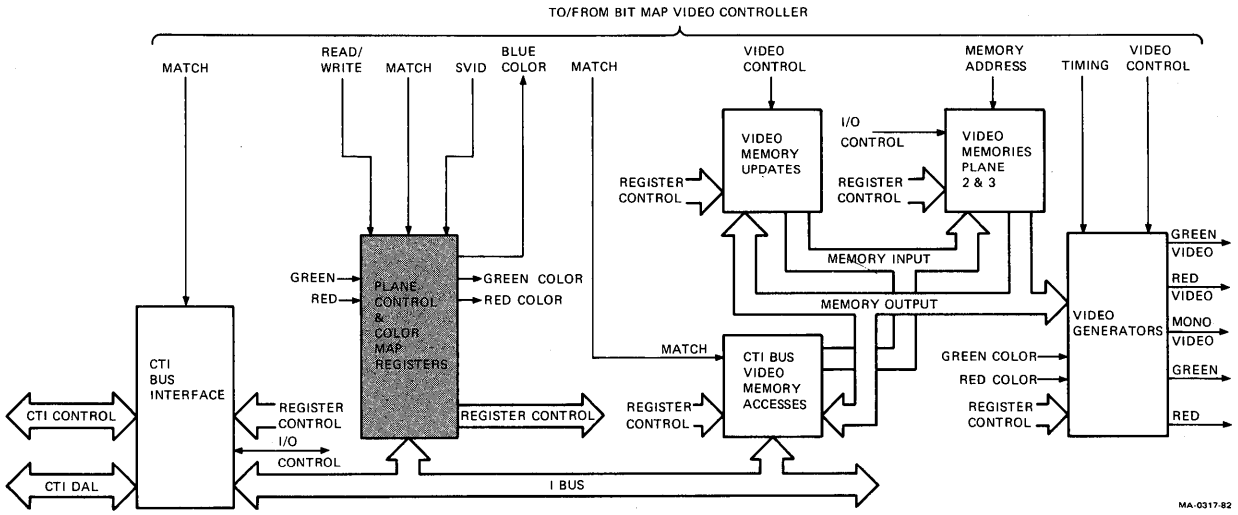


Figure 7-24 Plane 2 and 3 Control and Color Map Register Operation (Option Module)



After the CMR is loaded, serial video data from the three video generators on both modules form a 3-bit address for the color map register. The serial data from the plane 1 video generator is A0, the serial data from the plane 2 video generator plane is A1, and the serial data from the plane 3 video generator is A2.

The addressed 8-bit word is split up with certain bits passed back to each video generator. The bits select composite video signal levels which each video generator produces. For the plane 1 video generator, CM0 and CM1 select one of four levels; for the plane 2 video generator, CM2, CM3, and CM4 select one of eight levels; for the plane 3 video generator, CM5, CM6, and CM7 select one of eight levels.

The COLOR signal from the bit map video controller enables the color map register to operate and puts the video subsystem in the mapped operation mode.

The ENACOL signal is a 51 μs disable signal to blank the color map register output during horizontal and vertical screen retraces.

7.3.2.3 CTI BUS Video Memory Access Circuit Operation – The extended bit map contains two CTI BUS to video memory access circuits, one for each video memory plane. Figure 7-25 shows the operation of both pairs of circuits. To pass data between the host processor and each video memory, these circuits use the following components.

- Video memory plane access control circuit
- Plane 2 (green) video memory plane output port
- Plane 3 (red) video memory plane output port
- Plane 2 (green) video memory plane input port
- Plane 3 (red) video memory plane input port

Each port is controlled by the video memory plane access control circuit. this circuit is controlled by signals generated by the bit map video controller. The operation and function of this circuit is similar to the CTI BUS video memory access circuits on the bit map video controller. See Section 7.3.1.4 for further information.

7.3.2.4 Video Data Update Circuit Operation – The extended bit map contains two video data update circuits, one for each video memory plane. Figure 7-26 shows the circuits for both pairs of circuits. To update each video memory two video data modification chips use common control signals from the bit map video controller module but separate sub mode signals (SM2 – SM0) from the plane 2 and 3 control register. The operation of these chips is similiar to the video data modification chip described in Section 7.3.1.6.

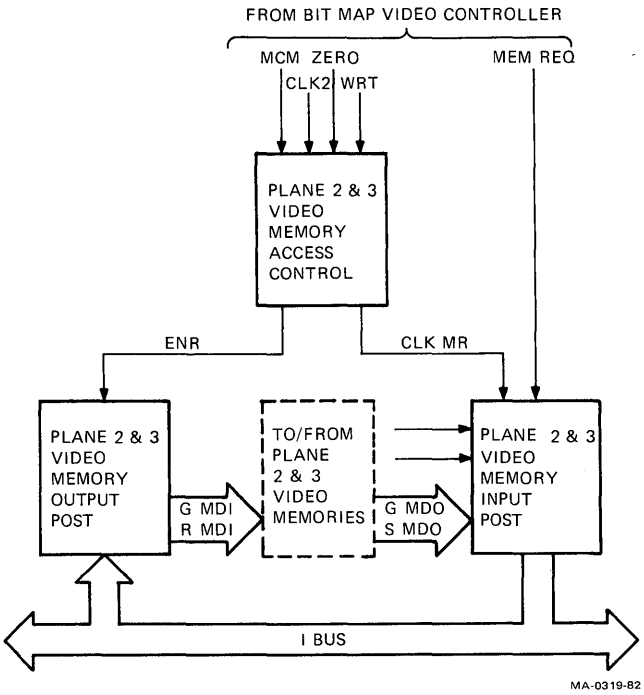
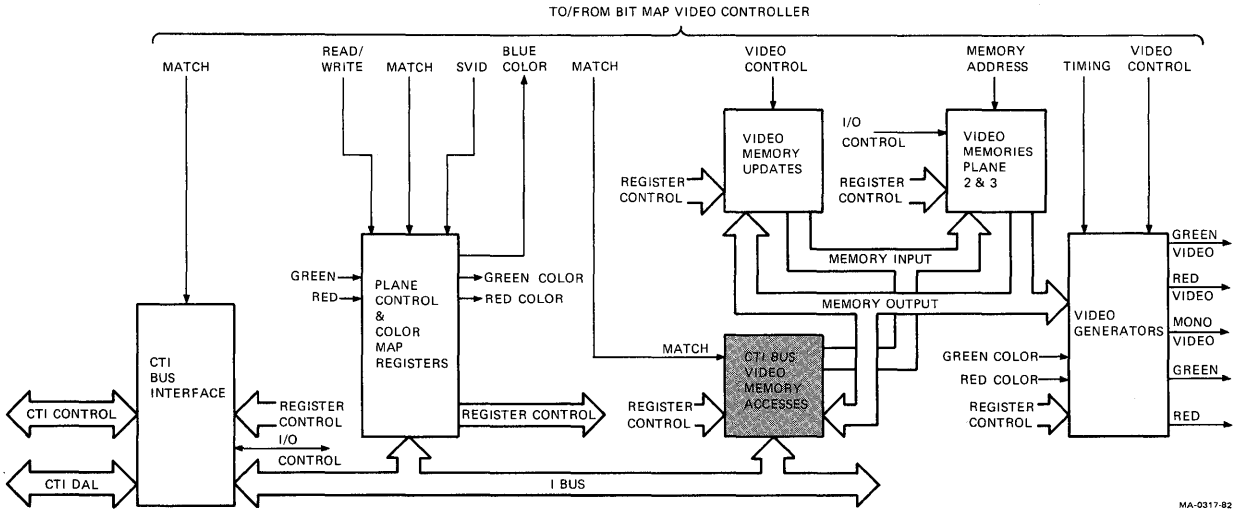


Figure 7-25 CTI BUS Video Memory (Plane 2 and 3) Access Circuits Operation (Option Module)



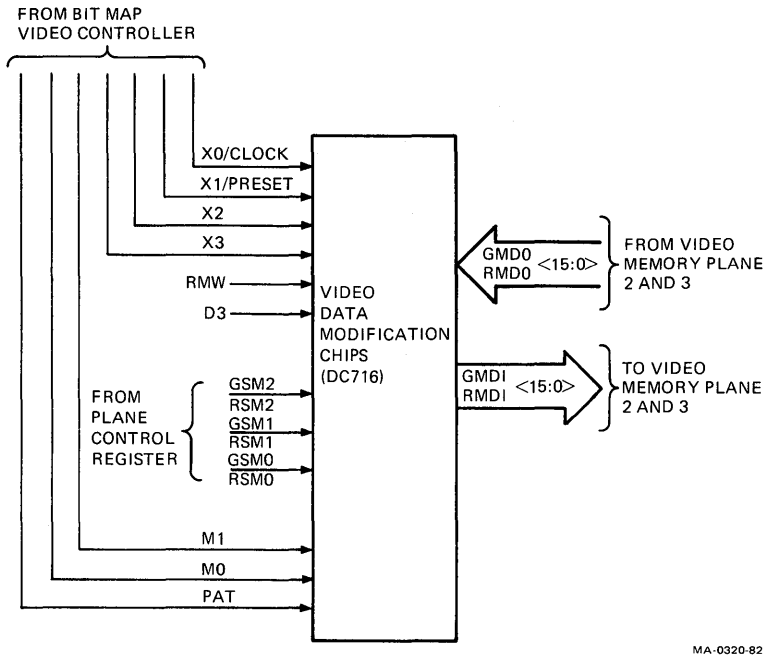
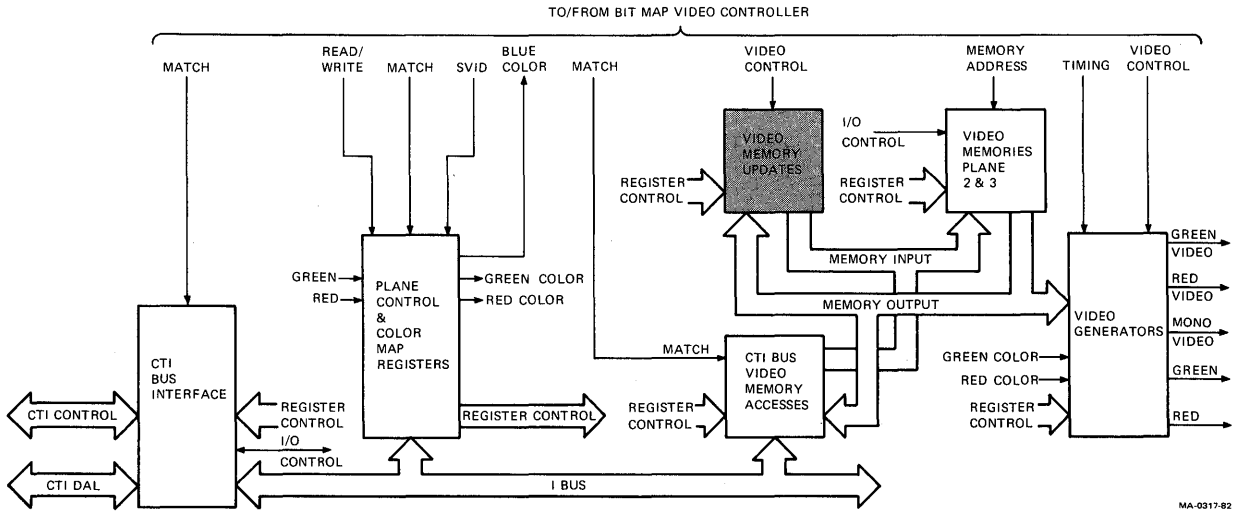


Figure 7-26 Video Data Update Circuit Operation (Option Module)



7.3.2.5 Video Memory Plane 2 and 3 Circuit Operation – The extended bit map contains two video memory planes, one for each video generator. Figure 7-27 shows the circuits for both planes. Each video memory plane is a 16K by 16-bit (32K byte) memory with a write control circuit. Both video memories are addressed by common address signals from the bit map video controller module. The write control circuits generate a memory high write (MHW) strobe and a memory low write (MLW) strobe by control signals it receives from the CTI BUS or the bit map video controller. Before these signals are generated, the write control circuit must be enabled by the Plane 2 and 3 control register (GSELD or RSELD) and the read-modify-write (RMW) signal. The operation of these video memory planes is similiar to the operation of the video memory on the bit map video controller.

7.3.2.6 Video Generators Circuit Operation – The extended bit map contains two video generator circuits, one for each video memory plane. Figure 7-28 shows the circuits for both pairs of circuits. These circuits generate MONO VIDEO signals which electrically connect to the MONO VIDEO signal generated by the bit map video controller. These circuits also generate composite GREEN VIDEO and RED VIDEO signals.

Each circuit receives common clocks, select, and synchronization signals from the bit map video controller module. Each circuit also receives its own data (RMD0 for red and GMD0 for green) from its video memory plane and separate resolution select signals (RR1 – RR0 for red and GR1 – GR0 for green).

The operation of these video generators is similar to the video generator described in Section 7.3.1.8. The only difference is each of these video generators contain a single video sync buffer that is used for both mapped and nonmapped applications.

NOTE

The SYNC signal, which is amplified by the plane 1 video generator when the extended bit map module is not in the video subsystem, is switched to the plane 2 video generator on the extended bit map for amplification. It appears on the GREEN VIDEO line and MONO VIDEO line when the extended bit map is in the system.

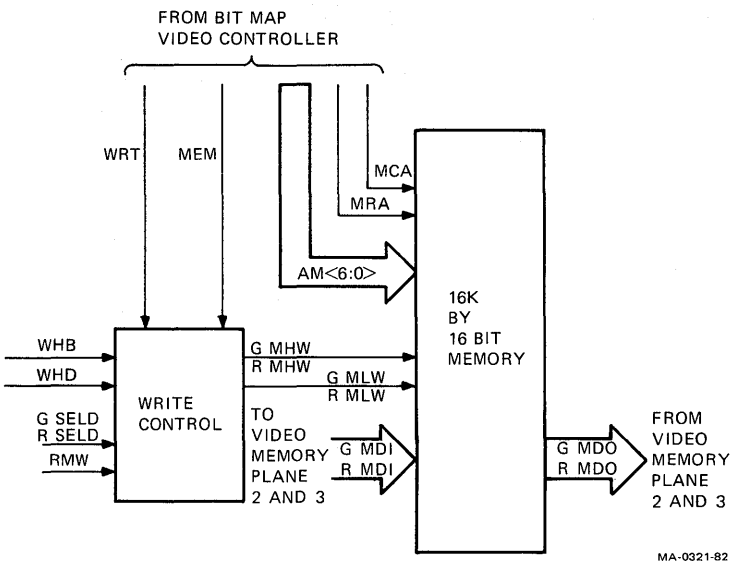
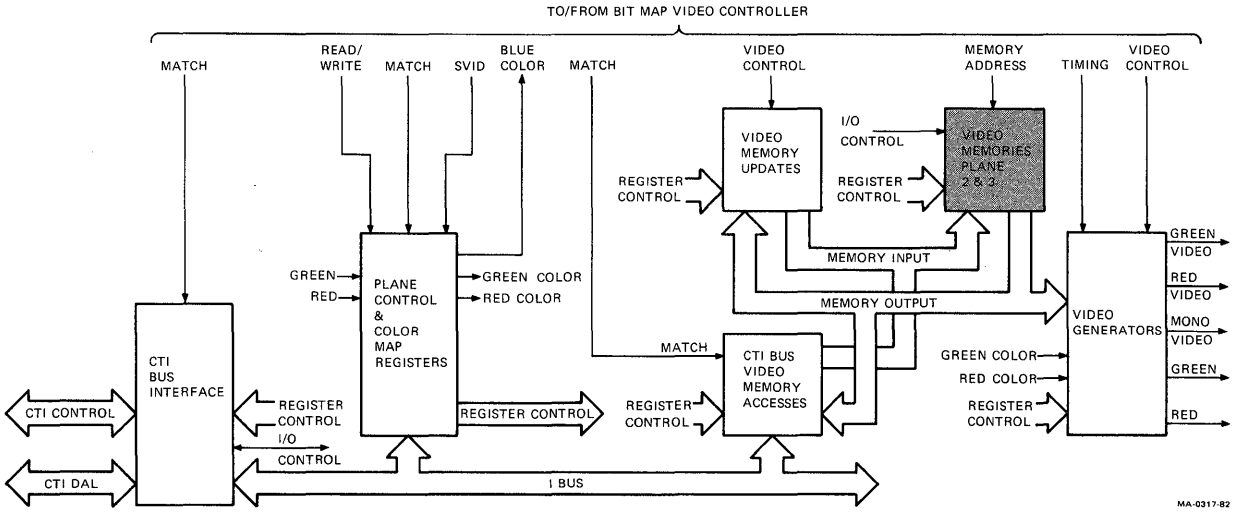


Figure 7-27 Video Memory (Plane 2 and 3) Circuit Operation (Option Module)



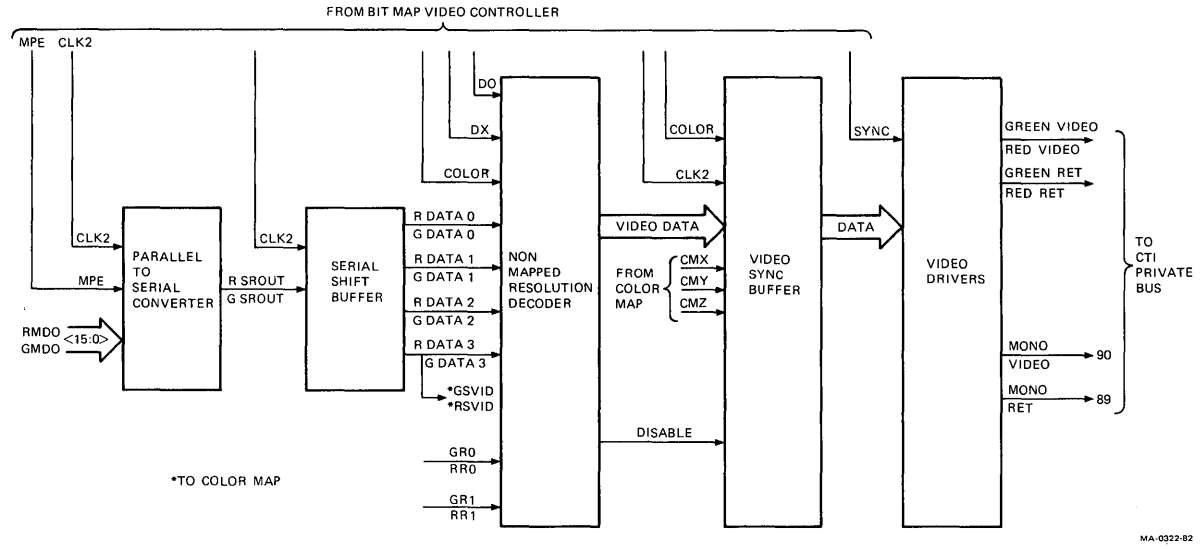
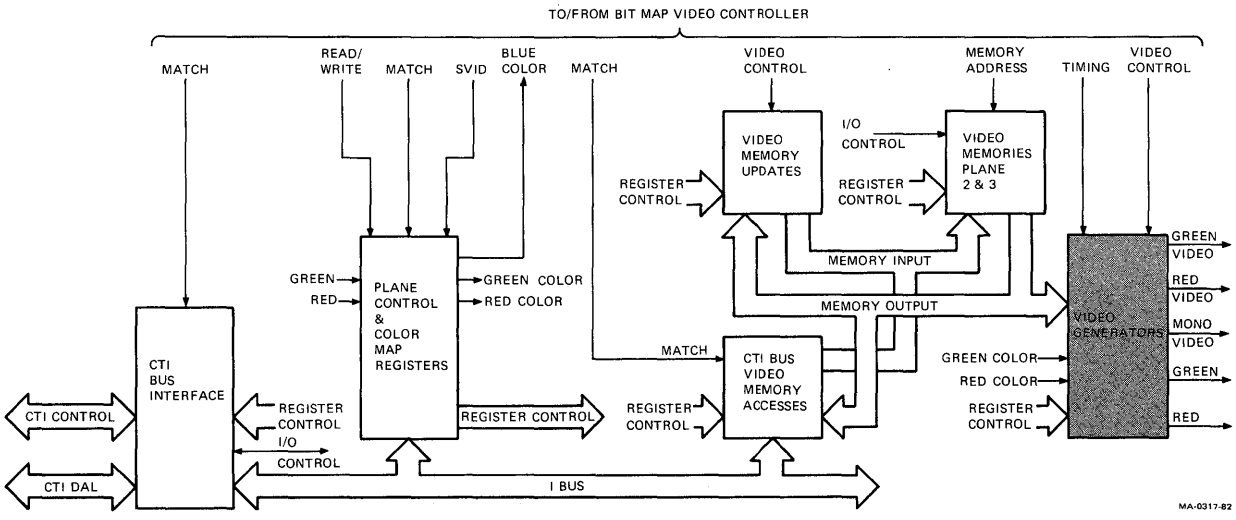


Figure 7-28 Video Generator Operation (Option Module)



7.4 DETAILED CONNECTOR DESCRIPTIONS

The following section describes the connectors of the bit map video controller and extended bit map modules. The pins on the connectors are described as either inputs or outputs of each module.

7.4.1 CTI BUS Interface J1

The bit map video controller and extended bit map modules use the data/address and control lines of the CTI BUS to implement program data transfers. Figure 7-29 shows the pin functions and signal directions of this connector (for details see Chapter 5).

7.4.2 Drive Interface Connector J2

Table 7-7 lists the pin functions of the bit map video controller and extended bit map modules J2 connector shown in Figure 7-29. this connector allows direct communication between the bit map video controller and extended bit map modules.

The signal mnemonic column describes the asserted state of the signal. An L after the mnemonic indicates an asserted low state (logic zero). An H after the signal name indicates an asserted high state (logic high).

7.4.2.1 NOMEM H Signal – The extended bit map module generates this signal. When asserted, it indicates that either plane 2 or 3 video memories is selected. A video memory plane must be selected before host processor or data modification assesses. To set the appropiate select bits, refer to the plane control register definitions in Section 7.5.

7.4.2.2 COLOR H Signal – The bit map video controller generates this signal. When asserted, it indicates that the color map is enabled.

7.4.2.3 BSELD L Signal – The bit map video controller generates this signal. When asserted, it indicates that the plane 1 video memory is enabled. If the plane 1 video memory is enabled for accesses then accesses, to plane 2 and 3 video memories are disabled.

7.4.2.4 WR12 H Signal – The bit map video controller generates this signal. It is a write strobe signal for the color map register during host processor accesses.

7.4.2.5 RD10 H Signal – The bit map video controller generates this signal. It is a read strobe signal for the plane 2 and 3 control register during host processor accesses.

7.4.2.6 WR10 H Signal – The bit map video controller generates this signal. It is a write strobe signal for the plane 2 and 3 control register during host processor accesses.

7.4.2.7 DX H Signal – The bit map video controller generates this signal. It is a 5 MHz Clock with a 25% duty cycle used during high resolution (quad-bit) applications.

7.4.2.8 D0 H Signal – The bit map video controller generates this signal. It is a 10 MHz Clock with a 50% duty cycle used during medium resolution (dual-bit) applications.

7.4.2.9 CM1 and CM0 Signals – The extended bit map generates these signals. When the subsystem operates in the mapped mode, the color map provides these signals to generate a BLUE VIDEO signal on the bit map video controller.

7.4.2.10 PAT H Signal – The bit map video controller generates this signal. It is a pattern signal used during video memory update modification cycles.

7.4.2.11 X3 H, X2 H, X1/PRESET H, and X0/CLOCK H Signals – The bit map video controller generates these signals. During bit mode operations for a video memory update modification cycle, these bits specify the bit within the designated word to modify. During word mode operations for a video memory update modification cycle, these bits control shift operations to be performed on the video memory data.

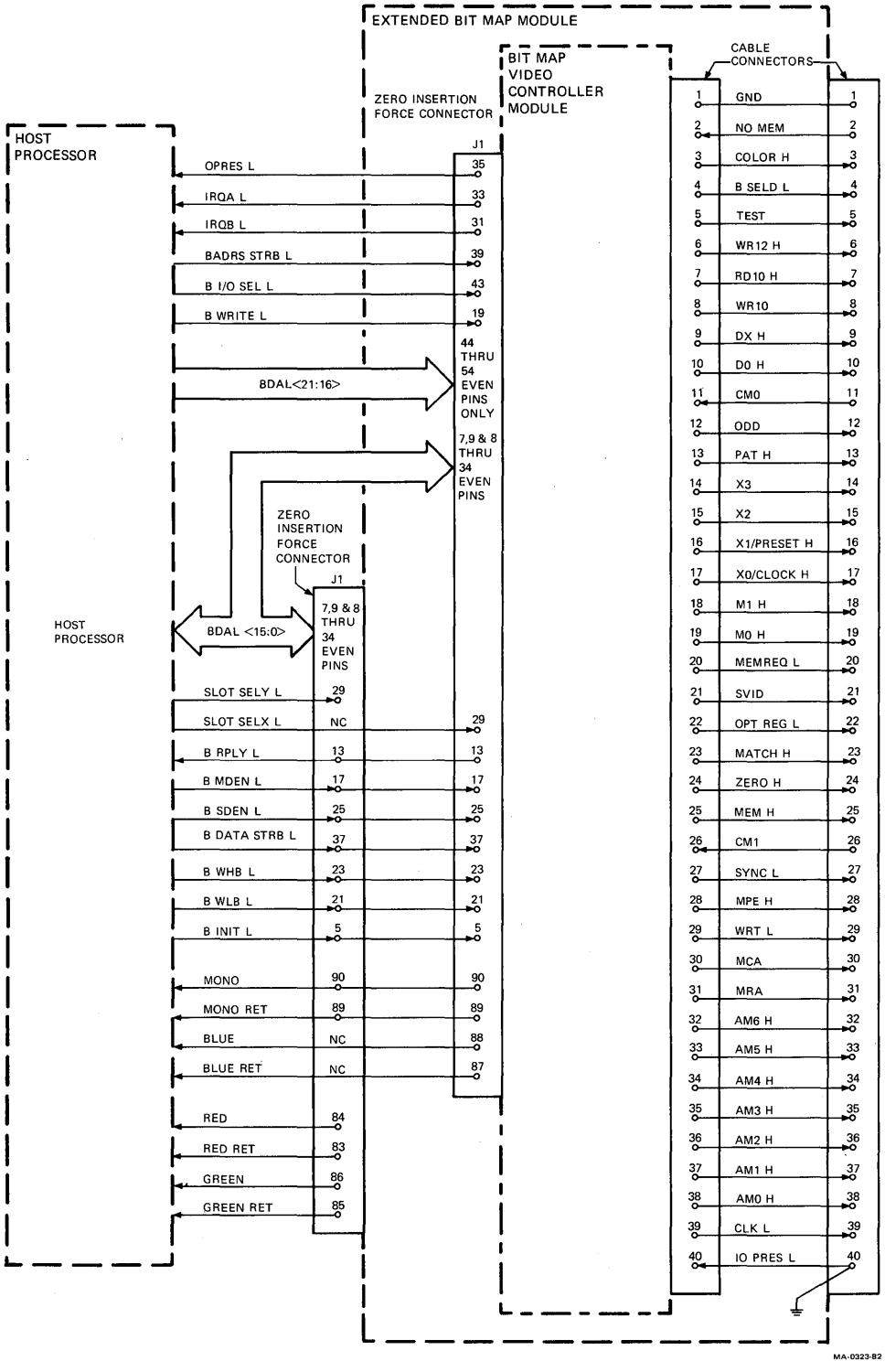


Figure 7-29 Bit Map Video Controller and Extended Bit Map Modules I/O Signal Flow

Table 7-7 Connector J2 Pin Description

Pin	Signal Meaning	Signal Mnemonic
1	Ground	
2	No memory	NOMEM H
3	Enable color map	COLOR H
4	Plane 1 selected	BSELD L
5	–	not used
6	Color map write strobe	WR12 H
7	Plane register read strobe	RD10 H
8	Plane register write strobe	WR10 H
9	5 MHz 25% duty clock	DX H
10	10 MHz clock	D0 H
11	Color map data	CM1
12	–	not used
13	Pattern	PAT H
14	Data modification bit	X3 H
15	Data modification bit	X2 H
16	Data modification bit	X1/PRESET H
17	Data modification bit	X0/CLOCK H
18	Data modification bit	M1 H
19	Data modification bit	M0 H
20	Host memory request	MEMREQ L
21	Plane 1 serial data	SVID
22	EBO register access	OPTREG L
23	Video memory access	MATCH H
24	Counter empty	ZERO H
25	Video memory enable	MEM H
26	Color map data	CM0
27	Video syncronization	SYNC L
28	Memory parallel enable	MPE H
29	Data modification write	WRT L
30	Memory column address	MCA
31	Memory row address	MRA
32	Memory address bit	AM6 H
33	Memory address bit	AM5 H
34	Memory address bit	AM4 H
35	Memory address bit	AM3 H
36	Memory address bit	AM2 H
37	Memory address bit	AM1 H
38	Memory address bit	AM0 H
39	20 MHz clock	CLK L
40	EBO present	IOPRES L

7.4.2.12 M1 H and M0 H Signals – The bit map video controller generates these signals. During video memory update modification cycles, these bits specify the bit or word mode operation to be performed.

7.4.2.13 MEMREQ L Signal – The bit map video controller generates this signal. It is a host processor to video memory access indicator signal that enables video memory output to the CTI BUS.

7.4.2.14 SVID Signal – The bit map video controller generates this signal. When the subsystem operates in the mapped mode, this plane 1 video memory serial data addresses the color map to generate the CM1 and CM0 signals during screen refresh cycles.

7.4.2.15 OPTREG L Signal – The bit map video controller generates this signal. It is a host processor to extended bit map register access enable indicator signal.

7.4.2.16 MATCH H Signal – The bit map video controller generates this signal. It is a host processor to video memory access indicator signal that enables circuits to process video memory accesses to plane 2 and 3 video memories.

7.4.2.17 ZERO H Signal – The bit map video controller generates this signal. It is a counter register empty indicator signal.

7.4.2.18 MEM H Signal – The bit map video controller generates this signal. It is a host processor to video memory access indicator signal to enable the video memory.

7.4.2.19 SYNC L Signal – The bit map video controller generates this signal. It is a video synchronization signal which contains the horizontal, vertical, and equalization pulses needed to generate a composite video signal.

7.4.2.20 MPE H Signal – The bit map video controller generates this signal. It is a memory parallel enable signal used during screen refresh cycles.

7.4.2.21 WRT L Signal – The bit map video controller generates this signal. It is a data modification write strobe used during video memory update modification cycles.

7.4.2.22 MCA Signal – The bit map video controller generates this signal. It is a video memory column address strobe used during all video memory access cycles.

7.4.2.23 MRA Signal – The bit map video controller generates this signal. It is a video memory row address strobe used during all video memory access cycles.

7.4.2.24 AM6 H Through AM0 H Signals – The bit map video controller generates these signals. They are the address bits for the video memory and are used with the MCA and MRA signals.

7.4.2.25 CLK L Signal – The bit map video controller generates this signal. It is a 20 MHz clock signal for the extended bit map module.

7.4.2.26 IOPRES L Signal – The extended bit map module generates this signal. If the cable is connected between the modules, this signal is generated. It indicates the presence of the extended bit map module.

7.5 PROGRAMMING

The following section describes the bit map video controller and extended bit map modules programming registers. These registers are the host processors access to the subsystems video processing commands.

The bit map video controller module contains nine 16-bit registers to allow the host processor access to commands and status data of the controller. The extended bit map module contains additional registers to control its operations: a plane control register and a color map register. Access to all registers is done by accessing the CTI BUS register space of the bit map video controller module.

The bit map video controller module can be installed in any one of the six slots in the CTI BUS card cage. The starting address of the register address space (XXXXXX) depends on the card cage slot the module is installed in. Refer to Chapter 5 for assigned slot addresses and their address ranges.

Table 7-8 defines the 11 registers of the bit map video controller and the extended bit map modules. The plane 2 and 3 control register (OPC) and the color map register (CMP) are located on the extended bit map module and are accessible only when the optional module is installed.

NOTE

The register address XXXXXX02, is used only for CTI BUS protocol and is not recognized by the bit map video controller.

The control status register (XXXXXX04) is the only register on the bit map video controller that is byte addressable, all other registers are word addressable.

These registers also control the interrupts the bit map video controller sends to the host processor. These interrupts are controlled via the control and status register. An end of frame interrupt controls CTI interrupt line IRQA if the interrupt is enabled. A transfer done interrupt controls CTI interrupt line IRQB if the interrupt is enabled.

Registers should not be loaded unless the transfer done bit (CSR bit 15) is set. However, the X and Y registers are an exception. They may be loaded during an operation without affecting that operation.

Table 7-8 Bit Map Video Controller Programming Registers

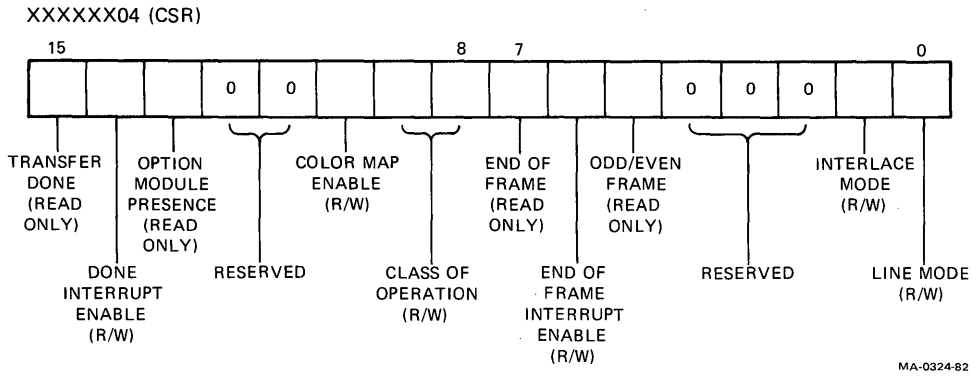
Address	Mnemonic	Function	Type
XXXXXX00	IDR	Identification code	Read only
XXXXXX02	–	Reserved	
XXXXXX04	CSR	Control status	Read/write
XXXXXX06	P1C	Plane 1 control	Read/write
XXXXXX10	OPC	Plane 2 and 3 control	Read/write
XXXXXX12	CMP	Color map	Write only
XXXXXX14	SCL	Scroll register	Read/write
XXXXXX16	X	X coordinate	Read/write
XXXXXX20	Y	Y coordinate	Read/write
XXXXXX22	CNT	Counter	Write only
XXXXXX24	PAT	Pattern	Write only
XXXXXX26	MBR	Memory base	Write only

7.5.1 Identification Code Register (IDR)

The host processor uses this register to identify the module for software routine selection. When read by the host processor, this register returns an identification value of 1002 (octal).

7.5.2 Control Status Register (CSR)

This register controls the general operation and video timing of the bit map video controller and the extended bit map module. The following is the bit organization of this register.



7.5.2.1 Bit 0 / Line Mode Definition – When this bit is reset (0), 525 line mode operation is selected (526 line for noninterlaced). When this bit is set (1), 625 line mode operation is selected (626 line for noninterlaced). This bit is reset during initialization.

7.5.2.2 Bit 1 / Interlace Mode Definition – When this bit is reset (0), a noninterlaced operation mode is selected. When this bit is set (1), an interlaced operation mode is selected. This bit is reset during initialization.

7.5.2.3 Bit 5 / Odd/Even Frame Definition – This bit indicates when the subsystem scans the odd lines (bit reset) or the even lines (bit set).

7.5.2.4 Bit 6 / End of Frame Interrupt Enable Definition – When this bit is reset (0), the end of frame interrupt to the host processor is disabled. When this bit is set (1), the end of frame interrupt is generated (IRQA) to the host processor when bit 7 goes set.

7.5.2.5 Bit 7 / End of Frame Definition – When this bit is set (1), the video subsystem performs a vertical retrace. The host processor can update the video memory without generating displayed distortion.

7.5.2.6 Bits 8 and 9 / Operation Class Definition – These bits select the bit and word mode operations the subsystem performs during update modifications to the video memory. The following are the bits and word mode selected operations.

Bits 9	Bits 8	Selected Operation
0	0	Bit transfers shifted left to right
0	1	Bit transfers shifted top to bottom
1	0	Word transfers shifted left to right
1	1	Word transfers shifted right to left

7.5.2.7 Bit 10 / Color Map Enable Definition – When this bit is reset (0), the color map is disabled and the video subsystem operates in the nonmapped mode. When this bit is set (1), the color map is enabled and the subsystem operates in the mapped mode.

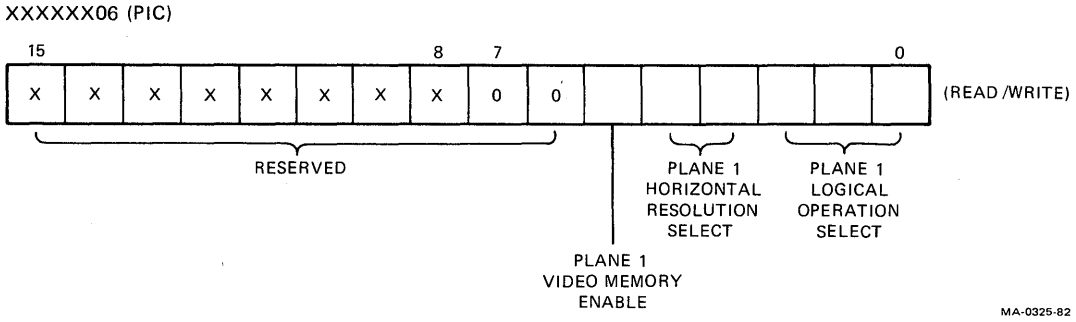
7.5.2.8 Bit 13 / Option Presence Definition – When this bit is reset (0), the extended bit map is present and connected to the bit map video controller. When this bit is set (1), the extended bit map is not present.

7.5.2.9 Bit 14 / Done Interrupt Enable Definition – When this bit is reset (0), the transfer done interrupt to the host processor is disabled. When this bit is set (1), the transfer done interrupt is (IRQB) generated to the host processor when bit 15 goes set.

7.5.2.10 Bit 15 / Transfer Done Definition – When this bit is set, the last host processor commanded transfer is complete (counter register equals 0) and any register may be accessed.

7.5.3 Plane 1 Control Register (P1C)

This register defines a logical operation (update modification) to be performed on the plane 1 video memory. If the subsystem is operating in the nonmapped mode, it selects the resolution mode. This register also enables the plane 1 video memory for logical operations and host processor accesses. The following are the bit definitions for this register.



NOTE
If the color map is enabled (CSR bit 10), the bit map video controller ignores this registers resolution bits (P1C bits 3 and 4) and sets the resolution to 1024.

7.5.3.1 Bits 2, 1, 0 / Plane 1 Logical Operation Select Definition – These bits select the logical operation to be performed on data stored in the plane 1 video memory. Since the CSR bits 8 and 9 select bit or word update modification modes, these bits define the logical operation for either mode. Table 7-9 defines the selected update modification for bit mode operations. Table 7-10 defines the selected update modification for word mode operations.

During bit mode logical operations 1–5, the pattern register is rotated. This is a bit-by-bit rotation of the pattern register starting with the least significant bit. Logic operations 6 and 7 do not use the pattern register.

Table 7-9 Bit Mode Logical Operations

Bits 2	1	0	Selected Operation
0	0	0	No operation
0	0	1	XOR pattern register and screen contents to screen.
0	1	0	Move pattern register to screen
0	1	1	Move complement of pattern register to screen
1	0	0	Bit set pattern to screen
1	0	1	Bit clear pattern to screen
1	1	0	Clear current bit on screen
1	1	1	Set current bit on screen

Table 7-10 Word Mode Logical Operations

Bits 2	1	0	Selected Operation
0	0	0	No operation
0	0	1	Complement screen
0	1	0	Move pattern register to screen
0	1	1	Move pattern complement to screen
1	0	0	(reserved)
1	0	1	Shift screen 1 bit (see CSR for shift direction)
1	1	0	Shift screen 2 bits (see CSR for shift direction)
1	1	1	Shift screen 4 bits (see CSR for shift direction)

Word mode logical operations use only the least significant bit of the pattern register. The pattern register does not rotate in word mode.

The shift screen operation shifts all bits in the words specified by the counter register either left or right. Bits shifted from the last word of each scan line are lost. The incoming bits are from the least significant bit of the pattern register.

7.5.3.2 Bits 4, 3 / Plane 1 Horizontal Resolution Select Definition – These bits select the horizontal resolution the plane 1 video generator operates in if the video subsystem is operating in the nonmapped mode. During an initialization these bits are reset (0) to select 1024 single bit resolution. These resolutions are selected as follows.

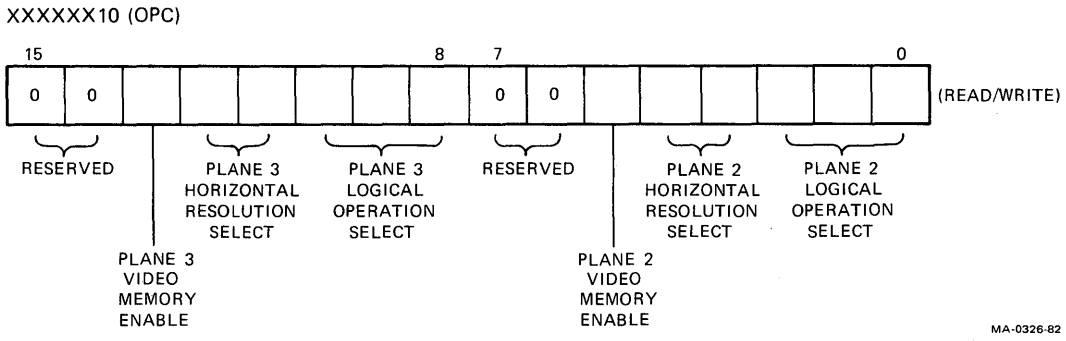
Bits 4	3	Selected Resolution
0	0	1024 single bit resolution (2 levels of intensity)
0	1	512 two bit resolution (4 levels of intensity)
1	0	256 four bit resolution (16 levels of intensity)
1	1	Display off (black)

7.5.3.3 Bit 5 / Plane 1 Video Memory Enable Definition – When this bit is set the host processor can perform write, read, or read-modify-write operations to the plane 1 video memory. When this bit resets all host processor accesses and video memory update modifications to the plane 1 video memory are inhibited.

During host processor accesses, write operations occur to all planes that have the video memory enable bit set (also see OPC register), read operations occur from the first video memory that has the video memory enable bit set starting with plane 1 and ending with plane 3. If no video memory plane is enabled, the host processor cannot read and times out.

7.5.4 Plane 2 and 3 Control Register (OPC)

This register defines a logical operation (update modification) to be performed on plane 2 and plane 3 video memories, selects the resolution mode for each plane if the subsystem operates in nonmapped mode, and enables the plane 2 and plane 3 video memories for logical operations and host processor accesses. This register is on the extended bit map module and is accessible when the option presence bit in the CSR is reset. The following are the bit definitions for this register.



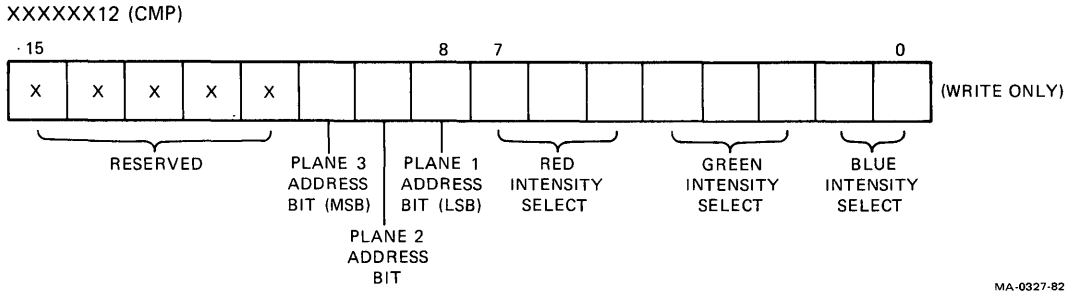
NOTE

If the color map is enabled (CSR bit 10), the bit map video controller ignores resolution bits (OPC bits 3, 4, 11, and 12) and sets the resolution to 1024.

The bit definitions for these register bits are identical to the P1C register except this register controls the plane 2 and plane 3 video memories.

7.5.5 Color Map Register (CMP)

The color map register allows for programming of the color map when the video subsystem operates in the mapped mode. This register contains eight locations, each of which holds eight bits of data. The low byte of this register defines the color intensity each video generator produces. Three bits of the high byte define the address of one of the eight words of the color map register. This is also the address formed from the combined serial outputs of the video memory planes. The RED and GREEN VIDEO signals allow for seven intensity levels. The BLUE VIDEO signal has four intensity levels, however they are in the same range as the red and green. The mono output always contains the sum of all the intensity levels (Section 7.3.1.8). The following is the bit organization of this register.

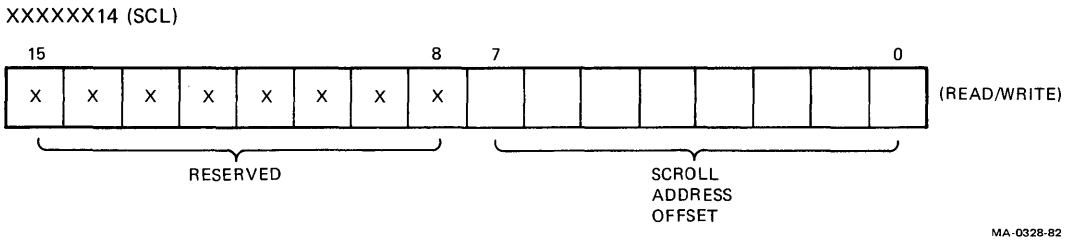


7.5.6 Scroll Register (SCL)

The scroll register controls the addressing of the video memory planes for all operations. This register's contents are always added to the Y coordinate addresses when writing and reading to the bit map. Changing the contents causes a vertical scroll on the screen (increment scrolls up; decrement scrolls down).

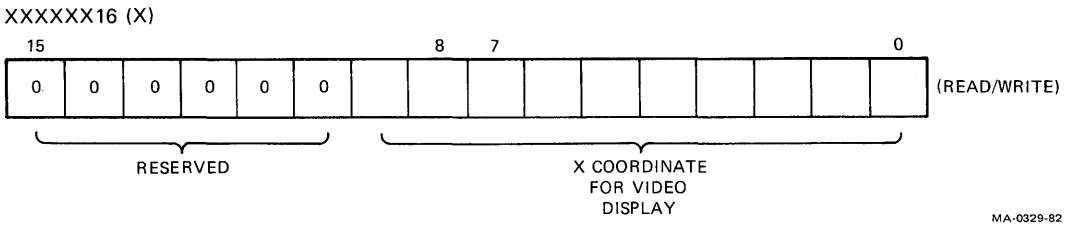
Operations with the scroll register can be absolute. However, the scroll register may have any value when a program starts. Therefore, the register contents must be incremented/decremented or added to/subtracted from.

After writing to the screen, the data is moved up or down by changing the scroll register contents. The following are the bit definitions of the scroll register.

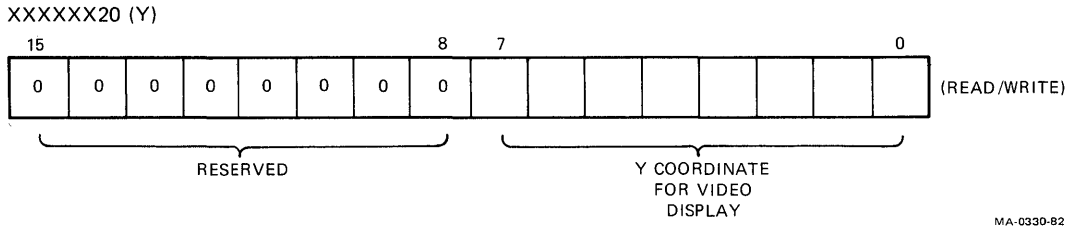


7.5.7 X and Y Registers (X) (Y)

The X register holds the horizontal scan location of all transfers to the video memory planes. It can be modified at any time during an operation with no effect on the operation. For word mode applications, the lower four bits of X register are ignored (bit within the word). For word mode shift right to left operations, the X register defines the coordinate of the rightmost word on the top line to be shifted. For word mode shift left to right operations, the X register defines the coordinate of the leftmost word. The following is the bit organization for this register.



The Y register holds the starting screen location of all video operations defined in the P1C or OPC registers to the video memory planes. It can be modified at any time during the operation with no effect on the operation. For 60 Hz operation, the row of words with Y coordinates 239 is always the bottom visible scan line. For 50 Hz operation, the row of words with Y coordinates 255 is the bottom scan line. The register contents are offset as described in the scroll register definition. The following are the bit definitions for this register.

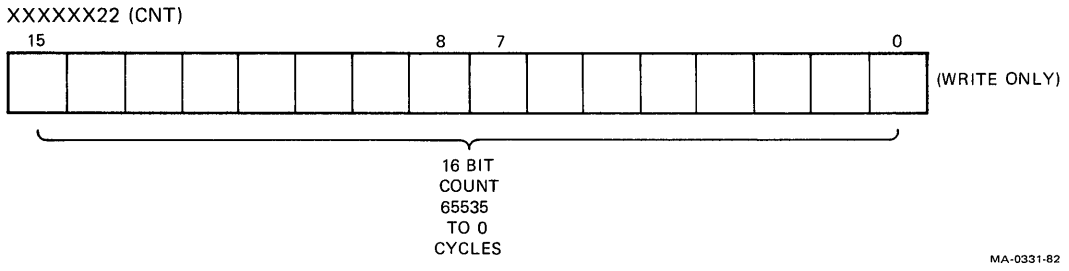


NOTE

Only 240 of the 256 available Y lines are visible at any time in 60 Hz mode.

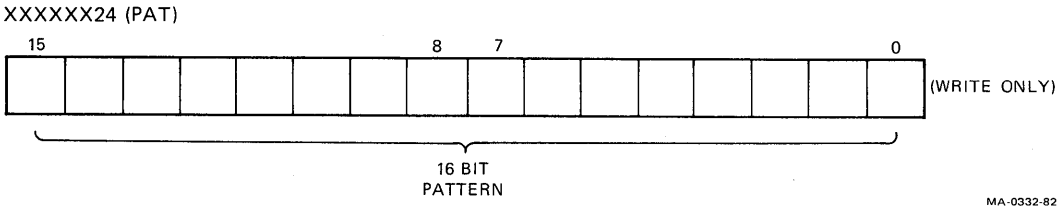
7.5.8 Counter Register (CNT)

When this register is loaded with anything but a zero, a transfer is started. The counter decrements after each cycle (bit or word) until the counter is zero. When zero, the counter is stopped and the transfer done bit (CSR bit 15) is set. If the interrupt is enabled, an interrupt is generated to the host processor. The counter can only be loaded if the transfer done bit is set. Loading the counter register clears the done bit. The following is the bit definition for this register.



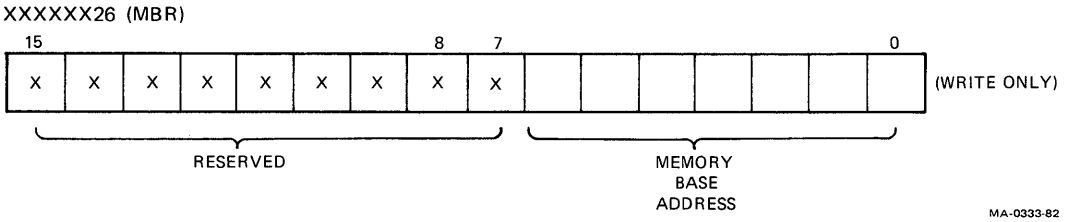
7.5.9 Pattern Register (PAT)

During a transfer, the least significant bit of this register can be used as data during an update modification cycle for each plane. After each cycle in bit mode (see CSR bits 8 and 9), the pattern register contents are rotated right one bit. For example, bit 0 shifts to 15, 1 to 0, 2 to 1, etc. In word mode, only the least significant bit of the pattern register is used, the upper 15 bits are ignored. The pattern register can only be loaded if the done bit (CSR bit 15) is set (the counter register is zero). The following are the bit definitions for this register.



7.5.10 Memory Base Register (MBR)

This register assigns the starting address of the 16K video memories page that the bit map video controller responds to. The starting addresses, as they appear on the CTI BUS, are on any 16K word boundary. The register contents are then compared to the CTI Bus DAL lines <21:15> respectively. The following are the bit definitions for this register.



7.6 SPECIFICATIONS

The following list contains the specifications for the bit map video controller module. Software for self-testing is not resident on the video controller. Any self-test to be used must be resident on some external device. No power-up testing is performed.

Item	Power
Bit map video controller	+5 Vdc ± 5% @ 3.3 A +12 Vdc ± 5% @ 55 mA
Extended bit map	+5 Vdc ± 5% @ 2.75 A +12 Vdc ± 5% @ 45 mA
Power Sequencing	No specific sequence is required for operation on this module.
Physical Dimensions (either module)	
Width	13.0 cm (5.2 in)
Length	30.0 cm (12 in)
Depth	1.5 cm (0.6 in)

Display Characteristics

The video subsystem is program selectable via the COMMAND/STATUS register (CSR) for 50 or 60 Hz operation and a variety of video timing characteristics.

Display	
Pixels/scan	256
Pixel rate	5 MHz
Pixel period	200 ns
Display	
Pixels/scan	512
Pixel rate	10 MHz
Pixel period	100 ns
Display	
Pixels/scan	1024
Pixel rate	20 MHz
Pixel period	50 ns

Horizontal Frequency	15625 Hz
Vertical Timing	The vertical timing is set to 60 Hz non-interlaced at power-up. 60 Hz non-interlaced/59.411 Hz 526 scan lines 240 displayed lines/page 60 Hz interlaced/59.524 Hz 525 scan lines 240 displayed lines/page 50 Hz non-interlaced/49.920 Hz 626 scan lines 256 displayed lines/frame 50 Hz interlaced/50.000 Hz 625 scan lines 256 displayed lines/frame

CHAPTER 8
MONOCHROME MONITOR

8.1 GENERAL

This chapter describes the VR201 monochrome monitor shown as the shaded part of the system functional block diagram in Figure 8-1.

The VR201 monochrome monitor is a raster scan device for displaying alphanumeric/graphic video information. It monitors the video display. However, the type of display presented is dependent on the video input to the monitor from the system box. This is determined by the operator and system software.

8.1.1 Related Documentation

Refer to the following related documentation while reading this chapter.

Title	Document No.
KEF11 Field Maintenance Print Set	MP-01473-00
VR201 Monochrome Monitor Field Maintenance Print Set	MP-01410-00

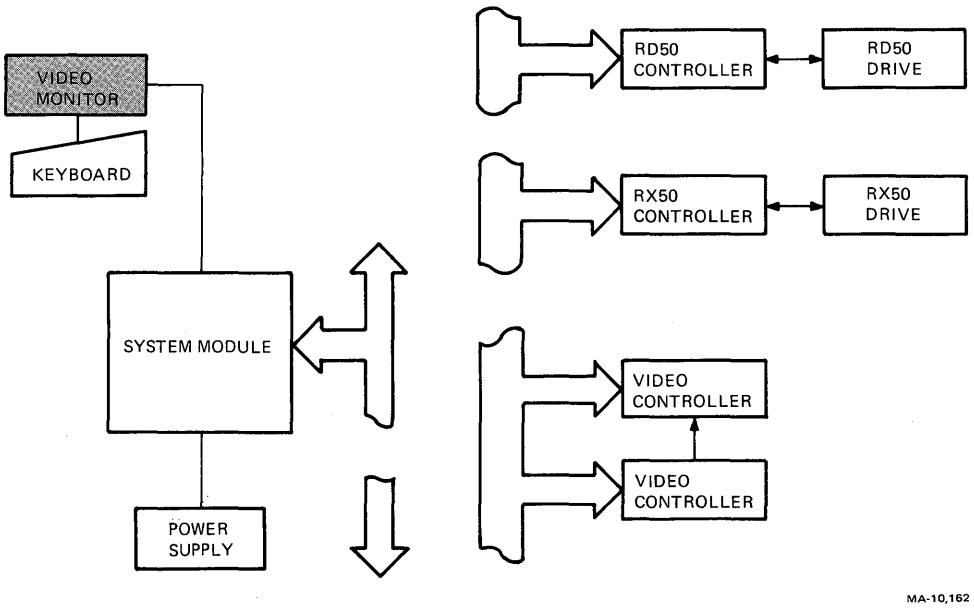


Figure 8-1 System Block Diagram

8.2 PHYSICAL DESCRIPTION

The VR201 monochrome monitor is enclosed in a wedge-shaped cabinet. The CRT face provides a viewing area of 12.7 × 20.3 cm (5 × 8 inches) on a screen that measures 30.5 cm (12 inches) diagonally. A plastic button covers a screw on the cabinet rear. This screw holds the cabinet to the internal wire frame. The CRT and the monochrome monitor module are mounted inside this frame.

The frame has metal finger stock that presses against the screw mounting bracket and a metal shield. To prevent electromagnetic radiation, this shield covers the entire inside of the cabinet. There is a folding carrying handle on the bottom rear of the cabinet.

The glass front of the monitor, the CRT face, is coated with a special treatment to reduce glare to the operator.

The monitor viewing angle is adjustable between +5 to −25 degrees. To adjust the angle, the operator pushes a release on the right side (Figure 8-2). This causes a friction-lock foot to drop down from the bottom of the cabinet housing.

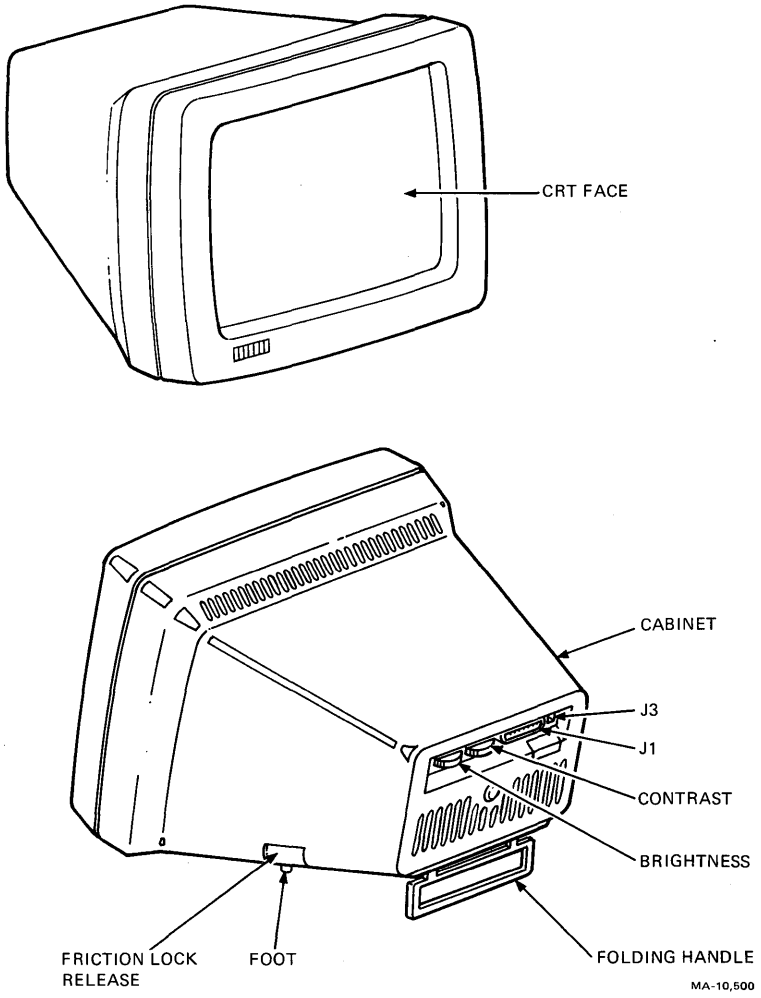


Figure 8-2 Monochrome Monitor Exterior View

The contrast and brightness controls are on the rear panel. There are also two connectors on the rear of the monitor: J1 and J3. J1 is a 15 pin D-type connector that connects to the system box with a cable (PN BCC02) and J3 is a modular telephone jack that connects to the keyboard with another cable (PN BCC02).

The following are the physical dimensions for the monochrome monitor.

Height	24.38 cm (9.75 in)
Width	29.33 cm (11.73 in)
Depth	30.57 cm (12.23 in)
Weight	6.6 kg (14.5 lb)

8.3 FUNCTIONAL OVERVIEW

The VR201 monochrome monitor consists of two main components: a 12-inch diagonal CRT with a yoke assembly mounted on it and an electronics module (Figure 8-3).

Display activity is the primary function of the monitor. A secondary function is to route information between the system box and the keyboard. The keyboard connects with the monitor via J3 (Figure 8-3). J3 is hardwired on the module to J1, which connects to the system box.

The monitor module controls the CRT and the yoke assembly. A composite video signal is input to the module from the system box (Figure 8-3). This signal consists of two types of information: video data (Section 8.3.1), and sync data (Section 8.3.2).

The monitor module provides the following power to the CRT.

- Anode voltage
- Grid 1 voltage (brightness)
- Grid 2 voltage (cutoff)
- Grid 4 voltage (focus)
- Heater voltage
- Cathode voltage

The control inputs to the CRT refine the electron beam. The anode voltage attracts the beam to the faceplate and provides a single connection between the CRT and the module (Figure 8-3). P1 provides all other CRT inputs. P1 is mounted directly on the CRT and is hardwired to the module. Refer to Section 8.7.7 for more information.

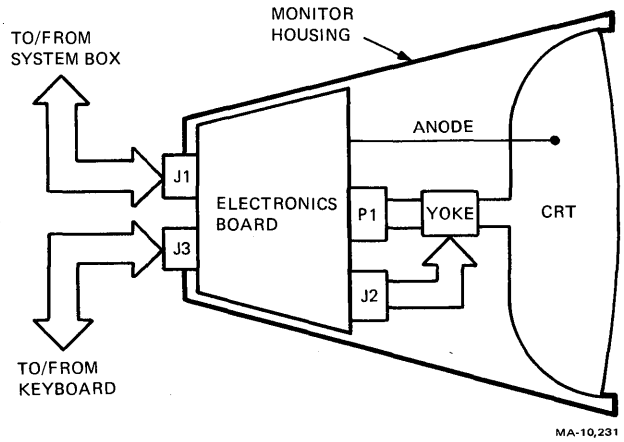


Figure 8-3 Monochrome Monitor Block Diagram

8.3.1 VIDEO Data

The monitor module uses the video portion of the signal to generate outputs to the CRT cathode. The CRT responds to the video by generating various intensities in the electron beam. The intensity of the beam is dependent on the amplitude of the video signal provided.

8.3.2 SYNC Data

The sync portion of the video synchronizes the generation of horizontal and vertical signals to the yoke assembly. The horizontal and vertical processor chips use peak detector circuits to separate the synchronizing signals. The yoke assembly, which connects to the electronics board via J2, consists of electromagnetic coils (Figure 8-3). These coils use the signals output by the module to generate magnetic fields which position the electron beam generated by the CRT. The horizontal signal to the yoke controls the sweep of the electron beam horizontally across the faceplate (each sweep is called a scan line). The vertical signal controls the positioning of the beam to a new scan line for vertical positioning.

8.4 MONOCHROME MONITOR SYSTEM COMMUNICATION

The monochrome monitor connects with both the system box and the keyboard. The system box connects to the monitor via J1, a 15-pin type D sub connector. The keyboard connects via J3, a modular telephone jack.

J1 has three basic functions: the supply of video input used only at the monitor, the supply of operational voltages used by both the monitor and the keyboard, and the transfer of keyboard data (Figure 8-4). The operational voltage and keyboard data lines are hardwired from J1 to J3 on the electronics board.

Table 8-1 provides a pin-out for J1 with signal identifications and functional descriptions. Table 8-2 provides the same information for J3.

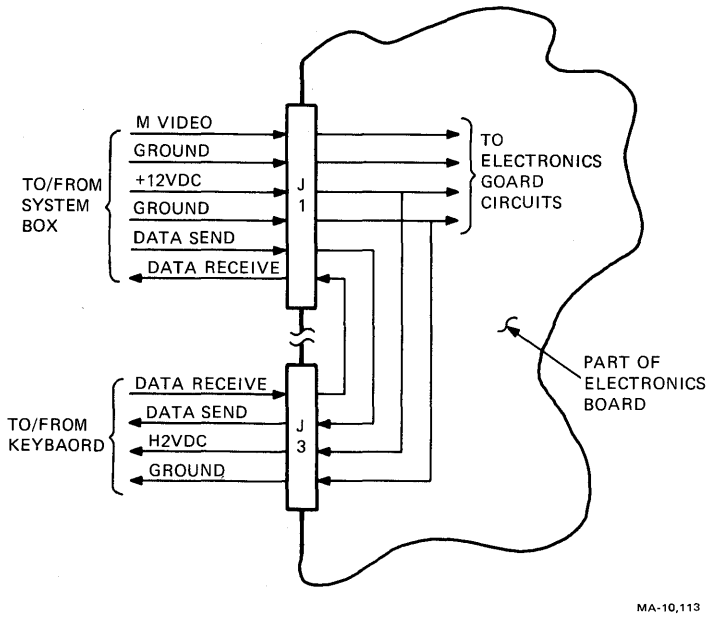


Figure 8-4 Monochrome Monitor System Communications Diagram

Table 8-1 J1 Pin-out

Pin(s)	Signal	Description
1-3	(Not used)	None
4	Ground	Video signal ground potential
5,6	Ground	Operational voltage ground potential
7,8	+12 Vdc	Operational voltage input
9-11	(Not used)	None
12	M Video	Composite video (refer to Section 8.3.1)
13	Ground	Tied to pins 5 and 6
14	Data Receive	Serial data line from the keyboard output to the system box (via J3)
15	Data Send	Serial data line from the system box output to the keyboard (via J3)

Table 8-2 J3 Pin-out

Pin	Signal	Description
1	Data Send	Serial data line for output from the system box to the keyboard (via J1, pin 15)
2	+12 Vdc	Output of operational voltage to the keyboard (from J1, pins 7 and 8)
3	Ground	Operational voltage ground potential (from J1, pins 5, 6 and 13)
4	Data Receive	Serial data line for input from the keyboard to the system box (via J1, pin 14)

8.4.1 Composite Video Signal

The video input to the monitor is a composite of two types of signals: video and sync. There are different levels of illumination within the video signal, ranging from totally black through maximum brightness.

Figure 8-5 represents a typical composite video signal and identifies the major terms associated with it. This signal, used with the monochrome monitor, is compatible with EIA RS170 standards. However, it is dc coupled to ground at the monitor module. Table 8-3 provides typical signal values.

Figure 8-6 shows the composite video signal and the sync portion of this signal. Table 8-4 describes the values for the sync components identified.

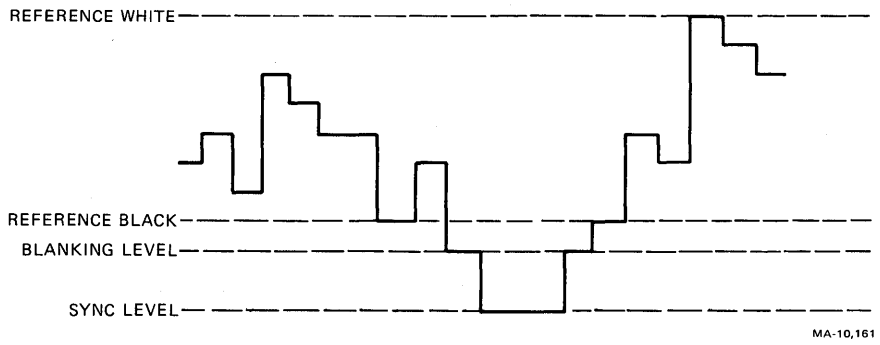


Figure 8-5 Composite Video Signal Representation

Table 8-3 Composite Video Values

Characteristics	Value
Output impedance	75 Ohms, dc coupled to 0 V
Amplitude	1.0 V peak-to-peak nom (the monitor accepts signals with peak-to-peak values of 0.9 V through 1.5 V)
Reference black	The low limit of display value. It equals 30% of the peak-to-peak value (0.3 V nom), and is the lowest voltage value to be amplified linearly at the electronics board
Reference white	The high limit of display value. It equals 100% of the peak-to-peak value (1.0 V nominal), and is the highest voltage value to be amplified linearly at the electronics board
Blanking level	Voltage value which reduces CRT electron beam current below cutoff
Sync level	Voltage level at which sync actions can take place; 0 V nom (dc coupled video to ground)
Continuous input	+2.0 V max (2.0 V saturates the video amplifier unless the contrast thumbwheel adjustment is reduced)

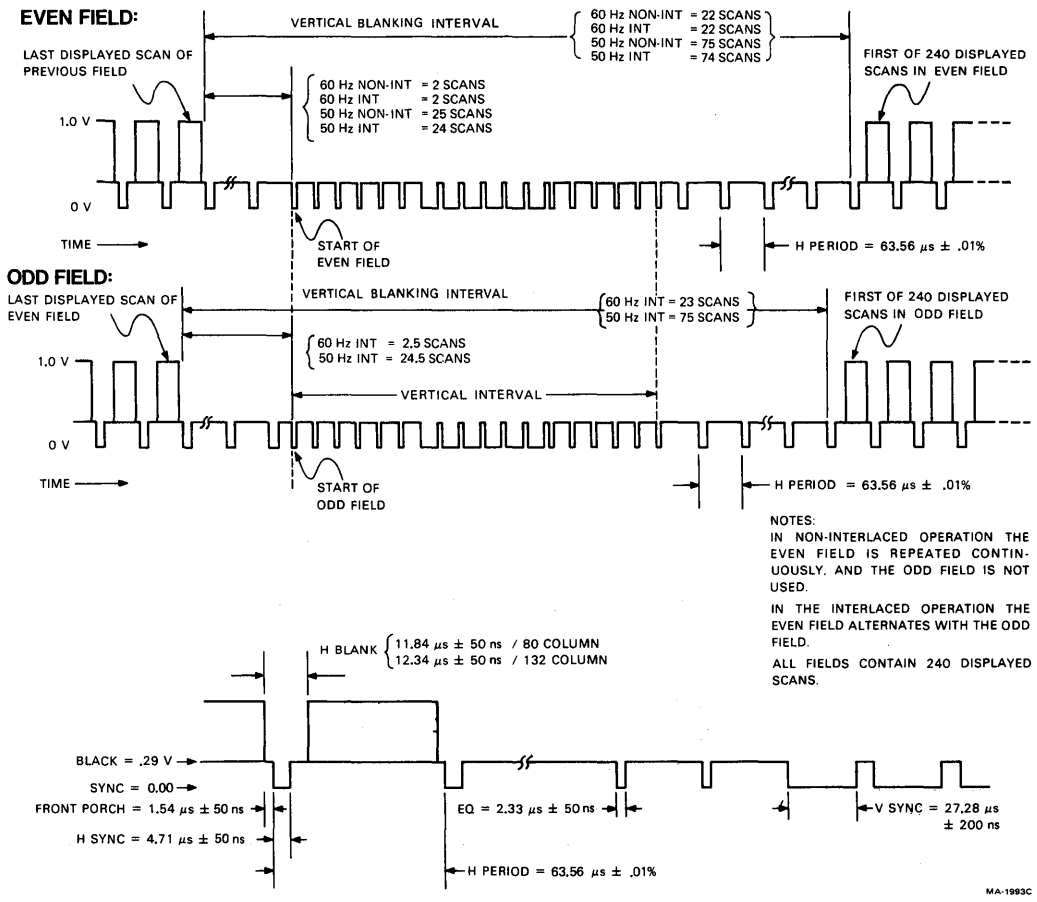


Figure 8-6 Composite Video Sync Timing Diagram

Table 8-4 Composite Video Sync Component

Component	Description
Vertical blanking interval	Period of time screen is blanked for vertical retrace activity. Vertical retrace is completed in less than 1.0 ms, and within an allowed frequency range of 49 – 61 times per second.
V Sync	Period of time in which vertical deflection circuitry on the electronics board is synchronized to the next frame.
H Sync	Period of time in which horizontal deflection circuitry on the electronics board is synchronized for retrace.
H Period	Period of time for the horizontal scan plus horizontal blanking (63.5 μs)
EQ	Equalizer pulse that synchronizes vertical deflection circuitry on electronics board for vertical retrace activity.
Front porch	Delay value between start of blanking and start of sync pulse.
Vertical interval	Period of time the actual synchronizing of the vertical deflection circuitry on the electronics board takes place. Consists of six EQ pulses, six V sync pulses, and six more EQ pulses.

8.5 CRT

The CRT provides the final video output, an electron beam, fired at a phosphor-coated faceplate.

The electron beam generation is controlled directly by the monitor module inputs. The module controls the yoke, which in turn controls positioning the beam at the faceplate.

The CRT contains an electron gun. The gun consists of the heater element, a cathode, three grids (G1, G2, and G4), an anode, and the faceplate, all encased in a vacuum.

The three grids control the beam generated by the gun: G1 for brightness, G2 for beam cutoff and G4 for focus.

G1 is directly affected by the brightness control thumbwheel. This enables the operator to adjust the background intensity of the display. G2 provides sharpening capabilities of the video. To do this, G2 acts as a gate or valve to the electron beam. A voltage, provided to G2, prevents the electron beam from passing to the faceplate unless the beam is of a specific minimum intensity. G4 focuses the electron beam.

The CRT plugs directly into P1 which is hardwired onto the module. Through P1, the operational voltages for the heater element, the cathode, and the three grids are provided. The anode voltage is provided by a separate connection between the module and the CRT. Its ground goes to the CRT case. This ground reduces shock hazard and consists of three parts: a connection between the module and a terminal block on the yoke, a connection between the block and the CRT case, and a connection between the block and P1.

8.6 YOKE

The yoke is a set of electromagnetic devices mounted on the neck of the CRT. One device is for horizontal deflection of the electron beam, the other is for vertical deflection.

Currents to control the horizontal scan line are applied to the yoke's coil (inductance) through the width inductor and the linearity inductor. The vertical trace control current comes from the vertical processor chip.

The yoke connects to the electronics board through J2: pins 2 and 3 for the horizontal deflection magnetic coils, pins 1 and 4 for the vertical.

8.7 MONITOR MODULE

The monitor module is made of discrete analog components. It can be divided into seven circuits to control the CRT and yoke.

Figure 8-7 is a block diagram of the module showing the seven circuits. The figure also identifies the fuse for the power input (F1), and three connectors (a fourth connector, J3, which routes signals between J1 and the keyboard is not shown). Descriptions of each of the items identified in Figure 8-7 are provided in the following paragraphs.

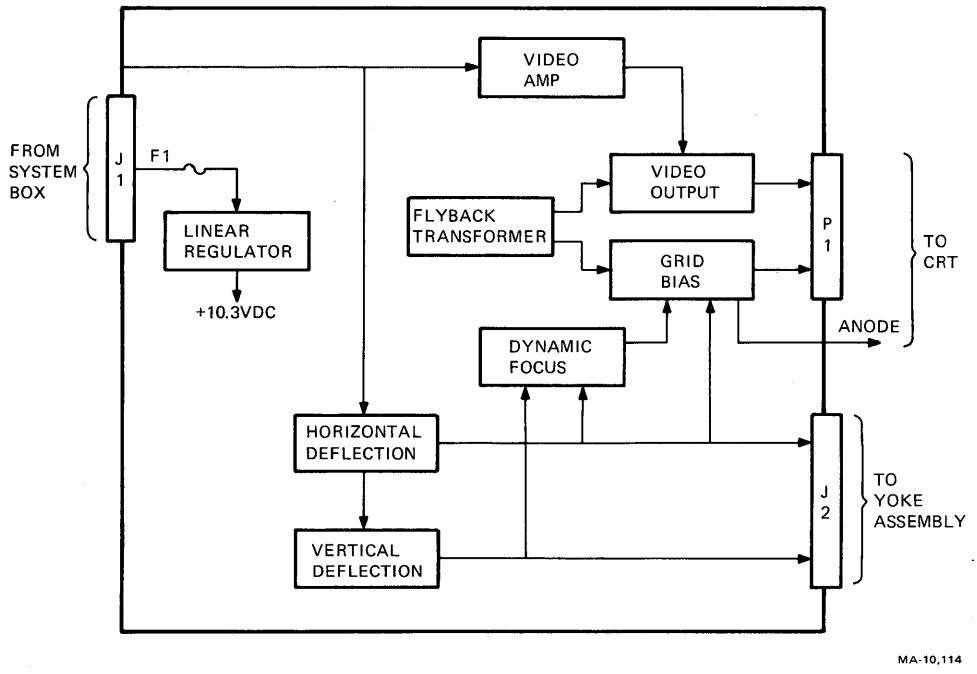


Figure 8-7 Monitor Module Block Diagram

8.7.1 Dynamic Focus

This circuit creates different focus voltages for different areas of the screen. Output from this circuit is tied to focus biasing circuitry within the grid bias circuit. This output offsets focus biasing based on horizontal and vertical deflection values. The circuit is primarily a single transistor which acts as a mixer for parabolic inputs from the horizontal and vertical deflection circuits. This changes focus biasing as a function of the position of the beam on the tube.

8.7.2 Grid Bias

This circuit generates CRT biasing values: focus (G4), cutoff (G2), and brightness (G1). These voltages are developed from the flyback transformer. Voltages from this transformer are routed to the G4 and G2 circuits. There are resistor networks each containing potentiometers for adjusting the bias in question, R43 for G4 (focus) or R120 for G2 (cutoff). The remaining bias circuit, G1 (brightness), is a resistor network between two voltage sources, +40 Vdc and −150 Vdc. This adjustment allows the operator to adjust the display background intensity. The voltage on G1 is adjustable from approximately 0 to −47 Vdc.

8.7.3 Horizontal Deflection

This circuit drives the CRT beam across the faceplate horizontally. This circuit contains the following elements.

- A horizontal processor
- A sync buffer circuit
- A horizontal driver and output
- RC networks that bias circuits internal to the horizontal processor
- A horizontal deflection generator output stage (width and linearity inductors, horizontal output transistor, damper diode, retrace capacitor, and yoke inductor)

An oscillator within the horizontal processor allows the horizontal deflection circuit to free run. The sync pulses then synchronize the operating running rate to the video input.

The sync buffer circuit amplifies the sync pulse and then applies it to the horizontal processor. When the horizontal output turns off, the electron beam flies back, returning the beam to the left of the screen. At the end of retrace, the conducting of the damper diode establishes a ramp of current in the yoke inductor. To make sure the output transistor is turned on at the proper time, the horizontal deflection IC also provides the correct timing on its output pulse. This allows the current ramp to continue after the damper diode stops conducting. The width coil portion of the output stage adjusts the width of the display. Two of the RC networks contain potentiometers for adjusting their biasing values: R211 for hold (horizontal) and R218 for centering (phase).

A secondary output from the generator is provided to the vertical deflection circuitry as a vertical sync signal.

8.7.4 Linear Regulator

This circuit provides power to the flyback transformer during initial power up and also regulates the input voltage. During initial power up, the +12 Vdc voltage is applied to the regulator. The voltage input (rising from 0 V to +12 Vdc) is shunted through a series of 4 diodes and then through the flyback transformer. This generates 40 Vdc at the input of L300 to the regulator field effect transistor (FETs) sources. The FETs are then turned on and conduct the load current instead of the diodes. A precision zener diode plus the regulator transistor's V_{BE} cause the circuit to provide 10.3 Vdc regulated output.

8.7.5 Vertical Deflection

This circuit positions the CRT beam across the faceplate vertically. This ciruit contains the following elements.

- A vertical processor
- Various RC networks responsible for biasing of circuits internal to the vertical processor
- An output filter network.

An oscillator within the vertical processor allows the vertical deflection circuit to free run. The sync pulses synchronize the vertical deflection to prevent vertical roll.

Three of the RC networks contain potentiometers for adjusting biasing values: R48 for hold (vertical), R50 for height, and R53 for linearity. At the beginning of each refresh cycle, the vertical processor receives a vertical sync pulse from the horizontal processor circuit. The horizontal processor detects the vertical sync pulse and sends it to the vertical processor. This sync pulse comes from the composite video input to the monitor module. The vertical sync pulse causes the beam to fly back vertically and begin a new frame.

8.7.6 Video Amp

The video amp consists of an input and output stage. The video signal is applied to an input push/pull transistor network which is part of an encapsulated transistor array. The input is provided from R5, the contrast thumbwheel potentiometer. The potentiometer is adjustable by the operator for personal contrast preference. The potentiometer, R119, provides a preamplifier adjustment to preset the range that can be affected by the contrast thumbwheel. Biasing of the input stage affects the biasing of the output stage which is another transistor network. The more positive the input to the input stage, the more positive the output from the transistor network. This output is provided to the video output stage.

The video output stage provides the operational voltage for the CRT beam. The video output stage uses the voltage from the flyback transformer (40 Vdc) to generate its output. The sync pulses (horizontal and vertical) set the video output to or below the cutoff voltage so the operator does not see the retrace lines. Applying increased positive video amp signal, decreases the output to the CRT. This also increases the intensity of the CRT display.

8.7.7 Flyback Transformer

The flyback transformer is the high voltage power supply and is synchronized to the horizontal deflection. It generates the voltages used by the grid bias circuit (G1, G2, G4), the anode voltage (12.5 kV nom), and the 40 Vdc voltage used by the linear regulator and video amplifier.

WARNING

The monochrome monitor contains shock hazard voltages. Use extreme caution when servicing the monitor.

There is a high voltage (12 kV nom) on the anode lead and the anode cup on the side of the CRT.

To avoid shock, use the following procedure when discharging the anode.

1. **Turn off system power and connect the monitor cable.**

2. **Attach the clip lead of the anode discharge tool to the metal frame.**

3. **Hold the tool by its insulated handle. Using one hand, carefully slide the tip of the tool under the plastic anode cap until it touches the anode. Avoid scratching or poking the glass CRT envelope.**

4. **Once discharged, remove the tool and clip lead.**

There is also 700 Vdc on the monitor module near the flyback transformer. Use caution when performing adjustments in this area. This area is covered with a protective shield.

CAUTION

Before removing the system module monitor cable, turn off the system power. Static discharge in the CRT can damage the monitor module and/or keyboard electronics.

Be sure the system power is off before connecting or disconnecting the monitor's cable for service or moving the monitor. When performing adjustments, secure the monitor's cable to the monitor with its thumbscrews so the cable does not loosen.

Failure to follow this procedure can damage monitor and/or keyboard components.

8.7.8 J1

This connector provides the voltage and video signals to the electronics board. Refer to Section 8.4 for the pin-out and signal descriptions for J1.

8.7.9 J2

This connector provides the horizontal and vertical deflection currents between the electronics board and the yoke assembly. It is a 4-pin connector. Pins 1 and 4 are used for vertical deflection, pins 2 and 3 for horizontal deflection.

8.7.10 P1

This connector mounts on the electronics board the CRT plugs into. Figure 8-8 shows the pin-out for P1.

8.8 SPECIFICATIONS

Height	24.38 cm (9.75 in)
Width	29.33 cm (11.73 in)
Depth	30.57 cm (12.23 in)
Weight	6.6 kg (14.5 lb)

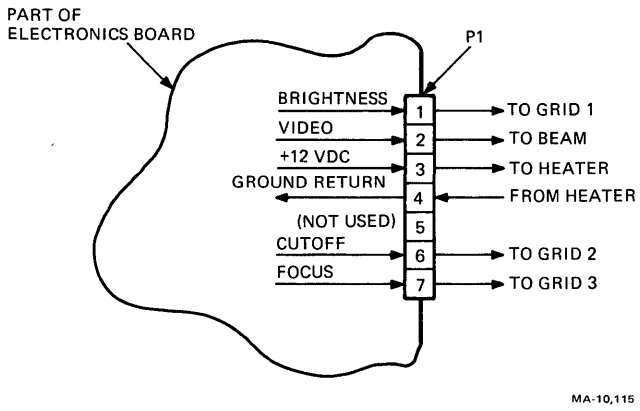


Figure 8-8 Monitor Module P1 Pin-out

CHAPTER 9
RX50 CONTROLLER MODULE

9.1 GENERAL INFORMATION

The RX50 controller module interfaces an RX50 dual diskette drive to the host processor. Figure 9-1 shows the controllers relationship to the other components of the Professional 350 system.

9.1.1 Related Documentation

Refer to the following related documentation while reading this chapter.

Title	Document No.
Professional 350 Field Maintenance Print Set	MP-01394-00

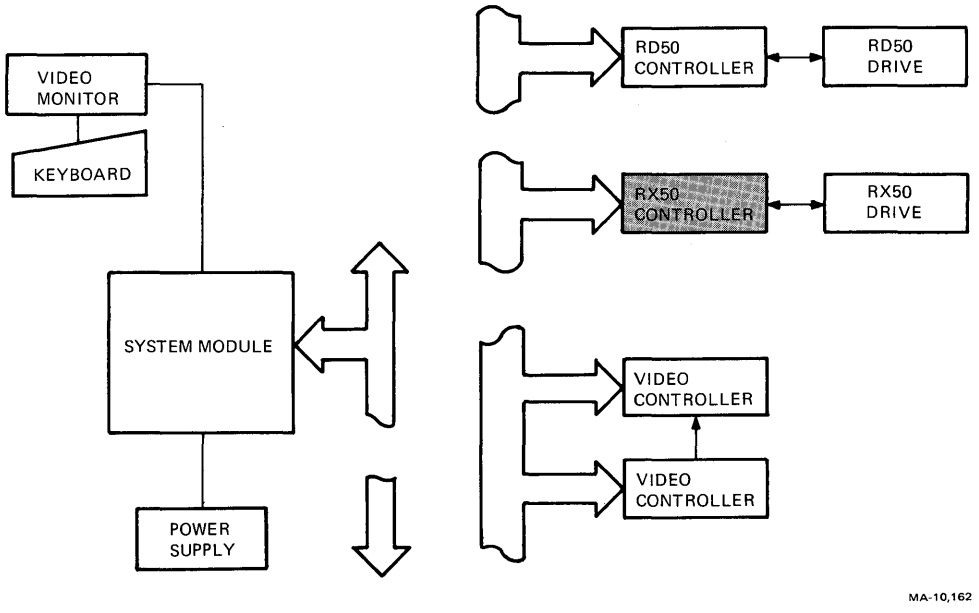


Figure 9-1 RX50 Controller Module System Relation

9.1.2 RX50 Controller Module Introduction

The RX50 controller module controls data transfers between the host processor and the RX50 dual diskette drive. This controller is a field replaceable unit (FRU PN 54-15058) which usually mounts in slot 2 of the CTI Bus option space. A single cable (FRU PN 17-00285) connects the controller to the drive. Figure 9-2 shows the RX50 controller module and the drive cable.

The controller interfaces one RX50 dual diskette drive to the host processor provide 819,200 bytes of storage. Commands, status, and data are transferred between the controller and host processor through register-to-register accesses by the host processor. The controller contains an auto-incrementing 512 8-bit byte sector buffer. This buffer holds the data transferred between the host processor and the RX50 drive. Accesses to this buffer can be started or stopped without loss of the sequential addressing.

The controller performs implied seeks when performing a read or write operation with the sector and track specified in the command registers. All data is stored on the diskettes using modified frequency modulated (MFM) data encoding.

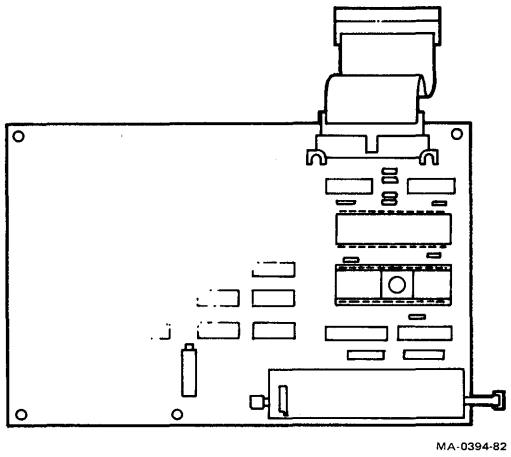


Figure 9-2 RX50 Controller Module

9.2 FUNCTIONAL COMPONENTS

The following paragraphs describe the components of the RX50 controller module.

9.2.1 Overview

The module is a single 5.2 × 8 inch module compatible with the CTI backplane. A connector on the bottom (J1) provides a connection path to the CTI BUS. A connector at the top of the module (J2) provides a connection path to the RX50 dual diskette drive.

The following steps describe how the RX50 controller performs data transfers from main memory to the disk surface.

1. The host processor controls the data transfer between main memory and the sector data buffer in the controller.

2. A microprocessor in the controller then controls the data transfer between the sector data buffer and the disk surface.

If the host processor requests data from the drive, these steps are reversed.

The controller performs the encoding, decoding, and data error detection for all transfers between the disk surface and the sector buffer.

The following are the major circuits that make up the RX50 controller module (Figure 9-3).

- CTI BUS to controller memory interface
- Microprocessor to controller memory interface
- Disk control and status interface
- MFM write data interface
- MFM read data interface

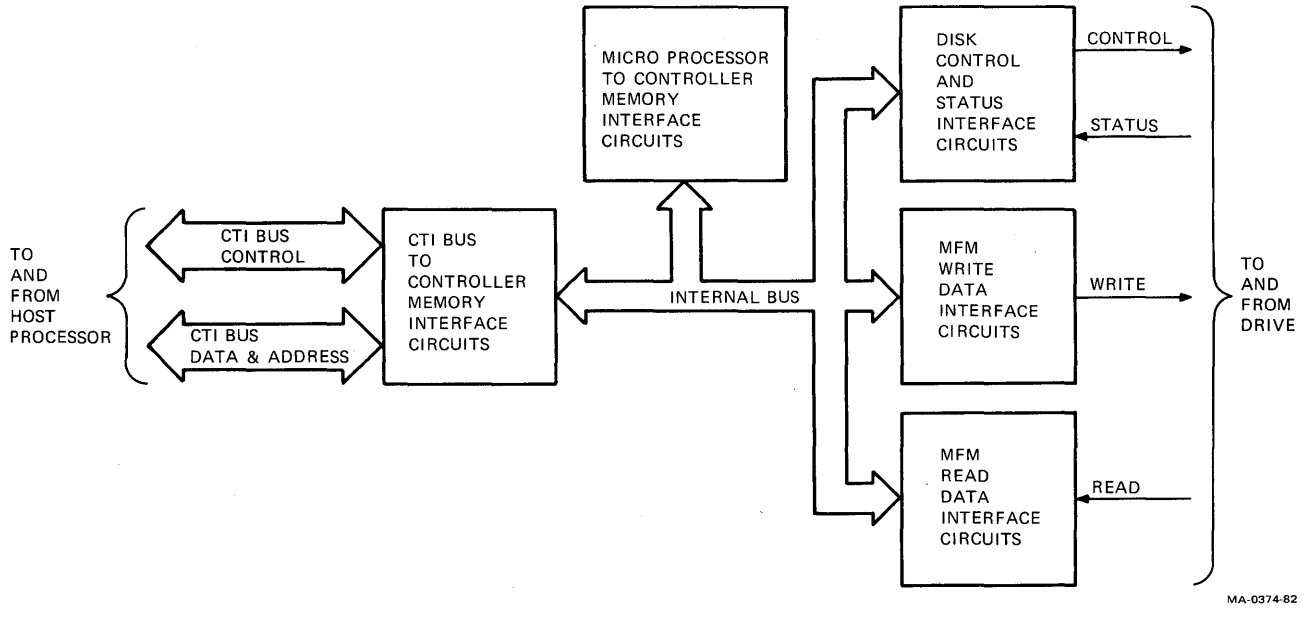


Figure 9-3 RX50 Controller Module Block Diagram

9.2.2 CTI BUS to Controller Memory Interface

The host processor accesses the controller by reading and writing the controller memory. All accesses to the RX50 identification register and the RX50 control and status registers are relocated to byte locations in the lower half of the lK controller memory. Table 9-1 describes this controller memory organization. The remaining 488 byte locations in the lower half of memory are reserved for future applications. All accesses to the RX50 data buffer registers are relocated to the upper half of the 1K controller memory. The 512 byte locations are used as the sector data buffer.

When the host processor accesses the controller memory, the CTI BUS to controller memory interface circuits perform the following operations.

- Acknowledges accesses to its registers (memory) by the host processor.
- Decodes CTI BUS control signals from the host processor.
- Passes data between the host processor and the controller registers (memory).
- Generates interrupts for the host processor when the controller completes a command.

Table 9-1 RX50 Controller Memory Organization

Memory Address (octal)	Byte Number	Function
1777 to 1000	1023 to 0512	Sector buffer sequential accesses to memory location 20 or 26 are relocated here
0777 to 0030	0511 to 0024	Reserved
0027 to 0020	0023 to 0016	Sector buffer relocation addresses and command addresses
0017 to 0010	0015 to 0008	Status registers
0007 to 0000	0007 to 0000	Command registers

9.2.3 Microprocessor to Controller Memory Interface

The microprocessor accesses the controller memory to retrieve commands and store status data. It then executes the commands and controls the internal data flow of the RX50 controller.

The microprocessor arbitrates the use of the internal I/O bus for the disk control and status interface, MFM write data interface, and MFM read data interface circuits.

9.2.4 Disk Control and Status Interface

The disk control and status interface passes control and status information between the module and the RX50 disk drive. The microprocessor I/O ports receive the drive status information from the drive and pass drive control information to the drive.

9.2.5 MFM Write Data Interface

The MFM write data interface converts data in the sector buffer to MFM data for the RX50 drive. These circuits perform the following operations.

- Converts the sector buffer contents to serial MFM encoded data.
- Precompensates the MFM encoded data for varying bit densities on the diskettes.
- Accumulates then adds two CRC bytes to the end of the serial data.
- Synchronizes the MFM encoded data to a reference clock cycle.
- Passes the MFM write data to the RX50 disk drive.

9.2.6 MFM Read Data Interface

The MFM read data interface converts MFM data read from the disk drive, into 8-bit bytes and places them in the sector buffer. These circuits perform the following operations.

- Recovers the MFM encoded data received from the drive.
- Converts the MFM encoded data to 8-bit bytes for the sector buffer.
- Calculates two CRC bytes and compares them to the values stored with the received data.

9.3 THEORY OF OPERATION

The RX50 module has five functions for storing and retrieving data on the RX50 disk drive by the host processor. This section describes each of the following functions at a block diagram level.

- CTI BUS to controller memory interface
- Microprocessor to controller memory interface
- Disk control and statu interface
- MFM write data interface
- MFM read data interface

9.3.1 CTI BUS to Controller Memory Interface Detail

The host processor accesses the controller memory through the following circuits when the microprocessor is not executing a command. The host processor can write to the command registers, read the status registers, and read or write to the sector buffer. The CTI BUS to controller memory interface uses the following circuits (Figure 9-4).

- CTI BUS control signal I/O buffer
- CTI BUS data/address I/O buffer
- Microprocessor
- R/$\overline{W}$ signal multiplexer
- Address latch
- Address decoder
- Sector buffer address counter
- Address multiplexer
- Sector buffer/command and status registers (memory)

These circuits perform the following functions.

- Passes power ok (POK) and initialization (INIT) signals from the CTI BUS to the controller.
- Passes interrupt (IRQA and IRQB) signals from the controller to the CTI BUS.
- Acknowledges accesses to the controller address range with a reply signal (RPLY).
- Controls data transfers between the controller memory and the CTI BUS.

9.3.1.1 RX50 Module Initialization – The CTI BUS control signal I/O buffer receives a B POK H and a B INIT L signal from the host processor. These signals reset or initialize circuits in the controller.

The B INIT L signal initializes the address latch, address decoder, sector buffer address counter, and the microprocessor. The B POK H signal initializes the address latch, address decoder, sector buffer address counter, microprocessor, and the floppy controller.

When the B INIT L signal is asserted on the CTI BUS, the INIT signal internal to the module is asserted. When the B POK H signal on the CTI BUS is unasserted, the POK signal internal to the module is unasserted and the INIT signal is asserted. The internal initialization signal generation does not depend on which function has control over the internal bus.

9.3.1.2 Interrupt Signal Generation – The CTI BUS control signal I/O buffer passes two interrupt signals (INRQ A and INRQ B) from the microprocessor on the module to the CTI BUS (IRQA L and IRQB L). The IRQA interrupt signal indicates a command completed execution. The IRQB L interrupt signal indicates a volume change (the drive door was opened and closed).

Only the first volume change between read status commands generates the interrupt. Volume changes received from the drive before the module receives a read status command do not generate interrupts.

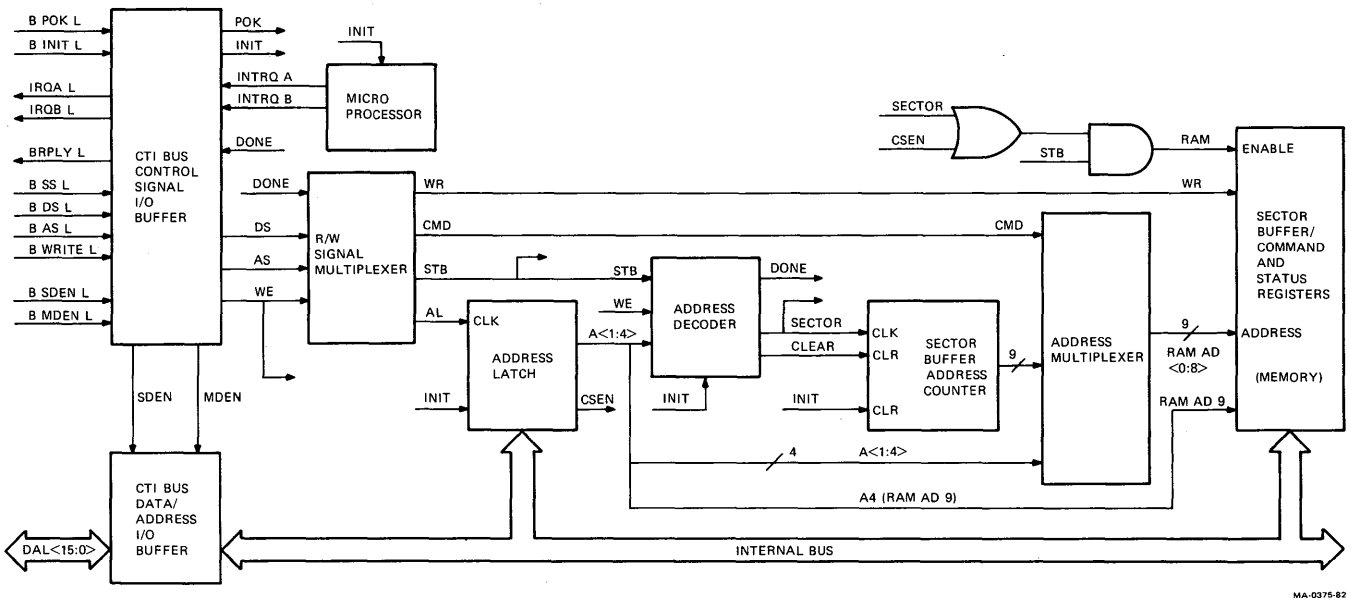
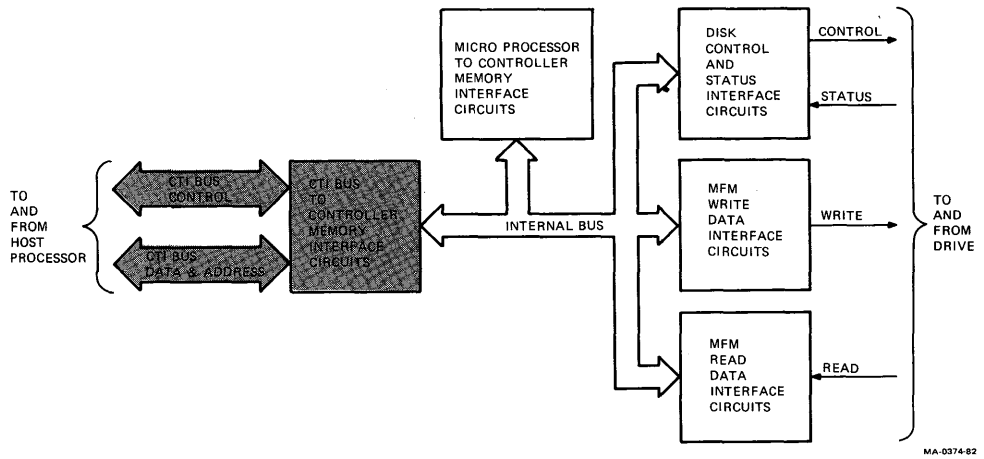


Figure 9-4 CTI BUS to Controller Memory Interface Circuits



9.3.1.3 RX50 Module Acknowledgment – The module responds to the CTI BUS by asserting the B RPLY L signal. This signal is generated by the module when the CTI BUS slot select (B SS L) and the data strobe (B DS L) are asserted.

9.3.1.4 Host Processor to Controller Memory Accessing – If the microprocessor on the module is not excuting any commands, the RX50 module memory can be addressed from the CTI BUS. The address decoder generates an unasserted DONE signal to indicate CTI BUS to controller accessing.

The address decoder is shared by both the host processor and the microprocessor to access the memory. Also shared are the R/W signal multiplexer, address latch, sector buffer address counter, and address multiplexer.

The memory on the RX50 module is addressed in two modes: command and status register memory addressing or sector buffer memory addressing. The command and status register mode allows random writing to the command registers and random reading of the status registers. The sector buffer mode allows sequential access to the 512 8-bit bytes. All memory locations are partially decoded and mapped into a 1K by 8-bit memory array. The module performs all memory address relocation operations for both modes. Memory accessing from the CTI BUS is done through the addresses listed in the programming section.

All accesses to the controller from the host processor are addressed on word boundaries. When the host processor accesses the memory in the command and status memory range, the CTI BUS write signal is used as an address bit for memory. The controller translates word accesses to byte accesses by shifting the address. It does not use the zero bit of the CTI BUS address. The address shift causes the CTI BUS address bit 1 to become controller memory address bit 0, the CTI BUS address bit 2 to become controller memory address bit 1 and also for all other address bits. This allows eight CTI BUS word address locations to be mapped into 16 controller memory address locations.

Command and Status Register Accessing
When the DONE signal is unasserted, the master device enable (B MDEN L) signal from the CTI BUS can enable the CTI BUS data/address I/O buffer to pass data and address on the CTI data/address lines to the internal bus. CTI BUS addresses in the range 00 to 16 access the command and status registers.

Once the address is on the internal bus, the CTI BUS address strobe (B AS L) passes to the R/W signal multiplexer and generates an address latch clock signal (AL). The AL signal clocks the address latch to accept four address bits (DAL 1, DAL 2, DAL 3, and DAL 4). This address goes to the address decoder and address multiplexer. Addresses in the 00 to 16 range disable the address decoder and the sector buffer address counter. This asserts the command and status enable signal (CSEN) to set up memory for a data transfer.

Once the data is present on the internal bus, the data strobe (B DS L) from the CTI BUS generates a data strobe (DS) from the CTI control signal I/O buffer to the R/W signal multiplexer. The multiplexer then generates a strobe (STB) for the memory. After the CSEN and STB signals are asserted, the memory is enabled for the data transfer.

Along with the data strobe, R/W select (B WRITE L) signal on the CTI BUS passes to the R/W signal multiplexer as WE. An asserted WE asserts a write signal (WR) for the memory and asserts a command select signal (CMD) for the address multiplexer. This selects a write operation to the command address range in the controller memory (addresses 00 to 07). When the WE signal is unasserted, both WR and CMD are unasserted. This selects a read operation to the status address range of the controller memory (addresses 10 to 17).

The address multiplexer uses the CMD signal and the four address bits from the address latch to generate an address for the memory. Since the memory is enabled when CSEN and STB signals are asserted, the address from the address multiplexer selects the desired location and WR specifies a write operation, internal bus to memory, or a read operation, memory to internal bus.

Sector Buffer Memory Accessing

Some of the same operations occur during a sector buffer memory access that occur during a command and status register access. The difference is the address decoder and sector buffer address counter provide the address to the address multiplexer for the memory.

When the DONE signal is not asserted, the master device enable (B MDEN L) signal from the CTI BUS can enable the CTI BUS data/address I/O buffer to pass an address on the CTI data/address lines to the internal bus. CTI BUS addresses in the range 20 to 26 access the sector buffer registers.

Once the address is on the internal bus, the CTI BUS address strobe (B AS L) passes to the R/W signal multiplexer and generates an address latch clock signal (AL). The address latch accepts only four address bits (DAL 1, DAL 2, DAL 3, and DAL 4) then provides them to the address decoder and address multiplexer. Addresses in the 20 to 26 range enable the address decoder and the sector buffer address counter and unasserts the CSEN signal. Table 9-2 defines these addresses and their functions.

The sector buffer address counter provides a 9-bit address to the address multiplexer. The 10th address bit comes from the address latch (A4). This bit enables the address multiplexer to pass the sector buffer address counter output to the memory as well as select the high bank of memory locations directly (RAM 9).

The data strobe (B DS L) from the CTI BUS generates a data strobe (DS) from the CTI control signal I/O buffer to the R/W signal multiplexer. The multiplexer then generates a strobe (STB) for the memory. When the SECTOR and STB signals are asserted, the memory is enabled.

Along with the data strobe, the R/W select (B WRITE L) signal on the CTI BUS passes to the R/W signal multiplexer as WE. An asserted WE asserts a write signal (WR) for the memory. When the WE signal is unasserted, the WR signal is unasserted.

When address 26 is used for write operations (WR asserted), the sector buffer may be accessed to accept data from the internal bus. When address 20 is used for read operations (WR unasserted) the sector buffer will place data on the internal bus.

Table 9-2 Controller Responses to CTI Bus Addresses 20 through 26

Address	Operations Performed
20	A read operation generates a SECTOR signal. This increments the sector buffer address counter at the end of a memory access cycle. When STB is asserted, memory is enabled.
22	Accessing this address generates a CLEAR signal. This resets the sector buffer address counter.
24	Accessing this address asserts the DONE signal. This notifies the microprocessor that new commands were loaded into the memory. The host processor can now turn control of the module over to the microprocessor.
26	A write operation allows the decoder to synchronize the generation of a SECTOR signal with an asserted WE (Section 9.5).

9.3.2 Microprocessor to Controller Memory Accessing

The microprocessor can access the memory in the RX50 controller after the host processor releases control of the module to the microprocessor (Figure 9-5). This is accomplished when the host processor accesses register 24. The address decoder asserts a DONE signal. This indicates microprocessor to controller memory accessing. The decoder is also used by the CTI BUS to memory interface function. Other items used by the CTI BUS for memory interface include: the R/W signal buffer, address latch, sector buffer address counter, and address multiplexer.

As in the CTI BUS to memory interface function, the memory on the RX50 module is addressed in two modes, command and status register memory addressing and sector buffer memory addressing. The command and status register mode accesses addresses 0 through 16 of the memory. The sector buffer mode accesses addresses 512 through 1023 (upper 512 8-bit words) of the memory. The module performs all memory address relocation operations for both modes.

The microprocessor performs both read and write operations to the command and status registers. The microprocessor can clear any command register after it has been read. This protects recorded data in the event of circuit failures.

9.3.2.1 Command and Status Register Accessing – When the DONE signal is asserted, the microprocessor controls the output of the R/W signal multiplexer. The microprocessor can place addresses on the internal bus and assert the address latch enable signal (ALE). This causes the AL signal to load the address into the address latch. Addresses in the range 00 to 16 access the command and status registers.

The address latch accepts only four address bits (DAL 1, DAL 2, DAL 3, and DAL 4) for the address decoder and address multiplexer. Addresses in the 00 to 16 range disable the address decoder and the sector buffer address counter and assert the command and status enable signal CSEN.

A microprocessor read or write signal (μPRD or μPWR) generates a strobe (STB) for the memory from the R/W signal multiplexer. When the CSEN and STB signals are asserted, the memory is enabled for read or write operations.

The microprocessor specifies a command register access or a status register access with a COMMAND signal. An asserted COMMAND signal asserts CMD for the address multiplexer selecting command registers. An unasserted COMMAND signal unasserts CMD for the address multiplexer selecting status registers.

The address multiplexer uses the CMD signal and the four address bits from the address latch to generate an address for the memory. Since the memory is enabled by an asserted CSEN and STB signals, the address from the address multiplexer selects the desired location. The μPWR asserts WR to specify a write operation (internal bus to memory), or unasserts WR to specify a read operation (memory to internal bus).

9.3.2.2 Sector Buffer Memory Accessing Function – Some of the same operations occur during a sector buffer memory access and a command and status register access. The difference is the address decoder and sector buffer address counter provide the address to the address multiplexer for the memory.

When the DONE signal is asserted, the microprocessor controls the output of the R/W signal multiplexer. The microprocessor places addresses on the internal bus and asserts the address latch enable signal (ALE). This asserts the AL signal and loads the address into the address latch. Addresses in the range 20 to 24 access the sector buffer registers.

The address latch accepts only four address bits (DAL 1, DAL 2, DAL 3, and DAL 4) then provides them to the address decoder and address multiplexer. Addresses in the 20 to 24 range enable the address decoder and the sector buffer address counter and unasserts the CSEN signal. Table 9-3 describes the operations these addresses access for the microprocessor.

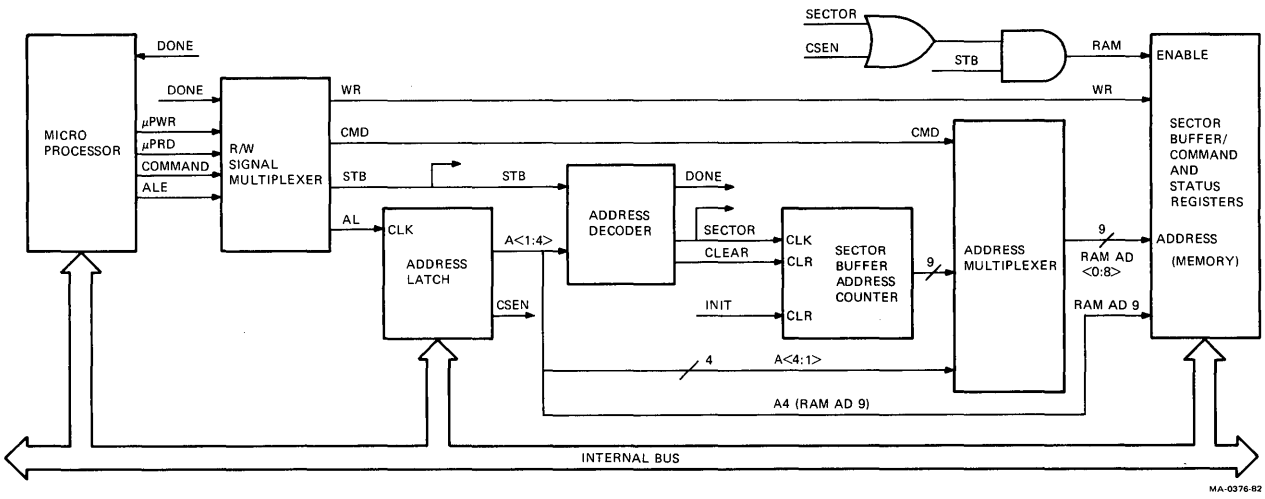


Figure 9-5 Microprocessor to Controller Memory Interface Circuits

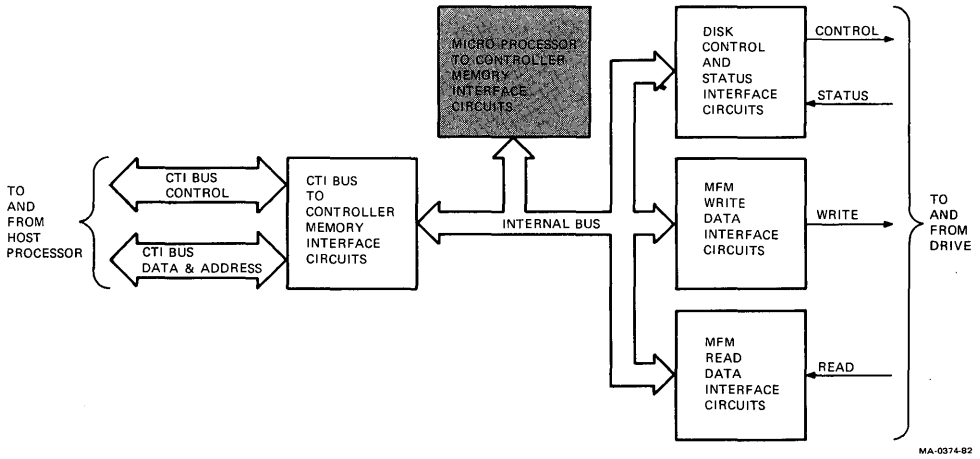


Table 9-3 Microprocessor Accesses to Addresses 20 through 26

Address	Operations Performed
20	Read and write operations generates a SECTOR signal. This increments the sector buffer address counter at the end of a memory access cycle. When STB is asserted, memory is enabled.
22	Accessing this address generates a CLEAR signal. This resets the sector buffer address counter.
24	Accessing this address unasserts the DONE signal. This turns control of the module over to the microprocessor.
26	This address is not used by the microprocessor to access the sector buffer.

The sector buffer address counter provides a 9-bit address to the address multiplexer. The 10th address bit (RAM9 which is A4) comes from the address latch. This bit also enables the address multiplexer to pass the sector buffer address counter output to the memory and selects the high bank of memory locations.

A microprocessor read or write signal (μPRD or μPWR) generates a strobe (STB) for the memory from the R/W signal multiplexer. When the SECTOR and STB signals are asserted, the memory is enabled for read or write operations.

The address multiplexer uses address latch bit A4 to select the sector buffer address counter output as the 9-bit address for the memory. Since the memory is enabled by asserted SECTOR and STB signals, the address from the address multiplexer and A4 (RAM A9) from the address latch select the desired location. The μPWR asserts WR to specify a write operation (internal bus to memory), or unasserts WR to specify a read operation (memory to internal bus).

9.3.3 Disk Control and Status Interface Function

The disk control and status function passes disk control and status signals between the RX50 drive and the RX50 controller module (Figure 9-6). The control signals for the RX50 drive are generated after the command registers are loaded with commands by the host processor (Section 9.3.1). The RX50 module receives the status signals from the RX50 drive. These signals are used for timing during command execution.

The following circuits allow the module to accept or generate these signals.

- Microprocessor
- Floppy controller
- Unit selection decoder
- Output drivers

Commands loaded into the RX50 controller registers generate the following control signals.

- Drive select signals (SEL0 L, SEL1 L, SEL2 L, and SEL3 L)
- Write enable signal (WG L)
- An RX50 drive spindle motor control signal (MOTOR PWR ON L)
- Write current selection signal (TG43 L)
- Track positioning signals (DIR L and STEP L)

The controller accepts the following status signals from the RX50 drive.

- The selected diskette is write protected (WRT PRT L)
- The heads are located over track zero (TK 00 L)
- The beginning of a track (INDEX L)
- The drive is ready for operation (READY L)

9.3.3.1 Control and Status Signal Processing – After the host processor loads the command registers and accesses the start command register (register address 24), the microprocessor directly accesses the registers (Section 9.3.2). The microprocessor read and write signals (μPRD and μPWR) used during a microprocessor to memory interface function also control the access to the floppy controller through the internal bus. This allows the microprocessor to control the RX50 module operations and access the floppy controller registers when executing commands.

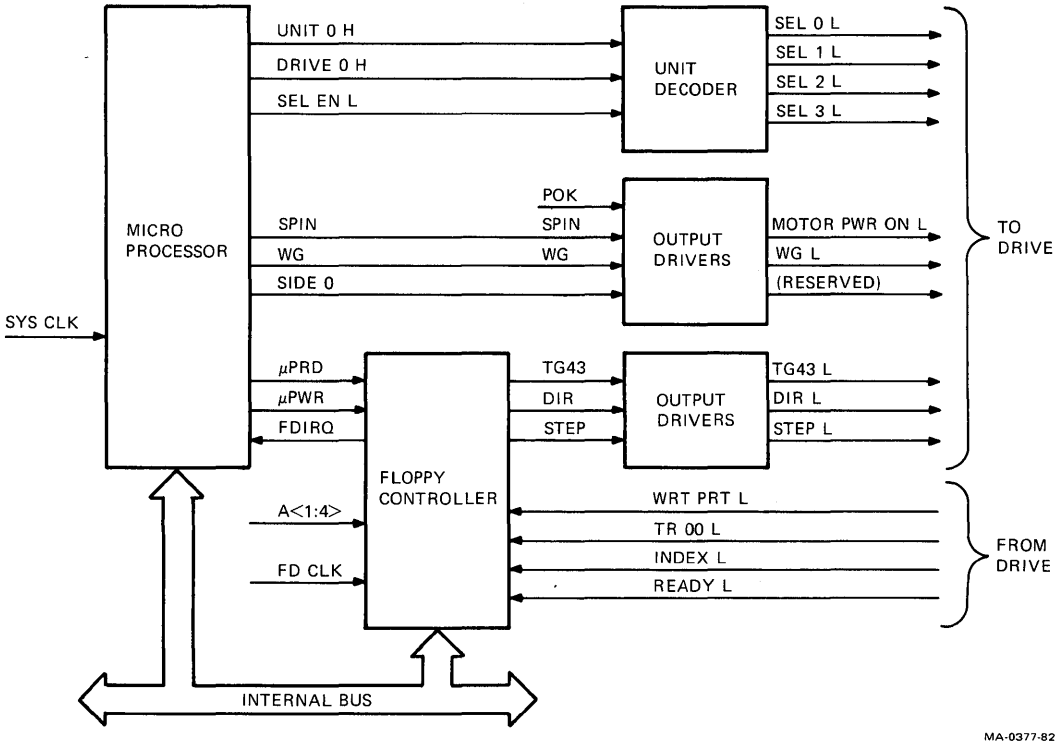
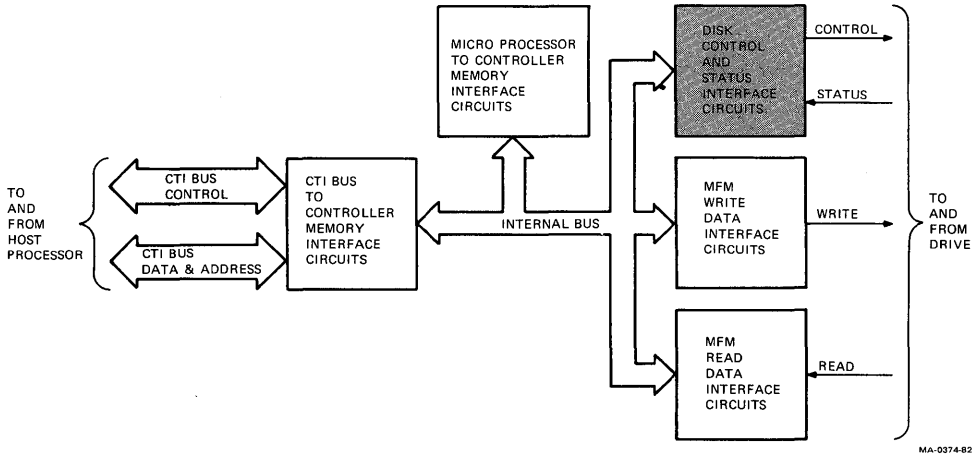


Figure 9-6 Disk Control and Status Interface Circuits



After the floppy controller executes a command, it generates an interrupt (FDIRQ) for the microprocessor. This signal indicates that the microprocessor can send another command to the floppy controller, or the microprocessor can read the floppy controller status registers.

None of the floppy controller status or command registers are directly accessible by the host processor. The microprocessor reads the floppy controller registers and transfers data over the internal bus to or from the memory for access by the host processor.

9.3.3.2 Drive Select Signal Conversion – The microprocessor generates four signals for selecting an RX50 drive: UNIT 0, DRIVE 0 and SEL EN, and SIDE. The SIDE signal is reserved for future use. A unit selection decoder decodes the remaining signals and generates the drive select signals, SEL0 L, SEL1 L, SEL2 L, or SEL3 L. Table 9-4 shows this conversion.

9.3.3.3 Drive Control Signal Gating – The microprocessor generates a write enable signal (WG) and a spindle motor control signal (SPIN) for the RX50 drive. These signals are sent to the drive only when the power levels for the system are within tolerance. This protects data on the RX50 drive when power is first applied to the system or during power loss situations.

The WG and SPIN signals go to an output driver. The driver passes them to the drive as WG L and MOTOR PWR ON L respectively. When the power is in tolerance, a power ok signal (POK) from the CTI BUS (Section 9.3.1) enables the microprocessor output to the RX50 drive.

9.3.4 Write Data Interface Function

A write data interface function converts the sector buffer contents to precompensated MFM write data for the RX50 drive (Figure 9-7). The following circuits also share this function.

- Microprocessor
- Floppy controller
- Input write data sync
- Precompensation ROM
- Output write data sync
- Clock generator

Table 9-4 Drive Select Signal Conversion

Asserted Control Signals			Asserted Selects			
UNIT0 H	**DRIVE0 H**	**SEL EN L**	**0**	**1**	**2**	**3**
X	X	No	No	No	No	No
No	No	Yes	No	No	No	Yes
Yes	No	Yes	No	No	Yes	No
No	Yes	Yes	No	Yes	No	No
Yes	Yes	Yes	Yes	No	No	No

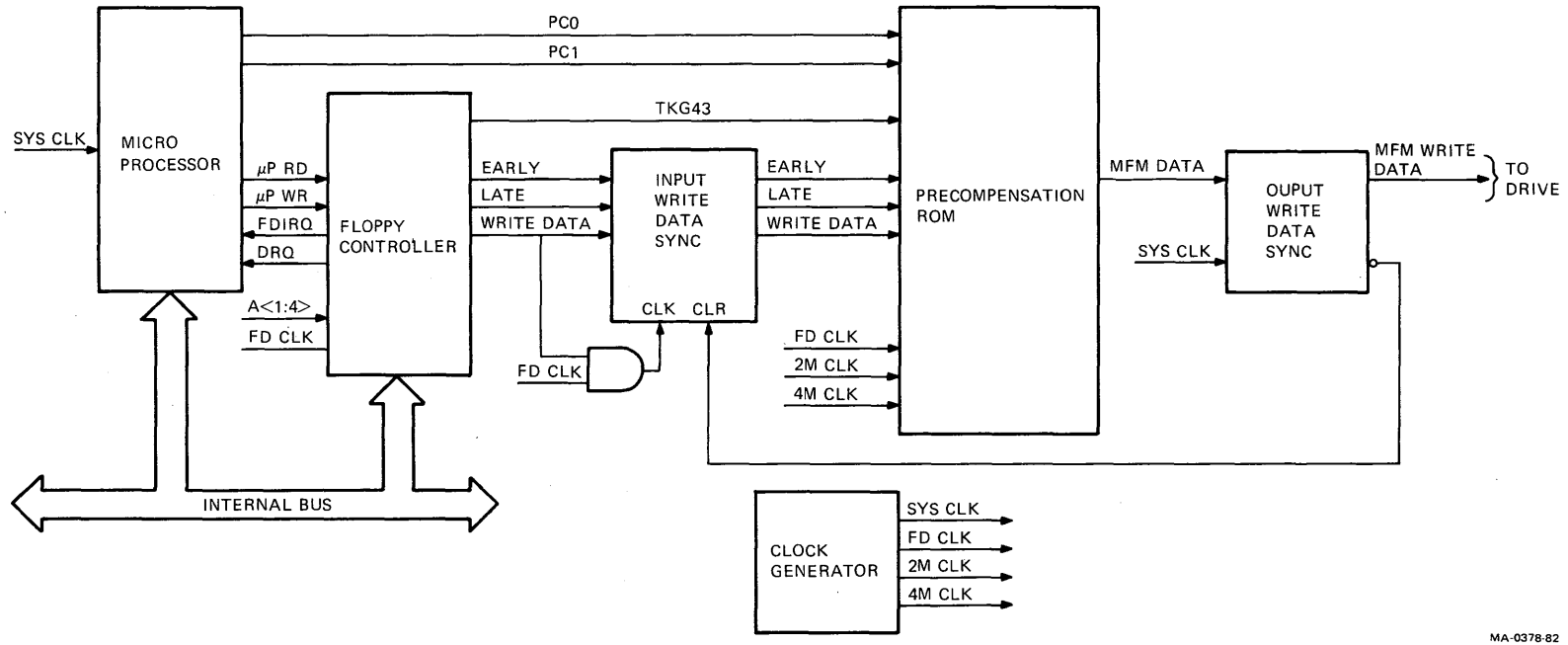
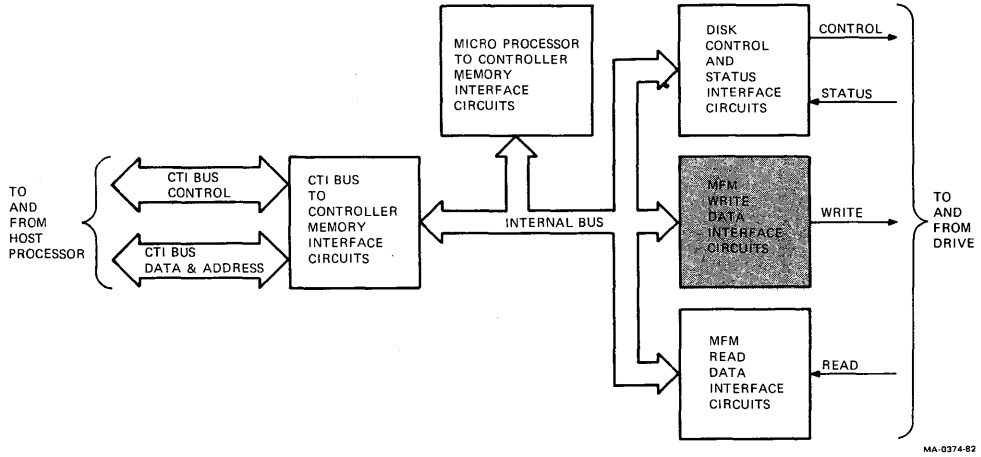


Figure 9-7 MFM Write Data Interface Circuits



9.3.4.1 Write Data Bytes to Floppy Controller Transfers – After the module receives a write command from the host processor, a write data function is performed (Section 9.4). The host processor loads the sector buffer (Section 9.3.1) with the data to be written to the drive and accesses the start command register (Section 9.4). The microprocessor then accesses the sector buffer (Section 9.3.2).

The microprocessor read and write signals (μPRD and μPWR) used during a microprocessor to controller memory interface function also control the access to the floppy controller over the internal bus. The microprocessor can then control the RX50 module operations and access the floppy controller registers when executing commands.

After the floppy controller executes a command, it generates an interrupt (FDIRQ) for the microprocessor. This signal indicates that the microprocessor can send another command to the floppy controller or the microprocessor can read the floppy controller status registers. When the floppy controller requires a data byte for conversion to MFM data, it generates a data request signal (DRQ) for the microprocessor.

The host processor cannot directly access the floppy controller data, status or command registers. The microprocessor reads and writes commands and data to the floppy controller registers over the internal bus to or from the module memory.

9.3.4.2 MFM Encoding – The floppy controller converts the 8-bit data bytes to serial MFM data patterns (WRITE DATA) and generates select signals (EARLY and LATE). The select signals indicate when a pulse should be generated within a 4μs bit frame. Table 9-5 shows how the floppy controller encodes MFM data.

As these signals are generated they pass to the input write data sync circuit. A 1 MHz clock (FDCLK) synchronizes the transfer of the EARLY, LATE, and WRITE DATA to the precompensation ROM.

Table 9-5 MFM Encoding

Already Sent		Data to be Sent		MFM
X	1	1	1	Early
X	0	1	1	Late
0	0	0	1	Early
1	0	0	0	Late

9.3.4.3 Write Data Precompensation – After the floppy controller generates the encoding signals for MFM data recording, precompensation is performed. Precompensation is a technique used in high density recording. It shifts each MFM data pulse earlier or later than normal MFM data pulses. This compensate for the drifting of magnetic domains on the media. Drifting results from the repulsion of the magnetic domains at high densities.

The microprocessor sends two precompensation designation signals (PC0 and PC1) to the precompensation ROM. The floppy controller sends a signal (TK43) which designates write operations to the outer tracks (0 – 43) or inner tracks (44 – 79). Three clock signals (FDCLK, 2MCLK, 4MCLK) shift the MFM data pulse depending on the track the data is to be written.

Table 9-6 shows the bit shift characteristics for each group of tracks on the media.

9.3.4.4 MFM Write Data Synchronization – The precompensation ROM sends the MFM data to the output write data sync circuit for transfer to the RX50 drive. This sync circuit, clocked at 8 MHz, allows for the proper accessing time of the precompensation ROM to pass the serial MFM write data to the drive.

9.3.5 MFM Read Data Interface Function

The MFM read data interface function (Figure 9-8) converts the MFM encoded data from the RX50 drive to 8-bit bytes for the sector buffer. The following circuits are used to perform this operation.

- Microprocessor
- Floppy controller
- Data separator/phase lock loop

9.3.5.1 Data Separator and Phase Lock Loop Operation – The floppy controller controls the operation of the data separator and phase lock loop. A variable frequency oscillator enable signal (VFOE) enables the data separator and phase lock loop to lock onto the frequency and phase of the read data (RD DATA) received from the drive. The data is locked in phase with read clock (RD CLK), derived from the read data, and is passed to the floppy controller and microprocessor.

Along with the read data, the data separator and phase lock loop generates a data pulse (RAW DATA) for every RD DATA pulse from the drive. The floppy controller searches for data fields of all ones or zeros then asserts a read gate signal (RG). When RG is asserted, the data separator and phase lock loop synchronizes with the incoming read data.

After the data field of the target sector has been read or a time out error occurs, the floppy controller unasserts the VFOE signal. This enables the phase lock loop to lock on to a 500 KHz signal (REF CLK) and stay within the capture range for the next read cycle.

Table 9-6 Precompensation MFM Data Pulse Shift

	TK0-43	TK44-60	TK61-79
Early	125 ns	250 ns	375 ns
Late	125 ns	250 ns	375 ns

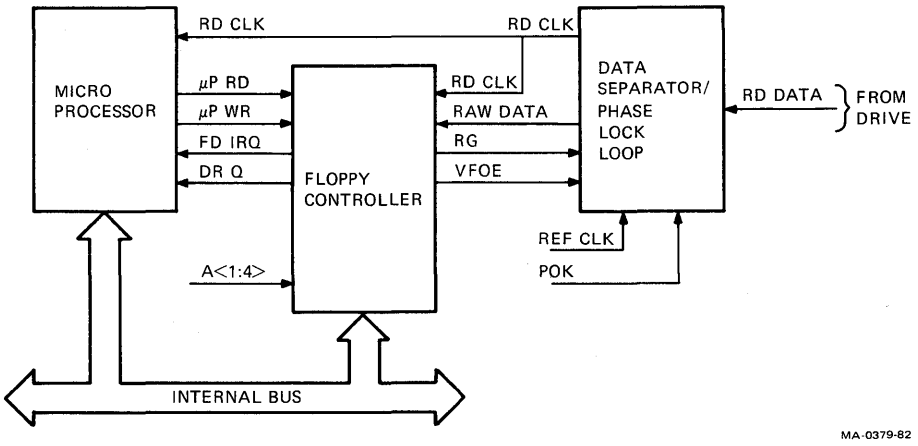
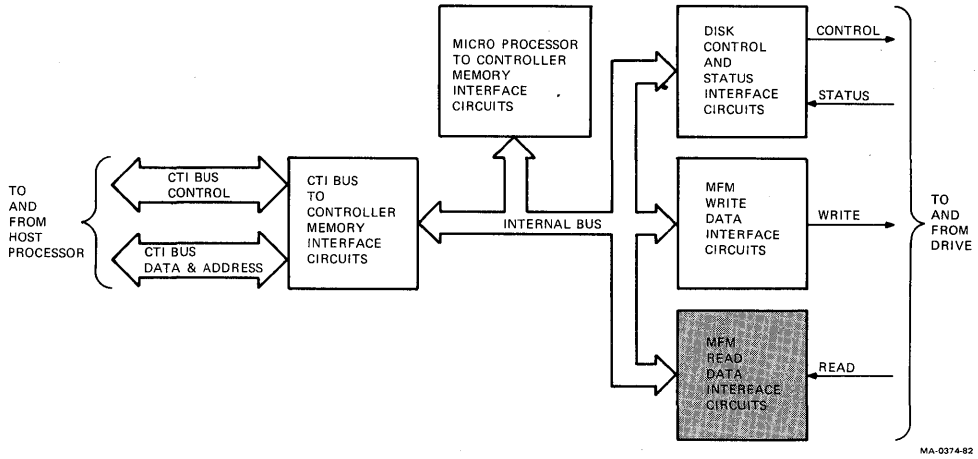


Figure 9-8 MFM Read Data Interface Circuits



9.3.5.2 Read Data Byte Conversion and Transfer – A read data operation is performed after the host processor loads the appropriate registers. (Refer to Section 9.3.1 for register loading and Section 9.4 for register definitions). The microprocessor read and write signals (μPRD and μPWR) used during a microprocessor to controller memory interface function, also control the access to the floppy controller over the internal bus. This allows the microprocessor to control the RX50 module operations and access the floppy controller registers when executing commands.

After the floppy controller executes a command, it generates an interrupt (FDIRQ) for the microprocessor. This signal indicates that the microprocessor can send another command to the floppy controller or the microprocessor can read the floppy controller status registers. When the floppy controller accumulates a data byte it decoded from the read data (RAW DATA), it generates a data ready signal (DRQ) for the microprocessor.

None of the floppy controller data, status, or command registers are directly accessible by the host processor. The microprocessor reads and writes commands and data to the floppy controller registers over the internal bus to or from the memory.

9.3.6 Module Data Flow Description

The following sections provide two examples of data flow, a drive command data flow and a write data flow. These examples do not follow the command sequences of the microcode but are presented as an aid in understanding the RX50 module capabilities.

Drive Command Data Flow

When the host processor sends a command to the drive the following events occur.

- The host processor places the address of the register it wants to access which will control the drive. Refer to Section 9.6 for register definitions.
- The host processor asserts the CTI BUS control signals in the correct sequence. This activates the RX50 module to accept the address.
- The address is loaded into the address latch.
- The host processor places the data for the register on the CTI BUS address/data lines.
- The host processor asserts the CTI BUS control signals in the correct sequence. This activates the RX50 module to accept the data and load it into the sector buffer/command and status registers.
- The microprocessor then performs the command and calculates any values designated by the command.
- The microprocessor accesses the floppy controller registers to perform the designated command.
- The microprocessor and floppy controller generate the appropriate signals for the unit selection decoder and output drivers.

Write Data Flow

When the host processor sends data to the drive for storage the following events occur.

- The host processor places the address of the register it wants to access to control the drive. Refer to Section 9.6 for register definitions.
- The host processor asserts the CTI BUS control signals in the correct sequence. This activates the RX50 module to accept the address.
- The address is loaded into the address latch.
- The host processor then places data words for the register on the CTI BUS address/data lines and asserts the CTI BUS control signals in the correct sequence. This activates the RX50 module to accept the data and load it into the sector buffer/command and status registers.
- When transferring data, the host processor continually accesses the data register to transfer data from the CTI BUS to the internal I/O bus to the sector buffer/command and status registers.
- When the transfer from the host processor to the RX50 module is complete, the microprocessor places the data words from the sector buffer on the internal I/O bus. The microprocessor then loads the data word into the floppy controller.

- The floppy controller and microprocessor then convert the data bytes to precompensated MFM data (Section 9.3.4).
- For every data word shifted out, the floppy controller generates a status signal for the microprocessor to request another data word.
- The floppy controller accumulates and adds two CRC bytes after the original write data is serially shifted out.

9.4 Detailed Connector Descriptions

The following paragraphs describe the RX50 controller connections.

9.4.1 CTI BUS Interface J1

The RX50 module uses the data/address and control lines of the CTI BUS to implement program data transfers. Figure 9-9 shows the pin functions and signal directions of this connector. Refer to Chapter 5 for further details.

9.4.2 Drive Interface Connector J2

Table 9-7 lists the pin functions of the RX50 modules J2 connector. The signal mnemonic column also describes the asserted state of the signal. An L after the mnemonic indicates an asserted low state (logic zero). An H after the mnemonic indicates an asserted high state (logic high).

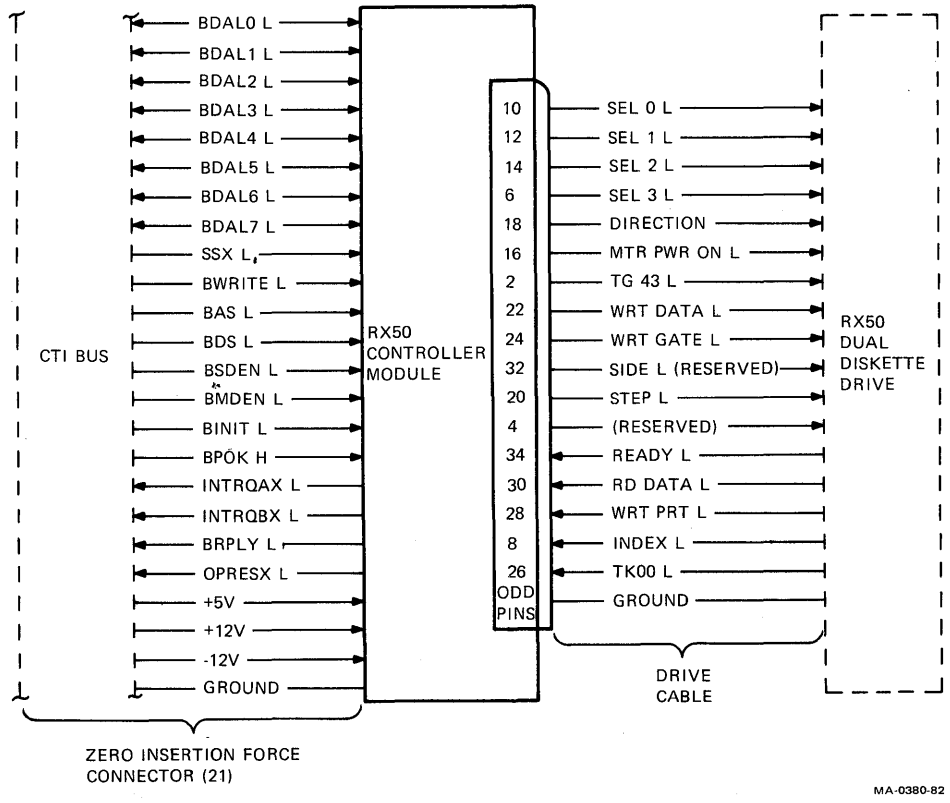


Figure 9-9 RX50 Controller Module Interface Signal Flow

Table 9-7 Connector J2 Pin Description

Pin	Signal Name	Signal Mnemonic
1	Ground	
2	Track 43	TG 43 l
3	Ground	
4	Reserved	
5	Ground	
6	Drive select 3	SEL 3 L
7	Ground	
8	Index	INDEX L
9	Ground	
10	Drive select 0	SEL 0 L
11	Ground	
12	Drive select 1	SEL 1 L
13	Ground	
14	Drive select 2	SEL 2 L
15	Ground	
16	Motor power on	MOTOR PWR ON L
17	Ground	
18	Direction	DIR L
19	Ground	
20	Step pulse	STEP L
21	Ground	
22	MFM write data	WRT DATA L
23	Ground	
24	Write gate	WG L
25	Ground	
26	Track zero	TRK 00 L
27	Ground	
28	Write protect	WRT PRT L
29	Ground	
30	MFM read data	RD DATA
31	Ground	
32	Reserved	SIDE
33	Ground	
34	Drive ready	READY L

9.4.2.1 TKG43 L Output Signal – The RX50 controller generates this signal and asserts it when writing data to tracks 44 through 79. In the asserted state, the selected RX50 drive reduces the write current. This occurs because there are higher bit densities at the inner tracks.

9.4.2.2 SEL 0 thru SEL 3 Output Signals – These signals select one of four diskettes that the controller interfaces to.

9.4.2.3 TK 00 L Input Signal – This signal indicates that the R/W heads in the selected RX50 drive are located over track 0 (the outermost track). This indicator signal is valid only when a drive is selected.

9.4.2.4 MOTOR PWR ON L Output Signal – This signal controls the spindle motor in the selected RX50 drive. When this signal is asserted, the spindle motor rotates. The spindle motor reaches the rated rotational speed within 1/4 second after an asserted MOTOR PWR ON signal.

9.4.2.5 DIR Output Signal – This signal defines the moving direction of the selected R/W head when STEP output line is pulsed. Step-out (moving away from the center of the disk) is defined as the HIGH level of this signal (logic 1). Step-in (moving toward the center of the disk) is defined as the LOW level of this signal (logic 0).

9.4.2.6 STEP L Output Signal – Each time this signal is pulsed, the R/W heads in the selected RX50 drive move one track. The heads move in the direction specified by the DIR signal. The minimum pulse width is 1 μs. The minimum time between step pulses is 6 ms. This signal is ignored by the drive when WRITE GATE L is asserted, MOTOR ON L is unasserted, or the drive is not selected.

9.4.2.7 WRT DATA L Output Signal – This signal is data to be stored on the diskette. The falling edge of each transition of the signal represents an MFM encoded clock or data pulse. Write pulses should not assert within 500 ns after WRITE GATE is asserted. A minimum of 36 ms head settling time is required after the last STEP pulse occurs. Write pulses are ignored when WRITE GATE or MOTOR ON are unasserted, the diskette is write protected, no diskette is present, or no drive is selected.

9.4.2.8 WG L Output Signal – This signal enables write operations of the selected RX50 drive. This signal is ignored by the drive if the selected diskette is write protected.

9.4.2.9 INDEX L Input Signal – The leading edge of this pulse signal indicates the detection of the index hole in the selected drive side. The INDEX L pulse is valid 250 ms after MOTOR ON L is asserted.

9.4.2.10 WRT PRT L Input Signal – When asserted, this signal indicates that the write enable notch of the selected diskette in the RX50 drive is masked. Writing of new data is also inhibited.

9.4.2.11 RD DATA L Input Signal – This signal is data retrieved from the diskette. RD DATA L is valid 250 ms after MOTOR ON L is asserted, 36 ms after receiving the last STEP L pulse, 1.3 ms after WRITE GATE signal is unasserted, or 30 ms after the drive is selected.

9.4.2.12 READY Input Signal – This signal indicates that a diskette is present in the selected RX50 drive side.

9.5 PROGRAMMING

The RX50 controller module contains eleven registers for communication with the host CPU. Nine registers pass data, commands, and status information between the host processor and the controller. Two registers are command only registers. Addressing either of these registers executes a command but reading or writing data has no affect.

Table 9-8 shows the functions, types, and addresses of the RX50 controller module registers described in this section.

Table 9-8 RX50 Controller Modules Registers

Description	Type	Address
RX5ID identification register	Read only	X00
RX5CS0 CSR 0	R-Status/W-Cmd	X04
RX5CS1 CSR 1	R-Status/W-Cmd	X06
RX5CS2 CSR 2	R-Status/W-Cmd	X10
RX5CS3 CSR 3	R-Status	X12
RX5CS4 CSR 4	R-Status	X14
RX5CS5 CSR 5	R-Status/W-Cmd	X16
RX5DEB data buffer output	Read only	X20
RX5CA clear address register	–	X22
RX5GO start command register	–	X24
RX5FB data buffer input	Write only	X26

NOTE

Address X02 (oct) is reserved for use by the CTI Bus protocol sequence. Writing to this register has no effect on the RX50 controllers operation. Reading this register provides a null word to the host processor.

All communication between the RX50 controller module and the host processor is through these registers. All registers, except the data buffers, are accessed randomly. The data buffers can only be accessed sequentially.

The CPU controls the registers unless the controller is executing a command. The worst case of response time to finish any command is 4 seconds.

The control and status registers (CS0, CS1, CS2, CS3, CS4, and CS5) are used in four modes: command mode, R/W status mode, maintenance status mode, and extended function mode. The command mode allows the host processor to send commands to the controller. The R/W status mode allows the host processor to read the status information of completed read sector or write sector commands. The maintenance status mode allows the host processor to read the status information of a completed maintenance command. The extended functions mode allows the host processor to access extended function commands or status information.

To access the command mode, the host processor writes to CS0, CS1, CS2, CS3, and CS5. Writing to CS4 has no affect on the controller operation. The registers are set up for R/W status mode, maintenance status mode, or are used in the extended status mode during a command mode access to CS0 (Section 9.5.2.1). The selected status mode information can then be read from CS0, CS1, CS2, CS3, and CS4 after the host processor receives a command complete interrupt.

The bit definitions of each CS register mode operation are provided in Sections 9.5.2 through 9.5.7.

9.5.1 RX5ID Identification Register (X00) Description

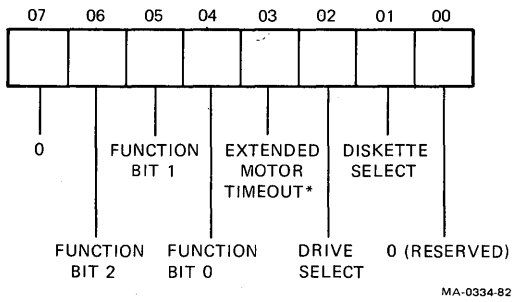
Location X00 contains a unique fixed code that identifies the RX50 controller module to the host processor. This is a read-only register that returns an ID number of 04 (hex) on the BDAL 0–7 lines to the host processor.

9.5.2 RX5CS0 Register (X04) Description

In the command mode, this register is the primary control link between the host processor and the controller. The host processor uses this register to command all functions to be performed by the controller.

This register also selects the registers to contain R/W status information, maintenance status information, or to be used in the extended function mode while in the command mode.

9.5.2.1 Command Mode Bit Definitions – When the host processor writes to this 8-bit register from the BDAL 0–7 L lines, each bit is defined in the following bit map.



Bit 1 and 2 Definition

The following bits select the specified diskette and the function to be performed.

Bit 2	Bit 1	Selected Drive / Diskette
0	0	drive 1 / diskette A
0	1	drive 1 / diskette B
1	0	drive 2 / diskette A
1	1	drive 2 / diskette B

Bit 3 Extended Motor Timeout Definition

This bit allows the host processor to extend the time length that the spindle drive motor rotates after the last disk transfer operation is completed. When this bit is clear, the spindle rotates for 3 seconds after the last R/W command. When it is set, the spindle rotates for 30 seconds after the last R/W command.

Bit 4, 5 and 6 Function Bit Definition

These three bits specify the function the subsystem performs and the mode information retrieved during a read register operation in the following way.

Bit 6	5	4	Function	Mode Type
0	0	0	Read status	Maint status
0	0	1	Main mode	Maint status
0	1	0	Restore drive	Maint status
0	1	1	RX INIT	Maint status
1	0	0	Read sector	R/W status
1	0	1	Extend functions	Extended-R/W status
1	1	0	Read address	R/W status
1	1	1	Write sector	R/W status

READ STATUS (000)
This function instructs the controller to supply the current status of the selected drive and diskette at the current track. During this function, no drives are accessed or restored and no maintenance tests are performed. After this function is completed, an INTRQA is asserted. Valid maintenance status information is contained in RX5CS0–RX5CS4. The primary status of interest for this function is the current status (RX5CS3), which contains the volume changed information. All volume change bits are reset after this command, and INTRQB is re-enabled.

MAINTENANCE MODE (001)
This function instructs the controller to perform an internal self-diagnostic test routine and provide maintenance status information in RX5CS0–RX5CS4 registers.

The host processor obtains a profile of the operational status of the currently installed RX drives. The profile is used mainly for diagnostic exercises and system start-up. After this function is completed an INTRQA is issued. Valid maintenance status information is contained in the RX5CS0–RX5CS4 registers.

RESTORE DRIVE (010)
This function instructs the specified drive to seek to track zero. The host processor restores one drive at a time without performing any R/W operations. Valid maintenance status information is contained in the RX5CS0–RX5CS4 registers.

RX INIT (011)
This function instructs the controller to restore both drives to track zero, check the current drive status, and perform an internal self-test of the controller. This function performs the same operation as the system start-up or asserting the BINIT signal on the CTI BUS. After this function is completed, an INTRQA is issued. Valid maintenance status information is contained in the RX5CS0–RX5CS4 registers.

READ SECTOR (100)
This function instructs the controller to read 512 data bytes from the specified drive, diskette, track, and sector. It then stores the 512 data bytes in the sector buffer (accessed through the RX5EB register by the host processor) and updates the RX5CS0–RX5CS3 registers with R/W status information. After this function is complete, an INTRQA is asserted.

EXTEND FUNCTIONS (101)
This function instructs the controller to access the RX5CS5 (X16) register for the actual function the controller will perform. Refer to Section 9.5.7 for details on the extended function commands.

READ ADDRESS (110)
This function instructs the controller to read the first encountered header at the current track location of the selected drive and diskette. The controller then transfers six bytes to the sector buffer. The six bytes transferred are the TRACK ADDRESS, SIDE ADDRESS, SECTOR ADDRESS, SECTOR LENGTH, HEADER CRC 1 and HEADER CRC 2 in that order. After the function is completed, an INTRQA is asserted. Valid R/W status information is contained in the RX5CS0–RX5CS4 registers. The host processor accesses the sector buffer through the RX5EB register.

WRITE SECTOR (111)
This function instructs the controller to transfer the sector buffer contents (the 512 bytes previously stored in the RX5FB by the host processor) to the specified drive, diskette, track, and sector. The controller then updates the RX5CS0–RX5CS4 registers with R/W status information. After this function is completed, an INTRQA is asserted.

NOTE

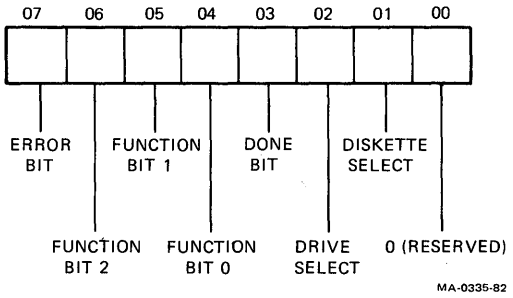
The processor needs no response to the INTRQA (disable INTRQA), and checks the DONE bit instead of INTRQA.

The internal bus is available to the processor after the DONE bit is asserted.

The internal bus is available to the processor 6 μs after INTRQA is asserted.

9.5.2.2 Maintenance Status Mode Definition – The following status information is available to the host processor when the controller executes any maintenance function (function code: 000, 001, 010, or 011). The register contents can be read back from the controller to the host processor. The contents are valid 6 μs after INTRQA is asserted or immediately after the DONE bit is set.

The following are the bit definitions for this register in the maintenance status mode. These bits correspond to the same bits in the RX5CS0 register during a command mode access.



Bit 3 Definition
When asserted, this bit indicates that the controller is not busy and the host processor can access all registers. If the controller is executing a command when the host processor tries to read this register (or any register), a null byte is returned and this bit is unasserted (0 = BUSY, 1 = DONE).

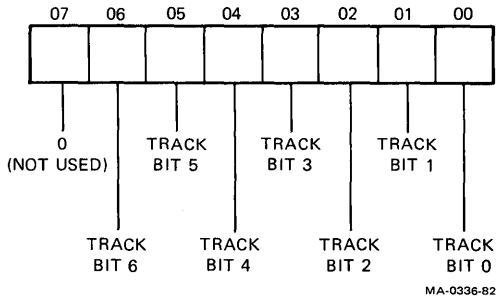
Bit 7 Definition
When asserted, this bit indicates that an error occurred when the controller executed the last function. To determine the cause of the error, the error code in RX5CS1 (error register X06) is read (0 = NO ERROR, 1 = ERROR).

9.5.2.3 Read/Write Status Mode Definition – The contents of this register are the same as in the maintenance status mode when the controller executes any R/W function (function code: 100, 110, or 111). The contents can be read back from the controller to the host processor. The contents are valid 6 μs after INTRQA is asserted or immediately after the DONE bit is set.

9.5.3 RX5CS1 Register (X06) Definition

In the command mode this register is loaded by the host processor with the target track number. In the extended function mode this register is loaded with the number of tracks the formatted diskette contains. This register is selected to contain maintenance status information, read/write status information, or extended function mode status information (Section 9.5.2.1) by command mode accesses to the RX5CS0 register.

9.5.3.1 Command Mode Bit Definitions – In the command mode a data word which specifies the target track, is written to this 8 bit register from the BDAL 0–7 Lines. The range of valid track number that are accepted is 00 to 4F (hex). The following are the bit definitions for this register in the command mode.



9.5.3.2 Maintenance Status Mode Definitions – The following maintenance status information is available to the host processor when the controller executes any maintenance function (function code: 000, 001, 010, or 011). The register contents can be read back from the controller to the host processor. The contents are valid 6 μs after INTRQA is asserted or immediately after the DONE bit is set.

This register contains information describing the cause of the error when the controller executed the last maintenance command. Table 9-9 describes the register contents and the specific maintenance mode function error.

Table 9-9 Maintenance Status Mode Definitions

Octal Code	Error Code Meaning
300	The lower nibble of the RAM failed to pass memory test
310	The higher nibble of the RAM failed to pass memory test
320	No index pulse detected
330	Drive speed not in limit
340	Bad format or a blank disk
350	Stepping error
360	PLL frequency not in limit
370	Data buffer is bad

9.5.3.3 Read/Write Status Mode Definitions – This register contains an error code for the host processor. The error code is issued if an error occurred when the controller executes any R/W functions (function code: 100, 101, 110, or 111) or extended functions (extended function code: 000, 001, 010, 011, 100, 101). The register contents can be read back from the controller to the host processor. The contents are valid 6 μs after INTRQA is asserted or immediately after the DONE bit is set.

Table 9-10 describes the error codes and the related errors.

9.5.3.4 Extended Functions Mode Definition – When this register is used with any extended function command, it contains an error code for the host processor. The error code occurs after the function was commanded to execute (Section 9.5.3.3).

This register mode is used with the set format parameters extended function command (extended function code 011, Section 9.5.7.4). It is loaded by the host processor with the track parameter for reading RX50 and non-RX50 formatted diskettes.

An octal value of 120 reads a diskette with 80 tracks. An octal value of 50 reads a diskette with 40 tracks.

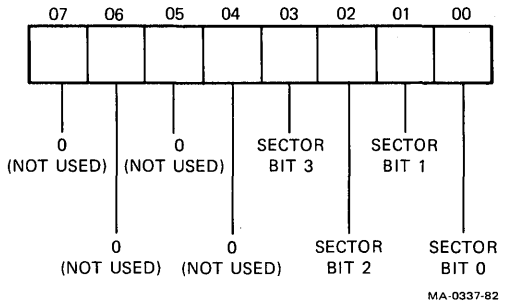
Table 9-10 Read/Write Status Mode Definition

Octal Code	Error Code Meaning
000	No error
010	Drive 0 track 00 sensor fail
020	Drive 1 track 00 sensor fail
030	Both drives failed to respond (no drives in system)
040	Tried to access an unspecified track number
050	Drive fails to see home
060	Data record not found; DAM not found within 43 bytes after ID
070	ID record not found
100	Timeout for FD command done
110	Reserved
120	Selected diskette is not ready
130	Diskette not installed correctly
140	ID CRC
150	Seek error
160	DRQ did not occur within 32 ms
170	Soft ID read error
200	Data CRC
210	Lost data (8051 did not respond to DRQ within 23 μs)
220	Tried to access an unavailable diskette
230	Drive not ready during write command
240	Drive not ready during read command
250	No sector matches the the specified sector
260	Diskette write protected on a write command
270	Tried to access a nonspecified sector number
354	Tried to set unsupported diskette parameters
364	Tried to read a sector with a deleted data mark
374	Tried to write to a non-RX50 formatted diskette

9.5.4 RX5CS2 Register (X10) Definition

In the command mode, this register is loaded by the host processor with the target sector number. This register is selected to contain R/W status information, maintenance status information, or be used in the extended function mode by command mode accesses to the RX5CS0 register.

9.5.4.1 Command Mode Register Definition – In the command mode, a data word which specifies the target sector number is written to this 8-bit register from the BDAL 0–7 Lines. The range of valid sector number that is accepted is 01 to 0A (hex). The following are the bit definitions.



9.5.4.2 Maintenance Status Mode Register Definition – The following status information is available to the processor when the controller executes any maintenance function (function code: 000, 001, 010, or 011). The contents of this register can be read back from the controller to the host processor. The contents are valid 6 μs after INTRQA is asserted or immediately after the DONE bit is set.

This register contains the current head position (track number) of the unit specified in the input command register. The bit definitions are the same as the RX5CS1 register in the command mode.

9.5.4.3 Read/Write Status Mode Register Definition – This register contains status information for the host processor when the controller executes a read sector (function code 100), read address (funtion code 110), and write sector (function code 111) command. The information is also available when the controller executes a read with retries (extended function code 000), a write sector with deleted data mark (extended function code 001), or a read and compare command (extended funtion code 101).

The register contents can be read back from the controller to the host processor. The contents are valid 6 μs after INTRQA is asserted or immediately after the DONE bit is set.

This register contains the track number that was specified in the input track register. The bit definitions are the same as the RX5CS1 register in the command mode.

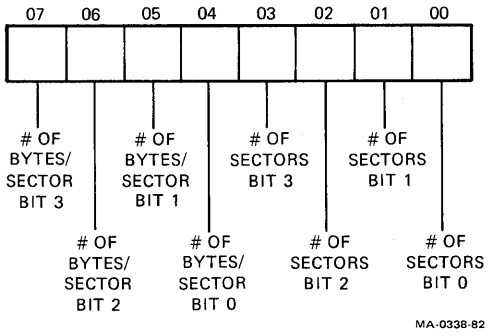
9.5.4.4 Extended Functions Mode Definition – This register mode is used with three extended functions commands: the report format parameters (extended function code 010), the set format parameters (extended function code 011), and the report controller version (extended function code 100) commands. The following paragraphs describe each extended function.

- After executing a report format parameter function (Section 9.5.7.3), this register contains the track quantity of the specified diskette for the host processor. An octal value of 120 indicates a diskette with 80 tracks. An octal value of 50 indicates a diskette with 40 tracks.

- Before executing a set format parameter function (Section 9.5.7.4), the host processor loads this register with a value indicating the sector quantity and capacity of the selected diskette. Bits 4 through 0 should be loaded with an octal value of 11 to select 9 sectors/track, an octal value of 12 to select 10 sectors/track, or an octal value of 20 to select 16 sectors/track. Bits 7 through 5 should be loaded with an octal value of 2 to select 256 bytes/sector or 3 to select 512 bytes/sector.

- After executing a report controller version extended function (Section 9.5.7.5), this register contains an octal number between 0 and 377. This number represents the microcode version of the RX50 controller module for the host processor.

The following shows the bit arrangement.



9.5.5 RX5CS3 Register (X12) Definition

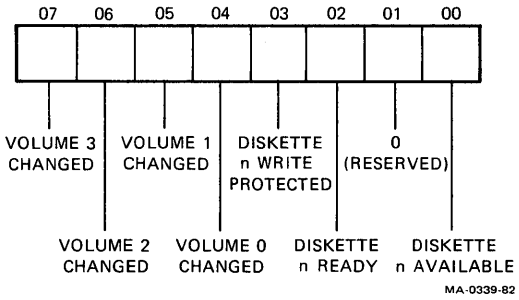
This register is not used in the command mode. It contains the R/W status information, maintenance status information or is used in the extended function mode by command mode accesses to the RX5CS0 register.

9.5.5.1 Maintenance Mode Status Register Definition – The following status information is available to the host processor when the controller executes any maintenance function (function code: 000, 001, 010, or 011). The register contents can be read back from the controller to the host processor. The contents are valid 6 μs after INTRQA is asserted or immediately after the DONE bit is set.

The lower nibble of this register contains the status of the selected drive specified by the input command register. During controller initialization these four bits contain the status of drive 0 side A. If drive 0 does not exist, these bits contain the status of drive 1 side A.

The higher nibble of this register contains the updated volume status since the last Read Status command. The volume status bits are cleared after the Read Status command. During controller initialization, the controller assumes that no media is placed in the drives. The controller tests for disk presence and sets the corresponding VOLUME CHANGED bit if media is detected, but INTRQB is unasserted. INTRQB is enabled after the first Read Status command.

The following are the bit assignments for the maintenance status mode of RX5CS3.



Bit 0 – Unit n Available

0 = The specified unit does not physically exist.
1 = The specified unit does physically exist.

NOTE

Bits 0 and 1 are copied from the respective 2 bits in RX5CS4, SYSTEM CONFIGURATION register for the specified drive and side.

Bit 2 – Unit n Ready

0 = The specified unit is not ready.
1 = The specified unit is ready.

Bit 3 – Unit n Write Protected

0 = The specified unit is not write protected.
1 = The specified unit is write protected.

Bit 4 – Volume 0 Changed

Bit 5 – Volume 1 Changed

Bit 6 – Volume 2 Changed

Bit 7 – Volume 3 Changed

0 = The READY single did not change since the last read status command.
1 = The READY single changed since the last read status command.

Any change in the READY signal from the drive sets the associated volume bit. Only the first change after a Read Status command is executed, asserts an INTRQB. Subsequent changes that occur before the next Read Status command are reported but INTRQB is unasserted. INTRQB is re-enabled after the next Read Status command.

9.5.5.2 Read/Write Status Mode Register Definition – This register mode is available to the host processor when the controller executes a read sector function (function code 100), a read address function (function code 110), and write sector (function code 111) command. The information is also available when the controller executes a read with retries (extended function code 000), write sector with deleted data mark (extended function code 001), or read and compare (extended function code 101) command.

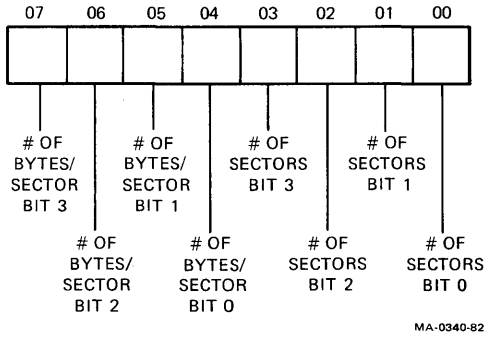
The contents are valid 6 μs after INTRQA is asserted or immediately after the DONE bit is set.

This register contains the sector number that was specified in the input sector register. The bit definitions of this register are the same as RX5CS2 in the command mode.

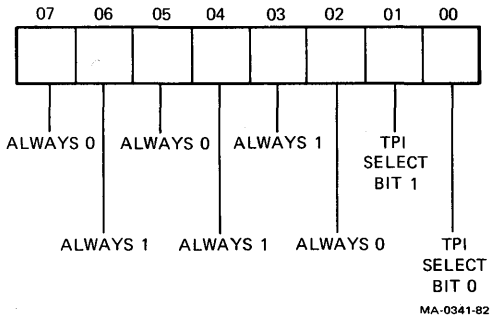
9.5.5.3 Extended Function Mode Register Definition – This register mode is used with the report format parameters (extended function code 010) or the set format parameters (extended function code 011) commands. The following paragraphs describe each extended function.

- After executing a report format parameter function (Section 9.5.7.3), this register contains values which indicate the sector quantity and capacity of the selected diskette for the host processor. Bits 4 through 0 contain an octal value of 11 to indicate 9 sectors/track, an octal value of 12 to indicate 10 sectors/track, or an octal value of 20 to indicate 16 sectors/track. Bits 7 through 5 contain an octal value of 2 to indicate 256 bytes/sector or 3 to indicate 512 bytes/sector.

The following shows the bit arrangement.



- Before executing a set format parameter function (Section 9.5.7.4), the host processor loads this register with a value to select the track density of the selected diskette. A value of 1 (octal) for bits 1 and 0 selects a 48 track/inch diskette. A value of 2 (octal) selects a 96 track/inch diskette. The remaining bits must be set as indicated in the bit arrangment below.



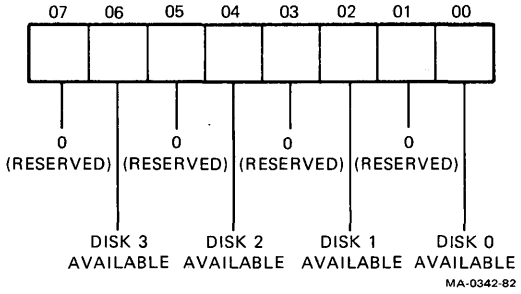
9.5.6 RX5CS4 Register (X14) Definition

This register is not used in the command mode. It contains R/W status information, maintenance status information or is used in the extended function mode as specified by command mode accesses to the RX5CS0 register.

9.5.6.1 Maintenance Status Mode Register Definition – The following status information is available to the host processor when the controller executes any maintenance function (function code: 000, 001, 010, or 011). The register contents can be read back from the controller to the host processor. The contents are valid 6 μs after INTRQA is asserted or immediately after the DONE bit is set.

This register contains a summary of the RX configuration that is available for use by the host processor. It is arranged in four groups of two bits each. Each group contains the status of each of the four possible drive sides. It is updated when the controller is initialized.

The following are the bit assignments for the maintenance status mode of RX5CS4.



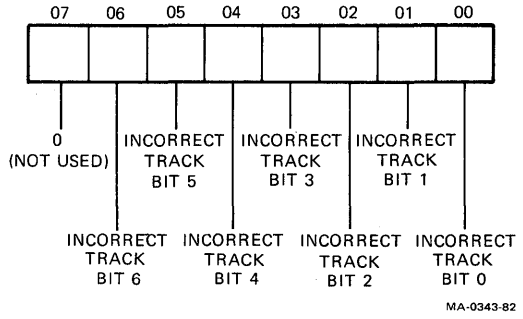
For all AVAILABLE bits:
0 = The disk does not physically exist.
1 = The disk does physically exist.

9.5.6.2 Read/Write Status Mode Register Definition – The following status information is available to the host processor when the controller executes a read sector function (function code 100), a read address function (function code 110), and write sector (function code 111) command. The information is also available when the controller executes a read with retries (extended function code 000), write sector with deleted data mark (extended function code 001), or read and compare (extended function code 101) command.

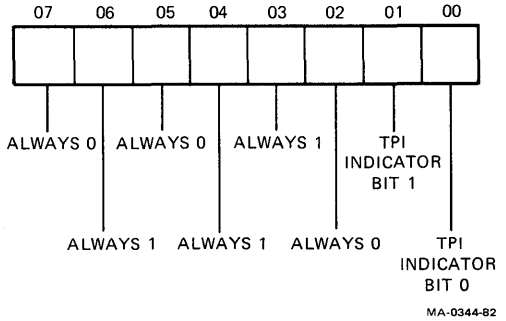
The register contents can be read back from the controller to the host processor. The contents are be valid 6 μs after INTRQA is asserted or immediately after the DONE bit is set.

The contents of this register are valid only when a SEEK error occurs while executing a command. This register contains the track address of the R/W heads location. If no SEEK error occurs, it contains all zeros.

The following are the bit assignments for the R/W status mode of RX5CS4.



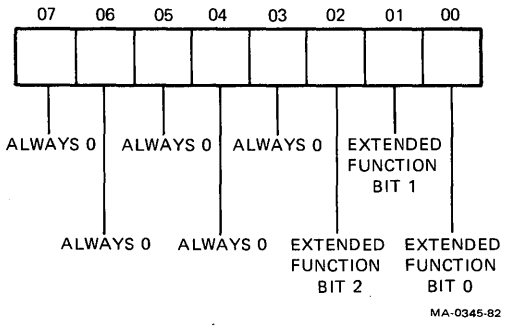
9.5.6.3 Extended Function Mode Register Definition – This register mode is used with the report format parameters (extended function code 010). After executing a report format parameter function (Section 9.5.7.3), this register contains a value which indicates the track density of the selected diskette for the host processor. A value of 1 (octal) for bits 1 and 0 selects a 48 track/inch diskette. A value of 2 (octal) selects a 96 track/inch diskette. The remaining bits must be set as indicated in the bit arrangment below.



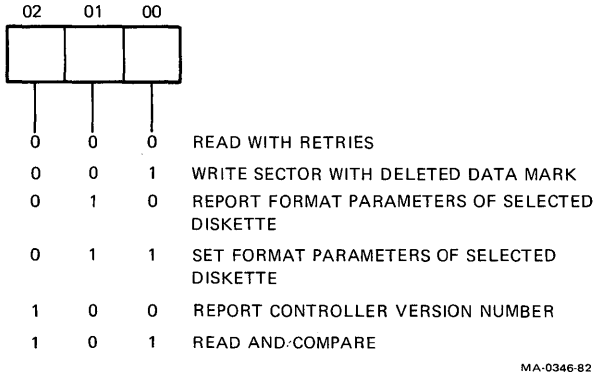
9.5.7 RX5CS5 Register (X16) Definition

This register selects the extended functions command to be executed when an extended functions (function code: 101) command is indicated in the RX5CS0 register. The host processor loads this register with one of six codes to select one of six extended functions.

The following are the bit definitions for this register.



The following are the selectable extended functions.



9.5.7.1 Read With Retries Definition (000) – This extended function is the same as the read sector function except that the controller repeats the read sector operation up to ten times until it finds a good sector. Retries are performed when an ID CRC, DATA CRC, DATA RNF or LOST DATA errors are detected.

If an error is detected in all 10 retries, an INTRQA is asserted with the error bit set. The error register (RX5CS1) contains the error code representing the last error occurrence. If a bad sector is detected, and a good sector is subsequently encountered, INTRQA is asserted and the error bit is cleared. The error register contains the appropriate error code for diagnostic purposes. The number of retries is not provided.

If no error is detected the RX5CS0 through RX5CS4 registers contain the standard R/W status information as previously described.

9.5.7.2 Write Sector With Deleted DATA MARK (001) – This extended function operates the same as a write sector function except the deleted data mark is set in the sector header. Data is written from the sector buffer to the target track and sector as in the write sector function.

Executing a read sector function or read sector with retries extended function with a deleted data mark in the target track and sector results in an error with code 364. The data is read and then placed into the sector buffer for the host processor.

After completing this command, the RX5CS0 through RX5CS4 registers contain the standard R/W status information as previously described.

9.5.7.3 Report Format Parameters of Selected Diskette (010) – This extended function and the set format parameters extended function read non-RX50 formatted diskettes. Four types of formatted diskettes are allowed: the RX50 formatted diskettes and three types of non-RX50 formatted diskettes.

NOTE

The report format parameters and set format parameters extended functions allow for data retrieval from diskettes. Data storage is allowed only on RX50 formatted diskettes. Attempts to store data on a non-RX50 formatted diskette result in an error with code 374 in RX5CS1.

All diskettes must be single-sided, soft-sectored, and use the MFM recording technique. The following diskette formats are allowed.

Format Type	TPI	Total Tracks	Sectors/ Track	Bytes/ Sector
RX50	96	80	10	512
Alternate	48	40	10	512
Alternate	48	40	9	512
Alternate	48	40	16	256

The detected parameters are indicated in the RX5CS2, RX5CS3, and RX5CS4 registers after the function is executed. Refer to Sections 9.5.4.4, 9.5.5.3 and 9.5.6.3 for further information.

9.5.7.4 Set Format Parameters of Selected Diskette (011) – This extended function and the report format parameters extended function read non-RX50 formatted diskettes. Four types of formatted diskettes are allowed: the RX50 formatted diskettes and three types of non-RX50 formatted diskettes.

NOTE

The report format parameters and set format parameters extended functions allow for data retrieval from diskettes. Data storage is allowed only on RX50 formatted diskettes. Attempts to store data on a non-RX50 formatted diskette result in an error with code 374 in RX5CS1.

All diskettes must be single-sided, soft-sectored, and use the MFM recording technique. The following diskette formats are allowed.

Format Type	TPI	Total Tracks	Sectors/ Track	Bytes/ Sector
RX50	96	80	10	512
Alternate	48	40	10	512
Alternate	48	40	9	512
Alternate	48	40	16	256

To select the parameters of the desired diskette, the host processor loads the RX5CS1, RX5CS2, and RX5CS3 registers before a read sector function or read and compare function is executed. Refer to Sections 9.5.3.4, 9.5.4.4 and 9.5.5.3 for further information.

Any attempt to set the diskette format to a type not previously listed causes an error with a code of 354.

9.5.7.5 Report Controller Version Number (100) – After executing this extended function, the RX5CS2 register contains an octal number between 0 and 377. This number represents the microcode version of the RX50 controller module for the host processor.

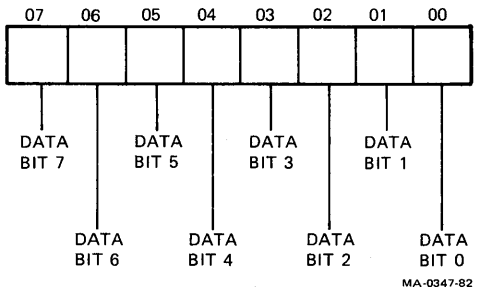
9.5.7.6 Read and Compare (101) – This extended function is similar to a read sector function except the host loads the sector buffer with data. Each byte read from the diskette is compared to its corresponding byte in the sector buffer. If the comparison fails for any byte, the error bit is set and an error code of 374 is located in the RX5CS1 register.

After completing this command, the RX5CS0 through RX5CS4 registers contain the standard R/W status information as previously described.

9.5.8 RX5EB Empty Data Buffer Register (X20) Definition

This 8-bit wide 512-byte data buffer can be read by the host processor from the BDAL 0–7 L lines any time the controller is not executing a command. Refer to Section 9.5.9 for further information on the sector data buffer.

The following are the bit assignments for the RX5EB.



9.5.9 RX5CA Clear Address Register (X22) Definition

Any access to this register by the host processor clears the sector data buffer address to zero.

The host processor and the controller use a 512-byte sector buffer as an intermediate storage area for writing and reading sector information to and from the disk. The controller performs automatic address sequencing after each sector buffer access.

The address should be reset to zero before the host processor starts to either fill (access RX5FB X26) or empty (access RX5EB X20) the sector buffer. The fill or empty operations continue from the last accessed location if no intermediate clear address is issued.

The buffer is exactly 512 bytes long. Continued accesses after the 512th byte returns the pointer to location zero. Specific address information is not available for reading by the host processor.

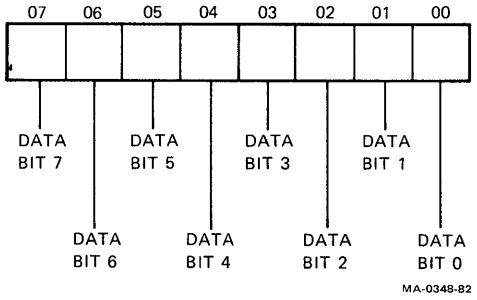
9.5.10 RX5GO Start Command Register (X24) Definition

If the host processor accesses this register, the controller executes the function specified in the command registers. When commanding any function, this access should be the last in a series of instructions issued by the host processor. When the host processor accesses this register, the controller gains control of the internal bus. After the controller finishes executing the command, it asserts INTRQA, then 6 μs later, the host processor gains control of the controller. The host processor can also gain control of the controller after the DONE bit is set.

9.5.11 RX5FB Fill Sector Buffer Register (X26) Definition

This 8-bit wide, 512-bytes sector buffer can be written to by the host processor from the BDAL 0–7 L lines any time the controller is not executing a command. Refer to Section 9.5.9 for further information on the sector data buffer.

The following are the bit assignments for the RX5FB.



9.5.12 Command and Status Register Summary

Table 9-11 shows a summary of the RX4CS0 through RX5CS4 command and status register.

Table 9-11 Command and Status Register Summary

Register Write	Command Read	R/W Status	Maintenance Read	Extended Functions Read	Write
RX5CS0	Function	Function	Function	Function	Function
RX5CS1	Track*	Error code	Error code	Error code	Tracks¶
RX5CS2	Sector*	Track	Current track	Tracks/Version‡	Sect+Bytes/Sect§
RX5CS3	None	Sector	Current status	Sect+Bytes/Sect§	TPI
RX5CS4	None	Incorrect track†	System configuration	TPI	None
RX5CS5	Extended	0 none	0 none	Extended	Extended

* Only used on R/W sector commands
† Only valid when Seek Error occurs
‡ Number of tracks or version number
§ Number of sectors and bytes per sector
¶ Number of tracks only

9.6 GENERAL SEQUENCE OF OPERATION

The following is the sequence for command and status operations. The host processor issues a command. The controller processes and executes the command internally. The controller then asserts an INTRQA and DONE BIT. The host processor responds to either the INTRQA or the DONE BIT by reading the status registers to determine the results of the previously issued command.

The controller asserts INTRQA after all functions are completed. The controller uses INTRQB to alert the host processor of VOLUME changes.

Status items in the RX5CS0 register are always located in the same place. For example, bits 0–2 contain the unit selected, bit 3 is the DONE BIT, bits 4–6 contain the specified function, and bit 7 is set if an error occurred in the last command.

The RX5CS1 always contains an error code associated with the last command selected to execute. If the command is executed correctly, this register is cleared. However, if the command is a READ WITH RETRY command, then this register contains the error code of the error that occurred last. If error bit in RX5CS0 is reset, it indicates that the command is completed. The RX5CS1 might still contain the error code of the last retry error before completion.

While the controller is busy, any DATA-OUT addressed to the controller is ignored, however a normal BUS REPLY is issued; any DATA-IN addressed to the controller results in a null response byte and a normal BUS REPLY.

The controller performs automatic scanning of ready status of all drive sides. If the host processor does not issue any other commands within 1.3 ms after the completion of the last command, then scanning is performed every second. Any changes in the ready status of any drive side are reported to the host processor as a volume change through the INTRQB signal. For proper operation, the operating system should respond to an INTRQB with a read status function. This updates the current status register with the changed status and clears the volume changed bits after the completion of the command. The controller issues only one INTRQB between read status commands, regardless of how many volume changes are detected.

If the READY signal of the selected unit changes while executing a command, then the command is aborted, the error bit is set and the error register contains the appropriate error code.

On controller initialization, the CURRENT STATUS register indicates which volumes are currently installed in the drives.

NOTE
If no commands are issued by the host processor within one second after the completion of the last command, all drive sides are de-selected.

9.6.1 Read/Write Operations

The host processor can store or retrieve data blocks of 512 8-bit bytes on one of the available drive side volumes. To store a data block, the host processor transfers the 512 bytes from the system memory to the sector data buffer contained in the controller.

A single CTI BUS address, RX5EB register (X20), accesses the sector data buffer for read operations. A single CTI BUS address, RX5FB (X26), accesses the sector buffer for write operations. Accesses to these registers increments the internal sector data buffer pointer after each byte is transferred.

The sector data buffer is cleared by accessing the RX5CA (X22). The host processor specifies one of the 80 tracks to be the target track by loading the track number into the track register (RX5CS1 X06). It then specifies one of the ten sectors to be the target sector by loading the sector number into the sector register (RX5CS2 X10).

The host processor assembles the parameters required to complete the desired transfer in the RX5CS0 register (X04). The host processor can load these registers in any order. To start the command, the host processor accesses the RX5GO (X24) register, then waits for INTRQA or DONE bit to signal the end of the command.

The following is a sample sequence the host processor would perform for a Write Sector command.

1. Accesses the RX5CA. This clears the data buffer address to zero.
2. Loads the RX5DB with the 512 data bytes to be stored.
3. Loads the RX5CS0 with the selected drive, function, and motor timeout option.
4. Loads the RX5CS1 with the target track.
5. Loads the RX5CS2 with the target sector.
6. Accesses the RX5GO. This executes the command.
7. Reads the RX5CS0 register when the controller asserts an INTRQA or DONE bit. This determines the status on completion of the command.

9.6.1.1 Read/Write Status – There are 5 bytes of status available to the host processor after the controller completes a Read Address, Read, or Write Sector command. These are contained in RX5CS0 through RX5CS4.

To determine successful disk transfers, the host processor reads the error bit in RX5CS0. This checks for errors and the execution of the correct function to the correct volume. If an error is detected, the host processor repeats the function or investigates the error cause using the second byte available in the error register (RX5CS1). The next 2 available bytes verify that the function occurred on the track and sector (RX5CS2 and RX5CS3) that was specified in the command registers. The last of the 5 bytes contains the incorrect track number (RX5CS4). This is valid only when a seek error occurs. If a seek error did not occur in the last operation it will be all zeros. The incorrect track number is also the current head position when a seek error occurred.

NOTE

If a seek error occurs, the controller automatically identifies the R/W head position. The host processor does not have to restore the drive to reposition the R/W heads but continues to issue the next command. If a seek error occurs several times, then the host processor might need to restore the drive.

9.6.2 Maintenance Operations

The host processor can direct the controller to execute an internal self-test. To do this it specifies the maintenance mode function in the RX5CS0 (function code 001) and accesses the RX5GO register. Neither drive is restored. Status information is contained in the RX5CS0 through RX5CS4 registers. An INTRQA or DONE bit indicates a completed function.

9.6.2.1 Maintenance Status – When the maintenance function is completed, the RX5CS0 through RX5CS4 registers contain the following profile of the current RX subsystem and its operational status.

RX5CS0 – contains the DONE indication and the ERROR flag from the self-test. The SELECT field contains the VOLUME as specified in the input command. The FUNCTION field contains the function as specified in the command (code 001).

RX5CS1 – contains the specific error code if an error occurred.

RX5CS2 – contains the current track address used during the Maint command.

RX5CS3 – contains a status summary of the VOLUME under test.

RX5CS4 – contains a copy of the SYSTEM CONFIGURATION that was connected at initialization.

RX5RDB – contains an incrementing pattern from 00 to FF and then a decrementing pattern from FF to 00 (hex). The host processor reads this as a final check of the data buffer integrity after a maintenance function. The data buffer contains the same pattern during controller initialization. Failure to detect this pattern indicates that a portion of the internal RAM test failed.

9.6.3 Controller Initialization and Self-Test Sequence

Table 9-12 summarizes the initialization and self-test operations the controller perform when certain commands are executed.

Table 9-12 Controller Initialization and Self-Test Sequence

Activity	Read Status (000)	MAINT Mode (001)	Restore Unit (010)	RX INIT (011)	Power-up Bus INIT P OK
Drives restored	None	None	1*	2	2
Read media	No	Yes	No	No	No
Track 00 check	No	No	Yes	Yes	Yes
Memory check	No	Yes	No	Yes	Yes
PLL check	No	Yes	No	Yes	Yes
Step check	No	Yes	No	No	No
Format check	No	Yes	No	No	No
Speed check	No	Yes	No	No	No
Update current status register	Yes (A)	Yes (B)	Yes (B)	Yes (C)	Yes (C)
Update system configuration register	No	No	Yes	Yes	Yes

NOTES

1. **Resets VOLUME CHANGED bits after the command.**
2. **VOLUME CHANGED bits are not reset after the command.**
3. **Resets VOLUME CHANGED bits. In this case the controller sets the bits that indicates the presence of a volume.**

* The controller restores the drive specified in the command register.

9.7 SPECIFICATIONS

The following paragraphs provide the specifications for the RX50 controller.

9.7.1 Electrical Characteristics

Power Dissipation

+5 Vdc ±5%
50 mV ripple maximum
800 mA maximum
4 Watts

+12 Vdc ±5%
100 mV ripple maximum
35 mA maximum
0.42 Watts

−12 Vdc ±5%
100 mV ripple maximum
35 mA maximum
0.42 Watts

9.7.2 Environmental Characteristics

Specification	Minimum	Maximum
Temperature	10° C (50° F)	50° C (104° F)
Humidity	10%	90%
Wet bulb reading	–	28° C (82° F)
Dew point	2° C (36° F)	–
Temperature fluctuation	–	20° C/hour 36° F/hour

9.7.3 Physical Characteristics

Dimensions

Width	1.27 cm (0.5 in)
Length	20.32 cm (8 in)
Height	13.21 cm (5.2 in)
Weight	200 grams (7.2 ozs)
Cable length	10 feet maximum #28 AWG flat ribbon cable

Interface connector

CTI connector	60-pin ZIF connector (PN 12-18818-00)
RX connector	34-pin connector AMP 10216-8 or equivalent (PN 12-18762-00)

CHAPTER 10
RX50 DUAL DISKETTE DRIVE

10.1 GENERAL INFORMATION

The RX50 dual diskette drive is the storage component of the RX50 controller and drive subsystem for the Professional 350 System. Figure 10-1 shows its relationship to the other components which make up the Professional 350 system.

10.1.1 Related Documentation

For further information on the RX50 drive, refer to the following documents.

Title	Document No.
Professional 350 Field Maintenance Print Set	MP-01394-00

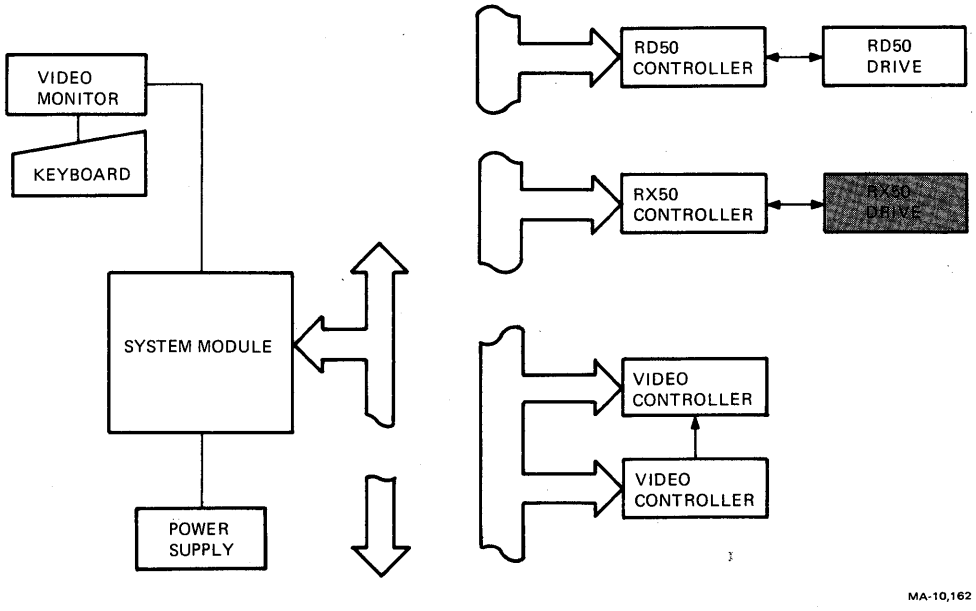


Figure 10-1 RX50 Dual Diskette System Relation

10.1.2 Introduction

The RX50 drive is a field replaceable unit (FRU PN RX50-AA) that mounts in the Professional 350 system box. One cable connects the RX50 drive to a controller (see RX50 Controller Module description in Chapter 9). One power cable (FRU PN 17-00281) connects the power supply to the RX50 drive.

The RX50 drive is a field replaceable part rather than a field repairable part. No adjustment or alignment procedures are provided in this chapter because of the test equipment required. The RX50 drive is adjusted and aligned at the time of manufacture.

10.1.3 Physical Description

Figure 10-2 shows the RX50 drive. The front bezel has two access slots with swinging doors to insert or remove diskettes. A head load indicator for each diskette slot lights when that unit is busy.

NOTE

Do not open either access door if either indicator is lit. This damages data stored on either diskette.

Internally, the drive has two counter-rotating spindles. The spindles are belt-driven by a single dc motor/ tachometer combination.

Each diskette has a read/write (R/W) head located back-to-back between the diskettes on a head carriage assembly. The heads are positioned over each track by a single stepper motor/lead screw combination.

The electronic components are mounted on three printed circuit modules. All motors and sensors plug into these modules. The power and interface cables from the controller plug into one of the circuit modules from the top rear of the RX50 drive.

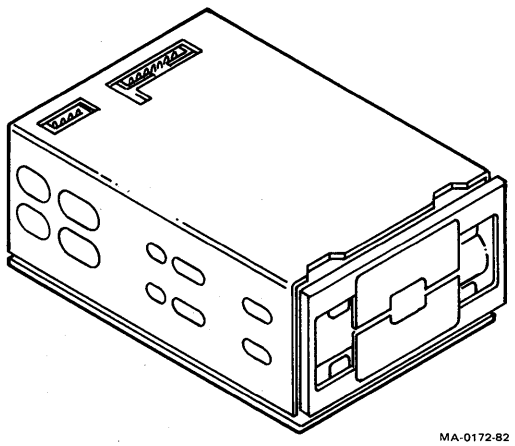


Figure 10-2 RX50 Dual Diskette Drive

10.1.4 Diskette Description

The RX50 drive uses standard 5.25 inch (133.4 mm) square diskettes (Figure 10-3). The recording media is a magnetic oxide coated flexible mylar disk, 5.125 inches (130.2 mm) in diameter. It is contained inside a protective jacket.

The media rotates freely inside the jacket and is continuously cleaned by the soft fabric liner of the jacket. The jacket has four openings: one each for the spindle, the R/W heads, the write protect sensor, and the index sensor.

The write protect opening is a small square notch along one side of the jacket. When this opening is covered, the diskette is write protected. For further information see Section 10.1.5.2.

10.1.5 Operating Procedures

The following paragraphs describe the diskette operating procedures.

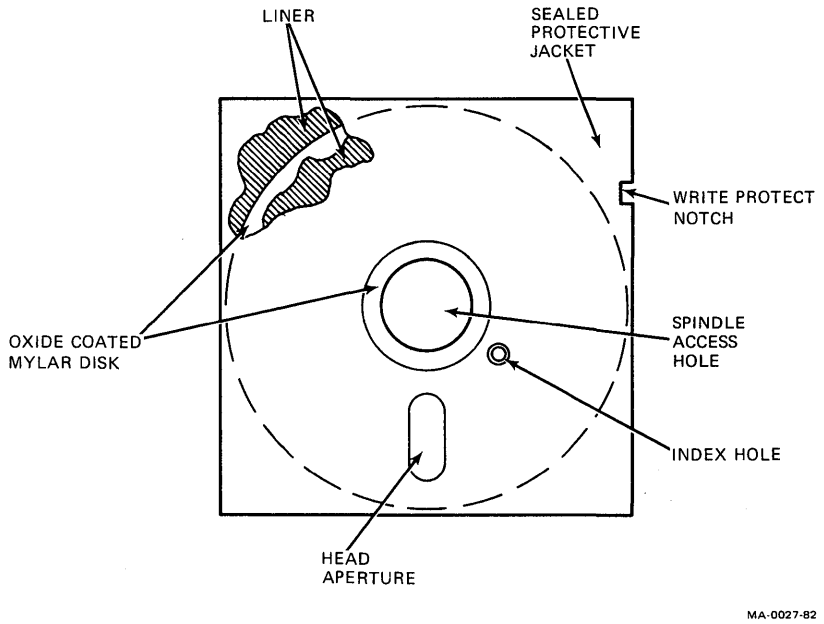


Figure 10-3 The 5.25 Inch Diskette

10.1.5.1 Diskette Handling and Storage – Improper handling or storage of diskettes can destroy recorded data and damage the R/W head. The following are some suggestions for diskette handling.

- Always return the diskette to its protective envelope when it is not installed in the RX50 drive.
- Always store diskettes vertically and loosely to prevent warping the jackets.
- Always mark the diskette jacket with a felt tip pen. Using a pencil or ballpoint pen creases the jacket and damages the mylar media inside.
- Always insert the diskette into the drive carefully. Never force the door closed if it seems to be stuck. This could crush your diskette.
- Never remove or insert a diskette if either indicator is lit.
- Never open or close the diskette door if either indicator is lit.
- Never touch the mylar recording surface where the jacket is cut away for the R/W heads. Fingerprints dirty the R/W heads and can cause data errors.
- Never store diskettes in direct sunlight or near heaters where temperatures go above 52° C (125° F). High temperatures warp the jackets.
- Never bend or fold the diskette jacket.
- Never bring the diskette near any strong magnetic fields (5 gauss or more) or touch the diskette with any steel objects. This could erase or weaken the data on the diskette.

10.1.5.2 Write Protection of Diskettes – The RX50 drive is equipped with a write protect feature that protects the diskette from accidental writing. To write protect a diskette, cover up the write protect notch on the side of the jacket. Most diskettes come with a package of adhesive-backed write protect tabs.

If write protect tabs are not available, ordinary adhesive-backed labels may be substituted. Figure 10-4 shows how to install write protect tabs.

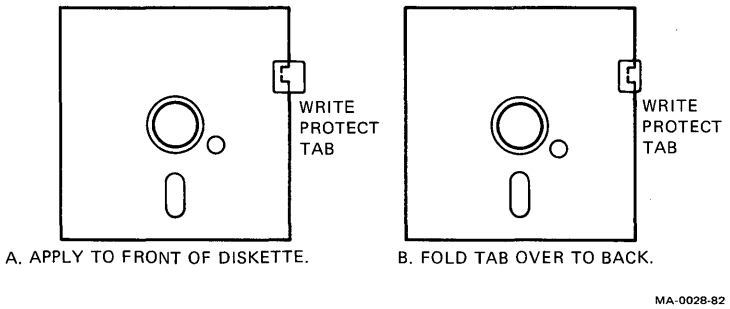


Figure 10-4 Write Protect Tab Application

10.1.5.3 Diskette Loading/Unloading

NOTE
Do not open either of the RX50 drive doors if either indicator is lit.

To load a diskette into the RX50 drive, perform the following procedure.

1. Make sure that both indicators are not lit.
2. Open the door of the desired drive side.
3. Properly orient the diskette to the slot.
4. Insert the diskette until it hits a solid stop.
5. Close the door.

To open the door, press on the door half closest to the outside of the drive (Figure 10-5). The diskette should be oriented so that the R/W head access slot in the jacket is inserted into the drive first. The drive records on the surface of the diskette closest to the center of the drive (Figure 10-6).

To close the door, gently push the end of the door toward the center of the drive until it is flush with the front bezel (Figure 10-7). Each of the head load lamps on the front bezel light when the controller is accessing the diskette on the indicated side.

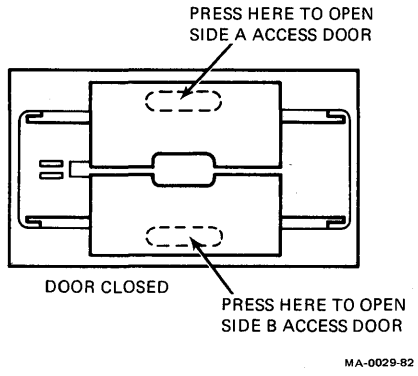


Figure 10-5 Opening Access Doors

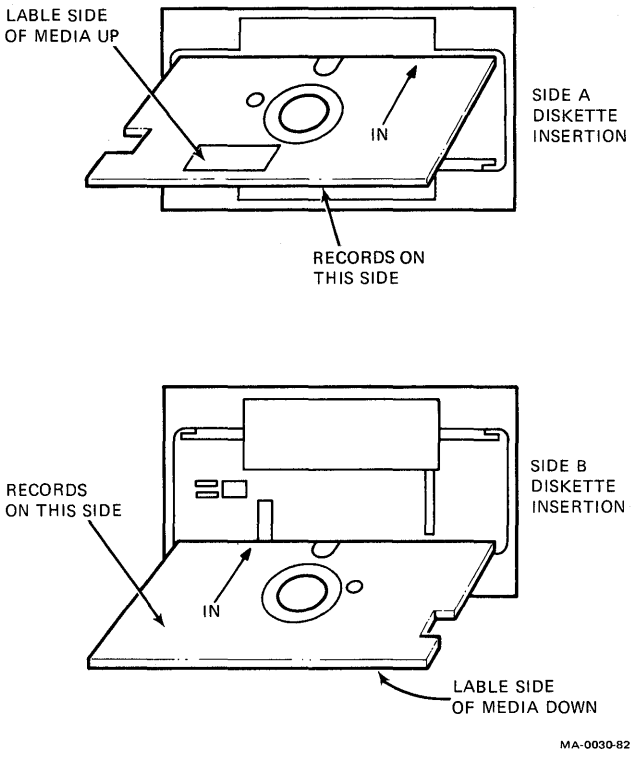


Figure 10-6 Inserting Diskette

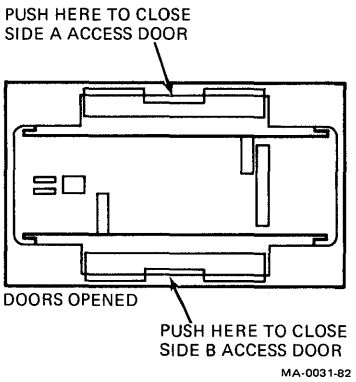


Figure 10-7 Closing Access Doors

10.1.6 Configuration Options

An RX50 dual diskette drive can be configured to be selected by one of two groups of select signals from the controller.

One configuration of the RX50 drive, requires no jumper on connector J17 (see Section 10.4.5.7). This enables controller signals DRIVE SEL 0 and DRIVE SEL 1 to select circuits in the drive (see Section 10.3.2.1).

The other configuration of the RX50 drive requires a jumper (PN 12-14314-00) installed on connector J17. This enables controller signals DRIVE SEL 2 and DRIVE SEL 3 to select circuits in the drive.

10.2 FUNCTIONAL COMPONENTS

Figure 10-8 is a simple block diagram of the RX50 drive. It shows the general operation and data flow of the drive.

The RX50 drive contains the following elements to perform read, write, and seek operations.

- Seek and interface module
  Select circuits
  Status circuits
  Stepper motor circuit
  Read/write interface circuits
- Motor control module
  Motor control circuit
- Spindle motor
- Two head load solenoids
- Diskette sensors
- Stepper motor
- Read/write (R/W) module
  Write circuits
  Read circuits
- Two read/write heads

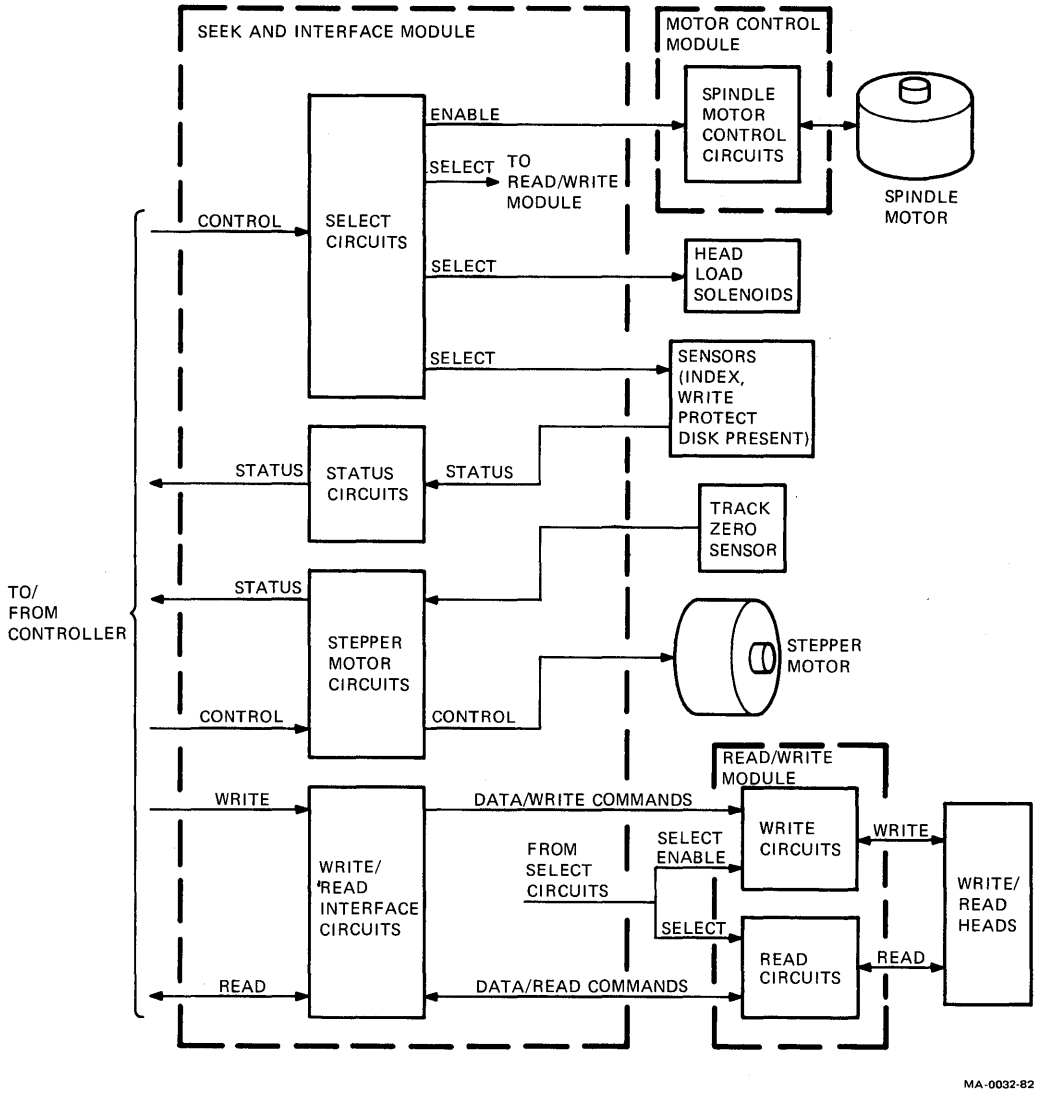


Figure 10-8 Simple Block Diagram

10.2.1 Seek and Interface Module Functions

The seek and interface module contains the following circuits.

- Select circuits
- Status circuits
- Stepper motor circuits
- Read/write interface circuits

The select circuits act as an interface between the controller and the RX50 drive. These circuits perform the following functions.

- Enable the motor control module.
- Select the head load solenoids.
- Select the sensors.
- Select and enable the circuits in the R/W module.

The status circuits interface the sensors to the controller. These circuits pass status signals to the controller from the selected sensors.

The stepper motor circuits interfaces the controller to the stepper motor. These circuits convert controller signals to stepper motor control signals.

The R/W interface circuits interfaces the controller and the R/W module. For a write operation, these circuits pass data and commands from the controller to the R/W module. For a read operation, these circuits pass commands from the controller to the R/W module and data from the R/W module to the controller.

10.2.2 Motor Control Module and Spindle Motor Function

The motor control module contains spindle motor control circuits that control the rotational speed of the spindle motor. These circuits are enabled to rotate the spindle motor or disabled to stop the spindle motor by select circuits.

When enabled, these circuits provide current to the spindle motor to keep it rotating at a constant speed. When disabled, these circuits inhibit current to the spindle motor so it does not rotate.

As the spindle motor rotates, a belt drives two counter-rotating spindles. Each spindle rotates the media in a diskette.

10.2.3 Head Load Solenoid Function

The RX50 drive contains two head load solenoids, one for each R/W head. The selected solenoid releases the head load arm and pad. This applies pressure to the surface of the media and brings the R/W head in contact with the media.

10.2.4 Sensor Functions

The RX50 drive contains two groups of sensors, one group for each side. A sensor group is selected by the select circuits. Each sensor group senses the following conditions.

- The presence of a diskette
- The write protection status of a diskette
- The index of a diskette
- Track zero home position

10.2.5 Stepper Motor Function

The RX50 drive contains a stepper motor that positions R/W heads over a data track. The motor is controlled by the stepper motor circuits. As this motor rotates, a head carriage assembly, moving in a linear plane, moves the R/W heads over the media.

10.2.6 Read/Write Module Function

The R/W module contains both read and write circuits. The read circuits convert the analog data sensed by the R/W heads to digital data. The write circuits generate the write currents for the R/W heads to record data on the media.

The read circuits receive a select signal from the select circuits. The select circuits select one of the two R/W heads. A read command from the R/W interface function then enables the read circuits to pass read data to the R/W interface circuits.

The write circuits are enabled by the select circuits. The select circuits select one of the two R/W heads. The write data and commands from the R/W interface circuits then control the currents generated by the write circuits for the heads.

10.2.7 RX50 Drive Set-up Sequence

Prior to read and write operations, the following set-up sequence must be performed.

1. Execute a restore unit command. This turns on the spindle motor and causes it to seek track zero. For further information, refer to Chapter 9, the RX50 controller module.

2. Load the target track and sector registers. For further information, refer to Chapter 9.

3. Execute a read or write sector command. This causes the heads to load and the stepper motor to seek the target track. For further information, refer to Chapter 9.

10.3 THEORY OF OPERATION

The following paragraphs describe the operation of the RX50 drive.

10.3.1 Drive Mechanism Detailed Operation

The following section describes the mechanical operations of the RX50 drive. These operations use mechanisms which orient the diskettes, allow the modules to read and write to the diskette, and perform seek operations. These mechanisms are discussed in the following paragraphs.

- Diskette positioning
- Spindle drive
- Head positioning
- Head load
- Sensors

Figure 10-9 is an exploded view showing the mechanical detail of the drive. Figure 10-10 shows the functional detail of the drive.

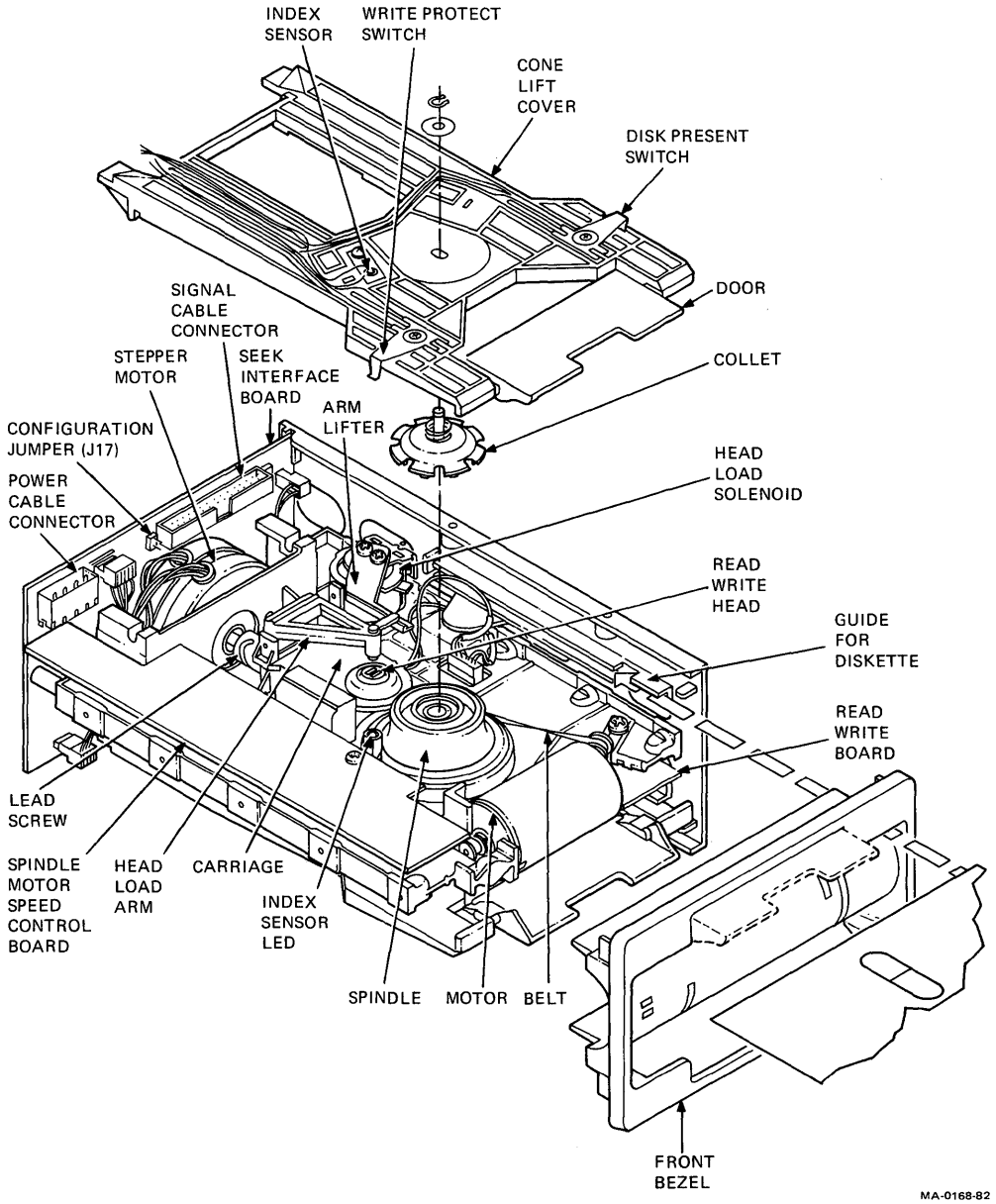


Figure 10-9 Mechanical Detail

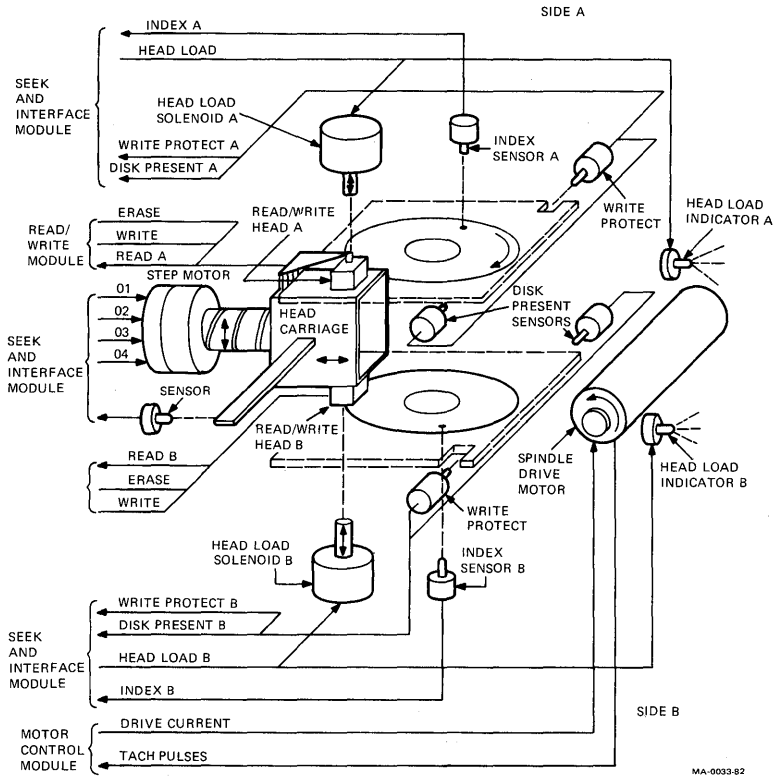
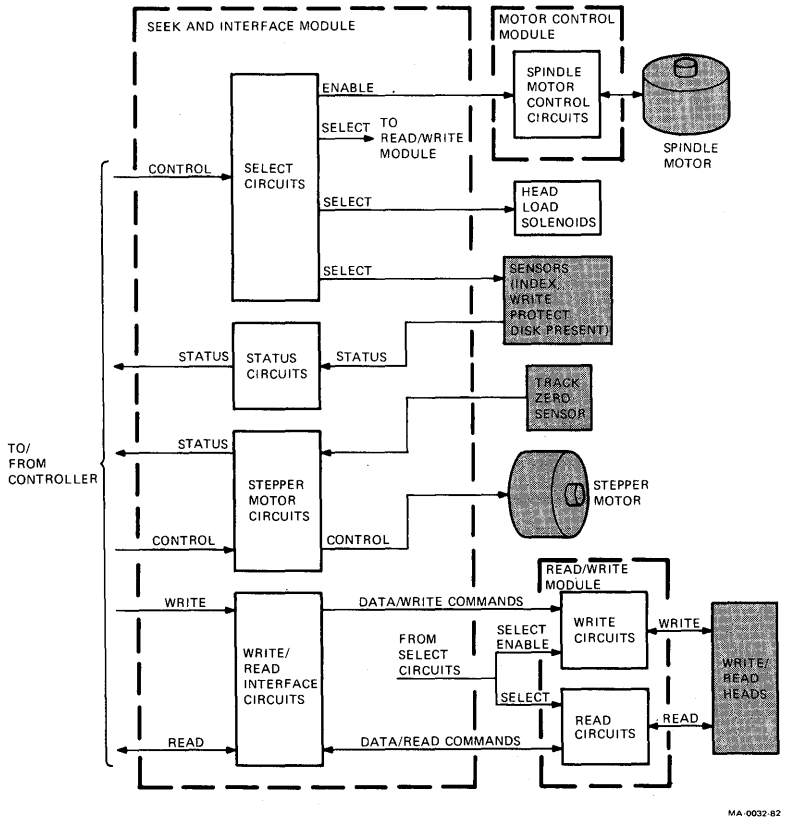


Figure 10-10 Mechanical Operation Detail



10.3.1.1 Diskette Positioning Mechanism – If the front door is open on either side A or B, a diskette slides easily in or out of the drive on grooves. These grooves are in the drive's side panels and have a solid backstop to position the diskette.

Each front door operates a cone lift cover. When the door is closed, the cone lift cover moves over the diskette. A collet, on the cone lift cover, clamps the media to the spindle through the diskette jacket cutout.

The diskette lightly presses against a reference plane near the R/W head. This ensures proper head to media height. The plane pushes the soft jacket liner against the media. This wipes the media surface clean before it comes into contact with the R/W head.

Positioning the diskette in each drive side, brings the switches in contact with the diskette. The switches pass status information, disk presence and write protection, to the seek and interface module. For further information see Section 10.3.1.5.

10.3.1.2 Spindle Drive Mechanism – The drive contains two counter-rotating spindles, one for each drive side. A single 12 Vdc spindle motor-tachometer combination drives the spindles with a belt. The motor operates at 1800 rpm while the spindles rotate at 300 rpm.

The motor control module keeps the motor rotating at a constant 1800 rpm. The module compares the tachometer pulses coming from the motor to a constant reference. This comparison determines the motor's current requirements provided by the motor control module. For further information on the motor control modules see Section 10.3.3.

10.3.1.3 Head Positioning Mechanism – A stepper motor control circuit on the seek and interface module controls a four-phase motor. The stepper motor positions the R/W heads over the data tracks on the media by rotating a grooved step cam lead screw. This positions a head carriage assembly over the 80 data tracks on the media. The stepper motor rotates in 15° increments, moving the head carriage assembly one data track for each increment.

The grooved step cam lead screw has a flat spot between each track ramp. A ruby ball, attached to the head carriage assembly, runs in the groove. The flat spots on the lead screw prevent the transfer of small angular vibrations from the screw to the ruby ball.

The head carriage assembly moves smoothly along two rods. Its position over the data tracks is determined by the location of the ruby ball in the lead screw. Two heads, located back to back on the head carriage assembly, can be positioned over any one of 80 data tracks on either diskette.

The head carriage assembly also contains a track zero interrupter bar. This bar is sensed when the head carriage assembly is near track zero and a signal is sent to the seek and interface module. For further information see Section 10.3.1.5.

10.3.1.4 Head Load Mechanism – A head load mechanism is a solenoid actuated arm with a head load pad. When energized, the solenoid releases a head load pad arm to press against the media opposite the R/W head. The pad conforms the media to the contour of the R/W head. This ensures good head to media contact during read or write operations.

When the head load solenoid is de-energized, the head load pad arm is raised away from the media. This reduces wear on the media and the R/W head.

The head automatically unloads if any of the following conditions occur.

- Either of the doors is open.
- The spindle motor is off.
- The drive side is not selected.
- No diskette is present in the drive side.

The front bezel of the drive contains two head load indicators. Each indicator lights when its corresponding head is loaded. These indicators warn the operator not to remove the diskette while the controller is accessing it.

For further information on the control of the head solenoids and indicators, see Section 10.3.4.

10.3.1.5 Sensors – The drive contains switch sensors and photo sensitive sensors for passing status information to the seek and interface module. Figure 10-10 shows that there are two sets of sensors for each drive side except for a single track zero sensor. Each set of sensors provides disk presence, write protection, and index hole location information.

Track Zero Sensor
The track zero sensor consists of a light emitting diode and a photo-transistor combination. As the carriage assembly nears track zero, a tab passes between the diode and the photo-transistor. This turns off the photo-transistor and asserts the track zero signal TKOS H to the seek and interface module. For further information see Section 10.3.7.

Disk Present and Write Protect Sensors
Each drive side has a write protect switch sensor and a diskette present switch sensor. A switch pair for each side is selected simultaneously. Signal SEL A L selects the switches for drive side A. Signal SEL B L selects the switches for drive side B.

When the door is closed, the switches come in direct contact with an inserted diskette. The switches are normally closed. However, inserting a write protected diskette in the drive, opens both switches. When the switches are open and selected, the DP and WP signals assert. These signals provide the seek and interface module with status signals. For further information see Section 10.3.6.

Index Sensor Detail Description
Each index sensor consists of a light emitting diode and a photo-transistor combination. As the index hole in the diskette passes through a sensor, the light from the diode passes through the hole striking the photo-transistor. This causes the photo-transistor to turn on and assert the appropriate index signal, INDEX A L or INDEX B L, to the seek and interface module. For further information see Section 10.3.6.

10.3.2 Select Circuit Detailed Operation

Figure 10-11 shows the operational detail of the select circuits. These circuits perform the following functions for the RX50 drive.

- Pass an enable signal to the motor control module.
- Generate a circuit enable signal.
- Activate headload solenoids and associated indicators.
- Generate sensor select and R/W head select signals.

The select circuit contains the following elements to perform these functions and are described in the following sections.

- Drive select circuit
- Motor enable circuit
- Head load circuit

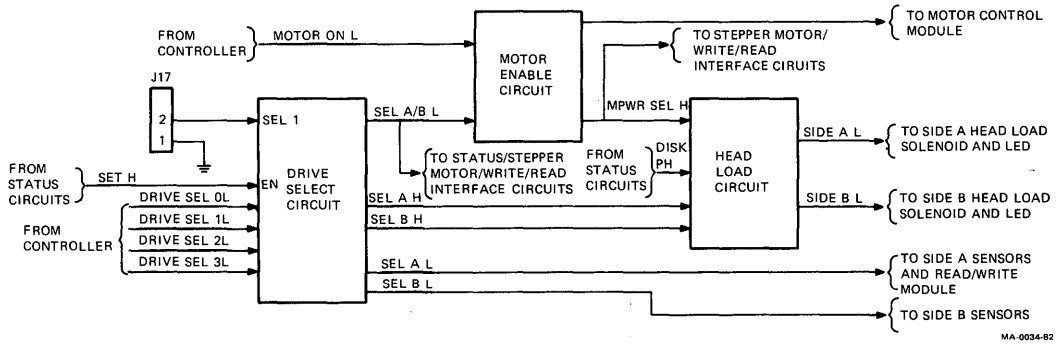
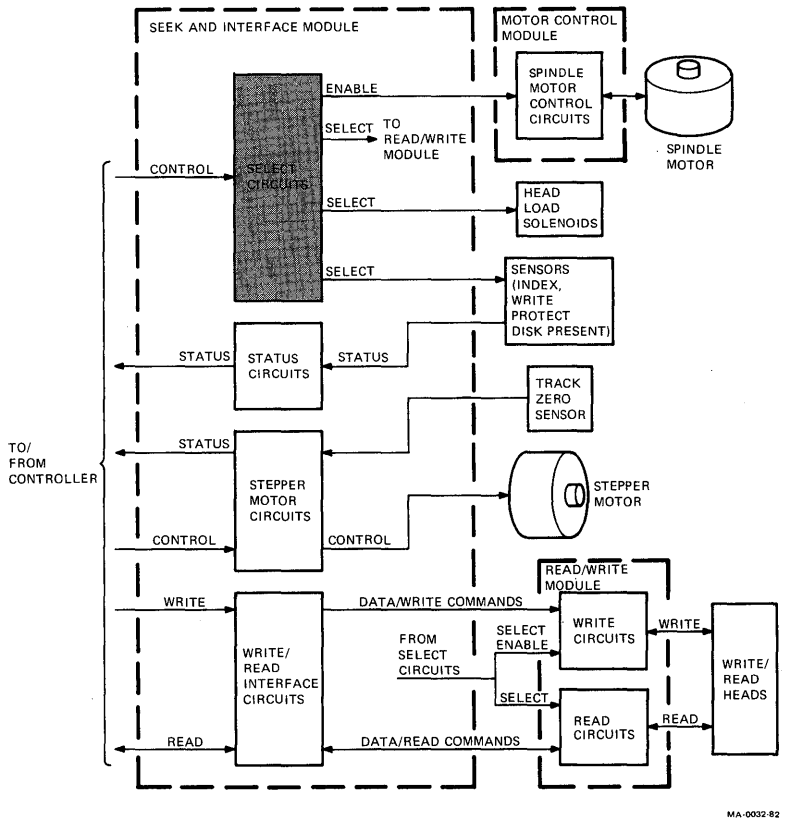


Figure 10-11 Select Circuit Detail



10.3.2.1 Drive Select Circuit Detail – The drive decodes the four drive select lines, DRIVE SEL 0 L through DRIVE SEL 3 L, depending on the condition of J17 (configuration jumper). With J17 open (without a jumper), the drive select circuit decodes DRIVE SEL 0 L and DRIVE SEL 1. With J17 closed (with a jumper), the drive select circuit decodes DRIVE SEL 2 L and DRIVE SEL 3.

The drive select circuit is enabled by a DC voltage status signal, SET H, from the status circuits. When the SET H signal is asserted, the drive select circuits decode the input signals and assert the output select signals.

Table 10-1 shows how the asserted DRIVE SEL inputs control the SEL outputs when a jumper is not installed at J17. Table 10-2 shows how the asserted DRIVE SEL inputs control the SEL outputs when a jumper is installed at J17.

10.3.2.2 Motor Enable Circuit Detail – The motor enable circuit performs the following functions.

- Asserts a spindle motor control circuit enable signal, MPWR H, when the controller asserts MOTOR ON L.
- Asserts a circuit enable signal, MPWR SEL H, when the drive is selected (SEL A/B L is asserted) and the spindle motor control circuit is enabled (MPWR H is asserted).

When the drive is selected and the motor is enabled, the head load circuits, stepper motor circuits, and the R/W interface circuits are enabled.

10.3.2.3 Head Load Circuit Detail – The head load circuits assert one of two select signals, SIDE A L or SIDE B L. Each of these signals activates a head load solenoid and a head load indicator.

An asserted SEL A H or SEL B H asserts the corresponding side signal when the following conditions exist.

- A diskette is present in the selected side and the door is closed (DISK P H is asserted).
- The drive is selected and the spindle motor is turned on (MPWR SEL H is asserted).

Table 10-1 Select Signals Jumper J17 Removed

DRIVE SEL INPUTS	A/B L	SEL OUTPUTS A L	B L	A H	B H
SEL 0 L	yes	yes	no	yes	no
SEL 1 L	yes	no	yes	no	yes
SEL 2 L	no	no	no	no	no
SEL 3 L	no	no	no	no	no

Table 10-2 Select Signals Jumper J17 Installed

DRIVE SEL INPUTS	A/B L	SEL OUTPUTS A L	B L	A H	B H
SEL 0 L	no	no	no	no	no
SEL 1 L	no	no	no	no	no
SEL 2 L	yes	yes	no	yes	no
SEL 3 L	yes	no	yes	no	yes

10.3.3 Motor Control Circuit Detail

Figure 10-12 shows the operational detail of the spindle motor control circuits. These circuits receive dc power and an enable signal, MPWR H, from the seek and interface module.

When enabled, these circuits supply spindle motor drive current to the spindle motor. They also monitor the motor speed and regulate the motor current. This maintains the spindle motor's constant angular speed.

To perform these functions, this circuit consists of the following elements. These elements are described in the following sections.

- Frequency to voltage converter
- Summer
- Integrator
- Gain amplifier and current limiter

10.3.3.1 Frequency to Voltage Converter Detail – The spindle motor contains a tachometer. When the motor is operating, the tachometer returns sinusoidial signals, TACK 1 and TACK 2, to the frequency to voltage converter. These signals represent the motors angular rotation.

The tachometer signal is converted to a voltage. This voltage, VSPEED, represents the motors speed as follows.

1. Each zero voltage crossing of the tachometer signal converts to alternating pulses. These pulses are observable at test point TP1 (Figure 10-13).

2. The leading edge of each pulse generates a transition from 0 V to 5 V or 5 V to 0 V. These transitions, which appear as a rectangular wave, are observable at TP2 (Figure 10-13).

3. The low transitions are averaged with the high transitions. This forms a saw-tooth wave that rides at an average voltage level. This signal, the speed voltage, is observable at test point TP3 (Figure 10-13).

10.3.3.2 Summer Detail – The summer adds a constant reference voltage to the speed voltage (VSPEED) signal. This adjusts the average voltage level of the VSPEED signal to the linear range of the integrator and gain amplifier. The reference voltage is adjusted at the time of manufacture and is not field adjustable.

The output of the summer equals the speed error, VERROR, for the integrator.

10.3.3.3 Integrator Detail – The integrator inverts the saw-tooth wave of the VERROR signal. This converts a decreasing average voltage to an increasing average voltage and vice versa. This inversion is needed because the sensed speed error voltage drops as the speed decreases. However, the motor requires more power to increase its speed and vice versa.

The output of the integrator is observable at test point TP4 (Figure 10-13). An asserted spindle motor control circuit enable signal, MPWR H, allows the integrator output to pass to gain amplifier and current limiter. When MPWR H is unasserted, the gain amplifier and current limiter is disabled.

10.3.3.4 Gain Amplifier and Current Limiter – The gain amplifier couples power to the spindle motor. The current limiter limits the amount of power coupled to the motor. This protects the motor during circuit or hardware faults and when the circuit is first enabled.

The gain amplifier operates in its linear range except when the spindle motor control circuit is first enabled. When initially enabled, the gain amplifier is forced into saturation. This occurs because the motors sensed speed causes the integrator to generate the maximum driving signal.

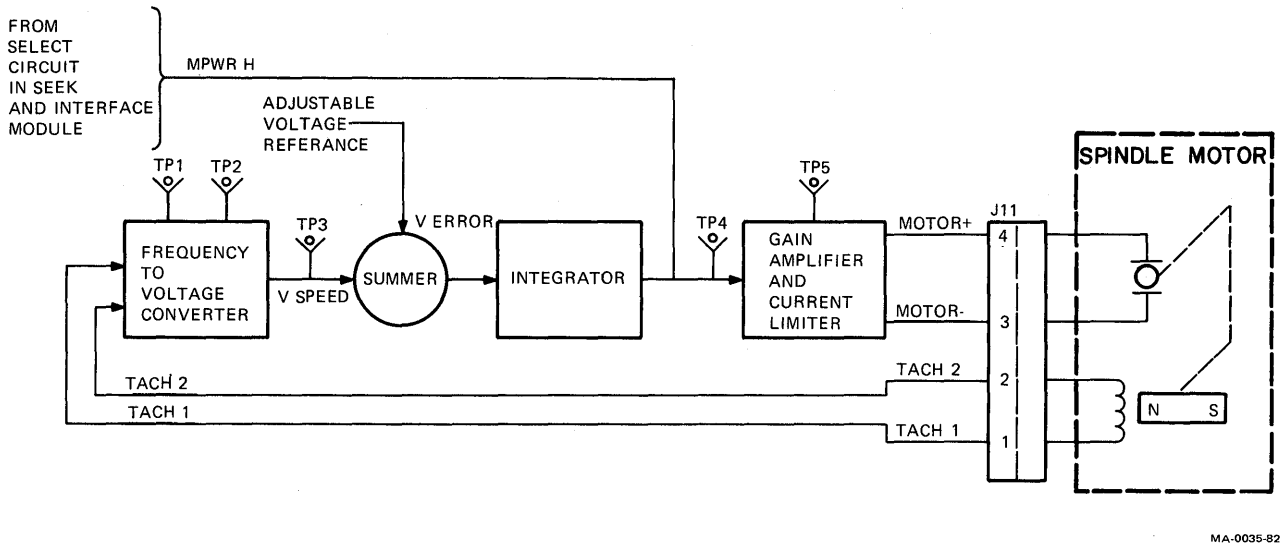
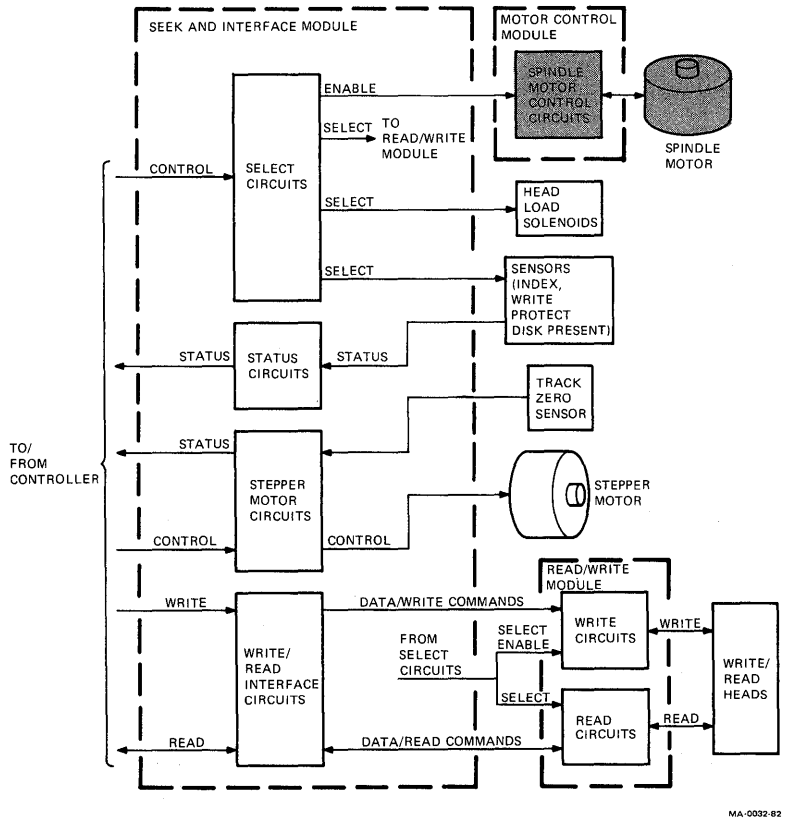


Figure 10-12 Motor Control Circuit Detail



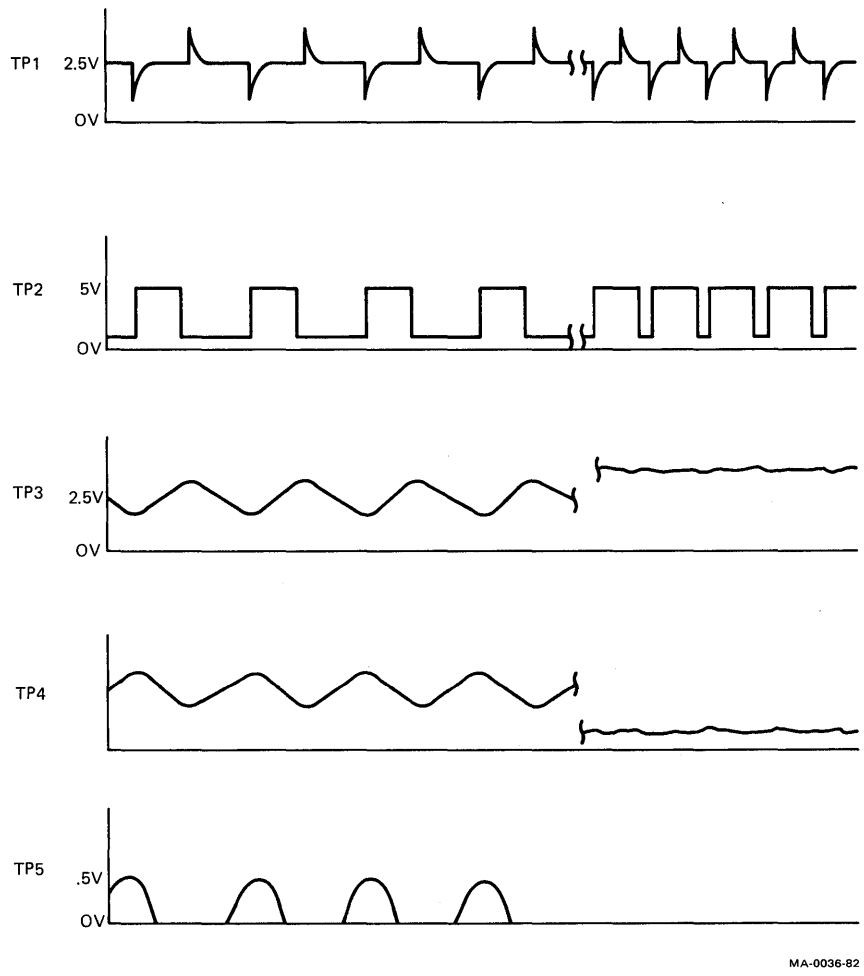


Figure 10-13 Motor Control Wave Forms

As the motor approches its required speed, the integrator generates a saw-tooth wave (see Section 10.3.3.3). This signal operates the gain amplifier in its linear range.

The high peaks of saw-tooth wave turn the gain amplifier on and off, forming current pulses for the motor. These pulses are observable at test point TP5 as voltage pulses (Figure 10-13).

10.3.4 Head Load Solenoids and Indicators

Figure 10-14 shows the electrical connections to the head load solenoids and indicators that are controlled by the select circuits. The drive contains two solenoids and two indicators, one set for each drive side. The select logic activates one set at a time when the following conditions exist.

- The spindle motor is operating.
- A diskette is properly inserted and the door is closed.
- The drive side is selected.

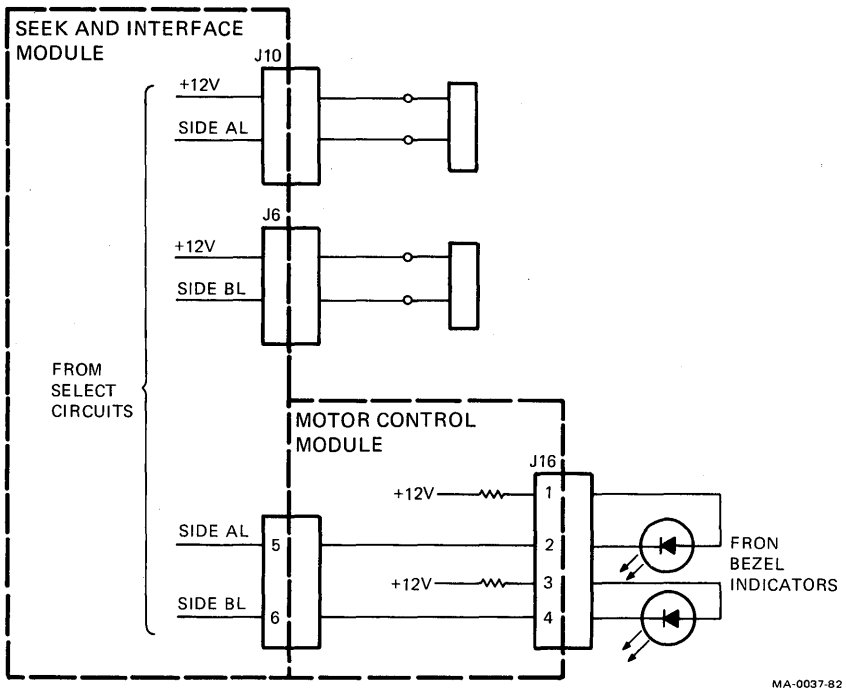
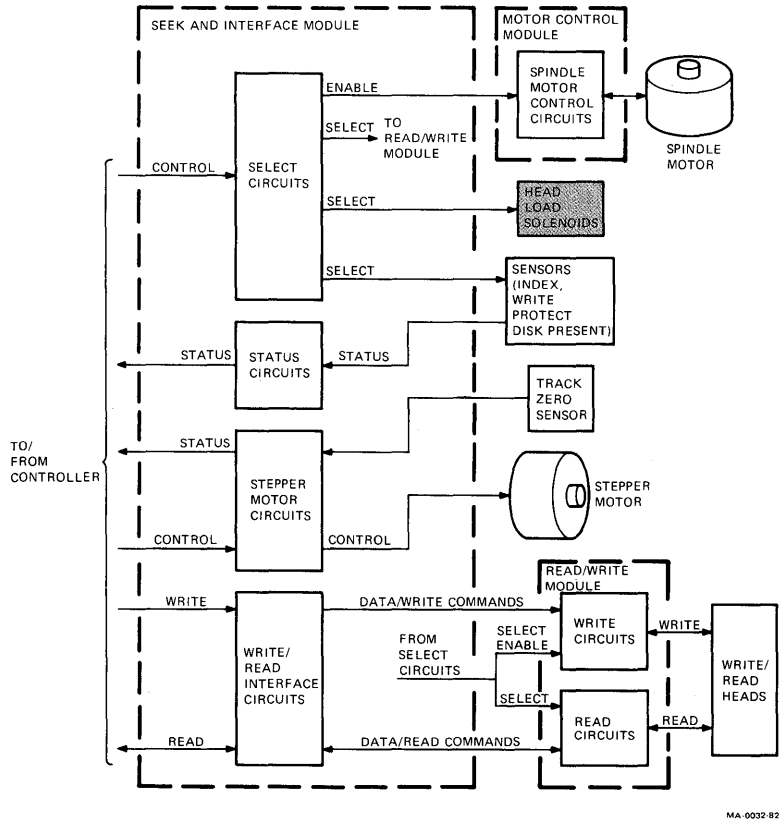


Figure 10-14 Connections to Head Load Solenoids and Indicators



10.3.5 Status Circuit Detail

Figure 10-15 shows the detail operation of the status circuits. Figure 10-16 shows the timing relationships between the circuit signals. These circuits perform the following functions for the RX50 drive.

- Pass status signals from the drive to the controller.
- Monitor the DC power for fluctuations.

These functions are performed by the following status circuit elements.

- Write protect status circuit
- Diskette present status circuit
- Output drivers
- +5 volt monitor

10.3.5.1 Write Protect Status Circuit Detail – This circuit monitors the write protect status signals, WP A H and WP B H, from the write protect sensors (see Section 10.3.6.2). If either signal asserts, this circuit asserts the write protect signal, WPROT H, for the output drivers and the R/W interface circuits.

10.3.5.2 Diskette Present Status Circuits Detail – This circuit monitors the diskette present status signals, DP A H and DP B H, from the diskette present sensors (see Section 10.3.6.2). If either signal asserts, this circuit asserts the diskette present signal, DISK P H, for the output drivers, select circuits, and the R/W interface circuits.

10.3.5.3 Output Driver Detail – These drivers pass the status signals from the RX50 drive to the controller. They are enabled by select circuits, SEL A/B H is asserted. The output drivers pass the signal state of the index (see Section 10.3.6.1), write protect, and diskette present signal as INDEX L, WRITE PROTECT L, and READY.

10.3.5.4 +5 Volt Monitor – This monitor generates enable and reset signals for the RX50 drive. It continually monitors the state of the +5 volt power of the drive. If it goes out of tolerance, the monitor deasserts DCOK L and SET H.

The DCOK L signal enables the write circuits to operate when they are selected. The SET H signal enables the select and stepper motor circuits.

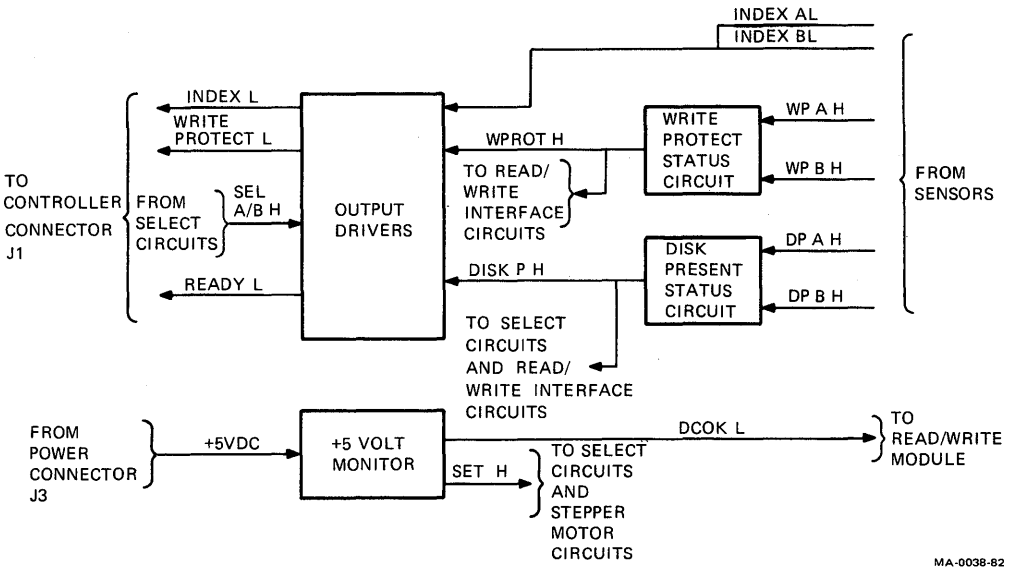
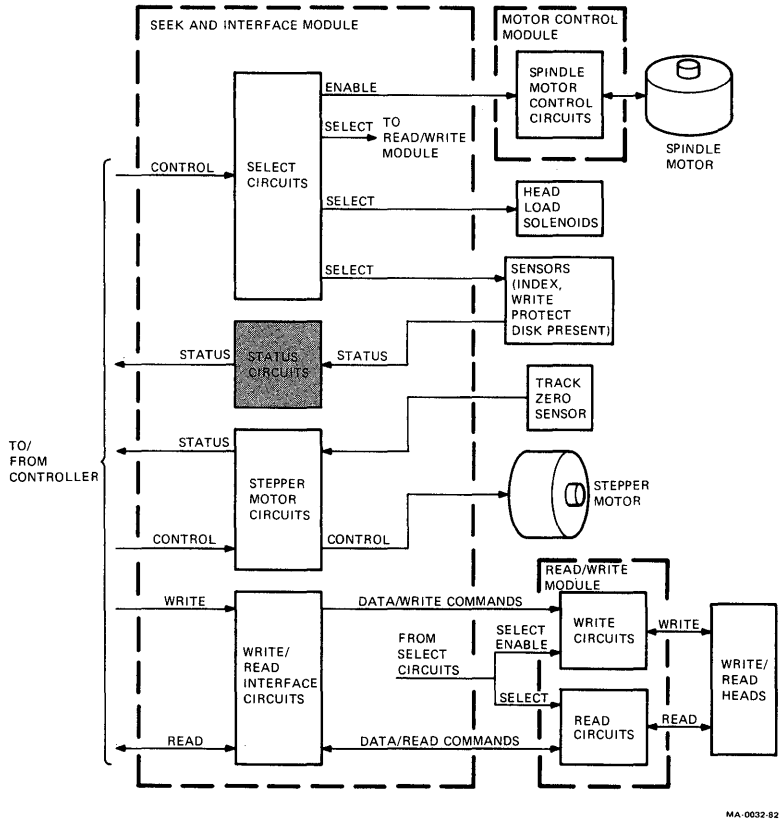


Figure 10-15 Status Circuit Detail



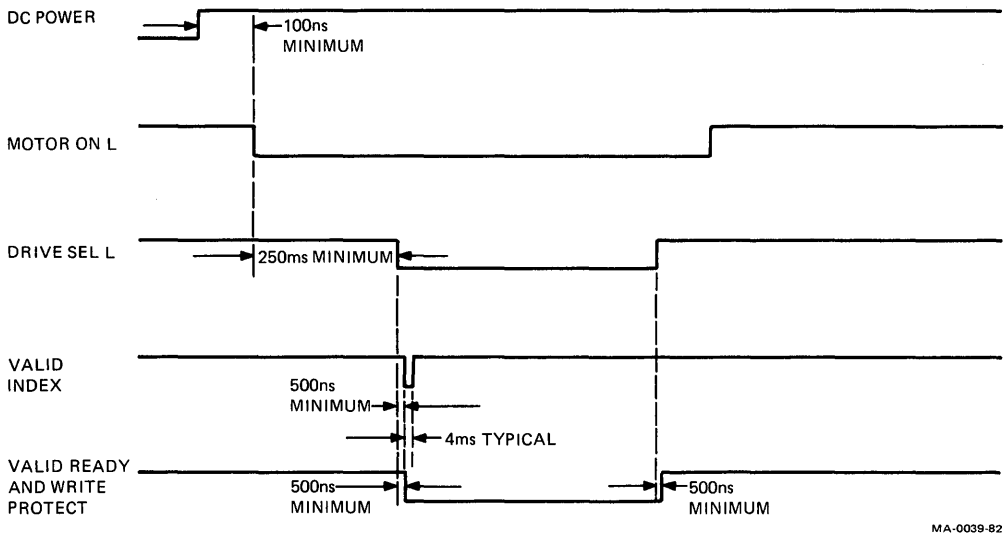


Figure 10-16 Status Circuit Timing Relationships

10.3.6 Status Sensor Detail

Figure 10-17 shows the detail operation of the status sensors. These sensors are a series of light emitting diodes with photo sensitive transistors and switches. These sensors perform the following functions for the RX50 drive.

- Sense the location of the index hole in the media for the status circuits.
- Sense the presence of the diskette for the status circuits.
- Sense the write protect status of the diskette for the status circuits.

10.3.6.1 Index Sensor Detail – The drive contains two index sensors, one sensor for each drive side. Each index sensor consists of a light emitting diode and photo-sensitive transistor. A select signal from the select circuits enables the photo-sensitive transistor. When the select signal is unasserted, the sensor is disabled.

When a sensor is enabled, it controls a status signal, INDEX A L or INDEX B L, for the status circuits. The signal is asserted when the index hole in the diskette passes through the selected sensor. The light from the light emitting diode then strikes the photo-sensitive transistor, turns it on and asserts the index signal.

10.3.6.2 Diskette Present and Write Protect Sensor Detail – The drive contains two sets of diskette present and write protect sensors, one set for each drive side. Each sensor provides a status signal to the status circuits. The sensors are switches selected by the select circuits.

Each drive side has a write protect switch and a diskette present switch. The switches for each side are selected as pairs. Signal SEL A L selects the switches for drive side A. Signal SEL B L selects the switches for drive side B.

When the door is closed, the switches come in direct contact with a diskette inserted in the drive side. The switches are normally closed. Inserting a write protected diskette in the drive opens both switches. When the switches are open and selected, the diskette present and write protect signals are asserted.

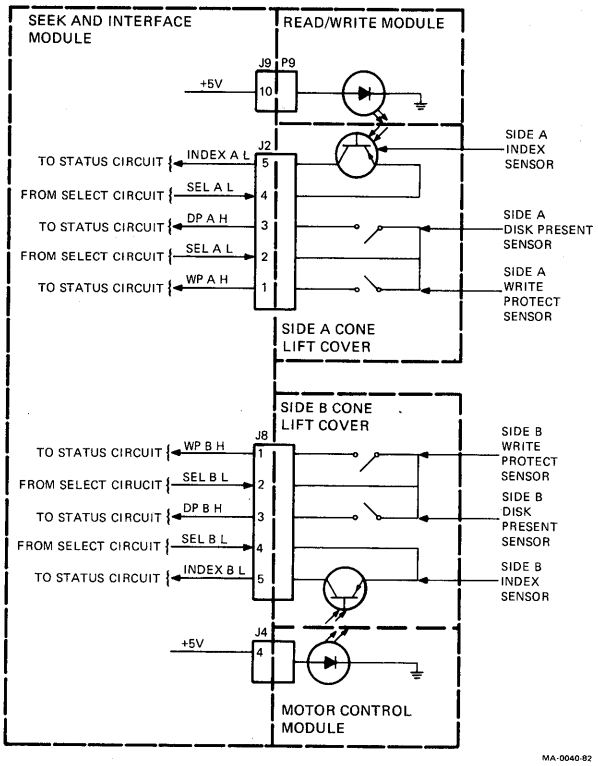
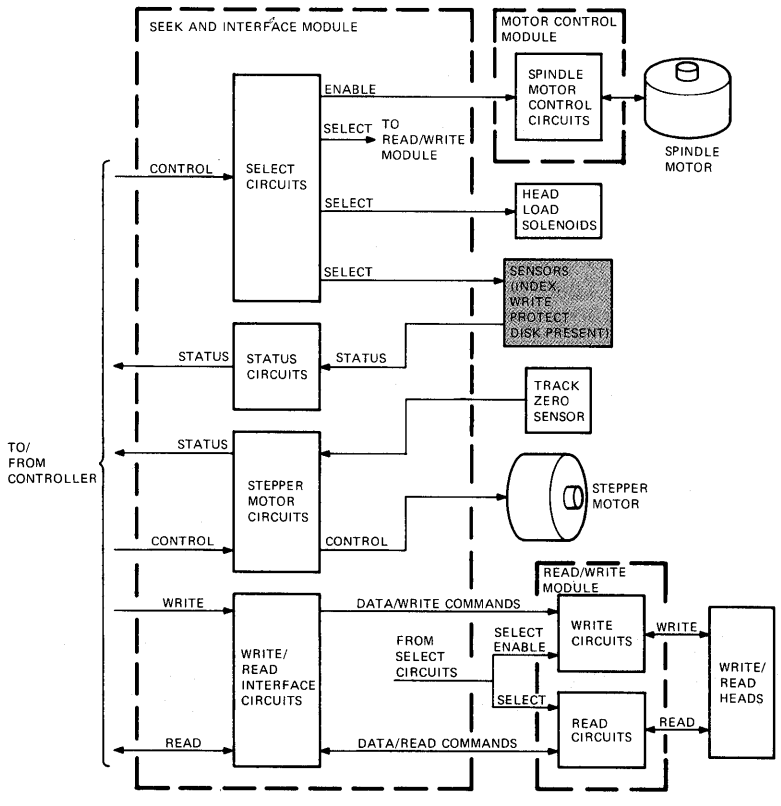


Figure 10-17 Sensor Detail



10.3.7 Stepper Motor Circuit Detail

Figure 10-18 shows the detailed operation of the stepper motor circuits. Figure 10-19 shows the timing relationships between the circuits signals. These circuits perform the following functions.

- Generate control signals that actuate the stepper motor.
- Pass a track zero status signal to the controller.

These functions are performed by the following stepper motor circuit elements.

- Stepper motor driver
- Track zero sensor
- Track zero status circuit

10.3.7.1 Stepper Motor Driver Detail – The stepper motor driver decodes control signals from the controller and generates phase control signals for the stepper motor coils. This driver also passes phase control signals to the track zero status circuit. These signals indicate a possible track zero head position.

The select and status circuits and the controller enable the stepper motor driver. The driver requires an asserted MPWR SEL H, SEL A/B H and SET H, while WRITE GATE L is unasserted. These signal states indicate that the following conditions exist for the stepper motor driver operation.

- The spindle motor is operating.
- The drive is selected.
- The +5 volt power level is in tolerance.
- The drive is not enabled for write operations.

The step motor controller generates four phase-control signals for the operation of the step motor, STMT1, STMT2, STMT3, STMT4. These driver outputs are decoded from two controller signals, DIRECTION and STEP L. Figure 10-19 shows the timing relationships between the controller inputs and the driver outputs.

The DIRECTION signal indicates the direction the stepper motor rotates. The STEP L signal indicates the number of steps the motor moves.

10.3.7.2 Track Zero Sensor Detail – The drive contains one track zero sensor. This sensor consists of a light emitting diode and photo-sensitive transistor and is always enabled. When the heads are located at track 0, 1, or 2, this sensor asserts a track zero sense signal, TK0S, for the stepper motor circuits.

The TK0S signal is asserted when a tab on the carriage assembly passes through the sensor. The tab stops light from the light emitting diode from striking the photo-sensitive transistor. This turns off the transistor and asserts TK0S.

10.3.7.3 Track Zero Status Circuit Detail – The track zero status circuit monitors for a track zero R/W head location. When the drive is selected this circuit is enabled by the select circuits. When enabled, this circuit returns a track zero status signal, TRACK 0 L, to the controller.

The track zero status circuit asserts the TRACK 0 L signal when the following conditions exist.

- When the heads are located over track 0, 1, or 2, (TK0S H asserted).
- When the stepper motor driver asserts the zero phase signals to the motor, (01 H and 03 H signals asserted).

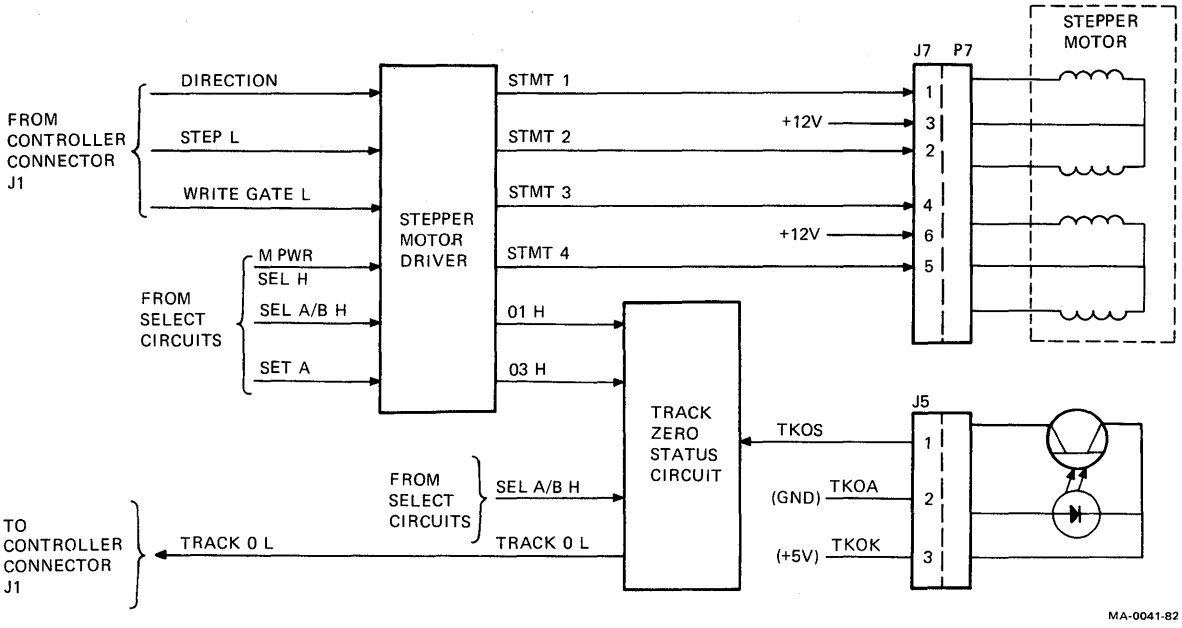
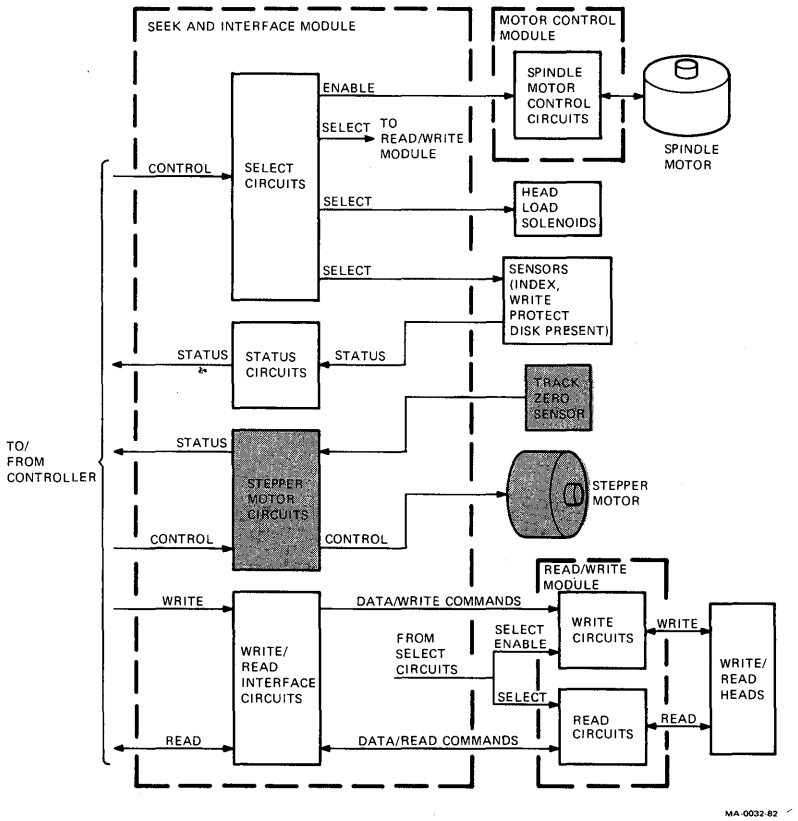


Figure 10-18 Stepper Motor Circuit Detail



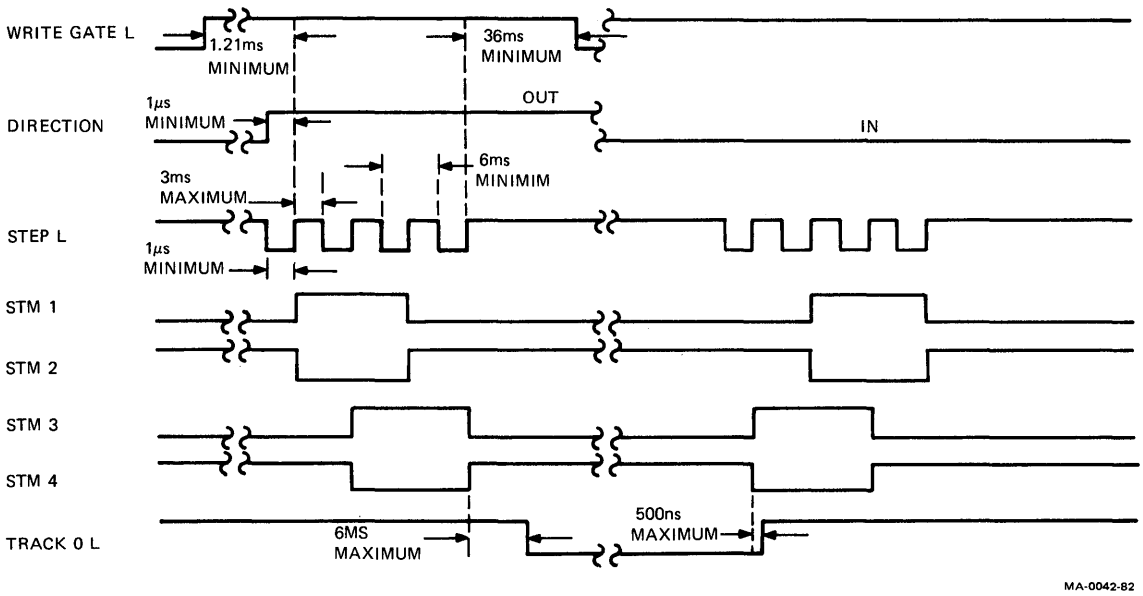


Figure 10-19 Stepper Motor Timing Relationships

10.3.8 Read/Write Interface Circuit Detail

Figure 10-20 shows the R/W interface circuit operational detail. Figures 10-21 and 10-22 show the timing relationships between the circuits signals and valid data. These circuits perform the following functions for the RX50 drive.

- Pass write data from the controller to the RW module,
- Pass write control signals from the controller to the R/W module.
- Generate an erase control signal for the R/W module.
- Pass read data from the R/W module to the controller.

These functions are performed by the following R/W interface circuit elements.

- Write driver circuit
- Erase gate timer
- Output driver

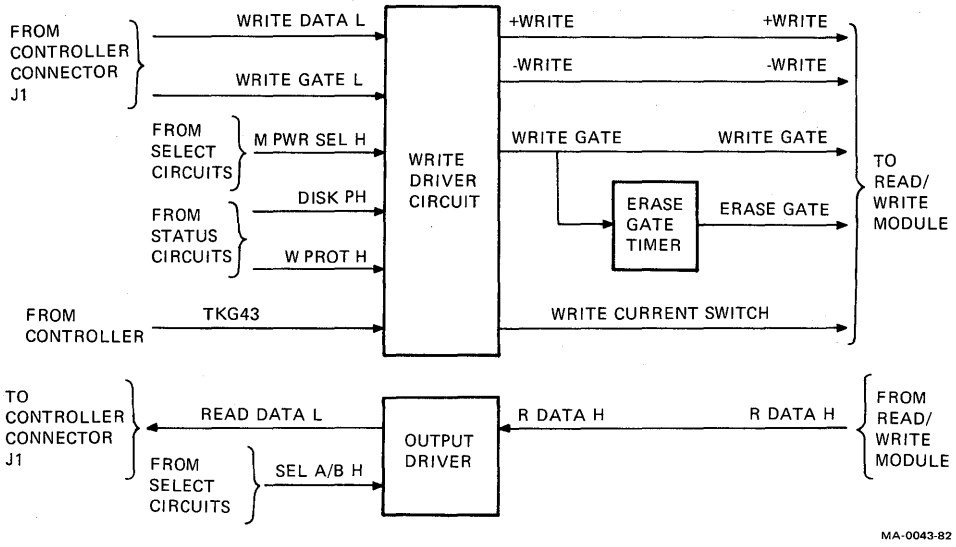
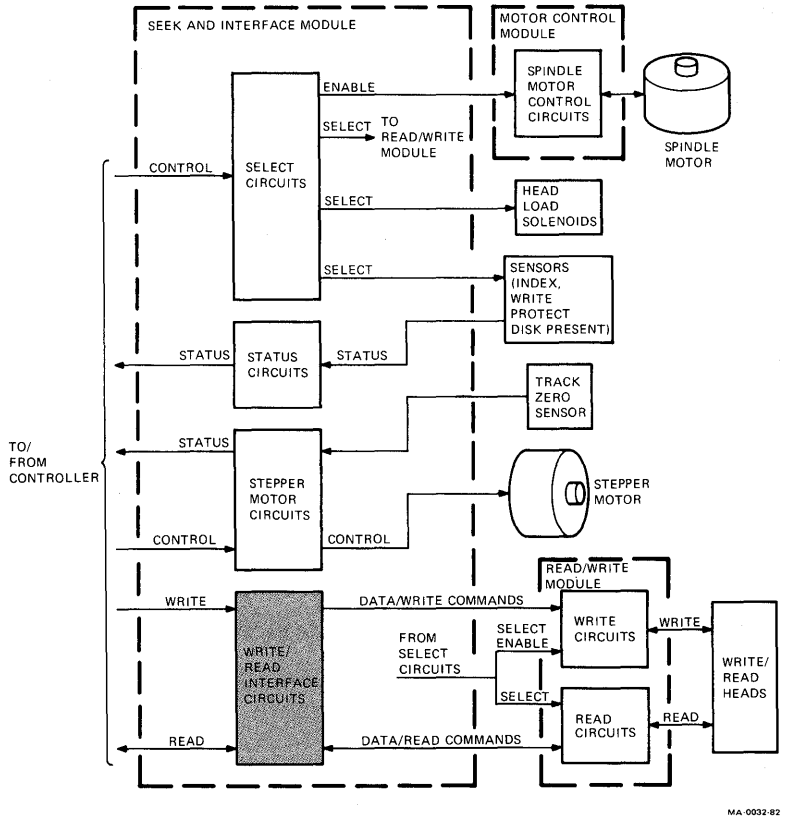


Figure 10-20 Read/Write Interface Circuit Detail



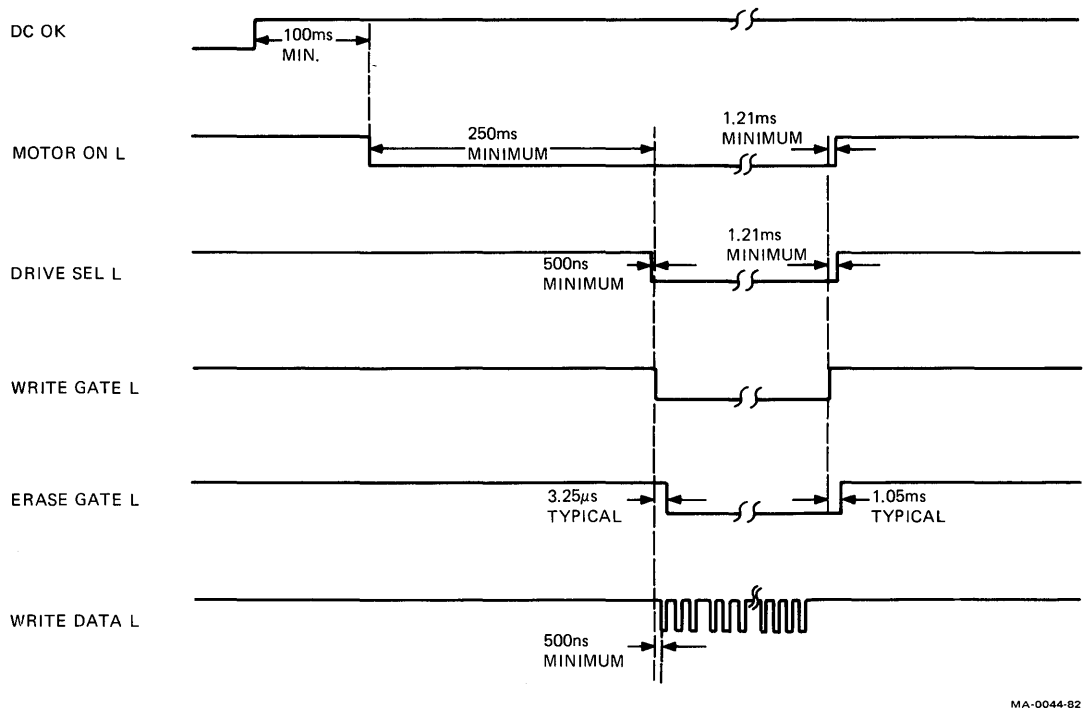


Figure 10-21 Write Data Timing Relationships

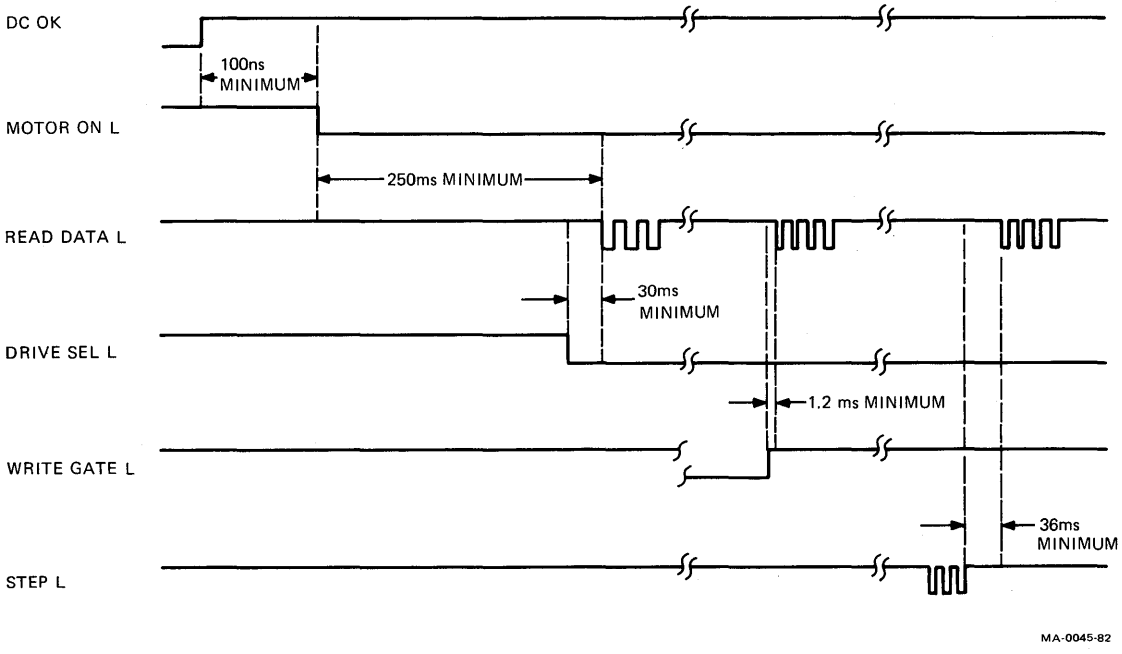


Figure 10-22 Read Data Timing Relationships

10.3.8.1 Write Driver Circuit – When enabled, the write driver circuit passes write data and commands to the erase gate and R/W module. This circuit is enabled by the controller, select circuits, and status circuits (Figure 10-20). The write driver circuit is enabled when the following conditions exist.

- The controller selects a write function by asserting WRITE GATE L.
- The spindle motor is enabled and the drive is selected. This is indicated by an asserted MPWR SEL H signal.
- A diskette is present in the selected side and the door is closed. This is indicated by an asserted DISK P H signal.
- The diskette is not write protected. This is indicated by an unasserted WPROT H signal.

When enabled, the write driver circuits divide write data from the controller by two. It then passes the data on differential lines to the R/W module. This converts the write data pulses to leading edge triggered differential data. For further information on the write data see Section 10.3.9.4.

The driver also passes two control signals from the controller to the R/W module, the WRITE GATE L signal as WRITE GATE and the TKG43 signal as WRITE CURRENT SWITCH. The WRITE GATE signal enables the write circuits in the R/W module. The WRITE CURRENT SWITCH signal controls the level of write current the write circuits generate.

10.3.8.2 Erase Gate Timer Detail – The erase gate timer delays the WRITE GATE signal to generate an ERASE GATE signal. This delay is necessary because of the R/W head design (See Section 10.3.11). Figure 10-21 shows the relationship of the ERASE GATE and WRITE GATE.

10.3.8.3 Output Driver Detail – The output driver passes read data, R DATA H, from the R/W module to the controller. Figure 10-22 shows the timing relationships between the circuit signals and the read data.

The output driver is enabled by the select logic when SEL A/B H is asserted. This signal state indicates that the RX50 drive is selected.

10.3.9 Write Circuit Detailed Operation

Figure 10-23 shows the write circuit operational detail. These circuits perform the following functions for the RX50 drive.

- Generate write currents for the heads.
- Generate an erase current for the heads.
- Generate head select signals.
- Protect the heads and previously written data when the dc power is out of tolerance.

These functions are performed by the following write circuit elements.

- Write current generator
- Voltage referance
- +12 volt gate
- Differential write switch
- Erase current generator
- Multiplexer

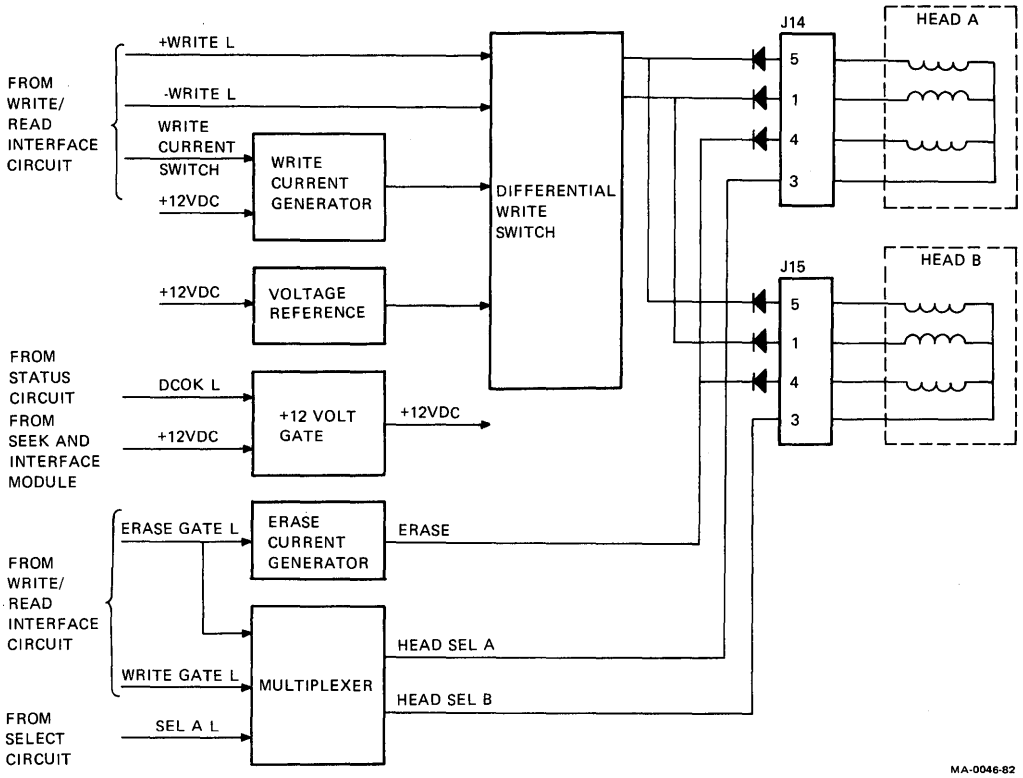
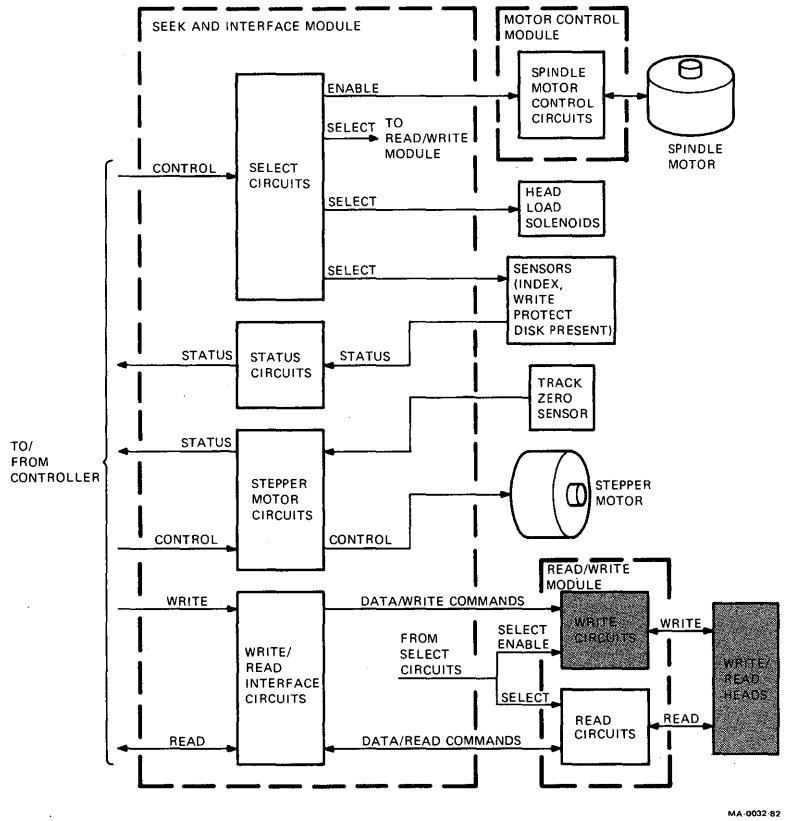


Figure 10-23 Write Circuit Detail



10.3.9.1 Write Current Generator Detail – The write current generator provides a selectable current for the differential write switch. These currents are derived from the +12 volts from the +12 volt gate.

When the WRITE CURRENT SWITCH signal is asserted, a low current for the inner tracks (44 through 79) is provided to the differential write switch. When the WRITE CURRENT SWITCH signal is unasserted, a high current for the outer tracks (0 through 43) is provided to the differential write switch.

10.3.9.2 Voltage Reference Detail – The voltage reference provides a stable voltage to the differential write switch. This voltage makes sure that the outputs of the differential write switch are balanced.

10.3.9.3 +12 Volt Gate Detail – The +12 volt gate receives the R/W modules supply voltage (+12 Vdc) and a DCOK signal. If DCOK remains asserted, the gate passes +12 Vdc to the modules circuits. This makes sure that the write circuits are disabled if a low power condition exists.

10.3.9.4 Differential Write Switch Detail – The differential write switch converts the write data from the R/W interface circuits to write currents for the R/W heads. Figure 10-24 shows the conversion of WRITE DATA from the controller (Section 10.3.8.1) to write currents for the heads. For this conversion, the differential write switch requires a write current and a reference voltage.

The write currents, +WRITE and −WRITE, generate magnetic fields in the heads which records data the media. For further information on the recording techniques see Section 10.3.11.

10.3.9.5 Erase Gate Generator Detail – The erase gate generator converts the ERASE GATE L signal to an ERASE current for the R/W heads. This current generates a magnetic field in the heads which tunnel erases recorded data on the media. For further information on the recording techniques see Section 10.3.11.

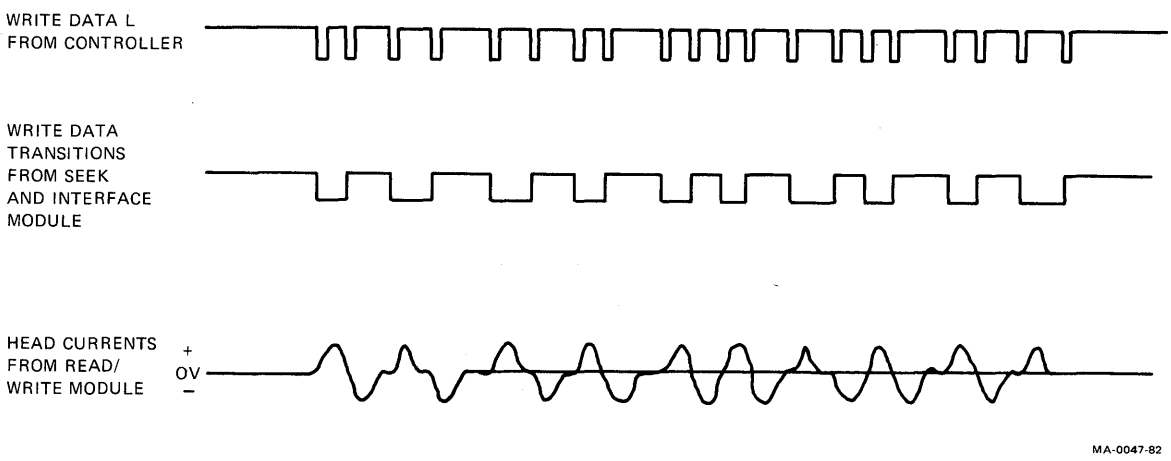


Figure 10-24 Write Data to Head Current Conversion

10.3.9.6 Multiplexer Detail – The multiplexer decodes three signals (ERASE GATE, WRITE GATE, and SELECT) to generate head select signals for a write function. Table 10-3 shows how the inputs assert the outputs, HEAD SEL A and HEAD SEL B signals.

10.3.10 Read Circuit Detailed Operation

Figure 10-25 shows the detailed operation of the read circuits. These circuits perform the following functions for the RX50 drive.

- Select a R/W head and read data.
- Convert the analog read data to digital data.

These functions are performed by the following read circuit elements.

- Read amplifier
- Multiplexer

Table 10-3 Write Function Head Select

INPUTS			OUTPUTS	
ERASE GATE L	**WRITE GATE L**	**SEL A L**	**HEAD SEL A**	**HEAD SEL B**
no	no	no	write not selected	
no	yes	no	yes	no
yes	no	no	yes	no
yes	yes	no	yes	no
no	no	yes	write not selected	
no	yes	yes	no	yes
yes	no	yes	no	yes
yes	yes	yes	no	yes

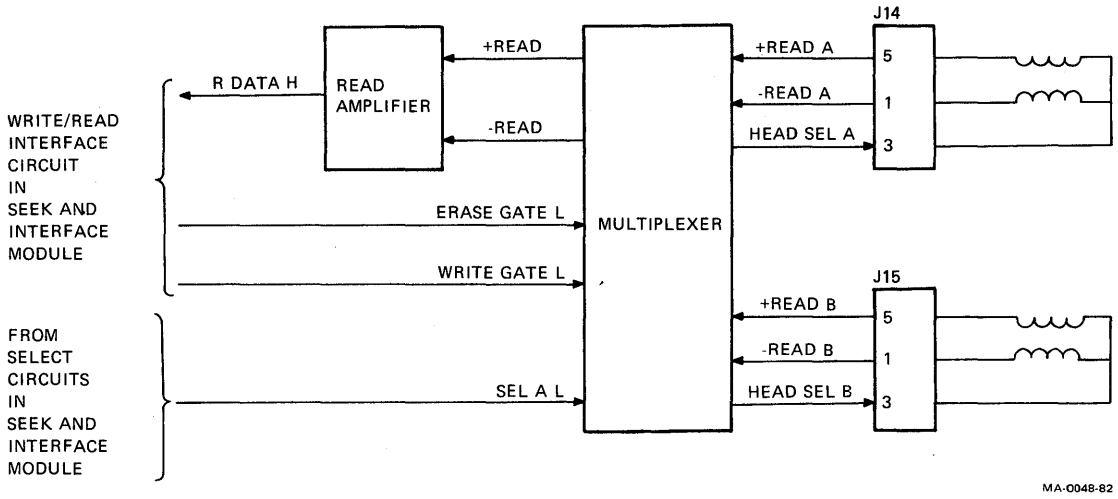
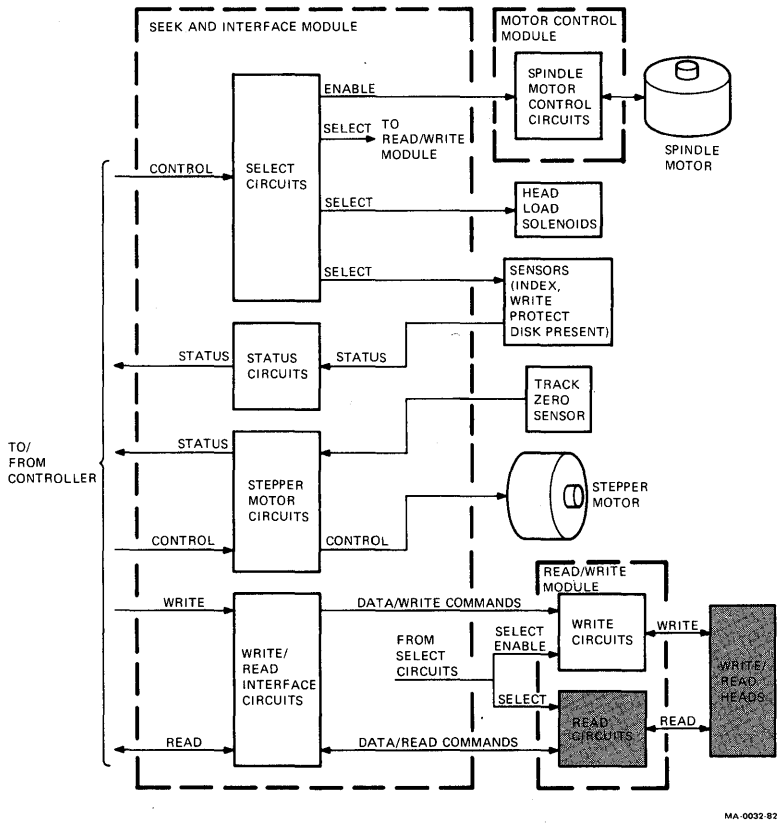


Figure 10-25 Read Circuit Detail



10.3.10.1 Read Amplifier Detail – The read amplifier converts analog read signals, developed in the R/W heads by the media, to digital read data for the R/W interface circuits. Magnetic flux reversals on the media generate the analog signals. These flux reversals represent previously recorded data and clocks. Figure 10-26 shows the possible frequency combinations and the conversion results.

10.3.10.2 Multiplexer Detail – The multiplexer decodes three signals (ERASE GATE, WRITE GATE, and SELECT) to generate head select signals and select read data for the read amplifier. The write circuits use the same multiplexer, however, the ERASE GATE L and WRITE GATE L signals are unasserted for a read function.

Table 10-4 shows how the seek and interface module inputs select read data and head select signals.

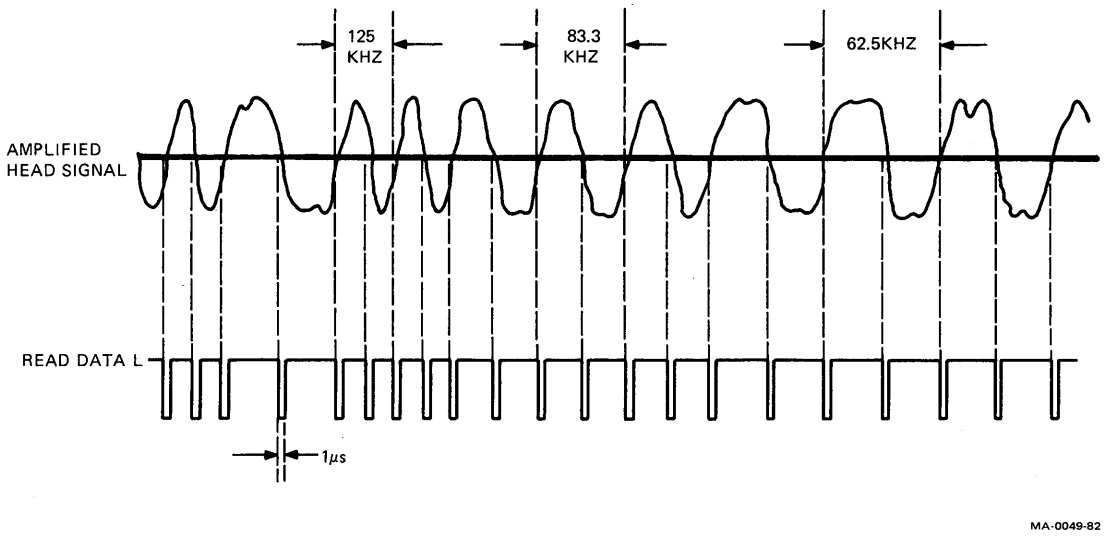


Figure 10-26 Head Signal to Read Data Conversion

Table 10-4 Read Function Head Select

ERASE GATE L	WRITE GATE L	SEL A L	HEAD SEL A	HEAD SEL B	HEAD DATA
no	no	yes	yes	no	A
no	yes	yes	read not selected		
yes	no	yes	read not selected		
yes	yes	yes	read not selected		
no	no	no	no	yes	B
no	yes	no	read not selected		
yes	no	no	read not selected		
yes	yes	no	read not selected		

10.3.11 Read/Write Heads Detailed Operation

The RD50 drive has two R/W heads, one for each drive side. The heads are selected by either the write circuits or read circuits. Figure 10-23 shows the head connections for a write function and Figure 10-25 shows the head connections for a read function.

Each head consists of a R/W ferrite core wound with a differential coil. The head also contains a forked erase ferrite core wound with a coil. The erase core is located behind the write core with the forked core straddling the write core. This accounts for the delayed erase gate signal. For more information, refer back to Section 10.3.8.2.

During write operations, current flows through the coils and generates a magnetic flux in the core. When the media passes under the R/W core, the surface of the media is magnetized in one direction. Reversing the current, magnetizes the surface in the opposite direction.

The forked erase core trims the edges of the magnetized surface. This ensures off-track reading capability for diskette interchangeability between drives.

During read operations only the R/W core is used. The erase core is not used. When the media passes under the R/W core, the recorded flux reversals generate small alternating currents in the R/W coils. This current passes to the read circuits for conversion to digital data.

10.4 INTERMODULE SIGNAL DEFINITIONS

This section defines all control and data signals that pass between the controller and the RX50 drive and between the modules of the RX50 drive. All signal definitions in this section are grouped by common connector for easy recognition.

10.4.1 Seek and Interface/Controller Module Connector J1

This section describes the signals passed between the seek and interface module and RX50 controller module. Figure 10-27 shows the control and data interface signal direction between the controller and the drive. The seek and interface module is part of the RX50 drive. Chapter 9 discusses the controller in detail.

Figure 10-28 shows the location of J1 and other connectors of the module. Odd numbered pins are grounded and are not discussed. An L attached to a signal name designates it asserted low (logic 0). An H attached to a signal name designates it asserted high (logic 1).

Pin	Mnemonic	Function
2	TKG43 L	Controls write current level
4	Reserved	Not used
6	DRIVE SEL3 L	Selects drive side B if J17 installed
8	INDEX L	Indicates index mark of selected side
10	DRIVE SEL0 L	Selects drive side A if J17 not installed
12	DRIVE SEL1 L	Selects drive side B if J17 not installed
14	DRIVE SEL2 L	Selects drive side A if J17 installed
16	MOTOR ON L	Turns spindle motor on or off
18	DIRECTION	Controls head movement direction
20	STEP L	Controls head movement distance
22	WRITE DATA L	Data to be stored on diskette
24	WRITE GATE L	Activates write circuits
26	TRACK 0 L	Track 0 head location indicator
28	WRITE PROTECT L	Indicates selected diskette is write protected
30	READ DATA L	Data retrieved from diskette
32	Reserved	Not used
34	READY L	Indicates selected drive side contains a diskette

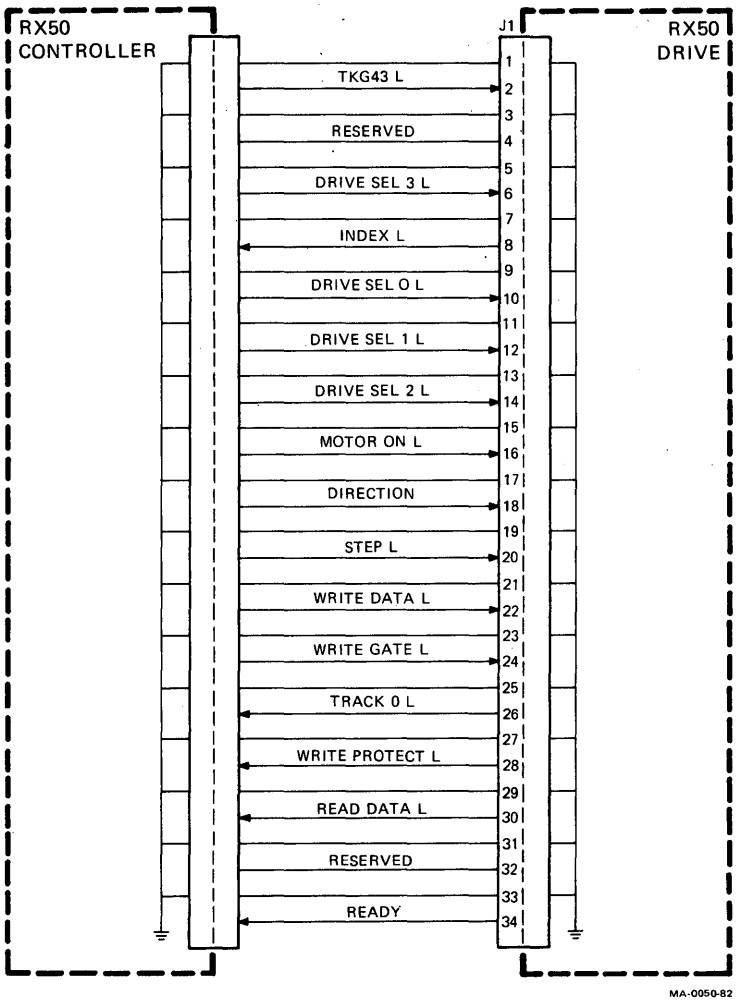


Figure 10-27 RX50 Controller and Drive Interface Signal Flow

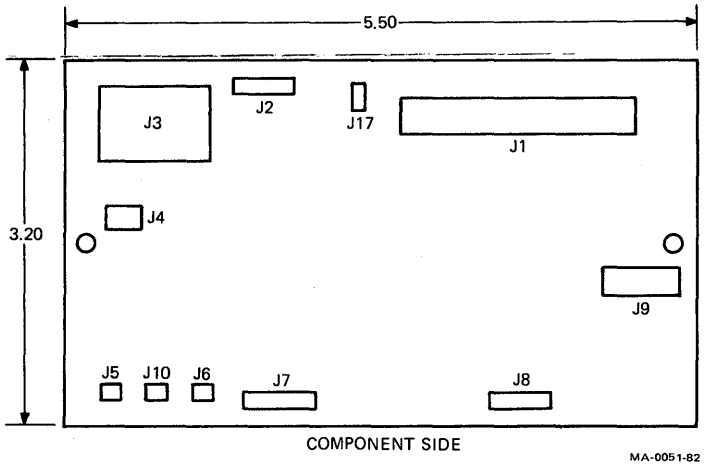


Figure 10-28 Seek and Interface Module Connector Locations

10.4.1.1 TKG43 L Input Signal – The RX50 controller generates this signal. It is asserted when writing data to tracks 44 through 79. In the asserted state, the seek and interface module reduces the write current. In the unasserted state, the seek and interface module generates a normal write current.

10.4.1.2 DRIVE SEL 0 thru DRIVE SEL 3 Input Signals – These signals select the drive side (A or B) on which a function occurs. When J17 is not installed, signal DRIVE SEL 0 selects drive side A and signal DRIVE SEL 1 selects drive side B. When J17 is installed, signal DRIVE SEL 2 selects drive side A, and signal DRIVE SEL 3 selects drive side B.

10.4.1.3 TRACK 0 L Output Signal – This signal indicates the heads are located over track 0 (the outermost track). This signal is valid only when a drive side is selected.

10.4.1.4 MOTOR ON L Input Signal – This signal controls the motor control module which controls the spindle motor. When this signal is asserted, the spindle motor rotates. The spindle motor reaches the rated rotational speed within 1/2 second after an asserted MOTOR ON signal.

10.4.1.5 DIRECTION Input Signal – This signal defines the moving head direction when STEP input line is pulsed. Step-out (moving away from the center of the disk) is defined as HIGH level of this signal (logic 1). Step-in (moving towards the center of the disk) is defined as LOW level of this signal (logic 0).

10.4.1.6 STEP L Input Signal – When pulsed, this signal moves the heads. Each pulse moves one track space in the direction indicated by the DIRECTION signal. The minimum pulse width is 1 μs. The minimum width between step pulses is 6 ms. This signal is ignored when WRITE GATE L is asserted, MOTOR ON L is unasserted, or no drive side is selected.

10.4.1.7 WRITE DATA L Input Signal – This signal represents data to be stored on the diskette. Each transition to the asserted state reverses the current to the R/W heads. Write pulses must begin a minimum of 500 ns after WRITE GATE is asserted. A minimum of 36 ms is required after the last STEP pulse occurs. Write pulses are ignored when WRITE GATE or MOTOR ON are unasserted, the diskette is write protected, no diskette is present, or no drive side is selected.

10.4.1.8 WRITE GATE L Input Signal – This signal enables writing and tunnel erasing of data to the diskette. This signal is ignored when the diskette is write protected.

10.4.1.9 INDEX L Output Signal – The leading edge of this pulse signal indicates the detection of the index hole in the selected drive side. The INDEX L pulse is valid 250 ms after MOTOR ON L is asserted. This indicator signal is invalid if no drive side is selected.

10.4.1.10 WRITE PROTECT L Output Signal – When asserted, this signal indicates that the write enable notch of the selected diskette is masked and the writing of new data is inhibited. This signal is invalid if no drive side is selected.

10.4.1.11 READ DATA L Output Signal – This signal represents data retrieved from the diskette. READ DATA L is valid 250 ms after MOTOR ON L is asserted, 36 ms after receiving the last STEP L pulse, 1.21 ms after WRITE GATE signal is unasserted, or 30 ms after the drive side is selected.

10.4.1.12 READY Output Signal – This signal indicates that a diskette is present in the selected drive side. It is valid only if a drive side is selected.

10.4.2 Seek and Interface/Motor Control Modules Connector J4

This section describes the signals passed between the seek and interface module and motor control module. Figure 10-28 shows the location of J4 and other connectors of the module. Power and ground signals are not discussed in detail. An L attached to a signal name designates it asserted low (logic 0). An H attached to a signal name designates it asserted high (logic 1).

Pin	Mnemonic	Function
1,2	+12 V RET	Ground
3	MPWR H	Turns on spindle motor
4	+5 V DC	Side B index light emitting diode power source
5	SIDE A L	Drive A indicator control
6	SIDE B L	Drive B indicator control
7,8	+12 V DC	Spindle motor and control logic power source

10.4.2.1 MPWR H Input Signal – This signal controls the spindle motor. When the signal is asserted, the spindle motor control logic is enabled and the spindle motor turns on.

10.4.2.2 SIDE A L Input Signal – This signal controls the drive A operational indicator on the front panel. When the signal is asserted, the indicator lights when the drive is in use.

10.4.2.3 SIDE B L Input Signal – This signal controls the drive B operational indicator on the front panel. When the signal is asserted, the indicator lights when the drive is in use.

10.4.3 Seek and Interface/Read Write Modules Connector J9

This section describes the signals passed between the seek and interface module and R/W module. Figure 10-28 shows the location of J9 and other connectors of the module. Power and ground signals are not discussed in detail. An L attached to a signal name designates it asserted low (logic 0). An H attached to a signal name designates it asserted high (logic 1).

Pin	Mnemonic	Function
1	DCOK L	Turns on +12 V power to module
2	+12 V RET	Ground
3	+WRITE L	Plus write data
4	R DATA H	Read data
5	W GATE L	Enables a write function
6	–WRITE L	Minus write data
7	SIDE 0	Not used
8	WRITE CURRENT SWITCH	Controls the level of the write current
9	ERASE GATE L	Controls tunnel erase function
10	+5 V DC	Side B index light emitting diode power source
11	SEL A L	Head select control signal
12	+12 V DC	+12 volt power source

10.4.3.1 DCOK L Output Signal – This signal controls the +12 volt power on the R/W module. When asserted, +12 volt power is applied to the write and erase circuits on the module. When unasserted, +12 volt power is removed from the circuits for protection of data on the diskette.

10.4.3.2 ±WRITE L Output Signals – This differential signal pair switches the direction of the write current in the R/W heads. The signals are alternately asserted but not simultaneously asserted. During write protected or non write operations both signals are unasserted.

10.4.3.3 R DATA H Input Signals – This signal is the data output of the R/W module to the seek and interface module. The signal contains positive going pulses averaging 1 μs in duration. Positive going edges contain timing information to reconstruct non return to zero (NRZ) data.

10.4.3.4 W GATE L Output Signal – This signal controls the write circuits on the R/W module. When asserted, this signal enables the write circuits. This signal is unasserted during both non write and write protected operations. It is also unasserted if the spindle motor is off, the drive side is not selected, the diskette is missing, or the diskette is in backwards.

10.4.3.5 WRITE CURRENT SWITCH Output Signal – This signal switches the write current level above and below track 44. This action minimizes peak shift in the heads and media due to close tolerances of the flux changes. When asserted, this signal enables a high write current when the heads are positioned over tracks 0 through 43. When unasserted, this signal enables a low write current when the head are over tracks 44 through 79.

10.4.3.6 ERASE GATE L Output Signal – This signal controls the current to the erase coils. When asserted, a current is produced in the selected erase coil. When writing is inhibited, this signal stays unasserted to disable the erase current.

10.4.3.7 SEL A L Output Signal – This signal selects one of the heads for read, write, and erase operations. When asserted, head A of drive side A is selected. When unasserted, head B of drive side B is selected.

10.4.4 Seek and Interface Power Connector J3

This section describes the connector which receives power for the entire drive. Figure 10-28 shows the location of J3 and other connectors of the module. Refer to Section 10.2.4 for the power requirements.

Pin	Mnemonic	Function
1	+12 VDC	Plus 12 volts DC
2	+12 VDC RET	Ground
3	+5 VDC RET	Ground
4	+5 VDC	Plus 5 volts DC

10.4.5 Seek and Interface Connectors J2,J5,J6,J7,J8,J10, and J17

This section describes the functions of the remaining connectors of the seek and interface module. A brief description of signal functions is also given. Figure 10-28 shows the location of these connectors and other connectors of the module. An L attached to a signal name designates it asserted low (logic 0). An H attached to a signal name designates it asserted high (logic 1).

10.4.5.1 Side A Switches and Indicators Connector J2

Pin	Mnemonic	Function
1	WP A H	Write protect indicator
2	SEL A L	Write protect/diskette present indicator select
3	DP A H	Diskette present indicator
4	SEL A L	Index indicator select
5	INDEX A L	Index indicator

10.4.5.2 Track 0 Sensor Connector J5

Pin	Mnemonic	Function
1	TK0S H	Track zero indicator
2	TK0A	Transmitter diode +5 volt source
3	TK0K	Transmitter/receiver diode sink

10.4.5.3 Side B Head Load Solenoid Connector J6

Pin	Mnemonic	Function
1	+12 VDC	Head load solenoid power source
2	SIDE B L	Solenoid control signal

10.4.5.4 Stepper Motor Connector J7

Pin	Mnemonic	Function
1	STM1	Stepper motor phase 1 control
2	STM2	Stepper motor phase 2 control
3	+12 VDC	Stepper motor +12 Vdc power source
4	STM3	Stepper motor phase 3 control
5	STM4	Stepper motor phase 4 control
6	+12 VDC	Stepper motor +12 Vdc power source

10.4.5.5 Side B Switches and Indicators Connector J8

Pin	Mnemonic	Function
1	WP B H	Write protect indicator
2	SEL B L	Write protect/diskette present indicator select
3	DP B H	Diskette present indicator
4	SEL B L	Index indicator select
5	INDEX B L	Index indicator

10.4.5.6 Side A Head Load Solenoid Connector J10

Pin	Mnemonic	Function
1	+12 VDC	Head load solenoid power source
2	SIDE A L	Solenoid control signal

10.4.5.7 Drive Select Jumper J17

Pin	Mnemonic	Function
1	GND	Ground
2	SEL 1 H	This signal selects the drive configuration. When asserted, jumper removed, DRIVE SEL 0 L and DRIVE SEL 1 L access the drive. When unasserted, jumper installed, DRIVE SEL 2 L and DRIVE SEL 3 L access the drive.

10.4.6 Motor Control Modules Connectors J4,J11,J16

This section describes the connectors of the motor control module. Figure 10-29 shows the location of these connectors and other connectors of the module. Connector J4 connects to the seek and interface modules connector J4 and is described in Section 10.4.2.

10.4.6.1 Spindle Motor Connector J11

Pin	Mnemonic	Function
1	TACH 1	Half of tachometer differential pair
2	TACH 2	Half of tachometer differential pair
3	MOT RET	Spindle motor power return
4	+12 VDC	+ 12 volt motor power source

10.4.6.2 Front Panel Operational Indicators Connector J16

Pin	Mnemonic	Function
1	+12 VDC	Indicator power source for side A
2	SIDE A L	Side A indicator control signal
3	+12 VDC	Indicator power source for side B
4	SIDE B L	Side B indicator control signal

10.4.7 Read/Write Module Connectors J9,J14,J15

This section describes the connectors of the R/W module. Figure 10-30 shows the location of these connectors and other connectors of the module. Connector J9 connects to the seek and interface modules connector J9 and is described in Section 10.4.3.

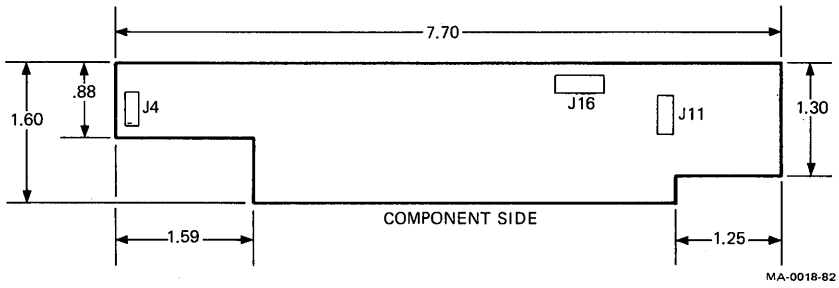


Figure 10-29 Motor Control Module Connector Locations

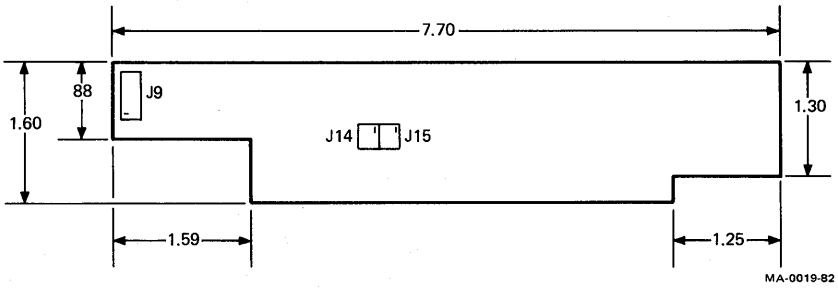


Figure 10-30 Read/Write Module Connector Locations

10.4.7.1 Side A Read, Write, and Erase Head Connector J14

Pin	Mnemonic	Function
1	HEAD SEL A	Side A head common
2	SHIELD	Head control line shield
3	ERASE COIL	Erase coil control line
4	+ COIL	Plus R/W coil control line
5	– COIL	Minus R/W coil control line
6	–	Not used

10.4.7.2 Side B Read, Write, and Erase Head Connector J15

Pin	Mnemonic	Function
1	HEAD SEL B	Side B head common
2	SHIELD	Head control line shield
3	ERASE COIL	Erase coil control line
4	+ COIL	Plus R/W coil control line
5	– COIL	Minus R/W coil control line
6	–	Not used

10.5 SPECIFICATIONS

The following paragraphs provide the specifications for the RX50 dual diskette drive.

10.5.1 Performance Specifications

Capacity (Formatted)	**MFM**	
Per drive	819,200	(800k bytes)
Per surface	409,600	(400k bytes)
Per track	5,120 bytes	
Diskette quantity	2	

Transfer Rate	**MFM**	
Per drive	250,000	(bits/sec)

Access Time	**Min**	**Typ**	**Max**
Track to track	6 ms	–	–
Head settling time	–	–	30 ms
Head load time	–	–	30 ms
Rotational latency	–	100 ms	200 ms
Random access	–	164 ms	–
Drive motor start	–	–	500 ms

10.5.2 Reliability Specifications

Mean time between failures	6000 POH at 30% duty cycle
spindle motor	2000 POH at 100% duty cycle
Mean time to repair	15 min
Error Rates	
(Typical Random Exerciser)	
Soft read errors	1 per 10^9 bits read
Hard read errors	1 per 10^{12} bits read
Seek errors	1 per 10^6 seeks
Media life	3×10^6 passes
Media insertion	1×10^4 insertions

10.5.3 Functional Specifications

Rotational speed	300 rpm
Speed variations	−1.5% to +1.5% max
Flux density (track 79)	5576 FCI
Track density	96 tracks per inch
Tracks (per diskette)	80
Outside track radius	57.15 mm (2.25 in)
Inside track radius	36.51 mm (1.427 in)
Data sectors (soft)	10
Data bytes per sector	512
Index	1

10.5.4 Electrical Specifications

Requirement	Min	Typ	Max
5 Volt Power	4.75 V	5.0 V	5.25 V
Ripple	–	–	50 mV
Current	–	0.50A	0.80A
12 Volt Power	11.4 V	12.0 V	12.6 V
Ripple	–	–	100 mV
Standby current	–	0.12A	0.25A
Operating current (seeking)	–	1.25A	1.8A
Startup current for 0.25 sec	–	–	2.7A

10.5.5 Environmental Specifications

Ambient temperature	15° C to 32° C (59° F to 90° F)
Relative humidity	20% to 80% noncondensing
Maximum wet bulb	25° C (78° F)
Shock and vibration	1G acceleration
Shipping shock	2G acceleration
Diskette jacket	40° C (40° F) max

10.5.6 Mechanical Specifications

Width	14.6.1 mm (5.75 in)
Height	82.55 mm (3.25 in)
Depth	215.9 mm (8.50 in)
Weight	2.18 kg (4.8 lb)
Operating power dissipation	17.5 W typ
Standby power dissipation	4.2 W typ

CHAPTER 11
RD50 HARD DISK CONTROLLER MODULE

11.1 GENERAL INFORMATION

The RD50 hard disk controller module is the interface component of the RD50 controller and drive subsystem for the Professional 350 system. Figure 11-1 shows the RD50 hard disk controller module and its relationship to the other components in the Professional 350 system.

11.1.1 Related Documentation

The following documents supplement this technical description on the RD50 controller.

Title	Document No.
Professional 350 Field Maintenance Print Set	MP-01394-00

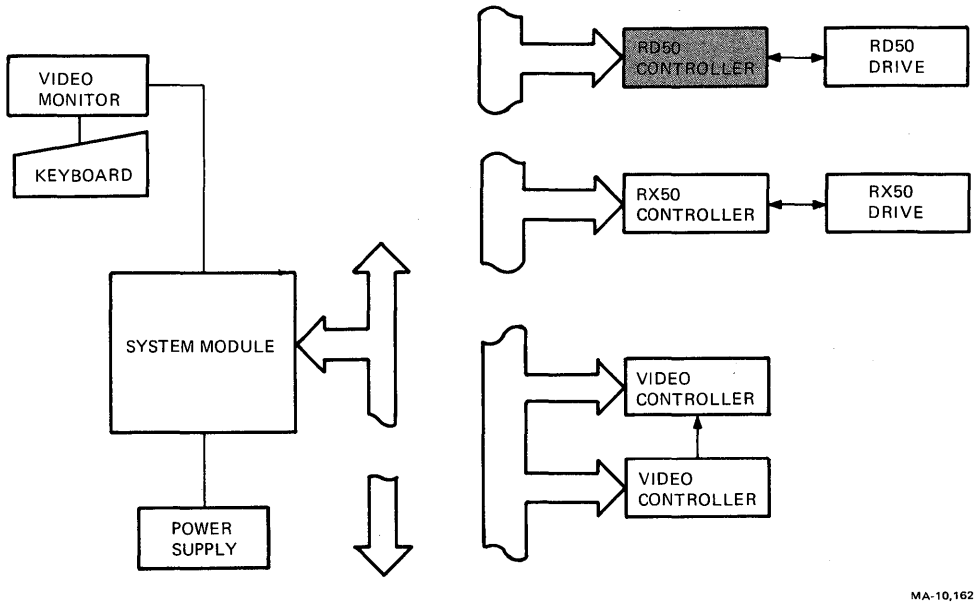


Figure 11-1 RD50 Module System Relation

11.1.2 RD50 Hard Disk Controller Module Introduction

The RD50 module interfaces a RD50 hard disk drive to the host processor (Figure 11-2). This module is a single 5.2 × 12 inch field replaceable unit (FRU PN 54-15134) which mounts in slot 1 of the Computing Terminal Interconnect (CTI) BUS option space. Three connectors on the module connect it to the host processor's CTI BUS and the drive.

A zero insertion force (ZIF) connector (J1) at the bottom of the module makes the module compatible to the CTI BUS. This connector allows the host processor to control the operations of the controller from the CTI BUS.

A 20-pin connector (J2) at the top of the module connects a cable (FRU PN 17-00282) from controller to the drive for data interfacing.

A 34-pin connector (J3) at the top of the module connects a cable (FRU PN 17-00286) from controller to the drive for command and status signal interfacing.

Refer to Chapter 5 for the connector description and signal definitions for J1. Section 11.4 provides connectors descriptions and signal definitions for J2 and J3.

11.2 FUNCTIONAL COMPONENTS

The following paragraphs describe the functional components of the RD50 module.

11.2.1 Overview

To the host processor, the RD50 controller appears as a set of registers accessible from the CTI BUS. The host processor reads and writes to these registers, issuing commands to the controller and retrieving or sending data to the controller. The RD50 controller then enables the RD50 hard disk drive to seek the data location and retrieve or store the data for the host processor. Seek operations are implied and embedded within the command sequence the controller accepts from the host processor. Refer to Sections 11.5 and 11.6 for more information about the registers and the sequence the host processor accesses them.

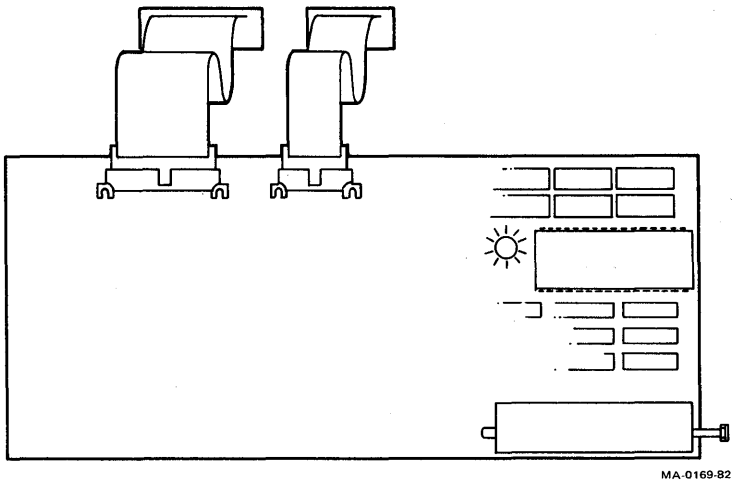


Figure 11-2 RD50 Disk Controller Module

The RD50 controller contains a memory for use as a sector buffer and storage for status and commands. The microprocessor (μP) control circuits map the memory for both functions. Accesses to the status and command registers are mapped into predefined memory locations for the μP control circuits. Accesses to the sector buffer are mapped into sequential address locations for use by the μP control circuits.

The transfers between the controller and the host processor are program controlled by the host processor. Under this program, the host processor loads or unloads a sector buffer on the controller by writing or reading to one of the registers. The controller then encodes or decodes the data between the sector data buffer and the drive. The controller performs the data error detection for all data transfers between its sector buffer and the drive.

The controller performs data transfers from the main memory to the disk surface in the following sequence.

1. The host processor controls a data transfer from main memory to a sector buffer in the controller.

2. The controller then controls the data transfer from its sector buffer to the RD50 disk drive.

Upon data request from the host processor, the steps are reversed for data transfers from the drive to main memory.

The following circuits in the RD50 controller pass data between the host processor and the RD50 hard disk drive (Figure 11-3).

- CTI BUS interface
- μP control
- Disk control and status
- MFM write data
- MFM read data

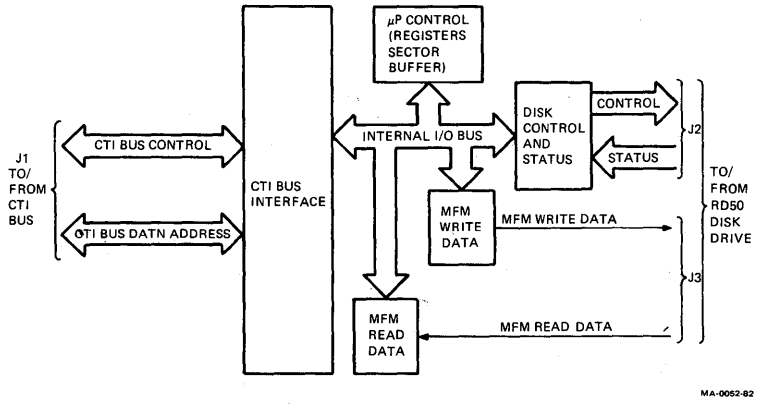


Figure 11-3 RD50 Controller Block Diagram

11.2.2 CTI BUS Interface Circuits

The host processor gains access to the controller through the CTI BUS interface circuits. This is done by reading and writing to the eight registers of the RD50 controller. (Refer to Section 11.5 for detailed information about the registers.) For the processor to access these registers, the CTI BUS interface circuits perform the following functions.

- Acknowledge addressing of its registers by the host processor.
- Pass data between the host processor and the controller.
- Generate interrupts for the host processor when the controller requires service.

Refer to Section 11.3.1 for more information on the operation of these circuits.

11.2.3 Microprocessor (μP) Control Circuits

The microprocessor control circuits are responsible for the internal operations of the RD50 controller. These circuits perform the following functions.

- Arbitrates the use of the internal I/O bus to control the internal data flow of the controller.
- Controls access to the memory in the μP control circuits.
- Generates the RD50 disk drive control signals from the commands the controller receives from the host processor.

Refer to Section 11.3.2 for more information on the operation of these circuits.

11.2.4 Disk Control and Status Circuits

The disk control and status circuits pass control and status information between the controller and the RD50 hard disk drive. The μP control circuits control these circuits to access drive status information from the drive and passing drive control information to the drive.

The μP control circuits process all control and status information. The host processor accesses the μP control circuits through the CTI BUS interface circuits. The μP control circuits then execute microprograms for computing the seek and select signals generated for the drive. The μP control circuits then cause the disk control and status circuits to pass the control and status information between the controller and drive.

Refer to Section 11.3.3 for further information on the detailed operation of these circuits.

11.2.5 MFM Write Data Circuits

The modified frequency modulation (MFM) write data circuits convert data the controller received from the host processor to MFM data for the RD50 hard disk drive. These circuits perform the following functions.

- Converts data bytes from the sector buffer in the μP control circuits to serial data.
- Calculates then adds two CRC bytes to the end of the serial data.
- Converts the serial data to MFM data.
- Generates status signals for the μP controller during the conversion.
- Passes the MFM write data to the RD50 hard disk drive.

The host processor selects the controller to perform a write operation by accessing registers in the μP control circuits through the CTI BUS interface circuits. The μP control circuits then execute a microprogram which allows the host processor to pass data through the CTI BUS interface circuits and store it in the sector buffer in the μP control circuits. The μP control circuits then cause the disk control and status circuits to pass control and status information between the controller and drive. This prepares and controls the drive to accept the data transfer. The μP control circuits then sequentially transfer the data stored in the sector buffer to the MFM write data circuits. The MFM write data circuits convert the data to MFM encoded data and pass it to the RD50 hard disk drive for storage.

Refer to Section 11.3.4 for further information on the detailed operation of these circuits.

11.2.6 MFM Read Data Circuits

The MFM read data circuits convert MFM data from the RD50 hard disk drive into data the host processor retrieves from the controller. These circuits perform the following functions.

- Searches the data on the RD50 hard disk drive for the valid MFM encoded header.
- Decodes the MFM data following the header from the RD50 hard disk drive.
- Converts the decoded data to bytes for the sector buffer in the μP control circuits.
- Calculates two CRC bytes from the data read from the drive and compares them to the values previously stored with the data.
- Generates status signals for the μP controller during the conversion.

The host processor selects the controller to perform a read operation by accessing registers in the μP control circuits through the CTI BUS interface circuits. The μP control circuits then execute a microprogram which causes the disk control and status circuits to send seek control signals to the drive and monitor status signals from the drive. The drive then returns MFM encoded data to the MFM read data circuits. These circuits convert the MFM encoded data to byte data which is stored in the sector buffer by the μP control circuits. After all the data is stored in the sector buffer, the host processor retrieves the data from the sector buffer through the CTI BUS interface circuits.

Refer to Section 11.3.5 for further information on the detailed operation of these circuits.

11.3 THEORY OF OPERATION

The RD50 controller has five circuit groups which interface the RD50 hard disk drive to the host processor. This section describes these circuits at a functional block diagram level and describes how the circuits function together.

The host processor accesses this controller by reading and writing to the registers of this controller. Only one register, the STATUS/INIT register, is discretely found in the controller's circuits. The remaining registers are mapped into memory by the μP control circuits. The μP control circuits control all accesses to the controllers memory. The memory is mapped as register space and sector buffer space.

The microprocessor on the controller processes all host processor accesses to all registers except the STATUS/INIT register. Accesses to registers require microprocessor intervention, but appear as address locations to the host processor.

Refer to Sections 11.5 and 11.6 for detailed descriptions of the RD50 controllers registers.

11.3.1 CTI BUS Interface Circuits

The CTI BUS Interface circuits allow the host processor access to the RD50 controllers registers. The CTI BUS interface circuit consists of the following circuits (Figure 11-4).

- CTI BUS I/O controller
- Data I/O port
- CTI BUS data/address transceivers
- Address buffer
- STATUS/INIT register

The host processor gains access to the RD50 controller through these circuits by passing an address to the circuits and then reading or writing the data. The host processor can address the STATUS/INIT register without intervention from the μP control circuits. To address the other seven registers, however, requires loading the address into the address buffer. The μP control circuits can then transfer the data between the data I/O ports and the μP control circuits over the internal I/O bus.

11.3.1.1 CTI BUS I/O Controller – Figure 11-4 shows the CTI BUS I/O controller receiving and generating CTI BUS control signals. The controller decodes CTI BUS control signals from the host processor and passes I/O control signals to the CTI BUS data/address transceivers, data I/O ports, address buffer, and the STATUS/INIT register. These I/O control signals cause the circuits to receive data and addresses from the CTI BUS or send data over the CTI BUS.

- **Interrupt Generation**

  Some of the CTI BUS control signals are interrupts and acknowledgements for the host processor. The CTI BUS I/O controller generates these interrupts from status signals it receives from the μP control circuits.

- **Controller Reset**

  Some of the CTI BUS control signals also generate a reset signal for the controller. This reset signal initializes the μP control circuits and the MFM write data circuits.

11.3.1.2 CTI Data/Address Transceivers – The CTI BUS data/address transceivers connect to the CTI BUS data/address lines. The I/O control signals cause the transceivers to pass data and addresses between the CTI BUS and the controller on internal data/address lines.

11.3.1.3 STATUS/INIT Register – When the STATUS/INIT register is addressed by the host processor, the CTI BUS I/O controller allows two things to occur. Either the controller status data is sent or the command signal, RESET, is received over the data/address lines. The reset signal initializes the μP control circuits and the MFM write data circuits. Accessing this register does not interrupt the μP controller circuits or the internal I/O bus.

11.3.1.4 Address Buffer – The address buffer receives three data/address lines from the CTI BUS data/address transceivers. When the host processor addresses any register except the STATUS/INIT register, this buffer is loaded with the bits that define access to one of the controllers registers. The μP control circuits receive this register address.

11.3.1.5 Data I/O Ports – The data I/O port contains buffers for temporarily holding the data and commands passed between the host processor and the RD50 controller. The CTI BUS I/O controller allows the host processor to write or read data from the CTI BUS through the CTI BUS data/address transceivers to the data I/O port. The read and write strobes generated by the μP controller circuits, allow the μP controller access to the data I/O port over the internal I/O bus.

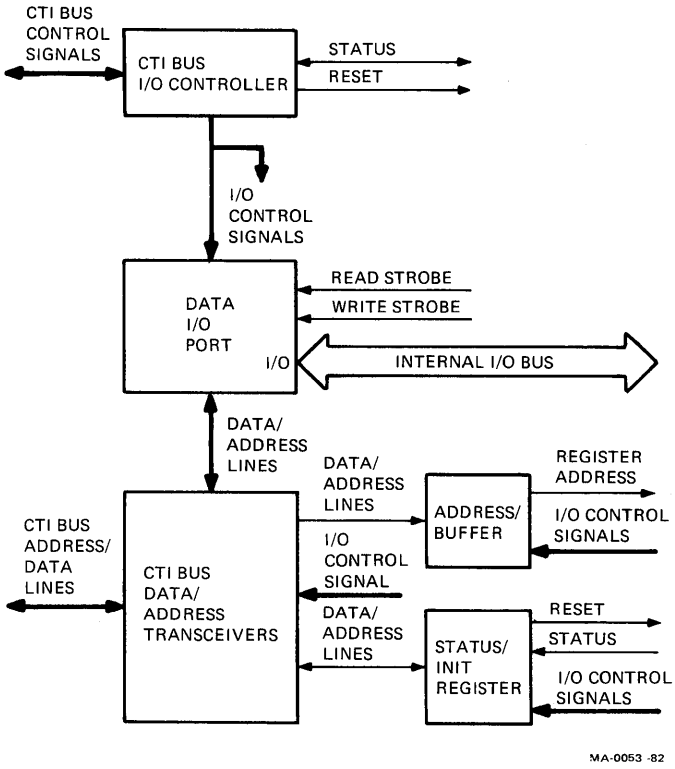
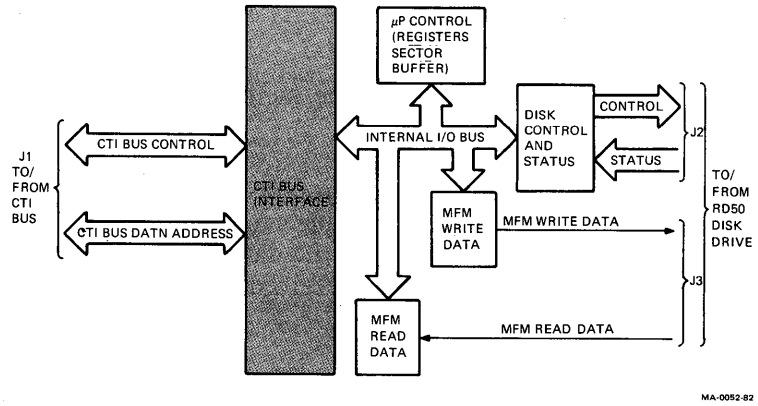


Figure 11-4 CTI BUS Interface Circuits



11.3.1.6 General Controller Access – While the controller performs a function, only the STATUS/INIT register can be accessed and no other RD50 controller register can be accessed. Figure 11-3, the block diagram, shows the structure of the internal I/O bus. All data and command transfers occur over this bus. It is an illegal procedure to interrupt the internal I/O bus while the controller is performing a function.

11.3.2 μP Control Circuits

The μP control circuits are responsible for the internal operation of the RD50 controller (Figure 11-5). The circuit consists of the following circuits.

- Microprocessor
- Microprogram ROMs
- Data flow controller
- Address/status buffer
- Memory
- Disk read/write controller

11.3.2.1 Internal I/O Bus Control – The μP control circuits control transfers over the internal I/O bus by generating the addresses for the microprogram ROMs data flow controller. The addresses access the microprograms to execute the RD50 controller functions. These addresses also generate read and write strobes to control transfers over the internal I/O bus.

The read and write strobes control accesses to the memory, address/status buffer, and disk R/W control buffer over the internal I/O bus. The read and write strobes also go to the other controller circuits to control transfers over the internal I/O bus.

11.3.2.2 Memory Mapping and Access – The microprocessor maps accesses to the memory for status and commands storage and sector buffer storage.

After the host processor addresses a register, except the STATUS/INIT register, the microprocessor causes the data flow controller to generate a read strobe. This strobe places the address/status buffer contents on the internal I/O bus. The microprocessor then maps the access to the memory and causes the data flow controller to generate read and write strobes. These strobes transfer data between memory and the data I/O port in the CTI BUS interface circuits. Accesses to all other circuits are performed in the same way.

When the host processor accesses the sector buffer, the memory returns a full status indicator to the address/status buffer for use by the microprocessor.

11.3.2.3 Disk Read Write Control Buffer – The microprocessor loads commands into the disk R/W control buffer. The buffer then generates data control signals to perform read and write functions between the controller and drive. These signals set up the MFM write data circuits to transmit data to the disk drive or sets up the MFM read data circuits to decode data received from the disk drive.

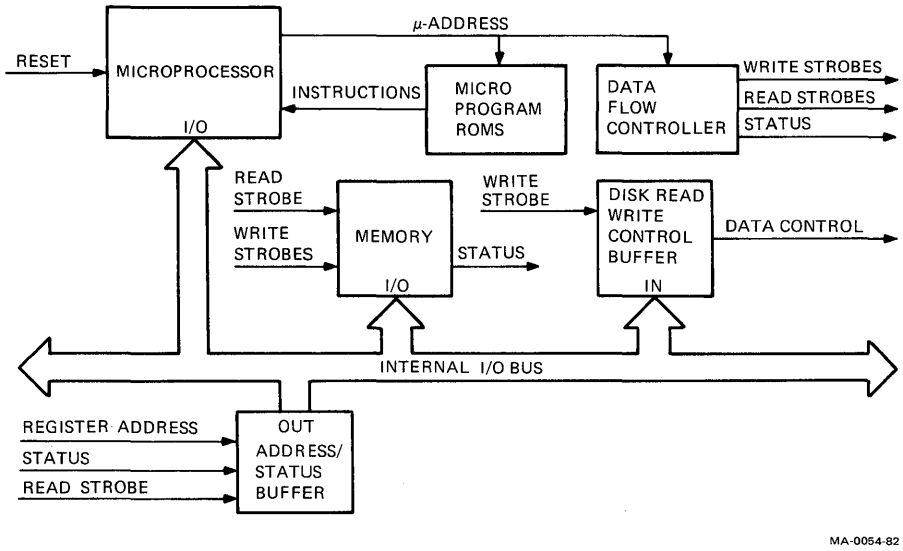
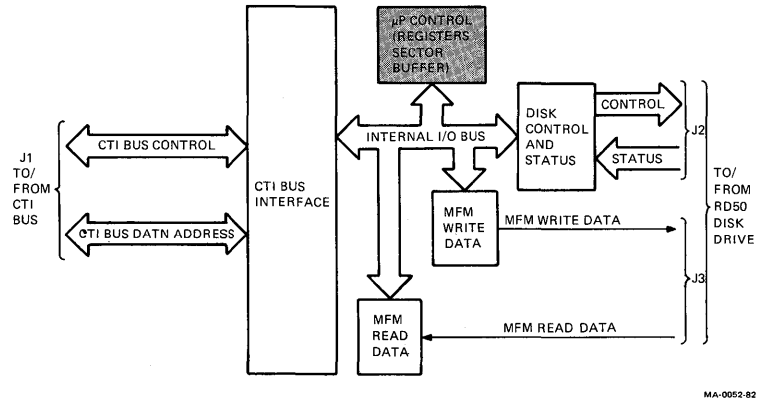


Figure 11-5 Microprocessor Control Circuits



11.3.3 Disk Control and Status Circuits – The disk control and status circuits pass control and status information between the RD50 controller and the RD50 hard disk drive (Figure 11-6). These circuits are used when the controller performs read and write functions between the controller and the drive. The disk control and status circuit consists of the following circuits.

- Disk control signal buffer
- Disk status signal buffer

The following sections describe the buffers and their uses. Refer to Section 11.4 for further information about the signals passed between the controller and drive by these buffers.

11.3.3.1 Disk Control Signal Buffer – This buffer passes disk control signals to the disk drive. Using write strobes, this buffer is loaded with control words on the internal I/O bus from the μP control circuits. The control words, generated by the μP control circuits, include select signals for the drive, write control signals, and seek control signals. The write control signals passed to the drive are also sent to the MFM write data circuits. This synchronizes drive control operations with the transmission of MFM write data to the drive.

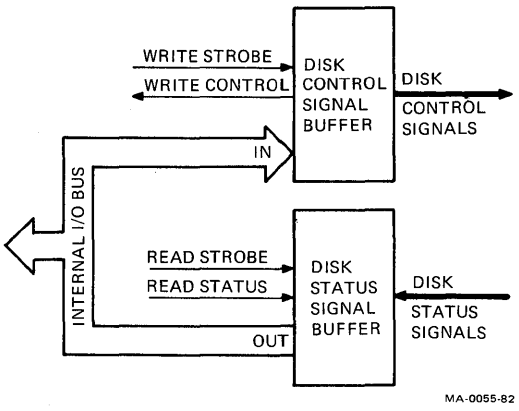
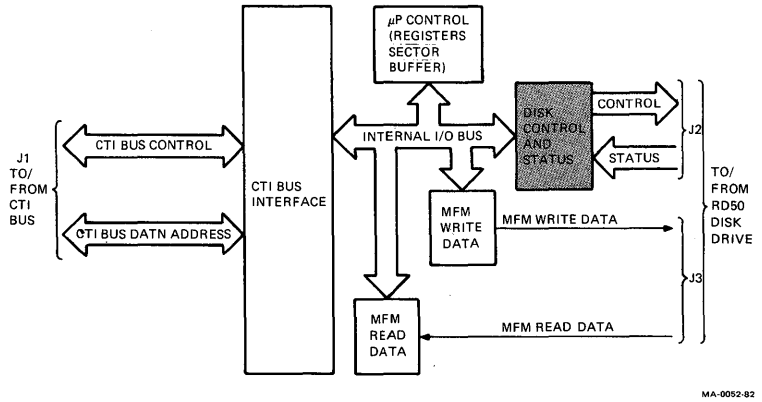


Figure 11-6 Disk Control and Status Circuits



11.3.3.2 Disk Status Signal Buffer – This buffer allows the μP control circuits to simultaneously access disk status information from the drive and read status information from the MFM read data circuits. When the μP control circuits generate a read strobe, this information passes over the internal I/O bus for the μP control circuits. The disk status information is used when the controller executes either a write or read function with the drive.

11.3.4 MFM Write Data Circuits

The MFM write data circuits convert byte data from the sector buffer to MFM data to be written to the disk (Figure 11-7). These circuits are used with the disk control and status circuits when the controller performs a write data function to the drive. The disk control and status circuits select the drive, cause the drive to seek to the desired cylinder, and enable the drive to write to the disks. The MFM write data circuits convert the data the controller received from the host processor to MFM data for the drive. The μP control circuits synchronizes all operations and signal generation to perform the write function.

The MFM write data circuit consists of the following circuits.

- Write clock generator
- Parallel-to-serial converter
- CRC generator/checker
- MFM generator

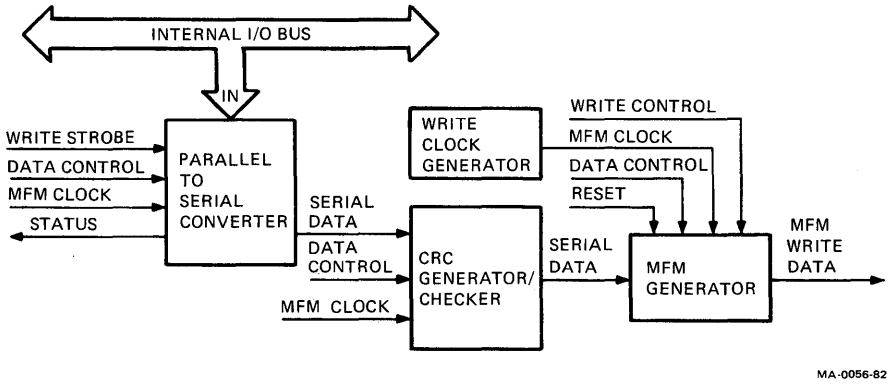
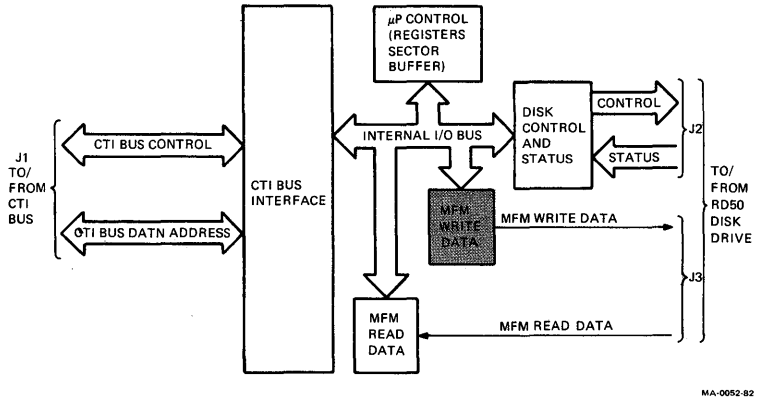


Figure 11-7 MFM Write Data Circuits



11.3.4.1 Parallel-to-Serial Converter – The μP control circuits use a data control signal to enable the parallel-to-serial converter. The μP control circuits also issue a write strobe. This action loads a data byte from the sector buffer over the internal I/O bus into the parallel-to-serial converter. The MFM clock from the write clock generator serially shifts the data byte to the CRC generator/checker. When the converter generates a byte shifted status signal, the μP control circuits loads the next data byte into the converter.

11.3.4.2 CRC Generator/Checker – When the μP control circuits enabled the parallel-to-serial converter, it also initialized the CRC generator/checker with a data control signal. The MFM clock shifts the data from the parallel-to-serial converter through the CRC generator/checker to the MFM generator. During the shift the CRC generator/checker calculates two CRC bytes. Those bytes are added to the end of the write data when the μP control circuits issue an end-of-data control signal.

11.3.4.3 MFM Generator – The MFM generator receives a data control signal from the μP control circuits. This initializes the generator before starting to convert the byte data to serial data. Write control signals from the disk control and status circuits indicate if the data is recorded on inner or outer tracks. They also indicate when the drive is enabled to write to the disks. The MFM generator can then select precompensation values and synchronizes transmission of MFM write data to the drive with a drive write control signal.

After the MFM generator is set up to convert the write data to MFM write data, the MFM clock causes the MFM generator to generate precompensated MFM write data for the drive.

11.3.5 MFM Read Data Circuits

The MFM read data circuits convert MFM encoded data read from the drive into 8-bit bytes for the sector buffer (Figure 11-8). The disk control and status circuits use these circuits when the controller performs a read data function with the drive. The disk control and status circuits select the drive, cause the drive to seek the desired cylinder, and enable the drive to read the disks. The μP control circuits synchronize all operations and signal generation to perform the read function.

The MFM read data circuit consists of the following circuits.

- Phase lock loop/data separator (PLL/DP)
- Address mark detector
- Serial-to-parallel converter
- CRC generator/checker

11.3.5.1 Phase Lock Loop/Data Separator – MFM read data is received from the disk drive via the phase lock loop/data separator. The μP control circuits enable this circuit with a data control signal to search for preambles.

Preambles indicate the start of MFM encoded read data for each sector. A detected preamble causes the separator to generate a read status signal to the disk control and status circuits for access by the μP control circuits.

During a preamble, the phase lock loop also locks to the MFM read data frequency and generates a delayed phase clock signal. The data separator then extracts the serial data at its clocked frequency from the MFM encoded read data. The phase lock loop/data separator then passes the serial data and data clocks to the address mark detector and the serial-to-parallel converter.

11.3.5.2 Address Mark Detector – The μP control circuits, with a data control signal, enable the address mark detector. The detector searches for an address mark in the serial data and data clocks. When the mark is detected, an address mark signal initializes and enables the serial-to-parallel converter.

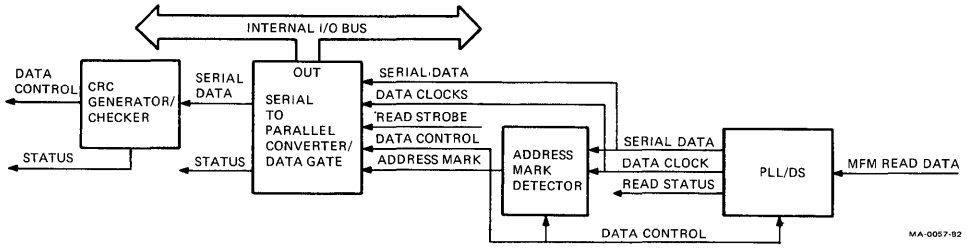
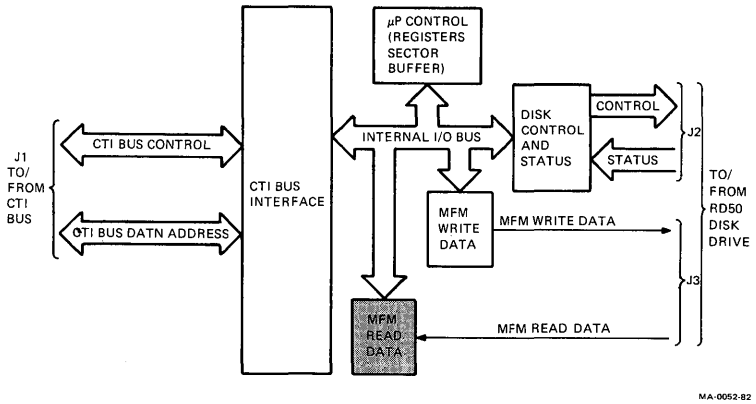


Figure 11-8 MFM Read Data Circuits



11.3.5.3 Serial-to-Parallel Converter – After the address mark detector enables the serial-to-parallel converter, the converter assembles byte data from the serial data and data clocks it receives from the phase lock loop/data separator. The converter assembles an 8-bit byte, then generates a byte ready status signal for the μP control circuits. The μP control circuits then generate a read strobe to retrieve the byte data over the internal I/O bus. This continues until the μP control circuits retrieve all the necessary data.

11.3.5.4 CRC Generator/Checker – The μP control circuits initialized the CRC generator/checker before the read cycle began. The serial-to-parallel converter assembles byte data, and passes the serial data to the CRC generator/checker. The CRC generator/checker monitors the data, computes two CRC bytes, and compares them to the CRC bytes at the end of the serial data. If the data is valid, the CRC generator/checker generates a status signal for the μP controller circuits.

11.3.6 Controller Data Flow Description

Figure 11-9 shows all the functional circuits described in Sections 11.3.1 through 11.3.5 and the data flow discussed below. Two examples of data flow are discussed below: a drive command data flow and a write data flow. These examples do not follow the microcode command sequences but are presented as an aid in understanding the RD50 controller capabilities.

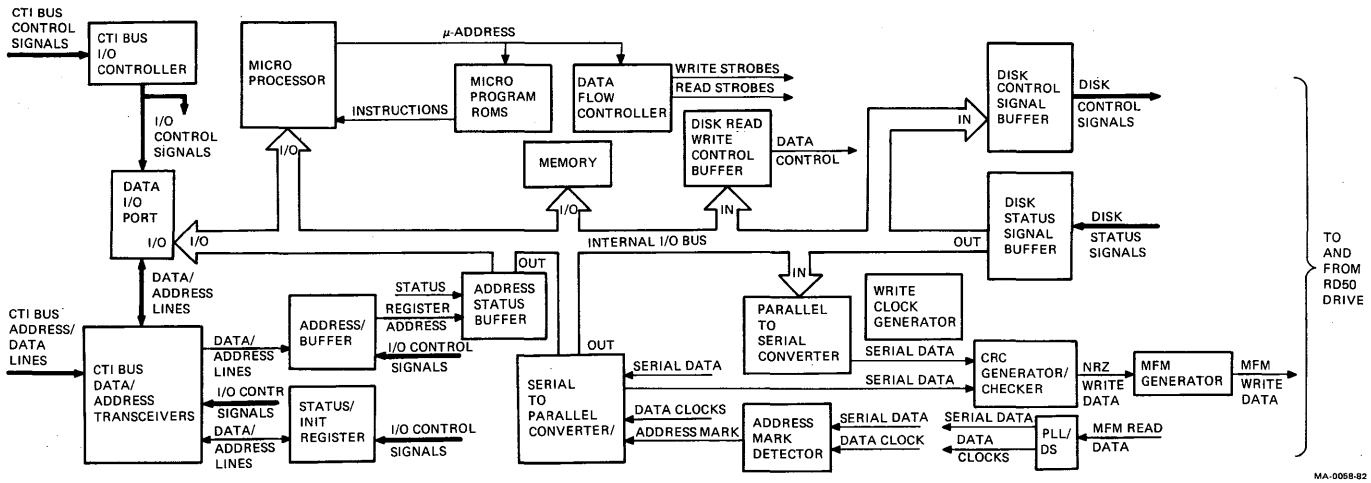


Figure 11-9 RD50 Controller Data Flow Diagram

11.3.6.1 Drive Command Data Flow – When the host processor sends a command to the drive, the following events occur.

- The host processor asserts the CTI BUS control signals in the correct sequence. The RD50 controller then accepts the register address and data and loads them into the address buffer and data I/O port.

- The μP control circuits access the register address in the address/status buffer then place the data in the assigned memory register location. The microprocessor interprets an access to the STA 2/COMMAND register as a go command.

- The μP control circuits perform the command and calculate the necessary values.

- The μP control circuits place a data command word on the internal I/O bus and then load the word into the disk control signal buffer.

- The disk control signal buffer then asserts the disk control signals selected by the data command word for the RD50 hard disk drive.

11.3.6.2 Write Data Flow – The following events occur when the host processor sends data to the drive for storage.

- Once the host processor issues a write command to the controller, it then accesses the data register continually. The host processor then places data words for the register on the CTI BUS address/data lines. The host processor then asserts the CTI BUS control signals in the correct sequence, activating the RD50 controller. The controller accepts the data and loads it into the data I/O ports.

- The μP controller continually accesses the data I/O ports and transfers the data over the internal I/O bus to the memory sector buffer.

- When the transfer from the host processor to the RD50 controller is complete, the controller places the data words from the memory on the internal I/O bus. It then loads the data word into the parallel-to-serial converter.

- The write clock generator clocks data through the MFM write data circuits, the parallel-to-serial converter, the CRC generator/checker, and the MFM generator.

- Once a data word is shifted past the parallel-to-serial converter, a status signal is generated for the address status register. This tells the μP controller when to load another data word into the converter.

- The serial data passes to the CRC generator/checker. Two CRC bytes are calculated to be added after the original write data is serially shifted out.

- The MFM generator continually receives the write data, encodes it into MFM format and sends it to the RD50 hard disk drive.

11.4 DETAILED CONNECTOR DESCRIPTIONS

The following section describes the signals passed between the RD50 controller, the RD50 hard disk drive and the host processor. Figure 11-10 shows the connectors on the controller, the signal names, and the signal flow.

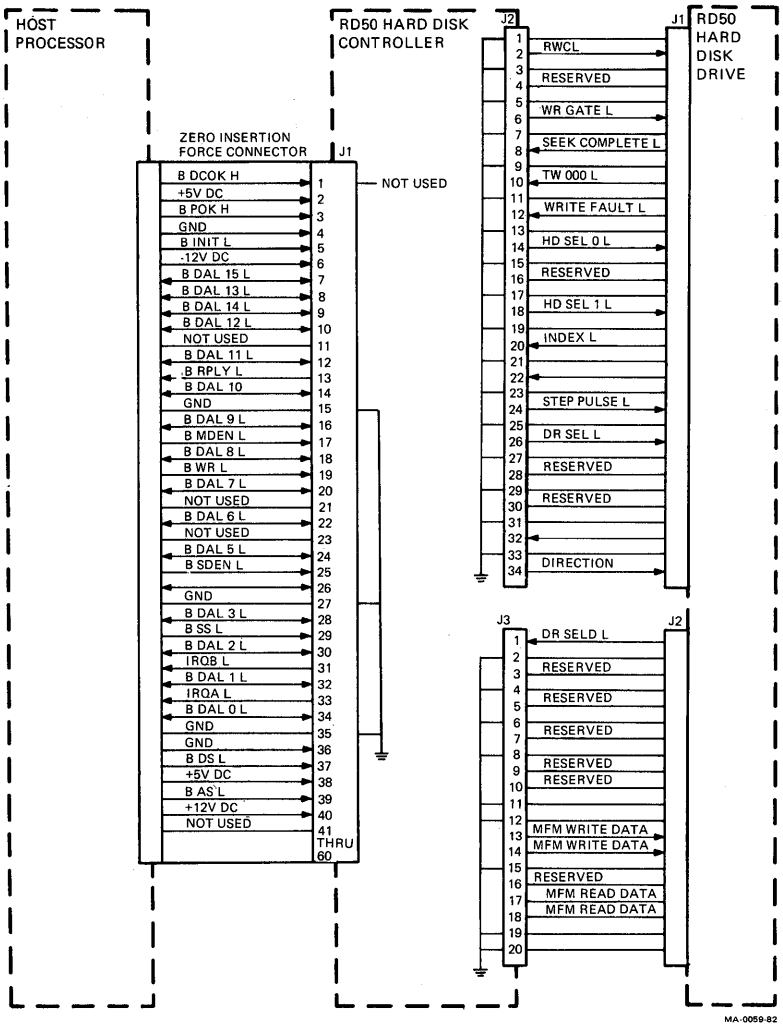


Figure 11-10 RD50 Controller Interface Signal Flow

11.4.1 CTI BUS Interface J1

The RD50 controller uses the data/address and control lines of the CTI BUS to implement program data transfers. For details see Chapter 5.

11.4.2 Disk Control/Status Connector J2

Table 11-1 lists the pin functions of the RD50 controller modules J2 connector. The signal mnemonic column also describes the asserted state of the signal. An L after the mnemonic indicates an asserted low state (logic zero). An H after the signal name indicates an asserted high state (logic high).

Table 11-1 Connector J2 Pin Description

Pin	Signal Name	Signal Mnemonic
1	Ground	
2	Reduced write current	RWC L
3	Ground	
4	Reserved	
5	Ground	
6	Write gate	WR GATE L
7	Ground	
8	Seek complete	SEEK COMPLETE L
9	Ground	
10	Track 000	TK000 L
11	Ground	
12	Write fault	WRITE FAULT L
13	Ground	
14	Head select 2^0	HD SEL 0 L
15	Ground	
16	Unspecified	
17	Ground	
18	Head select 2^1	HD SEL 1 L
19	Ground	
20	Index	INDEX L
21	Ground	
22	Ready	READY L
23	Ground	
24	Step	STEP PULSE L
25	Ground	
26	Drive select 1	DR SEL L
27	Ground	
28	Reserved	
29	Ground	
30	Reserved	
31	Ground	
32	Reserved	
33	Ground	
34	Direction In	DIRECTION IN L

11.4.2.1 REDUCED WRITE CURRENT (Pin 2) – This signal goes to the disk drive. When the controller asserts this signal and write gate, the disk drive uses a lower value of write current for writing on the disk. When this signal is unasserted, the disk drive uses a higher value of write current.

A lower write current is used when writing to tracks 128 through 157 rather than through tracks 0 through 127. This is because the heads fly lower over the inside tracks. When the heads are closer to the disk, a lower write current generates a weaker write magnetic field. Using a normal write current at the inside tracks would damage data in the adjacent tracks.

11.4.2.2 WRITE GATE (Pin 6) – This interface signal goes to the disk drive. The asserted state of this signal enables the write drivers when SEEK COMPLETE is asserted.

11.4.2.3 HEAD SELECT (Pin 14 and 18) – The two signals (HD SEL 0, and HD SEL 1) go to the disk drive. They form a binary word to select one of four disk drive heads.

11.4.2.4 STEP (Pin 24) – This interface signal goes to the disk drive. It controls the movement of the R/W heads. The DIRECTION IN signal defines direction of movement.

11.4.2.5 DIRECTION IN (Pin 34) – This interface signal goes to the disk drive. When a step pulse is issued, this signal defines the movement direction of the R/W heads. The asserted state of DIRECTION IN selects head movement towards the center of the disk. An unasserted signal selects head movement towards track zero.

11.4.2.6 DRIVE SELECT (Pin 26) – This signal goes to the drive. It indicates to the drive that the RD50 controller is ready. This signal becomes unasserted if any of the following occurs.

- The host processor sends a Reset command.
- POWER OK is unasserted on the CTI BUS.
- INIT is asserted on the CTI BUS.

11.4.2.7 SEEK COMPLETE (Pin 8) – This signal comes from the disk drive. When asserted, it indicates that the R/W heads have completed a seek command. When unasserted, all writing is inhibited. SEEK COMPLETE gets unasserted during any seek operation.

11.4.2.8 TRACK 000 (Pin 10) – This signal comes from the disk drive. When asserted, the R/W heads are positioned at track zero, the outermost track.

11.4.2.9 WRITE FAULT (Pin 12) – This signal comes from the disk drive. When asserted, one of the following conditions is detected and writing or R/W head motion is inhibited. The signal stays asserted until the condition is corrected.

- The heads receive current when WRITE GATE is asserted.
- DRIVE SELECT and WRITE GATE are asserted but the heads do not receive current.
- Either there are multiple heads, no head, or a head is incorrectly selected.
- The dc voltages are out of tolerance.

11.4.2.10 INDEX (Pin 20) – This signal comes from the disk drive as a low going pulse, and occurs once every disk revolution. The pulse indicates the beginning of the track.

11.4.2.11 READY (Pin 22) – This interface signal comes from the disk drive. When asserted, it indicates that the drive is ready to read, write, or seek. If SEEK COMPLETE and READY are asserted, then the I/O signals are valid. When unasserted, all writing and seeking actions are inhibited.

11.4.3 Disk Data I/O Connector J3

Table 11-2 lists the pin functions of the RD50 controller modules J3 connector. The signal mnemonic column also describes the asserted state of the signal. An L after the mnemonic indicates an asserted low state (logic zero). An H after the signal name indicates an asserted high state (logic high).

11.4.3.1 DRIVE SELECTED (Pin 1) – This signal comes from the disk drive. When asserted, it indicates that the drive is selected.

11.4.3.2 MFM WRITE DATA (Pins 13 and 14) – This differential pair goes to the disk drive and defines the transitions to be written on the disk surface. If WRITE GATE is asserted, a flux reversal occurs on the disk at the transition of +MFM WRITE DATA going more positive than the –MFM WRITE DATA. When the RD50 controller reads data from the drive, this signal becomes unasserted (+MFM WRITE DATA more negative than –MFM WRITE DATA).

11.4.3.3 MFM READ DATA (Pins 17 and 18) – This differential pair comes from the disk drive and is recovered read data from the selected head. The transition of the +MFM READ DATA signal going more positive than the –MFM READ DATA signal represents a flux reversal from the selected head.

Table 11-2 Connector J3 Pin Description

Pin	Signal Name	Signal Mnemonic
1	Drive selected	DRV SELD L
2	Ground	
3	Reserved	
4	Ground	
5	Spare	
6	Ground	
7	Unspecified	
8	Ground	
9	Spare	
10	Spare	
11	Ground	
12	Ground	
13	+MFM write data	+MFM WRITE DATA H
14	–MFM write data	–MFM WRITE DATA H
15	Ground	
16	Ground	
17	+MFM read data	+MFM READ DATA H
18	–MFM read data	–MFM READ DATA H
19	Ground	
20	Ground	

11.5 PROGRAMMING REGISTERS

The following sections describe the RD50 controller module registers. The registers access the sector buffer and the command modes of the controller.

The RD50 controller contains eight 16-bit registers for communications with the CTI BUS. These registers handle the communications between the RD50 controller and the host processor. All write operations to the registers are done by word transfers. Registers not defined are reserved. Table 11-3 defines the eight registers of the RD50 controller.

All the registers are available to the host processor unless the controller is executing a function. This is indicated by a set BUSY bit in the STATUS/INIT register. The STATUS/INIT register can be accessed at all times.

NOTE

An addressing error occurs, if the BUSY bit is set and then any register, except the STATUS/INIT register, is addressed. This forces the host processor to timeout trap to memory location 4. Refer to Chapter 5 for a detailed description of timeout trap.

11.5.1 ID Register (774000)

This is a read only (R/O) register. When read by the host, the register returns a 16-bit ID of 0101 hex, 000401 octal. This indicates the starting address range of the RD50 controller.

NOTE

If this register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor will timeout trap to memory location 4. Refer to Chapter 5 for a detailed description of timeout trap.

Table 11-3 Programming Registers

Bus Address	Name	Type
774000	ID	Read Only (R/O)
774004	ERROR/PRECOMP	R-Error/W-Precomp
774006	BACKUP REV/SECTOR ID	Read/Write (R/W)
774010	DATA BUFFER	R/W
774012	CYLINDER ID	R/W
774014	HEAD ID	R/W
774016	STA 2/COMMAND	R-STA 2/W-Command
774020	STATUS/INIT	R-Status/W-Init

11.5.2 ERROR/PRECOMP Register (774004)

This register has two functions: the high byte contains error information and the low byte stores the cylinder address at which write precompensation starts.

NOTE

If this register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor will timeout trap to memory location 4. Refer to Chapter 5 for a detailed description of timeout trap.

The high byte of this register is read only (R/O) for error information. This information is valid only if the error bit is set in the STA 2/COMMAND register. The high byte is cleared by issuing a new command. Table 11-4 defines the error bits of the high byte.

The low byte of this register is write only (W/O). It stores the cylinder number at which write precompensation starts. A default precompensation value is stored in this byte during a software or hardware initialization of the RD50 controller. The default value is cylinder number 128_{10} divided by 4. To use a different write precompensation point, divide the selected cylinder number by 4 and write the result into the low byte of this register.

11.5.2.1 DM Not Found, Bit 8 – This bit can only be set during a Read Sector command. It indicates that the Data Mark (DM) was not found after successfully reading the requested ID field.

11.5.2.2 TR000 Error, Bit 9 – This bit can only be set during a Restore command. It indicates that track zero (TR000) was not found after the drive performed seeks through 1100 tracks.

11.5.2.3 Illegal/Aborted Command, Bit 10 – This bit is set when any one of the following conditions occur.

- An invalid command is received.
- A command is received that cannot be executed based on status information from the drive (for example, write fault is present during a Write Sector command). The host must analyze other status bits to determine the cause of the error.
- A self-diagnostic error occurs during power-up or reset.

Table 11-4 Error Bit Definitions

Bit Number	Function
08	DM (data mark) not found
09	TR000 error
10	Illegal/aborted command
11	Not used
12	ID not found
13	CRC error, ID field
14	CRC error, data field
15	Not used

11.5.2.4 ID Not Found, Bit 12 – When this bit is set, it indicates that the disk the requested sector was not found after two revolutions of the disk.

NOTE

When bit 12 is set, a Restore command must be issued to return the drive to its track 000 reference point and clear the bit.

11.5.2.5 CRC Error ID Field, Bit 13 – When this bit is set, it indicates that a CRC error was found in the ID field. This bit can only be set if the comparing parameters (for example, cylinder number or sector number) match, but the CRC bytes do not match the computed CRC value.

11.5.2.6 CRC Error Data Field, Bit 14 – When this bit is set, it indicates that a CRC error was found in a data field during a Read Sector command. Although the data may be bad, the host may read the sector buffer.

11.5.3 BACKUP REVISION/SECTOR ID Register (774006)

This is a 16-bit read/write (R/W) register. The low byte of this register identifies the sector address used in the present operation. Refer to Table 11-5 for low byte bit definitions. The high byte of this register identifies the last time the sector was backed-up to off-line storage. Refer to Table 11-6 for high byte bit definitions.

NOTE

If this register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor will timeout trap to memory location 4. Refer to Chapter 5 for a detailed description of timeout trap.

NOTE

The sector ID byte can be read only after a Read Sector command is performed. It should not be read during a transfer of the internal sector buffer. Reading the byte during a transfer, resets the address pointer of the internal sector buffer to zero.

11.5.4 DATA BUFFER Register (774010)

This is a 16-bit read/write (R/W) register. It is the data transfer window between the RD50 controller and the host. Accessing this register resets both the DRQ bit in the STATUS/INIT register and the data request bit in the STA 2/COMMAND register.

When another word is ready to be read from or written to the sector buffer, the DRQ and data request bits are set again. The sequence is repeated until the buffer is completely read or written.

NOTE

If this register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor will timeout trap to memory location 4. Refer to Chapter 5 for a detailed description of timeout trap.

Table 11-5 Sector ID Bit Definitions

Bit Number	Function
0	Sector ID bit 0
1	Sector ID bit 1
2	Sector ID bit 2
3	Sector ID bit 3
4	Reserved
5, 6, 7	Not used

Table 11-6 Backup Revision Bit Definitions

Bit Number	Function
8	User-definable. Usually these
9	bits indicate the backup
10	code to off-line storage.
11	Codes are user defined.
12	
13	
14	
15	

11.5.5 CYLINDER ID Register (774012)

This is a 16-bit read/write (R/W) register. It identifies the cylinder used in the present operation. Refer to Table 11-7 for bit definitions.

NOTE

If this register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor will timeout trap to memory location 4. Refer to Chapter 5 for a detailed description of timeout trap.

11.5.6 HEAD ID Register (774014)

This is a read/write (R/W) register. It contains the ID of the surface/head used in the present operation. Refer to Table 11-8 for bit definitions.

NOTE

If this register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor will timeout trap to memory location 4. Refer to Chapter 5 for a detailed description of timeout trap.

Table 11-7 Cylinder ID Bit Definitions

Bit Number	Function
0	CYL ID bit 0
1	CYL ID bit 1
2	CYL ID bit 2
3	CYL ID bit 3
4	CYL ID bit 4
5	CYL ID bit 5
6	CYL ID bit 6
7	CYL ID bit 7
8	Reserved
9	Reserved
10–15	Not used

Table 11-8 Head ID Bit Definitions

Bit Number	Function
0	HD ID bit 0
1	HD ID bit 1
2	Reserved
3–15	Not used

11.5.7 STA 2/COMMAND Register (774016)

This is a read/write (R/W) register. The low byte contains the command used in the present operation; the high byte contains the secondary status (STA 2) of the operation. Refer to Table 11-9 for the bit definitions of the command byte. Refer to Table 11-10 for the bit definitions of the secondary status byte.

NOTE

If this register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor will timeout trap to memory location 4. Refer to Chapter 5 for a detailed description of timeout trap.

11.5.7.1 Restore – The Restore command moves the R/W head assembly to Track 000. This command is executed only if the DRIVE READY and SEEK COMPLETE signals are asserted and the WRITE FAULT signal is unasserted. Use this command after an ID Not Found error or a software INITIALIZE command.

After receiving the RESTORE command, the controller sets the BUSY bit in the STATUS/INIT register and tests for a TRACK 000 (TR000) signal.

If the TRACK 000 signal is asserted, the command is terminated. This sets the OP ENDED bit, and resets the BUSY bit in the STATUS/INIT register.

Table 11-9 Command Byte Bit Definitions

Command	Bits 7654 3210
Restore	0001 0000
Read sector	0010 0000
Write sector	0011 0000
Format	0101 0000

Table 11-10 Secondary Status Bit Definitions

Bit Number	Function
8	Error status
9	0 - not used
10	0 - not used
11	Data request
12	Seek complete
13	Write fault
14	Drive ready
15	0 - not used

If the TRACK 000 signal is unasserted when it is tested, a step pulse is issued to the drive. Step pulses are issued to the drive until the head assembly is positioned to track zero (TRACK 000 signal asserted) or 1100 step pulses are issued.

If track zero is found before 1100 step pulses are issued, the command is terminated with OP ENDED only.

However, if after 1100 step pulses are issued and the TRACK 000 signal is still unasserted, the command is terminated. The OP ENDED bit is set in the STATUS/INIT register, the error bit is set in the STA 2/COMMAND register, and the TR000 error bit is set in the ERROR/PRECOMP register.

11.5.7.2 Read Sector – A Read Sector command causes the RD50 controller to read one sector (256 16-bit words) from the drive to the sector buffer in the controller.

When the Read Sector command is received, the BUSY bit is set in the STATUS/INIT register. A seek is then performed to the requested cylinder in the CYLINDER ID register. Once the head assembly is positioned over the destination cylinder, each sector ID field is read. The sector IDs are compared with the head, sector, and cylinder addresses specified for the Read Sector command.

Once the correct sector is found, the ID field CRC is verified. If the ID field is correct, the controller then searches for the data mark.

When the data mark is detected, the data field is transferred to the sector buffer. The backup revision ID byte is loaded into the high byte of the BACKUP REV/SECTOR ID register. The CRC of the data field is then checked.

Once the data field CRC value is read, the BUSY bit is reset and the DRQ bit is set in the STATUS/INIT register.

If the computed data field CRC value does not compare to the value read from the sector, the error bit is set in the STA 2/COMMAND register. The CRC error data field (bit 14) is then set in the ERROR/ PRECOMP register.

If interrupts are enabled when the first DRQ bit is set, an interrupt to the host is generated. The host checks the error bit in the STA 2/COMMAND register or reads a data word out of the internal sector buffer using the DATA BUFFER register.

When the host reads the word from the DATA BUFFER register, the DRQ bit is reset. When the next word is ready, another DRQ is generated. This sequence is repeated 256 times before the buffer is completely read. Once the sector buffer is empty, OP ENDED is set in the STATUS/INIT register. This indicates that the operation is complete.

During a Read Sector command, errors may occur which will terminate the command. If this occurs, the BUSY bit is reset and the OP ENDED bit is set in the STATUS/INIT register. Also, the error bit is set in the STA 2/COMMAND register. This indicates that the ERROR/PRECOMP register contains detailed error information (see Section 11.5.2). The following events terminate a command.

- The correct ID field cylinder, head, or sector address cannot be found within two disk revolutions. The ID Not Found error (bit 12) is set in the ERROR/PRECOMP register.
- The ID field cylinder, head, and sector addresses are found but the computed ID field CRC does not match the one recorded. The CRC error ID field (bit 13) is set in the ERROR/PRECOMP register.
- The DM is not detected within 16 bytes of the ID field CRC and after two disk revolutions. The DM Not Found error (bit 8) is set in the ERROR/PRECOMP register.

11.5.7.3 Write Sector – The Write Sector command writes the internal sector buffer (256 16-bit words) to the specified cylinder, head, and sector of the disk.

When this command is received the DRQ bit is set in the STATUS/INIT register. If the interrupts are enabled, this generates an interrupt to the host.

The host then transfers a 16-bit data word to the DATA BUFFER register which resets the DRQ bit. After the controller stores the data word in the sector buffer, the controller sets the DRQ bit again. This sequence is repeated until 256 words are loaded into the sector buffer.

After the buffer is loaded, the BUSY bit is set in the STATUS/INIT register. A seek is then performed to the requested cylinder and the ID field is verified.

After the ID field is verified, the controller turns on the write gate and writes to the specified cylinder, head, and sector. This includes the data preamble, the sync mark, the data mark, the data, the backup revision level byte, the reserved bytes, and the two bytes of CRC.

When it has completed writing this information, the controller resets BUSY and sets OP ENDED in the STATUS/INIT register. If the interrupts are enabled, the OP ENDED bit generates an interrupt to the host. This indicates that the write operation is complete.

There are two error conditions that can occur during a Write Sector command: ID Not Found and ID Field CRC error. If either occurs, the operation terminates with ERROR set in the STA 2/COMMAND register and OP ENDED set and BUSY reset in the STATUS/INIT register. The ERROR/PRECOMP register contains detailed error information.

11.5.7.4 Format – This command is a special type of write command. It allows the host processor to format one track at a time and defines the physical location of each sector on the track.

To use this command, the host processor loads the cylinder ID and head ID of the track to be formatted into the CYLINDER ID register and the HEAD ID register. The host processor then loads the Format command into the STA 2/COMMAND register.

When the controller decodes the command, it generates the DRQs needed to load 256 words into the sector buffer. When the first DRQ occurs, the host processor loads the data buffer in the controller with the sector ID assigned to the first sector after the INDEX signal.

When the second DRQ occurs, the host processor loads the data buffer with the sector ID assigned to the second sector after the INDEX signal. The host processor continues to assign sector IDs until it reaches the seventeenth DRQ.

From the seventeenth DRQ until the last DRQ, the host loads data into the data buffer. This operation assigns the fill character to be written into the sector.

To address the sectors sequentially around the track from 0 to 15 load each word with the corresponding sector address (for example, word 0 with sector address zero, word 1 with sector address one, word 2 with sector address two).

To interleave the sectors in a random pattern such as 0, 8, 1, 9, 2, 10, 3, 11, 4, 12, 5, 13, 6, 14, 7, and 15, load each word with the random sector address (for example, word 0 with sector address zero, word 1 with sector address eight, word 2 with sector address one).

NOTE
The bit organization is the same for both these words and the BACKUP REV/SECTOR ID register (see Section 11.5.3 and Table 11-5)

Once the sector buffer is loaded, the controller sets the BUSY bit in the STATUS/INIT register. The drive seeks to the specified cylinder and selects the head.

The controller then waits for the INDEX signal from the drive. When the signal is received, the controller turns on the write gate and writes the complete track.

The cylinder address used is the cylinder address stored in the CYLINDER ID register. The head address used is the head address stored in the HEAD ID register. The sector address for the first sector is word 0 of the sector buffer, the sector address for the second sector is word 1 of the sector buffer, and so on.

The data fields, backup revision bytes, and reserved bytes are set to zero.

After the track is completely written, the controller resets the BUSY bit and sets the OP ENDED bit in the STATUS/INIT register. This indicates that the operation is complete.

11.5.7.5 Error Status – This bit indicates that the ERROR/PRECOMP register contains a valid error status. It provides a fast way for the host to check if error information is stored in the ERROR/PRECOMP register. Once the error status bit is set, the host reads the ERROR/PRECOMP register and determines what caused the error.

11.5.7.6 Data Request – This bit (together with DRQ) is set when data is ready to be read or written to the sector buffer. Reading or writing to the DATA BUFFER register clears both this bit and DRQ. When another word is ready to be read from or written to the sector buffer, the DRQ and data request bits are set again. The sequence is repeated until the buffer is completely read or written.

11.5.7.7 Seek Complete – This bit indicates the condition of the Seek Complete signal from the drive. When set, it indicates the drive is ready to read or write.

11.5.7.8 Write Fault – When this bit is set, it indicates a write fault condition exists at the drive. If a write operation was performed when this fault condition occurred, data was not written correctly because of a failure in drive electronics. This bit can only be reset by turning the system power off and then back on again.

11.5.7.9 Drive Ready – When this bit is set, it indicates that the drive is ready to seek, read, or write.

11.5.8 STATUS/INIT Register (774020)

This register may be read or written to at any time. All other registers should only be accessed if the BUSY bit in this register is reset. Table 11-11 defines the bits of this register.

11.5.8.1 OP ENDED – When this bit is set, it indicates that the operation specified in the command register is complete. The status of the completed operation is indicated in the STA 2/COMMAND register. If interrupts are enabled, this bit also causes an interrupt to the host. The OP ENDED bit is reset by reading or writing to the STA 2/COMMAND register.

11.5.8.2 RESET/INITIALIZE – When this bit is set it causes an INITIALIZATION sequence (see Section 11.5.4).

Table 11-11 STATUS/INIT Register Definitions

Bit Number	Function
0	OP ENDED (Operation ended) R/O
1	Not used
2	Not used
3	RESET/INITIALIZE W/O
4	Not used
5	Not used
6	Not used
7	DRQ (data transfer request) R/O
8	Reserved
9	Not used
10	Not used
11	Not used
12	Not used
13	Not used
14	Not used
15	BUSY (internal I/O bus in use) R/O

11.5.8.3 DRQ – When this bit is set, it indicates a data transfer is needed. The bit is cleared by accessing the Data Buffer register. When another word is ready to be read from or written to the sector buffer, the DRQ (data required) bit and the data request bit are set again. The sequence is repeated until the buffer is completely read or written.

If interrupts are enabled, this bit also causes an interrupt to the host processor.

11.5.8.4 BUSY – When this bit is set, it indicates no other register may be accessed. This bit is set when the controller uses the internal I/O bus.

11.6 GENERAL SEQUENCE OF OPERATION

The RD50 controller can store and recover data blocks of 256 16-bit words. The following sections describe the general sequence of operations for the RD50 controller.

11.6.1 Read Sector, Write Sector, Format Command

To perform a Read Sector, Write Sector, or Format command, the host processor does the following.

- Reads the STATUS/INIT register (774020) and determines that the BUSY bit is not set.
- Loads the CYLINDER ID register (774012) with a cylinder address.
- Loads the ERROR/PRECOMP register (774004) with the write precompensation cylinder address if the address is not cylinder 128.

NOTE
The ERROR/PRECOMP register is loaded with the write precompensation cylinder address during initialization. It is not necessary to load it during each operation.

- Loads the HEAD ID register (774014) with a head number.
- Loads the BACKUP REV/SECTOR ID register (774006) with a sector address and backup revision information.
- Enables the RD50 controller interrupts if the host processor wants them.
- Loads the STA 2/COMMAND register (774016) with a command.
- Waits for either a DRQ interrupt or for the BUSY bit to be reset and the DRQ bit to be set in the STATUS/INIT register.

11.6.1.1 Read Sector Command Follow-up Sequence – After the controller completes a Read Sector command, the host checks the error bit in the STA 2/COMMAND register. If the error bit is reset, the host moves the DATA BUFFER register contents to main memory. After each word transfer, the host waits for another DRQ interrupt or loops on the DRQ bit in the STATUS/INIT register.

Both the DRQ bit and the data request bit are set after each data word is loaded into the DATA BUFFER register. After all 256 words are read, the OP ENDED bit is set in the STATUS/INIT register and if interrupts are enabled an OP ENDED interrupt is generated.

11.6.1.2 Write Sector and Format Command Preparation – Before the controller executes a Write Sector or a Format command, the host moves the first data word from main memory to the DATA BUFFER register. After each word transfer, the host waits for another DRQ interrupt or loops on the DRQ bit in the STATUS/INIT register.

Both the DRQ bit and the data request bit are set when the controller is ready to load the next data word into the DATA BUFFER register. After all 256 words are loaded, the controller executes the command.

11.6.1.3 Write Sector and Format Command Follow-up – The controller indicates a completed command by resetting the BUSY bit and setting the OP ENDED bit in the STATUS/INIT register and if interrupts are enabled generates an OP ENDED interrupt. The host processor checks the error bit in the STA 2/COMMAND register to determine error free Write Sector or Format command completion.

11.6.2 Read After Write Verify Follow-up

A Read After Write Verify operation occurs when a Read Sector command follows a Write Sector command on the same sector. After the completion of the READ command, the host processor verifies the data written to the disk.

After loading a Read Sector command into the STA 2/COMMAND register, the host waits for the DRQ bit to set. The host then checks the error bit in the STA 2/COMMAND register to verify the data.

11.6.3 Restore Command

To perform a Restore command the host processor does the following.

- Enables RD50 controller interrupts in the CPU if the host processor wants them.
- Loads the STA 2/COMMAND register with the Restore command code.
- Waits for either an OP ENDED interrupt or for the BUSY bit to be reset and the OP ENDED bit to be set in the STATUS/INIT register.
- The host processor determines an error free Restore command completion by checking the error bit in the STA 2/COMMAND register.

11.6.4 Initialization Sequence

The controller executes a Reset/Initialize sequence for the following conditions.

- During the power-up sequence.
- When the CTI BUS signal INIT is asserted.
- When the CTI BUS signal P OK is unasserted then asserted.
- When the host processor sets the RESET/INITIALIZE bit in the STATUS/INIT register..

If any one of the above conditions occur, the microprocessor does the following.

- Sets the BUSY bit in the STATUS/INIT register.
- Performs an internal initialize sequence.
- Performs an internal memory test.
- Clears the internal sector buffer.
- Clears the CYLINDER ID, HEAD ID, and BACKUP REV/SECTOR ID registers.
- Stores a default write precompensation cylinder address of 128 in the PRECOMP byte.
- Clears the error byte in the ERROR/PRECOMP register.

NOTE
During a power-up initialization sequence, the drive performs an auto restore to track zero.

- Resets the BUSY bit and sets OP ENDED bit when the initialization sequence is complete.

NOTE
After an initialization sequence, the READY and SEEK COMPLETE bits must be set in the STA 2/ COMMAND register before the host processor accesses any register except the STATUS/INIT register.

11.7 SPECIFICATIONS

The following paragraphs provide the RD50 controller specifications.

11.7.1 Environmental

Specification	Min	Nom	Max
Temperature	10° C (50° F)	–	50° C (104° F)
Humidity	10%	–	90%
Wet bulb reading	–	–	28° C *82° F)
Dew point	2° C (36° F)	–	–
Temperature	–	–	20° C/hour
fluctuation	–	–	36° F/hour
Power dissipation	–	49 W	83 W

11.7.2 Power

Voltage	Current
+5 volts	4.8 A
−12 volts	200 mA
+12 volts	100 mA

CHAPTER 12
RD50 HARD DISK DRIVE

12.1 GENERAL INFORMATION

The RD50 hard disk drive is the storage component of the RD50 controller and drive subsystem for the Professional 350 computer system. Figure 12-1 shows the drive's relationship to other components of the system.

12.1.1 Related Documentation

The following documents also provide information on the RD50-A hard disk drive.

Title	Document No.
Professional 350 Field Maintenance Print Set	MP-01394-00

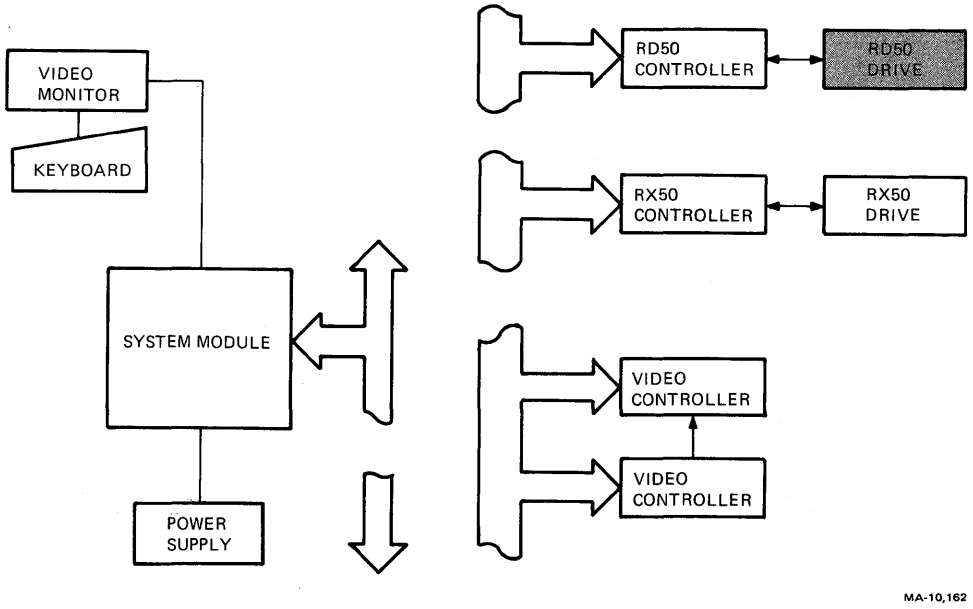


Figure 12-1 RD50 Hard Disk Drive System Relation

12.1.2 RD50 Hard Disk Drive Introduction

The RD50 drive is a 5.25 inch (130 mm) non-removable media disk drive. The disk drive, called a Winchester drive, allows the heads, which normally fly over the disk surface (media) to land when the drive is powered off. This drive uses lubricated media and lightly loaded (mechanically) read/write (R/W) heads.

High-bit densities on the media are achieved by flying the heads at a height of 20 micro-inches. This flying height requires a clean air environment. To ensure this, the head and disk assembly (HDA) is manufactured and sealed in an environmentally clean room.

A controller interfaces the RD50 drive to a host computer. This controls the drive operations and converts the data to or from the modified frequency modulation (MFM) format required by the drive.

12.2 FUNCTIONAL COMPONENTS

The following paragraphs describe the functions of the components that make up the RD50 drive.

12.2.1 Overview

The RD50 drive is a random access storage device which uses two non-removable 5.25 inch disks as storage media. Each disk surface uses one movable head to service 153 data tracks. The total formatted capacity of the drive is 5 megabytes (16 sectors per track, 512 bytes per sector, 612 tracks per drive). Figure 12-2 shows the RD50 drive and Figure 12-3 shows the functional components of the RD50 drive.

This drive consists of a drive mechanism and two circuit modules. The drive mechanism contains the storage media and the supporting mechanical assemblies. One circuit module, the motor control module, contains the spindle motor control circuit. The other module, the read/write (R/W) module, contains the following circuits.

- Power-on circuit
- Fault detection circuit
- Seek circuit
- Write circuit
- Read circuit

Two connectors on the R/W module connect the drive to a controller. A third connector on the R/W module connects the drive to a power source. A spring, located on the mounting plate, grounds the drive frame to the system chassis.

The RD50 drive is a field replaceable unit (FRU PN RD50-A). The R/W module is also a FRU of the RD50-A drive (PN 29-24112-00). Chapter 11 describes the two cables that connect the RD50 drive to a controller. Chapter 13 describes the power cable that connects the RD50 drive to a power supply. For more information on drive maintenance refer to Section 12.5.

12.2.2 Drive Mechanism

The drive mechanism is an HDA which contains a stepper motor, a head carriage assembly, a spindle motor, media, and sensors and hardware to support the HDA.

12.2.3 Spindle Motor Control Circuit

The spindle motor control circuit is located on the motor control module. This circuit keeps a brushless spindle motor rotating at a constant speed.

12.2.4 Power-Up Circuit

The power-up circuit provides the RD50 drive with a power-on sequence. This sequence allows the spindle motor time to rotate up to speed, forces a recalibration (recal) to the outer track of the media (track 0), and indicates that the RD50 drive is ready.

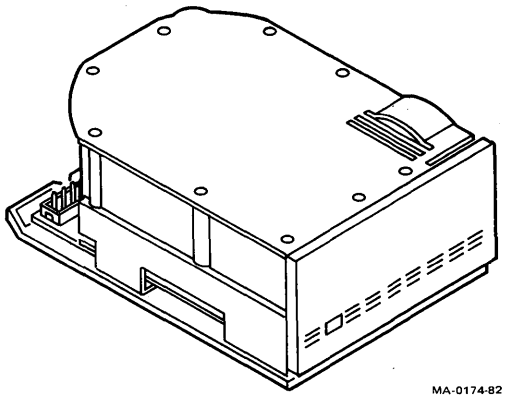


Figure 12-2 RD50 Hard Disk Drive

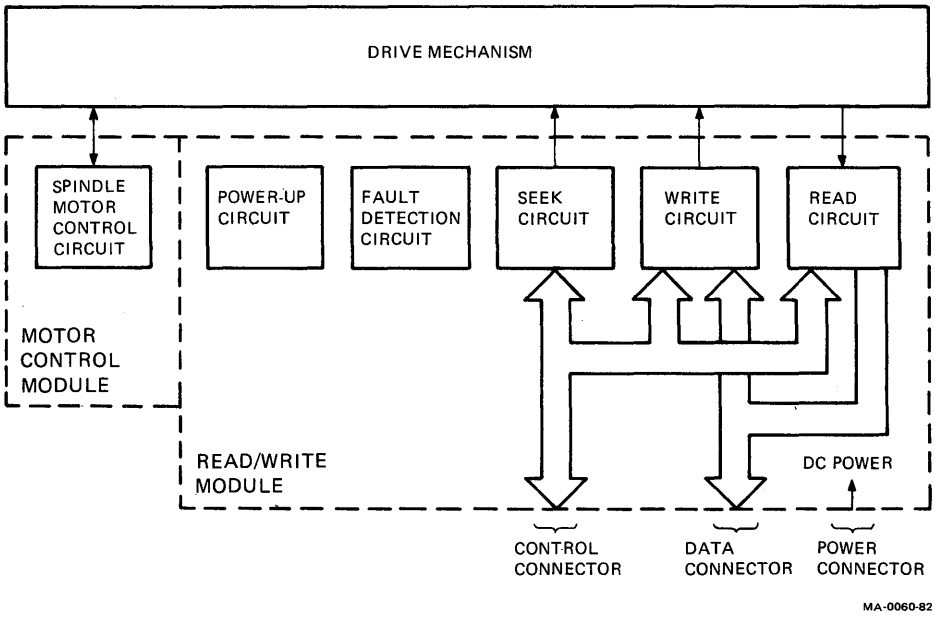


Figure 12-3 Simple Block Diagram

12.2.5 Fault Detection Circuit
The fault detection circuit monitors the RD50 drive for faults which could destroy stored data. When a fault is detected this circuit generates a status signal for the controller and disables the write circuit.

12.2.6 Seek Circuit
The seek circuit controls a stepper motor that actuates the head carriage assembly. This assembly positions the R/W heads over a data track. The seek circuit receives control signals directly from the controller.

12.2.7 Write Circuit
The write circuit receives modified frequency modulated (MFM) data and control signals from the controller. The circuit then generates the write current for the heads to store the data on the media as magnetic domains.

12.2.8 Read Circuit
The R/W heads sense the data recorded on the media. The read circuit then converts the data to MFM data pulses.

12.3 THEORY OF OPERATION
The following paragraphs describe the RD50 drive functions.

12.3.1 Drive Mechanism Detailed Operations
The drive mechanism is an HDA with the supporting sensors and hardware. The sealed HDA consists of the following items.

- Stepper motor and head carriage assembly
- Spindle motor assembly and speed sensor circuit
- Filters

The supporting sensors and hardware consist of the following items.

- Index sensor
- Track zero sensor
- Spindle brake
- Spindle ground spring
- Drive select indicator (LED)
- Mounting hardware

12.3.1.1 Sealed Head and Disk Assembly (HDA) – The following paragraphs describe the items contained in the sealed head and disk assembly.

NOTE

The HDA is an environmentally sealed unit. Opening this unit or breaking its seals destroys the data stored on the media and the reliability of the drive.

Stepper Motor and Head Carriage Assembly
Figure 12-4 shows the stepper motor and head carriage assembly. This assembly moves the flying R/W heads across rotating media and positions them over the data tracks. These tracks are 4000 microinches apart, and require close tolerances between all mechanical parts.

Three bearings rotate on shafts connected to the head carriage assembly. Each bearing makes a two point contact to a carriage rod. The bearings are arranged so that the two inner bearings roll on a common carriage rod and the outer bearing roll on a second carriage rod.

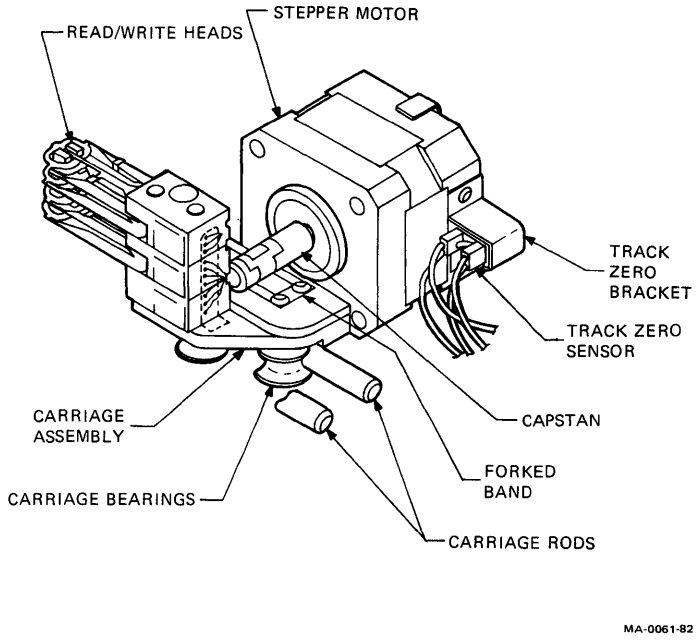
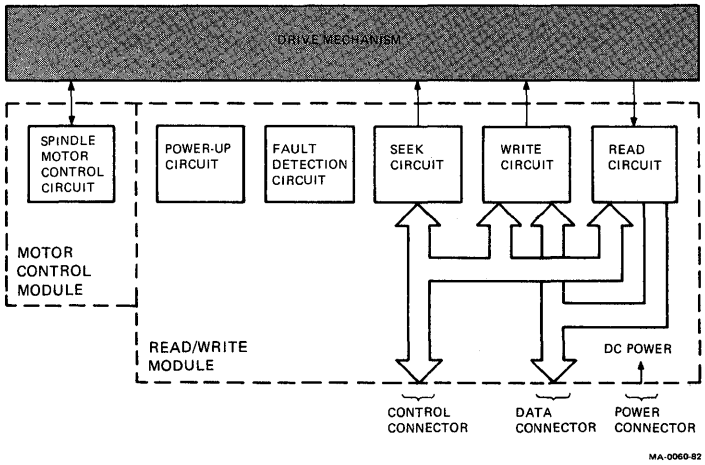


Figure 12-4 Stepper Motor and Head Carriage Assembly



A forked band wraps around the capstan of the stepper motor and attaches to the head carriage assembly. As the stepper motor capstan rotates, the head carriage assembly moves out towards track zero or in towards track 152.

The capstan is rotated in increments of 0.9° called half steps. Two stepper motor cycles, or 1.8° of rotation, move the heads one full track.

Spindle Motor Assembly and Speed Sensor Circuit

NOTE
The spindle motor assembly is part of the HDA. Removal or disassembly of this unit destroys the data stored on the media and the reliability of the drive.

The spindle motor assembly consists of two disks attached to a spindle and rotated at a constant speed of 3600 rpm by a brushless dc motor. A speed sensor circuit in the spindle motor sends a signal, representing the spindle motor's speed, to the spindle motor control circuit. The spindle motor control circuit then controls the spindle motor's speed. Refer to Section 12.3.2 for more information.

As the motor rotates the disks (media), an air cushion between the heads and the media is created. This causes the heads to fly above the media at an average height of 20 microinches. This distance allows high density data recording.

When power is removed from the drive, the motor and media slow down and stop rotating. This removes the air cushion and allows the heads to land on the media.

Filters

NOTE
The filters are part of the HDA. Disassembly of the HDA to access the filters destroy the data stored on the media and the reliability of the drive.

The stepper motor, head carriage assembly, and spindle motor are all environmentally sealed in a casting. An air filtration system inside the sealed casting removes particles that would damage the heads and media.

The filtration system consists of a dual chamber filter. One chamber removes 0.3 micrometer particles from the air. The filter maintains a clean air environment inside the sealed HDA for the life of the drive and requires no maintenance.

The other chamber is a filtered vent which allows pressure equalization between the sealed HDA and the outside environment. During normal operation there is no measurable air flow between the HDA and the outside environment.

Figures 12-5 and 12-6 show the air flow paths of this system.

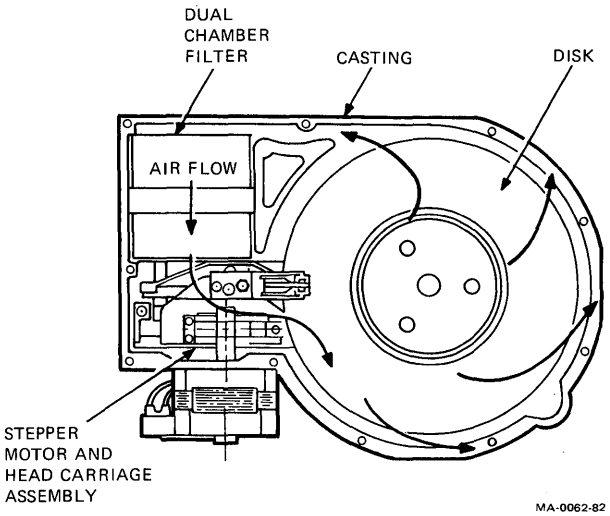
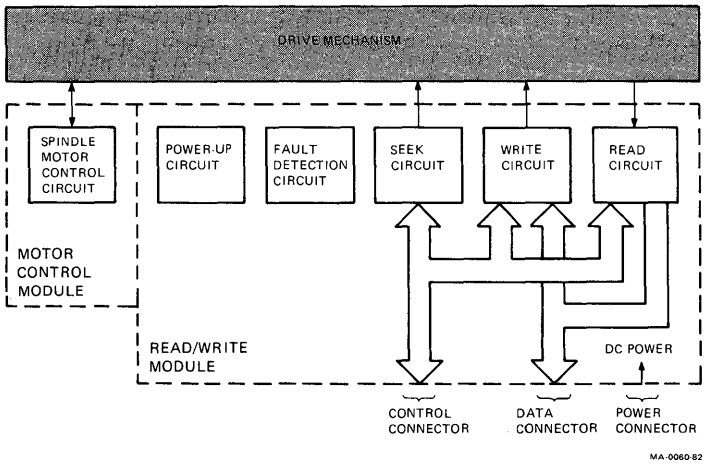


Figure 12-5 Air Flow Top View



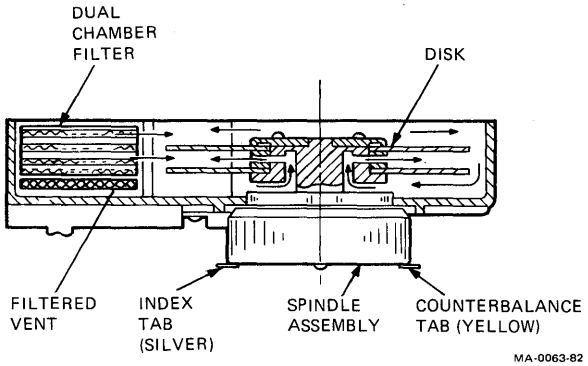
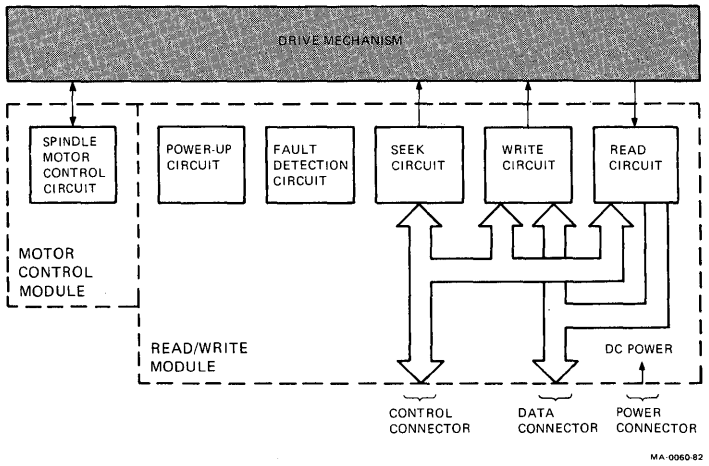


Figure 12-6 Air Flow Side View



12.3.1.2 Sensors and Hardware – The following paragraphs describe the sensors and hardware of the drive mechanism.

Index Sensor
The spindle motor hub has two tabs attached to it. One tab is a ferrous metal tab used by the index sensor; the other tab is nonferrous metal and is for counter balancing. The index sensor is a transistor which responds to magnetic field variations. This response is called a hall effect. The sensor is mounted on the HDA 0.030 inches away at its closest point from the ferrous metal tab on the spindle hub.

The ferrous tab distorts the magnetic field of the sensor. The sensor generates a pulse (INDEX SENSE) to the write circuits in the R/W module. For more information on this signal see Section 12.3.6.

Track Zero Sensor

NOTE
The track zero sensor position is set at the time of manufacture. Replacement or adjustment of this sensor alters the position of track zero.

The track zero sensor is an infrared light emitting diode, a photo sensitive transistor, and a light interrupting tab on the stepper motor shaft. When the tab interrupts the light from the diode to the photo sensitive transistor, the transistor turns off. This generates a signal (TRK 0 SENSE) for the R/W module. This occurs when the heads are located near track zero. For more information on this signal see Section 12.3.5.

Spindle Brake
A brake mounts on the HDA near the spindle hub. This brake minimizes head flutter when the spindle motor slows down after power is removed from the drive. Flutter is a condition where the heads bounce over the media. This occurs when the slower disk rotation creates an unstable air cushion.

This brake is a solenoid actuated brake pad. The brake is mounted on the HDA so that the pad is situated 0.010 inches from the spindle hub. When power is applied to the motor control module, the solenoid is activated and pulls the brake pad away from the spindle hub allowing the hub to spin freely.

When power is removed from the solenoid, the brake pad contacts the hub and slows it down. This allows the heads to land on the media quickly, extending the life of the media and the heads.

Spindle Ground Spring
The spindle ground spring provides a discharge path for static electricity which builds up on the spindle and the media. The spring bolts to the HDA allowing a carbon contact to touch a metal cone at the base of the spindle motor. This discharges static electricity from the HDA.

Drive Select Indicator
The drive select indicator on the front bezel of the drive lights if the controller has selected the RD50 disk drive. This indicator is controlled by a signal from the controller.

12.3.2 Spindle Motor Control Circuit Detailed Operations

The spindle motor control circuit is on the motor control module (Figure 12-7). The spindle motor control circuit performs the following functions.

- Provides maximum allowable current to the spindle motor when power is first applied. This rapidly brings the motor up-to-speed.
- Monitors the speed of the motor and adjusts the current driving the motor. This keeps the motor rotating at a constant speed.

These functions are performed in two stages. In the first stage, the HALL IN signal sets the current level required by the spindle motor. In the second stage, the HALL IN signal switches the current between the two spindle motor driver coils. This produces the magnetic fields required by the spindle motor.

The motor control module receives +12 Vdc power from a power supply. This power is routed directly to a connector for the brake and a +6.2 Vdc regulator. The regulator provides operating voltages to the module and a speed sensor circuit located in the spindle motor.

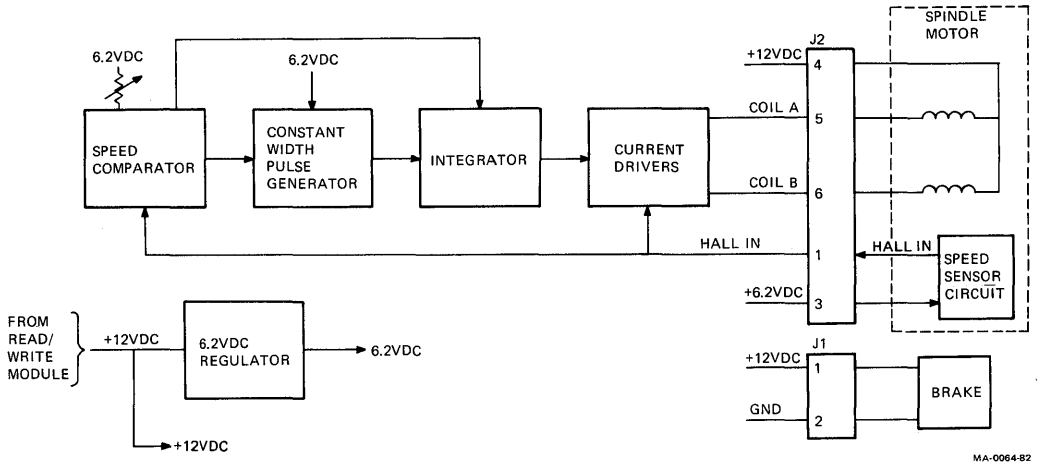
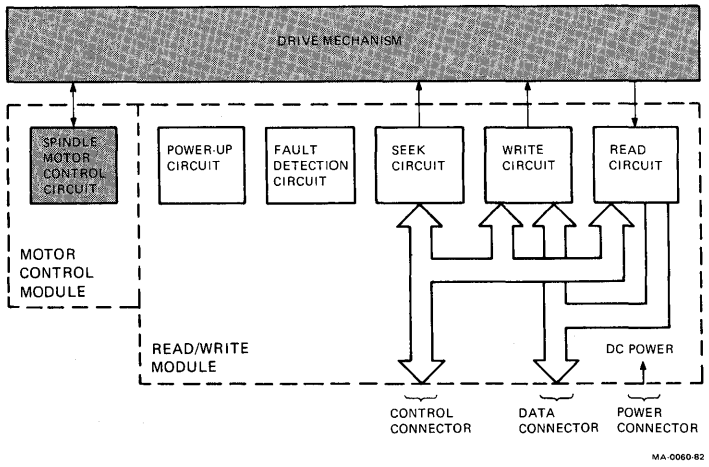


Figure 12-7 Spindle Motor Control Circuit Detail



12.3.2.1 Motor Current Control – Current coupled to the spindle motor is controlled by a speed comparator, constant pulse width generator, and an integrator. These three circuit segments set the current level for the current drivers and operate in two modes: start up and normal operation.

The speed comparator's output drives both the integrator and the constant width pulse generator. During start up the speed comparator controls the integrator, providing the maximum current to the current drivers. As the spindle speed increases to normal speed, the speed comparator minimizes its effect over the integrator and the constant width pulse generator controls the integrator.

The speed comparator receives the HALL IN signal from a speed sensor circuit in the spindle motor. This signal's frequency is two times that of the motor speed.

The comparator uses the falling edge of the HALL IN signal to discharge its capacitor. The charge rate of the capacitor is set at the factory. The combination of the frequency of discharge and the charge rate determines the width of a falling pulse from the comparator to the constant pulse width generator and integrator.

The constant pulse width generator uses the falling edge of the pulse from the speed comparator to generate a constant width falling pulse for the integrator. The average voltage level of these pulses represents the amount of current required by the motor to maintain a speed of 3600 rpm.

When the motor rotates slower than 3600 rpm the ratio of falling pulse widths to the rising pulse widths is greater than the established average. This causes the integrator to generate a higher average voltage. This voltage represents a higher current coupling by the current drivers causing the motor to speed up.

When the motor rotates faster than 3600 rpm, the ratio of falling pulse widths to rising pulse widths is less than the established average. This causes the integrator to generate a lower average voltage. This voltage represents a low current coupling by the current drivers causing the motor to slow down.

12.3.2.2 Spindle Motor Current Switching – The current drivers switch the current between the two coils of the motor and act as a current limiter. These drivers are controlled by the integrator and by the HALL IN signal from the motor.

The current drivers normally operate within their linear amplifying range except when power is first applied. The integrator output level saturates the drivers when power is first applied, providing the maximum current for the coils. This causes the motor to come up-to-speed quickly.

During normal operation the integrator output controls the level of current the drivers provide through the motor coils, while the HALL IN signal switches the drivers to provide current through coil A or coil B.

If the motor is obstructed from rotating when the power is on, the drivers are permanently damaged. This prevents overloading the coils and damaging the spindle motor in the HDA.

12.3.3 Power-up Circuit Detailed Operations

The power-up circuits provide the RD50 drive with a power-up sequence. This sequence begins when either of the following conditions occur:

1. Power is first applied to the drive.
2. Power goes out of tolerance then back into tolerance.

The power-up sequence initializes the drive in the following ways.

- Generates a 64ms POWER-ON RESET signal after the +5 Vdc stablizes.
- Counts 512 index pulses then generates an UP TO SPEED signal.
- Generates recalibration signals for the seek circuit until the heads are located over track zero.
- Generates a READY signal when the heads are located at track zero.

Figure 12-8 shows the power-up circuit in detail. Figure 12-9 shows a timing diagram and the relationship between drive control signals and signals generated by the power-up circuit.

12.3.3.1 Reset Signal Generation – When power is first turned on, a POWER-UP RESET signal is asserted. This signal stays asserted for 64ms after the +5 Vdc stabilizes and resets the power-up, fault detection, and seek circuits.

12.3.3.2 Up To Speed Signal Generation – An UP TO SPEED signal is controlled by an up-to-speed counter. This counter is reset when the POWER-UP RESET signal is asserted or the fault detection circuit asserts the DC UNSAFE signal.

This counter counts 512 index pulses from the write circuit after the power is stabilized, then asserts an UP TO SPEED signal. This signal enables the seek circuits and the recal or ready logic in the power-up circuit.

12.3.3.3 Recalibration Signal Generation – The power-up circuit controls two signals which recalibrate the RD50 drive to track zero, a FORCE OUT and a RECAL STEP signal. Both of these signals control the seek circuit to move the heads to track zero. For operation of the seek circuit see Section 12.3.5.

A track zero flip-flop is reset by a POWER-UP RESET or a DC UNSAFE signal from the fault detection circuit. Resetting the flip-flop unasserts TRK00 FOUND signal and asserts the FORCE OUT signal. The index pulse clocks the flip-flop with the state of the TRK00 signal. If the TRK00 signal is not asserted, the FORCE OUT signal remains asserted. If the TRK00 signal is asserted the TRK00 FOUND signal is asserted and the FORCE OUT signal is unasserted.

The recal or ready logic is enabled when the UP TO SPEED signal is asserted. If the TRK00 FOUND signal is unasserted the INDEX signal generates RECAL STEP signals for the seek circuit. If the TRK00 found signal is asserted the RECAL STEP signal is inhibited.

12.3.3.4 Ready Signal Generation – The recalibration or ready logic generates a ready signal for the fault detection circuit and the controller. When the up-to-speed counter asserts the UP TO SPEED signal and the track zero flip-flop asserts the TRK00 found signal, the READY signal is asserted. The signal indicates that the drive is initialized and ready to operate.

The logic state of the READY signal passes to the controller when the drive select (DSELECT) signal is asserted. This signal asserts when the drive select (DRSEL) signal from the controller is asserted or the radial jumper R is in place (Figure 12-9). For normal settings of these jumpers see Section 12.5.3.

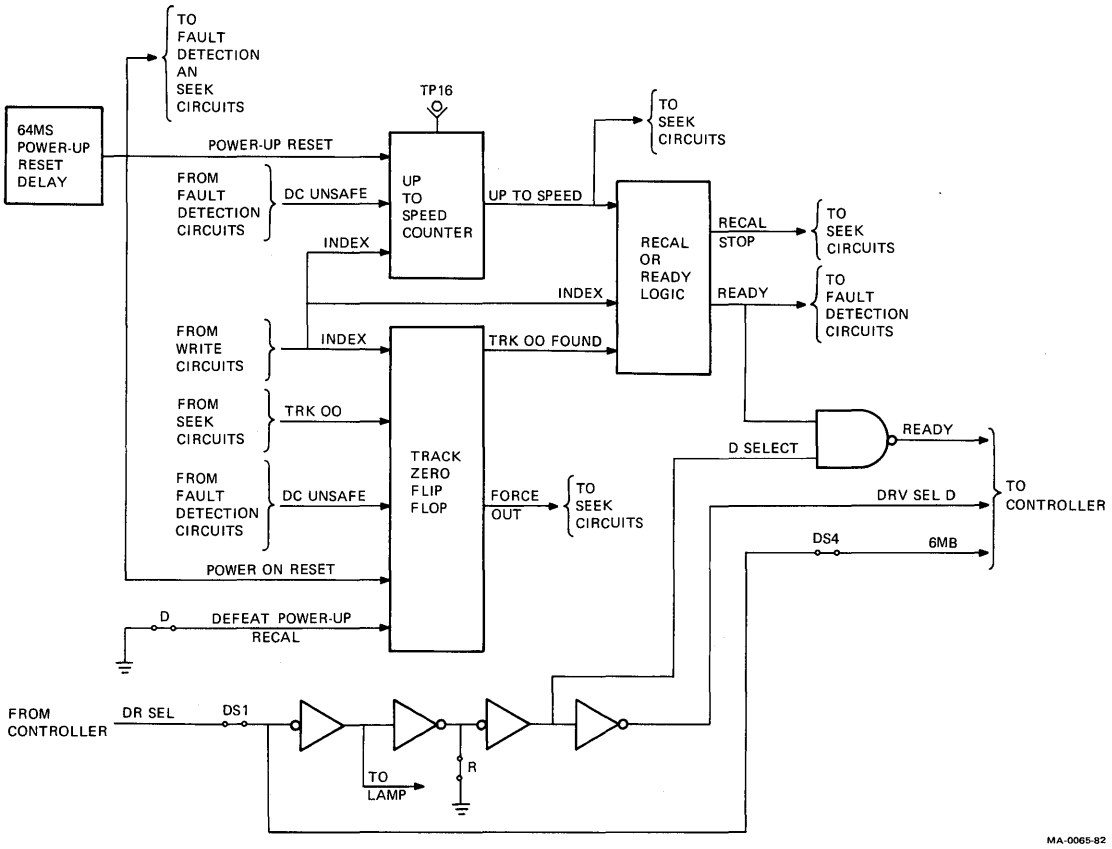
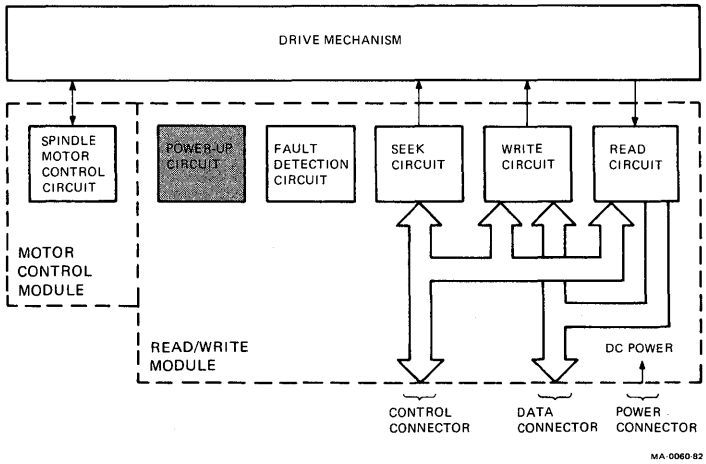


Figure 12-8 Power-up Circuit Detail



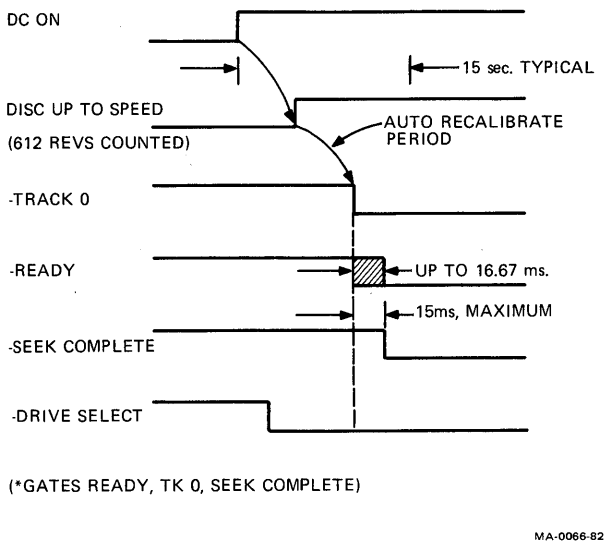


Figure 12-9 Power-up Sequence Timing

12.3.3.5 Recalibration Signal Generation Deselection – Generating recalibration signals during a power-up sequence can be prevented. A defeat power-up recal jumper (see Section 12.5.3 for normal settings) must be in place to preset the track zero flip-flop. The remaining sequences, power-up reset and up-to-speed, become the power-up sequence.

12.3.4 Fault Detection Circuits Detailed Operation

The fault detection circuit monitors the R/W module, protecting the recorded data and R/W heads during circuit malfunctions, illegal operations, or commands. If faults are detected, the fault detection circuits disable or reset circuits on the R/W module. If no faults are detected, the fault circuit generates an enable signal for the write circuit. Figure 12-10 shows the fault detection circuit in detail.

The fault circuit monitors the R/W module for the following faults.

- Head selection malfunction
- Unsafe voltage levels
- Unsafe write circuit

12.3.4.1 Head Selection Malfunction Detection – The head select unsafe detector receives two signals: HD BUSS from the read and write circuits and WR GATE from the controller. This detector monitors these signals for the following faults.

- No head is selected.
- More than one head is selected.
- A head is selected for a read operation when a write operation is to be performed.
- A head is selected for a write operation when a read operation is to be performed.

If one of these faults exists, a HD UNSAFE signal is asserted inhibiting the write circuit from operating. If none of these faults exist, the HD UNSAFE signal is unasserted. This signal is used by the write circuit and the write status logic in the fault detection circuit.

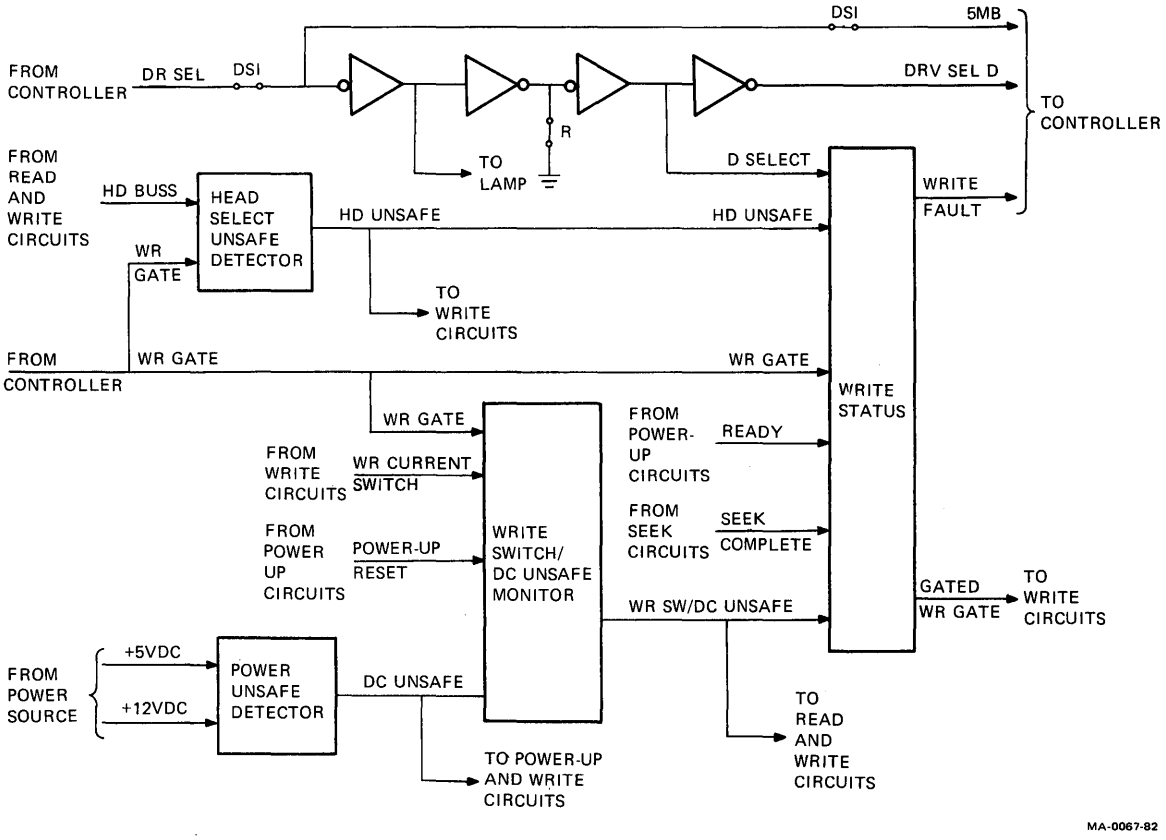
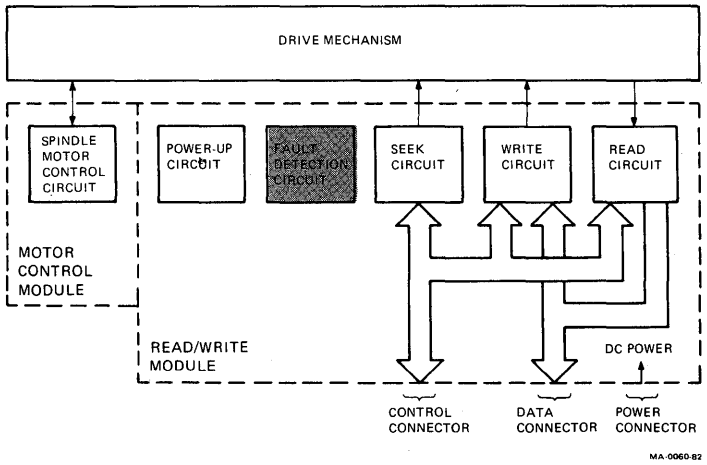


Figure 12-10 Fault Detection Circuit Detail



12.3.4.2 Power Unsafe Detection – A power unsafe detector monitors the levels of the +5 and +12 Vdc. If the level of either voltage is out of tolerance, the detector asserts a DC UNSAFE signal for the power-up, write, and seek circuits.

The following are power unsafe.

- If the +5 Vdc falls below 4.3 Vdc
- If the +12 Vdc falls below 9.5 Vdc

12.3.4.3 Write Circuit Unsafe Detection – The functions of the write circuit are monitored by the write switch/dc unsafe monitor. This monitor asserts a write current switch fault or power unsafe signal (WR SW / DC UNSAFE) to disable the write and read circuits.

The WR SW/ DC UNSAFE signal is asserted if any of the following conditions exist.

- The write function is selected but no write current exists.
- A write current exists but the write function is not selected.
- The DC power is unsafe (see Section 12.3.4.2).
- The POWER-UP RESET signal is asserted (see Section 12.3.3.1).

12.3.4.4 Write Status Detection – A write status monitor generates two signals: a WRITE FAULT signal for the controller and a GATED WR GATE for the write circuit. An asserted WRITE FAULT signal indicates a fault exists in the RD50 drive. An asserted GATED WR GATE signal indicates that the proper conditions exist for performing a write function.

The state of the write fault signal is sent to the controller when the controller selects the RD50 drive by asserting DRSEL or by installing jumper R (see Section 12.5.3 for normal settings).

The write fault signal is asserted when **any** of the following conditions exist.

- A head unsafe condition exists (see Section 12.3.4.1).
- The dc power is unsafe (see Section 12.3.4.2).
- The write circuit is unstable (see Section 12.3.4.3).

A GATED WR GATE signal is asserted when **all** of the following conditions exist.

- No faults are detected.
- The power-up circuit asserts READY (see Section 12.3.3.4).
- The seek circuit asserts SEEK COMPLETE (see Section 12.3.5.5).

12.3.5 Seek Circuit Detailed Operation

The seek circuit generates control signals for a stepper motor to position the R/W heads over any one of the 153 tracks. This circuit is controlled by the controller or by the power-up circuit during a power-up sequence. Figure 12-11 shows the seek circuit in detail.

The seek circuits are inhibited from operating during the power-up sequence by the power-up circuit (POWER-UP RESET asserted) or during a dc unsafe condition by the fault detection circuit (DC UNSAFE asserted). Inhibiting the seek circuits at these times protects R/W heads from damage.

To generate stepper motor control signals, the seek circuit performs the following.

- Selects the direction to move the heads.
- Receives step pulses.
- Converts step pulse and direction signals to stepper motor control signals.
- Monitors for a track zero head location.
- Indicates when the seek circuit is operating.

12.3.5.1 Head Direction Selection – The controller controls which direction the heads are to move, towards the center of the drive or towards track zero. When the controller asserts the DIRECTION IN signal, the heads move towards the center of the disk. When the controller unasserts DIRECTION IN signal, the heads move towards track zero.

During a power-up sequence the power-up circuit asserts a FORCE OUT signal (see Section 12.3.3.3). This signal selects a head movement towards track zero.

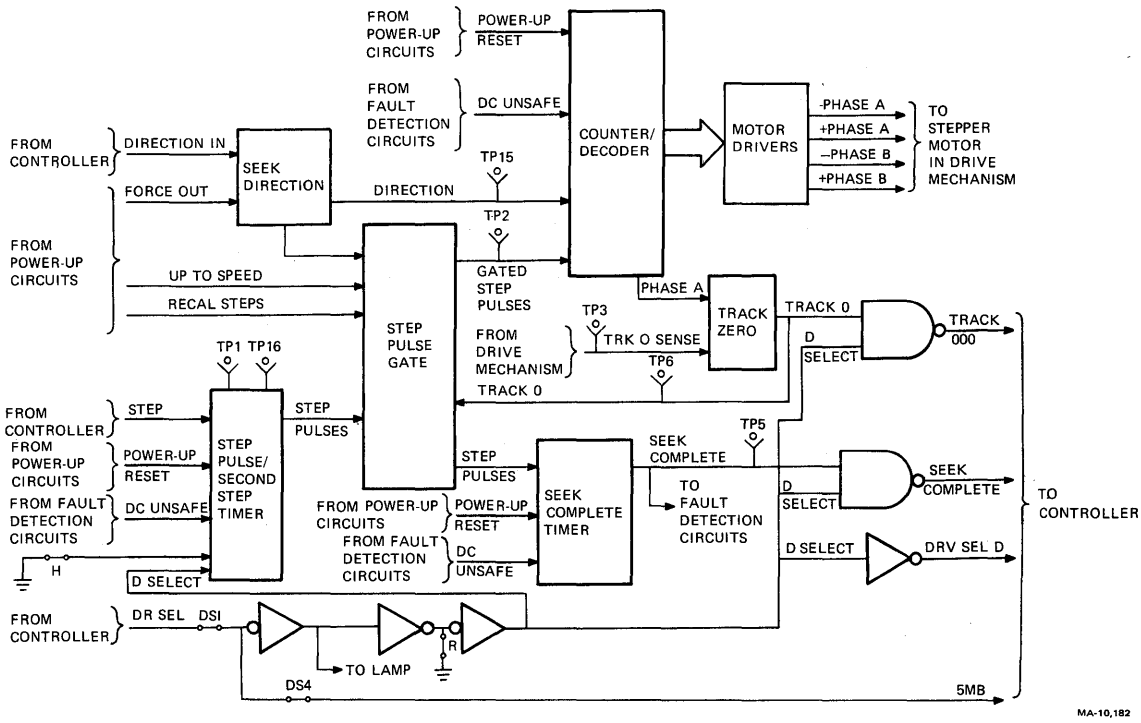


Figure 12-11 Seek Circuit Detail

12.3.5.2 Step Pulse Selection – Step pulses are normally generated for the counter/decoder by signals the seek circuit receives from the controller. The controller sends step pulses and a DRSEL (DSELECT) signal to the step pulse/second step one shot. This one shot operates in both double step or single step modes.

When jumper H is installed, the step pulse/second step one shot operates in the single step mode (see Section 12.5.3 for normal settings). It generates one pulse for every falling transistion it receives from the controller (Figure 12-12).

When jumper H is removed, the step pulse/second step one shot operates in the double step mode (see Section 12.5.3 for normal settings). It generates two 2 μs pulses for every falling transition it receives from the controller. The second pulse is 2.8ms after the first pulse. Refer to Figure 12-12 for timing relationships.

The step pulses then pass through a step pulse gate. This gate passes these pulses from the step pulse/second step one shot or the power-up circuit (RECAL STEP), as gated step pulses. This occurs when the following conditions exist.

- The UP TO SPEED signal from the power-up circuit is asserted.
- A head movement direction towards the center of the disk is selected when the heads are at track zero.

12.3.5.3 Step Pulse and Direction Signal Conversion – A counter/decoder and the motor drivers convert the direction and gated step pulses to stepper motor control signals. The DIRECTION signal causes the counter/decoder to count up or count down. The gated step pulses clock the counter in the counter/decoder.

The output of the counter is decoded to generate signals which select the motor drivers. The motor drivers then generate the motor control signals, –PHASE A, +PHASE A, –PHASE B, AND +PHASE B, for the stepper motor.

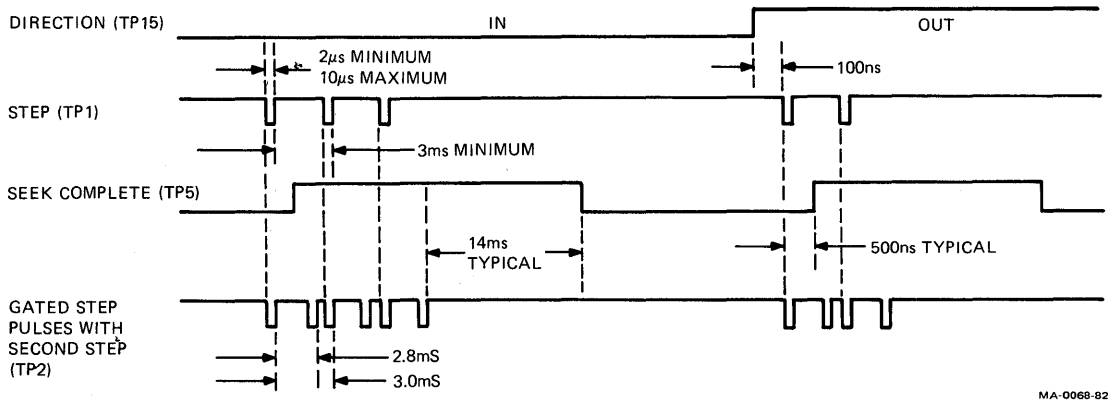


Figure 12-12 Seek Circuit Timing

12.3.5.4 Track Zero Monitoring – The seek circuits monitor for a track zero head location. When the heads are at track zero, a TRACK 0 signal is asserted. This signal is used by the power-up circuit, the step pulse gate, and the controller (TRACK000). When the drive is selected, DSELECT is asserted.

The TRACK 0 signal is generated when the sensor on the drive mechanism asserts a TRK 0 SENSE signal and the counter/decoder indicates a PHASE A stepper motor position. Refer to Section 12.3.1.2 for further information on the TRK 0 SENSE signal.

12.3.5.5 Seek Complete Indicator – A seek complete timer monitors the step pulses. This timer asserts a SEEK COMPLETE signal when the seek circuit does not receive a step pulse for 14ms or more (Figure 12-12). The SEEK COMPLETE signal is used by the fault detection circuit and the controller.

12.3.6 Write Circuit Detailed Description

The write circuit converts MFM encoded data from the controller to current pulses for the head coils. This creates a high flux magnetic field which orients the oxide coating on the media to form magnetic domains.

Figure 12-13 shows the write circuit detail. Timing relationships between data and command signals (Figure 12-14) are described in the following paragraphs.

A differental receiver, when enabled by the controller (DSELECT asserted), passes encoded data (MFM WRITE DATA) to a flip-flop. This divides the data by two, creating a rectangular wave which represents flux transitions. This signal drives a differential write switch (Figure 12-13).

The differential write switch, when provided with WRITE CURRENT, controls currents that drive a center tapped R/W coil. The current reverses at each edge of the rectangular wave. Reversing the current creates alternating magnetic fields in the coils and magnetic domains on the media.

A write current regulator provides WRITE CURRENT to the differential write switch. The regulator is also enabled and disabled by the fault detection and power-up circuits.

The write current regulator provides two levels of write current. These levels are selectable by the reduce write current (RWC) controller signal. One level of write current is used for recording data on tracks 0 through 127, RWC unasserted. The other current level is used for tracks 128 through 152, RWC asserted.

When the differential write switch generates the write currents, a R/W head select decoder asserts one of four head select signals for one of the four R/W heads. Each head select connects to the center tap of a R/W coil. The coils are selected for a write function by the controller (HD SEL 0, HD SEL 1, and WR GATE). The decoder is disabled for operation by the fault detection circuits (WR SW/DC UNSAFE asserted). For more information see Section 12.3.4.3.

A one shot in the write circuit converts the INDEX SENSE signal from the drive mechanism to a 1 ms pulse (Figure 12-15). This pulse is a reference signal which indicates the start of the track. It is used by the power-up circuits (Section 12.3.3) and the controller.

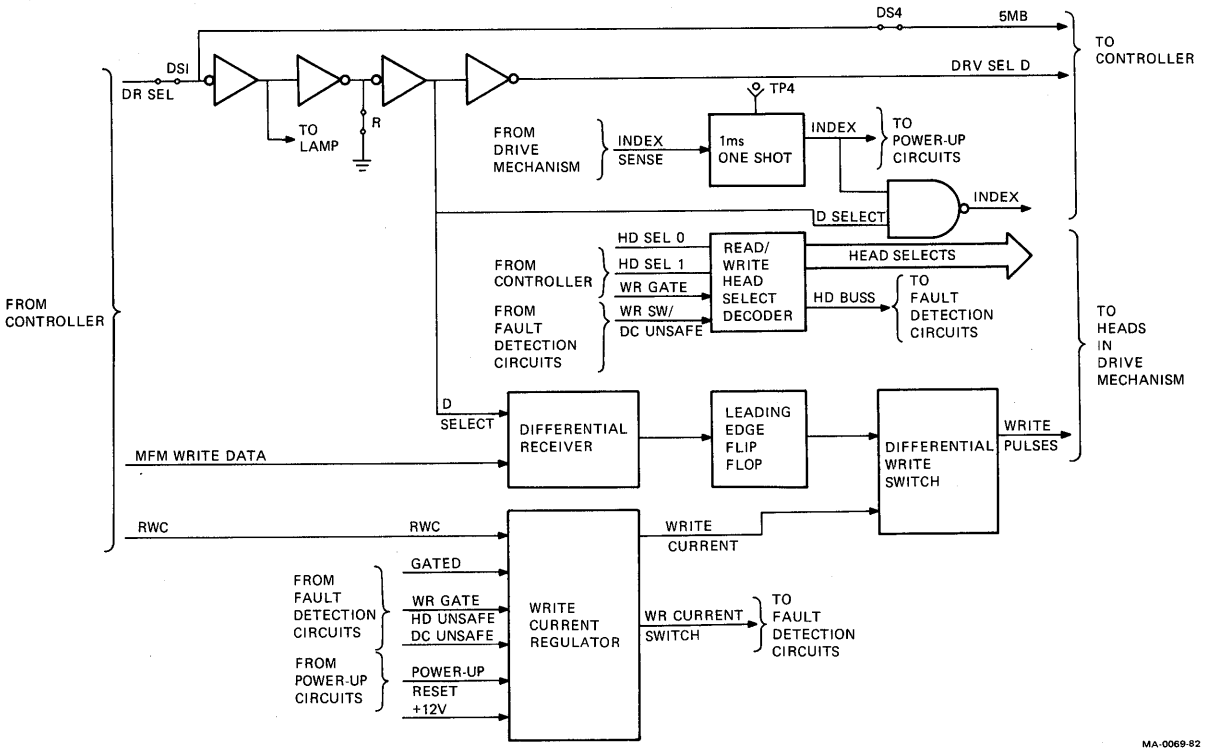
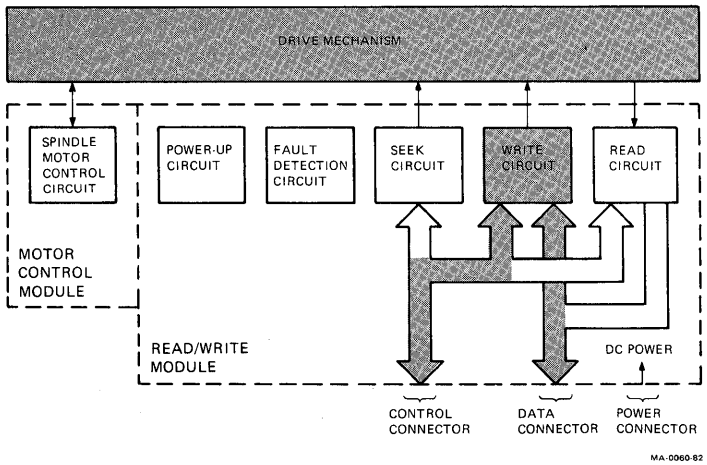


Figure 12-13 Write Circuit Detail



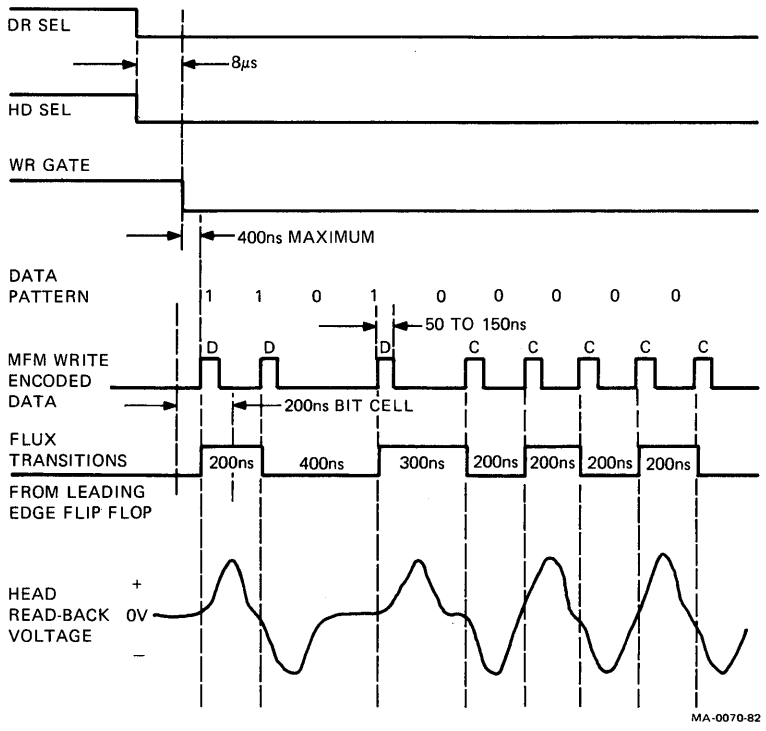


Figure 12-14 Write Data Timing

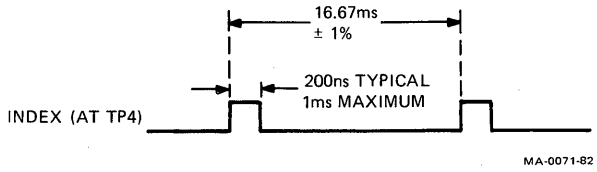


Figure 12-15 Index Signal Timing

12.3.7 Read Circuit Detailed Description

The read circuit converts flux transitions sensed by the R/W heads to MFM data pulses. The flux transitions reside on the media from previous write functions.

Figure 12-16 shows the read circuit in detail. Timing relationships between data and command signals (Figure 12-17) are described in the following paragraphs.

For the amplifier/filter to receive a proper signal from the heads, the R/W head select decoder asserts one of four head select signals for one of the four R/W heads. Each head select connects to the center tap of a R/W coil. The coils are selected for a read function by the controller (HD SEL 0, HD SEL 1, and WR GATE). The fault detection circuits disable the decoder when WR SW/DC UNSAFE is asserted. For more information see Section 12.3.4.3.

When the head is selected, the amplifier/filter receives a differential read signal from the heads. The read signal is a low voltage analog signal which represents the flux reversals recorded on the media.

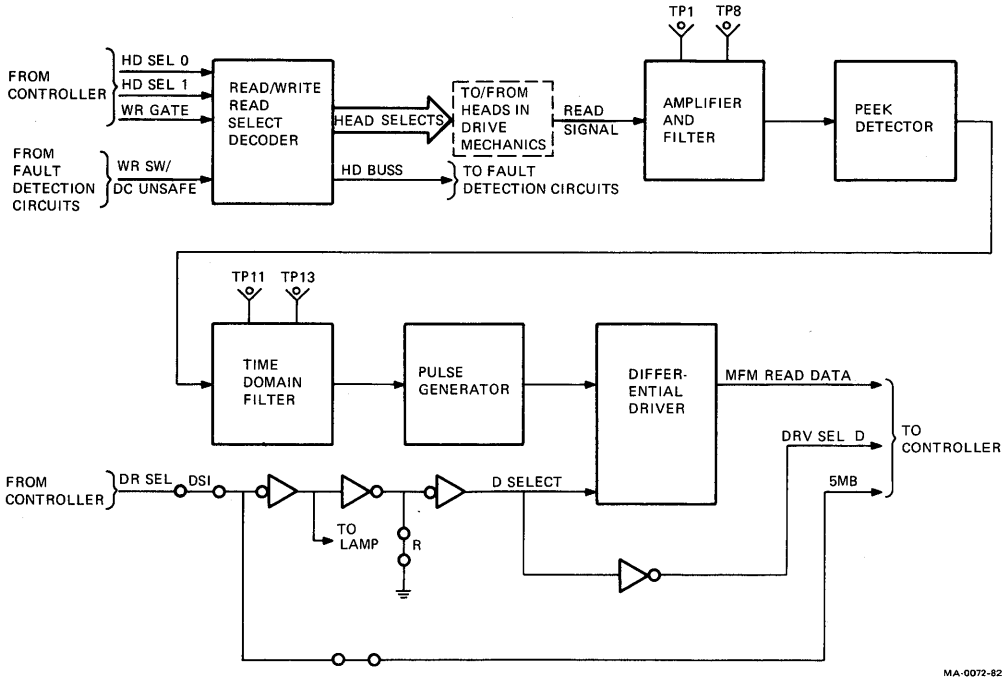
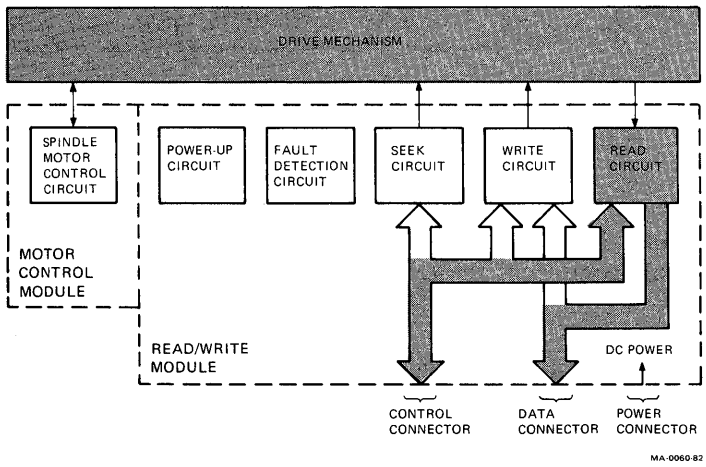


Figure 12-16 Read Circuit Detail



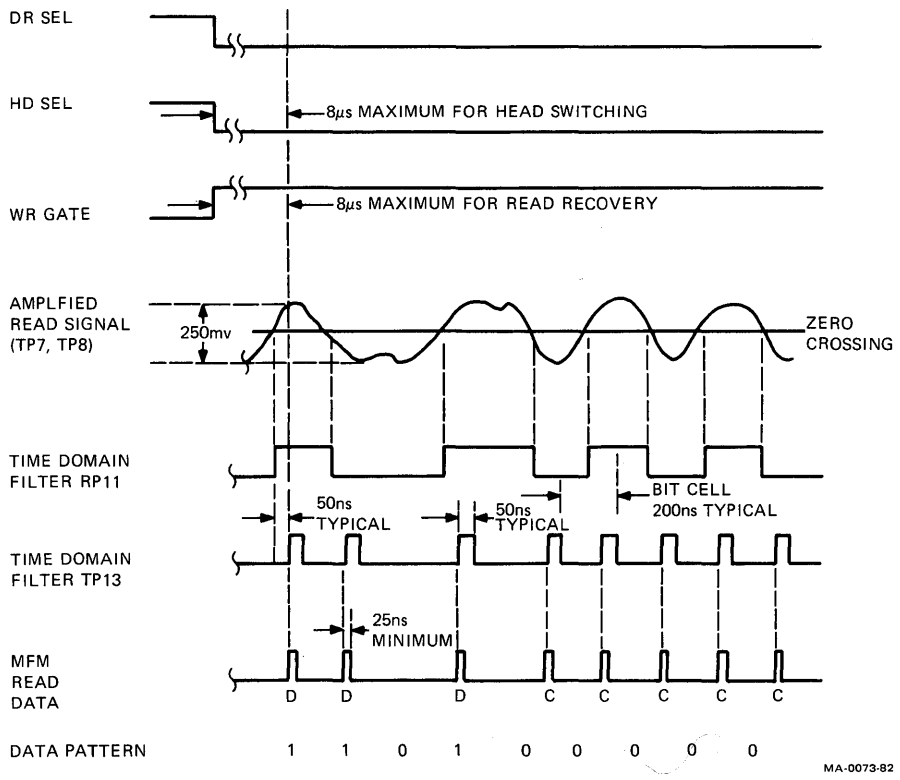


Figure 12-17 Read Data Timing

The signal is amplified 400 times and then passed through a 3.1 MHz low pass filter. It is observable at test points TP7 and TP8 (Figure 12-17). The amplification allows the rest of the read chain to convert the analog data signal to a digital data signal.

The amplifier/filter passes the amplified read signal to a peak detector. The peak detector converts the differential read data signal to rectangular wave signals. Each transition of the signal represents the zero crossings of the analog signal, the recorded flux changes. The peek detector passes this digital signal to a time domain filter.

The time domain filter stops noise mixed with the read data from passing to the pulse generator. This is done by comparing the digital signal to itself after a delay of 50ns. Both signals are observable at test points TP11 and TP13 (Figure 12-17).

Each transition of the filtered read data is then converted to a pulse by the pulse generator and sent to the differential driver. When the controller enables the driver by asserting DRSEL, differential MFM READ DATA is passed to the controller.

12.4 CONNECTOR DESCRIPTIONS

This section defines all signals that pass between the modules of the RD50 drive. Signal definitions are grouped by common connectors.

12.4.1 Connector J1, R/W Module

This section describes the control and status signals passed between the R/W module of the RD50 drive and the RD50 controller. Figure 12-18 shows the signal direction between the drive and the controller. Figure 12-19 shows the connector location.

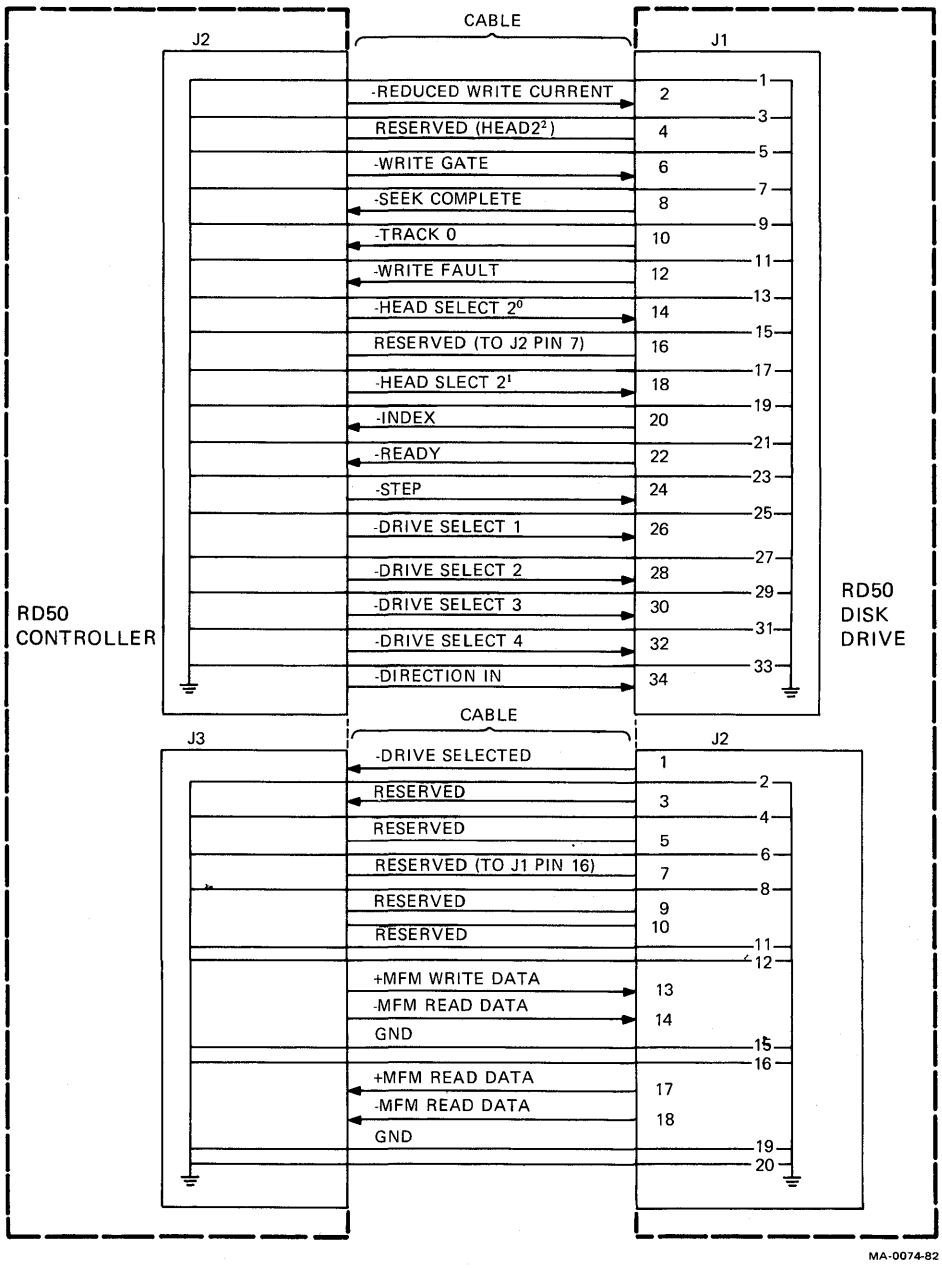


Figure 12-18 RD50 Interface Signal Connections

Table 12-1 lists the pin functions of the J1 connector. The odd-numbered pins of the connector are grounded and are not discussed. The signal mnemonic column describes the asserted state of the signal. An L after the mnemonic denotes an asserted low state. An H after the signal name denotes an asserted high state.

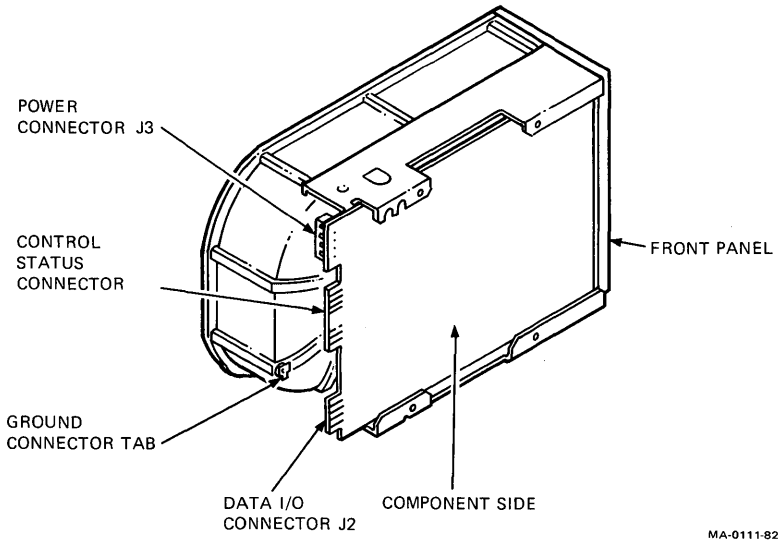


Figure 12-19 I/O Connector Locations

Table 12-1 Control/Status Connector J1

Pin	Signal Name	Signal Mnemonic
2	Reduced write current	RWC L
4	Reserved	
6	Write gate	WR GATE L
8	Seek complete	SEEK COMPLETE L
10	Track 000	TK000 L
12	Write fault	WRITE FAULT L
14	Head select 2^0	HD SEL 0 L
16	Unspecified	
18	Head select 2^1	HD SEL 1 L
20	Index	INDEX L
22	Ready	READY L
24	Step	STEP PULSE L
26	Drive select 1	DR SEL L
28	Reserved	
30	Reserved	
32	Drive capacity	5MB L
34	Direction in	DIRECTION IN L

12.4.1.1 REDUCED WRITE CURRENT (Pin 2) – This signal is asserted by the controller. When this signal and WRITE GATE are asserted, the RD50 drive uses a lower value of write current for writing on the disk. When this signal is unasserted, the drive uses a higher value of write current.

Tracks 128 to 152 require a lower write current than do tracks 0 to 127. Since the heads fly lower at the inner tracks, a lower write current ensures generating the proper magnetic fields. Using a high write current at inner tracks destroys data in the adjacent tracks.

12.4.1.2 WRITE GATE (Pin 6) – The controller asserts this signal, enabling the write drivers when SEEK COMPLETE is asserted.

12.4.1.3 SEEK COMPLETE (Pin 8) – The drive asserts this signal to the controller. This signal is asserted when the R/W module seek circuit does not receive a step pulse in 14ms and the R/W heads have settled. If this signal is unasserted, writing is inhibited. SEEK COMPLETE is unasserted during any seek operation.

12.4.1.4 TRACK 000 (Pin 10) – The drive asserts this signal to the controller. When the signal is asserted, the R/W heads are positioned at the outermost track (track zero).

12.4.1.5 WRITE FAULT (Pin 12) – The drive asserts this signal to the controller. When the signal is asserted, one of the following conditions is detected and writing or seeking is inhibited. The signal remains asserted until the condition is corrected.

- The heads receive current when WRITE GATE is unasserted.
- DRIVE SELECT and WRITE GATE are asserted, but the heads do not receive current.
- There are multiple heads selected, no head selected, or an improperly selected head.
- The dc voltages are out of tolerance.

12.4.1.6 HEAD SELECT (Pin 14 and 18) – The controller asserts the two signals, HD SEL 0 and HD SEL 1. They are decoded to select one of four disk drive heads.

12.4.1.7 INDEX (Pin 20) – The drive asserts this signal to the controller. The INDEX signal is an asserted pulse that occurs once per revolution of the disks. The leading edge of the pulse indicates the beginning of each track (sector 0).

12.4.1.8 READY (Pin 22) – The drive asserts this signal to the controller. When this signal is asserted, the drive is ready to read, write or seek. If SEEK COMPLETE and READY are asserted, the I/O signals are valid. When READY is unasserted, all writing and seeking actions are inhibited.

12.4.1.9 STEP (Pin 24) – The controller asserts this signal to control the R/W head movement in the direction defined by the DIRECTION IN signal.

12.4.1.10 DRIVE SELECT (Pin 26) – The controller asserts this signal. It selects the drive and the indicator on the bezel. This signal becomes unasserted if one of the following occurs.

- The host resets the controller.
- A power fault occurrs in the host processor.

12.4.1.11 DRIVE CAPACITY (Pin 32) – The drive asserts this signal to the controller. This signal is generated by the DRIVE SELECT signal on the 5 megabyte disk drive. This signal is always unasserted on the 10 megabytes disk drive.

12.4.1.12 DIRECTION IN (Pin 34) – The controller asserts this signal. It defines the direction of the R/W head movement when a step pulse is issued. The asserted state of DIRECTION IN selects head movement towards the center of the disk. An unasserted signal selects head movement towards track zero.

12.4.2 Connector J2, R/W Module

This section describes the data signals passed between the R/W module of the RD50 hard disk drive and the RD50 controller. Figure 12-18 shows the signal direction between the drive and the controller. Figure 12-19 shows the connector location.

Table 12-2 lists the pin functions of the RD50 drive J2 connector.

The signal mnemonic column describes the asserted state of the signal. An L after the mnemonic denotes an asserted low state (logic zero). An H after the signal name denotes an asserted high state (logic high).

12.4.2.1 DRIVE SELECTED (Pin 1) – The drive asserts this signal to the controller when the drive is selected.

12.4.2.2 MFM WRITE DATA (Pins 13 and 14) – The controller asserts this differential pair and defines the transitions to be written on the disk surface. If WRITE GATE is asserted, the transition of +MFM WRITE DATA line going more positive than the –MFM WRITE DATA causes a flux reversal on the disk. While the controller reads data from the drive, this signal is unasserted (+MFM WRITE DATA more negative than –MFM WRITE DATA).

12.4.2.3 MFM READ DATA (Pins 17 and 18) – The drive asserts this differential pair to define recovered read data from the selected head. The transition of the +MFM READ DATA line going more positive than the –MFM READ DATA line represents a flux reversal from the selected head.

Table 12-2 Data I/O Connector J2

Pin	Signal Name	Signal Mnemonic
1	Drive selected	DRV SELD L
2	Ground	
3	Reserved	
4	Ground	
5	Spare	
6	Ground	
7	Reserved	
8	Ground	
9	Spare	
10	Spare	
11	Ground	
12	Ground	
13	+MFM write data	+MFM WRITE DATA H
14	–MFM write data	–MFM WRITE DATA H
15	Ground	
16	Ground	
17	+MFM read data	+MFM READ DATA H
18	–MFM read data	–MFM READ DATA H
19	Ground	
20	Ground	

12.4.3 Connector J3, R/W Module

Connector J3 on the R/W module receives power for the entire RD50 drive. Section 12.6.5 provides these power requirements. Table 12-3 lists the pin functions of the RD50 drive J3 connector. Figure 12-19 shows the connector location.

12.4.4 Connector J4, R/W Module

Connector J4 on the R/W module passes power to the motor control module of the RD50 drive. Table 12-4 describes the connector pin functions. Figure 12-20 shows the location of the connector.

12.4.5 Connector J5, R/W Module

Connector J5 passes read, write, and head select signals between the R/W module and the HDA. Table 12-5 describes the connector pin functions. Figure 12-20 shows the location of the connector.

12.4.6 Connector J6, R/W Module

Connector J6 passes signals between the R/W module, the index sensor and front bezel indicator. Table 12-6 describes the pin functions of the connector. Figure 12-20 shows the location of the connector.

12.4.7 Connector J7, R/W Module

Connector J7 on the R/W module passes control signals to the stepper motor. Table 12-7 describes the pin functions of the connector. Figure 12-20 shows the location of the connector.

12.4.8 Connector J8, R/W Module

Connector J8 passes signals between the R/W module and the track zero sensor. Table 12-8 describes the pin functions of the connector. Figure 12-20 shows the location of the connector.

Table 12-3 Power Connector J3

Pin	Mnemonic	Function
1	+12 Vdc	Plus 12 Vdc
2	+12 V Return	Ground
3	+5 V Return	Ground
4	+5 Vdc	Plus 5 Vdc

Table 12-4 Motor Control Module Power Connector J4

Pin	Mnemonic	Function
1	+12 Vdc	Plus +12 Vdc
2	+12 V Return	Ground

Table 12-5 HDA Connector J5

Pin	Mnemonic	Function
1	+HEAD 0	+Head zero read and write data
2	HEAD SEL 0	Selects head zero
3	−HEAD 0	−Head zero read and write data
4	GND	Ground
5	+HEAD 1	+Head one read and write data
6	HEAD SEL 1	Selects head one
7	−HEAD 1	−Head one read and write data
8	GND	Ground
9	+HEAD 2	+Head two read and write data
10	HEAD SEL 2	Selects head two
11	−HEAD 2	−Head two read and write data
12	GND	Ground
13	+HEAD 3	+Head three read and write data
14	HEAD SEL 3	Selects head three
15	−HEAD 3	−Head three read and write data
16	GND	Ground

Table 12-6 Index and LED Connector J6

Pin	Mnemonic	Function
1	+ACTIVITY LED	+5 Vdc power source for indicator
2	−ACTIVITY LED	Indicator ground
3	GND	Spindle ground
4	INDEX SENSE	Index signal from sensor
5	+5VDC	Power for index sensor

Table 12-7 Stepper Motor Connector J7

Pin	Mnemonic	Function
1	−Phase B	Step motor control
2	+Phase B	Step motor control
3	GND	Ground
4	−Phase A	Step motor control
5	+Phase A	Step motor control

Table 12-8 Track Zero Sensor Connector J8

Pin	Mnemonic	Function
1	GND	Ground
2	TRK 00 SENSE	Track zero sensed
3	+5VDC	Track zero sensor power source
4	GND	Ground
5		Not used

12.4.9 Connector J1, Motor Control Module

Connector J1 on the motor control module passes power to the brake assembly. When power is applied the brake assembly, the brake releases the spindle hub. Table 12-9 describes the pin functions of the connector. Figure 12-20 shows the location of the connector.

12.4.10 Connector J2, Motor Control Module

Connector J2 on the motor control module passes controlled power signals to the spindle motor. Table 12-10 describes the pin functions of the connector. Figure 12-20 shows the location of the connector.

12.5 MAINTENANCE PROCEDURES

This section describes the the field serviceable portion of the RD50 drive. If field maintenance or repair is required, certain restrictions apply.

The environmentally sealed head and disk assembly (HDA) must not be opened. If the HDA is tampered with, the warranty does not hold for the drive. Any special tools or additional restrictions are covered in the appropriate sections.

12.5.1 Preventive Maintenance

The RD50 drive does not require preventive maintenance.

12.5.2 Test Point Locations

Figure 12-21 shows the locations of all test points on the R/W module described in Section 12.2. These test points are not accessable in the field and should not be touched by a field technician.

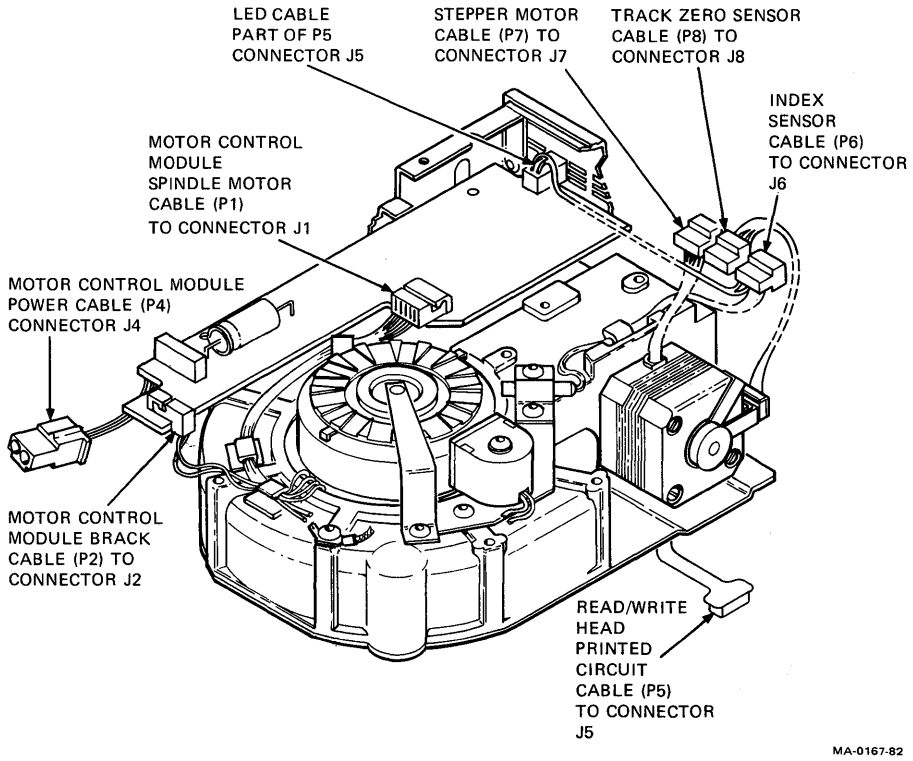


Figure 12-20 Internal Connection Locations

Table 12-9 Spindle Brake Connector J1

Pin	Mnemonic	Function
1	+12VDC	Brake release power source
2	GND	Ground

Table 12-10 Spindle Motor Connector J2

Pin	Mnemonic	Function
1	HALL IN	Sensed motor speed
2	GND	Ground
3	+6VDC	Motor speed sensor power
4	+12VDC	Motor power source
5	COIL A	Motor speed control
6	COIL B	Motor speed control

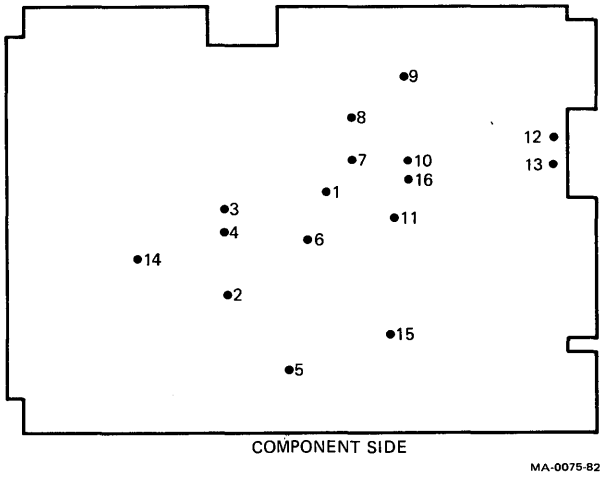


Figure 12-21 R/W Module Test Point Locations

12.5.3 Jumper/Dip Switch Settings

The RD50 drive contains a set of jumper or dip switches to select options described in Section 12.3. If the drive contains a 14-pin chip with jumpers, all jumpers are in place. If the drive contains a 14-pin dip switch, all settings are set to the ON position. The chip is located in pins 1 through 7 and 9 through 15 of the 16-pin socket. No jumper is between pins 8 and 16 of the 16-pin socket.

These settings indicate the drive is set to operate in the following ways.

- When power is first applied, the drive performs a recalibration to zero.
- The seek circuit causes the stepper motor to move two steps for every step pulse it receives from the controller. This occurs if the pulses are 2.8ms or more apart.
- The controller selects the drive for operation.

12.5.4 Removals and Adjustments

NOTE

Special clean room facilities and tools must be used for removal of any assembly not covered in this section.

Tools Required:

5/64 inch hex driver
Phillips head screw driver

Perform the following procedure.

1. Remove the four phillips screws holding the skid plate to the RD50 drive frame (Figure 12-22).
2. Remove the four hex head screws holding the R/W module to the RD50 drive frame.
3. Disconnect J1 through J8, noting their positions. Figure 12-21 shows the connector locations.
4. Slide the R/W module towards the rear of the drive and remove it.
5. To reinstall, reverse the above procedure.

NOTE

Do not flex the printed circuit cable when removing J5.

12.6 SPECIFICATIONS

The following paragraphs provide the specifications for the RD50 disk drive.

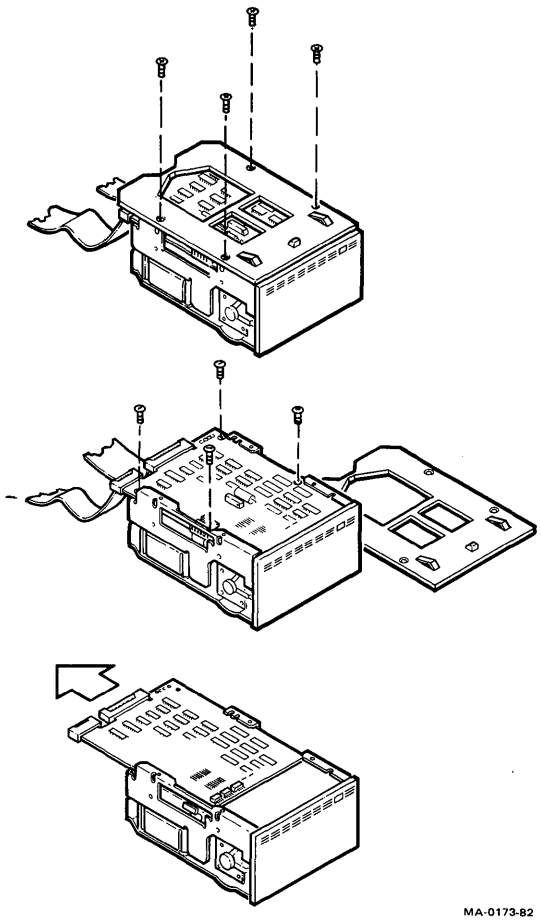


Figure 12-22 Assembly and Disassembly

12.6.1 Performance Specifications

Formatted Data Capacity

Per drive	5.0 megabytes
Per surface	1.25 megabytes
Per track	8192 bytes
Sectors per track	16
Per sector	512 bytes

Transfer rate 5.0 megabits/second

Access time

Track to track	3 ms
Average	170 ms
Maximum	500 ms
Head settling time	15 ms

Average latency 8.33 ms

12.6.2 Reliability Specifications

Mean time to repair	30 minutes
Preventive maintenance	Not required
Error rates	
Soft read errors	1 per 10^{10} bits read
Hard read errors*	1 per 10^{12} bits read
Seek errors	1 per 10^{6} seeks

12.6.3 Functional Specifications

Rotational speed	3600 rpm ± 1%
Recording density	7690 bpi maximum
Flux density	7690 fci maximum
Track density	255 tpi
Cylinders	153
Tracks	612
Read/write heads	4
Disks	2

12.6.4 Electrical Specifications

Requirement	Min	Mid	Max
+5 volt power	+4.75V	+5.0V	+5.25V
Ripple	—	—	50mV
Current	—	0.7A	1.0A
+12 volt power	+11.4V	+12.0V	+12.6V
Ripple	—	—	75mV
Current	—	1.8A	4.5A †

12.6.5 Environmental Specifications

Ambient Temperature

Operating	10° to 50° C (50° to 122° F)
Nonoperating	−40° to 66° C (−40° to 151° F)

Temperature Gradient

Operating	11° C/hr (20° F)
Nonoperating	20° C/hr (36° F)

Maximum elevation

Operating	2.4 km (8000 ft.)
Nonoperating	9.1 km (30,000 ft.)

* Not recoverable within 8 retries

† Current draw for 20 seconds at power on.

Heat Dissipation

Typical	25 W (85 BTU/hr)
Maximum	29 W (99 BTU/hr)

Relative Humidity

Operating	20 to 80%
Nonoperating	10 to 95%

Operating Shock

Half sine-shock pulse of 10g pk of 10 +3ms duration applied perpendicular to each side.

12.6.6 Mechanical Dimensions

Height	82.55 mm	(3.25 in)
Width	146.05 mm	(5.75 in)
Depth	204.47 mm	(8.05 in)
Weight	2.27 kg	(5 lbs)

CHAPTER 13
POWER SUPPLY

13.1 INTRODUCTION

This chapter describes the operation of the power supply in the Professional 350 computer. The shaded area in Figure 13-1 represents the relationship of the power supply to other components on the Professional 350 system.

The H7862 switching power supply converts line mains ac voltage to dc according to the Professional 350 specifications. To protect itself and the computer system, the power supply also monitors voltage input and output. Figure 13-2 shows the functional block diagram for the power supply.

The power supply also asserts two status signals to the CPU on the system module. These signals tell the CPU that ac and dc power have reached correct values. After receiving these signals, the CPU starts executing a boot program.

Section 13.6 provides the physical and electrical specifications for the power supply.

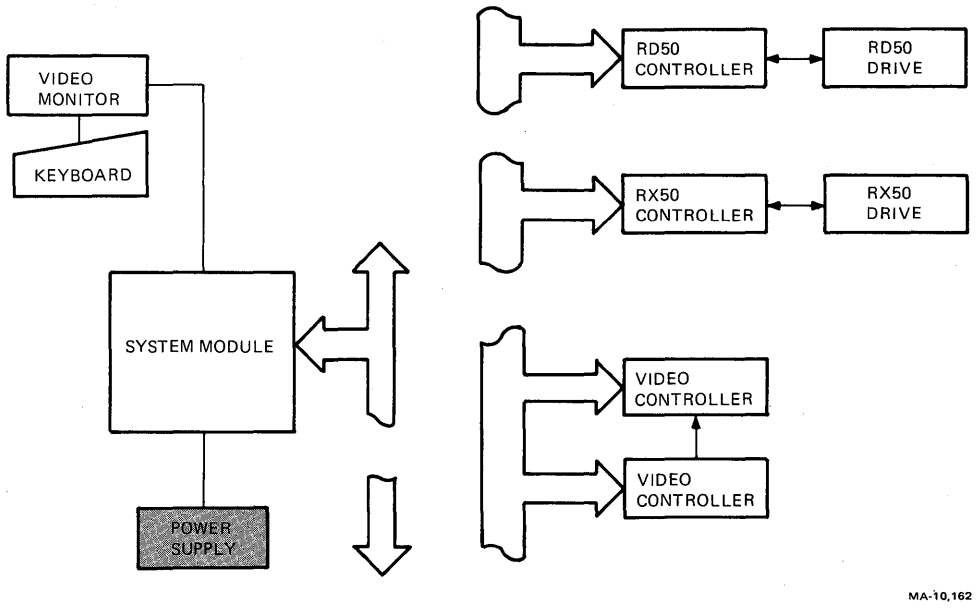


Figure 13-1 System Functional Block Diagram

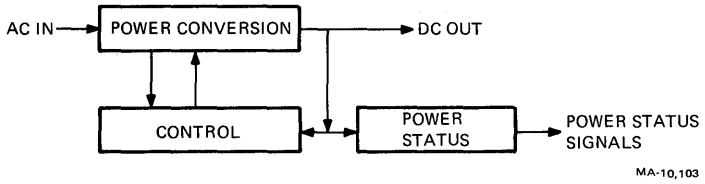


Figure 13-2 Power Supply Functional Block Diagram

13.2 PHYSICAL DESCRIPTION

The power supply connects to the system module with a cable (PN 17-00280) from J2 of the power supply. It connects to the RX50 diskette drive with a 6 inch cable (PN 17-00342-02) from P1 of the power supply, and to the RD50 hard disk drive with a 4 inch cable (PN 17-00342-01) from P2.

The power supply box mounts inside, on the top left of the Professional 350 computer's chassis. Two slide-lock connectors hold the four studs on the bottom of the power supply chassis. Figure 13-3 shows the power supply.

A rocker switch on the front panel (Figure 13-3) turns system power on and off and acts as a reboot switch for the CPU.

The exhaust fan on the left side cools the supply by pulling air across heat sinks and internal components. The air is drawn through the power supply chassis from the right side (which is all ventilating holes) and across the entire system chassis. This air movement cools the system components, option modules, and disk drive motor(s).

The rear panel has a connector for the ac power cable (Figure 13-3). The connector is polarized and allows the cable to be inserted in only one way. A circuit breaker protects internal wiring from component failure.

Before applying power for the first time, the user must set the voltage select slide switch for the ac mains operating voltage (line voltage). The user must also set this switch anytime the mains voltage changes.

The power supply contains three jacks. The rear jack connects to the system module circuit board. The two on the right side connect to the diskette motors and the optional hard disk drive.

Section 13.6 provides the physical and electrical specifications for the power supply.

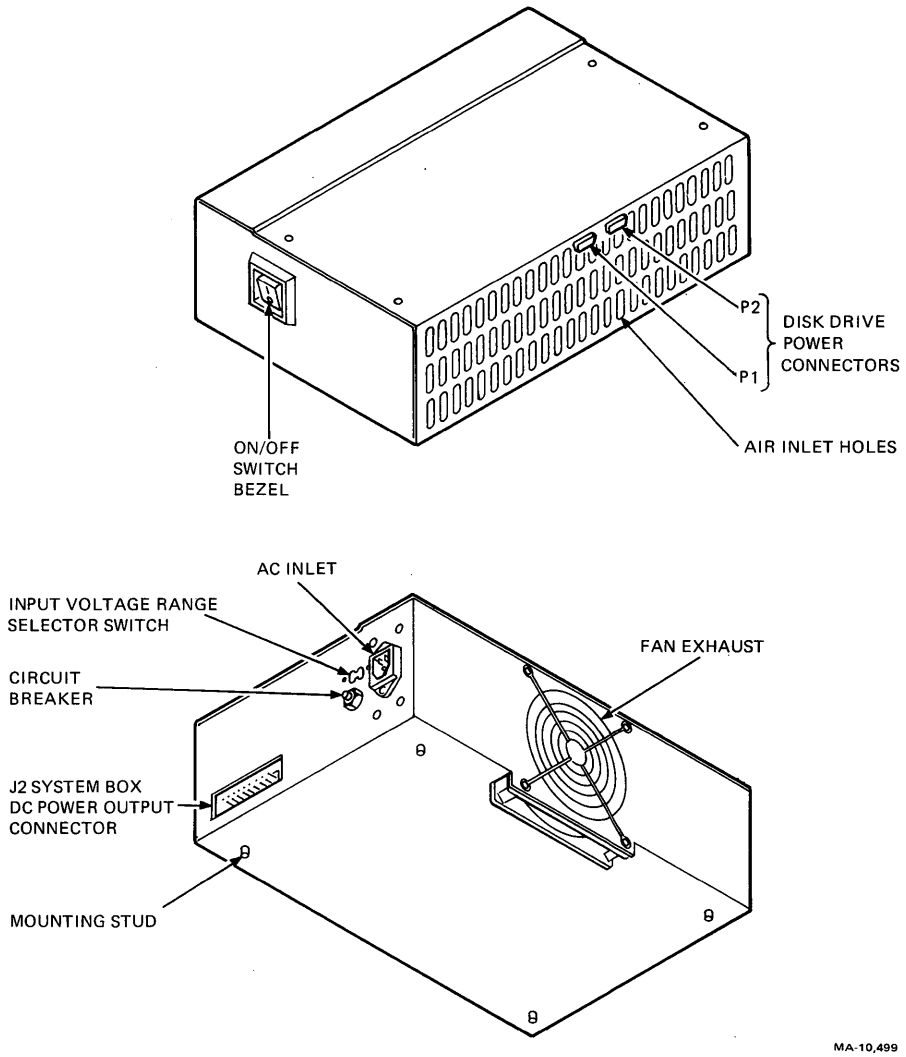


Figure 13-3 H7862 Power Supply

13.3 FUNCTIONAL DESCRIPTION

The power supply converts ac to dc at mains voltage. The user sets the voltage selection slide switch on the rear panel, plugs the ac power cable into the power supply and ac source, and turns on the front panel switch. Table 13-1 shows the possible combinations of settings for the voltage selection switch and the actual ac input. A separate rectifier and regulator on the circuit board power the internal circuits. these circuits control regulation, protection, and the power status signals to the CPU.

WARNING

Check the ac select switch setting. A setting for 120 Vac operation in a 240 Vac environment causes the internal fuse to blow. If the power switch is immediately turned off, it is possible to reset the switch correctly and then use the computer. However, the power supply must be repaired, before using the computer in a 120 Vac environment. If the circuit breaker trips within 3 to 8 seconds, the primary capacitors and possibly more components are destroyed.

13.3.1 Power Conversion

Mains ac voltage is first filtered and then rectified to produce a dc voltage. The dc is then switched by two switching transistors that present high voltage dc pulses to the power switching transformer primary. The transformer's output, dc pulses, are rectified and filtered again to produce smooth dc. This permits the regulator to control the amount of energy transferred to the rest of the computer.

The transistors' switching is controlled by a driver transistor. The switch control signal, SWCON, controls the driver transistor. Section 13.4.2.1 provides a detailed description of how this works.

A crowbar protection circuit grounds the +5 and +12 Vdc outputs in the event of component failure. This prevents excessive voltages from getting out to the system devices. A diode in the −12 Vdc output serves the same purpose.

WARNING

The input capacitors hold high voltages for up to 5 minutes after system power is turned off. Refer to Section 13.4.1 for high voltage testing instructions.

Table 13-1 AC Voltage Switch Settings

Switch Setting	Voltage	Operation
120	120	OK
240	240	OK
120	240	Internal fuse blows, protecting the transformer and fan. Refer to Section 13.3.
240	120	Fan turns at 1/2 speed. Green indicator on rear of system box does not light. Switching transistors do not turn on. No power is provided to rest of system.

13.3.2 Control Circuits

When power is first applied, the start-up regulator provides power for the internal control circuits and reference voltages used in protection circuits. The regulation circuit controls the duration of the switch pulse.

The two types of control circuits, regulation and protection, are discussed in the following paragraphs (Figure 13-4).

13.3.2.1 Regulation – Regulation circuits, using pulse width modulation, maintain the voltage levels. This is done by adjusting the pulse width of SWCON. As current demand changes, the current sensing circuit holds SWCON high, making its pulses longer. The longer pulse permits the switching transistors to stay on for a longer time, permitting additional energy transfer and output power.

13.3.2.2 Protection – Protection circuits prevent damage from incorrect voltages. There are three protection circuits: overvoltage, start-up undervoltage, and overcurrent. These are exclusive of the circuit breaker and fuse. The circuits are ANDed so that any fault condition stops the switching transistors (Figure 13-5). The circuit names indicate the kind of protection given by each circuit. Table 13-2 shows the threshold values for the protection circuits.

The −12 Vdc regulator chip has an internal overcurrent protection circuit. A diode protects the chip from reverse voltages.

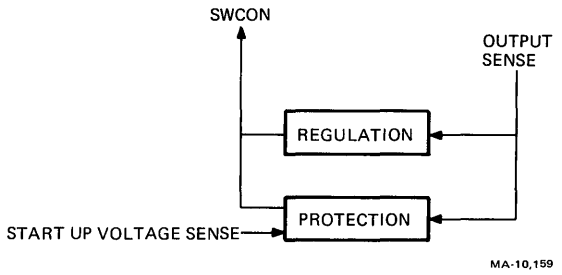


Figure 13-4 Control Block Diagram

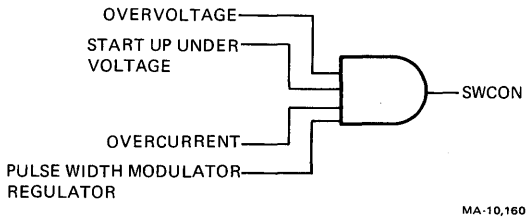


Figure 13-5 Protection

Table 13-2 Voltage Protection Thresholds

Output	Over Voltage	Over Current
+5	7.0 V max	21–29 A
+12	14.5 V max	11–15 A
−12	−14.0 V max	1.5–2.5 A

13.3.3 Power Status Signals

There are two power status signals sent to the CPU from the power supply: DCOK and POK. DCOK indicates that the dc levels are at specified voltages. POK tells the CPU that ac has been applied long enough to charge the primary capacitors so the emergency power loss program can be executed.

13.4 DETAILED DESCRIPTION

This section describes how each circuit group works.

13.4.1 Power Conversion

Incoming ac first passes through a line filter. This prevents computer-generated noise pulses from being generated into the ac mains (line voltage). A full wave bridge then converts the ac to dc. If the ac mains is 120 Vac, then the full wave bridge serves as a voltage doubler and rectifier. This provides 250-350 Vdc to the two input capacitors. The capacitors store the energy for the switching cycles (Figure 13-6).

The regulation circuits, using the signal SWCON, make the switch driver transistor pulse on and off. This places a voltage across the control winding of the base power transformer and turns the two switching transistors on and off. Section 13.4.2 describes the circuits that control SWCON.

The switching transistors place a dc pulse on the primary of the switching transformer. The pulse has high voltage (about 360 Vdc) at low current and the transformer converts this to low voltage at high current. The switching frequency stays constant at 50 kHz. However, the pulse width changes to control the amount of power the transformer couples to the power supply output.

There are three secondaries to the transformer, one for each of the output voltages. Each ac output is rectified. The dc passes through low pass filters to smooth the pulsing dc output. Inductors and capacitors work together to smooth the pulses and steady the dc.

Crowbar protection circuits on the outputs of the +5 and +12 Vdc lines protect the computer in the event of component failure in the power supply. These circuits short the outputs to ground. A diode in the −12 Vdc output protects the 3-pin regulator chip and its output devices from positive voltages in the same way.

WARNING

The input capacitors hold high voltages for 5 minutes after system power is turned off. Before removing the power supply cover, turn off the power supply. Wait 5 minutes. Then measure the dc voltage from the case of Q2 (TO-3 transistor closest to the open side of the case) to the end of bleeder resistor R4 (also closest to the open side of the case). First set the meter to at least 500 Vdc full scale and reduce it as needed. If the voltage is 20 V or less, proceed with caution.

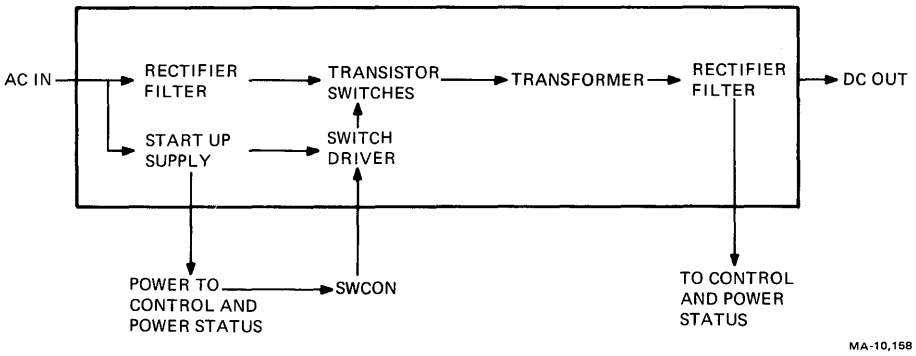


Figure 13-6 Power Conversion

13.4.2 Control

The signal, SWCON, controls the pulse width of the switched dc output from the power supply. Its sources are the regulation and protection circuits. When SWCON is high, it turns off a pre-driver transistor which turns off the driver transistor. The driver transistor controls the switching transistors by opening the control winding in the base power transformer. When the driver is off, the switching transistors are on.

The following sections describe the regulation and protection circuits.

13.4.2.1 Pulse Width Modulation Regulation – The +5 and +12 Vdc voltages are compared by a divider network and comparator circuit that provide a constant input to a regulator IC. When current demand is high, a drop in voltage occurs. The regulator senses the voltage drop and increases the pulse width (duty cycle). This permits additional energy transfer during the extended switch pulse.

The regulator's control signal is ANDed with the output of the protection circuits (Section 13.4.2.2) before going to the pre-driver transistor.

The −12 Vdc output has its own 3-pin regulator chip.

Soft Start – On power-up or when recovering from an overcurrent condition, the pulse width modulator goes through a soft start routine. This means the pulse width increases slowly from zero to operating width. The width is controlled by the charging of the output soft start capacitor. This prevents voltage surges on the output. If an output shorts this gives the overcurrent circuit time to act before damage occurs.

13.4.2.2 Protection – The overvoltage, start-up under voltage, and overcurrent circuits prevent internal damage to the power supply and the computer it is installed in. They are ANDed with the regulator's output so that any change from normal operation pulls SWCON low. This halts the switching transistors' control circuits (Figure 13-7) and prevents the switching transistors from applying input to the power transformer primary.

Overvoltage – Each output voltage is compared to internally generated reference voltages. These reference voltages come from the voltage across a precision zener diode. If any of the three output voltages exceed specified parameters, a latch circuit is tripped. The latch turns the switching transistors off and prevents further dc output. Since this latch is electrical, the operator must remove system power (turn it off) before power can flow again.

If the −12 Vdc circuit has a positive voltage applied to it, a diode protects the regulator chip by grounding the output.

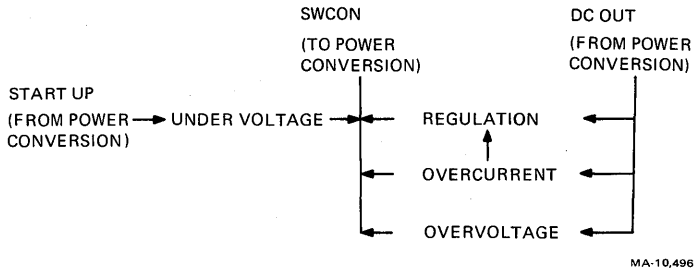


Figure 13-7 Protection Block Diagram

Start-Up Undervoltage – This circuit checks the power supply's start-up supply. If the voltage drops to 8.75 Volts or less, it turns off the switching transistors. When voltage rises to normal, switching can start again.

Overcurrent – This circuit checks the current drain on the +5 and +12 Volt lines. Divider networks compare the voltage drop across a current sense resistor. When the voltage across the sense resistor rises above the threshold value, a timing capacitor is discharged. SWCON is then held low, stopping the switching action. At the same time, the soft start capacitor begins discharging.

When the overcurrent condition clears, the timing capacitor starts charging. This begins a delay period. When the timing capacitor has charged enough, the overcurrent circuit releases SWCON so that switching can start again. However, the soft start capacitor discharg creates a slow restart. This helps prevent damage by detecting the fault, if it is still on the output, before the supply delivers full power.

The overcurrent sense capacitor requires 1 ms to charge up again. this allows the voltages and current to stabilize (soft start) before SWCON cycles again.

The −12 Vdc regulator chip has an internal overcurrent protection circuit.

13.4.3 Power Status Monitor

NOTE

In this section, ac and dc refer to mains alternating current and the direct current output. The signal names, AC and DC, refer to specific signals used in the power status monitor circuits.

The power supply control circuits assert two signals to the CPU on the main system board. There is a specific sequence for the two signals on power up and power down; DCOK is asserted before POK on power-up and POK is cleared before DCOK on power down (Figure 13-8).

The dc detector looks for minimum values for the +5, +12, and −12 Vdc outputs. DCOK indicates that the power supply voltages from the power supply to the system module are within tolerance.

The ac detector measures ac at the switching transformer's secondary and is related to the energy stored in the input filter capacitors. POK H tells the CPU that ac has been applied long enough to charge the primary capacitors so the emergency power loss program can be executed. The signal change from a low to a high state initiates the boot program in the CPU (DCOK is high also). The change from high to low initiates the emergency power loss program.

The following sections describe how the signals are generated. Refer to Figures 13-8 and 13-9 while reading these sections.

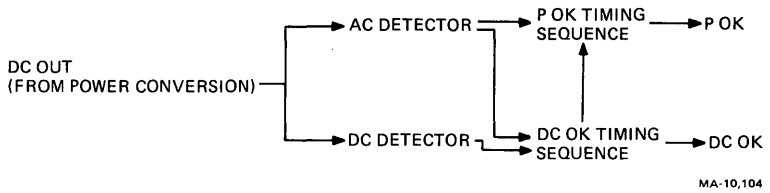


Figure 13-8 Power Status

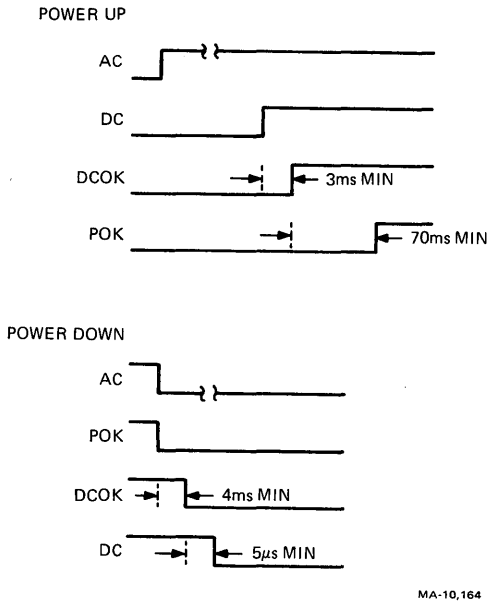


Figure 13-9 Power Status Signal Timing

13.4.3.1 DCOK – When all voltages have reached their minimum values, the protection circuit asserts DC. DC and AC (ac is present long enough to produce a +5 Vdc output) are asserted at the beginning of a timing chain. AC and DC clock a one-shot timer. DCOK is asserted to the CPU a minimum of three ms later.

The DCOK timing circuits also receive input from the ac detector (which asserts POK). The ac detect information permits the DCOK signal to time out through a capacitor if ac source voltage stops. On power down, the falling edge of AC removes POK. This starts timing out DCOK. A minimum of four ms after AC is removed, DCOK is removed and the CPU executes the emergency power loss program.

The monitor circuits indicate an output is in regulation if the voltage is greater than the following voltages.

- +5 Vdc +4.7 ±0.2 V
- +12 Vdc +11.1 ±0.3 V
- −12 Vdc +10.8 ±0.3 V

13.4.3.2 POK – On power up, the +12 Vdc asserts AC and sets a one-shot timer. This is ANDed with a signal that indicates the DCOK signal is asserted. A one-shot timer asserts POK a minimum of 70 ms later.

On power down, the falling edge of AC removes POK.

13.5 CONNECTORS

Table 13-3 shows the pinning for J2, the system module connector on the rear panel.

Table 13-4 shows the pinning for P1 and P2, the disk motor(s) connectors on the side panel.

Table 13-3 System Module Connector, J2

Pin	Voltage/Signal
1	DCOK
2	reserved
3	POK
4	−12 Vdc
5	+12 Vdc
6–9	+5 Vdc
10–16	Ground

Table 13-4 Disk Motor(s) Connectors, P1 and P2

Pin	Voltage/Signal
1	+12 Vdc
2–3	Ground
4	+5 Vdc

13.6 SPECIFICATIONS

The following paragraphs provide the specifications for the power supply.

13.6.1 Physical

Height	10.8 cm (4.25 in)
Width	21.0 cm (8.25 in)
Depth	33.0 cm (13.0 in)
Weight	4.54 kg (10 lbs)

13.6.2 Electrical

Line voltage	87 – 128 Vac (for 120 Vac operation) 174 – 256 Vac (for 240 Vac operation)
Line frequency	47 – 63 Hz (for either voltage range)
Input line current (at full rated output)	6 A rms (for 120 Vac operation) 4 A rms (for 240 Vac operation)
Real input power (at full rated output)	320 Watts
Output regulation	+5 Vdc ±5% +12 Vdc ±5% −12 Vdc ±5%
Rated output voltage and current specifications	+5 Vdc at 5 A min, 20 A max +12 Vdc at 1 A min, 8 A max −12 Vdc at 100 mA min, 1 A max

Printed in U.S.A.
EK-PC350-TM-001