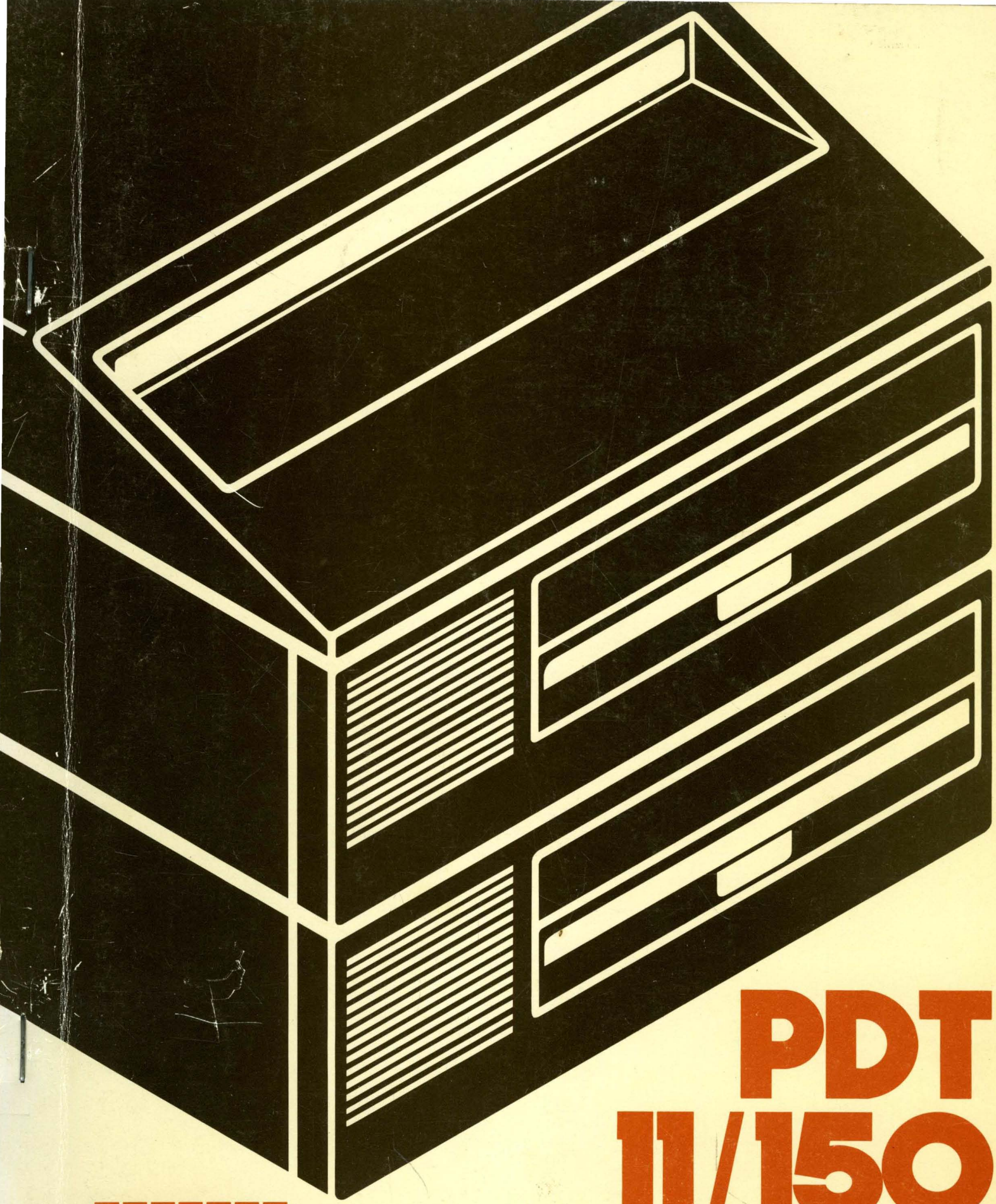

digital

PDT 11/150

USER GUIDE

EK-PT150-UG-003

PDT-11/150
USER GUIDE

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CHAPTER 1
INTRODUCTION

This guide contains the information required to unpack, inspect, install and verify the proper operation of the Programmable Data Terminal PDT-11/150. Also included is programming information necessary to develop the application software. The PDT-11/150 is a user-programmable disk storage system available as either a single flexible (floppy) disk drive unit or dual flexible disk drive unit. Input to and output from the system is through serial line terminals (consoles, printers, etc.) which conform to EIA standard RS-232C.

Chapter 1 provides a general introduction to the PDT-11/150 operating system and includes the specifications for the single and dual disk drive units. Also included is a list of the supporting publications.

Chapter 2 contains detailed procedures for unpacking the PDT-11/150, inspecting the unit and related contents, and connecting the unit to ac power and associated terminals.

Chapter 3 defines the switches and indicators and provides detailed procedures to verify the proper operation of the PDT-11/150.

Chapter 4 includes installation information required to incorporate the various options available into an existing PDT-11/150 unit.

Chapter 5 provides programming information and considerations for the development of application software.

1.1 GENERAL DESCRIPTION

Figure 1-1 is a typical operating system configuration which includes the maximum number of terminals. Three serial devices connect to the standard EIA-level converter, and three serial terminals connect to the cluster EIA-level converter (optional).

The standard EIA-level converter allows full or half duplex operation with a console terminal, printer terminal or communications device (modem). The cluster converter expands the capability of the unit to include three additional serial line terminals; however, only one console, one line printer, and one modem device are allowable for each system.

The data transfer rates to and from the devices and terminals are dependent on the applications program or operating system and the number and types of peripheral units connected to the PDT-11/150. Refer to Paragraph 5.2 for detailed data transfer rate information.

The PDT-11/150 is controlled by a DIGITAL LSI-11 microprocessor and application programs can be developed on PDP-11/V03 systems or equivalent using RT-11V3 (or later versions) operating systems available for the LSI-11 microprocessor.

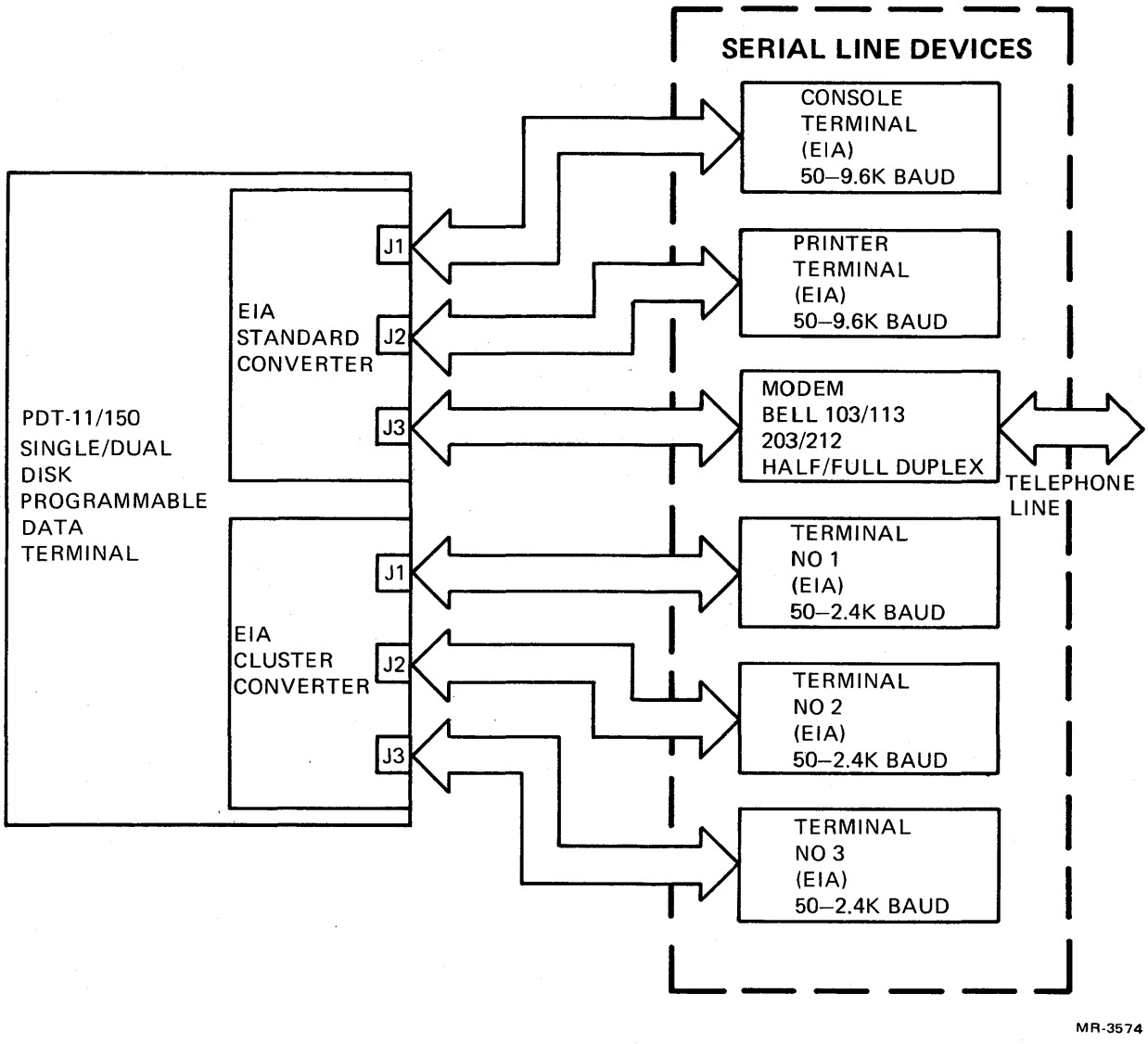


Figure 1-1 Typical PDT-11/150 Flexible Disk Operating System

1.1.1 System Configurations and Options

Figure 1-2 lists the model designations assigned to each of the PDT-11/150 units. The units are available with a single disk drive or dual disk drive. They operate with either 120 V/60 Hz input ac power or several voltage ranges for the 50 Hz power.

Table 1-1 lists and describes the options associated with the PDT-11/150. The RXT01-AA or -AC option is always included with a dual disk drive unit.

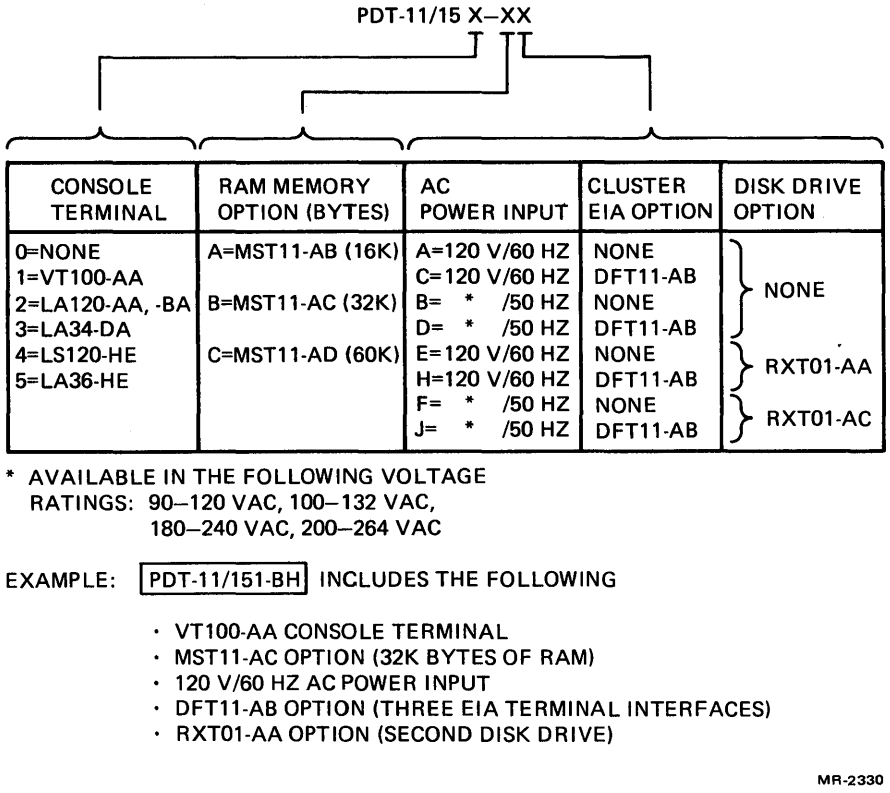


Figure 1-2 PDT-11/150 Model Designations

Table 1-1 PDT-11/150 Options

Option No.	Description
RXT01-AA	60 Hz disk drive assembly includes enclosure and front bezel
RXT01-AC	50 Hz disk drive assembly includes enclosure and front panel
DFT11-AA*	Standard EIA converter module (includes cable and USARTs)
DFT11-AB	Cluster EIA converter module (includes cable and USARTs)
MST11-AB †	RAM module/16K bytes
MST11-AC †	RAM module/32K bytes
MST11-AD†	RAM module/60K bytes
	(The MST11 modules include diagnostic ROM with bootstrap loader.)
KDT11-AA*	Intelligence module with ROM program
DLT11*	Peripheral module with USARTs for standard EIA terminals
RXT11*	Disk controller module with ROM program

*Included with all PDT-11/150 models.

†These options are factory installable only.

1.1.2 PDT-11/150 Equipment Specifications

Table 1-2 describes the mechanical, environmental and electrical characteristics of the PDT-11/150 units.

Table 1-2 PDT-11/150 Specifications

Characteristic	Description
Mechanical	
Overall Dimensions	
Single Disk Unit	51.0 cm (20.08 in) length × 33.02 cm (13.0 in) width × 20.9 cm (8.23 in) height
Dual Disk Unit	51.0 cm (20.08 in) length × 33.02 cm (13.0 in) width × 34.8 cm (13.42 in) height
Weight	
Unpackaged	Single disk unit: 33 lb Dual disk unit: 46 lb
Packaged	Single disk unit: 40 lb Dual disk unit: 55 lb
Environmental	
Temperature	
Operating	15° C to 32° C (59° to 90° F) ambient (Temperature is derated 1.8° C/1000 m or 1° F/1000 ft for altitude.)
Maximum gradient	11° C/hr (20° F/hr)
Nonoperating	-35° C to +60° C (-30° F to 140° F)
Humidity	
Operating	Maximum wet bulb: 25° C (77° F) Minimum dew point: 2° C (36° F) Relative humidity: 20% to 80%
Nonoperating	5% to 95% relative humidity (noncondensing)
System Reliability	Disk Life: 3 million revolutions per track with head loaded. The head contacts 5 tracks when loaded. Seek error rate: 1 in 10^6 seeks Soft read error rate: 1 in 10^9 bits read Hard read error rate: 1 in 10^{12} bits read NOTE **The above error rates only apply to media that is properly cared for. Seek error and soft read errors are usually attributable to random effects in the head/media interface, such as electrical noise, dirt, or dust. Both are defined as "soft" errors if the error is recoverable in ten additional tries or less. "Hard" errors cannot be recovered. Seek error retries should be preceded by an initialize or restore command.**

Table 1-2 PDT-11/150 Specifications (Cont)

Characteristic	Description
	NOTE **To ensure the integrity of the information stored on the disk, the disks should not be in the disk drives when the ac power is initially applied to the unit. The disks should be removed from the disk drives before the ac power is removed from the unit.**
Drive Performance Data transfer rate disk to RAM module	32 μs/16-bit word (nominal)
Track-to-track-move	10 ms/track max
Head settle time	20 ms max
Rotational speed	360 r/min ± 2.5%; 166 ms/rev nominal
Recording surfaces per disk	1
Tracks per disk	77 (0–76) or ($0–114_8$)
Sectors per track	26 (1–26) or ($1–32_8$)
Recording technique	Double frequency
Bit density	3200 bits/in at inner track
Track density	48 tracks/in
Average access*	488 ms
ac Power Requirements 115 V/60 Hz Input	Single disk drive: 2.5 A Dual disk drive: 3.0 A
90–130 V/50 Hz Input	Single disk drive: 2.5 A Dual disk drive: 3.0 A
180–264 V/50 Hz	Single disk drive: 1.5 A Dual disk drive: 2.0 A
Device Signals	All device signals are serial line and compatible with EIA standard RS-232-C. (Refer to Tables 2-4 and 2-5 for signal requirements.)

* **Seek** (77 tks/2) × 10 ms + **Settle** 20 ms + **Rotate** (166 ms/2) = **Total** 488 ms

1.1.3 Media Specifications

Table 1-3 describes the physical and electrical characteristics of the flexible disk media used with the PDT-11/150.

Table 1-3 Flexible Disk Specifications

Specifications	Description
Description	Mylar based, oxide-coated disk
Dimensions	
Disk	19.8 cm (7.8 in) diameter
Jacket	20.26 cm (7.94 in) square
Recording Format	Single-side, industry-compatible according to IBM 3740 floppy disk format, 77 data/address tracks
Operating Temperature/Humidity	Media temperature must be within PDT-11/150 operating temperature and humidity range before use
Storage	
Temperature	-34° C (-30° F) to 52° C (125° F)
Relative Humidity	10% to 80% (noncondensing)
Magnetic field	Exposure to magnetic field strength of 50 oersteds or greater may result in loss of data.

1.2 REFERENCE DOCUMENTS

Table 1-4 lists the related publications that are available for the PDT-11/150 system. These publications provide detailed operator and maintenance information.

Table 1-4 PDT-11/150 Related Publications

Document No.	Title	Medium*
EK-PT150-IN	PDT-11/150 Installation Guide	Printed
EK-PT150-J1	PDT-11/150 Mini Maintenance Hardware Guide	Printed
EK-PT150-TM	PDT-11/150 Technical Manual	Printed/ Microfiche

*Purchase orders for publications should be forwarded to:

Digital Equipment Corporation
Accessories and Supplies Group
Cotton Road
Nashua, New Hampshire 03060

Contact your local sales office or call toll-free 800-258-1710 from 8:30 a.m. to 5:00 p.m. eastern standard time (U.S. customers only). New Hampshire, Alaska, and Hawaii customers should dial (603)-884-6660. Terms and conditions include net 30 days and F.O.B. DIGITAL plant. Freight charges will be prepaid by DIGITAL and added to the invoice. Minimum order is $35.00. Minimum does not apply when full payment is submitted with an order. Checks and money orders should be made out to Digital Equipment Corporation.

1.3 SUPPLIES AND ACCESSORIES

DIGITAL's Direct Sales Catalog includes a complete line of computer and terminal supplies and accessories specifically designed for use with DIGITAL systems. These products enable reliable and efficient operation of your equipment. These products include:

- Preformatted flexible disks
- Power and terminal cables
- Printer and video terminals
- Storage cabinets and tables

A copy of the catalog may be obtained by calling toll free:

800-258-1710 (8:30 am 5:00 pm EST)
603-884-6660 (New Hampshire, Alaska, and Hawaii)

CHAPTER 2
UNPACKING/INSTALLATION

The PDT-11/150 programmable data terminal is a free-standing, self-enclosed unit that can be placed on a desk or table. The console device, modem, printer, and terminals which operate with the unit are attached by cables to the rear panel. The devices can be located adjacent to the unit or at a remote location.

The PDT-11/150 units are packaged in reinforced cartons and protected by side cushions and a protective cover. The *PDT-11/150 Installation Guide*, EK-PT150-IN, is included with the unit. All remaining publications, when ordered, are supplied in a separate container.

This chapter provides the information necessary to unpack PDT-11/150 and supporting documents; and to inspect the contents and connect the units with the associated devices.

2.1 UNPACKING AND INSPECTION

Figure 2-1 shows the method used to unpack a dual drive unit. The single drive unit is packaged in a similar manner.

1. Remove the unpacking procedure diagram attached to the outside of the PDT-11/150 container.

2. Remove the PDT-11/150 unit according to the procedures on the diagram.

CAUTION
Do not lift the unit by grasping the front door handles of the disk drive assembly.

3. Visually inspect the unit for any physical damage.

NOTE
If physical damage is evident, notify a local DIGITAL sales office.

4. Open and remove the contents of any other cartons supplied.

5. Using the packing lists attached to each carton, inspect the contents of each to ensure that all items listed are supplied.

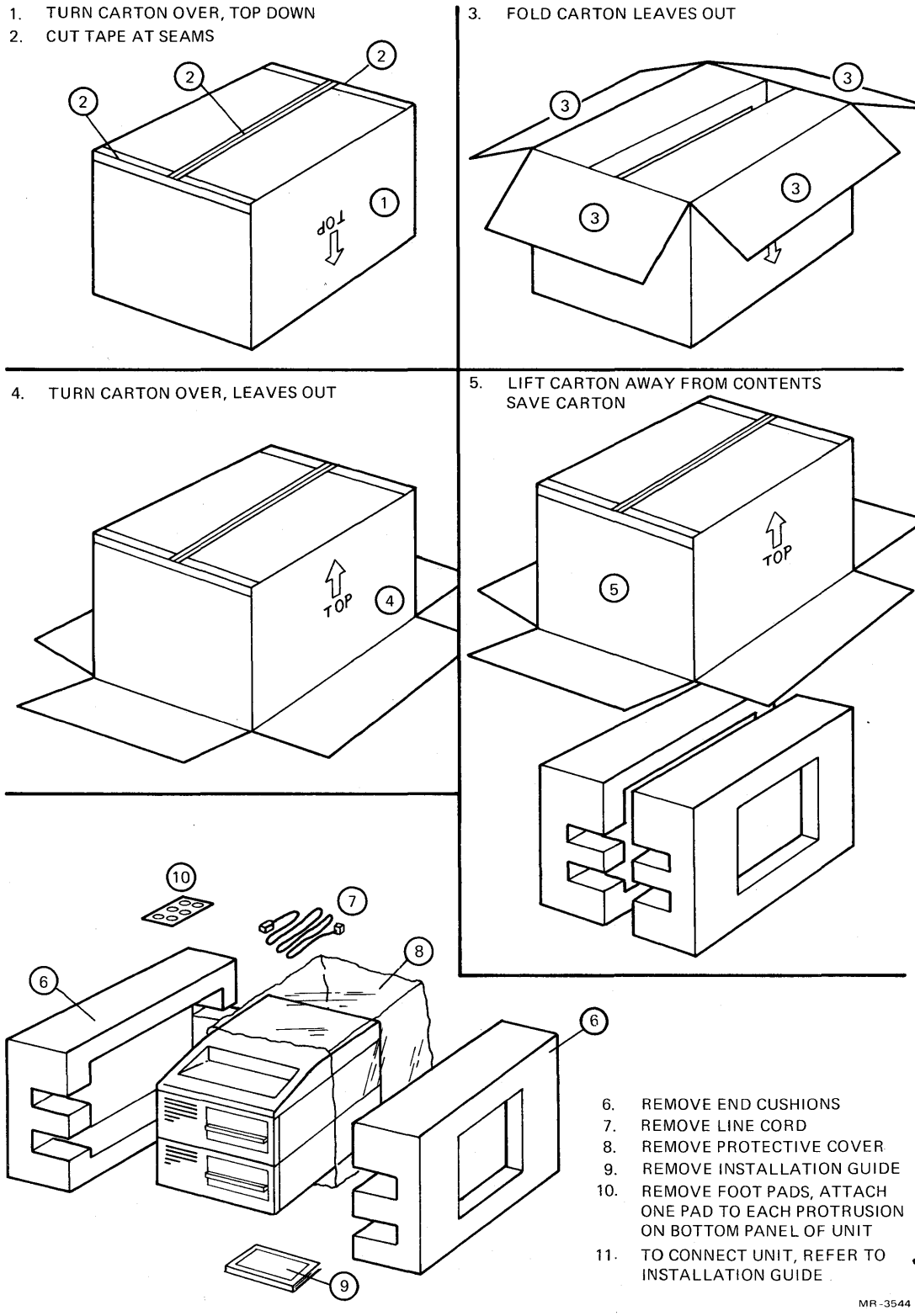


Figure 2-1 PDT-11/150 Unpacking Procedure Diagram

6. Connect the female end of the ac power cord to the recessed male connector on the rear panel of the unit.

CAUTION

The PDT-11/150 units are available to operate with several variations of the ac input power. Check the metallic label on the rear panel of the unit to ensure that the power supplied at the site is compatible with the unit requirements.

2.2 SITE PREPARATION AND CONNECTIONS

Figure 2-2 shows the overall dimensions of the single and dual drive units. Adequate clearance is required at the front of the unit for monitoring the indicators on the front panel and to allow the insertion and removal of the disk. Adequate area should be allowed at the rear of the unit for operation of the ac power switch and mode switch and to permit the free circulation of air through the fan also located on the rear panel. The signal and power cables that attach to the connectors on the rear panel should be free from obstructions and sharp bends.

NOTE

To prevent the accumlation of film and foreign matter on the disk and disk drive components, the PDT-11/150 should not be operated in locations having high levels of dust or industrial contaminants.

2.2.1 ac Power Requirements

Table 2-1 lists the voltage, frequency and current ratings of the PDT-11/150 models. Each unit is shipped with the appropriate ac power cable also listed. Additional cable lengths are also available on request. A separate ac power outlet is required for connecting the PDT-11/150 power cord and console terminal power cord. The main ac line to the outlet can be fused at 10 A or greater.

NOTE

Do not connect appliances or office equipment to the same ac circuits that supply power to the PDT-11/150 unit or associated console and terminals.

To connect the ac power, perform the following procedures:

1. Set the ac power switch on the rear panel to the OFF (0) position.
2. Connect the male end of the line cord to the ac outlet.
3. Connect the female end of the line cord to the rear panel of the PDT-11/150 unit.

2.2.2 Serial Line Cable Connectors

Three 25-pin serial line connectors are mounted on the rear panel of the PDT-11/150 and an additional three 25-pin connectors are optional as shown in Figure 2-3. All cables from the devices operating with the disk unit attach to these connectors through compatible 25-pin RS232-type plugs. Table 2-2 lists the type of devices that can be attached to each connector. The connector type used on the other end of the cable is dependent on the device. Cable assemblies are normally included with the terminals; however, additional cables of various lengths are available from DIGITAL.

Some of the typical cable assembly types are listed in Table 2-3 and can be ordered by contacting a local DIGITAL sales office.

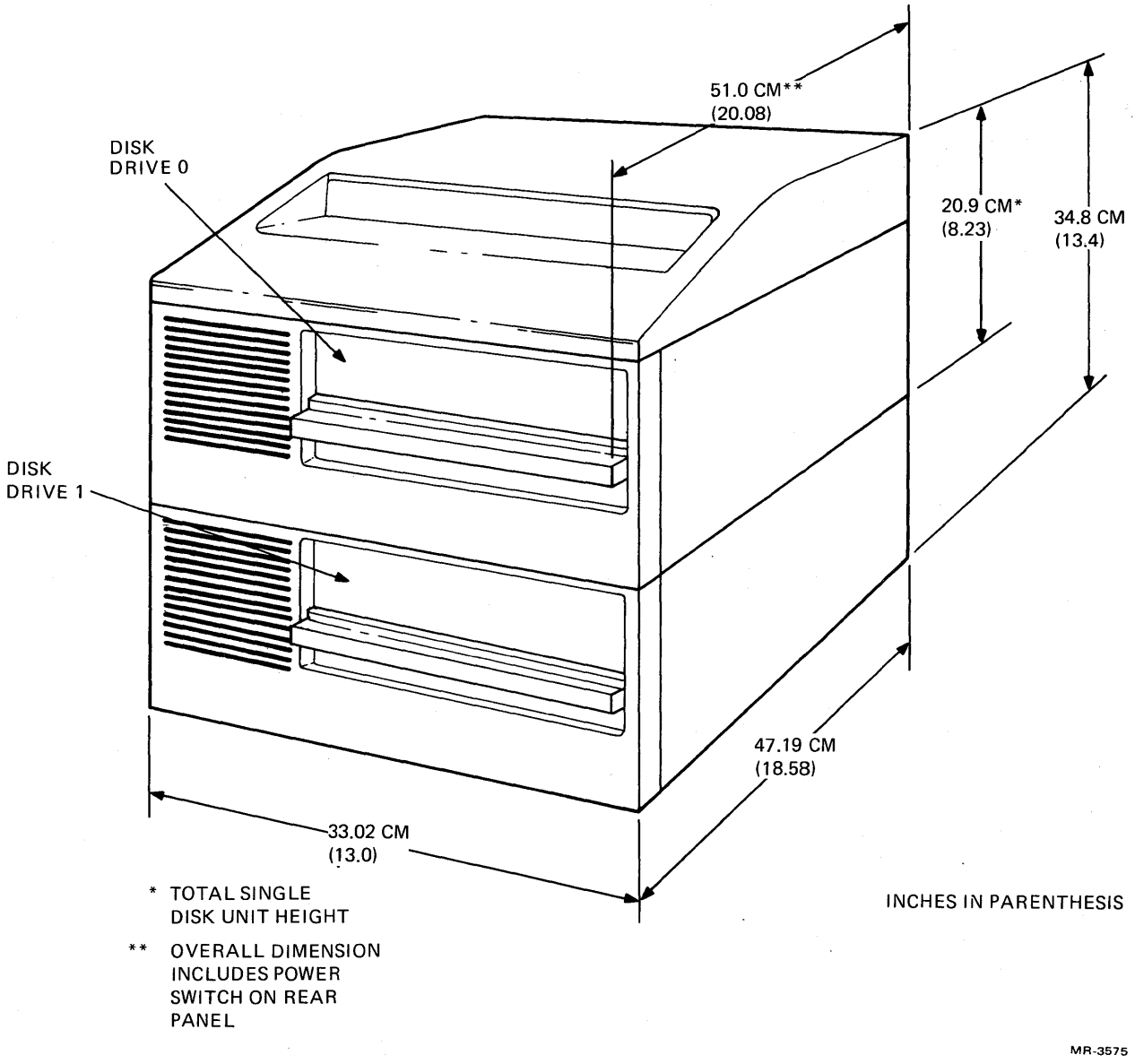


Figure 2-2 PDT-11/150 Single and Dual Disk Unit Dimensions

Table 2-1 ac Power Requirements

Model No.	Voltage (ac)/ Frequency	A/Unit	Cable No.
PDT-11/150-AA, -AC, -BA, -BC, -CA, CC (single disk drive)	100–125 V/60 Hz	2.5 A	1700083-09*
PDT-11/150-AE, -AH, -BE, -BH, -CE, -CH (dual disk drives)	100–125 V/60 Hz	3.0 A	
PDT-11/150-AB, -AD, -BB, -BD, -CB, -CD (single disk drive)	90–130 V/50 Hz 100–130 V/50 Hz	2.5 A	
	180–240 V/50 Hz 200–264 V/50 Hz	1.5 A	1700083-10* (Europe)
PDT-11/150-AF, -AJ, -BF, -BJ, -CF, -CJ (dual disk drive)	90–130 V/50 Hz 100–130 V/50 Hz	3.0 A	1700083-09* (Japan)
	180–240 V/50 Hz 200–264 V/50 Hz	1.5A	

*Cable lengths are 1.90 m (6.25 ft).

Table 2-2 Rear Panel, Device Connector Assignments

EIA Connections	
Standard	**Cluster**
Modem (J3)	Terminal 3 (J3)
Printer (J2)	Terminal 2 (J2)
Console (J1)	Terminal 1 (J1)

Table 2-3 Available Device Cable Assemblies

Cable No.	Cable Length	Connector	Cable Type	Connector
BC05C-25	25 ft	H856*	Round 25-conductor	RS232 (male)
BC05C-50	50 ft	H856*		RS232 (male)
BC05D-10	10 ft	RS232 (male)		RS232 (female)
BC05D-25	25 ft	RS232 (male)		RS232 (female)

*H856 40-contact female connector

2.2.2.1 EIA Connector Pin Assignments – Figure 2-3 shows the contact numbering of the rear panel EIA connectors. Connector J3 of the standard EIA connectors is male and all other connectors on both the standard EIA and cluster EIA option are female. The signal/pin assignments for the standard connectors are listed in Table 2-4 and those for the cluster connectors are listed in Table 2-5. These signals are pin-compatible with equipment conforming to RS-232-C specifications, but not all the signals defined by RS-232-C are required by the PDT-11/150.

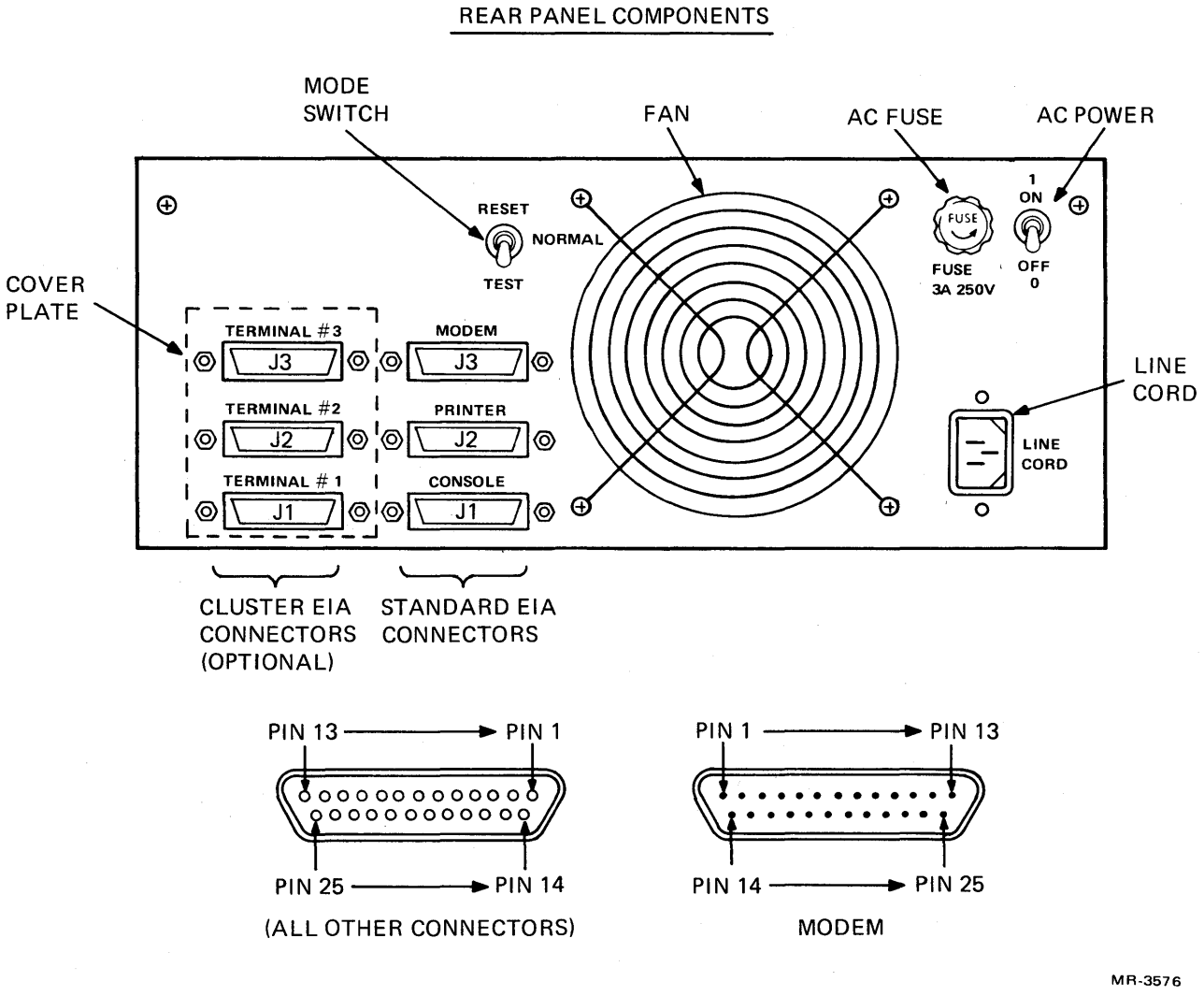


Figure 2-3 Rear Panel Components and Connector Pin Assignments

Table 2-4 Standard EIA Connector Signals

Connector	Signal Designation	Device
J1 (female) pin		*Console Terminal* DIGITAL-type:
2	Term Xmit Data	LA34 DECwriter IV
3	Term RCV Data	LA36 DECwriter II
20	Term RDY	VT50 DECscope
1	Chassis GND	VT100 video terminal
7	Signal GND	LA120 DECwriter III LS120 DECwriter III VT52 DECscope
J2 (female) pin		*Printer Terminal* DIGITAL-type:
2	LP Xmit Data	LA35 DECwriter II
3	LP RCV Data	LA36 DECwriter II
20	LP RDY	LA180 DECprinter
1	Chassis GND	LA34 DECwriter II
7	Signal GND	LA120 DECwriter III LS120 DECwriter III
J3 (male) pin		*Modem* Bell System type:
2	Modem RCV Data	103, 113, 202, 212, or equivalent
3	Modem Xmit Data	
12	SEC Carrier Detect	
5	PRI CTS	
22	Ring Indicator	
8	Carrier Detect	
6	Data Set RDY	
11	SEC RTS	
4	PRI RTS	
20	DTR	
17	SYN CLK R	
15	SYN CLK T	
1	Chassis GND	
7	Signal GND	

Table 2-5 Cluster Option EIA Connector Signals

Connector	Signal Designation	Device
J1 (female) pin		*Printer/Video Terminal* DIGITAL type:
2	Term 1 Xmit Data	LA36 DECwriter II
3	Term 1 RCV Data	VT50 DECscope
20	Term 1 RDY	VT52 DECscope
7	Signal IN (GND)	LA34 DECwriter IV
1	Chassis IN (GND)	VT100
		LA120 DECwriter III
		LS120 DECwriter III
J2 (female) pin		
2	Term 2 Xmit Data	
3	Term 2 RCV Data	Same as J1 terminal
20	Term 2 RDY	
7	Signal IN (GND)	
1	Chassis IN (GND)	
J3 (female) pin		
2	Term 3 Xmit Data	
3	Term 3 RCV Data	Same as J1 terminal
20	Term 3 RDY	
7	Signal IN (GND)	
1	Chassis IN (GND)	

2.2.2.2 Serial Line Cable Length – The maximum length of the serial line cables that connect from the PDT-11/150 to the terminals is 15.24 meters (50 feet).

2.3 SERIAL LINE DATA CHARACTERISTICS

The baud rate and character parameters of the serial line data transferred between the devices and terminals and the PDT-11/150 must be compatible. Refer to Chapter 5 for the initial data conditions and for the data parameter programming information.

CHAPTER 3
OPERATING PROCEDURES

The PDT-11/150 contains a series of diagnostic test programs stored in ROM and used to exercise the disk drives, the LSI-11 microprocessor and associated RAM module, and the peripheral ports which communicate with the serial line terminals. This chapter provides the information required to initiate the self-test functions and to monitor the results.

3.1 SWITCHES AND INDICATORS

The front panel indicators and the switches on the rear panel provide the controls used during the self-test programs. The console terminal display and keyboard are also used in conjunction with the controls and indicators.

3.1.1 Front Panel Indicators

The front panel is located at the front of the unit on the top cover. Figure 3-1 shows the four indicators and Table 3-1 lists and describes the function of each indicator.

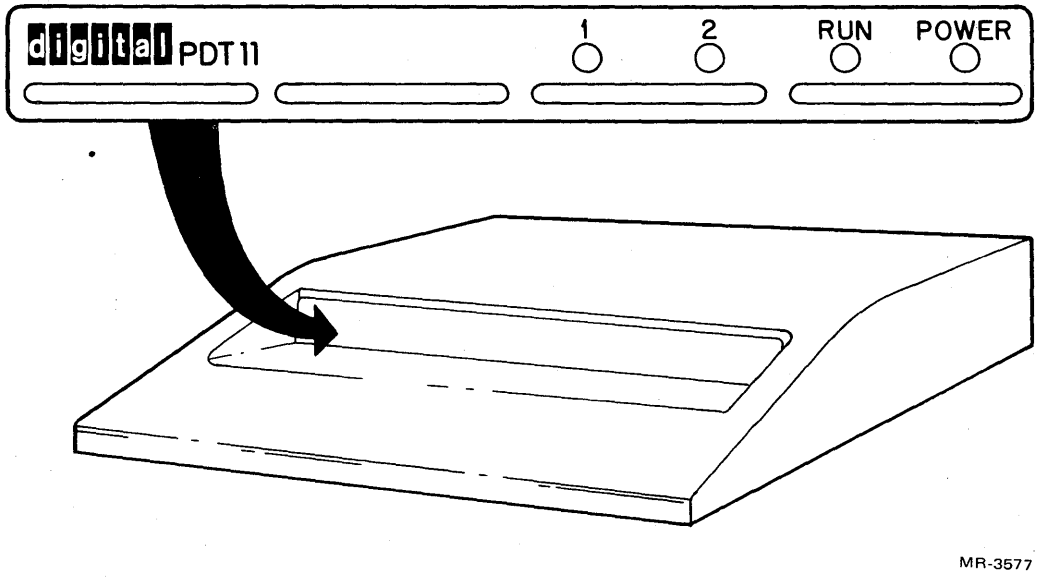


Figure 3-1 Front Panel Indicators

Table 3-1 Front Panel Indicators

Designation	Description
1	Lights to indicate a system error when in the self-test mode. During programmed operation, can be controlled by the user.
2	Lights to indicate that the system is waiting for an autobaud response from the console terminal. Occurs when ac power is applied to the unit or when the mode switch is momentarily set to the RESET position and released during program operation (NORMAL) or self-test mode. The autobaud function can be disabled by switch S1-1 (Table 5-24). During programmed operation, it can also be controlled by user program.
RUN	Lights to indicate that the LSI-11 microprocessor is executing instructions.
POWER	Lights to indicate that the +5 Vdc is present in the unit.

3.1.2 Rear Panel Switches and Components

The panel, mounted at the rear of disk drive 0, contains the ac power switch, fuse, and receptacle, a fan, the mode switch and the EIA 25-pin connectors. Figure 2-3 shows the location of the switches and components and Table 3-2 lists their functions. Refer to Paragraph 2.2.2 for a description of the 25-pin connectors and the associated devices.

3.1.3 Function Control Switch

The PDT-11/150 contains an internal 5-switch DIP pack (S1) used to select specific conditions during program operations and during test functions. The switch pack is mounted on the peripheral module and can only be accessed by removal of the top cover of the unit. When the unit is shipped, the switches are set to the positions shown in Table 3-3 (refer to Figure 4-11).

Table 3-2 Rear Panel Switches and Fuse

Item	Function
ac power toggle switch	Up position (ON) – applies ac power to the PDT-11/150.
Fuse (3 A, 250 V)	ac power fuse
Mode (toggle switch)	Three positions:
RESET	Up position (momentary) – Initializes the PDT-11/150 system by clearing registers and logic.
NORMAL	Center position (latch) – Allows normal operation of the PDT-11/150.
TEST	Down position (latch) – Initiates diagnostic testing of the PDT-11/150 system and allows the BREAK key detection from the console terminal keyboard.

Table 3-3 Function Control Switch Positions

Switch No. S1	Position	Function
1	OFF	Console terminal autobaud enabled
2	ON	Line time clock interrupt disabled
3	OFF	Dynamic RAM refresh enabled
4	ON	Self-test function of mode switch enabled
5	OFF	Manufacture mode disabled

3.2 DISK HANDLING AND STORAGE

The flexible disk used to store data and programs in the PDT-11/150 is shown in Figure 3-2. The oxide-coated disk is enclosed within a square plastic envelope. Precautions must be taken when handling and storing the disks to prevent loss of data or erroneous data and to ensure maximum operating life. The following practices are recommended.

1. To avoid touching the oxide surface of the disk, handle the disk by the envelope.

2. All disk identification should be written on a label prior to affixing on the disk. Do not write directly on envelope or apply a label over another label.

3. Solutions or chemicals should not be applied to the disk surface or to the envelope.

4. Clips or rubber bands should not be attached to the disk envelopes.

5. Heavy objects should not be placed on the disk.

6. Disks should not be subjected to sharp objects or magnetic fields.

7. Disks that are bent or mutilated should not be used.

8. The oxide-coated disk must not be removed from envelope.

9. Store disks in a box or contaminant-free enclosure.

10. Disks should not be exposed to direct sunlight or excessive heat.

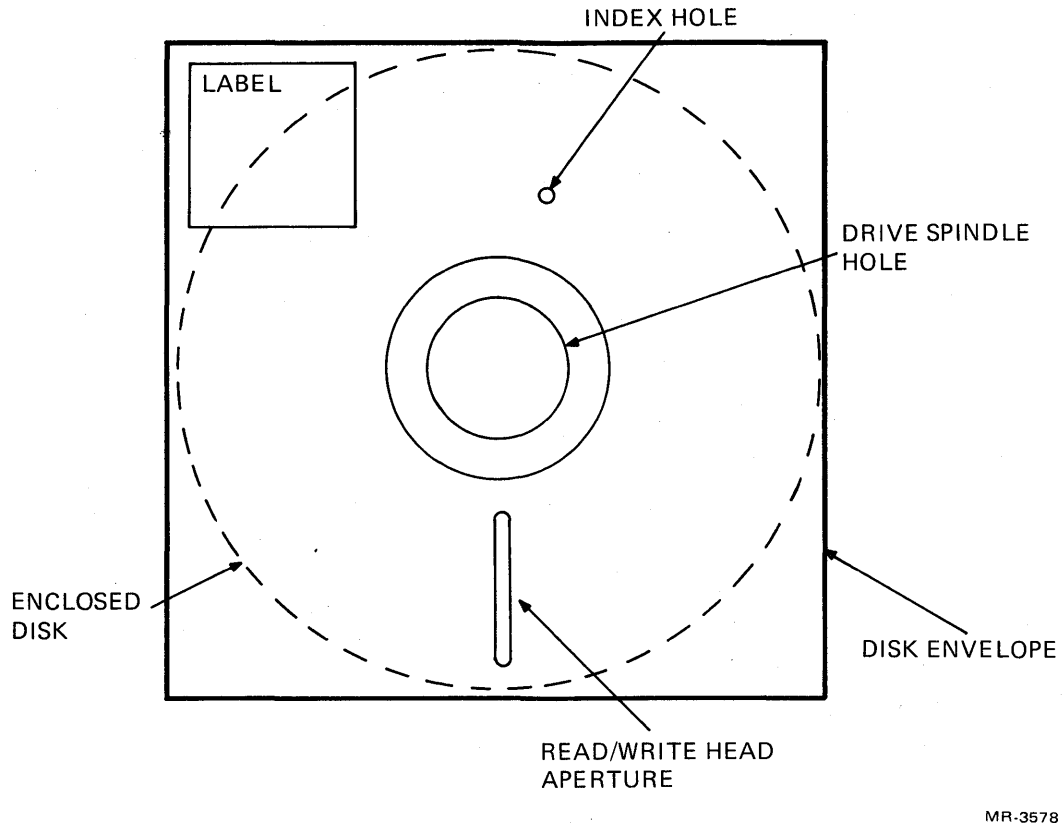


Figure 3-2 Flexible Disk

3.2.1 Insertion and Removal of a Disk

Perform the following procedures to load and remove a disk from the disk drive. Refer to Figure 3-3.

CAUTION

Remove all disks from the disk drives before applying ac power to the unit or removing the ac power from the unit. Do not install or remove a disk when the disk drive is performing read or write operations.

1. With the disk drive cover closed, grasp the center of the disk cover handle and press the release lever. The cover is spring-activated and will rise to the open position when the latch is released.

2. Hold the disk in the position shown with the read/write head aperture closest to the disk drive opening.

NOTE

The index hole aperture must be located on the left side of the disk center line as shown. If the hole is on the opposite side, turn the diskette over.

3. Insert the disk fully into the disk drive opening.

4. Press down on the top of the cover handle until the cover closes and remains in the latched position.

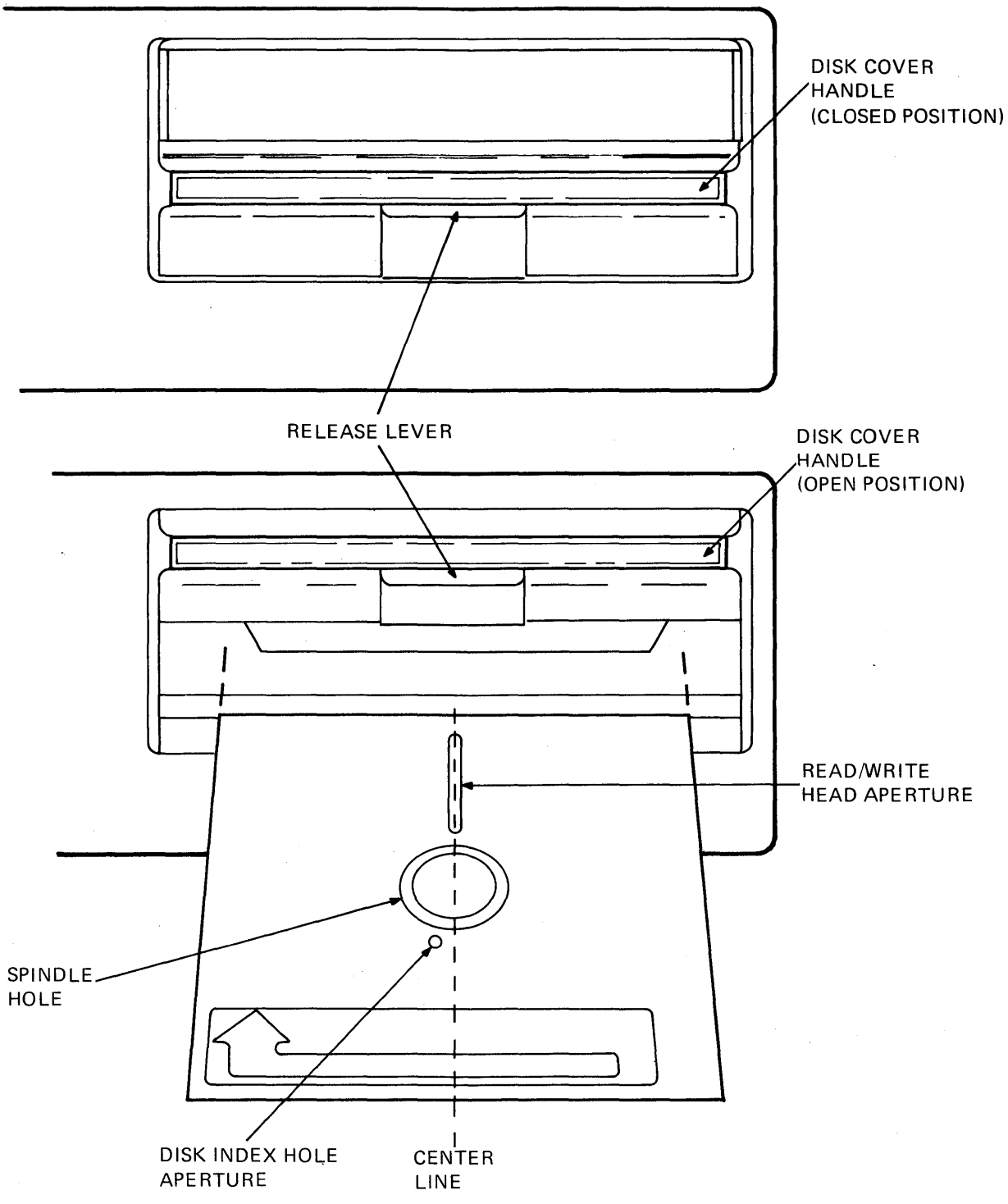


Figure 3-3 Loading the Disk into the Drive

5. To remove a disk, perform step 1, slide the disk gently from the drive unit and close the cover as described in step 4.

3.3 TEST PROCEDURES

The following procedures initiate the self-test diagnostic programs stored within ROM memory of the PDT-11/150. These procedures verify the correct operation of the disk drive and logical components within the unit. When the diagnostic tests have been successfully completed, the PDT-11/150 system exerciser program (CVKDAB0), contained on disk, may be initiated to further evaluate the performance of the unit.

NOTE

The PDT-11/150 system exerciser disk (CVKDAB0) can be ordered through your local DIGITAL sales office. The ordering designations are as follows:

Flexible Disk and Listing – ZJV03-RY
Flexible Disk only – ZJV03-PY
Listing only – ZJV03-RZ

3.3.1 Preliminary Set-Up

Prior to initiating the self-test procedure, ensure that the following conditions exist.

1. The ac power is properly applied.

2. The console device and terminals are properly connected to the PDT-11/150 (Paragraph 2.2.2) and to the ac power.

3. The function control switches (Table 3-3) are set to the positions indicated.

4. The ac power switch (Figure 2-3) on the rear panel of the unit is in the OFF (0) position.

5. The mode switch (Figure 2-3) on the rear panel is in the TEST position (down).

6. No blank or programmed disks are installed in the drive(s).

3.3.2 Optional Loopback Connector

The self-test procedures and system exerciser program include the facility for testing serial data transfers through the standard EIA connectors (except the console) and the Cluster EIA connectors. The loopback connector assembly is available as an option (DEC No. 70-16464) and must be attached to the connectors on the rear panel as shown in Figure 3-4. Remove all terminal cable connectors on the rear panel except the console terminal.

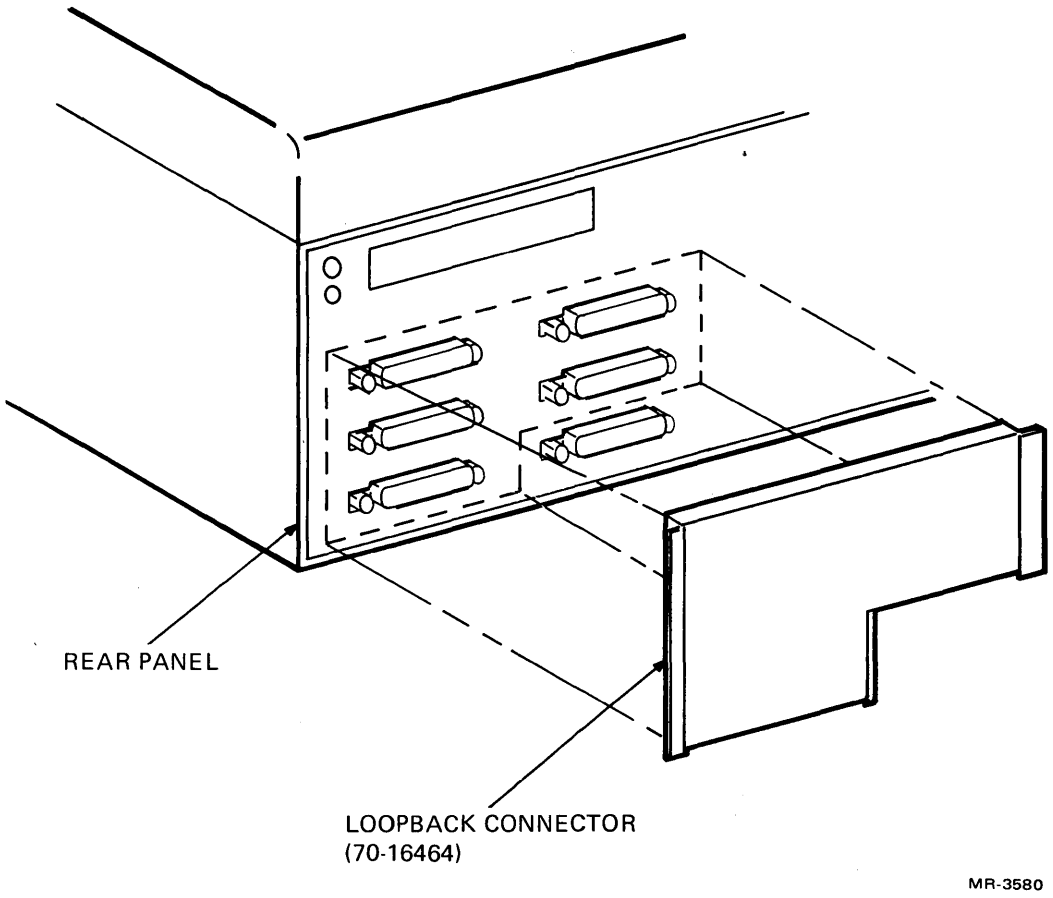


Figure 3-4 Loopback Connector Installation

3.3.3 Self-Test Procedures

Perform the following procedures in the sequence indicated. If a failure is detected during the performance of this test, one or more of the following events will take place.

1. The error indicators (1) on the front panel will light.
2. An improper response to the test procedure will occur.
3. No response will occur when a response is indicated by the test procedure.

If the self-test diagnostic does not run successfully, repeat the procedure for a minimum of three times. The function control switches must be set to the positions indicated in Table 3-3.

1. Set the ac power switch to the ON (1) position.

NOTE

All indicators on the front panel, except the RUN indicator, will light initially when the ac power is applied. This confirms that the indicators are operative.

2. The power indicator on the front panel will remain lighted.

3. When the (2) indicator on the front panel remains lighted, press the @ symbol key twice on the console terminal keyboard.

NOTE

Some terminal keyboards may require that the SHIFT key be pressed when typing the two @ symbols.

4. The (2) indicator will be extinguished. This procedure establishes the baud rate of the PDT-11/150 to be compatible with the console terminal. The console terminal will respond by displaying the following message:

SCRATCH FLOPPY INSTALLED?

5. Open the front cover of the disk drive and insert a scratch disk. Refer to Paragraph 3.2.1 for disk insertion. In a dual drive unit, insert a scratch disk in each drive.

NOTE

Scratch disks are preformatted blank disks without recorded data or disks with data no longer required.

6. Type Y on the console terminal when the disks are properly installed. This indicates a yes to the question in step 4.

NOTE

This initiates the read/write test of the disk. The disk controller module will write and read information from selected tracks. In a dual disk drive unit, disk 0 will be exercised first followed by disk 1. Allow approximately 2 minutes for the complete disk test.

7. If N is typed to indicate no, the disk drive exercise part of the self-test will not be performed. The console terminal will respond by displaying the following message:

EIA LOOPBACK TEST?

8. To run the EIA loopback test, the loopback connector assembly must be installed on the rear panel (Paragraph 3.3.2). Disconnect all terminal cable connectors from the rear panel except for the console terminal and attach the loopback connector. Type Y indicating yes on the console keyboard after the connector is attached. Type N indicating no if the loopback test is not desired.

9. After successful completion of this test, the console terminal will respond by displaying the following message:

XXXXXX (the six digits can be of any value)
@

10. To initiate the LSI-11 microprocessor test and RAM module test, set the mode switch to the RESET position and release to the NORMAL position.

11. When the (2) indicator on the front panel remains lighted, press the @ symbol key twice on the console terminal.

NOTE

Some terminal keyboards may require that the SHIFT key be pressed when typing the @ symbols.

12. The (2) light will be extinguished and the RUN indicator will light. After a short delay, the following message will be displayed on the console terminal.

```
NO BOOT ON VOLUME
TYPE START UNIT NUMBER (0 OR 1):
```

13. The PDT-11/150 has successfully completed the self-test diagnostic. If it is desired to load a program disk or system exerciser disk, remove the scratch disk and insert the appropriate programmed disk into drive 0 or 1.

NOTE

In a dual disk drive unit, the programmed disk may be inserted into either drive 0 or 1 and the scratch disk previously inserted can remain installed in the other disk drive.

3.3.4 Loading the System Exerciser Program

To continue the diagnostic testing of the unit, perform the following procedures immediately following the successful completion of the self-test.

NOTE

Switch S1-2 (Table 3-3) must be set to the OFF position to enable the line time clock before performing the system exerciser program.

1. Insert the PDT-11/150 system exerciser disk (CVKDAB0) into disk drive 0 or 1.

2. On the console keyboard, type the number of the disk drive where the disk is located.

```
(0 or 1)
```

3. The program will be entered and the console will display the identification of the disk program as follows.

```
CVKDAB PDT-11/150 SYSTEM EXERCISER

SWR = 000000 NEW =
```

4. Select the switch register SWR functions desired from the following list and add the content values for each function.

Content	Function
100000	Halt on error
20000	Inhibit error type outs
10000	Enable performance reports
2000	Bell on error

5. Enter the sum of the content values on the console keyboard and press the RETURN key. If the current value (000000) is desired, press only the RETURN key.

NOTE
The content value of 10000 must be entered to permit a display of the status of each test being performed.

Example:

To select performance report and bell on error, add the following values.

Enable performance reports	10000
Bell on error	2000
Content sum	012000

6. The console terminal will then display a message similar to the following.

DEVM = 000017 NEW =

7. The device map (DEVM) allows the selection of the system exerciser tests to be compatible with user requirements and system configuration. Select the tests desired from Table 3-4 by adding the content values.

a. A content value of DEVM = 000000 will exercise all configurations in external loopback mode.

b. Any content sum having the two least significant octal digits less than 17 requires installation of the loopback connector assembly on the rear panel (Paragraph 3.3.2).

DEVM = XXXX16 (or less)

c. The console connector will not be tested.

Example: A single disk drive unit has devices attached to all standard EIA connectors and one terminal attached to the Cluster terminal no. 1 connector. Perform all tests on external loopback.

Delete	Cluster terminal no. 3 test	40000
Delete	Cluster terminal no. 2 test	20000
Delete	Disk drive 1 test	1000
	Content sum	061000

8. Remove all device cables from the rear panel except the console cable and install the loopback connector.

9. Enter the sum of the content values on the console terminal keyboard and press the RETURN key. If no value is entered and the RETURN key is pressed, the group 2 options (internal loopback) will be selected by the current value of DEVM = 000017.

Table 3-4 Device Map Options (DEVM)

Group	Contents	Function
1	000000	Selects the following tests: External loopback for all three Cluster terminals External loopback for standard terminals (modem and printer) Asynchronous and synchronous testing of the modem Disk drive 0 and 1 Internal clock
	100000	Delete printer test
	40000	Delete Cluster terminal no. 3 test
	20000	Delete Cluster terminal no. 2 test
	10000	Delete Cluster terminal no. 1 test
	4000	Delete ASYNC modem test
	2000	Delete SYNC modem test
	1000	Delete disk drive 1 test
	400	Delete drive 0 test
	200	Delete clock test
2	10	Internal loopback for modem USART
	4	Internal loopback for Cluster terminal no. 1 USART
	2	Internal loopback for Cluster terminal no. 1 USART
	1	Internal loopback for Cluster terminal no. 1 USART

10. The console will display a message similar to the following.

```
30K MEMORY PRESENT
PRINTER NOT PRESENT

INSERT SCRATCH DISKS, TYPE 'P' FOR NORMAL TESTING
'240G' FOR NORMAL RESTARTS
'250G' TO COPY SYS EXERCISER DISK
'260G' FOR COMPATABILITY PASS 1: WRITE
'270G' FOR COMPATABILITY PASS 2: READ
003706
XXXXXX
@
```

11. Remove the system exerciser disk from disk drive 0 and insert a scratch disk in the drive(s) to be tested.

12. To start the normal program, type "P" on the console terminal keyboard. The exerciser will begin testing and the results of each test will be displayed on the console terminal. At the end of each pass, the console will display a message similar to the following:

END PASS #	1	TOTAL ERRORS:	0
		TOTAL SOFT ERRORS:	0
		TOTAL ERRORS THIS PASS:	0
		SOFT ERRORS THIS PASS:	0

13. Allow approximately 1/2 hour for the entire test to be completed. If an error is encountered during the test and a halt on error function has been selected in step 4, type the following to restart the program after the last error.

    240G

NOTE
Some terminals may require that the SHIFT key be pressed while typing the G.

14. To continue the test from where the error was detected, type "P" on the console keyboard.

15. To alter the content of the SWR while the exerciser program is operating,

    Press CTRL key while typing G.

16. The program will halt and the console will display the current SWR value.

    SWR = XXXXXX NEW =
    (XXXXXX = previous value selected)

17. Enter the new SWR content value as described in step 5 or press the RETURN key to retain the current content value. The program will resume when RETURN is pressed.

18. To alter the content of the DEVM while the exerciser program is operating, type the following on the console.

    Press CTRL key while typing G.

19. The program will halt and the console will display the current SWR value.

    SWR = 012000 NEW =
    (XXXXXX = previous value selected)

20. Type the following on the console keyboard.

    Press CTRL key while typing "C".

21. The console will display the current DEVM value.

    DEVM = XXXXXX NEW =
    (XXXXXX = previous value selected)

22. Enter the new DEVM content value as described in step 9. When the RETURN key is pressed the program will resume.

3.3.4.1 Exerciser Compatability Test – The system exerciser program includes a test to verify that data writen on a disk by one disk drive can be read by another disk drive. In a dual disk drive unit the disks can be exchanged between drives. In a single drive unit, disks may be exchanged between units.

1. The compatibility test is selected at step 10 of the system exerciser test (Paragraph 3.3.4) by typing the following.

   260G

   NOTE
   Some terminals may require that the SHIFT key be pressed while typing G.

   Data will be written on all tracks of disk drive 0 and 1 if both disk drives are selected by the DEVM (step 9 of Paragraph 3.3.4).

2. At the end of pass number 1 the console will print the following message. Allow approximately 1/2 hour for the entire pass to be completed.

   ```
   END PASS #      1          TOTAL ERRORS:              0
                              TOTAL SOFT ERRORS:         0

                              TOTAL ERRORS THIS PASS:    0
                              SOFT ERRORS THIS PASS:     0

   COMPATABILITY PASS 1 (WRITE) DONE
   DO 'P' FOR PASS 2 (READ)
   010236
   ```

3. If the disks are exchanged between drive 0 and 1 of the same PDT-11/150 unit, proceed as follows to initiate pass 2 (read).

   Type "P" on the console.

4. The console will display a message similar to the following.

   ```
   END PASS #      2          TOTAL ERRORS:              0
                              TOTAL SOFT ERRORS:         0

                              TOTAL ERRORS THIS PASS:    0
                              SOFT ERRORS THIS PASS:     0
   ```

5. If the disks are exchanged between drives in different PDT-11/150 units, each unit must have completed the self-test and system exerciser program to step 10 of Paragraph 3.3.4. Type the following on the console of the unit where the disk will be tested.

   240G

6. The console will display a message similar to the message in step 4.

3.3.4.2 Copying the System Exerciser Disk – The PDT-11/150 system exerciser disk program can be duplicated on a scratch disk by performing the following procedures.

1. The copy utility is selected at step 10 of Paragraph 3.3.4 by typing the following.

   250G

2. The console will display the following message.

   COPY DX0 TO DX1
   INSERT SCRATCH FLOPPY IN DX1. TYPE "P" TO PROCEED

3. Insert the scratch disk into disk drive 1.

4. Type "P" on the console keyboard.

   NOTE
   Allow approximately 1.5 minutes for transfer.

5. The console will display the following message.

   DONE . . . TYPE "P" TO DO AGAIN OR 240G FOR NORMAL TESTING

6. To reproduce another system exerciser disk, remove the disk in DX1 and replace it with another scratch disk.

7. Type "P" on the console keyboard.

8. To return to the system exerciser program, type 240G on the console keyboard after receiving the message in step 5.

3.3.5 Loading a System Program

A program disk can be initially loaded into the PDT-11/150 by the following procedures.

1. Check to ensure that no disks are installed in the disk drive(s).

2. Set the mode switch on the rear panel to the NORMAL position (center).

3. Apply power to the console device.

4. Set the power switch on the rear panel to the ON (1) position.

   NOTE
   All indicators on the front panel, except the RUN indicator, will light momentarily when the ac power is applied. This confirms that those indicators are operative.

5. The POWER indicator will remain lighted and the (2) indicator will again light.

6. Insert the program disk in disk drive 0. In a dual disk unit, disk drive 0 is located on top of disk drive 1.

7. If the application program requires data storage on disk drive 1, insert a preformatted scratch disk into disk drive 1 of the dual drive unit.

8. Press the @ symbol twice on the console device.

NOTE
Some consoles may require that the SHIFT key be pressed while typing the @ symbols.

9. The console will display the program title and contents for user selection.

3.3.6 Changing a System Program

If the PDT-11/150 is presently operating and it is desired to change the program disk, perform the following procedures.

1. Remove the disk in disk drive 0 and insert the program disk to be loaded.

2. Set the mode switch to the RESET position and release (momentary) to NORMAL position.

3. When the (2) indicator on the front panel lights, press the @ symbol key twice on the console keyboard.

NOTE
Some consoles may require that the SHIFT key be pressed while typing the @ symbols.

4. The console will display the program title and contents for user selection.

CHAPTER 4
OPTION INSTALLATION

Several options are available for the PDT-11/150 to expand the capability of a unit. These options include three configurations of RAM modules, an additional disk drive unit and a Cluster EIA-level converter kit. Table 1-2 lists and describes the available options. The installation of these options should only be performed by qualified service personnel.

4.1 RAM MODULE OPTION

Perform the following procedure to remove the existing RAM module. The RAM module is part of the TIM assembly and is located under the top cover assembly of the unit.

4.1.1 RAM Module Removal

1. Disconnect the ac power cord from the recessed receptable on the rear panel of the drive 0 enclosure (Figure 4-1).

2. Remove and retain the two cover release screws and washers (6-32) behind the access holes located at the top left and right side of the rear panel.

3. Gently slide the top cover assembly toward the front of the unit approximately 1.27 cm (0.5 in) to disengage the cover from the slotted tabs on the drive 0 enclosure. Lift the cover vertically and remove.

4. Disconnect the G2 flat cable connector P1 from the socket J4 on the Peripheral module.

> **NOTE**
> **Insert a flat screwdriver blade into the slot at each end between the cable connector and socket and carefully twist the blade to separate the connector from the socket.**

5. Disconnect the G3 flat cable connector P1 (if included) from the DIP socket J3 on the Peripheral module. See NOTE in step 4.

6. Pull up to release the nylon latches in the module hinge brackets located on the left and right side of the TIM assembly.

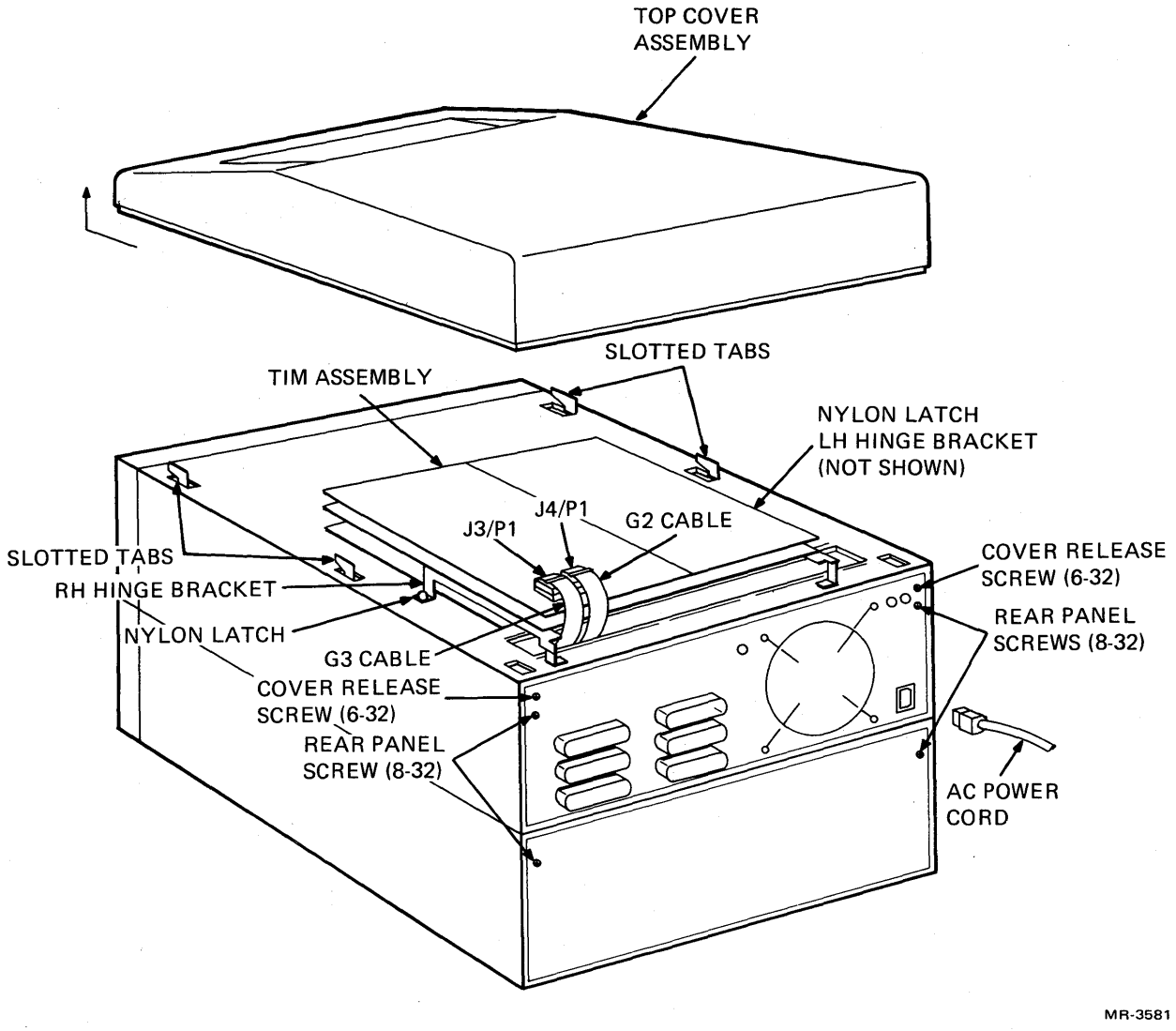


Figure 4-1 Top Cover and TIM Assembly Removal and Replacement

7. Raise the front of the TIM assembly until the assembly remains in the vertical position (Figure 4-2).

8. Carefully slide the slot of the RFI shield away from cable G1 and fold to position shown.

9. Disconnect the G1 flat cable connector P1 from J5 on the Intelligence module. See NOTE in step 4.

10. Disconnect the power supply cable connector P3 from connectors J6, J7, and J8 on the Intelligence module.

NOTE
The pins of J6, J7, and J8 insert into connector P3.

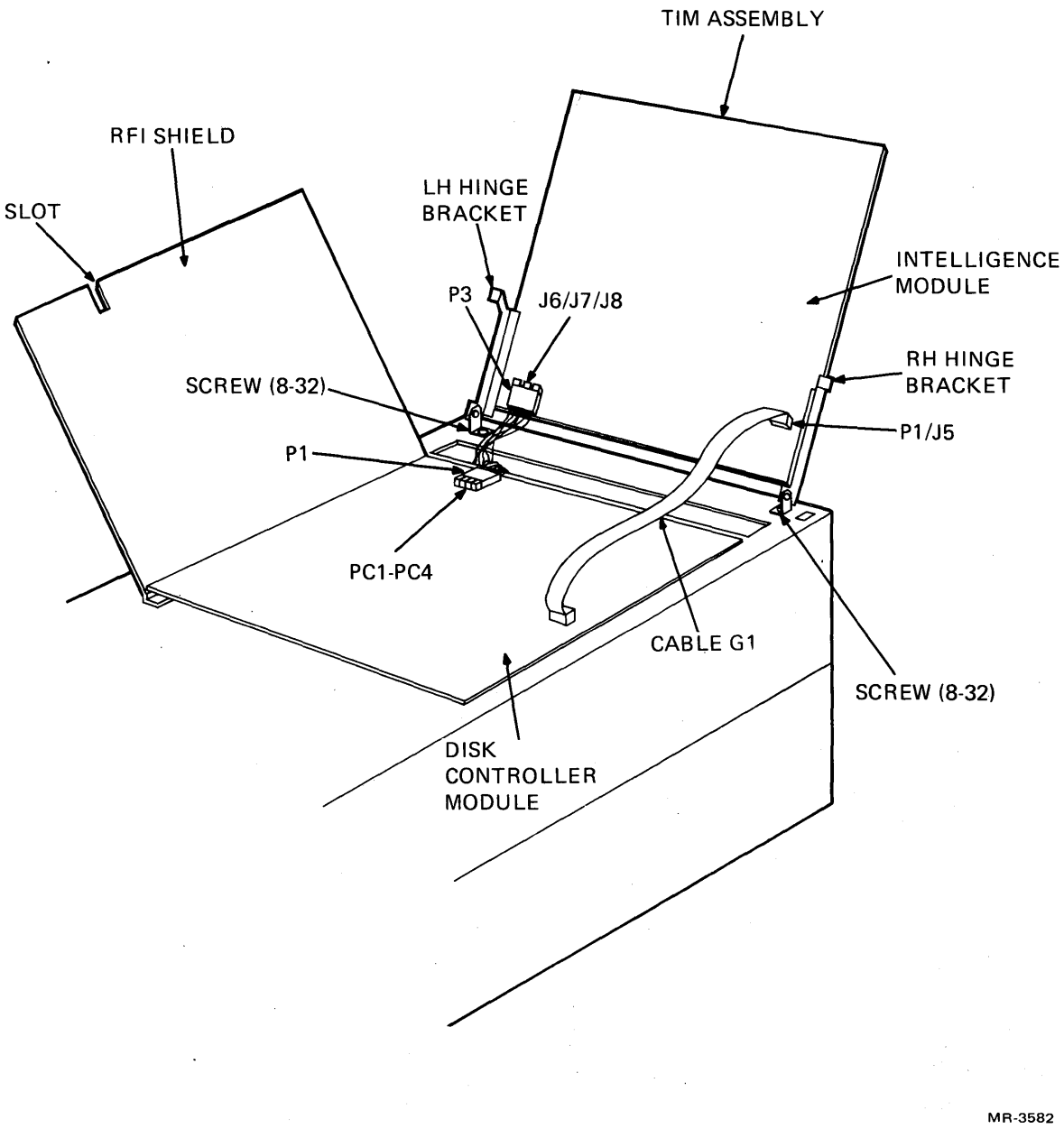


Figure 4-2 TIM Assembly Connections

11. Remove and retain the screws (8-32) used to secure the left and right hinge bracket to the top of the disk 0 enclosure.

12. Gently place the TIM assembly on a clean, flat surface with the component side of the Intelligence module facing up.

13. Remove and retain the two kepnuts (4-40) used to secure the left hinge bracket to the TIM assembly. Remove the hinge bracket (Figure 4-3).

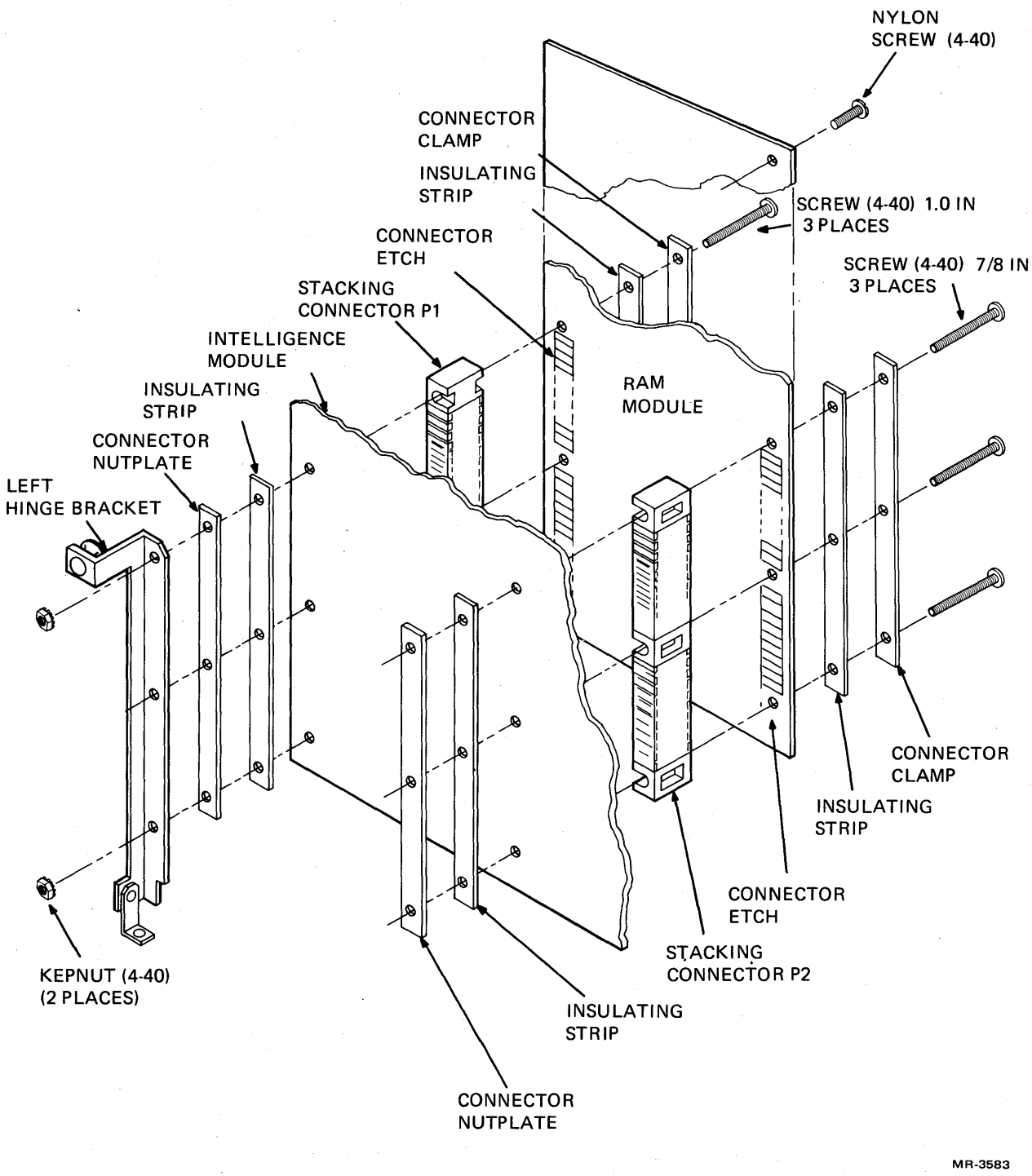


Figure 4-3 TIM Group, Assembly and Disassembly

14. Turn over the TIM assembly so that the component side of the RAM module is facing up.

15. Remove and retain the (4-40) nylon screw located at the front edge of the RAM module. This screw is mounted into a standoff between the two boards.

16. Remove and retain the three 1 in and three 7/8 in screws, (4-40) which are inserted through the two stacking connectors P1 and P2 and into the nutplates.

17. Remove and retain the two connector clamps and insulating strips located against the RAM module and the two insulating strips and nutplates located against the intelligence module.

18. Lift the RAM module away from the TIM assembly and retain the two stacking connectors P1 and P2.

NOTE
Use care when handling the stacking connectors to prevent damage to the connector contacts.

4.1.2 Bootstrap ROM Installation

The bootstrap ROM 0 and ROM 1 integrated circuits (ICs) are supplied separately and must be installed on the RAM module. To prevent damage to the ICs, perform the following procedure.

1. Place the RAM module on a clean surface, with the component side facing up.

2. Unpack the ROMs but do not remove from the conductive foam.

3. Gently press the conductive foam against the surface of the module.

4. Remove the ROMs from the conductive foam by grasping the body of the IC at the sides adjacent to the pins.

5. Inspect the pins to ensure that they are properly aligned, parallel and at a 90° angle with the body of the IC (Figure 4-4).

6. If any pins are not parallel, straighen each pin using needlenose pliers, making contact with only one pin a time.

7. If a row of pins is not at the proper angle, gently press the pins against a desk or table until all pins in the row are aligned.

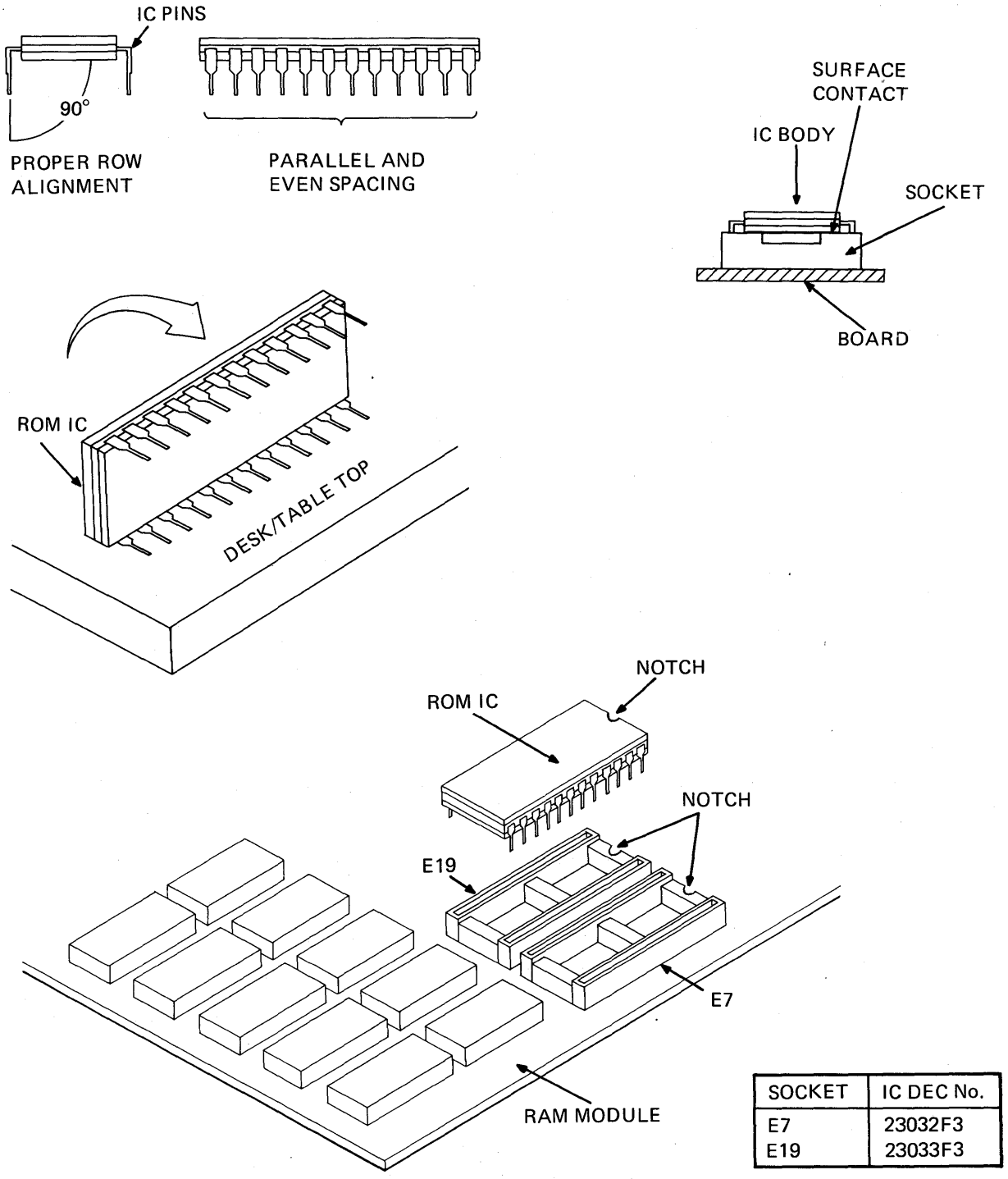
8. Locate the notch at the end of the IC body and at the end of the IC socket mounted on the module.

9. With the notches positioned at the same end, carefully insert the pins into the socket slots.

10. Insert the IC evenly into the socket by pressing on the top surface of the body.

CAUTION
If excessive resistance occurs, remove the IC and check the pin alignment.

11. When properly installed, the body of the IC should make contact with the inner edges of the socket.



SOCKET	IC DEC No.
E7	23032F3
E19	23033F3

Figure 4-4 RAM Module, PROM Installation

4.1.3 RAM Module Installation

1. Install the bootstrap ROMs on the RAM module (Paragraph 4.1.2).

2. Insert the screw (4-40) 1 inch, shown in Figure 4-3, through the end hole in a connector clamp, insulating strip and through the corresponding hole in the RAM module.

3. Slide the stacking connector P1 onto the screw and insert the screw through the corresponding hole in the Intelligence module.

4. Slide the insulating strip onto the screw and align the end of the screw with the corresponding threaded hole in the nutplate.

5. Tighten the screw with fingers.

6. Insert the remaining two screws (4-40) 1 inch through the corresponding holes and into the nutplate.

7. Perform steps 2 through 5, inserting the three screws (4-40) 7/8 inch on the opposite side of the RAM module and into stacking connector P2.

8. Align the RAM module with the Intelligence module and tighten all six screws (4-40).

NOTE

Use adequate amount of torque on the screws (4-40) to ensure proper pressure of the stacking connector contacts onto the module etch.

9. Replace the nylon (4-40) screw removed in step 15.

NOTE

The steps referenced in 9 through 20 refer to Paragraph 4.1.1.

10. Place the hinged bracket, removed in step 13, over the screw threads and replace the two (4-40) kepnuts removed in step 13. Tighten with a socket driver.

11. Remount the TIM assembly onto the disk drive 0 enclosure by replacing the two screws (8-32) previously removed in step 11.

12. Connect the G1 cable connector P1, removed in step 9, into the socket J5 (Figure 4-2).

NOTE

Check to ensure that all pins on P1 are straight and evenly spaced before inserting into the DIP socket. Using even pressure, carefully press the connectors together. Do not allow the ribbon cable to twist between connectors.

13. Fold the RFI shield down over the disk controller module and carefully slide the cable into the slot in the shield.

14. Connect the power supply cable connector removed in step 10 of Paragraph 4.1.1.

15. Lower the front of the TIM module assembly to the normal position and press the nylon latches released in step 6 to secure the assembly to the disk drive 0 enclosure.

16. Connect the G3 ribbon cable connector P1 previously removed in step 5. See NOTE in step 12 of this paragraph.

17. Connect the G2 ribbon cable connector P1 previously removed in step 4. See NOTE in step 12 of this paragraph.

18. Gently place the top cover assembly on the drive 0 enclosure so that the front of the cover extends over the front of the drive 0 enclosure approximately 1.27 cm (0.5 in).

19. Slide the top cover toward the rear of the unit to engage the slotted tabs.

20. Replace the two (6-32) screws and washers removed in step 2.

4.2 FLOPPY DISK DRIVE ASSEMBLIES

An optional disk drive can be added to a single disk drive PDT-11/150 unit to double the disk storage capacity. The RXT11-AA option is provided for the 60 Hz units and the RXT11-AC option for 50 Hz units. The optional disk drive assemblies mount below the existing disk drive unit.

To attach the disk drive option, perform the following procedure.

1. Disconnect the ac power cord from the recessed receptacle on the rear panel (Figure 4-1).

2. Disconnect any terminal cables attached to the rear panel.

NOTE

The cable connectors may be secured to the rear panel by two (4-40) screws located on each side of the connector.

3. Lift the rear of the PDT-11/150 chassis and remove and retain the two (8-32) screws located at the outside edges of the bottom panel, at the rear of the unit (Figure 4-5).

4. Slide the bottom panel toward the rear of the unit approximately 1.27 cm (0.5 in) to disengage the slotted tabs located at the center and front of the bottom panel.

5. Lower the bottom panel and remove.

6. Place the PDT-11/150 on top of the disk drive option enclosure so that the slotted tabs located at the center and front of the option chassis protrude through the slots at the bottom edges of the PDT-11/150 unit enclosure.

7. Slide the PDT-11/150 unit toward the rear of the option until the tabs are engaged.

8. Remove and retain the two (8-32) screws used to secure the rear panel to the disk drive 1 enclosure (Figure 4-1). Remove the rear panel.

9. Remove and retain the two (8-32) screws used to secure the rear panel to the disk drive 0 enclosure.

10. Allow the top edge of the panel to pivot away from the top edge of the enclosure and lift the panel vertically to disengage the two tabs on the bottom edge of the panel from the slots in the enclosure.

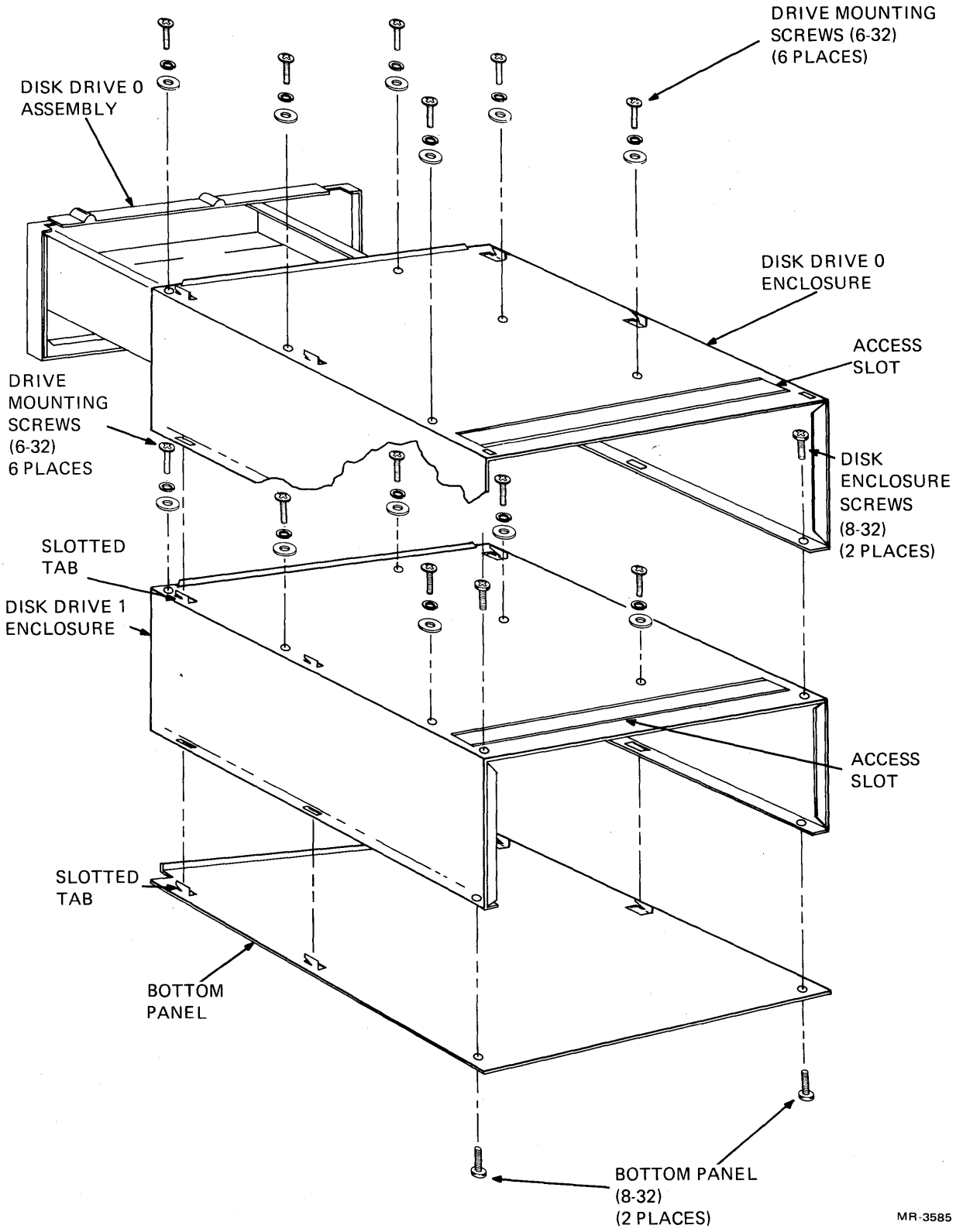


Figure 4-5 Disk Drive 1 Enclosure Mounting

11. Disconnect the flat cable connector P2 from the socket J4 on the Standard EIA Converter module (Figure 4-6).

NOTE

Insert a flat screwdriver blade into the slot at each end between the cable connector and socket. Carefully twist the blade to separate the connector from the socket.

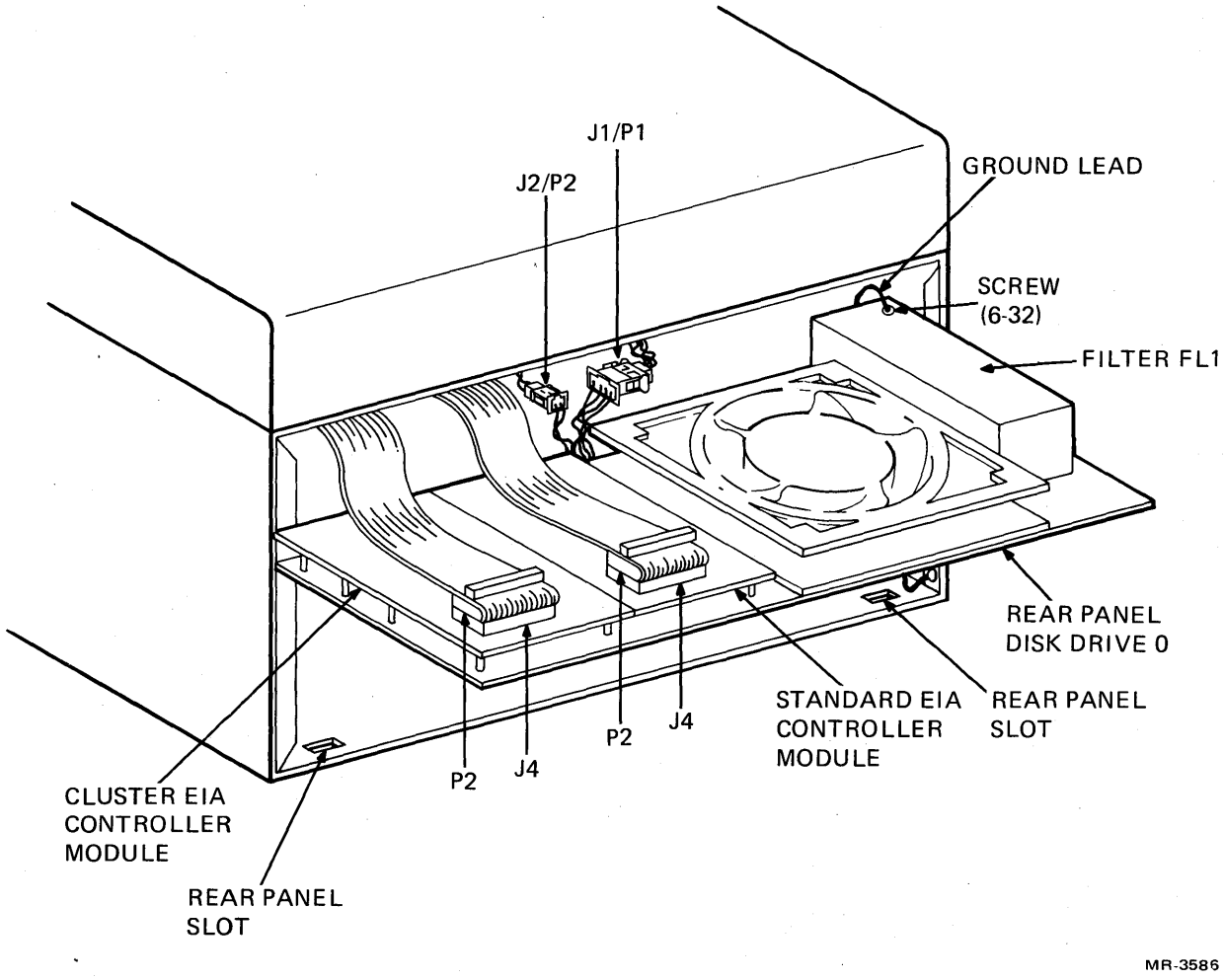


Figure 4-6 Rear Panel Removal, Disk Drive 0 Enclosure

12. If the Cluster EIA Converter module is included on the rear panel, disconnect the ribbon cable connector P2 from J4 as described in step 11.

13. Disconnect the ac power cable to the power supply from the inside of the rear panel by separating P2 from J2.

14. Disconnect the ac power cable from the rear panel by separating connector J1 and P1.

15. Disconnect the ground lead attached to filter FL1 on the rear panel by removing the screw (6-32).

16. Remove the rear panel.

17. Remove the top cover of the unit following steps 2 and 3 of Paragraph 4.1.1.

18. Locate the two disk enclosure screws (8-32) supplied with the disk drive 1 option.

19. Using a long shank screwdriver, install the (8-32) screws through the access slot at the rear of the PDT-11/150 and into the mating hole (Figure 4-5). The holes are located at the left and right side of the access slot in the top of the disk drive 1 enclosure.

20. Route the ground lead attached to disk drive 1 up through the access slot in the disk drive 0 enclosure (Figure 4-7).

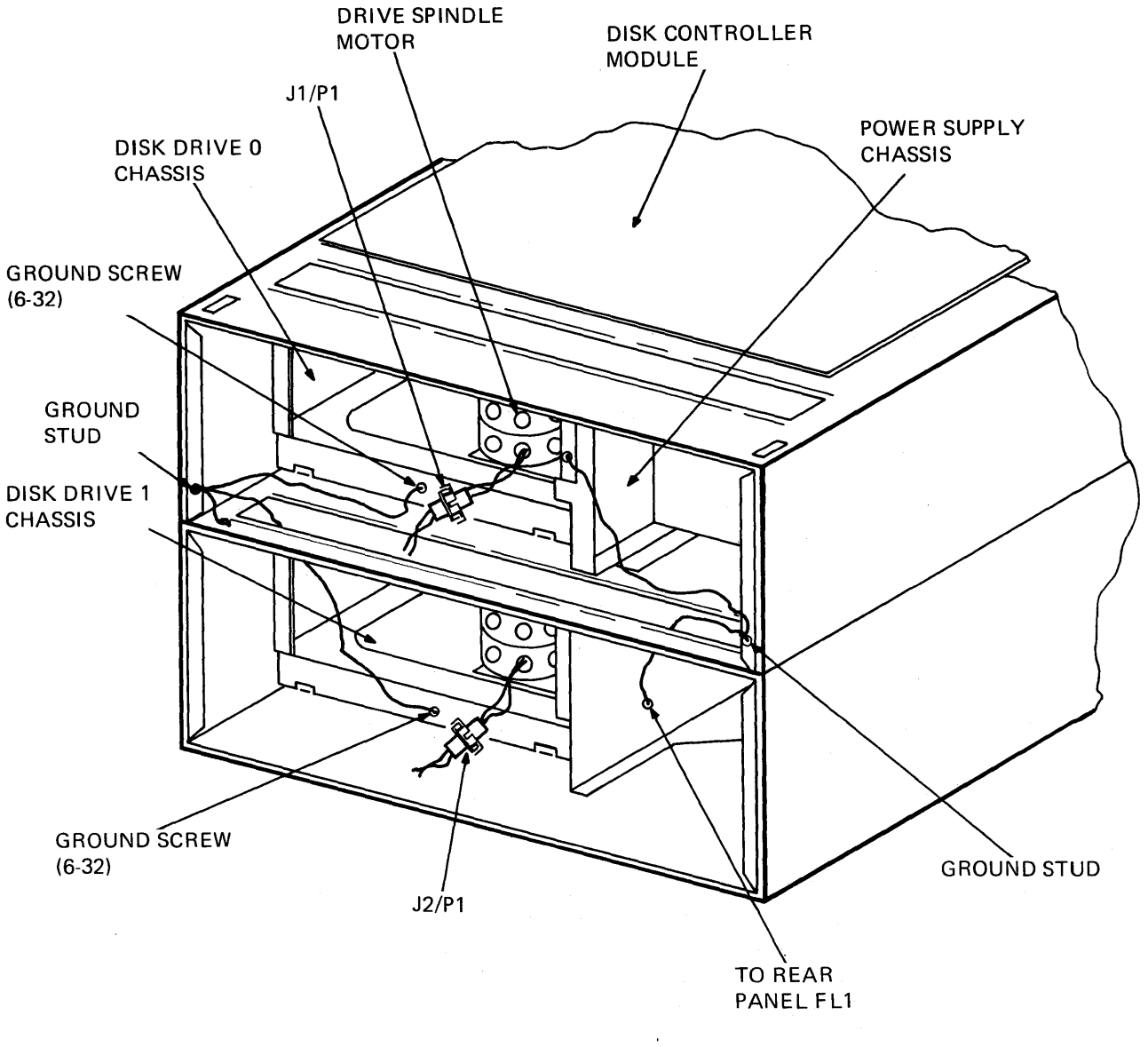


Figure 4-7 Ground Leads and ac Cable Routing

21. Remove the kepnut (8-32) from the ground stud on the left rear of the disk drive 0 enclosure. Attach the ground lead to the lug and replace the kepnut.

22. Connect the ac spindle motor cable connector P1 to cable connector J2.

23. Pull up on the nylon latches of the module hinge brackets located at the left and right side of the TIM assembly on the top of the disk drive 0 enclosure (Figure 4-1).

24. Raise the front of the TIM assembly until the assembly remains in the vertical position. Slide the RFI shield slot away from cable G1 and fold the shield to the position shown (Figure 4-2).

25. Release the Disk Controller module by carefully compressing the tabs on the nylon standoffs used to secure the module to the top of the disk drive 0 enclosure. When a tab is compressed, raise the module to release it from the standoff.

26. Locate cable connectors P3 and P4 from the disk drive 1 assembly and route the connector cables through the large cable routing hole in the disk drive 1 and disk drive 0 enclosure and through the rectangular slot in the disk controller module (Figure 4-8).

27. Align the mounting holes in the Disk Controller module over the standoff tabs and press the module down until the tabs are firmly engaged.

28. Connect P3 and P4 to the appropriate male connectors DIP3 and DIP4 on the Disk Controller module.

29. Locate the three female connectors P5, P6 and P7 which are attached by cable to the PC board mounted beneath the access slot at the rear of the disk drive 1 enclosure.

30. Route the cables through the access slot in the rear of the disk drive 0 enclosure and attach to the corresponding male connectors DIP5, DIP6 and DIP7 mounted at the rear of the Disk Controller module.

31. Fold the RFI shield down over the Disk Controller module and carefully slide the cable into the slot in the shield (Figure 4-2).

32. Lower the front of the TIM module assembly to the normal position and press the nylon latches to secure the assembly to the disk drive 0 enclosure (Figure 4-1).

33. Connect the rear panel ground lead previously removed in step 15.

34. Connect the ac cable connectors removed in step 13 and step 14.

35. Connect the flat cable connectors removed in step 11 and 12.

NOTE

Check to ensure that all pins are straight and evenly spaced before inserting into the socket. Carefully press the connectors together until fully seated. Do not allow the ribbon cable to twist between the connectors at each end.

36. Install the rear panel of the disk drive 0 enclosure using the hardware removed in step 9.

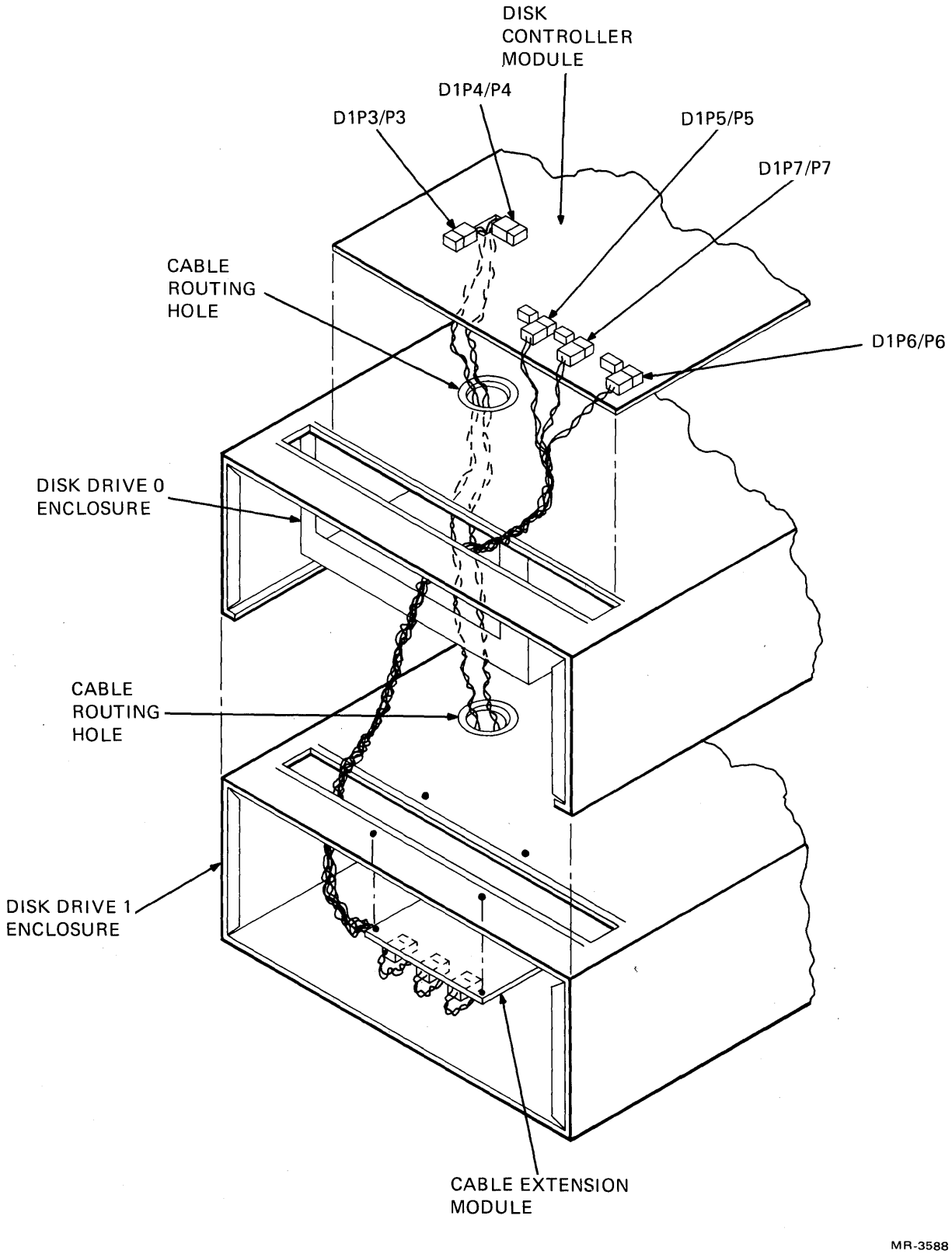


Figure 4-8 Disk Drive 1 Assembly, Cable Routing

37. Install the rear panel of the disk drive 1 enclosure using the hardware removed in step 8.

38. Install the top panel according to step 18, 19 and 20 of Paragraph 4.1.3.

4.3 EIA-LEVEL CONVERTER (CLUSTER OPTION)

The Cluster EIA-level converter kit option (DFT11-AB) enables the PDT-11/150 to operate with three additional serial line terminals. The option includes the Cluster EIA converter module, mounting hardware, a flat signal cable and three USARTS. The module mounts on the inside of the rear panel of the disk drive 0 enclosure.

To install the EIA-level converter option, perform the following procedures.

1. Remove the top cover assembly from the PDT-11/150 unit according to steps 1 through 4 of Paragraph 4.1.1.

2. Remove the rear panel of the disk drive 0 enclosure according to steps 9 through 11 and steps 13 through 16 of Paragraph 4.2.1.

3. From the inside of the rear panel, bend the two tabs upward on the plate covering the terminal no. 1 through no. 3 connector slots and remove the cover.

4. Locate the 1.27 cm (0.5 in) hex spacer supplied with the option and insert over the threaded (6-32) ground stud mounted to the inside of the rear panel (Figure 4-9).

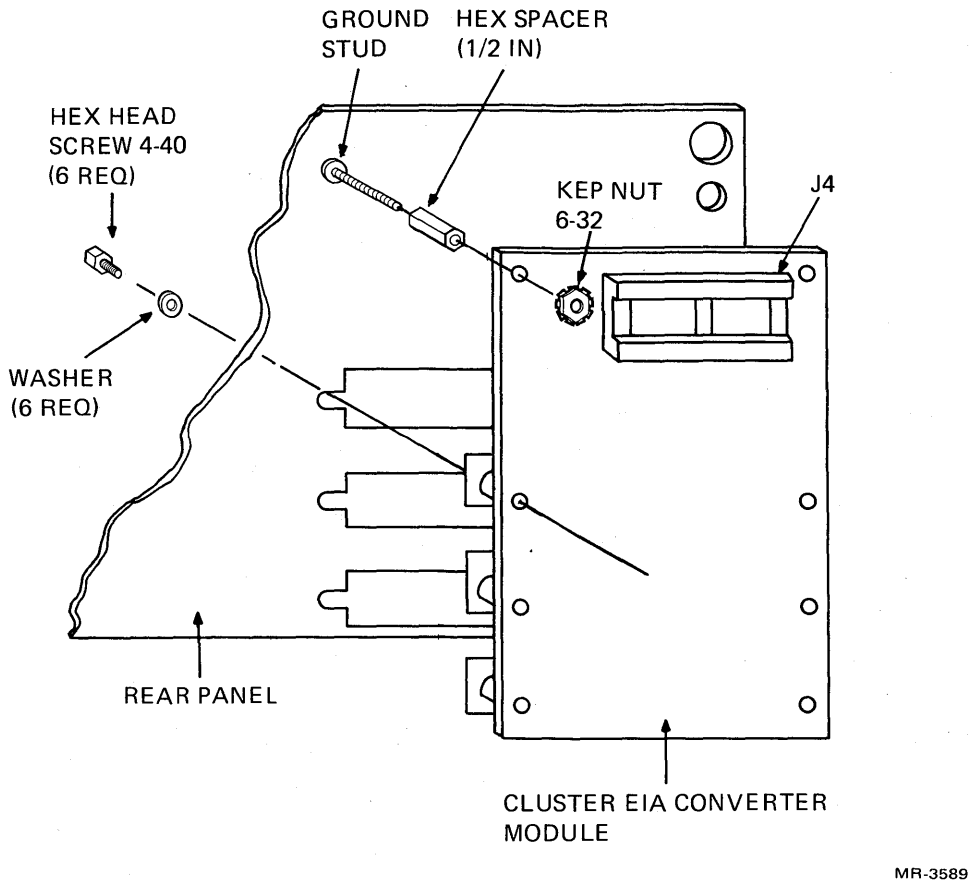


Figure 4-9 Cluster EIA Converter Module Mounting

5. Install the EIA-level converter module from the inside of the rear panel so that the three 25-pin connectors protrude through the terminal slots on the rear panel. The (6-32) ground stud will protrude through the large hole located at the top of the module.

6. Locate the six (4-40) hex head screws and six washers supplied with the option.

7. Place a washer over each screw thread and insert into the holes located on each side of the connector slots. Using a socket driver, tighten the six hex (4-40) screws.

8. Locate the kepnut (6-32) supplied with the option and install over the threaded ground stud. Tighten against the module ground etch.

9. Locate the flat cable assembly G3 supplied with the option and insert the male connector P2 into the female connector J4 located at the top edge of the Cluster EIA module. Insert the connector so that the cable is directed toward the bottom of the rear panel (Figure 4-10).

NOTE

Check to ensure all pins of the connector are straight and evenly spaced before inserting into the socket. Carefully, press the connectors together. Do not allow the ribbon cable to twist between connectors.

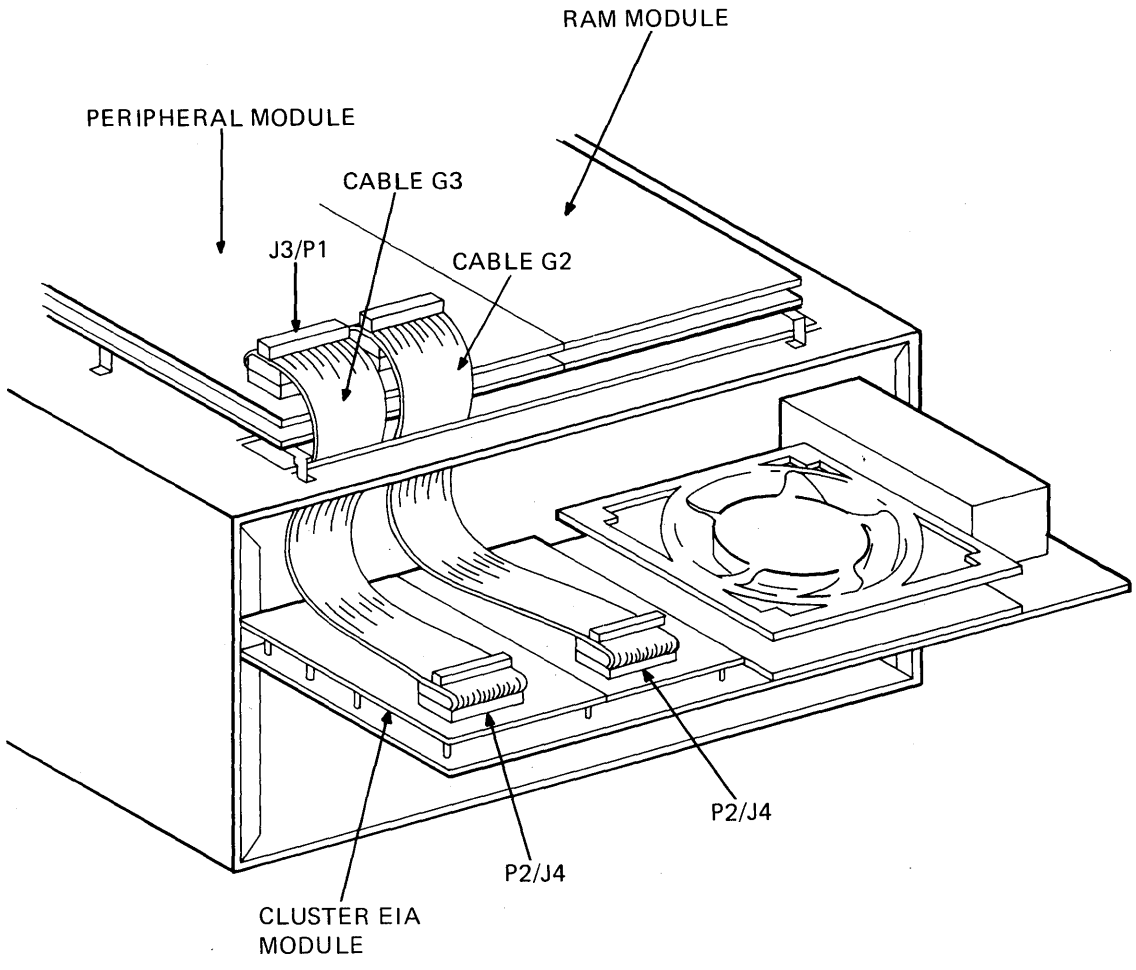


Figure 4-10 Cluster EIA Converter, Cable Routing

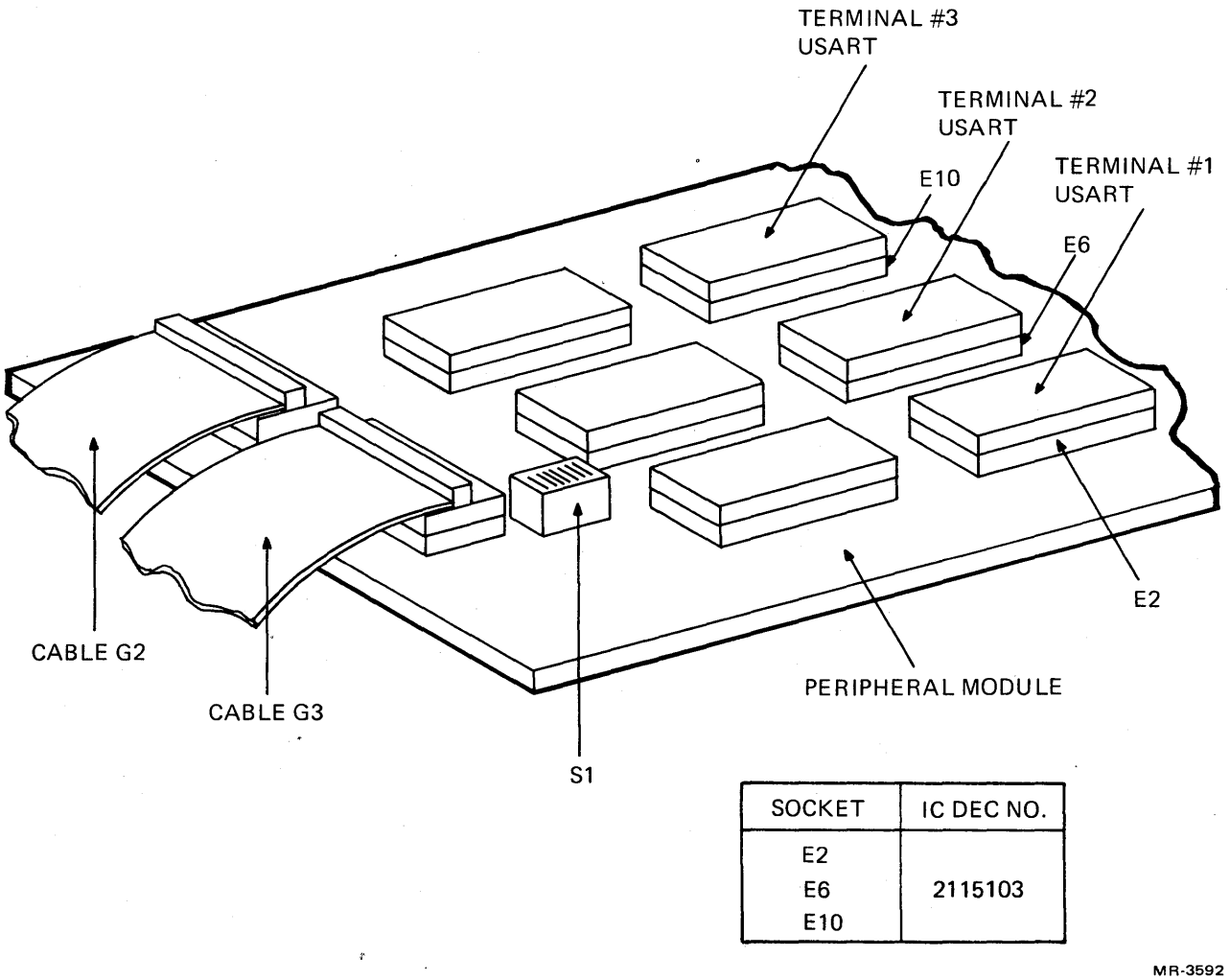
10. Route the cable up through the access slot located at the rear of the unit.

11. Connect the G2 flat cable connector P2 to connector J4 on the Standard EIA Converter module. See NOTE of step 9.

12. Install the rear panel to the disk drive 0 enclosure by performing steps 33, 34, and 36 of Paragraph 4.2.1.

13. Insert cable G3 connector P1 into J3 on the Peripheral module (Figure 4-1).

14. Locate the three USART integrated circuits supplied with the option and insert one into socket E2, E6 and E10 of the Peripheral module as shown in Figure 4-11.



SOCKET	IC DEC NO.
E2 E6 E10	2115103

Figure 4-11 Cluster EIA Module, USART Installation

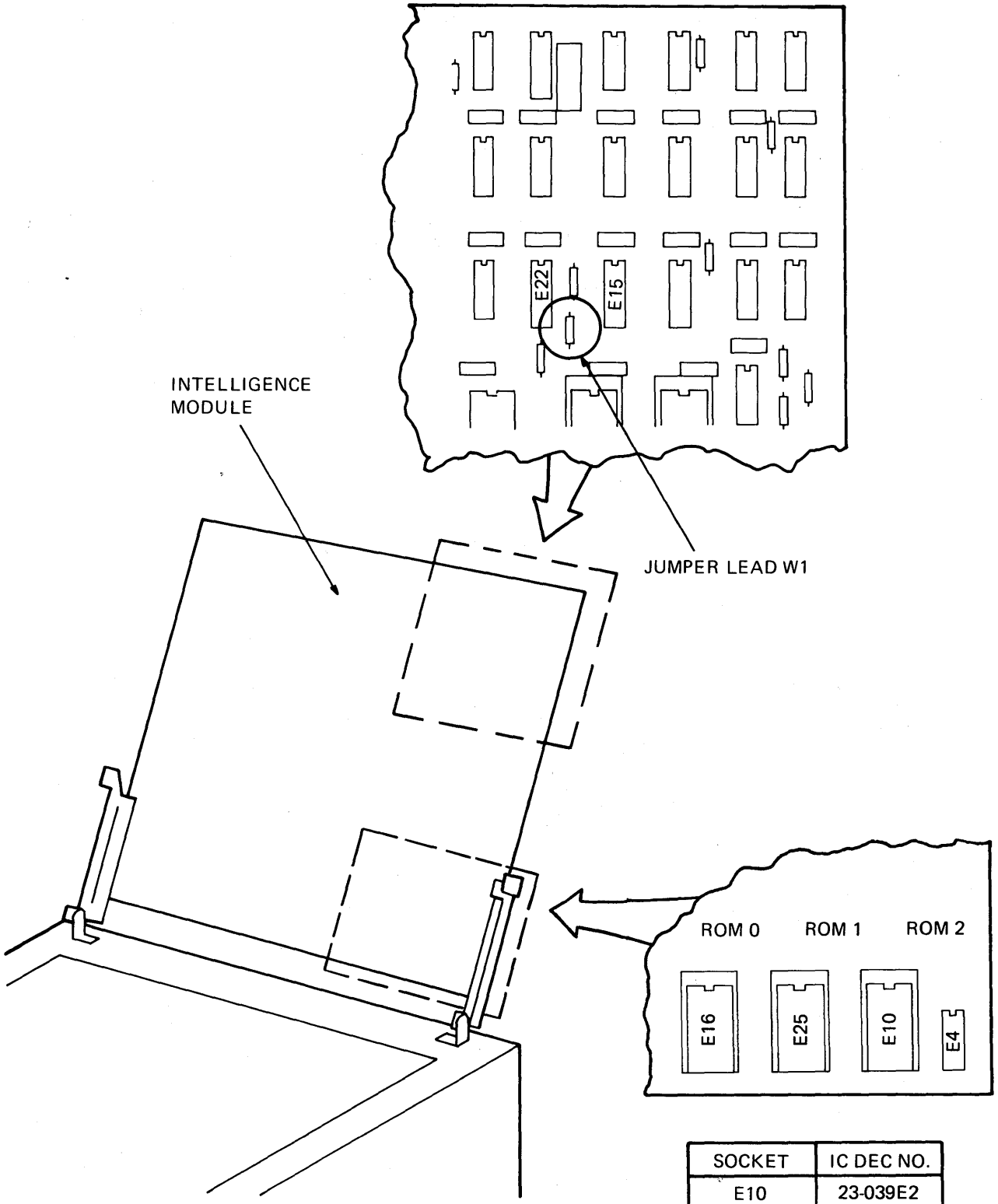
15. Pull up to release the nylon latches in the module hinge brackets located on the left and right side of the TIM assembly (Figure 4-1).

16. Raise the front of the TIM assembly to the position shown (Figure 4-12) and locate the W1 jumper lead.

17. Using a pair of wire cutters, remove the W1 jumper lead.

18. Lower the TIM assembly to the normal position and press the nylon latches, released in step 15, to secure the assembly to the disk drive 0 enclosure.

19. Install the top cover as described in steps 18 through 20 of Paragraph 4.1.3.



SOCKET	IC DEC NO.
E10	23-039E2
E16	23-043E2
E25	23-042E2

Figure 4-12 Intelligence Module, W1 Jumper Lead Location

CHAPTER 5
PROGRAMMING INFORMATION

This chapter describes the hardware characteristics of the PDT-11/150 and includes the addresses assigned to the internal registers and detailed description of the register bit functions and programming considerations.

User programs for the PDT-11/150 system can be developed using a DIGITAL PDP-11V03 microprocessor system or equivalent PDP-11 system. The PDP-11V03 contains a RXV11 dual flexible disk drive, and programs can be generated on a flexible disk for loading into the PDT-11/150.

The RT-11V3 operating software is used with the PDP-11 hardware to develop real-time application programs for the PDT-11/150 as shown in Figure 5-1. Refer to the DIGITAL *Microcomputer Processors* handbook for descriptions of the PDP-11V03 hardware and RT-11 operating system.

5.1 SYSTEM CHARACTERISTICS

The PDT-11/150 is an LSI-11 microprocessor-based system and is programmed using the same instruction set as the PDP-11V03. The memory assignments for the I/O page and user area are similar to standard PDP-11 systems with equivalent memory size. I/O page access time is approximately 90 μs. Any instruction addressed to the I/O page to write a byte of information will cause a dual transfer (read/write) and double the access time to 180 μs. For detailed hardware and software information relating to the LSI-11 microprocessor, refer to the DIGITAL *Microcomputer Processors* handbook.

The PDT-11/150 includes a parameter control register used to enable software control of the serial line devices. The system communicates externally with a maximum of six serial line devices and internally with a maximum of two flexible disks.

Each serial line device is interfaced to the PDT-11/150 through a USART and EIA-level converter. Data is transferred using programmed I/O instructions or through interrupt device routines.

When transmitting data to a device using the interrupt routines, the interrupt enable bit of the CSR associated with the device must be set prior to the transfer of data to the USART. If it is desired to end the data transmission, the interrupt enable bit must be cleared prior to the last data word transferred.

Console ODT commands are executed by the LSI-11 processor when the processor is in the HALT mode. These commands allow the operator to examine and alter the contents of memory and register locations through the console terminal. The halt condition is entered by pressing the BREAK key on the console keyboard when the mode switch on the rear panel is in the TEST position. If pressing the BREAK key does not cause the processor to enter the HALT mode, press the BREAK key again.

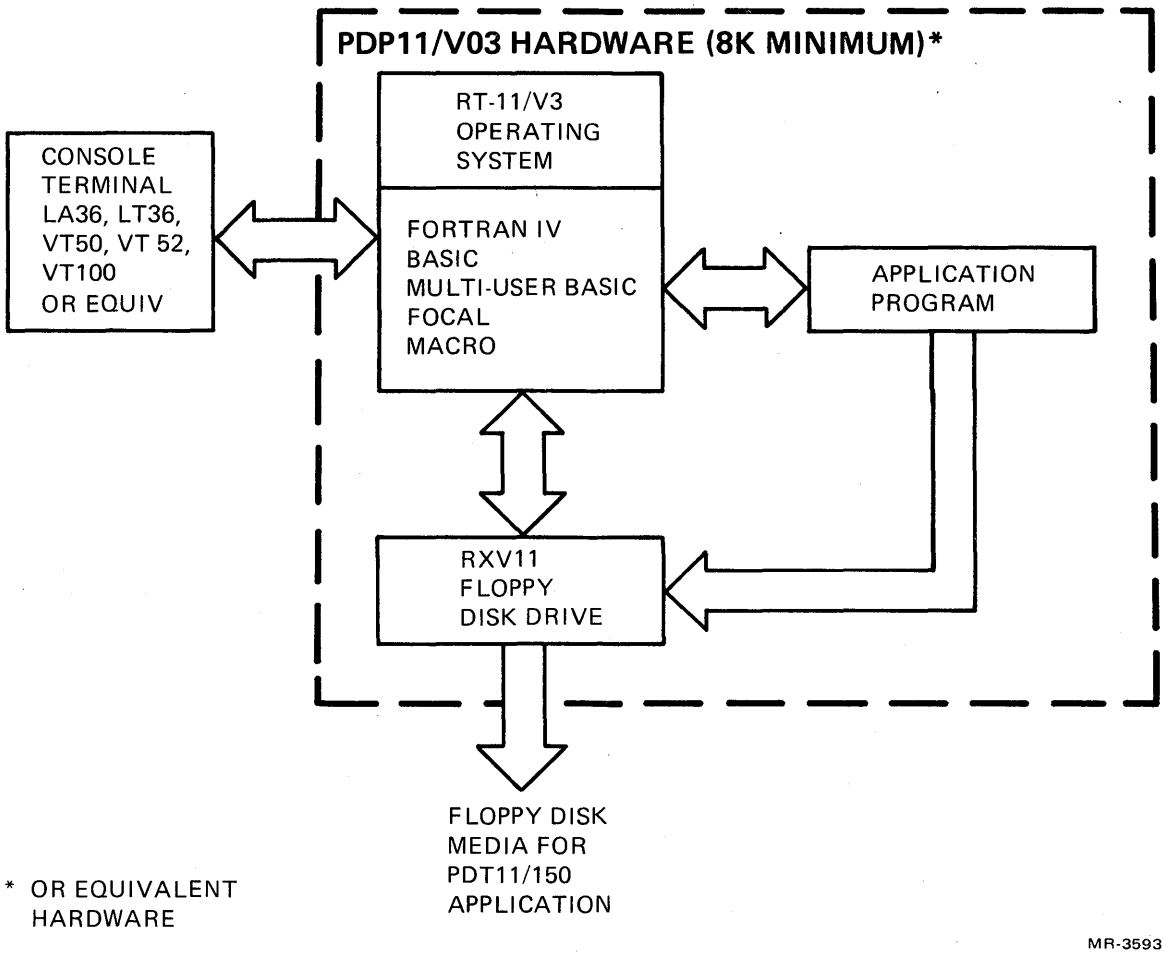


Figure 5-1 PDT-11/150 Program Development System

5.2 PERIPHERAL DEVICE COMMUNICATION

The PDT-11/150 is capable of communicating with the peripheral devices in a full-duplex transmission mode. In full-duplex mode, serial data characters can be simultaneously and independently transmitted and received. The actual operating baud rate of each device is dependent upon the transmission mode, the number of devices used with the system, the type of devices, and the operating or application system programs. The maximum baud rates must also be considered when using devices capable of transmitting continuous serial streams of characters of stored information from special function keys or from buffered data storage.

The maximum baud rate for each peripheral device is as follows.

Device	Baud Rate
Console	9600
Modem	2400 (synchronous) 4800 (asynchronous)
Printer (Line)	9600

Device (Cont)	Baud Rate (Cont)
Terminal 1	2400
Terminal 2	2400
Terminal 3	2400

5.2.1 Console Device

The operator's console provides direct communication between the user and software system through the keyboard. The maximum console baud rate is 9600 baud for data transfers using the standard ASCII keyboard characters. Some consoles include special function keys (cursor control, answerback functions, etc.) which when pressed cause a serial stream of continuous data. When these functions are required the console baud rate should be reduced to a maximum of 4800 to prevent the loss of data during the receive transmissions.

5.2.2 Communications Modem

The communications modem can be operated synchronously at a maximum baud rate of 2400. During asynchronous transfers the baud rate can be increased to 4800 maximum.

5.2.3 Line Printer Terminal

The printer terminal is capable of operating with the system at a maximum rate of 9600 baud.

5.2.4 Cluster Option Terminals

The cluster EIA interface permits the operation of three additional terminal devices at a maximum data transfer rate of 2400 baud. Each terminal can include a keyboard with the standard ASCII character set. When the terminal contains buffered data storage or special function keys as described in Paragraph 5.2.1, the baud rate should be reduced to a maximum of 2000.

5.2.5 Power Up and Manual Reset Conditions

When ac power is applied to the PDT-11/150 unit or when the mode switch on the rear panel is momentarily set to the RESET position, the following parameters will be preselected for the serial line interfaces and line time clock (LTC).

Device Interface	Baud Rate	Character Parameters
Console	9600*	8-bit length one start bit
Modem	1200 (asynchronous mode)	one stop bit Baud rates of 110
Printer	1200 No parity	require two stop bits.

*Autobaud function disabled (Table 5-24)

Device Interface (Cont)	Baud Rate (Cont)	Character Parameters (Cont)
Cluster Terminal 1 Terminal 2 Terminal 3	300	
Line Time Clock (LTC)*	The INT ENB (bit 06) of the TCSR is set to 1. Refer to Table 5-23.	

The baud rate and parameters of the console interface may be changed by selecting different parameters under program control when power is initially applied. Refer to Paragraph 5.3.1.

If the console autobaud function is selected (Table 5-24) the character parameters of the console device must be set to 8-bit length, one start bit, one stop bit and no parity prior to establishing the baud rate.

5.2.6 Programmed Reset Instruction (Initialize)

If a reset instruction is issued during programmed operation, all device registers will be reset and any operation in process will be terminated. If the INT ENB (bit 06) of the LTC was previously cleared, the reset instruction will set the bit to 1. If the synchronous mode was selected for the modem interface, the reset will cause the interface to default to the asynchronous mode.

5.3 DEVICE AND INTERRUPT VECTOR ADDRESS ASSIGNMENTS

Each of the registers associated with the device interfaces, disk drives, and the line time clock have specific device addresses assigned. In addition all interfaces which have the capability to generate programmed interrupt requests have unique vector address assignments to locations in RAM memory where the device service routines are stored. All device and vector addresses are fixed and may not be altered by the user. Figure 5-2 shows the relationship of the control and buffer registers within the PDT-11/150.

5.3.1 USART Parameter Control Register Address

The USART parameter control register (UPCSR) is used to select the operating parameters of the standard USART interfaces and the optional USART interfaces. The standard devices are the console, modem and printer. The optional devices are terminal 1, 2 and 3. The register also enables the user to control the 1 and 2 indicator lamps on the front panel of the unit. When operating synchronously with a modem on the communications interface, an additional parameter control/status register (PARCSR) is also used for selecting operating parameters. The following address is assigned to the USART parameter register.

USART PARAMETER 177420
REGISTER ADDRESS

*LTC enabled (Table 5-24)

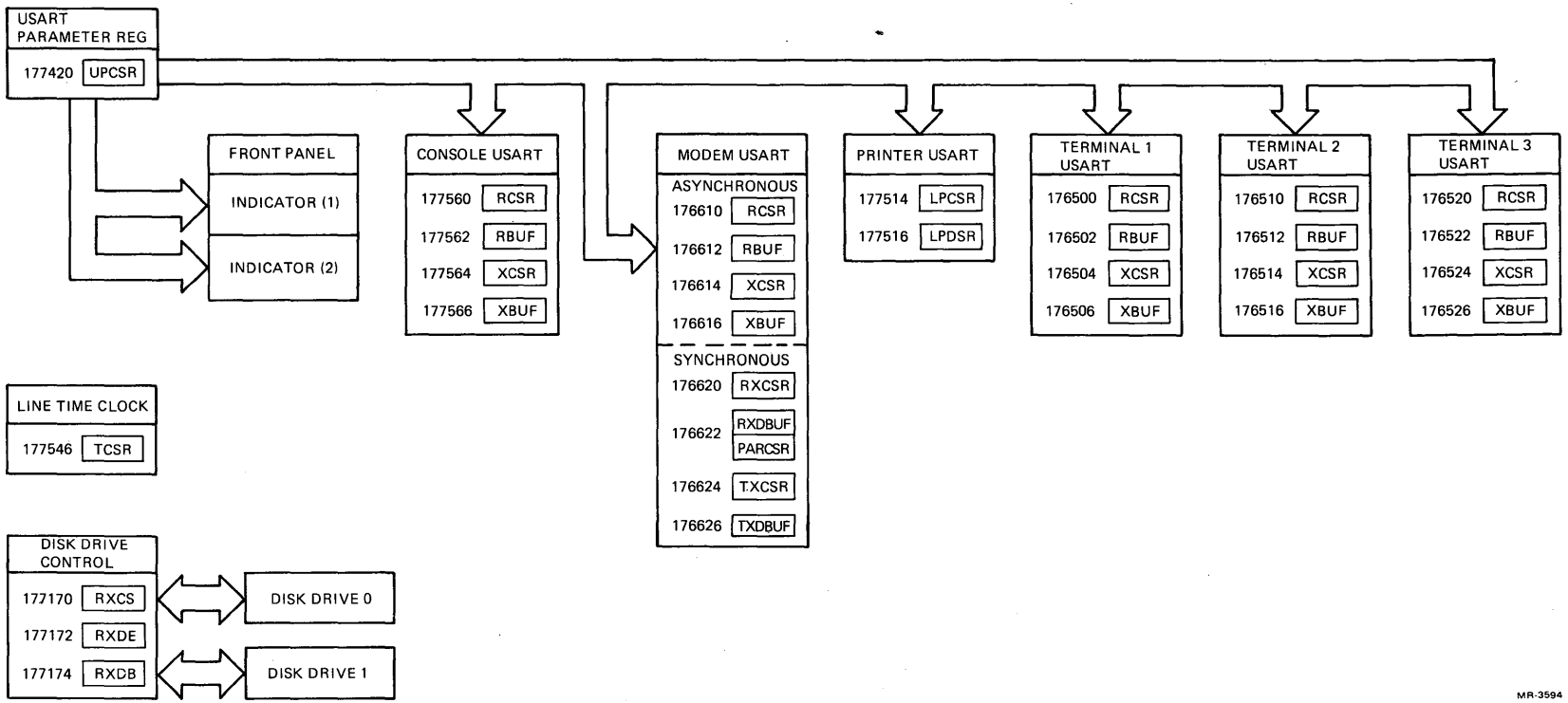


Figure 5-2 PDT-11/150 Control and Address Register, Buffer Assignments

5.3.2 Standard Terminal Addresses

Table 5-1 lists the device and interrupt vector address assignments for the I/O registers associated with each of the three standard devices that operate with the PDT-11/150. The address assignments are nonchangeable.

Table 5-1 Standard Device and Vector Addresses

	Address	
Device Type	**Register**	**Interrupt Vector**
Console Terminal		
Receiver Control Status Register (RCSR)	177560	Receive 000060 Transmit 000064
Receiver Data Buffer Register (RBUF)	177562	
Transmitter Control/ Status Register (XCSR)	177564	
Transmitter Data Buffer Register (XBUF)	177566	
Asynchronous Communications Modem		
Receiver Control/ Status Register (RCSR)	176610	Receive 000330 Transmit 000334
Receiver Data Buffer (RBUF)	176612	
Transmitter Control/ Status Register (XCSR)	176614	
Transmitter Data Buffer (SBUF)	176616	
Sunchronous Communications Modem		
Receiver Control/ Status Register (RXCSR)	176620	Receive 000340 Transmit 000344
Receiver Data Buffer (RXDBUF)	176622	
Parameter Control/ Status Register (PARCSR)	176622	
Transmitter Control/ Status Register (TXCSR)	176624	
Transmitter Data Buffer (TXDBUF)	176626	

Table 5-1 Standard Device and Vector Addresses (Cont)

Device Type	Address	
	Register	Interrupt Vector
Printer Control/Status Register (LPCSR)	177514	Transmit 000200
Receiver Data Buffer (LPDSR)	177516	

5.3.3 Optional (Cluster) Terminal Addresses

Table 5-2 lists the device and interrupt vector address assignments for the I/O registers associated with each of the three additional terminals. Terminals operate with the PDT-11/150 when option DFT11-AB is installed.

Table 5-2 Optional (Cluster) Terminals, Device and Vector Addresses

Device Type	Address	
	Register	Interrupt Vector
Terminal No. 1 (Similar to console, Table 5-1) Receiver Control/Status Register (RCSR)	176500	Receive 000300 Transmit 000304
Receiver Data Buffer (RBUF)	176502	
Transmitter Control/ Status Register (XCSR)	176504	
Transmitter Data Buffer (XBUF)	176506	
Terminal No. 2 (Similar to console, Table 5-1) Receiver Control/Status Register (RCSR)	176510	Receive 000310 Transmit 000314
Receiver Data Buffer (RBUF)	176512	
Transmitter Control/ Status Register (XCSR)	176514	

Table 5-2 Optional (Cluster) Terminals, Device and Vector Addresses (Cont)

Device Type	Address	
	Register	Interrupt Vector
Transmitter Data Buffer (XBUF)	176516	
Terminal No. 3 (Similar to console Table 5-1) Receiver Control/Status Register (RCSR)	176520	Receive 000320 Transmit 000324
Receive Data Buffer (RBUF)	176522	
Transmitter Control/ Status Register (XCSR)	176524	
Transmitter Data Buffer (XBUF)	176526	

5.3.4 Disk Drive Addresses

Table 5-3 lists the address assignments of the registers and interrupt vector for the single or dual disk unit. The RXCS register information specifies either disk drive 0 or 1.

Table 5-3 Disk Drive, Device and Vector Addresses

Device Type	Address	
	Register	Interrupt Vector
Receiver Control/ Status Register (RXCS)	177170	000264
Data Buffer Register (RXDE)	177172	
Used as data and error/ status register for the following two functions: RX Data Buffer (RXDB) RX Error and Status (RXSA)		
RX Track/Sector Register (RXSA)	177174	

5.3.5 Line Time Clock Addresses

Table 5-4 lists the device and interrupt vector address assignments for the line time clock within the PDT-11/150.

Table 5-4 Line Time Clock, Device and Vector Address

Device Type	Address	
	Register	Interrupt Vector
Line Time Clock	177546	000100

5.4 STANDARD TERMINAL REGISTER FORMATS

The following paragraphs describe the content and function of the registers associated with each of the three standard terminal interfaces.

5.4.1 USART Parameter Register

The operating parameters of the devices connected to the standard interface or optional interface (cluster) and the user lights 1 and 2 on the control panel can be selected and modified by the USART parameter register. The interface for each device is initialized at power-up time and must be programmed for operating conditions after initialization if different conditions are required. Figure 5-3 shows the word format and Table 5-5 describes the function of the bits. This register is write-only and must be programmed as a full 16-bit word.

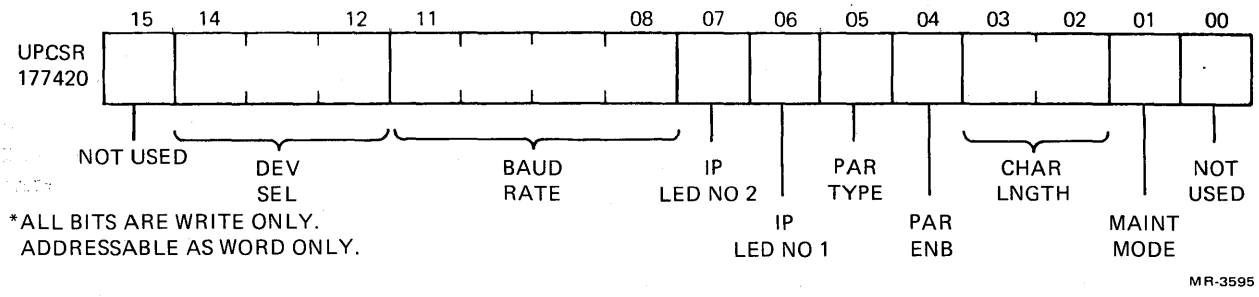


Figure 5-3 USART Parameter Control Register UPCSR Format

Table 5-5 USART Parameter Register, Bit Descriptions

Bit	Name	Description
15	Not Used	
14–12	DEV SEL	Device Select – Selects one of the six standard or optional device interfaces for parameter information as follows:

Bits

14	13	12	Interface Select
0	0	0	Cluster terminal no. 1 (option)
0	0	1	Console terminal
0	1	0	Printer terminal
0	1	1	Communications (modem)
1	0	0	Selects user lights on indicator panel
1	0	1	Cluster terminal no. 2 (option)
1	1	0	Cluster terminal no. 3 (option)

Bit	Name	Description
11–08	BAUD RATE	Baud Rate – Selects the desired baud rate for the interface selected as follows:

Bits				Baud Rate	Bits				Baud Rate
11	10	09	08		11	10	09	08	
0	0	0	0	50	1	0	0	0	1800
0	0	0	1	75	1	0	0	1	2000
0	0	1	0	110*	1	0	1	0	2400
0	0	1	1	134.5	1	0	1	1	3600
0	1	0	0	150	1	1	0	0	4800
0	1	0	1	300	1	1	0	1	7200
0	1	1	0	600	1	1	1	0	9600
0	1	1	1	1200					

Bit	Name	Description
07	LED No. 2	Indicator Panel – Set to light the "2" LED on the PDT-11/150 indicator panel.
06	LED No. 1	Indicator Panel – Set to light the "1" LED on the PDT-11/150 indicator panel.

*Baud rate 110 assumes two stop bits.

Table 5-5 USART Parameter Register, Bit Descriptions (Cont)

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>05</td><td>PAR TYPE</td><td>Parity Type – Selects odd or even parity when enabled by PARENB (bit 04) as follows:

1 = even parity
0 = odd parity</td></tr>
<tr><td>04</td><td>PAR ENB</td><td>Parity Enable – Enables or disables parity check function as follows:

1 = enable parity
0 = disable parity</td></tr>
<tr><td>03–02</td><td>CHAR LNTH</td><td>Character Length – Selects the number of bits in each character transferred as follows:

<table>
<tr><th colspan="2">Bits</th><th>Character Length (Bits)</th></tr>
<tr><td>03</td><td>02</td><td></td></tr>
<tr><td>0</td><td>0</td><td>5</td></tr>
<tr><td>0</td><td>1</td><td>6</td></tr>
<tr><td>1</td><td>0</td><td>7</td></tr>
<tr><td>1</td><td>1</td><td>8</td></tr>
</table>
</td></tr>
<tr><td>01</td><td>MAINT MODE</td><td>Maintenance Mode – Set to 1 to select the maintenance mode. Used during diagnostic programs to loop back cluster option interface data and communications interface data from standard interface.</td></tr>
<tr><td>00</td><td>Not Used</td><td></td></tr>
</table>

5.4.2 Console Device Interface

Program information and status and control information are transferred between the user and PDT-11/150 system using the console device and interface. Four registers are associated with the interface. The content and format of the registers are shown in Figure 5-4 and described in the following paragraphs.

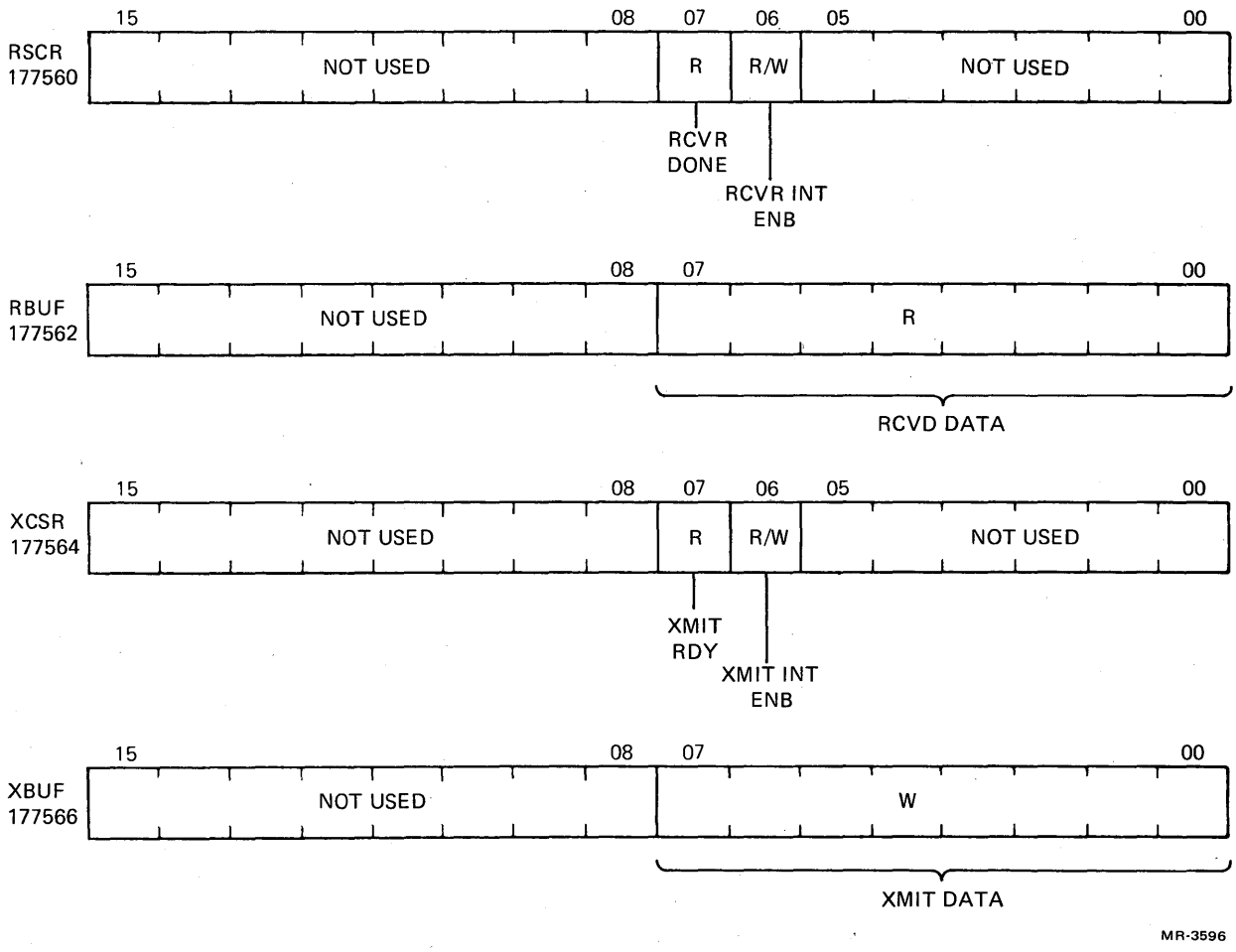


Figure 5-4 Console Terminal Interface Register Formats
and optional terminals

5.4.2.1 Receiver Control/Status Register (RCSR) – The RCSR provides control and status information for data transferred from the console device to the PDT-11/150. Table 5-6 describes the functions of the bits of the RCSR.

5.4.2.2 Receiver Data Buffer (RBUF) – The RBUF stores the data character received by the PDT-11/150 from the console device. Table 5-6 lists and defines the function of the bits in the RBUF.

Table 5-6 Console Interface, Receiver Register Bit Descriptions

Bit	Name	Description
15–08	Not Used	RCSR Receiver Control/Status Register
07	RCVR DONE	Receiver Done – A read-only bit set when an incoming character is available in the RCVR data register (RBUF). If the RCVR INT ENB (bit 06) is set, an interrupt request will be generated. Cleared by the INIT signal or when the RBUF is read.

Table 5-6 Console Interface, Receiver Register Bit Descriptions (Cont)

Bit	Name	Description
06	RCVR INT ENB	Receiver Interrupt Enable – A read/write bit, set by program to allow the RCVR DONE (bit 07) to generate an interrupt request. Cleared by the INIT signal or under program control.
05–00	Not Used	
15–08	Not Used	RBUF (Receiver Data Buffer)
07–00	RCVD DATA	Received Data – Read-only bits which are the last character, from the console, assembled by the USART. If the specified character length is less than eight bits, the character will appear right-justified with the low order bit in bit 00. The unused high order bits of the word will contain (0).

5.4.2.3 Transmitter Control/Status Register (XCSR) – The XCSR provides control and status information during information transfers from the PDT-11/150 to the console device. See Table 5-7.

5.4.2.4 Transmitter Data Buffer (XBUF) – The XBUF stores the data character for transmission to the console from the PDT-11/150. Table 5-7 lists the bit assignments and describes their function.

Table 5-7 Console Interface, Transmitter Register Bit Descriptions

Bit	Name	Description
XCSR (Transmitter Control/Status Register)		
15–08	Not Used	
07	XMIT RDY	Transmitter Ready – A read-only bit, set when the transmit buffer is ready to accept a character. Also set by the INIT signal. If the XMIT INT ENB (bit 06) is set, an interrupt request will be generated. Cleared when a character is loaded into the XBUF.
06	XMIT INT ENB	Transmitter Interrupt Enable – A read/write bit set by program to allow the XMIT RDY (bit 07) to generate an interrupt request. Cleared by the INIT signal or under program control.
05–00	Not Used	
XBUF (Transmitter Data Buffer)		
15–08	Not Used	
07–00	XMIT DATA	Transmit Data – Write-only bits which are the data character to be transmitted serially to the console. If the specified character length is less than eight bits, the character must be right-justified with the low order bit in bit 00 position when loaded.

5.4.3 Communications Interface (Modem)

The communications (modem) interface in the PDT-11/150 transmits and receives standard EIA levels from a Bell 103, 113, 202, or 212 data set or equivalent device. The communications interface is programmable to operate with synchronous and asynchronous data transmissions in either a half or full duplex mode.

Figure 5-5 indicates the methods used to select the synchronous or asynchronous transfers. When the PDT-11/150 system is initialized, the asynchronous mode is preselected with the parameters indicated on the diagram. To modify the parameter information in the asynchronous mode, follow the procedures on the left branch of the diagram. The synchronous transmission mode is selected by following the procedures indicated on the right branch of the diagram. Refer to the appropriate tables for the parameter definitions.

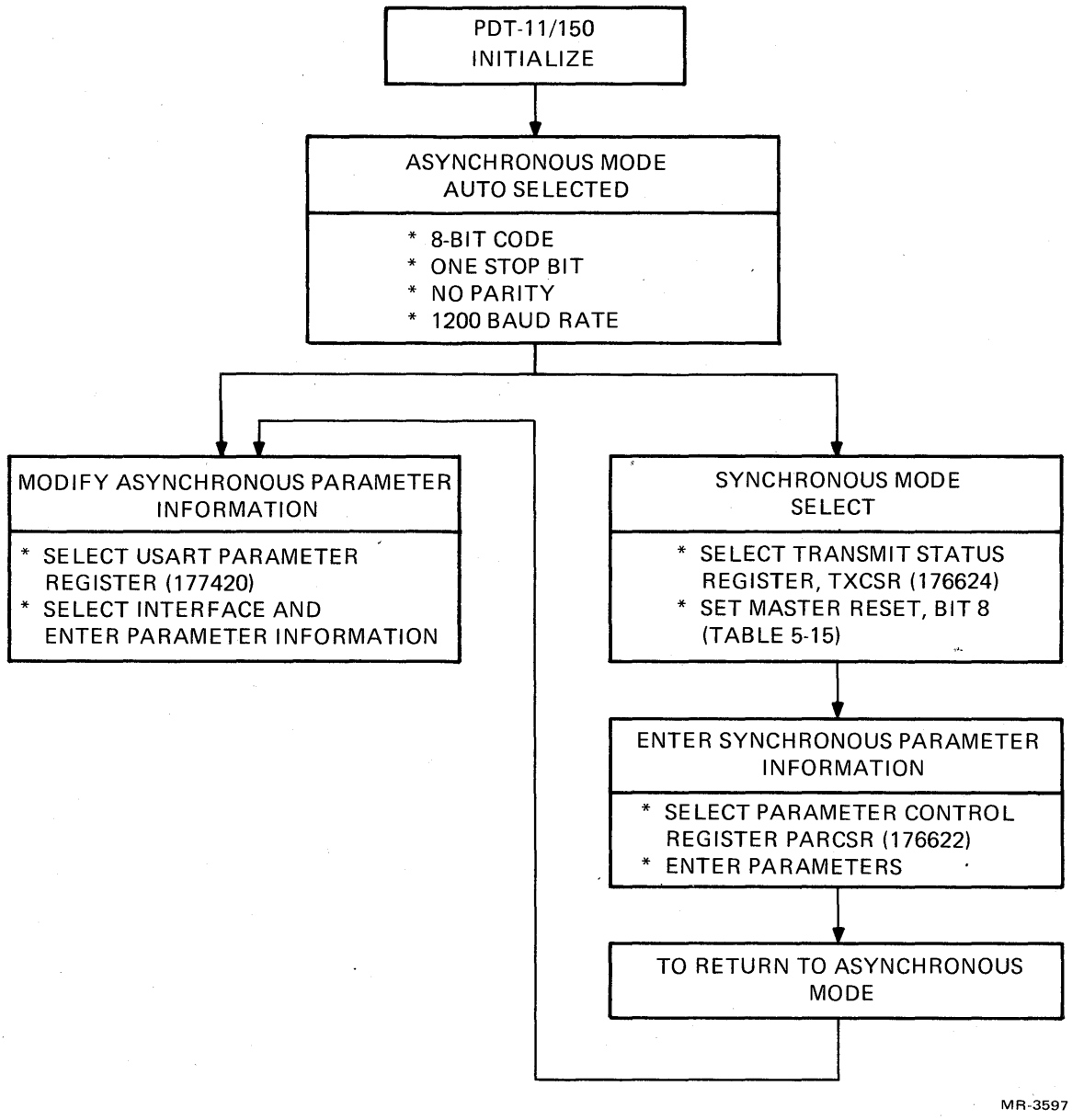


Figure 5-5 Communication Interface, Asynchronous/Synchronous Select

5.4.4 Asynchronous Modem Interface

Four registers are associated with the asynchronous communications. Two registers provide data control and status information during the receiver functions and two registers provide this information during transmit functions. In addition, the USART parameter register can be programmed to modify the parameter information. Figure 5-6 shows the bit formats for each of the registers associated with the interface. The asynchronous communications interface is designed to be compatible with theDIGITAL LSI-11 microprocessor, DLV11-E asynchronous serial line interface as described in the DIGITAL Memories and Peripherals handbook.

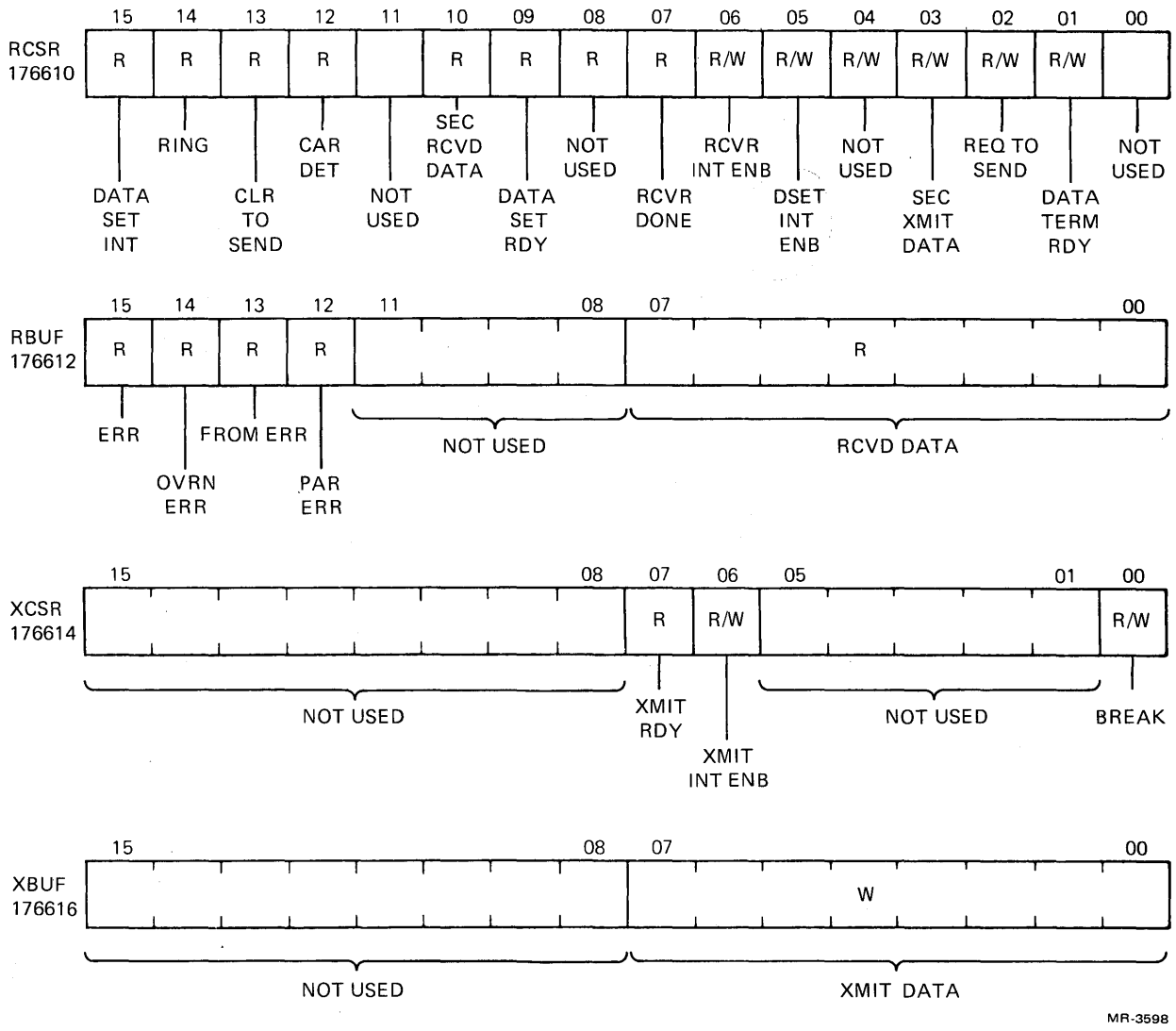


Figure 5-6 Asynchronous Communications Interface Register Formats

5.4.4.1 Asynchronous Receiver Control/Status Register (RCSR) – The RCSR provides control and status information during all operations. Table 5-8 lists and defines the function of each bit.

Table 5-8 Asynchronous Communication, RCSR Bit Descriptions

Bit	Name	Description
15	DATA SET CHNG Vector 330	Data Set Change – A read-only bit that initiates an interrupt sequence provided the DAT SET INT ENB bit (05) is also set. Set whenever CAR DET, CLR TO SEND, DATA SET READY, or SEC REC changes state in a 0-to-1 or 1-to-0 transition. Also set when Ring changes from 0 to 1. Cleared by the INIT signal or by reading the RCSR.
14	RING	Ring – A read-only bit; when set, indicates that a Ring signal is being received from the data set. The Ring signal is an EIA control with the cycle time of two seconds on and four seconds off.
13	CLR TO SEND	Clear to Send – A read-only bit; the state of this bit is dependent on the state of the Clear to Send signal from the data set. When set, indicates an ON condition; when clear, indicates an OFF condition.
12	CAR DET	Carrier Detect – A read-only bit, set when the data carrier is received. When clear, indicates either the end of the current transmission activity or an error condition.
11	Not Used	
10	SEC REC	Secondary Received or Supervisory Received Data – A read-only bit that provides a receive capability for the reverse channel of a remote station. A space (approx. 10 V) is a 1. (A transmit capability is provided by bit 03.)
09	DATA SET READY	Data Set Ready – A program read-only bit that is a direct reflection of the Data Set Ready (or interlock) lead emanating from the modem. This line, when asserted, indicates that the modem is powered up and is not in the test, talk, or dial mode. Any transition of this bit will cause the Data Set Change bit to be asserted.
08	Not Used	
07	RCVR DONE	Receiver Done – A read-only bit that is set when an entire character has been received and is ready for transfer to the LSI-11. When set, it initiates an interrupt sequence provided RCVT INT ENB (bit 06) is also set. Cleared whenever the receiver buffer (RBUF) is addressed and by the INIT signal.
06	RCVR INT ENB	Receiver Interrupt Enable – A read/write bit. When set, allows an interrupt sequence to start when DONE (bit 07) sets. Cleared by the INIT signal.

Table 5-8 Asynchronous Communication, RCSR Bit Descriptions (Cont)

Bit	Name	Description
05	DSET INT ENB	Data Set Interrupt Enable – A read/write bit. When set, allows an interrupt sequence to start when DATA SET INT (bit 15) sets. Cleared by the INIT signal.
04	Not Used	
03	SEC XMIT	Secondary Transmit or Supervisory Transmitted Data – A read/write bit that provides a transmit capability for a reverse channel of a remote station. When set, transmits a space (approx. 10 V). (A receive capability is provided by bit 10.) Cleared by the INIT signal.
02	REQ TO SEND	Request to Send – A read/write bit used in the control of the data set, transmitted data. Cleared by the INIT signal.
01	DTR	Data Terminal – A read/write bit. When set permits Ready the connection of the communications channel in the data set. When clear disconnects the interface from the channel. Cleared by the INIT signal.
00	Not Used	

5.4.4.2 Asynchronous Receiver Data Buffer (RBUF) – The RBUF register stores the data bits received from the line and indicates any error conditions associated with the data received. Table 5-9 lists and describes the bit functions.

Table 5-9 Asynchronous Communications, RBUF Bit Descriptions

Bit	Name	Description
15	ERROR	Error – A read-only bit that indicates an error condition is present. This bit is the logical OR of OR ERR, FR ERR, and P ERR (bits 14, 13 and 12, respectively). Whenever one of these bits is set, it causes ERROR to set. This bit is not connected to the interrupt logic. Cleared when the error producing the condition is removed. If a byte of data is read and no new data character is received, the error indication is cleared. Cleared by the INIT signal.
14	OVRN ERR	Overrun Error – A read-only bit; when set, indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character. Cleared by the INIT signal.
13	FR ERR	Framing Error – A read-only bit; when set, indicates that the character that was read had no valid STOP bit. Cleared by the INIT signal.

Table 5-9 Asynchronous Communications, RBUF Bit Descriptions (Cont)

Bit	Name	Description
12	P ERR	Parity Error – A read-only bit; when set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected.
11–08	Not Used	
07–00	Received Data Bits	Read-only bits which represent the character received from the modem. If less than eight bits are selected, the buffer is right-justified into the least significant bit positions. The higher unused bit or bits are read as 0s. Not cleared by the INIT signal. If parity is selected at the UPCSR (PAR ENB bit = 1) for characters less than 8 bits, the parity will be appended to the next bit position from the highest order bit of the character. No parity is present when an 8-bit character is used. When the character is read, RCVR DONE (bit 07) of the RCSR is cleared.

5.4.4.3 Asynchronous Transmitter Control/Status Register (XCSR) – The XCSR provides control and status information during transmit operations. Table 5-10 describes the function of each bit in the register.

Table 5-10 Asynchronous Communications, XCSR Bit Assignments

Bit	Name	Description
15–08	Not Used	
07	XMIT READY	Transmit Ready – A read-only bit, set when the transmitter buffer is ready to accept a character. This condition initiates an interrupt sequence when XMIT INT ENB (bit 06) is set. Also set by INIT signal.
06	XMIT INT ENB	Transmit Interrupt Enable – A read/write bit; when set it allows an interrupt sequence to start when XMIT READY, bit 07, is set.
05–01	Not Used	
00	BREAK	Break – A read/write bit; when set by program, transmits a continuous space character to the external device. Cleared by the INIT signal. The duration of the space character transmission must be controlled by the program using software timers.

5.4.4.4 Asynchronous Transmitter Data Buffer (XBUF) – The XBUF stores the data information for transmission to the line. The bit functions are described in Table 5-11.

Table 5-11 Asynchronous Communications, XBUF Bit Descriptions

Bit	Name	Description
15–08	Not Used	
07–00	XMIT DATA CHAR	Transmit Data Character – Stores the data character for transfer to the modem. If the character is less than eight bits, it must be loaded right-justified at the least significant bit. Write-only bits.

5.4.5 Synchronous Modem Interface

The synchronous mode of the communications interface is selected as described in Paragraph 5.4.3. Two registers are associated with the receive operation of the USART and two registers are associated with the transmit operations. Figure 5-7 shows the formats for each of the four registers. In addition, a parameter control register specifically for the synchronous mode is programmable to specify the transmission characteristics.

CAUTION

A programmed reset instruction from the microprocessor will cause the interface to change from the synchronous mode to the asynchronous mode and clear all flags.

NOTE

When clearing an interrupt enable bit, first set the processor to its highest priority (processor status word PSW bit 7 = 1). After the interrupt enable bit is cleared, the processor may be returned to its normal priority (PSW bit 7 = 0).

For example:

```
MTPS #200
BIC #100, CSR
MTPS #0
EXIT
```

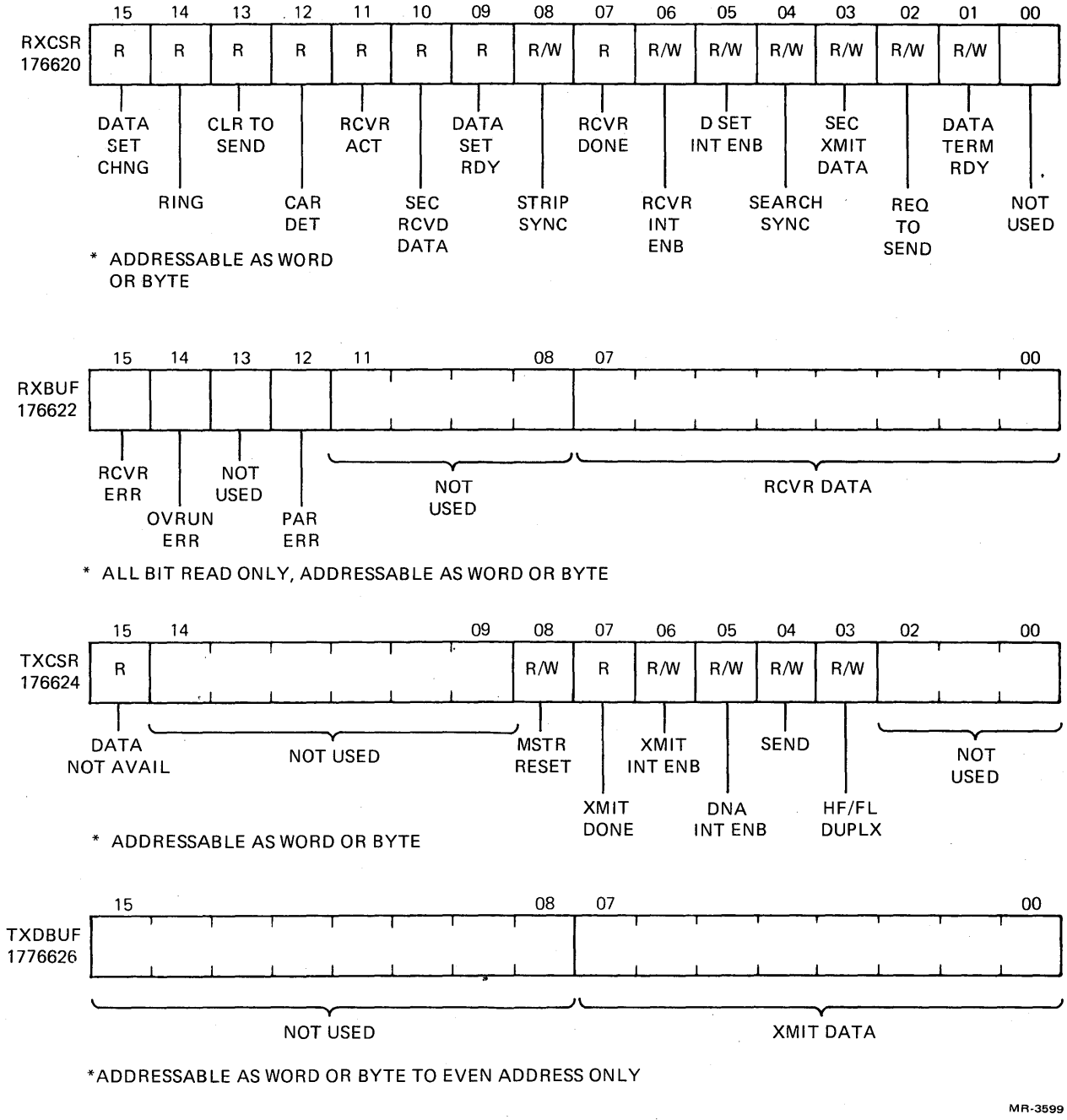


Figure 5-7 Synchronous Communications Interface Register Format

5.4.5.1 Parameter Control Register (PARCSR) – Figure 5-8 shows the word format of the PARCSR and Table 5-12 lists the bit assignments.

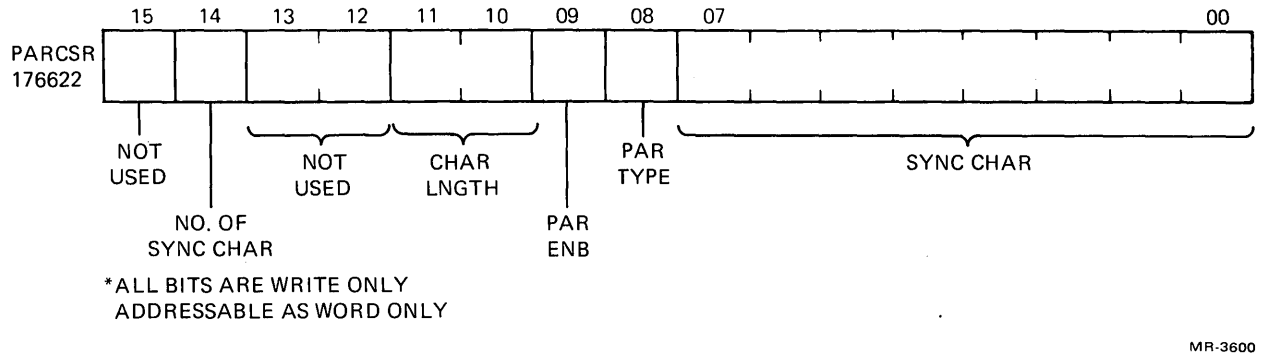


Figure 5-8 Synchronous Communications Parameter Control Register Format

Table 5-12 Parameter Control Register, PARCSR Bit Descriptions

Bit	Name	Description
15	Not Used	
14	NO SYNC CHAR	Number of Sync Characters – A write-only bit that selects either one or two sync characters which must be received for successful synchronization as follows: 1 – selects two sync characters 0 – selects one sync character
13–12	Not Used	
11, 10	CHAR LENGTH	Character Length – Write-only bits that select the number of bits associated with each character as follows: **Bit 11 10 — Character Length** 0 0 — 5 0 1 — 6 1 0 — 7 1 1 — 8
09	PAR ENB	Parity Enable – Enables or disables parity check function as specified by PARTYPE (bit 08) as follows: 1 = enable parity generation 0 = disable parity generation

Table 5-12 Parameter Control Register, PARCSR Bit Descriptions (Cont)

Bit	Name	Description
08	PARTYPE	Parity Type – Program write-only bit used to select odd or even parity generation when enabled by PARENB (bit 09) as follows: 1 = even parity 0 = odd parity Parity is added to transmitted characters and a parity check is performed on received characters.
07–0	SYNC CHAR	Sync Character – Program write-only. Used for character synchronization prior to transmitting serial character stream. Character format and number of characters transmitted is dependent on command mode. Refer to modem information. Sync character will be all 1s after master reset. Character length is right-justified from bit 00.

5.4.5.2 Synchronous Receiver Control/Status Register (RXCSR) – The RXCSR is programmed and monitored during receive data operations. The register is addressable as a word or byte and contains control and status information from the modem. Table 5-13 lists and defines the function of each bit.

Table 5-13 Synchronous Communications, RXCSR Bit Descriptions

Bit	Name	Description
15	DATA SET CHNG	Data Set Change – A read-only bit, set to indicate a level transition on one of the following modem lines: Ring Clear to Send Carrier Secondary Received Data Data Set Ready If D SET INT ENB (bit 05) is set, the level transition will cause an interrupt request by the receiver. Cleared by the INIT signal or when the RXCSR is read.
14	RING	Ring Indicator – A read-only bit, set to indicate that a ring signal is being received from the modem.
13	CLR TO SEND	Clear to Send – A program read-only bit, set to indicate that the modem is ready to receive data from the interface.
12	CAR DET	Carrier Detect – A program read-only bit set by the modem whenever an acceptable carrier is on the communications line.

Table 5-13 Synchronous Communications, RXCSR Bit Descriptions (Cont)

Bit	Name	Description
11	RCVR ACT	Receiver Active – A program read-only bit that is set when the selected number of continuous sync characters (either one or two) from the modem has been received. Cleared by the INIT signal.
10	SEC RCV DATA	Secondary Received Data – A program read-only bit that reflects the state of the Secondary Received Data line from the modem. Any transition on the line will also assert DATA SET CHANGE (bit 15). Supervisory data can be received over this line when operating with some modems. As a control line, it can also be used to acknowledge a message.
09	DATA SET RDY	Data Set Ready – A program read-only bit that reflects the state of the Data Set Ready line from the modem. When asserted, the line indicates that the modem is powered up and is not in the test, talk, or dial mode. Any transition on the line will also assert the DATA SET CHANGE (bit 15).
08	STRIP SYNC	Strip Sync – A program read/write bit; when set, prevents the receive characters which match the contents of the sync register from causing an RCVR interrupt provided no errors are detected in the RXDBUF. Cleared by the INIT signal.
07	RCVR DONE	Receiver Done – A program read-only bit, normally set when a character is transferred into the receive buffer. If the character received is a sync character and the STRIP SYNC (bit 08) and RCVR ACT (bit 11) are set, the RCVR DONE bit will not be asserted. Cleared by reading the RXBUF or by the INIT signal.
06	RCVR INT ENB	Receiver Interrupt Enable – A program read/write bit; when set, allows a receiver interrupt request to be generated, provided RCVR DONE (bit 07) is set. Cleared by the INIT signal.
05	D SET INT ENB	Data Set Interrupt Enable – A program read/write bit; when set, allows a receiver interrupt request to be generated provided the D SET CHANGE (bit 15) is asserted. Cleared by the INIT signal.
04	SEARCH SYNC	Search Sync – A program read/write bit; when set, enables the comparison of the received data with the sync code stored in the sync register. After the selected number of sync characters are detected, the RCVR ACT (bit 11) is asserted. Cleared by the INIT signal.
03	SEC XMIT DATA	Secondary Transmit Data – A program read/write bit that indicates the status of the secondary transmit transmit line of the modem. Supervisory data can be transmitted on this line with certain modems. It also can be used to acknowledge a message. Cleared by the INIT signal.

Table 5-13 Synchronous Communications, RXCSR Bit Descriptions (Cont)

Bit	Name	Description
02	REQ TO SEND	Request to Send – A program read/write bit; when set, causes the Request to Send line to the modem to be asserted. This line is asserted prior to transmitting serial data to the modem. Cleared by the INIT signal.
01	DATA TERM RDY	Data Terminal Ready – A program read/write bit; when set, causes the Data Terminal Ready line to the modem to be asserted. During Autodial and manual call origination, asserting the line maintains the established call. For Autoanswer, it allows handshaking in response to a ring signal. Cleared by the INIT signal.
00	Not Used	

5.4.5.3 Synchronous Receiver Data Buffer (RXDBUF) – The RXDBUF stores the character received from the modem and indicates error conditions associated with the received data. Table 5-14 lists and describes the function of the RXDBUF bits.

Table 5-14 Synchronous Communications RXDBUF Bit Descriptions

Bit	Name	Description
15	RCVR ERR	Receiver Error – A program read bit set when either or both the PAR ERR (bit 12) and OVRN ERR (bit 14) are set. Cleared when both the PAR ERR and OVRN ERR bits are cleared.
14	OVRN ERR	Overrun Error – A program read bit, set to indicate a data overrun in the receiver. When the RCVR DONE (bit 07) of the RXCSR is set, the processor must read the RXBUF within a specified time or the overrun error will occur. The time specified is as follows. Ts = (1/baud rate) × bits per character Cleared by the INIT signal or when the RXDBUF low byte is read.
13	Not Used	
12	PAR ERR	Parity Error – A program read bit; if parity detection is enabled, it is set when the parity of the received character is different from the parity selected by PAR TYPE (bit 08) of the PARCSR. A detected parity error will also set RCVR ERR (bit 15). Cleared by the INIT signal or when the RXDBUF low byte is read.

Table 5-14 Synchronous Communications RXDBUF Bit Descriptions (Cont)

Bit	Name	Description
11–08	Not Used	
07–00	RCVR DATA CHAR	Receiver Data Character – Program read bits that represent the data character from the modem and are stored in the RXDBUF. Character can be five to eight bits in length and is always right-justified. Parity, if selected, always appears after the MSB except for an 8-bit character where no parity will be indicated. Cleared by reading the low byte of RXDBUF which also clears RCVR DONE (bit 07) of the RXCSR.

5.4.5.4 Synchronous Transmit Control and Status Register (TXCSR) – The TXCSR is programmed and monitored to provide control and status operations. Table 5-15 describes the function of each bit.

Table 5-15 Synchronous Communications, TXCSR Bit Descriptions

Bit	Name	Description
15	DATA NOT AVAIL	Data Not Available – A program read bit set to indicate a character has been transmitted from the sync register to the modem. A sync character is transmitted if a new character is not loaded into the TXDBUF within a specified time after the XMIT DONE (bit 07) is set. The time interval is as follows. Ts = (1/baud rate) × (bits per character – 1/2 bit time) If the DNA INT ENB (bit 05) is set when DATA NOT AVAIL is asserted, a transmitter interrupt request will be generated. Cleared by the INIT signal or when a character is transmitted.
14–09	Not Used	
08	MSTR RESET	Master Reset – A program read/write bit; when set, causes the receiver and transmitter to enter an idle state. The transmitter idle state results in the following. 1. Internal timing is reset. 2. Transmitter sync register is set to all 1s. 3. All bits of the TXCSR are cleared.

Table 5-15 Synchronous Communications, TXCSR Bit Descriptions (Cont)

Bit	Name	Description
		The receiver state results in the following. 1. Internal timing is reset. 2. The following RXCSR bits are cleared. **Bit Name** 15 DATA SET CHANGE 11 RCVR ACT 08 STRIP SYNC 07 RCVR DONE 06 RCVR INT ENB 05 D SET INT ENB 04 SEARCH SYNC 03 SEC XMIT DATA 02 REQ TO SEND 01 DATA TERM RDY
07	XMIT DONE	Transmitter Done – A program read bit set to indicate that the TXDBUF is ready to receive a data character. If the XMIT INT ENB (bit 06) is set when XMIT DONE is asserted, a transmitter interrupt request is generated. Cleared by the INIT signal or when the TXDBUF receives a character.
06	XMIT INT ENB	Transmitter Interrupt Enable – A program read/write bit set to allow a transmitter interrupt request to be generated when the XMIT DONE (bit 07) is asserted. Cleared by the INIT signal.
05	DNA INT ENB	Data Not Available Interrupt Enable – A program read/write bit set to allow a transmitter interrupt request to be generated when DATA NOT AVAIL (bit 15) is asserted. Cleared by the INIT signal.
04	SEND	Send – A program read/write bit, set to enable data transfer from the transmitter. The SEND bit must be asserted for the entire message or only the current character will be transferred and the transmitter will enter the idle state. Cleared by the INIT signal.
03	HF/FL DUPLEX	Half or Full Duplex – A read/write bit used to select half or full duplex transmission. 1 = half duplex 0 = full duplex The receiver will be disabled if the SEND (bit 04) is asserted during half duplex operation.
02–00	Not Used	

5.4.5.5 Synchronous Transmit Data Buffer (TXDBUF) - The TXDBUF contains eight bits of data to be transmitted serially to the modem and is addressable as a word or byte to an even address only. The remaining eight bits in the word are not used. Table 5-16 describes the character formats for the eight data bits.

Table 5-16 Synchronous Communications TXDBUF Bit Descriptions

Bit	Name	Description
15–08	Not Used	
07–00	XMIT DATA CHAR	Transmit Data Character - Program write bits which represent the data character stored in the TXBUF for transfer to the modem. Character length is from 5 to 8 bits and right-justified at bit 00. The INIT signal sets all 1s in the TXDBUF.

5.4.6 Printer Terminal Interface

The printer terminal interface transfers EIA-compatible serial line data to the printer unit at a maximum rate of 9600 baud. To prevent the loss of data when the printer buffer is full, an X-OFF ASCII command is issued by the printer to stop the data transfers. The X-ON ASCII command indicates that the printer buffer can accept additional data.

When the interface, is initialized, the following data parameters are selected. However, the parameters can be modified through the USART parameter register as described in Paragraph 5.3.1.

DATA WORD PARAMETERS - 8-bit, one start bit, one stop bit, no parity, 1200 baud.

Figure 5-9 shows the bit formats for the printer terminal interface registers.

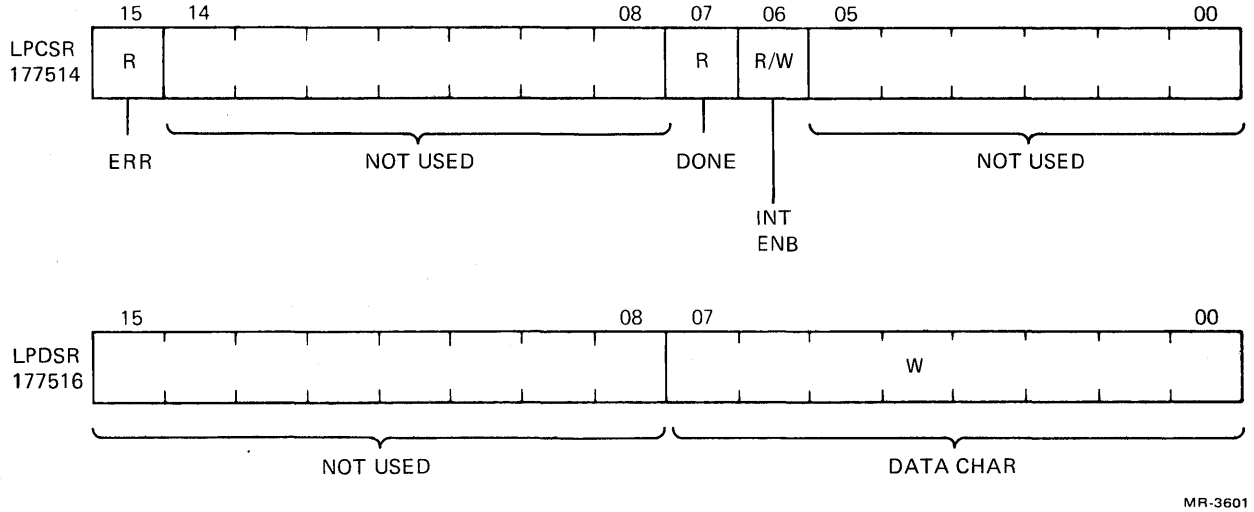


Figure 5-9 Printer Terminal Interface, Register Formats

5.4.6.1 Printer Control/Status Register (LPCSR) – Table 5-17 lists and defines the function of the bits in the LPCSR.

Xmit vec = 200

Table 5-17 Printer Interface PCSR Bit Descriptions

Bit	Name	Description
15	ERR	Error – A read-only bit set when the Data Terminal Ready line from the printer is negated. This condition occurs when the printer terminal paper is depleted or the printer is not powered up. Cleared when the condition is corrected or when power is applied.
14–08	Not Used	
07	DONE	Done – A read-only bit set when the printer is ready to accept a character. An interrupt request will be generated provided the INT ENB (bit 06) is set. The DONE bit is set by the INIT signal and cleared by loading a character into the data register (LPDSR).
06	INT ENB	Interrupt Enable – A read/write bit set or cleared under software control. When set, an interrupt request will be generated provided DONE (bit 07) is set. Cleared by the INIT signal.
05–00	Not Used	

5.4.6.2 Printer Data Buffer (LPDSR) – Table 5-18 lists and defines the function of the bits in the LPDSR.

Table 5-18 Printer Interface PDBUF, Bit Descriptions

Bit	Name	Description
15–08	Not Used	
07–00	DATA CHAR	Data Character – Write-only bits which represent the data character to be transferred to the printer. Bit 07 is the most significant bit of the 8-bit character.

5.5 OPTIONAL TERMINAL REGISTER WORD FORMATS

The Cluster option enables the PDT-11/150 to operate with three additional serial line devices. The interface parameters are selected by the USART parameter register as described in Paragraph 5.4.1. The register formats are identical to the console terminal described in Paragraph 5.3.2.

see p. 5-12

5.6 DISK DRIVE REGISTER FORMATS

Software control of the disk drive is through three registers available on the disk controller interface: the command and status register (RXCS) the data buffer register (RXDB) and the track and sector address register (RXSA). These registers can be read or loaded by programs using instructions that refer to the register device addresses. The interface also contains a read/write data buffer that can contain 64 16-bit words of disk data.

Read and write data transfers require two operations. When writing on a disk, the program is required to transfer data to the data buffer through the RXDB. When the buffer is full, a write sector command is issued through the RXCS and the data is written on the disk.

During a read operation, the data is first read into the buffer from the disk and then read from the buffer through the RXDB. At the completion of a function, the RXDB will contain the current error and status (RXES) of the function selected.

The RXSA that contains the track and sector addresses is loaded prior to issuing a read or write command.

Figure 5-10 shows the bit assignments for the registers described in the following paragraphs.

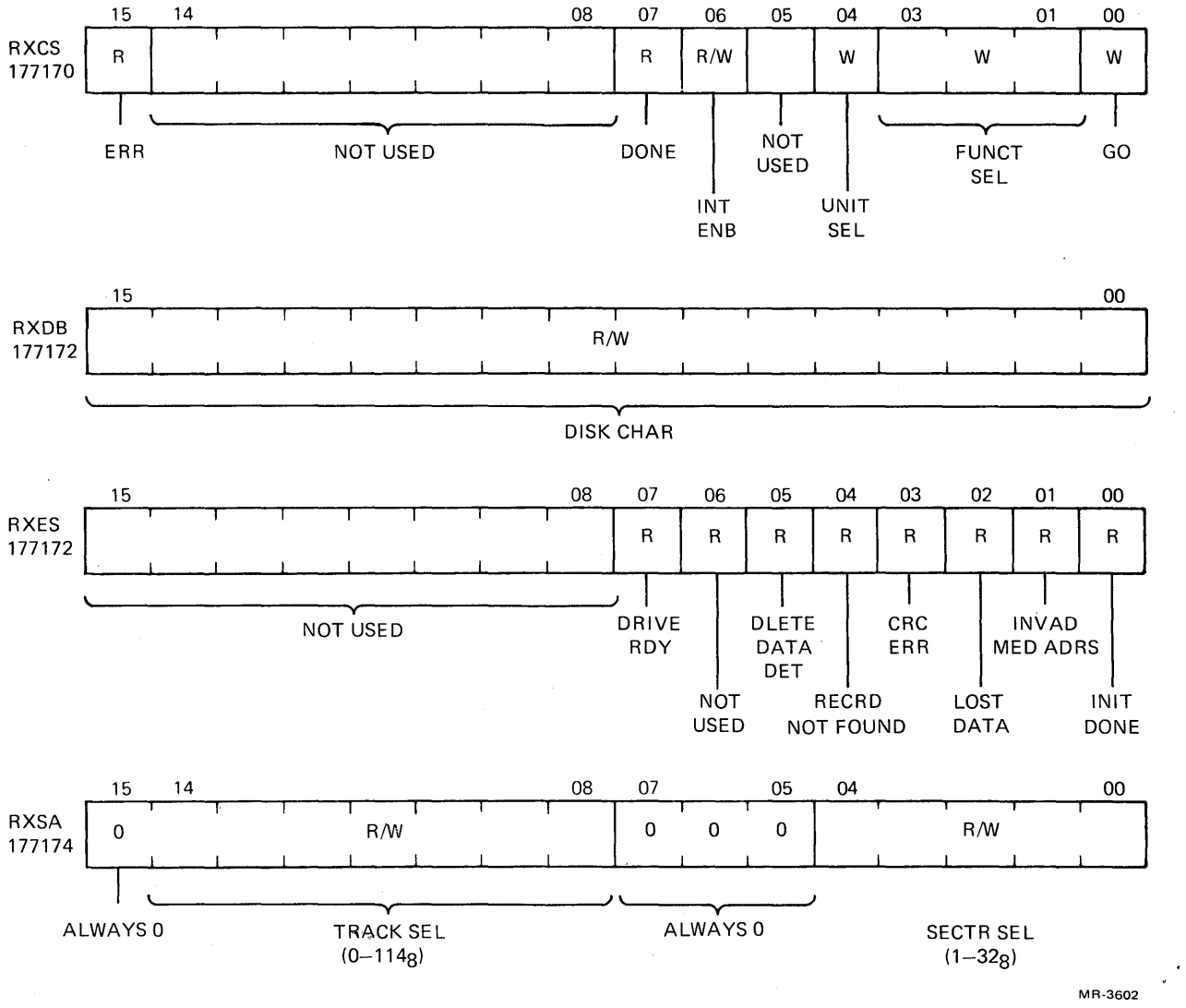


Figure 5-10 Disk Drive Interface, Register Formats

5.6.1 Drive Control/Status Register (RXCS)

Table 5-19 provides a description of each bit in the RXCS. The information in the RXCS initiates and selects the functions of the drives, indicates errors, and selects one of the two drives on a dual drive unit.

The FUNC SEL (bits 03–01) are used to select any of the eight functions associated with each drive. Detailed information of each function is as follows.

Table 5-19 Disk Controller RXCS Bit Descriptions

Bit	Name	Description
15	ERR	Error – A read-only bit set to indicate that an error has occurred during an attempt to execute a command. Cleared by the initiation of a new command and by the INIT signal.
14–08	Not Used	
07	DONE	Done – A read-only bit set to indicate the completion of a function. When set, results in an interrupt request provided the INT ENB (bit 06) is set.
06	INT ENB	Interrupt Enable – A read/write bit set by the program to enable an interrupt request when the disk drive has completed an operation (DONE bit set). Cleared by the INIT signal.
05	Not Used	
04	UNIT SEL	Unit Select – A read/write bit used to select disk drive 0 or 1. In a PDT-11/150 single drive unit, the drive is always 0. 0 = disk drive 0 1 = disk drive 1
03–01	FUNC SEL	Function Select – Three write-only bits used to select the operation associated with the selected drive as follows. **Code** — **Function** 000 — Fill buffer 001 — Empty buffer 010 — Write sector 011 — Read sector 100 — Initialize 101 — Read status 110 — Write deleted data sector 111 — Restore GO – A write-only bit; when set, initiates a command selected by bits 01–03 to the drive selected by bit 4.

Fill Buffer (000)
The fill buffer function is used to load the interface buffer with 64 16-bit words of data from the microprocessor memory. After loading, the contents of the buffer can be written onto a disk by a write sector function (010) or returned to the microprocessor by an empty buffer function (001). DONE (bit 07) is cleared at the start of the function and set when all 64 words are stored.

NOTE
To prevent loss of data, only 16-bit words, not 8-bit bytes, can be transferred during a fill buffer command. DONE (bit 07) will not be set at the completion of the transfer, when less than 64 words are loaded.

The UNIT SEL (bit 04) is not required for this function because no data transfer to a drive is specified.

Empty Buffer (001)
The empty buffer function transfers 64 words of data, previously loaded by a read sector (011), initialize (100) or fill buffer (000) function, to the microprocessor. DONE (bit 07) is cleared at the start of the command and set when all 64 words have been transferred.

NOTE
This function does not destroy the interface buffer content.

Write Sector (010)
The write sector command will write the 64 words of data stored in the interface buffer onto the disk sector that is specified by the track and sector address of the RXSA. The track and sector address must be issued prior to this command. Following the data information, a 16-bit CRC character will be written within the sector.

The initiation of this command clears all the status bits in the RXES register.

DONE (bit 07) is cleared at the start of the function and set at the completion of the operation.

If the specified sector has not been located within two revolutions of disk, ERR (bit 15) and DONE (bit 07) will be set and a program interrupt will be requested if INT ENB (bit 06) has been previously set.

NOTE
A write sector command issued after a power interruption of the PDT-11/150 may result in the recording of random data onto the disk from the buffer.

Read Sector (011)
The read sector command causes 64 16-bit words of data from a specified sector on the disk to be read and loaded into the interface buffer. The track and sector address information of the RXSA must be issued prior to this instruction. The initiation of this command clears all the status bits in the RXES register. DONE (bit 07) is cleared at the start of the function and set at the completion of the operation.

If the specified sector or track has not been located within two revolutions of the disk, ERR (bit 15) and DONE (bit 07) will be set and a program interrupt will be requested if the INT ENB (bit 06) was previously set.

If a deleted data address mark is detected after the sector is located the interface will set DEL DATA DET (bit 05) of RXES and ERR (bit 15) and DONE (bit 07) of the RXCS. A program interrupt will be generated at completion provided INT ENB (bit 06) was previously set. The contents of the RXES status register will then be available by reading the RXDB.

As data is loaded into the interface buffer, a CRC is computed based on the information in the data field, and compared with the 16-bit CRC character recorded on disk. If the two CRC characters are different, a read error is detected and CRC ERR (bit 03) of the RXES is set, and ERR (bit 15) and DONE (bit 07) of RXCS are set. A program interrupt will be requested at completion provided the INT ENB (bit 06) was previously set. The contents of the RXES status register will then be available by reading the RXDB.

Initialize (100)
The initialize command clears the registers and buffers within the disk drive interface and performs a restore followed by a read operation at sector 1, of track 1, of drive 0. In a two-disk drive unit, a restore operation will be performed on both drive 0 and drive 1 prior to reading data at drive 0. At the start of the command, DONE (bit 07) will be cleared. At the end of the command, bit 07 will be set. Upon completion of a successful initialize operation, the ERR (bit 15) of the RXCS and all RXES status bits will be cleared, except for DR RDY (bit 07) and INIT DONE (00) which will be set.

CAUTION

During power-up, an initialize command is automatically issued, and no programmed command can be issued until DONE (bit 07) is set indicating the initialize operation has been completed.

Read Status (101)
The read status command assembles the current status of the selected drive in the RXES for transfer to the program through the RXDB. At the start of the operation, DONE (bit 07) RXCS is cleared. The DR RDY (bit 07) of the RXES will reflect the status of the drive selected by UNIT SEL (bit 04) of the RXCS at the time the command was issued. At the completion of the operation, DONE (bit 07) will be set and an interrupt request will be generated provided the INT ENB (bit 06) was previously set. The contents of the RXDB can then be sampled to obtain the RXES.

Write Sector with Deleted Data (110)
This command initiates an operation similar to the write sector (010) command except that a deleted data address mark, instead of a standard data address mark, precedes the data field.

Restore (111)
The restore command moves the read/write head of the selected drive over track 0. At the completion of the command DONE (bit 07) is set, and an interrupt request is generated provided the INT ENB (bit 06) has been previously set.

5.6.2 Disk Controller Data Buffer Register (RXDB)
The RXDB provides a general purpose data path between the disk drives and the interface. All data information to and from the disk is transferred through this register. The register also contains the current error and status conditions for the disk specified at the completion of a disk function (RXES).

CAUTION

Either data or status information may be present in this register; therefore, violation of the protocol in the manipulation of this register may result in loss of data.

Figure 5-10 shows the RXDB register format during data transfers and Table 5-20 describes the function of the bits.

Table 5-20 Disk Controller RXDB Bit Descriptions

Bit	Name	Description
15–00	DISK CHAR	Disk Character – A 16-bit word that reflects the disk serial information read or to be written on the disk. All information to and from the floppy disk is transferred through the RXDB as word transfers only.

Figure 5-10 shows the RXES error and status information format at the completion of a function and Table 5-21 describes the function of each bit.

Table 5-21 Disk Controller RXES Bit Descriptions

Bit	Name	Description
15–08	Not Used	
07	DR RDY	Drive Ready – A read-only bit set when the following conditions exist. 1. Selected drive is present. 2. Selected drive has power. 3. Selected drive has disk properly installed with door closed and has reached operating speed. If a function FUNC SEL (bits 03–01 of RXCS) is issued prior to the above conditions, ERR (bit 15) and DONE (bit 07) of the RXCS will be asserted. DR RDY bit is valid only when retrieved during a read status function or at completion of initialize when it indicates the status of drive 0.
06	Not Used	
05	DEL DATA DET	Deleted Data Detected – A read-only bit, set to indicate that the identification mark preceding the data field was decoded as a deleted mark during data recovery function.
04	REC NOT FND	Record Not Found – A read-only bit, set to indicate that the specified track and sector were not located within two revolutions of the disk during a write or read operation. This condition results in ERR (bit 15) and DONE (bit 07) of the RXCS being set.

Table 5-21 Disk Controller RXES Bit Descriptions (Cont)

Bit	Name	Description
03	CRC ERR	Cycle Redundancy Check Error – A read-only bit set to indicate a cycle redundancy check error was detected as the information was retrieved from a data field on the disk. This condition results in ERR (bit 15) and DONE (bit 07) of the RXCS being set.
02	LOST DATA	Lost Data – A read-only bit set to indicate that the disk controller failed to respond to a data request in one byte time. This condition sets ERR (bit 15) and DONE (bit 07) of the RXCS.
01	INV MED ADRS	Invalid Media Address – A read-only bit, set to indicate that either the track or sector address was not within the range of valid addresses. This condition sets ERR (bit 15) and DONE (bit 07) of the RXCS.
00	INIT DONE	Initialize Done – A read-only bit set at the completion of the initialize routine. (Refer to Paragraph 5.5.1.1).

5.6.3 Disk Controller, Track and Sector Register (RXSA)

The RXSA is programmed with the appropriate track and sector address information where the data is to be written on or read from the disk. Table 5-22 describes the formats for each address.

Table 5-22 Disk Controller RXSA Bit Descriptions

Bit	Name	Description
15	Always 0	
14–08	TRK SEL	Track Select – Seven read/write bits used to select one of the 77 tracks ($0–114_8$) on the disk for the read or write function selected.
07–05	Always 0	
04–00	SECT SEL	Sector Select – Five read/write bits used to select one of the 26 sectors ($1–32_8$) of each track on a disk for the read or write function selected.

5.7 LINE TIME CLOCK (LTC)

The line time clock provides a real-time indication to the program at 16.6 ms intervals. The line time clock initiates an interrupt request every 16.6 ms provided the INT ENB (bit 06) of the TCSR shown in Figure 5-11 is set. A program reset instruction from the microprocessor will enable the LTC by setting the INT ENB bit. Table 5-23 defines the bits associated with the TCSR. The LTC can be disabled by the S1-2 switch on the Peripheral module. Refer to Table 5-24.

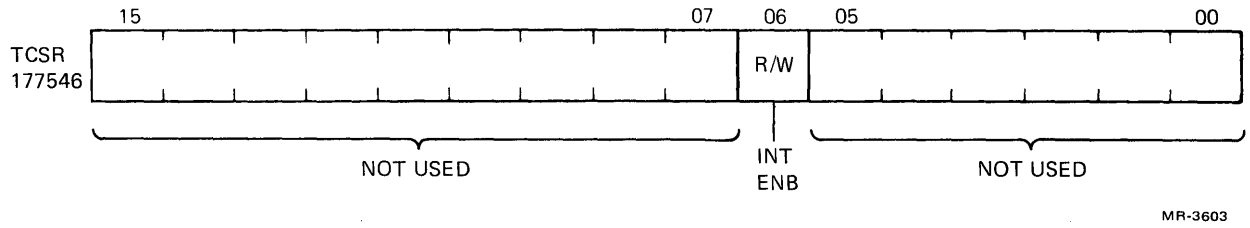


Figure 5-11 Line Time Clock (TCSR) Format

Table 5-23 Line Time Clock Control/Status Register (TCSR)

Bit	Name	Description
15–07	Not Used	
06	INT ENB	Interrupt Enable – Set by the program to allow an interrupt request to be generated every 16.66 ms. Set by the INIT signal.
05–00	Not Used	

Table 5-24 Function Control Switch Pack Selections

Switch No.	Function
1 Autobaud	OFF position – Enables the autobaud function which allows the PDT-11/150 to monitor the baud rate of the console terminal and select the same baud rate for the console terminal interface. During normal, maintenance (refer to switch no. 5), and test mode, when LED no. 2 lights on the indicator panel the operator is required to press the "@" key of the console keyboard two consecutive times. When the baud rate is established, the LED no. 2 light will go off. ON position – The PDT-11/150 defaults to a console baud rate of 9600. In either the ON or OFF position the PDT-11/150 assumes the transmit/receive character to be eight bits, no parity, and one stop bit (two stop bits for the 110 baud rate only).
2 Line Time Clock	OFF position – Enables the internal line time clock to generate an event program interrupt every 16.6 ms to the LSI-11 microprocessor. ON position – Disables the line time clock to inhibit the event program interrupt.
3 Dynamic Memory Refresh	OFF position – Enables the LSI-11 dynamic RAM memory to be refreshed every 1.0 ms. ON position – Disables the dynamic RAM memory function.

Table 5-24 Function Control Switch Pack Selections (Cont)

Switch No.	Function
4 Test Mode	OFF position – Prevents the self-test mode from being selected by the mode switch on the rear panel of the PDT-11/150. (Refer to Table 3-2). ON position – Allows the self-test mode to be selected by the mode switch on the rear panel.
5 Manufacture Mode	OFF position – Disables the manufacture mode which requires operator response from the console keyboard during performance of the self-test functions. (Refer to Paragraph 3.3.2). ON position – Enables the manufacture mode which eliminates the requirements of operator response from the console keyboard during the performance of the self-test functions.

5.8 FUNCTION CONTROL SWITCH SELECTIONS

Table 5-24 lists the functions of the switches on switch pack S1 located on the Peripheral module.

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