LSI-11 Systems Service Manual

FOR INTERNAL USE ONLY

Preliminary, April 1978
1st Edition, March 1979
1st Edition (Rev), September 1979
2nd Edition, November 1980
3rd Edition, August 1981

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

CONTENTS

SYSTEMS CONFIGURATIONS

GENERAL CONFIGURATION RULES

PDP-11V03 AND PDP-11T03 SYSTEMS

PDP-11T03-L AND PDP-11V03-L SYSTEMS

PDP-11V23 AND PDP-11T23 SYSTEMS

CONTENTS (CONT)

CONTENTS (CONT)

CPU/OPTIONS

CONTENTS (CONT)

CONTENTS (CONT)

SYSTEMS CONFIGURATIONS

GENERAL CONFIGURATION RULES

GENERAL CONFIGURATION RULES

The rules and considerations discussed in this section apply to all LSI-11 systems. Refer to subsequent sections for requirements peculiar to specific systems.

Backplanes

LSI-11 systems can be divided into two types: those that use only one backplane, and those that have multiple backplanes. Single backplane systems are viewed as lumped capacitance. Multiple backplane systems are regarded as transmission line systems. The characteristics of the two types differ enough to require separate sets of configuration rules. The rules are given in terms of power consumption, dc bus loading, and ac bus loading. DC loading is a measure of the leakage current a module's bus signal lines draw when high (undriven). One dc load is nominally 105 μA. AC loading is a measure of the capacitance a module adds to the bus signal lines. One ac load is 9.35 pF. Backplanes also add ac loading to the bus. The power consumption, dc loading, and ac loading is listed for each module in the "CPU/Options" section.

Configuring Single Backplane Systems

1. The bus can support up to 20 ac loads before additional termination is required. The processor has on-board termination for one end of the bus, and after 20 ac loads, the other end of the bus must be terminated with 120 Ω.

2. A terminated bus can support up to 35 ac loads.

3. The bus can support up to 20 dc loads.

4. The bus signal lines on the backplane can be up to 35.6 cm (14 in) long.

The preceding rules apply only to single backplane systems. The bus cannot be extended off the backplane in any way. If it is, the system is considered a multiple backplane system.

Configuring Multiple Backplane Systems

1. a. Up to three backplanes may be connected together.

   b. The signal lines on each backplane can be up to 25.4 cm (10 in) long.

2. Each backplane can have up to 20 ac loads. Unused ac loads from one backplane may not be added to another backplane if the second backplane loading will exceed 20 ac loads. It is desirable to load backplanes equally or with the highest ac loads in the first and second backplanes.

3. Total dc loading of all three backplanes combined can be up to 20 loads.

4. Both ends of the transmission line should be terminated with 120 Ω. This means that the first backplane should have impedance of 120 Ω, and the last backplane should have a termination of 120 Ω.

5. a. The cable connecting the first two backplanes should be at least 1.83 meters (6 ft) long.

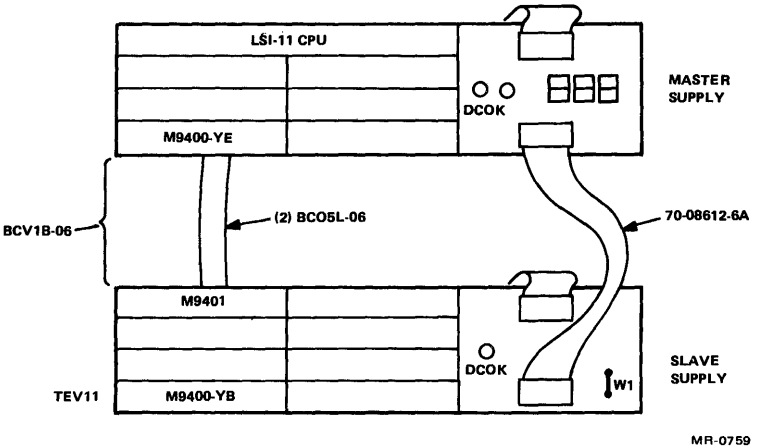
   b. The cable connecting the second backplane to the third backplane must be at least 1.22 m (4 ft) longer or shorter than the cable connecting the first and second backplanes.

   c. The combined length of the cables should not exceed 4.88 m (16 ft).

   d. The cables used must have a characteristic impedance of 120 Ω.

Power Supplies

The "CPU/Options" section lists the typical power requirements for each module. For reliable operation, the sum of all typical current requirements should be less than 70 percent of the maximum rated current of the power supply. Refer to the appropriate power supply section for voltage and current ratings.

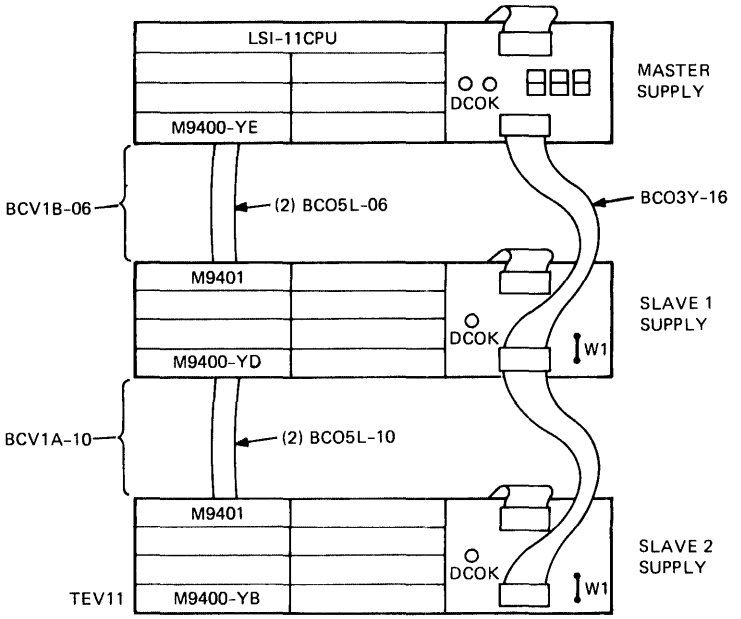


A Typical System Configuration Using BA11-M Boxes Showing Cables Needed for Expansion

NOTE

Expander boxes are normally shipped with W1 installed. This enables the slave power supply to be powered up and down without being cabled to the master supply. For system applications, however, it is recommended that W1 be removed. This will ensure that the slave supply does not power up unexpectedly if the cable is loosened.

Business Products systems (D322 and D324) do not use a PDP-11/03-J slave console. The two power supplies are connected by a cable (DEC part number (PN) 70-13371-00). No slave board is needed. In a standalone device, such as the RKV11-D disk drive controller, the W1 jumper must be installed and is not removed if it is added to a system.



NOTE:
THE TWO (2) BC05L-XX CABLE LENGTHS BETWEEN THE FIRST AND SECOND BOX SHOULD DIFFER FROM THE BC05L-XX CABLE LENGTHS BETWEEN THE SECOND AND THIRD BOX BY AT LEAST FOUR FEET BECAUSE OF LSI-11 BUS REFLECTIONS.

MR-2370

Typical System Configuration Using Three BA11-M Boxes Showing Cables Needed for Expansion

Master/Slave Interface Cables

Length		DEC PN
10.2 cm	(4 in)	70-08612-0D
15 cm	(6 in)	70-08612-0F
22.9 cm	(9 in)	70-08612-0K
27.5 cm	(11 in)	70-08612-0M
35.6 cm	(14 in)	70-08612-1B
45.7 cm	(18 in)	70-08612-1F
124 cm	(49 in)	70-08612-4A
61.0 cm	(2 ft)	70-08612-02
1.83 m	(6 ft)	70-08612-6A
3.05 m	(10 ft)	70-08612-10

Possible Problems Installing the 70-08612 or BC03Y-XX Cables
On a two box system, connect the remote sockets on the master console and the slave console with a 70-08612-XX cable.

NOTE

Some of the 70-08612 cables have been found with a connector on backwards. If the DCOK LED on the slave box does not come on when the master is turned on, the cable may be reversed.

If RT-11's clock does not update, the 70-08612 cable may be in upside down. The cable should be connected pin 1 to pin 1. The red line should be on the left of both J2 connectors.

Possible Problems Installing BC05L
Some BC05L-XX cables may have the "This Side Up" stickers on the wrong side of one end. The cables should be connected as follows.

- M9400-YE or YD pin AA (J1)
  to
  BC05L-XX pin 1

- BC05L-XX pin 1
  to
  M9401 pin AA (J1)

The pin markings on the BC05L cables are on the connector. The cables should be flat when run around the PDP-11/03 cable trays, and not twisted.

If the BC05L-XX is plugged in upside down, the bus DCOK line is grounded. The processor will not power up with this condition. Reverse the cables and try again.

MEMORY

Memory Refreshing Rules

All dynamic MOS RAM must be refreshed. Neither CORE RAM nor ROM/PROM memories need refreshing. Refreshing is available by three means: processor microcode, Direct Memory Access (DMA), and self-refreshing memory modules.

Processor Microcode Refresh – With processor microcode refresh, the processor must be strapped to enable the microcode refresh, and the memory module farthest from the processor on the bus must be configured to reply to refresh cycles. All other memory modules, including memory on the processor board itself, must have memory reply disabled. If only the 4K of RAM on the processor is being used, then that RAM must be strapped to respond to reply.

NOTE

Only quad-sized processor modules have microcode refresh capabilities. Double-sized processor modules do not. With double-sized processors, either DMA refresh or self-refreshing memory must be used.

DMA Refreshing – The REV11-A or REV11-C modules may be used to provide DMA memory refreshing. When using the REV11 to refresh memory, the REV11 refresh capability must be enabled via a strap on the REV11 board, and the processor microcode refreshing must be disabled. The memory module farthest from the REV11 should have reply to refresh enabled. If a quad-sized processor module with on-board RAM is used, usually that RAM will be the one strapped to reply to the refresh because it will be the farthest from the REV11 option.

DMA memory refreshing can be done by a customer's own module if that module makes sufficient memory accesses within the required time.

Self-Refreshing Memory – Self-refreshing memory does not use the bus to accomplish refreshing; therefore, no memory module need be strapped to reply to a memory refresh cycle.

Self-refreshing memory can be combined with nonself-refreshing memory on the same bus; however, when this is done, other refreshing techniques similar to processor microcode or DMA must be used to refresh the conventional memory. If an MSV11-C is used with a KD11-F or an MSV11-B, configure the MSV11-C for external refresh.

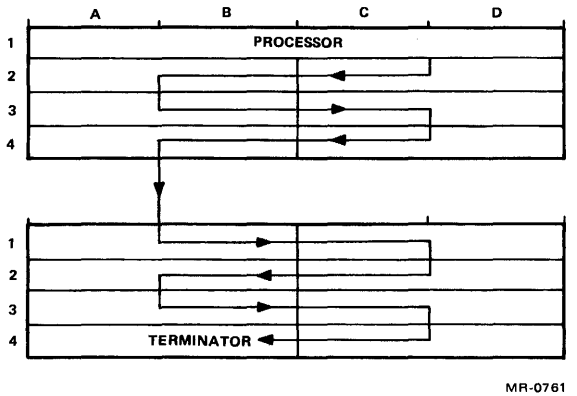
DMA Refresh Configuration

In systems that use a REV11-C for refresh and a TEV11 for bus termination, the REV11-C should be placed immediately after the memory modules.

DRV11-B or RKV11-D modules should follow the REV11-C in order to be lower in DMA priority.

Systems that use a REV11-A for both refresh and termination must have it in the last slot.

No open slots are permitted between the processor and the far-end bus terminator. The DMA and interrupt priority scheme is indicated in the following figure. The arrow indicates decreasing priority.



Q-Q Backplanes DMA/Interrupt Priority Scheme

Configuration Examples

If an LSI-11 system must be configured with memories other than the MSV11-CD, try to use one of the following engineering-approved examples.

Ex. 1

M7264-0, -AB, -BB CPU	
M7944 MSV11-B 4K MEMORY	M7940 DLV11 SLU
M7944 MSV11-B 4K MEMORY	M9400-YA REV11-A BOOT/TERMINATOR

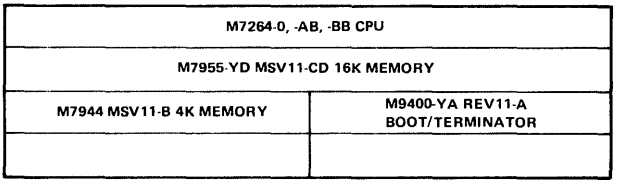
MR-0798

In this type of configuration, use the M9400 (REV11) to perform refresh operations.

Jumpers would be as follows.

M7264	W4	IN	Disable CPU controlled refresh.
	W9	OUT	Enable reply from CPU memory.
	W10	OUT	Enable CPU reply during refresh.
M7944	W4	IN (both modules)	Disable reply during refresh.
M9400-YA	W2	IN	Enable DMA refresh.

Ex. 2



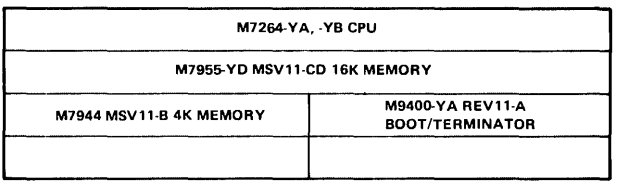
MR-0799

In this type of configuration, use REV11 to control refresh operations.

Jumpers would be as follows.

M7264	W4	IN	
	W9	OUT	
	W10	OUT	
M7955	W7	OUT	Disable internal refresh.
	W6	IN	Disable reply during refresh.
M9400-YA	W2	IN	

Ex. 3



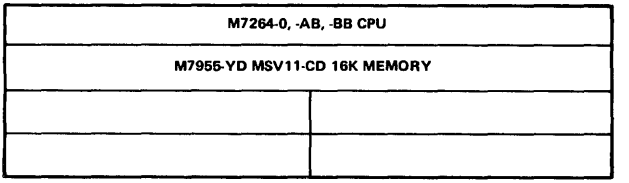
MR-0800

In this type of configuration, use REV11.

Jumpers would be as follows.

M7264	W4	IN	Disable CPU refresh.
	W9	IN	Disable reply from CPU memory.
	W10	OUT	This is a "don't care" (if W9 is in).
M7955	W7	OUT	Disable internal refresh.
	W6	OUT	Enable reply during refresh.
M7944	W4	IN	Disable reply during refresh.
M9400-YA	W2	IN	Enable DMA refresh.

Ex. 4



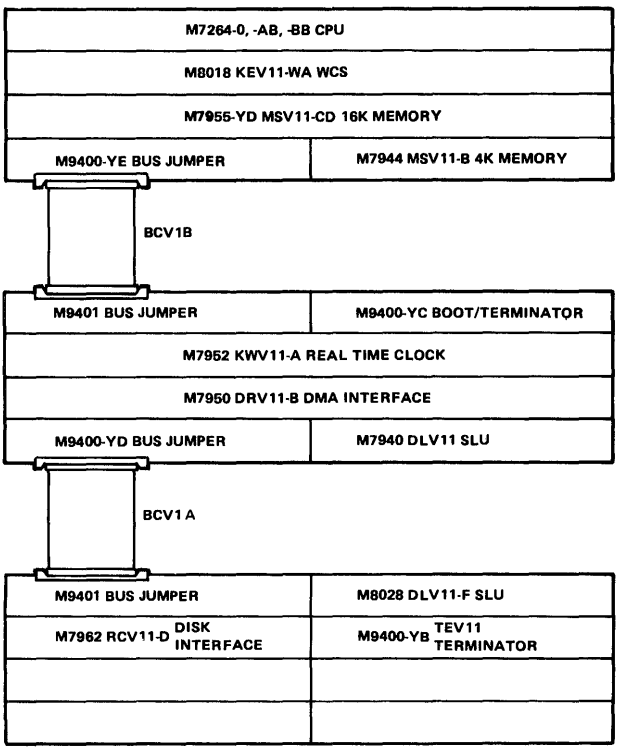
MR-0801

In this type of configuration, use CPU refresh.

Jumpers would be as follows.

M7264	W4	OUT	Enable CPU refresh.
	W9	OUT	Enable reply from CPU memory.
	W10	IN	Disable CPU reply during refresh.
M7955	W7	OUT	Disable internal refresh.
	W6	OUT	Enable reply during refresh.

Ex. 5



MR-0802

In this type of configuration, use the REV11-C (M9400-YC) to provide refresh.

Jumpers would be as follows.

M7264	W4	IN	Disable CPU controlled refresh.
	W9	OUT	Enable reply from CPU memory.
	W10	OUT	Enable CPU reply during refresh.
M7955	W7	OUT	Disable internal refresh.
	W6	IN	Disable reply during refresh.
M7944	W4	IN	Disable reply during refresh.
M9400-YC	W2	IN	Enable DMA refresh.

Do not use any configuration with DMA devices between the CPU and a REV11 performing DMA refresh.

The BDV11 (M8012) is always at end of the bus.

The preferred order of modules in systems is:

CPU
WCS
Memory
DMA refresh
Real time clock
INT fastest
↓
slowest
DMA fastest
↓
slowest
Program transfer (ROMs, D/As, etc.)
Terminator

REFRESH CONFIGURATION PROCEDURE

1 Is this CPU a KD11-H (M7264-YA)?

YES NO

- Go to step 6

2 Does the system contain an MSV11-B (M7944) memory?

YES NO

- The CPU should have jumpers W10 and W4 installed.
- If the system has a REV11-A (M9400-YA) or a REV11-C (M9400-YC), jumper W2 should be removed.
- If the system has MSV11-CD (M7955) memories, jumpers W6 and W7 should be installed in the MSV11-CD.
- If the system has:

  MSV11-DA M8044-YA
  MSV11-DB M8044-YB
  MSV11-DC M8044-YC
  or
  MSV11-DD M8044-YD

  there are no refresh configuration requirements for this module.

3 Does the system contain a DMA device other than the REV11-A (M7900-YA) or a REV11-C (M9400-YC), such as an RKV11-D (M7969) or DRV11-B (M7950)?

YES NO

- Does the system contain a REV11-A (M9400-YA) or REV11-C (M9400-YC)?

  YES NO

  - Is the CPU a DIBOL processor (40-pin chip with 2 dies)?

NO YES

- You cannot configure this system without a REV11.

- The CPU (M7264-YA) should control refresh; jumper W4 removed and W10 installed.

- The MSV11-B (M7944) farthest from the CPU will reply; jumper W4 removed.

- All other MSV11-B memories should have W4 installed.

- If the system has MSV11-CD (M7955) memories, jumpers W6 and W7 should be installed.

- If the system has:

  MSV11-DA M8044-YA
  MSV11-DB M8044-YB
  MSV11-DC M8044-YC
  or
  MSV11-DD M8044-YD

  there are no refresh configuration requirements for this module.

- The REV11-A (M9400-YA) or REV11-C (M9400-YC) should control refresh; jumper W2 on the M9400 should be installed.

- The MSV11-B (M7944) farthest from the REV11 should reply to refresh; W4 removed.

- All other MSV11-B memories should have W4 installed.

- The CPU should not control refresh; jumpers W4 and W10 installed.

- If the system has MSV11-CD (M7955) memories, jumpers W6 and W7 should be installed.

- If the system has:

  MSV11-DA M8044-YA
  MSV11-DB M8044-YB

MSV11-DC M8044-YC
or
MSV11-DD M8044-YD

there are no refresh configuration requirements for this module.

4 Does the system contain a REV11-C (M9400-YC)?

NO YES

- The REV11-C (M9400-YC) should control refresh; W2 installed.
- The MSV11-B (M7944) farthest from the REV11 should reply to refresh; jumper W4 removed.
- All other MSV11-B (M7944) memories should have W4 installed.
- There should not be a DMA device placed between the CPU and REV11-C (M9400-YC).
- If the system has MSV11-CD (M7955) memories, jumpers W6 and W7 should be installed.
- If the system has:

  MSV11-DA M8044-YA
  MSV11-DB M8044-YB
  MSV11-DC M8044-YC
  or
  MSV11-DD M8044-YD

  there are no refresh configuration requirements for this module.

5 Is the CPU a DIBOL processor (40-pin chip with 2 dies)?

NO YES

- You cannot configure refresh on a system without a REV11-C.

- The CPU (M7264-YA) must control refresh; jumper W10 installed and W4 removed.

- If a REV11-A (M9400-YA) is present, its refresh must be disabled. This means jumper W2 must be removed.
- The MSV11-B (M7944) farthest from the CPU should respond to refresh; jumper W4 removed.
- All other MSV11-Bs (M7944) should have W4 installed.
- If the system has MSV11-CD (M7955) memories, jumpers W6 and W7 should be installed.
- If the system has:

  MSV11-DA M8044-YA
  MSV11-DB M8044-YB
  MSV11-DC M8044-YC
  or
  MSV11-DD M8044-YD

  there are no refresh configuration requirements for this module.

FROM 1, 5

6 Does the system contain a REV11-A (M9400-YA) or REV11-C (M9400-YC)?

YES

NO

- Is the CPU a DIBOL CPU (40-pin chip with 2 dies)?

NO

YES

- You cannot configure this system without a REV11.

- Does the system contain an MSV11-B (M7944)?

YES

NO

- The CPU (M7264) must control refresh and reply to refresh; jumpers W4 and W10 removed.
- The MSV11-B (M7944) farthest from the CPU should reply to refresh; jumper W4 removed.
- All other MSV11-Bs (M7944) should have jumper W4 installed.

- If the system has:

  MSV11-DA M8044-YA
  MSV11-DB M8044-YB
  MSV11-DC M8044-YC
  or
  MSV11-DD M8044-YD

  there are no refresh configuration requirements for this module.

- The CPU must control refresh; jumper W4 removed and W10 installed.

- The MSV11-B (M7944) farthest from the CPU should reply to refresh; jumper 4 removed.

- All other system MSV11-Bs (M7944) should have jumper W4 installed.

- If the system has MSV11-CD (M7955) memories, jumpers W6 and W7 should be installed.

- If the system has:

  MSV11-DA M8044-YA
  MSV11-DB M8044-YB
  MSV11-DC M8044-YC
  or
  MSV11-DD M8044-YD

  there are no refresh configuration requirements for this module.

7 Does the system contain a DMA device other than that of the REV11-A (M9400-YA) or a REV11-C (M9400-YC), such as RKV11-B (M7969) or DRV11-B (M7950)?

YES NO

- Does the system contain MSV11-B (M7944) memory?

YES NO

- The REV11-YA (M9400-YA) or REV11-C (M9400-YC) should control refresh; jumper W2 installed.

- The CPU should reply to refresh; jumper W4 installed and W10 removed.

- All MSV11-B (M7944) memories should have jumper W4 installed.

- If the system has MSV11-CD (M955) memories, jumpers W6 and W7 should be installed.

  If the system has:

  MSV11-DA M8044-YA
  MSV11-DB M8044-YB
  MSV11-DC M8044-YC
  or
  MSV11-DD M8044-YD

  there are no refresh configuration requirements for this module.

- The REV11-A (M9400-YA) or REV11-C (M9400-YC) should control refresh; jumper W2 installed.

- The MSV11-B (M7944) farthest from the REV11-A (M9400-YA) or REV11-C (M9400-YC) should reply to refresh; jumper W4 removed.

- The CPU should not reply to refresh; jumper W4 installed and W10 installed.

- All remaining MSV11-B memories should have W4 installed.

- If the system has MSV11-CD (M7955) memories, jumpers W6 and W7 should be installed.

- If the system has:

  MSV11-DA M8044-YA
  MSV11-DB M8044-YB
  MSV11-DC M8044-YC
  or
  MSV11-DD M8044-YD

  there are no refresh configuration requirements for this module.

8 Does the system contain a REV11-C (M9400-YC)?

YES

NO

- Is the CPU a DIBOL processor (40-pin chip with 2 dies)?

NO

YES

- You cannot configure this system without a REV11.

- Does the system contain MSV11-B (M7944) memory?

YES

NO

- The CPU (M7264) should control refresh and reply; jumpers W4 and W10 removed.
- If the system has a REV11-A (M9400-YA); jumper W2 should be removed.
- If the system has MSV11-CD (M7955) memories, jumpers W6 and W7 should be installed.
- If the system has:

  MSV11-DA M8044-YA
  MSV11-DB M8044-YB
  MSV11-DC M8044-YC
  or
  MSV11-DD M8044-YD

  there are no refresh configuration requirements for this module.

- The CPU (M7264) should control refresh; jumper W4.
- The MSV11-B (M7944) farthest from the CPU should reply to refresh; jumper W4 removed.
- All remaining MSV11-Bs (M7944) should have jumper W4 installed.
- If the system has a REV11-A (M9400-YA), jumper W2 should be removed.
- If the system has MSV11-CD (M7955) memories, jumpers W6 and W7 should be installed.

- If the system has:

  MSV11-DA M8044-YA
  MSV11-DB M8044-YB
  MSV11-DC M8044-YC
  or
  MSV11-DD M8044-YD

  there are no refresh configuration requirements for this module.

9 Does the system have MSV11-B (M7944) memory?

YES NO

- The REV11-C (M9400-YC) should control refresh; jumper W2 installed.
- The CPU (M7264) should reply to refresh; jumper W10 removed and W4 installed.
- If the system has MSV11-CD (M7955) memories, jumpers W6 and W7 should be installed.
- If the system has:

  MSV11-DA M8044-YA
  MSV11-DB M8044-YB
  MSV11-DC M8044-YC
  or
  MSV11-DD M8044-YD

  there are no refresh configuration requirements for this module.

10 Is the CPU an M7264-EB, -FB, -HB, or -JB?

YES NO

- The REV11-C (M9400-YC) should control refresh; jumper W2 installed.
- The CPU should reply to refresh; jumper W10 removed and W4 installed.
- All MSV11-B (M7944) memories should have jumper W4 installed.

- If the system has MSV11-CD (M7955) memories, jumpers W6 and W7 should be installed.

- If the system has:

  MSV11-DA M8044-YA
  MSV11-DB M8044-YB
  MSV11-DC M8044-YC
  or
  MSV11-DD M8044-YD

  there are no refresh configuration requirements for this module.

- The REV11-C (M9400-YC) should control refresh; jumper W2 installed.

- The MSV11-B (M7944) farthest from the REV11-C should reply to refresh; jumper W4 removed.

- All other MSV11-Bs (M7944) should have jumper W4 installed.

- The CPU should have jumpers W4 and W10 installed.

- If the system has MSV11-CD (M7955) memories, jumpers W6 and W7 should be installed.

- If the system has:

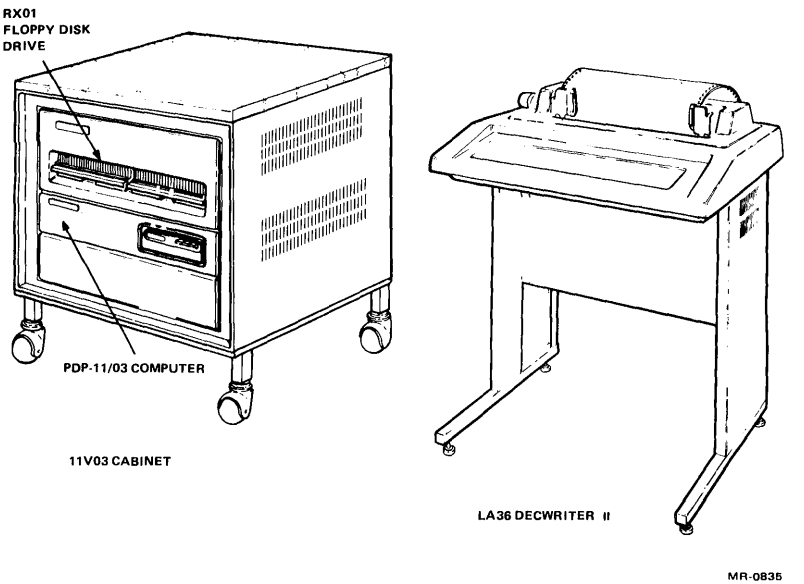
  MSV11-DA M8044-YA
  MSV11-DB M8044-YB
  MSV11-DC M8044-YC
  or
  MSV11-33 M8044-YD

  there are no refresh configuration requirements for this module.

PDP-11V03 AND PDP-11T03 SYSTEMS

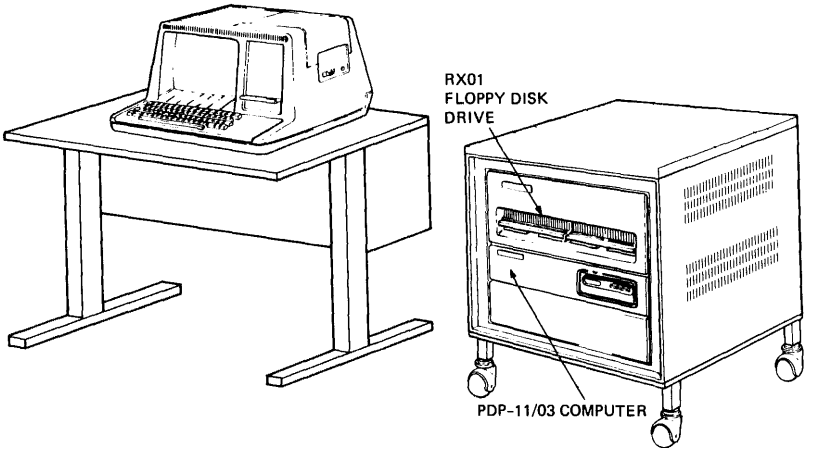
PDP-11V03

The PDP-11V03 includes a PDP-11/03 computer, an RX01 dual floppy disk drive, and either a VT52 DECscope or an LA36 DECwriter II. Early models have 8K of memory, while later models have 16K. All models are configured to boot on power-up and halt on BREAK. The figures and tables that follow describe the models, specifications, and components.



PDP-11V03-E/H

PDP-11V03

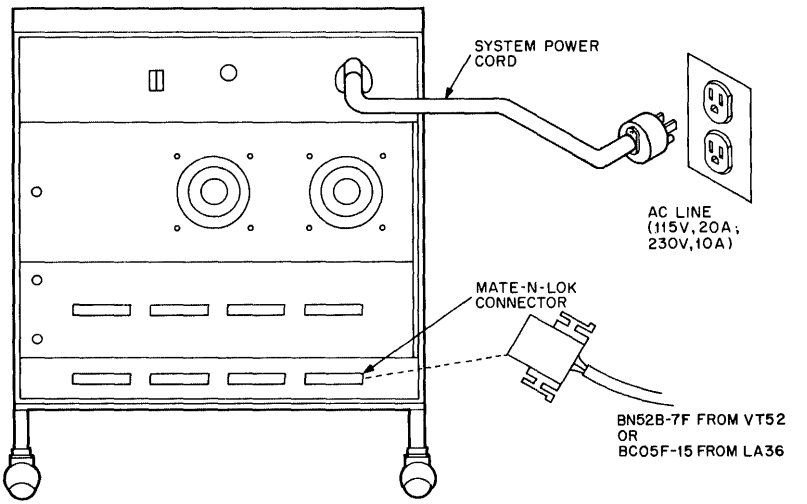


VT52 DECSCOPE

11V03 CABINET

MR-0836

PDP-11V03-A/F



MR-0837

	LA36	VT52
8K words	EA ED	AA AD
16K words	HA HB HC	FA FB FC

PDP-11V03 System Model Designations

8K System Component Model Designations

System Requirements	PDP-11V03 System Model Designations			
	AA	AD	EA	ED
Input Power (V)	115	230	115	230
Frequency (Hz)	60	50	60	50
PDP-11/03 Computer	EA	EB	EA	EB
LA36			DE	DJ
VT52	AA	AB		
RXV11 (RX01 Floppy with Interface)	BA	BD	BA	BD
H984 (Cabinet)	BA	BB	BA	BB

16K System Component Model Designations

System Requirements	PDP-11V03 System Model Designations					
	FA	FB	FC	HA	HB	HC
Input Power (V)	115	230	115	115	230	115
Frequency (Hz)	60	50	50	60	50	50
PDP-11/03 Computer	KA	KB	KA	KA	KB	KA
LA36				DE	DJ	DH
VT52	AA	AB	AC			
RXV11 (RX01 Floppy with Interface)	BA	BD	BC	BA	BD	BC
H984 (Cabinet)	BA	BB	BA	BA	BB	BA

	115 V 50/60 Hz			230 V 50 Hz		
POWER CONNECTOR	PLUG  NEMA # 5-15P DEC # 90-08938	RECEPTACLE  5-15R 12-05351		PLUG  NEMA # 6-15P DEC # 90-08853	RECEPTACLE  6-15R 12-11204	
	CPU CABINET	LA36	VT52	CPU CABINET	LA36	VT52
AMPERAGE TYPICAL MAXIMUM	9.6 10.8	2.0	1.0	4.7 5.3	1.0	0.5
WATTAGE TYPICAL MAXIMUM	800 940	160 300	118 118	820 960	160 300	118 118
BTU/HOUR TYPICAL MAXIMUM	2730 3210	550 1020	400 400	2800 3280	550 1020	400 400
WEIGHT	81.6 Kg (180 lbs)	46.3 Kg (102 lbs)	20.0 Kg (44 lbs)	81.6 Kg (180 lbs)	46.3 Kg (102 lbs)	20.0 Kg (44 lbs)

MR-0838

Modules Included in the Basic System

Processor

KD11-F (M7264) in PDP-11V03-A/E

Resident memory addressed as bank 0
CPU refresh disabled
Powers up to 173000

KD11-R (M7264-YA) in PDP-11V03-F/H

No resident memory
CPU refresh disabled
Powers up to 173000

Memory

MSV11-B (M7944) in PDP-11V03-A/E

4K RAM
Refreshed by REV11-A
Addressed as bank 1

MSV11-CD (M7955-YD) in PDP-11V03-F/H

16K RAM
Internal refresh
Addresses start at bank 0
Part of the KD11-R processor option

Serial Line Interface

DLV11 (M7940)

Device address 177560
Vector 60
300 baud in PDP-11V03-E/H (LA36)
9600 baud in PDP-11V03-A/F (VT52)
20 mA active transmitter and active receiver
One stop bit, eight data bits, no parity
Framing error (BREAK) asserts BHALT

PDP-11V03

Floppy Disk Interface

RXV11 (M7946)

First device address (disk 0) 177170
First vector 264
Second device address (disk 1) 177150
Second vector 270

Bootstrap/Diagnostic/Terminator

REV11-A (M9400-YA)

Bootstrap enabled
Diagnostics enabled
Refresh enabled in PDP-11V03-A/E
Refresh disabled in PDP-11V03-F/H
120 Ω terminator

PDP-11V03-A/E Module Utilization

A	B	C	D	
①	M7264 PROCESSOR (KD11-F)		②	1
④	M7944 (MSV11-B)	M7940 (DLV11)	③	2
⑤	M7946 FLOPPY CONTROL (RXV11)	M9400-YA (REV11-A)	⑥	3
⑧	EMPTY	EMPTY	⑦	4

NOTE: CIRCLED NUMBERS ① THROUGH ⑧ REFER TO DMA AND INTERRUPT PRIORITY SEQUENCE.

MR5919

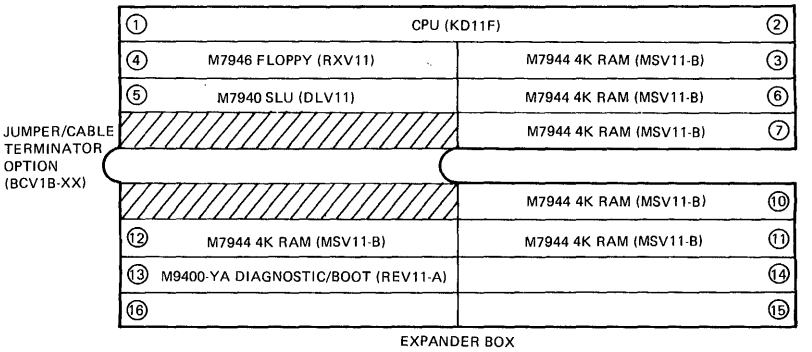
Basic 8K System

A	B	C	D	
①	M7264 PROCESSOR (KD11-F)		②	1
④	M7944 4K MEMORY (MSV11-B)	M7944 4K MEMORY (MSV11-B)	③	2
⑤	M7944 4K MEMORY (MSV11-B)	M7940 SERIAL LINE UNIT (DLV11)	⑥	3
⑧	M9400-YA BOOT/TERMINATOR (REV11-A)	M7946 FLOPPY DISK CONTROLLER (RXV11)	⑦	4

NOTE: CIRCLED NUMBERS ① THROUGH ⑧ REFER TO DMA AND INTERRUPT PRIORITY SEQUENCE.

MR-0839

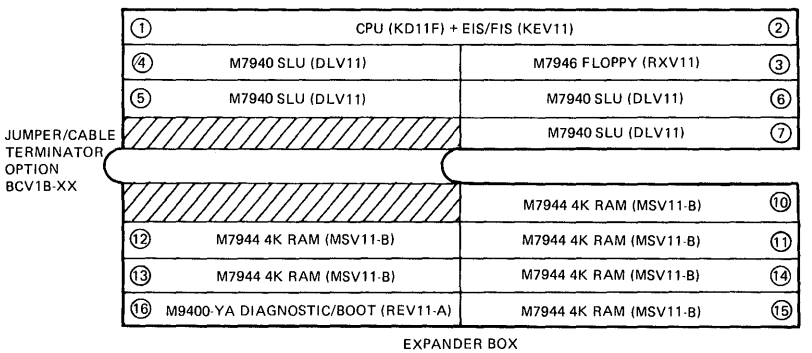
16K System



NOTE: CIRCLED NUMBERS ① THROUGH ⑯ REFER TO DMA AND INTERRUPT PRIORITY SEQUENCE.

11-3720

One-User 28K System

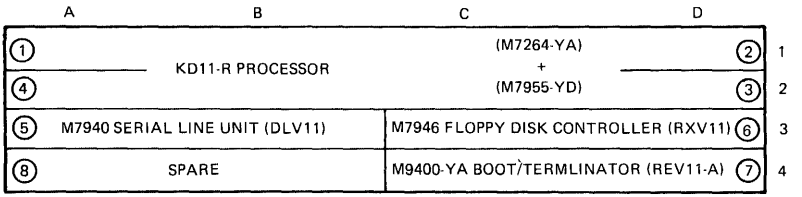


NOTE: CIRCLED NUMBERS ① THROUGH ⑯ REFER TO DMA AND INTERRUPT PRIORITY SEQUENCE.

11-3719

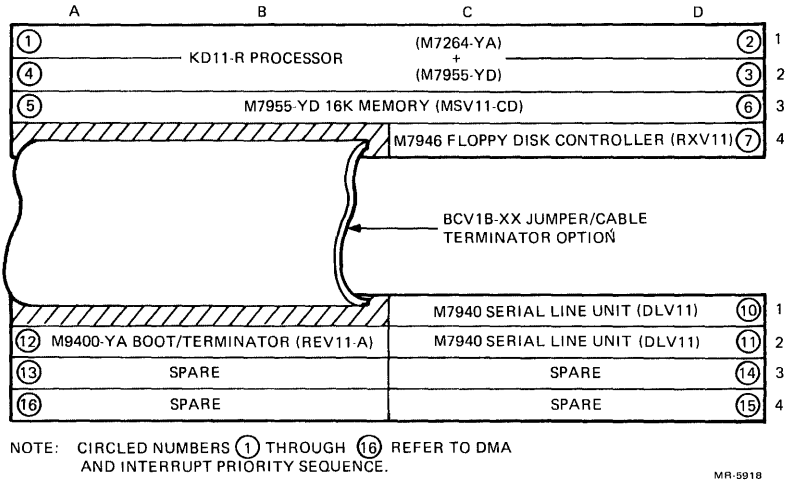
Four-User 28K System with EIS/FIS

PDP-11V03-F/H Module Utilization



NOTE: CIRCLED NUMBERS (1) THROUGH (8) REFER TO DMA AND INTERRUPT PRIORITY SEQUENCE.

Basic 16K System

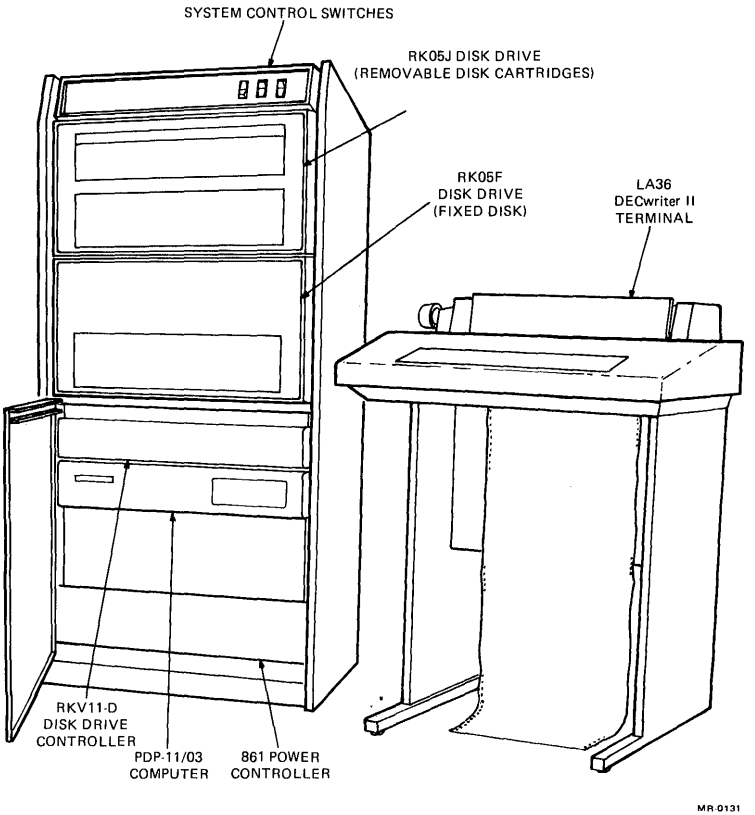


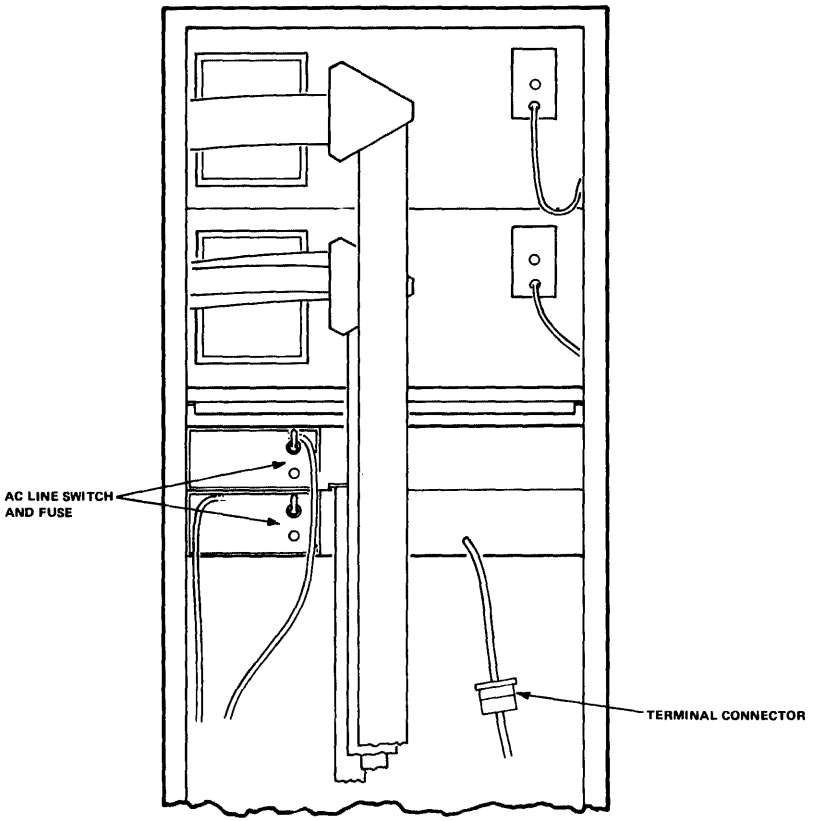
NOTE: CIRCLED NUMBERS (1) THROUGH (16) REFER TO DMA AND INTERRUPT PRIORITY SEQUENCE.

Two-User 28K System

PDP-11T03

The PDP-11T03 comprises a PDP-11/03 computer, two RK05 disk drives, and an LA36 DECwriter II. The basic system includes 16K of memory. The system may be ordered without the LA36. All models are configured to boot on power-up and halt on BREAK. The figures and tables that follow describe the models, specifications, and components.




AC LINE SWITCH
AND FUSE
TERMINAL CONNECTOR
MR-0140

System Component Model Designations

System Requirements	PDP-11T03 System Model Designation							
	AA	AB	AC	AD	BA	BB	BC	BD
Input Power (V)	115	230	115	230	115	230	115	230
Frequency (Hz)	60	60	50	50	60	60	50	50
PDP-11/03 Computer	KA	KB	KA	KB	KA	KB	KA	KB
LA36	DE	DF	DH	DJ				
RKV11-D	A	B	A	B	A	B	A	B
RK05	AA	AB	BA	BB	AA	AB	BA	BB

Specifications

	CPU CABINET		LA36	
	PLUG	RECEPTACLE	PLUG	RECEPTACLE
POWER CONNECTORS				
115 V 50/60 HZ	NEMA # L5-30P DEC # 12-11193	L5-30R 12-11194	NEMA # 5-15P DEC # 90-08938	5-15R 12-05351
230 V 50/60 HZ	 NEMA # L6-20P DEC # 12-11192	 L6 20R 12 11191	 NEMA # 6-15P DEC # 90-08853	 6-15R 12-11204
WATTS	860		300	
BTU/HOUR	2940		1020	
WEIGHT	294.8 KG (650 LBS)		46.4 (102 LBS)	

MR-0764

PDP-11T03

Modules Included in the Basic System

Processor

KD11-S (M7264-YA)

No resident memory
KEV11 EIS/FIS option included
CPU refresh disabled
Powers up to 173000

Memory

MSV11-CD (M7955-YD)

16K RAM
Internal refresh
Addresses start at bank 0
The memory is part of the KD11-R processor option

Serial Line Interface

DLV11 (M7940)

Device address 177560
Vector 60
300 baud
20 mA active transmitter and active receiver
One stop bit, eight data bits, no parity
Framing error (BREAK) asserts BHALT

Disk Drive Interface

RKV11-D (M7269 plus box)

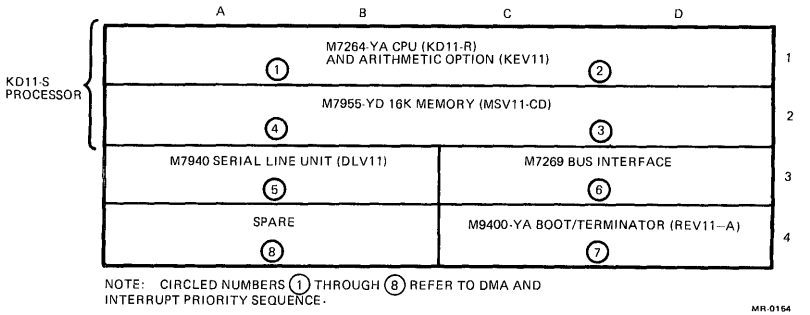
First device address (drive 0/1) 177170
First vector 264
Second device address (drive 2) 177150
Second vector 270

Bootstrap/Diagnostic/Terminator

REV11-A (M9400-YA)

Bootstrap enabled
Diagnostics enabled
Refresh disabled
120 Ω terminator

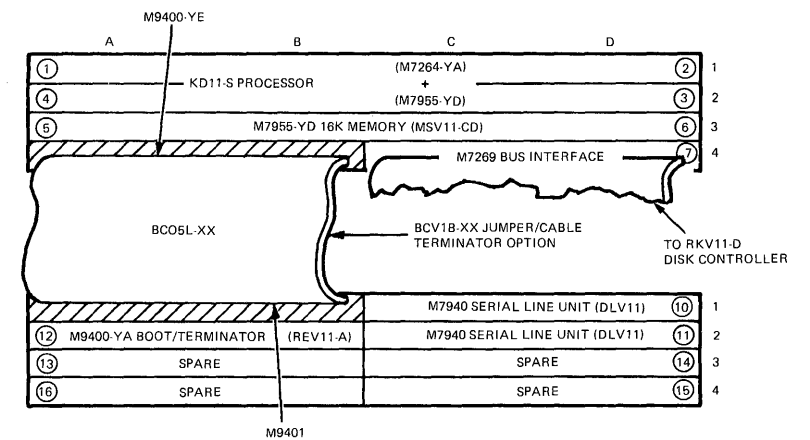
Module Utilization



NOTE: CIRCLED NUMBERS (1) THROUGH (8) REFER TO DMA AND INTERRUPT PRIORITY SEQUENCE.

MR-0164

Basic 16K System



NOTE: CIRCLED NUMBERS (1) THROUGH (16) REFER TO DMA AND INTERRUPT PRIORITY SEQUENCE.

MR-0153

Two-User Expanded 28K System

PDP-11T03-L AND PDP-11V03-L SYSTEMS

PDP-11T03-L
The PDP-11T03-L is a general purpose computer system that can be used for developing and executing programs in a variety of applications. RT-11 software provides a single user foreground and background system; it can support a real time application job execution in the foreground and an interactive or batch program development job in the background. RT-11 is also available for a single job configuration.

The PDP-11T03-L system consists of the following equipment.

PDP-11/03-LC (115 Vac) or PDP-11/03-LD (230 Vac) minicomputer with:

KD11-H microcomputer plus 16K words (32K bytes) of MOS memory (MSV11-CD)

BA11-NC (-ND) box with an H9273 backplane and an H786 power supply

BDV11-AA bootstrap/diagnostic/terminator and ROM option.

MSV11-CD configured as an additional 12K words (24K bytes) of MOS memory

KEV11 Extended Instruction Set/Floating Point Instruction Set (EIS/FIS)

RLV11 disk controller

RL01 five-megabyte dual disk drive units and cartridges

DLV11-F serial line unit

H9612-AC cabinet

Power controller

871-A	110 V	12 A	50/60 Hz
871-B	220 V	8 A	50/60 Hz
871-C	110 V	16 A	50/60 Hz

In addition to the preceding items, one RT-11 system software kit and one RLDP+ diagnostic kit are shipped with the system.

The following optional terminals are available for the system.

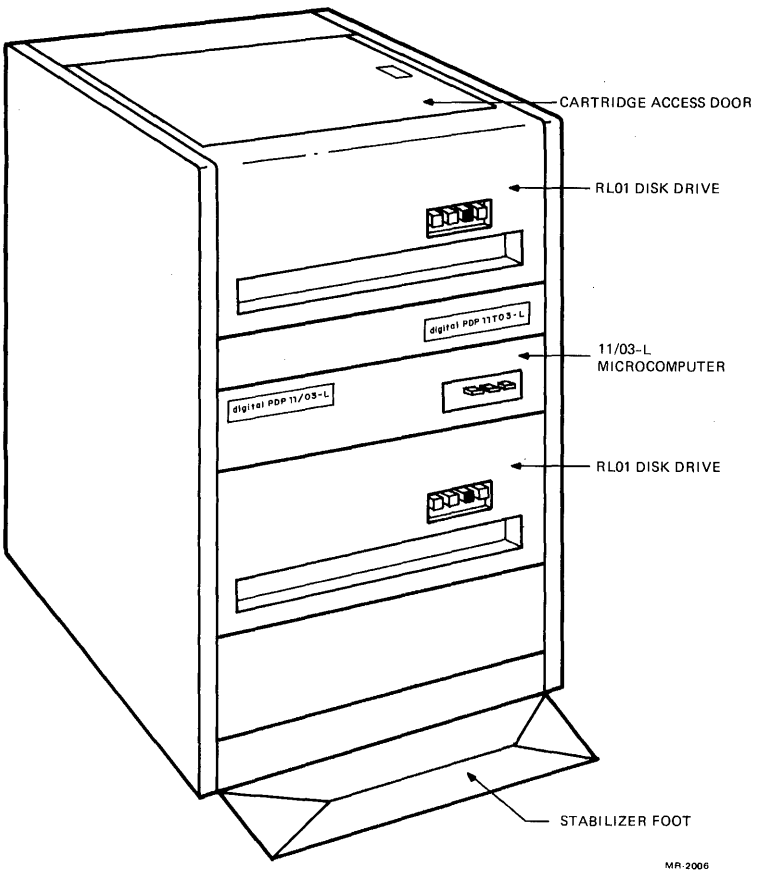
LA36 DECwriter
VT52 DECscope (with or without copier)
VT100 Alphanumeric Video Terminal

PDP-11T03-L Operator Switch Panel
Communication between the user and the processor is provided by switches on the front panel of the PDP-11/03-L or by the terminal connected to the system. The operator switch panel contains three switches: AUX ON/OFF, HALT, and RESTART. The functions and positions of the switches are as follows.

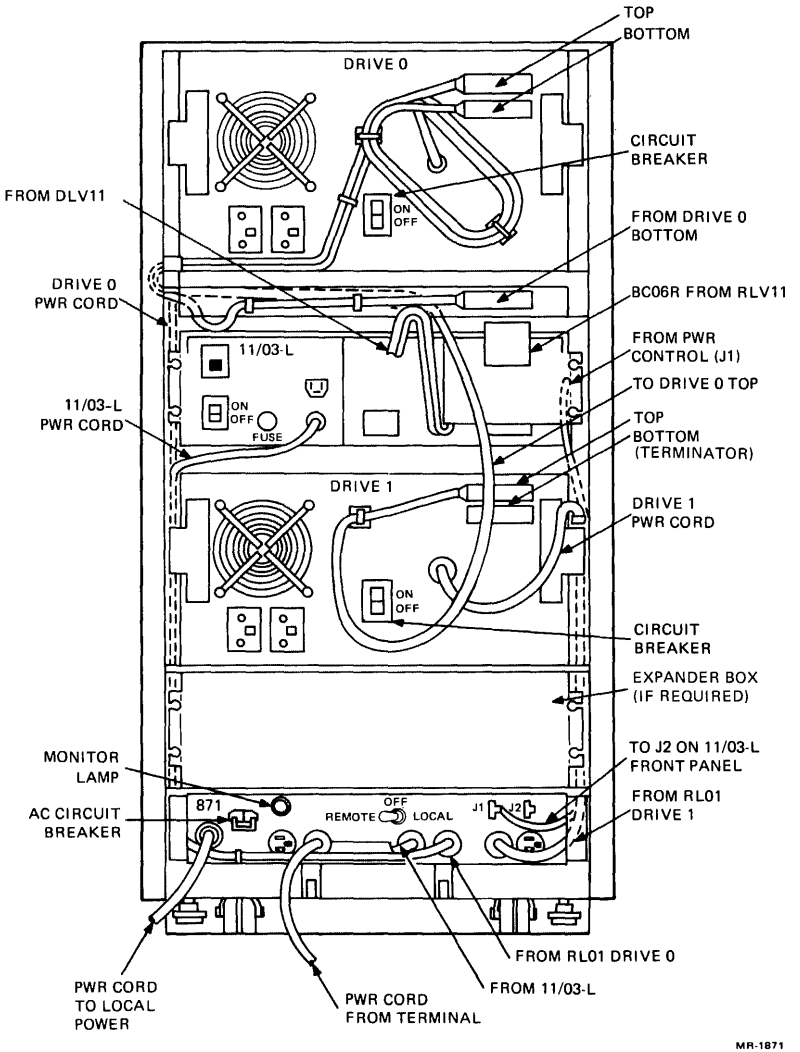
Switch	Position	Function
AUX ON/OFF	OFF	As configured at the factory, this switch, when turned off, removes ac power to the system.
	ON	As configured at the factory, it turns on ac power. If the automatic bootstrap is selected and the HALT switch is up, the system boots.
HALT	Up (Enable)	This enables the processor to run.
	Down (HALT)	This halts the processor, which responds to console ODT commands. Refer to the *Microcomputer Processor Handbook*, EB-18451-20, for ODT instructions.
RESTART	RESTART (Momentary Switch)	When this switch is activated, the processor carries out a power-up sequence. As shipped, the system presents the bootstrap dialog as: 28 START? The HALT switch must be up (enable).

The switch panel also contains two indicators that provide the following information.

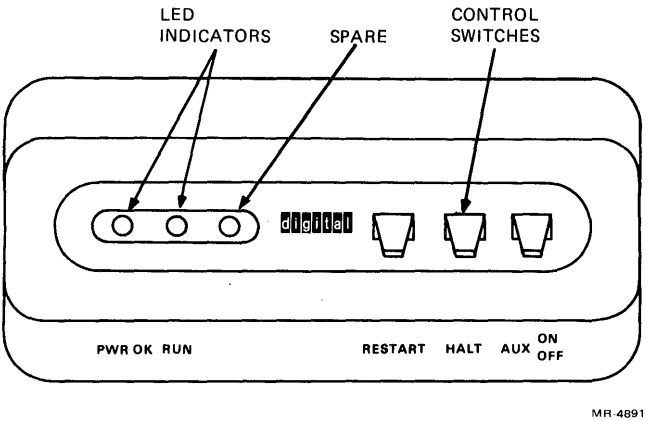
LED	Condition	Indication
PWR OK	ON	This LED lights when the proper dc output voltages are being generated by the H786 power supply.
RUN	ON	This LED lights when the processor is in the run state. It goes out when the processor is not executing instructions.



PDP-11T03-L Computer System



PDP-11T03-L (Rear Panel Removed)

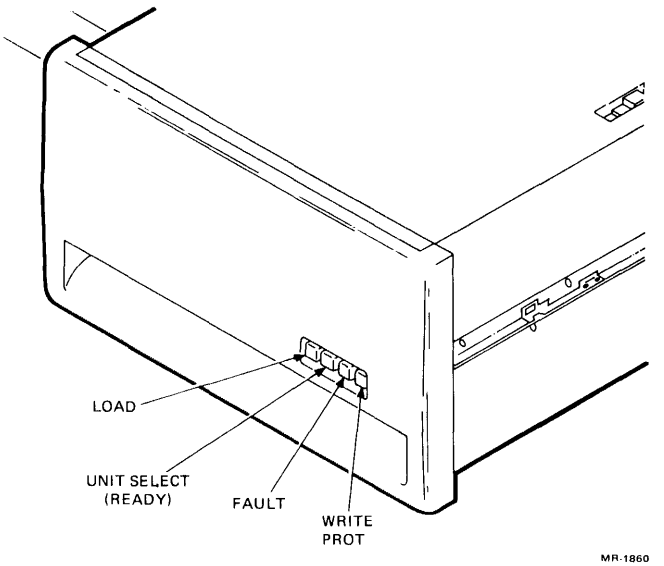


Front Panel Switches and Indicators

RL01 Disk Drives

The RL01 disk drive is a random access mass storage device with a removable, top-loading disk cartridge. Access to the disk is provided by a lift-up cover. The RL01 has four indicators on its front panel. Their functions are as follows.

Indicator	Function
LOAD (Push Button)	Lights to indicate that the spindle has stopped and a cartridge may be loaded.
UNIT SELECT (READY)	Lights to indicate that drive 0 or 1 is ready to read, write, or receive controller commands.
FAULT	Lights to indicate that a drive error condition exists.
WRITE PROT (Push Button)	Lights to indicate that the cartridge currently mounted is protected from having data written on it.



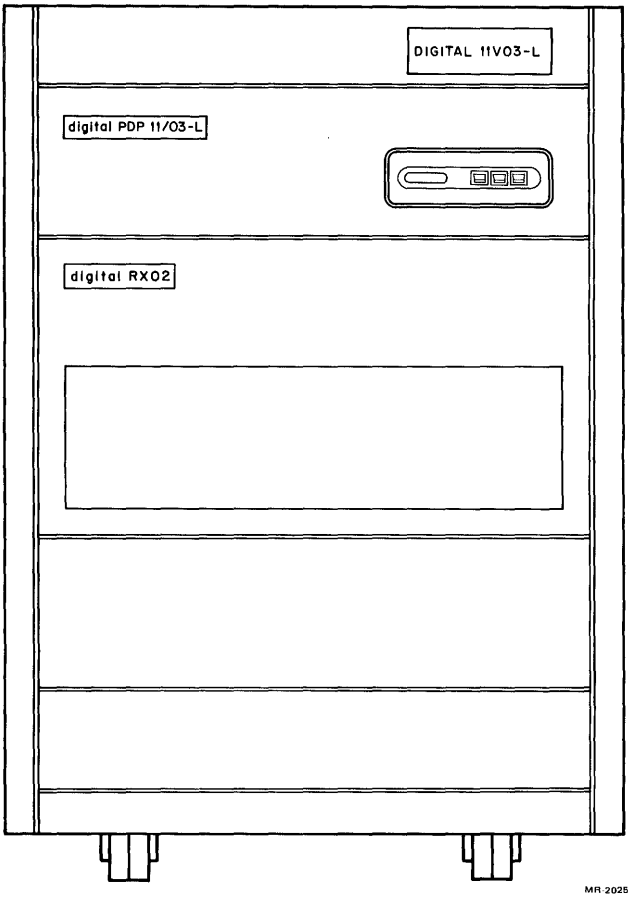
RL01 Disk Drive (Front View)

PDP-11V03-L

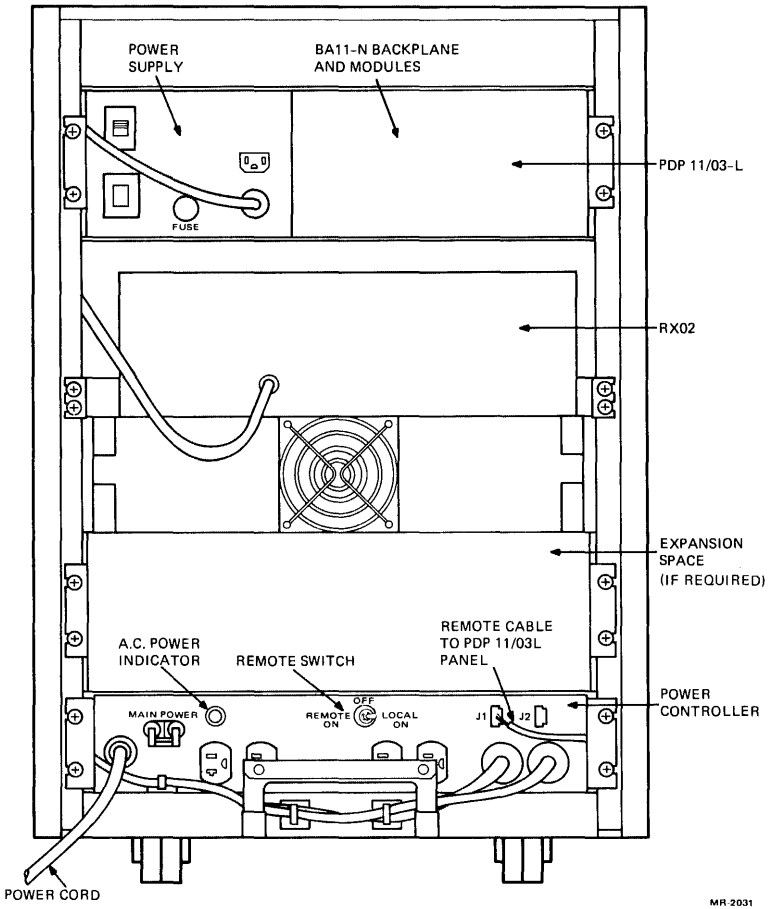
The PDP-11V03-L includes a PDP-11/03-L computer and an RX02 dual floppy disk system. The system also has 64K bytes or 32K words of RAM memory. Earlier systems have 32K bytes or 16K words of RAM memory that is expandable to 32K words. The system has the following optional terminals.

LA36 DECwriter
VT52 DECscope
VT100 DECscope

The figures and tables that follow describe the models, specifications, and components.



PDP-11V03-L System



PDP-11V03-L System (Backpanel Removed)

LOCAL POWER	POWER CONTROLLER	
	PLUG	RECEPTACLE
	871-A	
		
871-A 115V 15A 50/60HZ	NEMA # 5-15P DEC # 90-08938	5-20R 12-12265
	871-B	
		
871-B 230V 10A 50/60HZ	NEMA # 6-15P DEC # 90-08853	6-15R 12-11204-01
	871-C	
		
871-C 115V 20A 50/60HZ	HUBBELL # 5366-C DEC # 12-15183	NEMA # 5-20R 12-12265

MR-2406

Power Connectors

16K System Components

System Requirements	Models LA	LC	LD
Input Power (V)	115	115	230
Frequency (Hz)	60	50	50
PDP-11/03-L Computer	-LC	-LC	-LD
RX02 Floppy Disk	-BA	-BC	-BD
Power Controller	871-A	871-A	871-B

32K System Components

System Requirements	Models LE	LH	LJ
Input Power (V)	115	115	230
Frequency (Hz)	60	50	50
PDP-11/03-L Computer	-LK	-LK	-LL
RX02 Floppy Disk	-BA	-BC	-BD
Power Controller	871-A	871-A	871-B

11V03-L System (LE, LH, and LJ)
The PDP-11V03-L system consists of the following equipment.

A PDP-11/03LK-LL microcomputer consisting of:

KD11-HA (M7270)	a microcomputer board
MSV11-DD (M8044D)	a 32K word RAM
BA11-N	a mounting box with an H9273 backplane and an H786 power supply
BDV11-A	a bootstrap/diagnostic/terminator with expandable ROM space for the user (M8012-YA).

KEV11	A chip, mounted on the KD11-H microcomputer, that provides the system with the Extended Instruction Set (EIS) and Floating Point Instruction Set (FIS) features.
RXV21	The RX02 floppy disk controller module (M8029) interfaces the RX02 disk to the LSI-11 bus.
DLV11-J	The asynchronous four-channel line interface module (M8043) interfaces the terminal to the LSI-11 bus.
RX02	The dual floppy disk system.
H9610	The cabinet in which the hardware is mounted.
871	The primary power controller for the 11V03-L system.
Floppy Disks	The operational and diagnostic software programs are stored on floppy disks and are shipped as part of the system.

11V03-L Early Systems (LA, LC, and LD)
The PDP-11V03-L system consists of the following equipment.

A PDP-11/03LC-LD microcomputer consisting of:

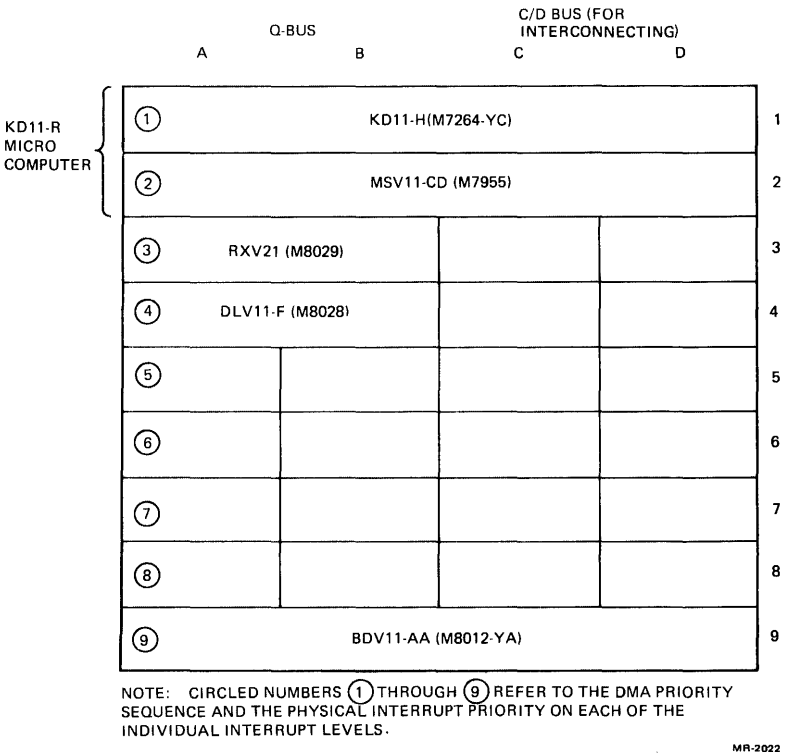
KD11-R	a KD11-H (M7264-YC) microcomputer board and a MSV11-CD (M7955) 16K MOS memory board
BA11-N	a mounting box with an H9273 backplane and an H786 power supply
BDV11-A	a bootstrap/diagnostic/terminator with expandable ROM space for the user (M8012-YA).

KEV11	A chip mounted on the KD11-H microcomputer that provides the system with the Extended Instruction Set (EIS) and Floating Point Instruction Set (FIS) features.
RXV21	The RX02 floppy disk controller module (M8029) interfaces the RX02 disk to the LSI-11 bus.
DLV11-F	The asynchronous line interface module (M8028) interfaces the terminal to the LSI-11 bus.
RX02	The dual floppy disk system.

H9610 The cabinet in which the hardware is mounted.

871 The primary power controller for the 11V03-L system.

Floppy Disks The operational and diagnostic software programs are stored on floppy disks and are shipped as part of the system.



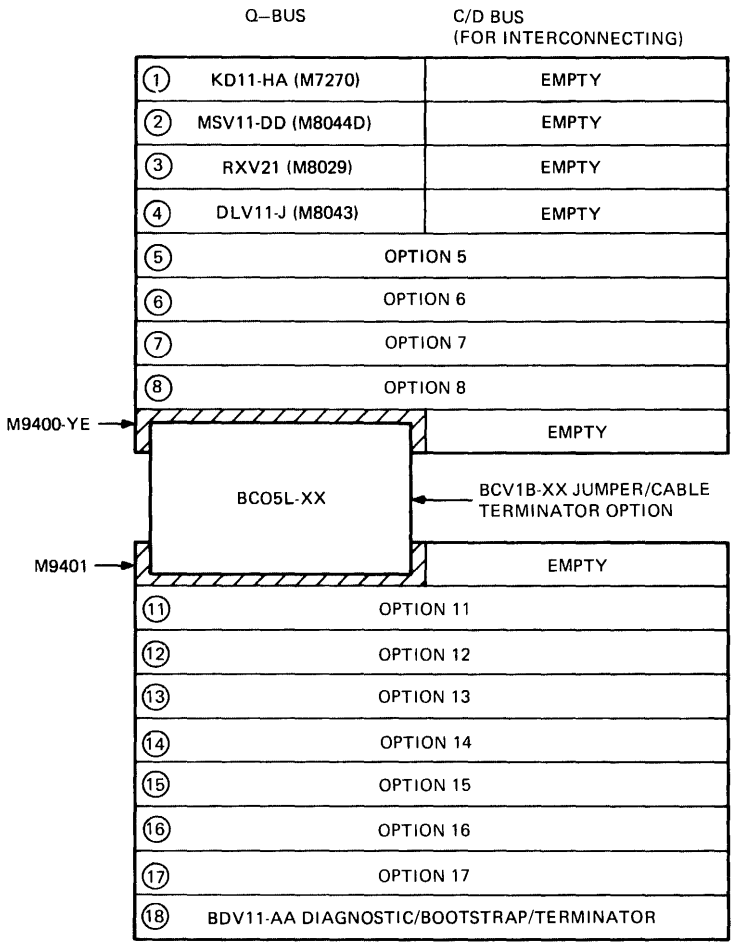
PDP-11V03-LA, -LC, and -LD Configuration

	Q–BUS A	Q–BUS B	C/D BUS (FOR INTERCONNECTING) C	C/D BUS (FOR INTERCONNECTING) D	
①	M7270 CPU (KD11-HA) AND OPTION (KEV11)		EMPTY		1
②	M8044D 32K MEMORY (MSV11-DD)		EMPTY		2
③	M8029 RX02 INTERFACE (RXV21)		EMPTY		3
④	M8043 SERIAL LINE UNIT (DLV11-J)		EMPTY		4
⑤	OPTION 5		EMPTY		5
⑥	OPTION 6		EMPTY		6
⑦	OPTION 7		EMPTY		7
⑧	OPTION 8		EMPTY		8
⑨	M8012-YA BOOTSTRAP/DIAGNOSTIC/TERMINATOR (BDV11-AA)				9

NOTE: CIRCLED NUMBERS ① THROUGH ⑨ REFER TO THE DMA PRIORITY SEQUENCE AND THE PHYSICAL INTERRUPT PRIORITY ON EACH OF THE INDIVIDUAL LEVELS.

MR-2407

PDP-11V03-LE, -LH, and -LJ Backplane Configuration



NOTE: CIRCLED NUMBERS ① THROUGH ⑱ REFER TO THE DMA PRIORITY SEQUENCE AND THE PHYSICAL INTERRUPT PRIORITY ON EACH OF THE INDIVIDUAL INTERRUPT LEVELS.

MR-2408

PDP-11V03-LE, -LH, and -LJ System Expansion

PDP-11V23 AND PDP-11T23 SYSTEMS

PDP-11V23 SYSTEM

The PDP-11V23 is a general purpose computer system that can be used for developing and executing programs for a variety of applications.

Optional hardware and software is available for applications such as high-level language program development support, foreground/background real time support, multiprogramming, and the ability to monitor and control equipment.

The PDP-11V23 can support a real time application job execution in the foreground and an interactive or batch program development in the background. RT-11 is also available for a single job configuration. The PDP-11V23 system contains the following equipment.

A PDP-11/23 minicomputer with:

KDF11-AA microprocessor module (M8186) contained on a double-height module

MSV11-DD (M8044D) two double-height modules with 128K bytes of MOS RAM (on two modules) expandable to 256K bytes (four modules)

BA11-N mounting box with an H9273 backplane, an H786 power supply, and H403-A ac input box and a front bezel panel (54-12985)

BDV11-AA bootstrap/diagnostic/terminator with expandable user ROM option (M8012-YA).

DLV11-J Asynchronous four-channel serial line interface unit (M8043). (Must be CS revision "E" or higher.)

RXV21 The RX02 floppy disk controller module (M8029) interfaces the RX02 to the LSI-11 bus. (Must be at CS revision "E1" or higher.)

RX02 The dual drive floppy disk system.

H9610 Free-standing 76.8 cm (30 in) high cabinet.

PDP-11V23

Power controller

871-A*	120 Vac	12 A	50/60 Hz (early 120 Vac systems)
871-B	230 Vac	8 A	50/60 Hz
871-C*	120 Vac	20 A	50/60 Hz (later 120 Vac systems)

In addition to the preceding configuration, the following items are shipped with the PDP-11V23 system.

RT-11 system software package

DYDP+ diagnostic kit

Floppy disk set. Disks contain the RT-11 operating system software and DYDP diagnostic programs.

Option terminals available for the system configuration include the following.

LA38 DECwriter IV
LA120 DECwriter III
VT100 Alphanumeric Video Terminal

PDP-11V23 Operator Switch Panel

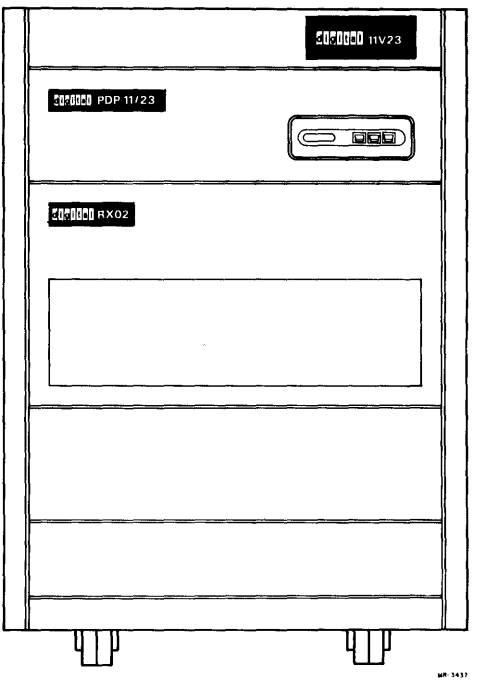
Three control switches on the front of the PDP-11/23 provide a communication link between the operator and the microcomputer system.

The switches labeled AUX ON/OFF, HALT, and RESTART provide power, stop, and bootstrap control for the PDP-11/23. The switch functions are defined as follows.

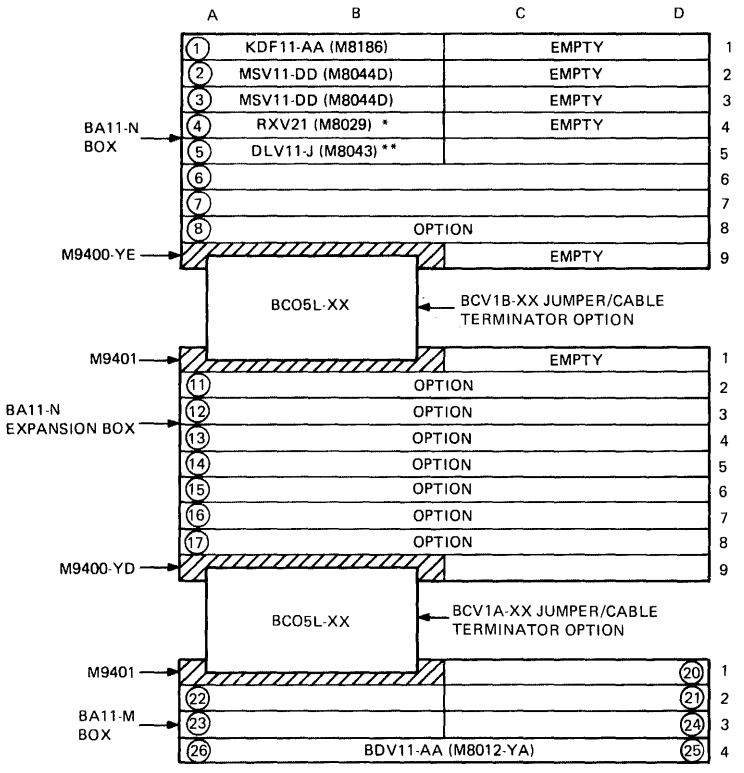
Switch	Position	Function
AUX ON/OFF	OFF	In the normal factory configuration, turning this switch off removes ac power from the system.
	ON	In the normal factory configuration, turning this switch on applies ac power to the system. If the HALT switch is up, the system is automatically booted.

*Systems built before April 1980 use 871-A power controllers. Systems built after April 1980 use 871-C power controllers.

HALT	Up (Enable)	This switch enables the processor to run.
	Down (HALT)	The HALT switch, when down, halts the processor, which responds to console ODT commands. Refer to the *Microcomputer Processor Handbook*, EB-18451-20, for ODT instructions.
RESTART	RESTART (Momentary Switch)	When this switch is activated, and when the HALT switch is up, the processor carries out a power-up sequence and displays the bootstrap dialog as: 28* START?



*The BDV11 software automatically sizes the available memory in the system and prints the number 28. The 28 is the present limit for the BDV11 ROM software. The actual available memory maximum is 124K words. The user should be aware of the actual memory and not depend on the printout. The memory-sizing software will be updated and eventually print out the actual memory size up to the addressing limit of the CPU.



*NOTE: MUST BE AT CS REVISION 'E1' OR HIGHER

** NOTE: MUST BE AT CS REVISION 'E' OR HIGHER

NOTE: CIRCLED NUMBERS (1) THROUGH (26) REFER TO THE DMA PRIORITY SEQUENCE AND THE PHYSICAL INTERRUPT PRIORITY ON EACH OF THE INDIVIDUAL INTERRUPT LEVELS

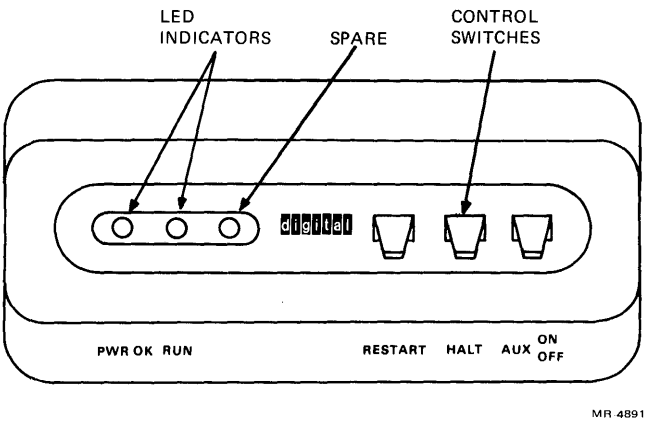
MR-4874

PDP-11V23 System Expansion Example

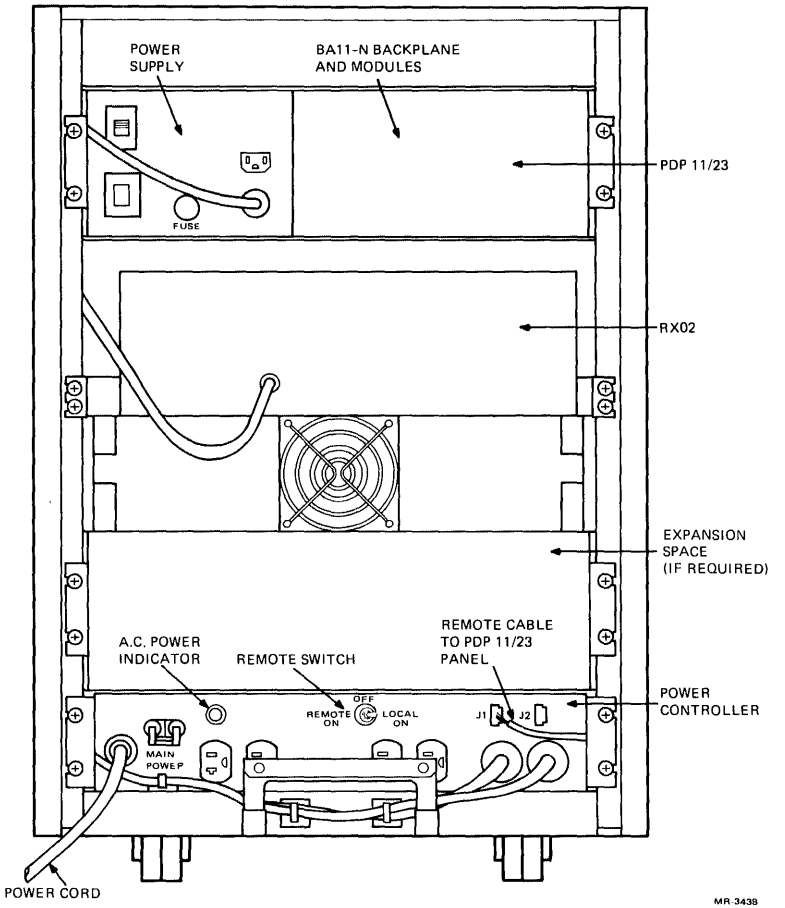
The PDP-11/23 front switch panel also contains two indicators that provide the following information.

LED	Function
PWR OK	Illuminated when the proper dc output voltages are being generated by the microcomputer system.
RUN	Illuminated when the processor is operating; turned off when the processor is not executing instructions.

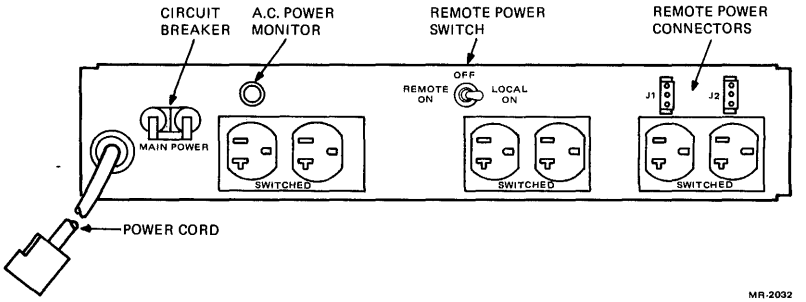
The following is an expanded PDP-11V23 configuration example using both the BA11-N and BA11-M boxes.



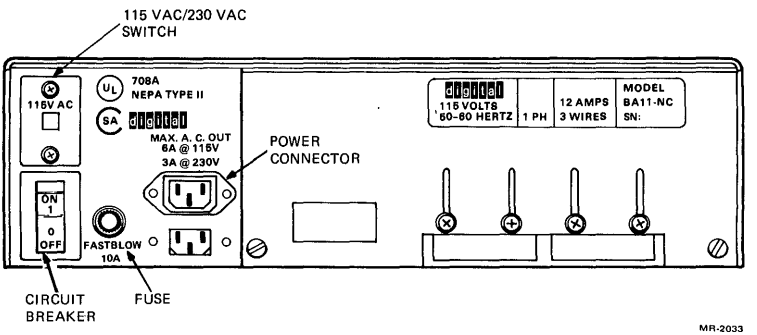
Front Panel Switches and Indicators



PDP-11V23 with Backpanel Removed



Power Controller (Rear View)



PDP-11/23 Microcomputer (Rear View)

	Q-BUS		C/D BUS (FOR INTERCONNECTING)		
	A	B	C	D	
①	KDF11-AA (M8186)				1
②	MSV11-DD (M8044D)				2
③	MSV11-DD (M8044D)				3
④	RXV21 (M8029) *				4
⑤	DLV11-J (M8043) **				5
⑥					6
⑦					7
⑧					8
⑨	BDV11-AA (M8012-YA)				9

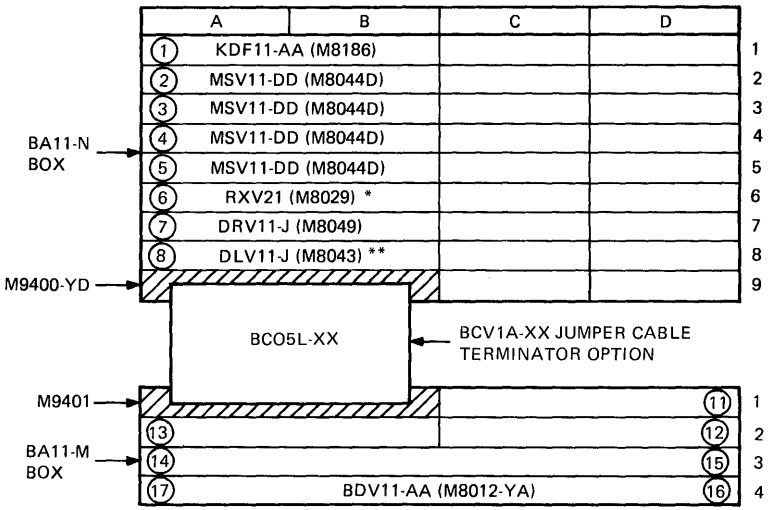
*NOTE: MUST BE AT CS REVISION 'E1' OR HIGHER

**NOTE: MUST BE AT CS REVISION 'E' OR HIGHER

NOTE: CIRCLED NUMBERS ① THROUGH ⑨ REFER TO THE DMA PRIORITY SEQUENCE AND THE PHYSICAL INTERRUPT PRIORITY ON EACH OF THE INDIVIDUAL INTERRUPT LEVELS.

MR-4873

PDP-11V23 Module Configuration



*NOTE: MUST BE AT CS REVISION 'E 1' OR HIGHER

**NOTE: MUST BE AT CS REVISION 'E' OR HIGHER

NOTE: CIRCLED NUMBERS (1) THROUGH (17) REFER TO THE DMA PRIORITY SEQUENCE AND THE PHYSICAL INTERRUPT PRIORITY ON EACH OF THE INDIVIDUAL INTERRUPT LEVELS.

MR-4875

PDP-11V23 Expansion Example

PDP-11V23

LOCAL POWER	POWER CONTROLLER	
	PLUG	RECEPTACLE
	871-A	
871-A 115V 15A 50/60HZ	 NEMA # 5-15P DEC # 90-08938	 5-20R 12-12265
	871-B	
871-B 230V 10A 50/60HZ	 NEMA # 6-15P DEC # 90-08853	 6-15R 12-11204-01
	871-C	
871-C 115V 20A 50/60HZ	 HUBBELL # 5366-C DEC # 12-15183	 NEMA # 5-20R 12-12265

MR-2405

System Requirements	Model AA	Model AC	Model AD
Input Power (V)	120	120	240
Frequency	60	50	50
Current	12	12	8
PDP-11V23 Computer	AA	AA	AB
RX02 Floppy Disk	BA	BC	BD
Power Controller	871-A* or 871-C	871-A* or 871-C	871-B

*Systems built before April 1980 use 871-A power controllers. Systems after April 1980 use 871-C power controllers.

PDP-11T23 SYSTEM

The PDP-11T23 is a general purpose computer system that can be used for developing and executing programs for a variety of applications.

Optional hardware and software are available for applications such as high-level language program development, foreground/background real time support, multiprogramming, and equipment monitoring and control capability.

PDP-11T23 can support a single user with a foreground/background system. It can support a real time application job execution in the foreground and an interactive or batch program development in the background. RT-11 is also available for a single job configuration.

The PDP-11T23 system contains the following equipment.

A PDP-11/23 minicomputer with:

KDF11-AA microprocessor module (M8186) contained on a double-height module

MSV11-DD (M8044D) two double-height modules with 128K bytes of MOS RAM (on two modules) expandable to 256K bytes (four modules)

BA11-N mounting box with an H9273 backplane, an H786 power supply, and H403-A ac input box and a front bezel panel

BDV11-AA bootstrap/diagnostic/terminator with expandable user ROM option (M8012-YA).

DLV11-J Asynchronous four-channel serial line interface unit (M8043). (Must be at CS revision "E" or higher.)

RL01 Five-megabyte dual disk drive units and cartridges

H9612 105 cm (42 in) high cabinet

Power controller

871-A*	120 Vac	12 A	50/60 Hz
871-B	230 Vac	8 A	50/60 Hz
871-C*	120 Vac	16 A	50/60 Hz

In addition to the preceding configuration, the following items are shipped with the system.

1 RT-11 or RSX-11M system software kit
1 DLDP+ diagnostic kit

*Systems built before April 1980 use 871-A power controllers. Systems built after April 1980 use 871-C power controllers.

Optional terminals available for the system include the following.

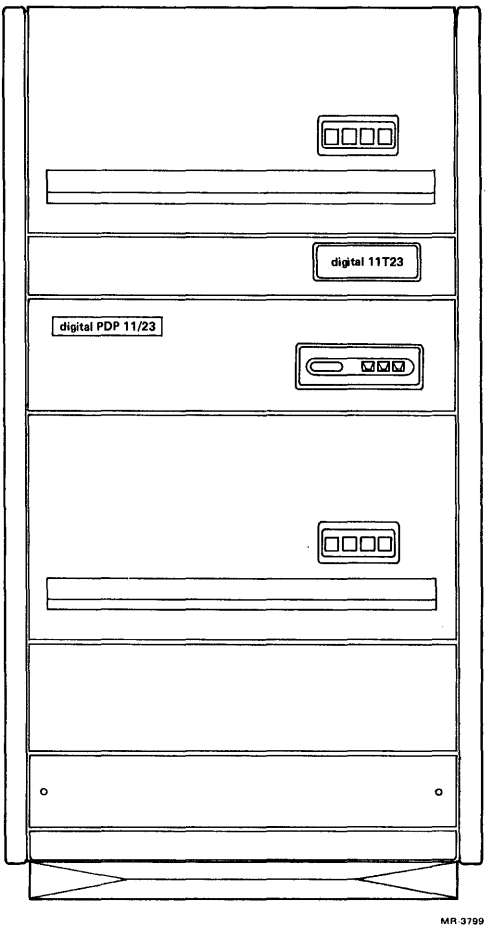
LA38 DECwriter IV
LA120 DECwriter III
VT100 Alphanumeric Video Terminal

PDP-11T23 Operator Switch Panel
Three control switches on the front of the PDP-11T23 provide a communication link between the operator and the microcomputer system.

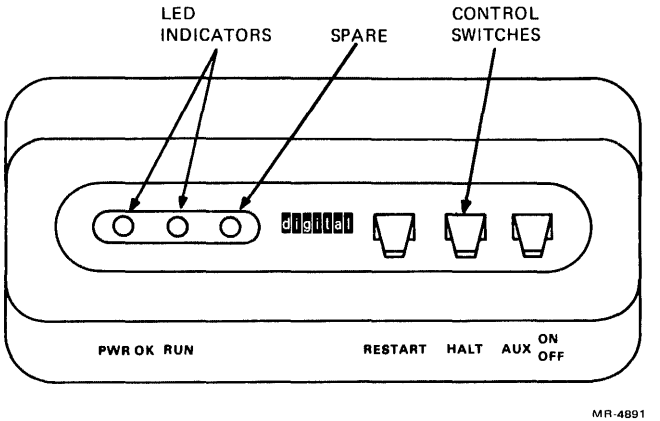
The switches labeled AUX ON/OFF, HALT, and RESTART provide power, stop, and bootstrap control, respectively. The switch functions are defined as follows.

Switch	Position	Function
AUX ON/OFF	OFF	In the normal factory configuration, this removes ac power from the system.
	ON	In the normal factory configuration, this applies ac power to the system. If the HALT switch is up, the system is automatically booted.
HALT	Up (Enable)	This enables the processor to run.
	Down (HALT)	This halts the processor, which will respond to console odt commands. Refer to the *Microcomputer Processor Handbook*, EB-18451-20, for ODT instructions.
RESTART	RESTART (Momentary Switch)	When this switch is activated, and when the HALT switch is up, the processor carries out a power-up sequence and displays the bootstrap dialog as: 28* START?

*The BDV11 software automatically sizes the available memory in the system and prints the number 28. The 28 is the present limit for the software. The actual available memory maximum is 124K words. The user should be aware of the actual memory and not depend on the printout. The memory-sizing software will be updated and eventually print out the actual memory size up to the addressing limit of the CPU.



PDP-11T23 Computer System



Front Panel Switches and Indicators

The PDP-11T23 front switch panel also contains two indicators that provide the following information.

LED	Function
PWR OK	Illuminated when the proper dc output voltages are being generated by the microcomputer system.
RUN	Illuminated when the processor is operating; turned off when the processor is not executing instructions.

RL01 Disk Drives

The RL01 disk drive is a random access mass storage device with a removable, top-loading disk cartridge. Access to the disk is provided by a lift-up cover. The RL01 has four indicators on its front panel. Their functions are as follows.

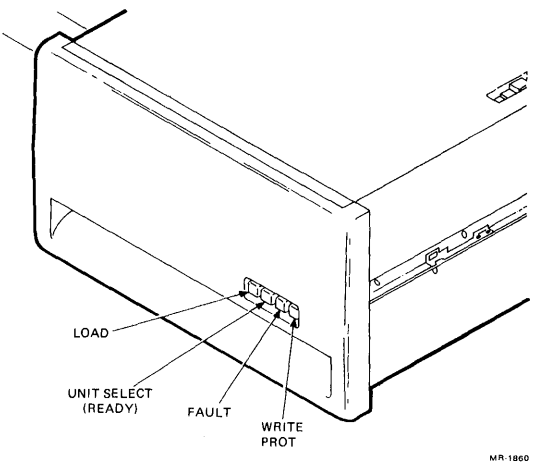
Indicator	Function
LOAD (Push Button)	Lights to indicate that the spindle has stopped and a cartridge may be loaded.
UNIT SELECT (READY)	Lights to indicate that drive 0 or 1 is ready to read, write, or receive controller commands.

FAULT	Lights to indicate that a drive error condition exists.
WRITE PROT (Push Button)	Lights to indicate that the cartridge currently mounted is protected from having data written on it.

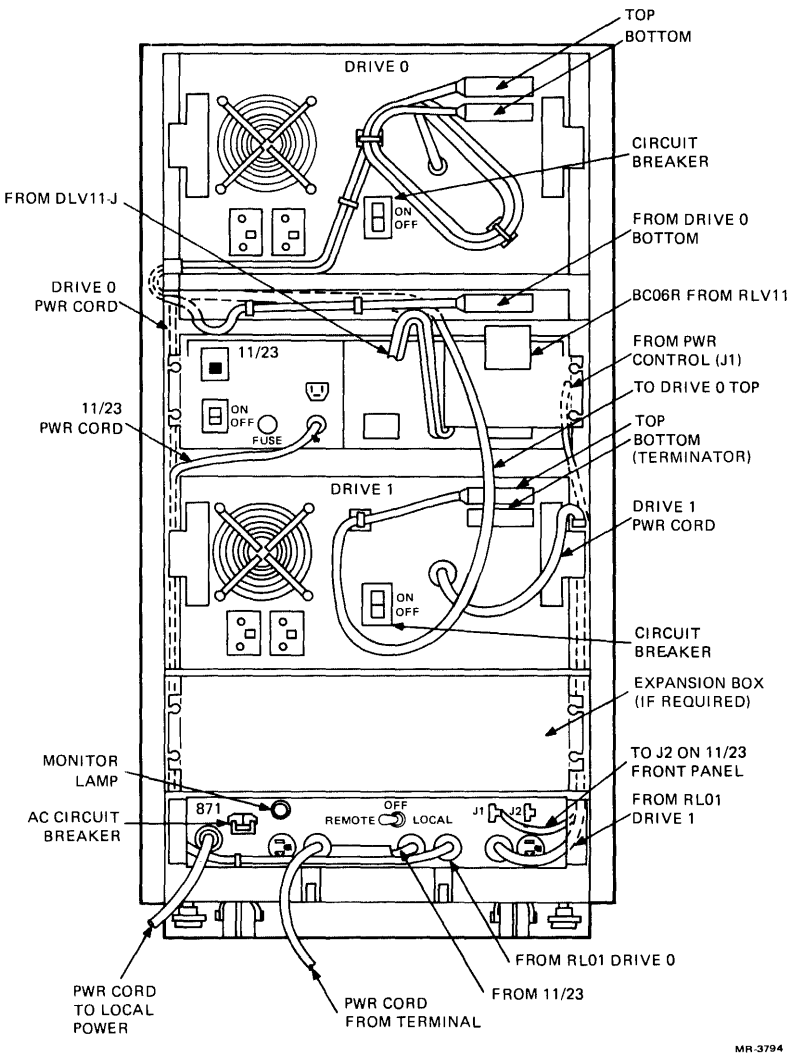
The following is an example of the PDP-11T23 microcomputer with an expanded configuration using both the BA11-N and BA11-M boxes.

System Requirements	Models AA	AB	AC
Input Power (V)	120	240	120
Frequency	50/60	50/60	50/60
Current	12 A	8 A	16 A
PDP-11T23 Computer	AA	AB	AA
RL01 Disk	AK	AK	AK
Power Controller	871-A* or 871-C	871-B	871-C*

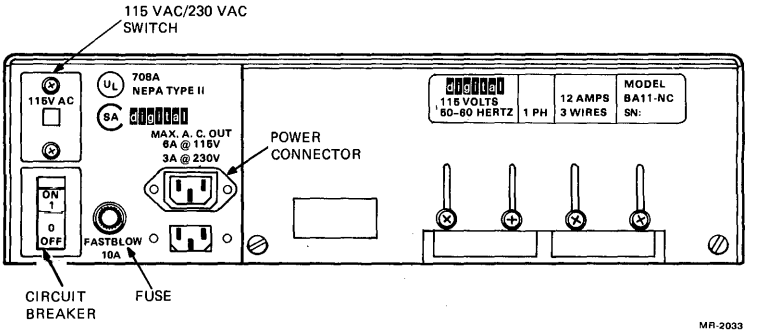
*Systems built before April 1980 use 871-A power controllers. Systems built after April 1980 use 871-C power controllers.



RL01 Disk Drive (Front View)



PDP-11T23 (Rear Panel Removed)



PDP-11/23 Microcomputer (Rear View)

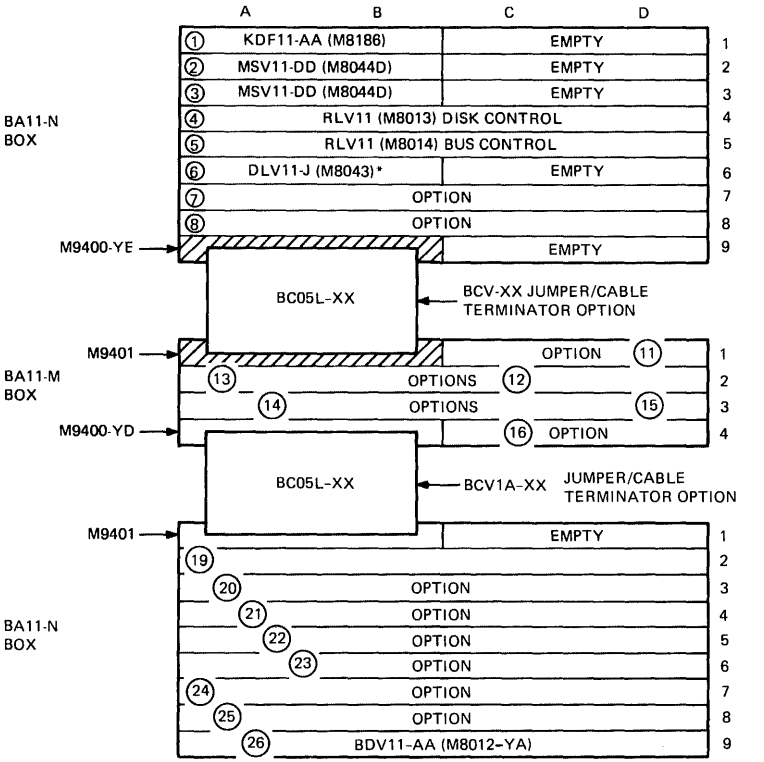
	Q–BUS		C/D BUS (FOR INTERCONNECTING)		
	A	B	C	D	
①	KDF11-AA (M8186)				1
②	MSV11-DD (M8044D)				2
③	MSV11-DD (M8044D)				3
④	RLV11 (M8013) DISK CONTROL				4
⑤	RLV11 (M8014) BUS CONTROL				5
⑥	DLV11-J (M8043) *				6
⑦					7
⑧					8
⑨	BDV11-AA (M8012-YA)				9

*NOTE: MUST BE AT CS REVISION 'E' OR HIGHER

NOTE: CIRCLED NUMBERS ① THROUGH ⑨ REFER TO THE DMA PRIORITY SEQUENCE AND THE PHYSICAL INTERRUPT PRIORITY ON EACH OF THE INDIVIDUAL INTERRUPT LEVELS.

MR-4877

Typical PDP-11T23 Module Configuration



*NOTE: MUST BE AT CS REVISION 'E' OR HIGHER

NOTE: CIRCLED NUMBERS ① THROUGH ㉖ REFER TO THE DMA PRIORITY SEQUENCE AND THE PHYSICAL INTERRUPT PRIORITY ON EACH OF THE INDIVIDUAL INTERRUPT LEVELS.

MR-4878

PDP-11T23 Module Expansion Example

COMMERCIAL SYSTEMS

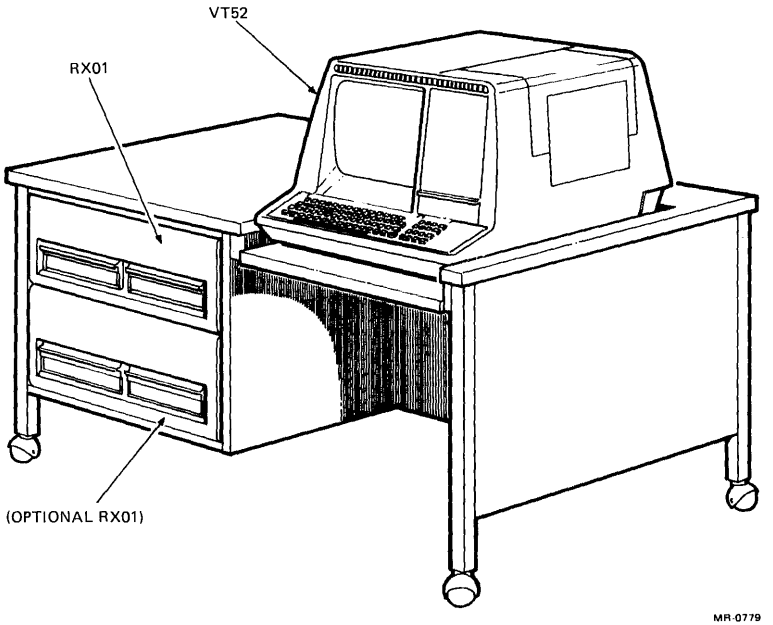
D322
The standard Datasystem 322 includes the following.

- Desk-like cabinet
- Central processor with 32K bytes of MOS memory
- One RX01 dual floppy disk unit with 512K bytes of data storage
- VT52 video/keyboard transaction terminal

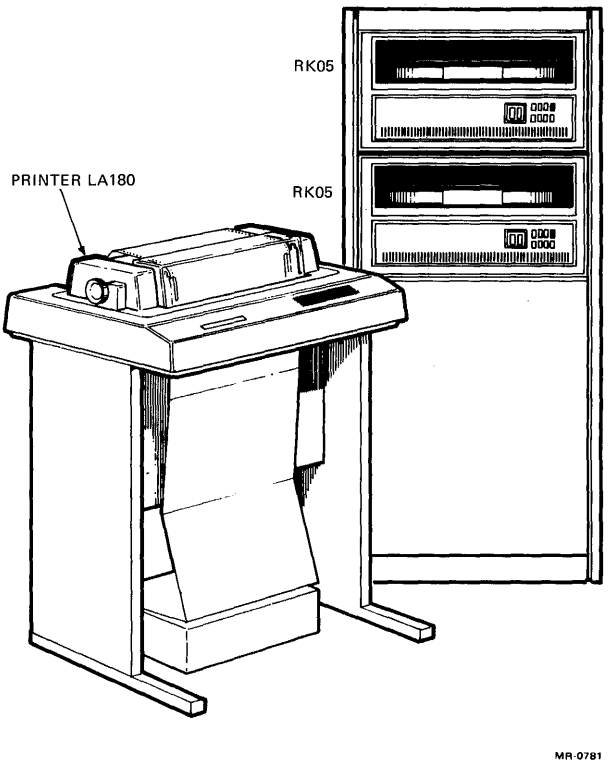
Options include:

- Additional memory up to a total of 56K bytes
- Additional dual floppy disk unit in the same cabinet
- Choice of printers (30 cps up to 300 lpm)
- Cartridge disk drives (2.5 million bytes removable; 5.0 fixed)
- Up to three video or hard-copy terminals
- 2780 communications package and CTS-300 DICAM, providing both batch and interactive communication capabilities.

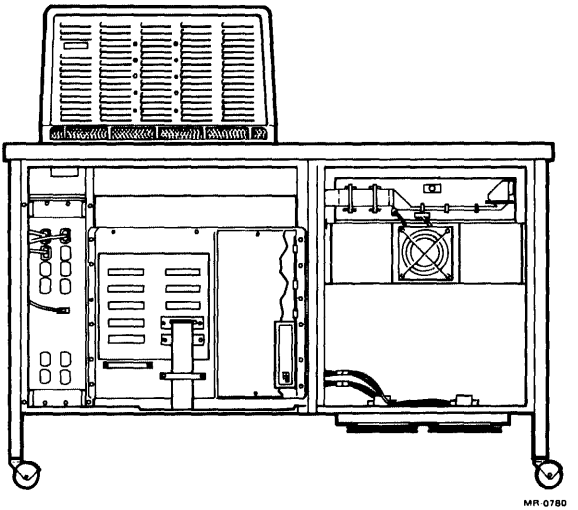
Further information may be found in the *DEC Datasystem 320 Family Service Manual*, EK-DDS03-SV.



Basic 322 System



Optional Cabinet and Printer



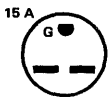
Basic D322 System, Rear View with Door Removed

D322 System Model Designations

		Model Designation		
D322A-	AA	AD	AY	AZ
Input Power/Frequency	115/60	230/50	115/60	230/50
Software Category	A	A	C	C
D322-	A	B	↑	↑
H9820-	W	W		
RXV11-	DA	DD	same	same
PDP-11/03-	JA	JB	as	as
VT52-	AE	AF	AA	AD
LAV11-*	PA	PD	column	column
DS3RK-	AA	AD		
H967-	HK	HL		
RKV11-	DA	DB	↓	↓

*Model AA + LAV11 = Model BA
Model AD + LAV11 = Model BD
Model AY + LAV11 = Model BY
Model AZ + LAV11 = Model BZ

D322 SPECIFICATIONS* SEE D324 SPECS FOR PRINTER SPECS

	BASIC 322		OPTIONAL CABINET	
	115 V 60 HZ	230 V 50 HZ	115 V 60 HZ	230 V 50 HZ
POWER CONNECTOR				
NEMA NO. DEC P/N	5-15P 90-08938	6-15P 90-08853	5-15P 90-08938	6-15P 90-08853
AMPERAGE	12 AMPS	6 AMPS	12 AMPS	6 AMPS
BTU/HOUR	3400	3400	1400	1400
HEAT DISSIPATION	1000 W	1000 W	400 W	400 W
SHIPPING WEIGHT (APPROXIMATE)	400 LBS 182 KG	400 LBS 182 KG	300 LBS 136 KG	300 LBS 136 KG

*SPECIFICATIONS HAVE BEEN FIGURED ON THE MAXIMUM CONTAINED IN EACH UNIT.

MR-0782

Modules Included in the Basic System

Processor

KD11-P (M7264-BB)

Resident memory addressed as bank 0
CPU refresh disabled
Powers up to 173000

Or

KD11-Q (M7264-YB)

No resident memory
CPU refresh disabled
Powers up to 173000

Memory

MSV11-B (M7944)

4K RAM
Three in basic system with KD11-P
Addresses start at bank 1
Refreshed by REV11-C

Or

D322

MSV11-C (M7955-YD)

16K RAM
One in basic system with KD11-Q
Addresses start at bank 0
Internal refresh

Serial Line Interface

DLV11 (M7940)

Device address 177560
Vector 60
9600 baud
EIA
One stop bit, eight data bits, no parity

RX01 Floppy Disk Interface

RXV11 (M7946)

First device address (disk 0) 177170
First vector 264
Second device address (disk 1) 177150
Second vector 270

Bootstrap/Diagnostic

REV11-C (M9400-YC)

Bootstrap enabled
Diagnostics enabled
Refresh enabled for MSV11-B
Refresh disabled for MSV11-C

Terminator

TEV11 (M9400-YB)

120 Ω terminator

Optional Modules for Recommended Expansion

LA180 Printer Interface

LAV11 (M7949)

Device address 177510
Vector 200

Or

LPV11 (M8027)

Device address 177510
Vector 200

RK05 Disk Interface

RKV11-D

Interfaced to computer by M7269
See the "CPU/Options" section for more detailed information.

Communications Interface

DUV11 (M7951)

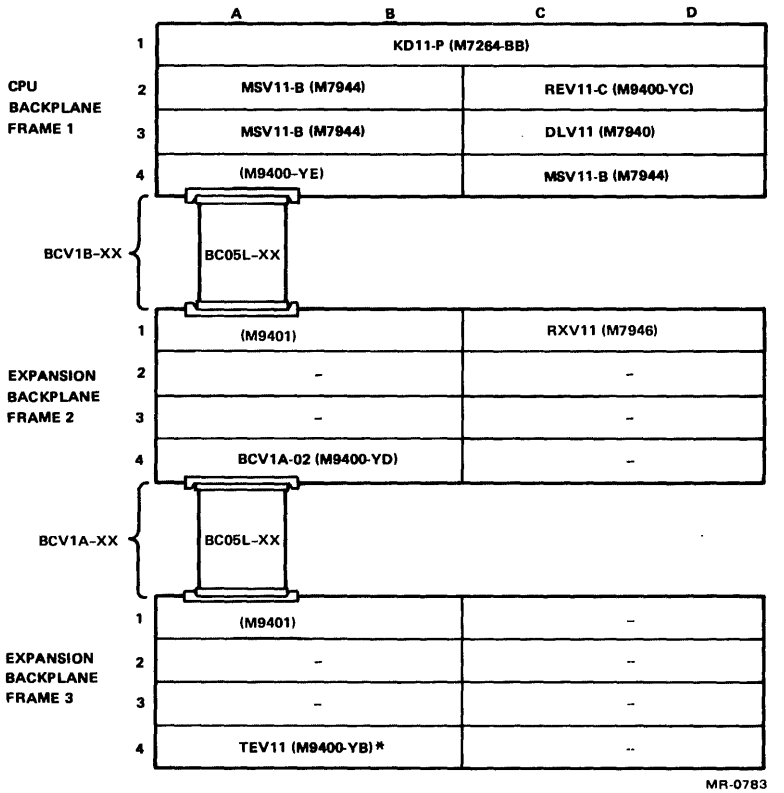
Device address 160010
Vector 440

DLV11 (M7940)

Device address:
console 177560
second terminal 176500

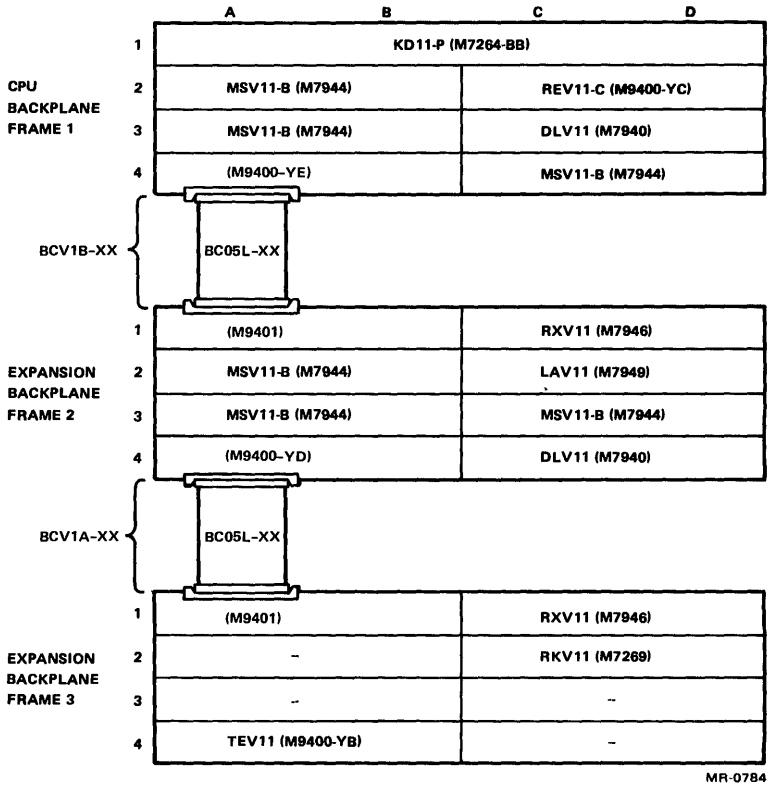
Vector:
console 60
second terminal 300

D322

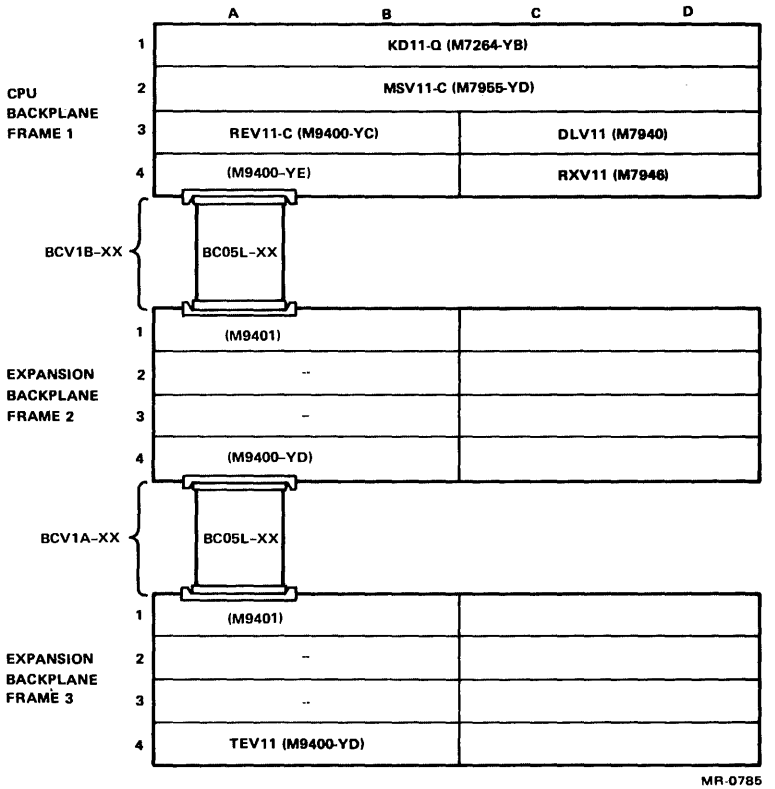


*IN MOST CASES M9400 MODULES ARE PLACED IMMEDIATELY FOLLOWING THE LAST MODULE IN THE SYSTEM. THE TEV11, HOWEVER, IS AN EXCEPTION TO THE GENERAL RULE. IN THE BUSINESS PRODUCTS SYSTEMS IT IS PLACED IN THE LAST SLOT OF THE LAST BACKPLANE IN ORDER TO MINIMIZE NOISE.

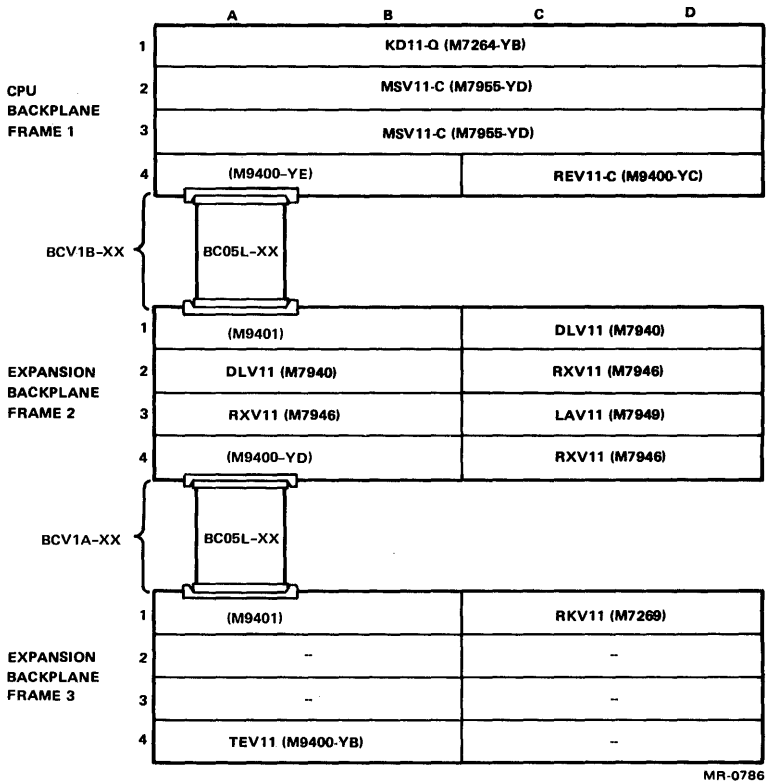
D322 Module Utilization Drawing for Basic System Using PDP-11/03-JA or - JB CPU Box



D322 Module Utilization Drawing for Recommended Expanded Systems Using PDP-11/03-JA or -JB CPU Box



D322 Module Utilization for Basic System
Using PDP-11/03-JC or -JD CPU Box



D322 Module Utilization for Recommended
Expanded Systems Using PDP-11/03-JC or -JD CPU Box

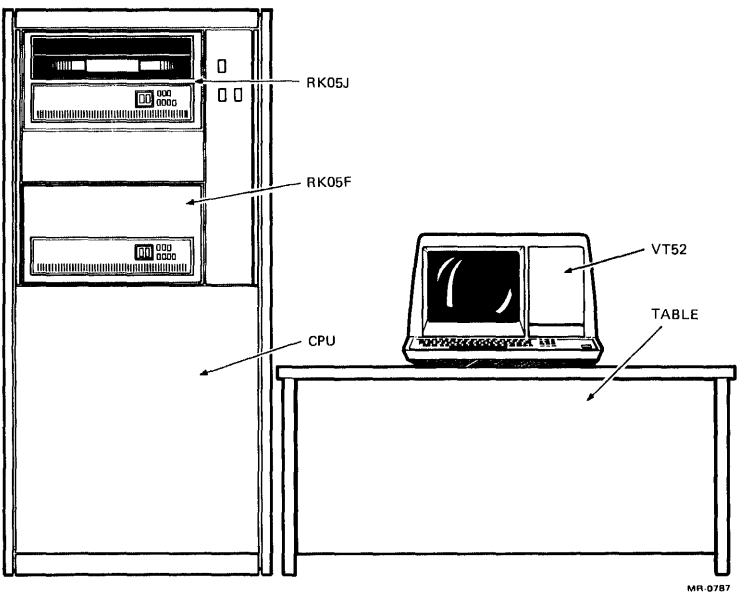
D324

The standard Datasystem 324 includes the following.

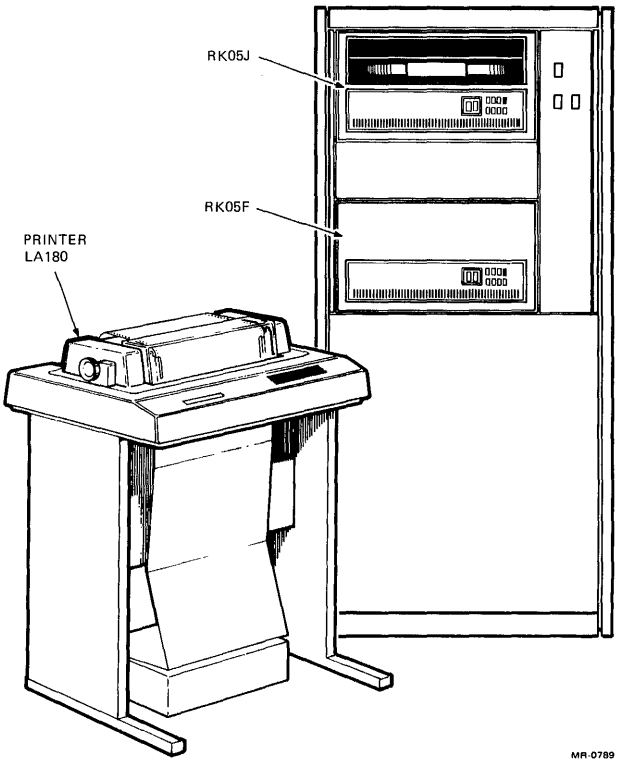
- Stylized cabinet and desk
- Central processor with 32K bytes of MOS memory
- One RK05J removable disk drive with a capacity of 2.4 million bytes of data
- One RK05F fixed disk drive with a capacity of 4.8 million bytes of data
- VT52 video/keyboard transaction terminal

Options include additional memory up to a total of 56K bytes.

Further information may be found in the *DEC Datasystem 320 Family Service Manual*, EK-DDS03-SV.



Basic 324 System



Optional Cabinet and Printer

D324 System Model Designations

	Model Designation			
D324A-	AA	AD	AY	AZ
Input Power/Frequency	115/60	230/50	115/60	230/50
Software Category	A	A	C	C
D324-	A	B	↑	↑
H9602-	CC	CD		
RKV11-	DA	DB	same	same
PDP-11/03-	JA	JB	as	as
H970-	DA	DA	AA	AD
VT52-	AE	AF	column	column
LAV11-*	PA	PD		
RXV11-	DA	DD	↓	↓

*Model AA + LAV11 = Model BA
Model AD + LAV11 = Model BD
Model AY + LAV11 = Model BY
Model AZ + LAV11 = Model BZ

D324 SPECIFICATIONS*

	PRINTER LA180		RK05 CABINET		CPU CABINET		VT52 DESK	
	115V 60HZ	230V 50HZ	115V 60HZ	230V 50HZ	115V 60HZ	230V 50HZ	115V 60HZ	230V 50HZ
POWER CONNECTOR	15 A 	15A 	30 A W 	30 A W 	30 A W 	20 A X 	15 A 	15 A 
NEMA NO. DEC P/N	5-15 P 90-08938	6-15 P 90-08853	15-30 P 12-11193	15-30 P 12-11193	15-30 P 12-11193	66-20 P 12-11192	5-15 P 90-08938	6-15 P 90-08853
AMPERAGE	3 A	1.5 A	24 A	6 A	24 A	6 A	1 A	.5 A
BTU/HOUR	1023	1023	1400	1400	3400	3400	400	400
HEAT DISSIPATION	300 W	300 W	400 W	400 W	1000 W	1000 W	118 W	118 W
SHIPPING WEIGHT (APPROXIMATE)	120 LBS 55 KG	120 LBS 55 KG	300 LBS 136 KG	300 LBS 136 KG	400 LBS 182 KG	400 LBS 182 KG	225 LBS 102 KG	225 LBS 102 KG

* SPECIFICATIONS HAVE BEEN FIGURED ON THE MAXIMUM CONTAINED IN EACH UNIT.

MR-0790

Modules Included in the Basic System

Processor

KD11-P (M7264-BB)

Resident memory addressed as bank 0
CPU refresh disabled
Powers up to 173000

Or

KD11-Q (M7264-YB)

No resident memory
CPU refresh disabled
Powers up to 173000

Memory

MSV11-B (M7944)

4K RAM
Three in basic system with KD11-P
Addresses start at bank 1
Refreshed by REV11-C

Or

MSV11-C (M7955-YD)

16K RAM
One in basic system with KD11-Q
Addresses start at bank 0
Internal refresh

Serial Line Interface

DLV11 (M7940)

Device address 177560
Vector 60
9600 baud
EIA
One stop bit, eight data bits, no parity

D324

Disk Drive Interface

RKV11-D

Interfaced to computer by M7269
Device address 177400
Vector 220

Bootstrap/Diagnostic

REV11-C (M9400-YC)

Bootstrap enabled
Diagnostic enabled
Refresh enabled for MSV11-B
Refresh disabled for MSV11-C

Terminator

TEV11 (M9400-YB)

120 Ω terminator

Optional Modules for Recommended Expansion

LA180 Printer Interface

LAV11 (M7949)

Device address 177510
Vector 200

Or

LPV11 (M8027)

Device address 177510
Vector 200

RX01 Floppy Disk Interface

RXV11 (M7946)

First device address (disk 0) 177170
First vector 264
Second device address (disk 1) 177150
Second vector 270

Communications Interface

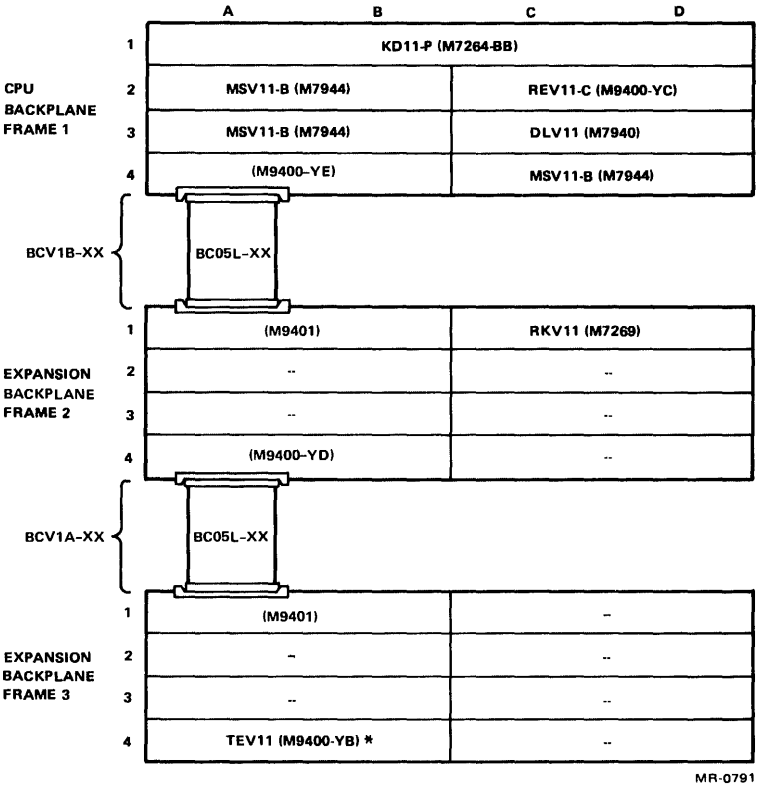
DUV11 (M7951)

Device address 160010
Vector 440

DLV11 (M7940)

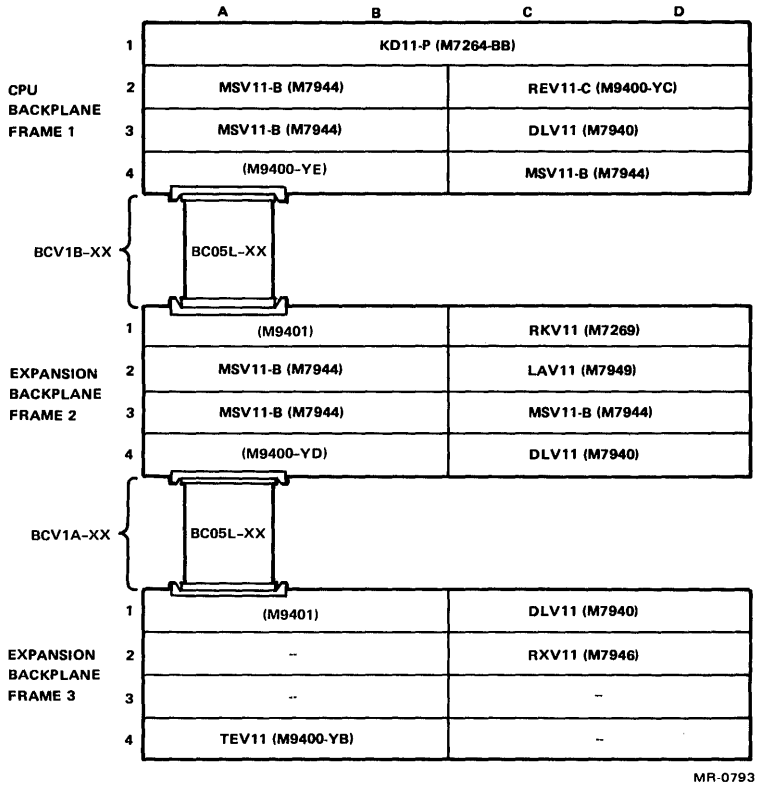
Device address:
console 177560
second terminal 176500

Vector:
console 60
second terminal 300

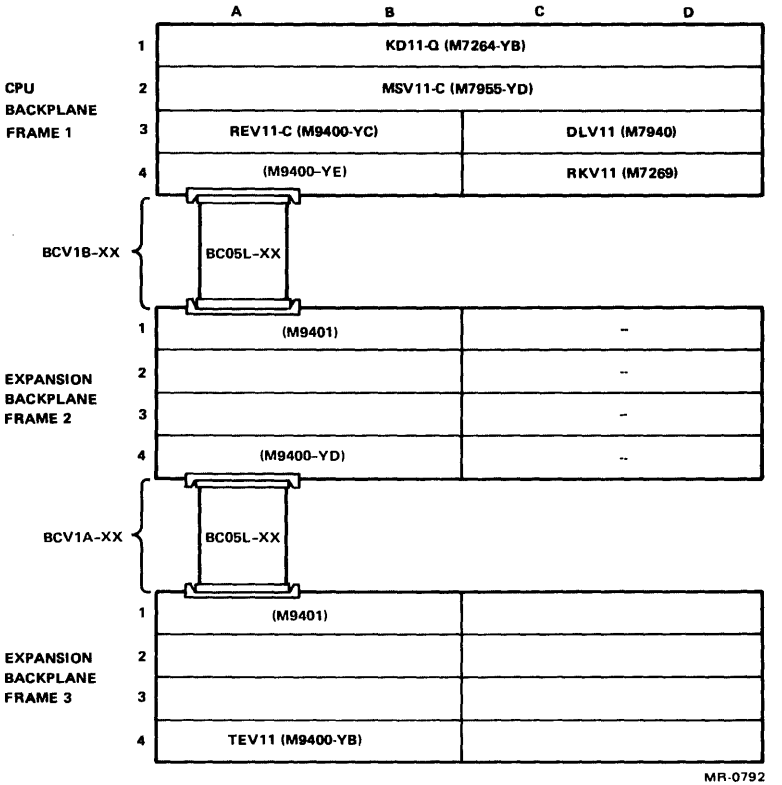


*IN MOST CASES M9400 MODULES ARE PLACED IMMEDIATELY FOLLOWING THE LAST MODULE IN THE SYSTEM. THE TEV11, HOWEVER, IS AN EXCEPTION TO THE GENERAL RULE. IN THE BUSINESS PRODUCTS SYSTEMS IT IS PLACED IN THE LAST SLOT OF THE LAST BACKPLANE IN ORDER TO MINIMIZE NOISE.

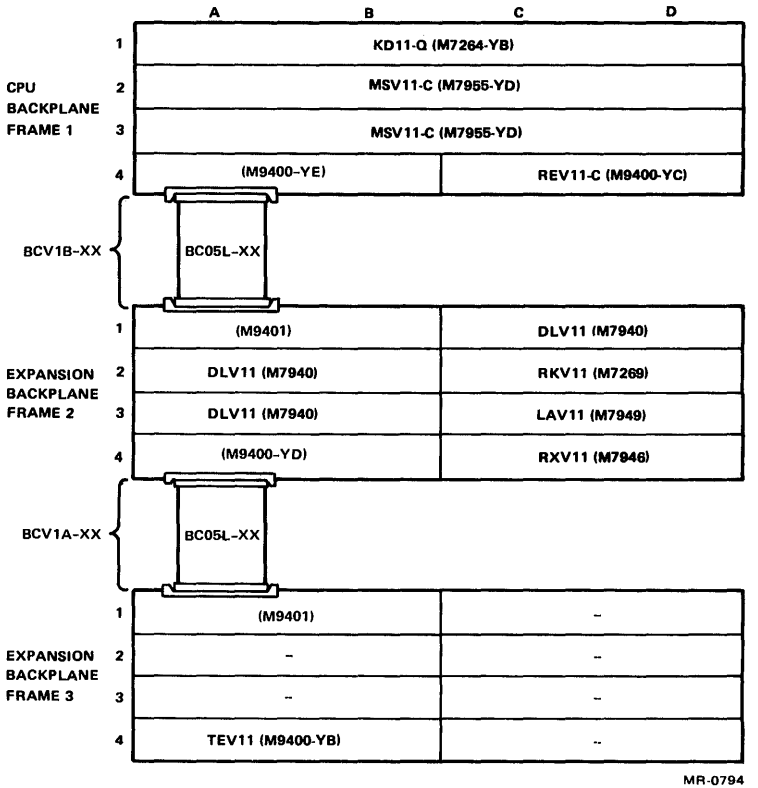
D324 Module Utilization Drawing for Basic System Using PDP-11/03-JA or - JB CPU Box



D324 Module Utilization Drawing for Recommended Expanded Systems Using PDP-11/03-JA or -JB CPU Box



D324 Module Utilization for Basic System
Using PDP-11/03-JC or -JD CPU Box

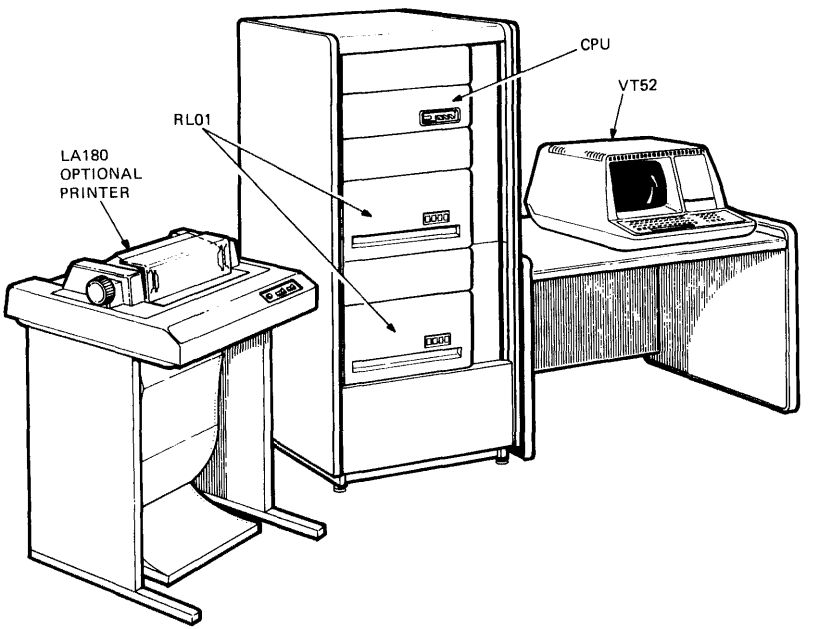


D324 Module Utilization for Recommended
Expanded Systems Using PDP-11/03-JC or -JD CPU Box

D325

The D325 system, with DIGITAL's fully supported CTS-300 software license and DIBOL instruction set, includes the PDP-11/03 central processor, 64K bytes of MOS memory, bootstrap loader, serial line interface, and VT52 CRT console terminal. There is an RLV11 controller with dual five-megabyte removable disk drives (RL01) for use as a system device and as a primary backup and load device. This configuration is arranged in an H9602 cabinet and an H9532-AA desk.

Space is reserved in this configuration for a printer. Any of the following may also be added: additional RL01 disk drives plus cabinet, dual floppy disk unit, choice of four printers, up to three video or hard-copy terminals and/or a 2780 communication package and CTS-300 DICAM (a software package).



D325 System

	Model Designation	
D325A	AA	AD
Input Power/Frequency	115/60	230/50
H9602	CM	CN
PDP-11/03	NC	ND
RL01	AK	AK
H9532	AA	AA
VT52	NE	NF
LA180*	PA	PD

*Model AA + LA180 = Model BA,
Model AD + LA180 = Model BD.

D325 SPECIFICATIONS

	PRINTER LA180		RL01 CABINET		CPU CABINET		VT52 DESK	
	115V 60HZ	230V 50HZ	115V 60HZ	230V 50HZ	115V 60HZ	230V 50HZ	115V 60HZ	230V 50HZ
POWER CONNECTOR	15A 	15A 	30A W 	30A W 	30A W 	20A X G 	15A 	15A 
NEMA NO	5-15 P	6-15 P	15-30 P	15-30 P	15-30 P	66-20 P	5-15 P	6-15 P
DEC P/N	90-08938	90-08853	12-11193	12-11193	12-11193	12-11192	90-08938	90-08853
AMPERAGE	3 A	1.5A	2.6A	1.3A	8A	4A	1A	.5A
BTU/HOUR	1023	1023	1100	1100	3400	3400	400	400
HEAT DISSIPATION	300W	300W	300W	300W	960W	960W	118W	118W
SHIPPING WEIGHT (APPROXIMATE)	120 LBS 55 KG	120 LBS 55 KG	275 LBS 125 KG	275 LBS 125 KG	350 LBS 159 KG	350 LBS 159 KG	225 LBS 102 KG	225 LBS 102 KG

MR-4883

D325

Modules Included in the Basic System

Processor

KD11-Q (M7264-YB)

No resident memory
CPU refresh disabled
Powers up to 173000

Memory

MSV11-DD (M8044)

64K byte MOS RAM
One in basic system
Addresses start at bank 0
Internal refresh

Serial Line Interface

DLV11 (M7940)

Device address 177560
Vector 60
9600 baud
EIA
One stop bit, eight data bits, no parity

Disk Drive Interface

RLV11 (M8013 and M8014)

Device address 174400
Vector 160

Bootstrap

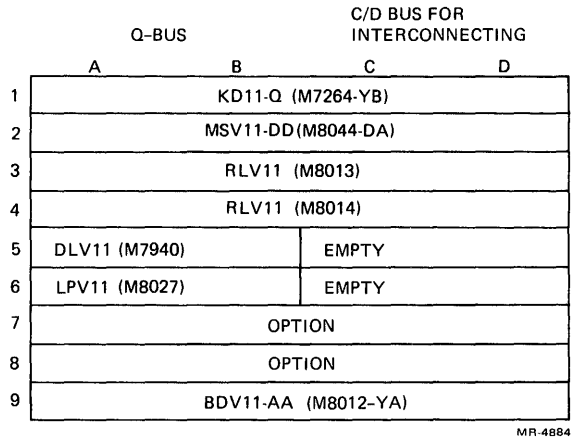
BDV11-AA (M8012)

Bootstrap enabled
Real time clock enabled (switch B5)

LA180 Printer Interface

LPV11 (M8027)

Device address 177514
Vector 200



D325 Module Configuration Using PDP-11/03-NC or PDP-11/03-ND Box

D333C

The D333C data system with DIGITAL's fully supported CTS-300 software license and DIBOL instruction set includes the PDP-11/23 microcomputer with 128K bytes of MOS memory, a four-channel serial line interface with bootstrap/terminator and a VT100 CRT console terminal. There is an RXV21 controller for a dual RX02 floppy disk storage medium. This configuration is arranged in an H9642 system cabinet and an H9532 work table. This system can be expanded for greater storage capacity.

	Model Designation	
D333C	AA	AD
Input Power/Frequency	115/60	230/50
H9652	-	-
PDP-11/23	AA	AB
VT100	NA	NB
LA180	PA	PD
RX02	BA	BC

D333C

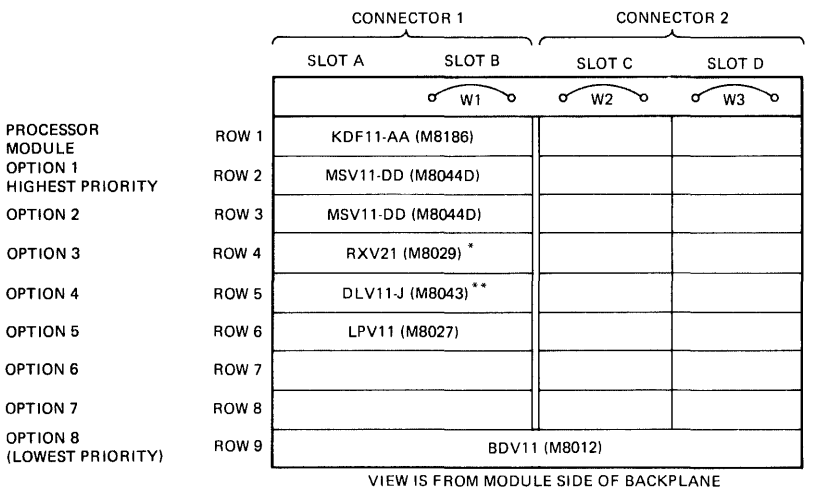
Compatible Options

- An additional 128K bytes memory
- Additional video or hard-copy terminals for a total of four
- Additional storage medium
  Second dual floppy disk (1 megabyte storage)
- Choice of printers
- BATCH or interactive communication software languages:

  DICAM - Data System Interactive Communications Access Method (for IBM 360/370 hosts)

  DIBOL - DIGITAL Business-Oriented Language

  RDCP - 2780/3780 BATCH Communication Package.



*NOTE: MUST BE AT CS REVISION 'E1' OR HIGHER.
**NOTE: MUST BE AT CS REVISION 'E' OR HIGHER.

MR-4885

D333 Module Configuration

D335C

The D335C data system, with DIGITAL's fully supported CTS-300 software license and DIBOL instruction set, includes the PDP-11/23 microcomputer with 128K bytes of MOS memory, a four-channel serial line interface with bootstrap/terminator, and a VT100 CRT console terminal. There is an RLV11 controller with 10-megabyte removable RL01 dual disk drives for use as a system device and a primary backup and load device. This configuration is arranged in an H9642 system cabinet and an H9532 work table.

Space is available in this configuration for a printer.

	Model Designations	
D335C	AA	AD
Input Power/Frequency	115/60	230/40
H9642	-	-
PDP-11/23	AA	AB
RL01	AK	AK
H9532	AB	AB
VT100	NA	NB
LA180*	PA	PD

*Optional

Modules Included in the Basic System

Processor

KDF11-AA (M8186)

Memory management standard
KEF11-A floating point (optional)

Memory

MSV11-DD (M8044)

64K bytes MOS RAM (two in basic system)
Addresses start at bank 0
Internal refresh

D335C

Serial Line Interface

DLV11-J (M8043) (Must be at CS revision "E" or higher.)

Console device address 177560
Vector address 60
9600 baud
EIA RS423 and RS-232C
One stop bit, eight data bits, no parity

Disk Drive Interface

RLV11 (M8013 and M8014)/RL01

Device address 174400
Vector address 160

Bootstrap

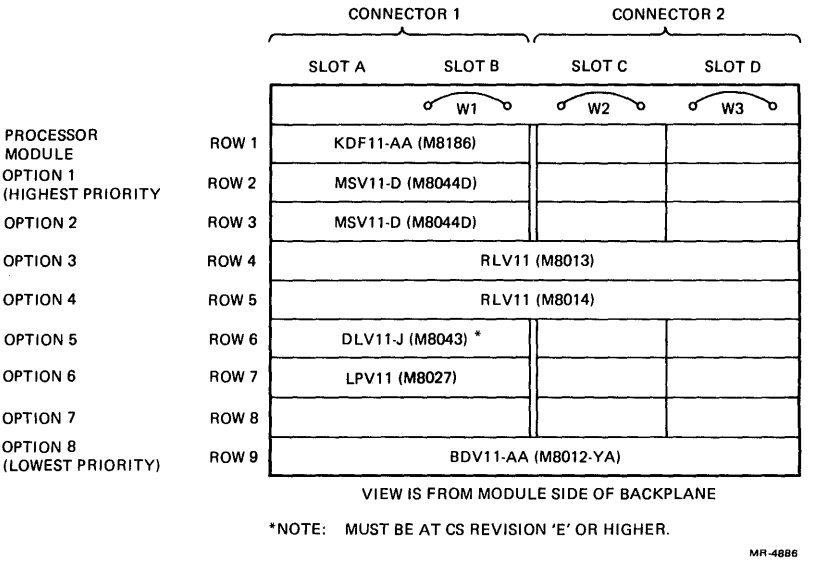
BDV11-AA (M8012)

Bootstrap enabled
Real time clock enabled (switch B5)

LA180 Printer Interface

LPV11 (M8027)

Device address 177514
Vector address 200



D335 Module Configuration

D336C

The D336C data system, with DIGITAL's fully supported CTS-300 software license and DIBOL instruction set, includes the PDP-11/23 microcomputer with 128K bytes of MOS memory, a four-channel serial line interface with bootstrap/terminator, and a VT100 CRT console terminal. There is an RLV11 controller with 20-megabyte removable dual RL02 disk drives for use as a system device and a primary backup and load device. This configuration is arranged in an H9642 system cabinet and an H9532 worktable.

Space is available in this configuration for added expansion such as a printer, a serial line interface, synchronous communication, memory, floppy control, etc.

	Model Designations	
D336C	AA	AD
Input Power/Frequency	115/60	230/50
H9642	-	-
PDP-11/23	AA	AB
RL02	AK	AK
H9532	AB	AB
VT100	NA	NB
LA180*	PA	PD

*Optional

Modules Included in the Basic System

Processor

KDF11-AA (M8186)

Memory management standard
KEF11-A floating point (optional)

Memory

MSV11-DD (M8044)

64K bytes MOS RAM (two in basic system)
Addresses start at bank 0
Internal refresh

Serial Line Interface

DLV11-J (M8043) (Must be at CS revision "E" or higher.)

Console device address 177560

Vector address 60
9600 baud
EIA RS423 and RS-232C
One stop bit, eight data bits, no parity

Disk Drive Interface

RLV11 (M8013 and M8014)/RL02

Device address 174400
Vector address 160

Bootstrap

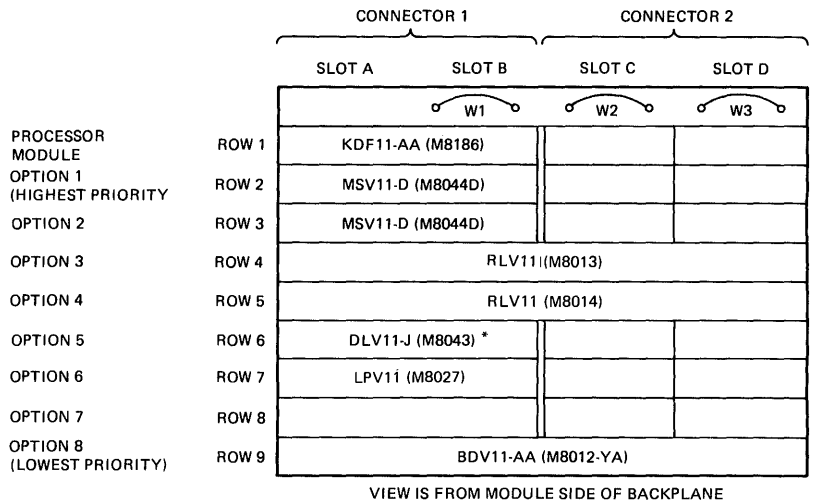
BDV11-AA (M8012)

Bootstrap enabled
Real time clock enabled (switch B5)

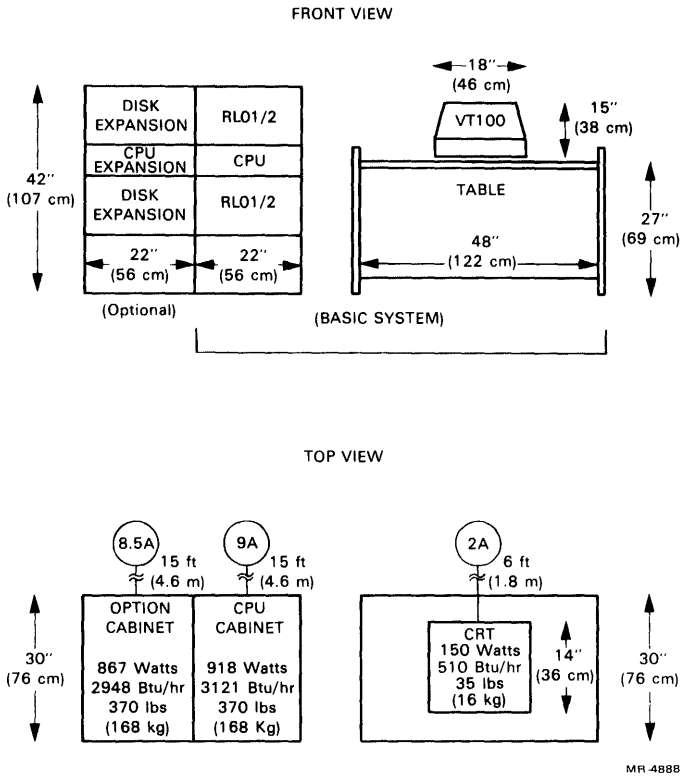
LA180 Printer Interface

LPV11 (M8027)

Device address 177514
Vector address 200



D336 Module Configuration



D325, D335, and D336 Data Systems

TELEPHONE COMPANY SYSTEM

CC1A PDP-11V03 SYSTEM

A non-DIGITAL terminal is used with this system. The terminal is a Tektronix™ 4023 AN. The Tektronix terminal must be an "AN" version and is configured for 9600 baud and checked out by the Western Electric Company (WECO) representative.

For installation, a null modem is provided by DIGITAL Field Service. Use of an H312 null modem will cause receive status errors, therefore a BC03M-L cable is recommended for installation checkout. The terminal will be connected through the null modem directly to the DLV11, by-passing the Bell interface cabinet located on top of the PDP-11V03 cabinet. After system check, the WECO representative will connect the Bell interface.

When running the Tektronix terminal after the screen is full, the first seven characters will be scrambled owing to terminal and software incompatibilities. Hit the ERASE key or change the baud rate on the back of the terminal (rotary SW) and DLV11 interface to 2400 baud. The diagnostics will run at this lower speed. Remember to return the system to 9600 for the customer.

Step 4 of the installation procedure asks the DIGITAL Field Service engineer to show that the floppy disk will boot from drives 0 and 1. Other versions of the monitor would only boot from drive 0, but recent shipments of this system should contain the newer floppies that will boot from both drives.

Step 4 also asks the DIGITAL engineer to demonstrate the clock diagnostic VKAHAO for at least 10 minutes. After several passes, the "TIME" printout must have incremented to indicate that the clock is running. The clock is unlike most PDP-11 real time clocks in that it is only a line "BEVNT" which goes to the CPU causing an interrupt. If it is not working, check the "LTC" switch on front panel and items in FA&T checklist, sheets 15 and 16.

For troubleshooting, the two backplanes can be separated by removing the M9400-YE in slot 4 and switching DRV11 No. 1 and DLV11 (see sheet 11 of configuration). This will allow the BA11-MA to function as a system without the BA11-ME connected. Remember to reconfigure to the original condition when finished.

TELEPHONE COMPANY SYSTEM

DRV11 No. 1 and DRV11 No. 2 must be set up properly for the slot position where they are located or the wrong lines may be connected to them.

The *PDP-11/V03 System Manual*, EK-11V03-TM, should be available to the Field Service engineer for 11V03 and diagnostic information. The *Microcomputer Handbook* is also a good source of technical PDP-11V03 information.

CC# 1A Diagnostic Check List

RXDP Diskettes

- ☐ #1
- ☐ #2
- ☐ #7
- ☐ #10
- ☐ #15
- ☐ #25
- ☐ #26
- ☐ #30
- ☐ SPECIAL DECX 4

☐ 11V03 ———	VKAAAO	Basic Inst. Test	#25
☐ ———	VKABAO	EIS	#25
☐ ———	VKACBO	FIS	#25
☐ ———	VKADBO	TRAPS	#25
☐ ——— 1 —	VKAHAO	TIME	#25
☐ DLV11 M7940 ———	VKAEB1		#25
☐ DRV11 M7941 — 2 —	VKAFBO		#25
☐ MSV11CD M7955 —	ZKMADO		#25
☐ RXV11 M7946 — 3 —	ZRXBEO		#15
☐ ———	ZRXAEO		#15
☐ REV M9400-YA ———	ZM9ADO		#10

1. Run two passes minimum, approximately 10 minutes and check that "TIME" printout is incrementing.

2. Use a BC08R-1 loopback cable for testing. Diagnostic will come up testing DRV11 No. 2; therefore, after several passes, halt CPU and change address and vector information as shown:

```
$DX0
DZQUJ-C 21-JUL-76 R
.R VKAFB0
END OF PASS
END OF PASS
END OF PASS

004410
@1200/167770 167760
001202/167772 167762
001204/167774 167764
001206/167773 167763
001210/000300 310
001212/000302 312
001214/000304 314
001216/000306 316
001220/167770
@200GEND OF PASS
END OF PASS

004402
@
```

TESTING OF DRV11 2

MODIFICATION OF PROGRAM ADDRESS AND VECTORS FOR DRV11 1
TYPE L.F. AFTER ENTRY ONLY.
TYPE C.R. ON LAST ENTRY.
TYPE 200G.
TESTING OF DRV11 1

3. Run ZRXBEO before running ZRXAEO.

4. Special DECX map:

```
.MAP

CPAF0 AT 017752 STAT 040020
CPBI0 AT 021502 STAT 040020
FPAF0 AT 023242 STAT 040020
DRCH0 AT 024522 STAT 040020
BMCM0 AT 025430 STAT 040020
RXAD0 AT 030054 STAT 140000
.
```

5. Diagnostics available on single floppy.

NOTE

This is not an official software package and is intended for field use only.

ENTRY#	FILNAM.EXT	DATE	LENGTH	START
000001	RXDP .BIN	7-MAR-78	17	000050
000002	UPD2 .BIN	7-MAR-78	30	000071
000003	XTECO .BIN	7-MAR-78	26	000127
000004	VKAAA0.BIC	7-MAR-78	17	000161
000005	VKABA0.BIC	7-MAR-78	17	000202
000006	VKACB0.BIC	7-MAR-78	16	000223
000007	VKADB0.BIC	7-MAR-78	12	000243
000010	VKAEB1.BIC	10-MAR-78	7	000257
000011	VKAFB0.BIN	10-MAR-78	6	000266
000012	ZKMAB1.BIC	10-MAR-78	9	000274
000013	ZKMAD0.BIC	10-MAR-78	9	000305
000014	ZRXBE0.BIC	10-MAR-78	17	000316
000015	ZRXAE0.BIC	10-MAR-78	20	000337
000016	ZM9AD0.BIC	10-MAR-78	7	000363
000017	VKAHA0.BIC	4-APR-78	17	000372
000020	CHAIN .CCC	5-APR-78	1	000413

CC# 1A Module Jumper Information

Module	Option	Jumpers	*Microcomputer Handbook* Page
M7264	CPU	W4, W6, W9 IN	243, 236
M7955	MSV11CD	1-5 ON, 6-8 OFF	244
M7955	MSV11CD	3, 6, 7, 8 OFF, others ON	244
M7941	DRV11 No. 1	A3, A12 IN [A = 767760] V4, V5 IN [V = 310]	290
M7941	DRV11 No. 2	A12, V3, V4, V5 IN [A = 767770 V = 300]	290
M9400-YA	REV11-A	Remove W2	380
M7940	DLV11	Refer to *Micro Handbook*	259

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

MANUFACTURING SPECIFICATION — DATE 14 JUN 78

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	DLV11 is currently being shipped with system due to unavailability of DLV11-F. Change package to reflect DLV11 instead of DLV11-F.	1	J.Tomaswick	6/14/78	J.Tomaswick	6/14/78

ENG	APPD	SIZE	CODE	NUMBER	REV
J.Tomaswick		A		MFGENG-0 CONF-0004	A

EN-01083-16-N672-(392)

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

INDEX

SIZE	CODE	NUMBER	REV
A		MFGENG-0 CONF-0004	A

DEC 16-(392)-1082-N672

SHEET 1 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

CONFIGURATION APPROVALS

_____
Digital Account Representative

_____
Digital Project Manager

_____
Digital Manufacturing Engineering Manager

_____
Digital Quality Control Manager

_____
Digital Field Service Product Support

_____
Digital TELCO Engineering

_____
Diagnostic Engineering

_____
Production Manager

* CONFIGURATION REVIEWED

_____
Bell Labs Representative

_____
Western Electric Purchasing

*Any review of these specifications by any Bell System representative shall be for general arrangement of the work and shall in no case relieve you in any way of your responsibilities as defined by our purchase orders.

	SIZE	CODE	NUMBER	REV
	A		MFGENG-0 CONF-0004	*

DEC 16-(392)-1082-N672

SHEET 2 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

TO THE USERS OF THIS DOCUMENT:

This is a Digital Manufacturing Specification for a DEC system purchased by Western Electric. Configuration approvals are included in order to assure that a system is manufactured in accordance with the latest known requirements.

The information contained herein is consistent with the information included in:

Bell Telephone Laboratories - SD# 1P039-01
Western Electric J-Drawing - # J1C016K-1
DEC Standard Price List

It is imperative that the Bell Laboratories and/or Western Electric Purchasing signatories contact the Digital Account Representative in the event of changes to the SD and/or J-drawing. Should these changes affect the contents of this document, the Digital Account Representative shall contact the Digital Project Manager who, in turn, shall have this document updated. Conversely, no changes shall be made to the product manufactured under this specification without written notification to and expressed approval of the Bell System signatories.

When Digital issues a new price list, the Digital Account Representative shall assure that all requisite equipment continues to be offered under the DEC codes listed herein. If any of these items is no longer listed, either of the following procedures shall apply.

1) The Digital Account Representative shall notify the Bell Laboratories and Western Electric signatories of changes to nomenclature and packaging in order to include the then current equipment lists in the next issued SD and J-drawing.

-or-

2) The Digital Project Manager shall convene a configuration review committee meeting (attended by all the signatories of this document or their designated representatives) for the purpose of identifying the alternate equipment to be used for this project configuration. At such a time, the short-term requirements and availabilities of the equipment listed herein shall be determined and the appropriate transition plans shall be made.

Digital Field Service shall adhere to the information contained in this document. If the end-user wishes anything different, the end-user should be told to contact the appropriate Western Electric Regional Office.

This specification is included with all shipments of DEC equipment for this project.

SIZE	CODE	NUMBER	REV
A		MFGENG-0 CONF-0004	*

DEC 16-(392)-1082-M672

SHEET 3 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

SYSTEM DESCRIPTION

The PDP11V03-WA configuration is a subsystem of the switching control center system's control console No. 1A.

The control console No. 1A is used to provide remote maintenance, alarm, surviellance and control of unattended electronic telephone switching offices. Its most important function is to provide remote control capabilities to restore the telephone switching office to service after certain types of failures. The reliability and availability of the control console are extremely important due to its potential use during critical periods where telephone service in a particular telephone switching office has been interrupted. It may be used in continuous service (24 hr/day) application.

The microcomputer is connected via the DLV11 to a CRT for display of alarm data as well as input of remote control requests. The connection is accomplished via a null modem cable to provide the proper handshaking and data interchange.

A telemetry data network is driven via a DRV11 and is the primary link from the control console to the remote telephone switching office. Another DRV11 sends data to a circuit that drives a local alarm display.

The microcomputer configuration carries a Western Electric designation of J1C016K-1. The telemetry equipment, local alarm interface and cables (including a null modem cable) have a designation of J1C016L-1. The CRT is designated J1C016M-1.

SIZE	CODE	NUMBER	REV
A		MFGENG-0 CONF-0004	A

DEC 16-(392)-1082-N672

SHEET 1 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

CONFIGURATION NOTES

1. This is a fixed configuration. There is no optional equipment.

2. Diagnostic media is RXDP diskette.

3. The DLV11 will be configured as follows: EIA, 9600 BAUD, 8 data bits, 1 stop, no parity, framing error halt strap removed. Other options not specified here shall be set to DEC Standards.

4. The REV11 will be configured as follows: DMA refresh disabled, ROM enabled.

5. At the time of installation or service call, a working 9600 BAUD terminal compatible with the system must be made available by the customer.

6. Warranty is 90 days from date of installation or six months from ship date, whichever comes first.

7. The clock operation must be verified by running MD-11-DVKAH-XX a minimum of two passes. See item 7 on page 15.

8. The ability of the system to boot MAINDEC 11 - DZQUJ-DO from both drive #0 and #1 must be demonstrated.

9. System enviromental requirements will be in accordance with Bell System BSP - Section 760-251-150, "Site Prep and Enviromental Considerations for Minicomputers in Standard Systems".

10. For installation testing, a null modem is required between the DLV11-F serial line unit and the 9600 BAUD terminal. DEC shall provide this null modem during installation testing of PDP 11V03/WA.

11. Installer will remove DRV11 #1 and #2 and visually verify the vector address on each per the Device Address Assignment Sheet. Using DEC diagnostic MD-11DVKAF-B only one DRV11 will be run at a time.

12. Maximum current limitation on power strip for use by customer is four (4) amps.

13. The DRV11's will have a label placed on the handle on side 2 depicting the address and vector of the DRV11 as per the following example:

DRV11 #1 ADD 767760 VECT 310
or
DRV11 #2 ADD 767770 VECT 300

SIZE	CODE	NUMBER	REV
A		MFGENG-0 CONF-0004	A

DEC 16-(3S2)-1082-N672

SHEET 5 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

CONFIGURATION NOTES (cont.)

14. In order to assure a higher quality level, pages 15 and 16 (Telco FA&T 11V03WA, SCCS Control Console NO. 1A (CC NO. 1A) Configuration Checklist) is to be completed by the PSI personnel for each system. Their initials will signify that they have completed or verified each indicated procedure.

SIZE	CODE	NUMBER	REV
A		MFGENG-0 CONF-0004	*

DEC 16-(302)-1082-N672

SHEET 6 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

EQUIPMENT LIST

One (1) 11V03WA composed of the following:

ITEM	QTY	DESCRIPTION
1	1	11/03-KA consisting of: -MSV11-CD -KEV11A -KD11-R -BA11-MA
2	2	DRV11
3	1	DLV11
4	1	MSV11-CD
5	1	REV11-A
6	1	BA11-ME
7	1	BCV1B-06
8	1	H984-DA
9	1	BC05C-25
10	1	RXV11-BA

SIZE	CODE	NUMBER	REV
A		MFGENG-0 CONF-0004	A

DEC 16-(3982)-1082-N672

SHEET 7 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

INSTALLATION PROCEDURE

The control console No. 1A consists of:

-DEC Processor, J1CO16K-1
-Interface Unit, J1CO16L-1
-Tektronix model 4023AN CRT Terminal, J1CO16M-1

After the above equipment has arrived at the site storage location, the following procedures and guidelines shall be followed.

1. The Western Electric (WECO) installer shall verify that the CRT terminal is operational.

2. The WECO installer shall make arrangements for the DEC representative to be at the job location and will secure permission for movement of the DEC processor from the storage location to the job site.

3. At the job site, WECO installation shall provide all labor required for unpacking and placing the equipment in the desired location. The DEC representative will supervise the unpacking and placement of DEC equipment and verify any evident damages for subsequent claims.

4. After the WECO installer has mounted the interface unit on the processor and lowered the interconnect cables to the processor area, the DEC installer will run diagnostics on the processor. The DEC installer will provide the null modem cable to interconnect the DLV11 to the CRT terminal for testing. In addition to DEC diagnostics, the DEC installer shall demonstrate the capability to boot from drive 0, Drive 1 and demonstrate that the system clock is operational.

5. Upon successful completion of the diagnostics, the DEC installer shall connect the following cables, previously lowered by the WECO installer, to the processor.

   "J1-DRV(2).side up"
   "J2-DRV(2).side up"
   "J-DLV.side up"
   "J1-DRV(1).side up"
   "J2-DRV(1).side up"
   AC Power Plug

6. The DEC installer shall demonstrate that the removal and reinsertion of processor boards for cable connection did not affect processor operation.

7. Upon successful completion, the WECO installer will accept the DEC processor and initiate control console No. 1A diagnostics.

SIZE	CODE	NUMBER	REV
A		MFGENG-0 CONF-0004	A

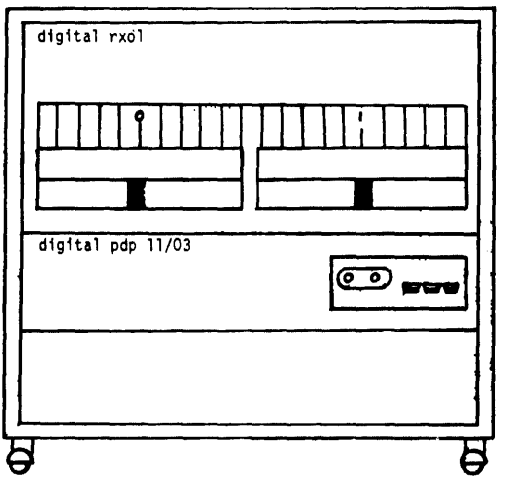
DEC 10-(392)-1082-M678

SHEET 8 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCSS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

CABINET LAYOUT



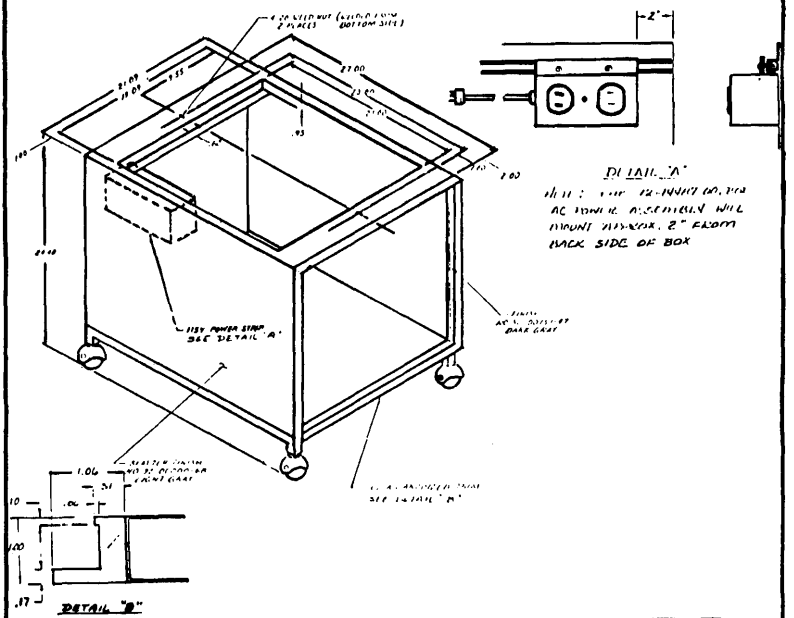
	SIZE	CODE	NUMBER	REV
	A		MFGENG-0 CONF-0004	*

DEC 16-(3082)-1082-N672

SHEET 9 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION



LEGEND	
MODEL NO.	DESCRIPTION
M984-DA	24-13007-02
	78-1612
	12-14481-00

	SIZE	CODE		REV
	A		MFGENG-0 CONF-0004	*

DLC 16-(302)-1082-N672

SHEET 10 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

CABINET LAYOUT

BA11-MA

	A	B	C	D
1		M7264-YA	(KD11-H)	
2		M7955	(MSV11-CD)	
3		M7955	(MSV11-CD)	
4	M9400-YE		M7941	(DRV11 #1)

BA11-ME

	A	B	C	D
1	M9401		M7940	(DLV11)
2	M7946	(RXV11)	M7941	(DRV11 #2)
3	M9400-YA	(REV11-A)	UNUSED	
4	UNUSED		UNUSED	

SIZE	CODE	NUMBER	REV
A		MFGENG-0 CONF-0004	A

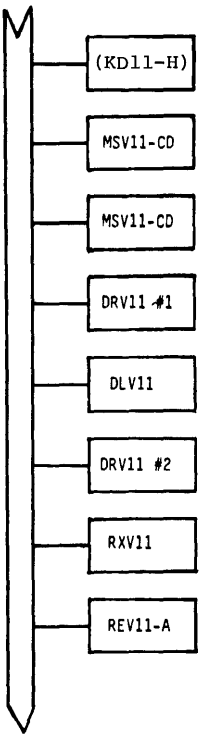
DEC 16-(3B2)-1062-M672

SHEET 11 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

BUS SEQUENCE



SIZE	CODE	NUMBER	REV
A		MFGENG-0 CONF-0004	A

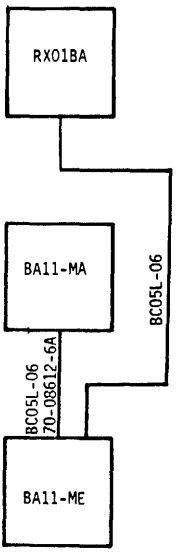
DEC 16-(092)-1082-N672

SHEET 12 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

CABLE LAYOUT



	SIZE	CODE	NUMBER	REV
	A		MFGENG-0 CONF-0004	*

DEC 16-(392)-1082-N672

SHEET 13 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE

DEVICE ADDRESS ASSIGNMENT

DEC DESIGNATION	WECO DESIGNATION	REGISTER ADDRESS	VECTOR ADDRESS	PRIORITY	MOUNTING CODE	+5VDC	BUS LOADS	COMMENTS
DRV11 #1	Parallel 1	767760	310	1	2 Slots		1	
DRV11 #2	Parallel 2	767770	300	3	2 Slots		1	
DLV11	Serial 1	777560	60	2	2 Slots		1	9600 BAUD
RXV11	Disk-Cont	777170	264	4	2 Slots		1	

NOTE: PRIORITY DETERMINED BY DEVICE CLOSEST TO THE CPU. SEE BUS SEQUENCE: PRIORITY 1 = HIGHEST

SIZE	CODE		REV
A	MFGENG-0 CONF-0004		A

SHEET 14 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

TELCO FA&T 11V03-WA SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CHECKLIST

INITIAL

1.) The cab fan power cord should be plugged into the rear plug of the dual receptacle. (Mounted on side of cab). _____

2.) DRV11's should have a sticker on the module, side 2 under the cable, giving address, vector and DRV11 number 1 or 2. _____

3.) Cables for DRV11 should be installed ribbed side up. _____

4.) Check for a green wire on the console board between TP2 and W4. _____

5.) All ribbon cables should have the red strip on the right. _____

6.) Cable from J2 (console board) should be routed behind the switch panel. _____

7.) Run diagnostic VKAHA0 as shown. If the time is 000000, the clock is not running. Write the time printed for pass number 2: _____ (it takes 5 minutes per pass). _____

```
@DX0
DZQUJ-C 21-JUL-76 RXDP - XXDP RX11/RX01 MONITOR 28K
.R VKAHA0

DVKAH-A
MEMORY= 152726

PASS=000001 ERROR=000000 RXERROR=000000 TIME=044416

PASS=000002 ERROR=000000 RXERROR=000000 TIME=110707
```

8.) DLV11 should be set up for EIA before software is run. (NOTE: Do not ship 70-08360 cable). _____

9.) 74-16240-0-0 stickers on 11V03 and BA11-ME should be filled out as shown. Note that DRV11 #1 is addressed at 767760, vector 310 and is in the 11V03 box. DRV11 #2 is addressed at 767770, vector 300 and is in the BA11-ME box. _____

SIZE	CODE	NUMBER	REV
A		MFGENG-0 CONF-0004	*

DEC 16-(3B2)-1082-M672

SHEET 15 OF 17

MANUFACTURING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE SCCS CONTROL CONSOLE NO. 1A (CC NO. 1A) CONFIGURATION

CPU

SLOT	MODULE NUMBER A	B	CS REV	ETCH REV	MODULE NUMBER C	D	CS REV	ETCH REV
1	KD		1	1	-R	H	*	*
2	MSV		1	1	-CD		*	*
3	MSV		1	1	-CD		*	*
4	BCV1B-06		*	*	DRV11 #1		*	*

CPU

SLOT	MODULE NUMBER A	B	CS REV	ETCH REV	MODULE NUMBER C	D	CS REV	ETCH REV
1	BCV1B-06		*	*	DLV11		*	*
2	RXV11		*	*	DRV11 #2		*	*
3	REV11-A		*	*				
4								

* = Current Revision

INITIAL

10.) Check that the red light (D1) on the console board goes off when DC power is turned off. _____

11.) Check that drive Ø and drive 1 will boot, load and run RXDP diagnostics (Rev D required). _____

DEC# _____

SIZE	CODE	NUMBER	REV
A		MFGENG-0 CONF-0004	A

DEC 16-(392)-1082-N672

SHEET 16 OF 17

MANUFACTURING SPECIFICATION — CONTINUATION SHEET

TITLE CONFIGURATION CHANGE PAGE

Date	Change #	Requested By	Effective Date**	Production Manager	Material Manager	Pages Affected	Final Approval	Change Description
6/14/78	1	J.Tomaswick	6/14/78			1,4,5,7,8,11,12,14,16	J.Tomaswick	DLV11 is currently being shipped with system due to unavailabilty of DLV11-F. Change Document to reflect DLV11 instead of DLV11-F.

** All ships on or after this date must have change incorporated.

NOTE: These changes will be incorporated in the next release cycle.

REV *

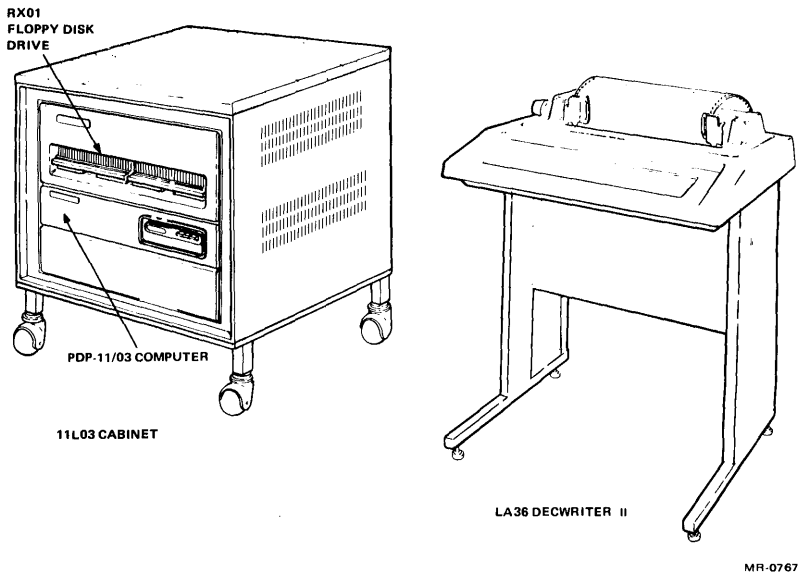
SIZE A | CODE MFGENG-0 CONF-0004 | SHEET 17 OF 17

DEC 16-(302)-1002-4672

LABORATORY SYSTEMS

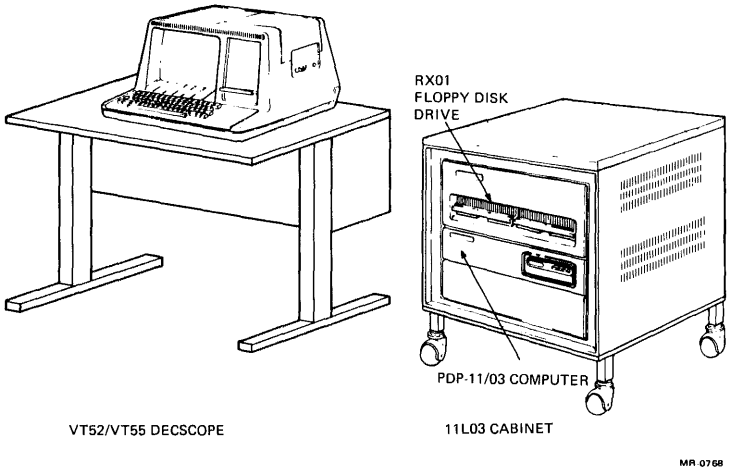
PDP-11L03

The DECLAB-11/03 (11L03) system includes a PDP-11/03 computer, an RX01 dual floppy disk drive, and a terminal. The terminal is normally an LA36 DECwriter II or a VT55 DECscope, although some custom systems may have a VT52. Each system also includes some combination of DECLAB modules and an H322 distribution panel to facilitate user I/O connections. All models are configured to boot on power-up and halt on BREAK. Early systems have 20K of memory, while later versions use a 16K memory. The figures and tables that follow describe the models, specifications, and components.

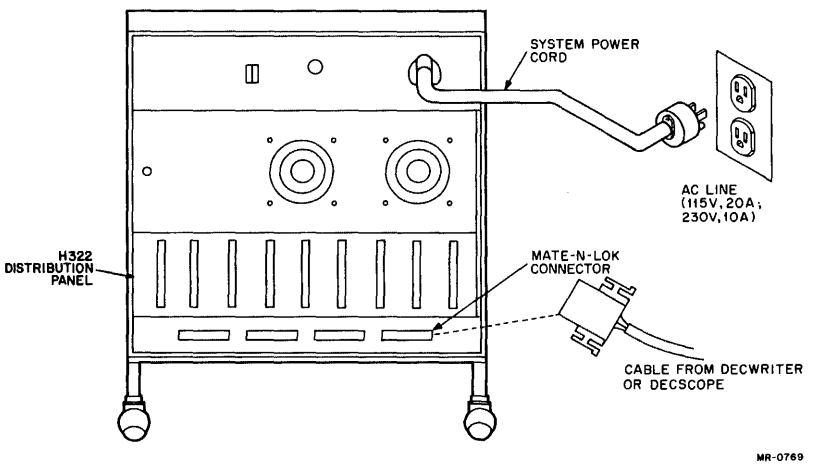


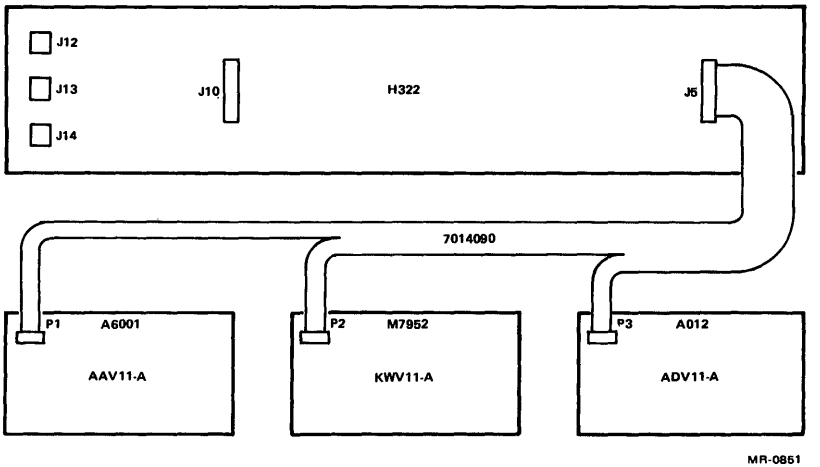
DECLAB-11/03-CA, -CC, -CD, -GD, -HA, -HC, -HD, -MA, -MC, -MD, -KA

PDP-11L03

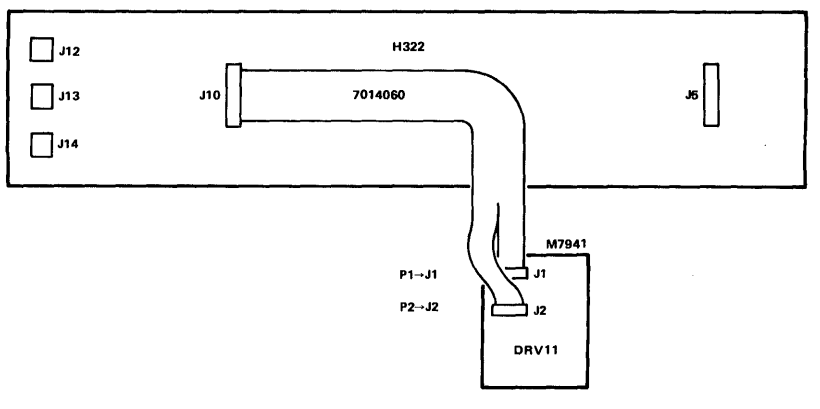


DECLAB-11/03-DA, -DC, -DD, -GC, -JA, -JC, -JD, -NA, -NC, -ND, -LA





Analog Cable Connections



Digital Cable Connections

DECLAB-11/03 System Model Designations

System Requirements	CA	CC	CD	GD	DA	DC	DD	GC	HA	HC	HD
Input Power (V)	115	115	220	115	115	115	220	115	115	115	220
Frequency (Hz)	60	50	50	60	60	50	50	60	60	50	50
PDP-11V03	HA	HC	HD	HA	JA	JC	JD	JA	HA	HC	HD
LA36	DE	DH	DJ	DE	-	-	-	-	DE	DH	DJ
VT55	-	-	-	-	FA	FC	FB	FA	-	-	-
RXV11	BA	BC	BD	BA	BA	BC	BD	BA	BA	BC	BD
H984 (Cabinet)	BA	BA	BB	BA	BA	BA	BB	BA	BA	BA	BB
BA11 Extension Box	ME	ME	MF	ME	ME	ME	MF	ME	ME	ME	MF
ADV11 (AD12)	1	1	1	1	1	1	1	1	-	-	-
KWV11 (M7952)	1	1	1	1	1	1	1	1	1	1	1
AAV11 (A6001)	-	-	-	-	-	-	-	-	1	1	1
DRV11 (M7941)	-	-	-	-	-	-	-	-	1	1	1
IBV11 (M7954)	-	-	-	-	-	-	-	-	-	-	-

DECLAB-11/03 System Model Designations (Cont)

System Requirements	CA	CC	CD	GD	DA	DC	DD	GC	HA	HC	HD
PDP-11V03	JA	JC	JD	HA	HC	HD	JA	JC	JD	HA	JA
Input Power (V)	115	115	220	115	115	220	115	115	220	115	115
Frequency (Hz)	60	50	50	60	50	50	60	50	50	60	60
LA36	-	-	-	DE	DH	DJ	-	-	-	DE	-
VT55	FA	FC	FB	-	-	-	FA	FC	FB	-	FA
RXV11	BA	BC	BD	BA	BC	BD	BA	BC	BD	BA	BA
H984 (Cabinet)	BA	BA	BB	BA	BA	BB	BA	BA	BB	BA	BA
BA11 Extension Box	ME	ME	MF	-	-	-	-	-	-	ME	ME
ADV11 (AD12)	-	-	-	-	-	-	-	-	-	1	1
KWV11 (M7952)	1	1	1	-	-	-	-	-	-	1	1
AAV11 (A6001)	1	1	1	-	-	-	-	-	-	1	1
DRV11	1	1	1	-	-	-	-	-	-	1	1
IBV11 (M7954)	-	-	-	1	1	1	1	1	1	-	-

Specifications

	115 V 50/60 HZ			230 V 50 HZ		
POWER CONNECTOR	PLUG  NEMA # 5-15P DEC # 90-08938		RECEPTACLE  5-15R 12-05351	PLUG  NEMA # 6-15P DEC # 90-08853		RECEPTACLE  6-15R 12-11204
	CPU CABINET	LA36	VT55	CPU CABINET	LA36	VT55
AMPERAGE						
TYPICAL	10.1			4.9		
MAXIMUM	11.3	2.0	2.4	5.5	1.0	1.2
WATTAGE						
TYPICAL	960	160		1000	160	
MAXIMUM	1340	300	300	1380	300	300
BTU/HOUR						
TYPICAL	2730	550	500	2800	550	500
MAXIMUM	3210	1020	1000	3280	1020	1000
WEIGHT						
KG	87.3	46.3	25.8	87.3	46.3	25.8
LBS	192	102	57	192	102	57

MR-0770

Modules Included in the Basic System

Processor

KD11-F (M7264) in systems purchased prior to Oct. 1, 1977.

Resident memory addressed as bank 0
CPU refresh disabled
Powers up to 173000

KD11-R (M7264-YA) in systems purchased after Oct. 1, 1977.

No resident memory
CPU refresh disabled
Powers up to 173000

Memory

MSV11-B (M7944) in systems purchased prior to Oct. 1, 1977.

4K RAM
Refreshed by REV11-A
Addressed as bank 1

MSV11-CD (M7955-YD) in systems purchased after Oct. 1, 1977.

16K RAM
Internal refresh
Addresses start at bank 0
Part of the KD11-R processor option

Serial Line Interface

DLV11 (M7940)

Device address 177560
Vector 60
300 baud in systems using LA36 DECwriter II terminals

9600 baud in systems using VT55 DECscope
20 mA active transmitter and active receiver
One stop bit, eight data bits, no parity
Framing error (BREAK) asserts BHALT

Floppy Disk Interface

RXV11 (M7946)

First device address (disk 0) 177170
First vector 264
Second device address (disk 1) 177150
Second vector 270

Bootstrap/Diagnostic/Terminator

REV11-A (M9400-YA)

Bootstrap enabled
Diagnostics enabled
Refresh enabled in PDP-11V03-A/E
Refresh disabled in PDP-11V03-F/H
120 Ω terminator

Additional Modules Included in Optional Systems*

Analog-to-Digital Converter

ADV11-A (A012)

*For configuration details refer to the "CPU/Options" section.

PDP-11L03

Digital-to-Analog Converter

AAV11-A (A6001)

Programmable Real Time Clock

KWV11-A (M7952)

Parallel Line Unit

DRV11 (M7941)

IEEE Instrument Bus Interface

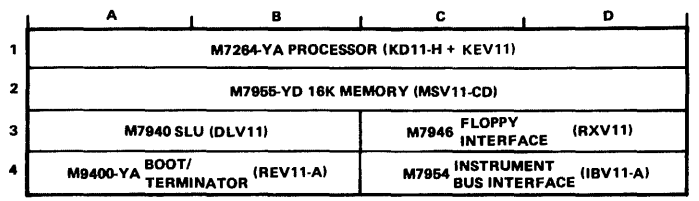
IBV11-A (M7954)

Module Utilization Notes

1. Systems purchased before Oct. 1, 1977 have four MSV11-B 4K memory boards instead of one MSV11-CD module. They also have a KD11-F processor instead of a KD11-H.

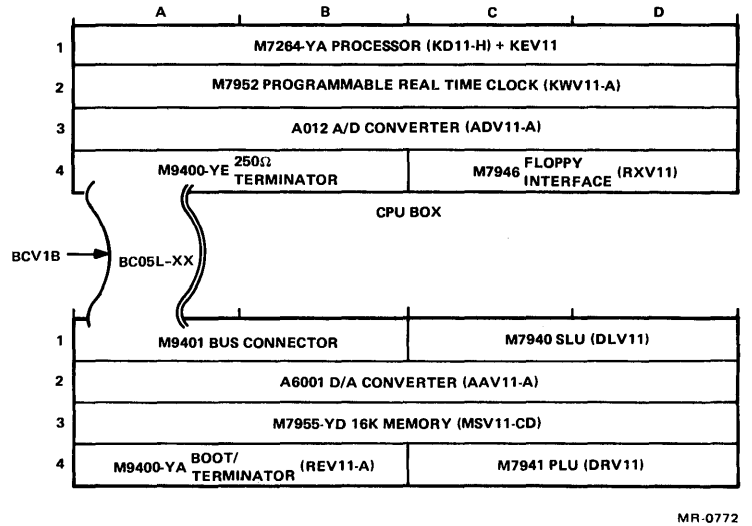
2. KD11-R = KD11-H + MSV11-CD
   KD11-S = KD11-R + KEV11-A

3. All models of PDP-11L03 include the KEV11 EIS/FIS option.



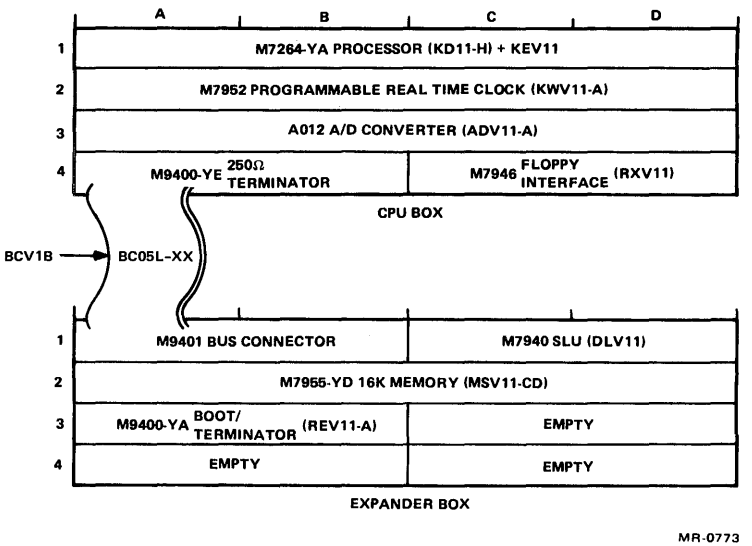
MR-0771

PDP-11L03-MA, -MC, -MD, -NA, -NC, -ND



MR-0772

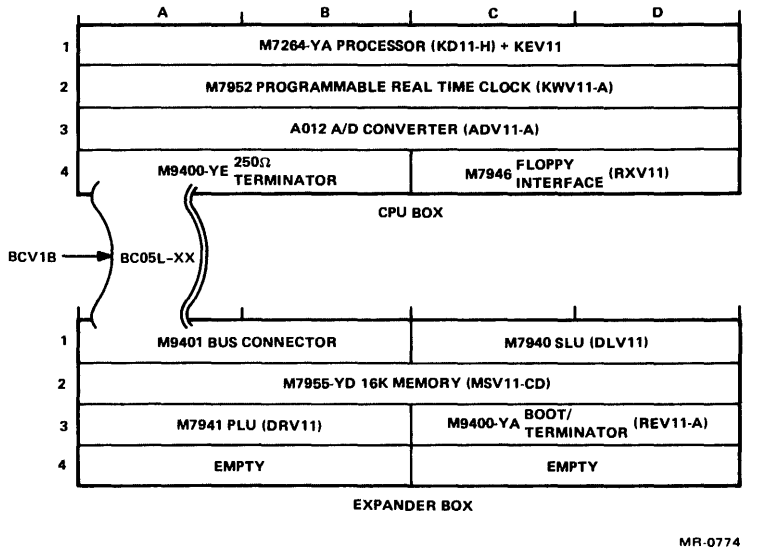
PDP-11L03-KA, -LA



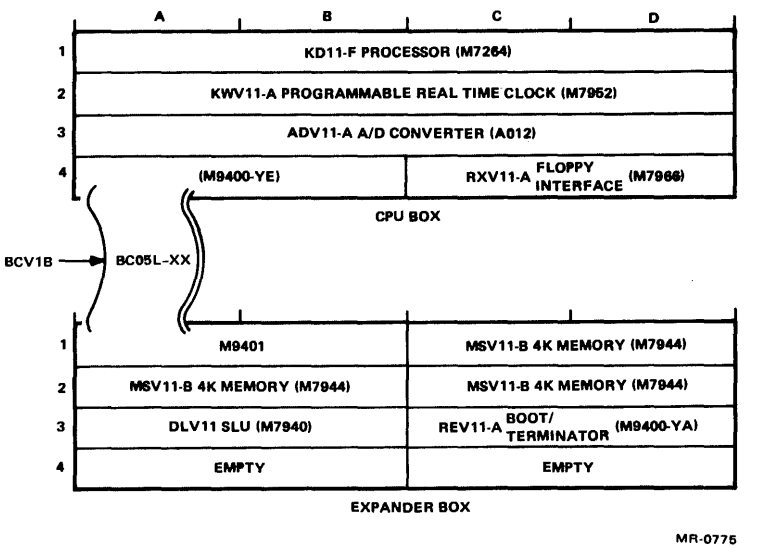
MR-0773

PDP-11L03-HA, -HC, -HD, -JA, -JC, -JD

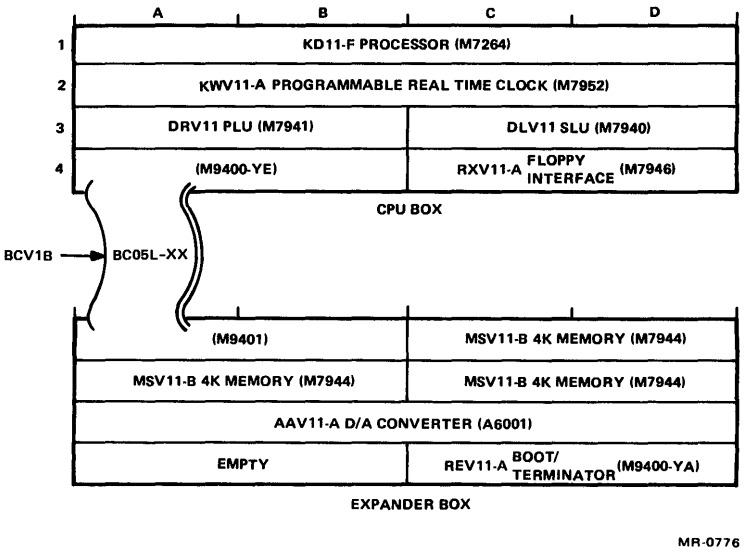
PDP-11L03



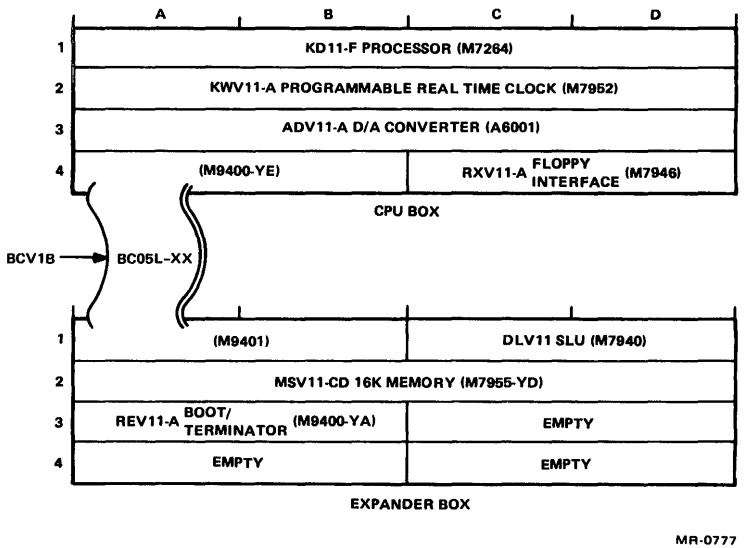
PDP-11L03-CA, -CC, -CD, -GD, -DA, -DC, -DD, -GC



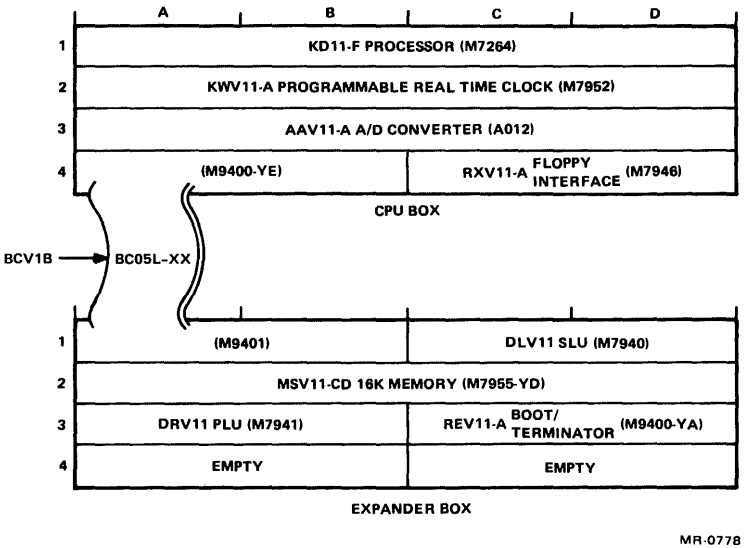
Early 16K PDP-11L03-CA, -CC, -CD, -DA, -DC, -DD Systems



Early 16K PDP-11L03-HA, -HC, -HD, -JA, -JC, -JD Systems



Early 20K PDP-11L03-CA, -CC, -CD, -DA, -DC, -DD Systems



Early 20K PDP-11L03-HA, -HC, -HD, -JA, -JC, -JD Systems

PDP-11/03-BASED MINC/DECLAB-11/MINC SYSTEMS

MODULAR INSTRUMENTATION COMPUTER (MINC)

The **M**odular **IN**strumentation **C**omputer (MINC) is a real time operating system featuring on-line data storage and BASIC software with graphics, scientific, and laboratory subroutine packages. Each system consists of a MINC chassis, an RX02 dual floppy disk drive, and a VT105 terminal mounted on a roll-around cart. The MINC chassis houses a power supply, CPU and related modules, and up to eight MINC laboratory options.

The physical components of a MINC system are grouped into two categories: items common to all MINC systems, and those that can be purchased as options either when the system is first acquired or at some later time as add-ons. Each MINC system is configured to boot on power-up and halt on BREAK. The figures and tables that follow describe the modules, specifications, and components.

All PDP-11/03 MINC systems include the following standard items.

MINC cart, which provides support and transport for:

1. Dual diskette drive (RX02M)

2. MINC chassis (MNCBA) with power supply (H786). This contains:

KD11-NA	- LSI-11 processor with EIS/FIS
MSV11-DD	- Memory (64K bytes) single board
RXV21	- Diskette drive interface
DLV11-J	- Four-channel serial ASCII interface
IBV11-A	- IEEE bus interface
BDV11-A	- Bus terminator/diagnostic/bootstrap module.

3. VT105 terminal with built-in graphics capability.

MINC systems can include some or all of the following lab modules.

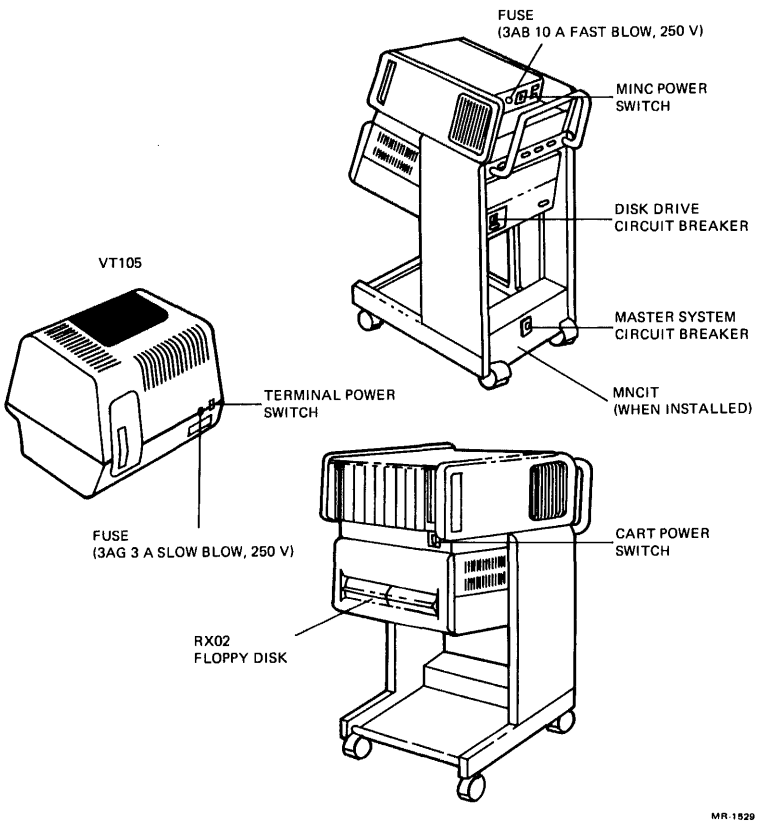
Analog-to-digital converter (MNCAD)
Preamplifier (MNCAG)
Dual multiplexer (MNCAM)
Clock (MNCKW)

11/03-BASED MINC

Digital-to-analog converter (MNCAA)
Digital input unit (MNCDI)
Digital output unit (MNCDO)

MINC systems can also include:

Dot matrix printer (LA35)
Isolation transformer (MNCIT)
110 baud, 20 mA serial line interface (DLV11-KC).

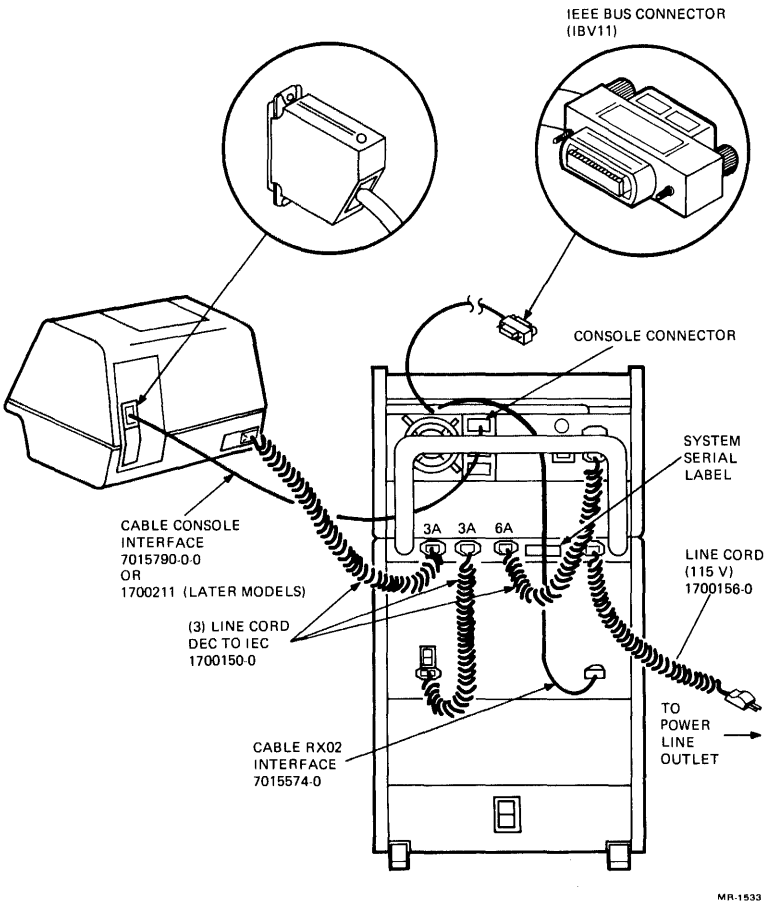


MINC System

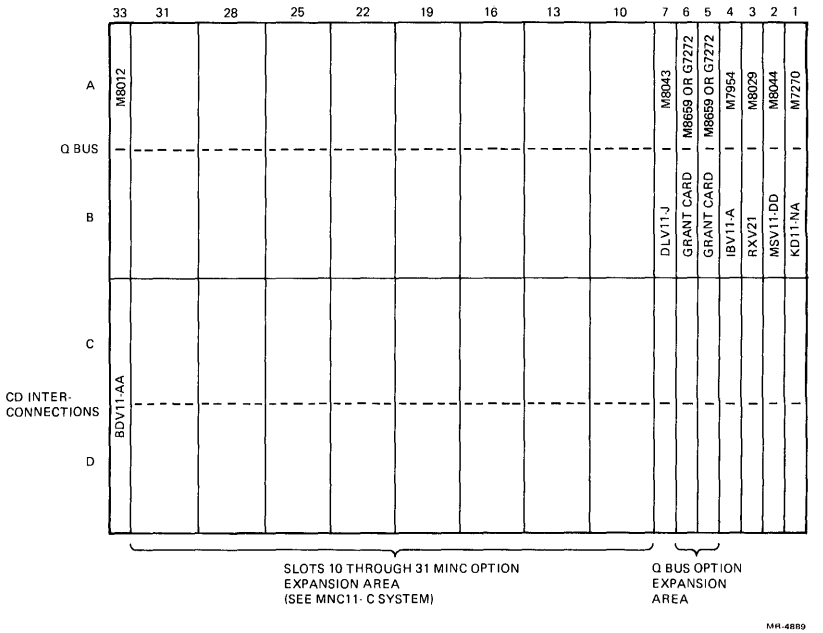
MINC System Model Designation

System Requirements	MNC11 -AA	-BA	-BC	-BD	-CA	-CC	-CD
Input Power (V)	115	115	115	230	115	115	115
Frequency (Hz)	60	60	50	50	60	60	50
		1	1		1	1	
MNC11-		AA	AA		AA/BA	AA/AC	BID
Chassis MNC BA	1	-	-	-	-	-	-
KD11-NA (M7270)	1						
MSV11D (M8044)	1						
RXV21 (M8029)	1						
IBV11-A (M7954)	1						
BDV11-A (M8012)	1				1	1	1
MINC Cart	-	1	1	1	1	1	1
RX02		MA	MC	MD	MA	MC	MC
VT105		MA	MA	MB	MA	MA	MB
LA35					HE	HH	HS
					1	1	
MNC11-AB				1			
MNCAD		*	*	*	1	1	1
MNCAA		*	*	*	1	1	1
MNCAM		*	*	*	1	1	1
MNCDI		*	*	*	1	1	1
MNCDO		*	*	*	1	1	1
MNCKW		*	*	*	1	1	1
MNCAG		*	*	*	1	1	1
Cable Console Interface	1				1	1	1
Software Kit (English)		1	1	1			
Blank Control Panel (MNCBL)		**	**	**	**	**	**

*User's options
**As required to fill MNCBA plus one extra



MINC System Cable Connections



PDP-11/03 Module Utilization (MINC)

DECLAB/MINC Specifications

	115 V, 50/60 Hz				230 V, 50 Hz			
	Plug		Receptacle		Plug		Receptacle	
Power Connector	NEMA No. 5-15P DEC No. 90-089 38		5-15R 12-05351		NEMA No. 6-15P DEC No. 90-08853		6-15R 12-11204	
	MINC Chassis*	RX02	VT105	LA35	MINC Chassis	RX02	VT105	LA35
Amperage								
Typical		3.75	3.0				1.5	
Maximum	19			2.0	8	1.75		1.0
Wattage								
Typical	500		300	160			250	160
Maximum	1200	460	250	300		460	300	
Btu/Hour								
Typical		225		550		225		550
Maximum				1020				1020
Weight								
Kilograms		34.02	16.3	46.3		34.02	16.3	46.3
Pounds		75	36	102		75	36	102

*Includes MNCBA chassis with MINC lab modules and RX02 and VT105.

NOTE

MINC option expansion area is to be used only for MINC lab module add-ons. No Qbus add-ons should be inserted in this expansion area. No backplane expansion of the MINC system is possible. All Qbus add-ons must be inserted in either slot 5 or 6 (A and B only for double-height options).

System-Level Diagnostics

Two diagnostic chains are contained on the diagnostic floppy for system troubleshooting. The diagnostic chain MINC11.CCC provides the required diagnostics for testing the CPU and related modules including the BDV11, the VT105 option, and MINC lab modules. This chain requires turnaround connectors on SLU 0, SLU 1, SLU 2. For detailed operational information, refer to Book 7, *Working with MINC Devices*, AA-D572A-TC. The contents of file MINC11.CCC is as follows.

R VMNF??/1	MINC-AA option sizer program
R VKAA??/1	CPU test
R VKAB??/1	Extended instruction test
R VKAC??/1	Floating point instruction set test
R VKAL??/1	Traps test
R VIBB??/1	IBV11 test
R VDLA??/1	DLV11-J test
R VMNC??/1	Clock test
R VMNB??/1	MNCDI test
R VMNE??/1	MNCOO (digital out) diagnostic
R VMND??/1	D/A test
R VMNA??/1	A/D test
R ZVTN??/1	VT105 test
R VMNG??/1	Termination program

The second diagnostic chain MNC11.CCC provides the required diagnostics for performing a quick check of the MINC lab modules only. The contents of file MNC11.CC are listed below.

R VMNF??/1	Startup/sizer program
R VMNC??/1	Floating point instruction set test
R VMNB??/1	MNCDI test
R VMNE??/1	MNCDO test
R VMND??/1	D/A test
R VMNA??/1	A/D test
R VMNG??/1	Termination program

Both programs are stored on the MINC diagnostic disk, available from the Software Distribution Center (SDC).

Kit No. ZJ281 - RZ (hard-copy documents)
ZJ281 - PX (RX02 floppy)
ZJ281 - RX (hard-copy/RX02 floppy kit)

11/03-BASED MINC

Modules in the Basic System

MNC11-AA (115 V, 60 Hz) and MNC11-AB (230 V, 50 Hz)

Processor KD11-NA (M7270)

With Extended Instruction Set/Floating Point Instruction Set (KEV11-A, 23-003B5)

Jumper W1 installed - crystal clock
Jumper W3 removed - enable event line
Jumper W6 installed - } power-up to 173000 (BDV11)
Jumper W5 removed - }

Memory - MSV11-DD (M8044)

64K byte MOS RAM without parity
On-board memory refresh
Jumper configuration

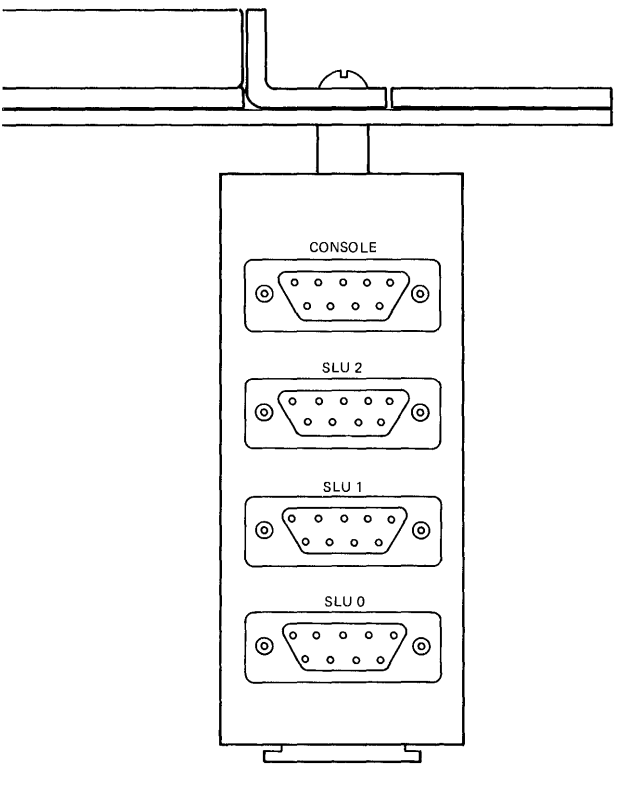
Jumper	Jumper State	Function Implemented
Pin 1 to 3 Pin 1 to 2	OUT IN	Enable 2K I/O page option
W2	IN	Enable normal system power (+5 V)
W3	IN	Enable normal system power (+12 V)
W4	OUT	Disable battery power (+12 V)
W5	OUT	Disable battery power (+5 V)
Pin 10 to 14 Pin 16 to 15	IN IN	Select memory size of 64K bytes
S1 through S5	ON	Starting address bank 0

Serial Line Interface – DLV11-J (M8043)

Number of serial lines: 4

Factory-set address and vector switches

Device	Address	Vector	Baud Rate
Console	777560	60	9600
SLU 2	776520	320	300
SLU 1	776510	310	1200
SLU 0	776500	300	9600



MINC Terminal Distribution Panel

Bus Terminator/Diagnostic/Bootstrap BDV11-A (M8012)

Diagnostic/bootstrap conditions are factory-selected using switch packs.

Switch A (E15)	RX02 Bootstrap
A1	ON
A2	ON
A3	OFF
A4	OFF
A5	OFF
A6	ON
A7	OFF
A8	OFF

Switch B (E21)	RX02 Bootstrap
B1	OFF
B2	OFF
B3	OFF
B4	OFF
B5	ON

IEEE Bus Interface – IBV11-A (M7954)

Address and vector switch settings:

Address 171420	Vector 420
S2-1, 4 and 5 = ON only	S-1 and 5 = ON only

Floppy Disk Interface – RXV21 (M8029)

Address and vector switch settings:

Address 177170	Vector 264
A7 and A8 = OUT only	V3, V6 and V7 = OUT only

DECLAB-11/MNC SYSTEM

The DECLAB-11/MNC is a real time operating system featuring on-line data storage, and FORTRAN software with graphics, scientific, and laboratory subroutine packages. Each system contains as its main components an MNC chassis, dual RL01 disk drives, and a terminal (VT105 or LA36). The MNC chassis houses a power supply, CPU, and related modules, and up to eight MNC- series options.

The physical components of the DECLAB system are grouped into two categories: items common to all MNC systems, and those that can be purchased as options, either when the system is first acquired or at some later time. Each DECLAB system is configured to boot on power-up and halt on BREAK. The figures and tables that follow describe the modules, specifications, and components.

All DECLAB systems include the following standard items.

Mass storage device containing two RL01 disk drives

MNC chassis (MNCBA) with power supply (H786). This contains:

KD11-NA	-	LSI-11 processor with EIS/FIS
MSV11-DD	-	Memory (32K word) single board
RLV11	-	Controller (disk)
DLV11-J	-	Four-channel serial ASCII interface
IBV11-A	-	IEEE bus interface (optional)
BDV11-A	-	Bus terminator/diagnostic/bootstrap module.

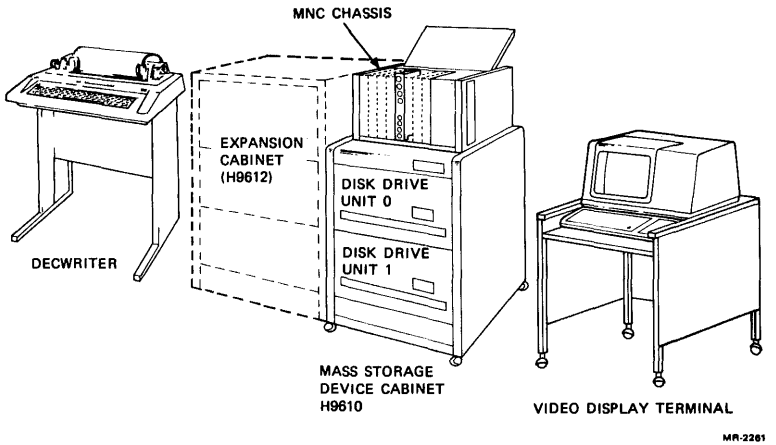
VT105 terminal with built-in graphics capability

DECLAB systems can include some or all of the following lab modules.

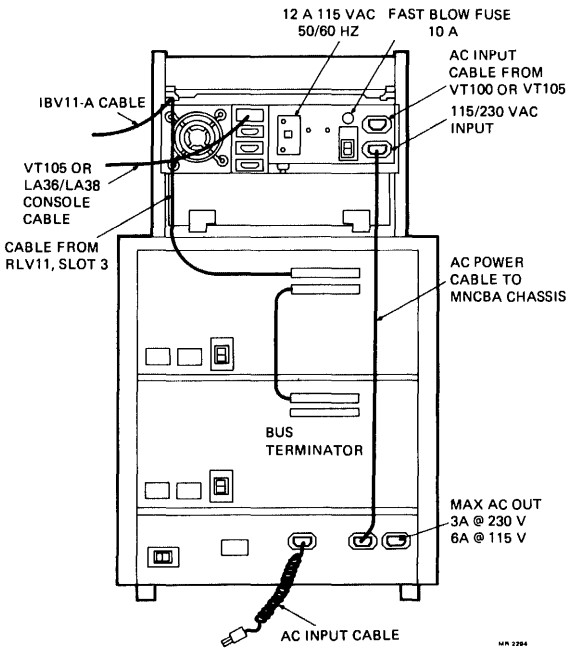
Analog-to-digital converter (MNCAD)
Preamplifier (MNCAG)
Dual multiplexer (MNCAM)
Clock (MNCKW)
Digital-to-analog converter (MNCAA)
Digital input unit (MNCDI)
Digital output unit (MNCDO)

DECLAB systems can also include:

Dot matrix printer (LAV11 + LA180 or LA35)
110 baud, 20 mA serial line interface (DLV11-KC).



DECLAB-11/MNC System with Optional Units



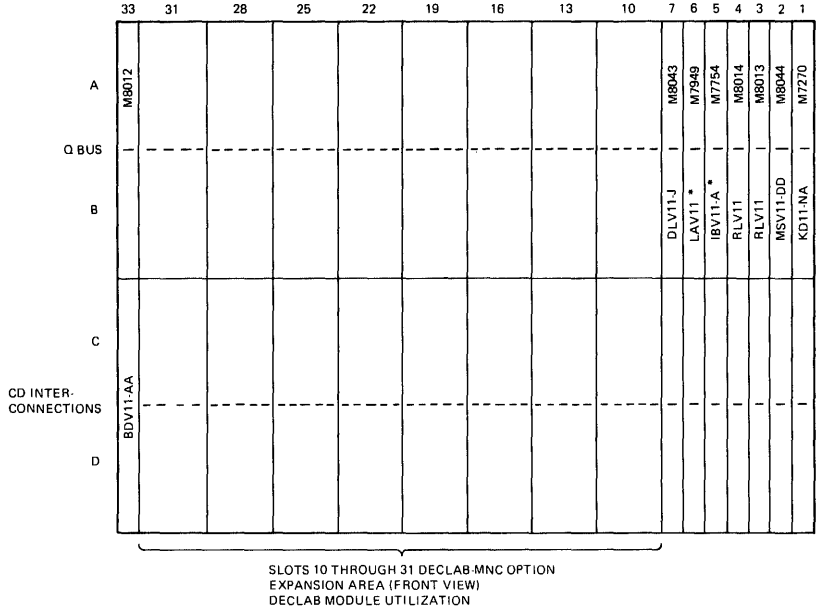
DECLAB-11/MNC Cable Connections

DECLAB-11/MNC System Model Designation

System Requirements	MNC11 -D	-J	-K	-L
Input Power (V)	115	115	115	115
Frequency (Hz)	60	60	60	60
Cabinet/Power Controller (H9610)		BB/BC	BB/BC	
MNC11-		D	D	K
Chassis (MNCBA)	1			
KD11-NA (M7270)	1			
MSV11D (M8044)	1			
DLV11-J (M8043)	1			
IBV11-A (M7954)				1
BDV11-A (M8012)	1			
RLV11- (M8013)	1			
RLV11- (M8014)	1			
LAV11-LA180 Printer				1
VT105 Terminal			MA	
LA36		HE		
RL01 Disk Drive		2	2	
MNC11-AD		*	*	1
MNC11-AA		*	*	1
MNC11-AM		*	*	1
MNC11-DI		*	*	1
MNC11-DO		*	*	1
MNC11-KW		*	*	1
MNC11-AG		*	*	1
Cable Console Interface	1			
Software Kit (English)	1	1	1	1
Blank Control Panel (BNCBL)		**	**	**
Installation Kit (MNCIK)				

*User's options
**As required to fill MNCBA plus one extra

DECLAB-11/MNC



* REPLACE THESE OPTIONS WHEN NOT REQUIRED WITH M8659 GRANT CARD OR G7272

MR-4890

PDP-11/03 DECLAB Module Utilization

NOTE

DECLAB-MNC option expansion area is to be used only for MNC-series module add-ons. No Qbus add-ons should be installed in this expansion area. No backplane expansion of the MNC system is possible.

System-Level Diagnostics

Two diagnostic chain files are contained on the RL01 diagnostic disk for system troubleshooting. The diagnostic chain MNC11A.CCC provides the required diagnostics for testing the CPU and related modules and MNC-series modules. This program does not test the BDV11 or VT105 options. The contents of file MNC11A.CCC are as follows.

R VMNF??/1	MINC-11 option sizer program
R VKAA??/1	CPU test
R VKAB??/1	Extended instruction test
R VKAC??/1	Floating point instruction set test
R VKAL??/1	Traps test

R VIBB??/1	IBV11 test
R VDLA??/1	DLV11-J test
R VMNC??/1	Clock test
R VMNB??/1	MNCDI test
R VMNE??/1	MNCOO (digital out) diagnostic
R VMND??/1	
R VMNA??/1	A/D test
R ZVTN??/1	VT105 test
R VMNG??/1	Terminator program

The second diagnostic chain MNC11.CCC provides the required diagnostics for performing a quick check of the MNC-series modules only. The contents of file MNC11.CCC are as follows.

R VMNF??/1	Start-up/sizer program
R VMNC??/1	Floating point instruction set test
R VMNB??/1	MNCDI test
R VMNE??/1	MNCDO test
R VMND??/1	D/A test
R VMNA??/1	A/D test
R VMNG??/1	Termination program

Both programs are stored on the MNC diagnostic disk, Software Distribution Center (SDC) kit no. AX-E380EMC.

Modules in the Basic System

MNC11-AA (115 V, 60 Hz) and MNC11-AB (230 V, 50 Hz)

Processor KD11-NA (M7270)

With Extended Instruction Set/Floating Point Instruction Set (KEV11-A 23-003B5).

Jumper W1 installed - crystal clock
Jumper W3 removed - enable event line
Jumper W6 installed - } power-up to 173000
Jumper W5 removed - }

Memory - MSV11-DD (M8044)

64K byte MOS RAM without parity
On-board memory refresh
Jumper configuration

Jumper	Jumper State	Function Implemented
Pin 1 to 3 Pin 1 to 2	OUT IN	Enable 2K I/O page option
W2	IN	Enable normal system power (+5 V)
W3	IN	Enable normal system power (+12 V)
W4	OUT	Disable battery power (+12 V)
W5	OUT	Disable battery power (+5 V)
Pin 10 to 14 Pin 16 to 15	IN IN	Select memory size of 64K bytes
S1 through S5	ON	Starting address = bank 0

Serial Line Interface – DLV11-J (M8043)

Number of serial lines: 4

Factory-set address and vector switches

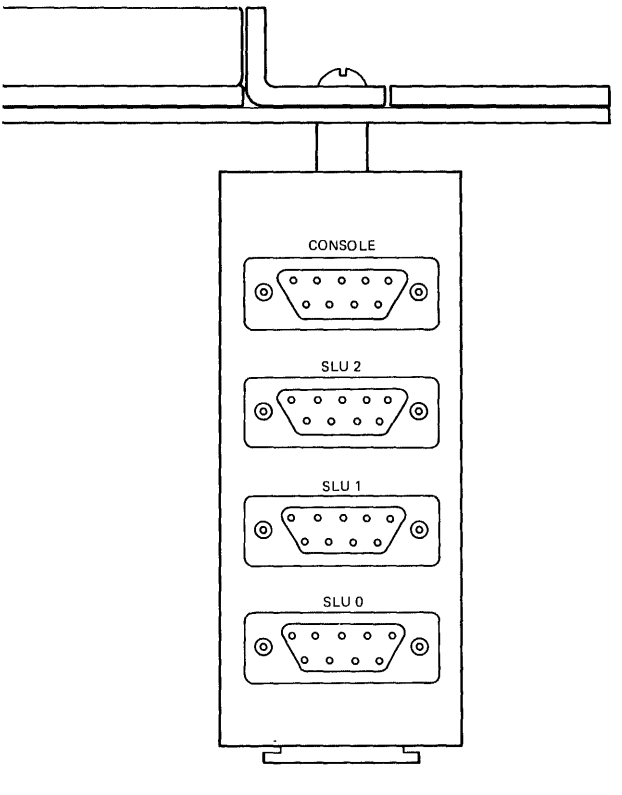
Device	Address	Vector	Baud Rate
Console	777560	60	9600/300*
SLU 2	776520	320	300
SLU 1	776510	310	1200
SLU 0	776500	300	9600

*Varies depending on type of terminal.

DECLAB System Specifications

	115 V, 50/60 Hz				230 V, 50 Hz			
	Plug		Receptacle		Plug		Receptacle	
Power Connector	NEMA No. 5-15P DEC No. 90-089 38		5-15R 12-05351		NEMA No. 6-15P DEC No. 90-08853		6-15R 12-11204	
	DECLAB/ MINC System*	RL01	VT105	LA36	DECLAB/ MNC System	RL01	VT105	LA36
Amperage								
Typical			3.0					
Maximum	19	3.5		2.0	19	2.5	1.5	1.0
Wattage								
Typical	500	150		160	500	150		160
Maximum	1200	200	150	300	1200	200	150	300
Btu/Hour								
Typical				550		600		550
Maximum		600		1020				1020
Weight								
Kilograms	134	34.02	16.3	46.3	134	34.02	16.3	46.3
Pounds	295	75	36	102	295	75	36	102

*Includes MNCBA chassis with MNC-series module and two RL01 drives.



MINC Terminal Distribution Panel

Bus Terminator/Diagnostic/Bootstrap BDV11-A (M8012)

Switch A (E15)	RL01 Bootstrap
A1	ON
A2	ON
A3	OFF
A4	OFF
A5	OFF
A6	OFF
A7	ON
A8	OFF

Switch B (E22)	RL01 Bootstrap
B1	OFF
B2	OFF
B3	OFF
B4	OFF
B5	ON

IEEE Bus Interface – IBV11-A (M7954) (Optional)

Address and vector switch settings:

Address 171420 Vector 420
S2-1, 4 and 5 = ON only S1-1 and 5 = ON only

Disk Interface – RLV11 (M8014, M8013)

Address and vector switch settings on M8014 bus module:

Address 174400 Vector 160

M8014 Switch Setting

Switch	Position	Function
Bus Address (174400)	ON	A12 (MSB)
	ON	A11
	OFF	A10
	OFF	A09
	ON	A08
	OFF	A07
	OFF	A06
	OFF	A05
	OFF	A04
	OFF	A03 (LSB)
Vector Switch (160)	OFF	V8 (MSB)
	OFF	V7
	ON	V6
	ON	V5
	ON	V4
	OFF	V3
	OFF	V2 (LSB)

NOTE

Additional MINC/DECLAB information can be found in the following manuals.

MINC/DECLAB Service Manual **EK-MNC11-SV**
DECLAB-11/MNC User's Guide **EK-MNC11-UG**

PDP-11/23-BASED MINC/DECLAB-11/MINC SYSTEMS

MINC

The **M**odular **IN**strumentation **C**omputer (MINC) is a real time operating system featuring on-line data storage, and BASIC software with graphics, scientific, and laboratory subroutine packages. Each system consists of a MINC chassis, an RX02 dual floppy disk drive, and a VT105 terminal mounted on a roll-around cart. The MINC chassis houses a power supply, CPU and related modules, and up to eight MINC laboratory options.

The physical components of a MINC system are grouped into two categories: items common to all MINC systems, and those that can be purchased as options, either when the system is first acquired or at some later time as add-ons. Each MINC system is configured to boot on power-up and halt on BREAK. The figures and tables that follow describe the modules, specifications, and components.

All PDP-11/23 MINC systems include the following standard items.

MINC cart, which provides support and transport for:

Dual diskette drive (RX02M)

MINC chassis (MNCBA) with power supply (H786). This contains:

KDF11-AB	-	LSI-11 processor with memory management EIS/FIS
MSV11-DD	-	Memory (64K words) on two modules
RXV21	-	Diskette drive interface
DLV11-J	-	Four-channel serial ASCII interface
IBV11-A	-	IEEE bus interface
BDV11-A	-	Bus terminator/diagnostic/bootstrap module.

VT105 terminal with built-in graphics capability.

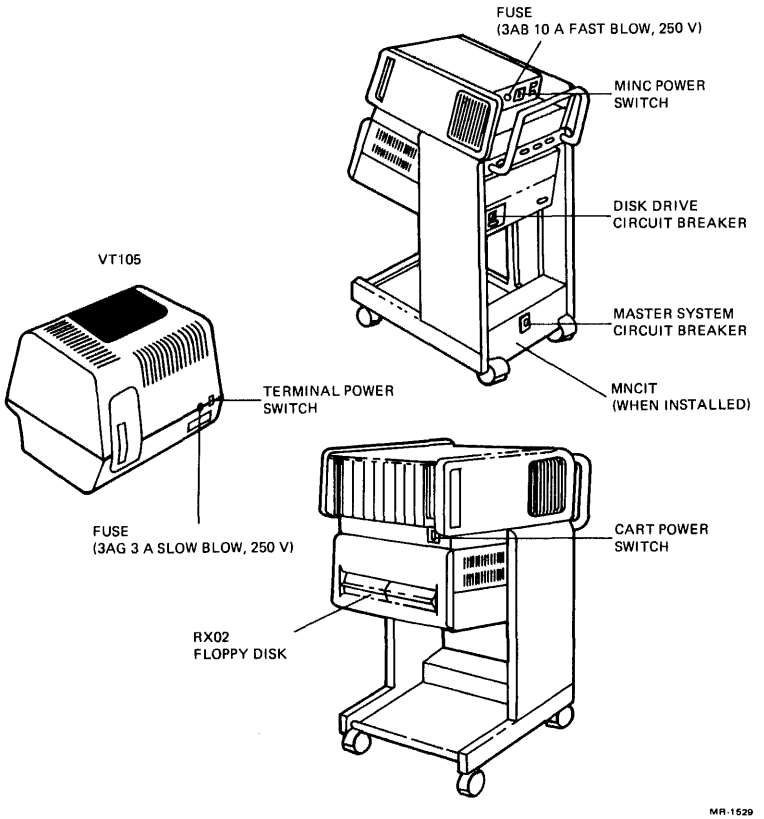
MINC systems can include some or all of the following lab modules.

Analog-to-digital converter (MNCAD)
Preamplifier (MNCAG)
Dual multiplexer (MNCAM)
Clock (MNCKW)
Digital-to-analog converter (MNCAA)
Digital input unit (MNCDI)
Digital output unit (MNCDO)

11/23-BASED MINC

MINC systems can also include:

Dot matrix printer (LA35)
Isolation transformer (MNCIT)
110 baud, 20 mA serial line interface (DLV11-KC).



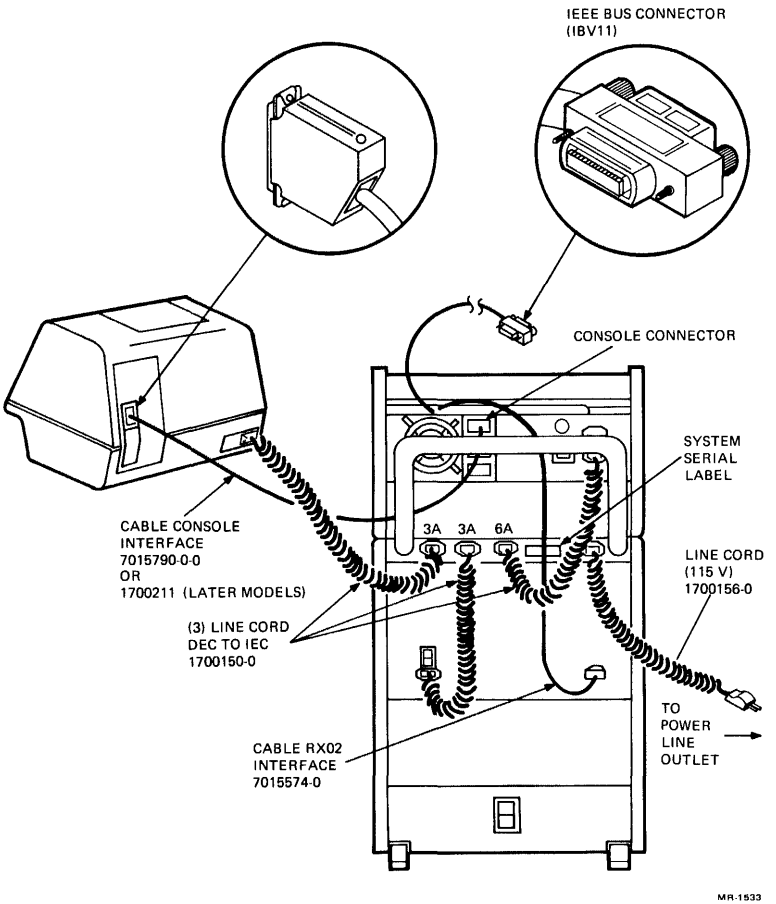
MINC System

MINC System Model Designation

System Requirements	MNCFA -AA	-BA	-BC	-BD	-CA	-CC	-CD
Input Power (V)	115	115	115	230	115	115	115
Frequency (Hz)	60	60	50	50	60	60	50
		1	1		1	1	
MNCFA-		AA	AA		AA/BA	AA/AC	BD
Chassis MNC BA	1	-	-	-	-	-	-
KDF11-AB (M8186)	1						
MSV11D (M8044)	2						
RXV21 (M8029-	1						
IBV11-A (M7954)	1						
BDV11-A (M8012)	1				1	1	1
MINC Cart	-	1	1	1	1	1	1
RX02		MA	MC	MD	MA	MC	MC
VT105		MA	MA	MB	MA	MA	MB
LA35					HE	HH	HS
					1	1	
MNCFA-AB				1			
MNCAD		*	*	*	1	1	1
MNCAA		*	*	*	1	1	1
MNCAM		*	*	*	1	1	1
MNCDI		*	*	*	1	1	1
MNCDO		*	*	*	1	1	1
MNCKW		*	*	*	1	1	1
MNCAG		*	*	*	1	1	1
Cable Console Interface	1				1	1	1
Software Kit (English)		1	1	1			
Blank Control Panel (MNCBL)		**	**	**	**	**	**

*User's options
**As required to fill MNCBA plus one extra

QJV35-AX (RX02) diagnostic package supplied



MINC System Cable Connections

*NOTE: MUST BE AT CS REVISION 'E' OR HIGHER.

**NOTE: MUST BE AT CS REVISION 'E1' OR HIGHER.

MR-4892

PDP-11V23 MINC Module Configuration

MINC System Specifications

	115 V, 50/60 Hz				230 V, 50 Hz			
	Plug		Receptacle		Plug		Receptacle	
Power Connector	NEMA No. 5-15P DEC No. 90-089 38		5-15R 12-05351		NEMA No. 6-15P DEC No. 90-08853		6-15R 12-11204	
	MINC Chassis*	RX02	VT105	LA35	MINC Chassis	RX02	VT105	LA35
Amperage								
Typical			3.0				1.5	
Maximum	19	4.0		2.0	8	2.0		1.0
Wattage								
Typical	500	460	250	160		460	250	160
Maximum	1200		300	300			300	
Btu/Hour								
Typical		225		550		225		550
Maximum				1020				1020
Weight								
Kilograms			16.3	46.3			16.3	46.3
Pounds			36	102			36	102

*Includes MNCBA chassis with MINC lab modules and RX02 and VT105.

NOTE

MINC option expansion area is to be used only for MINC lab module add-ons. No Qbus add-ons should be inserted in this expansion area. No backplane expansion of the MINC system is possible. All Qbus add-ons must be inserted in either slot 5 or 6 (A and B only for double-height options).

System-Level Diagnostics

Two diagnostic chain files are contained on the diagnostic floppy for system troubleshooting. The diagnostic chain MNC11F.CCC provides the required diagnostics for testing the CPU and related modules including the BDV11, the VT105 option, and MINC lab modules. This chain requires turnaround connectors on SLUs 0, 1, and 2. For detailed operational information, refer to Book 7 of *Working with MINC Devices*, AA-D572A-TC. The contents of file MNC11F.CCC are as follows.

R VMNF??/1	MINC-11 option sizer program
R JKDA??/1	CPU test
R JKDB??/1	Extended instruction test
R JKDC??/1	Floating point instruction set test
R JKDD??/1	Traps test
R VIBB??/1	IBV11 test
R VDLA??/1	DLV11-J test
R VMNC??/1	Clock test
R VMNB??/1	MNCDI test
R VMNE??/1	MNCOO (digital out) diagnostic
R VMND??/1	D/A test
R VMNA??/1	A/D test
R ZVTN??/1	VT105 test
R VMNG??/1	Termination program

The second diagnostic chain MNCFA.CCC provides the required diagnostics for performing a quick check of the MINC lab modules only. The contents of file MNCFA.CC are listed below.

R VMNF??/1	Start-up/sizer program
R VMNC??/1	Floating point instruction set test
R VMNB??/1	MNCDI test
R VMNE??/1	MNCDO test
R VMND??/1	D/A test
R VMNA??/1	A/D test
R VMNG??/1	Termination program

Both programs are stored on the MINC diagnostic disk, available from the Software Distribution Center (SDC).

Kit No. QJV35 - RZ (hard-copy documents)
QJV35 - AX (RX02 floppy)
ZJ281 - RX (hard-copy/RX02 floppy kit)

11/23-BASED MINC

Modules in the Basic System

MNC11F-AA (115 V, 60 Hz) and MNC11F-AB (230 V, 50 Hz)

Processor (KDF11-AB) M8186

With warm floating point instruction set (KEF11-A) and memory management.

Jumper W1 installed - crystal clock
Jumper W4 removed - enable event line
Jumper W5 removed - } power-up to 773000 (BDV11)
Jumper W6 installed - }
Jumper W7 removed - enter console ODT on HALT
Jumper W8 installed - power-up with PC at 173000_8 (bootstrap)

Memory - MSV11-DD (M8044-D)

64K bytes MOS RAM without parity
On-board memory refresh
Jumper configuration

Jumper	Jumper State	Function Implemented
Pin 1 to 3 Pin 1 to 2	IN OUT	Disable memory I/O page options
W2	IN	Enable normal system power (+5 V)
W3	IN	Enable normal system power (+12 V)
W4	OUT	Disable battery power (+12 V)
W5	OUT	Disable battery power (+5 V)
Pin 10 to 14 Pin 16 to 15	IN IN	Select memory size of 64K bytes

MSV11-DD Switch Settings

Switch	Position 1st Module Bank 0–7	Position 2nd Module Bank 10–17	Position 3rd Module Bank 20–27	Position 4th Module Bank 30–37
S-1	ON	ON	OFF	OFF
S-2	ON	OFF	ON	OFF
S-3	ON	ON	ON	ON
S-4	ON	ON	ON	ON
S-5	ON	ON	ON	ON

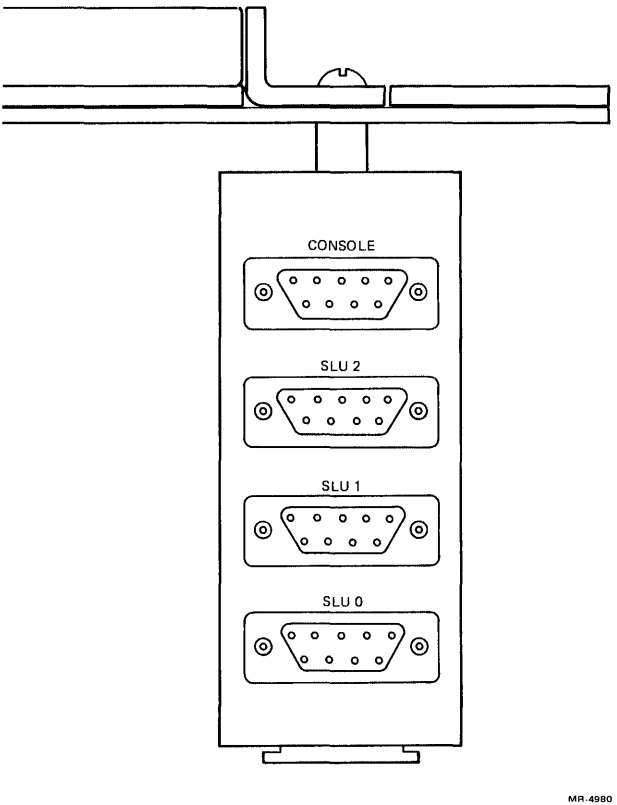
Serial Line Interface - DLV11-J (M8043)

Must be at CS revision "E" or higher.

Number of serial lines: 4

Factory-set address and vector switches

Device	Address	Vector	Baud Rate
Console	777560	60	9600
SLU 2	776520	320	300
SLU 1	776510	310	1200
SLU 0	776500	300	9600



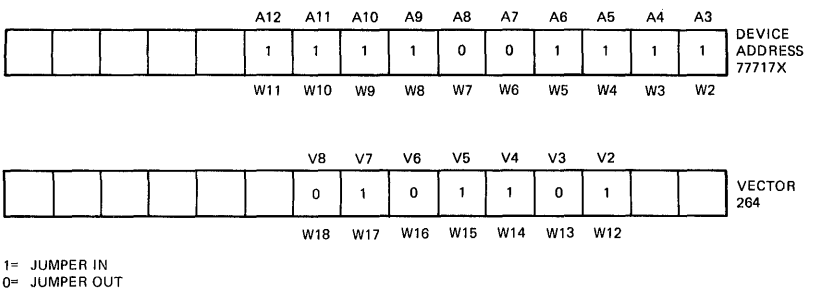
MINC Terminal Distribution Panel

Bus Terminator/Diagnostic/Bootstrap BDV11-A (M8012)
Diagnostic/bootstrap conditions are factory-selected using switch packs.

Switch A (E15)	RX02 Bootstrap
A1	ON
A2	ON
A3	OFF
A4	OFF
A5	OFF
A6	ON
A7	OFF
A8	OFF

Switch B (E21)	RX02 Bootstrap
B1	OFF
B2	OFF
B3	OFF
B4	OFF
B5	ON

Floppy Disk Interface – RXV21 (M8029)



RXV21 Address and Switch Settings

DECLAB-11/MNC 11/23

DECLAB-11/MNC PDP-11/23-BASED SYSTEM

The DECLAB-11/MNC is a real time operating system featuring on-line data storage, and FORTRAN software with graphics, scientific, and laboratory subroutine packages. Each system contains as its main components, an MNC chassis, dual RL01 disk drives, and a terminal (VT105 or LA36). The MNC chassis houses a power supply, CPU, and related modules, and up to eight MNC- series option.

The physical components of the DECLAB system are grouped into two categories: items common to all MNC systems, and those that can be purchased as options, either when the system is first acquired or at some later time as add-ons. Each DECLAB system is configured to boot on power-up and halt on BREAK. The figures and tables that follow describe the modules, specifications, and components.

All DECLAB systems include the following standard items.

Mass storage device containing two RL01 disk drives

MNC chassis (MNCBA) with power supply (H786). This contains:

KDF11-AB	-	LSI-11 processor with memory management, floating point (KEF11-A)
MSV11-DD	-	Memory (128K byte: two modules)
RLV11	-	Controller (disk)
DLV11-J	-	Four-channel serial ASCII interface
IBV11-A	-	IEEE bus interface (optional)
BDV11-A	-	Bus terminator/diagnostic/bootstrap module.

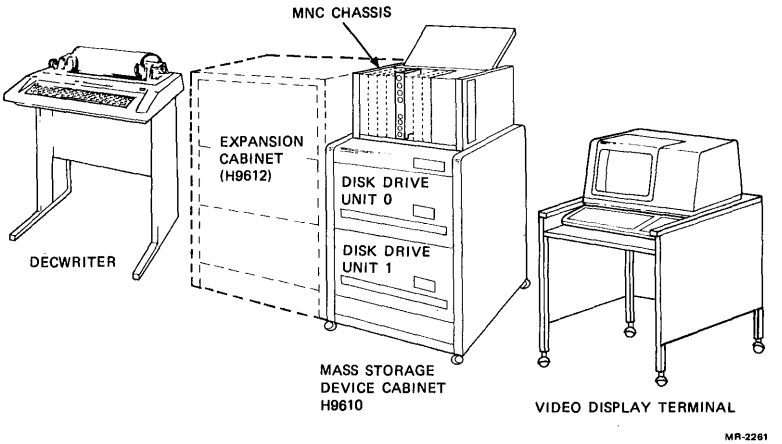
VT105 terminal with built-in graphics capability

DECLAB systems can include some or all of the following lab modules.

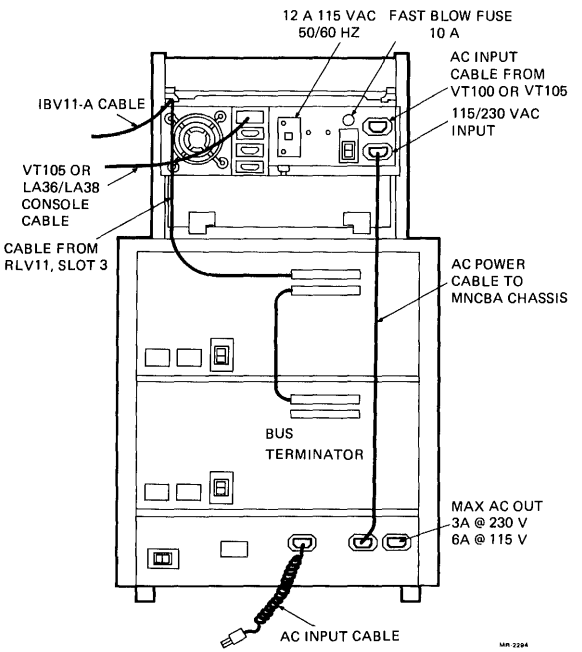
Analog-to-digital converter (MNCAD)
Preamplifier (MNCAG)
Dual multiplexer (MNCAM)
Clock (MNCKW)
Digital-to-analog converter (MNCAA)
Digital input unit (MNCDI)
Digital output unit (MNCDO)

DECLAB systems can also include:

Dot matrix printer (LAV11 + LA180 or LA35)
110 baud, 20 mA serial line interface (DLV11-KC).



DECLAB-11/MNC System with Optional Units

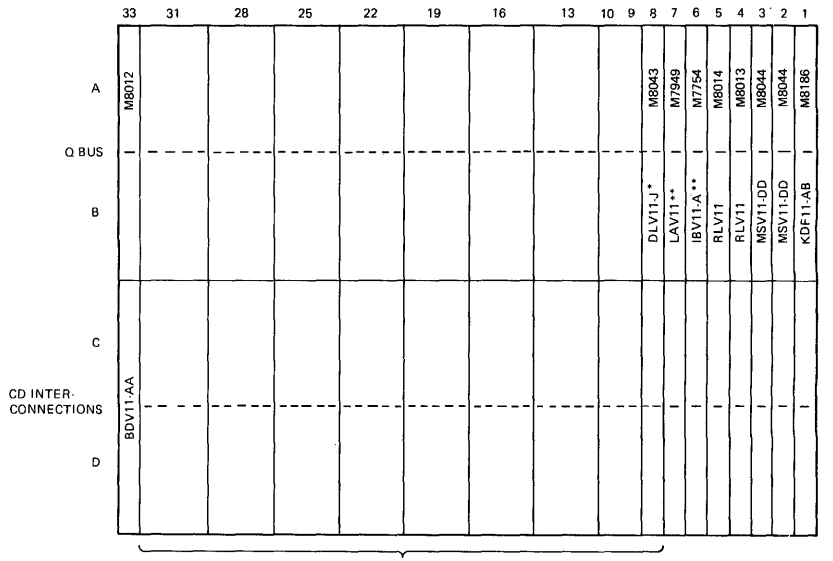


DECLAB-11/MNC Cable Connections

DECLAB-11/MNC System Model Designation

System Requirements	MNCFA -J	-K
Input Power (V)	115	115
Frequency (Hz)	60	60
Cabinet/Power Controller (H9610)	BB/BC	BB/BC
MNC11-	D	D
Chassis (MNCBA)		
KDF11-AB (M8186)	1	1
MSV11D (M8044)	2	2
DLV11-J (M8043)	1	1
IBV11-A (M7954)		
BDV11-A (M8012)	1	1
RLV11- (M8013)	1	1
RLV11- (M8014)	1	1
LAV11-LA180 Printer		
VT105 Terminal		MA
LA36	HE	
RL01 Disk Drive	2	2
QJV35-AR Diagnostic Package (RL01)	1	1
MNC11-F-AD	*	*
MNC11-F-AA	*	*
MNC11-F-AM	*	*
MNC11-F-DI	*	*
MNC11-F-DO	*	*
MNC11-F-KW	*	*
MNC11-F-AG	*	*
Cable Console Interface		
Software Kit (English)	1	1
Blank Control Panel (BNCBL)	**	**
Installation Kit (MNCIK)		

*User's options
**As required to fill MNCFA



PDP-11/23 DECLAB Module Configuration

NOTE

DECLAB-11/MNC option expansion area is to be used only for MNC-series module add-ons. No Qbus add-ons should be installed in this expansion area. No backplane expansion of the MNC system is possible.

System-Level Diagnostics

Two diagnostic chain files are contained on the RL01 diagnostic disk for system troubleshooting. The diagnostic chain MNC11F.CCC provides the required diagnostics for testing the CPU and related modules and MNC-series modules. This program does not test the BDV11 or VT105 options. This chain requires turnaround connectors on SLUs 0, 1, and 2. For detailed operational information, refer to Book 7 of *Working with MINC Devices*, AA-D572A-TC. The contents of file MNC11F.CCC are as follows.

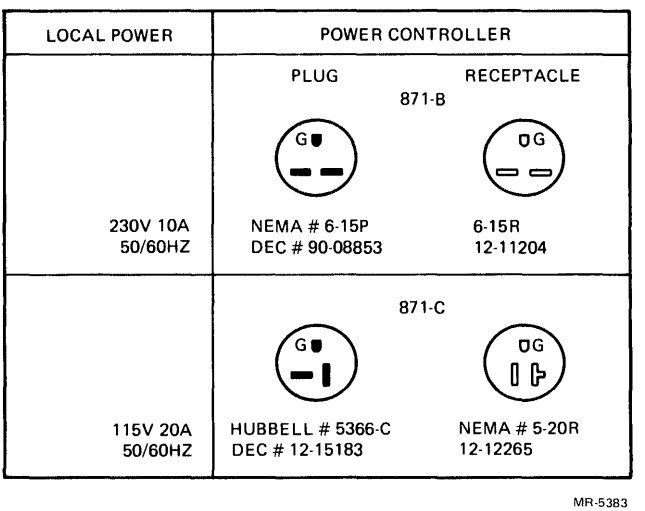
R VMNF??/1	MINC-11 option sizer program
R JKDA??/1	CPU test
R JKDB??/1	Extended instruction set

R JKDC??/1	Floating point instruction set test
R JKDD??/1	Traps test
R VIBB??/1	IBV11 test
R VDLA??/1	DLV11-J test
R VMNC??/1	Clock test
R VMNB??/1	MNCDI test
R VMNE??/1	MNCDO test (digital out)
R VMND??/1	D/A test
R VMNA??/1	A/D test
R ZVTN??/1	VT105 test
R VMNG??/1	Termination program

The second diagnostic chain MNC11F.CCC provides the required diagnostics for performing a quick check of the MNC-series modules only. The contents of file MNC11F.CCC are as follows.

R VMNF??/1	Start-up/sizer program
R VMNC??/1	Floating point instruction set test
R VMNB??/1	MNCDI test
R VMNE??/1	MNCDO test
R VMND??/1	D/A test
R VMNA??/1	A/D test
R VMNG??/1	Termination program

Both programs are stored on the MNC diagnostic disk, Software Distribution Center (SDC) kit no. BA-F018*-MC.



DECLAB/MINC and MINC RL01 Add-On Power Requirements

	115 V, 50/60 Hz				230 V, 50 Hz			
	Plug		Receptacle		Plug		Receptacle	
Power Connector	NEMA No. 5-15P DEC No. 90-089 38		5-15R 12-05351		NEMA No. 6-15P DEC No. 90-08853		6-15R 12-11204	
	DECLAB/ MINC System*	RL01	VT105	LA36	DECLAB/ MNC System	RL01	VT105	LA36
Amperage								
Typical			3.0				1.5	
Maximum	19	3.5		2.0		2.5		1.0
Wattage								
Typical	500	150	250	160		150	250	160
Maximum	1200	200	300	300		200	300	300
Btu/Hour								
Typical		600		550			600	550
Maximum				1020				1020
Weight								
Kilograms	134	34.02	16.3	46.3	134	34.02	16.3	46.3
Pounds	295	75	36	102	295	75	36	102

*Includes MNCBA chassis with MNC-series module and two RL01 drives.

DECLAB-11/MNC 11/23

Modules Included in the Basic PDP-11/23 System

MNC11F-AA (115 V, 60 Hz) and MNC11F-AB (230 V, 50 Hz)

Processor (KDF11-AB) M8186

With warm floating point instruction set (KEF11-A) and memory management.

Jumper W1 installed - crystal clock
Jumper W4 removed - enable event line
Jumper W5 removed - } power-up to 773000 (BDV11)
Jumper W6 installed - }
Jumper W7 removed - enter console ODT on HALT
Jumper W8 installed - power-up with PC at 173000_8 (bootstrap)

Memory - MSV11-DD (M8044)

64K byte MOS RAM (without parity)
On-board memory refresh
Jumper configuration

Jumper	Jumper State	Function Implemented
Pin 1 to 3 Pin 1 to 2	IN OUT	Disable memory I/O page option
W2	IN	Enable normal system power (+5 V)
W3	IN	Enable normal system power (+12 V)
W4	OUT	Disable battery power (+12 V)
W5	OUT	Disable battery power (+5 V)
Pin 10 to 14 Pin 16 to 15	IN IN	Select memory size of 64K bytes

MSV11-DD Switch Settings

Switch	Position 1st Module Bank 0–7	Position 2nd Module Bank 10–17	Position 3rd Module Bank 20–27	Position 4th Module Bank 30–37
S-1	ON	ON	OFF	OFF
S-2	ON	OFF	ON	OFF
S-3	ON	ON	ON	ON
S-4	ON	ON	ON	ON
S-5	ON	ON	ON	ON

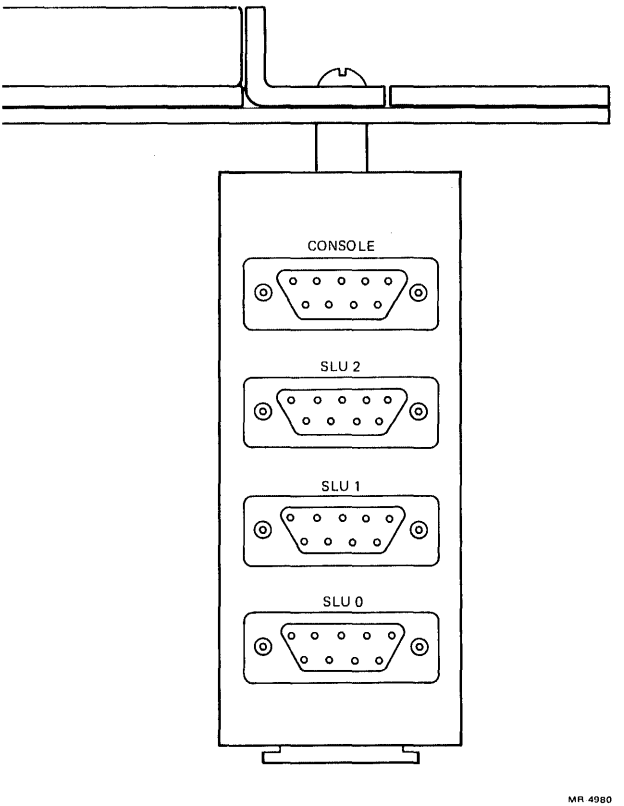
Serial Line Interface - DLV11-J (M8043)

Must be at CS revision "E" or higher.

Number of serial lines: 4

Factory-set address and vector switches

Device	Address	Vector	Baud Rate
Console	777560	60	9600
SLU 2	776520	320	300
SLU 1	776510	310	1200
SLU 0	776500	300	9600



MINC Terminal Distribution Panel

Bus Terminator/Diagnostic/Bootstrap BDV11-A (M8012)

Diagnostic/bootstrap conditions are factory-selected using switch packs.

Switch A (E15)	RL01 Bootstrap
A1	ON
A2	ON
A3	OFF
A4	OFF
A5	OFF
A6	OFF
A7	OFF
A7	ON
A8	OFF

Switch B (E21)	RL01 Bootstrap
B1	OFF
B2	OFF
B3	OFF
B4	OFF
B5	ON

IEEE Bus Interface – IBV11-A (M7954) optional

Address and vector switch settings:

Address 171420
S2-1, 4 and 5 = ON only

Vector 420
S-1 and 5 = ON only

Disk Interface – RLV11 (M8013, M8014)

Address and vector switch settings as shown in the following.

M8014 Switch Settings

Switch	Position	Function
Bus Address (174400)	ON	A12 (MSB)
	ON	A11
	OFF	A10
	OFF	A09
	ON	A08
	OFF	A07
	OFF	A06
	OFF	A05
	OFF	A04
	OFF	A03 (LSB)
Vector Switch (160)	OFF	V8 (MSB)
	OFF	V7
	ON	V6
	ON	V5
	ON	V4
	OFF	V3
	OFF	V2 (LSB)

CPU/OPTIONS

GENERAL MODULE INFORMATION

GENERAL MODULE INFORMATION

This section lists LSI-11 modules alphanumerically by module number. The tables below list modules by option designation for cross-referencing. All modules are (or will be) covered in *Microcomputer Processor Handbook*, EB-20175-20, (CPUs and memories) or the *Minicomputer Interfaces Handbook*, EB-18451-20.

The following conventions are used in presenting module data.

Registers

The base address is listed first. This is normally the address of a control status register. Abbreviations containing "CS" or "CSR" are for control status registers. Abbreviations containing "DB," "DBR," or "BUF" refer to data buffer registers.

Switches

Switches are labeled "S1, S2, S3, ... " although they may be located in the same DIP switch pack. Rocker switch states are selected by pressing the side closest to the label of the state desired. For example, to select the ON position, press the side of the rocker closest to the edge of the switch on which "ON" is printed; disregard the red line on the end of the rocker.

Jumpers

"I" indicates that a jumper is inserted. "R" indicates that it is removed. "X" indicates a "don't care" condition. Location drawings show jumpers installed, for clarity, although they may not actually be installed for the standard configuration. Tables define the jumper states. Jumpers are shown as a solid line if they are normally installed.

NOTE

Jumpers are not always installed for a 1 and removed for a 0; on some modules the reverse is true. See Appendix A for XXDP+ diagnostic names, functions, and multimedia assignments.

A012
ADV11-A ANALOG-TO-DIGITAL CONVERTER

Amps		Bus Loads		Cables
+5	+12	AC	DC	
2.0	0.45	3.25	1	BC04Z BC04R BCV11 BC08R used with H322

Standard Addresses

CSR	170400
DBR	170402

Vectors

A/D Done	400
Error	404

Diagnostic Programs

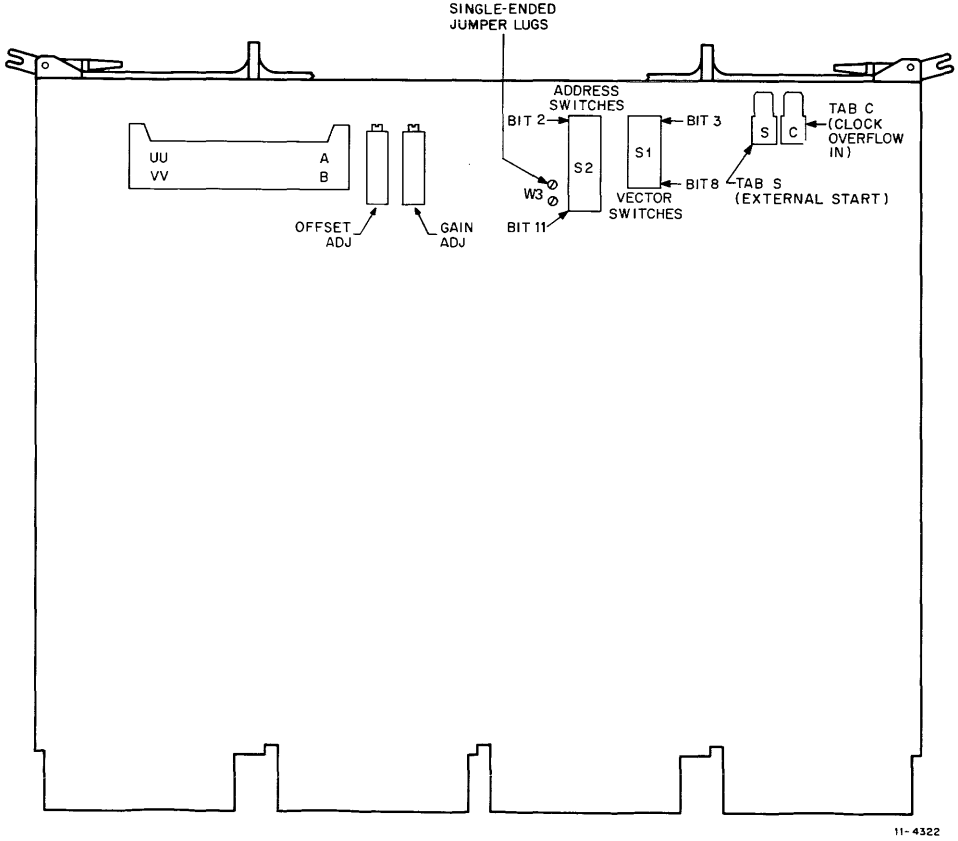
Refer to Appendix A.

NOTE

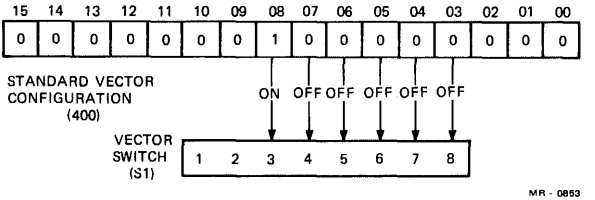
CVADA?? and CXADC?? tests require wraparound connector PN 70-12894.

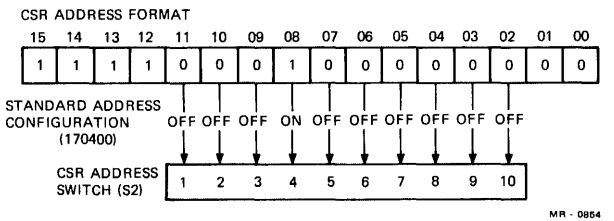
Related Documentation

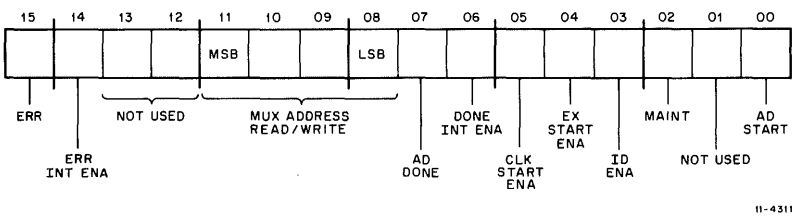
ADV11-A, KWV11-A AAV11-A, DRV11 User's Manual (EK-ADV11-OP)
Field Maintenance Print Set (MP00193)
Microcomputer Interfaces Handbook (EB-20175-20)


SINGLE-ENDED
JUMPER LUGS
ADDRESS
SWITCHES
BIT 2
BIT 3
S2
S1
W3
BIT 11
BIT 8
VECTOR
SWITCHES
TAB C
(CLOCK
OVERFLOW
IN)
S
C
TAB S
(EXTERNAL START)
UU
VV
A
B
OFFSET
ADJ
GAIN
ADJ
11-4322

Jumper W3 is inserted for single-ended operation, and removed for quasi-differential operation.







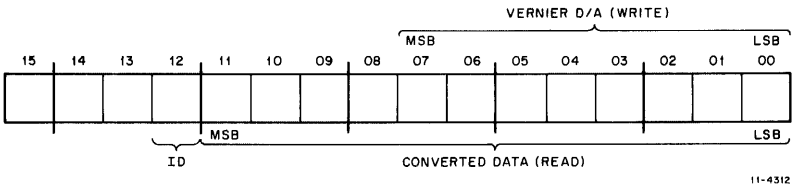
ADV11-A Control/Status Register (CSR)

CSR Bit Definition

Bit	Function
15	A/D Error (read/write) - The A/D Error may be program set or cleared and is cleared by the processor initialize. It is set by any of the following: a. attempting an external or clock start during the transition interval b. attempting any start during a conversion in progress c. failing to read the result of a previous conversion before the end of the current conversion.
14	Error Interrupt Enable (read/write) - When set, enables a program interrupt upon an error condition (A/D Error). Interrupt is generated whenever bits 14 and 15 are set, regardless of which was set first.
13-12	Not used.
11-8	Multiplexer Address (read/write) - Contain the number of the current analog input channel being addressed.
07	A/D Done (read) - Set at the completion of a conversion when the data buffer is updated. Cleared when the data buffer is read, and by the processor initialize. If enabled interrupts are requested simultaneously by bits 07 and 15, bit 07 has the higher priority.
06	Done Interrupt Enable (read/write) - When set, enables a program interrupt at the completion of a conversion (A/D Done). Interrupt is generated when bit 07 and bit 06 are both set, regardless of sequence.
05	Clock Start Enable (read/write) - When set, enables conversions to be initiated by an overflow from the clock option.
04	External Start Enable (read/write) - When set, enables conversions to be initiated by an external signal or through a Schmitt trigger from the clock option.
03	ID Enable (read/write) - When set, causes bit 12 of the data buffer register to be loaded to a 1 at the end of any conversion.

CSR Bit Definition (Cont)

Bit	Function
02	Maintenance (read/write) - Loads, when set, all bits of the converted data output equal to multiplexer address LSB (bit 08) at the completion of the next conversion. Cleared by the processor initialize. Used for "all 0s" and "all 1s" tests of A/D conversion logic.
01	Not used.
00	A/D Start (read/write) - Initiates a conversion when set. Cleared at the completion of the conversion and by the processor initialize.



ADV11-A Data Buffer Register (DBR)

DBR Bit Definition

The DBR is actually two separate registers: one read only, the other, write only.

Bit	Function
Read Only	(Cleared at processor initialize.)
15-13	Not used. Should read as 0.
12	ID (read) - When ID Enable (bit 03) of the CSR has been set, BDR bit 12 will be loaded to a 1 at the end of conversion.
11-00	Converted Data (read) - These bits contain the results of the last A/D conversion.
Write Only	(Set to 200 at processor initialize.)
15-08	Not used.
07-00	Vernier D/A (write) - These bits provide a programmed offset to the converted value (scaled 1 D/A LSB = 1/50 A/D LSB). The hardware initializes this value to 200 (mid-range). Values greater than 200 make the input voltage appear more positive.

A6001
AAV11-A DIGITAL-TO-ANALOG CONVERTER

Amps		Bus Loads		Cables
+5	−12	AC	DC	
1.5	0.4	1.91	1	BC04Z
				BC04R
				BC11V
				BC08R used with H322

Standard Addresses

DAC1	170440
DAC2	170442
DAC3	170444
DAC4	170446

Vectors

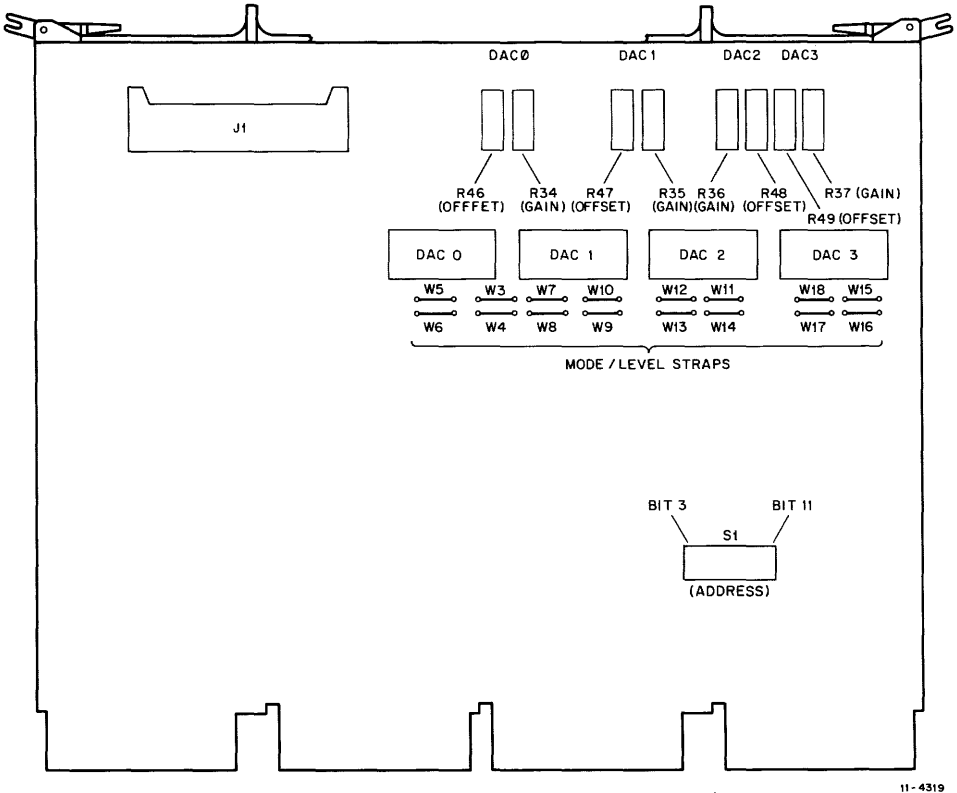
None. The AAV-11 does not cause interrupts.

Diagnostic Programs

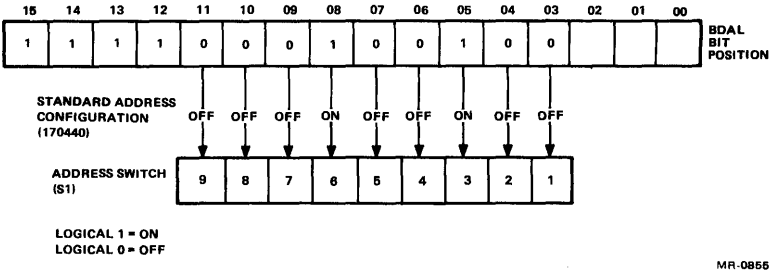
Refer to Appendix A.

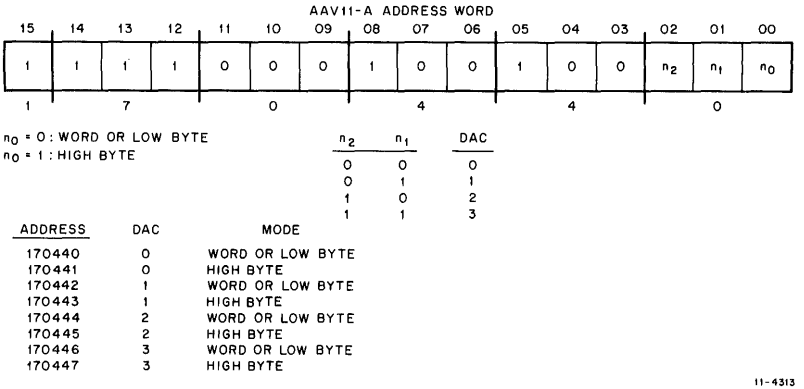
Related Documentation

ADV11-A, KWV11-A, AAV11-A, DRV11 User's Manual (EK-ADV11-OP)
Field Maintenance Print Set (MP00186)
Microcomputer Interfaces Handbook (EB-20175-20)



AAV11-A Address Switches (Set for 17044n)





AAV11-A Address Decoding

Jumper Configurations for Bipolar Operation (as Shipped)

	±2.56 V	±5.12 V	±10.24 V
DAC1			
W3	IN	IN	OUT
W4	OUT	OUT	IN
W5	IN	OUT	OUT
W6	IN	IN	IN
DAC2			
W7	IN	IN	OUT
W8	OUT	OUT	IN
W9	IN	OUT	OUT
W10	IN	IN	IN
DAC3			
W11	IN	IN	OUT
W12	OUT	OUT	IN
W13	IN	OUT	OUT
W14	IN	IN	IN
DAC4			
W15	IN	IN	OUT
W16	OUT	OUT	IN
W17	IN	OUT	OUT
W18	IN	IN	IN

Jumper Configurations for Unipolar Operation

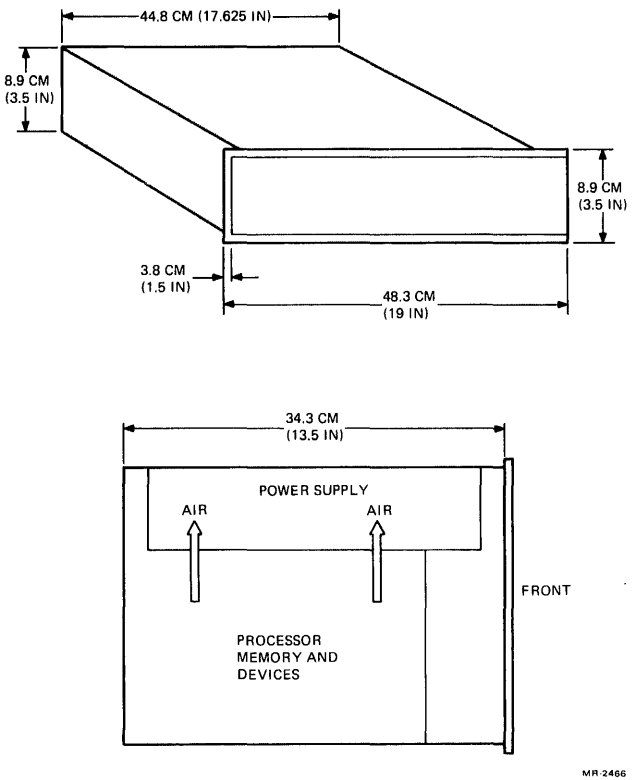
	0 V – +5.12 V	0 V – +10.24 V
DAC1		
W3	IN	IN
W4	OUT	OUT
W5	IN	OUT
W6	OUT	OUT
DAC2		
W7	IN	IN
W8	OUT	OUT
W9	IN	OUT
W10	OUT	OUT
DAC3		
W11	IN	IN
W12	OUT	OUT
W13	IN	OUT
W14	OUT	OUT
DAC4		
W15	IN	IN
W16	OUT	OUT
W17	IN	OUT
W18	OUT	OUT

AAV11-A Input Code/Output Voltage Relationship

Input Code	Unipolar	Bipolar
0000	0 V	−FS
4000	1/2 FS	0 V
7777	+FS - 1/2 LSB	+FS - 1/2 LSB

BA11-M

Mounting Box: Physical Specifications



BA11-M Assembly Unit

Electrical *(These specifications reflect the characteristics of the H780 power supply.)*

Input Voltage (Continuous: see Note 1.)
100 Vac-127 Vac (H780-C, -H, -K)
200 Vac-254 Vac (H780-D, -J, -L)

Temporary Line Dips Allowed
100% of voltage, 20 ms max.

AC Inrush Current
70 A at 127 V 60 Hz (8.33 ms)
25 A at 254 V 50 Hz (10 ms)

Input Power (Fans Included)
340 W at full load max.
290 W at full load typical

EMI (Emission and Susceptibility)
Per DEC STD 102.7 and VDE N-12 limits

Input Protection
H780-C, -H, -K (100 Vac-127 Vac) fast blow, 5 A fuse
H780-D, -J, -L (200 Vac-254 Vac) fast blow, 2.5 A fuse

Hi-Pot
2 kV for 60 seconds from input to output, or input to chassis

Output Power (Combinations not to exceed 110 W.)
+5 V, 1.5 A - 18 A
+12 V, 0.25 A - 3.5 A

Maximum DC Current Under Fault Conditions
+5 V bus = 28 A
+12 V bus = 9.5 A

+5 V Output

Total regulation	5 V ± 3%
Line regulation	±0.5%
Load regulation	± 1.0%
Stability	0.1%/1000 hours
Thermal drift	0.025%/° C (See Note 2.)
Ripple	150 mV p-p (1% for f<3 kHz)
Dynamic load regulation	± 1.2% di/dt = 0.5 A/μs ΔL = 5 A

Noise	1% peak at 5 > 100 kHz (noise is superimposed on ripple)
Interaction due to +12 V	± 0.05%
+12 V Output	
Total regulation	12 V ± 3%
Line regulation	±0.25%
Load regulation	±0.5%
Stability	0.1%/1000 hours
(See Note 2.)	0.025%/° C above 25° C
Ripple	350 mV p-p (1% for f <3 kHz)
Dynamic load regulation	±0.8% di/dt = 0.5 A/μs f<500 Hz ΔL = 3 A
Noise	1% peak f > 100 kHz (Noise is superimposed on ripple.)
Interaction due to +5 V	±0.2%
Overvoltage Protection	
+5 V	6.3 V nominal 5.65 V min. 6.8 V max.
+12 V	15 V nominal 13.6 V min. 16.5 V max.
Adjustments	
+5 V output	4.05 V-6.8 V Guarantee range 4.55 V-5.65 V
+12 V output	10.6 V-16.5 V Guarantee range 11.7 V-13.6 V
Controls	
Rear panel	AC ON/OFF switch
Front console	DC ON/OFF switch HALT/ENABLE switch
(Master only)	LTC ON/OFF switch

Console Indicators
- DC ON
- RUN (master)
- SPARE (master only)

Backplane Signals
- BPOK H
- BDCOK H
- BEVNT L } Transmitted
- BHALT L
- SRUN L Received (master only)

Mechanical

Cooling
Two self-contained fans provide 0.7140 m^3/min (30 ft^3/min) air flow.

Size
13.97 cm w × 8.43 cm h × 37.15 cm l
(5-1/2 in w × 3-1/3 in h × 14-5/8 in l)

Weight
5.90 kg (13 lb)

Environmental

Temperature

Ambient	5°-50° C (41°-122° F)
Storage	−40°-70° C (−40°-158° F)

Humidity
90% maximum without condensation

NOTES

1. **Operation from ac lines below 100 V may cause the power supply to overheat because of decreased air flow from the cooling fans.**

2. **Thermal drift parameters apply after five minutes of warm-up and are measured with an averaging meter at the processor backplane terminal block under system loading.**

BA11-M

Option Variations

BA11-MA Consists of a BA11-MC mounting box with H9270-A backplane and H780A power supply for 115 Vac, 60 Hz.

BA11-MB Consists of BA11-MC mounting box with H9270-A backplane and H780-B power supply for 230 Vac, 50 Hz.

BA11-MC Consists of 3.5 inch high mounting box with no backplane or power supply.

BA11-ME Consists of BA11-MC mounting box with H9270-A backplane and H780-E power supply for 115 Vac, 60 Hz.

BA11-MF Consists of BA11-MC mounting box with H9270-A backplane and H780-F power supply for 230 Vac, 50 Hz.

Power Supply Models

	115 Vac	230 Vac	Line Cord	Fans	Console Type
H780-A	X		X	X	Master
H780-B		X	X	X	Master
H780-C	X			X	None
H780-D		X		X	None
H780-E	X		X	X	Slave
H780-F		X	X	X	Slave
H780-H	X			X	Master
H780-J		X		X	Master
H780-K	X			X	Slave
H780-L		X		X	Slave
H780-M	X				Note 1
H780-N		X			Note 1
H780-P	X		X	X	Note 2
H780-R			X	X	Note 2

NOTES

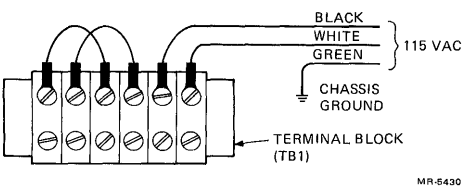
1. **The H780-M and -N have no control panel on the basic option. The Business Products 320 line uses a control panel that has two DC ON indicators (PN 54-12695). This control panel is carried as part of the 11/03-J computer.**

2. **The H780-P and -R also use the 54-12695 control panel. They differ from the -M and -N in that the basic power supply option includes the control panel, a line cord, and fans.**

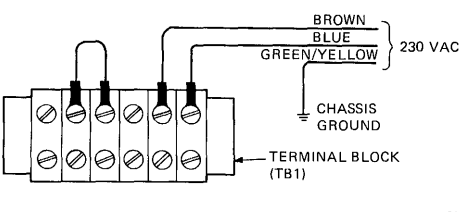
3. **The 115 Vac options operate on 100 Vac–127 Vac at either 50 or 60 Hz. The 230 Vac options operate on 200 Vac–254 Vac at either 50 or 60 Hz.**

Power Supply/Control Panel Interface Cables

Cable	DEC PN
DC output cable	7011584-0-0
Power supply status cable (logic cable)	7011411-0K-0
Power supply console cable	7008612-0M-0

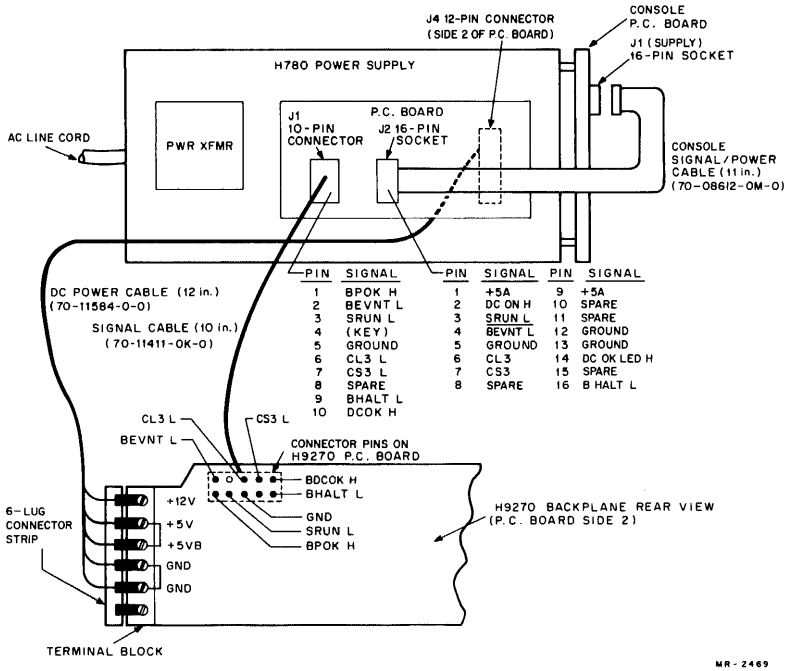


115 Vac Terminal Block Wiring



230 Vac Terminal Block Wiring

Cable Interconnections



H780 to H9270 Backplane Connections

Master/Slave Interface Cables

Length		DEC PN
10.2 cm	(4 in)	7008612-0D
15.0 cm	(6 in)	7008612-0F
22.9 cm	(9 in)	7008612-0K
27.5 cm	(11 in)	7008612-0M
35.6 cm	(14 in)	7008612-1B
45.7 cm	(18 in)	7008612-1F
124.0 cm	(49 in)	7008612-4A
61.0 cm	(2 ft)	7008612-02
1.83 m	(6 ft)	7008612-6A
3.05 m	(10 ft)	7008612-10
4.88 m	(16 ft)	BC034-16*

*Refer to the "Systems Configurations" section for applications using this cable.

+12 V Adjustment

Perform the following procedure when adjusting the +12 Vdc output.

1. Apply power to the LSI-11 or PDP-11/03 system and allow a five minute warm-up period.
2. Using a DVM, measure the +12 V output at the LSI-11 or PDP-11/03 backplane terminal block.
3. Using a small screwdriver, adjust R87 until the DVM indicates +12.0 V (+11.64 V to +12.36 V acceptable range). Turning R87 CW (clockwise) decreases the +12 V output, while turning CCW (counterclockwise) increases the output.

NOTE

If R87 is turned too far CCW, the +12 V output will crowbar and drop to approximately 0 V. This will occur between +13.0 V and +16.5 V. Do not allow the supply to crowbar as this may blow the internal fuse (F1) protecting the +12 V regulator.

4. Using an oscilloscope, measure the ripple on the +12 V output at the backplane terminal block. The ripple should not be greater than 350 mV peak-to-peak.

+5 V Adjustment

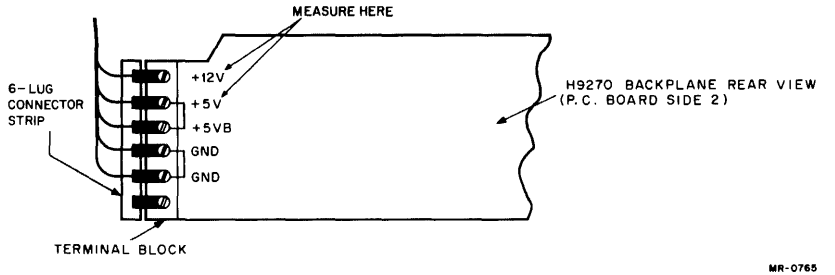
Perform the following procedure when adjusting the +5 Vdc output.

1. Apply power to the LSI-11 or PDP-11/03 system and allow a five minute warm-up period.
2. Using a DVM, measure the +5 V output at the LSI-11 or PDP-11/03 backplane terminal block.
3. Using a small screwdriver, adjust R88 until the DVM indicates +5.0 V (+4.85 V to +5.15 V acceptable range). Turning R88 CW decreases the +5 V output, while turning CCW increases the output.

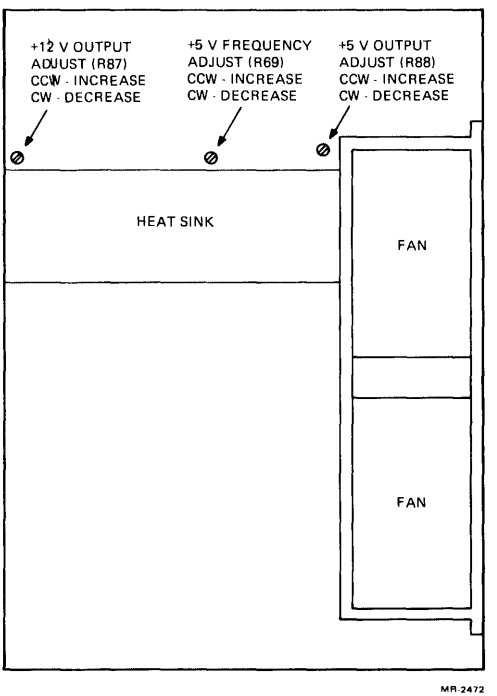
NOTE

If R88 is turned too far CCW, the +5 output will crowbar and drop to approximately 0 V. This will occur between +5.6 V and +6.8 V. Do not allow the supply to crowbar as this may blow the internal fuse (F2) protecting the +5 V regulator.

4. Using an oscilloscope, measure the amplitude and frequency of the ripple on the +5 V output at the backplane terminal block. The ripple should not be greater than 150 mV peak-to-peak with a period from 80 μs-140 μs. If the ripple period is not within 80 μs-140 μs, adjust R96. Turning R96 CW decreases the ripple period, while turning CCW increases the period. After adjusting the ripple period, recheck the +5 V output (steps 2 and 3).



Backplane Terminal Block



Locations of H780 Adjustments

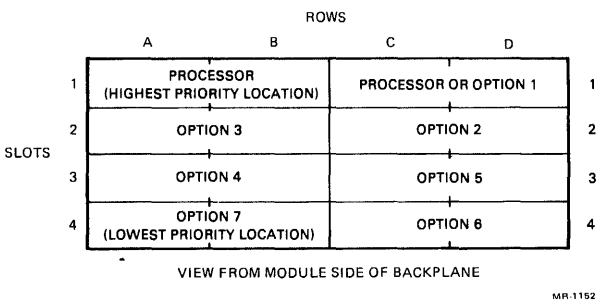
Controls and Indicators

BA11-M/H780 Controls and Indicators

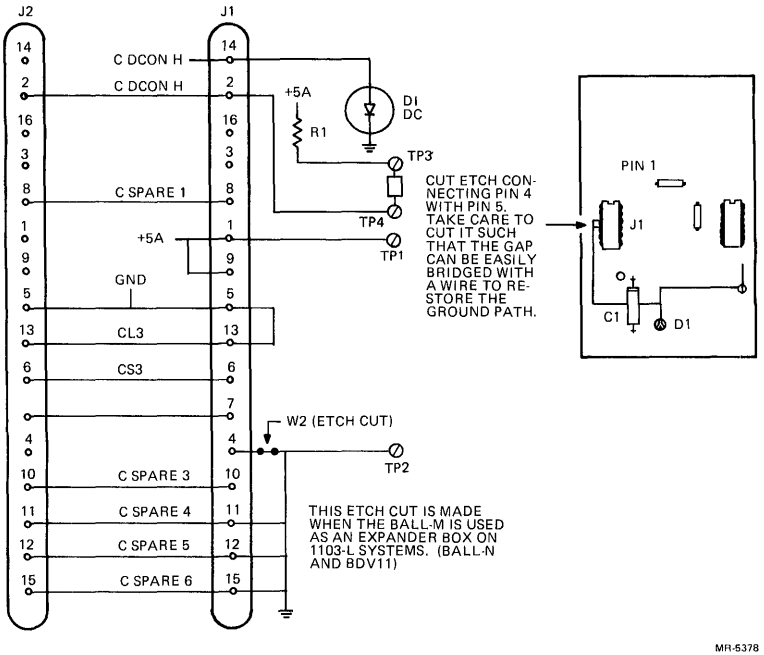
Control/ Indicator	Type	Function
DC ON	LED Indicator	Illuminates when the DC ON/OFF toggle switch is set to ON and proper dc output voltages are being produced by the H780. If either the +5 or +12 V output from the H780 is faulty, the DC ON indicator will not illuminate. This is the only indicator on the H780-K and -L slave supplies.
RUN	LED Indicator	Illuminates when the processor is in the run state (see ENABLE/HALT).
SPARE	LED Indicator	Not used by the H780 or processor. The H780 contains circuitry for driving this indicator for user applications.
DC ON/OFF	Two-Position Toggle Switch	When set to ON, enables the dc outputs of the H780. The DC ON indicator will illuminate if the H780 dc output voltages are of proper values. If a slave supply is connected to a master, the slave DC ON indicator will light if the slave dc output voltages are of proper value. When set to OFF, the dc outputs from the H780 are disabled and the DC ON indicator is extinguished. If a slave supply is connected to a master, the slave DC ON indicator will also extinguish.
ENABLE/HALT	Two-Position Toggle Switch	When set to ENABLE, the BHALT L line from the H780 to the processor is not asserted and the processor is in the run mode (RUN indicator illuminated).

BA11-M/H780 Controls and Indicators (Cont)

Control/ Indicator	Type	Function
ENABLE/HALT	Two-Position Toggle Switch	When set to HALT, the BHALT L line is asserted, allowing the processor to execute console ODT microcode (RUN indicator extinguished).
LTC ON/OFF Switch	Two-Position Generation	When set to ON, enables the toggle of the line time clock (LTC) BEVNT L signal by the H780. When set to OFF, disables the H780 line time clock.
AC ON/OFF (Rear Panel)	Two-Position Toggle Switch	When set to ON, applies ac power to the H780. When set to OFF, removes ac power from the H780.
FUSE (Rear Panel)	5 A or 2.5 A Fast Blow	Protects H780 from excessive current. H780-C, -H, and -K use a 5 A fuse. H780-D, -J, and -L use a 2.5 A fuse.



H9270 Option Positions



H780 Slave Console Modification

H780 Slave Console Modification

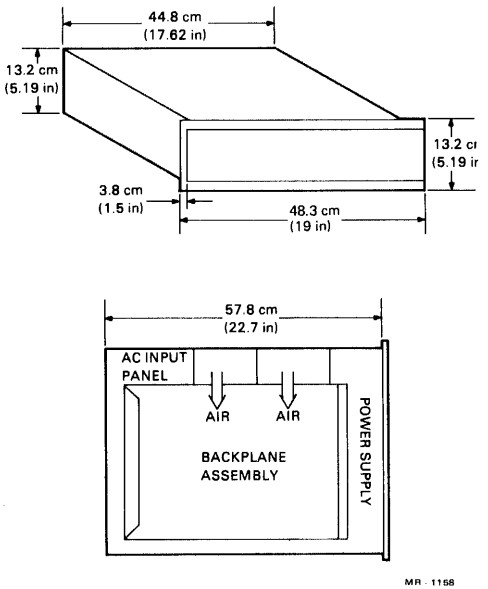
The slave console (54-12143) for the H780 (in the BA11-ME/F 3.5 inch PDP-11/03 expander box) contains an etch that applies a ground signal to pin 4 (and others) on J1. This is desirable except when the BA11-M is used as an expander box and contains a line clock, such as with the BDV11 or when a BA11-M is used to expand an PDP-11/03-L system. In this case, the BDV11 requires the BEVNT signal to generate line clock interrupts. If this etch is present, the signal BEVNT L is asserted (reference H780 sheet 3 schematic), turning off the BEVNT signal.

To correct this unwanted condition, it is necessary to cut an etch on the 54-12143 slave console board. This etch is made *only* for the reason described above.

ECO no. 54-12143-PN002 has been written to document this change. In the ECO, the etch cut is referred to as W2. Pay particular attention to this when adding a BA11-M as an expander box, or when replacing the power supply/slave console assembly (H780-E/F/K/L) or the slave console board.

BA11-N

Mounting Box: Physical Specifications



BA11-NE and BA11-NF Assembly Unit

Power Supply Specifications

Item	Specification
Current Rating	5.5 A at 115 Vrms 2.7 A at 230 Vrms
Inrush Current	100 A peak for one-half cycle at 128 Vrms or 256 Vrms
Apparent Power	630 VA
Power Factor	The ratio of input power to apparent power shall be greater than 0.6 at full load and low input voltage.
Output Power	+5 Vdc, ±250 mV at 22 A. (A minimum of 2 A of +5 Vdc power must be drawn to ensure that the +12 Vdc supply regulates properly.) +12 Vdc, ±600 mV at 11 A.

Power-Up/Power-Down Characteristics

Static Performance

Power-up	BDCOK H goes high: 75 Vac BPOK H goes high: 90 Vac
Power-down	BPOK H goes low: 80 Vac BDCOK H goes low: 75 Vac

Dynamic Performance

Power-up	3 ms (min.) from dc power within specification or to BDCOK H asserted. 70 ms (min.) from BDCOK H asserted to BPOK H asserted.
Power-down	4 ms (min.) from ac power off to BPOK H negated. 4 ms (min.) from BPOK H negated to BDCOK H negated. 5 microseconds (min.) from BDCOK H negated to dc power as of specifications.

Option Variations

BA11-NC Consists of 13.2 cm (5.2 inch) mounting box with metal cover, H9273 backplane, and H786 power supply with console, for 115 Vac, 60 Hz.

BA11-ND Consists of 13.2 cm (5.2 inch) mounting box with metal cover, H9273 backplane, and H786 power supply with console, for 230 Vac, 50 Hz.

BA11-NE Consists of 13.2 cm (5.2 inch) mounting box with metal cover, H9273 backplane, and H786 power supply without console, for 115 Vac, 60 Hz.

BA11-NE Consists of 13.2 cm (5.2 inch) mounting box with metal cover, H9273 backplane, and H786 power supply without console, for 230 Vac, 50 Hz.

CONFIGURATION
Jumpers and Switches

Backplane Jumper Positions – There are three jumper positions on the H9273 backplane: W1, W2, and W3. Jumpers are installed in all three positions when the backplane is manufactured. The conditions under which jumpers should be inserted or removed are described in the "Backplane Jumpers" table.

The jumper in position W1 is involved with CPU event interrupts. These interrupts can be initiated in two ways. First, a signal source external to the BA11-N can be used to pull the LSI-11 bus BEVNT L line low; in this case, the jumper of W1 of each H9273 backplane in the system would have to be removed. Second, the LTC signal generated in the H786 power supply can be used to pull the BEVNT L line low, thereby initiating vectored interrupts at a rate that depends on the BA11-N line frequency. W1 connects the LTC signal to the BEVNT L line; hence, in this case, the jumper would be left in position W1 of the H9273 backplane. In a multiple-box system, the box containing the M8012 module (i.e., the last box in the system) must be the source of the LTC signal; thus, the W1 jumper must be inserted in the backplane of this box and must be removed from the backplane of the other box(es).

The jumper in W2 connects CK1 to CL1 in row 1, while the jumper in W3 connects DK1 to DL1, also in row 1. These jumpers must be inserted whenever a quad KD11 CPU resides in row 1 of the first box.

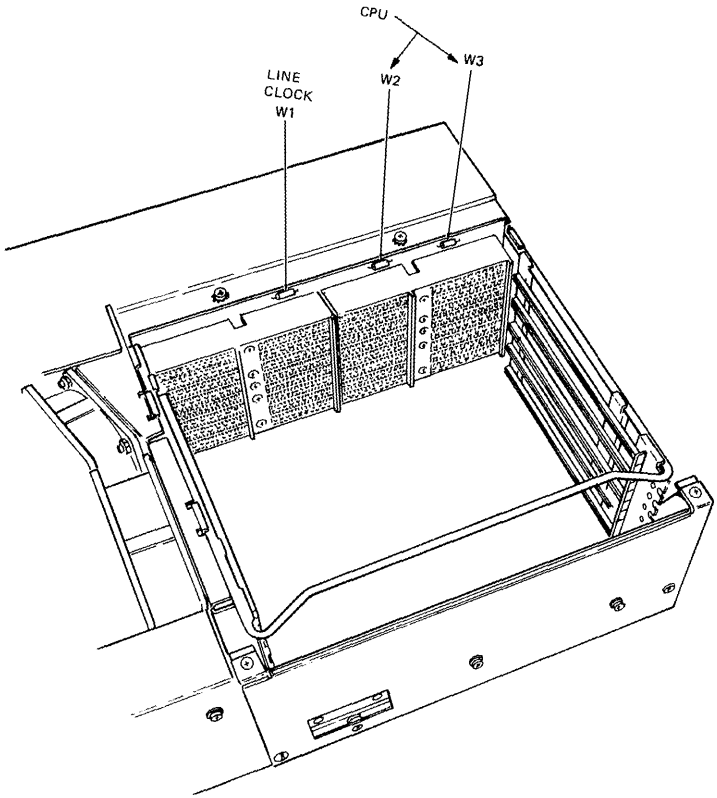
All three of these jumpers can be inserted and removed without any need for disassembly, other than removing the logic box base from the cover. However, if it ever becomes necessary to have clear access to the backplane, follow the instructions given for removal of the logic assembly in the *BA11-N Mounting Box Technical Manual*, EK-BA11N-TM.

Backplane Jumpers

Jumper Position	Jumper(s) In	Jumper(s) Out
W1	When the H786 power-supply generated LTC signal is used to assert the LSI-11 bus BEVNT L signal.	When it is not desired to have line time clock (LTC) sourcing BEVNT L, such as when an external source is used instead.
W2, W3	When a processor module (KD11 or KDF11) is inserted in row 1 of the backplane.	When any other module is installed in row 1; that is, when the backplane is part of an expander box.

NOTE

In multiple backplane systems, only the one backplane can have jumper W1 installed. If a BDV11 module is used, install the jumper in the backplane containing the BDV11 module.



Backplane Jumpers

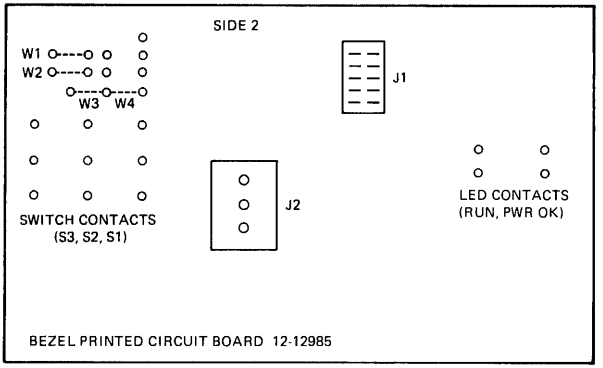
MR-2470

Bezel Assembly Jumper Positions – There are four jumper positions, W1, W2, W3, and W4, on the printed circuit board of the bezel assembly. When the board is manufactured, jumpers are inserted in positions W1, W2, and W4; position W3 is left blank.

If it is necessary to remove the bezel assembly printed circuit board for any reason, follow the instructions for removal of the bezel assembly given in the *BA11-N Mounting Box Technical Manual*, EK-BA11N-TM.

Bezel Assembly Jumpers

Jumper Position	Jumper In	Jumper Out
W1, W2	When the bezel AUX ON/OFF switch is used to control the power-supply-generated LTC signal. (When the switch is in the AUX ON position, LTC-initiated interrupts are possible).	When the bezel AUX ON/OFF switch is used to turn the system power controller on and off.
W3	When the bezel is to be mounted on the expander box. (W3 permits the HALT switch to light the RUN indicator.)	When the bezel is part of the main box; that is, the CPU is mounted in this bezel's backplane.
W4	When the bezel is part of the main box. (W4 enables the S RUN L signal to light the RUN indicator.)	When the bezel is mounted on an expander box.



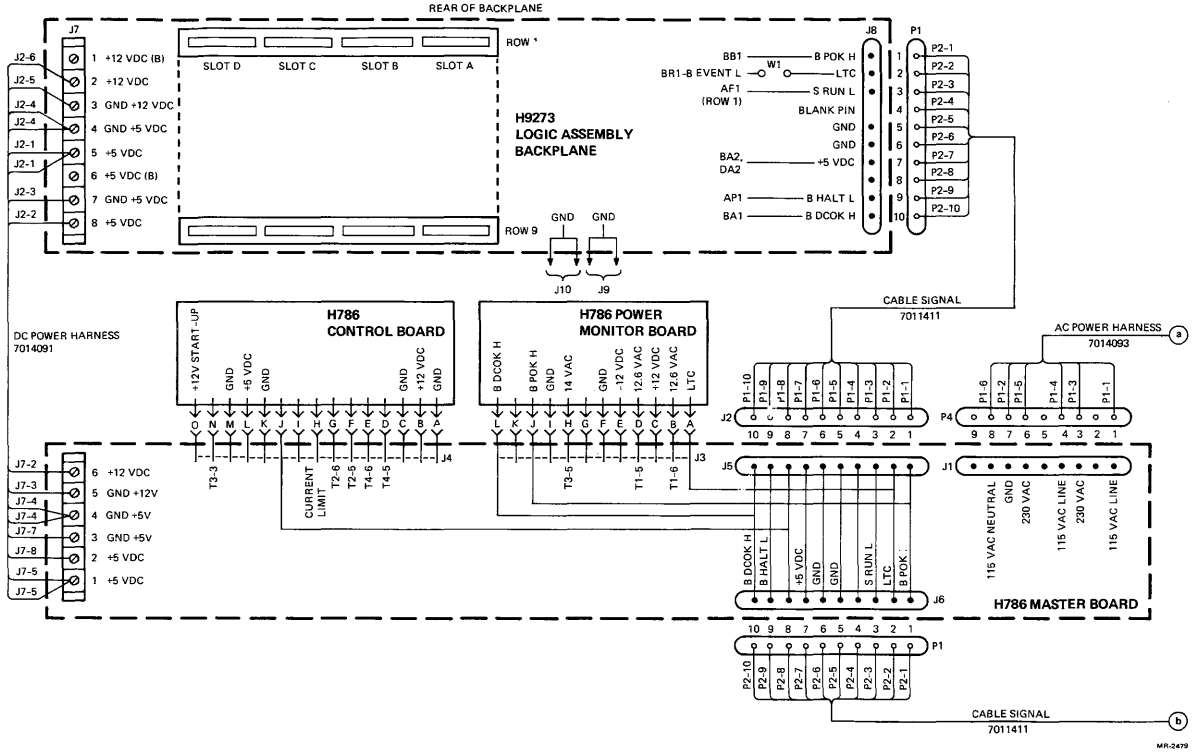
NOTES:
1. VIEW IS FROM THE REAR OF THE BEZEL WHEN THE BOARD IS MOUNTED ON THE BEZEL.
2. JUMPERS ARE MOUNTED ON SIDE 1.

BEZEL ASSEMBLY JUMPERS

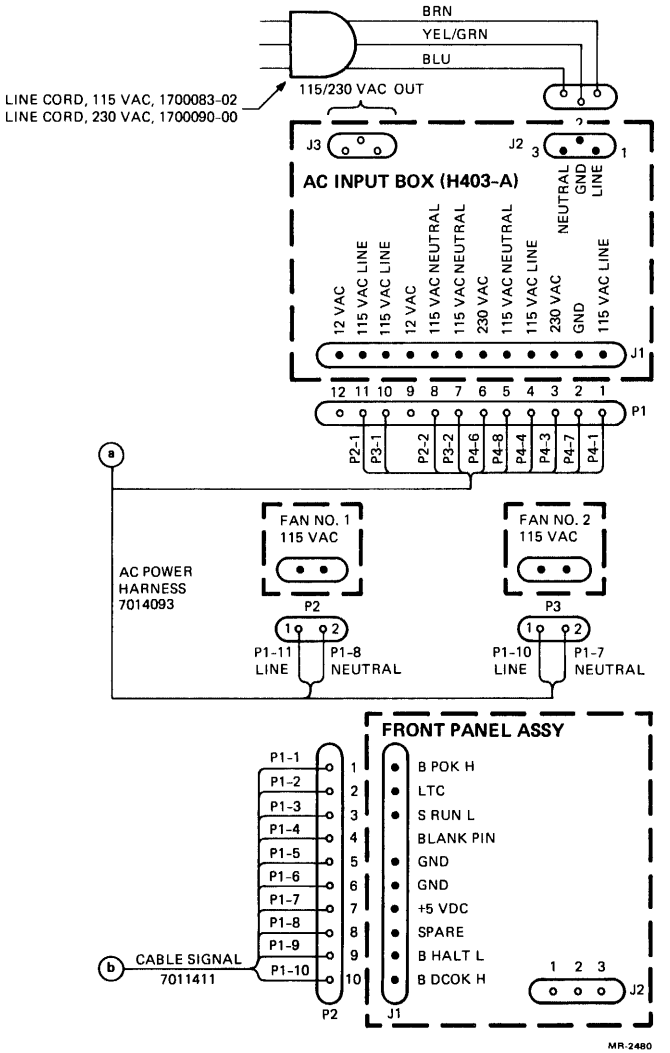
JUMPER POSITION	JUMPER IN	JUMPER OUT
W1, W2	WHEN THE BEZEL AUX ON/OFF SWITCH IS USED TO CONTROL THE POWER SUPPLY GENERATED LTC SIGNAL (WHEN THE SWITCH IS IN THE AUX ON POSITION, LTC-INITIATED INTERRUPTS ARE POSSIBLE).	WHEN THE BEZEL AUX ON/OFF SWITCH IS USED TO TURN THE SYSTEM POWER CONTROLLER ON AND OFF.
W3	WHEN THE BEZEL IS TO BE MOUNTED ON THE EXPANDER BOX (W3 PERMITS THE HALT SWITCH TO LIGHT THE RUN INDICATOR).	WHEN THE BEZEL IS PART OF THE MAIN BOX, I.E., THE CPU IS MOUNTED IN THIS BEZEL'S BACKPLANE.
W4	WHEN THE BEZEL IS PART OF THE MAIN BOX (W4 ENABLES THE S RUN L SIGNAL TO LIGHT THE RUN INDICATOR).	WHEN THE BEZEL IS MOUNTED ON AN EXPANDER BOX.

MR-2471

Bezel Printed Circuit Board



BA11-N Unit Interconnection (Sheet 1 of 2)



BA11-N Unit Interconnection (Sheet 2 of 2)

Adjustments

DC Voltage Measurement – The +5 Vdc and +12 Vdc regulated voltages can be measured at J7 of the backplane or, preferably, at the tip jacks on the M8012 module. The pins of J7 are numbered, and the wires connected to them are color coded. +12 Vdc and +5 Vdc are assigned the following pins and colors.

+12 Vdc - pin 2, purple wire
+12 Vdc ground - pin 3, black wire
+5 Vdc - pin 5, red wire
+5 Vdc ground - pin 4, black wire

The tip jacks on the M8012 module are color coded and labeled as follows.

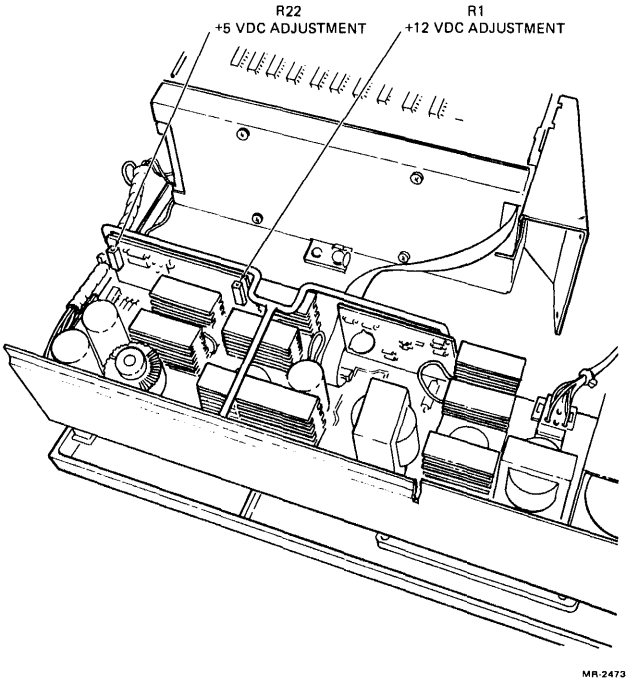
+12 Vdc - J3, purple
+5 Vdc - J2, red
ground - J1, black

Use a calibrated digital voltmeter to measure the voltages under normal load conditions.

NOTE

Do not measure the dc voltages without a load on the power supply; incorrect readings will result.

The +5 Vdc output should be +5 V ± 250 mV, while the +12 Vdc output should be +12 V ± 600 mV. If either voltage is out of tolerance, adjust the appropriate potentiometer on the control board. R1 varies the +12 Vdc output and R22 varies the +5 Vdc output. The potentiometers are identified in the figure that follows. The correct output should be achieved when a potentiometer is near its mid-range position. If a potentiometer must be turned to near an extreme position to achieve tolerance limits, there is perhaps a problem somewhere in the regulator. If the output cannot be brought within limits, replace the entire control board.



Power Supply Adjustments

Controls and Indicators

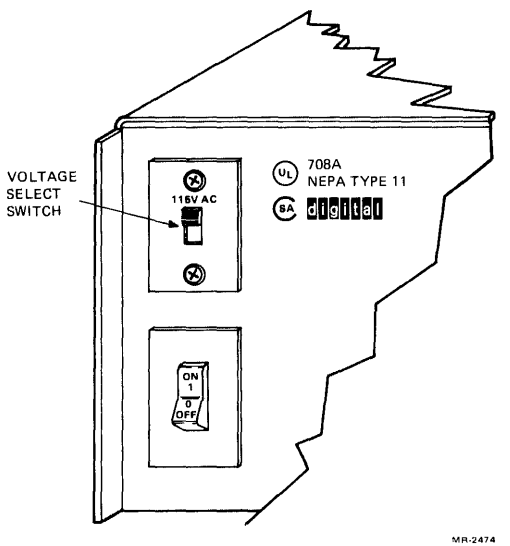
Operation – The BA11-N can have a blank front panel or one equipped with three switches and three indicators. In addition to the front panel switches and indicators, there is an ON/OFF switch and a primary voltage selection switch, both on the ac input box. The ON/OFF switch remains in the ON position when a power controller is used to apply primary power to the BA11-N; if a power controller is not used, the switch can be used to turn power on and off.

BA11-N Front Panel Switches and Indicators

Switch	Indicator	Function
AUX ON/OFF		Can be used for any desired function (switch is rated at 48 V, 1 A dc). Two functions are explained below. If the BA11-N is wired to control system power, the AUX switch turns the power on and off; if the BA11-N is **not wired** to control system power, the switch can control the LTC signal, disabling the signal when the switch is in the OFF position.
HALT		In the down position, the HALT switch forces the CPU to suspend normal program execution, enables console ODT microcode operation, and permits single-instruction execution. To resume program execution, return the HALT switch to the up position and enter a P command from the console terminal (providing that the contents of register R7 were not changed). Refer to the *Microcomputer Processor Handbook*, EB-18451-20, for a description of console ODT command usage. In an expander box, the HALT switch can be used to light the RUN indicator.
RESTART		When the momentary RESTART switch is activated, the CPU automatically carries out a power-up sequence; thus, the CPU can be rebooted at any time from the front panel.
	PWR OK	The PWR OK indicator lights when the power supply dc voltages are present.
	RUN	The RUN indicator lights when the CPU is executing programs.

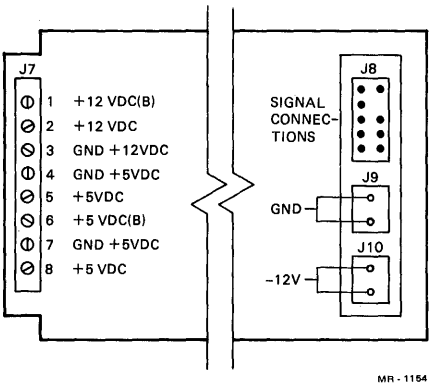
AC Voltage Selection – The BA11-N can be used with line voltage of either 115 Vac or 230 Vac. Only the ac line cord is different for the two voltages. However, a voltage selecting switch must be set to a position that corresponds to the line voltage being used. This switch is located on the rear of the ac input box, above the circuit breaker. The switch lever protrudes through a plate that is attached to the box.

If the line voltage being used is 115 Vac, the designation "115 Vac" should be printed on the plate above the switch lever. If the printing on the plate is 230 Vac, remove the plate. Flip the plate over and notice that 115 Vac is printed on the opposite side; also, notice that the switch lever itself is imprinted with 230 Vac. Move the switch lever down; 115 Vac should appear on the top of the lever. Replace the plate over the switch lever so that the printing on the outside of the plate reads "115" Vac. (When the plate is on, the printing on the switch lever cannot be seen.) The plate is fabricated so that the screw holes in the plate and the input box line up only when the switch position corresponds to the printing on the outside of the plate.

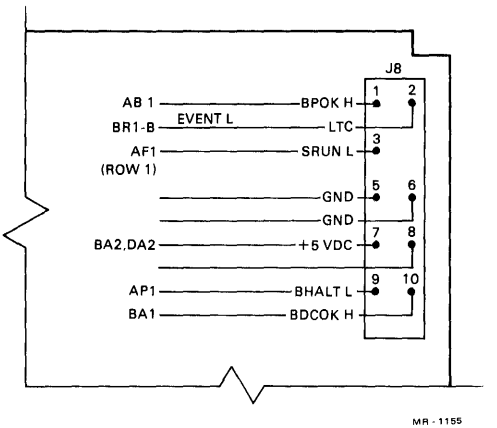


BA11-N Voltage Select Switch

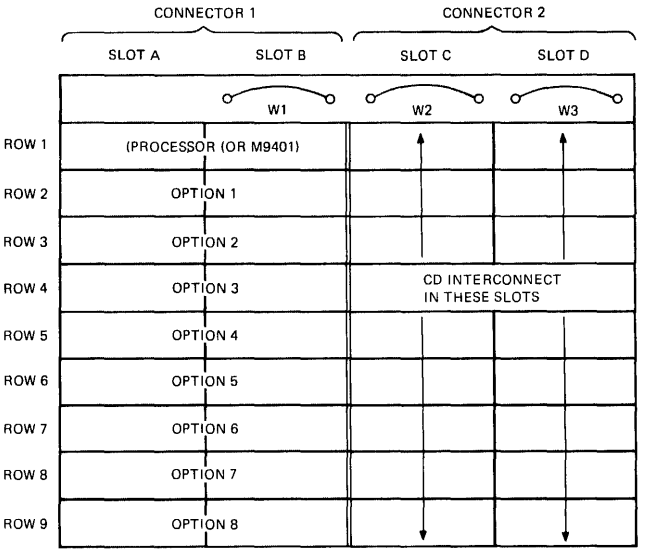
Backplanes



H9273-A Power Connections



H9273-A Signal Connections



VIEW IS FROM MODULE SIDE OF CONNECTORS.

BACKPLANE JUMPERS

JUMPER POSITION	JUMPER(S) IN	JUMPER(S) OUT
W1	WHEN THE H786 POWER SUPPLY GENERATED LTC SIGNAL IS USED TO ASSERT THE LSI-11 BUS BEVNT L SIGNAL.	WHEN IT IS NOT DESIRED TO HAVE LINE TIME CLOCK (LTC) SOURCING BEVNT L, SUCH AS WHEN AN EXTERNAL SOURCE IS USED INSTEAD.
W2, W3	WHEN A CPU MODULE IS INSERTED IN ROW 1 OF THE BACKPLANE.	WHEN ANY OTHER MODULE IS INSTALLED IN ROW 1, I.E., WHEN THE BACKPLANE IS PART OF AN EXPANDER BOX.

MR-2475

H9273-A Backplane Connectors

CD Bus Signals – The CD bus signals are supplied by slots C and D. The +5 V supply voltage is bused to all rows on pin A2 of slots C and D (that is, pins CA2 and DA2). Likewise, ground connections on pins CC2, CT1, DC2, and DT1 are bused to all rows. All other pins connect only to an adjacent row.

For example, pin CF2 of any row connects only to pin CF1 of the adjacent higher-numbered row. Pins on side 2 of the slot (B2, C2, etc.) connect to the adjacent higher-numbered row (except DT2, which connects to CT2 of the adjacent lower-numbered row), while pins on side 1 of the slot (B1, C1, etc.) connect to the adjacent lower-numbered row (except pin A1, which connects to C1 of the adjacent higher-numbered row).

Thus, each row, except 1 and 9, has 33 signal connections (other than +5 V and ground) to both the adjacent higher-numbered row and the adjacent lower-numbered row. To facilitate references to these two groups of 33 signals, group 1 is defined as the group of signals connecting a row (row X) to its adjacent lower-numbered row (row X-1). Group 2 is defined as the group of signals connecting a row to its adjacent higher-numbered row (row X+1). Generally, group 1 signals are found on side 1 pins, while group 2 signals are found on side 2 pins.

BA11-M/BA11-N Expansion Configuration

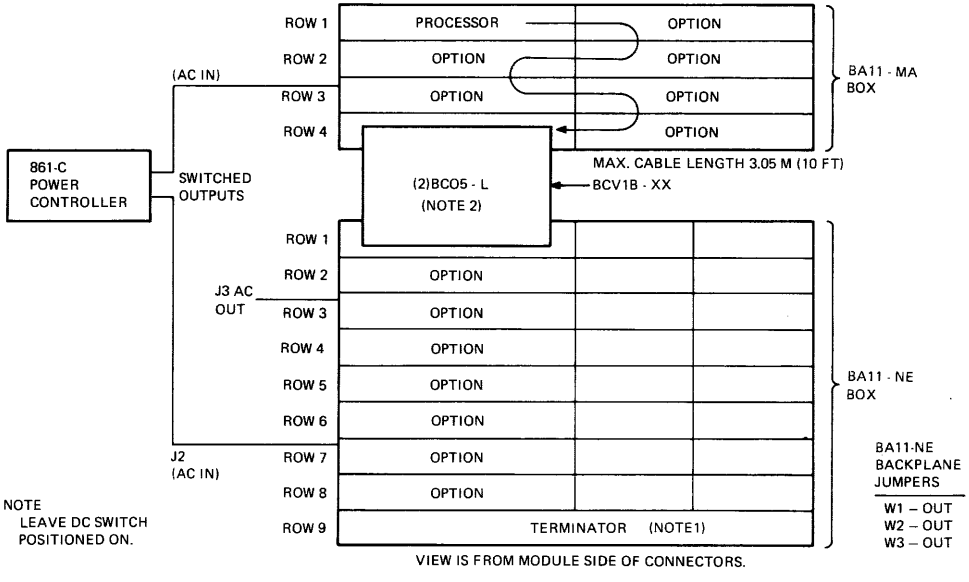
- The LTC is sourcing the BEVNT L in the BA11-MA box. (BDV11 is not being used.)
- Power is controlled by the 861C power controller ON/OFF switch.

NOTES

1. **If a BDV11, with E21 switch 5 "on," is used as the last module in the BA11-WE, install W1 in the BA11-NE backplane. Turn off LTC switch (must remain off) in the BA11-MA.**

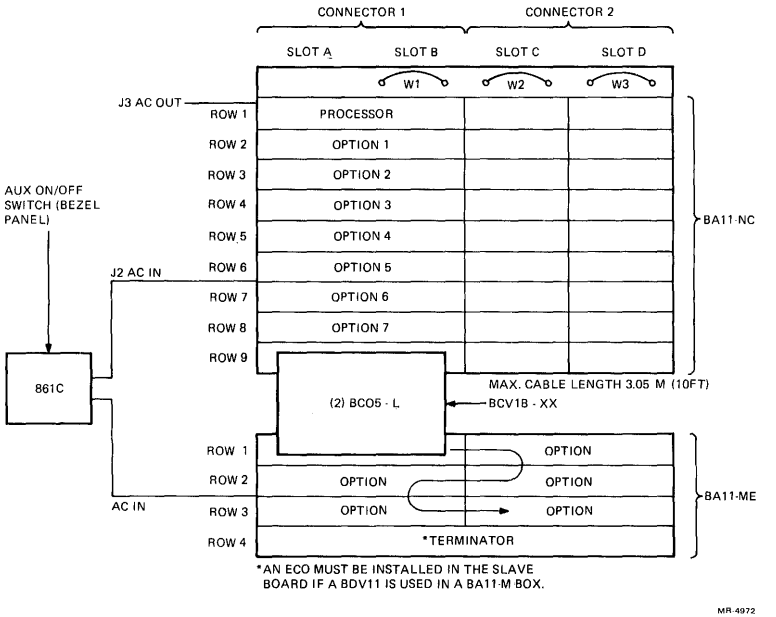
2. **BCV1B-XX* configuration: M9400 KE in first A-B slot after options in BA11-MA backplane. M9400 KD in first A-B slot in BA11-NE backplane.**

*XX denotes cable length.



MR-4973

BA11-MA to an NE Box Expansion



BA11-NC to an ME Box Expansion

BA11-NC backplane jumpers:

W1 - IN
W2 - IN (If M7264 or M7264-YA CPU is present.
W3 - IN If not, remove jumper.)

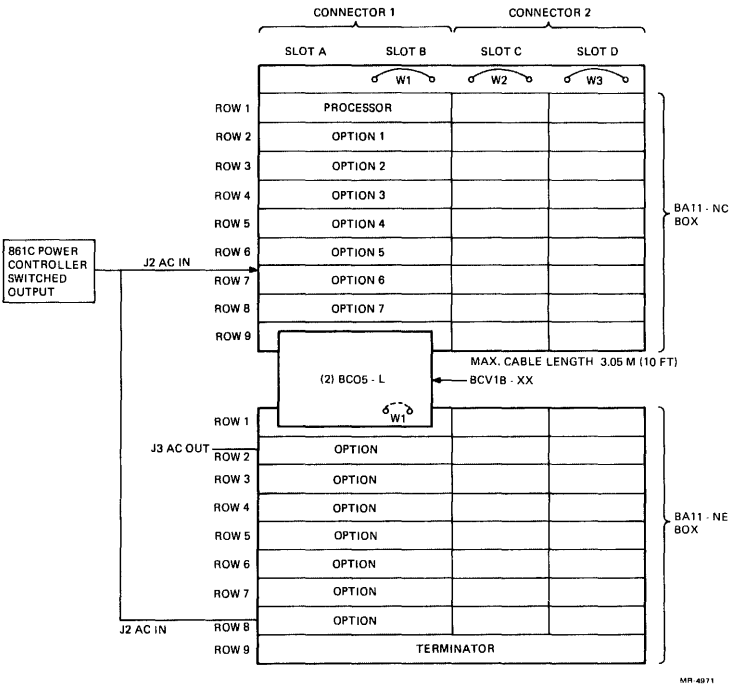
BA11-NC bezel jumpers:

W1 - OUT
W2 - OUT When bezel AUX ON/OFF switch is used to turn system power controller on or off; otherwise IN.
W3 - OUT
W4 - IN

NOTES

1. **If a BDV11, with E21 switch 5 "on," is used as the last module in the BA11-ME, install ECO (see Appendix B) in backplane of BA11-ME. Remove W1 from the backplane of BA11-NC.**

2. **BCV1B-XX configuration: see BA11 MA/NE configuration figure.**



BA11-N to Another N Box Expansion

NOTES

1. **If a BDV11, with E21 switch 5 "on," is used as the last module in the BA11-NK, install W1 in the BA11-NK backplane. Remove W1 from the BA11-NC backplane.**

2. **BCV1B-XX* configuration: M9400 KE in first A-B slot after options in BA11-NC. 9400 KD in first A-B slot of BA11-NK.**

*XX denotes cable length.

BA11-NC backplane jumpers:

W1 I
W2 I
W3 I If using CPU M7264 or M7264-YA; otherwise R.

BA11-NC bezel jumpers:

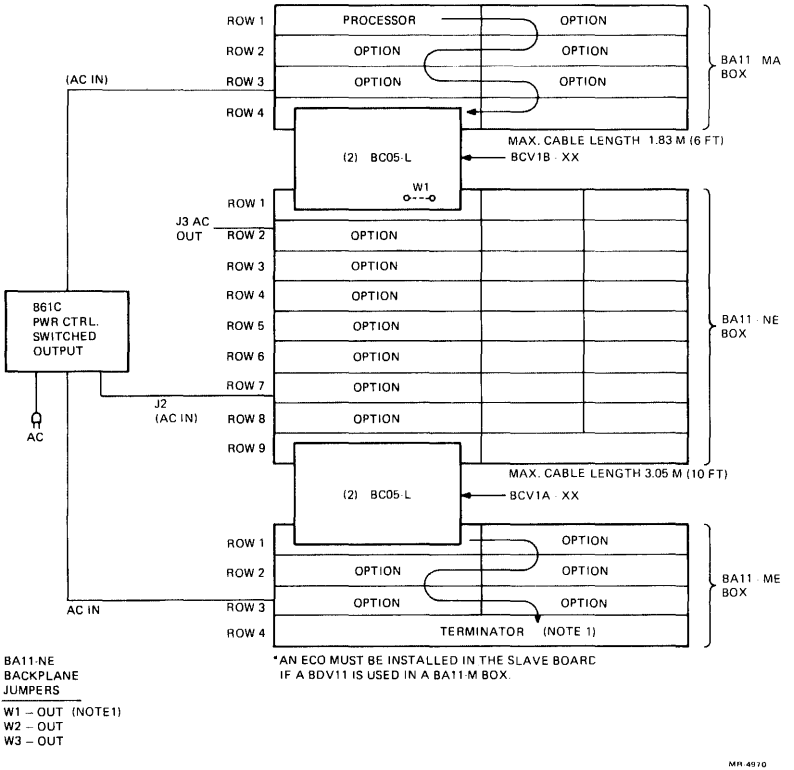
W1 I
W2 I
W3 R
W4 I

BA11-NE backplane jumpers:

W1 R
W2 R
W3 R

CAUTION

Do not attempt to source ac power for the BA11-N mounting box from the BA11-N box ac outlet, because the current rating of the BA11-N box will be exceeded and severe damage may occur. Also, do not attempt to provide ac power to three BA11-N boxes from one 861C power controller.



BA11-MA to an ME Box Expansion

NOTES

1. **If a BDV11, with E21 switch 5 "on," is used as the last module in the BA11-ME, install ECO (see Appendix B) in the BA11-ME backplane. Remove W1 from this BA11-NE backplane. Turn off LTC switch (must remain off) on BA11-MA.**

2. **BCV1B-XX* configuration**: BCV1A-XX; M9400 YD in first A-B slot after options in BA11-NE; M9401 in first A-B slot in BA11-ME backplane.**

*XX denotes cable length.
**See BA11-MA to an NE Box Expansion figure.
(See Appendix B for ECO information.)

DLV11-KA
EIA TO 20 MA CONVERTER

Amps		Bus Loads		Cables
+5	−12	AC	DC	BC21A-03 EIA
0	0	N/A	N/A	BC05F-XX 20 mA

+12 V@ 0.275 max. (supplied by EIA SLU interface module).

Standard Addresses and Vectors, Diagnostic Programs

None

Related Documentation

DLV11-KA EIA to 20 mA Installation Guide (EK-DLVKA-IN)
DLV11-KA Maintenance Print Set (MP00694)
Microcomputer Interfaces Handbook (EB-20175-20)

CONFIGURATION

General
The DLV11-K requires the configuration of 11 jumper wire connections and 1 capacitor connection. The configurations and functions of these jumpers are shown in the following table.

DLV11-KB Jumper Configurations

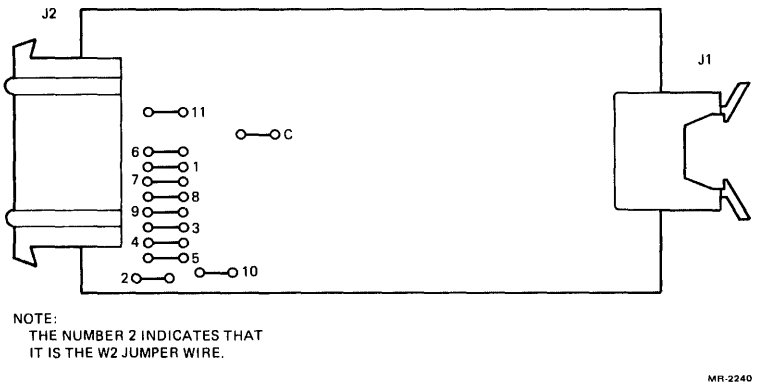
Function	Jumper In	Jumper Out
Passive 20 mA Receiver	W7, W9	W6, W8, W10
Active 20 mA Receiver*	W6, W8, W10	W7, W9
Passive 20 mA Transmitter	W2, W4	W1, W3, W5
Active 20 mA Transmitter*	W1, W3, W5	W2, W4
110 Baud Enabled*	W11	-
110 Baud Disabled	-	W11
Noise Suppression	See following Note.	See following Note.

*Factory configuration

NOTE

For use with an ASR-33 Teletype™, insert a 0.047 μF axial ceramic capacitor (DEC PN 10-12784-00) in the location designated C. This capacitor is inserted for the factory configuration. For any other terminal there is nothing inserted in this location.

For proper operation of Teletype ASR-33 with DEC-supplied paper tape software, the SLU should be configured for eight data bits, two stop bits, and no parity. The Teletype models can be LT33-DC, LT33-DD, LT33-DE, or an ASR-33 Teletype with the LT33-MB modification kit installed.



DLV11-KB Jumper Locations

Installation Requirements

The DLV11-KA option can be installed in a system that requires conversion from EIA RS-232 standard to a 20 mA current loop. The DLV11-KA option consists of a DLV11-KB converter box and a BC21A-03 interface cable as shown in the preceding illustration. The BC21A-03 is a 0.9 m (3 ft) cable that interconnects the DLV11-KB to an EIA SLU interface module. The smaller connector (2 × 5 pin) connects to the SLU module and the larger connector (2 × 7 pin) connects to the DLV11-KB box. Keying is provided on both connectors, and cable retention is provided by "locking pins" on the SLU connector. To disengage, pull back on the connector shell and the connector will slide free. However, if the cable is pulled, the locking pins will hold the connector firmly in place. A BC05F-XX cable can be used to connect the DLV11-KB converter box to DEC 20 mA terminals including the DEC-modified ASR-33 Teletype.

Cabling

Cables other than the DEC BC05F-XX can be used when installing the DLV11-KA option. However, any other cable must conform to the following parameters to meet the baud rate versus cable length specification.

1. Resistance - NMT 30 Ω/305 m (1000 ft) (NLT 22 AWG)
2. Capacitance to ground - NMT 50 pF/ft
3. Capacitance wire-to-wire - NMT 35 pF/ft

The BC05F-XX cable meets the above requirements. If the user desires to use shielded cable, the shield should be grounded to the chassis at the entry point and not to the DLV11-KB converter box. The user can fabricate custom cables for the 20 mA interface by using DEC connector, PN 12-09340-01 (AMP PN 1-480460-0), and pins PN 1209378-03 (AMP PN 350079-4).

Baud Rate

The DLV11-KA option will operate up to a maximum of 9600 baud, provided that the interface module can accommodate these rates. However, the maximum operational baud rate is also limited by the length of cable. Maximum recommended cable lengths for the specific baud rates are given in the following table. These recommendations are conservative and will yield satisfactory operation for almost all applications. These guidelines may be exceeded, but this should only be done after reviewing the DLV11-KA specifications, the severity of the operating environment, and the error rate that can be tolerated.

Baud Rate vs Cable Length

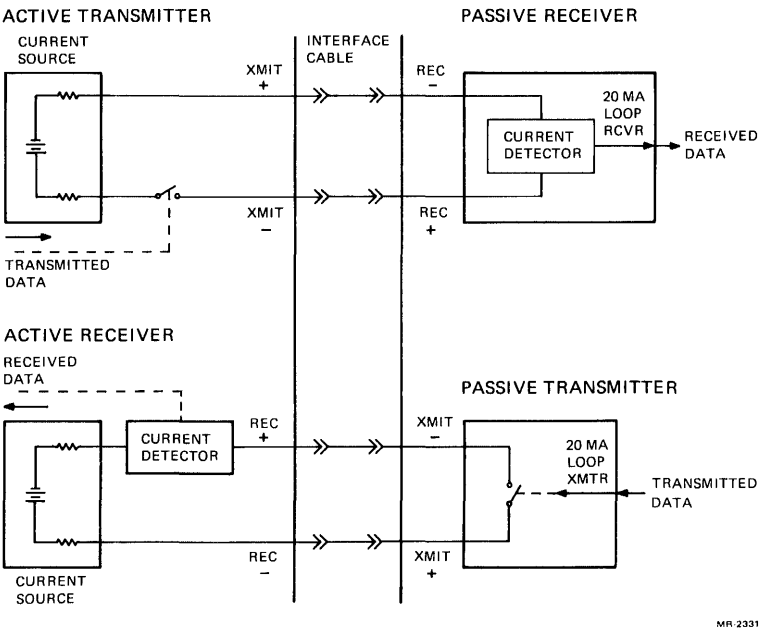
Baud Rate	Max. Cable Length
9600	30 m (100 ft)
4800	76 m (250 ft)
2400	152 m (500 ft)
1200	305 m (1000 ft)
600	610 m (2000 ft)
300	1220 m (4000 ft)
110	1220 m (4000 ft)

DLV11-KA

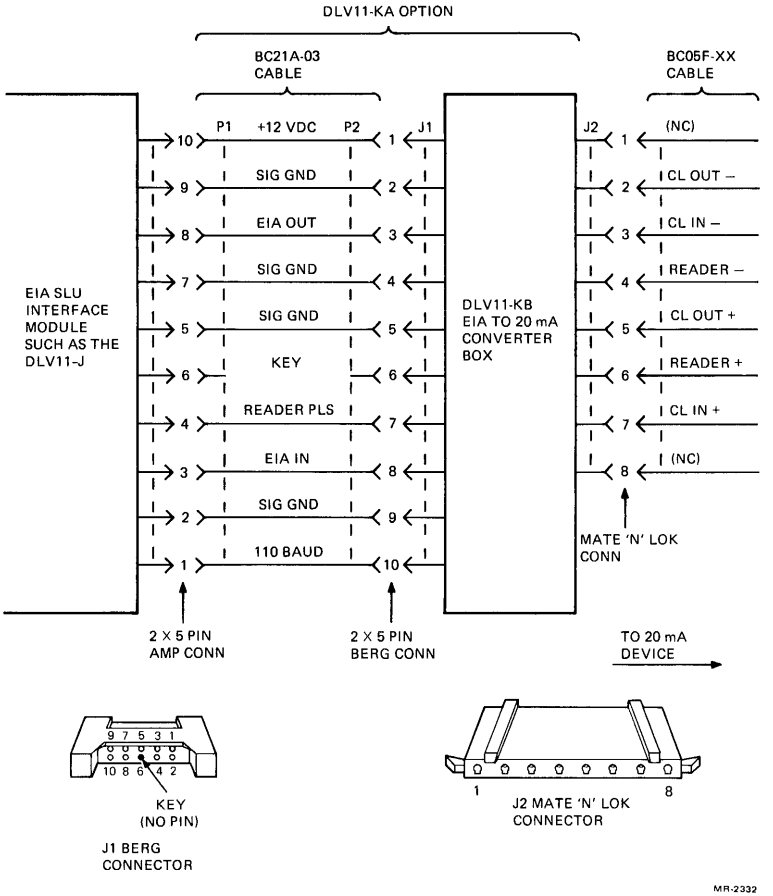
Terminal Recommendations

DIGITAL Terminals or SLUs	Active DLV11-KA Max. Cable Length (22 GA)	Max. Baud Rate	Passive DLV11-KA Max. Cable Length (22 GA)	Max. Baud Rate
DLV11	1220 m (4000 ft)	*	**	*
DLV11-F	1220 m (4000 ft)	*	**	*
DLV11-KA	1220 m (4000 ft)	9600	1220 m (4000 ft)	9600
M598	1220 m (4000 ft)	9600	**	9600
LA36	457 m (1500 ft)	300	457 m (1500 ft)	300
VT52	1220 m (4000 ft)	9600	**	9600
LA180S	1220 m (4000 ft)	*	NA	NA
LA120	1220 m (4000 ft)	*	671 m (2200 ft)	*
VT100	1220 m (4000 ft)	9600	**	9600
LA120	1220 m (4000 ft)	9600	**	9600
Teletype ASR-33	305 m (1000 ft)	110	NA	NA

* Operation at 9600 baud only recommended for benign environments.
** Operation with more than 8 m (25 ft) of cable is not recommended.

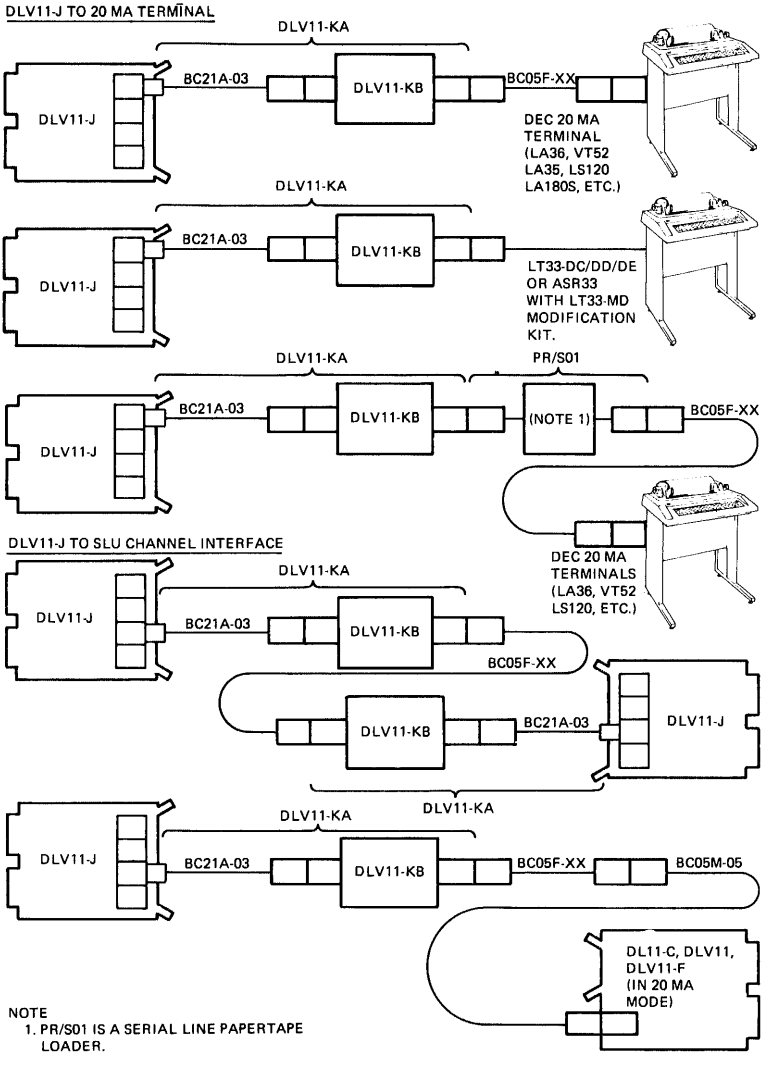


Standard Current Loop Interface



DLV11-KA Typical Installation

DLV11-KA



Typical Installation

G653/H223
MMV11-A CORE RAM MEMORY

Amps			Bus Loads		Cables
	+5	+12	AC	DC	
Stby.	3.0	0.2	1.91	1	None
Act.	7.0	0.6			

Standard Address

Not applicable

Vectors

None

Diagnostic Programs

Refer to Appendix A.

Related Documentation

Microcomputer Processor Handbook (EB-18451-20)
11V03 Field Maintenance Print Set (MP00094)

NOTE

Because of addressing limitations, this module is not compatible with PDP-11/23 systems with more than 64K bytes of memory.

Backplane Jumpers

When installing the MMV11-A in any slot but the last slot in a backplane, two jumpers must be inserted on the backplane to maintain the interrupt and DMA daisy-chain grants. If the MMV11-A is placed in an even-numbered slot, the jumpers must connect as follows.

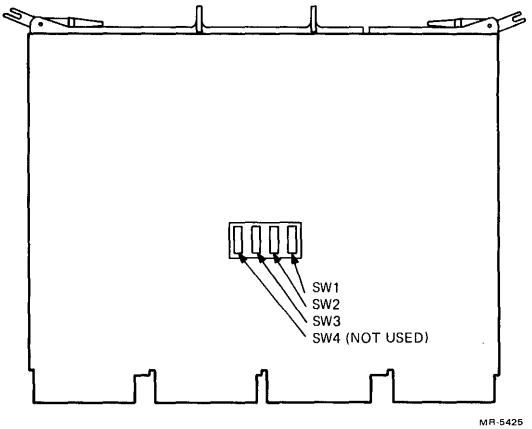
in the option slot preceding MMV11-A	to the option slot following MMV11-A
CN2	CM2
CS2	CR2

If the MMV11-A is placed in an odd-numbered slot, the jumpers must connect as follows.

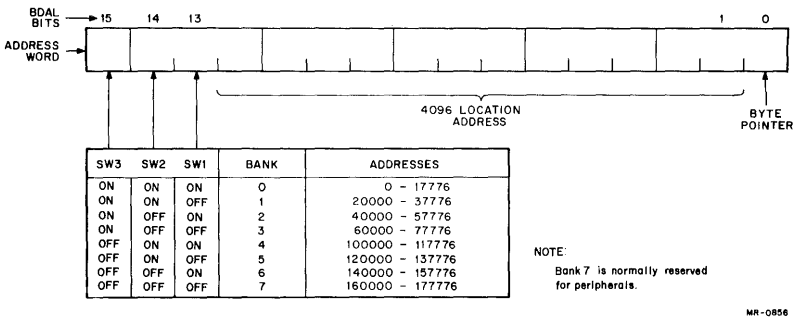
in the option slot preceding MMV11-A	in the option slot following MMV11-A
AN2	AM2
AS2	AR2

NOTE

The MMV11-A cannot be used in the BA11-N mounting box, in the H9273 backplane, or in any other backplane that does not have the LSI-11 bus pinning in the "C" and "D" slots.



G653/H223



SW3	SW2	SW1	BANK	ADDRESSES
ON	ON	ON	0	0 - 17776
ON	ON	OFF	1	20000 - 37776
ON	OFF	ON	2	40000 - 57776
ON	OFF	OFF	3	60000 - 77776
OFF	ON	ON	4	100000 - 117776
OFF	ON	OFF	5	120000 - 137776
OFF	OFF	ON	6	140000 - 157776
OFF	OFF	OFF	7	160000 - 177776

NOTE:
Bank 7 is normally reserved for peripherals.

MR-0856

MMV11-A Addressing

H780 POWER SUPPLIES

H780 Power Supplies

Models, specifications, and basic adjustments are presented in this section. For more detailed technical information, refer to *H780-C,-D,-H,-J,-K,-L Power Supply User's Manual*, EK-H780C-OP-001, or to *Microcomputer Handbook*, EB0794853.

H780 Specifications

Input Voltage
100 Vac-127 Vac (H780-A, -C, -E, -H, -K, -M, -P)
200 Vac-254 Vac (H780-B, -D, -F, -J, -L, -N, -R)

Operation from ac lines below 100 V may cause the power supply to overheat because of decreased air flow from the cooling fans.

Temporary Line Dips Allowed
100% of voltage, 20 ms max.

AC Inrush Current
70 A @ 127 V, 60 Hz (8.33 ms)
25 A @ 254 V, 50 Hz (10 ms)

Fuses
5.0 A fast blow for 115 Vac options
2.5 A fast blow for 230 Vac options

Input Power (Fans Included)
340 W @ full load max
290 W @ full load typical

EMI (Emission and Susceptibility)
Per DEC STD. 102.7 and VDE N-12 limits

Output Power (Combinations not to exceed 110 W)
+5 V 1.5 A-18 A
+12 V 0.25 A-3.5 A

+5 V Output	
Total regulation	5 V ±3%
Line regulation	±0.5%
Load regulation	±1.0%
Ripple	150 mV p-p (1% for f <3 kHz)
Dynamic load regulation	±1.2% di/dt = 1.5 A/s Δ1 = 5 A
Noise	1% peak at f > 100 kHz (noise is superimposed on ripple)
Interaction due to +12 V	±0.05%
+12 V Output	
Total regulation	12 V ±3%
Line regulation	±0.25%
Load regulation	±0.5%
Ripple	350 mV p-p (1% for f < 3 kHz)
Dynamic load regulation	±0.8% di/dt = 0.5 A/ s f < 500 Hz Δ1 = 3 A
Noise	1% peak f > 100 kHz (noise is superimposed on ripple)
Interaction due to +5 V	±0.2%
Overvoltage Protection	
+5 V	6.3 V nominal min. = 5.65 V max. = 6.8 V
+12 V	15 V nominal min. = 13.6 V max. = 16.5 V
Adjustments	
+5 V output	4.05 V-6.8 V guarantee range 4.55 V-5.65 V
+12 V output	10.6 V-16.5 V guarantee range 11.7 V-13.6 V

Backplane Signals
- BPOK H
- BDCOK H
- BEVNT L
- BHALT L
- SRUN L

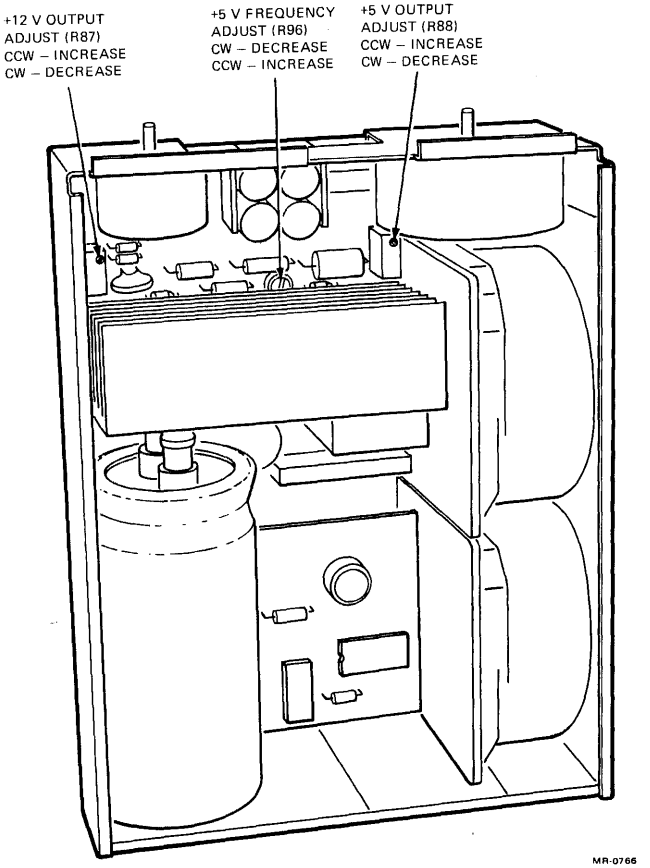
H780

Size

13.97 cm w × 8.43 cm h × 37.15 cm l
(5-1/2 in w × 3-1/3 in h × 14-5/8 in l)

Weight

5.90 kg (13 lbs)



H780 Voltage Adjustments

H780 Controls and Indicators

Control/ Indicator	Type	Function
DC ON	LED Indicator	Illuminates when the DC ON/OFF toggle switch is set to ON and proper dc output voltages are being produced by the H780. If either the +5 V or +12 V output from the H780 is faulty, the DC ON indicator will not illuminate. This is the only indicator on the H780-K and -L slave supplies.
RUN	LED Indicator	Illuminates when the LSI-11 or PDP-11/03 processor is in the run state (see ENABLE/HALT).
SPARE	LED Indicator	Not used by the H780 or processor. The H780 contains circuitry for driving this indicator for user applications.
DC ON/OFF	Two-Position Toggle Switch	When set to ON, enables the dc outputs of the H780. The DC ON indicator will illuminate if the H780 dc output voltages are of proper values. If a slave supply is connected to a master, the slave DC ON indicator will light if the slave dc output voltages are of proper value. When set to OFF, the dc outputs from the H780 are disabled and the DC ON indicator is extinguished. If a slave supply is connected to a master, the slave DC ON indicator will also be extinguished.
ENABLE/HALT	Two-Position Toggle Switch	When set to ENABLE, the BHALT L line from the H780 to the LSI-11 bus is not asserted and the processor is in the run mode (RUN indicator illuminated). When set to HALT, the BHALT L line is asserted, allowing the processor to execute console ODT microcode (RUN indicator extinguished).

H780 Controls and Indicators (Cont)

Control/ Indicator	Type	Function
LTC ON/OFF	Two-Position Toggle Switch	When set to ON, enables the generation of the line time clock (LTC) by the H780. When set to OFF, disables the H780 line time clock.
AC ON/OFF (Rear Panel)	Two-Position Toggle Switch	When set to ON, applies ac power to the H780. When set to OFF, removes ac power from the H780.
FUSE (Rear Panel)	5 A or 2.5 A Fast Blow	Protects H780 from excessive current. H780-C, -H, and -K use a 5 A fuse. H780-D, -J, and -L use a 2.5 A.

M7264-XX
LSI-11 PROCESSOR MODULES

Processor option designations and processor module numbers do not have a one-for-one correspondence. This section describes processors both in terms of option designations (KD11-X) and module numbers (M7264-XX). When replacing chip sets, check both the number on the handle and etch revision on the board. The jumpers are defined in this section; however, the "Systems Configurations" section presents the general rules for configuring refresh reply. For details of differences between various revisions of the processor modules, refer to Appendix B of the *Microcomputer Processor Handbook*, EB-18451-20. For all commercial products systems, refer to the *DEC Datasystem 320 Family Service Manual*, EK-DDS03-SV-001, available in hard copy or microfiche.

Processor Model Designations

KD11-F

Processor with 4K RAM:

M7264 Mostek 4096	M2264-EB Mostek 4027
M7264-AB Intel® 2104	M7264-FB DEC 4027
M7264-CB Fujitsu 8224	M7264-HB Motorola 4027
M7264-DB Intel 2104-A	M7264-JB Fujitsu 8227

KD11-H (M7264-YA)

Processor without 4K RAM

EIS/FIS option can be added:
- Etch Revs C and D use KEV11
- Etch Rev D uses KEV11-B (EIS only)
- Etch Revs E and F use KEV11-A

KD11-L

Processor with on-board 4K RAM and EIS/FIS:
- Etch Rev C or D KD11-F plus KEV11 or
- Etch Rev E or F KD11-F plus KEV11-A

KD11-N

Processor without on-board 4K RAM and with EIS/FIS:
Etch Rev C or D KD11-H plus KEV11 or
Etch Rev E or F KD11-H plus KEV11-A

KD11-P

Processor with on-board 4K RAM and with DIS:
Etch Rev E or F M7264-BB plus KEV11-CA

KD11-Q

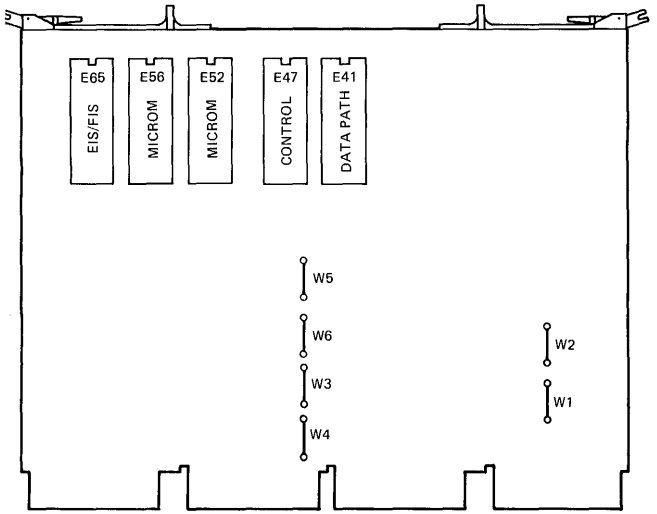
Processor without on-board 4K RAM and with DIS:
Etch Rev E or F M7264-YB plus KEV11-CA

M7264 Specifications

Size:	Quad-height module 26.6 cm (10.5 inches) × 22.8 cm (8.9 inches)
Power:	+5 V ±5%, 1.8 A + 12 V ± 5%, 0.8 A
Bus Loads:	AC - 2.4 unit loads
	DC - 1 unit load
Environment:	DEC STD 102 Class C

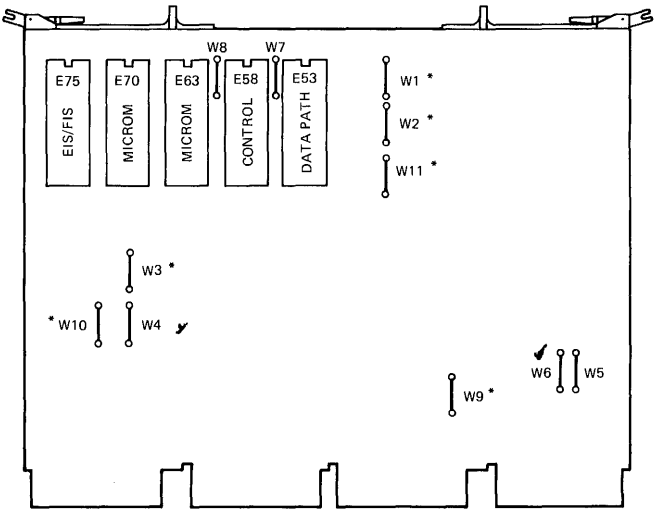
Related Documentation

Microcomputer Processor Handbook (EB-18451-20)
KD11-F Field Maintenance Print Set (MP-00049-00)
KD11-H Field Maintenance Print Set (MP-00050-00)
KD11-P Field Maintenance Print Set (MP-00264-00)
KD11-Q Field Maintenance Print Set (MP-00357-00)
KD11-WA Field Maintenance Print Set (MP-00569-00)
LSI-11 Maintenance Card (EK-LSI11-MC)



M7264 ETCH REV. C, D (W7 - W11 NOT USED)

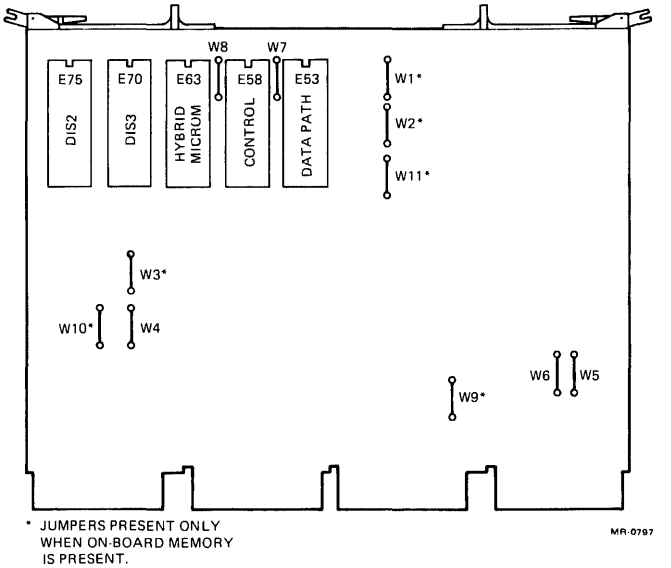
MR-0795



NOTE
M7264 ETCH REV E AND AFTER

* JUMPERS PRESENT ONLY WHEN ON-BOARD MEMORY IS PRESENT

MR-0796



M7264-BB DIBOL Processor

Jumper	Function
W1	Insert to select resident memory bank 1.
W2	Insert to select resident memory bank 0.
W3	Remove to enable event line (LTC) interrupt.
W4	Remove to enable processor controlled memory refresh.

W5, W6

Power-Up Modes

Mode	Jumpers W6	Jumpers W5	Mode Selected
0	R	R	PC at 24 and PS at 26, or halt mode
1	R	I	ODT microcode.
2	I	R	PC at 173000 for user bootstrap
3	I	I	Special processor microcode (not implemented).

Jumper	Function
W7	Factory-selected biasing voltage. Installed for VDATA = VROM.
W8	Factory-selected biasing voltage. Installed for VCTL = VROM.
W9	Remove to enable reply from resident memory.
W10	Remove to enable reply from resident memory during refresh.
W11	Enable on-board memory select.

Processor Module Jumper States

	(LSI-11 With 4K On-Board Memory)		(LSI-11 Without On-Board Memory)	
Jumper	KD11-F, -L	KD11-P	KD11-H, -J, -M, -R, -S, -U	KD11-Q
W1	R	R	R	R
W2	I	I	R	R
W3	R	R	R	R
W4	R	I	I	I
W5	R	R	R	R
W6	R	I	R	I
W7	*	*	*	*
W8	*	*	*	*
W9	R	R	I	I
W10	R	R	R	R
W11	I	I	R	R

*May vary with ECO level. Do not alter.

Diagnostic Programs

The following diagnostic programs are for use with LSI-11 processors except for the limitations noted.

VKAA?? LSI-11 basic instruction test

VKAB?? LSI-11 Extended Instruction Set (EIS) test. This program can only be run on LSI-11 CPUs with the KEV11 (EIS/FIS) or KEV11-CA (DIBOL instruction set) options installed.

VKAC?? LSI-11 Floating Point Instruction (FIS) test. This runs only on LSI-11 CPUs that have the KEV11 (EIS/FIS) option (23-00385).

NOTE

The KD11-P (or Q) supports DIS (DIBOL Instruction Set) and EIS (Extended Instruction Set) but not FIS (Floating Instruction Set). Therefore, FIS test (-VKACA0) will not run on a D322 or D324.

VKAD?? LSI-11 traps test. This diagnostic auto-sizes for the EIS, FIS, and DIBOL options.

- Older versions (Rev B1 and below) require the setting of a bit in the software switch register if EIS, FIS, or DIBOL is present.
- Rev A diagnostics will not run on D322 or D324 systems because of the DIS instructions.

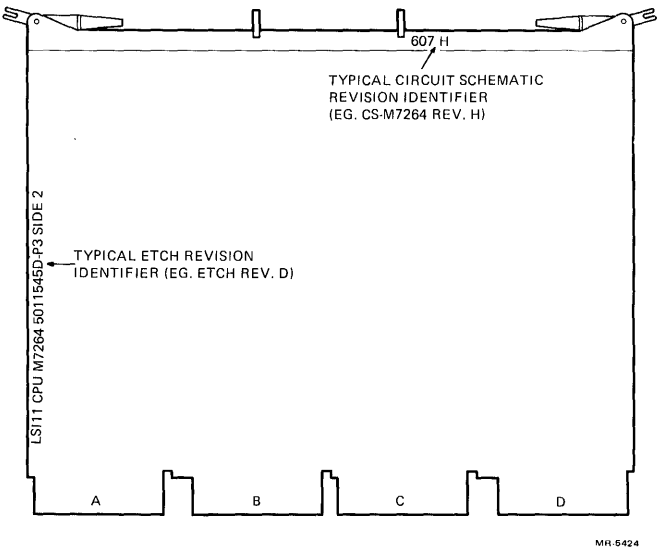
NOTE

See Appendix A for XXDP+ multimedia assignments.

VKAH?? Basic system exerciser. Tests serial line unit, memory, processor, EIS/FIS, clock, and both floppy disks under various conditions. Software switch register must be set for options.

VKAI?? DIS move and string instruction tests. This diagnostic tests the DIBOL instruction set. The CPU must have KEV11-CA (DIS) option installed. Ref D322, 324.

VKAJ?? DIS decimal instruction tests. This diagnostic tests the DIBOL instruction set. The CPU must have the KEV11-CA (DIS) option installed. Ref D322, 324.



M7264 Revision Identifiers

M7264-YA Etch Rev C

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1611 B-51	21-11549-00	−5.1	
CONTROL	CP 1621 B-451	23-001C2-01	−5.1	2004 pattern
MICROM-0	CP 1631 B-3006	23-086A5-01	−5.1	Without ECO 2
	CP 1631 B-3010	23-088A5-01	−5.1	With ECO 2
MICROM-1	CP 1631 B-3007	23-087A5-01	−5.1	
EIS/FIS (if present) KEV11	CP1631 B-3015	23-091A5-01	−5.1	
RAMs				
M7264	Mostek	21-11749	−9	Without ECO 2A
M7264-YA	None			With ECO 2A

M7264-AB, M7264-YA Etch Rev D

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1611 B-51	2111549-00	−5.1	2004 pattern
MICROM-0	CP 1631 B-3010	23-088A5-01	−5.1	
MICROM-1	CP 1631 B-3007	23-087A5-01	−5.1	
EIS/FIS (if present)				
KEV11	CP 1631 B-3015	23-091A5-01	−5.1	
KEV11-B (EIS only)	CP 1631 B-12	12-090A5-01	−3.9	
RAMs				
M7264	Mostek	21-11749	−9	Without ECO 4
M7264	Mostek 4096	21-12726-00	−5.1	With ECO 4
M7264-AB	Intel 2104	21-12958-01	−5.1	With ECO 4
M7264-YA	None			Not present

M7264-AB, M7264-YA Etch Rev E

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1611 B-39	21-11549-01	−3.9	
	PQ 1611 H	21-15579-00	−3.9	With ECO 21
CONTROL 2004 pattern	CP 1621 B-173	23-002C4	−3.9	With ECO 12
	CP 1621 B-439	23-001C3	−3.9	Without ECO 12
MICROM-0	CP 1631 B-103	23-001B5	−3.9	
MICROM-1	CP 1631 B-073	23-002B5	−3.9	
EIS/FIS (if present)				
KEV11-A	CP 1631 B	23-003B5	−3.9	
RAMs				
M7264	Mostek 4096	21-12726-00	−5.1	
M7264-AB	Intel 2104	21-12958-01	−5.1	
M7264-YA	None			Not present

M7264-BB, M7264-YB Etch Rev E

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1611 B-51	21-11549	−5.1	Without ECO 5
	CP 1611 B-39	21-11549-01	−3.9	With ECO 5
	PQ 1611 H	21-15579-00	−3.9	With ECO 21
CONTROL				
2004				
pattern	CP 1621 B-451	23-001C2-01	−5.1	With ECO 5
2007	CP 1621 B-439	23-001C3	−3.9	Without ECO 12
pattern	CP 1621 B-173	23-002C4	−3.9	With ECO 12
	CP 1621 B	23-003C3	−3.9	With ECO 21*
MICROM-0/1	CP 1631 B-3010	23-008A5-01	−5.1	Without ECO 10
		23-001B6	−3.9	With ECO 10
		23-002B6	−3.9	With ECO 12
		23-003B6	−3.9	With ECO 16
DIS				
(KEV11-CA)				
DIS 2		23-004B5	−3.9	3025 pattern
DIS 3		23-005B5	−3.9	3026 pattern
RAMs				
M7264-BB	Mostek 4096	21-12726-00	−5.1	
M7264-YB	None			Not present

*This part of ECO 21 applies to M7264-BB and -YB variations only.

M7264-CB, M7264-DB Etch Rev E

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1611 B-39	21-11549-01	−3.9	
	PQ 1611 H	21-15579-00	−3.9	With ECO 21
CONTROL	CP 1621 B-173	23-001C4	−3.9	2007 pattern
MICROM-0	CP 1631 B-103	23-001B5	−3.9	
MICROM-1	CP 1631 B-073	23-002B5	−3.9	
EIS/FIS (if present)				
KEV11-A	CP 1631 B	23-003B5	−3.9	
RAMs				
M7264-CB	Fujitsu 8224	21-13787-01	−3.9	
M7264-DB	Intel 2104A	21-13795-01	−3.9	

M7264, M7264-AB, -CB, -DB, -EB, -FB, -HB, -JB Etch Rev F

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1611 B-39	21-11549-01	−3.9	
	PQ 1611 H	21-15579-00	−3.9	With ECO 21
CONTROL	CP 1621 B-173	23-002C4	−3.9	2007 pattern
MICROM-0	CP 1631 B-103	23-001B5	−3.9	
MICROM-1	CP 1631 B-073	23-002B5	−3.9	
EIS/FIS (if present)				
KEV11-A	CP 1631 B-135	23-003B5	−3.9	
RAMs				
M7264	Mostek 4096	21-12726-00		350 ns
M7264-AB	Intel 2104	21-12958-01		350 ns
M7264-CB	Fujitsu 8224	21-13787-01	−3.9	350 ns
M7264-DB	Intel 2104A	21-13795-01	−3.9	350 ns
M7264-EB	Mostek 4027	21-13735-01		200 ns
M7264-FB	DEC 4027	21-12914-01		200 ns
M7264-HB	Motorola 4027	21-14114-01		200 ns
M7264-JB	Fujitsu 8227	21-14475-01		200 ns

M7264-BB, M7264-YB Etch Rev F

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1611 B-39	21-11549-01	−3.9	
	PQ 1611 H	21-15579-00	−3.9	With ECO 21
CONTROL	CP 1621 B-173	23-002C4	−3.9	
		23-003C3	−3.9	With ECO 21
MICROM-0	CP 1631 B-101	23-003B6	−3.9	
MICROM-1				Not present
DIS				
KEV11-CA				
DIS 2		23-004B5	−3.9	
DIS 3		23-005B5	−3.9	
RAMs				
M7264-BB	Mostek 4096	21-12726-00	−5.1	350 ns
M7264-YB	None			Not present

Circuit Schematic/ECO History

Etch Rev	CS Rev	ECO No.	Change
C	C		(Basic model)
C	D	1	Change value of C8 in clock pulse generator circuit from 150 pF to 47 pF.
C	E	2	1. Logic changed to clock BRPLY into reply flip-flop with an earlier timing signal. 2. Logic changed to disable BBS7 L for the duration of BDMG L or BSACK L assertion. 3. SRUN L signal decoded and applied to backplane. 4. ECO 2A created M7264-YA.
D	F	3	Logic changes for etch Rev C boards.
D	H	4	Circuit changes implemented to provide −5 V. Documentation updated by ECO 4A.

Circuit Schematic/ECO History (Cont)

Etch Rev	CS Rev	ECO No.	Change
E	J	5	New module layout. (DMA synchronization logic changed.) Add jumpers for resident memory reply and refresh reply. Add factory jumpers for V_{BB} selection. Logic change to allow external selection of resident memory. Add factory adjustment (R15) for setting refresh clock to 1.6 ms. Terminate bus lines AA1, AB1, AC1, AD1, and BP1. Replace E53, E58, E63, E70 with −3.9 V chips.
E	K	6	1. Change DMA synchronization logic. 2. Terminate E45-12, −13 to +3 V.
E	L	7	Correct documentation errors.
E	M	8	Change R44 from 22Ω to 27Ω. Change R45 from 10Ω to 22Ω.
C	D1,E1	9	Logic change implemented to inhibit BBS7 L during memory refresh.
D	F1,H1		Canceled by ECO 9A.
E	N		
C D E	D2,E2 F2,H2 P	10	1. Logic change implemented to inhibit BBS7 L during memory refresh. 2. Removed DMA/refresh alternate cycle scheme. 3. Changed M7264-BB to −3.9 V LSI chips. 4. Documentation corrrected by ECOs 10A and 10B.
E	R	11	Created M7264-YB.
E	S	12	Phased out 23-001C3 control chip and replaced it with 23-002C4.
E	T	13	Replaced 23-001B6 microm with 23-002B6.
E	U	14	1. Created M7264-CB, -DB.

Circuit Schematic/ECO History (Cont)

Etch Rev	CS Rev	ECO No.	Change
E	U	14	2. Operating frequency changed to 2.5 MHz min.-2.631 MHz max.
E	V	15	Routed IF CLR to pin AF1 from CH1.
E	W	16	Replaced 23-002B6 microm with 23-003B6.
F	Y	17	1. Released etch Rev F. 2. Refresh 625 ± 20 Hz adjustment. 3. Pins 22 and 24 of E75 tied to phase 2 and phase 4 for WCS. 4. SRUN buffered to CH1, AF1. 5. BPOK line deglitched. 6. Chip set changes (see data sheets). 7. Documentation updated by ECO 17A.
C	D3,E3 F3,H3	18	Added resistors R24, R25, R26, and R27 to D pull up BDAL16 and BDAL17 (formerly BAD16 and BAD17). This ECO is normally required in systems using DRV11-Bs or MSV11-Ds.
F	Z	19	Created M7264-EB, -FB, -HB, and -JB.
F	AA	20	Create M7264-YC document changes. 1. Delete R50. 2. Add R60.
F	AB	21	Use 1611H (21-15579-00) data chip instead of 1611A (21-14549-01). Use 23003C3 control chip instead of 23002C4. Change R45 from 22Ω to 15Ω and clock frequency to 2.47 MHz for -YB and -BB only.

M7269
BUS INTERFACE FOR RKV11-D DISK DRIVE CONTROLLER

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.8 max.	0	1.93	1	(2) BC05L + M993-YA

Standard Address

RKDS	(Drive Status)	177400
RKER	(Error)	177402
RKCS	(Control/Status)	177404
RKWC	(Word Count)	177406
RKBA	(Bus Address)	177410
RKDA	(Disk Address)	177412
RKDB	(Data Buffer)	177416

Vector

220

Diagnostic Programs

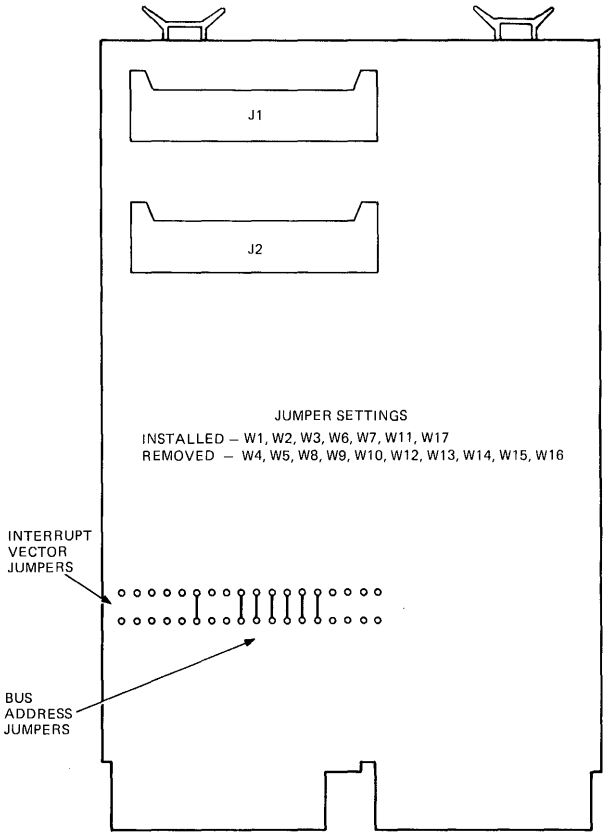
Refer to Appendix A.

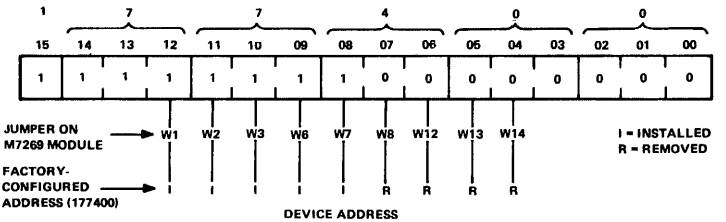
NOTE

The logic test programs should be run first, then the dynamic test, and finally the performance exerciser.

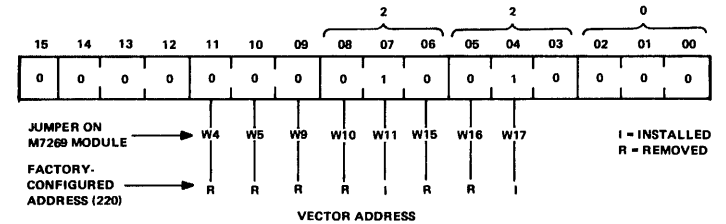
Related Documentation

RKV11-D Disk Drive Controller User's Manual (EK-RKV11-OP-001)
RKV11-Disk Drive Controller Technical Manual (EK-RKV11-TM-001)
Field Maintenance Print Set (MP00223)
RK05/RK05J/RK05F Disk Drive Maintenance Manual (EK-RK5JF-MM-001)
RK05/RK05J Disk Drive Preventive Maintenance Manual (EK-RK05J-PM-001)
RK05F DEC Disk Drive Preventive Maintenance Procedure (ED-RK05F-PM-001)
Microcomputer Interfaces Handbook (EB-20175-20)


J1
J2
JUMPER SETTINGS
INSTALLED – W1, W2, W3, W6, W7, W11, W17
REMOVED – W4, W5, W8, W9, W10, W12, W13, W14, W15, W16
INTERRUPT VECTOR JUMPERS
BUS ADDRESS JUMPERS
NOTE:
NORMALLY INSTALLED JUMPERS ARE SHOWN AS SOLID LINES.
MR-6114



MR-0803



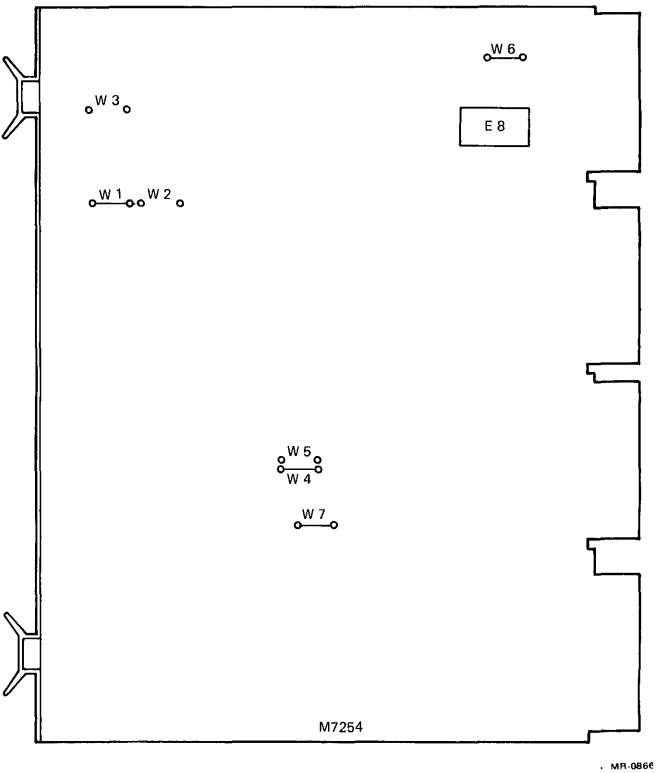
MR-0804

Jumper settings on the three RKV11-D modules are identical to those in the standard RK11-D configuration. A breakdown is given below for reference. There are no jumpers on M7268.

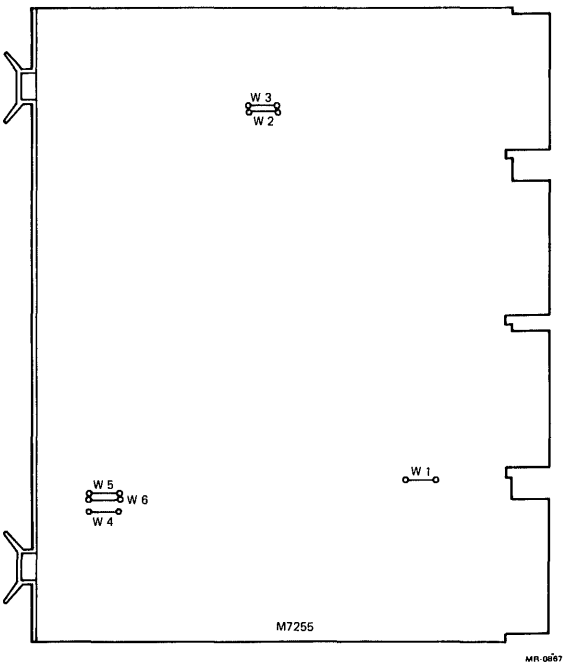
Module	Installed	Removed
M7254*	W1, W4, W6, W7	W2, W3, W5
M7255**	W1, W2, W6	W3, W4, W5
M7256	W2, W5, W7	W1, W3, W4, W6, W8

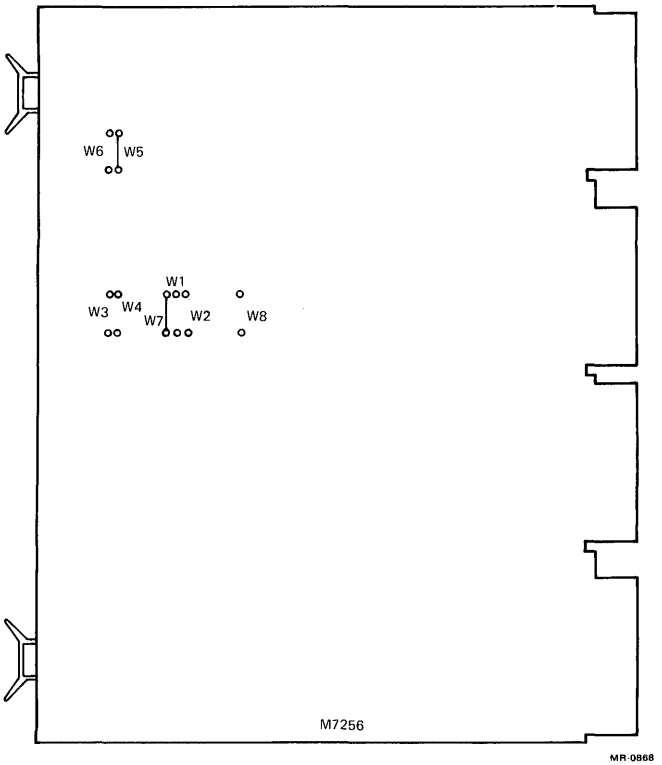
* Interrupt priority jumper (BR4-7) in socket E8 is not required since the RKV11-D was designed for only single-line interrupt scheme.

** 2.88 MHZ crystal used DEC PN 18-10694-3.

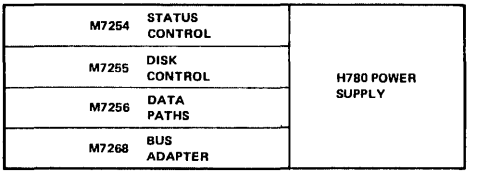

W 6
W 3
E 8
W 1
W 2
W 5
W 4
W 7
M7254
MR-0866

M7269




W6
W5
W1
W3
W4
W7
W2
W8
M7256
MR-0868

RKV11-D Module Utilization



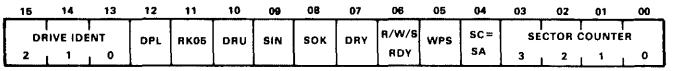
MR-0762

Drive Status Register (RKDS)

Address = 177400

NOTE

This register is a read-only register, and contains the selected drive status and current sector address.



CP-3137

Bit Definitions

Bit	Function
00-03	Sector Counter (SC) - These four bits are the current sector address of the selected drive. Sector address 00 is defined as the sector following the sector that contains the index pulse.
04	Sector Counter Equals Sector Address (SC = SA) - Indicates that the disk heads are positioned over the disk address currently held in the sector address register.
05	Write-Protect Status (WPS) - Sets when the selected disk is in the write-protected mode.
06	Read/Write/Seek Ready (R/W/S RDY) - Indicates that the selected drive head mechanism is not in motion, and that the drive is ready to accept a new function.
07	Drive Ready (DRY) - Indicates that the selected disk drive complies with the following conditions.

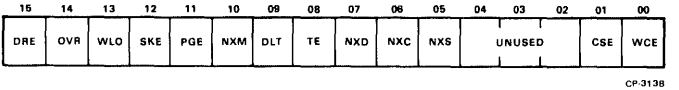
Bit Definitions (Cont)

Bit	Function
	1. The drive is properly supplied with power. 2. The drive is loaded with a disk cartridge. 3. The disk drive door is closed. 4. The LOAD/RUN switch is set to RUN. 5. The disk is rotating at a proper speed. 6. The heads are properly loaded. 7. The disk is not in a DRU (bit 10 or RKDS) condition.
08	Sector Counter OK (SOK) - Indicates that the sector counter operating on the selected drive is not in the process of changing, and is ready for examination. If this bit is not set, the sector counter is not ready for examination, and a second attempt should be made.
09	Seek Incomplete (SIN) - Indicates that due to some unusual condition, to seek function cannot be completed. Can be accompanied by RKER 15 (drive error). Cleared by a drive reset function.
10	Drive Unsafe (DRU) - Indicates that an unusual condition has occurred in the disk drive, and it is unable to properly perform any operations. Reset by setting the RUN/LOAD switch to LOAD. If, when the switch is returned to RUN, the condition recurs, an inoperative drive can be assumed, and corrective maintenance procedures should begin. Can be accompanied by RKER 15 (drive error).
11	RK05 Disk on Line (RK05) - Always set, to identify the selected disk drive as RK05.
12	Drive Power Low (DPL) - Sets when an attempt is made to initiate a new function, or if a function is actively in process when the control senses a loss of power to one of the disk drives. Can be accompanied by RKER 15 (drive error). Reset by a BUS INIT or a control reset function.
13-15	Identification of Drive (ID) - If an interrupt occurs as the result of a hardware poll operation, these bits will contain the binary representation of the logical drive number that caused the interrupt.

Error Register (RKER)

Address = 177402

NOTE
This is a read-only register.



CP-3138

Bit Definitions

Bit	Function
00	Write Check Error (WCE) - Indicates that an error was encountered during a write check function as a result of a faulty bit comparison between disk data and memory data. Clears upon the initiation of a new function. This is a soft error condition.
01	Checksum Error (CSE) - Sets while performing a read function as a result of a faulty recalculation of the checksum. Cleared upon the initiation of any new function. This is a soft error condition.
02-04	Unused.

The remaining bits of the RKER are all hard errors, and are cleared only by a BUS INIT or a control reset function.

Bit Definitions

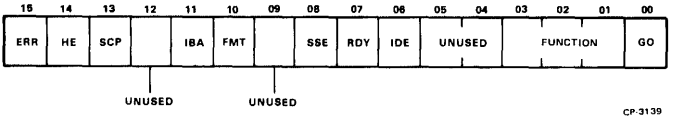
Bit	Function
05	Nonexistent Sector (NXS) - Indicates that an attempt was made to a sector address greater than 13_8.
06	Nonexistent Cylinder (NXC) - Indicates that an attempt was made to initiate a transfer to a cylinder address greater than 312_8.
07	Nonexistent Disk (NXD) - Indicates that an attempt was made to initiate a function on a nonexistent drive.
08	Timing Error (TE) - Indicates that a loss of timing pulses for at least 5 μs has been detected.

Bit Definitions (Cont)

Bit	Function
09	Data Late (DLT) - Sets during a write or write check function when the multibuffer file is empty and the operation is not yet complete. Sets during a read function when the multibuffer file is filled and the operation is not yet complete.
10	Nonexistent Memory (NXM) - Sets if memory does not respond with a RPLY within 20 μs of the time when the RKV11-D becomes bus master during a DMA sequence. Because of the speed of the RK05 disk drive, it is possible that NXM will be accompanied by RKER 09 (data late).
11	Programming Error (PGE) - Indicates that RKCS 10 (format) was set while initiating a function other than read or write.
12	Seek Error (SKE) - Sets if the disk head mechanism is not properly positioned while executing a normal read, write, read check, or write check function. The control checks 16 times before flagging this error. A simple jumper change will force the control to check just once.
13	Write Lockout Violation (WLO) - Sets if an attempt is made to write on a disk that is currently write protected.
14	Overrun (OVR) - Indicates that during a read, write, read check, or write check function, operations on sector 13_8, surface 1 of cylinder address 312_8 were finished, and the RKWC has not yet overflowed. This is essentially an attempt to overflow out of a disk drive.
15	Drive Error (DRE) - Sets if a function is either initiated or in process, and a. one of the drives in the system senses a loss of either ac or dc power; or b. the selected drive is not ready, or is in some error condition.

Control Status Register (RKCS)

Address = 177404



Bit Definitions

Bit **Function**

00 Go - This bit can be loaded by the operator and causes the control to carry out the function contained in bits 01-03 of the RKCS (functions). Remains set until the control actually begins to respond to go, which may take from 1 μs to 3.3 ms, depending on the current operation of the selected disk drive (to protect the format structure of the sector). Write only.

01-03 Function - The function register, or function bits, are loaded with the binary representation of the function to be performed by the control when a GO command is initiated. These bits are loaded by the program and cleared by BUS INIT. Read/write. The binary codings are as follows.

Bit 3	Bit 2	Bit 1	Operation
0	0	0	Control Reset
0	0	1	Write
0	1	0	Read
0	1	1	Write Check
1	0	0	Seek
1	0	1	Read Check
1	1	0	Drive Reset
1	1	1	Write Lock

04, 05 Unused. The RK11-D uses these bits. Since the PDP-11/03 bus structure has no provision for extended addressing, no connection is made to the bus from these bits on the RKV11-D. They will respond as two unused read/write bits in the status register; but, like the RK11-D they, will increment should the RKBA overflow.

Bit Definitions (Cont)

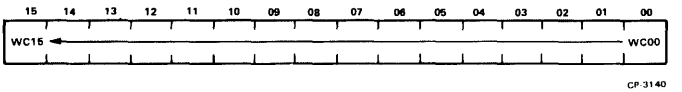
Bit	Function
06	Interrupt on Done Enable (IDE) - When set causes the control to issue a bus request and interrupt to vector address 220 if: a. a function has completed activity b. a hard error is encountered c. a soft error is encountered and bit 08 of the RKCS (SSE) is set d. RKCS 07 (RDY) is set and go is not set. Read/write.
07	Control Ready (RDY) - Indicates that the control is ready to perform a function. Set by INIT, a hard error condition, or by the termination of a function. Cleared by go being set. Read only.
08	Stop on Soft Error (SSE) - If a soft error is encountered when this bit is set: a. all control action will stop at the end of the current sector if RKCS 06 (IDE) is reset, or b. all control action will stop and a bus request will occur at the end of the current sector if RKCS 06 (IDE) is set. Read/write
09	Unused.
10	Format (FMT) - FMT is under program control, and must be used only in conjunction with normal read and write functions. Used to format a new disk pack or to reformat any sector erased due to control or drive failure. Alters the normal write operation, under which the header is rewritten each time the associated sector is rewritten, in that the head position is not checked for proper positioning before the write. Alters the normal read operation in that only one word, the header word, is transferred to memory per sector. For example, a three-word read function in format mode will transfer header words from three consecutive sectors to three consecutive memory locations for software checking. Read/write.
11	Inhibit Incrementing the RKBA (IBA) - Inhibits the RKBA from incrementing during a normal transfer function. This allows data transfers to occur to or from the same memory location throughout the entire transfer operation. Read/write.
12	Unused.

Bit Definitions (Cont)

Bit	Function
13	Search Complete (SCP) - Indicates that the previous interrupt was the result of some seek or drive reset function. Cleared at the initiation of any new function. Read only.
14	Hard Error (HE) - Sets when any of RKER 05-15 are set. Stops all control action, and processor reaction is dictated by RKCS 06 (IDE), until cleared, along with RKER 05-15, by INIT or a control reset function. Read only.
15	Error (ERR) - Sets when any bit of the RKER sets. Processor reaction is dictated by RKCS 06 and RKCS 08 (IDE and SSE). Cleared if all bits in the RKER are cleared. Read only.

Word Count Register (RKWC)

Address = 177406

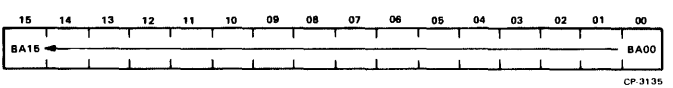


Bit Definition

Bit	Function
00-15	WC00-WC15 - The bits in this register contain the 2's complement of words to be affected or transferred by a given function. The register increments by 1 after each word transfer. When the register overflows (all WC bits go to 0), the transfer is complete and RKV11-D operation is terminated at the end of the present disk sector. However, only the number of words specified in the RKWC are transferred. Read/write.

Current Bus Address Register (RKBA)

Address = 177410

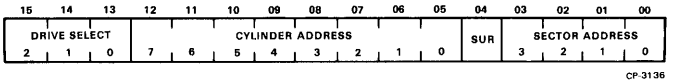


Bit Definition

Bit	Function
00-15	BA00-BA15 - The bits in this register contain the bus address to or from which data will be transferred. The register is incremented by two at the end of each transfer. Read/write.

Disk Address Register (RKDA)

Address = 177412



NOTE

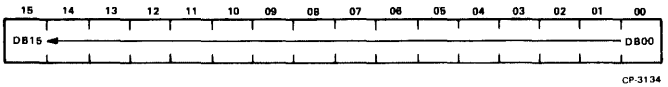
This register will not respond to commands while the controller is busy. Therefore, RKDA bits are loaded from the bus data lines only in the control ready (RDY – bit 07 of the RKCS) state, and are cleared by BUS INIT and control reset. The RKDA is incremented automatically at the end of each disk sector.

Bit Definitions

Bit	Function
00-03	Sector Address (SA) - Binary representation of the disk sector to be addressed for the next function. The largest valid address (or number) for the sector address is 13_8.
04	Surface (SUR) - When set, enables the lower disk head so that operation is performed on the lower surface; when reset, enables the upper disk head.
05-12	Cylinder Address (CYL ADDR) - Binary representation of the cylinder address currently being selected. The largest valid address or number for the cylinder address is 312 .
13-15	Drive Select (DR SEL) - Binary representation of the logical drive number currently being selected.

Data Buffer Register (RKDB)

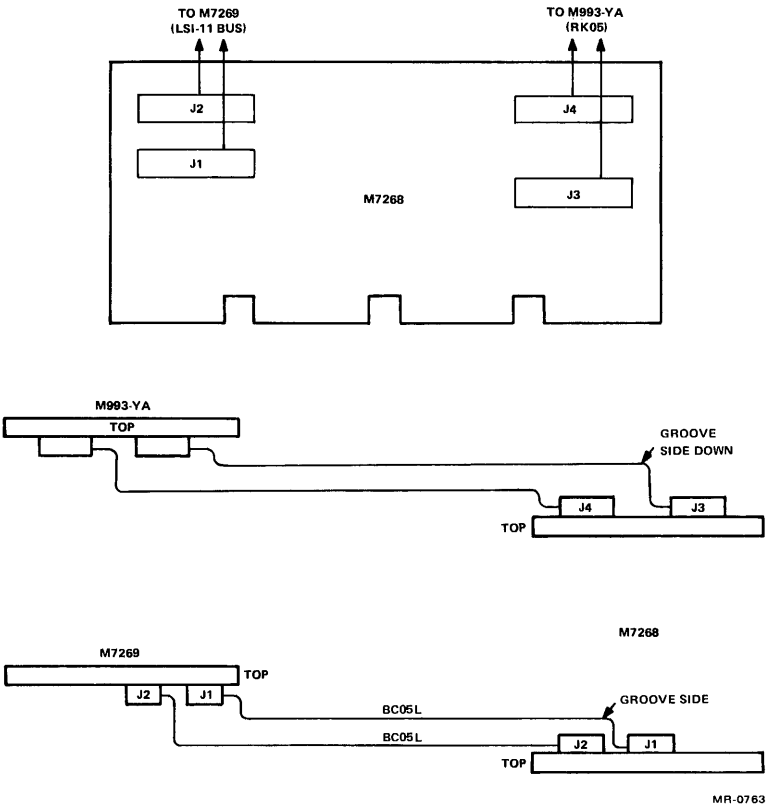
Address = 177416



Bit Definition

Bit	Function
00-15	DB00-DB15 - The bits of this register work as a general data handler in that all information transferred between the control and the disk drive must pass through this register. Loaded from the bus only while the RKV11-D is bus master during a DMA sequence. Read only.

NOTE
Address 177414 is unused.



RKV11-D Cable Connection

M7270
LSI-11/2 PROCESSOR MODEL DESIGNATIONS

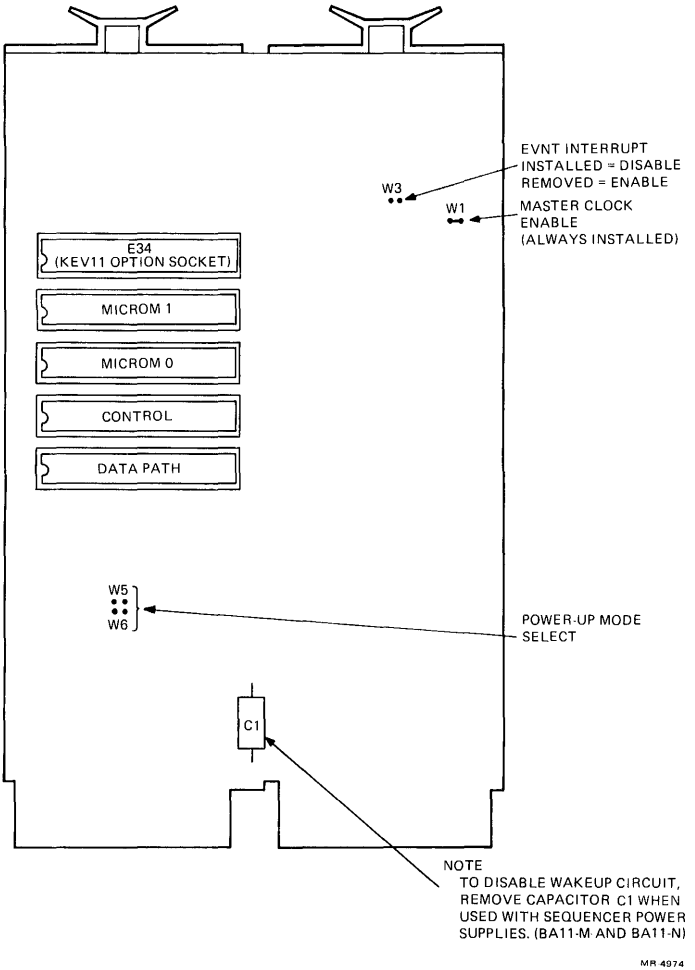
KD11-HA	Dual-height LSI-11 processor without memory	
KD11-HB	KD11-HA + MSV11-DB 8K word memory	
KD11-HC	KD11-HA + MSV11-DC 16K word memory	
KD11-HD	KD11-HA + MSV11-DD 32K word memory	
KD11-HF	KD11-HA + MSV11-DA 4K word memory	
KD11-HJ	KD11-HA + MMV11-A 4K word core memory	
KD11-HU	KD11-HA + MRV11-BA	
KD11-XA	KD11-HA, 2 MSV11-ED 64K word memory	(Heathkit)
KD11-XB	KD11-HA, 4 MSV11-ED 128K word memory	(Heathkit)
KD11-XC	KD11-HA, 9 MSV11-ED 288K word memory	(Heathkit)
KD11-XD	KD11-HA, 3 MSV11-DD	(Heathkit)
KD11-XH	KD11-HA, 3 MSV11-DC	(Heathkit)
KD11-XJ	KD11-HA, 3 MSV11-DB	(Heathkit)

M7270 Specifications

Size:	Double-height module
Dimensions:	13.34 cm (5.25 in) × 22.8 cm (8.9 in)
Power:	+5 Vdc ±5%, 1 A + 12 Vdc ± 5%, .22 A
Bus Loads:	AC - 1.7 unit loads DC - 1 unit load

Related Documentation

Microcomputer Processor Handbook (EB-18451-20)
KD11-HA Print Set (MP-00495)
LSI-11 Maintenance Card (EK-LSI11-MC)



M7270 Jumpers and Socket Locations

Jumper

W1 Always installed - master clock enabled.

W3 Removed - external event interrupt (line clock) enabled.
Installed - external event interrupt disabled.

W6	W5	Mode Selected
R*	R	PC at 24 and PS at 26, or halt mode (mode 0).
R	R	ODT microcode (mode 1).
I	R	PC at 173000 for user bootstrap (mode 2).
I	I	Special processor microcode; not implemented (mode 3).

Diagnostic Programs
The following diagnostic programs are for use with LSI-11 processors except for the limitations noted.

VKAA?? LSI-11 basic instruction test.

VKAB?? LSI-11 Extended Instruction Set (EIS) test. This program can be run only on LSI-11 CPUs with the KEV11 (EIS/FIS) or KEV11-CA (DIBOL instruction set) options installed.

VKAC?? LSI-11 Floating Point Instruction (FIS) test. This runs only on LSI-11 CPUs that have the KEV11 (EIS/FIS) option (23-00385).

VKAD?? LSI-11 traps test. This diagnostic auto-sizes for the EIS, FIS, and DIBOL options.

a. Older versions (Rev B1 and below) require the setting of a bit in the software switch register if EIS, FIS, or DIBOL is present.

b. Rev A diagnostics will not run on D322 or D324 systems because of the DIS instructions.

NOTE
See Appendix A for XXDP+ multimedia assignments.

VKAH?? Basic system exerciser. Tests serial line unit, memory, processor, EIS/FIS, clock, and both floppy disks under various conditions. Software switch register must be set for options.

*R = jumper removed; I = jumper installed.

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1611 B-39	21-11549-01	−3.9	
		21-15579-00	−3.5	With ECO 6
CONTROL	CP 1621 B-173	23-002C4	−3.9	2007 pattern
MICROM-0	CP 1631 B-103	23-001B5	−3.9	
MICROM-1	CP 1631 B-073	23-002B5	−3.9	
EIS/FIS (if present) KEV11-A	CP 1631 B-135	23-003B5	−3.9	

ECOs for Etch Rev E

CS Rev	ECO No.	Change
A	1	1. Remove blanking pulse. 2. Generate clock driver V_{cc} from +12 V. 3. Move K1 MSTB L from E34-3 to E34-4. 4. Relayout board.
B	2	Change C31 and C32 from 10-12312-01 to 10- 10279-0.
C	3	Change Augat socket to Burndy socket.
F	3A	Allow customer to remove C81.
H	4	Change R18 from 13-10317 to 13-10522.
J	5	Alternate part 19-14282-01 may be used to replace E37.
K	6	Change part E30 from 21-11549-01 to 21-15579-00.

M7940
DLV11 SERIAL LINE UNIT

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.0	0.18	2.48	1	BC05M for 20 mA
(1.6 max.)	(0.25 max.)			BC05C for Bell 103 modem and EIA
				BC05C plus H312A or H308 for EIA terminal

Standard Addresses

	Console	Second Terminal	Modem (Auto Mode)
RCSR	177560	176500	175610
RBUF	177562	176502	175612
XCSR	177564	176504	175614
XBUF	177566	176506	175616

Vectors

	Console	Second Terminal	Modem
Receiver Interrupt	60	300	300
Transmitter Interrupt	64	304	304

Diagnostic Program

Refer to Appendix A.

NOTE

The DECX module DLA? requires a wraparound connector to run. The connector is not available and must be made up from the following parts:

Berg connector	**PN 12-10918-15**
Berg pins	**PN 12-10089-07**
No. 22 AWG wire	**PN 90-07350-00.**

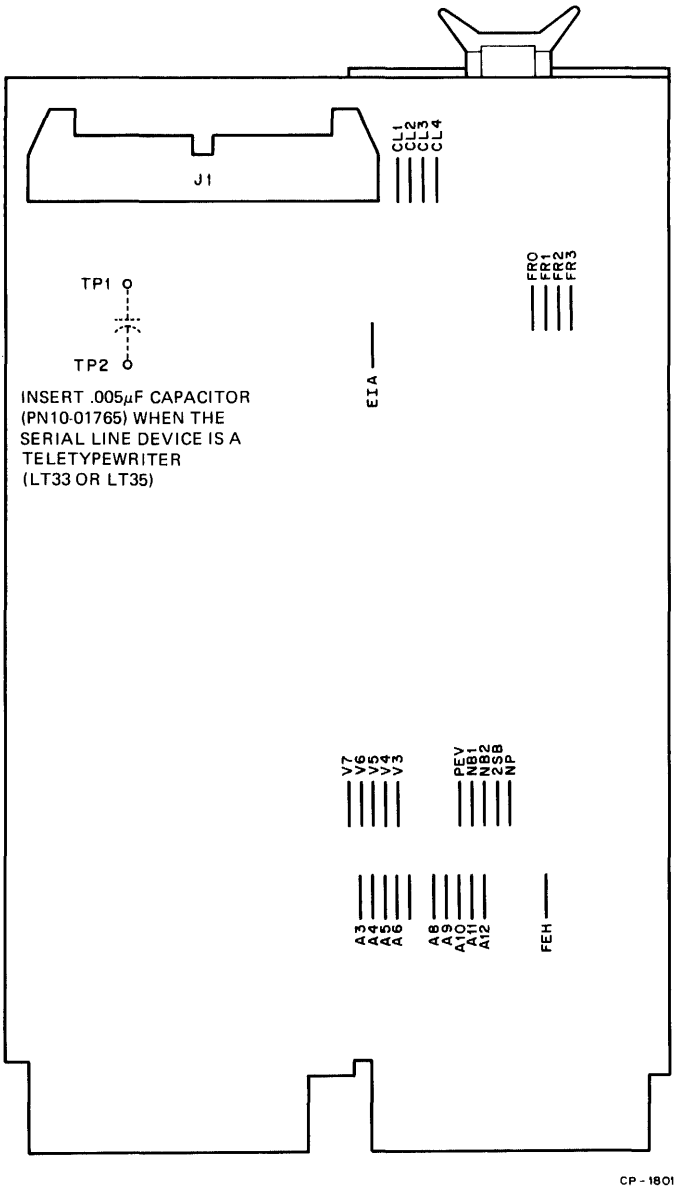
Connect the following pins:

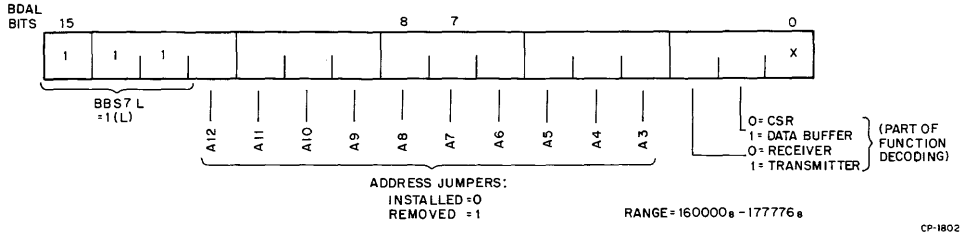
F to J
M to E

Related Documentation

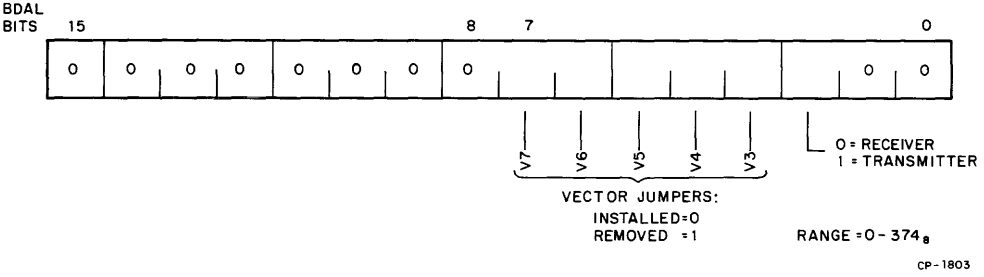
Field Maintenance Print Set (MP00055)
Microcomputer Interfaces Handbook (EB-20175-20)

M7940


J1
CL1
CL2
CL3
CL4
TP1
TP2
INSERT .005μF CAPACITOR
(PN10-01765) WHEN THE
SERIAL LINE DEVICE IS A
TELETYPEWRITER
(LT33 OR LT35)
EIA
FR0
FR1
FR2
FR3
V7
V6
V5
V4
V3
PEV
NB1
NB2
2SB
NP
A3
A4
A5
A6
A8
A9
A10
A11
A12
FEH
CP-1801



DLV11 Address Bits



DLV11 Interrupt Vector Bits

DLV11 SLU Factory Jumper Configuration

Jumper Designation	Jumper Status	Function
A3	I	This arrangement of jumpers A3 through A12 implements the octal device address 17756X, which is the assigned address for the console device SLU. The least significant digit is hardwired on the module to address the four SLU device registers as follows: X = 0, RCSR address X = 2, Receive data register address X = 4, XCSR address X = 6, Transmit data register address.
A4	R	
A5	R	
A6	R	
A7	I	
A8	R	
A9	R	
A10	R	
A11	R	
A12	R	
V3	I	This jumper arrangement implements the interrupt vector addresses 60 for received data and 64 for transmitted data.
V4	R	
V5	R	
V6	I	
V7	I	
NP	R	No parity.
2SB	R	Two stop bits (installed on D322 and D324).
NB2	R	Eight data bits.
NB1	R	
PEV	R	Even parity if NP installed.
FEH	I	Halt on framing error (removed on D322 and D324).
EIA	R	12 V EIA operation disabled (installed on D322 and D324).
FR0	R	
FR1	R	110 baud rate selected.
FR2	R	
FR3	R	
CL1	I	20 mA current loop active receiver and transmitter selected.
CL2	I	
CL3	I	
CL4	I	

Number of Data Bits

	NB1	NB2
5	Installed	Installed
6	Removed	Installed
7	Installed	Removed
8	Removed	Removed

Number of Stop Bits Transmitted

2SB installed = one stop bit.
2SB removed = two stop bits.

Parity Transmitted

NP removed = no parity bit.
NP and PEV installed = odd parity.
NP installed and PEV removed = even parity.

Framing Error

FEH installed = halt on framing error (console).
FEH removed = do not halt on framing error.

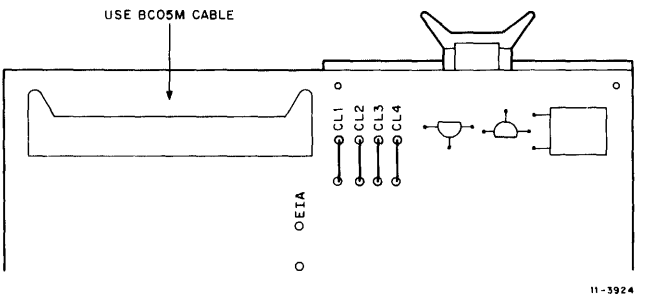
Unit	Address	Address Jumpers									
		A12	A11	A10	A9	A8	A7	A6	A5	A4	A3
Console	177560	R	R	R	R	R	I	R	R	R	I
First Option	176500	R	R	R	I	R	I	R	I	I	I
Second Option	176510	R	R	R	I	R	I	R	I	I	R
Third Option	176520	R	R	R	I	R	I	R	I	R	I
Modem	175610	R	R	I	R	R	R	I	I	I	R

Unit	Vector	Vector Jumpers				
		V7	V6	V5	V4	V3
Console	60	I	I	R	R	I
First Option	300	R	R	I	I	I
Second Option	310	R	R	I	I	R
Third Option	320	R	R	I	R	I
Modem	300	R	R	I	I	I

Baud Rate Selection

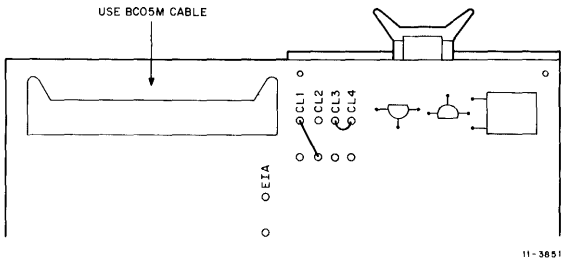
Baud Rate	FR3	FR2	FR1	FR0
50	I	I	R	I
75	I	I	R	R
110	R	R	R	R
134.5	I	R	I	I
150	R	R	R	I
200	I	R	I	R
300	R	R	I	R
600	I	R	R	I
1200	R	I	R	R
1800	R	I	R	I
*2400	I	R	R	R
*2400	R	R	I	I
4800	R	I	I	R
9600	R	I	I	I

*Either configuration may be used. Use second configuration for D322 and D324.



Active transmit = CL3 and CL4 installed.
Active receive = CL1 and CL2 installed.

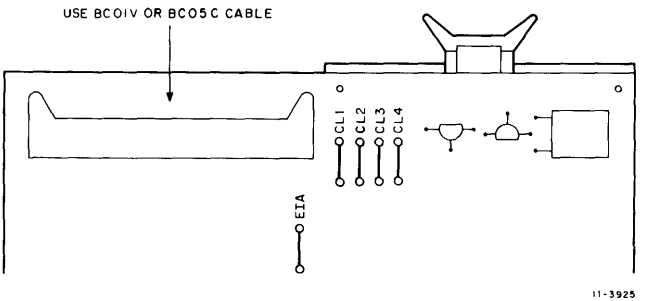
NOTE
CL2 and CL3 are 180 Ω resistors.



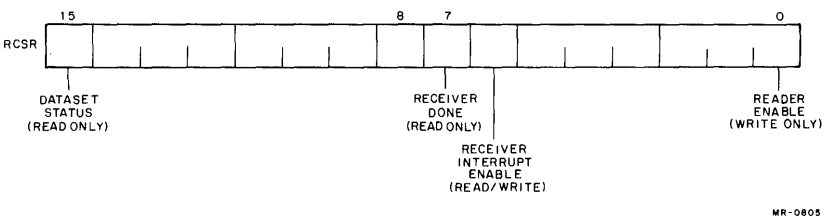
Passive transmit = CL3 and CL4 as in preceding figure.
Passive receive = CL1 and CL2 as in preceding figure.

NOTE

When configured for passive operation, the (+) and (−) lines are reversed. Use a BC05F cable.



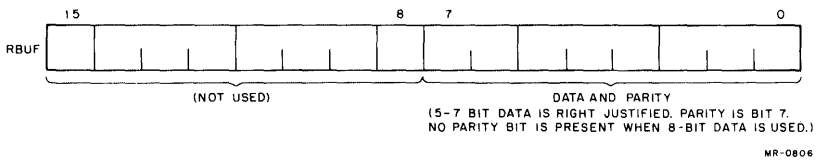
Jumper EIA must be inserted for EIA operation. Jumpers CL1 through CL4 do not have to be removed when EIA is inserted.



Receiver Control/Status Register (RCSR)

RCSR Bit Definitions

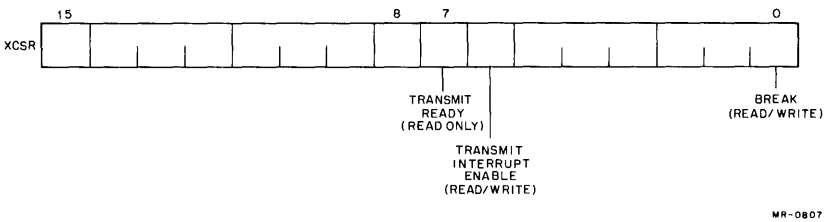
Bit	Function
15	Dataset Status - Set when CARRIER or CLEAR TO SEND and DATA SET READY signals are asserted by an EIA device. Read-only.
14-08	Not used. Read as 0.
07	Receiver Done - Set when an entire character has been received and is ready for input to the processor. This bit is automatically cleared when RBUF is addressed or when the BDCOK H signal goes false (low). A receiver interrupt is enabled by the DLV11 when this bit is set and receiver interrupt is enabled (bit 6 is also set). Read-only.
06	Interrupt Enable - Set under program control when it is desired to generate a receiver interrupt request when a character is ready for input to the processor (bit 7 is set). Cleared under program control or by the BINIT signal. Read/write.
05-01	Not used. Read as 0.
00	Read Enable - Set by program control to advance the paper tape reader on a teletypewriter device to input a new character. Automatically cleared by the new character's start bit. Write only.



Receiver Buffer Register (RBUF)

RBUF Bit Definitions

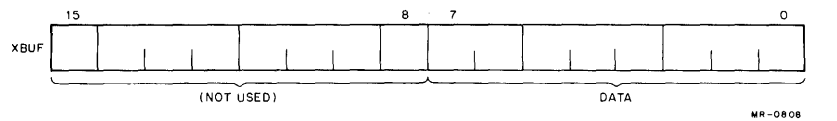
Bit	Function
15-08	Not used. Read as 0.
07-00	Contains five to eight data bits in a right-justified format. MSB is the optional parity bit. Read only.



Transmitter Control/Status Register (XCSR)

XCRS Bit Definitions

Bit	Function
15-08	Not used. Read as 0.
07	Transmit Ready - Set when XBUF is empty and can accept another character for transmission. It is also set during the power-up sequence by the BDCOK H signal. Automatically cleared when XBUF is loaded. When transmitter interrupt is enabled (bit 6 also set), an interrupt request is asserted by the DLV11 when this bit is set. Read only.
06	Interrupt Enable - Set under program control when it is desired to generate a transmitter interrupt request when the DLV11 is ready to accept a character for transmission. Reset under program control or by the BINIT signal. Read/write.
05-01	Not used. Read as 0.
00	Break - Set or reset under program control. When set, a continuous space level is transmitted. BINIT reset this bit. Read/write.



Transmitter Buffer Register (XBUF)

XBUF Bit Definitions

Bit	Function
15-08	Not used.
07-00	Continuous five to eight right-justified data bits. Loaded under program control for serial transmission to a device. Write only.

M7941
DRV11 PARALLEL LINE UNIT

Amps		Bus Loads		Cables
+5	+12	AC	DC	
0.9	0	2.80	1.0	(2) BC07D
(1.6 max.)				(2) BC08R

Standard Addresses

	First Device	Second Device	MINC/ DECLAB
DRCSR	167770	167760	171770
DROUTBUF	167772	167762	171772
DRINBUF	167774	167764	171774

Vectors

Interrupt A	300	310	370
Interrupt B	304	314	374

Diagnostic Programs

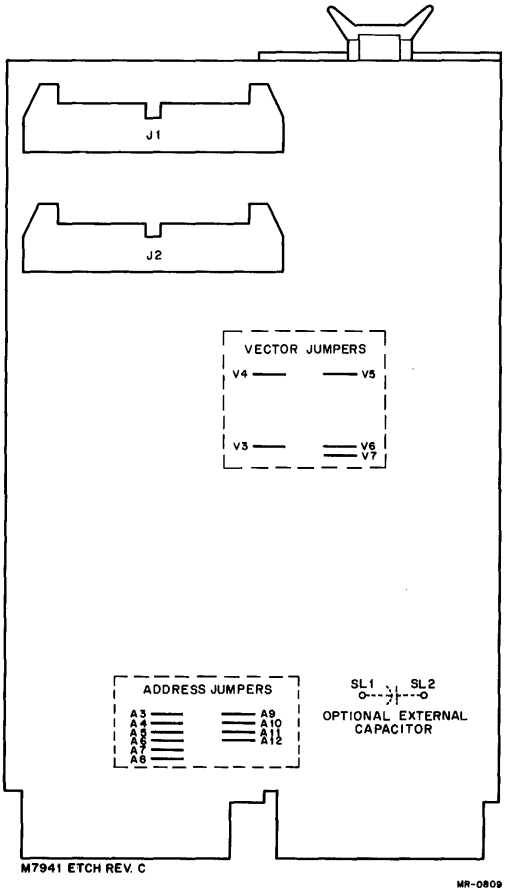
Refer to Appendix A.

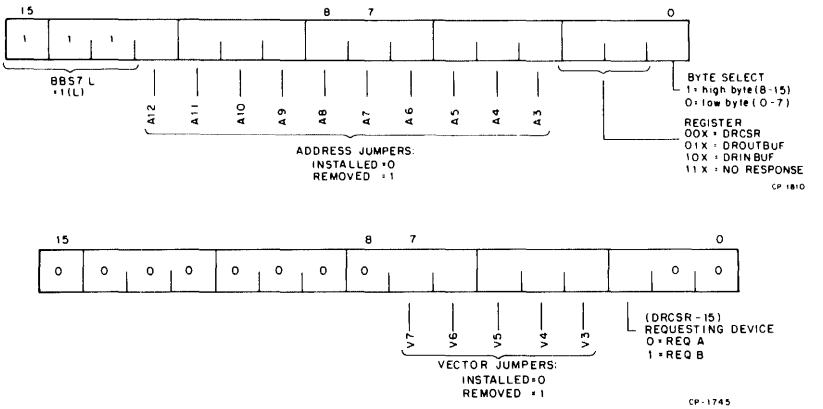
NOTE

Full testing requires a BC08-R wraparound cable for VKAF?? and DRA?.

Related Documentation

ADV11-A, KWV11-A, AAV11-A, DRV11 User's Manual (EK-ADV11-OP)
Field Maintenance Print Set (MP00054)
Microcomputer Interfaces Handbook (EB-20175-20)


J1
J2
VECTOR JUMPERS
V4
V5
V3
V6
V7
ADDRESS JUMPERS
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
SL1
SL2
OPTIONAL EXTERNAL CAPACITOR
M7941 ETCH REV. C
MR-0809



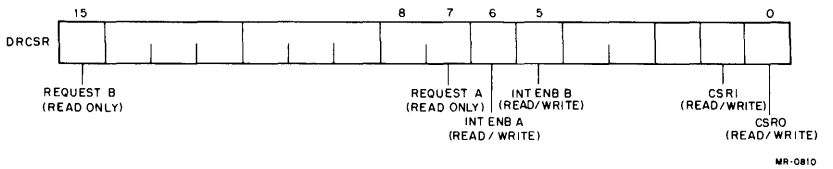
DRV11 PLU Factory Jumper Configuration

Jumper Designation	Jumper State	Function
A3	R	This arrangement of jumpers A3 through A12 assigns the device address 16777X to the PLU. This address is the starting address of a reserved block in memory bank 7 which is recommended for user device address assignments. The least significant digit X is hardwired on the module to implement the three PLU device addresses as follows: X = 0, DRCSR address X = 2, Output buffer address X = 4, Input buffer address.
A4	R	
A5	R	
A6	R	
A7	R	
A8	R	
A9	R	
A10	R	
A11	I	
A12	I	
V3	I	This factory-installed jumper configuration implements the two interrupt vector addresses 300 and 304 for use as defined by application requirements.
V4	I	
V5	I	
V6	R	
V7	R	
SL1	R	These jumper posts are provided for the installation of an external capacitor.
SL2	R	

External Capacitor
The pulse width of NEW DATA READY and DATA TRANSMITTED may be modified by installing an external capacitor. Note that the trailing edge of one of these two pulses **must** be used to clear interrupt requests.

Capacitor (μF)	Pulse Width (ns)
None (as shipped)	350
.0047	750
.01	1550
.02	2330
.03	3150

NOTE
Any system containing a REV11 and a DRV11 that has a capacitor to extend NEW DATA READY and DATA TRANSMITTED greater than 1800 ns may cause the REV11 to hang the system unless the REV11 is at ECO 5 level or greater (Circuit Schematic Rev K).



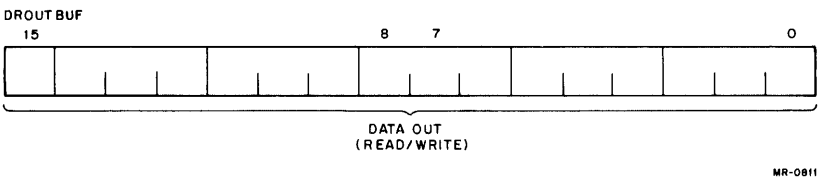
Control/Status Register

DRCSR Bit Definitions

Bit	Function
15	REQUEST B - This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program.
14-08	Not used. Read as 0.
07	REQUEST A - Performs the same function as REQUEST B (bit 15) except that an interrupt is generated only if INT ENB A (bit 06) is also set. When the maintenance cable is used, the state of REQUEST A is identical to that of CSR0 (bit 00). Cleared by INIT when in maintenance mode. Read-only.

DRCSR Bit Definitions (Cont)

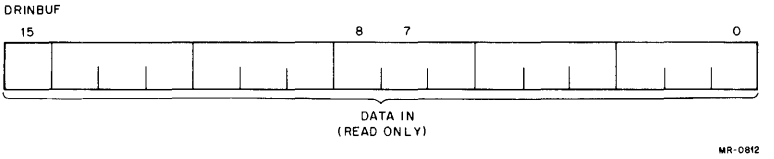
Bit	Function
06	INT ENB A - Interrupt enable bit. When set, allows an interrupt request to be generated, provided REQUEST A (bit 07) becomes set.
05	INT ENB B - Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST B (bit 15) becomes set.
04-02	Not used. Read as 0. Can be loaded or read by the program. Cleared by INIT. Read/write.
01	CSR1 - This bit can be loaded or read (under program control) and can be used for a user-defined command to the device (appears only on connector no. 1). When the maintenance cable is used, setting or clearing this bit causes an identical state in bit 15 (REQUEST B). This permits checking operation of bit 15 which cannot be loaded by the program. Can be loaded or read by the program. Cleared by INIT. Read/write.
00	CSR0 - Performs the same functions as CSR1 (bit 01) but appears only on connector no. 2. When the maintenance cable is used, the state of this bit controls the state of bit 07 (REQUEST A). Cleared by INIT. Read/write.



Output Data Buffer Register (DROUTBUF)

DROUTBUF Bits 15-00
Output Data Buffer - Contains a full 16-bit word or one or two 8-bit bytes: high byte = 15-8; low byte = 7-0.

Loading is accomplished under a program-controlled DATO or DATOB bus cycle. It can be read under a program-controlled DATI cycle.



Input Data Buffer Register (DRINBUF)

DRINBUF Bits 15–00
Input Data Buffer - Contains a full 16-bit word or one or two 8-bit bytes. The entire 16-bit word is read under a program-controlled DATI bus cycle.

M7942
MRV11-AA READ-ONLY MEMORY

Amps			Bus Loads		Cables
	+5	−12	AC	DC	
W/O PROMs (0.6 max.)	0.4	0	1.84	1.0	none
With PROMs (4.1 max.)	2.8	0			

Standard Addresses

Module is shipped with all jumpers installed, selecting bank 0 addresses (0-1777).

Vectors, Diagnostic Program, Exerciser Program

None

Related Documentation

Field Maintenance Print Set (MP00066)
Microcomputer Processor Handbook (EB-18451-20)

NOTES

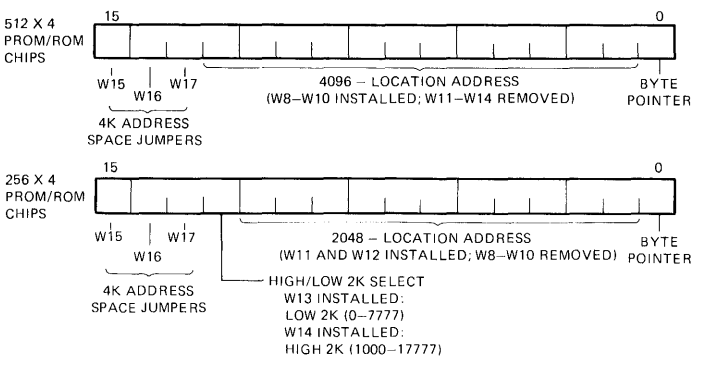
1. **Jumpers W8–W14 select chip set types (512 or 256).**
2. **Any row not populated with PROMs must have the BRPLY L jumper (W0–W7) removed.**

MRV11-AA Address Word Formats

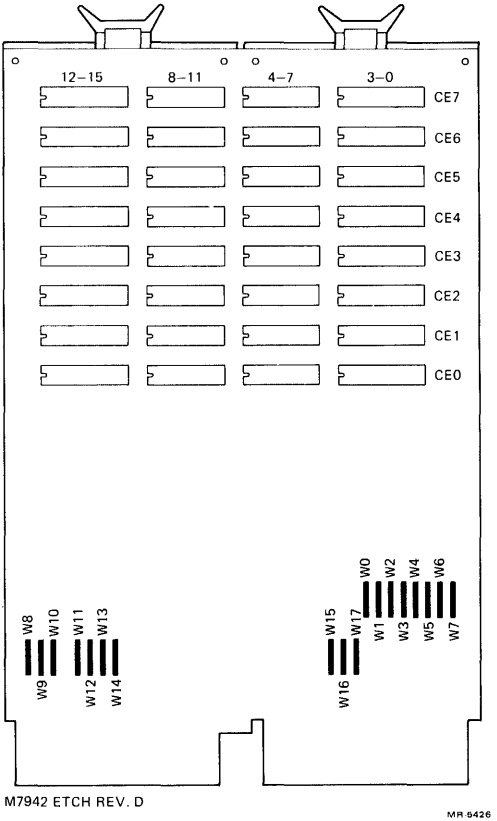
Bank Select			
Bank	**W15**	**W16**	**W17**
0	I	I	I
1	I	I	R
2	I	R	I
3	I	R	R
4	R	I	I
5	R	I	R
6	R	R	I
7	R	R	R

NOTE

Because of addressing limitations, this module is not compatible with PDP-11/23 systems with more than 64K bytes of memory.



MRV11-A Address Word Format



M7942 Etch Rev D

512 by 4-Bit PROM Addresses

Bank Address Jumpers			Word/Byte Address	Physical Row	BRPLY L Jumper
W15	W16	W17			
I	I	I	0-1777	CE0	W0
I	I	R	2000-3777	CE1	W1
I	R	I	4000-5777	CE2	W2
I	R	R	6000-7777	CE3	W3
R	I	I	10000-11777	CE4	W4
R	I	R	12000-13777	CE5	W5
R	R	I	14000-15777	CE6	W6
R	R	R	16000-17777	CE7	W7

256 by 4-Bit ROM Addresses

Bank Address Jumpers			Word/Byte Address			
W15	W16	W17	W13 Installed W14 Removed	W13 Removed W14 Installed	Physical Row	BRPLY L Jumper
I	I	I	0-7776	100000-107776	CE0	W0
I	I	R	10000-17776	110000-117776	CE2	W2
I	R	I	20000-27776	120000-127776	CE4	W4
I	R	R	30000-37776	130000-137776	CE6	W6
R	I	I	40000-47776	140000-147776	CE1	W1
R	I	R	50000-57776	150000-157776	CE3	W3
R	R	I	60000-67776	160000-167776	CE5	25
R	R	R	70000-77776	170000-177776	CE7	W7

BRPLYL Select

Empty Row	Remove Jumper
CE0	W0
CE1	W1
CE2	W2
CE3	W3
CE4	W4
CE5	W5
CE6	W6
CE7	W7

M7944
MSV11-B READ/WRITE MEMORY

Amps		Bus Loads		Cables
+5	+12	AC	DC	
0.6	0.3	1.89	1.0	none
(1.12 max.)	(0.7 max.)			

Standard Addresses

Module is shipped with all jumpers installed, selecting bank 0 (0-17776).

Vectors, DEC/X11 Exerciser Program

None

Diagnostic Programs

Refer to Appendix A.

Related Documentation

Field Maintenance Print Set (MP00067)
Microcomputer Processor Handbook (EB-18451-20)

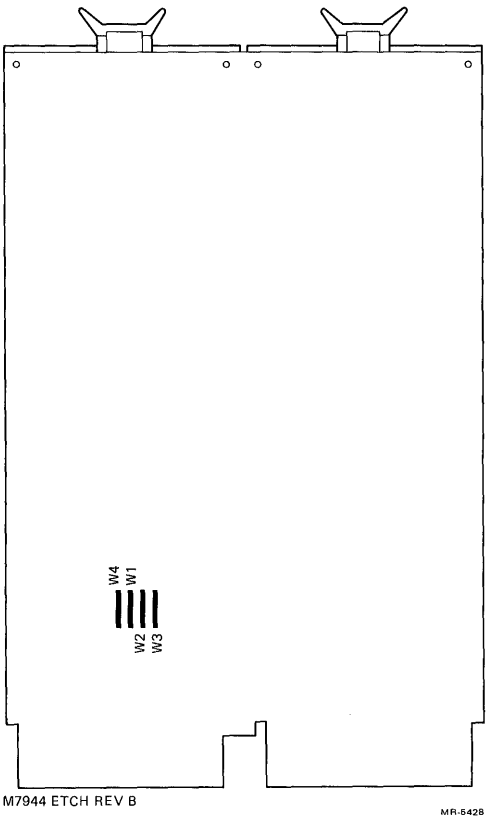
NOTES

1. **Only one dynamic memory module in a system is needed to reply to the refresh bus functions initiated by the processor. The module selected should be the one with the longest access time (usually the module electrically farthest from the refreshing device).**

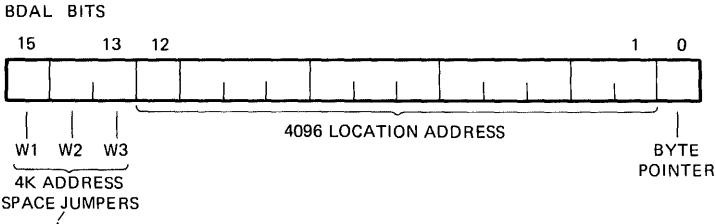
NOTES (Cont)

2. **If a REV11 (M9400YA or YC) provides refresh, only the processor-resident memory (if present) should reply to refresh. If the processor board has no resident memory, the memory module electrically farthest from the REV11 should reply.**

3. **Refer to the Refresh Configuration Procedures in the "Systems Configurations" section.**



M7944 Etch Rev B



W1	W2	W3	Bank No.	Address Range	Octal Address Range
I	I	I	0	0-4K	000000-017776
I	I	R	1	4-8K	020000-037776
I	R	I	2	8-12K	040000-057776
I	R	R	3	12-16K	060000-077776
R	I	I	4	16-20K	100000-117776
R	I	R	5	20-24K	120000-137776
R	R	I	6	24-28K	140000-157776
R	R	R	7	28-32K	160000-177776

NOTE: I = Installed, R = Removed

MR-5429

MSV11-B Address Format/Jumpers

NOTE

Because of addressing limitations, this module is not compatible with PDP-11/23 systems with more than 64K bytes of memory.

MSV11-B Address Format/Jumpers

Reply to Refresh

Function	**W4**
Reply	R
Don't reply	I

M7946
RXV11 FLOPPY DISK INTERFACE

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.5 max.	0	1.74	1	BC05L

Standard Addresses

	First Device	Second Device
RXCS	177170	177150
RXDB	177172	177152
Vector	264	270

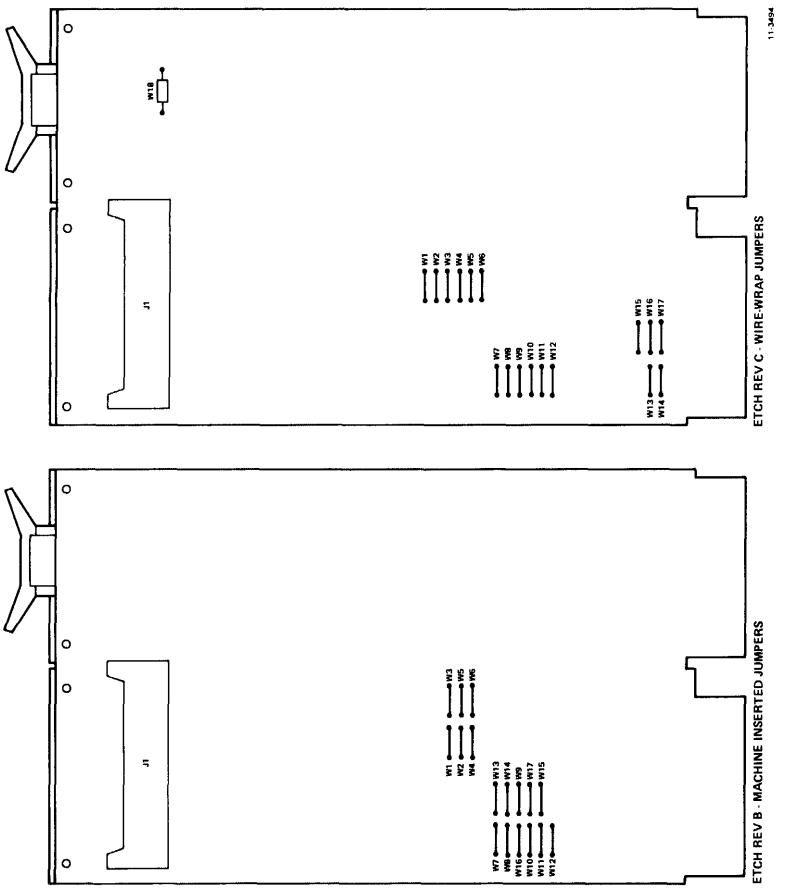
Diagnostic Programs

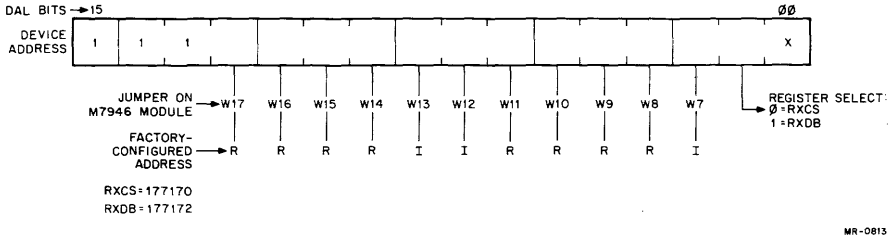
Refer to Appendix A.

NOTE
Run DZRXB before DZRXA.

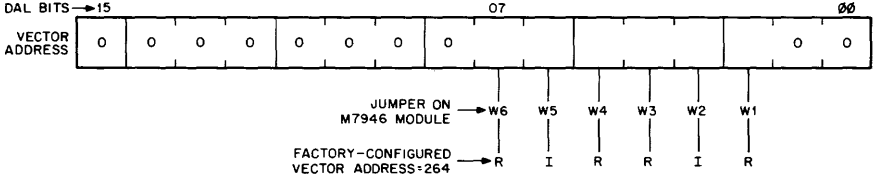
Related Documentation

RXV11 User's Manual (EK-RXV11-OP-001)
Field Maintenance Print Set (MP00024)
Microcomputer Interfaces Handbook (EB-20175-20)


J1
W18
W1
W2
W3
W4
W5
W6
W7
W8
W9
W10
W11
W12
W15
W16
W17
W13
W14
ETCH REV C - WIRE-WRAP JUMPERS
11-3494
J1
W1
W2
W3
W4
W5
W6
W7
W8
W9
W10
W11
W12
W13
W14
W15
W16
W17
ETCH REV B - MACHINE INSERTED JUMPERS



Device Address



NOTE:
I = Jumper installed = Logical Ø
R = Jumper removed = Logical 1
X = Don't care

Vector Address

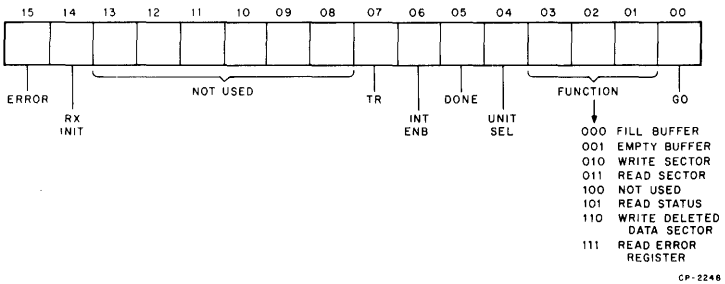
Unit	Address	Address Jumpers										
		W17	W16	W15	W14	W13	W12	W11	W10	W9	W8	W7
First (Drives 0, 1)	177170	R	R	R	R	I	I	R	R	R	R	I
Second (Drives 2, 3)	177150	R	R	R	R	I	I	R	R	I	R	I

Unit	Vector	Vector Jumpers					
		W6	W5	W4	W3	W2	W1
First (Drives 0, 1)	264	R	I	R	R	I	R
Second (Drives 2, 3)	270	R	I	R	R	R	I

NOTES

1. **When inserting the cable in the RXV11 interface module, the red edge of the cable should be at the center of the module (near the pin A end of J1).**

2. **BUS INIT – Install W18 to pass bus INIT to the RX01 as initialize.**



Receiver Control/Status Register (RCSR)

Bit Definitions

Bit	Function
0	Go - Initiates a command to RX01. Write only.
1-3	Function Select - These bits code one of the eight possible functions. Write only.
4	Unit Select - This bit selects one of the two possible disks for execution of the desired function. Write only.
5	Done - This bit indicates the completion of a function. Done will generate an interrupt when asserted if interrupt enable (RXCS bit 6) is set. Read only.
6	Interrupt Enable - This bit is set by the program to enable an interrupt when the RX01 has completed an operation (done). The condition of this bit is normally determined at the time a function is initiated. This bit is cleared by the LSI-11 bus initialize (BINIT L) signal, but it is not cleared by the RXV11 initialize bit (RXCS bit 14). Read/write.

Bit Definitions (Cont)

Bit	Function
7	Transfer Request - This bit signifies that the RXV11 needs data or has data available. Read only.
8-13	Unused.
14	RXV11 Initialize - This bit is set by the program to initialize the RXV11 without initializing all of the devices on the LSI-11 bus. Write only.

CAUTION

1. **Loading the lower byte of the RXCS will also load the upper byte of the RXCS.**

2. **Setting this bit (BIS instruction) will not clear the interrupt enable bit (RXCS bit 06).**

Upon setting this bit in the RXCS, the RXV11 will negate done and move the head position mechanism of drive 1 (if two are available) to track 0. Upon completion of a successful initialize, the RX01 will zero the error and status register, set initialize done, and set RXES bit 7 (DRV RDY) if unit 0 is ready. It will also read sector 1 of track 1 and drive 0.

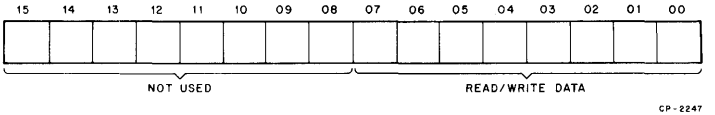
15	Error - This bit is set by the RX01 to indicate that an error has occurred during an attempt to execute a command. This read-only bit is cleared by the initiation of a new command or by setting the initialize bit. When an error is detected, the RXES is automatically read into the RXDB.

The RXDB register serves as a general purpose data path between the RX01 and the RXV11 interface. It may represent one of five RX01 registers according to the protocol of the command function in progress. The RX01 registers include RXDB, RXTA, RXSA, RXES, and RXER.

CAUTION

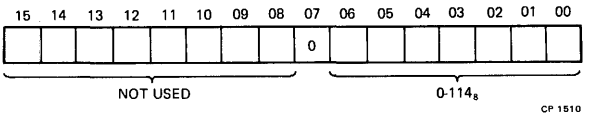
Violation of protocol in manipulation of this register may cause permanent data loss. Refer to *RXV11 User's Manual.*

RXDB-RX Data Buffer – All information transferred to and from the floppy media passes through this register and is addressable only under the protocol of the function in progress.



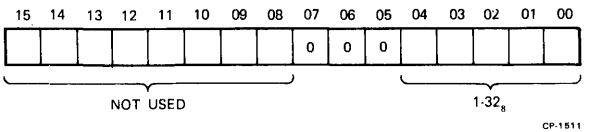
RXDB Format

RXTA-RX Track Address – This register is loaded to indicate on which of the 114 tracks a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.



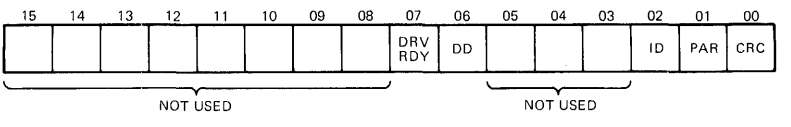
RXTA Format

RXSA-RX Sector Address – This register is loaded to indicate on which of the 32 sectors a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.



RXSA Format

RXES-RX Error and Status – This register contains the current error and status conditions of the drive selected by bit 4 (unit select) of the RXCS. This read-only register can be addressed only under the protocol of the function in progress. The RXES is located in the RXDB upon completion of a function.



RXES Format

RXDB Bit Definitions

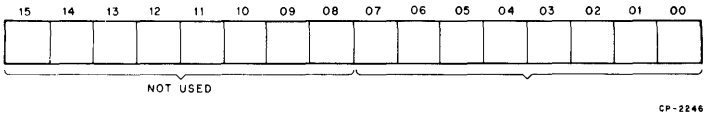
Bit	Function
0	CRC Error - A cyclic redundancy check error was detected as information was received from a data field of the diskette. The RXES is moved to the RXDB, and error and done are asserted.
1	Parity Error - A parity error was detected on command or on address information being transferred to the RX01 from the LSI-11 bus interface. A parity error indication means that there is a problem in the interface cable between the RX01 and the interface. Upon detection of a parity error, the current function is terminated; the RXES is moved to the RXDB, and the error and done are asserted.
2	Initialize Done - This bit is asserted in the RXES to indicate completion of the initialize routine, which can be caused by RX01 power failure, system power failure, or programmable or LSI-11 bus initialize.
3-5	Unused.
6	Deleted Data Detected - During data recovery, the identification mark preceding the data field was decoded as a deleted data mark.
7	Drive Ready - This bit is asserted if the unit currently selected exists, is properly supplied with power, has a diskette installed correctly, has its door closed, and has a diskette up to speed.

NOTES

1. **The drive ready bit is valid only when retrieved via a read status function or at completion of initialize when it indicates status of drive 0.**

2. **If the error bit was set in the RXCS but error bits are not set in the RXES, then specific error conditions contained in the RXER can be accessed from the RXDB via a read error register function.**

RXER-RX Error – This register is located in the RX01 and contains specific RX01 error information. This information is normally accessed when the RXCS error bit 15 is set but RXES error bits 0 and 1 are not set. This is *a* read-only register.



RXER Format

Octal Code	Error Code Meaning
0010	Drive 0 failed to see home on initialize.
0020	Drive 1 failed to see home on initialize.
0030	Found home when stepping out 10 tracks for INIT.
0040	Tried to access a track greater than 77.
0050	Home was found before desired track was reached.
0060	Self-diagnostic error.
0070	Desired sector could not be found after looking at 52 headers (two revolutions).
0110	More than 40 microseconds and no SEP clock seen.
0120	A preamble could not be found.
0130	Preamble found but no I/O mark found within allowable time span.
0140	CRC error on a header; no flag.
0150	The header track address of a good header does not compare with the desired track.
0160	Too many tries for an ID address mark.
0170	Data mark not found in allotted time.
0200	CRC error on reading the sector from the disk. No code appears in the ERREG.
0210	Parity error on some word from interface.

M7948
DRV11-P FOUNDATION MODULE

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.0	—	2.08	1.0	BC07A
Plus user's logic				BC07D
				BC08R
				BC04Z

Standard Addresses

No standard designated. Configurable within the range of 760000-777776. May conflict with DEC standard device addresses.

Vectors

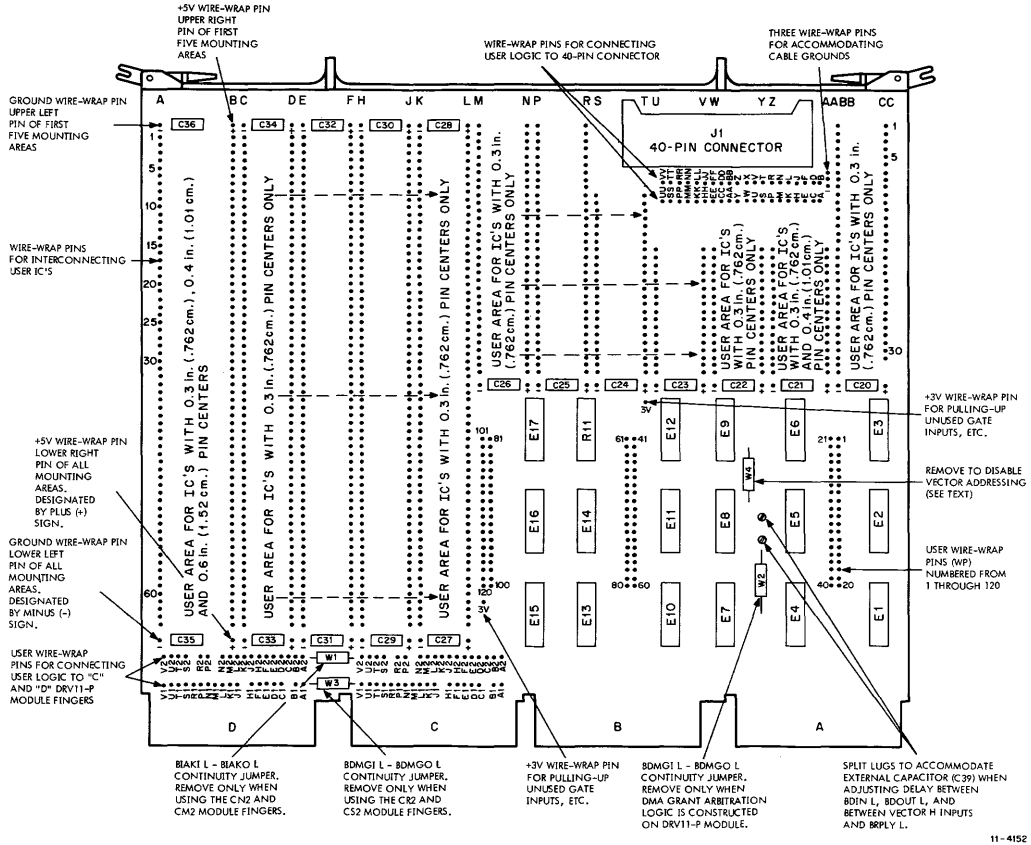
None assigned. Configurable within the range of 0-374. May conflict with DEC standard device vectors.

Diagnostic Program

None

Related Documentation

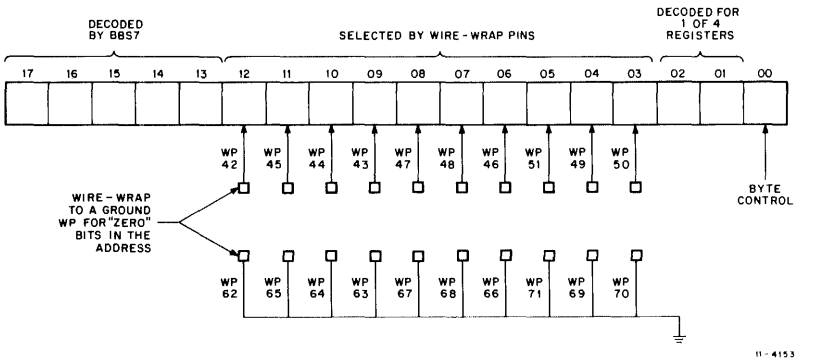
DRV11-P Foundation Module User's Manual
(EK-DR11-OP)
Field Maintenance Print Set (MP00119)
Microcomputer Interfaces Handbook (EB-20175-20)


+5V WIRE-WRAP PIN UPPER RIGHT PIN OF FIRST FIVE MOUNTING AREAS
WIRE-WRAP PINS FOR CONNECTING USER LOGIC TO 40-PIN CONNECTOR
THREE WIRE-WRAP PINS FOR ACCOMMODATING CABLE GROUNDS
GROUND WIRE-WRAP PIN UPPER LEFT PIN OF FIRST FIVE MOUNTING AREAS
WIRE-WRAP PINS FOR INTERCONNECTING USER IC'S
+5V WIRE-WRAP PIN LOWER RIGHT PIN OF ALL MOUNTING AREAS, DESIGNATED BY PLUS (+) SIGN.
GROUND WIRE-WRAP PIN LOWER LEFT PIN OF ALL MOUNTING AREAS, DESIGNATED BY MINUS (-) SIGN.
USER WIRE-WRAP PINS FOR CONNECTING USER LOGIC TO "C" AND "D" DRV11-P MODULE FINGERS
J1 40-PIN CONNECTOR
USER AREA FOR IC'S WITH 0.3 in. (.762 cm.), 0.4 in. (1.01 cm.) AND 0.6 in. (1.52 cm.) PIN CENTERS
USER AREA FOR IC'S WITH 0.3 in. (.762 cm.) PIN CENTERS ONLY
USER AREA FOR IC'S WITH 0.3 in. (.762 cm.) PIN CENTERS ONLY
USER AREA FOR IC'S WITH 0.3 in. (.762 cm.) PIN CENTERS ONLY
USER AREA FOR IC'S WITH 0.3 in. (.762 cm.) PIN CENTERS ONLY
USER AREA FOR IC'S WITH 0.3 in. (.762 cm.) AND 0.4 in. (1.01 cm.) PIN CENTERS ONLY
USER AREA FOR IC'S WITH 0.3 in. (.762 cm.) PIN CENTERS ONLY
+3V WIRE-WRAP PIN FOR PULLING-UP UNUSED GATE INPUTS, ETC.
REMOVE TO DISABLE VECTOR ADDRESSING (SEE TEXT)
USER WIRE-WRAP PINS (WP) NUMBERED FROM 1 THROUGH 120
BIAKI L - BIAKO L CONTINUITY JUMPER. REMOVE ONLY WHEN USING THE CN2 AND CM2 MODULE FINGERS.
BDMGI L - BDMGO L CONTINUITY JUMPER. REMOVE ONLY WHEN USING THE CR2 AND CS2 MODULE FINGERS.
+3V WIRE-WRAP PIN FOR PULLING-UP UNUSED GATE INPUTS, ETC.
BDMGI L - BDMGO L CONTINUITY JUMPER. REMOVE ONLY WHEN DMA GRANT ARBITRATION LOGIC IS CONSTRUCTED ON DRV11-P MODULE.
SPLIT LUGS TO ACCOMMODATE EXTERNAL CAPACITOR (C39) WHEN ADJUSTING DELAY BETWEEN BDIN L, BDOUT L, AND BETWEEN VECTOR H INPUTS AND BRPLY L.
11-4152

Device Address Selection

The DRV11-P will respond to up to four consecutive addresses in the bank 7 area (addresses between 160000 and 177776). The register addresses are sequential by even numbers and are as follows.

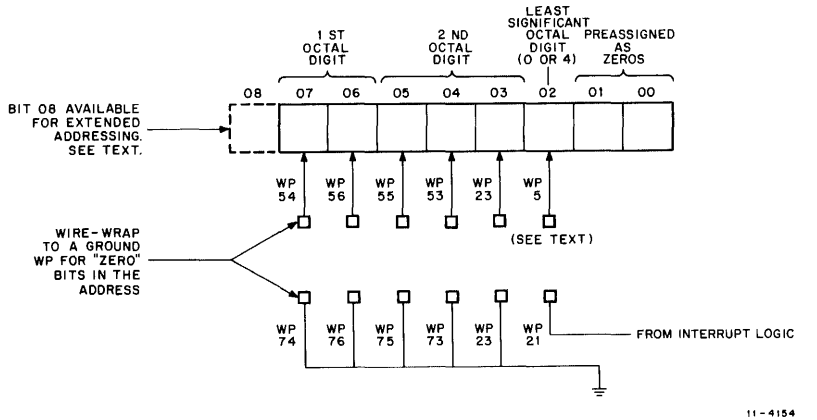
Register	BBS7	Octal Address
1	1	1xxxx0
2	1	1xxxx2
3	1	1xxxx4
4	1	1xxxx6



DRV11-P Device Address Select Format

Vector Address Selection

To cause separate vectors for an interrupt A and an interrupt B, wirewrap WP5 to WP21.



DRV11-P Vector Address Select Format

Bus Reply

The BRPLY L signal is normally issued within 85 ns (max.) of receiving either BDIN L or BDOUT L, depending on the bus cycle. If the user's interface requires more time before ending the bus cycle, the BRPLY L signal can be delayed up to a maximum of 10 by adding capacitor C39 across the split lugs in the BRPLY delay circuit. The amount of capacitance required for various delays is given in the following table.

C39 R-C Delays for BRPLY

Resistor (Constant)	Capacitance (C39 Option)	Delay (Typical)*
680 Ω	0 pF	50 ns
680 Ω	100 pF	75 ns
680 Ω	120 pF	80 ns
680 Ω	470 pF	165 ns
680 Ω	560 pF	185 ns
680 Ω	680 pF	210 ns
680 Ω	1200 pF	340 ns

*Typical BRPLY delay with respect to DBOUT and BDIN.

Maximum DRV11-P IC Density (All Areas)

IC Type	Max ICs
6 pin	122
8 pin	97
14 pin	61
16 pin	52
18 pin	44
20 pin	43
22 pin	6
24 pin	5
40 pin	3

User Wirewrap Pins

Wirewrap Pin	Function
WP1	SPARE 0 - Spare input to the vector address multiplexer. This input can be used to read part of a control/status register.
WP2	SPARE 3 - See WP1.
WP3	Ground for vector address bit V3. See WP23.
WP4	SPARE 1 - See WP1.
WP5	V2 - Vector address bit 02.
WP6	ENB CLK A H - ENB CLK A H is the clock input to the enable A flip-flop of the A interrupt logic. When ENB CLK A H goes high, ENB DATA A is clocked into the enable A flip-flop.
WP7	SPARE 2 - See WP1.
WP8	ENB B ST H - ENB B ST H is the status output from the enable B flip-flop of the B interrupt logic. When ENB B ST H is high, the enable B flip-flop is set.
WP9	IAKI L - Test point for the BIAK I bus signal. BIAKI L is the processor's response to BIRQ L and is daisy-chained such that the first requesting device blocks the signal propagation. Nonrequesting devices pass the signal on as BIAKO L. The leading edge of BIAKI L causes BIRQ L to be unasserted by the requesting device.
WP10	D01 L - Test point for data/address bit one. Useful when testing the protocol logic. D01 is latched in the protocol logic at the asserted edge of BSYNC L. D01 and D02 are decoded to produce the SEL DEV outputs.
WP11	BWTBT L - Test point for the BWTBT bus signal, while BDOUT L is asserted, BWTBT L indicates a byte or word operation: BWTBT L asserted indicates byte operation; BWTBT L unasserted indicates word operation. BWTBT L decoded with BDOUT L and BDAL 0 L forms OUT LB L or OUT HB L.
WP12	R C X X - Test point for monitoring the delay of BRPLY.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP13	BSYNC H - Test point for the BSYNC L bus signal. BSYNC L indicates that the address is valid. At the assertion of BSYNC L, address information is trapped in four latches. While unasserted, disables all outputs except the vector term of BRPLY L. BSYNC L is held throughout the entire bus cycle.
WP14	D00 H - One of 16 data or address lines from the transceivers for user applications. Address bit 00 is used for byte selection: 0 = low byte; 1 = high byte.
WP15	BDOUT L - Test point for the BDOUT L bus signal. BDOUT is a strobe signal to effect a data output transaction. BDOUT L is decoded with BWTBT L and BDAL0 to form OUT LB L and OUT HB L. BDOUT L also causes BRPLY L to be issued through the delay circuit.
WP16	IN WD L - In Word (IN WD) is used to gate input data from a selected register onto the LSI-11 bus. Enabled by BSYNC L and strobed by BDIN L.
WP17	D01 H - One of 16 data or address lines from the transceivers for user applications.
WP18	INIT 0 L - An initialize signal (asserted low) for user applications.
WP19	INIT 0 H - An initialize signal (asserted high) for user applications.
WP20	BRPLY L - Test point for the BRPLY L bus signal. BRPLY L is generated by VECTOR H (vector term), or by BSYNC and ENB in combination with either BDIN L, or BDOUT L. Capacitor C37 can be added by the user to extend the delay.
WP21	VEC RQST B H - Used to distinguish whether device A or device B is making a request. VECT RQST B H is asserted for device B requests and unasserted for device A requests.
WP22	V3 - Vector address bit 03. WP23 is used to select the state of vector address bit 03. When not wrapped to a ground pin, vector address bit 03 is a 1. When wrapped to WP3, vector address bit 03 is a 0.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP24	ENB DATA A H - Interrupt enable A data line. The level on this line, in conjunction with the ENB CLK A H (see WP6) line, determines the state of the A interrupt enable flip-flop within the interrupt logic.
WP25	BIAKO L - Test point for the BIAKO L bus signal. BIAKO L is the daisy-chained signal that is passed by all devices not requesting interrupt service (see WP9).
WP26	ENB CLK B H - ENB CLK B H is the clock input to the enable B flip-flop of the B interrupt logic. When ENB CLK B H goes high. ENB DATA B is clocked into the enable B flip-flop.
WP27	ENB DATA B H - Interrupt enable B data line. The level on this line, in conjunction with the ENB CLK B H (see WP 26) lines, determines the state of the B interrupt enable flip-flop within the interrupt logic.
WP28	RQST B H - When RQST B H is asserted, the bus request flip-flop for device B in the interrupt logic is enabled, and BIRQ L becomes asserted if the interrupt enable flip-flop is set.
WP29	VECTOR H - Test point for VECTOR H. This signal causes BRPLY L (vector term) to be generated through a delay independently of BSYNC L and ENB H. VECTOR H also gates the vector address onto the LSI-11 bus via the vector address generator.
WP30	D02 L - Test point for data/address bit 2. Useful when testing the protocol logic. D02 is latched at the asserted edge of BSYNC L. D02 and D01 are decoded to produce the SEL DEV outputs.
WP31	ENB H - Test point for ENB H. This signal is the result of a comparison between the device address on the LSI-11 bus and the device address established by the user. When the addresses compare, ENB H is asserted and sent to the protocol logic.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP32	SEL DEV 6 L - One of four select signals that is true as a function of BDAL1 L and BDAL2 L if ENB H (see WP31) is asserted at the asserted edge of the BSYNC L. The four select signals indicate that a user's register has been selected for a data transaction. The select signals remain asserted until BSYNC L becomes unasserted.
WP33	SEL DEV 4L - See WP32.
WP34	SEL DEV 2L - See WP32.
WP35	SEL DEV 0L - See WP32.
WP36	OUT LB L - Out Low Byte is used to load (write) data into the low byte of a selected user register. See WP37.
WP37	OUT HB L - Out High Byte is used to load (write) data into the high byte of a selected user register. If used with OUT LB L, the higher, lower, or both bytes can be written. OUT HB L is enabled by BSYNC L and the decode of BWTBT L and BDAL0 L, and strobed by BDOUT L.
WP38	BIRQ L - Test point for the BIRQ L bus signal. This signal is asserted by a device needing interrupt service.
WP39	BDMGO L - This signal is generated by DMA devices as a result of arbitrating the BDMGI L line. Jumper W2 must be removed if the DRV11-P is to be used for DMA service.
WP40	BDMGI H - Used as a source for the BDMGI signal to drive the user's DMA request arbitration logic. See WP39.
WP41	ENB A ST H - ENB A ST H is the status output from the enable A flip-flop of the A interrupt logic. When ENB A ST HA is high, the enable A flip-flop is set.
WP42	A12 - Used to select the user's device address along with WP45, 44, 43, 47, 48, 46, 51, 49, 50. When not wrapped to a ground pin, the particular device address bit will be a 1. When wrapped to a ground pin (WP62 for bit A12), the particular bit will be a 0.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP43	A09 - User's device address bit 09. The associated ground pin is WP63. See WP42.
WP44	A10 - User's device address bit 06. The associated ground pin is WP64. See WP42.
WP45	A11 - User's device address bit 06. The associated ground pin is WP65. See WP42.
WP46	A06 - User's device address bit 06. The associated ground pin is WP66. See WP42.
WP47	A08 - User's device address bit 06. The associated ground pin is WP67. See WP42.
WP48	A07 - User's device address bit 06. The associated ground pin is WP68. See WP42.
WP49	A04 - User's device address bit 04. The associated ground pin is WP69. See WP42.
WP50	A03 - User's device address bit 06. The associated ground pin is WP705. See WP42.
WP51	A05 - User's device address bit 05. The associated ground pin is WP17. See WP42.
WP52	SPARE 4 - See WP1.
WP53	V4 - Vector address bit 03. The associated ground pin is WP73. See WP 23.
WP55	V5 - Vector address bit 05. The associated ground pin is WP75. See WP23.
WP56	V6 - Vector address bit 06. The associated ground pin is WP76. See WP23.
WP57	IN03 H - One of 16 data or address lines to the transceivers for user applications.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP58	SPARE ENB 0 - SPARE ENB 0 and SPARE ENB 1 (WP59) both must be driven low to write data from SPARE inputs 0 through 7 to the LSI-11 bus via the transceiver. For 8-bit input applications, SPARE ENB 0 could be driven by one of the SEL DEV lines, while SPARE ENB 1 could be driven by IN WD L.
WP59	SPARE ENB 1 - See WP58.
WP60	IN00 H - See WP57.
WP61	D09 H - See WP17.
WP62	Ground for user's device address bit A12. See WP42.
WP63	Ground for user's device address bit A09. See WP42.
WP64	Ground for user's device address bit A10. See WP42.
WP65	Ground for user's device address bit A11. See WP42.
WP66	Ground for user's device address bit A06. See WP42.
WP67	Ground for user's device address bit A08. See WP42.
WP68	Ground for user's device address bit A07. See WP42.
WP69	Ground for user's device address bit A04. See WP42.
WP70	Ground for user's device address bit A03. See WP42.
WP71	Ground for user's device address bit A05. See WP42.
WP72	D04 H - See WP17.
WP73	Ground for vector address bit V4. See WP23.
WP74	Ground for vector address bit V5. See WP23.
WP75	Ground for vector address bit V6. See WP23.
WP76	Ground for vector address bit V7. See WP23.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP77	BBS7 H - Test point for the bank 7 select (BBS7) bus signal. This line is asserted by the bus master when an address in the upper 4K bank (28K-32K range) is placed on the LSI-11 bus.
WP78	SPARE 6 - See WP1.
WP79	D02 H - See WP17.
WP80	IN 02 H - See WP57.
WP81	D15 H - See WP17.
WP82	IN 13 H - See WP57.
WP83	D14 H - See WP17.
WP84	D13 H - See WP17.
WP85	D12 H - See WP17.
WP86	IN 12 H - See WP57.
WP87	D03 H - See WP17.
WP90	SPARE 7 - See WP1.
WP91	D10 H - See WP17.
WP92	IN 09 H - See WP57.
WP93	Not used.
WP94	TRANS ENB C L - Enables user's data to be placed onto the LSI-11 bus. Both TRANS ENB C and A (WP94 and WP120) and TRANS ENB D and B (WP95 and WP100) must be driven low prior to the processor's read data time.
WP95	TRANS ENB D L - See WP94.
WP96	IN 01 H - See WP57.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP97	VEC ENB H - Test point for VEC ENB H. This signal gates the vector address to the LSI-11 bus, provided that jumper W4 has not been removed. WP97 can be used as the source for VEC ENB H when adding an additional gate to the DRV11-P for vector address expansion up to 774.
WP98	IN 06 H - See WP57.
WP99	IN 04 H - See WP57.
WP100	TRANS ENB B L - See WP94.
WP101	IN 15 H - See WP57.
WP102	IN 14 H - See WP57.
WP103	Used to pull up the VEC ENB H line when jumper W4 is removed.
WP104	Not used.
WP105	Not used.
WP106	D08 H - See WP17.
WP107	D06 H - See WP17.
WP108	IN 11 H - See WP17.
WP109	D11 H - See WP57.
WP110	Not used.
WP111	Not used.
WP112	SPARE 5 - See WP1.
WP113	IN 08 H - See WP57.
WP114	Not used.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP115	BSYNC H - Test point for BSYNC H. At the asserted edge of this signal, address information is trapped in four latches. BSYNC H is the inversion of BSYNC L. See WP13.
WP116	Not used.
WP117	D05 H - See WP17.
WP118	IN 07 H - See WP57.
WP119	IN 05 H - See WP57.
WP120	TRANS ENB A L - See WP94.
+3 V	There are two +3 V source wirewrap pins on the DRV11-P. Each +3 V source can drive up to 13 TTL unit loads. These sources can be used for pulling up unused TTL inputs.

M7949
LAV11 PRINTER INTERFACE

Amps		Bus Loads		Cables
+5	+12	AC	DC	
0.5	0	1.8	1.0	BC11S (for LA180) 7009087 (for Centronics line printer™ models 101, 101A, 101D, 102A, and 303)

Standard Addresses

LACS 177514
LADB 177516

Vectors

200

Diagnostic Program

Refer to Appendix A.

Related Documentation

LAV11 User's Manual (EK-LAV11-OP-001)
Field Maintenance Print Set (MP00306)
LA180 DECprinter I Maintenance Manual (EK-LA180-MM)
Microcomputer Interfaces Handbook (EB-20175-20)

CAUTIONS

1. Switching – Switching the LA180 off-line while the operating system is running a program may result in the computer hanging and crashing the program. If this occurs, type P to continue. This problem does not occur if the LPV11 is used in place of the LAV11.

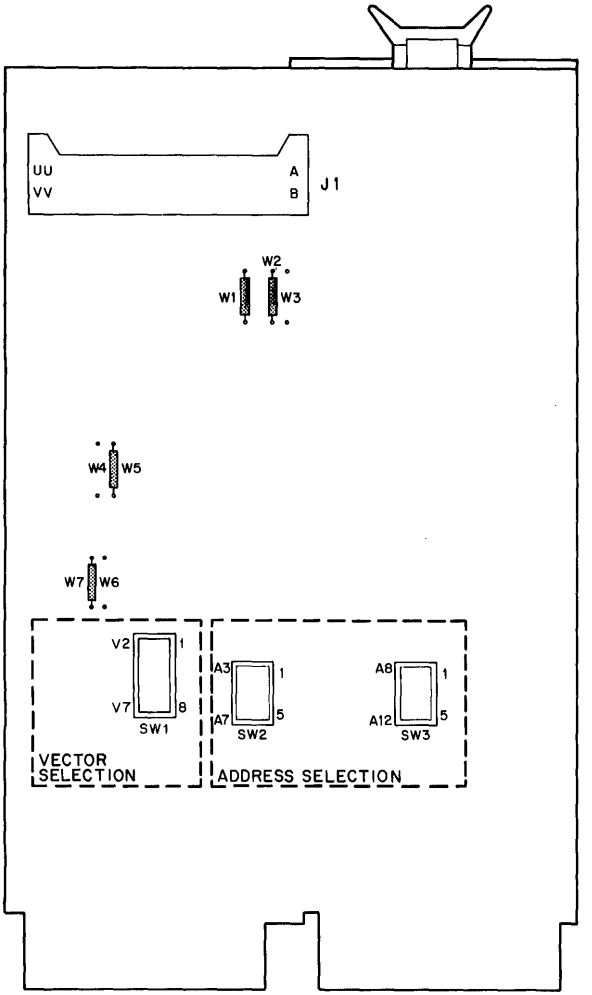
2. LA180 to LAV11 Cable – The only acceptable cable for use between the LA180 and the LAV11 is the BC11S. The end labeled P2 must attach to the LA180. The end labeled P1 must be attached to the LAV11.

3. LA180 Modifications – On the LA180 logic board (54-11023), jumper W6 must be inserted. This ensures +5 Vdc sense will read the LAV11. Failure to do so will result in a continued error condition in the LAV11 LACS buffer. W6 is located between J2 and J3 on the 54-11023 module.

4. Miscellaneous Jumpers – For an LA180, the following jumper configuration must be maintained.

Jumper	Condition	Function if Inserted
W1	I	Transmit parity on line
W2	I	+5 Vdc sense from LA180
W3	R	+5 Vdc sense from LAV11
W4	R	DEMAND is asserted low
W5	I	DEMAND is asserted high
W6	R	P STROBE is asserted low
W7	I	P STROBE is asserted high

5. The field replacement for the LAV11 (M7949) is the LPV11 (M8027).



STANDARD CONFIGURATION

ADDRESS		
SW3	1	OFF
	2	OFF
	3	OFF
	4	OFF
	5	OFF
SW2	1	OFF
	2	ON
	3	ON
	4	OFF
	5	ON
VECTOR		
SW1	1	ON
	2	ON
	3	ON
	4	ON
	5	ON
	6	OFF
	7	ON
	8	N.A.

STANDARD ADDRESS = 17751X

VECTOR = 200

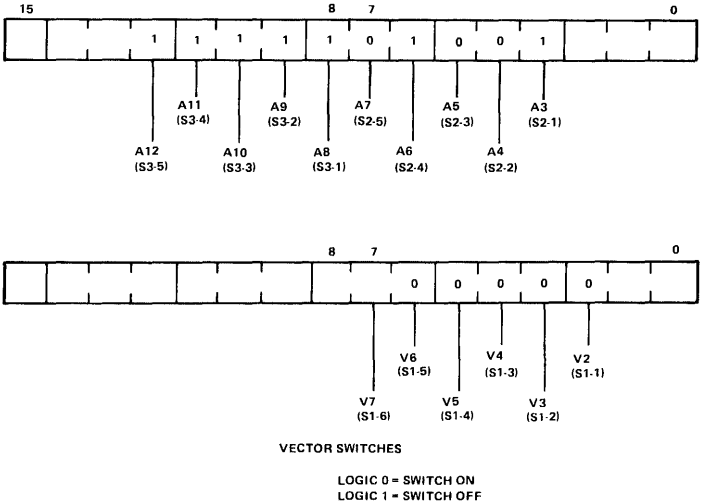
JUMPER	LA180	CENTRONICS
W1	I	I
W2	I	R
W3	R	I
W4	R	R
W5	I	I
W6	R	R
W7	I	I

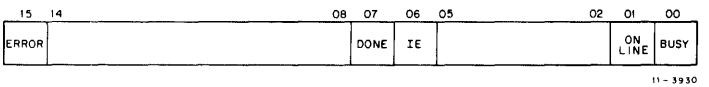
KEY:

I = INSERT

R = REMOVE

11-4146





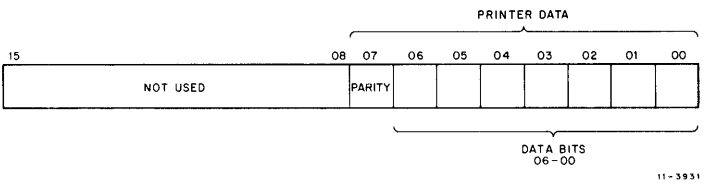
LAV11 Control/Status Register (LACS)

LACS Bit Definitions

Bit	Function
15	Error - The error bit is asserted (1) when an error condition (i.e., torn or no paper) exists in the line printer. This is a read-only bit, which is reset only by manual correction of the error condition.
14-08	Unused.
07	Done - The done bit is asserted (1) when the printer is ready to accept another character. This is a read-only bit set by INIT. The done bit is cleared by loading the LADB register. An interrupt sequence is started if IE (interrupt enable, bit 06) is also set.

LACS Bit Definitions (Cont)

Bit	Function
06	IE - The interrupt enable bit is set or cleared (read or write bit) under program control. It is cleared by the INIT (initialize) signal on the LSI-11 bus. (INIT is caused by programmed RESET instruction, console start function, or a power-up or power-down condition.) When IE is set, an interrupt sequence is started if either error or done is also set.
05-02	Unused.
01	On Line - The on line bit is asserted (1) when the LA180 printer (only) is on-line. Read only.
00	Busy - The busy bit is asserted (1) when the LA180 printer (only) is performing a print or paper advance operation.



LAV11 Data Buffer Register (LADB)

LADB Bit Definitions

Bit	Function
15-08	Unused.
07	Parity - The parity bit is loaded with the data word if the parity jumper is installed. Write only.
06-00	Data - The data comprises seven bits, with bit 06 being the most significant. This buffered 7-bit character will be transferred to the printer. These are all write-only bits.

M7950
DRV11-B GENERAL PURPOSE DMA INTERFACE

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.9	0	3.3	1.0	Two BC04Z Two BC08R

Standard Addresses

		MINC/ DECLAB
Word Count Register (WCR)	772410	171770
Bus Address Register (BAR)	772412	171772
CSR	772414	171774
DBR	772416	171776

Vector

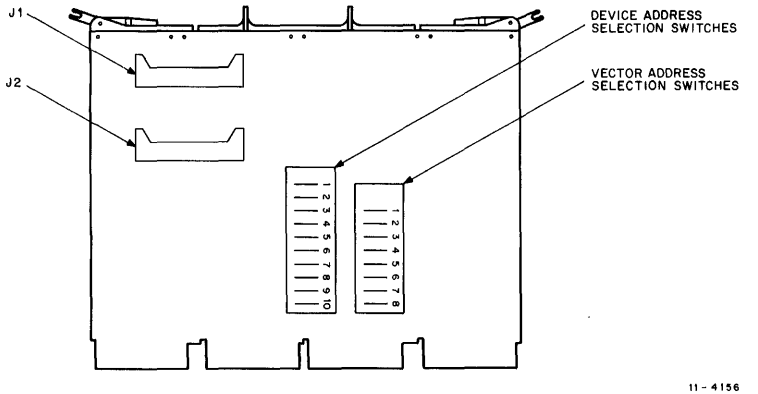
124 370

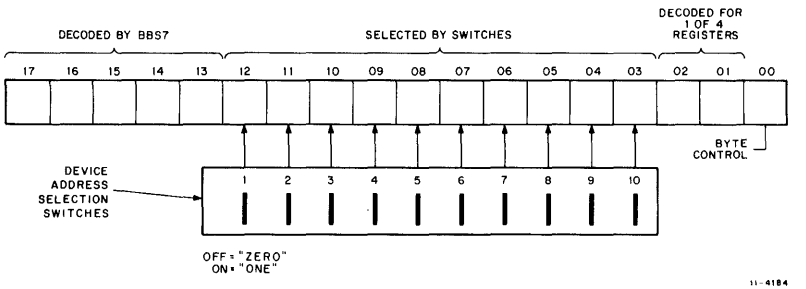
Diagnostic Programs

Refer to Appendix A.

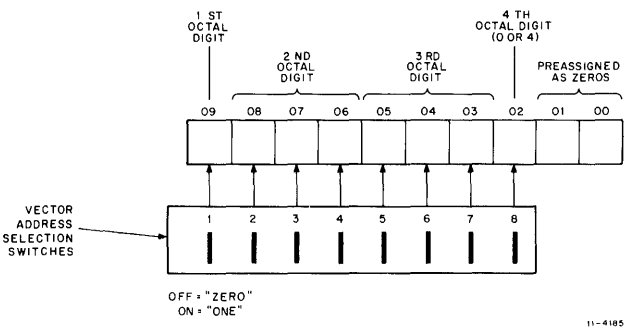
Related Documentation

DRV11-B General Purpose DMA Interface User's Manual (EK-DRV1B-OP-001)
Field Maintenance Print Set (MP00160)
Microcomputer Interfaces Handbook (EB-20175-20)

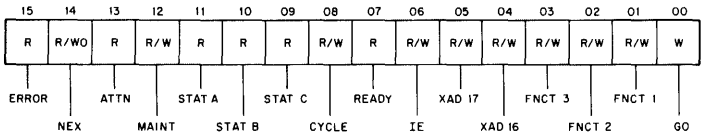




DRV11-B Device Address Select Format



DRV11-B Interrupt Vector Address Select Format



LEGEND:

R = Read only
R/W = Read / Write
R/WO = Read / Write to 0
W = Write only. Always reads as a 0

11-4186

CSR Format (11-4186)

CSR Bit Functions

Bit	Function
00	Go - Write only. Always reads as 0. 1. Causes ready to be sent to the user's device, indicating that a command has been issued. 2. Allows DMA operation.
01, 02, 03	FNCT 1, 2, 3 - Read/write. 1. Three output. 2. Cleared by INIT.
04, 05	XAD 16,17 - Read/Write. Two bits used for extended addressing. Bits 04 and 05 increment with the address count with the BAR wraps around to 0.
06	IE - Read/write. 1. Enables interrupts to occur when ready set. 2. Cleared by INIT.
07	Ready - Read only. Indicates that the DRV11-B is able to accept a new command. Set by INIT. WCOFLO, ERROR; cleared by go (bit 00).
08	Cycle - Read/write. Cycle eis used to prime a DMA bus cycle; set by CYCLE REQUEST, cleared during DMA cycle, INIT.
09, 10, 11	STAT A, B, C - Read only. Three device status input bits that indicate the state of the DSTAT A, B, and C user signals.

CSR Bit Functions (Cont)

Bit	Function
12	MAINT - Read/write. Maintenance bit for use with the MAINDEC diagnostic.
13	ATTN - Read only. Indicates the state of the ATTN user user signal; sets ready, error.
14	NEX - Read/write to 0 bit. 1. Nonexistent memory; indicates that as bus master, the DRV11-B did not receive BRPLY or that a DATIO cycle was not completed. 2. Set error. 3. Cleared by INIT or by writing it to a 0.
15	Error - Read only. 1. Indicates one of the following special conditions. • NEX (bit 14) • ATTN (bit 130) 2. Sets ready (bit 7) and causes an interrupt if IE (bit 6) is set. 3. Cleared by removing the special condition as follows. a. NEX is cleared by writing bit 14 to a 0. b. ATTN is cleared by the user device.

M7951
DUV11-DA SYNCHRONOUS SERIAL LINE INTERFACE

Amps		Bus Loads		Cables
+5	+12	AC	DC	
0.86	0.32	1.0	1.0	BC05C

Standard Addresses

Floating - Configurable in the range of 760000-777776. Refer to Appendix B.

Vector

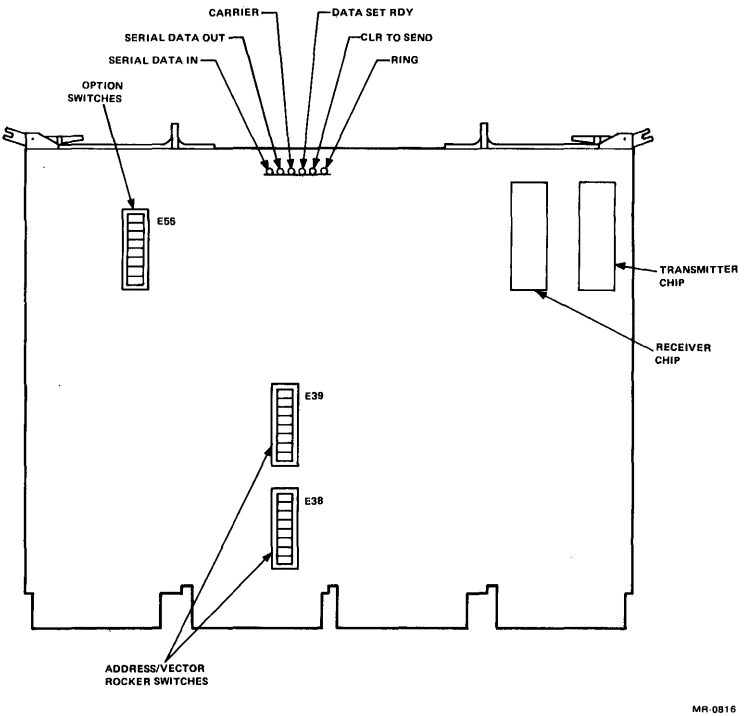
Floating - Configurable in the range of 300-770. Refer to Appendix B.

Diagnostic Programs

Refer to Appendix A.

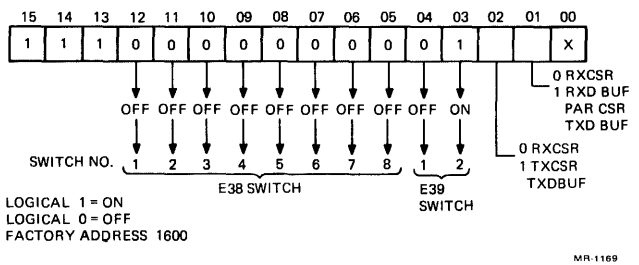
Related Documentation

DUV11 Line Interface Technical Manual (EK-DUV11-TM-001)
Field Maintenance Print Set (MP00297)
Microcomputer Interfaces Handbook (EB-20175-20)

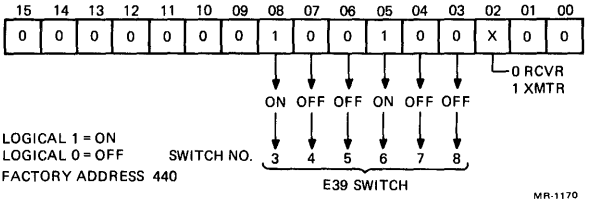

CARRIER
DATA SET RDY
SERIAL DATA OUT
CLR TO SEND
SERIAL DATA IN
RING
OPTION SWITCHES
E56
TRANSMITTER CHIP
RECEIVER CHIP
E39
E38
ADDRESS/VECTOR ROCKER SWITCHES
MR-0816

Switch Assignment for Option Switch Pack E55

Switch Number	Function
SW1	Optional clear - Switch ON enables CLR OPT, which is used to clear RXCSR bits 03, 02, and 01.
SW2	Secondary transmit - Switch ON enables secondary data channel between the modem and DUV11.
SW3	Secondary receive - Switch ON enables secondary data channel between the modem and DUV11.
SW4	Sync characters - Switch ON enables the receiver to synchronize internally upon receiving one sync character. The normal condition of receiving two sync characters exists when SW4 is off.
SW5	Special feature - Switch ON allows external clock to be internally generated, used when a modem is not being utilized.
SW6	Special feature - Optional feature is switched ON for program control of data rate selector.
SW7	Maintenance clock - Switch ON enables the clock that is used for maintenance purposes only.
SW8	Not used.



Device Address Selection



Interrupt Vector Selection

Guide for Setting Switches to Select Device Address

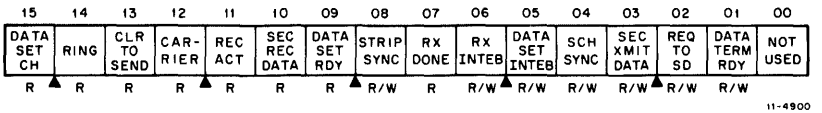
Module	E38								E39		
Switch No.	1	2	3	4	5	6	7	8	1	2	Device
Bit No.	12	11	10	9	8	7	6	5	4	3	Address
										ON	760010
									ON		760020
									ON	ON	760030
								ON			760040
								ON		ON	760050
								ON	ON		760060
								ON	ON	ON	760070
							ON				760100
						ON					760200
						ON	ON				760300
					ON						760400
					ON		ON				760500
					ON	ON					760600
					ON	ON	ON				760700
				ON							761000
			ON								762000
			ON	ON							763000
		ON									764000

NOTE

ON means switch closed to respond to logical 1 on the bus.

Guide for Setting Switches to Select Vector Address

Switch No. / Bit No.	3 / 8	4 / 7	E39 5 / 6	6 / 5	7 / 4	8 / 3	Vector Address
		ON	ON				300
		ON	ON			ON	310
		ON	ON		ON		320
		ON	ON		ON	ON	330
		ON	ON	ON			340
		ON	ON	ON		ON	350
		ON	ON	ON	ON		360
		ON	ON	ON	ON	ON	370
	ON						400
	ON		ON				500
	ON	ON					600
	ON	ON	ON				700



Receiver Status Register (RXCSR)

Receiver Status Register Bit Description

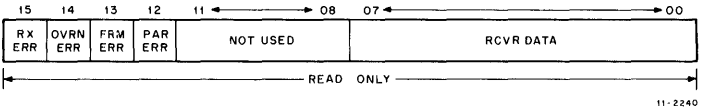
Bit	Function
15	Data Set Change (DAT SET CH) - When set, this bit indicates a modem status change. This bit is set by a transition of any of the following lines: • Ring • Clear to send • Carrier • Secondary received data • Data set ready. If bit 05 of this register is set, the setting of this bit will cause a RCVR interrupt. Read only; cleared by INIT, master reset, and the DTI SEL 0 (RXCSR read strobe).

Receiver Status Register Bit Description (Cont)

Bit	Function
14	Ring - This bit reflects the state of the modem ring line. When set, this bit indicates that a ring signal is being received from the modem. Read only.
13	Clear to Send (CLR TO SEND) - This bit reflects the state of the clear to send line from the modem. When set, this bit indicates that the modem is ready to accept data.
12	Carrier - This bit reflects the state of the modem carrier. When set, this bit indicates that the carrier is up. Read only.
11	Receiver Active (REC ACT) - When the internal synchronous mode is selected, this bit is set when the proper number of contiguous sync characters (either one or, normally, two) have been received. If external synchronous or isochronous mode is selected, this bit follows the state of the search sync bit (bit 04 of this register). Read only; cleared by INIT, master reset, and SCH SYNC (1) H (search sync) making 1 to 0 transition.
10	Secondary Receive Data (SEC RCV DAT) - This bit reflects the state of the secondary receive data line from the modem. This bit provides a receive channel for supervisory data from the modem to the processor. Read only.
09	Data Set Ready (DAT SET RDY) - This bit reflects the state of the data line from the modem. When set, this bit indicates that the modem is powered up and ready. Read only.
08	STRIP SYNC - This bit determines whether sync characters received from the modem are to be presented to the program for reading. When this bit is set, received characters that match the contents of the sync register do not cause a RCVR interrupt provided no errors are detected, i.e., bit 15 of the RXDBUF is clear.
07	Receiver Done (RX DONE) - This bit is set when synchronization has been achieved and a character has been loaded into the RXDBUF, provided the STRIP SYNC bit is not set. If the STRIP SYNC bit is set and the received character is a sync character without errors, i.e., bit 15 of the RSDBUF is clear, this bit will not be set.

Receiver Status Register Bit Description (Cont)

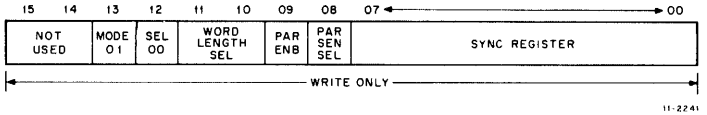
Bit	Function
06	Receiver Interrupt Enable (RX INTEB) - When set, allows a RCVR interrupt request to be generated when the RX done bit is set. Read/write; cleared by INIT and master reset.
05	Data Set Interrupt Enable (DAT SET INTEB) - When set, allows a RCVR interrupt request to be generated when the DAT SET CH bit is set.
04	Search Sync (SCH SYNC) - When set in the internal synchronous mode, enables the RCVR synchronization logic and causes the RCVR to start comparing incoming data bits to the contents of the sync register in an attempt to recognize a sync character. Read/write; cleared by INIT and master reset.
03	Secondary Transmit Data (SEC XMIT) - This bit reflects the state of the secondary transmit data line to the modem. This bit provides a transmit channel for supervisory data from the processor to the modem.
02	Request to Send (REQ TO SD) - When set, this bit causes the request to send line to the modem to be reasserted. The request to send line is a control lead to the modem. This line must be asserted before the interface can transmit data to the modem.
01	Data Terminal Ready (DATA TERM RDY) - When set, this bit indicates that the interface is powered up, programmed, and ready to receive data from the modem. Setting this bit causes the data terminal ready line to the modem to be asserted. The data terminal ready line is a control lead for the modem communication channel. When asserted, it permits the interface to be connected to the channel. Read/write; optionally cleared by INIT and master reset.



Receiver Data Buffer (RXDBUF)

Receiver Data Buffer Bit Description

Bit	Function
15	Receiver Error (RX ERR) - This bit is set whenever one of the three receiver error bits is set (logical OR of bits 14, 13, and 12). Read only; cleared only when bits 14, 13, and 12 are cleared.
14	Overrun Error (OVRN ERR) - When set, this bit indicates that the processor has failed to service the RX DONE flag within the time required to load another character into the RXDBUF, i.e., (1/baud rate) X (bit/char) seconds. Hence, the previous character was overwritten (lost). This condition indicates the loss of at least one character. Read only; cleared by INIT, master reset, and DTI SEL 2 (RXDBUF read strobe).
13	Framing Error (FRM ERR) - When set, indicates that character received was not followed by a valid stop bit. This error only occurs in the isochronous mode of operation. Read only; cleared by INIT, master reset, and DTI SEL 2.
12	Parity Error (PAR ERR) - When set, indicates that the parity of the received character does not agree with the parity programmed (odd or even). If parity is not programmed, this bit is always cleared.
07-00	Receiver Data (RCVR DATA) - This register holds the received character for transfer to the program. The buffer is right justified for 5, 6, 7, or 8 bits. If parity is received it is also loaded into the buffer at the next vacant higher order bit position. Therefore, if a 5-bit character plus parity is framed by the RCVR, the parity bit would be loaded into bit position 05 in the RXDBUF and presented to the program for reading. If an 8-bit character plus parity is framed, the parity bit would not be presented to the program for reading. Read only buffer; cannot be cleared; INIT or master reset sets the buffer to all 1s. Reading the RDXBUF causes the RXDONE bit in the RXCSR to clear.



Parameter Status Register (PARCSR)

Parameter Status Register Bit Description

Bit	Function

13,12 Mode Select (MODE SEL) - These bits control the mode of operation. Modes are selected as follows.

Mode	Bit 13	Bit 12
Internal Synchronous	1	1
External Synchronous	1	0
Isochronous	0	0
Illegal (Not Used)	0	1

Write only.

11, 10 Word Length Select (WORD LEN SEL) - These bits control the length of characters received and transmitted by interface. Word length (not including parity) is selected as follows.

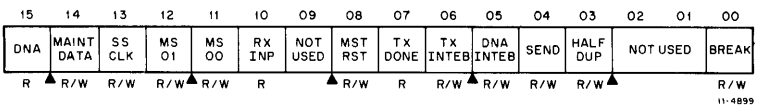
Bit/Char	Bit 11	Bit 10
5	0	0
6	0	1
7	1	0
8	1	1

Write only.

09 PAR ENB - If this bit is set, parity for each character will be (parity enable) generated by the XMTR and checked by the RCVR. If character length is fewer than eight bits, the parity bit for received data is loaded into the RXDBUF for reading by the program. If bad parity is detected at the RCVR, the parity error flag is set (bit 12 of the RXDBUF). Write only.

Parameter Status Register Bit Description (Cont)

Bit	Function
08	Parity Sense Select (PAR SEN SEL) - When the parity enable bit (bit 09 of this register) is set, the sense of the parity (odd or even) is controlled by this bit. When this bit is set, even parity is generated by the XMTR and checked for by the RCVR (the program does not have to provide a parity bit to the XMTR). When this bit is cleared, odd parity is generated and checked. Write only.
07-00	Sync Register - This register contains the sync character. The sync character is used by the RCVR to detect received sync characters and thereby achieve synchronization. The sync character is used as a fill character by the XMTR when operating in the synchronous mode. Fill characters are operating in the synchronous mode. Fill characters are transmitted when the program fails to provide characters to the XMTR fast enough to maintain continuous transmission, i.e., (1 /baud rate) X (bit/char) seconds - 1/2 (bit time).



Transmitter Status Register (TXCSR)

Transmitter Status Register Bit Description

Bit	Function
15	Data Not Available (DNA) - This bit is set by the XMTR when a fill character is transmitted. This applies only to the synchronous mode of operation and is caused by late program response to a TX DONE interrupt request. The processor response to TX DONE must be within (16fbaud rate) — (bit/char) seconds - 1/2 (bit time). If not, the fill character is transmitted. If bit 05 of this register is set, setting this bit causes an XMTR interrupt request. Read only; cleared by INIT, master reset, and DTI SEL 4 (TXCSR read strobe).

Transmitter Status Register Bit Description (Cont)

Bit	Function
14	Maintenance Data (MAINT DATA) - This bit is used in the internal loop and external loop maintenance. Read/write bit; cleared by INIT or master reset.
13	Single Step Maintenance Clock (SS CLK) - This bit is used in the internal loop and external loop maintenance modes by diagnostic program to simulate the XMTR and RCVR clocks. Read/write; cleared by INIT or master reset.
12, 11	Maintenance Mode Select 01 and 00 (MS01-MS00) - These bits are used to select the normal mode of operation or one of three maintenance modes. Modes are selected as follows.

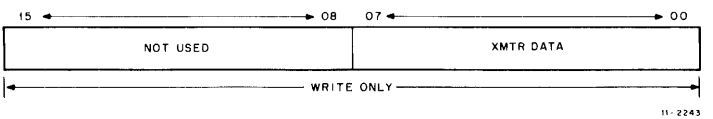
Mode	Bit 12	Bit 11
Normal	0	0
Internal Maintenance Loop	0	1
External Maintenance Loop	1	0
System Test	1	1

Read/write; cleared by INIT and master reset.

10	Receiver Input (RX INP) - This bit monitors the RCVR input in the internal loop and external loop maintenance modes. Read only.
08	Master Reset (MSTRST) - This bit is used to generate a CLR (clear) pulse, which initializes the registers and the XMTR and RCVR and inhibits the BRPLY L (bus reply) signal. This bit remains at a 1 for only 3 μs after being set. Read/write.
07	Transmitter Done (TX DONE) - This bit is set by INIT and master reset and when the first bit of the character contained in the XMTR register is placed on the XMTR output line. If bit 06 of this register is set when this bit is set, an XMTR interrupt request is generated.
06	Transmitter Interrupt Enable (TX INTEB) - When set, this bit allows an XMTR interrupt request to be generated by the TX DONE bit.

Transmitter Status Register Bit Description (Cont)

Bit	Function
05	Data Not Available Interrupt Enable (DNA INTEB) - When set, this bit allows a XMTR interrupt request to be generated by the DNA bit.
04	Send - When set, this bit enables the XMTR and transmission will start when a character is loaded into the TXDBUF. This bit must remain set until the entire message is transmitted. If not, transmission of the character currently in the XMTR register is completed and the XMTR will enter the idle state. Read/write; cleared by INIT and master reset.
03	Half Duplex (HALF DUP) - When this bit is set, operation will be in the half-duplex mode. In this mode, the RCVR is disabled whenever bit 04 of this register is set.
00	Break - When this bit is set, the serial XMTR output D5 SERIAL DATA OUT H is held in the space (constant low) condition; otherwise, operation is normal. This bit is used by the diagnostic program in the internal loop or external loop maintenance modes to inhibit the XMTR output while inputting data to the RCVR via bit 14 of this register. Read/write; cleared by INIT and master reset.



Transmitter Data Buffer (TXDBUF)

Transmitter Data Buffer Bit Description

Bit	Function
07-00	Transmitter Data (XMTR DATA) - This register is loaded by the program with the character to be transmitted. Character length is from five to eight bits. The character is right justified. If a parity bit is enabled, it is generated by the interface. Write only. INIT or master reset places all 1s in this register.

M7952
KWV11-A PROGRAMMABLE REAL TIME CLOCK

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.75	0.01	3.41	1	BC04Z BC08R

Standard Addresses

CSR	170420
Buffer/Preset Register (BPR)	170422

Vector

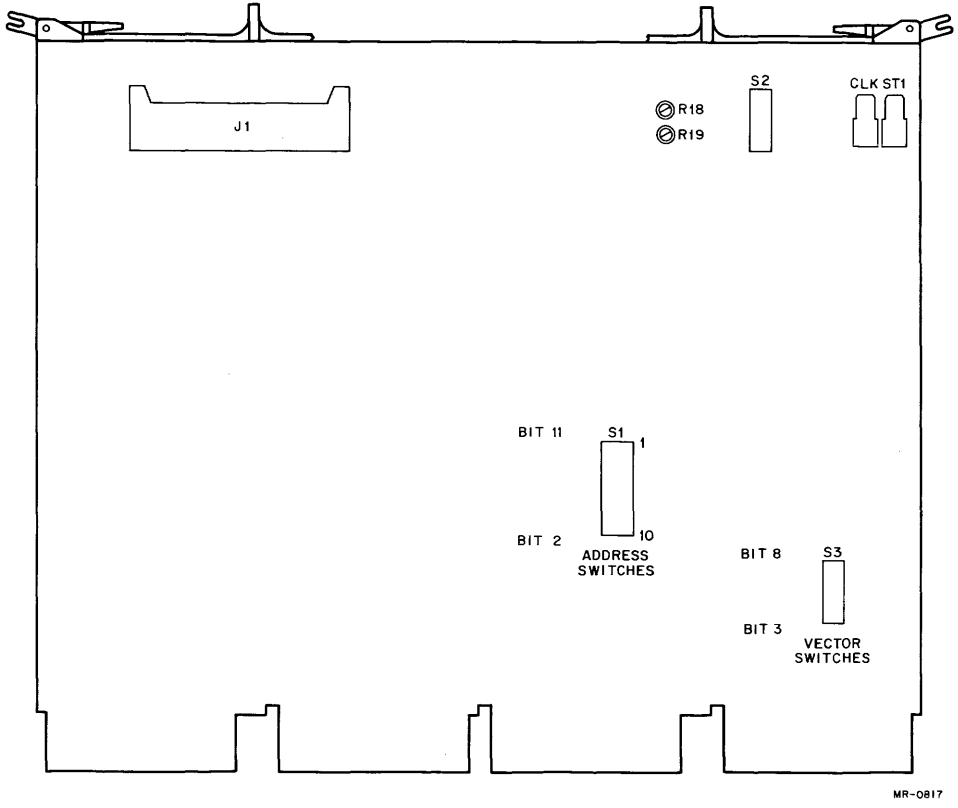
440

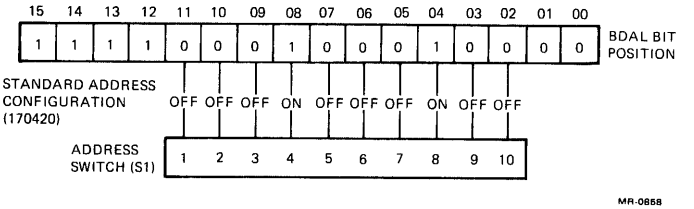
Diagnostic Programs

Refer to Appendix A.

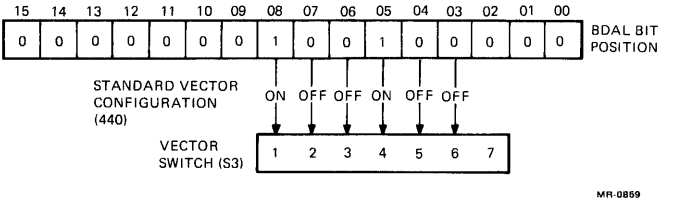
Related Documentation

ADV11-A, KWV11-A, AAV11-A, DRV11 User's Manual (EK-ADV11-OP)
Field Maintenance Print Set (MP00200)
Microcomputer Interfaces Handbook (EB-20175-20)

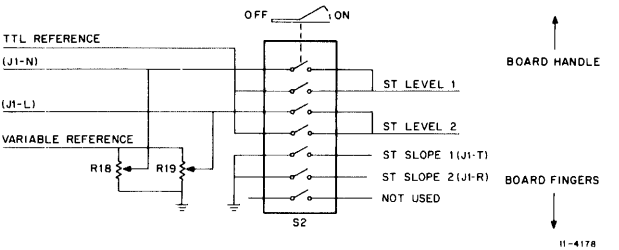

J1
R18
R19
S2
CLK ST1
BIT 11
S1
1
BIT 2
10
ADDRESS
SWITCHES
BIT 8
S3
BIT 3
VECTOR
SWITCHES
MR-0817



KWV11-A CSR Address Switches (Set for 170420)



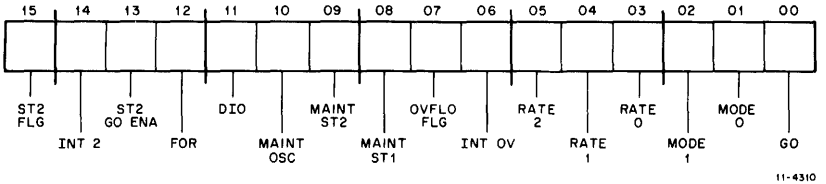
KWV11-A Vector Address Switches (Set for 000440)



KWV11-A Slope/Reference Level Selector Switches and Controls

NOTE

The user should take care that both TTL and variable switches for either Schmitt trigger are not on simultaneously. This condition will not damage components, but will produce unpredictable reference levels. Note also that if no signal is connected to a Schmitt trigger input, both threshold switches for that ST should be open for noise immunity. Alternatively, ST1 IN and ST2 IN can be grounded externally.



CSR Bit Assignments

CSR Bit Definitions

Bit	Function
15	ST2 Flag - Set by the firing of Schmitt trigger 2 or the setting of the MAINT ST2 bit in any mode while the go bit or the ST2 go enable bit is set. Cleared under program control. Also cleared at the 1-going transition of the go bit unless the ST2 go enable bit has previously been set. Must be cleared after servicing an ST2 interrupt to enable further interrupts. When cleared, any pending ST2 interrupt request will be canceled. If enabled interrupts are requested at the same time by bits 07 and 15, bit 07 has the higher priority. Read/write to 0.
14	Interrupt on ST2 (INT 2) - Set and cleared under program control. When set, the assertion of ST2 flag will cause an interrupt. If set while ST2 flag is set, an interrupt is initiated. When cleared, any pending ST2 interrupt request will be canceled. Read/write.
13	ST2 Go Enable - Set and cleared under program control. Also cleared at the 1-going transition of the go bit. When set, the assertion of ST2 flag will set the go bit and clear the ST2 go. enable bit. Read/write.
12	Flag Overrun (FOR) - Set when an overflow occurs and the overflow flag is still set from a previous occurrence, or when ST2 fires and the ST2 flag is already set. Cleared under program control and at the 1-going transition of the go bit. This bit provides the programmer with an indication that the hardware is being asked to operate at a speed higher than is compatible with the software. Read/write.

CSR Bit Definitions (Cont)

Bit	Function
11	Disable Internal Oscillator (DIO) - Set and cleared under program control. For maintenance purposes, this bit inhibits the internal crystal oscillator from incrementing the clock counter. Used in conjunction with bit 10 below. Read/write.
10	MAINT OSC - Set under program control. Clearing is not required. Always read as a 0. For maintenance purposes, setting this bit high simulates one cycle of the internal 10 MHz crystal oscillator used to increment the clock counter. Write only.
09	MAINT ST2 - Set under program control. Clearing is not required. Always read as a 0. Setting this bit simulates the firing of Schmitt trigger 2. All functions initiated by ST2 can be exercised under program control by using this bit. Write only.
08	MAINT ST1 - Set under program control. Clearing is not required. Always read as a 0. Setting this bit simulates the firing of ST1. All functions initiated by ST1 can be exercised under program control by using this bit. Write only.
07	OVFLO FLAG - Set each time the counter overflows. Cleared under the program control and at the 1-going transition of the go bit. If bit 6 is set, bit 7 will initiate an interrupt. Bit 7 must be cleared after the interrupt has been serviced to enable further overflow interrupts. If cleared while an overflow interrupt request to the processor is pending, the request is canceled. If enabled interrupts are requested at the same time by bits 07 and 15, bit 07 has the higher priority. Read/write to 0.

CSR Bit Definitions (Cont)

Bit **Function**

06 Interrupt on Overflow (INTOV) - Set and cleared under program control.

When this bit is set, the assertion of OVFLO flag will generate an interrupt. Interrupt is also generated if bit 6 is set while OVFLO flag is set. If cleared while an overflow interrupt request to the procesor is pending tne request is canceled. Read/write.

05, 04, 03 Rate - Set and cleared under program control.

These bits select clock counting rate or source.

5	4	3	Rate
0	0	0	Stop
0	0	1	1 MHz
0	1	0	100 kHz
0	1	1	10 kHz
1	0	0	1 kHz
1	0	1	100 Hz
1	1	0	ST1
1	1	1	Line (50/60 Hz)

Read/write to 0.

2, 1 Mode - Set and cleared under program control.

	2	1
Mode 0:	0	0
Mode 1:	0	1
Mode 2:	1	0
Mode 3:	1	1

Read/write.

0 Go - Set and cleared under program control. Also cleared when the counter overflows in mode 0.

Setting this bit initiates counter action as determined by the rate and mode bits. In modes 1, 2, and 3 it remains set until cleared. In mode 0 it clears itself when counter overflow occurs. Clearing bit 0 zeros and inhibits the counter. Read/write.

CSR Bit Settings for Mode 0, Single Interval

Bit and CSR Name	Bit Condition as Written by Processor	Remarks
15-ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of go bit assertion except when ST2 GO ENA has previously been set.
14-INT2	x	Set to 1 by program if interrupt on ST2 event is desired.
13-ST2 GO ENA	x	Set to 1 by program if go is to be set by external signal to ST2. Cleared by leading edge of go bit assertion.
12-FOR	(0)	
11-DIO	0	
10-MAINT OSC	0	
9-MAINT ST2	0	
8-MAINT ST1	0	
7-OVFLO FLG	(0)	Will be set to 1 by counter overflow. Always cleared by leading edge of go bit assertion.
6-INT OV	x	Set to 1 by program for interrupt on counter overflow.
5-Rate 2	x	
4-Rate 1	x	See bit definitions.
3-Rate 0	x	
2-Mode 1	0	Set by program to 0.
1-Mode 0	0	Set by program to 0.
0-Go	x	Set by program to 1 unless ST2 GO ENA is set; remains 1 until written to 0 by program. Cleared when counter overflows.

x = 0 or 1, depending on user requirements.
(0) = automatically cleared by go bit assertion.

CSR Bit Settings for Mode 1, Repeated Interval

Bit and CSR Name	Bit Condition as Written by Processor	Remarks
15-ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of go bit assertion except when ST2 GO ENA has previously been set.
14-INT 2	x	Set to 1 by program if interrupt on ST2 event is desired.
13-ST2 GO ENA	x	Set to 1 by program if go is to be set by external signal to ST2. Cleared by leading edge of go bit assertion.
12-FOR	(0)	
11-DIO	0	
10-MAINT OSC	0	
9-MAINT ST2	0	
8-MAINT ST1	0	
7-OVFLO FLG	(0)	Will be set to 1 by counter overflow. Always cleared by leading edge of go bit assertion.
6-INT OV	x	Set to 1 by program for interrupt on counter overflow.
5-Rate 2	x	
4-Rate 1	x	See bit definitions.
3-Rate 0	x	
2-Mode 1	0	Set by program to 1.
1-Mode 0	1	
0-Go	x	Same as for mode 0, except that bit is not cleared when counter overflows.

x = 0 or 1, depending on user requirements.
(0) = automatically cleared by go bit assertion.

CSR Bit Settings for Mode 2, External Event Timing

Bit and CSR Name	Bit Condition as Written by Processor	Remarks
15-ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of go bit assertion except when ST2 GO ENA has previously been set.
14-INT2	x	Set to 1 by program if interrupt on ST2 event is desired.
13-ST2 GO ENA	x	Set to 1 by program if go is to be set by external signal to ST2. Cleared by leading edge of go bit assertion.
12-FOR	(0)	
11-DIO	0	
10-MAINT OSC	0	
9-MAINT ST2	0	
8-MAINT ST1	0	
7-OVFLO FLG	(0)	Will be set to 1 by counter overflow. Always cleared by leading edge of go bit assertion.
6-INT OV	x	Set to 1 by program for interrupt on counter overflow.

x = 0 or 1, depending on user requirements.
(0) = automatically cleared by go bit assertion.

CSR Bit Settings for Mode 2, External Event Timing (Cont)

Bit and CSR Name	Bit Condition as Written by Processor	Remarks
5-Rate 2	x	
4-Rate 1	x	See bit definitions.
3-Rate 0	x	
2-Mode 1	1	Set by program to 2.
1-Mode 0	0	
0-Go		Set by program to 1 unless ST2 GO ENA is set; remains 1 until written to 0 by program. Cleared when counter overflows.

x = 0 or 1, depending on user requirements.
(0) = automatically cleared by go bit assertion.

Mode 3 (external event timing from 0 base) is identical to mode 2 except that the counter is zeroed after ST2 pulse. Counter continues to increment until go bit is set to 0.

M7954
IBV11-A LSI-11/INSTRUMENT BUS INTERFACE

Amps		Bus Loads		Cables
+5	+12	AC	DC	
0.8	0	1.77	1.0	BN11A used from IBV11-A to first instrument.
(1.5 max.)				BN01A used to any additional instruments.

Addresses

	Standard	MINC
IBS (Instrument Bus Status Register)	160150	171420
IBD (instrument Bus Data Register)	160152	171422

Vectors

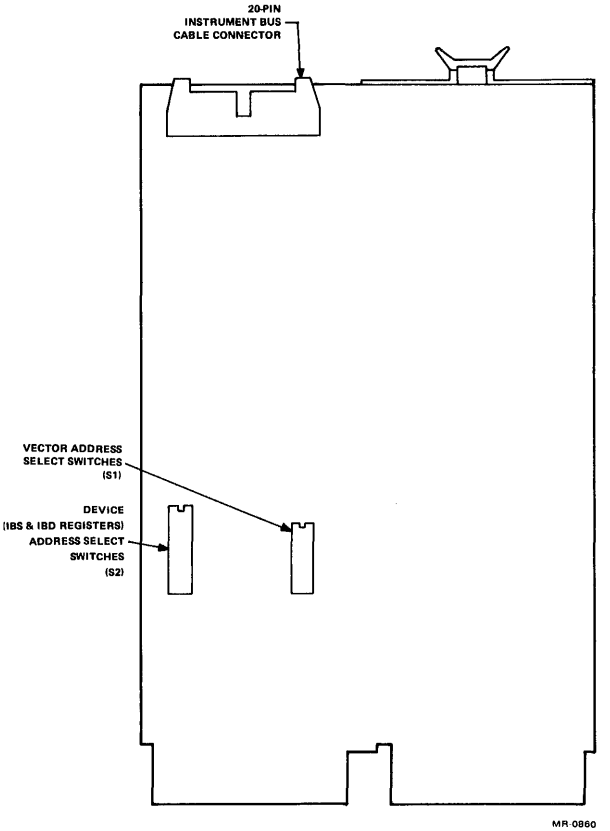
Error	420
Service request	424
Command and talker	430
Listener	434

Diagnostic Program

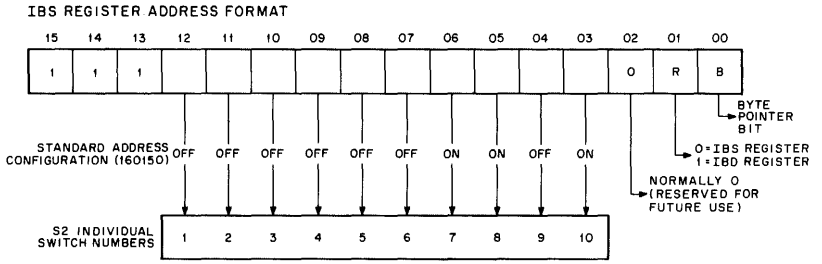
Refer to Appendix A.

Related Documentation

IBV11-A LSI-11/Instrument Bus Interface User's Manual (EK-IBV11-TM)
Digital Interface for Programmable Instrumentation (IEEE Std. 488-1975)
Field Maintenance Print Set (MP00274)
Microcomputer Interfaces Handbook (EB-20175-20)



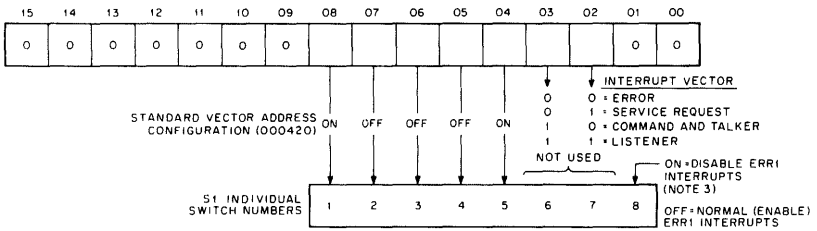
IBV11-A Address Bits



NOTES:

1. OFF = Logical 0; ON = Logical 1
2. Only the IBS REGISTER ADDRESS is configured via S2. The IBD REGISTER ADDRESS always equals the IBS REGISTER ADDRESS +2.

11-4887

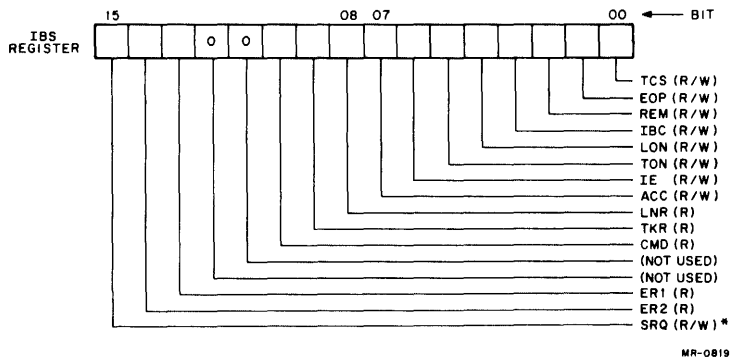


NOTES:

1. OFF = Logical 0, ON = Logical 1
2. Only the VECTOR ADDRESS bits (8:4) are configured via S1. Bits 3 and 2 are IBV11-A hardware-selected for the functions shown
3. S1-8 OFF = IBV11-A is the only system controller connected to the instrument bus; ERR1 interrupts enabled.
   S1-8 ON = Another system controller is connected to the instrument bus; ERR1 interrupts disabled.

MR-0818

IBV11-A Interrupt Vector Addresses



MR-0819

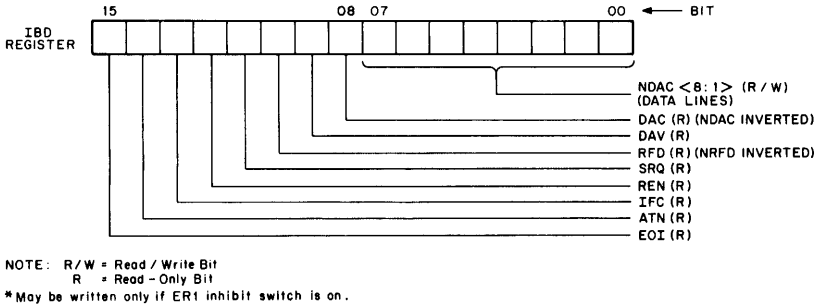
Instrument Bus Status Register

IBS Register Bits Description

Bit	Function
00	Take Control Synchronously (TCS) - Set and cleared under program control to enable or disable the IBV11-A controller-in-charge function by taking control synchronously or by negating ATN. Setting TCS will cause NRFD to be asserted for at least 500 ns before DAV is checked. ATN is then asserted when DAV is not asserted. NRFD must be unasserted and CMD is set 500 ns (minimum) after ATN is asserted. TCS is cleared by BINIT L and IFC.
01	End or Poll (EOP) - Set and cleared under program control to assert or unassert the EOI line. EOP is cleared by BINIT L and IFC.
02	Remote On (REM) - Set and cleared under program control to assert or unassert the REM line. REM is cleared by BINIT L and IFC.
03	Interface Bus Clear (IBC) - When set, the leading edge of IBC produces IFC for 125 (approximately). At the end of IFC, TCS is automatically asserted and IBC is automatically cleared. IBC is cleared by BINIT L.
04	Listener On (LON) - Set or cleared by the program to enable or disable the IBV11-A listener function. When LON is set and the DAV line is asserted, the IBS LNR bit (bit 08) becomes set. When LON is cleared, the IBV11-A ignores DAV. LON is cleared by BINIT L and IFC.
05	Talker On (TON) - Set or cleared by the program to enable or disable the IBV11-A talker function. TON is cleared by BINIT L and IFC.
06	Interrupt Enable (IE) - Set and cleared by the program to enable or disable the IBV11- A talker function. TON is cleared by BINIT L and IFC.
07	Accept Data (ACC) - Set and cleared by the program. When ACC is cleared, reading a data byte from the DIO lines will automatically assert the DAC line and clear the LNR bit (bit 08). When ACC is set, the program must clear the low byte of the IBD register in order to clear the LNR status bit and assert the DAC line.

IBS Register Bits Description (Cont)

Bit	Function
08	Listener Ready (LNR) - When set, LNR indicates that the IBV11-A has a data or command byte that is ready for reading from the low byte of the IBD. LNR is set when LON is set and the DAV line becomes asserted. LNR is cleared by reading the IBD low byte if ACC is cleared, or by clearing the IBD low byte if ACC is set. LNR is also cleared when LON is cleared by the program and by BINIT L and IFC.
09	Talker Ready (TKR) - When set, TKR indicates to the LSI-11 processor that the IBV11-A is ready for the next data byte to betransmitted to the DIO lines via the low byte of the IBD register.
10	Command Done (CMD) - When set, CMD indicates to the LSI-11 processor that the IBV11-A is ready for the next command byte to be transmitted to the DIO lines via the low byte of the IBD register.
11	Not used. Read as 0.
12	Not used. Read as 0.
13	Error 1 (ER1) - Set whenever a conflict occurs between the instrument bus ATN, IFC, or REN lines and their IBV11-A control hardware. When set, ATN H is cleared and cannot be set. This condition can only be cleared by clearing the cause of the error. ER1 can occur when another system controller is connected to the instrument bus. The error can then be suppressed by setting the ER1 inhibit switch (S1-8) on the IBV11-A module to the ON position. If the IBV11-A is the only system controller, set S1-8 to the OFF position.
14	Error 2 (ER2) - Set when the IBV11-A tries to send a data or command byte while there is no active listener or command acceptor on the instrument bus. ER2 is cleared by clearing both the TON and TCS bits.
15	Service Request (SRQ) - This bit always indicates the status of the instrument bus SRQ line. It may be written (set and cleared) if the ER1 inhibit switch is set.



Instrument Bus Data Register

IBD Register Bit Description

Bit	Function
15-8	Instrument bus control line status. The program can monitor the signal status of all eight control signals by reading this byte. Note that DAC (bit 08) and RFD (bit 10) are inverted with respect to the actual instrument bus signal lines.
7-0	Instrument bus data input/output. The program can read or write via the register byte to receive or transmit command or data bytes over the instrument bus. Bits 7-0 correspond to DIO lines 8-1.

M7955
MSV11-C MOS READ/WRITE MEMORY

Module	Model	Description
M7955-YA	MSV11-CA	4K by 16-bit read/write memory

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.1	0.54	2.32	1	None
(2.0 max.)	(0.56 max.)			

Standard Addresses

Module is shipped configured to start at bank 0.

Vectors

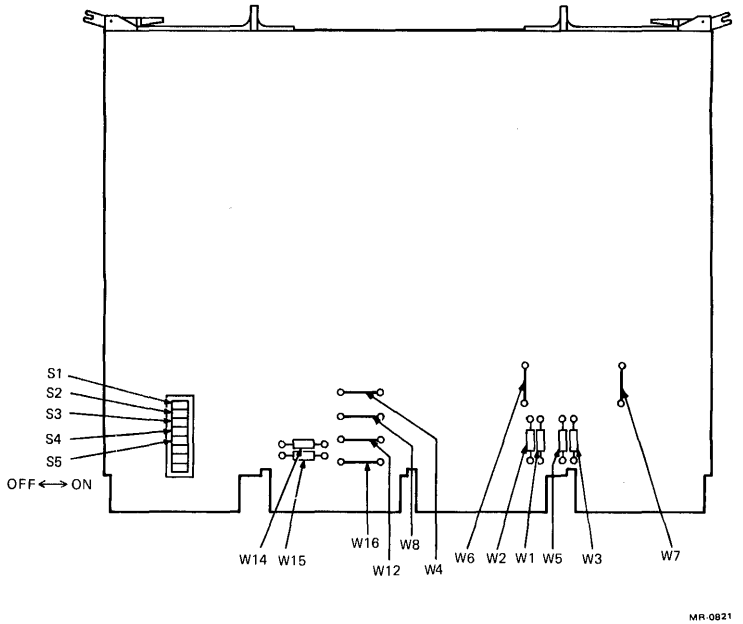
None

Diagnostic Programs

Refer to Appendix A.

Related Documentation

MSV11-C User's Manual (EK-MSV11-OP)
Field Maintenance Print Set (MP00259)
Microcomputer Processor Handbook (EB-18451-20)



M7955/MSV11-C Jumpers

NOTES

1. **Only one dynamic memory module in a system is needed to reply to the refresh bus transactions initiated by the processor. The module selected should be the one with the longest access time.**

2. **If a REV11 (M9400-YA or M9400-YC) provides refresh, only the processor-resident memory (if present) should reply to refresh. If the processor board has no resident memory, the memory module electrically farthest from the REV11 should reply.**

3. **If MSV11-Cs are mixed with MSV11-Bs, the MSV11-Cs should use internal refresh. Again, the memory electrically farthest from the refreshing device should reply. Refer to the "Refresh Configuration Procedure" in the "Systems Configurations" section.**

MSV11-C Jumper Configuration When Shipped

Jumper Name	Jumper State	Function Implemented
W1 W2 W3 W5	I I I I	Battery backup power connected to system power.
		Battery backup power only. W1 R I; W2 I R; W3 I R; W5 R I
		Battery backup power available but not desired for this MSV11-C module.
W6 W7	I I	Internal refresh enabled. Reply to refresh disabled.
		W6 W7
		External refresh; no reply. I R
		External refresh; reply enabled. R R
W4 W8 W12 W16	* * * *	Factory configured to enable the memory banks appropriate to the memory model. These are normally not changed except for: 1. Maintenance - Refer to chapter 4 of *MSV11-C User's Manual*, EK-MSV11-OP. 2. Configuring for 28K system: Remove W16 to disable upper 4K. See configuration rules in the "Systems Configurations" section.
W14	I	Bus grant continuity provided.
W15	I	

*Memory bank enable jumpers when supplied.

Module Number	Option Designation	Memory Size	W4	W8	W12	W16
M7955-YD	MSV11-CD	16K	I	I	I	I
M7955-YC	MSV11-CC	12K	I	I	I	R
M7955-YB	MSV11-CB	8K	I	I	R	R
M7955-YA	MSV11-CA	4K	I	R	R	R

MSV11-CD Addressing Summary

Starting Address	MSV11-CD Banks	Address Range	Switch Setting S1	S2	S3	S4	S5
0	0-3	0-77777	1	1	1	1	1
20000	1-4	20000-117777	0	1	1	1	1
40000	2-5	40000-137777	1	0	1	1	1
60000	3-6	60000-157777	0	0	1	1	1
100000	4-7	100000-177777	1	1	0	1	1
120000	5-10	120000-217777	0	1	0	1	1
140000	6-11	140000-237777	1	0	0	1	1
160000	7-12	160000-257777	0	0	0	1	1
200000	10-13	200000-277777	1	1	1	0	1
220000	11-14	220000-317777	0	1	1	0	1
240000	12-15	240000-337777	1	0	1	0	1
260000	13-16	260000-357777	0	0	1	0	1
300000	14-17	300000-377777	1	1	0	0	1
320000	15-20	320000-417777	0	1	0	0	1
340000	16-21	340000-437777	1	0	0	0	1
360000	17-22	360000-457777	0	0	0	0	1
400000	20-23	400000-477777	1	1	1	1	0
420000	21-24	420000-517777	0	1	1	1	0
440000	22-25	440000-537777	1	0	1	1	0
460000	23-26	460000-557777	0	0	1	1	0
500000	24-27	500000-577777	1	1	0	1	0
520000	25-30	520000-617777	0	1	0	1	0
540000	26-31	540000-637777	1	0	0	1	0
560000	27-32	560000-657777	0	0	0	1	0
600000	30-33	600000-677777	1	1	1	0	0
620000	31-34	620000-717777	0	1	1	0	0
640000	32-35	640000-737777	1	0	1	0	0
660000	33-36	660000-757777	0	0	1	0	0
700000	34-37	700000-777777	1	1	0	0	0
720000	x	x-x	0	1	0	0	0
740000	x	x-x	1	0	0	0	0
760000	x	x-x	0	0	0	0	0

NOTES

1. Switch setting:

   1 = ON
   0 = OFF

2. Each memory bank = one 4K address space.

3. Switches 6, 7, and 8 are not used.

NOTE

When used in PDP-11/23 systems, the MSV11-C memory cannot be configured in the 56K–64K byte (28K–32K word) range or in the 248K–256K byte (124K–128K word) range.

M7957
DZV11 ASYNCHRONOUS MULTIPLEXER

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.15	0.39	1.26	1.0	BC11-U

Standard Addresses

Floating - Configurable within the range of 160000-177770.

Register	Mnemonic	Address
Control and Status Register	CSR	16XXX0
Receiver Buffer	RBUF	16XXX2
Line Parameter Register	LPR	16XXX2
Transmitter Control Register	TCR	16XXX4
Modem Status Register	MSR	16XXX6
Transmit Data Register	TDR	16XXX6

XXX = selected in accordance with floating device address convention. Refer to Appendix B.

Vectors

300-777 in accordance with floating interrupt vector assignments. Refer to Appendix B.

Diagnostic Programs

Refer to Appendix A.

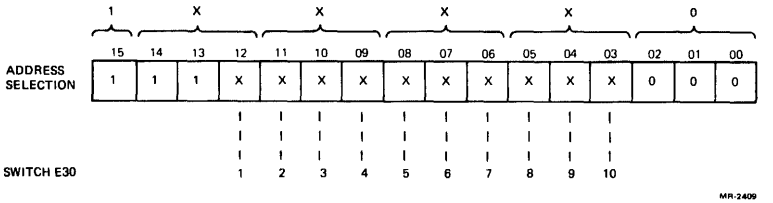
Related Documentation

DZV11 Asynchronous Multiplexer Technical Manual (EK-DZV11-TM)
DZV11 Print Set (MP-00462-00)
Microcomputer Interfaces Handbook (EB-20175-20)

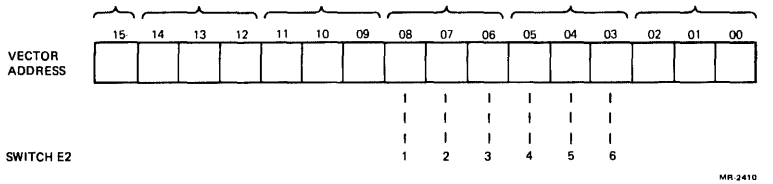
NOTES

1. **Use H325 test connector to test individual lines.**

2. **Use H329 test connector to test module without cables.**



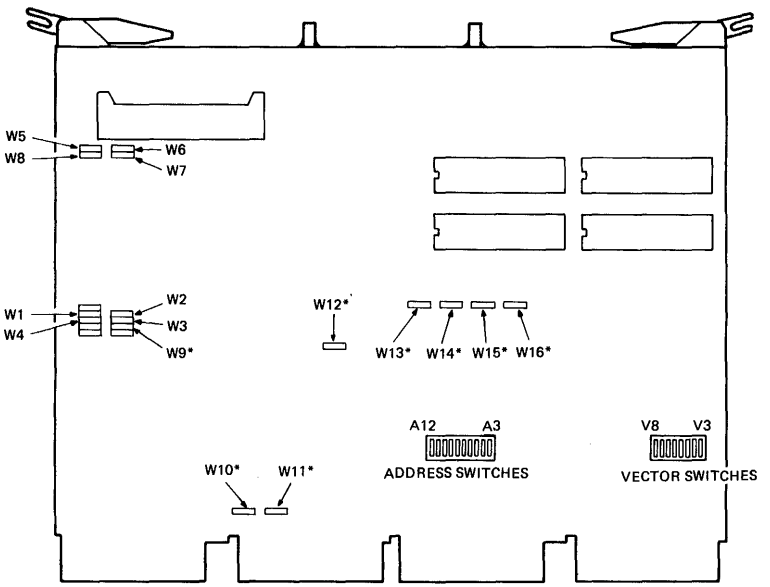
Address Switches



Vector Switches

Modem Control Jumpers

There are eight jumpers used for modem control. The jumpers labeled W1 through W4 connect Data Terminal Ready (DTR) to Request To Send (RTS). This allows the DZV11 to assert both DTR and RTS if using a modem that requires control of RTS. These jumpers must be installed to run the cable and external test diagnostic programs. The remaining four jumpers; W5 through W8, connect the Forced Busy (FB) leads to the RTS leads. With these jumpers installed, the assertion of an RTS lead places an ON or BUSY signal on the corresponding forced busy lead. The forced busy jumpers (W5 through W8) are cut out unless the modem requires them.



*NOTES:

JUMPERS W9, W12, W13, W14, W15, AND W16 ARE REMOVED ONLY FOR MANUFACTURING TESTS. THEY SHOULD NOT BE REMOVED IN THE FIELD.

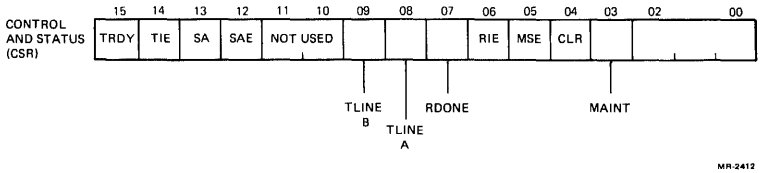
JUMPERS W10 AND W11 MUST REMAIN INSTALLED WHEN THE MODULE IS USED IN A BACKPLANE THAT SUPPLIES LSI-11 BUS SIGNALS TO THE C AND D CONNECTORS OF THE DZV11 (SUCH AS THE H9270). WHEN THE MODULE IS USED IN A BACKPLANE THAT INTERCONNECTS THE C AND D SECTIONS TO AN ADJACENT MODULE, JUMPERS W10 AND W11 MUST BE REMOVED.

MR-2411

M7957 Jumper Locations

Jumper Configuration

Jumper	Connection	Line
W1	DTR to RTS	03
W2	DTR to RTS	02
W3	DTR to RTS	01
W4	DTR to RTS	00
W5	RTS to FB	03
W6	RTS to FB	02
W7	RTS to FB	01
W8	RTS to FB	00



CSR Bit Assignments

CSR Bit Assignments

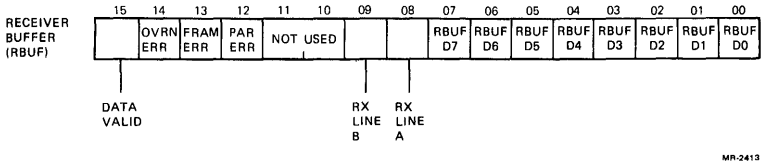
Bit	Function
00-02	Not used.
03	Maintenance - This bit, when set, loops all the transmitter's serial output leads to the corresponding receiver's serial input leads on a TTL basis. While operating in maintenance mode, the EIA received data leads are disabled. Normal operating mode is assumed when this bit is cleared. Read/write.
04	Master Clear - When written to a 1, this bit generates "initialize" within the DZV11. A read-back of the CSR with this bit set indicates initialize in progress within the device. This bit is self-clearing. All registers, silos, and UARTS are cleared with the following exceptions. 1. Only bit 15 of the receiver buffer register (valid data) is cleared; the remaining bits, 00-14, are not. 2. The high byte of the transmitter control register is not cleared by master clear. 3. The modem status register is not cleared by master clear.
05	Master Scan Enable - This read/write bit must be set to permit the receiver and transmitter control sections to begin scanning. When cleared, transmitter ready (CSR 15) is inhibited from setting and the received character buffers (silos) are cleared.
06	Receiver Interrupt Enable - This bit, when set, permits setting CSR 07 or CSR 13 to generate a receiver interrupt request. Read/write.

CSR Bit Assignments (Cont)

Bit	Function
07	Receiver Done - This is a read-only bit that sets when a character appears at the output of the first-in/first-out (FIFO) buffer. To operate in interrupt-per-character mode, CSR 06 must be set and CSR 12 must be cleared. With CSR 06 and CSR 12 cleared, character flag mode is indicated. Receiver done clears when the receiver buffer register (RBUF) is read or when master scan enable (CSR 05) is cleared. If the FIFO buffer contains an additional character, the receiver done flag stays cleared a minimum of one microsecond before presenting that character.
08-09	Transmitter Line - These read-only bits indicate the line number whose transmit buffer requires servicing. These bits are valid only when transmitter ready (CSR 15) is set, and are cleared when master scan enable is cleared. Bit 08 is the least significant bit.
10-11	Not used.
12	Silo Enable Alarm - This is a read/write bit. When set, it enables the silo alarm counter to keep count of the number of characters stored in the FIFO buffer. The counter is cleared when the silo alarm enable bit is cleared. Conditioning of this bit must occur prior to any character reception.
13	Silo Alarm - This is a read-only bit set by the hardware after 16 characters have been entered into the FIFO buffer. Silo alarm is held cleared when silo alarm enable (CSR 12) is cleared. This bit is reset by a read to the receiver buffer register and does not set until 16 additional characters are entered into the buffer. If receiver interrupt enable (CSR 06) is set, the occurrence of silo alarm generates a receiver interrupt request. Reception with CSR 06 cleared, permits flag mode operation of the silo alarm bit.
14	Transmitter Interrupt Enable - This bit must be set for transmitter ready to generate an interrupt. Read/write.

CSR Bit Assignments (Cont)

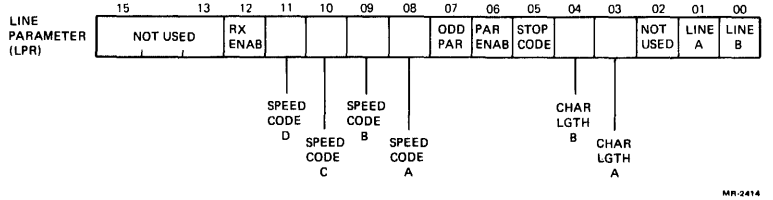
Bit	Function
15	Transmitter Ready - This bit is read only and is set by the hardware. This bit sets when the transmitter clock stops on a line whose transmit buffer may be loaded with another character and whose associated TCR bit is set. The transmitter number, specified in CSR 08 and CSR 09, is valid only when transmitter ready is set. Transmitter ready is cleared by any of the following conditions: a. when master scan enable is cleared b. when the associated TCR bit is cleared for the line number pointed to in CSR 08 and CSR 09 c. at the conclusion of the load instruction of the transmit data register (low byte only). If additional transmit lines require service, transmitter ready reappears within 1.4 microseconds from the completion of the transmit data register load instruction. The occurrence of transmitter ready with transmitter interrupt enable set, generates a transmitter interrupt request.



RBUF Bit Assignments

RBUF Bit Assignments

Bit	Function
00-07	Received Character - These bits contain the received character, right justified. The least significant bit is bit 00. Unused bits are 0. The parity bit is not shown.
08-09	Received Character Line Number - These bits contain the line number upon which the received character was received. Bit 08 is the least significant bit.
10-11	Not used.
12	Parity Error - This bit is set if the sense of the parity of the received character does not agree with that designated for that line.
13	Framing Error - This bit is set if the received character did not have a stop bit present at the proper time. This bit is usually interpreted as indicating the reception of a break.
14	Overrun Error - This bit is set if the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding buffer on that line.
15	Valid Data - This bit, when set, indicates that the data presented in bits 00-14 is valid. This bit permits the use of a character-handling program that takes characters from the FIFO buffer until there are no more available. This is done by reading this register and checking bit 15 until the program obtains a word for which bit 15 is 0.



LPR Bit Assignments

LPR Bit Assignments

Bit	Function
00-01	Parameter Line Number - These bits specify the line number for which the parameter information (bits 3-12) is to apply. Bit 00 is the least significant bit.
02	Not used. Must always be written as a 0 when specifying the parameter line number. Writing this bit as a 1 extends the parameter line number field into nonexistent lines. Parameters for lines 00-03 are not affected.
03-04	Character Length - These bits are set to receive and transmit characters of the length (excluding parity) as shown below.

04	03	
0	0	5 bit
0	1	6 bit
1	0	7 bit
1	1	8 bit

05	Stop Code - This bit sets the stop code length (0 = 1 unit stop; 1 = 2 unit stop or 1.5 unit stop if a five-level code is employed).
06	Parity Enable - If this bit is set, characters transmitted on the line have an appropriate parity bit affixed, and characters received on the line have their parity checked.
07	Odd Parity - If this bit is set and bit 06 is set, characters of odd parity are generated on the line and incoming characters are expected to have odd parity. If this bit is not set, but bit 06 is set, characters of even parity are generated on the line, and incoming characters are expected to have even parity. If bit 06 is not set, the setting of this bit is immaterial.

LPR Bit Assignments (Cont)

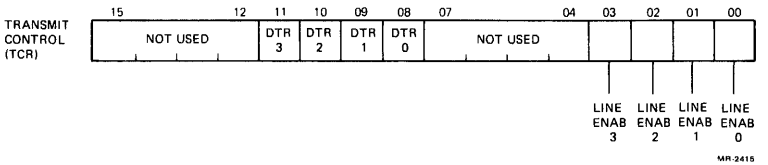
Bit **Function**

08-11 Speed Code - The state of these bits determines the operating speed for the transmitter and receiver of the selected line.

11	10	09	08	Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	0	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	Invalid

12 Receiver Enable - This bit must be set before the UART receiver logic can assemble characters from the serial input line. This bit is cleared following a BINIT or device master clear.

13-15 Not used.



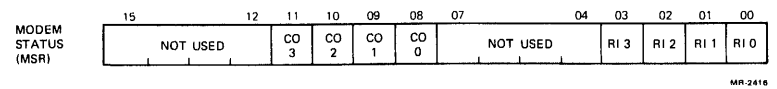
TCR Bit Assignments

The TCR bits are represented in bits 00-03. These bits are read/write and are cleared by BINIT or device master clear. Bits 04-07 are not used and read as 0.

The high byte of the TCR register contains the writable modem control lead, the Data Terminal Ready (DTR). Bit designations are as follows.

Bit	Name
08	DTR line 00
09	DTR line 01
10	DTR line 02
11	DTR line 03
12-15	Unused; read as 0.

Assertion of a DTR bit puts an ON condition on the appropriate modem circuit for that line. DTR bits are read/write and are cleared only by BINIT. Jumpers have been provided to allow the RTS circuits to be asserted with DTR assertions.



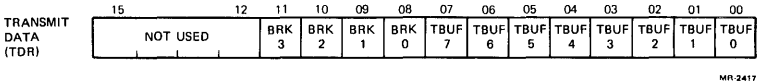
MSR Bit Assignments

Modem Status Register

The Modem Status Register (MSR) is a 16-bit read-only register. A read to this register results in the status of the readable modem control leads, ring and carrier. The ON condition of a modem control lead is interpreted as a logical 1. Bits 04-07 and 12-15 are unused and read as a 0. Remaining bit designations are as follows.

Bit	Name
00	Ring line 00
01	Ring line 01
02	Ring line 02
03	Ring line 03
04-07	Unused; read as 0.

Bit	Name
08	Carrier line 00
09	Carrier line 01
10	Carrier line 02
11	Carrier line 03
12-15	Unused; read as 0.



TDR Bit Assignments

Transmit Data Register

The Transmit Data Register (TDR) is a byte- and word-addressable, write-only register. Characters for transmission are loaded into the low byte. TDR bit 00 is the least significant bit. Loading of a character should occur only when transmitter ready (CSR 15) is set. The character that is loaded into this register is directed to the line defined in CSR bits 08 and 09. The high byte of the TDR is designated as the break control register.

Each of the four multiplexer lines has a corresponding break bit for that line. TDR bit 08 represents the break bit for line 00, TDR bit 09 for line 01, etc. TDR bits 12-15 are unused. Setting a break bit forces that line's output to space. This condition remains until cleared by the program. This register is cleared by BINIT or device master clear. The break control register can be utilized regardless of the state of the device maintenance bit (CSR 03).

M8012
BDV11 BUS TERMINATOR, BOOTSTRAP, AND DIAGNOSTIC ROM

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.6	.07	2	1	None

Standard Addresses

ROM Window	173000-173776
Page Control Reg.	177520
Scratch Pad Reg.	177522
Option Select Reg.	177524 (read only)
Display Reg.	177524 (write only)
Line Clock CSR	177546

Standard Vectors

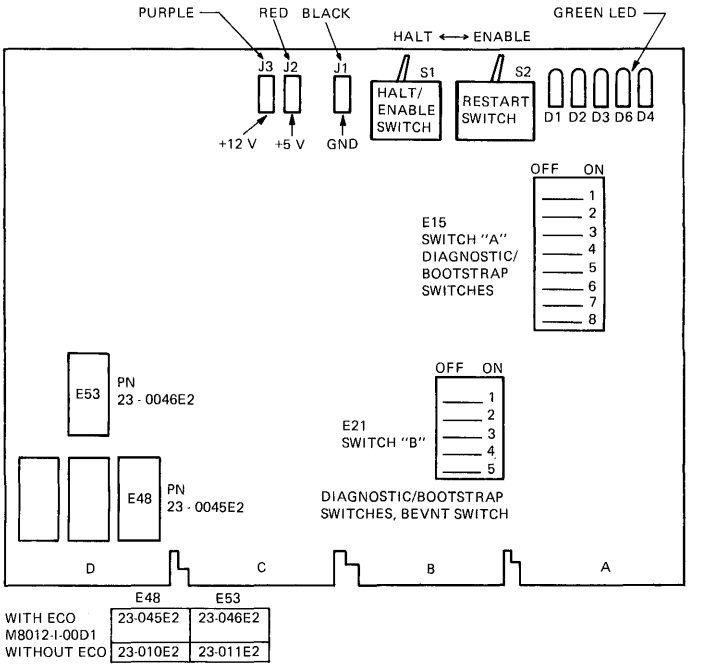
Line Clock	100

Diagnostic Programs

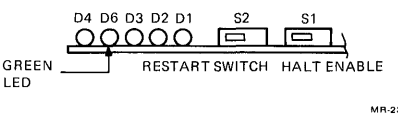
Refer to Appendix A.

Related Documentation

BDV11 Bus Terminator, Bootstrap, Diagnostic ROM Technical Manual (EK-BDV11-TM)
Field Maintenance Print Set (MP00489)
Microcomputer Interfaces Handbook (EB-20175-20)

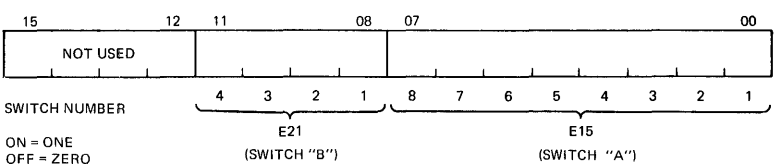


BDV11-A Switches and Indicators



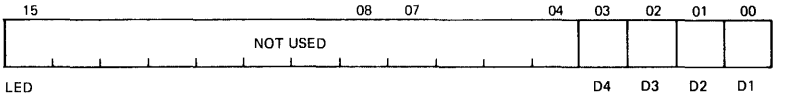
Diagnostic Light Display

777524 READ ONLY



Switch Register

777524 WRITE ONLY

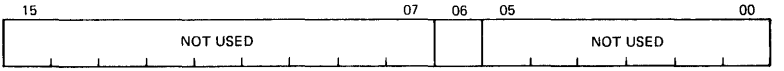


LOAD "0" TO TURN ON LED

MR-2384

Display Register

777546



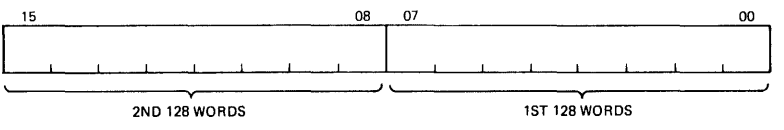
1 = LINE CLOCK ENABLE

SWITCH "B5" MUST BE
"ON" FOR PROGRAM CONTROLLED
LINE CLOCK

MR-2385

Line Clock CSR

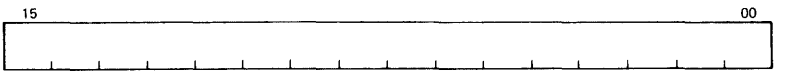
777520



MR-2386

Page Control Register

777522



MR-2387

Read/Write Register

BDV11 Hardware Registers

Register	Function	Bus Address
Page Control Register (PCR)	Controls mapping of ROM pages into physical ROM addresses. Cleared when power is turned on or when RESTART switch is activated. Sixteen bits.	177520. Word or byte byte addressable; can be read or written.
Read/Write Register	Maintenance register used for diagnostics. Cleared when power is turned on or when RESTART switch is activated. Sixteen bits.	177522. Word or byte byte addressable; can be read or written.
Switch Register	Used for maintenance and system configuration (selects diagnostic and/or bootstrap programs for execution). Bits 0-11 of the register (corresponding to E15-1 through E15-8 and E21-1 through E21-4, respectively) are associated with BDAL <0:11> L, respectively. When an individual switch of the register is closed (on), the corresponding BDAL signal is low (1). Twelve bits.	177524. Read-only register.
Display Register	Controls the diagnostic light display. Bits 0-3 of the register control LEDs D1-D4, respectively. When a bit is set, the corresponding LED is off; cleared (all lights on) when power is turned on or when RESTART switch is activated. Four bits.	177524. Word or byte addressable; write-only register.

BDV11 Hardware Registers (Cont)

Register	Function	Bus Address
Line Clock CSR	When cleared, this register clamps the BEVNT signal low (if BEVNT switch is closed). This action permits program control of the LSI-11 line time clock (LTC) function. Register cleared when power is turned on or when RESTART switch is activated. One bit.	177546. Word or byte addressable; write-only register.

BDV11 (For ROMs 23-045E2 and 23-046E2 only)

Switch Settings and Mnemonics

For the discussion that follows, the M8012 switch E15 will be called "A" and E21, "B."

Switches A1 through B4 are defined as follows:

A1 ON Execute CPU tests on power-up or restart.
A2 ON Execute memory test on power-up or restart.
A3 ON DECNET BOOT - A4, A5, A6, A7 are used as arguments.

Device	A4	A5	A6	A7
DUV11	ON	OFF	OFF	OFF
DLV11-E	OFF	ON	OFF	OFF
DLV11-F	OFF	ON	OFF	ON

DLV11-E RCSR = 175610; DLV11-F RCSR = 176500.

A4 ON Console test and dialog (A3 OFF).
A4 OFF Turnkey BOOT dispatched by switch setting (A3 OFF). Switches A5, A6, A7, A8, B1 are used as arguments.

Device	A5	A6	A7	A8	B1
Loop on Error	OFF	OFF	OFF	OFF	ON
RK05	OFF	OFF	OFF	ON	OFF
RL01	OFF	OFF	ON	OFF	OFF
RX01	OFF	ON	OFF	OFF	OFF
RX02	OFF	ON	ON	OFF	OFF
BDV11 ROM	ON	OFF	OFF	OFF	OFF

The BDV11 ROM BOOT uses the following switches as arguments. (X = don't care.)

ROM	B2	B3	B4
Extended DIAG	ON	X	X
2708s	OFF	ON	X
Program ROM	OFF	OFF	ON

All unused patterns or mnemonics will default to ROM BOOT if switch B2, B3, or B4 is ON.

If an unrecognized mnemonic or switch setting (A5 through B1) is encountered, the presence of additional ROM is checked (by checking B2, 3, 4) and if present, the ROM BOOT is envoked.

If an unrecognized switch setting is encountered, a copy of the switches is placed in location 2 with bit 15 set.

If no additional ROM exists, the switch checking routine will halt or the mnemonic routine will reprompt.

If the console test is selected, the console test prompts with:

ZZK Where ZZ is the decimal multiple of 1024.
START? Words of RAM found in the system.

Allowed responses are a two-character mnemonic with a one-digit octal unit number, or one of two special, single-character mnemonics. The response must be followed by a return. The special single-character mnemonics are:

Y Use switch settings to determine boot device; or,
N HALT. Enter microcode ODT.

The two-character mnemonics are as follows. "N" is a digit from 1 to 7 indicating the unit number of the device.

DKN	RK05 bootstrap
DLN	RL01 bootstrap
DXN	RX01 bootstrap
DYN	RX02 bootstrap

BDV11 HALT/ENABLE, RESTART, AND BEVNT SWITCHES

HALT/ENABLE Switch

When this switch is in the ENABLE position, the LSI-11 CPU can operate under program control. If the switch is placed in the HALT position, the CPU enters the halt mode and responds to console ODT commands. While in the halt mode, the CPU can execute single instructions, facilitating maintenance of the system. Program control is re-established by returning the switch to the ENABLE position and entering a "P" command at the console terminal (providing the contents of register R7 were not changed). Refer to chapter 2 of the *Microcomputer Handbook* (1977-1978) for a description of console ODT command usage.

RESTART Switch

When the RESTART switch is cycled, i.e., moved from one side to the other and back, the CPU automatically carries out a power-up sequence. Thus, the system can be rebooted at any time for maintenance purposes.

BEVNT L Switch

Contact 5 of dip-socket switch E21 is the BEVNT L switch. When the switch is off (open) the LSI-11 bus BEVNT L signal can be controlled by the power-supply-generated LTC signal. When the switch is on (closed), the LTC function is program controlled; i.e., a single-bit write-only register in the logic (address 177546, bit 6) clamps BEVNT L low when the register is cleared. (The register is automatically cleared when the power is turned on or when the RESTART switch is cycled.) The KW11-L line time clock option also uses bit 6 as the enable bit.

POWER OK LED and Tip Jacks

This green LED is lighted when the +12 Vdc supply voltage is greater than +10 V and the +5 Vdc supply voltage is greater than +4 V. The +12 Vdc voltage and the +5 Vdc voltage can be measured at the tip jacks as indicated below. (Both J2 and J3 have a 560 Ω resistor in series to prevent damage from a short circuit; use at lease a 20,000 Ω V meter to measure the voltage.)

Jack	Color	Voltage
J1	Black	Ground
J2	Red	+5 Vdc
J3	Purple	+12 Vdc

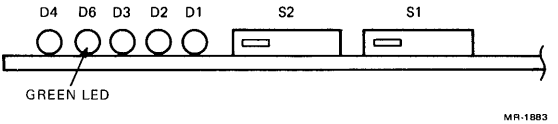
Secondarily, the LED indicates the octal point for the diagnostic light display.

The BDV11 (M8012) is the new bootstrap module for the PDP-11/03s. It is a quad module and it has 2K words of diagnostics in ROM installed on the board. The failures of these diagnostics are indicated by the HALT address in the ROM and by the state of the error lights on the board.

The "Diagnostic LED Error Display" table provides a cross-reference between the indications in the error lights and the failing system function. The "BDV11 Diagnostic Error Addresses" table provides a cross-reference between the HALT PC and the failing system function. (The HALT PC will be displayed on the console terminal.)

Diagnostic LED Error Display

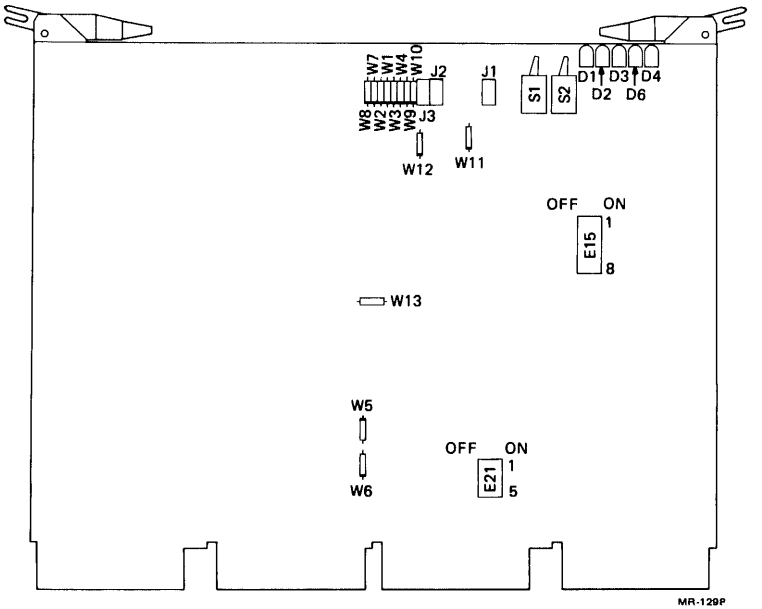
D4 Red	D6 Green DC OK	D3 Red	D2 Red	D1 Red	Comments
X	OFF	X	X	X	+12 Vdc or +5 Vdc is bad.
OFF	ON	OFF	OFF	ON	CPU test error or fault, or configuration error.
OFF	ON	OFF	ON	OFF	Memory test error; register R1 points to bad location.
OFF	ON	OFF	ON	ON	Console serial line unit does not transmit.
OFF	ON	ON	OFF	OFF	Console terminal test waiting for response from operator on keyboard.
OFF	ON	ON	OFF	ON	Load device status error.
OFF	ON	ON	ON	OFF	Secondary bootstrap code incorrect. NOP instruction is not in location 000000; the medium is probably bad.
OFF	ON	ON	ON	ON	DECNET waiting for response from host computer.
ON	ON	OFF	OFF	OFF	DECNET received DONE FLAG set.
ON	ON	OFF	OFF	ON	DECNET message received.
ON	ON	OFF	ON	OFF	ROM BOOTSTRAP error.
ON	ON	ON	ON	ON	HALT switch is ON, unable to run (check computer and BDV11 HALT switch); or power-up mode is wrong; or system is hung.



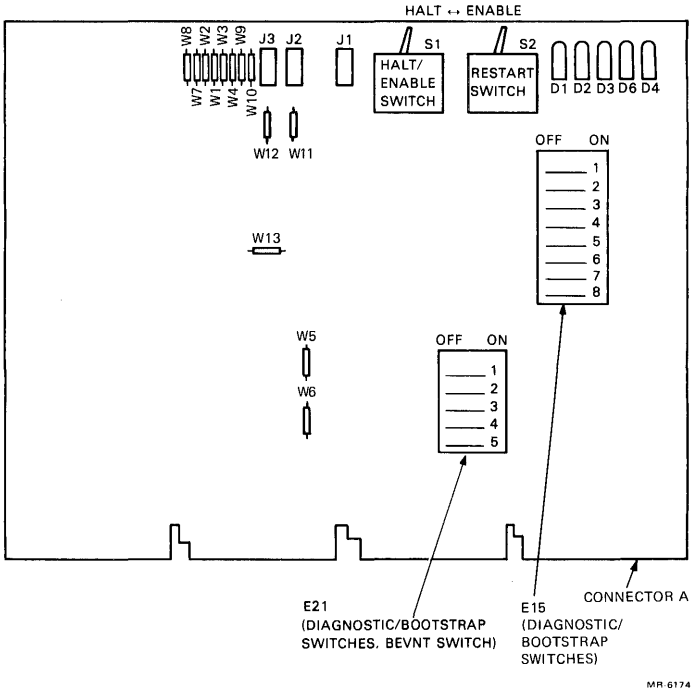
Diagnostic LED Error Display

BDV11 Diagnostic Error Addresses

Error Address	Cause of Error
173022	Memory error 1. Write address into itself.
173040	Serial line unit switch selection incorrect; error in switches.
173046	Serial line unit error. CSR address for selected device in error. Check CSR for selected device in floating CSR address area.
173050	CPU error 1. Register R0 contains address of error.
173052	Memory error 2. Data test failed.
173106	Memory error 3. Write and read bytes failed.
173202	ROM loader error. Checksum on data block.
173240	CPU error 4. R0 contains address of error.
173366	ROM loader error. Checksum on address block.
173402	ROM loader error. Jump address is odd.
173532	RL device error.
173634	CPU error 3. R0 points to cause of error.
173642	A "NO" typed in console terminal test.
173656	Switch mode HALT. A match was not made with switches.
173656	RK device error
173670	Console terminal test. No DONE flag.
173706	CPU error 2. R0 points to cause of error.
173712	RX device error



BDV11 Switch and Jumper Locations



BDV11 Switches and Indicators

Socket Selection Logic

The socket selection logic determines which pair of sockets responds to the ROM address signals. (Although the ROMs in the sockets actually respond, it is said, for ease of explanation, that the sockets respond).

Jumpers are inserted selectively in positions W1-W4 and W9-W12. These jumpers cause the PCR page numbers and the selection signals (and, therefore the sockets) to be related in definite ways. Group A in the "BDV11 Selection Signals/Sockets" table indicates that PCR pages are assigned to specific ROM sockets. This is true within the confines of the BDV11 module shipped by DIGITAL. On such a module, jumpers W1-W4 and W9-W12 are arranged as indicated under Group A in the table. Thus, the PCR pages 0-17, for example, cause selection signal SB1 L to be asserted, and SB1 L causes sockets XE53 and XE48 to respond to address signals A<0:10> H. Other combinations of jumpers are possible, as indicated by Groups B through G in the table. Note that each selection signal always selects the same pair of sockets; however, the relation of PCR pages to selected sockets varies with jumper configuration.

Group	W1	W2	W3	W4	W9	W10	W11	W12	PCR Page	Primary Selection Signal	Addresses (A<0:14>H)	Sockets Selected
A	R	I	I	R	I	R	R	I	0-17	SB1 L	0K-2K	XE53/XE48
									20-37	SB2 L	2K-4K	XE58/XE44
									40-47	SE1 L	4K-5K	XE57/XE40
									50-57	SE2 L	5K-6K	XE52/XE36
									360-377	SP1 L	30K-32K	XE39/XE50
									340-357	SP2 L	28K-30K	XE43/XE46
									320-337	SP3 L	26K-28K	XE47/XE42
									300-317	SP4 L	24K-26K	XE51/XE38
									260-277	SP5 L	22K-24K	XE55/XE37
									240-257	SP6 L	20K-22K	XE60/XE41
									220-237	SP7 L	18K-20K	XE59/XE45
									200-217	SP8 L	16K-18K	XE54/XE49
B	*	*	*	*	I	R	I	R	40-57	SB1 L	4K-6K	XE53/XE48
									60-77	SB2 L	6K-8K	XE58/XE44
									0-7	SE1 L	0K-1K	XE57/XE40
									10-17	SE2 L	1K-2K	XE52/XE36
C	*	*	*	*	R	I	R	I	200-217	SB1 L	16K-18K	Ibid.
									220-237	SB2 L	18K-20K	
									240-247	SE1 L	20K-21K	
									250-257	SE2 L	21K-22K	
D	*	*	*	*	R	I	I	R	240-257	SB1 L	20K-22K	Ibid.
									260-277	SB2 L	22K-24K	
									200-207	SE1 L	16K-17K	
									210-217	SE2 L	17K-18K	

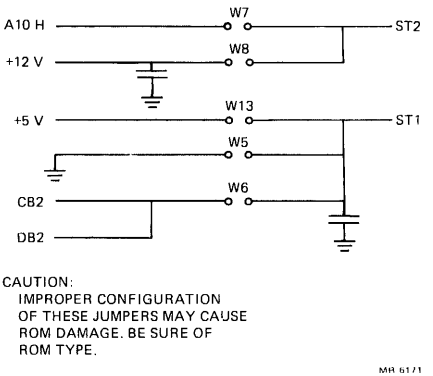
BDV11 Selection Signals/Sockets (Cont)

Group	W1	W2	W3	W4	W9	W10	W11	W12	PCR Page	Primary Selection Signal	Addresses (A<0:14>H)	Sockets Selected
E	I	R	I	R	*	*	*	*	270-277	SP1 L	23K-24K	XE39/XE50
									250-257	SP2 L	21K-22K	XE43/XE46
									230-237	SP3 L	19K-20K	XE47/XE42
									210-217	SP4 L	17K-18K	XE51/XE48
									260-267	SP5 L	22K-23K	XE55/XE37
									240-247	SP6 L	20K-21K	XE60/XE41
									220-227	SP7 L	18K-19K	XE59/XE45
									200-207	SP8 L	16K-17K	XE54/XE49
F	R	I	R	I	*	*	*	*	160-177	SP1 L	14K-16K	Ibid.
									140-157	SP2 L	12K-14K	
									120-137	SP3 L	10K-12K	
									100-117	SP4 L	8K-10K	
									60-77	SP5 L	6K-8K	
									40-57	SP6 L	4K-6K	
									20-37	SP7 L	2K-4K	
									0-17	SP8 L	0K-2K	
G	I	R	R	I	*	*	*	*	70-77	SP1 L	7K-8K	Ibid.
									50-57	SP2 L	5K-6K	
									30-37	SP3 L	3K-4K	
									10-17	SP4 L	1K-2K	
									60-67	SP5 L	6K-7K	
									40-47	SP6 L	4K-5K	
									20-27	SP7 L	2K-3K	
									0-7	SP8 L	0K-1K	

I = inserted; R = removed.

ROM Sockets Logic

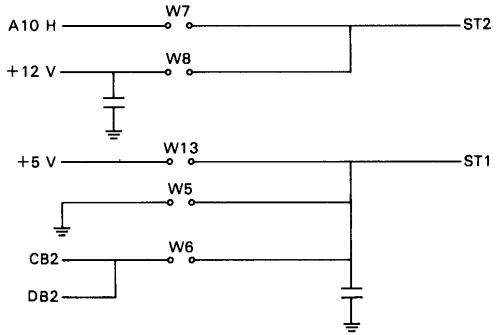
The following figure represents the ROM sockets and shows the address signals and enabling signals for each functional group of sockets. The diagnostic/bootstrap ROM sockets (which are selected by signals SB1 L and SB2 L) are supplied with 11 address bits, since these sockets are reserved for 2K-word ROMs. The EPROM sockets (selected by signals SE1 L and SE2 L) are reserved for 1K ROMs; therefore, these sockets are supplied with 10 address bits. The system ROM sockets can be occupied by either 2K ROMs or 1K ROMs; five jumpers on the BDV11 module permit ROMs of either size to be used.



The following figure shows how these five jumpers control the selection signals for the system ROM sockets, and relates the jumpers to the types of ROM that can be used in the BDV11. (If ROMs other than 8316E, 2716, and 2708 are used, do not alter configuration. See Caution.)

CAUTION

Improper configuration of these jumpers may cause ROM damage. Be sure of ROM type.



ROM TYPE	JUMPERS INSERTED[1]				
	W5	W6	W7	W8	W13
2708[2]	R	I	R	I	R
2716	R	R	I	R	I
8316E[3]	I	R	I	R	R
8316E[4]	R	R	I	R	I

1. I=INSERTED; R=REMOVED
2. CB2 AND DB2 MUST BE SUPPLIED WITH EXTERNAL -5V POWER.
3. CHIP SELECT SIGNALS MUST BE PROGRAMMED AS FOLLOWS:

CS1	CS2	CS3
LOW	LOW	LOW

4. CHIP SELECT SIGNALS MUST BE PROGRAMMED AS FOLLOWS:

CS1	CS2	CS3
LOW	LOW	HIGH

MA-1351

M8013, M8014 RLV11 CONTROLLER

Amps		Bus Loads		Cables
+5	+12	AC	DC	BC08R-XX
6.5	1.0	3.2	1	70-12122 (1 per drive)

Transition Bracket Assembly 70-12415-00
Terminator 70-12293-00

Standard Addresses

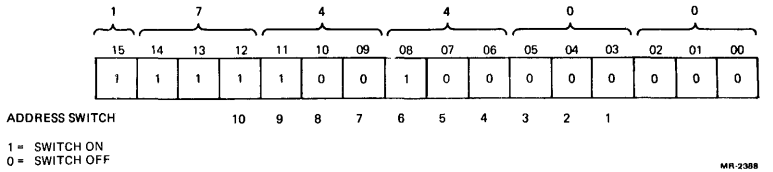
CSR	174400
BAR	174402
DAR	174404
MPR	174406

Standard Vectors

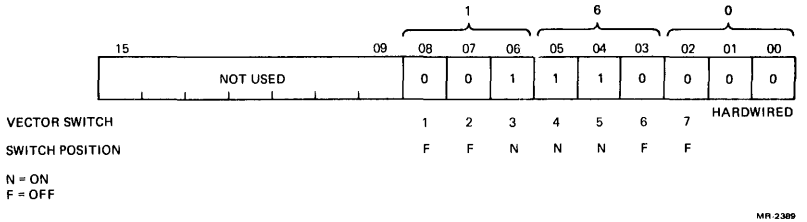
160

Diagnostic Programs

Refer to Appendix A.



Address Selection



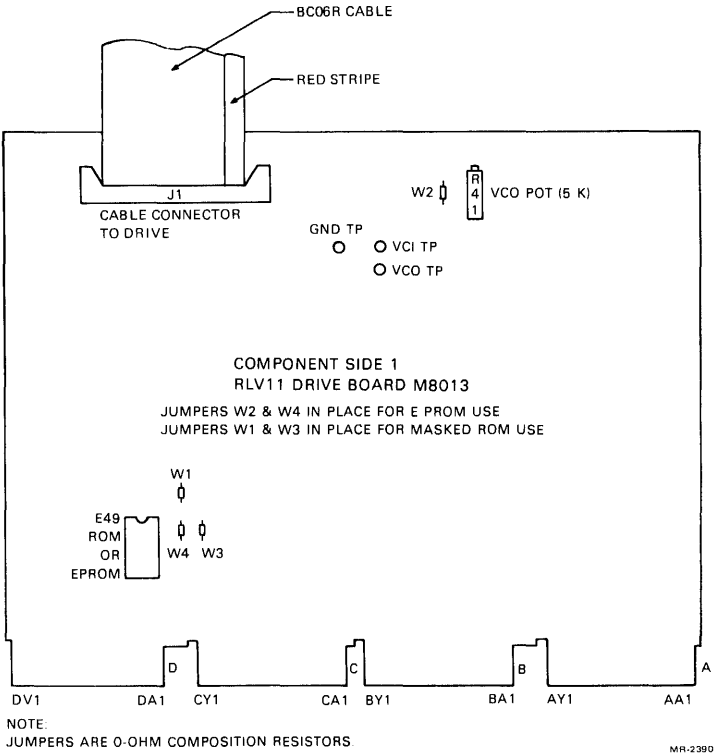
Vector Selection

Related Documentation

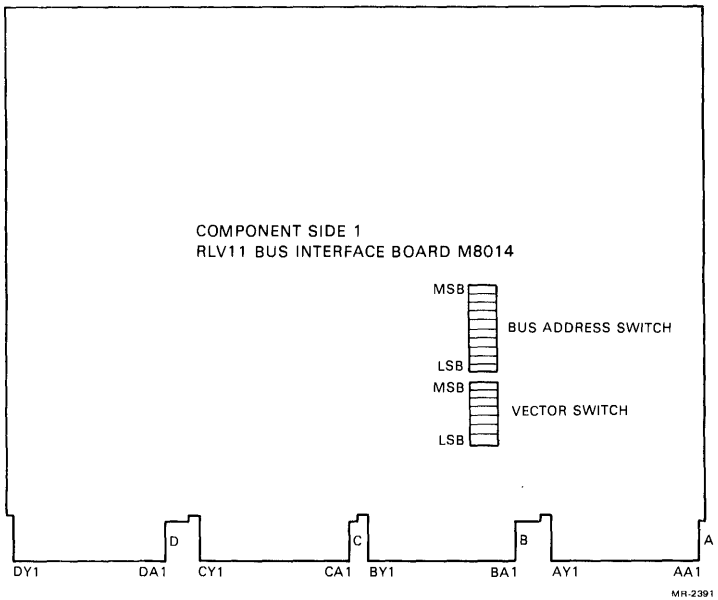
RLV11 Controller Technical Description Manual (EK-RLV11-TD)
RLV11 Field Maintenance Print Set (MP00635)
RL01 Field Maintenance Print Set (MP00347)
RL02 Field Maintenance Print Set (MP00553)
RL01 Disk Drive IPB (EK-ORL01-IP)
RL02 Disk Drive IPB (EK-ORL02-IP)
RL01/RL02 User's Guide (EK-RL012-UG)
RL01/RL02 Pocket Service Guide (EK-RL012-PG)
Microcomputer Interfaces Handbook (EB-20175-20)

NOTE

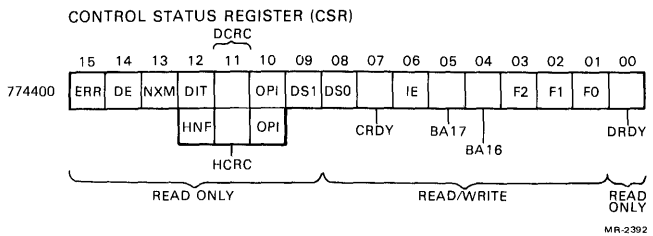
The M8013 must be installed above the M8014. The RLV11 controllers can only be used in a backplane built as an H9273 (slots A and B = LSI bus and slots C and D = interboard bus). The BA11-N box currently is the only box that contains an H9273 backplane.



RLV11 Drive Module (M8013)



RLV11 Bus Interface Module (M8014)



Control Status Register

CSR Bit Definitions

Bit **Function**

0 Drive Ready (DRDY) - When set, this bit indicates that the selected drive is ready to receive a command (no seek operation in progress). The bit is cleared when a seek operation is initiated and set when the seek operation is completed.

1-3 Function Code - These bits are set by software to indicate the command to be executed.

F2	F1	F0	Command	Octal Code
0	0	0	MAINTENANCE MODE	0
0	0	1	WRITE CHECK	1
0	1	0	GET STATUS	2
0	1	1	SEEK	3
1	0	0	READ HEADER	4
1	0	1	WRITE DATA	5
1	1	0	READ DATA	6
1	1	1	READ DATA WITHOUT HEADER CHECK	7

Command execution starts when CRDY (bit 7) of the CSR is cleared by software. In a sense, bit 7 can be considered a negative go bit.

4-5 Bus Address Extension Bits (BA15, BA17) - Two most significant bus address bits. Read and written as bits 4 and 5 of the CSR, they function as address bits 16 and 17 of the BAR.

6 Interrupt Enable (IE) - When this bit is set by software, the controller is allowed to interrupt the processor at the assertion of CRDY. This occurs at the normal or error termination of a command. Once an interrupt request is posted on the LSI bus, it is not removed until serviced even if IE is cleared.

CSR Bit Definitions (Cont)

Bit	Function
7	Controller Ready (CRDY) - When cleared by software, this bit indicates that the command in bits 1-3 is to be executed. Software cannot set this bit because no registers are accessible while CRDY is 0. When set, this bit indicates that the controller is ready to accept another command.
8-9	Drive Select (DS0, DS1) - These bits determine which drive will communicate with the controller via the drive bus.
10	Operation Incomplete (OPI) - When set, this bit indicates that the current command was not completed within the OPI timer period.
11	Data CRC (DCRC) or Header CRC (HCRC) or Write Check (WCE) - If OPI (bit 10) is cleared and bit 11 is set, the CRC error occurred on the data (DCRC). If OPI (bit 10) is set and bit 11 is also set, the CRC error occurred on the header (HCRC). If OPI (bit 10) is cleared and bit 11 is set and the function command was a write check, a write check error (WCE) has occurred.

NOTE

Cyclic redundancy checking is done only on the desired header. It is performed on the first and second header words, even though the second header word is always 0.

12	Data Late (DLT) or Header Not Found (HNF Error) - When OPI (bit 10) is cleared and bit 12 is set, it indicates that a data late condition occurred on a read without header check operation. One of two conditions exists: **Write Operation –** The silo is empty, but the word count has not reached zero. (Bus request was ignored for too long.) **Read Operation –** The silo is full (word being read could not enter the silo and the bus request was ignored too long.) When OPI (bit 10) is set and bit 12 is also set, it indicates that a timeout occurred while the controller was searching for the correct sector to read or write (no header; compare [NHF]).

CSR Bit Definitions (Cont)

Bit **Function**

Error Summary

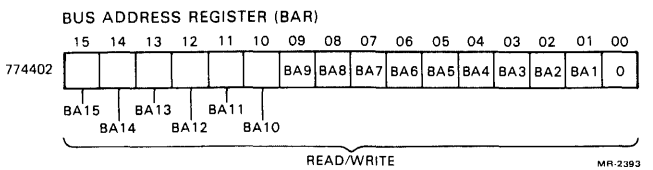
Error	Bit 12	Bit 11	Bit 10	Comments
OPI	0	0	1	200 ms timeout
DCRC	0	1	0	
WCE	0	1	0	Function command is a write check.
HCRC	0	1	1	
DLT	1	0	0	
HNF	1	0	1	

13 Nonexistent Memory (NXM) - When set, this bit indicates that during a DMA data transfer, the memory location addressed did not respond within 14 ms.

14 Drive Error (DE) - This bit is buffered from the drive error interface line. When set, it indicates that the selected drive has flagged an error, the source of which can be determined by executing a GET STATUS command.

To clear the drive error bit, execute a GET STATUS command with bit 3 of the DAR.

15 Composite Error (ERR) - When set, this bit indicates that one or more of the error bits (bits 10-14) is set. When an error occurs, the current operation terminates and an interrupt routine is initiated if the interrupt enable bit (bit 6 of the CSR) is set.



Bus Address Register

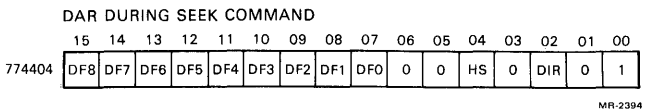
BAR Bit Definitions

The Bus Address Register (BAR) is a 16-bit word-addressable register with an address of 774 402. Bits 0 through 15 can be read or written; bit 0 should normally be written 0. Expansion bits 16 and 17 are programmable via bits 4 and 5 of the CSR.

The bus address register indicates the memory location involved in the DMA data transfer during a read or write operation. The contents of the BAR are automatically incremented by 2 as each word is transferred between system memory and controller in either direction. Clear the BAR by executing a BUS INIT.

Disk Address Register (DAR)
The Disk Address Register (DAR) is a 16-bit read/write word-addressable register with an address of 774 404. Its contents can have one of three meanings, depending on the function being performed. Clear this register by executing a BUS INIT.

DAR During a SEEK Command – To perform a seek function, it is necessary to provide address difference, head select, and head directional information to the selected drive.

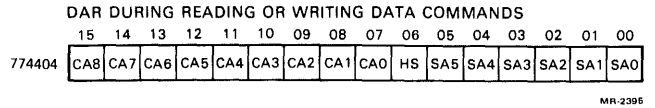


DAR SEEK Command

Bit Definitions

Bits	Function
0	Marker (MRKR) - Must be a 1.
1	Must be a 0, indicating to the drive that a SEEK command is being requested and that the remaining bits in the register will contain the seek specifications.
2	Direction (DIR) - This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 7-14).
3	Must be a 0.
4	Head Select (HS) - Indicates which head (disk surface) is to be selected. Set = lower; clear = upper.
5-6	Reserved.
7-14	Cylinder Address Difference (DF<8:0>) - Indicates the number of cylinders the heads are to move on a seek.
15	Must be a 0.

DAR During READ or WRITE DATA Command – For a read, write, or write check operation, the DAR is loaded with the address of the first sector to be transferred. Thereafter, as each adjoining sector is transferred, the DAR is automatically incremented by 1. If the DAR increments to the nonexistent sector address 50_8, an OPI timeout will occur. The drive must then seek to a new track if the transfer is to continue.

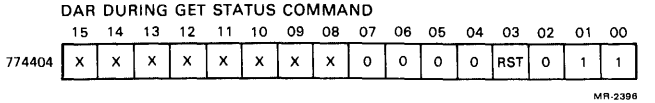


DAR READ/WRITE DATA Command

Bit Definitions

Bit	Function
0-5	Sector Address (SA<5:0>) - Address of one of the 40 sectors on a track. (Octal range is 0 to 47.)
6	Head Select (HS) - Indicates which head (disk surface) is to be selected. Set = lower; clear = upper.
7-14	Cylinder Address (CA<8:0>) - Address of one of the 256 cylinders. (Octal range is 0 to 377.)
15	Must be a 0.

DAR During a GET STATUS Command – After the GET STATUS command is deposited in the CSR, it is the DAR's responsibility to get the command transferred to the drive. Therefore, the DAR must also be programmed along with the CSR to do the GET STATUS command.



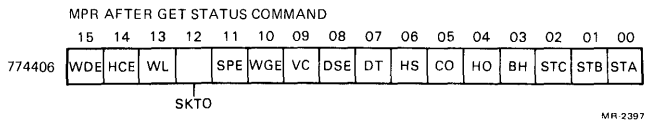
DAR GET STATUS Command

For a GET STATUS command, the DAR register bits must be programmed as follows.

DAR Register Bits for a GET STATUS Command

Bit	Function
0	Marker (MRKR) - Must be a 1.
1	Get Status (GS) - Must be a 1, indicating to the drive that its status word is being requested. At the completion of the GET STATUS command, the drive status word is read into the controller multipurpose (MP) register (output stage of FIFO). With this bit set, bits 8-15 are ignored by the drive.
2	Must be a 0.
3	Reset (RST) - When this bit is set, the drive clears its error register of soft errors before sending a status word to the controller.
4-7	Must be a 0.
8-15	Not used.

Multipurpose Register (MPR)
The MPR is two registers bearing the same base address. When writing into that location, the word counter accepts the data. When reading from that location, the FIFO output buffer provides the data.



MPR Status Word

MPR After a GET STATUS Command – When a GET STATUS command is executed and a status word is returned to the controller, the contents of the MPR (FIFO output stage) are defined as follows.

Bits 0-2 - State<C:A) (ST<C:A>) - These bits define the state of the drive.

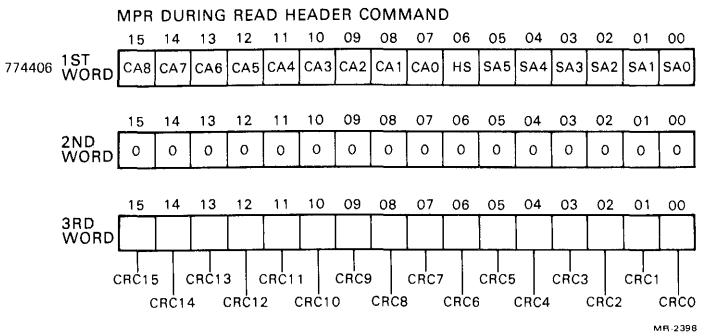
Bits			Definition
C	B	A	
0	0	0	Load Cartridge
0	0	1	Spin Up
0	1	0	Brush Cycle
0	1	1	Load Heads
1	0	0	Seek Track Counting
1	0	1	Seek Linear Mode (Lock On)
1	1	0	Unload Heads
1	1	1	Spin Down

Bit Definitions

Bit	Function
3	Brush Home (BH) - Asserted when the brushes are not over the disk.
4	Heads Out (HO) - Asserted when the heads are over the disk.
5	Cover Open (CO) - Asserted when the cover is open or the dust cover is not in place.
6	Head Select (HS) - Indicates the currently selected head.
7	Drive Type (DT) - Set = lower; clear = upper. Set = RL02; clear = RL01.
8	Drive Select Error (DSE) - Indicates that multiple drive selection was detected.
9	Volume Check (VC) - VC is set every time the drive goes into load heads state. This asserts a drive error at the controller but not on the front panel. VC is an indication that the program does not really know which disk is present until it has read the serial number and bad sector file. (The disk might have been changed while the heads were unloaded.)
10	Write Gate Error (WGE) - Indicates that the drive sensed that write gate was asserted when sector pulse was asserted, or write gate was set with the drive not ready, or the drive was write locked.

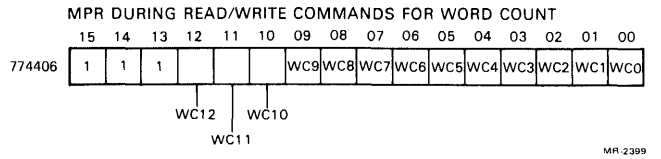
Bit Definitions (Cont)

Bit	Function
11	Spin Error (SPE) - Indicates that the spindle did not reach speed in the required time; or indicates over speeding.
12	Seek Time Out (SKTO) - Indicates that the heads did not come on track in the required time during a SEEK command or loss of "ready to read/write during lock on" mode.
13	Write Lock (WL) - Indicates write lock status of selected drive. Set = write protected.
14	Head Current Error (HCE) - Indicates that write current was detected in the heads when write gate was not asserted.
15	Write Data Error (WDE) - Indicates that write gate was asserted but no transitions were detected on the write data line.



MPR Three Header Words

MPR After a Read Header Command – When a READ HEADER command is executed, three words will be stored in the multipurpose register (FIFO output buffer). The first header word will contain sector address (SA0:SA5), head select (HS - set = lower; clear = upper), and cylinder address information (CA0:CA8). The second word will contain all 0s. The third word will contain the header CRC information. All three words are readable by the main program.



MPR Used As Word Counter

Bit Definitions

Bit	Function
0-12	Word Count (WC<12:0>) - 2's complement of total number of words to be transferred.
13-15	Must be a 1 for word count in correct range.

MPR During READ/WRITE DATA Commands – When transferring data via DMA, the MPR functions as a word counter and is loaded by program with the 2's complement of the number of words to be transferred. It is then incremented by 1 by the controller as each word is transferred. The reading or writing operation generally is terminated when the word counter overflows. The word counter can keep track of from one data word to the full 40-sector count of 5120 data words (decimal). The maximum number of words that can be transferred in a single operation is limited by the number of sectors available to be written in the track.

NOTE

The RL01/RL02 disk drive will not do spiral read/writes. If data is to be transferred past the end of the last sector of a track, it is necessary to break up the operation into the following steps.

1. **Program the data transfer to terminate at the end of the last sector of the track.**

2. **Program a seek to the next track. This can be accomplished either by a head switch to the other surface but the same cylinder, or a head switch to move to the next cylinder.**

3. **Program the data transfer to continue at the start of the first sector on the next track.**

M8016
KPV11-A (M8016) POWER FAIL/LINE TIME CLOCK
KPV11-B (M8016-YB) KPV11-A + 120 Ω TERMINATOR
KPV11-C (M8016-YC) KPV11-A + 250 Ω TERMINATOR

Amps 24 V		Bus Loads		Cables
+5	+12	AC	DC	
0.11	0.82	1.6	1.0	70-12754 (for remote operation)

Standard Address

LKS 177546

Standard Vector

LTC 100

Diagnostic Programs

Refer to Appendix A.

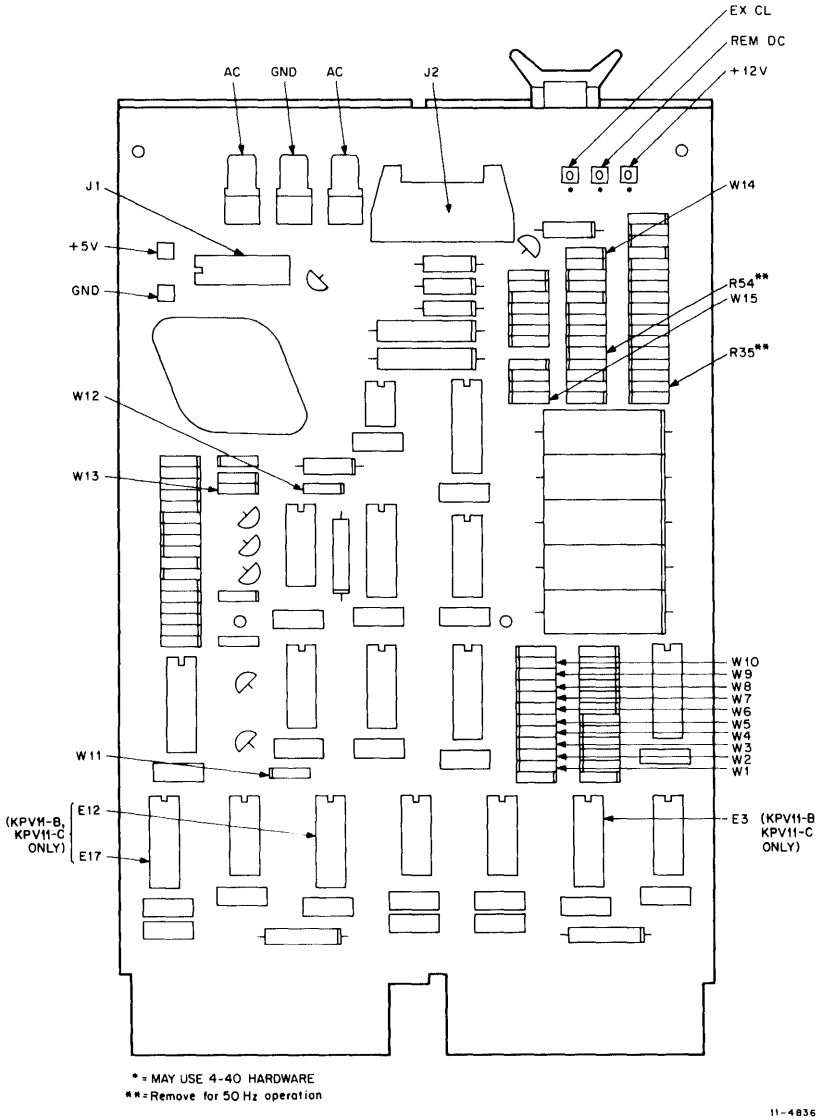
Related Documentation

Field Maintenance Print Set (MP00356)
Microcomputer Interfaces Handbook (EB-20175-20)

Options to KPV11

DEC PN	Description
54-11808	Console panel printed circuit board assembly
70-11656	Console bezel (dress panel)
70-08612	Console signal/power cable (required for optional console panel use)

M8016


EX CL
REM DC
+12V
AC
GND
AC
J2
J1
+5V
GND
W14
R54**
W15
R35**
W12
W13
W10
W9
W8
W7
W6
W5
W4
W3
W2
W1
W11
(KPVM-B, KPV11-C ONLY)
E12
E17
E3 (KPV11-B KPV11-C ONLY)
* = MAY USE 4-40 HARDWARE
** = Remove for 50 Hz operation
11-4836

KPV11 Factory Jumper Configuration

Jumper Designation	Jumper State	Function Implemented
W1	I	Sets address of line time clock status register (LKS) to 177546.
W2	I	
W3	I	
W4	I	
W5	I	
W6	R	
W7	I	
W8	I	
W9	R	
W10	R	
W11	-	Do not change. Must be installed for proper terminator function on KPV11-B and KPV11-C.
W12	R	Disables continuous or manual control of LTC interrupt request operation. Do not install when W13 is installed.
W13	I	LTC interrupt requests can be enabled and disabled by program. Do not install when W12 is installed.
W14	I	Console (optional) LTC ON/OFF switch enabled.
W15	I	LTC signal occurs at the power line frequency.

NOTES

1. Line Time Clock (LTC) controls

Function	W12	W13
disable LTC	I	R
enable LTC and enable LTC program control	R	I
enable LTC and disable LTC program control	R	R

2. LTC Remote Console Switch

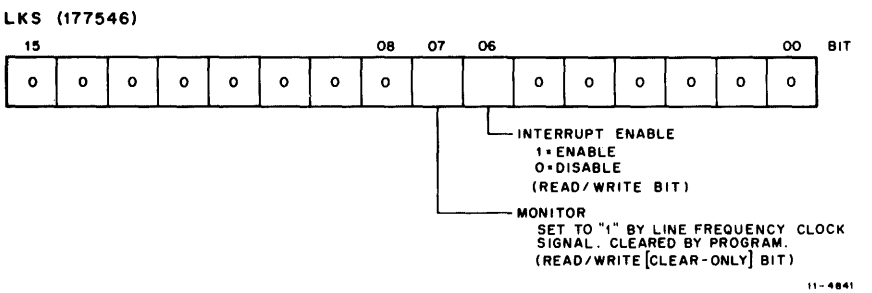
Function	W14
console switch enabled	I
console switch disabled	R

3. Select LTC Frequency

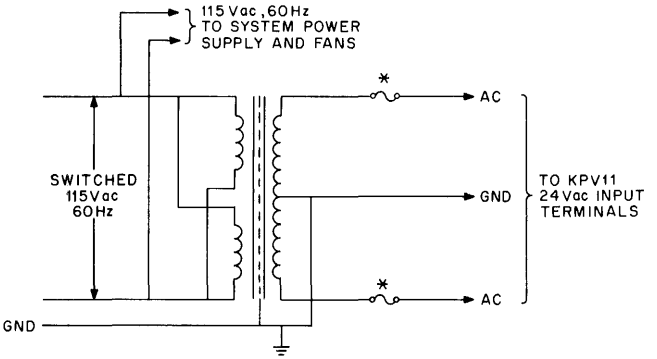
Function	W15
LTC signal occurs at line frequency	I
LTC signal occurs at frequency inserted at EXT TIME REF	R

4. External Transformer

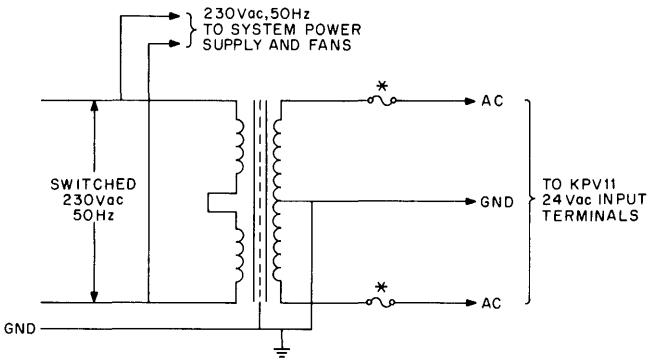
The user must supply a 24 Vac, 200 mA center tapped transformer to be connected to the two ac and the ground tabs on the top of the module. If a transformer capable of supplying more than 200 mA is used, current limiting in the form of a fuse must be used to protect the KPV11-A module.



Line Time Clock Status Register (LKS)



(A) 115V CONNECTIONS (TYPICAL)



(B) 230V CONNECTIONS (TYPICAL)

*1 AMP FAST BLOW FUSES ARE RECOMMENDED ON THE AC INPUT LINES TO PROVIDE ADEQUATE PROTECTION TO THE KPV11.

11-4839

Power Line Monitor Transformer Installation

M8017
DLV11-E ASYNCHRONOUS SERIAL LINE INTERFACE

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.0	0.15 (0.20 max.)	1.26	1	BC05C

Standard Address

RCSR	175610
RBUF	175612
XCSR	175614
XBUF	175616

NOTE
The DLV11-E is shipped configured for use with a modem.

Standard Vectors

Floating - Configurable within the range of 000-770. Refer to Appendix B.

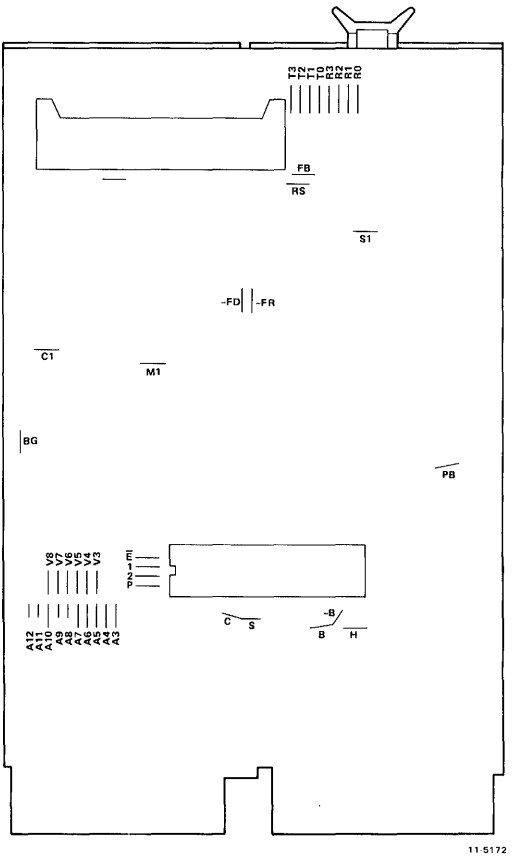
		MINC/DECLAB
Receiver Interrupt	300	330
Transmitter Interrupt	304	334

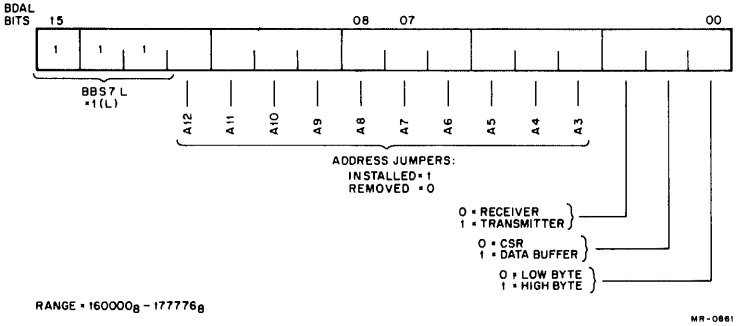
Diagnostic Programs

Refer to Appendix A.

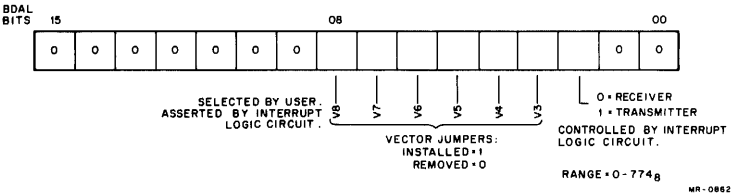
Related Documentation

DLV11-E and DLV11-F Asynchronous Line Interface User's Manual (EK-DLV11-OP)
Field Maintenance Print Set (MP00460)
Microcomputer Interfaces Handbook (EB-20175-20)


T3
T2
T1
T0
R3
R2
R1
R0
FB
RS
S1
-FD
-FR
C1
M1
BG
PB
V8
V7
V6
V5
V4
V3
E
1
2
P
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
C
S
-B
B
H
11-5172



DLV11-E Addresses



DLV11-E Interrupt Vectors

Unit	Address	Address Jumpers									
		A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
Console	177560	R	I	I	I	R	I	I	I	I	I
First Option	176500	R	R	R	I	R	I	R	I	I	I
Second Option	176510	I	R	R	I	R	I	R	I	I	I
Third Option	176520	R	I	R	I	R	I	R	I	I	I
Modem	175610	I	R	R	R	I	I	I	R	I	I

Unit	Vector	Vector Jumpers					
		V3	V4	V5	V6	V7	V8
Console	60	R	I	I	R	R	R
First Option	300	R	R	R	I	I	R
Second Option	310	I	R	R	I	I	R
Third Option	320	R	I	R	I	I	R
Modem	300	R	R	R	I	I	R

Jumper Configuration When Shipped

Jumper Designation	Jumper State	Function Implemented
A3	I	Jumpers A3 through A12 implemented device address 17561X. The least significant octal digit is hardwired on the module to address the four device registers as follows.
A4	R	
A5	R	
A6	R	
A7	I	
A8	I	X = 0 RCSR
A9	I	X = 2 RBUF
A10	R	X = 4 XCSR
A11	I	X = 6 XBUF
A12	I	
V3	R	This jumper selection implements interrupt vector address 300 for receiver interrupts and 304 for transmitter interrupts.
V4	R	
V5	R	
V6	I	
V7	I	
V8	R	
R0	I	The module is configured to receive at 100 baud (see "Baud Rate Selection" table, which follows).
R1	R	
R2	I	
R3	I	
T0	I	The transmitter is configured for 9600 baud if split speed operation is used.
T1	R	
T2	R	
T3	R	
BG	I	Break generation is enabled.

Jumper Configuration When Shipped (Cont)

Jumper Designation	Jumper State	Function Implemented
P	R	Parity bit is disabled.
E	R	Parity type is not applicable when P is removed.
1 2	R R	Operation with eight data bits per character (see "Data Bit Selection" table, which follows).
PB	R	Programmable baud rate function disabled.
C C1	I I	Programmable baud rate function disabled. Common speed operation enabled.
S S1	R R	Split speed operation disabled.
H	R	Halt on framing error disabled.
B -B	R I	Boot on framing error disabled.
-FD	I	The DATA TERMINAL READY signal is not forced continuously true.
-FR	I	The REQUEST TO SEND signal is not forced continuously true.
RS	I	The circuitry controlling the REQUEST TO SEND signal is enabled.
FB	R	The FORCE BUSY signal is disabled.
M M1	R R	Factory test jumpers. Not defined for field use.

Baud Rate Selection

	Bit	Bit	Bit	Bit	Bit	Baud Rate
Program Control	15	14	13	12	11*	
Receive Jumpers	R3	R2	R1	R0		
Transmit Jumpers	T3	T2	T1	T0		
	I	I	I	I		50
	I	I	I	R		75
	I	I	R	I		110
	I	I	R	R		134.5
	I	R	I	I		150
	I	R	I	R		300
	I	R	R	I		600
	I	R	R	R		1200
	R	I	I	I		1800
	R	I	I	R		2000
	R	I	R	I		2400
	R	I	R	R		3600
	R	R	I	I		4800
	R	R	I	R		7200
	R	R	R	I		9600

I = jumper inserted = program bit cleared.
R = jumper removed = program bit set.

*Bit 11 of the XCSR (write-only bit) must be set in order to select a new baud rate under program control. Jumper PB must be inserted to enable baud rate selection under program control.

Data Bit Selection

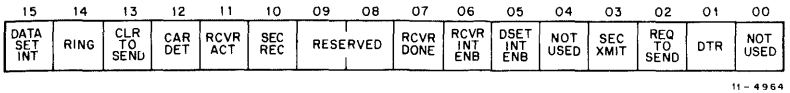
Jumpers 2	1	Number of Data Bits
I	I	5
I	R	6
R	I	7
R	R	8

Jumper Definitions

Jumper	Function
A3-A12	These jumpers correspond to bits 3-12 of the address word. When inserted, they will cause the bus interface to check for a true condition on the corresponding address bit.
V3-V8	Used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding address bit on the LSI-11 bus.
R0-R3	Receiver and transmitter baud rate jumpers selected during common speed operation. Receiver-only baud rate select jumpers used during split speed operation.
T0-T3	Transmitter baud rate select jumpers used during split speed operation. Both receiver and transmitter baud rates used if maintenance mode is entered during split speed operation.
BG	Jumper is inserted to enable break generation.
P	Jumper is inserted for operation with parity.
E	Removed for even parity; inserted for odd parity. Receive checks for appropriate parity and transmitter inserts appropriate parity.
1, 2	These jumpers select the desired number of data bits.
PB	Jumper is inserted to enable the programmable baud rate capability.
C, C1	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted.)

Jumper Definitions (Cont)

Jumper	Function
S, S1	Inserted for split speed operation. (Note that C and C1 must be removed when S and S1 are inserted.)
H	This jumper is inserted to assert BHALT L when a framing error is received, except when the maintenance bit is set. This places the LSI-11 in the halt mode.
B, -B	Jumper B is inserted to negate BDCOK H when a BREAK signal or framing error is received, except when the maintenance bit is set. This causes the LSI-11 to reload the bootstrap. (Jumper -B must be removed when B is inserted.)
-FD	Jumper is removed to force DATA TERMINAL READY signal on.
-FR	Jumper is removed to force REQUEST TO SEND signal on.
RS	This jumper is inserted to enable normal transmission of the REQUEST TO SEND signal.
FB	Inserted to enable transmission of the FORCE BUSY signal (for Bell model 103E data sets).
M, M1	These are test jumpers used during the manufacturing of the module. They are not defined for field use.

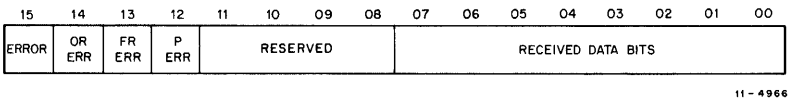


DLV11-E RCSR Bit Assignments

Bit	Function
15	DATA SET INT (Data Set Interrupt) - This bit initiates an interrupt sequence, provided that the DATA SET IN ENB, bit (05) is also set. This bit is set whenever CAR DET, CLR TO SEND, or SEC REC changes state; i.e., on a 0-to-1 or 1-to-0 transition of any one of these bits. It is also set when ring changes from 0 to 1. Cleared by INIT or by reading the RCSR. Because reading the register clears the bit, it is, in effect, a "read-once" bit.
14	Ring - When set, indicates that a RINGING signal is being received from the dataset. Note that the RINGING signal is not a level but an EIA control with the cycle time as shown below. Read only. 
13	CLR TO SEND (Clear to Send) - The state of this bit is dependent on the state of the CLEAR TO SEND signal from the data set. When set, this bit indicates an ON condition; when clear, it indicates an OFF condition. Read only.
12	CAR DET (Carrier Detect) - This bit is set when the data carrier is received. When clear, it indicates either the end of the current transmission activity or an error condition. Read only.
11	RCVR ACT (Receiver Active) - When set, this bit indicates that the DLV11-E's receiver is active. The bit is set at the center of the START bit, which is the beginning of the input serial data from the device, and is cleared by the leading edge of R DONE H. Read-only bit; cleared by INIT or by R DONE H (bit 07).

DLV11-E RCSR Bit Assignments (Cont)

Bit	Function
10	SEC REC (Secondary Received or Supervisory Received Data) - This bit provides a receive capability for the reverse channel of a remote station. A space (+10 V) is read as a 1. (A transmit capability is provided by bit 03.) Read only.
9-8	Not used. Reserved for future use.
07	RCVR DONE (Receiver Done) - This bit is set when an entire character has been received and is ready for transfer to the LSI-11. When set, initiates an interrupt sequence, provided that RCVR INT ENB (bit 06) is also set. Cleared whenever the receiver buffer (RBUF) is addressed. Also cleared by INIT. Read only.
06	RCVR INT ENB (Receiver Interrupt Enable) - When set, allows an interrupt sequence to start when RCVR DONE (bit 07) sets.
05	DSET INT ENB (Data Set Interrupt Enable) - When set, allows an interrupt sequence to start when DATA SET INT (bit 15) sets.
04	Not used. Reserved for future use.
03	SEC XMIT (Secondary Transmitted or Supervisory Transmitted Data) - This bit provides a transmit capability for a reverse channel of a remote station. When set, transmits a space (+10 V). (A receive capability is provided by bit 10.) Read/write bit; cleared by INIT.
02	REQ TO SEND - A control lead to the data set which is required for transmission. Ajumper on the DLV11-E ties this bit to REQ TO SEND or FORCE BUSY in the data set. Read/write bit; cleared by INIT.
01	DTR (Data Terminal Ready) - A control lead for the data set communication channel. When set,permits connection to the channel. When clear, disconnects the interface from the channel. Read/write bit; must be cleared by the program, not by INIT. The state of this bit is not defined after power-up.
00	Not used. Reserved for future use.



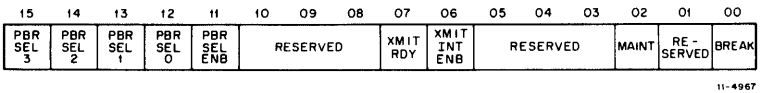
DLV11-E RBUF Bit Assignments

Bit	Function
15	Error - Used to indicate that an error condition is present. This bit is the logical OR of OR ERR, FR ERR, and P ERR (bits 14, 13, and 12, respectively). Whenever one of these bits is set, it causes the error bit to set. This bit is not connected to the interrupt logic. Read-only bit; cleared by removing the error-producing condition.

NOTE

Error indications remain present until the next character is received, at which time the error bits are updated. INIT clears the error bits.

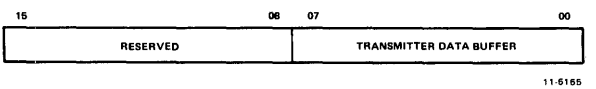
14	OR ERR (Overrun Error) - When set, indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character. Read only; cleared by INIT.
13	FR ERR (Framing Error) - When set, indicates that the character that was read had no valid stop bit.
12	P ERR (Parity Error) - When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected. Read-only bit; cleared by INIT.
11-08	Not used. Reserved for future use.
07-00	Received Data Bits - Holds the character just read. If fewer than eight bits are selected, then the buffer is right-justified into the least significant bit positions. In this case, the higher unused bit or bits are read as 0s. Read-only bits; not cleared by INIT.



DLV11-E XCSR Bit Assignments

DLV11-E XCSR Bit Assignments

Bit	Function
15-12	PBR SEL (Programmable Baud Rate Select) - When set, these bits choose a baud rate from 50-9600 baud. Write only.
11	PBR ENB (Programmable Baud Rate Enable) - This bit must be set in order to select a new baud rate indicated by bits 12 to 15.
10-08	Not used. Reserved for future use.
07	XMIT RDY (Transmitter Ready) - This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT ENB (bit 06) is also set. Read-only bit; set by INIT.
06	XMIT INT ENB (Transmitter Interrupt Enable) - When set, allows an interrupt sequence to start when XMIT RDY (bit 07) is set. Read/write bits; cleared by INIT.
05-03	Not used. Reserved for future use.
02	MAINT Used for maintenance function. When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receiver serial input. It also forces the receiver to run at transmitter baud rate speed when split speed operation is enabled. Read/write bit; cleared by INIT.
01	Not used. Reserved for future use.
00	Break - When set, transmits a continuous space to the external device. Read/write bit; cleared by INIT.



DLV11-E XBUF Bit Assignments

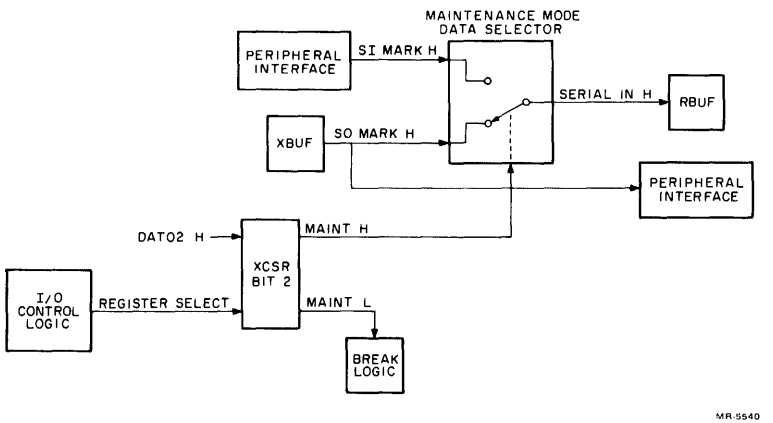
Bit	Function
15-08	Not used or defined. Not necessarily read as 0s.
07-00	Transmitter Data Buffer - Holds the character to be transferred to the external device. If fewer than eight bits are used, the character must be loaded so that it is right-justified in the least significant bits. Write-only bits; not necessarily read as 0s.

Maintenance Aids

The DLV11 is shipped with an H315 modem test connector. This is plugged into the interface cable in place of a data set when maintenance programs are running.

Maintenance Mode Logic

In the maintenance mode, the DLV11-E and DLV11-F modules route their output data back to their input. To accomplish this, the computer program sets the maintenance bit in the XCSR. The latch holding this bit has two outputs. One goes to the break logic to prevent the generation of framing error signals during operation in the maintenance mode. The other output is applied to the maintenance mode data selector. The data selector normally routes the incoming data from the peripheral interface to the RBUF. In the maintenance mode, however, it switches its input to the output of the XBUF. This action loops the serial data out of the XBUF back into the RBUF and disconnects the peripheral interface's data. While in the maintenance mode, the serial output of the XBUF continues to go to the peripheral interface and out to the peripheral device.



Maintenance Mode Logic

M8018
KUV11-AA WRITABLE CONTROL STORE

Amps		Bus Loads		Cables
+5	+12	AC	DC	17-00124-00
3		1.4	1	17-00124-01 (maintenance)

Standard Addresses

CSR and RAM Address	177540
DATA I/O, bits 0-15	177542
DATA I/O, bits 16-21	177544

Standard Vectors

None

Diagnostic Program

Refer to Appendix A.

Related Documentation

LSI-11 WCS User's Guide (EK-KUV11-TM)
KD11-WA Maintenance Print Set (MP00571-00)

NOTES

1. **An M8018 can only be used with an M7264-YC LSI-11 processor.**

2. **To extend the M8018, the maintenance cable is required (17-00124-01).**

Switch Configurations

The range of microcode addresses to which the WCS will respond on the microinstruction bus (MIB) (when the CSR enable bit is a 1) is determined by an 8-wide DIP switch (SW1) on the M8018 module.

Set switches S1 through S7 (S8 is not used) on SW1 as shown in the "WCS Address Mode Switch Settings" table to select one of the four modes of operation described below.

Mode I – The microcode is loaded from the LSI-11 bus into WCS RAM locations 0 to 1777. The WCS correspondingly responds to microaddresses 2000 to 3777 on the MIB.

Mode II – The microcode is loaded from the LSI-11 bus into WCS RAM locations 0 to 1777. The WCS initially responds to MIB microaddresses 3000 to 3777 from the first 512 words of RAM. If bits 21-18 of the microinstruction are coded to a 7 (octal) then the next microinstruction will be accessed from the second 512 words of RAM. A second 7 (octal) will toggle back to the first 512 words of RAM. This swapping between 512 word blocks for the same microaddress range is called "paging" and allows 1024 words of microcode to be implemented when only 512 microaddresses are available.

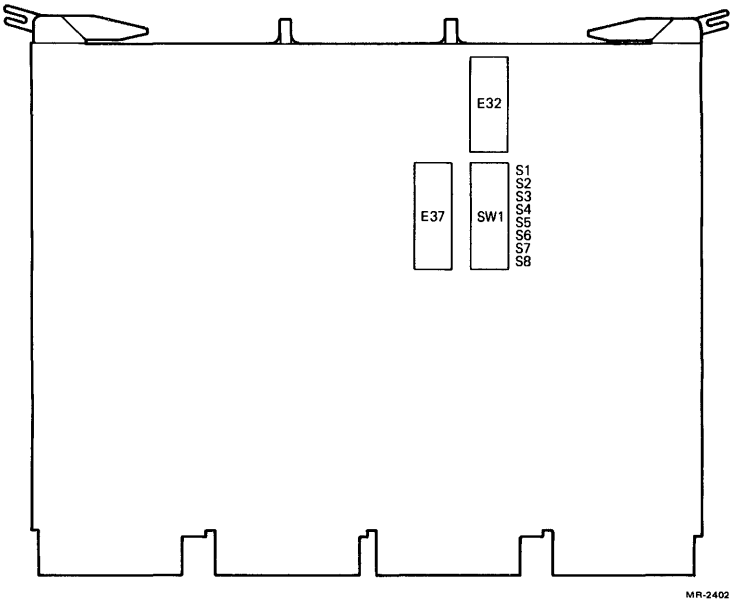
Mode III – This mode is the same as Mode I except that the two blocks of 512 words of RAM have been interchanged on the module. Addressing is identical to that of Mode I.

Mode IV – The microcode is loaded from the LSI-11 bus into WCS RAM locations 0 to 1777. The WCS correspondingly responds to MIB microaddresses 0 to 1777. This microaddress space is identical to MICROMs 0 and 1, which contain the base PDP-11 microcode for the LSI-11.

MODE	SWITCH SW1							
	S1	S2	S3	S4	S5	S6	S7	S8
I	ON	OFF	OFF	ON	OFF	ON	OFF	–
II	OFF	ON	OFF	ON	OFF	OFF	ON	–
III	OFF	OFF	ON	ON	OFF	ON	OFF	–
IV	ON	OFF	OFF	OFF	ON	ON	OFF	–

MR-1060

WCS Address Mode Switch Settings

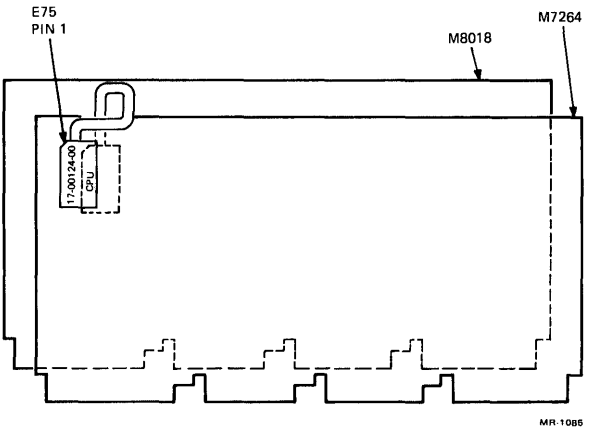


Address Mode Switch Location

ITEM	MODELS			
	KUV11-UH	KD11-WA	11/03-WC	11/03-WD
KD11-H CPU	X			
M8018 WCS MODULE	X	X	X	X
WCS CABLE Part NO 17-00124-00	X	X	X	X
KD11-R CPU (Includes MSV11-CD memory)		X	X	X
BDV11-AA BOOT MODULE			X	X
BA11-NC BOX (115 V)			X	
BA11-ND BOX (230V)				X

MR-1059

Items Supplied Per Configuration



WCS to CPU Installation

LSI-11 Bus Address Decode and Control
This logic does the LSI-11 bus interface, and responds to four device addresses which have the following meanings.

LSI-11 Address	Meaning
177540	Control/status register and RAM address.
177542	Data input/output for RAM data word bits 0-15, or output for trace stack.
177544	Data input/output for RAM data word bits 16-21 and data input/output for two user bits.
177546	Unused (but still responds) A DIN will read all 0s.

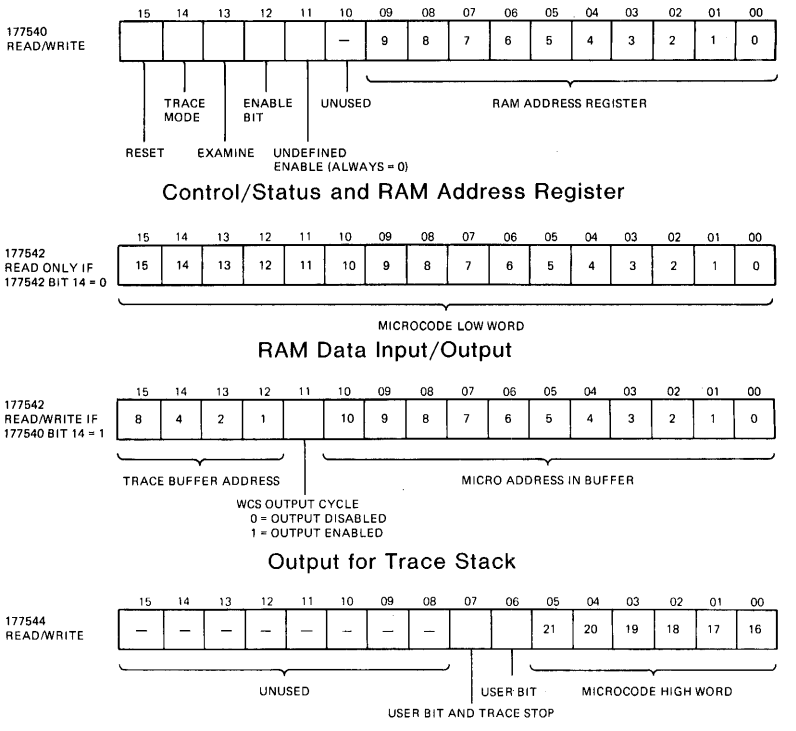
NOTE
The address 177546 is the same address normally assigned to the KW11-L clock status register.

Read Back MUX
The read back MUX selects the source of the data to be output to the LSI-11 bus at the proper time during an LSI-11 DATAI bus cycle.

Control Status Register
The CSR consists of five control/status bits and a RAM address register. The control/status bits are described below.

CSR Bit	Definition
15	When this bit is asserted, it resets the WCS module, in particular, the trace feature.
14, 13, 11	These bits control the trace mode of the WCS.
12	When this bit (the enable bit) is asserted, the WCS is enabled to respond to the MIB. When it is disabled, the WCS cannot respond to the MIB.

After the enable bit is disabled in the CSR, the RAM can be accessed by writing an address (with enable bit = 0) to the CSR address. Then the lower 16 bits at that address of RAM (microcode bits 0-15) can be accessed (read or write) at the second device address, and the upper eight bits at the same address of RAM (the two user bits and microcode bits 16-21) can be accessed (read or write) at the third device address.



RAM Data Input/Output, User Bits Data Input/Output
LSI-11 Bit Assignments

M8021
MRV11-BA UV PROM-RAM

	Amps		Bus Loads		Cables
	+5	+12	AC	DC	
W/O PROM	0.58 (0.67 max.)	0.34	2.8 (0.41 max.)	1.0	None
With PROMs	0.62 (0.744 max.)	0.5	(0.6 max.)		

Standard Addresses

RAMs	20000-20777
PROMs	140000-157777

Standard Vectors

None

Diagnostic Programs

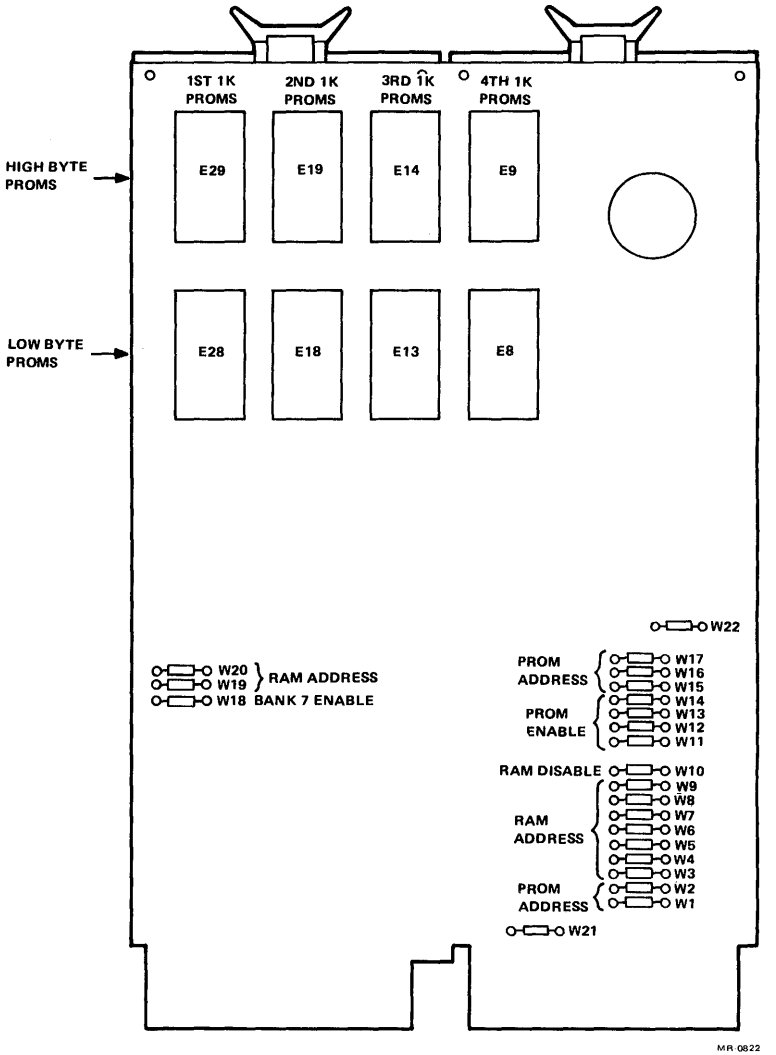
Refer to Appendix A.

Related Documentation

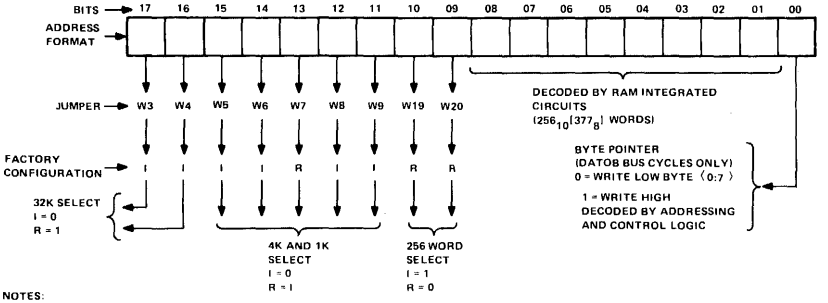
MRV11-BA LSI-11 UV PROM-RAM User's Manual (EK-MRV11-TM)
Field Maintenance Print Set (MP00354)
Microcomputer Processor Handbook (EB-18451-20)

Recommended PROM Types

DEC MRV11-BC Intel 2708 (DEC PN 23-00087-01)	1024 × 8-bit, MOS, tri-state, erasable ultraviolet (24-pin DIP)



MRV11-BA RAM Addressing

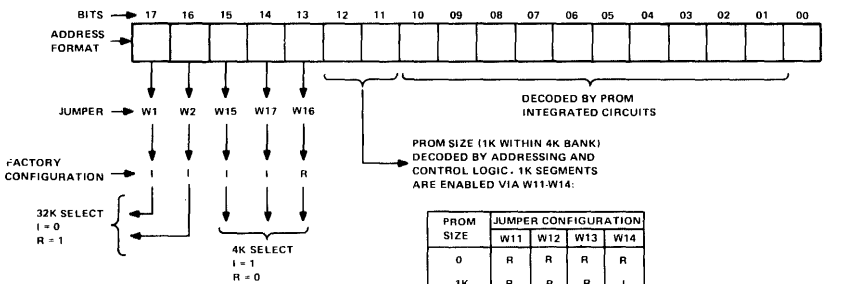


NOTES:

1. Factory configured address range = 20000 – 20377
2. I = Jumper installed; R = Jumper removed
3. W10 removed = RAM ENABLE
   W10 installed = RAM DISABLE

MR-5536

MRV11-BA RAM Addressing



PROM SIZE	JUMPER CONFIGURATION			
	W11	W12	W13	W14
0	R	R	R	R
1K	R	R	R	I
2K	R	R	I	I
3K	R	I	I	I
4K	I	I	I	I

NOTES:

1. Factory configured address range = 140000-157777
2. I = Jumper installed, R = Jumper removed

MR-5537

MRV11-BA PROM Addressing

RAM Addressing Summary

Address Range (Octal)	Memory Jumper Configuration (I=Installed; R=Removed)									
	Bank	W3	W4	W5	W6	W7	W8	W9	W19	W20
000000-000777	0	I	I	I	I	I	I	I	R	R
001000-001777	0	I	I	I	I	I	I	I	R	I
002000-002777	0	I	I	I	I	I	I	I	I	R
003000-003777	0	I	I	I	I	I	I	I	I	I
004000-004777	0	I	I	I	I	I	I	R	R	R
005000-005777	0	I	I	I	I	I	I	R	R	I
006000-006777	0	I	I	I	I	I	I	R	I	R
007000-007777	0	I	I	I	I	I	I	R	I	I
010000-010777	0	I	I	I	I	I	R	I	R	R
011000-011777	0	I	I	I	I	I	R	I	R	I
012000-012777	0	I	I	I	I	I	R	I	I	R
013000-013777	0	I	I	I	I	I	R	I	I	I
014000-014777	0	I	I	I	I	I	R	R	R	R
015000-015777	0	I	I	I	I	I	R	R	R	I
016000-016777	0	I	I	I	I	I	R	R	I	R
017000-017777	0	I	I	I	I	I	R	R	I	I
020000-020777	1	I	I	I	I	R	I	I	R	R
021000-021777	1	I	I	I	I	R	I	I	R	I
022000-022777	1	I	I	I	I	R	I	I	I	R
023000-023777	1	I	I	I	I	R	I	I	I	I
024000-024777	1	I	I	I	I	R	I	R	R	R
025000-025777	1	I	I	I	I	R	I	R	R	I
026000-026777	1	I	I	I	I	R	I	R	I	R
027000-027777	1	I	I	I	I	R	I	R	I	I
030000-030777	1	I	I	I	I	R	R	I	R	R
031000-031777	1	I	I	I	I	R	R	I	R	I
032000-032777	1	I	I	I	I	R	R	I	I	R
033000-033777	1	I	I	I	I	R	R	I	I	I
034000-034777	1	I	I	I	I	R	R	R	R	R
035000-035777	1	I	I	I	I	R	R	R	R	I
036000-036777	1	I	I	I	I	R	R	R	I	R
037000-037777	1	I	I	I	I	R	R	R	I	I
040000-040777	2	I	I	I	R	I	I	I	R	R
041000-041777	2	I	I	I	R	I	I	I	R	I
042000-042777	2	I	I	I	R	I	I	I	I	R
043000-043777	2	I	I	I	R	I	I	I	I	I
044000-044777	2	I	I	I	R	I	I	R	R	R
045000-045777	2	I	I	I	R	I	I	R	R	I
046000-046777	2	I	I	I	R	I	I	R	I	R
047000-047777	2	I	I	I	R	I	I	R	I	R

RAM Addressing Summary (Cont)

Address Range (Octal)	Memory Jumper Configuration (I=Installed; R=Removed) Bank	W3	W4	W5	W6	W7	W8	W9	W19	W20
050000-050777	2	I	I	I	R	I	R	I	R	R
051000-051777	2	I	I	I	R	I	R	I	R	I
052000-052777	2	I	I	I	R	I	R	I	I	R
053000-053777	2	I	I	I	R	I	R	I	I	I
054000-054777	2	I	I	I	R	I	R	R	R	R
055000-055777	2	I	I	I	R	I	R	R	R	I
056000-056777	2	I	I	I	R	I	R	R	I	R
057000-057777	2	I	I	I	R	I	R	R	I	I
060000-060777	3	I	I	I	I	R	I	I	R	R
061000-061777	3	I	I	I	I	R	I	I	R	I
062000-062777	3	I	I	I	I	R	I	I	I	R
063000-063777	3	I	I	I	I	R	I	I	I	I
064000-064777	3	I	I	I	I	R	I	R	R	R
065000-065777	3	I	I	I	I	R	I	R	R	I
066000-066777	3	I	I	I	I	R	I	R	I	R
067000-067777	3	I	I	I	I	R	I	R	I	I
070000-070777	3	I	I	I	I	R	R	I	R	R
071000-071777	3	I	I	I	I	R	R	I	R	I
072000-072777	3	I	I	I	I	R	R	I	I	R
073000-073777	3	I	I	I	I	R	R	I	I	I
074000-074777	3	I	I	I	I	R	R	R	R	R
075000-075777	3	I	I	I	I	R	R	R	R	I
076000-076777	3	I	I	I	I	R	R	R	I	R
077000-077777	3	I	I	I	I	R	R	R	I	I
100000-100777	4	I	I	R	I	I	I	I	R	R
101000-101777	4	I	I	R	I	I	I	I	R	I
102000-102777	4	I	I	R	I	I	I	I	I	R
103000-103777	4	I	I	R	I	I	I	I	I	I
104000-104777	4	I	I	R	I	I	I	R	R	R
105000-105777	4	I	I	R	I	I	I	R	R	I
106000-106777	4	I	I	R	I	I	I	R	I	R
107000-107777	4	I	I	R	I	I	I	R	I	I
110000-110777	4	I	I	R	I	I	R	I	R	R
111000-111777	4	I	I	R	I	I	R	I	R	I
112000-112777	4	I	I	R	I	I	R	I	I	R
113000-113777	4	I	I	R	I	I	R	I	I	I
114000-114777	4	I	I	R	I	I	R	R	R	R
115000-115777	4	I	I	R	I	I	R	R	R	I
116000-116777	4	I	I	R	I	I	R	R	I	R
117000-117777	4	I	I	R	I	I	R	R	I	I

RAM Addressing Summary (Cont)

Address Range (Octal)	Bank	Memory Jumper Configuration (I=Installed; R=Removed) W3	W4	W5	W6	W7	W8	W9	W19	W20
120000-120777	5	I	I	R	I	R	I	I	R	R
121000-121777	5	I	I	R	I	R	I	I	R	I
122000-122777	5	I	I	R	I	R	I	I	I	R
123000-123777	5	I	I	R	I	R	I	I	I	I
124000-124777	5	I	I	R	I	R	I	R	R	R
125000-125777	5	I	I	R	I	R	I	R	R	I
126000-126777	5	I	I	R	I	R	I	R	I	R
127000-127777	5	I	I	R	I	R	I	R	I	I
130000-130777	5	I	I	R	I	R	R	I	R	R
131000-131777	5	I	I	R	I	R	R	I	R	I
132000-132777	5	I	I	R	I	R	R	I	I	R
133000-133777	5	I	I	R	I	R	R	I	I	I
134000-134777	5	I	I	R	I	R	R	R	R	R
135000-135777	5	I	I	R	I	R	R	R	R	I
136000-136777	5	I	I	R	I	R	R	R	I	R
137000-137777	5	I	I	R	I	R	R	R	I	I
140000-140777	6	I	I	R	R	I	I	I	R	R
141000-141777	6	I	I	R	R	I	I	I	R	I
142000-142777	6	I	I	R	R	I	I	I	I	R
143000-143777	6	I	I	R	R	I	I	I	I	I
144000-144777	6	I	I	R	R	I	I	R	R	R
145000-145777	6	I	I	R	R	I	I	R	R	I
146000-146777	6	I	I	R	R	I	I	R	I	R
147000-147777	6	I	I	R	R	I	I	R	I	I
150000-150777	6	I	I	R	R	I	R	I	R	R
151000-151777	6	I	I	R	R	I	R	I	R	I
152000-152777	6	I	I	R	R	I	R	I	I	R
153000-153777	6	I	I	R	R	I	R	I	I	I
154000-154777	6	I	I	R	R	I	R	R	R	R
155000-155777	6	I	I	R	R	I	R	R	R	I
156000-156777	6	I	I	R	R	I	R	R	I	R
157000-157777	6	I	I	R	R	I	R	R	I	I
160000-160777	7*	I	I	R	R	R	I	I	R	R
161000-161777	7*	I	I	R	R	R	I	I	R	I
162000-162777	7*	I	I	R	R	R	I	I	I	R
163000-163777	7*	I	I	R	R	R	I	I	I	I
164000-164777	7*	I	I	R	R	R	I	R	R	R
165000-165777	7*	I	I	R	R	R	I	R	R	I
166000-166777	7*	I	I	R	R	R	I	R	I	R

*The bank 7 enable jumper W18 is factory installed to allow addressing in bank 7.

RAM Addressing Summary (Cont)

Address Range (Octal)	Memory Jumper Configuration (I=Installed; R=Removed) Bank	W3	W4	W5	W6	W7	W8	W9	W19	W20
167000-167777	7*	I	I	R	R	R	I	R	I	I
170000-170777	7*	I	I	R	R	R	R	I	R	R
171000-171777	7*	I	I	R	R	R	R	I	R	I
172000-172777	7*	I	I	R	R	R	R	I	I	R
173000-173777	7*	I	I	R	R	R	R	I	I	I
174000-174777	7*	I	I	R	R	R	R	R	R	R
175000-175777	7*	I	I	R	R	R	R	R	R	I
176000-176777	7*	I	I	R	R	R	R	R	I	R
177000-177777	7*	I	I	R	R	R	R	R	I	I

*The bank 7 enable jumper W18 is factory installed to allow addressing in bank 7.

NOTE

The following jumper configurations illustrate configuring the address range in banks above bank 7 (not implemented in present LSI-11 system configurations). W8, W9, W19, and W20 can be configured as shown in the preceding pages to select the desired segment within the bank.

Address Range (Octal)	Memory Jumper Configuration (I=Installed; R=Removed)					
	Bank	W3	W4	W5	W6	W7
200000-217777	10	I	R	I	I	I
220000-237777	11	I	R	I	I	R
240000-257777	12	I	R	I	R	I
260000-277777	13	I	R	I	R	R
300000-317777	14	I	R	R	I	I
320000-337777	15	I	R	R	I	R
340000-357777	16	I	R	R	R	I
360000-377777	17	I	R	R	R	R
400000-417777	20	R	I	I	I	I
420000-437777	21	R	I	I	I	R
440000-457777	22	R	I	I	R	I
460000-477777	23	R	I	I	R	R
500000-517777	24	R	I	R	I	I
520000-537777	25	R	I	R	I	R
540000-557777	26	R	I	R	R	I
560000-577777	27	R	I	R	R	R
600000-617777	30	R	R	I	I	I
620000-637777	31	R	R	I	I	R
640000-657777	32	R	R	I	R	I
660000-677777	33	R	R	I	R	R
700000-717777	34	R	R	R	I	I
720000-737777	35	R	R	R	I	R
740000-757777	36	R	R	R	R	I
760000-777777	37	R	R	R	R	R

PROM Addressing Summary

Address Range (Octal)	Memory Jumper Configuration (I = Installed; R = Removed) Bank	W1	W2	W15	W17	W16
000000-017777	0	I	I	R	R	R
020000-037777	1	I	I	R	R	I
040000-057777	2	I	I	R	I	R
060000-077777	3	I	I	R	I	I
100000-117777	4	I	I	I	R	R
120000-137777	5	I	I	I	R	I
140000-157777	6	I	I	I	I	R
160000-177777	7*	I	I	I	I	I
200000-217777	10	I	R	R	R	R
220000-237777	11	I	R	R	R	I
240000-257777	12	I	R	R	I	R
260000-277777	13	I	R	R	I	I
300000-317777	14	I	R	I	R	R
320000-337777	15	I	R	I	R	I
340000-357777	16	I	R	I	I	R
360000-377777	17	I	R	I	I	I
400000-417777	20	R	I	R	R	R
420000-437777	21	R	I	R	R	I
440000-457777	22	R	I	R	I	R
460000-477777	23	R	I	R	I	I
500000-517777	24	R	I	I	R	R
520000-537777	25	R	I	I	R	I
540000-557777	26	R	I	I	I	R
560000-577777	27	R	I	I	I	I
600000-617777	30	R	R	R	R	R
620000-637777	31	R	R	R	R	I
640000-657777	32	R	R	R	I	R
660000-677777	33	R	R	R	I	I
700000-717777	34	R	R	I	R	R
720000-737777	35	R	R	I	R	I
740000-757777	36	R	R	I	I	R
760000-777777	37	R	R	I	I	I

*The bank 7 enable jumper W18 is factory installed to allow addressing in bank 7.

PROM Addressing

Address* Octal	Binary	10 22	09 23	08 1	07 2	06 3	05 4	04 5	03 6	02 7	01 8	Address Bits PROM Pins
0	00000000000	L	L	L	L	L	L	L	L	L	L	
2	00000000010	L	L	L	L	L	L	L	L	L	H	
4	00000000100	L	L	L	L	L	L	L	L	H	L	Actual Logic
6	00000000110	L	L	L	L	L	L	L	L	H	H	Levels Required
10	00000001000	L	L	L	L	L	L	L	H	L	L	(1024_{10}
12	00000001010	L	L	L	L	L	L	L	H	L	H	Locations)
14												
.												
.												
.												
3776	11111111110	H	H	H	H	H	H	H	H	H	H	

*Bus address bit 0 is not used. Therefore, only even-numbered addresses are shown.

M8027
LPV11 LP05/LA180 INTERFACE MODULE /LP25

Amps		Bus Loads		Cables
+5	+12	AC	DC	
0.8	0	1.4	1	BC11S-25 for LA180 70-11212-25 for LP05

Standard Addresses

LPCS	177514
LPDB	177516

Standard Vector

Done or error interrupt 200

Diagnostic Programs

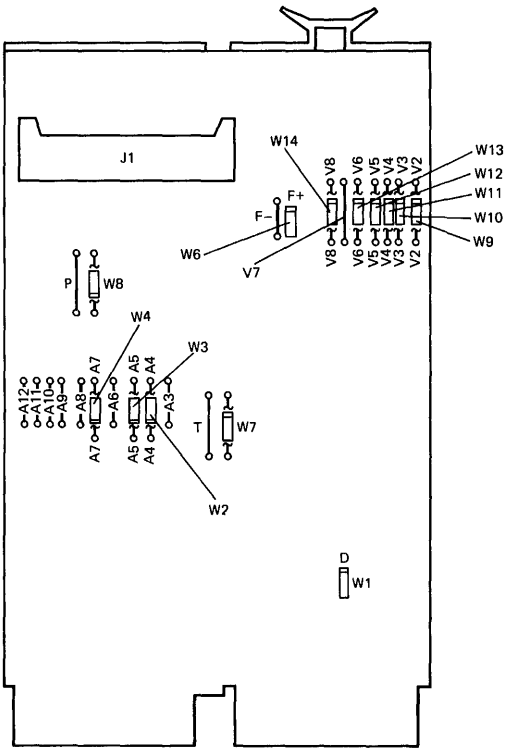
Refer to Appendix A.

Related Documentation

LP25 Line Printer Maintenance Guide (ER-OLP25-5V)
LPV11 Printer User's Manual (EK-LPV11-OP)
LA180 DECprinter I User's Manual (EK-LA180-OP)
LA180 Field Maintenance Print Set (MP-LA180-00)
LA180 DECprinter I Maintenance Manual (EK-LA180-MM)
LP05 Technical Manual, Model 2230 Line Printer (Dataproducts Corporation)
LPV11-V Field Maintenance Print Set (MP00467)
Microcomputer Interfaces Handbook (EB-20175-20)

NOTE

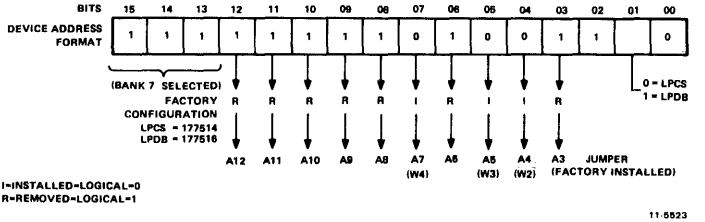
The LPV11 (M8027) is a direct replacement for the LAV11 (M7949).



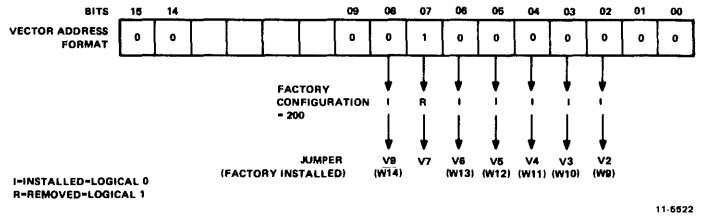
NOTE:

- =JUMPERS BROKEN FOR CLARITY ON THIS FIGURE. THESE WIRE-WRAP JUMPERS WOULD NORMALLY BE USED TO REPLACE PREVIOUSLY REMOVED FACTORY INSTALLED (W) JUMPERS (SHOWN INSTALLED).
- o =WIRE WRAP PIN.

MR-0863



LPV11 Interrupt Device Address Format and Jumpers



LPV11 Vector Address Format and Jumpers

LPV11 Jumper Definitions

Jumper Designation	Configuration When Shipped	Function
A12	R	Jumper wires W2, W3, and W4 are factory installed to negate address bits 4, 5, and 7, respectively.
A11	R	
A10	R	
A9	R	
A8	R	This sets 177514 as the base address.
A7	I	
A6	R	
A5	I	
A4	I	
A3	R	
V8	I	Jumper wires W9 through W14 are factory installed to negate vector bits 2, 3, 4, 5, 6, and 8.
V7	R	
V6	I	
V5	I	
V4	I	This sets 200 as the interrupt vector.
V3	I	
V2	I	

LPV11 Jumper Definitions (Cont)

Jumper Designation	Configuration When Shipped	Function
D	I	W1 installed to delay BRPLY L.
T W7	R I	Supports both uppercase and lowercase printing. For uppercase only, remove W7 and install T. Do not configure the module with both jumpers W7 and T installed.
P W8	R I	Configured to transmit parity (bit 07) to printer.

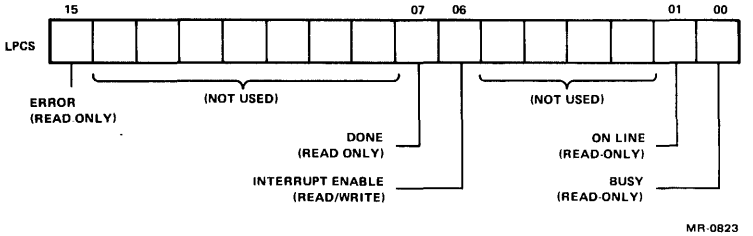
Parity Option	Jumper W8	Jumper P
Normal parity bit	Installed	Removed
No parity, bit 07 low	Removed	Removed
No parity, bit 07 high	Removed	Installed

Do not configure the module with both jumpers W8 and P installed.

NOTE

If the LPV11 interface module is used with an LP05 printer equipped with the Direct Access Vertical Form Unit (DAVFU), it is recommended that the user remove jumper W8. The LP05 interface module does not support the DAVFU Function.

F− F+	R O	W6 is installed at F+ to enable error filter operation with the LP05. For operation without the error filter, remove W6 and install a jumper at F−. Do not configure the module with jumpers installed at both F+ and F−. The LSI-A180 automatically enables the error filter circuit regardless of the jumper configuration.



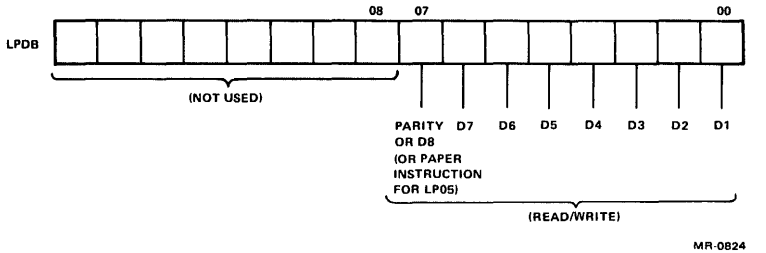
LPV11 Control/Status Register (LPCS)

LPCS Register Bit Functions

Bit	Function
15	Error - Asserted (1) whenever an error condition exists in the line printer. Error conditions include the following. LP05 errors: • Power off • No paper • Printer drum gate open • Over-temperature alarm • PRINT INHIBIT switch off • Printer off-line • Torn paper LA180 errors: • Fault (paper fault) • ON-LINE switch (in OFF position) Reset by manual correction of error condition if LPCS bit 06 is not set. If bit 06 is set, bit 15 is reset by manual correction of the error and (1) reading the interrupt vector if the interface is "ready," or (2) after reading the LPCS if the interface is "not ready." Read only.
14-08	Not used. Read as 0s.

LPCS Register Bit Functions (Cont)

Bit	Function
07	Done LP05 - Asserted (1) whenever printer is ready for next character to be loaded. Indicates that previous function is either complete or has been started and continued to a point where the printer can accept the next command. This bit is set by the LSI-11 processor asserting BINIT L; if bit 06 is also set, an interrupt sequence is initiated. Also set by the printer when on-line and ready to accept a character. Cleared by loading (writing into) the LPDB register. Inhibited when bit 15 is set. Read only. LA180 - Asserted (1) when the printer is ready to accept another character. Done is set by the LSI-11 processor asserting BINIT L and is cleared by loading (output transfer to) the LPDB register. If the interrupt enable bit is set, setting done will initiate an interrupt request.
06	Interrupt Enable - Set or cleared by the program. Also cleared by the LSI-11 processor asserting BINIT L. When set, an interrupt sequence is initiated if either the error or done bit is set.
05-02	Not used. Read as 0s.
01	On-Line - Not supported and not required by DEC software.
00	Busy - Not supported and not required by DEC software. The following information is for reference only. LA180 - Set when the LA180 prints a line or advances paper. LP05 - Not used. Read as 0.



LPV11 Data Buffer Register (LPDB)

LPDB Register Bit Functions

Bit	Function
15-08	Not used. Read as 0s. Data written into these bits is lost.
07	Parity or D8 - Optional use. Read as 0. LA180 - Optional parity bit. LP05 - Optional paper instruction bit. Not supported by the LPV11 (read as 0).
06-00	Data - Seven-bit ASCII character register. Characters are sequentially output to the printer buffer via this register. Read as all 0s.

M8028
DLV11-F ASYNCHRONOUS SERIAL LINE INTERFACE

Amps		Bus Loads		Cables
+5	+12	AC	DC	BC05M for 20 mA
1.0	0.18	2.2	1.0	BC05C for EIA modem
				BC05C plus H312A for EIA terminal

Standard Addresses

	Console	Second Terminal	Modem	MINC/DECLAB
RCSR	177560	176500	175610	175610
RBUF	177562	176502	175612	175612
XCSR	177564	176504	175614	175614
XBUF	177566	176506	175616	175616

Standard Vectors

Floating - Configurable in the range of 000-770. Refer to Appendix B.

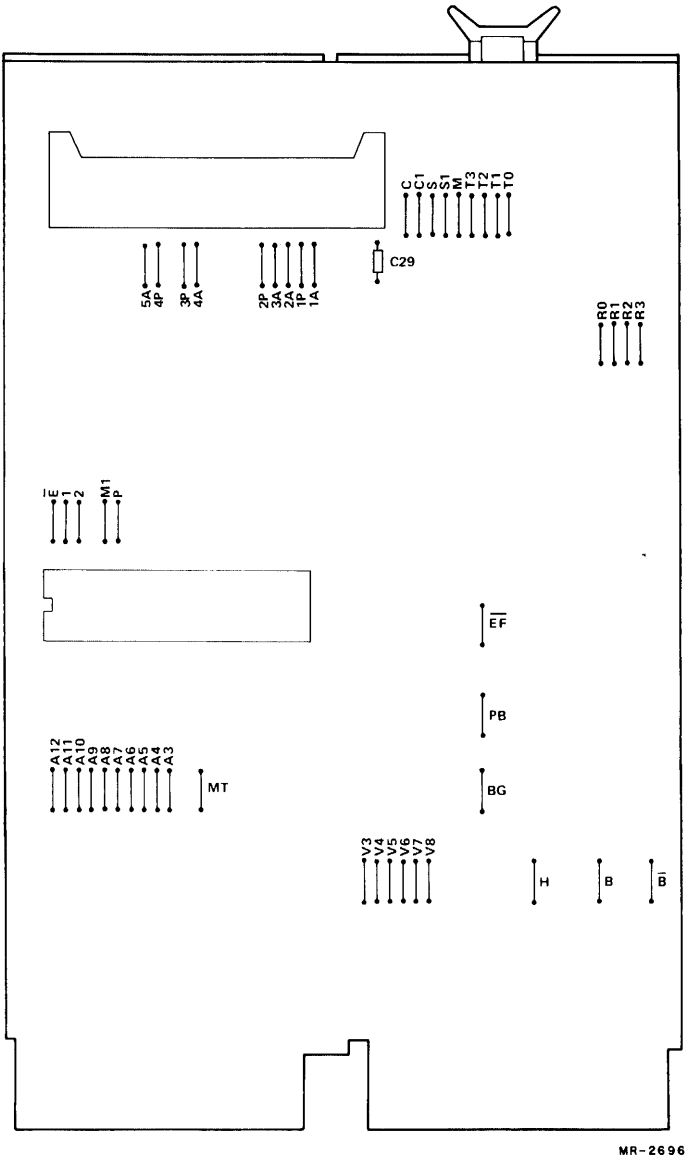
	Console	Second Terminal	Modem	MINC/DECLAB
Receiver	60	300	300	330
Transmitter	64	304	304	334

Diagnostic Programs

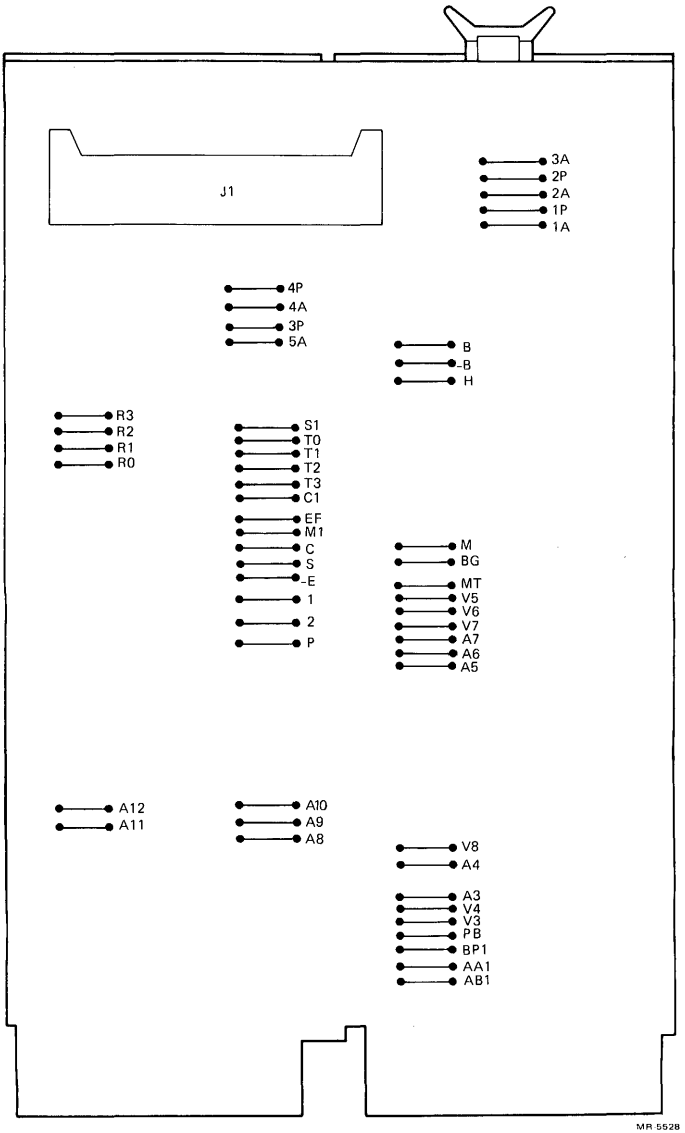
Refer to Appendix A.

Related Documentation

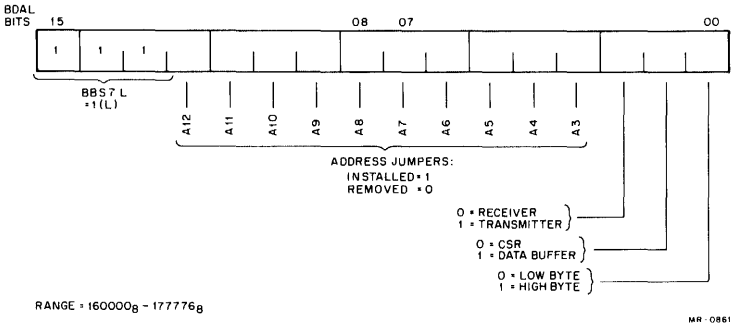
DLV11-E and DLV11-F Asynchronous Line Interface User's Manual (EK-DLV11-OP)
Field Maintenance Print Set (MP00461)
Microcomputer Interfaces Handbook (EB-20175-20)



DLV11-F Etch Rev B Jumper Locations



DLV11-F Etch Rev C Jumper Locations



DLV11-F Addresses

Address Jumpers

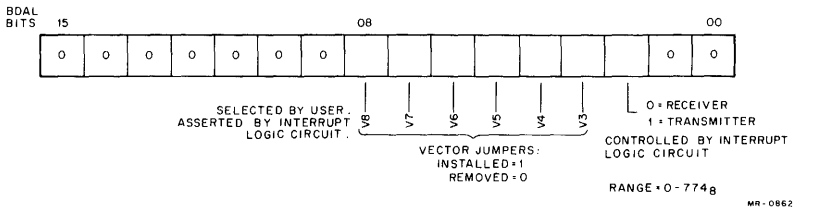
Unit	Address	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3
Console	177560	R	I	I	I	R	I	I	I	I	I
First Option	176500	R	R	R	I	R	I	R	I	I	I
Second Option	176510	I	R	R	I	R	I	R	I	I	I
Third Option	176520	R	I	R	I	R	I	R	I	I	I
Modem	175610	I	R	R	R	I	I	I	R	I	I

Etch Rev C

BD1	R
AA1	R
AB1	R

Vector Jumpers

Unit	Vector	V8	V7	V6	V5	V4	V3
Console	60	R	I	I	R	R	R
First Option	300	R	R	R	I	I	R
Second Option	310	I	R	R	I	I	R
Third Option	320	R	I	R	I	I	R
Modem	300	R	R	R	I	I	R



DLV11-F Interrupt Vectors

Jumper Configuration When Shipped

Jumper Designation	Jumper State	Function
A3	R	Jumpers A3 through A12 implement device
A4	I	address 17756X. The least significant octal
A5	I	digit is hardwired on the module to address
A6	I	the four device registers as follows.
A7	R	
A8	I	X = 0 RCSR
A9	I	X = 2 RBUF
A10	I	X = 4 XCSR
A11	I	X = 6 XBUF
A12		
V3	I	This jumper selection implements interrupt
V4	R	vector address 60 for receiver interrupts
V5	R	and 64 for transmitter interrupts.
V6	I	
V7	I	
V8	I	
T0	I	The transmitter is configured for 9600 baud
T1	R	if split speed operation is used.
T2	R	
T3	R	
BG	I	Break generation is enabled.
P	R	Parity bit is disabled.
E	R	Parity type is not applicable when P is removed.

Jumper Configuration When Shipped (Cont)

Jumper Designation	Jumper State	Function
1	R	Operation with eight data bits per character.
2	R	(See "Data Bit Selection" table.)
PB	R	Programmable baud rate function disabled.
C	I	Common speed operation enabled.
C1	I	
S	R	Split speed operation disabled.
S1	R	
H	I	Halt on framing error enabled.
B	R	Boot on framing error disabled.
B	I	
1A	I	The 20 mA current loop receiver is
2A	I	configured as an active receiver.
3A	I	
1P	R	
2P	R	
4A	I	The 20 mA current loop transmitter is
5A	I	configured for active operation.
3P	R	
4P	R	
EF	I	Error flags disabled.
M	R	Factory test jumpers. Not defined for field use.
M1	R	
MT	R	Maintenance bit disabled.

Baud Rate Selection

	Bit	Bit	Bit	Bit	Bit	Baud Rate
Program Control	15	14	13	12	11*	
Receive Jumpers	R3	R2	R1	R0		
Transmit Jumpers	T3	T2	T1	T0		
	I	I	I	I		50
	I	I	I	R		75
	I	I	R	I		110**
	I	I	R	R		134.5
	I	R	I	I		150
	I	R	I	R		300
	I	R	R	I		600
	I	R	R	R		1200
	R	I	I	I		1800
	R	I	I	R		2000
	R	I	R	I		2400
	R	I	R	R		3600
	R	R	I	I		4800
	R	R	I	R		7200
	R	R	R	I		9600
	R	R	R	R		19200

I = jumper inserted = program bit cleared.
R = jumper removed = program bit set.

* Bit 11 of the XCSR (write-only bit) must be set in order to select a new baud rate under program control. Also, jumper PB must be inserted to enable baud rate selection under program control.

** When configured for 110 baud, the UART is set for two stop bits.

Data Bit Selection

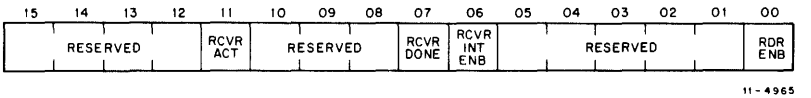
Jumpers		Number of Data Bits
2	1	
I	I	5
I	R	6
R	I	7
R	R	8

Jumper Definitions

Jumper	Function
A3-A12	These jumpers correspond to bits 3-12 of the address word. When inserted, they will cause the bus interface to check for a true condition on the corresponding address bit.
V3-V8	Used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding vector address bit on the LSI-11 bus.
R0-R3	Receiver and transmitter baud rate jumpers selected during common speed operation.
	Receiver-only baud rate select jumpers used during split speed operation.
T0-T3	Transmitter baud rate select jumpers used during split speed operation.
	Both receiver and transmitter baud rates used if maintenance mode is entered during split speed operation.
BG	Jumper is inserted to enable break generation.
P	Jumper is inserted for operation with parity.
E	Removed for even parity; inserted for odd parity. Receiver checks for appropriate parity and transmitter inserts appropriate parity.
1, 2	These jumpers select the desired number of data bits.
PB	Jumper is inserted in order to enable the programmable baud rate capability.

Jumper Definitions (Cont)

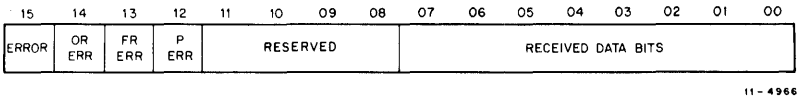
Jumper	Function
C, C1	These jumpers are inserted for common speed operation. Note that S and S1 must be removed when C and C1 are inserted.
S, S1	Inserted for split speed operation. Note that C and C1 must be removed when S and S1 are inserted.
H	This jumper is inserted to assert BHALT L when a framing error is received, except when the maintenance bit is set. This places the LSI-11 in the halt mode.
B,B	Jumper B is inserted to negate BDCOK H when a BREAK signal or framing error is received, except when the maintenance bit is set. This causes the LSI-11 to reload the bootstrap. (Jumper B must be removed when B is inserted.)
1A, 2A, 3A	These three jumpers are inserted to make the 20 mA and 3A current loop receiver active. (Jumpers 1P and 2P are removed when 1A, 2A, and 3A are inserted.)
1P, 2P	These jumpers are inserted to make the 20 mA current loop receiver passive. (Jumpers 1A, 2A, and 3A must be removed when 1P and 2P are installed.)
4A, 5A	Inserted to make the 20 mA current loop transmitter active. (3P and 4P must be removed when 4A and 5A are inserted.)
3P, 4P	Inserted to make the 20 mA current loop transmitter passive. (4A and 5A must be removed when 3P and 4P are inserted.)
EF	Jumper is removed to enable the error flags to be read in the high byte of the receiver buffer.
MT	When inserted, enables maintenance bit.
M, M1	These are test jumpers used during the manufacturing of the module. They are not defined for field use.



DLV11-F RCSR Bit Assignments

DLV11-F RCSR Bit Assignments

Bit	Function
15-12	Not used. Reserved for future use.
11	Receiver Active (RCVR ACT) - When set, this bit indicates that the DLV11-F interface receiver is active. The bit is set at the center of the start bit, which is the beginning of the input serial data from the device, and is cleared by the leading edge of RDONE H.
10-08	Not used. Reserved for future use.
07	Receiver Done (RCVR DONE) - This bit is set when an entire character has been received and is ready for transfer to the LSI-11 bus. When set, initiates an interrupt sequence provided RCVR INT ENB (bit 06) is also set. Read-only bit; cleared whenever the receiver buffer (RBUF) is addressed or whenever RDR ENB (bit 00) is set. Also cleared by INIT.
06	Receiver Interrupt Enable (RCVR INT ENB) - When set, allows an interrupt sequence to start when RCVR DONE (bit 07) sets. Read/write bit; cleared by INIT.
05-01	Not used. Reserved for future use.
00	Reader Enable (RDR ENB) - When set, this bit advances the paper-tape reader in DIGITAL-modified TTY units (LT33-C; LT35-A, -C) and clears the done bit (bit 07). This bit is cleared at the middle of the start bit, which is the beginning of the serial input from an external device. Also cleared by INIT. Write only.



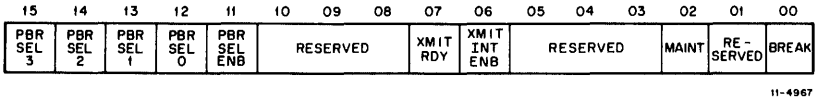
DLV11-F RBUF Bit Assignments

Bit	Function
15	Error - Used to indicate that an error condition is present. This bit is the logical OR of OR ERR, FR ERR, and P ERR (bits 14, 13, and 12, respectively). Whenever one of these bits is set, it causes the error bit to set. This bit is not connected to the interrupt logic. Read-only bit; cleared by removing the error condition.

NOTE

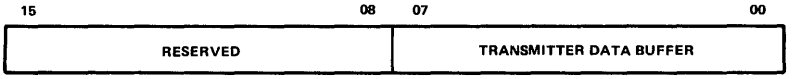
Error indications remain present until the next character is received, at which time the error bits are updated. INIT clears the error bits.

14	Overrun Error (OR ERROR) - When set, indicates that the reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character. Read-only bit; cleared by INIT.
13	Framing Error (FR ERR) - When set, indicates that the character that was read had no valid stop bit. Read-only bit; cleared by INIT.
12	Parity Error (P ERR) - When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected.
11-08	Not used. Reserved for future use.
07-00	Received (Data Bits) - Holds the character just read. If fewer than eight bits are selected, then the buffer is right-justified into the least significant bit positions. Then, the higher unused bit or bits are read as 0s. Read-only bits; not cleared by INIT.



DLV11-F XCSR Bit Assignments

Bit	Function
15-12	Programmable Baud Rate Select (PBR SEL) - When set, these bits choose a baud rate from 50-9600 baud. Write only.
11	Programmable Baud Rate Enable (PBR ENB) - This bit must be set in order to select a new baud rate indicated by bits 12 to 15. Write only.
10-08	Not used. Reserved for future use.
07	Transmitter Ready (XMIT RDY) - This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT ENB (bit 06) is also set.
06	Transmitter Interrupt Enable (XMIT INT ENB) - When set, allows an interrupt sequence to start when XMIT RDY (bit 07) is set. Read/write bits; cleared by INIT.
05-03	Not used. Reserved for future use.
02	MAINT - Used for maintenance function. When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receiver serial input. It also forces the receiver to run at transmitter baud rate speed when split speed operation is enabled. Read/write bit; cleared by INIT.
01	Not used. Reserved for future use.
00	Break - When set, transmits a continuous space to the external device. Read/write bit; cleared by INIT.



DLV11-F XBUF Bit Assignments

Bit	Function
15-08	Not used. Not defined. Not necessarily read as 0s.
07-00	Transmitter Data Buffer - Holds the character to be transferred to the external device. If fewer than eight bits are used, the character must be loaded so that it is right-justified into the least significant bits.

M8029
RXV21 FLOPPY DISK CONTROLLER

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.8		3.0	1.0	BC05L-15

Standard Addresses

	First Controller	Second Controller
RXCS	177170	177200
RXDB	177172	177202

Standard Vectors

264 270

Diagnostic Programs

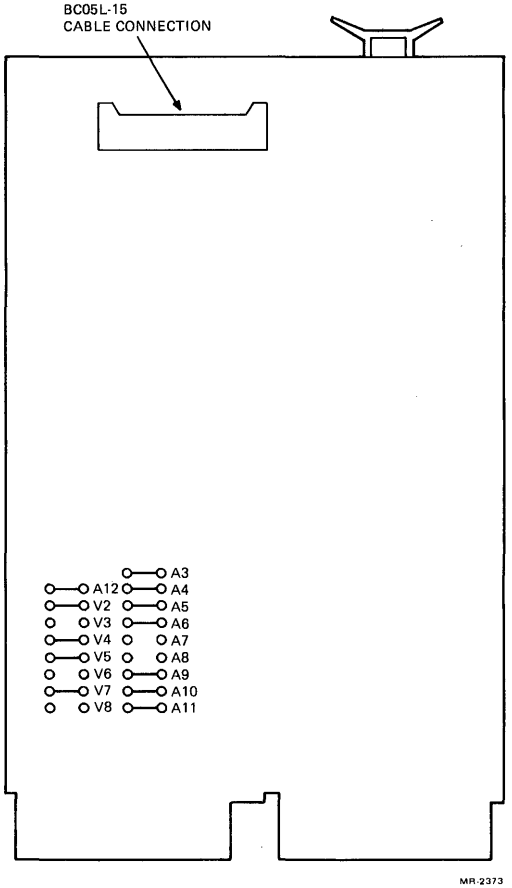
Refer to Appendix A.

Related Documentation

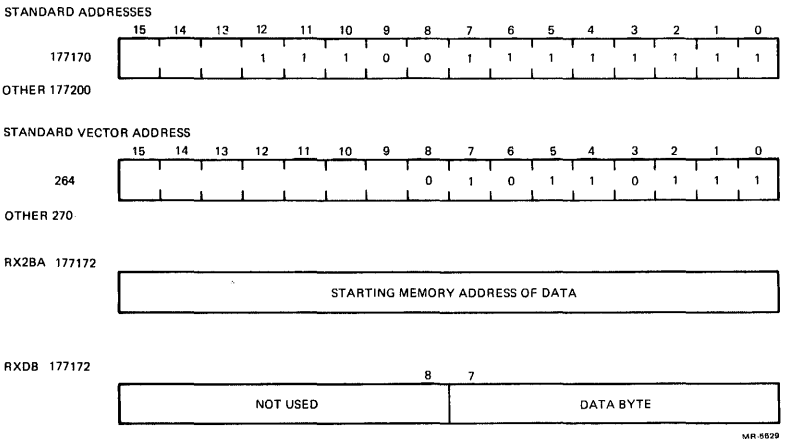
RXV21 Field Maintenance Print Set (MP00628)
RX02 Floppy Disk System User's Guide (EK-RX02-UG)
RX01/RX02 Reference Card (EK-RX102-RC)
RX02 Technical Manual (EK-0RX02-TM)
Minicomputer Interfaces Handbook (EB-20175-20)
RX02 Field Maintenance Print Set (MP-00629-00)

CAUTION

PDP-11/23 systems require the M8029 to be at CS revision E1 or higher.



M8029 Module Address and Vector Jumpers



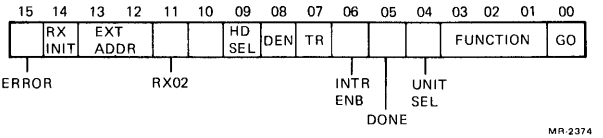
RXV21 Error Codes

Error Reg	Error Codes							
15 14 13 12 11 10 9 8 **Track addr sel DV**	7 **DV SEL**	6 **DEN DV1**	5 **HD LD**	4 **DEN DVO**	3	2	1	0 **DEN CMD**
Target Sector	Target Track							
Current Track DV1	Current Track DVO							
Word Count Reg	Error Code							

The following sequence is used to get definitive error information following a bootstrap operation. (It is assumed that the bootstrap program has halted and the CPU is in ODT.)

1. Examine R5 (RF will contain RXES after an error).
2. Examine RXER by:

   - Loading the READ ERROR REGISTER command into RX2CS (777170/XXXXXX 17<CR>).
   - Examining the four words of error information that will be transferred into locations 2000, 2002, 2004, and 2006.
   - Reading and decoding this information using the format shown below. The error code can be used to help identify the failing FRU.



RX2CS Format RXV21

Bit Definitions

Bit	Function
0	Go - Initiates a command to RX02. Write only.
1-3	Function Select - These bits code one of the eight possible functions described below. Write only.

Code	Function
000	Fill Buffer
001	Empty Buffer
010	Write Sector
011	Read Sector
100	Set Media Density
101	Read Status
110	Write Deleted Data Sector
111	Read Error Code

4	Unit Select - This bit selects one of the two possible disks for execution of the desired function. This bit is readable only when done is set, at which time it indicates the unit previously selected. Read/write.
5	Done - This bit indicates the completion of a function. Done will generate an interrupt when asserted if interrupt enable (RX2CS bit 6) is set. Read only.
6	Interrupt Enable - This bit is set by the program to enable an interrupt when the RX02 has completed an operation (done). The condition of this bit is normally determined at the time a function is initiated. Read/write; cleared by initialize.
7	Transfer Request - This bit signifies that the RXV21 needs data or has data available. Read only.
8	Density - This bit determines the density of the function to be executed. This bit is readable only when done is set, at which time it indicates the density of the function previously executed. Read/write.

Bit Definitions (Cont)

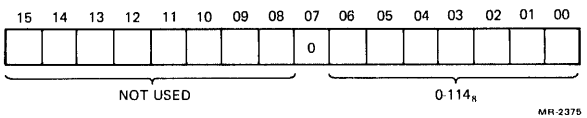
Bit	Function
9	Head Select - This bit selects one of two heads for double-sided operation, readable only when done is set. At that time the side that was previously selected is not valid.
10	Reserved for future use. Must be written as a 0.
11	RX02 - This bit is set by the interface to inform the programmer that this is an RX02 system. Read only.
12-13	Extended Address - These bits are used to declare an extended bus address. Write only.
14	RXV21 Initialize - This bit is set by the program to initialize the RXV21 without initializing all devices on the UNIBUS. Write only.

CAUTION

Loading the lower byte of the RX2CS will also load the upper byte of the RX2CS.

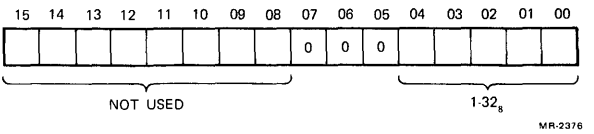
Upon setting this bit in the RX2CS, the RXV21 will negate done and move the head position mechanism of both drives (if two are available) to track 0. Upon completion of a successful initialize, the RX02 will zero the error and status register, and set initialize done. It will also read sector 1 of track 1 on drive 0 into the buffer.

15	Error - This bit is set by the RX02 to indicate that an error has occurred during an attempt to execute a command. Read only; cleared by the initiation of a new command or an initialize.



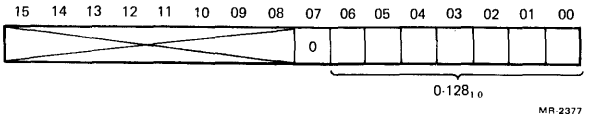
RX2TA Format (RXV21)

RX2TA (RX Track Address) – This register is loaded to indicate on which of the 114_8 ($0-76_{10}$) tracks a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8-15 are unused and are ignored by the control.



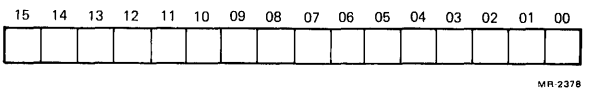
RX2SA Format (RXV21)

RX2SA (RX Sector Address) – This register is loaded to indicate on which of the 32_8 ($1-26_{10}$) sectors a given function is to operate. It can be addressed only under the protocol of the function in progress.



RX2WC Format (RXV21)

RX2WC (RX Word Count Register) – For a double-density sector, the maximum word count is 128_{10}. For a single-density sector the maximum word count is 64_{10}. If a word count is beyond the limit for the density indicated, the control asserts word count overflow (bit 10 of RX2ES). This is a write-only register. The actual word count, and not the 2's complement of the word count, is loaded into the register.



RX2BA and RX2DB Format (RXV21)

RX2BA (RX Bus Address Register) – This register specifies the bus address of data transferred during fill buffer, empty buffer, and read definitive error operations. Incrementation takes place after a memory transaction has occurred. The RX2BA, therefore, is loaded with the address of the first data word to be transferred. This is a 16-bit, write-only register.

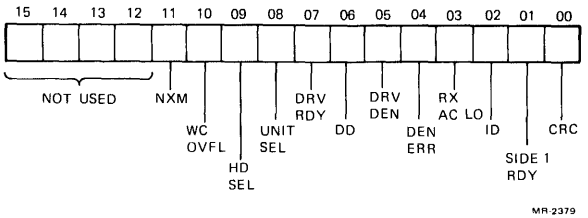
RX2DB (RX Data Buffer) – All information transferred to and from the floppy media passes through this register and is addressable only under the protocol of the function in progress.

RX2DB (Data Buffer Register [177172]) – This register serves as a general purpose data path between the RX02 and the interface. It may represent one of six RX02 registers according to the protocol of the function that is in progress.

This register is read/write if the RX02 is not in the process of executing a command; that is, it may be manipulated without affecting the RX02 subsystem. If the RX02 is actively executing a command, this register will only accept data if RX2CS bit 7 (TR) is set. In addition, valid data can only be read when TR is set.

CAUTION

Violation of protocol in manipulation of the data buffer register may cause permanent data loss.



RX2ES Format (RXV21)

RX2ES (RX Error and Status) – This register contains the current error and status conditions of the drive selected by bit 4 (unit select) of the RX2CS. This read-only register can be addressed only under the protocol of the function in progress. The RX2ES is located in the RX2DB upon completion of a function.

RXES bit assignments are as follows.

Bit Definitions

Bit	Function
0	CRC Error - A cyclic redundancy check error was detected as information was retrieved from a data field of the diskette. The data collected must be considered invalid. The RX2ES is moved to the RX2DB, and error and done are asserted. It is suggested that the data transfer be tried up to 10 times, as most errors are recoverable (soft).
1	Side 1 Ready - This bit, when set, indicates that a double-sided diskette is mounted in a double-sided drive and is ready to execute a function. This bit is valid only at the termination of an initialize sequence or a maintenance READ STATUS command.

Bit Definitions (Cont)

Bit	Function
2	Initialize Done - This bit is asserted in the RX2ES to indicate completion of the initialize routine which can be caused by RX02 power failure, system power failure, or programmable or bus initialize.
3	RX AC LO - This bit is set by the interface to indicate a power failure in the RX02 subsystem.
4	Density Error - This bit indicates that the density of the function in progress does not match the drive density. Upon detection of this error the control terminates the operation and asserts error and done.
5	Drive Density - This bit indicates the density of the diskette in the drive selected (indicated by bit 8). The density of the drive is determined during read and write sector operations.
6	Deleted Data - This bit indicates that in the course of recovering data, the "deleted data" address mark was detected at the beginning of the data field. The DRV DEN bit indicates whether the mark was a single- or double-density deleted data address mark. The data following the mark will be collected and transferred normally, as the deleted data mark has no further significance other than to establish drive density. Any alteration of files or actual deletion of data due to this mark must be accomplished by user software.
7	Drive Ready - This bit indicates that the selected drive is ready if bit 7=1 and all conditions for disk operation are satisfied, such as door closed, power OK, diskette up to speed, etc. The RX02 may be presumed to be ready to perform any operation. This bit is only valid when retrieved via a read status function or initialize.
8	Unit Select - This bit indicates that drive 0 is selected if bit 8=0. This bit indicates the drive that is currently selected.
9	Head Select - This bit indicates which side of a double-sided drive performed the last operation.
10	Word Count Overflow - This bit indicates that the word count is beyond sector size. The fill or empty buffer operation is terminated and error and done are set.
11	Nonexistent Memory Error - This bit is set by the interface when a DMA transfer is being performed and the memory address specified in RX2BA is nonexistent.

Function Codes
Following the strict protocol of the individual function, data storage and recovery on the RXV21 occur with careful manipulation of the RX2CS and RX2DB registers. The penalty for violation of protocol can be permanent data loss.

A summary of the function codes is presented below.

000	Fill Buffer
001	Empty Buffer
010	Write Sector
011	Read Sector
100	Set Media Density
101	Read Status
110	Write Deleted Data Sector
111	Read Error Code

The following paragraphs describe in detail the programming protocol associated with each function encoded and written into RX2CS bits 1-3 if done is set.

Fill Buffer (000) – This function is used to fill the RX02 data buffer with the number of words of data specified by the RX2WC register. Fill buffer is a complete function in itself: the function ends when RX2WC overflows, and if necessary, the control has zero-filled the remainder of the buffer. The contents of the buffer may be written on the disk by means of a subsequent WRITE SECTOR command or returned to the host processor by an EMPTY BUFFER command. If the word count is too large, the function is terminated, error and done are asserted, and the word count overflow bit is set in RX2ES.

To initiate this function the RX2CS is loaded with the function. Bit 4 of the RX2CS (unit select) does not affect this function since no disk operation is involved. Bit 8 (density) must be properly selected since this determines the word count limit. When the command has been loaded, the done bit (RX2CS bit 5) goes false. When the TR bit is asserted, the RX2WC may be loaded into the data buffer register. When TR is again asserted, the RX2BA may be loaded into the RX2DB. The data words are transferred directly from memory and when RX2WC overflows and the control has zero-filled the remainder of the sector buffer, if necessary, done is asserted, ending the operation. If bit 6 RX2CS (interrupt enable) is set, an interrupt is initiated. Any read of the RX2DB during the data transfer is ignored by the interface. After done is true, the RX2ES is located in the RX2DB register.

Empty Buffer (001) – This function is used to empty the contents of the internal buffer through the RXV21 for use by the host processor. This data is in the buffer as the result of a previous FILL BUFFER or READ SECTOR command.

The programming protocol for this function is identical to that for the FILL BUFFER command. The RX2CS is loaded with the command to initiate the function. (This function will ignore bit 4 RX2CS, unit select.) RX2CS bit 8 (density) must be selected to allow the proper word count limit. When the command has been loaded, the done bit (RX2CS bit 5) goes false. When the TR bit is asserted, the RX2WC may be loaded into the RX2DB. When TR is again asserted the RX2BA may be loaded into the RX2DB. The RXV21 assembles one word of data at a time and transfers it directly to memory. Transfers occur until word count overflow, at which time the operation is complete and done goes true. If bit 6 RX2CS (interrupt enable) is set, an interrupt is initiated. After done is true, the RX2ES is located in the data buffer register.

Write Sector (010) – This function is used to locate a desired sector on the diskette and fill it with the contents of the internal buffer. The initiation of the function clears RX2ES, TR, and done.

When TR is asserted, the program must load the desired sector address into RX2DB, which will drop TR. When TR is again asserted, the program must load the desired track address into the RX2DB, which will drop TR. TR will remain unasserted while the RX02 attempts to locate the desired sector. The diskette density is determined at this time and is compared with the function density. If the densities do not agree, the operation is terminated; bit 4 RX2ES is set, RX2ES is moved to the RX2DB, error (bit 15 RX2CS) is set, done is asserted, and an interrupt is initiated, if bit 6 RX2CS (interrupt enable) is set.

If the densities agree but the RX02 is unable to locate the desired sector within two diskette revolutions, the interface will abort the operation, move the contents of RX2ES to the RX2DB, set error (bit 15 RX2CS), assert done, and initiate an interrupt if bit 6 RX2CS (interrupt enable) is set.

If the desired sector has been reached and the densities agree, the RXV21 will write the 128_{10} or 64_{10} words stored in the internal buffer followed by a CRC character which is automatically calculated by the RX02. The RXV21 ends the function by asserting done and, if bit 6 RX2CS (interrupt enable) is set, initiating an interrupt.

CAUTION

The contents of the sector buffer are not valid data after a power loss has been detected by the RX02. However, write sector will be accepted as a valid instruction and the (random) contents of the buffer will be written, followed by a valid CRC.

NOTE

The contents of the sector buffer are not destroyed during a write sector operation.

Read Sector (011) – This function is used to locate the desired sector and transfer the contents of the data field to the internal buffer in the control. This function may also be used to retrieve rapidly (5 ms) the current status of the drive selected. The initiation of this function clears RX2ES, TR, and done.

When TR is asserted the program must load the desired sector address into the RX2DB, which will drop TR. When TR is again asserted, the program must load the desired track address into the RX2DB, which will drop TR.

TR and done will remain negated while the RX02 attempts to locate the desired sector. If the RX02 is unable to locate the desired sector within two diskette revolutions for any reason, the RXV21/RX211 will abort the operation, set done and error (bit 15 RX2CS), move the contents of the RX2ES to the RX2DB, and if bit 6 RX2CS (interrupt enable) is set, initiate an interrupt.

If the desired sector is successfully located, the control reads the data address mark and determines the density of the diskette. If the diskette (drive) density does not agree with the function density the operation is terminated and done and error (bit 15 RX2CS) are asserted. Bit 4 RX2ES is set (density error) and the RX2ES is moved to the RX2DB. If bit 6 RX2CS (interrupt enable) is set, an interrupt is initiated.

If a legal data mark is successfully located, and the control and densities agree, the control will read data from the sector into the internal buffer. If a deleted data address mark was detected, the control will set bit 6 RX2ES (DD). As data enters the internal buffer, a CRC is computed based on the data field and the CRC bytes previously recorded. A nonzero residue indicates that a read error has occurred and the control sets bit 0 RX2ES (CRC error) and bit 15 RX2CS (error). The RXV21 ends the operation by asserting done and moving the contents of the RX2ES into the RX2DB. If bit 6 RX2CS is set, an interrupt is initiated.

If the desired sector is successfully located, the densities agree and the data is transferred with no CRC error; done will be set and if bit 6 RX2CS (interrupt enable) is set, the RXV21 initiates an interrupt.

Set Media Density (100) – This function causes the entire diskette to be reassigned to a new density. Bit 8 RX2CS (density) indicates the new density. The control reformats the diskette by writing new data address marks (double or single density) and zeroing all of the data fields on the diskette.

The function is initiated by loading the RX2CS with the command. Initiation of the function clears RX2ES and done. When TR is set, an ASCII "I" (111) must be loaded into the RX2DB to complete the protocol. This extra character is a safeguard against an error in loading the command. When the control recognizes this character it begins executing the command.

The control starts at sector 1, track 0 and reads the header information, then starts a write operation. If the header information is damaged, the control will abort the operation.

If the operation is successfully completed, done is set and if bit 6 RX2CS (interrupt enable) is set, an interrupt is initiated.

CAUTION

This operation takes about 15 seconds and should not be interrupted. If for any reason the operation is interrupted, an illegal diskette will be generated which may have data marks of both densities. This diskette should be completely reformatted.

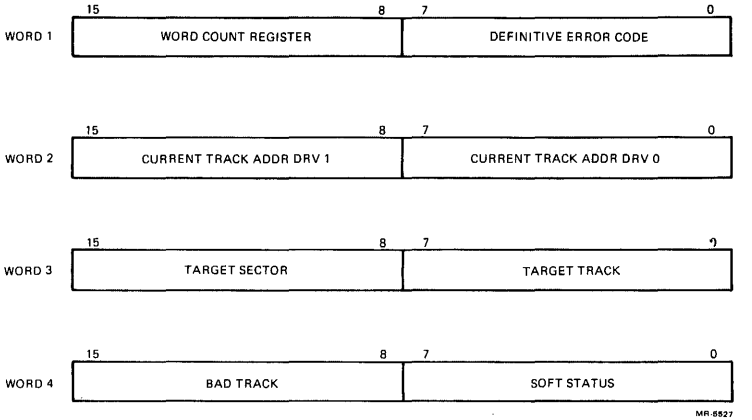
Maintenance Read Status (101) – This function is initiated by loading the RX2CS with the command. Done is cleared. The drive ready bit (bit 7 RX2ES) is updated by counting index pulses in the control. The drive density is updated by loading the head of the selected drive and reading the first data mark. The RX2ES is moved into the RX2DB. The RX2CS may be sampled when done (bit 5 RX2CS) is again asserted and if bit RX2CS (interrupt enable) is set, an interrupt will occur. This operation requires approximately 250 ms to complete.

Write Sector with Deleted Data (110) – This operation is identical to function 010 (write sector) with the exception that a deleted data address mark is written preceding the data rather than the standard data address mark. The density bit associated with the function indicates whether a single- or double-density deleted data address mark will be written.

Read Error Code (111) – The read error code function implies a read extended status. In addition to the specific error code, a dump of the control's internal scratch pad registers also occurs. This is the only way that the word count register can be retrieved. This function is used to retrieve specific information as well as drive status information depending upon detection of the general error bit.

The transfer of the registers is a DMA transfer. The function is initiated by loading the RX2CS with the command; then done goes false. When TR is true, the RX2BA may be loaded into the RX2DB and TR goes false. The registers are assembled one word at a time and are then transferred directly to memory.

FOLLOWING IS THE REGISTER PROTOCOL.



Definitive Error Codes

10	Drive 0 failed to see home on initialize.
20	Drive 1 failed to see home on initialize.
40	Tried to access a track greater than 76.
50	Home was found before desired track was reached.
70	Desired sector could not be found after 52 tries.
110	More than 40 μs and no SEP clock seen.
120	A preamble could not be found.
130	A preamble found but no ID mark found within allowable time.
150	The track address of a good header does not compare with desired track.
160	Too many tries for IDAM.
170	Data was not found in allotted time.
200	CRC on reading the sector from the disk.
220	Failed maintenance wraparound check.
230	Word count overflow.

240 Density error.

250 Incorrect key word on SET DENSITY command.

Register Protocol

Word 1<7:0>	Definitive error codes
Word 1<15:8>	Word count register
Word 2<7:0>	Current track address of drive 0
Word 2<15:8>	Current track address of drive 1
Word 3<7:0>	Target track of current disk access
Word 3<15:8>	Target sector of current disk access
Word 4<7>	Unit select bit*
Word 4<5>	Head load bit*
Word 4<6><4>	Drive density bit of both drives*
Word 4<0>	Density of READ ERROR REGISTER command*
Word 4<15:8>	Track address of selected drive**

RX02 Power Fail or Initialize

When the RX02 control senses a loss of power within the RX02, it will unload the head and abort all controller action. The RXAC L line is asserted to indicate to the RXV21 that subsystem power has gone. The RXV21 asserts done and error and sets the RXAC L bit in the RXZES.

When the RX02 senses the return of power, it will remove done and begin a sequence to:

1. Move each drive head position mechanism to track 0
2. Clear any active error bits
3. Read sector 1 of track 1, on drive 0
4. Assert initialize done in the RXES.

Upon completion of the power-up sequence, done is again asserted. There is no guarantee that information being written at the time of a power failure will be retrievable; however, all other information on the diskette will remain unaltered.

---

* For DMA interfaces, the controller status soft register is sent to the interface at the end of the command. The four status bits are included in an 8-bit word. Unit select = bit 7; density of drive 1 = bit 6; head load = bit 5; density of drive 0 = bit 4; density of READ ERROR REGISTER command = bit 0.

** The track address of the selected drive-error is only meaningful on a code 150 error. The register contains the address of the cylinder that the head reached on a seek error.

M8043
DLV11-J SERIAL LINE UNIT

Amp		Bus Loads		Cables
+5 V	+12 V	AC	DC	
1.0	0.25	1	1	BC21B-XX BC20N-XX (Refer to DLV11-KA) BC20M-XX

Standard Addresses

Configuration No. 1	Channel 0	Channel 1	Channel 2	Channel 3
RCSR	176500	176510	176520	177560
RBUF	176502	176512	176522	177562
XCSR	176504	176514	176524	177564
XBUF	176506	176516	176526	177566
Configuration No. 2				
RCSR	176500	176510	176520	176530
RBUF	176502	176512	176522	176532
XCSR	176504	176514	176524	176534
XBUF	176506	176516	176526	176536

Standard Vectors

Configuration No. 1				
Receiver	300	310	320	60
Transmitter	304	314	324	64

Configuration No. 2

Receiver	300	310	320	330
Transmitter	304	314	324	334

Diagnostic Programs

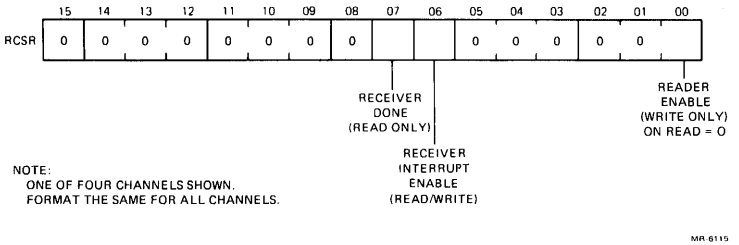
Refer to Appendix A.

NOTE

This test requires that four H3270-A loopback plugs be inserted into the DLV11-J module in order for the diagnostic to run.

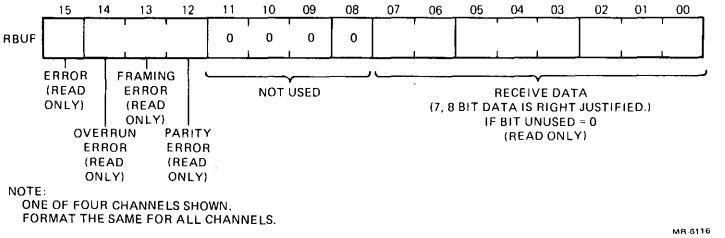
Related Documentation

DLV11-J User's Guide (EK-DLV1J-UG)
Field Maintenance Print Set (MP00586)
Microcomputer Interfaces Handbook (EB-20175-20)



RCSR Registers Bit Assignments

Word	Bit	Function
RCSR	8-15	Not used. On read = 0.
	7	Receiver Done - Set when an entire character has been received and is ready for input to the processor. This bit is automatically cleared when RBUF is read, when INIT is asserted (on power-up or reset instruction), or when reader enable bit is set. Read only. If receiver interrupt enable (bit 6) is set, the setting of receiver done starts an interrupt sequence.
	6	Receive Interrupt Enable - Set under program control when it is desired to allow a receiver interrupt sequence to occur when a character is ready for input to the processor (signified by receiver done being set). Cleared under program control or by INIT. Read/write.
	1-5	Not used. On read = 0.
	0	Reader Enable - Setting this bit advances the paper tape reader on an LT-33 terminal one character at a time and the setting of this bit clears receiver done (bit 7). Write only. The DLV11-KA 20 mA current loop option is required for operation of this bit.



RBUF Register Bit Assignments

Word	Bit	Function
RBUF	15	Channel Error Status - Logical OR of bits 14, 13, and 12. Read only.
	14	Overrun Error - When set, indicates that the reading of the previously received character was not completed (RCVR done not cleared) prior to receiving a new character. The first character is "lost." Read only; cleared by INIT being asserted.

NOTE

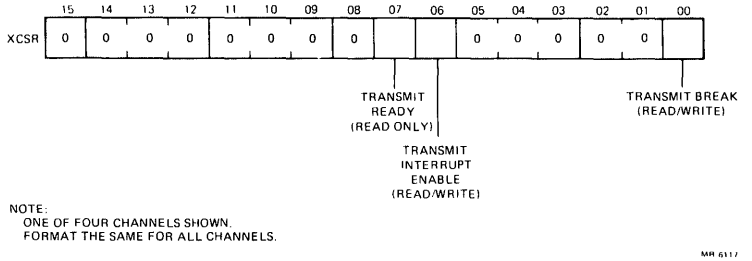
When back-to-back characters are received, one full character time is allowed from the instant when receiver done (bit 7) is set to the occurrence of an overrun error.

	13	Framing Error - When set, indicates that the character read had no valid stop bit. This indicates that the currently received character and the next character are invalid. Read only; cleared by INIT.
	12	Parity Error - When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no-parity operation is configured for the channel. Read only.

NOTE

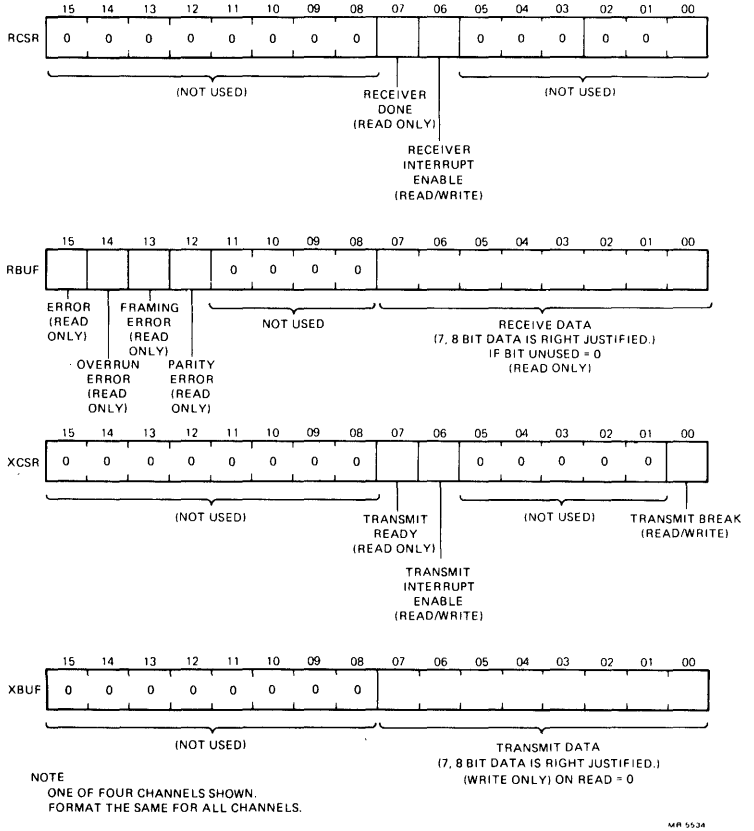
Error bits remain valid until the next character is received, at which time the error bits are updated.

	8-11	Not used. On read = 0.
	0-7	Data Bits - Contains seven or eight data bits in a right-justified format. Bit 7 = 0 when seven data bits are enabled. Read only.



XCSR Registers Bit Assignments

Word	Bit	Function
XCSR	8-15	Not used. On read = 0.
	7	Transmit Ready - Set when XBUF is empty and can accept another character for transmission. It is also set by INIT during the power-up sequence or during a reset instruction. If transmitter interrupt enable (bit 6) is set, the setting of transmit ready will start an interrupt sequence. Read only.
	6	Transmit Interrupt Enable - Set under program control when it is desired to generate a transmitter interrupt request (when transmitter is ready to accept a character for transmission). The bit is cleared under program control, during power-up sequence, or reset instruction. Read/write.
	1-5	Not used. On read = 0.
	0	Transmit Break - Set or reset under program control. When set, a continuous space level is transmitted. However, transmit done and transmit interrupt enable can still operate, allowing software timing of break. When not set, normal character transmission can occur. Read/write; cleared by INIT being asserted.

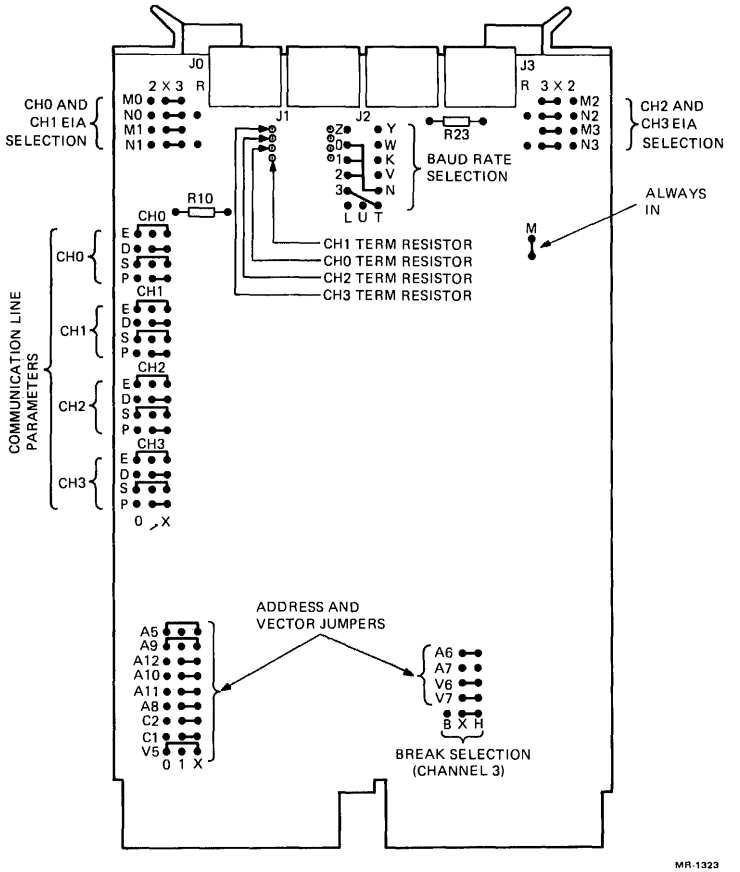


DLV11-J SLU Register Formats

XBUF Register Bit Assignments

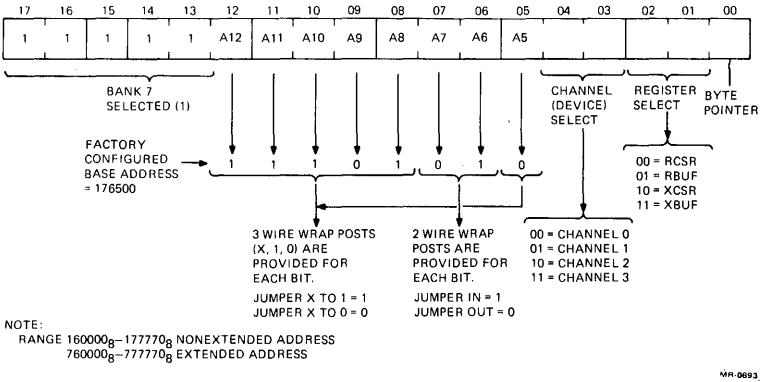
XBUF	8-15	Not used. On read = 0.
	0-7	Data bits - Contains seven or eight right-justified data bits. Loaded under program control for serial transmission. Write only.

Jumper Configurations



DLV11-J Component and Jumper Factory Configuration Summary

Address Selection



Device Register Address Format

It is possible to independently configure the last four addresses (channel 3) to the LSI-11 console device (addresses 177560-177566) when certain base addresses and console select jumpers* are installed. In this configuration, the preceding addresses (channels 0, 1, and 2) are not affected; they are normal offsets of the configured base device address as shown in the following table.

General Device Register Address Assignments (Without Console Selected)

Address	Device Register
Module Base Address (BA)	Channel 0 RCSR
BA + 2	Channel 0 RBUF
BA + 4	Channel 0 XCSR
BA + 6	Channel 0 XBUF
BA + 10	Channel 1 RCSR
BA + 12	Channel 1 RBUF
BA + 14	Channel 1 XCSR
BA + 16	Channel 1 XBUF
BA + 20	Channel 2 RCSR
BA + 22	Channel 2 RBUF
BA + 24	Channel 2 XCSR
BA + 26	Channel 2 XBUF
BA + 30	Channel 3 RCSR
BA + 32	Channel 3 RBUF
BA + 34	Channel 3 XCSR
BA + 36	Channel 3 XBUF

*Console select jumpers C1 and C2 installed select channel 3 as console device.

General Device Register Address Assignments (General Configuration With Console Selected)

Address	Device Register
Module Base Address (BA)	Channel 0 RCSR
BA + 2	Channel 0 RBUF
BA + 4	Channel 0 XCSR
BA + 6	Channel 0 XBUF
BA + 10	Channel 1 RCSR
BA + 12	Channel 1 RBUF
BA + 14	Channel 1 XCSR
BA + 16	Channel 1 XBUF
BA + 20	Channel 2 RCSR
BA + 22	Channel 2 RBUF
BA + 24	Channel 2 XCSR
BA + 26	Channel 2 XBUF
177560	Channel 3* RCSR
177562	Channel 3 RBUF
177564	Channel 3 XCSR
177566	Channel 3 XBUF

*Channel 3 is enabled as a console device.

Specific Device Register Address Assignments (DLV11-J Configured With BA = 176500 and BV = 300 Without Console Selected)

Address	Register	Vector	Channel
176500	RCSR	300	
176502	RBUF		Channel 0
176504	XCSR	304	
176506	XBUF		
176510	RCSR	310	
176512	RBUF		Channel 1
176514	XCSR	314	
176516	XBUF		
176520	RCSR	320	Channel 2
176522	RBUF		
176524	XCSR	324	
176526	XBUF		
176530	RCSR	330	
176532	RBUF		Channel 3
176534	XCSR	334	
176536	XBUF		
177560	RCSR	60	
177562	RBUF		
177564	XCSR	64	Channel 3
177566	XBUF		Console Device

NOTE
All addresses are in octal notation.

Vector Selection

When channel 3 is configured as the console device interface using console select jumpers C1 and C2, the interrupt vectors of the channel become 60 and 64. This is true regardless of the configured base vector of the module. It should be noted that the preceding channels (0, 1, and 2) are not affected and their vectors are normal offsets of the base vector configured, as shown in the following table.

General Vector Assignments (Without Console Selected)

Vector Offsets	Interrupt Vector
Module Base Vector (BV)	Channel 0 Receiver
BA + 4	Channel 0 Transmitter
BA + 10	Channel 1 Receiver
BA + 14	Channel 1 Transmitter
BA + 20	Channel 2 Receiver
BA + 24	Channel 2 Transmitter
BA + 30	Channel 3 Receiver
BA + 34	Channel 3 Transmitter

General Vector Assignments (With Console Selected)

Vector Offsets	Interrupt Vector
Module Base Vector (BV)	Channel 0 Receiver
BA + 4	Channel 0 Transmitter
BA + 10	Channel 1 Receiver
BA + 14	Channel 1 Transmitter
BA + 20	Channel 2 Receiver
BA + 24	Channel 2 Transmitter
60	Channel 3 Receiver*
64	Channel 3 Transmitter*

*Console selected

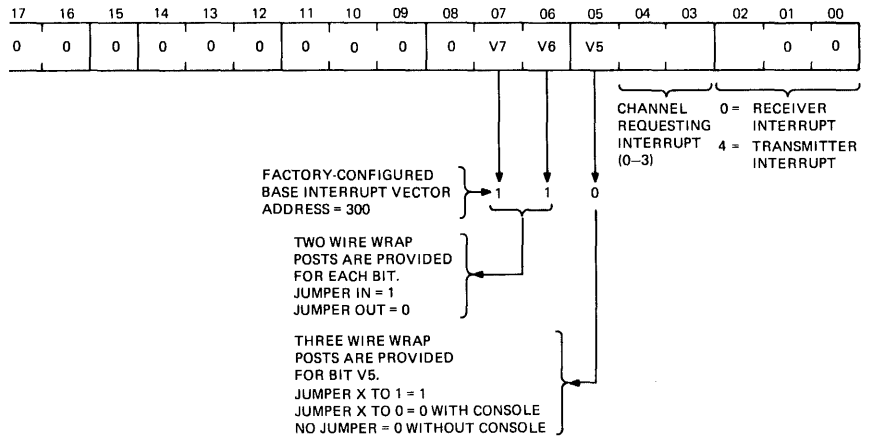
Specific Vector Assignments
(DLV11-J Configured With BV = 300
Without Console Selected)

Octal Vector	Interrupt Vector
300	Channel 0 Receiver
304	Channel 0 Transmitter
310	Channel 1 Receiver
314	Channel 1 Transmitter
320	Channel 2 Receiver
324	Channel 2 Transmitter
330	Channel 3 Receiver
334	Channel 3 Transmitter

Specific Vector Assignments
(Factory-Configured With BV = 300
With Console Selected)

Octal Vector	Interrupt Vector
300	Channel 0 Receiver
304	Channel 0 Transmitter
310	Channel 1 Receiver
314	Channel 1 Transmitter
320	Channel 2 Receiver
324	Channel 2 Transmitter
60	Channel 3 Receiver*
64	Channel 3 Transmitter*

*Console selected



OTE:
RANGE $0–377_8$ (040_8 NOT ALLOWED IN CONSOLE MODE)

MR-0895

Console device jumpers are used to select channels as the console interface. These jumpers (C1 and C2) will affect address and vector selection.

Summary of Console Selection Jumper Configurations

Label	Console Selected	Console Not Selected
C1	Install jumper from wirewrap pins X to 1.	Install jumper from wirewrap pins X to 0.
C2	Install jumper from wirewrap pins X to 1.	Install jumper from wirewrap pins X to 0.

Configuring Channel Word Formats

Each DLV11-J SLU channel can be individually configured for number of data bits (7 or 8); even, odd, or not parity; 1 or 2 stop bits, and baud rate (described in the next section). A summary of possible character format jumper configurations is shown below.

Summary of Character Format Jumper Configurations

Label	UART Parameter	X to 0	X to 1	Comments
D	Number of data bits	7 bits	8 bits	LSB is transmitted first
S	Number of stop bits	1 bit	2 bits	
P	Parity inhibit	Parity generation and detection enabled	Parity generation and detection disabled	
E	Even parity enabled	Odd parity enabled	Even parity enabled	Requires P jumper connected from X to 0

NOTE

E jumper must be connected to either 0 or 1, even if the parity bit is disabled. Two stop bits are generally used only with Teletype terminals.

CAUTION

To prevent hardware damage within the channel, the E jumper must ALWAYS be installed. This is true regardless of the configuration of the P (parity) jumper.

Baud Rate Selection

NOTE

A 110 baud rate clock generator circuit is contained on the optional DLV11-KA 20 mA option. When 110 baud operation is desired, do not connect the baud rate jumper on the DLV11-J module for that particular channel. The 110 baud rate will be supplied by the DLV11-KA option through the interface connector.

Configure baud rates (except 110 baud) by connecting a jumper from an appropriate baud rate generator output wirewrap pin to the baud rate clock input pin (labeled 0-3); one jumper is required for each channel. Baud rate generator outputs are identified below.

Baud Rate Generator Outputs

Wirewrap Pin Label	Baud Rate (Bit/S)
U	150
T	300
V	600
W	1200
Y	2400
L	4800
N	9600
K	19200
Z	38400

NOTE

If more than one channel requires the same baud rate, the wirewrap jumpers may be daisy-chained.

Channel 3 Break Response

Channel 3 (normally used as the console device) can respond to a break condition on the receive line such as when an operator presses the BREAK key on the associated terminal. The BREAK key transmits a continuous space signal which is detected by the DLV11-J circuits as a framing error. If no operation is desired, do not connect jumpers to the B, X, and H wirewrap pins.

Channel 3 Break Operation Jumper Summary

Break Response Operation	Jumper Connection
Boot	Install jumper between wirewrap pins X and B.
Halt	Install jumper between wirewrap pins X and H.
No response	No jumper installed.

Summary of Serial Channel Signal Level Compatibility Configurations

Serial Channel Signal Level

Serial Channel Signal Level Modifiers	EIA RS-422	EIA RS-232C and RS-423	20 mA Current Loop (Required DLV11-KA Option)
M0-3 jumpers	Connect wire-wrap pins X and 2.	Connect wire-wrap pins X and 3.	Connect wirewrap pins X and 3.
N0-3 jumpers	Connect wire-wrap pins X and 2.	Connect wire-wrap pins X and 3.	Connect wirewrap pins X and R for program-controlled paper tape reader functionality.
Termination resistor (one per channel)	Install a 100 Ω, 1/4 W, non-wire-wound, fusible resistor.	No resistor installed.	No resistor installed.
Wave shaping resistor, one per channel pair (channel pairs 0 and 1; 2 and 3).	Not required.	Install resis-tor (see next table). 1/4 W non-wirewound.	Install 22 K Ω non-wirewound resistor.

EIA RS-422 - To configure an SLU channel for EIA RS-422 signal levels, connect the M(M0-M3) and N(N0-N3) jumper wirewrap pin X of the desired channel to the respective wirewrap pin 2. Install (solder) a 100 ohm, 1/4 W fusible resistor (non-wirewound) into the termination resistor mounting pads for the channel being configured. The resistor must be removed for any configuration other than EIA RS-422.

EIA RS-423 and RS-232C - To configure an SLU channel to be compatible with both the EIA RS-423 and RS-232C (which on the DLV11-J are met simultaneously), connect each M(M0-M3) and N(N0-N3) jumper X wirewrap pin of the desired channel to the respective wirewrap pin 3.

Slew Rates - The signal rise and fall time may be controlled on EIA RS-423 and RS-232C SLU channel configurations by installing (soldering) an appropriate value of non-wirewound, 1/4 W resistor into the wave-shaping resistor pads provided (R10 and/or R23). An appropriate resistor value can be selected by referring to the following table. The value of resistor R10 determines the slew rate of both channels 0 and 1 which are simultaneously set to the same value. Similarly, R23 controls the slew rate of both channels 2 and 3.

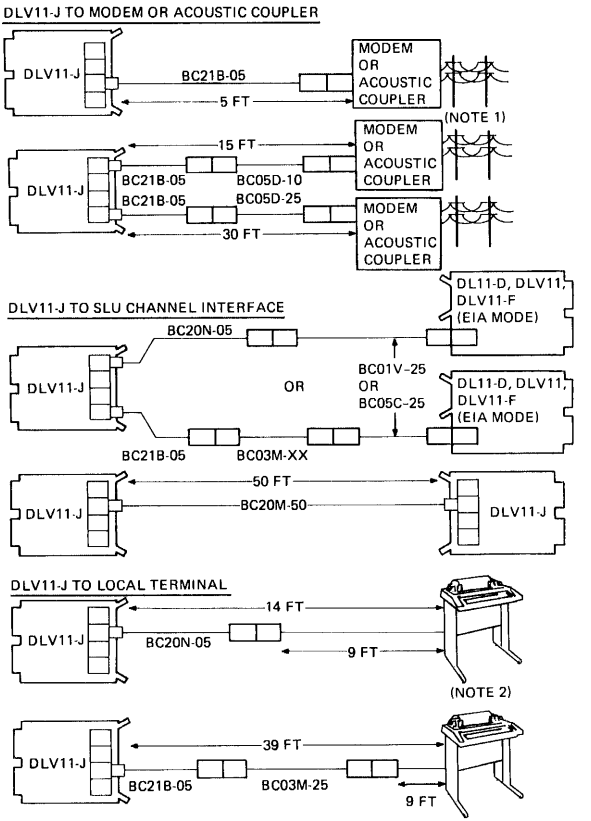
EIA RS-423 and RS-232C Wave-Shaping Resistor Values

Baud Rate	Wave-Shaping Resistor
38.4K	22 kΩ
19.2K	51 kΩ
9.6K	120 kΩ
4.8K	200 kΩ
2.4K	430 kΩ
1.2K	820 kΩ
600.0	1 MΩ
300.0	1 MΩ
150.0	1 MΩ
110.0	See Note.

NOTE
Determined by other channel of the two-channel pair.

20 mA Current Loop - To configure an SLU channel for 20 mA current loop operation, connect the M(M0-M3) jumper pin X to pin 3 for the desired channel. If the 20 mA terminal contains a paper-tape reader that can be program-controlled (such as a DEC-modified LT-33 Teletype or Teletype ASR-33 with LT22-MD modification kit), connect wirewrap jumper N(N0-N3) pin X to the respective pin R.

When the DLV11-KA 20 mA current loop option is connected to the channel interface connector, operating power for the option circuits is supplied by the DLV11-J. To configure a channel for 110 baud operation, enable the 110 baud rate clock on the DLV11-KA option and remove the baud rate selector jumper for the channel on the DLV11-J module. The clock needed by the DLV11-J is automatically supplied through the serial line connector cable.

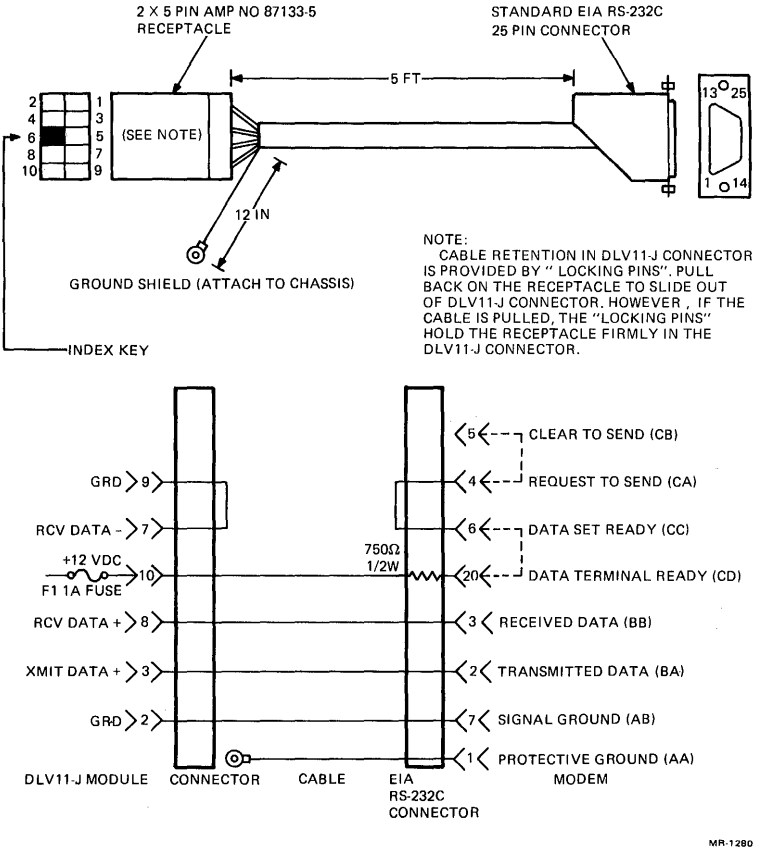


NOTES:

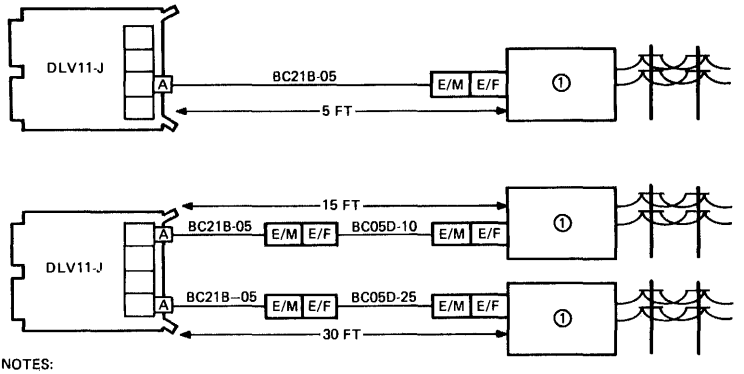
1. MODEM USED IS A "MANUAL TYPE" SUCH AS BELL 103A WITH 804B.
2. DEC EIA RS-232C TERMINALS (VT52, LA36, LS120, ETC.) COME EQUIPPED WITH A 9 FT CABLE. NON-DEC EIA RS-232C TERMINALS ARE CONNECTED SIMILARLY EXCEPT 9 FT OF LENGTH MUST BE DEDUCTED FROM THE TOTAL CABLE LENGTH.

MR-1326

DLV11-J Cabling Summary



BC21B-05 Peripheral Device Cable



NOTES:

① MODEM OR ACOUSTIC COUPLER. MODEMS SHOWN ARE "MANUAL" MODEMS SUCH AS BELL 103A DATA SETS WITH 804B AUXILIARY SET.

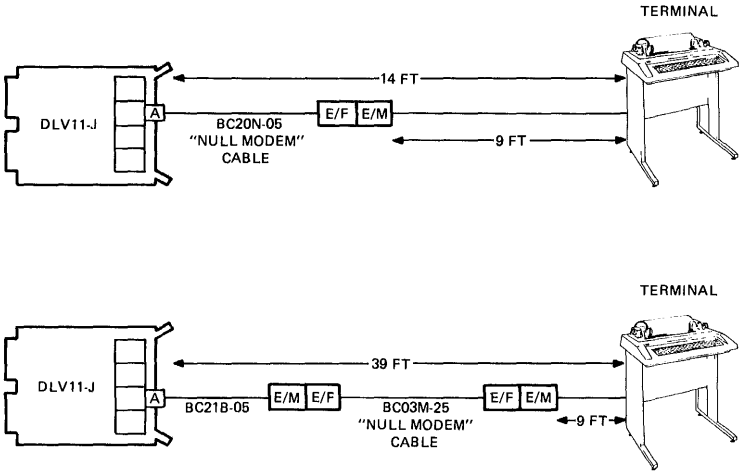
A = 2 X 5 PIN AMP NO 87133-5 CONNECTORS

E/M = EIA RS-232C 25 PIN MALE CONNECTORS

E/F = EIA RS-232C 25 PIN FEMALE CONNECTORS

MR-1281

DLV11-J to Modem or Acoustic Coupler



NOTES

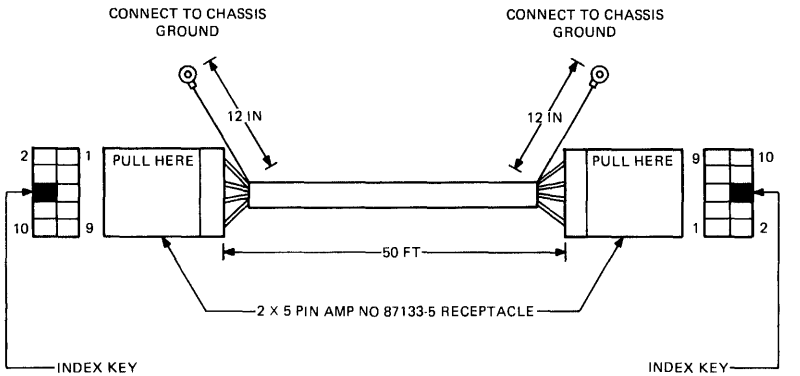
TERMINALS SHOWN ARE DEC EIA RS-232C TERMINALS (SUCH AS VT52, LA36, LS120, ETC.)

DEC TERMINALS ARE CONSTRUCTED WITH 9 FOOT CABLES, WHEN USING NON-DEC EIA RS-232C TERMINALS DEDUCT 9 FEET FROM THE TOTAL CABLE LENGTH.

[A] = 2 X 5 PIN AMP NO 87133-5 CONNECTORS
[E/M] = EIA RS-232C 25 PIN MALE CONNECTORS
[E/F] = EIA RS-232C 25 PIN FEMALE CONNECTORS

MR-1282

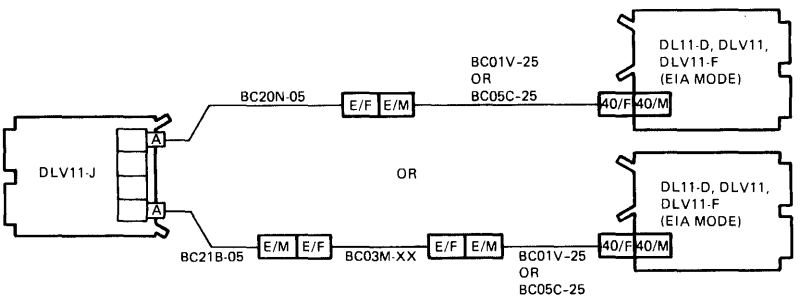
Local Terminal Cabling



NOTE
BOTH CONNECTORS HAVE THE SAME CABLE RETENTION MECHANISM. CABLE RETENTION IS PROVIDED BY "LOCKING PINS". PULL ON RECEPTACLE TO RELEASE.

MR-1283

BC20M-50 DLV11-J to DLV11-J Cable



A = 2 x 5 PIN AMP NO 87133-5 CONNECTORS

E/M = EIA RS-232C 25 PIN MALE CONNECTORS

E/F = EIA RS-232C 25 PIN FEMALE CONNECTORS

40/M = 40 PIN BERG MALE CONNECTORS

40/F = 40 PIN BERG FEMALE CONNECTORS

MR-1328

DLV11-J to SLU Module Cabling

M8044/45
MSV11-D, -E MOS READ/WRITE MEMORY

Model	Memory Capacity	Module	Parity Bits
MSV11-DA	4K by 16 bits	M8044-AA	No
MSV11-DB	8K by 16 bits	M8044-BA	No
MSV11-DC	16K by 16 bits	M8044-CA	No
MSV11-DD	32K by 16 bits	M8044-DA	No
MSV11-ED	32K by 18 bits	M8045-DA	Yes

Amps		Bus Loads		Cables
+5	+12	AC	DC	
2.0	0.41	2	1	None

Standard Addresses

Module is shipped configured to start at bank 0.

Vectors

None

Diagnostic Programs

Refer to Appendix A.

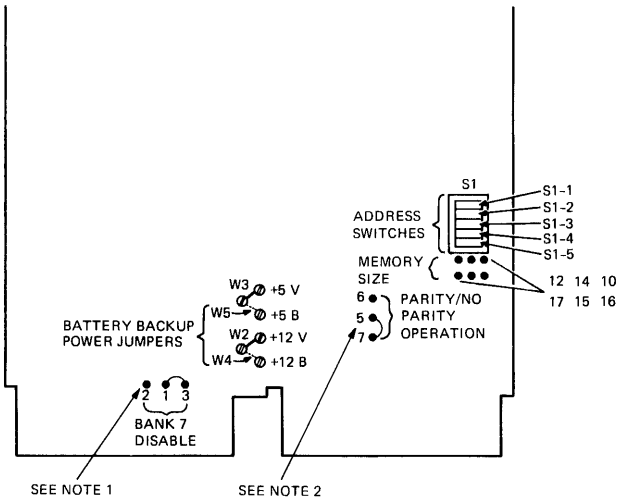
NOTE
DEC diagnostic will not check parity.

Related Documentation

MSV11-D, -E User's Manual (EK-MSV1D-OP)
Field Maintenance Print Set (MP00259)
Microcomputer Processor Handbook (EB-18451-20)

Address Selection

The MSV11-D or MSV11-E address can start at any 4K bank boundary. The address configured is the starting address for the contiguous portion of memory (4K, 8K, 16K, or 32K) contained on the module.



MSV11-D, MSV11-E Switch and Jumpers M8044,45

Set the switches to the desired starting address as listed in the table. Note that the module is designated to accommodate a 128K system addressing capability. However, the present addressing capability of the LSI-11 system, including all PDP-11/03, PDP-11V03 and PDP-11T03 systems, is 32K. PDP-11/23 systems, however, can address within the full 128K word range. By PDP-11 convention, the upper 4K address space is normally reserved for peripheral device and register addresses. Thus, with the present LSI-11 maximum addressing capability of 32K, bank 7 (address 160000-177777) normally should not be used for system memory.

Factory-configured modules will not respond to bank 7 addresses. In special applications that permit the use of the lower 2K portion of bank 7 for system memory (i.e., MINC), enable the lower 2K portion of bank 7 by removing the jumper from wirewrap pins 1 and 3 and connecting a new jumper from 1 to 2.

NOTE

If 30K option is enabled, some diagnostics may not run.

Battery Backup Power

MSV11-D and MSV11-E modules are factory configured with power jumpers installed for normal system power only. If the system uses a battery backup power source, remove jumpers W2 and W3. Install new jumpers W4 and W5. (Two jumpers are removed and two new jumpers are installed.)

Parity

One jumper is factory installed for nonparity (MSV11-D) or parity (MSV11-E) operation, depending on the model. Do not reconfigure this jumper. Standard jumper configurations are listed below.

- All MSV11-D models: jumper installed from pin 7 to pin 5.
- All MSV11-E models: jumper installed from pin 6 to pin 5.

NOTE

This memory parity feature is not supported by DEC diagnostics or CPUs.

Memory Size

Two jumpers are factory installed to configure addressing logic for memory size (number and type of memory-integrated circuits). Do not reconfigure these jumpers. Standard jumper configurations are listed below.

Models	Jumpers (Two Installed) Memory Select Pins	Memory Range Pins
MSV11-DA	From 17 to 14	From 17 to 15
MSV11-DB	From 12 to 14	From 17 to 15
MSV11-DC	From 16 to 14	From 16 to 15
MSV11-DD, ED	From 10 to 14	From 16 to 15

MSV11-D, MSV11-E Addressing Summary

Starting Address	Switch Settings S1-1	S1-2	S1-3	S1-4	S1-5	MSV11-DA, MSV11-EA	4K Memory Bank(s) Selected MSV11-DB, MSV11-EB	MSV11-DC, MSV11-EC	MSV11-DD, MSV11-ED
0	N	N	N	N	N	0	0-1	0-3	0-7
20000	N	N	N	N	F	1	1-2	1-4	1-10
40000	N	N	N	F	N	2	2-3	2-5	2-11
60000	N	N	N	F	F	3	3-4	3-6	3-12
100000	N	N	F	N	N	4	4-5	4-7	4-13
120000	N	N	F	N	F	5	5-6	5-10	5-14
140000	N	N	F	F	N	6	6-7	6-11	6-15
160000	N	N	F	F	F	7	7-10	7-12	7-16
200000	N	F	N	N	N	10	10-11	10-13	10-17
220000	N	F	N	N	F	11	11-12	11-14	11-20
240000	N	F	N	F	N	12	12-13	12-15	12-21
260000	N	F	N	F	F	13	13-14	13-16	13-22
300000	N	F	F	N	N	14	14-15	14-17	14-23
320000	N	F	F	N	F	15	15-16	15-20	15-24
340000	N	F	F	F	N	16	16-17	16-21	16-25
360000	N	F	F	F	F	17	17-20	17-22	17-26
400000	F	N	N	N	N	20	20-21	20-23	20-27
420000	F	N	N	N	F	21	21-22	21-24	21-30
440000	F	N	N	F	N	22	22-23	22-25	22-31
460000	F	N	N	F	F	23	23-24	23-26	23-32

MSV11-D, MSV11-E Addressing Summary (Cont)

Starting Address	Switch Settings S1-1	S1-2	S1-3	S1-4	S1-5	MSV11-DA, MSV11-EA	4K Memory Bank(s) Selected MSV11-DB, MSV11-EB	MSV11-DC, MSV11-EC	MSV11-DD, MSV11-ED
500000	F	N	F	N	N	24	24-25	24-27	24-33
520000	F	N	F	N	F	25	25-26	25-30	25-34
540000	F	N	F	F	N	26	26-27	26-31	26-35
560000	F	N	F	F	F	27	27-30	27-32	27-36
600000	F	F	N	N	N	30	30-31	30-33	30-37
620000	F	F	N	N	F	31	31-32	31-34	X
640000	F	F	N	F	N	32	32-33	32-35	X
660000	F	F	N	F	F	33	33-34	33-36	X
700000	F	F	F	N	N	34	34-35	34-37	X
720000	F	F	F	N	F	35	35-36	X	X
740000	F	F	F	F	N	36	36-37	X	X
760000	F	F	F	F	F	37	X	X	X

NOTES

1. Switch settings:
   N = ON
   F = OFF
2. In unmapped systems, bank 7 cannot be selected as factory configured; however, the user can enable the lower 2K portion of bank 7.
3. X = Do not use.

M8047
MXV11-AA/AC MULTIFUNCTION MODULE

The MXV11 is a multifunction option module used for the LSI-11, LSI-11/2, or LSI-11/23 systems. It contains read/write memory provisions for read-only memory, two asynchronous serial line interfaces and a 60 Hz clock derived from a crystal oscillator.

Detailed technical information is beyond the scope of this document. Additional information can be found in the *Microcomputer Processor Handbook*, EB-18451-20.

Model Designations

- MXV11-AA contains 8K bytes of random access memory.
- MXV11-AC contains 32K bytes of random access memory.

Both models have two 24-pin sockets that provide for +5 V read-only memories in which 1K × 8, 2K × 8, or 4K × 8 ROMs may be used. These sockets may also be used for 256 words of bootstrap code.

Amps		Bus Loads		Cables
+5	+12	AC	DC	BC20M-XX
1.2	0.1	2	2	BC20N-XX (Refer to DLV11-KA)
				BC21B-XX

Standard Addresses

RAM - Starts on any 8K boundary below 64KB.

SLU	Channel 0	Channel 1
	176500	177560

Standard Vectors

SLU	300	60

M8047

Diagnostic Programs

Refer to Appendix A.
Requires wraparound connectors to completely exercise SLU.

Options

MXV11-A2 Boot ROMs for RX02, RX01, or TU58
PNs: 23-039D1-00, 23-040D1-00

ROMs

Power: +5 V ± 5%

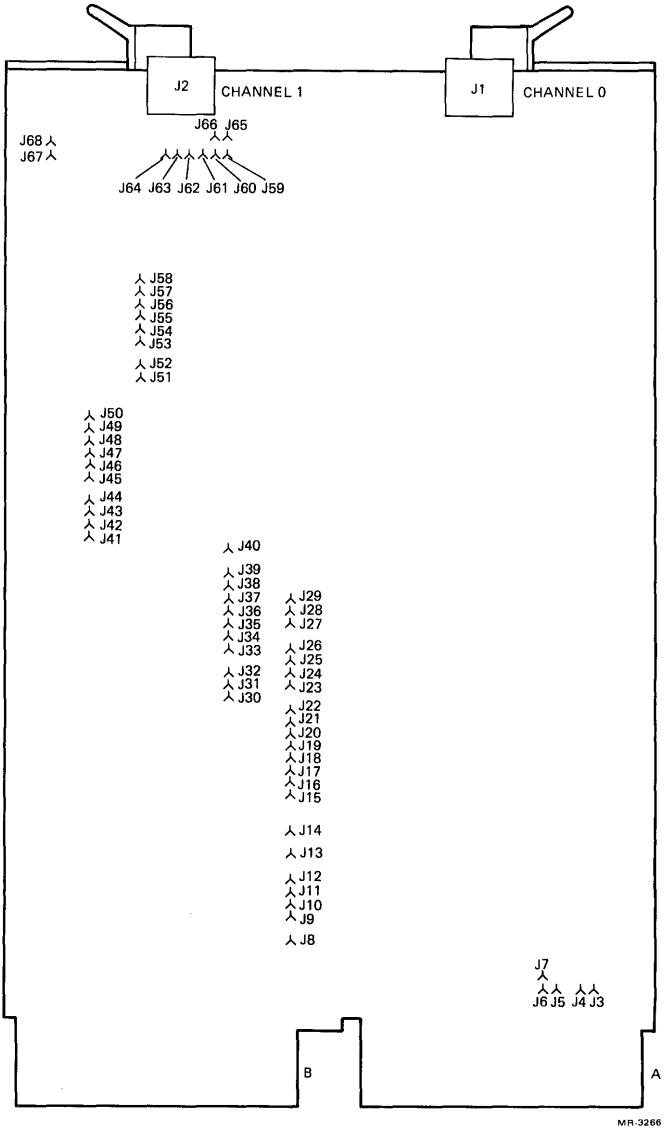
Pins: 24-Pin DIP

Access Time: Up to 450 nanoseconds

Array Size: 1K × 8, 2K × 8, or 4K × 8 bits

Type: Typical PROM types:

UV PROMs	Chip Array Size	Memory Size
Intel 2758	1K × 8 bits	1K words
Intel 2716	2K × 8 bits	2K words
Intel 2732	4K × 8 bits	4K words
Mostek MK2716	2K × 8 bits	2K words
T.I. TMS 2516	2K × 8 bits	2K words
T.I. TMS 2532	4K × 8 bits	4K words
Bipolar PROMs		
Intel 3628	1K × 8 bits	1K words
Signetics 82S 2708	1K × 8 bits	1K words
Signetics 82S 181	1K × 8 bits	1K words
Signetics 82S 191	2K × 8 bits	2K words



MXV11-A Jumper Locations

MXV11-A Jumper Functions

Pin	Function	Option
J3	Clock L. Open collector output of the clock. Connected to pin AF1 (SSpare 2). Wirewrap to J4 to implement the clock option.	60 Hz
J4	BEVNT L. Event interrupt (pin BR1) used for the clock option.	60 Hz
J5	BDCOK H. DCOK (pin BA1) when high allows the processor to operate; when low initializes the system. Connected to J6 to use the boot option.	Boot
J6	Framing Error. Open collector output of framing error from serial line one. Connected to pin AE1 (SSpare 1). Wirewrap to J5 to implement the boot option. Reset by bus initialize or reception of a valid character.	Break
J7	BHALT L. Halt (pin AP1) when low will stop program execution and cause the processor to enter ODT microcode. Connected to J6 to implement the halt option.	Halt
J8	GND. A ground signal that can be used to disable ROM by wirewrapping to J21 or to disable a serial line by wirewrapping to an address input pin (J23 or J24 for serial line 0; or J25, J26, J27, or J28 for serial line 1).	ROM
J9	A13 L. Address bit 13 asserted low. Wirewrap to J11 to select bank 1 with the ROM address decoder.	ROM
J10	A13 H. Address bit 13 asserted high. Wirewrap to J11 to select bank 0 with the ROM address decoder.	ROM
J11	A13 M. Address bit 13 input to the ROM address decoder. See J9 and J10. Used only if J20 is wirewrapped to J21.	ROM
J12	A03 H. Address bit 03 asserted high. Wirewrapped to the serial line address decoders (J23 or J24 for serial line 0, J25, J26, J27 or J28 for serial line 1) when address bit 03 is to be decoded as a 1.	SLU

MXV11-A Jumper Functions (Cont)

Pin	Function	Option
J13	A04 H. Address bit 04 asserted high. Wirewrapped to the serial line address decoders when address bit 04 is to be decoded as a 1.	SLU
J14	A05 H. Address bit 05 asserted high. Wirewrapped to the serial line one address decoder when address bit 05 is to be decoded as a 1.	SLU
J15	A09 H. Address bit 9 asserted high. Wirewrapped to the serial line one address decoder when address bit 09 is to be decoded as a 1.	SLU
J16	A09 L. Address bit 09 asserted low. Wirewrapped to the serial line one address decoder when address address bit 09 is to be decoded as a 0.	SLU
J17	A05 L. Address bit 05 asserted low. Wirewrapped to the serial line one address decoder when address bit 05 is to be decoded as a 0.	SLU
J18	A04 L. Address bit 04 asserted low. Wirewrapped to the serial line address decoders when address bit 04 is to be decoded as a 0.	SLU
J19	A03 L. Address bit 03 asserted low. Wirewrapped to the serial line address decoders when address bit 03 is to be decoded as a 0.	SLU
J20	ROM address. Output of the ROM address decoder. Connected to J21 when ROM is to be used in bank 0 or bank 1.	ROM
J21	ROM select. ROM address selection enable asserted high. Wirewrapped to J8 (GND) to disable ROM, to J20 for bank 0 or bank 1, or to J22 for bootstrap.	ROM
J22	Boot address. Output of the bootstrap address decoder. Connected to J21 when ROM is to be used in the bootstrap range from 173000-173776 (773000-773776 for LSI-11/23).	BOOT
J23	Serial line 0 address decoder input asserted high. May be wirewrapped to A03 H (J12), A03 L (J19), A04 H (J13), or A04 L (J18).	SLU

MXV11-A Jumper Functions (Cont)

Pin	Function	Option
J24	Serial line 0 address decoder input asserted high. May be wirewrapped to A03 or A04, whichever bit is not wired to J23. May be wirewrapped to GND (J8) to disable serial line 0.	SLU
J25-J28	Serial line 1 address decoder input asserted high. Four address decoder inputs to be connected to address bits A03, A04, A05, and A09. Whether the high or low assertion state of a bit is wirewrapped to an input determines if that bit is decoded as a 1 or a 0. See J12 through J19. May be wirewrapped to GND (J8) to disable serial line 1.	SLU
J29	ROM address bit 09 input. Wirewrapped to A09 H (J15) for normal ROM addressing and also for the MXV11-A2 option when the TU58 bootstrap is desired. Wirewrapped to A09 L (J16) for the MXV11-A2 option when the disk bootstrap is desired.	ROM
J30-J32	RAM starting address selection. These pins are wirewrapped to J33 (logic 0) or J34 (logic 1) to select the RAM starting address (see the following).	RAM

J32	J31	J30	Bank	Starting Address
0	0	0	0	000000
0	0	1	1	020000
0	1	0	2	040000
0	1	1	3	060000
1	0	0	4	100000
1	0	1	5	120000
1	1	0	6	140000
1	1	1	7	160000

J33	GND. Logic 0 level signal used for selecting the RAM starting address and for enabling some ROM ICs in the ROM sockets.	RAM, ROM
J34	+3 V. Logic 1 level signal used for selecting the RAM starting address and for enabling some ROM ICs in the ROM sockets.	RAM, ROM

MXV11-A Jumper Functions (Cont)

Pin	Function	Option
J35	A12 H. Address bit 12 asserted high. Used for addressing 4K × 8 bit ROMs. Wirewrapping to J37, J38 or J39, depending on the ROM used.	ROM
J36	A11 H. Address bit 11 asserted high. Used for addressing 2K × 8 and 4K × 8 bit ROMs. Wire-wrapping to J37, J38, or J39, depending on the ROM.	ROM
J37	Pin 18 on both ROM sockets. Used for addressing or enabling ROM. Wirewrapped to J33 for ground, to J34 for +13 V, to J35 for A12, or to J36 for A11.	ROM
J38	Pin 19 on both ROM sockets. Used for addressing or enabling ROM. Wirewrapped to J33 for ground, to J34 for +3 V, to J35 for A12, or to J36 for A11.	ROM
J39	Pin 21 on both ROM sockets. Used for addressing or enabling ROM. Wirewrapped to J33 for ground, to J34 for +3 V, to J35 for A12 to J36 for A11 or to J40 for +5 V.	ROM
J40	+5 V. Used to power some ROMs on pin 21.	ROM
J41	Used for 150 baud. Wirewrapped to J45 for serial line 0, to J46 for serial line 1. (See following table.)	SLU
J42	Used for 1200 baud.	SLU
J43	Used for 300 baud.	SLU
J44	Used for 2400 baud.	SLU
J45	Clock 0. The clock input for serial line 0 transmit and receive, 16 times the baud rate. Wirewrapped to either J41, J42, J43, J44, J47, J48, J49, or J50.	SLU
J46	Clock 1. The clock input for serial line 1 transmit and receive, 16 times the baud rate. Wirewrapped to either J41, J42, J43, J44, J47, J48, J49, or J50.	SLU
J47	Used for 4800 baud.	SLU
J48	Used for 9600 baud.	SLU

MXV11-A Jumper Functions (Cont)

Pin	Function	Option
J49	Used for 19.2K baud.	SLU
J50	Used for 38.4K baud.	SLU
J51	Vector 0. Vector enable for channel 0. Used to drive vector bits that pass the test: logic 1 for channel 0, and logic 0 for channel 1. Wirewrapped to J53 for bit 03, to J54 for bit 04, to J55 for bit 05, to J56 for bits 06 and 07.	SLU
J52	Vector 1. Vector enable for channel 1. Used to drive vector bits that pass the test: logic 0 for channel 0 and logic 1 for channel 1. Wirewrapped to J53 for bit 03, to J54 for bit 04, to J55 for bit 05, to J56 for bits 06 and 07.	SLU
J53	Vector bit 03. Selects how bit 03 is to be driven for interrupt vectors. Wirewrapped to J51 if a logic 1 for channel 0 and a logic 0 for channel 1; to J52 if a logic 0 for channel 0 and a logic 1 for channel 1; to J57 if a logic 0 for both channel 0 and channel 1; or to J58 if a logic 1 for both channel 0 and channel 1.	SLU
J54	Vector bit 04. Selects how bit 04 is to be driven for interrupt vectors. Wirewrapped the same as J53.	SLU
J55	Vector bit 05. Selects how bit 05 is to be driven for interrupt vectors. Wirewrapped the same as J53.	SLU
J56	Vector bits 06 and 07. Selects how bits 06 and 07 are to be driven for interrupt vectors. Wirewrapped the same as J53.	SLU
J57	GND. Logic 0 signal for configuring vector bits. Wirewrapped to J53, J54, J55 and/or J56 when the corresponding vector bit(s) will be logical 0 for both serial line channels.	SLU
J58	+3 V. Logic 1 signal for configuring vector bits. Wirewrapped to J53, J54, J55 and/or J56 when the corresponding vector bit(s) will be logical 1 for both serial line channels.	SLU

MXV11-A Jumper Functions (Cont)

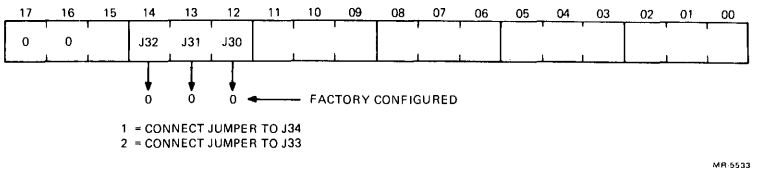
Pin	Function	Option
J59	Seven bits parity, eight bits no parity, channel 1. Wirewrapped to ground (J65) for seven bits with parity or to +3 V (J66) for eight bits with no parity.	SLU
J60	Two stop bits. Selects one or two stop bits for channel 1. Wirewrapped to ground (J65) for one stop bit or to +3 V (J66) for two stop bits.	SLU
J61	Even parity. Selects odd or even parity for channel 1 when seven bits with parity (J59 wirewrapped to ground) is selected. Wirewrapped to ground (J56) for odd parity or to +3 V (J66) for even parity.	SLU
J62	Seven bits parity, 8 bits no parity, channel 0. Wirewrapped to ground (J65) for seven bits with parity or to +3 V (J66) for eight bits with no parity.	SLU
J63	Two stop bits. Selects one or two stop bits for channel 0. Wirewrapped to ground (J65) for one stop bit or to +3 V (J66) for two stop bits.	SLU
J64	Even parity. Selects odd or even parity for channel 0 when seven bits with parity (J59 wirewrapped to ground) is selected. Wirewrapped to logic 0 (J65) for odd parity or to logic 1 (J66) for even parity.	SLU
J65	Logic 0. Ground signal used for configuring serial line interfaces.	SLU
J66	Logic 1. +3 V signal used for configuring line interfaces.	SLU
J67	Clock in. Clock input for baud rates, memory refresh and negative voltage generator. Wirewrapped to J68. Not a user option.	SLU
J68	Clock out. Crystal oscillator output at 19.6608 MHz. Wirewrapped to J67. Not a user option.	SLU

Standard Factory Configuration

Function	Wirewrap From	Pins To	Wirewrap Level
RAM Bank 0	J30	J31	L1
	J32	J33	L1
	J31	J32	L2
SLU Channel 0 Address 176500	J23	J18	L1
	J24	J19	L1
SLU Channel 1 Address 177560	J28	J19	L2
	J26	J15	L1
	J25	J14	L1
	J27	J13	L1
ROM Bootstrap (TU58)	J37	J38	L1
	J21	J22	L1
	J34	J37	L2
	J33	J39	L2
	J29	J15	L2
SLU Vectors CH0 (300)	J53	J57	L1
CH1 (60)	J54	J52	L1
	J56	J51	L1
	J54	J55	L2
SLU Parameters (8 Data Bits,	J59	J61	L1
No Parity, 1 Stop Bit)	J62	J64	L1
	J60	J63	L1
	J61	J62	L2
	J59	J66	L2
	J63	J65	L2
Baud Rates CH0 (38.4K)	J45	J50	L1
CH1 (9600)	J46	J48	L1
Break Generation (Halt Option)	J6	J7	L1
Crystal Clock	J68	J67	L1

Configuring the RAM
The RAM can be configured to start on any 8KB boundary below 64KB. Because of this restriction, the MXV11 (8KB version) is not usable for memory above 56KB. The MXV11 can be used in 18-bit memory address systems, but it is restricted to being assigned to the memory area at or below 56KB.

Five wirewrap terminals, J30 through J34, select the starting address. The following figure shows the jumper configurations required to obtain the desired starting addresses.



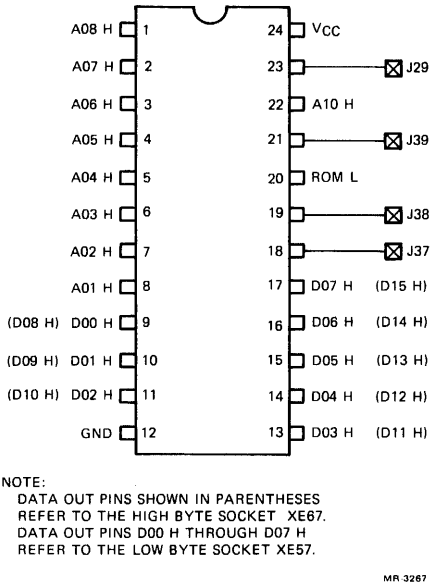
RAM Starting Address Selection

Configuring the ROM
Depending on the ROM type, the module's capacity is 1K, 2K, or 4K words using a pair of 1024 × 8-, 2048 × 8-, or 4096 × 8-bit ROMs respectively. The user configures jumpers on the module for the ROM type being used. The actual procedure for loading data into EPROMs, PROMs (or writing specifications for masked ROMs) will vary depending on the manufacturer, and is beyond the scope of this section. The user must refer to the manufacturer's data sheets and to the chapter, "Using PROMs" in the *Microcomputer Processor Handbook*, EB-18451-20. The user must be aware of the relationship of the EPROM, PROM, or ROM pins to the LSI-11 data bits, and the relationship of the pins to the memory address bits. Refer to the following figure for ROM socket pin assignments. All ROMs used on the MSV11-A must conform to these pin assignments.

The factory configuration allows for using the MSV11-A2 bootstrap ROMs.

Configuring the Bootstrap ROM – The ROM can be configured to operate in the I/O page to support bootstrap programs. The address area contains 256 words from 173000 to 173776 (773000 to 773776 for the LSI-11/23).

The MXV11-A is configured at the factory to allow for using the MXV11-A2 TU58 bootstrap. To reconfigure the MXV11-A to use the disk bootstrap, remove jumper J29 to J15 and install jumper J29 to J16.



MXV11-A ROM Socket Pin Assignment

ROM Bank Selection – If the MXV11-A sockets are used for program ROM instead of a bootstrap ROM, the memory must be selected by a jumper connecting J20 to J21. When main ROM memory is selected, the entire 4K word bank is enabled. If a 1K or 2K ROM is used, it will "wraparound" and give invalid data, depending on how the address lines are configured when the nonexisting ROM area is addressed. Main memory may be positioned in bank 0 or bank 1. To position the ROM in bank 0, jumper J10 to J11. To position the ROM in bank 1, jumper J9 to J11.

Configuring the Specific ROM Types – Additional jumpers must be connected depending on the type of ROM used. The "EPROM Address Jumpers" table describes the jumper configuration when using typical ROMs such as the Intel 2716 (2K × 8) or 2732 (4K × 8) EPROMs. The user must refer to the manufacturer's data sheets when configuring jumpers for other ROM types.

The function of wirewrap pins J29, J38, J37, and J39 are shown in the following table. These pins are to be connected as required to pins J33 through J40.

EPROM Address Jumpers

Function	From	2716 ROM Bank 0 to	2716 ROM Bank 1 to	2732 ROM Bank 0 to	2732 ROM Bank 1 to
Bank Enable	J20	J21	J21	J21	J21
Bit 09 Input	J29	J15	J15	J15	J15
Address or Enable	J38	J36	J36	J36	J36
Address or Enable	J37	J33	J33	J35	J35
Address or Enable	J39	J40	J40	J33	J34

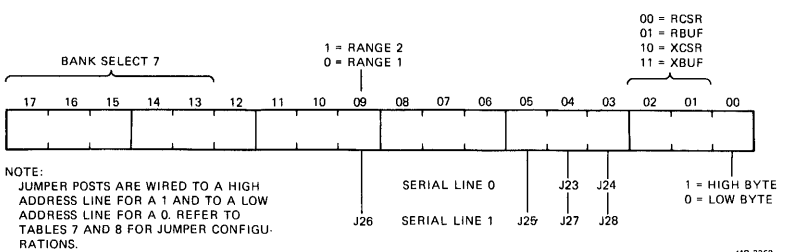
CONFIGURING THE SERIAL LINE UNITS

Serial Line Register Address Selection

Four device registers (RCSR, RBUF, XCSR, and XBUF) are provided for each of the two serial lines. Jumpers are configured to establish separate base addresses for each serial line as shown.

- Serial port 0 may be assigned to one of the four starting addresses: 176500, 176510, 176520, 176530.
- Serial port 1 may be assigned addresses in two ranges. The first range starts at 176500 and covers the eight starting addresses from 176500 to 176570. The second range starts at 177500 and also contains eight possible starting addresses, including the standard console address, 177560. Since several other standard DIGITAL devices use addresses in this second range, it is recommended that only the console address be used.

The format of an SLU address is shown in the following figure. Note that bits 13-17 are neither configured nor decoded by the MXV11-A module. These bits are decoded by the bus master module as the bank 7 select (BBS7 L) bus signal. This signal becomes active only when the I/O page is accessed. Bit 0 is used as the byte pointer.



MXV11-A SLU Address Format

Bits 1 and 2 select one of the four device registers within the addressed serial line. Bits 3 and 4 are used to select one of four possible device addresses for serial line 0. Bits 3, 4, 5, and 9 are used to select the device addresses in two ranges for serial line 1 (console). The following table describes the jumper combinations to select one of four device addresses for serial line 0 (I/O).

Serial Line 0 Address Jumpers

Address (Octal)	Jumper Posts J23 to	J24 to
176500	J18 (Logic 0)	J19 (Logic 0) Factory Configuration
176510	J18 (Logic 0)	J12 (Logic 1)
176520	J13 (Logic 1)	J19 (Logic 0)
176530	J13 (Logic 1)	J12 (Logic 1)

NOTE

Logic 1	Logic 0
J13 (A04 H)	J18 (A04 L)
J12 (A03 H)	J19 (A03 L)

Serial line 1 may have 16 possible device addresses in two ranges. The following table describes the jumper combinations to select the eight device registers available in range 1. Only one device address is used in range 2.

Serial Line 1 Address Jumpers

Address (Octal) Range 1	Jumper Posts J26 to	J25 to	J27 to	J28 to
176500	J16	J17	J18	J19
176510	J16	J17	J18	J12
176520	J16	J17	J13	J19
176530	J16	J17	J13	J12
176540	J16	J14	J18	J19
176550	J16	J14	J18	J12
176560	J16	J14	J13	J19
176570	J16	J14	J13	J12
Range 2				
177560	J15	J14	J13	J19

(See the following Note.)

NOTE

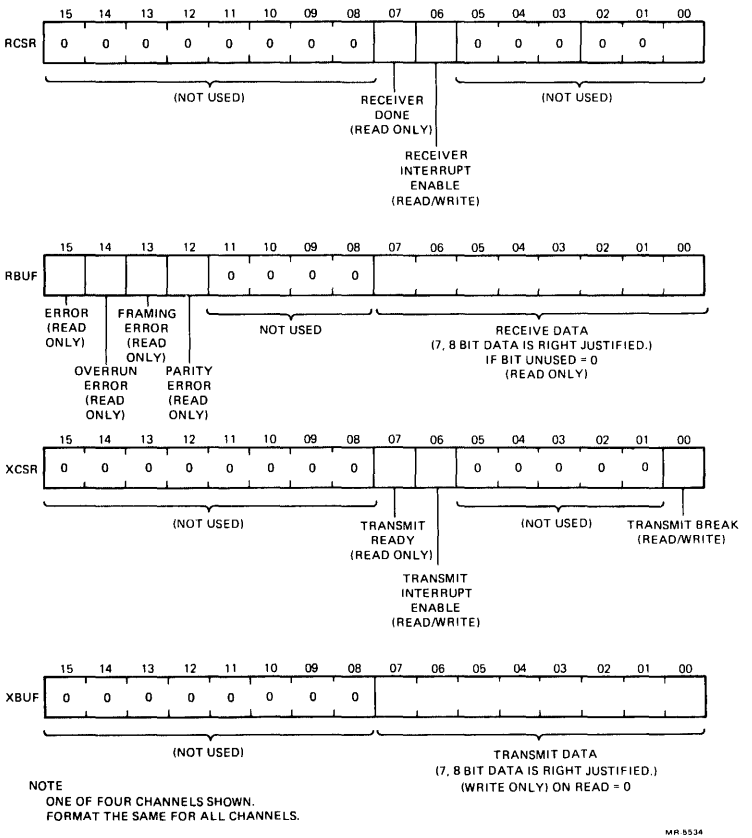
Factory configurations use only one address in range 2 to avoid possible device conflicts. The remaining addresses are pre-assigned to other devices.

Logic 1	Logic 0
J15 (A09 H)	J16 (A09 L)
J14 (A05 H)	J17 (A05 L)
J13 (A04 H)	J18 (A04 L)
J12 (A03 H)	J19 (A03 L)

Control/Status Register

The MXV11-A has two control/status registers (CSRs) for each of its two serial line units. The following figure shows the control/status registers and the read/write data registers. Transmitter control/status registers 0 and 1 (XCSR0 and 1) and receiver control/status registers 0 and 1 (RCSR0 and 1) operate with serial lines 0 and 1, respectively.

Both serial line units have the same bit assignments. There are four registers for each serial line. They are sequential in this order: 0, receiver status; 2, receiver data; 4, transmitter status; and 6, transmitter data. All unused bits are read as 0.



MXV11-A SLU CSR Formats

Bit Assignments for the Receiver Status Register

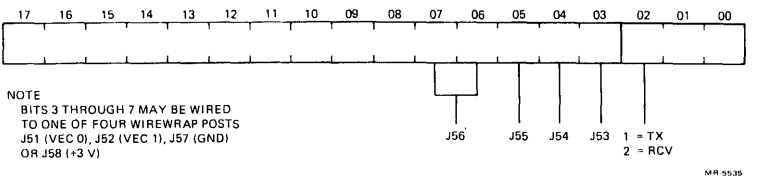
Bit	Function
6	Interrupt enable, read/write. A 1 enables receiver interrupts, a 0 disables interrupts. Cleared by initialize.
7	Receiver done, read only. A 1 indicates that the serial interface has received a character. If enabled by bit 6, receiver done will request an interrupt. Receiver done is cleared by reading the receiver data register or by initialize.
0-7	Data bits, read only. Bit 0 is the least significant bit and bit 7 is the most significant. If seven data bits plus parity is selected, bit 7 will always read as a 0.
12	Parity error, read only. A 1 indicates that the word being read in bits 0 through 6 has a parity error. Bit 12 will always read 0 when eight data bits and no parity are selected. Cleared when read, or by initialize.
13	Framing error, read only. A 1 indicates that a start bit was detected, but there was no corresponding stop bit. A framing error will be generated when a break is received. Cleared when read, or by initialize.
14	Overrun error, read only. A 1 indicates that a word in the receiver buffer had not been read when another word was received and placed in the receiver buffer. Cleared when read, or by initialize.
15	Error, read only. A 1 indicates that one or more of bits 12, 13, and 14 are 1. Cleared when read, or by initialize.

Bit Assignments for the Transmitter Status Register

Bit	Function
0	Break, read/write. When set to a 1, bit 0 causes the serial output signal to go to a space condition. A space condition longer than a character time causes a framing error when it is received and is regarded as a break. Cleared by writing a 0, or by bus initialize.
6	Interrupt enable, read/write. A 1 enables transmitter interrupts; a 0 disables interrupts. Cleared by initialize.
7	Transmitter ready, read only. A 1 indicates that the serial interface is ready to accept a character into the transmitter data register. If enabled by bit 6, transmitter ready will request an interrupt. Transmitter ready is cleared when data is written into the transmitter data register. It is set by initialize.
0-7	Data bits, write only. Bit 0 is the least significant bit and bit 7 is the most significant bit. If seven data bits plus parity are selected, bit 7 will not be transmitted. The transmitter data register will read all 0s.

Interrupt Vector Selection

Two consecutive interrupt vectors (one for receive and one for transmit) are provided for each of the two serial lines. The interrupt vector format is shown in the following figure. Each SLU port can be independently configured to operate in one of two ranges: 000 to 074, or 300 to 376.



MXV11-A Interrupt Vector Format

The following table lists the vector addresses that may be assigned to the serial lines. Note that all vector addresses in the 000 to 074 range, except 060, are reserved vector locations. The jumper selectable bits are 3 through 7. Bits 6 and 7 are wired together.

Serial Line Vector Addresses

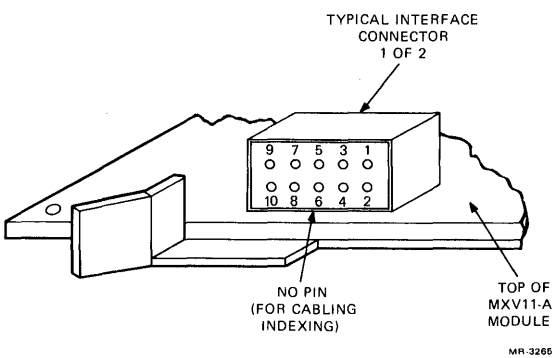
Serial Line 1 (Console)	Serial Line 0 (I/O)
000	300
010	310
020 DIGITAL Reserved	320
030 Do not use	330
040	340
050	350
060 Console	360
070 DIGITAL Reserved	370

The following example illustrates the procedure for configuring the vector addresses. Assume that 60 is the address for serial line 1 (console) and 310 is the address for serial line 0 (I/O). The example describes the relationship between the vector bases, vector address bits, and the jumper posts. The jumpers are configured using the following four rules.

1. If a bit = 1 in both vector bases, it is tied to J58 (logic 1).
2. If a bit = 0 in both vector bases, it is tied to J57 (logic 0).
3. If a bit = 1 for serial line 1 and a 0 for serial line 0, it is tied to J52 (vector 1).
4. If a bit = 0 for serial line 1 and a 1 for serial line 0, it is tied to J51 (vector 0).

Interface Connector Pins

Two 10-pin connectors (one for each serial line) are provided on the MXV11-A module. Connector pins and signal functions are described in the following table and shown in the following figure.



MXV11-A Connector Pins

MXV11-A I/O Connector Pin Functions

Pin	Signal	Function
1	UART CLOCK	The baud rate clock appears on this pin. When an internal baud rate is selected, this pin is a TTL output. When no baud rate is selected on the module, this is an external baud rate input. The high level for the clock > 3.0 V.
2	GND	
3	XMIT+	Transmitter output
4	GND	
5	GND	
6	NC	Key, pin not provided
7	RCV−	Receiver input most negative
8	RCV+	Receiver input most positive
9	GND	
0	+12 V	Power for the DLV11-KA option

Current Loop

The MXV11-A module can interface with 20 mA active or passive current loop devices when used with the DLV11-KA option. This option consists of a DLV11-KB (EIA to 20 mA current loop converter) and a BD21A-03 interface cable. The MXV11-A does not have the capability to support the reader-run portion of the DLV11-KA option. The DLV11-KA option is placed between the MXV11-A serial line output and the 20 mA current loop peripheral device.

MXV11-A Interface Cables

Cable	Application	Length
BC21B-05	EIA RS-232C modem cable to interface with modems and acoustic couplers (2 × 5-pin AMP female to RS-232C male).	1.5 m (5 ft)
BC20N-05	EIA RS-232C null modem cable to directly interface with a local EIA RS-232C terminal (2 × 5-pin AMP female to RS-232C female).	1.5 m (5 ft)
BC20M-50	EIA RS-422 or RS-423 cable for high-speed transmission (19.2K baud) (2 × 5-pin AMP female to 2 × 5-pin AMP female).	15 m (50 ft)
BC05D-10	Extension cable used in conjunction with BC21B-05.	3 m (10 ft)
BC05D-25	Extension cable used in conjuntion with BC21B-05.	7.6 m (25 ft)
BC03M-25	"Null modem" extension cable used in conjunction with BC21B-05.	7.6 m (25 ft)

NOTE

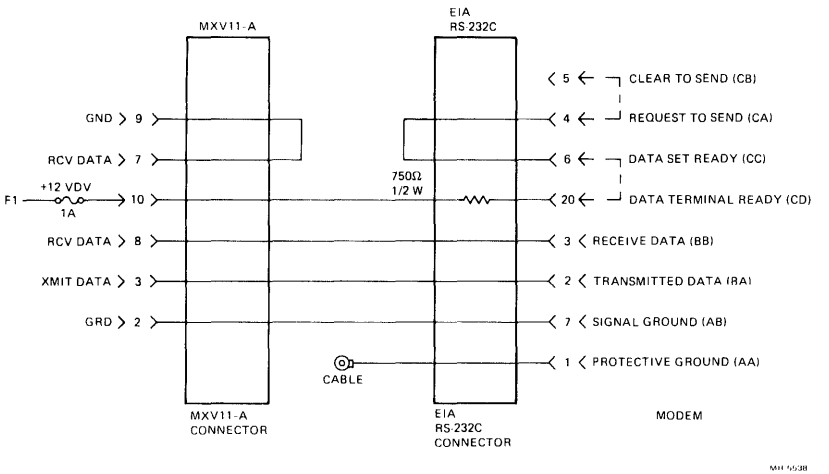
"Strapped" logic levels are provided on Data Terminal Ready (DTR) and Request To Send (RTS) for operation of modems with manual provisions (such as Bell 103A data set with 804B auxiliary set).

The MXV11-A may operate with several peripheral device cables and options for flexibility when configuring systems. A variety of cables and options, as well as the primary application of each, are shown with the MXV11-A.

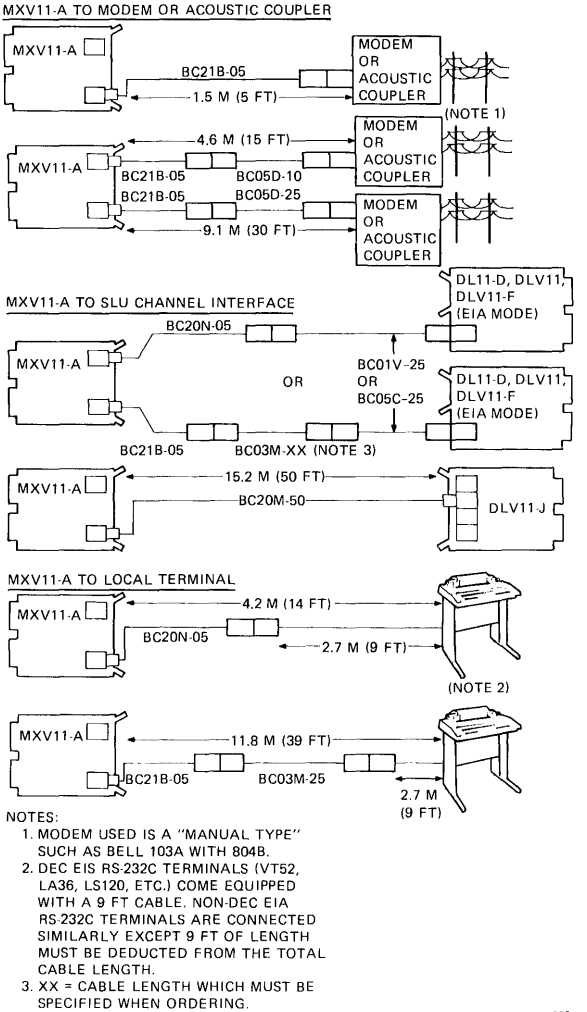
1. The receivers on the MXV11 have differential inputs. Therefore, when designing an RS-232C or RS-423 cable, receive data (pin 7 on the 2 × 5-pin AMP connector) must be tied to signal ground (pins 2, 5, or 9) in order to maintain proper EIA levels (see the following figure).
2. To connect directly to a local EIA RS-232C terminal, it is necessary to use a null modem. To design the null modem into the cable, one must switch received data (pin 2) with transmitted data (pin 3) on the RS-232C male connector as shown in the following figure.

To mate to the 2 × 5-pin connector block, the following parts are needed:

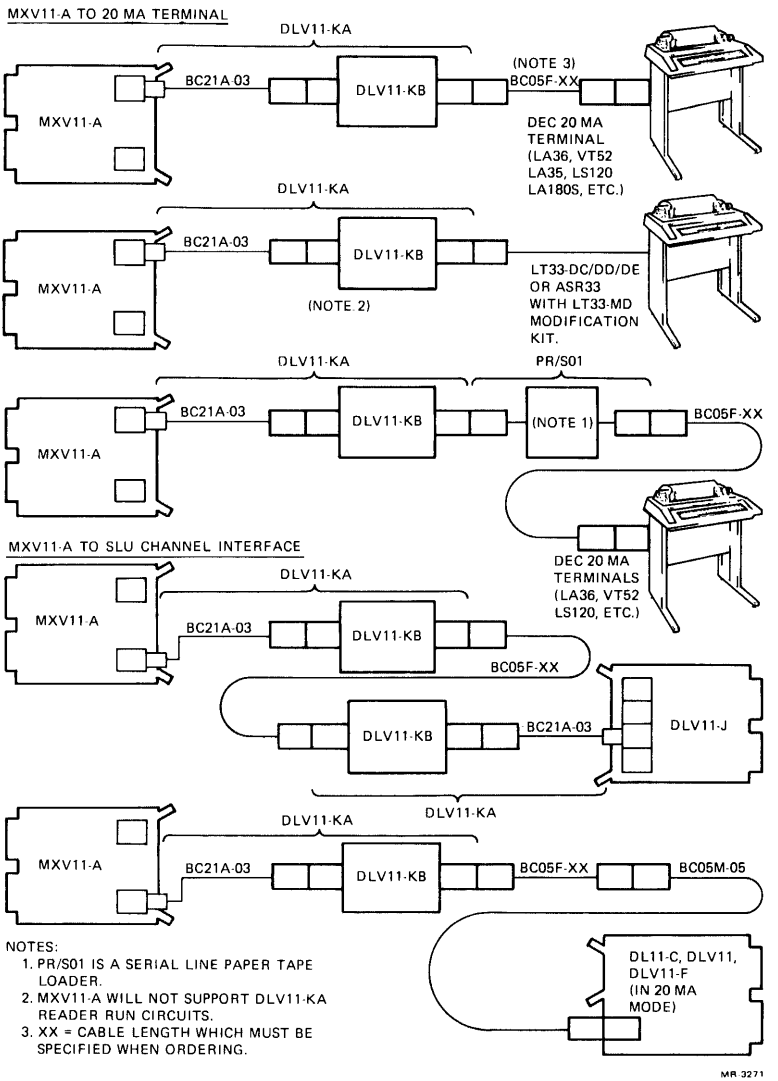
Cable Receptacle (QTY 1)	AMP PN 87133-5 DEC PN 12-14268-02
Locking Clip Contacts (QTY 9)	AMP PN 87124-1 DEC PN 12-14267-00
Key Pin (pin 6) (QTY 1)	AMP PN 87179-1 DEC PN 12-15418-00



B21B-05 Modem Cable



MXV11-A EIA Cable Configurations



NOTES:
1. PR/S01 IS A SERIAL LINE PAPER TAPE LOADER.
2. MXV11-A WILL NOT SUPPORT DLV11-KA READER RUN CIRCUITS.
3. XX = CABLE LENGTH WHICH MUST BE SPECIFIED WHEN ORDERING.

MXV11-A 20 mA Cable Configurations

M8048
MRV11-C READ-ONLY MEMORY (ROM) MODULE

The MRV11-C is a flexible, high-density ROM module used with the LSI-11 bus. The module contains 129 wirewrap pins and 16 24-pin ROM chip sockets that use a variety of user-supplied ROM chips. Masked ROMs, fusible link ROMs and ultraviolet erasable PROMs are acceptable to use. The MRV11-C is shipped without jumpers installed.

Using 4K × 8 ROM chips, the total capacity of one M8048 module can be 64K bytes, accessible either by direct access or window mapping.

Amps		Bus Loads		Cables
+5	+12	AC	DC	None
0.8		2	1	

(plus ROM chip power)

Standard Addresses

Recommended window starting address 760000
Bootstrap starting address: 16-bit system 173000; 18-bit system 773000

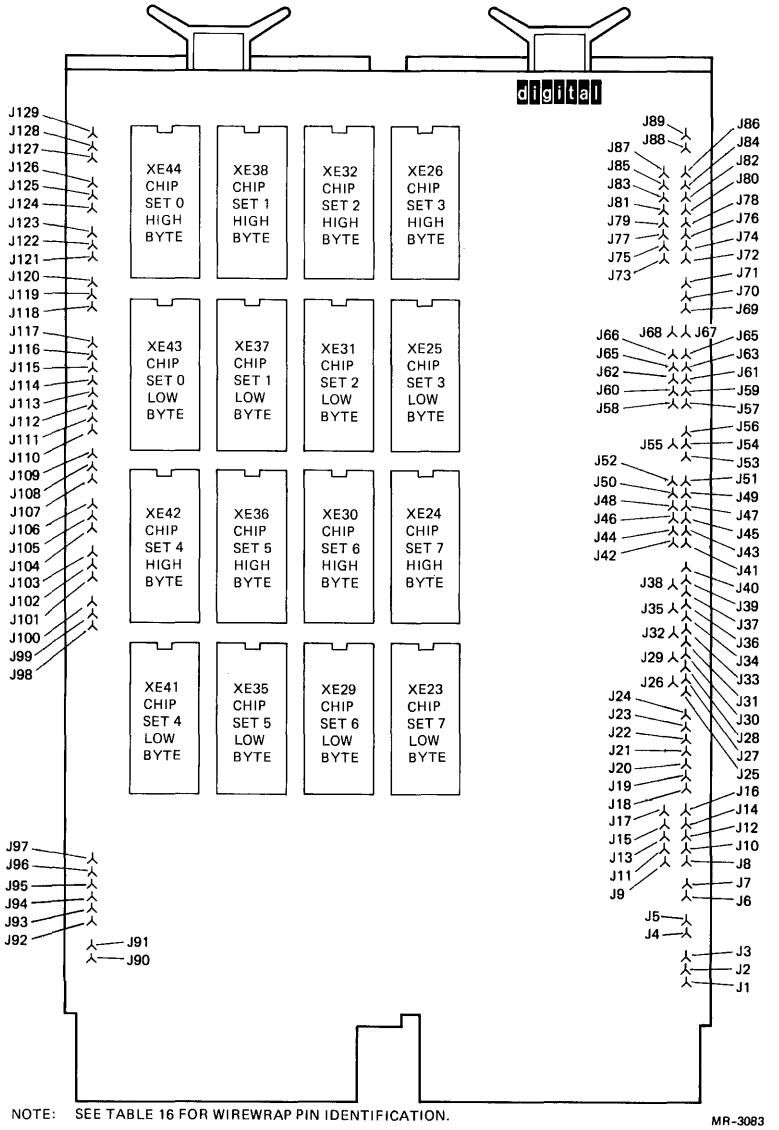
Technical detailed information is beyond the scope of this manual. Additional information can be found in the *Microcomputer Processor Handbook*, EB-18451-20.

Compatible UV PROMs (Ultraviolet)

UV PROMs	Chip Array Size	Maximum Memory Size
Intel 2758	1K × 8	16K bytes
Intel 2716	2K × 8	32K bytes
Intel 2732	4K × 8	64K bytes
Mostek MK2716	2K × 8	32K bytes
T.I. TMS 2516	2K × 8	32K bytes
T.I. TMS 2532	4K × 8	64K bytes

Compatible PROMs

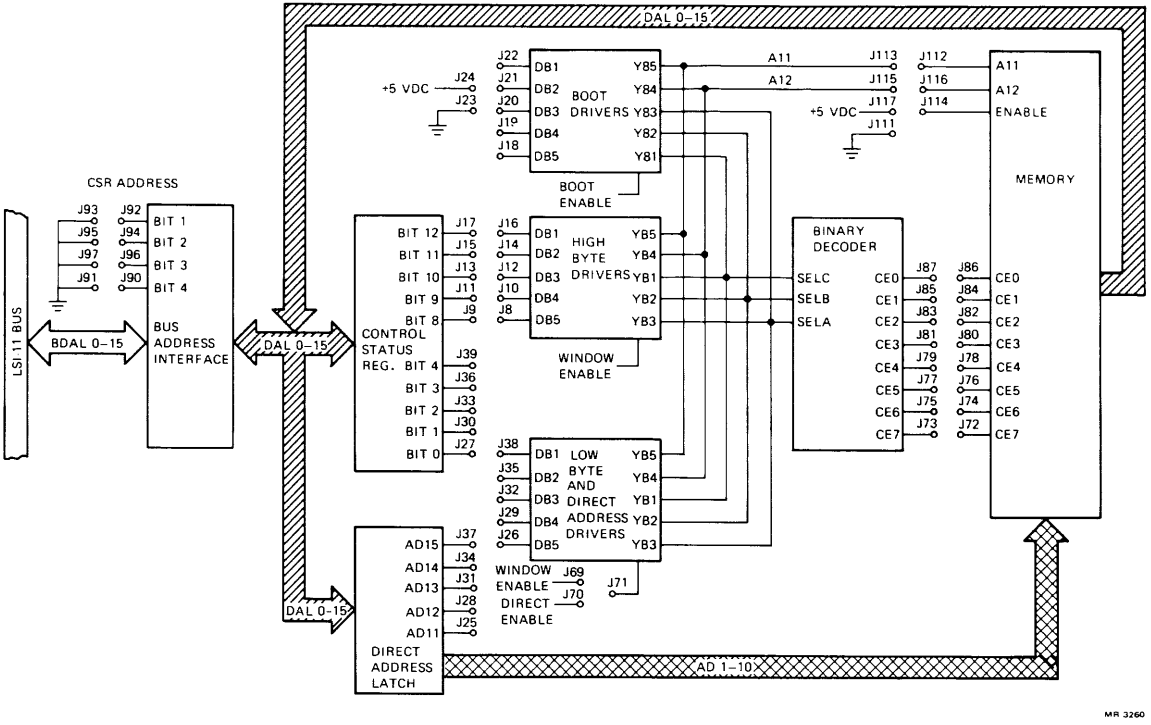
PROM	Chip Array Size	Maximum Memory Size
Intel 3628	1K × 8	16K bytes
Signetics 82S 2708	1K × 8	16K bytes
Signetics 82S 181	1K × 8	16K bytes
Signetics 82S 191	2K × 8	32K bytes



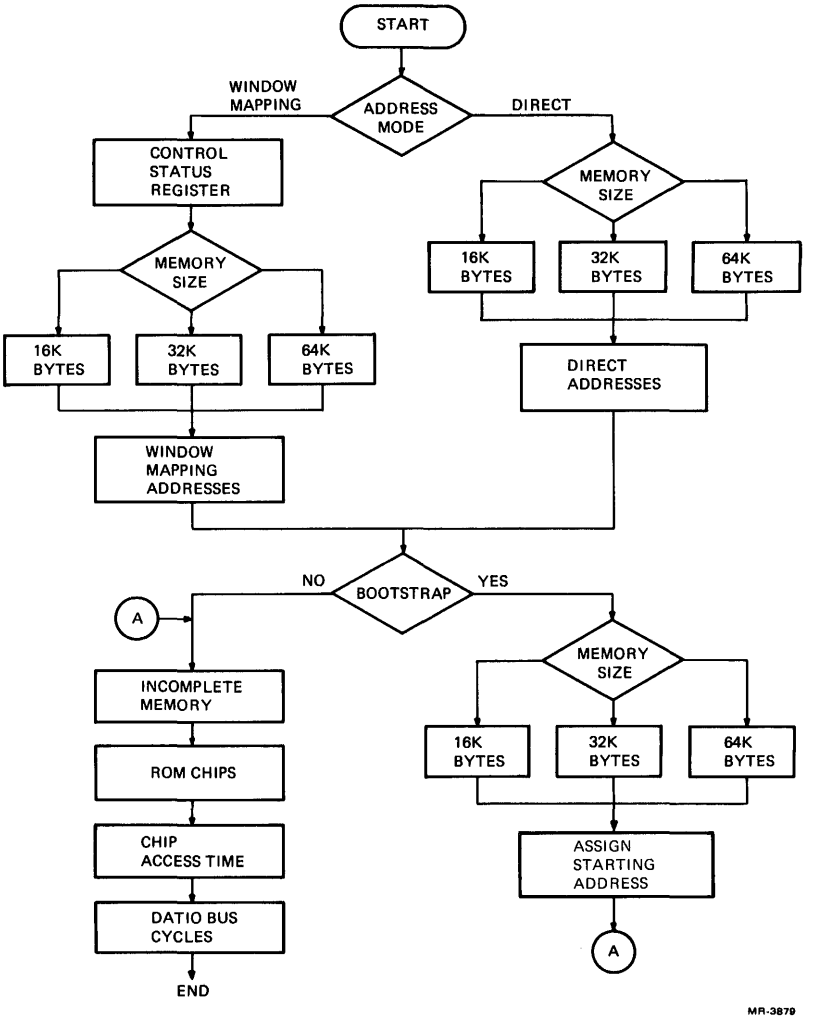
NOTE: SEE TABLE 16 FOR WIREWRAP PIN IDENTIFICATION.

MR-3083

MRV11-C Wirewrap Pin Locations



MRV11-C Configuration Interconnections



Configuration Procedure

Wirewrap Pin Identification

Wirewrap Pin Designation	Function
J1	RXCX pull-up resistor
J2	RXCX optional capacitor
J3	RXCX signal
J4	LMATCH input for BDOUT control
J5	LMATCH for BDOUT control
J6	Window address enable ground
J7	Window address enable
J8	High byte chip enable bit A11
J9	CSR high byte bit 8 chip enable output
J10	High byte chip enable bit A12
J11	CSR high byte bit 9 chip enable output
J12	High byte chip enable least significant bit
J13	CSR high byte bit 10 chip enable output
J14	High byte chip enable intermediate bit
J15	CSR high byte bit 11 chip enable output
J16	High byte chip enable most significant bit
J17	CSR high byte bit 12 chip enable output
J18	Boot address chip enable bit A11
J19	Boot address chip enable bit A12
J20	Boot address chip enable least significant bit
J21	Boot address chip enable intermediate bit
J22	Boot address chip enable most significant bit
J23	Boot address chip enable ground reference
J24	Boot address chip enable 5 V reference
J25	Direct address bit 11 chip enable output
J26	Low byte chip enable A11 bit
J27	CSR low byte bit 0 chip enable output
J28	Direct address bit 12 chip enable output
J29	Low byte chip enable A12 bit
J30	CSR low byte bit 1 chip enable output
J31	Direct address bit 13 chip enable output
J32	Low byte chip enable least significant bit
J33	CSR low byte bit 2 chip enable output
J34	Direct address bit 14 chip enable output
J35	Low byte chip enable intermediate bit
J36	CSR low byte bit 3 chip enable output
J37	Direct address bit 15 chip enable output
J38	Low byte chip enable most significant bit
J39	CSR low byte bit 4 chip enable output
J40	Reserved for future DIGITAL use.
J41	Window address bit 15 compare ground
J42	Window address bit 13 compare input
J43	Window address bit 12 compare ground

Wirewrap Pin Identification (Cont)

Wirewrap Pin Designation	Function
J44	Window address bit 14 compare input
J45	Window address bit 14 compare ground
J46	Window address bit 15 compare input
J47	Window address bit 16 compare ground
J48	Window address bit 16 compare input
J49	Window address bit 13 compare ground
J50	Window address bit 17 compare input
J51	Window address bit 17 compare ground
J52	Window address bit 12 compare input
J53	Direct address 32K memory limit output
J54	Direct address 16K memory limit output
J55	Direct address memory limit input
J56	Direct address 8K memory limit output
J57	Direct address bit 17 compare ground
J58	Direct address bit 16 compare input
J59	Direct address bit 16 compare ground
J60	Direct address bit 17 compare input
J61	Direct address bit 15 compare ground
J62	Direct address bit 15 compare input
J63	Direct address bit 14 compare ground
J64	Direct address bit 14 compare input
J65	Direct address bit 13 compare ground
J66	Direct address bit 13 compare input
J67	CSR high byte bit 15 enable ground
J68	CSR high byte bit 15 enable input
J69	High byte chip enable window address function
J70	High byte chip enable direct address function
J71	High byte chip enable function select drivers
J72	Bit 7 chip select enable input
J73	Bit 7 chip enable decoder output
J74	Bit 6 chip select enable input
J75	Bit 6 chip enable decoder output
J76	Bit 5 chip select enable input
J77	Bit 5 chip enable decoder output
J78	Bit 4 chip select enable input
J79	Bit 4 chip enable decoder output
J80	Bit 3 chip select enable input
J81	Bit 3 chip enable decoder output
J82	Bit 2 chip select enable input
J83	Bit 2 chip enable decoder output
J84	Bit 1 chip select enable input
J85	Bit 1 chip enable decoder output
J86	Bit 0 chip select enable input

Wirewrap Pin Identification (Cont)

Wirewrap Pin Designation	Function
J87	Bit 0 chip enable decoder output
J88	Boot address enable ground
J89	Boot address enable
J90	DAL 4 CSR address select signal
J91	DAL 4 CSR address select ground
J92	DAL 1 CSR address select signal
J93	DAL 1 CSR address select ground
J94	DAL 2 CSR address select signal
J95	DAL 2 CSR address select ground
J96	DAL 3 CSR address select signal
J97	DAL 3 CSR address select ground
J98	Pin 18 input for chip set 5
J99	Chip wirewrap interconnection for chip set 5
J100	Pin 20 input for chip set 5 (chip enable 5)
J101	Pin 18 input for chip set 4
J102	Chip wirewrap interconnection for chip set 4
J103	Pin 20 input for chip set 4 (chip enable 4)
J104	Pin 18 input for chip set 6
J105	Chip wirewrap interconnection for chip set 6
J106	Pin 20 input for chip set 6 (chip enable 6)
J107	Pin 18 input for chip set 7
J108	Chip wirewrap interconnection for chip set 7
J109	Pin 20 input for chip set 7 (chip enable 7)
J110	Reserved for future DIGITAL use.
J111	ROM interconnection, ground reference
J112	Chip enable bit bus input
J113	Address bit A11, used as chip input A10
J114	Chip interconnection loop (to wirewrap pins)
J115	Address bit A12, used as chip input A11
J116	Chip interconnection loop for chip pin 21
J117	ROM interconnection +5 Vdc voltage reference
J118	Pin 18 input for chip set 0
J119	Chip wirewrap interconnection for chip set 0
J120	Pin 20 input for chip set 0 (chip enable 0)
J121	Pin 18 input for chip set 1
J122	Chip wirewrap interconnection for chip set 1
J123	Pin 20 input for chip set 1 (chip enable 1)
J124	Pin 18 input for chip set 2
J125	Chip wirewrap interconnection for chip set 2
J126	Pin 20 input for chip set 2 (chip enable 2)
J127	Pin 18 input for chip set 3
J128	Chip wirewrap interconnection for chip set 3
J129	Pin 20 input for chip set 3 (chip enable 3)

Control and Status Register

Each MRV11-C board uses one 16-bit control and status register located in the system I/O page to determine mapping of ROM segments into windows in the window mapped mode. The default address for this CSR is 177000 (777000 in the PDP-11/23 system). The valid address range for CSRs is 177000 to 177036 (777000 to 777036 on PDP-11/23s).

The CSR contains a 5-bit read/write field for each window. The number stored in this field (0 to 31_{10}) selects the desired 2Kb region from the MRV11-C board to be associated with the window in question. CSR bits 0 through 4 control the mapping of the low address window, window 0. The low five bits of the upper byte (bits 8 through 12) control the mapping of window 1.

The MRV11-C optionally provides a window enable/disable capability. When this option is selected, bit 15 of the CSR is used to enable or disable window response under program control. When bit 15 is a 0, the board will respond to references to the CSR or DATI or DATIO references to either of the windows. When bit 15 is a 1, only the CSR will respond. If the enable/disable option is not selected, bit 15 of the CSR will be read only and will always be 0. The enable/disable bit has no effect on direct mode addressing or the bootstrap window capability. If enable/disable option is used, bit 15 on system initializes, disabling the board.

Control and Status Register Addresses

CSR Address	Bit 4 J90 to J91	Bit 3 J96 to J97	Bit 2 J94 to J95	Bit 1 J92 to J93
177000*	R	R	R	R
177002	R	R	R	I
177004	R	R	I	R
177006	R	R	I	I
177010	R	I	R	R
177012	R	I	R	I
177014	R	I	I	R
177016	R	I	I	I
177020	I	R	R	R
177022	I	R	R	I
177024	I	R	I	R
177026	I	R	I	I
177030	I	I	R	R
177032	I	I	R	I
177034	I	I	I	R
177036	I	I	I	I

R = jumper removed. I = jumper installed.

*Default address

NOTE

Install J67 to J68 to allow the use of bit 15 of the CSR.

MRV11-C Direct Addressing Starting Address

Starting Address	Bank	Bit 17 57 to 60	Bit 16 59 to 58	Bit 15 61 to 62	Bit 14 63 to 64	Bit 13 65 to 66
0	0	I	I	I	I	I
20000	1	I	I	I	I	R
40000	2	I	I	I	R	I
60000	3	I	I	I	R	R
100000	4	I	I	R	I	I
120000	5	I	I	R	I	R
140000	6	I	I	R	R	I
160000	7	I	I	R	R	R
200000	10	I	R	I	I	I
220000	11	I	R	I	I	R
240000	12	I	R	I	R	I
260000	13	I	R	I	R	R
300000	14	I	R	R	I	I
320000	15	I	R	R	I	R
340000	16	I	R	R	R	I
360000	17	I	R	R	R	R
400000	20	R	I	I	I	I
420000	21	R	I	I	I	R
440000	22	R	I	I	R	I
460000	23	R	I	I	R	R
500000	24	R	I	R	I	I
520000	25	R	I	R	I	R
540000	26	R	I	R	R	I
560000	27	R	I	R	R	R
600000	30	R	R	I	I	I
620000	31	R	R	I	I	R
640000	32	R	R	I	R	I
660000	33	R	R	I	R	R
700000	34	R	R	R	I	I
720000	35	R	R	R	I	R
740000	36	R	R	R	R	I
760000	37	R	R	R	R	R

R = jumper removed.
I = jumper installed.

Using Multiple Boards

Up to 16 MRV11-C boards may be configured in a single system. When multiple boards are present, each board has a unique control and status register address assigned in increasing order from 177000 (777000 in PDP-11/23 systems). Each board can have a unique 4Kb area of the physical address space set aside for its windows, but it is also possible to share one 4Kb area of the address space among all MRV11-C boards installed in the system. This is done by using the enable/disable capability discussed earlier. When enable/disable is implemented, the disable bit in the CSR will be set automatically by BINIT on the bus or by execution of the RESET instruction. Therefore, the initial state of the system will have all boards disabled. To access a particular segment of ROM in this multiboard configuration, the programmer first enables the desired board and maps the segment. When access to that segment is completed, the board is again disabled to allow another board to be selected some other time.

Chip Enable Jumpers

Sockets Enabled	Chip Enable Signal	Wirewrap Jumpered Pins
XE43, XE44	CE0	J86 to J87
XE37, XE38	CE1	J84 to J85
XE31, XE32	CE2	J82 to J83
XE25, XE26	CE3	J80 to J81
XE41, XE42	CE4	J78 to J79
XE35, XE36	CE5	J76 to J77
XE29, XE30	CE6	J74 to J75
XE23, XE24	CE7	J72 to J73

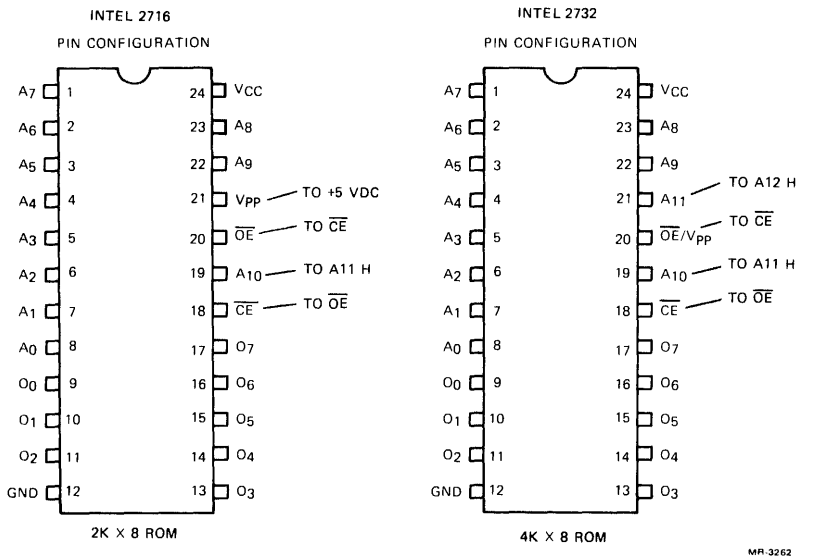
NOTE
J40 and J110 are unused at this time.

ROM Chips

The ROM is provided by the user and consists of up to 16 chips that are inserted into prewired sockets. The chips will be either 1K × 8 bit, 2K × 8 bit, or 4K × 8 bit ROMs. When the MRV11-C is fully populated, the result will be either 16K, 32K, or 64K bytes of memory. These ROMs can be supplied by a variety of vendors and the basic configuration for many of the ROMs is standardized except for pins 18, 19, 20, and 21. The configuration of these pins will vary depending upon the size of the ROM and the vendor who supplies them. The user should verify the vendor's specifications in order to determine if a particular ROM can be used on the MRV11-C.

The MRV11-C module is configured so that the user can select the signals that are applicable to pins 18, 19, and 21. The board provides wirewrap pins for the user to select the A11, A12, 5 Vdc or ground. There are three individual loops that interconnect all chips and three wirewrap pins available for each individual chip. Wirewrap pin J112 interconnects pin 19 of all the chips and pin J116 interconnects pin 21 of all the chips; these are normally designated as the A10 or A11 inputs to the chips.

Wirewrap pin J114 interconnects wirewrap pins that are individually associated with each chip. Pin 18 of each chip is individually wired to a wirewrap pin and chip pin 20 is wired to the chip enable signal. Chip pin 20 is also individually wired to a wirewrap pin. The user must determine from the vendor's specifications which signals apply to which pins and must install jumper wires as needed to configure an operational module.



MRV11-C ROM Pin Configuration Sample

M8049
DRV11-J GENERAL PURPOSE PARALLEL LINE INTERFACE

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.8A		2	1	BC02D-XX BC08Y-XX BC05W-XX (For loopback half-twist connection)

Standard Addresses

	A	B	C	D
CSR	764160	764164	764170	764174
DBR	764162	764166	764172	764176

Standard Vectors

Software programmable in the range 0000_8–1774_8.

Diagnostic Programs

Refer to Appendix A.

NOTE

Both the XXDP+ diagnostics and the DEC/X11 module require the installation of a BC05W-XX loopback cable.

Related Documentation

DRV11-J Field Maintenance Print Set (MP-00866-00)
DRV11-J User Guide (EK-DRV11J-UG)

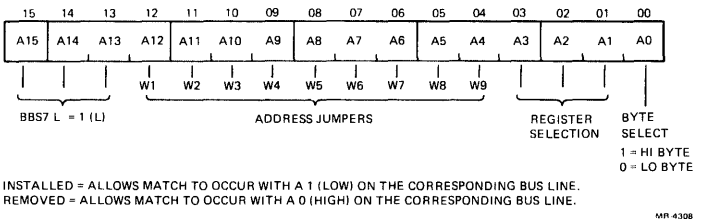
Technical, detailed information is beyond the scope of this manual. Additional information can be found in the *Microcomputer Interfaces Handbook*, EB-20175-20.

Device Address

There are eight device registers on the M8049 module that can be individually addressed by the computer program. These registers are divided into four control status registers (CSR A, B, C, D), and four data buffer registers (DBR A, B, C, and D).

Addresses for the module are selectable from location 760000 octal through 777600 octal address range. When more than one DRV11-J is desired, the module's starting address must be assigned in descending order and separated by 20 octal addresses. Example: the first module will be 760060, the second 760040, and the third, 760020 octal.

Nine address jumpers (W1 through W9) are installed or removed to establish a base device register address. Note that address bits A13 through A15 are neither configured nor decoded by the module. These bits are decoded by the bus master module as the bank 7 select (BBS7L) bus signal. Address bit 0 is used by the program to select a high-byte or low-byte operation. Address bits 1 through 3 are used to select one of the eight device registers in the addressed module.



DRV11-J Device Address Format

DRV11-J Registers

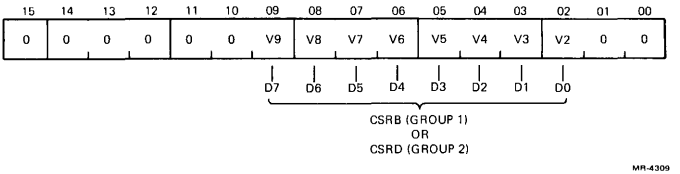
Mnemonic	Description	Address (Octal)*
CSRA	Control Status Register A	7XXXX0
DBRA	Data Buffer Register A	7XXXX2
CSRB	Control Status Register B	7XXXX4
DBRB	Data Buffer Register B	7XXXX6
CSRC	Control Status Register C	7XXX10
DBRC	Data Buffer Register C	7XXX12
CSRD	Control Status Register D	7XXX14
DBRD	Data Buffer Register D	7XXX16

*XXXX is jumper selectable between 60000 and 77760 octal in a modulas of 20 octal.

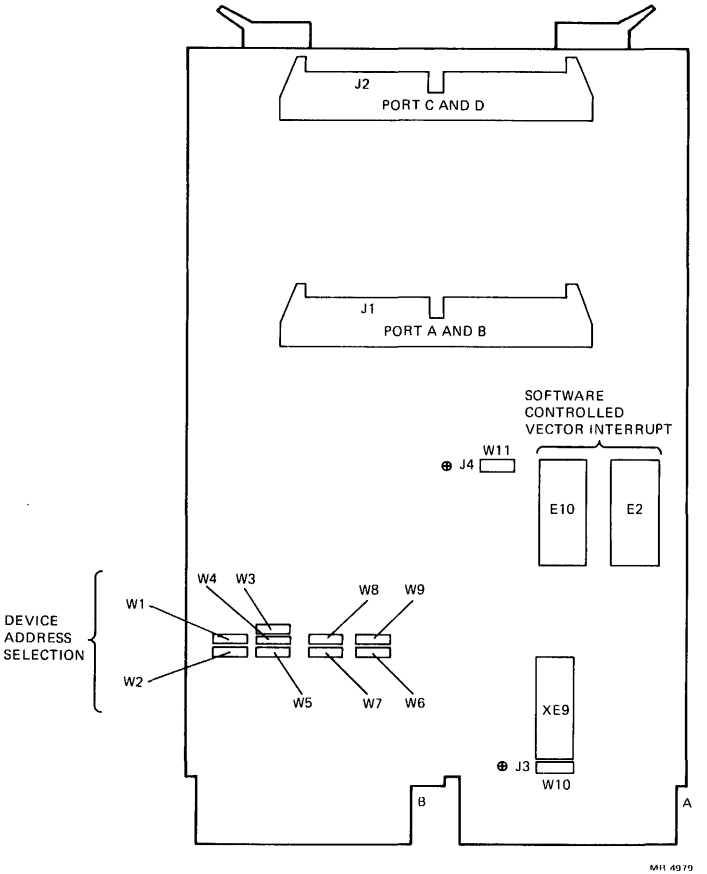
Interrupt Vector Addresses

The DRV11-J may be programmed to operate in systems requiring either vectored interrupts or polled interrupts. If the DRV11-J is used in a system that required vectored interrupts, the interrupt vector addresses must be programmed into a 64 × 8-bit RAM (vector address memory) contained in two interrupt controller chips (E2 and E10). Each interrupt controller chip may store a maximum of 32 interrupt vector addresses. CSRB bits D 07-00 are used in conjunction with CSRA bits 07-00 to program the 32 vector addresses for group 1 interrupt control. CSRD bits 07-00 are used in conjunction with CSRC bits to program the 32 vector addresses for group 2 interrupt control. Note that vector address bits V9 through V2 are programmed by CSRB or CSRD bits D7 through D0, respectively.

A total of 64 vector addresses in the 0000 through 1774 octal range may be stored in the vector address memory. To avoid device conflicts, refer to Appendix A of the *Microcomputer Interfaces Handbook*, EB-20175-20, when assigning vector addresses.



DRV11-J Vector Address Format

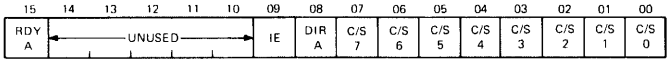


DRV11-J Jumper Locations

DRV11-J Factory Jumper Configuration

Jumper	Function	Jumper State*	Function
W1	A12	R	This arrangement of jumpers W1 through W9 assigns the device address 764160 octal to the first of eight addressable bus registers. With a starting address of 764160 octal, the remaining bus registers are automatically assigned the following contiguous addresses. CSRA 764160 DBRA 764162 CSRB 764164 DBRB 764166 CSRC 764170 DBRC 764172 CSRD 764174 DBRD 764176
W2	A11	I	
W3	A10	R	
W4	A9	R	
W5	A8	R	
W6	A7	R	
W7	A6	I	
W8	A5	I	
W9	A4	I	
W10		I	Reserved for future use.
W11	Group Vector Interrupts	I	DRV11-J monitors group 2 vectored interrupts using port A I/O bits 11-08 and USER RPLY (A through D) signals (default configuration).

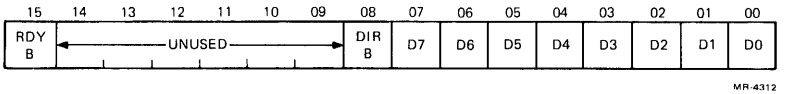
*R = removed = 0.
I = installed = 1.



CSRA Bit Assignments

CSRA Bit Function and Description

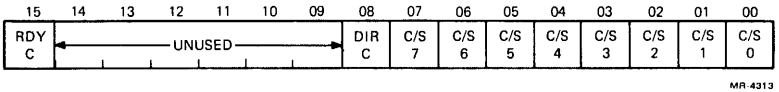
Bit	Function
07-00	C/S7-C/S0 - These bits are used in conjunction with CSRD bits (07-00) to program interrupt control group 1. They contain status information when read, and command words when written. Unaffected by BINIT. Read/write.
08	Direction A (DIR A) - Used for controlling DBRA. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DRV11-J RDY output signal is asserted and the DRV11-J is the input device. When set and the USER RDY signal is asserted, the DRV11-J is the output device. The negation of either DIR or USER RDY will cause the DRV11-J outputs to remain in their high impedance state. Cleared by BINIT. Read/write.
09	Interrupt Enable (IE) - Enables the DRV11-J to generate processor interrupts when set. Used to enable both group 1 and group 2 interrupts. Cleared by BINIT. Read/write.
14-10	Unused. Read as 0s.
15	User Ready A (RDY A) - Used for controlling DBRA. When read, yields the state of the USER RDY signal. A 0 equals negated, and a 1 equals asserted. It is used in conjunction with the DIR bit to enable DRV11-J output operations. The user device asserts this signal when it desires the DRV11-J to output data. Unaffected by BINIT. Read only.



CSRB Bit Assignments

CSRB Bit Function and Description

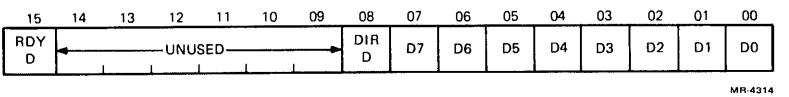
Bit	Function
07-00	D7-DO - These bits are used in conjunction with CSRA bits (07-00) to program interrupt control group 1. They contain information selected by the command word loaded through CSRA. The registers available are the IRR, ISR, ACR, IMR and the vector address memory. Unaffected by BINIT. Read/write.
08	Direction B (DIR B) - Used for controlling DBRB. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DRV11-J RDY output signal is asserted and the DRV11-J is the input device. When set and the USER RDY signal is asserted, the DRV11-J is the output device. The negation of either DIR or USER RDY will cause the DRV11-J outputs to remain in their high impedance state. Cleared by BINIT. Read/write.
14-09	Unused. Read as 0s.
15	User Ready B (RDY B) - Used for controlling DBRB. When read, yields the state of the USER RDY signal. A 0 equals negated, and a 1 equals asserted. It is used in conjunction with the DIR bit to enable DRV11-J output operations. The user device asserts this signal when it desires the DRV11-J to output data. Unaffected by BINIT. Read only.



CSRC Bit Assignments

CSRC Bit Function and Description

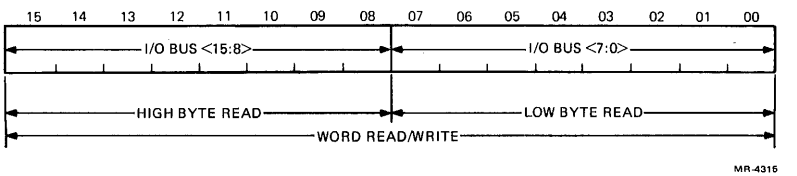
Bit	Function
07-00	C/S7-C/S0 - These bits are used in conjunction with CSRD bits (07-00) to program interrupt control group 2. They contain status information when read and command words when written. Unaffected by BINIT. Read/write.
08	Direction C (DIR C) - Used for controlling DBRC. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DRV11-J RDY output signal is asserted and the DRV11-J is the input device. When set and the USER RDY signal is asserted, the DRV11-J is the output device. The negation of either DIR or USER RDY will cause the DRV11-J outputs to remain in their high impedance state. Cleared by BINIT. Read/write.
14-09	Unused. Read as 0s.
15	User Ready C (RDY C) - Used for controlling DBRC. When read, yields the state of the USER RDY signal. A 0 equals negated, and a 1 equals asserted. It is used in conjunction with the DIR bit to enable DRV11-J output operations. The user device asserts this signal when it desires the DRV11-J to output data. Unaffected by BINIT.



CSRD Bit Assignments

CSRD Bit Functions and Description

Bit	Function
07-00	D7-D0 - These bits are used in conjunction with CSRC bits (07-00) to program interrupt control group 2. They contain information selected by the command word loaded through CSRC. The registers available are the IRR, ISR, ACR, IMR and the vector address memory. Unaffected by BINIT. Read/write.
08	Direction D (DIR D) - Used for controlling DBRD. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DRV11-J RDY output signal is asserted and the DRV11-J is the input device. When set and the USER RDY signal is asserted, the DRV11-J is the output device. The negation of either DIR or USER RDY will cause the DRV11-J outputs to remain in their high impedance state. Cleared by BINIT. Read/write.
14-09	Unused. Read as 0s.
15	User Ready D (RDY D) - Used for controlling DBRD. When read, yields the state of the USER RDY signal. A 0 equals negated, and a 1 equals asserted. It is used in conjunction with the DIR bit to enable DRV11-J output operations. The user device asserts this signal when it desires the DRV11-J to output data. Unaffected by BINIT. Read only.



Data Buffer Register Bit Assignment

Data Buffer Registers

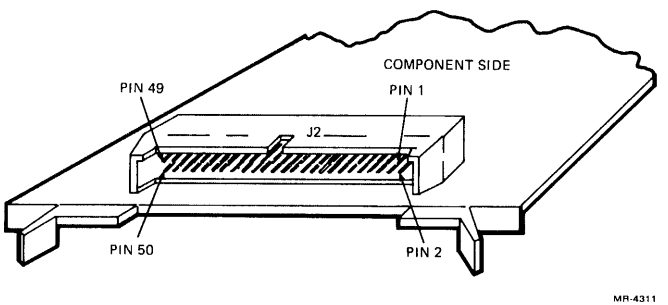
The data buffer registers (DBRA, DBRB, DBRC, and DBRD) are 16-bit word-addressable registers that contain output data when written and input data when read. In an output mode, reading the input register will yield the output buffer contents. The output buffers DBRA through DBRD are not cleared by initialize. The bit assignment is the same for all four registers.

Programmed Data Transfer

Input and output data transfers may be performed under program control by addressing the data buffer registers (DBRA, B, C, or D) and then reading or writing the data. Data is transferred on a 16-bit word-by-word basis by reading or writing the appropriate data buffer.

Interfacing to User's Device

Two board-mounted 50-pin male connectors (J1 and J2) interface the DRV11-J to the user device. Connector J1 is used to interface the port A and port B signals, while J2 is used for the port C and port D signals. Location of the connector pins is shown below with the interface signal names and their respective connector pins listed in the table that follows.



DRV11-J I/O Connector Pin Locations

I/O Connector Pin Functions

Signal Name	J1 Connector Pin	Signal Name	J2 Connector Pin
DRV11-J RDY A	J1-29	DRV11-J RDY D	J2-29
DRV11-J RPLY A	J1-33	DRV11-J RPLY D	J2-33
USER RDY A	J1-31	USER RDY D	J2-31
USER RPLY A	J1-27	USER RPLY D	J2-27
A I/O 15	J1-45	D I/O 15	J2-45
A I/O 14	J1-46	D I/O 14	J2-46
A I/O 13	J1-43	D I/O 13	J2-43
A I/O 12	J1-49	D I/O 12	J2-49
A I/O 11	J1-48	D I/O 11	J2-48
A I/O 10	J1-44	D I/O 10	J2-44

I/O Connector Pin Functions (Cont)

Signal Name	J1 Connector Pin	Signal Name	J2 Connector Pin
A I/O 9	J1-50	D I/O 9	J2-50
A I/O 8	J1-47	D I/O 8	J2-47
A I/O 7	J1-41	D I/O 7	J2-41
A I/O 6	J1-36	D I/O 6	J2-36
A I/O 5	J1-42	D I/O 5	J2-42
A I/O 4	J1-35	D I/O 4	J2-35
A I/O 3	J1-40	D I/O 3	J2-40
A I/O 2	J1-38	D I/O 2	J2-38
A I/O 1	J1-39	D I/O 1	J2-39
A I/O 0	J1-37	D I/O 0	J2-37
GND	J1-26	GND	J2-26
GND	J1-28	GND	J2-28
GND	J1-30	GND	J2-30
GND	J1-32	GND	J2-32
GND	J1-34	GND	J2-34
DRV11-J RDY B	J1-20	DRV11-J RDY C	J2-20
DRV11-J RPLY B	J1-24	DRV11-J RPLY C	J2-24
USER RDY B	J1-22	USER RDY C	J2-22
USER RPLY B	J1-18	USER RPLY C	J2-18
B I/O 15	J1-6	C I/O 15	J2-6
B I/O 14	J1-5	C I/O 14	J2-5
B I/O 13	J1-8	C I/O 13	J2-8
B I/O 12	J1-2	C I/O 12	J2-2
B I/O 11	J1-3	C I/O 11	J2-3
B I/O 10	J1-7	C I/O 10	J2-7
B I/O 9	J1-1	C I/O 9	J2-1
B I/O 8	J1-4	C I/O 8	J2-4
B I/O 7	J1-10	C I/O 7	J2-10
B I/O 6	J1-15	C I/O 6	J2-15
B I/O 5	J1-9	C I/O 5	J2-9
B I/O 4	J1-16	C I/O 4	J2-16
B I/O 3	J1-11	C I/O 3	J2-11
B I/O 2	J1-13	C I/O 2	J2-13
B I/O 1	J1-12	C I/O 1	J2-12
B I/O 0	J1-14	C I/O 0	J2-14
GND	J1-17	GND	J2-17
GND	J1-19	GND	J2-19
GND	J1-21	GND	J2-21
GND	J1-23	GND	J2-23
GND	J1-25	GND	J2-25

I/O Signal Functions

Signal Name*	Function
DRV11J RDY [X]	This signal is asserted by the DRV11-J to inform the user that data may be placed on the I/O bus associated with the signal. It is asserted when the corresponding DIR bit is cleared.
DRV11J RPLY [X]	This signal is asserted when the DRV11-J has accepted data (DRV11-J is the input device) by reading the corresponding data buffer with the associated DIR bit cleared, or when data is available for the user device (DRV11-J is the output device) by writing the corresponding data buffer with the associated DIR bit set.
[X] I/O <15:00>	These are the 16 three-state data buffer inputs and outputs.
USER RDY [X]	This signal is asserted by the user device to inform the DRV11-J that it requires input data (DRV11-J is the output device) and, in conjunction with the associated DIR bit, enables the DRV11-J three-state outputs.
USER RPLY [X]	This signal is asserted by the user device when data is accepted (DRV11-J is the output device) or when data is available (DRV11-J is the input device).

* [X] equals either A, B, C, or D.

Cables

The three types of cable used to connect the DRV11-J to a user device are described below.

Cable Description

Cable Type*	Description	Max. Length**
BC02D-XX	Flat, 50 wires, shielded connectors (DEC PN 12-11664) on both ends	1.83 m (6 ft)
BC08Y-XX	Round, 50-pin Berg to 50-pin Berg, 50 wires	1.83 m (6 ft)
BC05W-XX	Flat, 50 wires, shielded connectors (DEC PN 12-11664) on both ends	7.6 m (25 ft)

I/O Signal Specifications

All data buffer signals (I/O <15:00>) at the connectors (J1 and J2) are defined as being asserted (1) high (+3 V) and negated (0) low (GND). All protocol signals (DRV11-J RDY, DRV11-J RPLY, USER RDY and USER RPLY) at the connectors are defined as being asserted (1) low (GND) and negated (0) high (+3 V).

I/O Signal Loopback Connections

The DRV11-J signal pin assignments are arranged to permit loopback operation when a BC05W-XX cable is installed with a half-twist connecting J1-1 to J2-50. With the cable installed in this manner, the proper connections are made to loopback the DRV11-J protocol signals.

---

* -XX in the cable denotes length in feet. For example, a 1.83 m (6 ft) BC02D cable would be ordered as BC02D-06.

** Maximum cable length is specified as being from DRV11-J to DRV11-J.

DRV11-J Loopback Signal Connections

J1 Pin No.		Signal	Signal	J2 Pin No.	
Port B	1	B I/O 9	⟷ D I/O 9	50	Port D
	2	B I/O 12	⟷ D I/O 12	49	
	3	B I/O 11	⟷ D I/O 11	48	
	4	B I/O 8	⟷ D I/O 8	47	
	5	B I/O 14	⟷ D I/O 14	46	
	6	B I/O 15	⟷ D I/O 15	45	
	7	B I/O 10	⟷ D I/O 10	44	
	8	B I/O 13	⟷ D I/O 13	43	
	9	B I/O 5	⟷ D I/O 5	42	
	10	B I/O 7	⟷ D I/O 7	41	
	11	B I/O 3	⟷ D I/O 3	40	
	12	B I/O 1	⟷ D I/O 1	39	
	13	B I/O 2	⟷ D I/O 2	38	
	14	B I/O 0	⟷ D I/O 0	37	
	15	B I/O 6	⟷ D I/O 6	36	
	16	B I/O 4	⟷ D I/O 4	35	
	18	USER RPLY B	← DRV11-J RPLY D	33	
	20	DRV11-J RDY B	→ USER RDY D	31	
	22	USER RDY B	← DRV11-J RDY D	29	
	24	DRV11-J RPLY B	→ USER RPLY D	27	
	27	USER RPLY A	← DRV11-J RPLY C	24	
	29	DRV11-J RDY A	→ USER RDY C	22	
	31	USER RDY A	← DRV11-J RDY C	20	
	33	DRV11-J RPLY A	→ USER RPLY C	18	
	35	A I/O 4	⟷ C I/O 4	16	
	36	A I/O 6	⟷ C I/O 6	15	
	37	A I/O 0	⟷ C I/O 0	14	
	38	A I/O 2	⟷ C I/O 2	13	
Port A	39	A I/O 1	⟷ C I/O 1	12	Port C
	40	A I/O 3	⟷ C I/O 3	11	
	41	A I/O 7	⟷ C I/O 7	10	
	42	A I/O 5	⟷ C I/O 5	9	
	43	A I/O 13	⟷ C I/O 13	8	
	44	A I/O 10	⟷ C I/O 10	7	
	45	A I/O 15	⟷ C I/O 15	6	
	46	A I/O 14	⟷ C I/O 14	5	
	47	A I/O 8	⟷ C I/O 8	4	
	48	A I/O 11	⟷ C I/O 11	3	
	49	A I/O 12	⟷ C I/O 12	2	
	50	A I/O 9	⟷ C I/O 9	1	

Connector pins 17, 19, 21, 23, 25, 26, 28, 30, 32, 34 on J1 and J2 are grounds.

M8186
KDF11-AX 11/23 MICROCOMPUTER

The KDF11-A is a 16-bit, double-height, multilayered, microcomputer module. The processor (microcomputer) uses the existing LSI-11 bus. The KDF11 is backward-compatible with existing LSI-11/2 processors and I/O interfaces. Memory management is included as a standard feature.

The KEF11-A option (not part of a standard system) is a floating point microcode extension chip that mounts to a socket on the KDF11-A processor module. This chip option can execute the PDP-11/34 (FP11) floating point instruction set. These instructions supplement the integer arithmetic instructions (for example, MUL, DIV) in the basic instruction set.

Four 40-pin chip sockets mounted on the KDF11-A module are to accommodate the following chip functions.

- Memory Management Unit (MMU)
- Spare
- Floating point (optional)
- Data/control unit (the basic processor)

KDF11 Specifications

Identification:	M8186
Size:	Double-height module
Power Requirements:	+5 V ± 5% 2.0 A +12 V ± 5% 0.2 A
Bus Loads:	AC 2 unit loads DC 1 unit load
Environmental:	DEC STD 102 Class C

Diagnostic Programs
The following diagnostic programs are used with the LSI-11/23 processor, except for the limitations noted.

JKDBBO CPU trap and EIS diagnostics

JKDABO Memory Management Unit (MMU)

Requires KTF11-A option (21-15542-00/01) installed in IC socket E57.

JKDCAO Floating point diagnostic - Part 1

JKDDAO Floating point diagnostic - Part 2

The floating tests require the KEF 11 option to be installed on the board. These diagnostics expect the CPU to be fault free. Therefore, the JKDB?? diagnostic should be run before the floating point diagnostics.

NOTE
See Appendix A for multimedia assignments.

Related Documentation
Microcomputer Processor Handbook (EB-18451-20)
KDF11-A Field Maintenance Print Set (MP-00734-00)
LSI-11, PDP-11/23 Reference Card (EH-17898-20)

KEF11-A (Floating Point Option Installation)
The KEF-11AA floating point option resides in two MOS/LSI chips contained on one 40-pin hybrid package (57-00001-01). The KEF11-AA requires the memory management chip to be present along with the base MOS/LSI chips, since all of the floating point accumulators and status registers are in the MMU chip. Chapter 10 in the *Microcomputer Processor Handbook*, EB-18451-20 covers the KEF11 in detail.

Early revision M8186s require an ECO (M8186-S-0007) to accommodate the KEF11-AA option. Modules at hardware revision A5 (A etch) or C1 (C etch) and below, require this change.

Remove E57 (DEC PN 21-15542-00)
Install E57 (DEC PN 21-15542-01)
Remove E31 (DEC PN 57-00000-00)
Install E21 (DEC PN 57-00000-01)

NOTE
Mark Rev A6 or C2 on the module handle to indicate the new revision, depending on original etch rev.

After the ECO is installed, install the KEF11-AA option (57-00001-01) in IC socket position E39.

KDF11 Variations

AA -LSI-11/23 16-bit microcomputer with KTF11-AA memory management (M8186)

AB -KDF11-AA with KEF11-AA (floating point option)

AC -KDF11-AA without KTF11-A

GD -KDF11-AC with MXV11-AC and MSV11-CD (32K words)

HD -KDF11-AC with MSV11-DD (32K words)

HF -KDF11-AA with two MSV11-DD (64K words)

HH -KDF11-AA with three MSV11-DD (96K words)

HK -KDF11-AA with four MSV11-AA (128K words)

RE -KDF11-AA with MXV11-AC, MSV11-DD (48K words) and QJV13-DZ (RT2 V 4.0, license only)

RE -KDF11-AA with MXV11-AC, two MSV11-DD (80K words) and QJV13-DZ

RJ -KDF11-AA with MXV11-AC, three MSV11-DD (112K words) and QJV13-DZ

SE -KDF11-AA with MXV11-AC, MSV11-DD (48K words) and QJ642-DZ (RSX11-S V 2.2, license only)

SG -KDF11-AA with MXV11-AC, two MSV11-DD (80K words) and QJ642-DZ

SJ -KDF11-AA with MXV11-AC, three MSV11-DD (112K words) and QJ642-DZ

XA -KDF11-AA with two MSV11-ED (64K word) (parity)

XB -KDF11-AA with four MSV11-ED (128K word) (parity)

Data/Control (DC302, DC303) Hybrid

The data chip (DC302) contains the PDP-11 general registers, the processor status word (PS), several working registers, the arithmetic and logic unit (ALU), and conditional branching logic. The DC302 chip:

- performs all arithmetic and logical functions
- handles all data and address transfers with the LSI-11 bus (except relocation, which is handled by the MMU)
- generates most of the signals used for interchip communication and external system control.

Control Chip

The control chip (DC303) contains the microprogram sequence logic and 552 words of microprogram storage in programmable logic arrays (PLA) and read-only memory (ROM) arrays. The control chip accesses the appropriate microinstruction in the PLA or ROM and sends it along the MIB to the data and MMU chips for execution. The control chip accesses only its local storage.

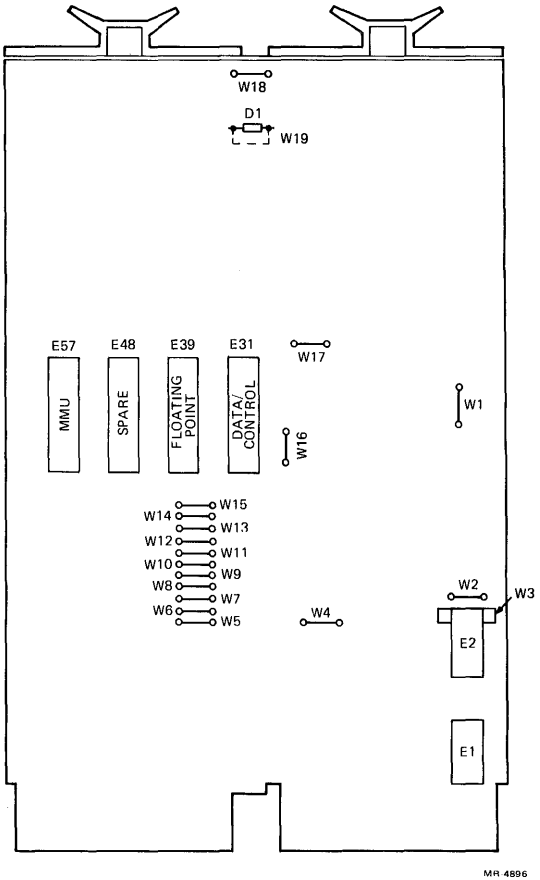
MMU Chip

The MMU chip serves two purposes.

- It provides the memory management function.
- It provides storage for the KEF11-AA floating point accumulators and status registers.

This chip provides user and kernel mode address relocation of 18 bits. Sixteen-bit virtual addresses are relocated via mapping registers (PARs) to the appropriate 18-bit physical address for the transmission to the external system bus.

The MMU chip is controlled by information received on the microinstruction bus (MIB) from both the data chip and the control chip and by several discrete control inputs. The KDF11-AA can operate without the MMU chip; however, the memory would be limited to 32K words and the floating point registers would not be available.



KDF11-AA Rev A Jumpers

M8186 (Etch Rev A) Jumper Configurations

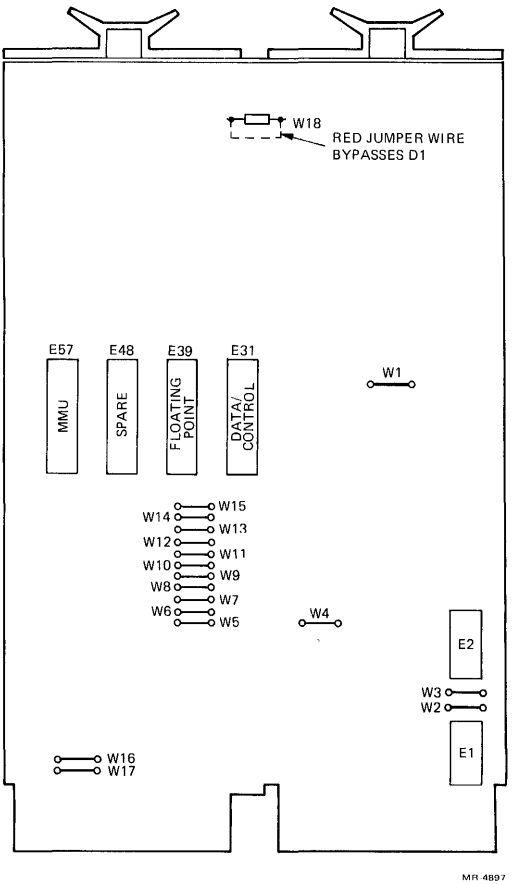
Jumper	Name	Function	Factory Set
W1	Master clock	In - enabled	In
W2	Reserved for DEC use	Removed - do not install	Out
W3	Reserved for DEC use	Installed - do not remove	In
W4	Event line enabled	Out - enabled	In
W5, W6	Power-up mode	(*See footnote.)	W5 - In W6 - Out
W7	Halt/trap option	In - traps to 10_8 on HALT Out - enters console ODT on HALT	In
W8	Bootstrap address	In - powers up to bootstrap address 173000_8 Out - powers up to address specified by W9-W15	In
W9-W15	User-selectable bootstrap address	W9-W15 correspond to address bits 9 through 15, respectively, in mode 2 In = logic 1 Out = logic 0	W9-W15-In

* **Power-Up Mode Selection**

Mode	Name	W5	W6
0	PC @ 24	Out	Out
1	Console ODT	In	Out
2	Bootstrap	Out	In
3	Extended microcode	In	In

M8186 (Etch Rev A) Jumper Configurations (Cont)

Jumper	Name	Function	Factory Set
W16	Reserved for DEC use	Factory-installed; do not remove.	In
W17	Reserved for DEC use	Factory-installed; do not remove.	In
W18	Reserved for DEC use	Factory-installed; do not remove.	In



KDF11-A Rev C Jumpers

M8186 (Etch Rev C) Jumper Configurations

Jumper	Name	Function	Factory Set
W1	Master clock	In - Enabled	In
W2	Reserved for DEC use	Removed - do not install	Out*
W3	Reserved for DEC use	Installed - do not remove	In*
W4	Event line enabled	Out - enabled	In
W5, W6	Power-up mode	(**See footnote.)	W5 - In W6 - Out
W7	Halt/trap option	In - traps to 10_8 on HALT Out - enters console ODT on HALT	Out
W8	Bootstrap address	In - powers up to 173000_8 Out - powers up to address specified by W9-W15	In
W9-W15	User-selectable bootstrap address	W9-W15 correspond to address bits 9 through 15, respectively In = logic 1 Out = logic 0	W9-W15-In

*Refer to FCO M8186-R0009

** Mode	Name	W5	W6
0	PC @ 24 PS @ 26	Out	Out
1	Console ODT	In	Out
2	Bootstrap	Out	In
3	Extended microcode	In	In

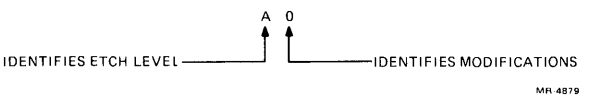
M8186 (Etch Rev C) Jumper Configurations (Cont)

Jumper	Name	Function	Factory Set
W16, W17	Reserved for DEC use	Factory-installed; do not remove.	W16, W17-In
W18	Wake-up circuit	Out = disabled In = enabled	In

Hardware Revision System

As other modules have the etch revision level coded into the etch and the circuit schematic revision level coded on the module handle, the M8186 has both codes stamped on the module handle.

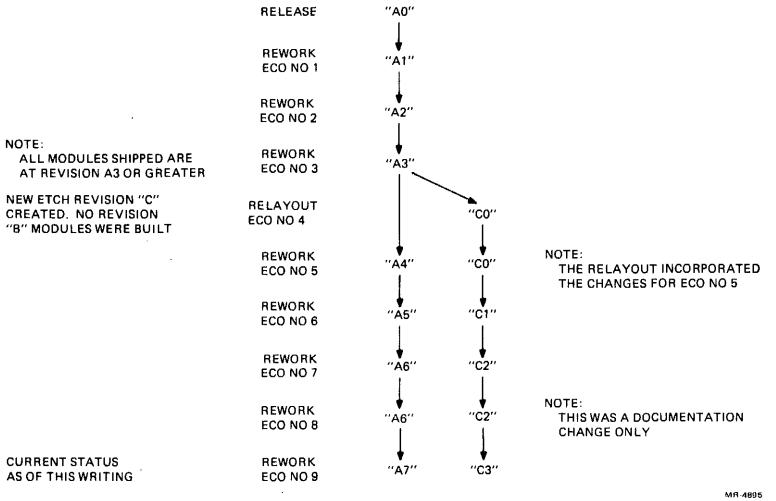
The revision identifier is a two-field alphanumeric designation. The first field indicates the etch revision. The second field indicates the modifications to this etch.



M8186 Revision Identifiers

The M8186 started as hardware revision A0, as shown above; that is, etch revision "A" with no modifications or work. As ECOs were released calling for rework (not a new etch), the hardware revisions were released and the etch revision field was incremented from A to B to C. No etch revision "B" for the M8186 modules was built so the revision level appeared to change from "A" to "C" via ECO no. 4. Etch revision "C" modules had ECO no. 5 incorporated on them before being released, therefore their hardware revision status did not change with ECO no. 5.

The hardware revision history of the M8186 is shown below.



M8186 ECO Summary

11/23 (M8186) ECO Summary

The following table details the ECOs issued since the first M8186 shipment. These ECOs are coded "M8186-ML000X", where "X" is the ECO number shown below.

ECO No.	Problem	Quick Verify
4	Too many wires and etch cuts, new etch needed. Note that the jumper locations change for etch revision "C".	Module handle will be stamped "C?" (where "?" refers to the CS revision).
5	Possible parity errors when using parity memories (MSV11-E, etc.)	Check for etch cut to E7 pins 16 and 18.
	NOTE **Implementation of this ECO impacts configurations. This ECO is discussed in detail below.**	
6	The internal wake-up circuit defeats the sequencing provided by standard DEC power supplies. This ECO should be installed when the M8186 is used with same.	Red jumper wire is installed in parallel with D1.
7	CTL/DAT hybrid (57-00000-00) and MMU IC (21-15542-00) were not compatible with KEF11-AA floating point option. The FP registers in the MMU were inaccessible, and the CTL/DAT data path caused intermittent errors in floating point instructions.	CTL/DAT should be 57-00000-01 and MMU should be 21-15542-01 for floating point compatibility. *Coordinate with ECO M8186-0009.*
8	MMU (21-15542-01) was included as part of the M8186 module. It should have been specified as an option that could have added to the MMU from the M8186. ECO KDF11A-0001 adds it back in at the option level (KDF11-AB, KDF11-AA). This is a documentation change only.	Modules in systems may or may not have MMU, depending upon which option they represent. Spares, however, are ordered as modules and will *not* have MMUs. MMUs must be ordered separately.

ECO No.	Problem	Quick Verify
9	1. No jumper table in print set (documentation change only).	1. Prints contain a jumper table.
	2. Metal oscillator may short to adjacent components.	2. Oscillator has nylon spacer. Manufacturing change only. Do *not* retrofit in field!
	3. Possibility of worst case MMU timing violations. Change configuration of W2 and W3 to adjust timing. This ECO *must* be installed: a. when ECO M8186-0007 is put in b. when a microcode option (i.e., KEF11) is installed c. when a 40-pin IC (CTL/DAT, MMU or KEF11) is replaced d. whenever unexplained system crashes occur.	3. Module will have W2 removed and W3 in. On etch Rev "A" modules, W3 is installed by soldering a jumper wire from E2 pin 5 to E2 pin 15.

ECO No. 5

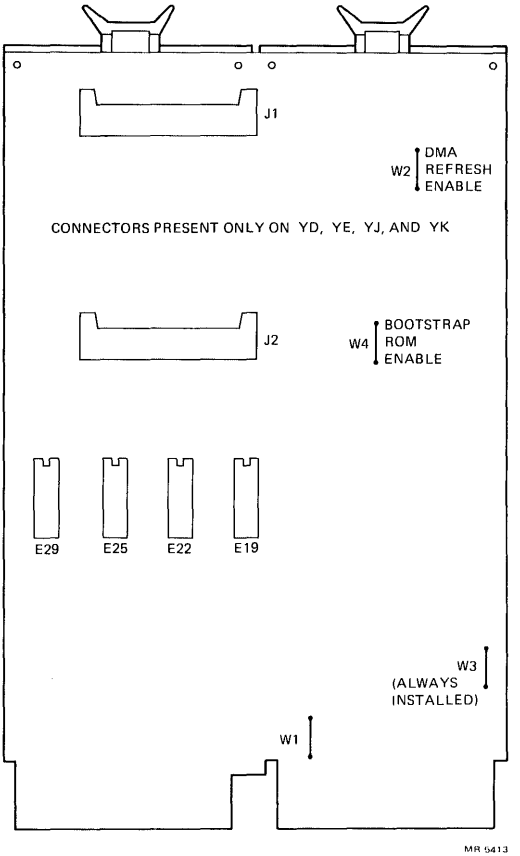
A circuit was included in the KDF11-A to compensate for a design limitation in the MSV11-C and MRV11-C. That is, these devices do not use BBS7 to deselect themselves. It is this limitation that causes the requirement to jumper-deselect memory in the 28K-32K range on LSI-11s; otherwise the MSV11-C would respond to peripheral addresses. Unfortunately, the parity problem with MSV11-E could not be fixed except by disabling this circuit. As a result, after this ECO is installed (hardware revision "A4" and above, and all etch revision "C"), the MSV11-C *cannot* be configured in the 28K-32K (word) or in the 124K-128K (word) range. MRV11-C cannot be configured in the 28K-32K (word) range on mapped systems when used in the "direct" or "window" addressed modes. On unmapped systems (11/03 and KDF11-AC) it may be configured in the I/O page.

M9400-XX
REV11, TEV11, AND BCV1X

	Amps		Bus Loads		Cables
	+5	+12	AC	DC	
M9400-YA (REV11-A)	1.64 (2.24 max.)	0	2.21	1.0	
M9400-YB (TEV11)	0.54 (0.70 max.)	0		1.0	
M9400-YC (REV11-C)	1.0 (1.85 max.)	0	2.21	1.0	
M9400-YD (BCV1A)	0	0	0	0	(2) BC05 L
M9400-YE (BCV1B)	0.29	0	0	0	(2) BC05 L
M9400-YF (REV11-F)					
M9400-YH (REV11-H)	1.64	0	2.21	1.0	
M9400-YJ (REV11-J)					(2) BC05 L
M9400-YK (REV11-K)					
M9400-YL (REV11-L)					
M9400-YM (REV11-M)					
M9400-YN (REV11-N)	1.64	0	2.21	1.0	

Related Documentation

REV11-A, C Field Maintenance Print Set (MP00073)
REV11-H Field Maintenance Print Set (MP00331)
TEV11 Field Maintenance Print Set (MP00074)
Microcomputer Interfaces Handbook (EB-20175-20)



M9400 Jumper Locations

W1: Installed to enable BDMG arbitration.
Installed on -YB, -YD, and -YE modules.
Not installed on -YA, -YC, -YF, -YH, -YK, and -YJ modules.

W2: Install to enable DMA refresh.

W3: Always installed.

W4: Install to enable bootstrap ROMs.

If REV11 refresh is enabled, the memory electrically farthest from the REV11 must reply to refresh. Also, processor refresh must be disabled.

NOTES

1. **If no memory replies to REV11 refresh, the REV11 may hang the processor. The problem will appear to be a non-functioning CPU.**

2. **If the REV11 is not up to ECO no. 5 level or greater, the same symptoms may occur if a DRV11 is present that has an external capacitor to extend NEW DATA READY to greater than 1.8 μs.**

	120 Ω TERMINATOR	250 Ω TERMINATOR	BOOT & DIAG ROMS	DMA REFRESH	CABLE CONNECTOR	W1 BDMG	W2 REFRESH ENABLE	W3 (FACTORY)	W4 ROM ENABLE	OPTION DESIGNATION
YA*	X		X	X		R	I	I	I	REV11-A
YB	X					I	R	I	R	TEV11
YC*			X	X		R	I	I	I	REV11-C
YD					X	I	R	I	R	BCV1A-XX
YE		X			X	I	R	I	R	BCV1B-XX
YF*	X					R	I	I	I	REV11-F
YH*	X		X	X		R	I	I	I	REV11-H **
YJ*		X	X	X	X	R	I	I	I	REV11-J
YK*			X	X		R	I	I	I	REV11-K **

X = FEATURE PRESENT
I = JUMPER INSTALLED
R = JUMPER REMOVED
* FACTORY-SET POTENTIOMETER
** REMOTE BOOT

MR-0829

M9400 Jumper Variations

The jumper states indicated in the preceding figure are as they are shipped from the factory.

BCV options also include M9401 backplane connectors and BC05L expansion cables. Certain rules for cable lengths and module locations must be observed. Refer to the "Systems Configurations" section for these configuration rules.

REV11 ROM Program Commands

Command **Function**

OD — ODT (Halt). This allows the operator to examine and/or alter memory and register locations via the console device. Control can be returned to the REV11 program by entering the ODT P (proceed) command if the PC has not been altered, and the console device will display the $ prompt character. If the PC has been altered, the operator can start program execution by entering the starting address 165006 and the G (go) commands as follows.

```
@ 165006G
$
```

The processor responds by displaying the $ prompt character on a new line and another REV11 command can be entered.

XM<CR> — Memory Diagnostic program. After successfully completing the diagnostic, the prompt character ($) is displayed on the console device. Errors are indicated by the following displays on the console device.

1. *173732*
   @

   This is an address test error. The expected (normal) data is in R3 and the invalid data is in the memory location pointed to by R2. If desired, continue diagnostic program execution by entering the ODT P command.

2. *173756*
   @

   This is a data test error. The expected (normal) data is stored in R3 and the invalid data is in the memory location pointed to by R2. If desired, continue diagnostic program execution by entering the ODT P command.

3. *000010*
   @

   A timeout trap has occurred in testing memory locations outside of the first (lowest) 4K memory.

REV11 ROM Program Commands (Cont)

Command **Function**

4. *nnnnnn*
   @

   A timeout trap has occurred in testing memory locations within the first 4K memory. The nnnnnn displayed is an indeterminate number.

The actual memory test consists of an address test and a data test. The address test first writes all memory locations with addresses; it then reads and verifies the addresses. The data test consists of two parts. An "all 1s" word is first walked through all memory locations, which are initially 0. The second part consists of walking an all 0s word through all memory locations which are all 1s.

XC<CR> Processor Diagnostic program. This is a memory-modifying instruction test. Successful execution of the diagnostic program results in the prompt character ($) being displayed on the console device. Errors are indicated by the following.

1. The program halts when an instruction sequence is not correctly executed.

2. The program halts in the trap vector area for various traps.

NOTE

When a halt occurs, the console ODT M command can be used to determine how the halt mode was invoked. When the system fails to successfully execute the above diagnostics, maintenance diagnostic programs should be used to thoroughly test processor (and memory) functions.

DX<CR> or DXn<CR> RXV11 floppy disk system bootstrap. Entering the DX<CR> command starts the memory-modifying CPU instruction test and memory test execution (see the XC and XM commands). Successful test execution results in execution of the bootstrap program for disk drive 0, the system disk. Otherwise, specify the drive number (n) as 0 (drive 0) or 1 (drive 1).

REV11 ROM Program Commands (Cont)

Command **Function**

Floppy disk bootstrap errors are:

1. The program halts and the console device displays the following.

   165316
   @

   This indicates that the device done flag in the RXV11 interface was not set within the required time (approximately 1.3 seconds). The bootstrap can be restarted by entering the P command; the $ is then displayed on the console device and the bootstrap command can be entered.

2. The program halts and the console displays the following.

   165644
   @

   This indicates that a bootstrap error occurred. The RXV11's error register contents are stored in R2. By examining the contents of R2 and using the information contained in the *RXV11 User's Manual*, the exact nature of the error can be determined. Examine the contents of R2 (nnnnnn) as follows.

   @ R2/*nnnnnn*<CR>
   @ P
   $

   After examining R2, the bootstrap can be restarted by the P command; enter the desired bootstrap command immediately after the $ prompt character.

3. The program halts in the trap vector for traps; a timeout trap returns the program to the $ prompt character. If a timeout trap occurs, first check for proper system cable connections and device interface module installation. Then, attempt to bootstrap the system by again entering the desired bootstrap command.

REV11 ROM Program Commands (Cont)

Command	Function
DK<CR> or DKn<CR>	Disk Drive System Bootstrap. Entering the DK command starts the memory-modifying CPU instruction test and memory test execution (see the XC and XM commands). Successful test execution results in execution of the bootstrap program for disk drive 0, the system disk. Otherwise, specify the drive number n as 0 (drive 0), 1 (drive 1), or 2 (drive 2).

Disk bootstrap errors are:

1. The program halts and the console device displays the following.

   165724
   @

   This indicates that the device done flag in the RKF11-D interface was not set within the required time (approximately 1.3 seconds). The bootstrap can be started by entering the P command; the $ is then displayed on the terminal and the bootstrap command can be entered.

2. The program halts and the console then displays the following.

   165644
   @

   This indicates that a bootstrap error occurred. The RKV11-D error register contents are stored in R2. By examining the contents of R2 and using the information contained in the *RKV11-D User's Guide*, EK-RKV11-OP, the nature of the error can be determined. Examine the contents of R2 (nnnnnn) as follows:

   @R2/*nnnnn*<CR>
   @P
   $

   After examining R2, the bootstrap can be restarted by the P command; enter the desired bootstrap command immediately after the $ prompt character.

REV11 ROM Program Commands (Cont)

Command **Function**

3. The program halts in the trap vector for traps; a timeout trap returns the program to the $ prompt character. If a timeout trap occurs, first check for proper system cable connections and device interface module installation. Then, attempt to bootstrap the system by again entering the desired bootstrap command.

AL<CR> Absolute Loader program, normal (absolute address) loading operation. Entering AL<CR> specifies that a paper tape is to be loaded via the console device (CSR address = 177560). However, another device can be specified by entering the appropriate CSR address. For example, to load paper tapes in absolute loader format via a device whose CSR address is 177550, enter the following command.

$ AL177550<CR>

The program responds by first executing the memory-modifying CPU instruction test and memory test (refer to the XC and XM commands). Successful test execution results in execution of the Absolute Loader program.

A successful program load is indicated when the console device displays the following.

165625
@

The loaded program automatically starts execution, or Absolute Loader errors are:

1. Checksum error, with the program halting and producing the following display.

   165534
   @

2. Program halts in the trap vector area for traps other than a timeout trap.

3. Timeout trap occurs, causing the display of $ on a new line on the console device.

REV11 ROM Program Commands (Cont)

Command	Function
AR<CR>	Absolute Loader program, relocated loading operation. When this command is entered, the memory-modifying CPU instruction test and memory test are automatically first executed (refer to the XC and XM commands), followed by the Absolute Loader program. Successful execution of the tests results in the program halting with the following console display.

165412
@

The operator must then enter the appropriate "software switch register" contents in R4. To select relocated loading, which uses an address (bias) contained in the software switch register, enter the following commands.

@ R4/ *xxxxxx* nnnnnn<CR>
@ P

The value nnnnnn is a relocation value selected by the operator as directed in the *PDP-11 Paper Tape Software Handbook*, 11-XPTSA-BD. Observe that the least significant "n" value entered must be an odd number; this sets the software switch register (R4) bit 0 to a logical 1, selecting the relocated loading mode. Note that the program being loaded must be in Position Independent Code (PIC) format for relocated loading.

When large programs are contained on more than one tape, the program halts at the end of the first tape. Install the second tape in the reader and enter a "1" in R4 using the ODT command shown below; resume loading by entering the P command.

@ R4/*xxxxxx* 1<CR>
@ P

The six octal digits (xxxxxx) are the present contents of R4. Entering a value of 1 selects relocated loading for the next program tape, starting at the address following the end of the previous load operation. The P command allows the Absolute Loader program execution to continue the loading process once the software switch register value has been entered.

REV11 ROM Program Commands (Cont)

Command Function

A successful program load is indicated when the loaded program automatically starts execution, or the console device displays.

165626
@

Absolute Loader errors are as described for the AL command.

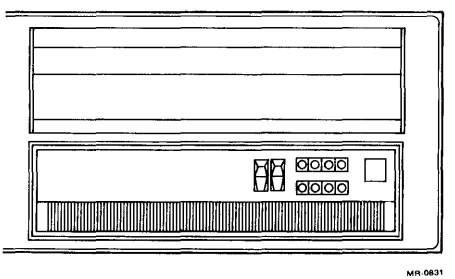
RK05

RK05 Disk Drive

The RK05-J disk drive uses a removable disk cartridge and the RK05-F uses a fixed, dual-density disk cartridge. Both drives are interfaced by the RKV11-D option. The RKV11-D is set at address 177400 and vector 220. Applicable diagnostic programs are found in Appendix A.

Related Documentation

RKV11-D Field Maintenance Print Set (MP-00223-00)
RK05-J Field Maintenance Print Set (MP-0RK05-0J)
RK05-F Field Maintenance Print Set (MP-0RK05-0F)
RKV11-D User's Guide (EK-RKV11-OP)
Microcomputer Interfaces Handbook (EB-20175-20)
RK05 Disk Drive User's Guide (EK-0RK05-OP)
RK05/05J/05F Maintenance Manual (EK-RK5JF-MM)
RK05 Exercisor Maintenance Manual (EK-RK05X-MM)



RK05 Disk Drive

Controls and Indicators for the RK05, RK05-J, and RK05-F

Controls and Indicators	Description
RUN/LOAD (Rocker Switch)	Placing this switch in the RUN position (provided that all interlocks are safe): a. locks the drive front door b. accelerates the disk to operating speed c. loads the read/write heads d. lights the RDY indicator. Placing this switch in the LOAD position: a. unloads the read/write heads b. stops the disk rotation c. unlocks the drive front door when the disk has stopped d. lights the LOAD indicator.
	CAUTION **Do not switch to the LOAD position during a write operation; this results in erroneous data being recorded.**
WT PROT (Rocker Switch Spring-Loaded Off)	Placing this momentary contact switch in the PROT position lights the WT PROT indicator and prevents a write operation; it also turns off the FAULT indicator, if that is lit. Depressing this switch in the WT PROT position a second time turns off the WT PROT indicator and allows a write operation.
PWR (Indicator)	Lights when operating power is present. Goes off when operating power is removed.
RDY (Indicator)	Lights when: a. the disk is rotating at the correct operating speed b. the heads are loaded c. no other conditions are present (all interlocks safe) to prevent a seek, read, or write operation. Goes off when the RUN/LOAD switch is set to LOAD.

Controls and Indicators for the RK05, RK05-J, and RK05-F (Cont)

Controls and Indicators	Description
ON CYL (Indicator)	Lights when: a. the drive is in the ready condition b. a seek or restore operation is not being performed c. the read/write heads are positioned and settled. Goes off during a seek or restore operation.
FAULT (Indicator)	Lights when: a. erase or write current is present without a write gate b. the linear positioner transducer lamp is inoperative. Goes off when the WT PROT switch is pressed, or when the drive is recycled through a run/load sequence.
WT PROT (Indicator)	Lights when: a. the WT PROT switch is pressed b. the operating system sends a WRITE PROTECT command. Goes off when the WT PROT switch is pressed a second time, or when the drive is recycled through a run/load sequence.
LOAD (Indicator)	Lights when the read/write heads are fully retracted and the spindle has stopped rotating.
WT (Indicator)	Lights when a write operation occurs. Goes off when the write operation terminates.
RD (Indicator)	Lights when a read operation occurs. Goes off when the read operation terminates.

RK05

Performance Specifications

Storage Medium

Type	Single-disk magnetic cartridge (RK05, RK05J - removable; RK05F - nonremovable)
Disk Diameter	5.51 cm (14 inches)

Magnetic Heads

Number	2

Bit Transfer

Transfer Code	Double frequency, NRZ recording
Transfer Rate	1.44 m bit/s

Electrical Requirements

Voltage	115/230 Vac @ 50/60 Hz ± .05 Hz
Power	250 VA
Starting Current	Power only: 1.8 A Start spindle: 10 A (for 2 seconds)

Model Designation

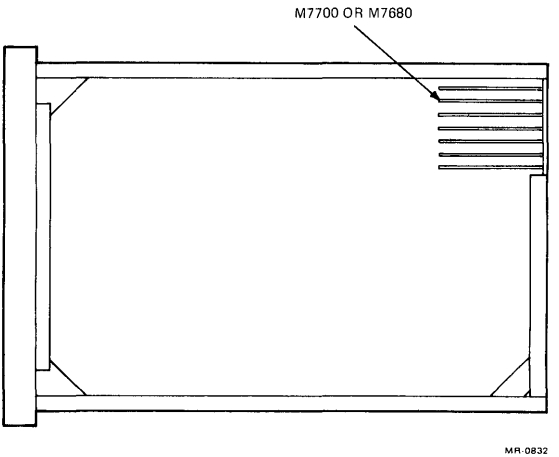
RK05-AA, RK05J-AA, RK05F-AA, RK05F-FA 95 - 130 Vac @ 60 ± 0.5 Hz
RK05-AB, RK05J-AB, RK05F-AB, RK05F-FB 290 - 260 Vac @ 60 ± 0.5 Hz
RK05-BA, RK05J-BA, RK05F-AC, RK05F-FC 95 - 130 Vac @ 50 ± 0.5 Hz
RK05-BB, RK05J-BB, RK05F-AD, RK05F-FD 190 - 260 Vac @ 50 ± 0.5 Hz

Dimensions and Weight

Width: 48 cm (19 in)
Depth: 67 cm (26.5 in)
Height: 27 cm (10.5 in)
Weight: 50 kg (110 lb)

Unit Selection

An RK05 disk drive may be configured to respond to a desired unit designation by selecting the appropriate setting on a rotary switch. The rotary switch is located on the second module in the card cage. The circuit cards are located behind the prefilter, and may be accessed by removing the rear cover panel on the bottom side of the disk drive unit. In the RK05-J, the rotary switch is on the M7700 module. In the RK05-F it is on the M7680.



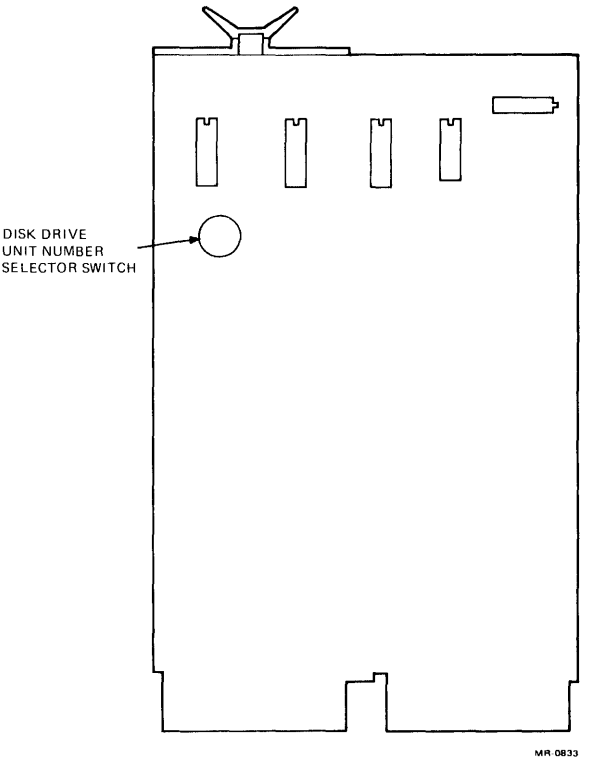
M7700 or M7680 Placement

Bootstrap Program for RK05

If an RK05 is used in a system that has no hardware bootstrap module, the disk drive may be booted by entering the following program manually.

```
@R0/000000 0n0000<CR>*
@R1/000000 177404<CR>
@1000/000000 000005<LF>
001002/000000 010061<LF>
001004/000000 000006<LF>
001006/000000 012761<LF>
001010/000000 177400<LF>
001012/000000 000002<LF>
001014/000000 012711<LF>
001016/000000 000005<LF>
001020/000000 105711<LF>
001022/000000 100376<LF>
001024/000000 005007<CR>
@1000G
```

*n = 0 for drive 0; 2 for drive 1; and 4 for drive 2.



Controller Switches

RL01/RL02 Disk Drive

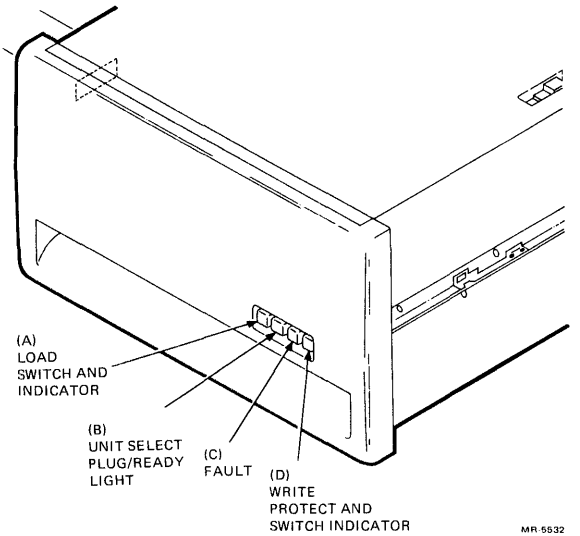
The RL01 is a 5,000,000 byte disk drive that uses a modified, removable, 5440-style cartridge (RL01K-DC). The RL02 is a dual-density version of the RL01. The RL02 uses an RL02K-DC cartridge. Both the RL01 and RL02 use the RLV11 interface module. Up to four drives of either type in any combination can be connected to an RLV11 interface. The RLV11 is normally configured for a bus address of 77440X octal with a vector address of 160 octal. For more in-depth information, refer to the RLV11 (M8013/8014) section. Additional information can be found in the following manuals.

RL01/RL02 Disk Drive Technical Manual (EK-RL012-TM)
RLV11 Technical Description (EK-RLV11-TD)
RL01/RL02 Pocket Service Guide (EK-RL012-PG)
RL01/RL02 Disk Subsystem User's Guide (EK-RL012-UG)
RL01 Illustrated Parts Breakdown (EK-0RL01-IP)
RL02 Illustrated Parts Breakdown (EK-0RL02-IP)
RL01 Field Maintenance Print Set (MP-00527-00)
RL02 Field Maintenance Print Set (MP-00698-00)
RLV11 Field Maintenance Print Set (MP-00635-00)
Microcomputer Interfaces Handbook (EB-20175-20)

Specifications RL01/RL02

Medium

Type:	Single platter, top-loading cartridge (similar to IBM 5440). Embedded servo information.
Capacity:	RL01K-DC = 5.2 Mb RL02K-DC = 10.4 Mb
Cylinders:	RL01 = 256 RL02 = 512
Sectors:	40
Heads:	2



RL01/RL02 Controls and Indicators

Data Transfer
MFM (Miller coding) recording; 244 ns cell time; 4.1 megabytes/s (4.9 μs/word).

RL01/RL02 Bootstrap
Ensure that the heads are over cylinder 0 and head 0 is selected by releasing the LOAD switch, waiting for the LOAD indicator to light, then depressing the LOAD switch. After the drive is ready, initialize the controller with a system initialize. Perform a bit status clear. Load the following program into memory.

LOC	Contents	Comments
10000	012737	Load CSR
10002	000014	
10004	174400	
10006	000001	Wait

Start the program at 10000 and allow it to run for a few seconds, halt the program and restart at 00000.

RL01/RL02 Controls and Indicators

Switches	Function
Power ON/OFF Circuit Breaker (Located in the rear of the drive)	In the OFF position, ac power is removed from the drive. In the ON position, ac power is supplied to the drive.
(A) LOAD	This is a PUSH/PUSH alternating action switch. When depressed, the RL01/RL02 begins a "cycle up" sequence, provided that: • the RL01/RL02K cartridge is installed • the cartridge cover is in place • the access door is closed • all ac and dc voltages are within spec • the R/W heads are retracted • the brushes are in the "home" position. When released, the RL01/RL02 will begin a "cycle down" sequence.
(B) UNIT SELECT PLUG	This is a cam-operated switch that is activated by inserting a numbered, cammed button. The switch contacts are binary encoded so that the drive assumes the logical unit number that is printed on the button.
(D) WRITE PROTECT	This is an alternating action PUSH/PUSH switch. When depressed, the drive assumes a write protect status (during a write operation). When released, the drive is no longer write protected.

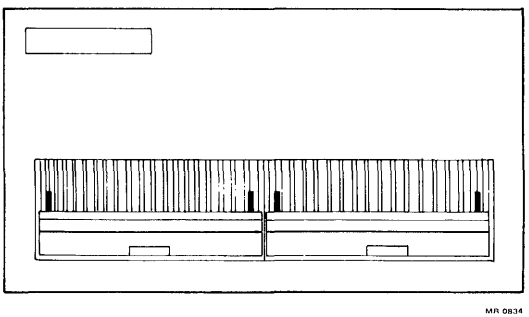
RL01/RL02 Controls and Indicators (Cont)

Indicators	Function
(A) LOAD (Yellow)	Indicates that the drive is ready to have a cartridge loaded (or unloaded). The LOAD indicator will light when: • the spindle is stopped • the R/W heads are "home" • the brushes are "home."
(B) READY (White)	When lit, indicates a "drive ready" condition; i.e., the heads are loaded and detented.
(C) FAULT (Red)	Indicates when one of the following has occurred. • drive select error • seek timeout error (1.5 second) • write current in heads during "sector time" • loss of system clock from RLV11 • write data error (no transitions) • spin error (over speed or 40 sec timeout) • write gate error (attempting to write when not ready, when write protected, or during sector time)
(D) WRITE PROTECT (Yellow)	Indicates that drive is write protected. That is, write operations to the cartridge will be inhibited (and the FAULT indicator will light).

RX01

RX01 Floppy Disk Drive

The RX01 floppy disk drive is part of the RXV11 floppy disk system, and is interfaced by the RXV11 interface module (M7946). The disk system uses address 177170 and vector 264 for the first option, and address 177174 and vector 270 for a second option.



RX01 Floppy Disk

Model Designations

RXV11-AA Single Drive System, 115 V/60 Hz
RXV11-AC Single Drive System, 115 V/50 Hz
RXV11-AD Single Drive System, 230 V/50 Hz
RXV11-BA Dual Drive System, 115 V/60 Hz
RXV11-BC Dual Drive System, 115 V/50 Hz
RXV11-BD Dual Drive System, 230 V/50 Hz

RX01

Related Documentation

RXV11 User's Manual (EK-RXV11-00)
RX01/RX8/RX11 Floppy Disk System Maintenance Manual (EK-RX01-MM)
RXV11 Field Maintenance Print Set (MP-00024-00)
RX01 Field Maintenance Print Set (MP-00296-00)
RX01/RX02 Reference Card (EK-RX01-RC)
Microcomputer Interfaces Handbook (EB-20175-20)

NOTE

50 Hz versions are available in voltages of 105, 115, 220, and 240 Vac by field-pluggable conversion. Refer to the *RX01/RX8/RX11 Floppy Disk System Maintenance Manual* for complete input power modification details.

AC Power

The RXV11 floppy disk system is available in the following three ac voltage/model configurations.

Models	Voltage/Frequency
RXV11-AA, -BA	100 Vac-132 Vac, 60 Hz
RXV11-AC, -BC	100 Vac-132 Vac, 50 Hz
RXV11-AD, -BD	180 Vac-264 Vac, 50 Hz, in one of two voltage ranges. The actual voltage range is user-selected by installing the appropriate power harness during system installation, as follows.

Voltage Range	Power Harness PN
180-240	70-10696-04
200-264	70-10696-03

Power Consumption

RX01	3 A at 24 V (dual), 75 W; 5 A at 5 V, 25 W
RXV11 interface (M7946)	Not more than 1.5 A at 5 Vdc
Power input (ac)	4 A at 115 Vac 2 A at 230 Vac

Bootstraps for Manual Entry

Full Length Version

@1000/000000 12702<LF>
001002/000000 1002n7<LF>*
001004/000000 12701<LF>
001006/000000 177170<LF>
001010/000000 130211<LF>
001012/000000 1776<LF>
001014/000000 112703<LF>
001016/000000 7<LF>
001020/000000 10100<LF>
001022/000000 10220<LF>
001024/000000 402<LF>
001026/000000 12710<LF>
001030/000000 1<LF>
001032/000000 6203<LF>
001034/000000 103402<LF>
001036/000000 112711<LF>
001040/000000 111023<LF>
001042/000000 32011<LF>
001044/000000 1776<LF>
001046/000000 100756<LF>
001050/000000 103766<LF>
001052/000000 105711<LF>
001054/000000 100771<LF>
001056/000000 5000<LF>
001060/000000 22710<LF>
001062/000000 240<LF>
001064/000000 1347<LF
001066/000000 122702<LF>
001070/000000 247<LF>
001072/000000 5500<LF>
001074/000000 5007<CR>

*n = 4 for unit 0
n = 6 for unit 1
<LF> = Line Feed
<CR> = Carriage Return
Starting address = 1000

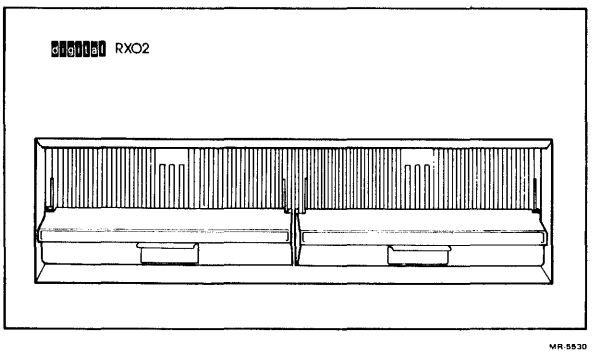
Abbreviated Version (Drive 0 Only)

@1000/000000 5000<LF>
001002/000000 12701<LF>
001004/000000 177170<LF>
001006/000000 105711<LF>
001010/000000 1776<LF>
001012/000000 12711<LF>
001014/000000 3<LF>
001016/000000 5711<LF>
001020/000000 1776<LF>
001022/000000 100405<LF>
001024/000000 105711<LF>
001026/000000 100004<LF>
001030/000000 116120<LF>
001032/000000 2<LF>
001034/000000 770<LF>
001036/000000 0<LF>
001040/000000 5007<CR>

RX02

RX02 Floppy Disk Drive

The RX02 is part of the RXV11-XX floppy disk system. The RXV21-BX options use the RX02 in double-density mode with the RXV21 (M8029) interface module. The RXV21-DX options use the RX02 in single-density mode with the RXV11 (M7946) interface module.



Front View of the Floppy Disk System

The density mode of the RX02 is selected by switches on the M7744 controller module. This module is located in the RX02 floppy disk drive. The following switch settings define the mode of the RX02.

Controller Configuration Switch Settings (Located on M7744 Module)

Interface	S1-1	S1-2
RX211/RXV21	OFF	ON
RX8E/RX11/RXV11	ON	OFF
RX28	OFF	OFF

NOTE

The subject of the RX02 as used in a PDP-8 system is beyond the scope of this document.

Detailed configuration and diagnostic information is contained in this manual. Refer to the section covering the applicable interface (M7946 or M8029).

Related Documentation

RX02 Floppy Disk System User's Guide (EK-0RX02-UG)
RX01/RX02 Reference Card (EK-RX102-RC)
Microcomputer Interface Handbook (EK-20175-20)
RX02 Print Set (MP-00629-00)

Module Designations

RXV21	-DA	M7946	RX02-DA	115 V, 60 Hz
	-DC	M7946	RX02-DC	115 V, 50 Hz
	-DD	M7946	RX02-DD	230 V, 50 Hz
	-BA	M8029	RX02-BA	115 V, 60 Hz
	-BC	M8024	RX02-BC	115 V, 50 Hz
	-BD	M8027	RX02-BD	230 V, 50 Hz

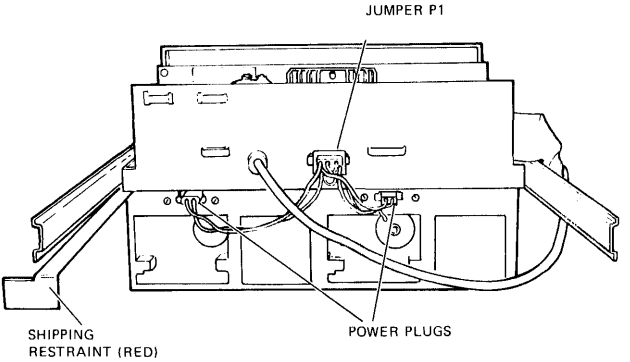
Power Requirements

The RX02 is designed to use either a 60 Hz Vac or a 50 Hz power source. The 60 Hz version will operate from 90 Vac-128 Vac, without modifications, and will use less than 4 A operating. The 50 Hz version will operate within four voltage ratings and will require field verification/modification to ensure that the correct voltage option is selected. The voltage ranges of 90 Vac-120 Vac and 184 Vac-240 Vac will use less than 4 A operating. The voltage ranges of 100 Vac-128 Vac and 200 Vac-256 Vac will use less than 2 A. Both versions of the RX02 will be required to receive the input power from an ac source (e.g., 861 power control) that is controlled by the system's power switch.

Input Power Modification Requirements

The 60 Hz version of the RX02 uses the H771-A power supply and will operate on 90 Vac-128 Vac, without modification. To convert to operate on a 50 Hz power source in the field, the H771-A supply must be replaced with an H771-C or -D and the drive motor belt and drive motor pulley must be replaced. The H771-C operates on a 90 Vac-120 Vac or 100 Vac-128 Vac power source. The H771-D operates on a 184 Vac-240 Vac or 200 Vac-256 Vac power source. To convert the H771-C to the higher voltage ranges or the H771-D to the lower voltage ranges, the power harness and circuit breaker must be changed. The appropriate jumper and circuit breaker are shown in the following figure.

RX02



VOLTAGE (VAC)	JUMPER	CIRCUIT BREAKER
90-120	70-10696-02	3.5 A, 12-12301-01
100-128	70-10696-01	3.5 A, 12-12301-01
184-240	70-10696-04	1.75 A, 12-12301-00
200-256	70-10696-03	1.75 A, 12-12301-00

MR 5531

RX02 (Rear View)

Bootstrap for Manual Entry (ODT)

RX02/RXV11 (M7946)

```
@1000/XXXXXX    5000<LF>
1002/XXXXXX     12701<LF>
1004/XXXXXX     177170<LF>
1006/XXXXXX     105711<LF>
1010/XXXXXX     1776<LF>
1012/XXXXXX     12711<LF>
1014/XXXXXX     3<LF>
1016/XXXXXX     5711<LF>
1020/XXXXXX     1776<LF>
1022/XXXXXX     100405<LF>
1024/XXXXXX     105711<LF>
1026/XXXXXX     1000004<LF>
1030/XXXXXX     116120<LF>
1032/XXXXXX     2<LF>
1034/XXXXXX     770<LF>
1036/XXXXXX     0<LF>
1040/XXXXXX     5000<LF>
1042/XXXXXX     110<CR>
@1000G
```

<LF> = Line Feed.
<CR> = Carriage Return.
XXXXXX = Original contents of location opened.

RX02/RXV21 (M8029)

@2000/XXXXXX	12701<LF>
2002/XXXXXX	177170<LF>
2004/XXXXXX	12700<LF>
2006/XXXXXX	100240<LF>
2010/XXXXXX	5002<LF>
2012/XXXXXX	12705<LF>
2014/XXXXXX	200<LF>
2016/XXXXXX	12904<LF>
2020/XXXXXX	401<LF>
2022/XXXXXX	12703<LF>
2024/XXXXXX	177172<LF>
2026/XXXXXX	10011<LF>
2030/XXXXXX	1776<LF>
2032/XXXXXX	100440<LF>
2034/XXXXXX	12711<LF>
2036/XXXXXX	407<LF>
2040/XXXXXX	10011<LF>
2042/XXXXXX	1776<LF>
2044/XXXXXX	100433<LF>
2046/XXXXXX	110413<LF>
2050/XXXXXX	304<LF>
2052/XXXXXX	30011<LF>
2054/XXXXXX	1776<LF>
2056/XXXXXX	110413<LF>
2060/XXXXXX	304<LF>
2062/XXXXXX	30011<LF>
2064/XXXXXX	1776<LF>
2066/XXXXXX	100422<LF>
2070/XXXXXX	12711<LF>
2072/XXXXXX	408<LF>
2074/XXXXXX	10011<LF>
2076/XXXXXX	1776<LF>
2100/XXXXXX	100415<LF>
2102/XXXXXX	10513<LF>
2104/XXXXXX	30011<LF>
2106/XXXXXX	1776<LF>
2110/XXXXXX	100411<LF>
2112/XXXXXX	10213<LF>
2114/XXXXXX	6052<LF>
2116/XXXXXX	60502<LF>
2120/XXXXXX	122474<LF>
2122/XXXXXX	120427<LF>
2124/XXXXXX	7<LF>

RX02/RXV21 (M8029) (Cont)

```
2126/XXXXXX     3737<LF>
2130/XXXXXX     5000<LF>
2132/XXXXXX     5007<LF>
2134/XXXXXX     0<CR>
@2000G
```

Module Number	Option Name	Diagnostic and DEC/X11 File Names	Notes	Diagnostic and DEC/X11 Module Titles		Listing and Paper Tape PNs	RX01	RX02	RK05	RL01	RL02
M7264-XX	KD11-F/ KD11-H/ KD11-HW (LSI-11)	VKAA??.BI?		LSI-11 Basic Instruction Test	(Listing)	AC-8186C-MC	4	13	18	19	20
					(Binary PT)	AK-8188C-MC					
		VKAB??.BI?		LSI-11 EIS Instruction Set Test	(Listing)	AC-8190A-MC	4	13	18	19	20
					(Binary PT)	AK-8192A-MC					
		VKAC??.BI?	5	LSI-11 FIS Instruction Set Test	(Listing)	AC-8194C-MC	4	13	18	19	20
					(Binary PT)	AK-8197C-MC					
		VKAD??.BI?	5	LSI-11 Traps Test	(Listing)	AC-8198C-MC	4	13	18	19	20
					(Binary PT)	AK-8-IC-MC					
		VKAH??.BI?		LSI-11 4K System Exerciser	(Listing)	AC-8210A-MC	4	13	18	19	20
					(Binary PT)	AK-8212A-MC					
		VKAI??.BI?	6	LSI-11 DIS Move & String Test	(Listing)	AC-8214A-MC	4	13	18	19	20
					(Binary PT)	AK-8217A-MC					
		VKAJ??.BI?	6	LSI-11 DIS Decimal Instructions	(Listing)	AC-8218A-MC	4	13	18	19	20
					(Binary PT)	AK-8221A-MC					
		VKAL??.BI?	5	LSI-11 Trap Test (30K + FIS)	(Listing)	AC-F012A-MC	4	13	18	19	20
					(Binary PT)	AK-F014A-MC					
		XCPA??.OBJ		DEC/X11 Processor Test Module	(Listing)	AC-E664G-MC					
					(Binary PT)	AK-E665G-MC					
		XCPB??.OBJ		DEC/X11 EIS Exerciser Module	(Listing)	EC-E667J-MC	1	14	18	19	20
					(Binary PT)	AK-E668J-MC					

Module Number	Option Name	Diagnostic and DEC/X11 File Names	Notes	Diagnostic and DEC/X11 Module Titles		Listing and Paper Tape PNs	RX01	RX02	RK05	RL01	RL02
M7269	RKV11-D	ZRKH??.BI?	7,8	RK11/RK05 Performance Exerciser	(Listing) (Binary PT)	AC-9232G-MC AK-9235G-MC	2	13	18	19	20
		ZRKI??.BI?	7	RK11 Utility Package	(Listing) (Binary PT)	AC-9236F-MC AC-9239F-MC	2	13	18	19	20
		ZRKJ??.BI?	7	RK11 Basic Logic Test No. 1	(Listing) (Binary PT)	AC-9240E-MC AK-9243E-MC	2	13	18	19	20
		ZRKK??.BI?	7,9	RK11 Basic Logic Test No. 2	(Listing) (Binary PT)	AC-9244F-MC AK-9247F-M1	2	13	18	19	20
		ZRKL??.BI?	7,10	RK11/RK05 Dynamic Test	(Listing) (Binary PT)	AC-9248E-MC AK-9251E-MC	2	13	18	19	20
		XRKA??.OBJ	7	DEC/X11 RK11 Exerciser Module	(Listing) (Binary PT)	AC-E676G-MC AK-E677G-MC	6	16	18	19	20
M7270	KD11-HA	VKAA??.BI?		LSI-11 Basic Instruction Test	(Listing) (Binary PT)	AC-8186C-MC AK-8188C-MC	4	13	18	19	20
		VKAB??.BI?		LSI-11 EIS Instruction Set Test	(Listing) (Binary PT)	AC-8190A-MC AK-8192A-MC	4	13	18	19	20
		VKAC??.BI?	5	LSI-11 FIS Instruction Set Test	(Listing) (Binary PT)	AC-8194C-MC AK-8197C-M1	4	13	18	19	20
		VKAD??.BI?	5	LSI-11 Traps Test	(Listing) (Binary PT)	AC-8198C-MC AK-8201C-MC	4	13	18	19	20
		VKAH??.BI?		LSI-11 4K System Exerciser	(Listing) (Binary PT)	AC-8210A-MC AK-8212A-MC	4	13	18	19	20
		XCPA??.OBJ		DEC/X11 Processor Test Module	(Listing) (Binary PT)	AC-E664G-MC AK-E665G-MC	1	14	18	19	20
		XCPB??.OBJ		DEC/X11 EIS Exerciser Module	(Listing) (Binary PT)	AC-E667J-MC AK-E668J-MC	1	14	18	19	20

Module Number	Option Name	Diagnostic and DEC/X11 File Names	Notes	Diagnostic and DEC/X11 Module Titles		Listing and Paper Tape PNs	RX01	RX02	RK05	RL01	RL02
M7940	DLV11	VKAE??.BI?	11a,12	DLV11 Test	(Listing)	AC-8202B-MC	4	13	18	19	20
					(Binary PT)	AK-8205B-MC					
		XDLA??.OBJ	11a	DEC/X11 DL11 Exerciser Module	(Listing)	AC-E709J-MC	5	14	18	19	20
					(Binary PT)	AK-E710J-MC					
M7941	DRV11	VKAF??.BI?	13	DRV11 Test	(Listing)	AC-8206D-MC	4	13	18	19	20
					(Binary PT)	AK-8208D-MC					
		XDRA??.OBJ	13	DEC/X11 DR11-A Exerciser Module	(Listing)	AC-E854D-MC	5	13	18	19	20
					(Binary PT)	AK-E855D-MC					
M7942	MRV11-AA	NA									
M7944	MSV11-B	ZKMA??.BI?	4a	MOS/Core 0-124K Exerciser	(Listing)	AC-8850F-MC	4	13	18	19	20
					(Binary PT)	AK-8854F-MC					
		ZQMC??.BI?	4b	0-124K Memory Exerciser (16K)	(Listing)	AC-9045F-MC	12	13	18	19	20
					(Binary PT)	AK-9048F-MC					
M7946	RXV11	ZRXA??.BI?	7,14	RX11 System Reliability TEST	(Listing)	AC-9334E-MC	7	13	18	19	20
					(Binary PT)	AK-9337E-MC					
		ZRXB??.BI?	7	RX11 Interface Diagnostic	(Listing)	AC-9339F-MC	7	13	18	19	20
					(Binary PT)	AK-9343F-MC					
		XRXA??.OBJ	7	DEC/X11 RX01 Exerciser Module	(Listing)	AC-E736E-MC	6	16	18	19	20
					(Binary PT)	AK-E737E-MC					

Module Number	Option Name	Diagnostic and DEC/X11 File Names	Notes	Diagnostic and DEC/X11 Module Titles		Listing and Paper Tape PNs	RX01	RX02	RK05	RL01	RL02
M7948	DRV11-P	NA									
M7949	LAV11	ZLAE??.BI?		LA180 Printer Diagnostic	(Listing)	AC-8906B-MC	7	13	18	19	20
					(Binary PT)	AK-8908B-MC					
		XLPA??.OBJ		DEC/X11 LP11 Exerciser Module	(Listing)	AC-E670F-MC	6	14	18	19	20
					(Binary PT)	AK-E671F-MC					
M7950	DRV11-B	VDRA??.BI?	13,15	DRV11-B DMA Interface Diagnostic	(Listing)	AC-8178A-MC	8	15	18	19	20
					(Binary PT)	AK-8180A-MC					
		VDRB??.BI		DRV11-B Interprocessor Exerciser	(Listing)	AC-8182A-MC	8	15	18	19	20
					(Binary PT)	AK-8184A-MC					
		XDRF??.OBJ	13	DEC/X11 DRV11-B Exerciser Module	(Listing)	AC-E739C-MC	5	14	18	19	20
					(Binary PT)	AK-E740C-MC					
M7951	DUV11-DA	ZDUQ??.BI?	16	DUV11 Off-Line Logic Tests	(Listing)	AC-8704C-MC	12	15	18	19	20
					(Binary PT)	AK-8707C-MC					
		ZDUR??.BI?	16	DUV11 Off-Line Receiver Tests	(Listing)	AC-8708B-MC	12	15	18	19	20
					(Binary PT)	AK-8711B-MC					
		ZDUS??.BI?	16	DUV11 Off-Line Receiver Timing	(Listing)	AC-8712B-MC	12	15	18	19	20
					(Binary PT)	AK-8715B-MC					
		ZDUT??.BI?	16	DUV11 Off-Line Transmitter Tests	(Listing)	AC-8716B-MC	12	15	18	19	20
					(Binary PT)	AK-8719B-MC					
		ZDUU??.BI?	16	DUV11 Off-Line Timing & Interrupt	(Listing)	AC-8720B-MC	12	15	18	19	20
					(Binary PT)	AK-8723B-MC					
		ZDUV??.BI?	16	DUV11 Off-Line Combined Tests	(Listing)	AC-8724B-MC	12	15	18	19	20
					(Binary PT)	AK-8727B-MC					
		XDUA??.OBJ		DEC/X11 DU11 Exerciser Module	(Listing)	AC-E718I-MC	5	14	18	19	20
					(Binary PT)	AK-E719I-MC					

Module Number	Option Name	Diagnostic and DEC/X11 File Names	Notes	Diagnostic and DEC/X11 Module Titles		Listing and Paper Tape PNs	RX01	RX02	RK05	RL01	RL02
M7952	KWV11-A	VKWA??.BI?	17,18 19,20 21	KWV11-A Diagnostic	(Listing)	AC-8222C-MCM	4	13	18	19	20
					(Binary PT)	AK-8225C-MC					
		XKWE??.OBJ		DEC/X11 KWV11-K Exerciser Module	(Listing)	AC-E920B-MC	5	14	18	19	20
					(Binary PT)	AK-E921B-MC					
M7954	IBV11-A	VIBA??.BI?	22,23 24	IBV11-A Diagnostic	(Listing)	AC-A880A-MC	8	15	18	19	20
					(Binary PT)	AK-A882A-MC					
		VIBB??.BI?	22,23 24	IBV11-A (30K) Diagnostic	(Listing)	AC-F015A-MC	12	15	18	19	20
					(Binary PT)	AK-F017A-M1					
		XIBA??.OBJ	25	IBV11-A Exerciser Module	(Listing)	AC-E914D-MC	5	14	18	19	20
					(Binary PT)	AK-E915D-MC					
M7955	MSV11-C	ZKMA??.BI?	4a	MOS/Core 0-124K Exerciser	(Listing)	AC-8850F-MC	4	13	18	19	20
					(Binary PT)	AK-8854F-MC					
		ZQMC??.BI?	4b	0-124K Memory Exerciser (16K)	(Listing)	AC-9045F-MC	12	13	18	19	20
					(Binary PT)	AK-9048F-MC					
M7957	DZV11	VDZA??.BI?	26,27	DZV11 4 Line Asynch MUX 1 OF 2	(Listing)	AC-A877A-MC	9	15	18	19	20
					(Binary PT)	AK-A879A-MC					
		VDZB??.BI?	26,27	DZV11 4 Line Asynch MUX 2 OF 2	(Listing)	AC-A938A-MC	9	15	18	19	20
					(Binary PT)	AK-A940A-MC					
		VDZC??.BI?	26,27	DZV11 Cable and Echo Test	(Listing)	AC-A941A-MC	9	15	18	19	20
					(Binary PT)	AK-A943A-MC					
		VDZD??.BI?		DZV11 Overlay for ITEP	(Listing)	AC-A935A-MC	9	15	18	19	20
					(Binary PT)	AK-A937A-MC					
		XDZB??.OBJ		DEC/X11 DZV11 Exerciser Module	(Listing)	AC-E911C-MC	5	14	18	19	20
					(Binary PT)	AK-E912C-MC					

Module Number	Option Name	Diagnostic and DEC/X11 File Names	Notes	Diagnostic and DEC/X11 Module Titles		Listing and Paper Tape PNs	RX01	RX02	RK05	RL01	RL02
M8012	BDV11-AA	VM8A??.BI?	28,29 30	BDV11-AA Diagnostic	(Listing) (Binary PT)	AC-B061C-MC AK-B063C-MC	8	13	18	19	20
		XBMD??.OBJ		DEC/X11 LSI-11 BDV11 Exerciser	(Listing) (Binary PT)	AC-F060C-MC AK-F061C-MC	1	14	18	19	20
M8013/ M8014	RLV11	VRLA??.BI?		RLV11 RL01 Diskless Test	(Listing) (Binary PT)	AC-B107B-MC AK-B109B-MC	10	17	18	19	20
		ZRLG??.BI?	7,31	RL11/RLV11 Controller Test 1	(Listing) (Binary PT)	AC-F111B-MC AK-F108B-MC	10	17	18	19	20
		ZRLH??.BI?	7,32 33 •	RL11/RLV11 Controller Test 2	(Listing) (Binary PT)	AC-F115B-MC AK-F112B-MC	10	17	18	19	20
		ZRLI??.BI?	7,34 35 •	RL01/02 Drive Test 1	(Listing) (Binary PT)	AC-F119C-MC AK-F116C-MC	10	17	18	19	20
		ZRLJ??.BI?	7,36	RL01/02 Drive Test 2	(Listing) (Binary PT)	AC-F123B-MC AK-F120B-MC	10	17	18	19	20
		ZRLK??.BI?	7,35 37	RL01/02 Performance Exerciser	(Listing) (Binary PT)	AC-F127B-MC AK-F124B-MC	10	17	18	19	20
		ZRLL??.BI?	7,35	RL01/02 Drive Compatibility Test	(Listing) (Binary PT)	AC-F131B-MC AK-F128B-MC	11	17	18	19	20
		ZRLM??.BI?	7,35 38	RL01/02 Bad Sector File Tool	(Listing) (Binary PT)	AC-F135B-MC AK-F132B-MC	11	17	18	19	20
		ZRLN??.BI?	7,39 40 •	RL01/02 Drive Test 3	(Listing) (Binary PT)	AC-F843A-MC AK-F844-MC	11	17	18	19	20
		XRLA??.OBJ	7	RL11/RLV11/RL01/RL02 Exerciser	(Listing) (Binary PT)	AC-E965D-MC AK-E966D-MC	6	16	18	19	20

Module Number	Option Name	Diagnostic and DEC/X11 File Names	Notes	Diagnostic and DEC/X11 Module Titles		Listing and Paper Tape PNs	RX01	RX02	RK05	RL01	RL02
M8016	KPV11-X	VKPA??.BI?	41,42 43	KPV11-A Diagnostic	(Listing) (Binary PT)	AC-A883A-MC AK-A885A-MC	8	13	18	19	20
M8017	DLV11-E	VDVA??.BI?	11b	DLV11-E Off-Line Test	(Listing) (Binary PT)	AC-B150B-MC AK-B152B-MC	8	13	18	19	20
		XDLA??.OBJ	11b	DEC/X11 DL11 Exerciser Module	(Listing) (Binary PT)	AC-E709J-MC AK-E710J-MC	5	14	18	19	20
M8018	KUV11-AA	VKUA??.BI?	44	KUV11-AA (LSI WCS) Diagnostic	(Listing) (Binary PT)	AC-E102A-MC AK-E104A-MC	4	13	18	19	20
		XKUA??.OBJ	45	DEC/X11 KUV11-AA Exerciser Module	(Listing) (Binary PT)	AC-E992B-MC AK-E993B-MC	5	14	18	19	20
M8021	MRV11-BA	VMRA??.BI?		LSI-11 UVPROM-RAM (MRV11-BA) Test	(Listing) (Binary PT)	AC-B153A-MC AK-B155A-MC	8	15	18	19	20
		ZKMA??.BI?	4a,46	MOS/Core 0-124K Exerciser	(Listing) (Binary PT)	AC-8850F-MC AK-8854F-MC	4	13	18	19	20
		ZQMC??.BI?	4b,46	0-124 K Memory Exerciser (16K)	(Listing) (Binary PT)	AC-9045F-MC AK-9048F-MC	12	13	18	19	20
M8027	LPV11	ZLAE??.BI?		LA180 Printer Diagnostic	(Listing) (Binary PT)	AC-8906B-MC AK-8908B-MC	7	13	18	19	20
		XLPA??.OBJ		DEC/X11 LP11 Exerciser Module	(Listing) (Binary PT)	AC-E670F-MC AK-E671F-MC	6	14	18	19	20

Module Number	Option Name	Diagnostic and DEC/X11 File Names	Notes	Diagnostic and DEC/X11 Module Titles		Listing and Paper Tape PNs	RX01	RX02	RK05	RL01	RL02
M8028	DLV11-F	VDVC??.BI?	11a	DLV11-F Off-Line Test	(Listing)	AC-E0068-MC	8	13	18	19	20
					(Binary PT)	AK-E008B-MC					
		XDLA??.OBJ	11a	DEC/X11 DL11 Exerciser Module	(Listing)	AC-E709J-MC	5	14	18	19	20
					(Binary PT)	AK-E710J-MC					
M8029	RXV21	ZRXC??.BI?	7	RX02 Utility Driver	(Listing)	AC-E509A-MC	3	13	18	19	20
					(Binary PT)	AK-E511A-MC					
		ZRXD??.BI?	7	RX02 SS Performance Exerciser	(Listing)	AC-E512B-MC	3	13	18	19	20
					(Binary PT)	AK-E514B-MC					
		ZRXE??.BI?	7	RX02 Formatter Program	(Listing)	AC-E622A-M2	2	13	18	19	20
					(Binary PT)	AK-E624A-M2					
		ZRXF??.BI?	7	RX02 FCTN/Log	(Listing)	AC-E625A-MC	3	13	18	19	20
					(Binary PT)	AK-E627A-M1					
		XRXB??.OBJ	7	DEC/X11 RX02 Exerciser Module	(Listing)	AC-F098C-MC	6	16	18	19	20
					(Binary PT)	AK-F100C-MC					
M8043	DLV11-J	VDLA??.BI?	47,48	DLV11-J Test	(Listing)	AC-E188B-MC	8	15	18	19	20
					(Binary PT)	AK-E190B-MC					
		XDLA??.OBJ	48	DEC/X11 DL11 Exerciser Module	(Listing)	AC-E709J-MC	5	14	18	19	20
					(Binary PT)	AK-E710J-MC					
M8044/ M8045	MSV11-DX/ MSV11-EX	ZKMA??.BI?	4a	MOS/Core 0-124K Exerciser	(Listing)	AC-8850F-MC	4	13	18	19	20
					(Binary PT)	AK-8854F-MC					
		ZQMC??.BI?	4b	0-124K Memory Exerciser (16K)	(Listing)	AC-9045F-MC	12	13	18	19	20
					(Binary PT)	AK-9048F-MC					

Module Number	Option Name	Diagnostic and DEC/X11 File Names	Notes	Diagnostic and DEC/X11 Module Titles		Listing and Paper Tape PNs	RX01	RX02	RK05	RL01	RL02
M8047	MXV11-AX	VMXA??.BI?	48	MXV11-AX Diagnostic	(Listing)	AC-E656A-MC	12	15	18	19	20
					(Binary PT)	AK-E658A-MC					
		ZKMA??.BI?	4a	MOS/Core 0-124K Exerciser	(Listing)	AC-8850F-MC	4	13	18	19	20
					(Binary PT)	AK-8854F-MC					
		ZQMC??.BI?	4b	0-124K Memory Exerciser (16K)	(Listing)	AC-9045F-MC	12	13	18	19	20
					(Binary PT)	AK-9048F-MC					
		XDLA??.OBJ	48	DEC/X11 DL11 Exerciser Module	(Listing)	AC-E709J-MC	5	14	18	19	20
					(Binary PT)	AK-E710J-MC					
M8048	MRV11-C	NA									
M8049	DRV11-J	VDRC??.BI?	49	DRV11-J Diagnostic Test Part 1	(Listing)	AC-F756A-M1	8	15	18	19	20
					(Binary PT)	AK-F757A-M1					
		VDRD??.BI?	49	DRV11-J Diagnostic Test Part 2	(Listing)	AC-F759A-MC	8	15	18	19	20
					(Binary PT)	AK-F760A-MC					
M8186	KDF11-A	JKDA??.BI?	50	KTF11-AA Diagnostic	(Listing)	AC-F138C-MC	9	13	18	19	20
					(Binary PT)	AK-F136C-MC					
		JKDB??.BI?		DCF11-AA Diagnostic	(Listing)	AC-F141C-M1	9	13	18	19	20
					(Binary PT)	AK-F139C-MC					
		JKDC??.BI?		KEF11-AA Diagnostic no. 1	(Listing)	AC-F241B-MC	9	13	18	19	20
					(Binary PT)	AK-F240B-MC					
		JKDD??.BI?	51	KEF11-AA Diagnostic no. 2	(Listing)	AC-F244B-MC	9	13	18	19	20
					(Binary PT)	AK-F243B-MC					
		XCPA??.OBJ		DEC/X11 Processor Test Module	(Listing)	AC-E664G-MC	1	14	18	19	20
					(Binary PT)	AK-E665G-MC					
		XCPB??.OBJ		DEC/X11 EIS Exerciser Module	(Listing)	AC-E667J-MC	1	14	18	19	20
					(Binary PT)	AK-E668J-MC					
		XFPA??.OBJ		DEC/X11 FP11 Exerciser Module	(Listing)	AC-E742G-MC	5	14	18	19	20
					(Binary PT)	AK-E743G-MC					

Module Number	Option Name	Diagnostic and DEC/X11 File Names	Notes	Diagnostic and DEC/X11 Module Titles		Listing and Paper Tape PNs	RX01	RX02	RK05	RL01	RL02
M9400/ M9401	REV11-X/ TEV11/ BCV1X	ZM9A??.BI?		Bootstrap/Terminator Test	(Listing)	AC-8954E-MC	7	13	18	19	20
					(Binary PT)	AK-8957E-MC					
		XBMC??.OBJ		DEC/X11 Bootstrap/Terminator	(Listing)	AC-F057N-MC	1	14	18	19	20
					(Binary PT)	AK-F058N-MC					
A012	ADV11-A	VADA??.BI?	1	ADV11 Performance Test	(Listing)	AC-8174C-MC	8	13	18	19	20
					(Binary PT)	AK-8176C-MC					
					(DOC/PT Kit)	ZJ250-RB					
		XADC??.OBJ	2,3	DEC/X11 ADV11 Exerciser Module	(Listing)	AC-E923B-MC	1	14	18	19	20
					(Binary PT)	AK-E924B-MC					
A6001	AAV11-A	VAAA??.BI?		AAV11 Diagnostic Test	(Listing)	AC-8169A-MC	8	15	18	19	20
					(Binary PT)	AK-8172A-MC					
					(DOC/PT Kit)	ZJ248-RB					
		XAAC??.OBJ		DEC/X11 AAV11 Exerciser Module	(Listing)	AC-E917B-MC	1	14	18	19	20
					(Binary PT)	AK-E918B-MC					
G653/ H223	MMV11-A	ZKMA??.BI?	4a	MOS/Core 0-124K Exerciser	(Listing)	AC-8850F-MC	4	13	18	19	20
					(Binary PT)	AK-8854F-MC					
		ZQMC??.BI?	4b	0-124K Memory Exerciser (16K)	(Listing)	AC-9045F-MC	12	13	18	19	20
					(Binary PT)	AK-9048G-MC					

Notes

1. Wraparound test and auto-tests require Berg test connector 70-12894-00.

2. Requires an analog ground on any channel to be tested.

3. May be run asynchronously if KWV11 is present in system. If run asynchronously, XKWE??.OBJ must be deselected from the DEC/X11 run.

4a. Memory space under test should be contiguous and read/write. For systems having noncontiguous memory, the memory boundaries must be defined by the operator before running the program. This diagnostic requires 8K of memory space to run in.

4b. This test will run successfully only on an 11/23 processor with a minimum of 16K of memory.

5. LTC must be disabled.

6. VKAA??.BI? and VKAD??.BI? should be run on the CPU prior to running this test.

7. Scratch media must be mounted in drives to be tested before starting the diagnostic.

8. ZRKJ??.BI?, ZRKK??.BI?, ZRKL??.BI?, and ZRKI??.BI? (if needed) should be run on subsystem before running this test.

9. ZRKJ??.BI? should be run on the sybsystem before running this test.

10. ZRKJ??.BI? and ZRKK??.BI? should be run on the subsystem before running this test.

11a. A wraparound test connector must be installed to run this test. The connector is not available from stock. The F.E. must make one up himself. The following instructions (excerpted from Tech Tip PDP-11/03 TT-11) tell how this is done. The following items are required:

1 Berg connector	(12-10918-15)
4 Berg pins	(12-10089-07)
#22 wire	(90-07350-00).

Crimp a short length of wire between two Berg pins. Make up two sets of these. Install one set from pin F to pin J, and one set from pin E to pin M of the Berg connector.

11b. To completely exercise the modem control portion of the DLV11-E, a special wraparound connector (H315) must be installed on the modem end of the I/F cable. This test connector loops back certain control lines as well as the data lines.

12. The test has baud rate dependent configuration requirements.

Baud Rate	No. of Stop Bits	No. of Bits
110	2	8
All others	1	8

13. Requires BC08R test cable for full test of module's data lines.

14. ZRXB??.BI? should be run on the subsystem before running this test.

15. If a REV11 is in the system, DMA refresh must be disabled and CPU refresh must be enabled.

16. H315A connector required for external loopback testing.

17. If customer hardware is connected to the KWV11 which could inject signals on ST1, ST2 or slave in inputs, it must be disconnected from the inputs.

18. All switches in switch pack 2 should be left off unless you are instructed otherwise.

19. I/O signal test no. 1 (ST1 in, ST2 out); install a jumper between J1-SS (ST2 out) to J1-VV (ST1 in).

Switch Pack 2

Switch	State
1	Off
2	On
3	Off
4	Off
5	On
6	On
7	Not used.

Use a program starting address of 210.

20. I/O signal test no. 2 (clock overflow tests); install a jumper between J1-RR (clock overflow) to J1-TT (ST2 in).

Switch Pack 2

Switch	State
1	Off
2	Off
3	Off
4	On
5	Off
6	On
7	Not used.

Use a program starting address of 214.

21. I/O signal test no. 3 (ST1 out, ST2 in); install a jumper between J1-UU (ST1 out) to J1-TT (ST2 in).

Switch Pack 2

Switch	State
1	Off
2	Off
3	Off
4	On
5	On
6	On
7	Not used.

Use a program starting address of 220.

22. Test may be run with a "known good module" in the system for comparison. The good module should be located second (electrically) on the bus, with a cable connecting it and the module under test.

"known good module" address - 760160
"known good module" vector - 660

23. Starting restrictions:

If a free-running clock, such as 60 Hz from the power supply, is attached to the BEVNT bus line on REV C/D/E systems, an interrupt to location 100 will occur when using the ODT "G" and "L" commands. This will happen prior to the program executing the first instruction. This program cannot disable the BEVNT bus line by inhibiting interrupts.

User systems requiring a free-running clock attached to the BEVNT bus line can temporarily avoid this situation by setting the PSW to 200, loading the PC with the starting address, and then using the "P" command, instead of using the starting address and the "G" command.

Before using the "L" command, the PSW can be set to 200 to inhibit interrupts after loading the absolute loader.

24. Possible program bombs:

The first two tests check to see if the IBV11-A responds to the address the program thinks it is at. If not, a bus error occurs.

Bus errors may alter the preset contents of location 4 before the trap is executed. Program control may be transferred to an area of the program which is not set up to handle the trap. Or, control may be passed to some totally unknown and irrelevant piece of code residing accidently in memory. If this occurs, the program will most probably bomb, and it may also overwrite parts of itself. If this occurs, the program must be reloaded before proceeding.

25. If the IB-bus cable is not removed from the module under test, any errors which are detected could be from some device out on the IB-bus and not necessarily from the IBV11-A.

26. If run in staggered maintenance mode, an H329 staggered turn-around connector is required.

27. If run in external maintenance mode, an H325 cable turn-around connector is required on all lines which have been selected to be tested.

28. This test assumes that the module under test resides in the same backplane where the line time clock is generated.

29. Test 3 assumes that switch no. 5 of E21 is in the ON position.

30. For the rocker switch test, the operator should specify the configuration for the module under test.

31. VRLA??.BI? should be run on the subsystem before running this test.

32. VRLA??.BI? and ZRLG??.BI? should be run on the subsystem before running this test.

33. A KWV11 programmable line clock is required to run test no. 7.

34. VRLA??.BI?, ZRLG??.BI?, and ZRLH??.BI? should be run on the subsystem before running this test.

35. A KWV11 programmable line clock is required for some tests.

36. VRLA??.BI?, ZRLG??.BI?, ZRLH??.BI?, and ZRLI??.BI? should be run on the subsystem before running this test.

37. VRLA??.BI?, ZRLG??.BI?, ZRLH??.BI?, ZRLI??.BI?, ZRLJ??.BI?, and ZRLN??.BI? should be run on the subsystem before running this test.

38. VRLA??.BI?, ZRLG??.BI?, ZRLH??.BI?, ZRLI??.BI?, ZRLJ??.BI?, ZRLK??.BI, and ZRLN??.BI? should be run on the subsystem before running this test.

39. VRLA??.BI?, ZRLG??.BI?, ZRLH??.BI?, ZRLI??.BI?, and ZRLJ??.BI? should be run on the subsystem before running this test.

40. A KWV11 programmable line clock is required for tests 1 and 4.

41. To check the power fail circuitry, nonvolatile memory must be in the first 4K of memory.

42. Power up option no. 1 should be selected on the CPU module for power fail testing.

43. The module should be in the standard factory configuration.

    jumpers in: W1-W5, W7, W8, W11, W13-W15
    jumpers out: W6, W9, W10, W12

44. If the test is to be run in all address modes, then an extender card and a special test cable (17-00124-01) are required.

45. The exerciser may be run with the module in address modes 1 or 3 only.

46. This test may be run only if RAM is present on the board.

47. All channels must be configured to the same bit-word length.

48. A wraparound connector (H3270) is required for the data wraparound tests for each of the lines to be tested.

49. Requires a BC05W-02 cable to be installed between the Berg connectors. The cable should have a half twist in it.

50. JKDB??.BI? should be run on the first 16K of memory before running this test.

51. JKDC??.BI? should be run on the module before running this test.

Media Availability

No.	Media Package Identifier	Title	Notes	Media PNs	Documentation Media Kit PNs
1	CZZGG??	DXDP+ 7 DEC/X11 EXEC 1	1	AS-9645?-M?	ZJ271-RY
2	CZZGL??	DXDP+ 12 RC,RF,RK11		AS-9650?-M?	
3	CZZGO??	DXDP+ 15 RX11 DIAG		AS-9653?-M?	
4	CZZGY??	DXDP+ 25 LSI FLP 1	1	AS-9663?-M?	ZJ271-RY
5	CZZGZ??	DXDP+ 26 DEC/X11 EXEC 2	1	AS-9664?-M?	ZJ271-RY
6	CZZHD??	DXDP+ 30 DEC/X11 EXEC 3	1	AS-9668?-M?	ZJ271-RY
7	CZZHE??	DXDP+ 31 LSI FLP 2	1	AS-9669?-M?	ZJ271-RY
8	CZZHG??	DXDP+ 33 LSI FLP 3	1	AS-9671?-M?	ZJ271-RY
9	CZZHQ??	DXDP+ 43 LSI FLP 4	1	AS-C638?-M?	ZJ271-RY
10	CZZHZ??	DXDP+ 52 RL02 DIAG no. 1	1	AS-F547?-M?	ZJ271-RY
11	CZZID??	DXDP+ 56 RL02 DIAG no. 2	1	AS-F753?-M?	ZJ271-RY
12	CZZIH??	DXDP+ 60 LSI FLP 5	1	AS-F804?-M?	ZJ271-RY
13	CZZMC??	DYDP+ 3 LSI-11 no. 1	2	BA-F021?-M?	ZJ271-RX
14	CZZMD??	DYDP+ 4 DEC/X11 no. 1	2	BA-F022?-M?	ZJ271-RX
15	CZZMT??	DYDP+ 20 LSI-11 no. 2	2	BA-F048?-M?	ZJ271-RX
16	CZZMU??	DYDP+ 21 DEC/X11 no. 2	2	BA-F049?-M?	ZJ271-RX
17	CZZMZ??	DYDP+ 26 LSI-11 no. 3	2	BA-F558?-M?	ZJ271-RX
18	CZZZD??	LSI-11 DKDP + Diagnostic PKG		AN-9696?-M?	ZJ278-RE
19	CZZLA??	DLDP+ (RL01) Diagnostic PKG no. 1		AX-E380?-M?	ZJ278-RQ
20	CZZLN??	DLDP+ (RL02) Diagnostic PKG		BC-F916?-M?	ZJ278-RH

Notes

1. Documentation/media kit ZJ271-RY contains all of these floppies as well as all of the applicable documentation.
2. Documentation/media kit ZJ271-RX contains all of these floppies as well as all of the applicable documentation.

APPENDIX B
FLOATING ADDRESSES / VECTORS

FLOATING ADDRESSES

The conventions for the assignment of floating addresses for modules on the LSI-11 bus are the same as UNIBUS devices. UNIBUS devices are used to explain the ranking sequence.

The floating-address convention used for communications and for other devices that interface with the PDP-11 series of products assigns addresses sequentially starting at 760 010 (or 160 010) and proceeds upward to 763 776 (or 163 776). For the sake of compatibility with UNIBUS conventions, addresses are expressed as consisting of 18 bits (7XX XXX) rather than 16 bits (1XX XXX).

Floating addresses are assigned in the following sequence.

Rank	UNIBUS Device	LSI-11 Device
1	DJ11	
2	DH11	
3	DQ11	
4	DU11	DUV11
5	DUP11	
6	LK11A	
7	DMC11	
8	DZ11	DZV11
9	KMC11	
10	RL11 (extras)	RLV11 (extras)

FLOATING VECTORS

The conventions for the assignments of floating vectors for modules on the LSI-11 bus will adhere to those established for UNIBUS devices. UNIBUS devices are used to explain the priority ranking for floating vectors and are included in the subsequent table of trap and interrupt vectors as a guide for the user.

The floating-vector convention used for communications and for devices that interface with the PDP-11 series of products assigns vectors sequentially starting at 300 and proceeding upward to 777. (Some LSI-11 bus modules, such as the DLV11 and DRV11, have an upper vector limit of 377.) The following table shows the sequence for assigning vectors to modules. It can be seen that the first vector address, 300, is assigned to the first DLV11 in the system. If another DLV11 is used, it would then be assigned to all the DLV11s (up to a maximum of 32); addresses are then assigned consecutively to each unit of the next highest-ranked device (DRV11 or DLV11-E, and so forth), then to the other devices according to their rank.

Ranking for Floating Vectors
(Start at 300 and proceed upward.)

Rank	UNIBUS	LSI-11 Bus
1	DC11	
2	KL11, DL11-A, -B	DLV11, -F, -J
3	DP11	
4	DM11-A	
5	DN11	
6	DM11-BB	
7	DR11-A	DRV11-B
8	DR11-C	DRV11
9	PA611 Reader	
10	PA611 Punch	
11	DT11	
12	DX11	
13	DL11-C, -D, -E	DLV11-E
14	DJ11	
15	DH11	
16	GT40	
17	LPS11	
18	DQ11	
19	KW11-W	KWV11
20	DU11	DUV11