CHK11

REFERENCE MANUAL

DEC-10-CKRMA-A-D

digital equipment corporation · maynard. massachusetts

First Printing April 1976

CONTENTS

TABLES

PREFACE

This manual is intended for those who will be loading PDP-11 communications systems such as the DAS44, DAS78, DN80, DN81, DN82, DN85 and DN87. It provides the information required to evaluate the information displayed by the CHK11 hardware test software.

1.0 INTRODUCTION

CHK11 is a hardware test module for PDP-11 communications systems such as the DAS44, DAS78, DN80, DN81, DN82, DN85 and DN87. When the system program for one of these machines is started, CHK11 is brought in to perform an initial hardware survey. This module makes sure the devices and memory of the system are functioning correctly. CHK11 does not perform a total system diagnostic check, but rather checks for the most common problems affecting PDP-11 communications systems.

During execution, CHK11 prints the names and quantities of each device type present in the system. All CHK11 test information is printed on the PDP-11 communications system's console terminal (CTY). If the PDP-11 communications system does not have a console terminal, CHK11 displays any errors as codes in the data lights. In such cases, additional information can be obtained by connecting a terminal to the PDP-11. A sample CHK11 printout for a DN82 node is:

```
INITIALIZING DN82 V7
    1 CR11
    1 LP11
    2 DM11BB'S
    2 DH11'S
    1 DQ11
RESTARTING DN82 SMD22(22)
```

If a problem is detected by CHK11, the error information is printed in the following format:

```
? [device-name #number (ADR= address)]
    ERROR AT PC listing-address
        message-describing-problem
        REG/ADR=address   GD=expected   BD=received   XOR=bits in
                in question       value          value          question
        [FATAL ERROR]
```

If the problem is a device error, the device name, number and address are printed. Device numbers are sequential, starting with zero (0). The address printed is the first address of the device. The listing-address informs the user where in the CHK11 source listing to look for the error.

Next, CHK11 prints a brief message describing the error. The line following the message gives the actual address in question, along with the value CHK11 expected to find in that location, the value CHK11 actually did find, and the exclusive OR (XOR) between the expected and actual values. The XOR reveals which bits in the location differ between expected and actual values.

If CHK11 is unable to continue, it prints the FATAL ERROR message and halts. The operator of the system must evaluate the problem, correct it, and reboot the system. Examples of fatal errors are memory errors or problems with the KW11.

When CHK11 halts on a fatal error, a stop-code is displayed in the data lights on the console. (Obviously, a problem with the CTY cannot be printed on the CTY.) Table 1 lists the error stop-codes and their meanings.

Table 1
CHK11 Stop Codes

STOP CODE	MEANING
1	Time out or bus error (trap to address 4)
2	DL10 error
5	No console terminal
6	Memory error
7	KW11 error
12	Other CHK11 error

To display the address of the error in the data lights, press CONTINUE after the machine halts.

To restart CHK11, press CONTINUE a second time.

If CHK11 completes the tests with no discovered errors, it transfers control to the PDP-11 communications system code and the system is then running.

If errors are detected, CHK11 prints:

? ERRORS DETECTED - DO YOU WANT TO PROCEED (Y OR N)?

Any response other than "Y" causes CHK11 to halt.

To execute the PDP-11 communications software for purposes of testing, type a "Y". CHK11 then prompts to verify that response with the question:

ARE YOU SURE?

A "Y" response to this question causes control to pass to the PDP-11 communications system program. Any response to this question other than "Y" causes CHK11 to halt.

NOTE
Under certain conditions, although an error is reported by CHK11, the PDP-11 communications system may still be partially functional. If the limited functioning is adequate for user needs, the operator may use the above mechanism to proceed.

2.0 BIT CLEAR AND SET TEST

CHK11 uses the Bit Clear and Set Test to test those bits in a device register that can be both written and read.

CHK11 first attempts to clear all the READ/WRITE bits that are to be tested in a register. It then checks to determine if all those bits actually did clear. If any tested bit is not clear, CHK11 prints an error message. For example:

```
? LP11 #0 (ADR= 177514)
    ERROR AT PC 15352
        BIT DID NOT CLEAR
        REG/ADR = 177514 GD = 0 BD = 100 XOR = 100
```

In the example above, the problem occurred with the register of device LP11 number 0. The address of the first device register is 177514. The listing address of the error is 15352. The error message indicates that a bit did not clear. The register under test was 177514. The expected content of that register was zero, the value found in that register was 100 (octal). Therefore, CHK11 could not clear bit 6 in the LP11 status register. This bit is shown by the XOR value 100.

After the register is known to be cleared, CHK11 sets and checks each bit in the register individually. Each bit is set and tested to make sure it is set. If set, the bit is then cleared, and checked to make sure that it cleared. If any bit is not set when tested, CHK11 prints an error message. For example:

```
? DQ11 #0 (ADR= 177264)
    ERROR AT PC 15376
        BIT DID NOT SET
        REG/ADR = 177264 GD = 100 BD = 0 XOR = 100
```

A bit in the DQ11 failed to set. The DQ11 first device address is 177264. The listing address of the error is 15376. The error message indicates that a bit did not set. The line following it indicates that the status register in question is at location 177264. The GD value is the expected value. The BD value is the actual value. The XOR value indicates that the bit that could not be set was bit 6.

If any bit could not be cleared after being set, CHK11 prints an error message. The XOR value in this message indicates the bit that was set, but not cleared. For example:

```
? CR11 #0 (ADR= 177160)
    ERROR AT PC 15422
        BIT DID NOT CLEAR
        REG/ADR = 177160 GD = 0 BD = 2 XOR = 2
```

Bit 1 in the CR11 status register could not be cleared. The location of that register is 177160.

3.0 INTERRUPT TEST

CHK11 performs the Interrupt Test to verify that the various devices interrupt correctly.

The test initially checks to make sure that the device interrupts by establishing a legitimate interrupt condition in the device register(s) and initializing an interrupt timer. CHK11 then lowers the Processor Interrupt (PI) level to zero. If the device does not interrupt within the allotted test time, a time-out error occurs. For example:

```
? DN11 #0 (ADR = 175200)
    ERROR AT PC 16244
        DID NOT INTERRUPT
```

The DN11 status register is 175200. The listing address of this error is shown to be 16244. The error message indicates that the device did not interrupt.

If the device does interrupt, CHK11 saves the device interrupt level and verifies that the interrupt was directed to the correct vector address. If the interrupt was to an incorrect vector address, an error message is printed. For example:

```
? KW11 #0 (ADR = 171200)
    ERROR AT PC 16274
        INTERRUPTED TO WRONG VECTOR
        ADR/REG = 171200 GD = 240 BD = 300 XOR = 140
```

The listing address is 16274. The first hardware address of the KW11 is 171200. CHK11 then prints an error message. The device address in which the interrupt bits were set is the ADR/REG value 171200. The GD value indicates the vector address to which the interrupt should have trapped. The BD value is the actual address trapped to. The XOR provides the bits that differ in the vector addresses.

CHK11 then tests the interrupt conditions for the device by individually setting interrupt enable bits and verifying that an interrupt occurs when each related interrupt condition is set. If the interrupt traps to the wrong vector address at any point in this test, the above error message is displayed. After each interrupt occurs, CHK11 verifies that the device trapped to the same PI level as it did on the first interrupt. If the PI level differs, an error message is printed. For example:

```
? DH11 #0 (ADR = 175240)
    ERROR AT PC 16354
        INTERRUPTED TO DIFFERENT PI LEVEL
        ADR/REG = 175240 GD = 240 BD = 200 XOR = 40
```

The first hardware register for the device DH0 is 175240. The listing address of the error is 16354. CHK11 then prints an appropriate error message. The value 175240 on the next line specifies the device address in which the interrupt bits were set. The GD value indicates the device's first interrupt level (bit locations 5-7). The BD value is the device's current priority level. The XOR displays the difference in priority levels.

After verifying that the proper interrupts occur with the interrupt enable bit set, CHK11 makes sure that an interrupt does not happen if that bit is cleared. This is done by setting the interrupt condition bit, lowering the PI level to zero and waiting a specified amount of time for an interrupt to occur. If an interrupt occurs, an error message is printed. For example:

```
? DN11 #3 (ADR = 175220)
    ERROR AT PC 16442
        INTERRUPTED WITHOUT INTERRUPT ENABLED
```

If no errors are discovered by these interrupt tests, CHK11 assumes that the interrupts are working correctly.

4.0 MEMORY TEST

This test checks to verify that all bits located in core, except this routine, can be read and written by setting a bit, reading it, and then rotating the pattern. (This is called a sliding bit pattern.) If any bit cannot be written or read, an error exists. An error in memory is fatal and the machine halts with a stop-code of 6 displayed in the console data lights. For example:

```
? MEM ERR
    ERROR AT PC 12242
        REG/ADR = 20000 GD = 1 BD = 0 XOR = 1
        FATAL ERROR
```

The listing address of this error is 12242. The address 20000 on the next line is the word in memory under test. The GD value is what CHK11 expected to find in that location. The BD value is what was in that location. The bit in question is shown by the XOR value.

5.0 DETERMINING THE DL10 BASE ADDRESS

In addition to testing the hardware, CHK11 also determines the DL10 Base Address. The DL10 Base Address must be a location that is a multiple of 2000. The following algorithm is used.

CHK11 evaluates the first location following the CHK11 code that is a multiple of 2000. A PDP-11 BIS instruction is performed on the Clear NXM, Clear Parity Error, Clear Word Count Overflow, and the Clear 11-Interrupt bits in that location. CHK11 then clears that location and tests the contents. If the location does not contain a zero, an error message of the following form is printed:

```
? CAN'T CLEAR DL10 OR MEM
    ERROR AT PC 12244
        ADR/REG = 20000 GD = 0 BD = 1 XOR = 1
```

This error message indicates that the reference in the program listing is address 12244. ADR/REG shows the location that could not be cleared. The GD value is the expected result. The BD value is the actual contents of the location. The XOR indicates the bit(s) in error.

If the location is clear, CHK11 then sets the NXM, Parity Error, Word Count Overflow, and 11-Interrupt bits, and tests those bits. If any of these bits is not set, an error message of the following form is printed:

```
?ERROR AT ADR PC 12326
    DL10 OR MEM ERR
        ADR/REG = 100000 GD = 105200 BD = 5200 XOR = 100000
```

This message indicates that the error occurred at listing address 12326. ADR/REG indicated the location under test. The GD value is the expected value. The BD value is the actual contents of the location. The XOR reveals the bit(s) in error.

If the bits are set properly, CHK11 issues the BIS instruction to clear those bits. The location is then tested and if it contains a zero value, it is the DL10 Base Address. If the location does not contain a zero, CHK11 repeats the procedure using an address which is 2000 words larger than the one just tested. This is repeated using multiples of 2000 until a DL10 Base Address is found or until the memory space is exhausted.

The following sections describe the error messages applicable to the various devices.

6.0 CONSOLE TERMINAL

If there is no console terminal interface, or there is an error in the interface that does exist, a fatal error occurs and the machine halts with a stop-code value of 5 in the console data lights.

7.0 MEMORY ERROR MESSAGE

MEM ERR

During the memory test, the contents read from ADR differ from the expected value. This is a fatal error with a stop-code value of 6. See Section 4.0.

8.0 DL10 OR MEMORY ERROR MESSAGES

CAN'T CLEAR DL10 OR MEMORY

To locate the DL10 base address, CHK11 places 42500 into a location and if the location is the DL10 base address, it is cleared. The following instruction is a CLR which should definitely leave the location zeroed. If the location is not clear, the fatal error message is printed and the machine halts with a stop-code of 2 displayed in the data lights. Section 5.0 describes the test.

DL10 OR MEM ERR

After a location is cleared, the value 105200 is deposited into that address. That location is then tested and if the value was not retained, an error has occurred. This is a fatal error and the machine halts with a stop-code of 2 displayed in the data lights. Section 5.0 describes the test.

9.0 CR11 ERROR MESSAGES

CR11 NOT READY

The Busy Bit in the status register is set. This may indicate a power-off condition. The device cannot be checked.

CR11 TIMED OUT

A read was performed with the interrupt enable set. The error bit or the done bit was not set within the predetermined time limit.

INTERRUPT DID NOT OCCUR

With the interrupt condition on and the interrupt enable set in the device, lowering the priority level to zero did not cause an interrupt to occur. (See Section 3.0.)

INTERRUPTED TO WRONG VECTOR

The device interrupted to the wrong vector address. (See Section 3.0.)

10.0 DH11 ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the DH11 register being tested. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the DH11 register being tested. (See Section 2.0.)

DATA ERROR

While CHK11 was testing the DH11 in loopback, the data received differed from the data transmitted. The ADR/REG value is the line under test. The GD value is the transmitted data. The BD value is the received data. The XOR shows the bits that differed.

DATA ERROR BIT SET

While CHK11 was testing the DH11 in loopback, the Next Received Character register had the DATA OVERRUN bit (bit 14) set, the FRAMING ERROR bit (bit 13) set, or the PARITY ERROR bit (bit 12) set.

ILL XMIT INT

An interrupt occurred to the XMIT vector when the XMIT interrupt bit was not set. The output following this message indicates the line number under test.

ILLEGAL INT

An undetermined interrupt occurred while CHK11 was waiting for a receive or transmit interrupt in the DH11 loopback test.

ILLEGAL LINE NUMBER

An incorrect line number was set in the Next Character Received register. The output following this message indicates the number of the line under test.

INTERRUPT DID NOT OCCUR

With the interrupt condition on and the interrupt enable set in the device, lowering the priority level to zero did not cause an interrupt to occur. (See Section 3.0.)

INTERRUPTED TO DIFFERENT PI LEVEL

The current Processor Interrupt level of the device differs from the first interrupt level. (See Section 3.0.)

INTERRUPTED TO WRONG VECTOR

The device interrupted to the wrong vector address. (See Section 3.0.)

INTERRUPTED WITHOUT INTERRUPT ENABLED

An interrupt occurred when the interrupt bit was set and the interrupt enable bit was not set. (See Section 3.0.)

NO INTERRUPT

With interrupts enabled and the PI level at zero, an interrupt did not occur within the allotted time. The output following this message indicates the line under test.

NOT VALID DATA

The VALID DATA PRESENT bit (bit 15) was not set in the Next Received Character register. The output following this message indicates the line under test.

SILO FULL

With the silo alarm level set to 4, the receiver interrupt bit became set, indicating that the number of characters stored in the silo exceeds the alarm level. The output following this message indicates the number of the line under test.

XMIT NXM

While CHK11 was testing the DH11 in loopback, the NXM bit (bit 10) became set in the System Control Register. The output following this message indicates the line that was under test.

11.0 DL10 ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the DL10 status register beingtested. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the DL10 status register being tested. (See Section 2.0.)

INTERRUPT DID NOT OCCUR

With the interrupt condition on and the interrupt enable set in the device, lowering the priority level to zero did not cause an interrupt to occur. (See Section 3.0.)

INTERRUPTED TO DIFFERENT PI LEVEL

The current Processor Interrupt level of the device differs from the first interrupt level. (See Section 3.0.)

INTERRUPTED TO WRONG VECTOR

The device interrupted to the wrong vector address. (See Section 3.0.)

INTERRUPTED WITHOUT INTERRUPT ENABLED

An interrupt occurred when the interrupt bit was set and the Interrupt Enable bit was not set. (See Section 3.0.)

12.0 DL11 ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the DL11 register being tested. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the DL11 register being tested. (See Section 2.0.)

13.0 DM11BB ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the DM11BB register being tested. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the DM11BB register being tested. (See Section 2.0.)

BUSY DID NOT SET

After CHK11 set the Scan Enable bit, the Busy Bit was tested and found to be cleared.

BUSY DID NOT CLEAR

After CHK11 set the Clear Scan bit and waited an appropriate amount of time, the Busy Bit was found not to be cleared.

CLEAR SCAN ERROR

After CHK11 set the Clear Scan bit in the status register, a bit that should have been cleared was set. The bits that should be cleared are: DONE, Maintenance Mode, Interrupt Enable, Scan Enable, and Line Number Field.

INTERRUPT DID NOT OCCUR

With the interrupt condition on and the Interrupt Enable set in the device, lowering the priority level to zero did not cause an interrupt to occur. (See Section 3.0.)

INTERRUPTED TO DIFFERENT PI LEVEL

The current Processor Interrupt level of the device differs from the first interrupt level. (See Section 3.0.)

INTERRUPTED WITHOUT INTERRUPT ENABLED

An interrupt occurred when the interrupt bit was set and the Interrupt Enable bit was not set. (See Section 3.0.)

14.0 DN11 ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the DN11 register being tested. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the DN11 register being tested. (See Section 2.0.)

INTERRUPT DID NOT OCCUR

With the interrupt condition on and the Interrupt Enable set in the device, lowering the priority level to zero did not cause an interrupt to occur. (See Section 3.0.)

INTERRUPTED TO DIFFERENT PI LEVEL

The current Processor Interrupt level of the device differs from the first interrupt level. (See Section 3.0.)

INTERRUPTED TO WRONG VECTOR

The device interrupted to the wrong vector address. (See Section 3.0.)

INTERRUPTED WITHOUT INTERRUPT ENABLED

An interrupt occurred when the interrupt bit was set and the Interrupt Enable bit was not set. (See Section 3.0.)

15.0 DP11 ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the DP11 register being tested. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the DP11 register being tested. (See Section 2.0.)

INTERRUPT DID NOT OCCUR

With the interrupt condition on and the Interrupt Enable set in the device, lowering the priority level to zero did not cause an interrupt to occur. (See Section 3.0.)

INTERRUPTED TO DIFFERENT PI LEVEL

The current Processor Interrupt level of the device differs from the first interrupt level. (See Section 3.0.)

INTERRUPTED TO WRONG VECTOR

The device interrupted to the wrong vector address. (See Section 3.0.)

INTERRUPTED WITHOUT INTERRUPT ENABLED

An interrupt occurred when the interrupt bit was set and the Interrupt Enable bit was not set. (See Section 3.0.)

16.0 DQ11 ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the DQ11 register being tested. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the DQ11 register being tested. (See Section 2.0.)

CAN'T CLR DATASET FLG

The test program was not able to clear the DQ11 data set flag.

ERR INT

While CHK11 was determining the DQ11 special characters, an interrupt occurred on Vector B.

ILLEGAL INTERRUPT

While CHK11 was determining the DQ11 special characters, an interrupt occurred that was not a special character interrupt.

INTERRUPT DID NOT OCCUR

With the interrupt condition on and the Interrupt Enable set in the device, lowering the priority level to zero did not cause an interrupt to occur. (See Section 3.0.)

INTERRUPTED TO DIFFERENT PI LEVEL

The current Processor Interrupt level of the device differs from the first interrupt level. (See Section 3.0.)

INTERRUPTED TO WRONG VECTOR

The device interrupted to the wrong vector address. (See Section 3.0.)

INTERRUPTED WITHOUT INTERRUPT ENABLED

An interrupt occurred when the interrupt bit was set and the Interrupt Enable bit was not set. (See Section 3.0.)

MORE THAN 4 SPEC CHAR DET

More than four special characters were detected in the DQ11.

SECONDARY REG ERROR

The data loaded into the secondary register does not agree with the data read. ADR/REG indicates the secondary register under test.

SPEC CHAR CODE FIELD 0

A special character interrupt occurred, but the special character code field contains a zero.

17.0 DS11 ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the DS11 register being tested. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the DS11 register being tested. (See Section 2.0.)

18.0 KG11 ERROR MESSAGES

CAN'T LOAD BCC CORRECTLY

The data loaded into the Data Register is not the same as the data read from the BCC register.

INCORRECT CRC

While CHK11 was calculating the Cyclic Redundancy Check (CRC) polynomials, the simulated value differed from the actual value calculated by the KG11.

NOT PRESENT

The KG11 is not connected or it cannot be accessed.

19.0 KW11 ERROR MESSAGES

FAST

A clock tick occurred too soon. This is a fatal error with a stop-code of 7.

INTERRUPT DID NOT OCCUR

With the interrupt condition on and the Interrupt Enable set in the device, lowering the priority level to zero did not cause an interrupt to occur. (See Section 3.0.)

INTERRUPTED TO WRONG VECTOR

The device interrupted to the wrong vector address. (See Section 3.0.)

NOT PRESENT

The KW11 is not present or it is defective. This is a fatal error with a stop-code of 7.

SLOW

There was no response from the KW11 in the allocated time, which is significantly greater than one tick time. This is a fatal error with a stop-code of 7.

20.0 LP11 ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the LP11 status register. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the LP11 status register. (See Section 2.0.)

INTERRUPT DID NOT OCCUR

With the interrupt condition on and the Interrupt Enable set in the device, lowering the priority level to zero did not cause an interrupt to occur. (See Section 3.0.)

INTERRUPTED TO WRONG VECTOR

The device interrupted to the wrong vector address. (See Section 3.0.)

INTERRUPTED WITHOUT INTERRUPT ENABLED

An interrupt occurred when the interrupt bit was set and the Interrupt Enable bit was not set. (See Section 3.0.)

LP11 #N NOT READY

The error bit is set in the LP11 status register.

21.0 MM-11 PARITY OPTION ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the MM-11 status register. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the MM-11 status register. (See Section 2.0.)

INTERRUPT DID NOT OCCUR

With the interrupt condition on and the Interrupt Enable set in the device, lowering the priority level to zero did not cause an interrupt to occur. (See Section 3.0.)

INTERRUPTED TO WRONG VECTOR

The device interrupted to the wrong vector address. (See Section 3.0.)

INTERRUPTED WITHOUT INTERRUPT ENABLED

An interrupt occurred when the interrupt bit was set and the Interrupt Enable bit was not set. (See Section 3.0.)

NOT FOUND

The PDP-11 being tested does not have the required MM-11 Memory Parity Option.

22.0 PA611 ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the PA611 status register. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the PA611 status register. (See Section 2.0.)

23.0 PP11 ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the PP11 status register. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the PP11 status register. (See Section 2.0.)

INTERRUPT DID NOT OCCUR

With the interrupt condition on and the Interrupt Enable set in the device, lowering the priority level to zero did not cause an interrupt to occur. (See Section 3.0.)

INTERRUPTED TO WRONG VECTOR

The device interrupted to the wrong vector address. (See Section 3.0.)

INTERRUPTED WITHOUT INTERRUPT ENABLED

An interrupt occurred when the interrupt bit was set and the Interrupt Enable bit was not set. (See Section 3.0.)

24.0 PR11 ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the PR11 status register. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the PR11 status register. (See Section 2.0.)

INTERRUPT DID NOT OCCUR

With the interrupt condition on and the Interrupt Enable set in the device, lowering the priority level to zero did not cause an interrupt to occur. (See Section 3.0.)

INTERRUPTED TO WRONG VECTOR

The device interrupted to the wrong vector address. (See Section 3.0.)

INTERRUPTED WITHOUT INTERRUPT ENABLED

An interrupt occurred when the interrupt bit was set and the Interrupt Enable bit was not set. (See Section 3.0.)

25.0 TC11 ERROR MESSAGES

BIT DID NOT CLEAR

A bit did not clear in the TC11 register being tested. (See Section 2.0.)

BIT DID NOT SET

A bit failed to set in the TC11 register being tested. (See Section 2.0.)

INTERRUPT DID NOT OCCUR

With the interrupt condition on and the Interrupt Enable set in the device, lowering the priority level to zero did not cause an interrupt to occur. (See Section 3.0.)

INTERRUPTED TO DIFFERENT PI LEVEL

The current Processor Interrupt level of the device differs from the first interrupt level. (See Section 3.0.)

INTERRUPTED TO WRONG VECTOR

The device interrupted to the wrong vector address. (See Section 3.0.)

INTERRUPTED WITHOUT INTERRUPT ENABLED

An interrupt occurred when the interrupt bit was set and the Interrupt Enable bit was not set. (See Section 3.0.)