PDP 1

SUPPLEMENT

(PDP-1D-45)

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

PDP-1D-45
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FOREWORD

This supplement describes special instructions added to PDP-1D-45 at Bolt Beranek and Newman. They are grouped as follows:

Memory Reference Instructions

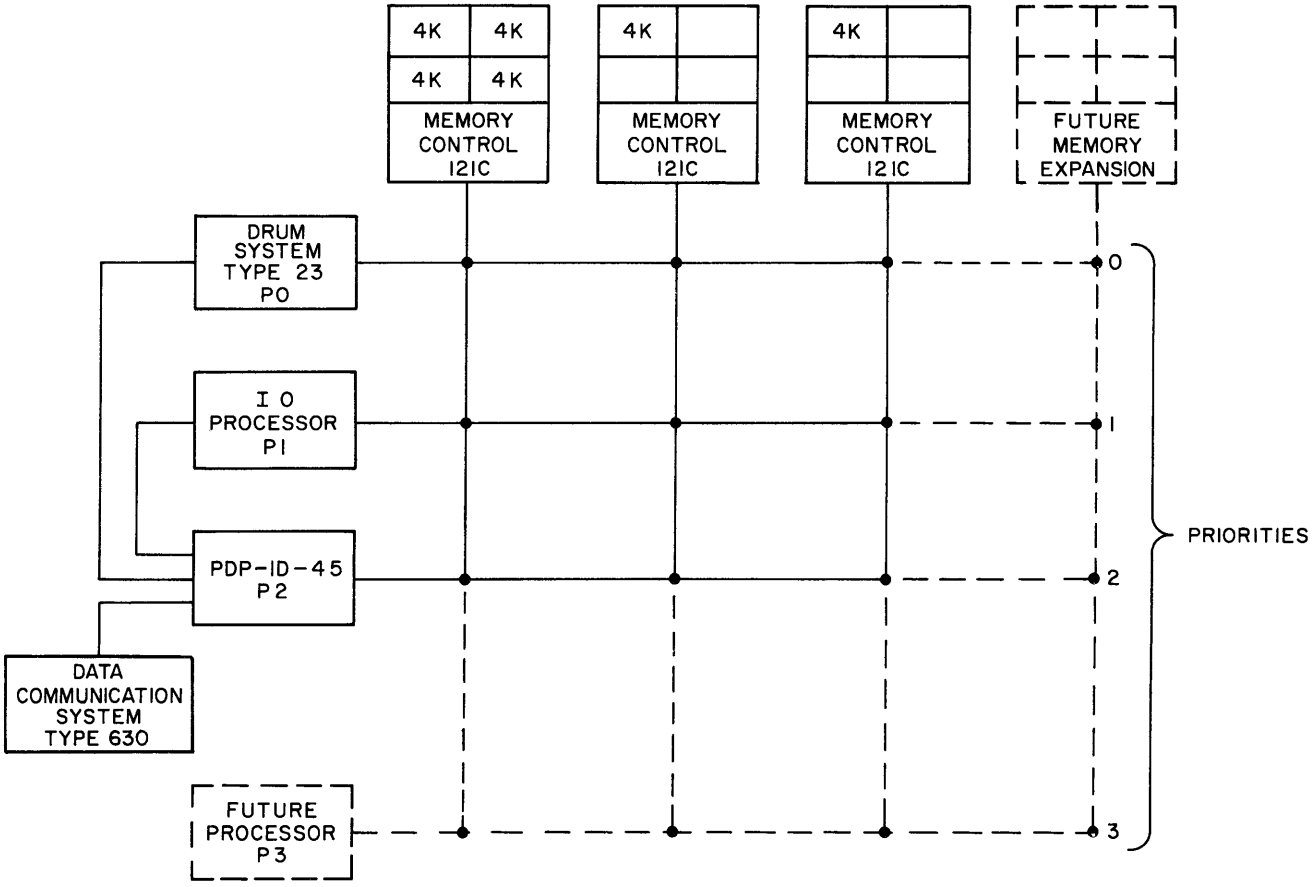
- Load Character (LCH)
- Deposit Character (DCH)
- Twos Complement Add (TAD)

The Skip Group

The Special Operate Group

The Input-Output Transfer Group

CONTENTS



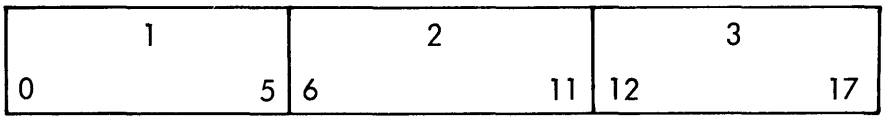
PDP-ID-45 SYSTEM

MEMORY REFERENCE INSTRUCTIONS

LCH - Octal Code 12 - Load accumulator with a character from memory.

DCH - Octal Code 14 - Deposit a character from accumulator in memory.

Each of these instructions is interpreted as being deferred, hence requiring three memory cycles for execution. The MB and AC are divided into three sections of six bits each. Bits 0-5 = character one (1), bits 6-11 = character two (2), and bits 12-17 = character three (3).



The instructions are sub-decoded from MB bits 0 and 1 during the defer cycle. MB bits 0 and 1 are placed in the load-deposit register (LD) and decoded:

Octal Code 12 and LD - 01 = LC1 - Load character one loads accumulator from memory bits 0-5 and places in accumulator bits 0-5. (AC_{0-5})

Octal Code 12 and LD - 10 = LC2 - Load character two loads accumulator from memory bits 6-11, and shifts into AC bits 0-5.

Octal Code 12 and LD - 11 = LC3 - Load character three loads accumulator from memory bits 12-17, and shifts into AC bits 0-5.

Octal Code 14 and LD - 01 = DC1 - Deposit character one deposits accumulator bits 0-5 in memory bits 0-5.

Octal Code 14 and LD - 10 = DC2 - Deposit character two deposits accumulator bits 0-5 in memory bits 6-11.

Octal Code 14 and LD - 11 = DC3 - Deposit character three deposits accumulator bits 0-5 in memory bits 12-17.

LCH

The registers below show a single step sequence through the LCH instruction if 100_8 is the starting location, and it contains a 12_8 to address 1000_8. The LCH instruction automatically forces a defer cycle. During the defer cycle, the memory address (MA) contains 1000_8, and the contents of the MB contain a 01 in the XX position and 2000_8 in the address portion of the

MB. During cycle one, 2000_8 would be the address. If the MB at this time is assumed to contain A, B, and C, the character A is transferred into the accumulator and the remaining 12 bits are cleared as shown in Figure a. During the defer cycle, if the XX portion of the MB contains 10, the character is transferred into the accumulator and the last 12 bits are cleared as shown in Figure b. If the XX portion of the MB contains 11 during the defer cycle, the results would appear as shown in Figure c.

CYCLE ZERO

MA

000	001	000	000

MB

001	010	001	000	000	000

DEFER CYCLE

001	000	000	000

XX0	000	010	000	000	000

CYCLE ONE

010	000	000	000

A		B		C	
110	001	110	010	110	011

ACCUMULATOR

Figure a

A					
110	001	000	000	000	000

Figure b

B					
110	010	000	000	000	000

Figure c

C					
110	011	000	000	000	000

The LCH instruction clears AC bits 6-17 and leaves the single character in AC bits 0-5.

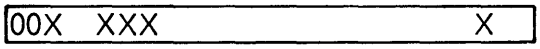
XXX	XXX	000	000	000	000

LCH Octal Code 13

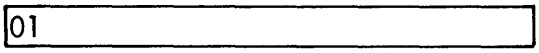
001	01	1	

When the defer bit is a 1 during cycle zero, it sets a one to the increment flip-flop (INC) placing the instruction in the automatic increment mode. In the defer cycle, this takes the first two bits of the MB and effectively adds one (+1) to them. The first time this is used or to enter the automatic mode, the first two bits of the MB should be zeros as the incrementing takes place before the character handling cycle (cycle one).

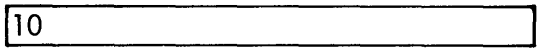
When entering the defer cycle if the address contains a:



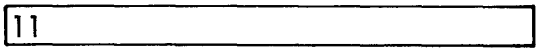
It is incremented to contain:



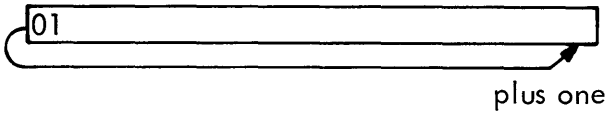
If entered with a 01, it is incremented to:



A 10 is incremented to a:



In the last situation, an 11 causes the character bits to be forced to a 01 and the address portion of the MB to be incremented by one.



Summary: In the automatic mode a sequence performs as follows:

00 - Loads character one
01 - Loads character two
10 - Loads character three
11 - Increments the address (+1) and loads character one in the new address
01 - Character two
10 - Character three
11 - Plus one to address and loads character one in new address
01 - Character two
10 - Character three
11 - Plus one to address and loads character one in new address

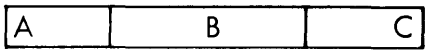
NOTE: If the automatic mode is entered with a 01 in the first two bits of the memory location brought out during the defer cycle, the first character is skipped.

If a 00 is used in the non-automatic instruction, it is interpreted as a LC1 (01) and loads the accumulator from memory bits 0-5.

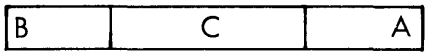
In the automatic mode a mid-instruction break is not allowed between the defer cycle and cycle one. (No sequence breaks can occur between the defer cycle and cycle one).

DCH Octal Code 14

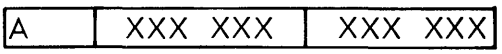
Assuming a sequence of cycles as used in the LCH instruction, if the accumulator contains a series of characters thus:



and the memory location addressed during the defer cycle contains a DC1 (01) in the first two bits, at the end of cycle one the AC would contain:

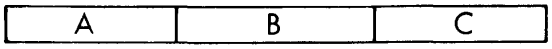


The MB:



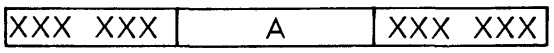
The X's indicate the information originally contained here remains unchanged.

If the memory location addressed during the defer cycle contains a DC2 (10), and the AC initially contains

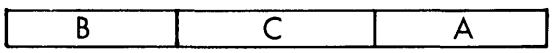


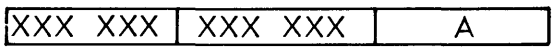
The result in the AC would be

In the MB



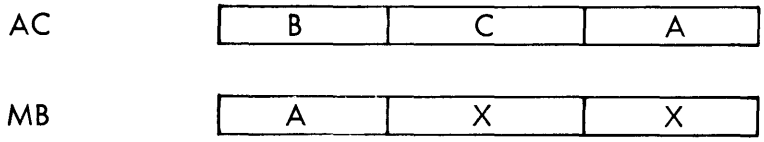
A DC3 (11) provides the following results in the AC and MB if the AC initially contains the ABC.

AC 

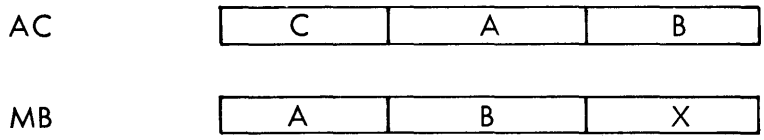
MB 

The following is the result left in the AC and MB if a sequence of DCH instructions is used (non-automatic) and the AC initially contains an ABC in that order:

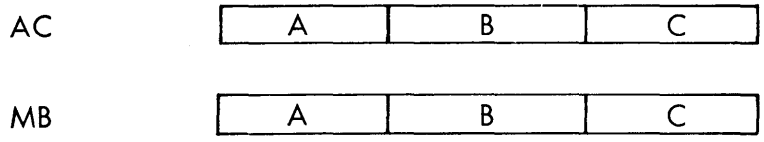
DC1



DC2



DC3



Summary: The DCH instruction always takes the character that is in the first six bits of the AC and places it in the character position designated by the first two bits decoded in the defer cycle: first character to first position, first character to second position, or first character to third position.

DCH Octal Code 15

The DCH instruction, using the indirect address bit (bit 5) of the word as a 1, sets the INC flip-flop and during the defer cycle increments the sub-instruction through the same sequence as shown for LCH. The automatic mode should be entered with a 00 in the location addressed in the defer cycle. (Reference from AC to MB)

DCH 00 - Deposits first character in first position.
DCH 01 - Deposits first character in second position.
DCH 10 - Deposits first character in third position.
DCH 11 - Increments the address and deposits the first character in the first position of the new address.

If the alphabet were typed in by a program sequence it might resemble this:

```
Start    cla V clf        /clear accumulator and flag 1
         szf i (1)        /listen loop
         jmp.-1
         tyi              /bring in typed character
         rcr (6)          /move from I/O to AC
         sad (77)         /compare for end character (77)
         hlt
         dch i store
         jmp start
```

The MB storage locations would be packed thus:

1	A	B	C
2	D	E	F
3	G	H	I
4	J	K	L
5	M	N	O
6	P	Q	R
7	S	T	U
10	V	W	X
11	Y	Z	

Summary: The DCH instruction deposits the accumulator bits 0-5 into the character location of the memory buffer specified by the bits 0, 1 of the location addressed in the defer cycle, and rotates the next character or that character contained in accumulator bits 6-11 into accumulator bits 0-5 so that it might be deposited in memory on the next use of this same DCH instruction.

If the automatic mode is entered with other than a 00, a character is skipped. A 00 used in the non-automatic mode is interpreted as a 01.

TAD Octal Code 36

TAD - 2's complement add

The state of the link is sensed, and if a ONE, one is added to the AC (+1 to AC). The C(Y) are then added to the C(AC). The result is left in the AC and the original C(AC) are lost. The C(Y) are unchanged. A carry out of bit 0 is retained in the link flip-flop.

THE SKIP GROUP

644000	SNI	Skip on non-zero I/O Tests the I/O register for the presence of a one. Skips the next instruction in sequence if any of the I/O bits is a one.
654000	SZI	Skip on zero I/O Tests the I/O register for the all-zero condition. Skips the next instruction in sequence if it exists.
760020	LIA	Load I/O register from AC Loads the I/O register from the accumulator
760040	LAI	Load accumulator from I/O Loads the accumulator from the I/O register
760060	SWP	Exchange AC and I/O Places the original contents of the AC into the I/O and the original contents of the I/O into the AC
770000	CMI	Complement the I/O Is the logical NOT of the contents of the I/O register

THE SPECIAL OPERATE GROUP

The special operate group of instructions is a new set of microprogram instructions. It uses octal code (74). Execution time is 5 microseconds.

The ring mode is also handled by the special operate group. The ring mode flip-flop (RNG) is set, cleared, or sampled with the program flag instructions. Its condition is transferred to I/O bit 11, and it can be set by the condition of I/O bit 11.

Ring mode is the condition whereby the address portion of the word can be caused to loop repetitively over a section of memory. Ring mode is an eight location loop, starting with the three least significant bits in the address portion of the word. It is indexed to seven (111_2) and then back to zero (000_2). See figure at end of SPC group on page 11.

Three instructions are affected by the ring mode: the load or deposit a character (LCH + DCH); index a character (IDC); and index the accumulator (IDA). Ring mode does not affect the add or normal index instructions (ADD or IDX). Setting, clearing, or sampling of the RNG flip-flop can be thought of as program flag zero.

The link flip-flop has been added to the accumulator to receive the carry out of AC_0 in 2's complement add (TAD). The link flip-flop is placed in I/O bit 10 when transferring the contents of the program flags to the I/O. It is set when transferring the contents of the I/O to the program flags by the condition of I/O bit 10.

Event Times

Event Time 1	SCI	SCF	CLL	SZL
Event Time 2	SCM	IFI	IIF	
Event Time 3	IDA	CML		
Event Time 4	IDC			

Bit Configuration

5	6	7	8	9	10	11	12	13	14	15	16	17
Reverse Skip	IIF	IFI	IDC	IDA	SCM	SCI	SCF	SZL	CLL	CML	X	X

744000 IIF

Inclusive OR of the I/O from flags. Forms the inclusive OR of the link, RNG, and program flags 1 through 6 in I/O register bits 10 through 17

- Link - I/O_{10}
- Ring Mode - I/O_{11}
- Program Flag 1 - I/O_{12}
- Program Flag 2 - I/O_{13}
- Program Flag 3 - I/O_{14}
- Program Flag 4 - I/O_{15}
- Program Flag 5 - I/O_{16}
- Program Flag 6 - I/O_{17}

If used with SCI, the I/O is cleared prior to readin.

742000 IFI

Inclusive OR of the flags from I/O. Forms the inclusive OR of I/O register bits 10-17 and leaves in the link, RNG, and program flags 1 through 6 respectively.

I/O_{10} = Link
I/O_{11} = Ring Mode
I/O_{12} = Program Flag 1
I/O_{13} = Program Flag 2
I/O_{14} = Program Flag 3
I/O_{15} = Program Flag 4
I/O_{16} = Program Flag 5
I/O_{17} = Program Flag 6

741000 IDC

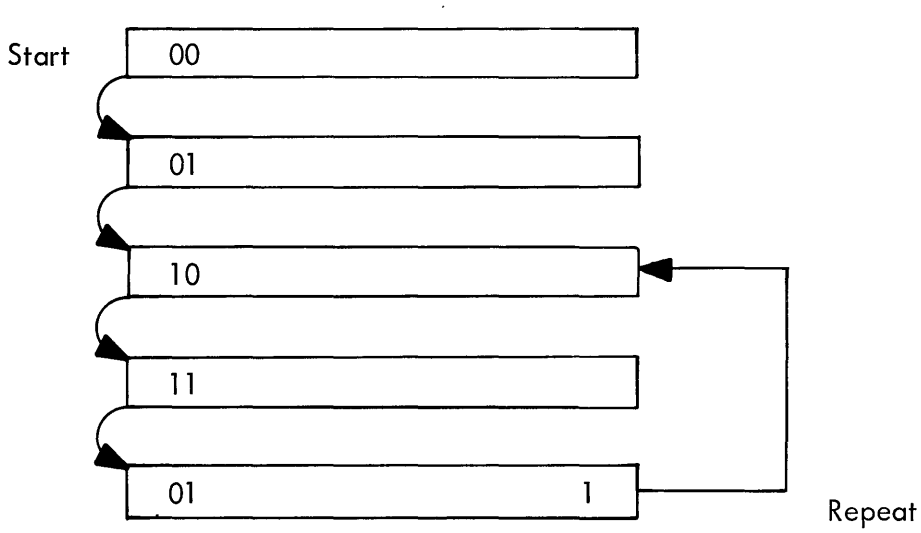
Index character

Indexes bits 0 and 1 of the AC. Operates as a pointer word for the LCH or DCH instructions

$AC_{0-1} \neq$ to 11 - $\xrightarrow{/+1}$ to AC_1

AC_{0-1} = to 11 - $\xrightarrow{/+1}$ to AC_0. The end around carry then causes the address portion of the word to be indexed.

See figure below.



740400	IDA	Index Accumulator, Adds one to the contents of the AC (no effect on MB).
740200	SCM	Special Complement Complements the accumulator and adds one to the accumulator if the link bit was a one. (Does not perform the 2's complement in itself.) ANDed with IDA the 2's complement — complement of a number is obtained.
740100	SCI	Special Clear I/O Clears the I/O register at the first event time.
740040	SCF	Special Clear Flags Clears the link, RNG and the six program flags.
740020	SZF	Skip on zero link Skips the next instruction in sequence if the link is a zero. 750020 will skip the next instruction in sequence if the link is a one.
740010	CLL	Clear Link Clears the link flip-flop at event time one.
740004	CML	Complement Link Forms the logical negation of the link. If a one it is changed to a zero. If a zero it is changed to a one.

RNG

Address portion of MB

XXX	XXX	XXX	000
			001
			010
			011
			100
			101
			110
			111
XXX	XXX	XXX	000

.
.
.

IN/OUT TRANSFER GROUP

Memory and Processor Control IOT's

720011	ERG	Enter Ring Mode
720010	LRG	Leave Ring Mode
720064	LRM	Leave restrict mode
720065	ERM	Enter restrict mode
720066	RNM	Rename memory
720067	RSM	Reset memory banks

Miscellaneous Processor IOT's

72XX32	RCK	Read clock
72XX35	CTB	Clear trap buffer
72XX17	RRO	Rem-rand out
72XX37	RRI	Rem-rand in

Type 23 Drum IOT's

72XX61*	DIA	Drum initial address
72XX62*	DWC	Drum word count
720063*	DCL	Drum core location
722061	DBA	Drum break address
722062	DRA	Drum request address

Data Communication System Type 630

720022	RCH	Receive a character
721022	RCR	Receive a character and release the scanner
725022	TCC	Transmit a character from receiver counter
724022	TCB	Transmit a character from send buffer
720122	RRC	Read the receiver counter
724122	SSB	Set the send buffer
721122	RSC	Clear flag and release scanner

Display IOT's

720007	DPY	Display one point (intensify)
722027	GPL	Generator plot left
720027	GPR	Generator plot right
720127	GCF	Reset
722026	GLF	Load format
720026	GSP	Space
722007	SDB	Load buffer, no intensify

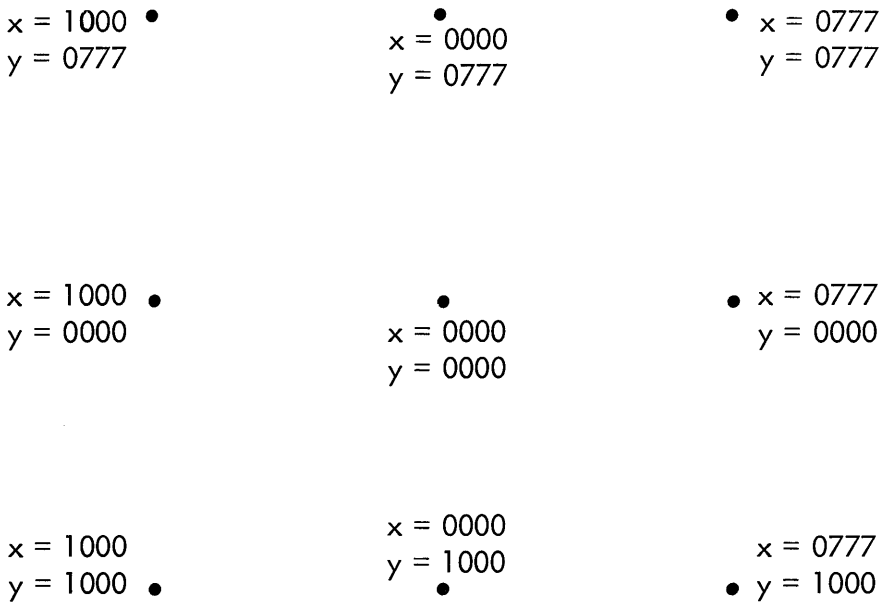
Precision CRT Display (30)

720007	DPY	Display one point. Clears the light pen status bit and displays one point using bits 0 through 9 of the AC to represent the (signed) X coordinate of the point and bits 0 through 9 of the I/O as the (signed) Y coordinate

AC bits 0-9 and I/O bits 0-9 are loaded before the DPY instruction is given. The line specified by the AC is the signed X coordinate. Plus (0) in AC bit 0 plots points from the center of the

*Above must be given in sequence shown.

cathode ray tube to the right 4-5/8 inches. Minus (1) in AC bit 0 plots the points from the center of the tube to the left 4-5/8 inches. The line specified by the I/O is the signed Y coordinate. Plus (0) in I/O bit 0 plots points vertically up from the center. Minus (1) in I/O bit 0 plots the points from the center down.



Character Generator (33)

722027	GPL	Generator plot left. Transfers the contents of the I/O register of the symbol generator and initiates plotting of the first 17 dots. I/O_{17} of this word sets or resets the subscript control as the bit is a 1 or a 0.
720027	GPR	Generator plot right. Transfers the contents of the I/O register to the shift register of the symbol generator and initiates plotting of the last 18 dots. The "Clear" is inhibited by MB_7^0 to prevent losing the count contained in the horizontal and vertical counter which controls dot position.
720127	GCF	Reset. Clears the light pen status flip-flop in the display. The light pen status will also be cleared when a normal point plot (IOT-07) is performed.

722026 GFL — Load format. The three least significant bits of the I/O register are sent to the character-size control flip-flops and the spacing control circuits. Bits 16 and 17 specify one of four symbol sizes as shown in the tables below. Bit 15, if a 1, specifies automatic spacing between symbols. A completion pulse is not generated by the display when this instruction is performed.

Matrix size, and hence character size, is determined by the number of increments separating the dots on the matrix, when an increment is defined as 1/1024th of the width of height of the display area. The relationship between character size and incremental separation of dots is given below.

Character Size	Bit 16	Bit 17	Number of Increments
1	0	0	2
2	0	1	3
3	1	0	4
4	1	1	5

720026 GSP — Space. Increments the X buffer-counter to position the beam one character position to the right. Since the contents of the I/O register are transferred to the shift register by this instruction, the I/O register should be cleared before performing the "Space" instruction.

720007 DPY — Load buffer - intensify

722007 SDB — Load buffer - no intensify. By use of the MB_{12} bit, the normal point plotting instruction (IOT-07) can be used to load the position coordinates of the first character to be displayed without illuminating that point. When the "No Intensify" instruction is performed, the display will not generate a completion pulse; therefore, the computer must allow at least 25 microseconds before executing a gpl instruction.

Except for the gcf, glf, and sdb instructions, which do not cause the generation of a completion pulse, the preceding iot instructions can be coded to perform the in-out wait operations.

72X061* DIA — Drum initial address

Transfers the contents of the I/O register to the drum and is decoded to mean:

IO_0^1 = Read

IO_{1-5} = Field to be read

IO_{6-7} = Drum initial address

720062* DWC — Drum word count

Transfers the contents of the I/O register to the drum and is decoded to mean:

IO_0^1 = Write

IO_{1-5} = Field to be written

IO_{6-17} = Words to be transferred

720063* DCL — Drum core location

$IO_2^0 - IO_3^0$ = Select memory 0

$IO_2^0 - IO_3^1$ = Select memory 1

$IO_2^1 - IO_3^0$ = Select memory 2

$IO_2^1 - IO_3^1$ = Select memory 3

IO_{4-17} = Starting core address and GO $\longrightarrow$

722061 DBA — Drum break address

Is decoded the same as DIA. When a DBA instruction is given, a sequence break occurs when drum address = drum initial address. If programming consideration can accept the break, DBA can be used in place of DIA in the drum sequence of instructions.

720064 LRM — Leave restrict mode

Zeros the restricted mode flip-flops. No memories are protected. All instructions are legal except incorrect OP code selections.

*Above must be given in sequence shown.

720065 ERM

Enter restrict mode

When entering restrict mode, the I/O register should be preloaded with the desired memories to be protected.

IO_0^1 = Protect memory 0

IO_1^1 = Protect memory 1

IO_2^1 = Protect memory 2

IO_3^1 = Protect memory 3

When in the restrict mode if an incorrect operation code, in-out transfer (IOT), a HLT or any protected memory is addressed, it causes the restrict mode logic to initiate a break to channel 16_8 in the sequence break logic.

72XX66 RNM

Rename memory

Rename memory takes the memory designated by X and renames it to the number contained in Y. There are four memories and they can be named in any of 16 different configurations. All addressed memories are checked for name. Memory rename logic cannot be bypassed. See RSM.

720067 RSM

Reset memory

Restores the physical name to all memories. Zero is a zero, etc.

720032 RCK

Read clock

The I/O is cleared and the clock buffer is read into the I/O register.

The clock register is automatically synchronized to the computer timing, and it is not necessary to read clock register more than once. The clock is a pulse at a 1 kc rate and can be read as often as desired.

72XX35 CTB

Clear trap buffer

The trap buffer (which is loaded at the time a restrict mode trap occurs) is cleared by this IOT.

72XX17	RRO	Rem-rand out Transfers the condition of the I/O register bits 0-17 to the Rem-Rand Control.
72XX37	RRI	Rem-rand in Clears the I/O and reads the conditions of the Rem-Rand Control into the I/O register bits 0-17.
720011	ERG	Enter ring mode Places the computer in the ring mode. (See special operate group for detailed description.)
720010	LRG	Leave ring mode Zeros the ring mode flip-flop.

Data Communication System

The 630 Data Communication System is assigned one basic IOT instruction, octal code 720022. (Bits 0-17)

The basic instruction is microprogrammed to form a set of useful computer instructions for operating the DCS. Adding or ORing 2000_8 to the octal equivalent causes the I/O to be cleared before the operation is executed.

The following instructions control the scanner, the teletype transmitters and teletype receivers. For convenience, bit configurations are assigned mnemonics as follows:

720022	RCH	Receive a character to I/O 10-17 (8 bits) (13-17, 5 bits) using the receiver counter. The OR function occurs. Clear the receiver flag. I/O bits 10-17 must be zeros prior to operation execution.
721022	RCC	Same as RCH. Clear the scanner flag (release the scanner).
725022	TCC	Transmit a character using the receiver counter (I/O 10-17, 8 bits; I/O 13-17, 5 bits, to the transmitter). Clear the receiver flag. Clear the scanner flag (release the scanner).

724022	TCB	Transmit a character using the send buffer (I/O 10-17, 8 bits; I/O 13-17, 5 bits, to the transmitter). Clear the receiver flag.
720122	RRC	Read the receiver counter (counter to I/O 12-17). The OR function occurs.
724122	SSB	Set the send buffer (I/O 12-17 to send buffer). Used to select an idle station for transmission.
721122	RSC	Clear the scanner flag (release the scanner).

The state of the scanner flag may be read into I/O register bit 16, using the check status instruction (1 = flag on).

Initialization procedures must at least include clearing of the scanner flag. (Actually all receiver flags should be cleared.)

The priority level to which the scanner flag is assigned is dependent upon the equipment configuration of your system.