digital

Computer
Special
Systems

TM02-FE/FF

MAGNETIC TAPE CONTROLLER

OPTION DESCRIPTION

ADDENDUM
REQUIRED

COMPUTER TYPE PDP11	DRAWING SET NO. TM02-0
PROGRAM NO. DECSPEC-11-AYVAD DECSPEC-11-AYVBD DECSPEC-11-AYVCD DECSPEC-11-AYVDD DECSPEC-11-AYVED DECSPEC-11-AYVFD	DOCUMENT NO. CSS-MO-F-5.2-22A
DATE February 1977	

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UNIBUS	MASSBUS
DECUS	

PREFACE

This manual is organized in a modular format to aid the user in finding information, at the level desired, in the shortest period of time. To accomplish this, the manual is broken down into three chapters, the contents of which are as follows:

CHAPTER 1, GENERAL INFORMATION - Contains general introductory information of interest to the operator, such as operating instructions, specifications, system configuration, and magnetic tape fundamentals.

CHAPTER 2, THEORY OF OPERATION - Presents an overview "Big Picture" of the theory of operation of the SLAVE/TM02 Tape Drive System. This chapter is intended to aid servicing personnel in understanding the basic principles of operation of the SLAVE/TM02. The final section of this chapter is a guide to the detailed servicing information in Chapter 3.

CHAPTER 3, SERVICING - Consists of servicing pamphlets which describe various functional areas of the TM02. The first pamphlet, Maintenance Modes, describes on-line and off-line maintenance capabilities; the remaining pamphlets contain detailed theory of operation.

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

The TM02-FE/FF is a Massbus-compatible, versatile Tape Controller for TU45 Tape Transport(s). The TM02 records and reads digital data in industry standard PE or NRZI mode at a maximum data transfer rate of 120,000 tape characters per second. Tape density and tape character format are program selectable. Forward/reverse tape speed is 75 in./sec, while rewind is performed at 250 in./sec. The TM02 Controller System also has forward and reverse read/space capability.

1.2 OPTIONS

Table 1-1 lists options available in the TM02 Tape Controller.

Table 1-1
TM02 Options

Unit	Designation	Data Features	Power Requirement
TM02	FE	16-bit/PE/NRZI	115 Vac at 50/60 Hz
	FF	16-bit/PE/NRZI	230 Vac at 50/60 Hz

1.3 SPECIFICATION

Table 1-2 contains operational, environmental, mechanical, and electrical specifications for the TM02 Controller.

Table 1-2
TM02 Specifications

PARAMETER   SPECIFICATION

Maximum Transfer Rate   120,000 characters/sec
    (w/TU45)

Recording Method   NRZI   or   PE   recording;   industry
                                   compatible.

Voltage Requirement   115/230 Vac +/-10% at 50/60 Hz +/-2%

Power Dissipation   300W (max.)

TM02 Tape Contoller   23 in. (0.58cm)
    Depth
    Width   19 in. (0.48m)
    Height   7 in. (0.17m)
    Weight   45 lbs (21 Kg)

TM02 Power Supply (H740DA)
    Depth   8 in. (0.18m)
    Width   19 in. (0.48m)
    Height   5 in. (0.13m)
    Weight   24 lbs (11.2 Kg)

Environmental Limits

    Temperature   60 to 95 degrees F (15 to 35 degrees C)*
    Relative Humidity   20 to 80% (no condensation)*

*Magnetic tape operation is more reliable if the temperature is
limited to 65 degrees to 75 degrees F (18 degrees to 24 degrees C) and
relative humidity to 40 to 60 %.

        TM02 Power Supply (H740DA) - Provides the ac and dc power
        required by the TM02 logic assembly.

        861 Power Controller - Controls power to the TM02 and TU45

                              NOTE

        Only TU45/TM02 master cabinets contain
        the TM02 logic assembly and power
        supply. TU45 slaves are controlled by
        the TM02 in the master cabinet.

1.4   REFERENCE DOCUMENTS

The following documents should be available to the user:

        TM02 Engineering Drawing Set
        TWU45 Magtape System Manual (CSS-MO-F-5.2-25)
        TJU45 Magtape System Manual (CSS-MO-F-5.2-21)
        RH70/Special Option Description (CSS-MO-F-5.2-27)
        RH11/Special Option Description (CSS-MO-F-5.2-26)
        M.T.A. Option Description (CSS-MO-F-5.2-23)
        TU45 Operating and Service Manual (Pertec # 104597)
        861-A, B, C Power Controller Maintenance Manual
        (DEC-00-H861A-A-D)
        H740D Power Supply Maintenance Manual (DEC-11-H740A-A-D)

Other useful documents include:

        Recorded Magnetic Tape for Information Interchange (800 CPI,
        NRZI, ANSI Document No. X3.22-1973)

        Recorded Magnetic Tape for Information Interchange (1600 CPI,
        PE, ANSI Document No. X3.39-1973)

1.5   SYSTEM CONFIGURATION

Figure 1-1 illustrates a TU45/TM02 Tape Drive System configuration.
Each TM02 can control up to eight slave TU45 Tape Transports. In
turn, each Massbus Controller can control up to eight TM02 Tape
Controllers.   Thus, a maximum of 64 TU45 Tape Transports could be
interfaced to a Massbus Controller.
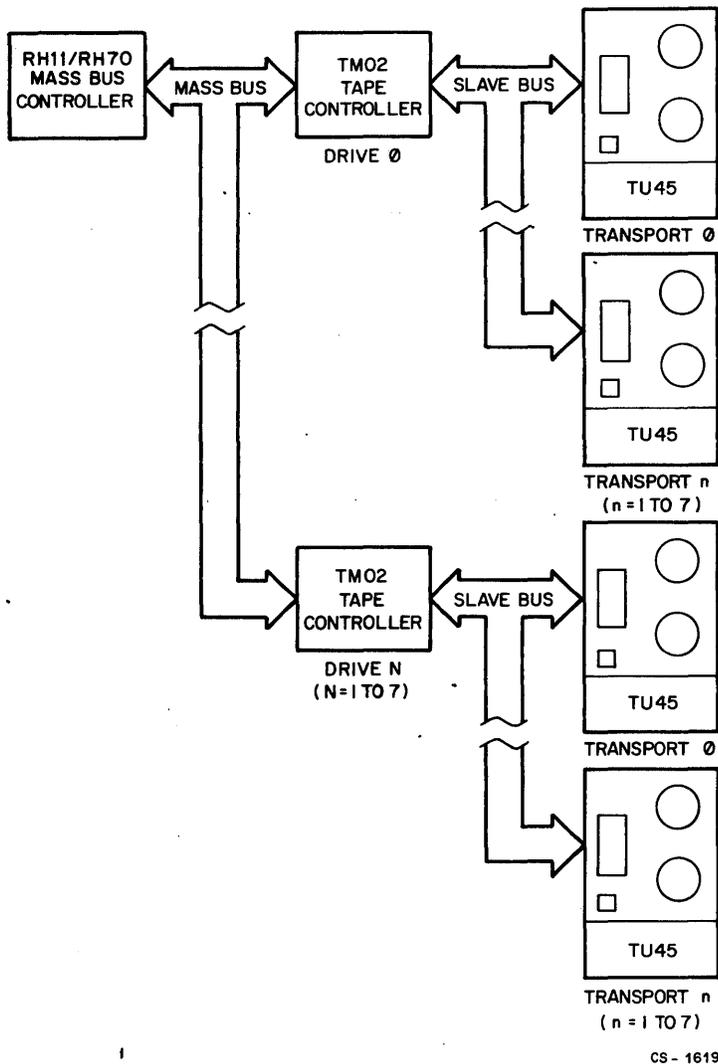
CS - 1619

Figure 1-1 TU45/TM02 Tape Drive
System Configuration

1.6 OPERATING PROCEDURES

1.6.1 Application of Power

1. If the 861 Power Controller REMOTE ON/OFF/LOCAL ON switch is
    in the REMOTE ON position, TU45/TM02 power is controlled by
    the processor POWER key switch.   This method is used in
    normal operation.

2. If the processor POWER key switch is not activated, TU45/TM02
    power may be turned on locally by setting the 861 Power
    Controller REMOTE ON/OFF/LOCAL ON switch to LOCAL ON.   This
    method may be used during maintenance.

1.6.2 Tape Handling

WARRANTY

Removable media involve use, handling, and maintenance which are beyond DEC's direct control. DEC disclaims responsibility for performance of the equipment when operated with media not meeting DEC specifications or with media not maintained in accordance with procedures approved by DEC. DEC shall not be liable for damages to the equipment or to media resulting from such operation.

The operator should observe the following precautions when handling magnetic tape:

1. Always handle a tape reel by the hub hole; squeezing the reel flanges can cause damage to the tape edges when winding or unwinding tape.

2. Never touch the portion of tape between the BOT and EOT markers. Oil from fingers attracts dust and dirt. Do not allow a tape end to drag on the floor.

3. Never use a contaminated reel of tape; this spreads dirt to clean tape reels and can affect tape transport operation.

4. Always store tape reels inside their respective containers. Keep empty containers closed so dust and dirt cannot get inside.

5. Inspect tapes, reels, and containers for dust and dirt. Replace damaged take-up reels.

6. Do not smoke near the transport or tape storage area. Tobacco smoke and ash are especially damaging to tape.

7. Do not place the TU45 Tape Transport near a line printer or other device that produces paper dust.

8. Clean the tape path (see TU45 Manual).

1.7 MAGNETIC TAPE FUNDAMENTALS - DEFINITIONS

1. Reference Edge - The edge of the tape as defined by Figure 1-2. For tape loaded on a TU45, the reference edge is toward the observer.

2. BOT (Beginning of Tape) Marker - A reflective strip placed on the nonoxide side of the tape, against the reference edge, 15 feet (+/-1 ft) from the beginning of the tape.

3. EOT (End of Tape) Marker - A reflective strip placed on the nonoxide side of the tape, against the nonreference edge, 25 to 30 feet from the trailing edge of the tape.

4. Nine-Channel Recording - Eight tracks of data plus one track of vertical parity. Figure 1-3 shows the relationship between track and bit weight for a nine-channel transport.

5. Tape Character - A bit recorded in each of the nine channels.

6. Record - A series of consecutive tape characters.

7. File - An undefined number of records (minimum = zero, no maximum).

8. Interrecord Gap (IRG) - A length of erased tape used to separate records (0.5 in. minimum for nine-track; maximum IRG is 25 ft).

9. Extended IRG - A length of erased tape (3 in. minimum) optionally used to separate records. It must be used between BOT and the first record.

10. Tape Speed - The speed at which tape moves past the read/write heads; normally stated in inches per second.

11. Tape Density - The density of sequential characters on the tape. It is normally specified in bytes per inch (bpi). This is equivalent to characters per inch (cpi), since 800 bpi means that there are 800 tape characters per inch of tape.

12. Write Enable Ring - A rubber ring which must be inserted on the supply reel to allow the transport to write on the particular tape. This safety feature helps prevent accidental destruction of previously recorded data.

13. Tape Mark (TM) - A record written on the tape to designate the end of a file; sometimes referred to as a file mark (FMK). In the SLAVE/FM02, the tape mark is always preceeded by an extended IRG.
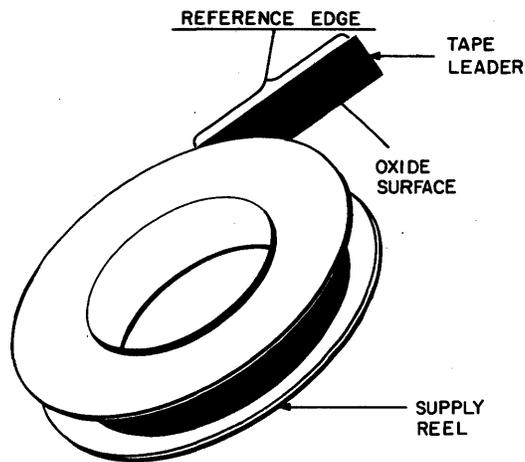
Figure 1-2 Reference Edge of Tape
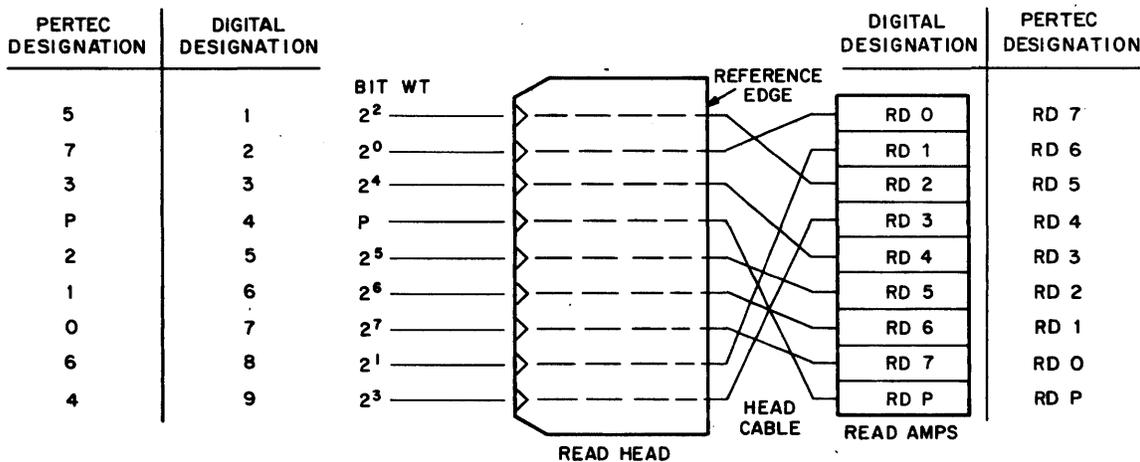
Figure 1-3 Track-Bit Weight Relationship
for Nine-Channel Transport

1.8 TU45/TM02 RECORDING TECHNIQUES

1.8.1 NRZI (Non-return to Zero - Change on a 1)

1.8.1.1 Definition - NRZI is a recording technique which requires a change of state (flux change) to write a 1, and no change of state (no flux change) to write a 0.

1.8.1.2 Format - Cyclic Redundance Check Character (CRCC) - A check character that is written four character spaces after the last character of an NRZI record (nine-channel only). CPCC is derived by a complex mathematical formula applied to the characters written in the record. The result of this manipulation (CRCC) can be used to recover a lost bit in a record read from tape.

Longitudinal Parity Check Character (LRCC) - A check character written four character spaces after CRCC (nine-channel). LRCC consists of one bit of even parity for each track of data. For example, if track 1 had an odd number of 1s written in a record, then a 1 must be written in the LRCC bit associated with track 1 (occurs at reset of write drives).

Tape Mark - A nine-channel NRZI tape mark consists of one tape character (23(8)), followed by seven blank spaces, and then LRCC (23(8)). (CRCC is not written.) Figure 1-4 illustrates nine-channel NRZI tape format.

1.8.2 PE (Phase Encoding)

1.8.2.1 Definition - Phase encoding is a recording technique in which a flux reversal occurs for each bit of information written on the tape. A 1 can be defined as a positive level followed by a negative transition, while a 0 can be defined as a negative level followed by a positive transition.
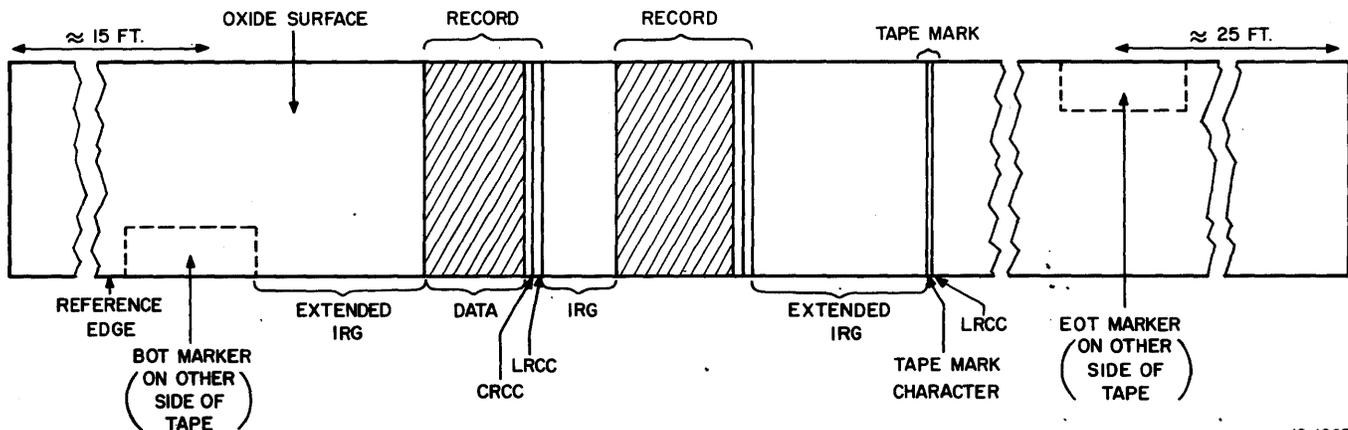
Figure 1-4 NRZI Format (Nine-Channel)

Sequential flux transitions on the tape are either at the data rate or at twice the data rate. Sequential 1s or sequential 0s will cause flux reversals to occur at twice the data rate:
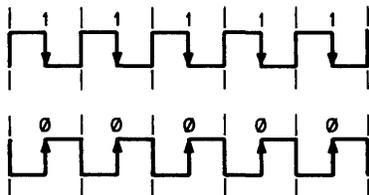
10-1271

Alternate 1s and 0s cause flux reversals to occur at the data rate:
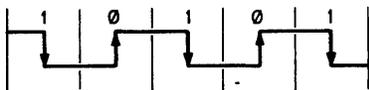
10-1269

1.8.2.2 Format - To ensure proper extraction of PE data from the serial stream of transitions coming off the tape, PE data must be recorded in a precise format. A PE record consists of preamble, data, and postamble.

1. Preamble - Forty characters of 0s in all nine tracks, followed by a character of 1s in all nine tracks.

2. Postamble - One character of 1s in all nine tracks, followed by 40 characters of 0s in all nine tracks.

The PE read electronics uses a data window to isolate data transitions. For example,

10-1270

1-9
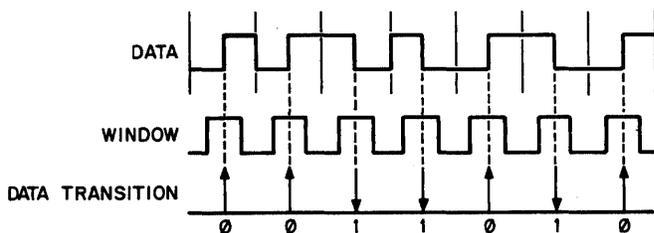
Zeros in the preamble are used to set the window in position when reading in a forward direction, while 0s in the postamble perform this function when reading in the reverse direction. The all-1s character in the preamble and postamble is used to mark the beginning and end of data.

Tape Mark - A PE tape mark consists of forty 0s in tracks 1, 2, 4, 5, and 8 (bit positions 2, 0, P, 5, and 1) with tracks 3, 6, 7, and 9 (bit positions 4, 6, 7, and 3) erased. (See Figure 1-3 for the Digital to Pertec designation conversion).

Identification Burst (IDB) - The IDB identifies the tape as being a PE tape. It consists of alternating 1s and 0s in the parity track (track 4) with all other tracks erased. The IDB is located at BOT, and has a minimum length of 1.7 in. Figure 1-5 illustrates PE tape format.
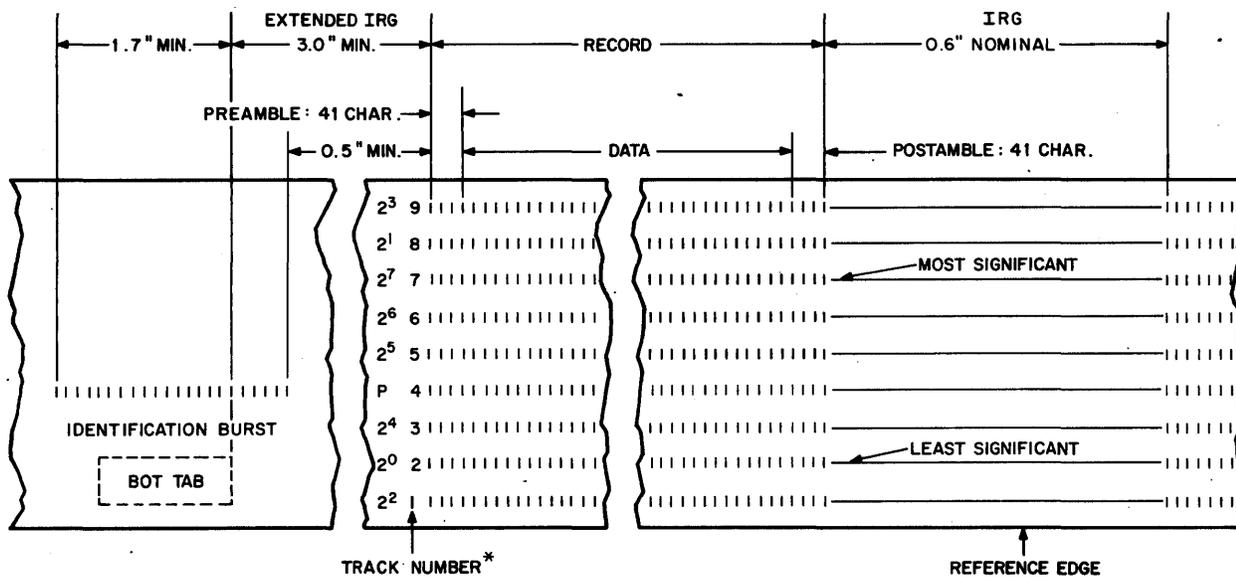
Figure 1-5 PE Recording Format

* See Figure 1-3 for Digital to Pertec designation conversion.

CHAPTER 2

THEORY OF OPERATION

2.1   INTRODUCTION

The TU45/TM02 Tape Drive System (Figure 2-1) interfaces with the central processor (CPU) via the Massbuss Controller. However, the Massbus Controller is almost transparent to the CPU, and the CPU operates as though it were controlling the drive directly.

The TU45/TM02 interfaces with the Massbus Controller via the Massbus. The Massbus consists of an asynchronous control bus with its associated control lines, and a synchronous data bus with its associated control lines. Transactions on the control bus control the TU45/TM02 and determine its status, while transactions on the data bus transfer data to or from the TU45/TM02. Because the data and control buses operate independently, the Massbus Controller can monitor drive status while a data transfer operation is being performed. Table 2-1 lists the Massbus interface signals and their functions.

The TM02 can control up to eight TU45 Tape Transports via the slave bus. All TU45'S controlled by a TM02 are "daisy-chained" on the slave bus (Figure 1-2). Essentially, this means that the TU45's are configured in parallel with each other. The slave bus consists of slave (TU45) select lines, write data lines, read data lines, transport control lines, and various TU45 status lines. Table 2-2 lists the slave bus interface signals and their functions. Figure 2-2 shows the Massbus and slave bus signals connecting the TM02, with the TU45 and Massbus Controller.

TU45/TMO2 TAPE SYSTEM

CPU — RH11/RH70 MASSBUS CONTROLLER — MASSBUS — TMO2 TAPE CONTROLLER — SLAVE BUS — SLAVE TAPE TRANSPORT

TO 1-7 OTHER DRIVES

TO 1-7 OTHER TU45 TRANSPORTS
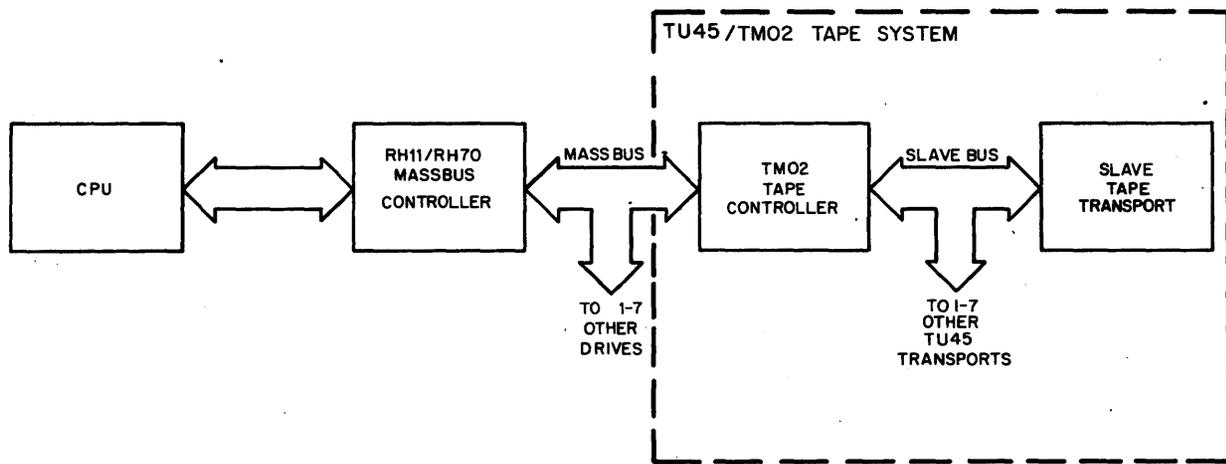
CS-1615

Figure 2-1 TU45/TM02 In System Configuration

Table 2-1
Massbus Interface Signals

SIGNAL	FUNCTION
Data Bus Data Lines [D(0;17)]	These bidirectional lines transmit 18 parallel data bits to or from the TM02.
Data Lines Parity (DPA)	This bidirectional line transmits the data parity bit (odd parity) to or from the TM02. Data parity is simultaneously transmitted with the bits on the Data lines.
Sync Clock (SCLK)	During a data write, this line transmits SCLK from the TM02 to request write data from the Massbus Controller. During a data read, this line transmits SCLK to the Massbus Controller to indicate that read data is present on the Data lines.
Write Clock (WCLK)	During a data write, this line transmits WCLK from the Massbus Controller to strobe write data into the TM02.
Run (RUN)	This line transmits RUN from the Massbus Controller to initiate data transfer execution.
End of Block (EBL)	Normally, this line transmits EBL from the TM02 at the end of each record. However, for certain abnormal conditions where it is necessary to terminate the transport operation immediately, EBL is transmitted prior to the end of the record.
Exception (EXC)	This bidirectional line transmits EXC from the TM02 to indicate that an error has occurred during data transfer. In some systems, EXC H can also be transmitted over this line from the controller to abort an in-progress data transfer.
Occupied (OCC)	During a data transfer (read/write), this bidirectional line transmits OCC from the TM02 to indicate that a transport has control of the data bus. Once asserted, this signal prevents any other transport from using the data bus.
Control Bus Control Lines [C(0:15)]	These bidirectional lines transmit 16 parallel control or status bits to or from the TM02.

Table 2-1 (Cont.)
Massbus Interface Signals

Control Lines Parity (CPA)   This bidirectional line transmits control lines parity (odd parity) to or from the TM02. Control parity is simultaneously transmitted with the bits on the Control lines.

Drive Select [DS(0:2)]   These three lines transmit a three-bit binary code from the Massbus Controller to select a particular drive (TM02).

Register Select [RS(0:4)]   These five lines transmit a five-bit binary code from the Massbus Controller to select one of the ten TM02 registers.

Controller to Drive (CTOD)   This line transmits the CTOD signal from the Massbus Controller to indicate in which direction data is to be transferred on the Control lines. For a controller-to-drive transfer, the controller assertes CTOD. Conversely, for a drive-to-controller transfer, the controller negates CTOD.

Demand (DEM)   This line transmits DEM from the Massbus Controller to initiate a control bus transfer (initiate "handshake").

Transfer (TRA)   This signal is asserted by the drive in response to DEM. For a controller-to-drive transfer, TRA is asserted when the data is strobed and is negated when DEM is negated. For a drive-to-controller transfer, TRA is asserted after the data is asserted on the bus and negated when the negation of DEM is received.

Attention (ATTN)   This line transmits ATTN from the TM02 to indicate that an abnormal condition or transport status change has occurred in the drive.

Initialize (INIT)   This line transmits INIT from the Massbus Controller to initialize all TM02's and transports on the daisy chain. INIT is transmitted at system start-up or whenever the Massbus Controller issues an initialize command.

Table 2-1 (Cont.)
Massubs Interface Signals

Massbus Fail (MASSFAIL)   This line transmits MASSFAIL L negated from
                           the Massbus Controller to indicate that the
                           controller power supply is operating
                           properly. If the controller power supply
                           fails, MASSFAIL L is asserted, thus
                           initializing the TM02 logic as well as
                           preventing it from accepting erroneous
                           control bus information.

Table 2-2
Slave Bus Interface Signals

SLAVE BUS SIGNAL   FUNCTION

Slave Select [SS(0:2)]   These lines select one out of eight
                            possible TU45 Transports for command
                            execution.

Forward (FWD)   These are the four command lines which
Reverse (REV)   determine TU45 operation.
Rewind (RWND)
Write Enable (WRITE)

Slave Set Pulse   This signal initiates TU45 response
(SLAVE SET PLS)   to the four command lines.

Stop (STOP)   This signal causes the TU45 to terminate
                            motion. (Does not apply to rewind,
                            which terminates independently).

Enable Motion Delay (EMD)   This signal enables the TU45 (M8921) to
                            gate out a coded motion delay preset
                            onto the read lines.

Accelerate (ACCL)   Asserted by the TM02 while the transport
                            is getting up to speed or not moving
                            tape. Not asserted while the IDB is
                            being written.

Write Data [WD(0:7,P)]   These nine lines transmit the data to be
                            written by the TU45.

Record (REC)   A pulse that causes data to be written
                            on tape.

Density Select [DEN(0:2)]   These three lines control the density at
                            which data is written on tape. They
                            must also represent the density of tape
                            data during a read operation.

Table 2-2 (cont.)
Slave Bus Interface Signals

Clock (CLOCK)	A 240-kHz clock generated in the TU45, MTA (M8921), present at all times when the unit is on-line.
Write Clock (WRT CLK)	This clock is transmitted to the TM02 by a powered, on-line TU45 loaded with tape when it is running at speed (ACCL not asserted). The frequency of WRT CLK is a function of the DEN lines, and controls the write timing frequency.
LRC Strobe (LRC STRB)	Asserted by the TM02 prior to the REC PULSE that writes the LRC character.
Read Data [RD(0:7,P)]	These nine lines transmit read data from the TU45 to the TM02. (They also transmit the motion delay preset).
Read Strobe Delay Over (RSDO)	A Read Strobe pulse generated by the transport at the end of the skew delay in NRZI mode.
Beginning of Tape (BOT)	Asserted when the TU45 detects the beginning-of-tape marker.
End of Tape (EOT)	Asserted when the TU45 detects the end-of-tape marker.
Rewind Status (RWS)	Asserted while the selected TU45 is performing a rewind operation.
7-Channel (7 CH)	Always negated by a selected TU45.
Slave Present (SPR)	Asserted by a selected, powered TU45.
Medium On-Line (MOL)	Asserted by a selected powered TU45 which is loaded with tape.
Tape Unit Ready (TUR)	Asserted by a selected TU45 to indicate that tape motion has stopped.
Settle Down (SDWN)	Asserted while the transport is decelerating, until it has stopped.
Phase Encoded Status (PES)	Asserted by a TU45 when instructed to operate in PE mode (DEN2 asserted).
Slave Attention (SLA)	Asserted by a TU45 when it comes on-line.

Set Slave Status Change (SET SSC)	Asserted at the completion of a rewind or when the unit comes on-line. It is also pulsed when the transport goes off-line or when the TU45 power fails. This line may be asserted by any slave, selected or not.
Write Lock (WRL)	Asserted when the selected TU45 detects that the write enable ring has been removed from the tape reel.
Interchange Read (IRD)	A maintenance function which inhibits on-the-fly error correction, in PE mode.
Drive Type [DT(0:2)]	In the TU45 (MTA, M8921), these three bits are always asserted as follows:

DT0 0
DT1 1
DT2 0

SERIAL NUMBER [SN(0:15)]	These 16 lines contain the BCD code of the last four digits of the serial number of the selected TU45.
Drive Clear Pulse (DRV CLR PLS)	When asserted by the TM02, DRV CLR PLS clears SLA in the selected TU45.
Initialize Pulse (INIT PLS)	When asserted by the controller, INIT PLS L clears SLA and terminates tape motion (except rewinds) in all on-line transports.
+5V	The TM02 supplies this voltage to power the slave bus terminator networks.
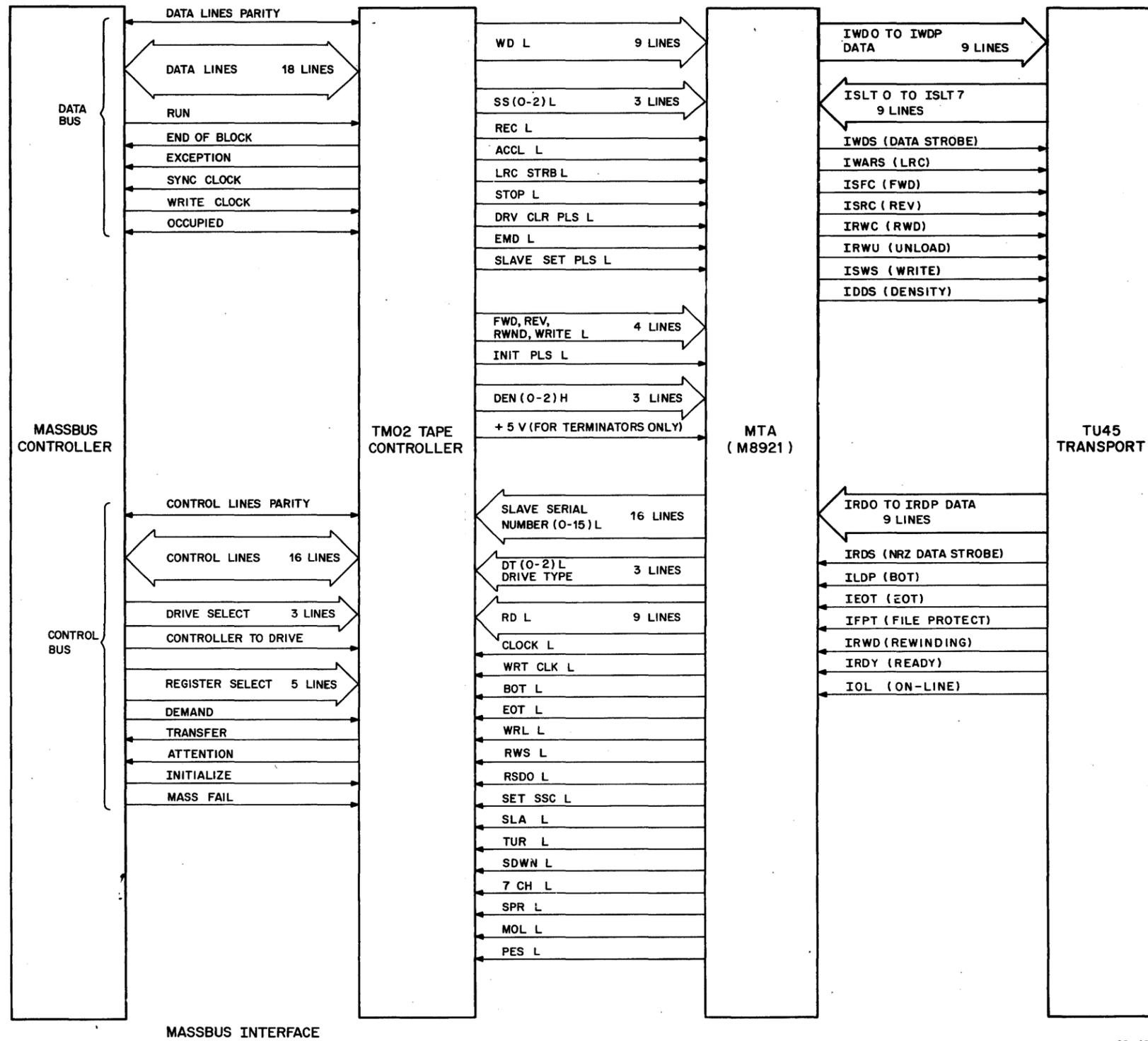
Figure 2-2 Interface Signals

2.2   SYSTEM OPERATION

Figure 2-3 is a block diagram of the TU45/TM02, and shows the major
functional groups, control lines, and data paths. The following
paragraphs describe these functional groups.

2.2.1   Massbus Interface (M8909)

The Massbus Interface interfaces the TU45/TM02 with the Massbus
Controller. It contains circuitry which decodes the Drive Select
signals on the Massbus. If enabled by the proper Drive Select address
code, the Massbus Interface can carry on the "handshake" operations,
with the Massbus Controller, which read and write TM02 registers. The
most important of the TM02 registers, the Control register, is located
in the Massbus Interface. The Massbus Controller writes the function
code of the next operation to be performed into the Control register.
The Massbus Interface decodes this register and generates   the
appropriate control signals (FWD, REV, RWND, WRITE) to control the
TU45 and various TM02 functions.

The Massbus Interface contains several other registers: the Error
register and Attention Summary register can be read by the Massbus
Controller to determine TU45/TM02 status; the Frame Count register
may also be read by the Massbus Controller to determine TU45/TM02
status, and is critical for proper operation of the tape drive.   The
Frame Count register must be loaded prior to a space or write
operation with the number (in 2s complement form) of records to be
spaced or tape characters to be written. This register is incremented
as the operation proceeds, and will terminate the operation with
register overflow.

The Massbus Interface decodes the Control register to determine that a
data transfer operation is to be performed. When this is the case, it
generates OCC on the Massbus to notify the controller and other drives
that it has occupied the data bus, and enables the Bit Fiddler.

2.2.2   Bit Fiddler (M8906)

The Bit Fiddler interfaces the TU45/TM02 data paths to the Massbus
Controller;   it contains circuitry that performs synchronous data
transfers on the data bus of the Massbus.

The Bit Fiddler is enabled for operation by the Massbus Interface with
BF ENABLE H.   The mode of Bit Fiddler operation is determined by
control lines: FMT 0-3 (tape character format), WRITE H (direction of
the transfer, i.e., read or write), and FWD H (direction of tape
motion, i.e., forward or reverse). WRITE H and FWD H are decodes of
the Control register function bits.   FMT 0-3 are the Tape Control
register format bits, and are decoded in the Bit Fiddler.

During a write operation, the Massbus Controller places an 18-bit data

Upon receiving WCLK, the Bit Fiddler strobes in the word on the data bus, performs a data bus parity check, and begins disassembling the 18-bit data word into 8-bit characters. (Vertical parity bits are added at a later stage.) After generating WCLK, the controller places the next data word on the data bus. When the Bit Fiddler has finished disassembling the previous data word, it issues another SCLK, receives another WCLK, and strobes in the next data word for disassembly. The process continues until all the data has been transferred (precluding occurrence of data errors or other failures).

During a read operation, the Bit Fiddler assembles 8-bit characters into 18-bit data words. When the 18-bit data word has been assembled, it is placed on the data bus along with a parity bit (DPA), and the Bit Fiddler generates an SCLK pulse. When the Massbus Controller receives SCLK, it strobes in the data on the data bus. The Bit Fiddler continues to assemble data characters into 18-bit data words, and notifies the controller that a data word is available by generating SCLK. As in a write operation, the method of assembly is determined by the FMT 0-3, WRITE H, and FWD H signals input to the Bit Fiddler.

2.2.3 Maintenance Register Module (M8905-YA)

The Maintenance Register module is part of the read data path; read data is multiplexed through the Maintenance Register module from the PE or NRZI read circuitry (M8901-YC or M8904-YA) to the Bit Fiddler. The Maintenance Register module also contains the Tape Control register, the Check Character register, and the Maintenance register. The Tape Control register contains Slave Select bits, which are translated to slave bus signals (SS 0-2) and determine which TU45 will perform the operations specified by the Massbus Controller. This register also contains tape data format and density information. Therfore, the Tape Control register must be properly loaded by the Massbus Controller prior to the specification of a particular functional operation.

The Maintenance Register module plays an important role in maintenance mode operation. By writing into the Maintenance register (R03), the Massbus Controller can select one of several maintenance modes. These modes allow:

1. Testing of various TM02 circuits independently of the TU45.

2. Testing of the TU45/TM02 under tighter operation criteria.
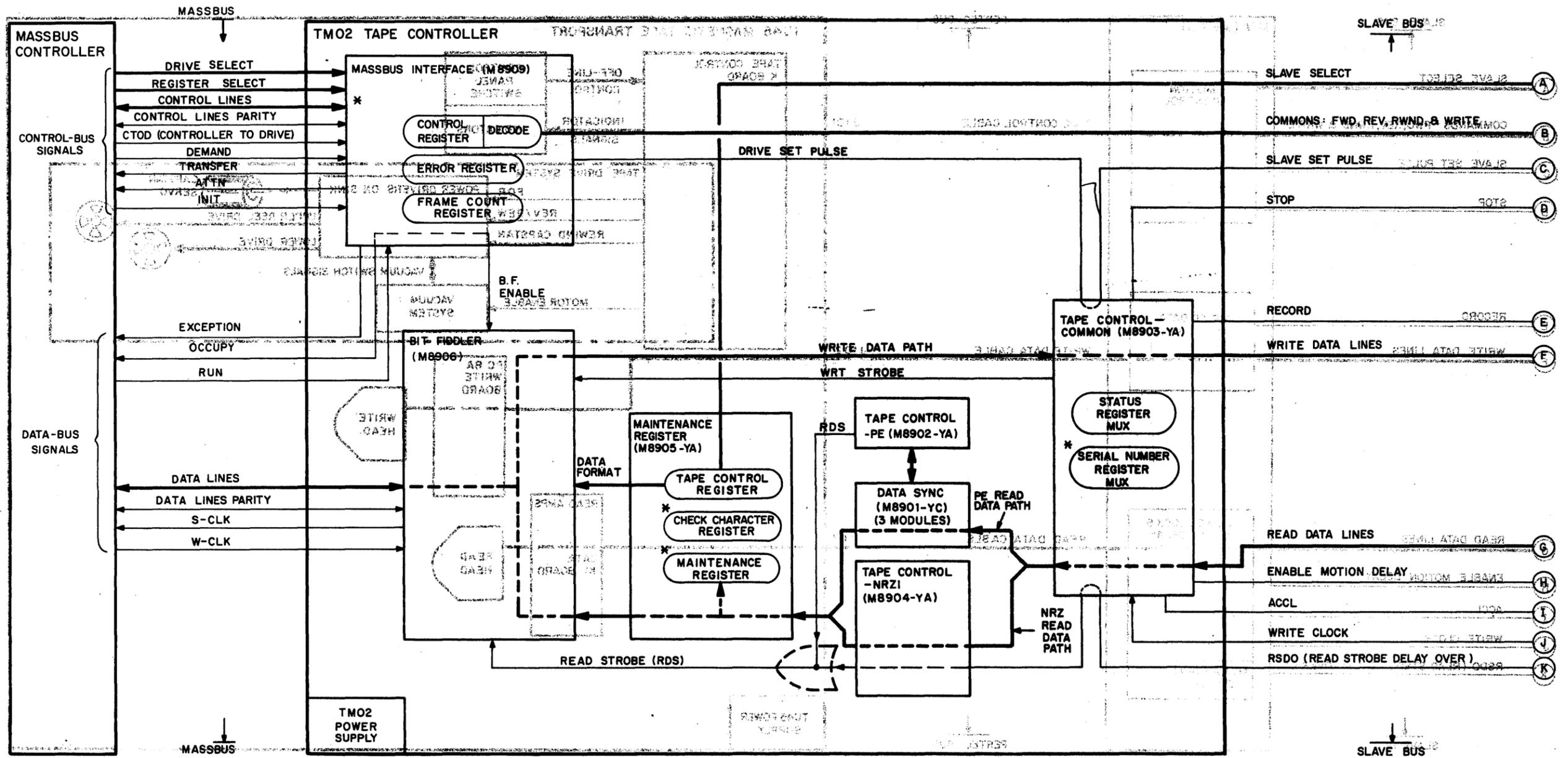
Figure 2-3 TU45/TM02 Block Diagram (sheet 1 of 2)

2-11
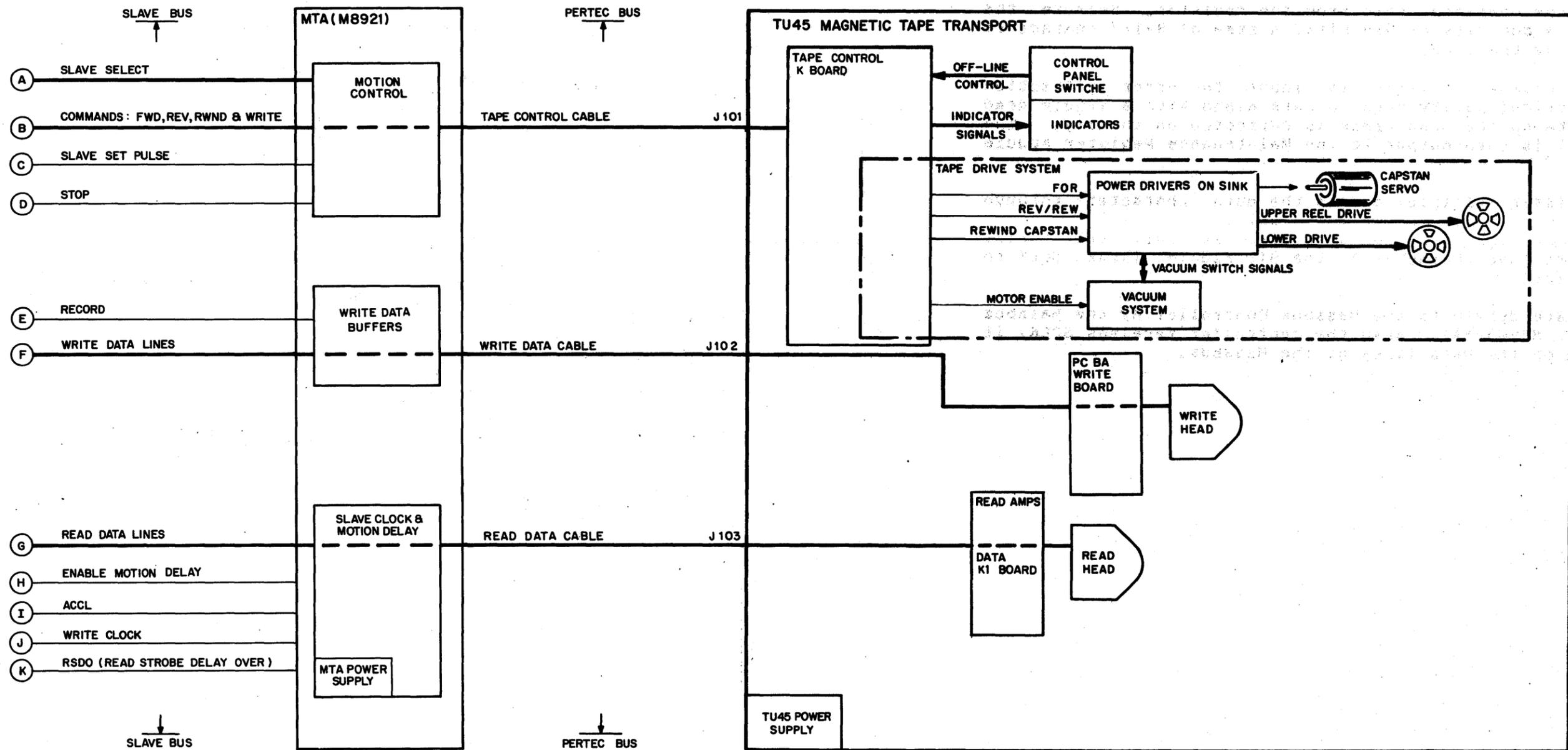
Figure 2-3 TU45/TM02 Block Diagram (sheet 2 of 2)

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2-12

2.2.4 Tape Control-NRZI Module (M8904-YA)

The Tape Control-NRZI module performs functions relating only to NRZI data storage and retrieval. During an NRZI read operation, the Tape Control-NRZI module is part of the read data path. When informed by the Slave Clock and Motion Delay module that a tape character is available [RSDO L (Read Strobe Delay Over) asserted], the Tape Control-NRZI generates RDS H (Read Strobe) and strobes the tape character from the Tape Control Common Mode module (M8903-YA) into an NRZ Read Latch. The output of the latch, multiplexed through the Maintenance Register module, becomes available to the Bit Fiddler.

During an NRZI read operation, the Tape Control-NRZI module also generates and checks LRCC (Longitudinal Parity Check Character) and CRCC (Cyclic Redundancy Check Character), checks vertical parity, detects tape marks (file marks), and determines that the minimum criteria for normal termination have been met.

During an NRZI write operation, the Tape Control-NRZI module generates the CRCC and controls the timing for writing the tape mark (TM) character.

2.2.5 Data Sync-PE Module (M8901-YC)

The Data Sync module (one of three) is part of the PE read data path. It processes PE read data from the Tape Control Common Mode (TCCM) Module (M8903-YA), converting the PE information to binary and deskewing the data. It operates with the Tape Control-PE module (M8902-YA) to detect preamble, data, postamble, and TM. It also performs on-the-fly error correction based on Vertical Parity Errors (VPE) detected by the Tape Control-PE module.

The Data Sync-PE module performs no write data path operations. However, it does do a read-after-write during PE write operations.

2.2.6 Tape Control-PE Module (M8902-YA)

During a PE read operation, the Tape Control-PE module (M8902-YA) operates with the Data Sync module to detect preamble, data, postamble, and TM. It also checks for vertical parity errors and PE format errors.

During a PE write operation, the Tape Control-PE module establishes the timing for writing the preamble, data, and postamble.

2.2.7 Tape Control Common Mode Module (M8903-YA)

The TCCM module (M8903-YA) contains tape control functions that are used by both PE and NRZI modes. The TCCM module generates clock waveforms used throughout the TM02 from a base clock frequency it receives from the TU45 via the slave bus. It also plays a role in the control of TU45 tape motion and the synchronization of TU45 tape motion to TM02 operations.

When the Control register is loaded with a function code requiring tape motion, the function code is decoded by the Massbus Interface, and a FWD, REV or RWND signal is applied to the TU45 via the slave bus. Soon after, a DRIVE SET Pulse is generated by the Massbus Interface to initialize TM02 circuitry. DRIVE SET Pulse enters the TCCM module and produces SLAVE SET Pulse and EMD (Enable Motion Delay) – both of which are transmitted to the Transport via the slave bus. SLAVE SET Pulse sets a motion flip-flop in the MTA (M8921 module), and thereby initiates tape motion. EMD causes a preset to be applied on the Read Data lines of the slave bus by the Clock and Motion Delay in the MTA (M8921), and loads a Motion Delay Counter in the TCCM with the preset. The counter is then upcounted to 2 to the 14th power at which time ACCL H is negated; the TU45 is now assumed to be up to speed. ACCL negated is transmitted from the TCCM module to various TM02 circuitry, and to the transport, as notification that the TU45 is at speed. A similar motion delay is generated upon termination of a motion command, in which ACCL H is asserted, and the TCCM issues STOP L to the TU45, causing the transport to cease tape motion.

During a read operation, read data is multiplexed from the slave bus Read Data lines (and the TM02 slave bus receivers), through the TCCM module, to the Data Sync module (for PE) or Tape Control-NRZI module (for NRZI).

During a write operation, data is inputted to the TCCM module from the Bit Fiddler. The TCCM generates vertical parity bits for the data characters to form nine-bit characters for transfer to tape. The TCCM controls the timing for writing the LRCC and CRCC. It also contains a Write Multiplex and Write Buffer, which:

1. Convert binary characters to PE mode.

2. Multiplex 0's and 1's to write PE preambles and postambles.

3. Multiplex the generated CRCC onto the write data path.

4. Force IDB (identification burst) and TM (tape mark) character patterns onto the write data path.

Figure 2-4 Write Data Path (sheet 1 of 2)
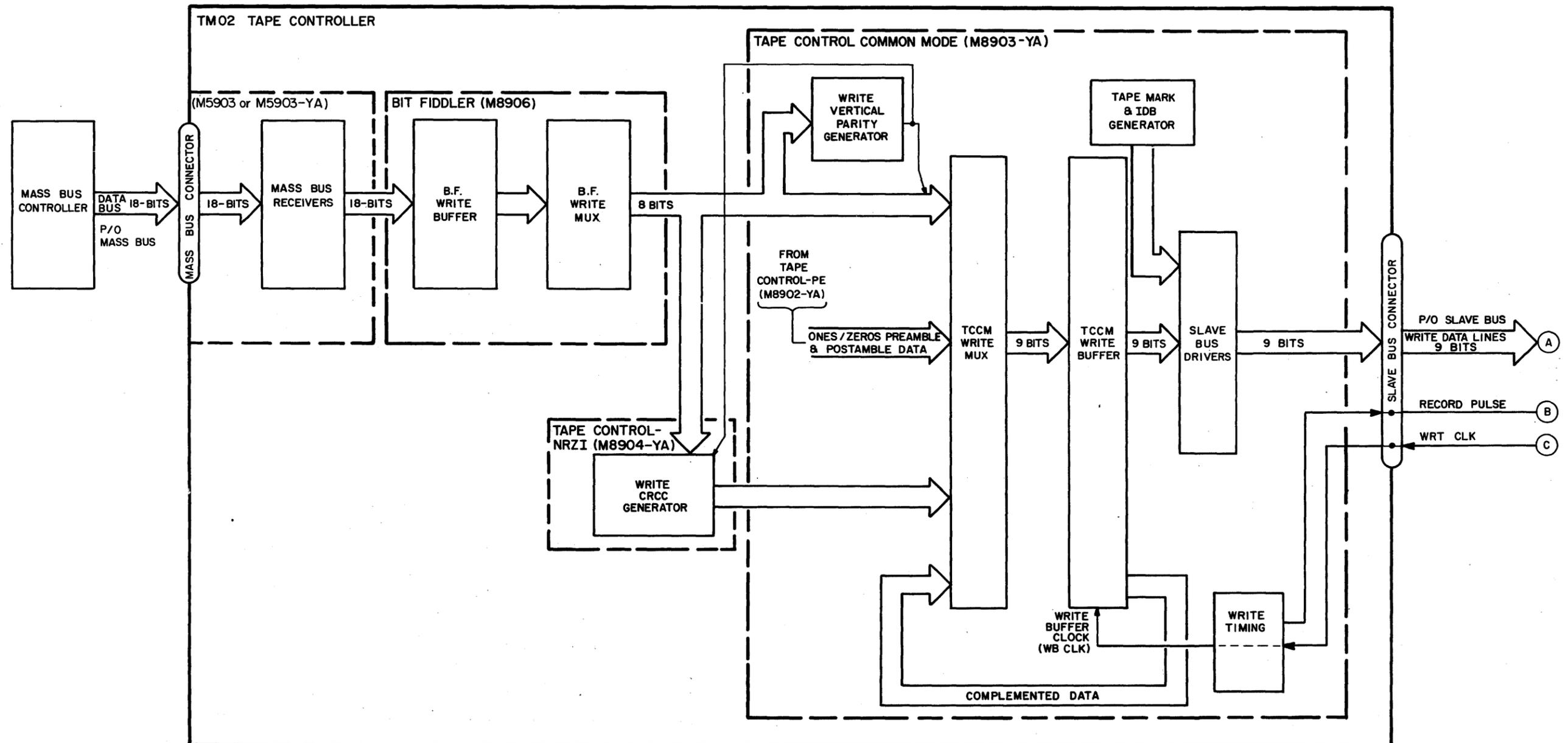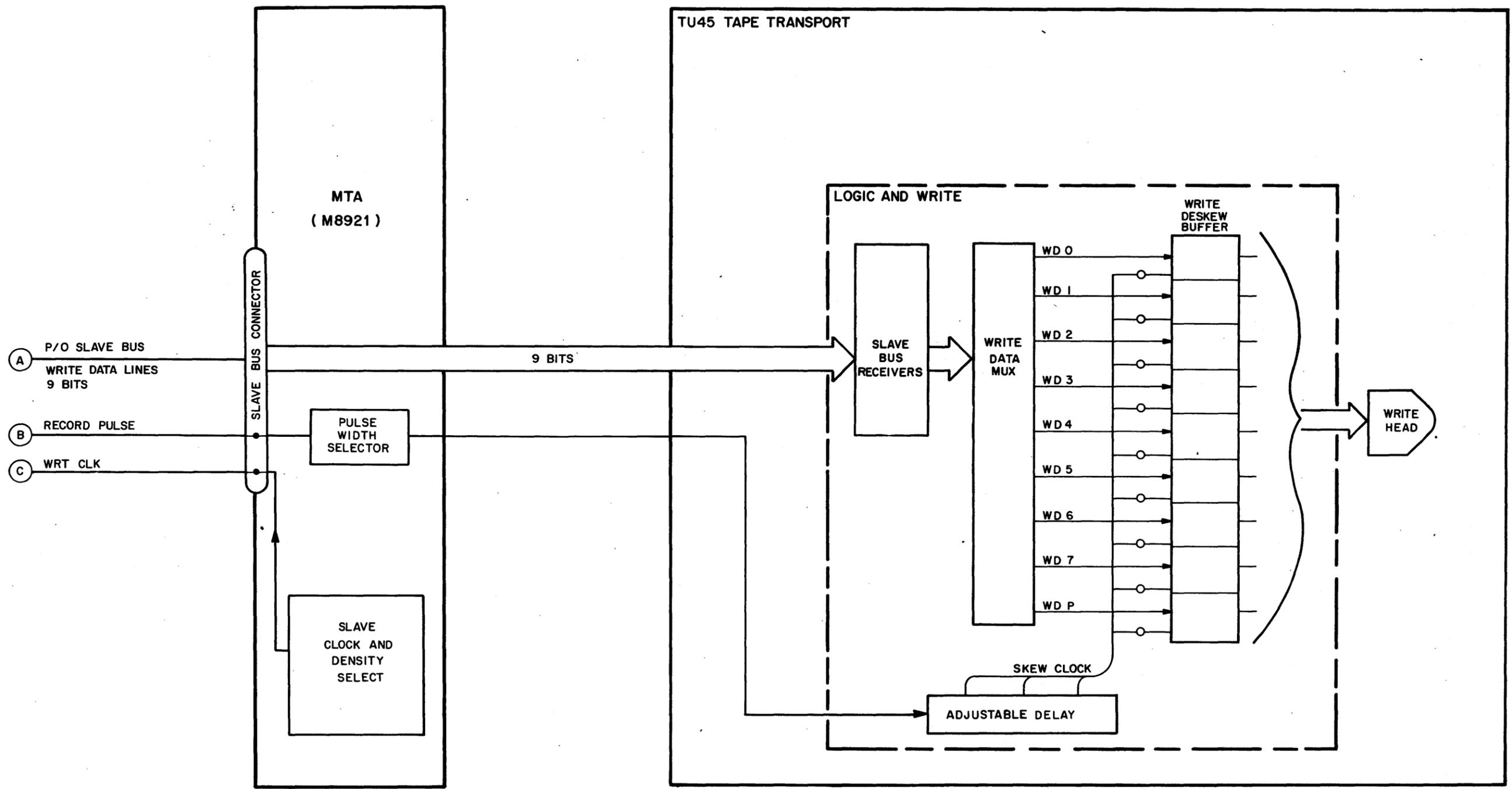
CS-1604

Figure 2-4 Write Data Path (sheet 2 of 2)

CS-1605

Data in the TCCM Write Buffer is output via slave bus drivers to the TU45, along with REC L (SB). REC L (Record) is derived from WRT CLK (SB), generated in the SLAVE Clock and Motion Delay Roms module (M8921) its frequency depends on the mode (PE/NRZI) and density in which the write operation is performed.

2.2.8 MTA Logic Module (M8921)

The MTA Logic Module (M8921) interfaces the TM02 Motion Control signals and write data path to the TU45.

Write Data Path - Input to the MTA circuitry of each track is the data line corresponding to that track. PE write data has been converted from binary to PE mode in the TCCM module. NRZI write data is still in binary mode and is converted to NRZI mode (transition for 1's, no transition for 0's) in the TU45. The Write Data signals are then applied to the write heads.

Tape Motion - The MTA module contains motion control flip-flops and various sequencing circuits. The sequencing circuits provide smooth mechanical operation, which protects data and hardware. The flip-flops enable capstan rotation. These flip-flops are controlled by the TM02 via the slave bus when the TU45 is on-line. when the TU45 is on-line and the MTA receives a motion/write command from the TM02, the flip-flop corresponding to that command will be set upon receipt of SLAVE SET Pulse, at which time the motion will commence (the write amplifiers will be enabled). Receipt of STOP L from the TM02 causes the motion flip-flops to be reset, and the motion terminates.

2.2.9 Slave Clock and Motion Delay on MTA (M8921)

The Slave Clock and Motion Delay LOGIC (M8921) generates clock signals (CLOCK and WRT CLK) used by the TM02. CLOCK is a 240-kHz clock transmitted via the slave bus by a selected, on-line, and powered TU45 loaded with tape. CLOCK is used in the TM02 to generate other clock signals, which perform various housekeeping functions. The frequency of WRT CLK depends on the selected mode (PE/NRZI) and density. It is transmitted to the TM02 by a selected, on-line TU45 loaded with tape when it is running at speed. WRT CLK plays a crucial role in the TM02 during read and write operations. The Slave Clock and Motion Delay logic (M8921), also generates presets for the Motion Delay Counter in the TCCM module. The presets are multiplexed onto the slave bus Read Data lines whenever the MTA receives EMD (Enable Motion Delay) from the TM02.

2.2.10 Read Head and Read Amplifiers

The read head converts changes in magnetic flux on the tape into voltage signals which are then amplified by the Read Amplifiers in

When reading in NRZI mode, the Read Amplifer of each track produces output level for each change of magnetic flux on its tape track (Figure 2-7). These levels will be strobed into the TM02 read logic. Zero bits are recognized by no change in flux on a track when at least one other track has flux change. Because of parity conventions, each character on the tape will have at least one flux change on one of the tape tracks.

When reading in PE mode, the Read Amplifer output for each track will coincide with the direction of flux on its track (Figure 2-7). Because of the nature of phase encoding, each track of PE data contains all of the information necessary to decode it.

2.3 WRITE DATA PATH

The write data path, shown in the TU45/TM02 block diagram (Figure 2-3), is discussed in this section in greater detail (Figure 2-4).

To write data on tape, the Massbus Controller, after loading the Tape Control register and the Frame Count register, loads the write data function code into the Control register, places data on the data bus, and asserts RUN H to the TM02. When the TM02 is ready to accept a data word it asserts SCLK to the Massbus Controller, which reponds by asserting WCLK to the TM02.

The data word, transmitted over the Massbus, is received in the TM02 by the Massbus Receivers (M5903 or M5903-YA) and applied to the Bit Fiddler Write Buffer. When WCLK is received by the TM02, the data word is strobed into this buffer. The Bit Fiddler Write Multiplex now disassembles the data word by multiplexing different portions of the word onto the eight Write Data Bit Fiddler Output (WDBFO) lines. Some of these lines may not contain true data, but may be forced high or low to conform to the format in which data is to be written on tape. The manner in which the Bit Fiddler operates will be determined by the format bits in the Tape Control register.

The outputs of the Bit Fiddler are input to the Tape Control Common Mode (TCCM) module (M8903-YA) where they are used to generate a vertical parity bit for the tape character. The Bit Fiddler outputs, together with the vertical parity bit, are one set of inputs to the TCCM Write Multiplex.

The Bit Fiddler outputs, along with the vertical parity bit, are also input to the Write CRCC Generator on the Tape Control-NRZI module (M8904-YA), where in NRZI mode they generate the CRCC that will be written on the tape (nine-track only) at the end of the record. The outputs of the CRCC Generator are another set of inputs to the TCCM Write Multiplex.

A third set of inputs to the TCCM Write Multiplex are the all 1's/0's. These inputs are controlled by the Tape Control-PE circuitry

(M8902-YA), and are selected by the TCCM Write Multiplex when the Preamble or Postamble is written. They cause the all-1's and all-0's characters of the PE Preamble and Postamble to be written.

The fourth set of inputs to the TCCM Write Multiplex are the inverted contents of the multiplex that are fed back from the TCCM Write Buffer. These inverted inputs are used to convert binary inputs to the TCCM Write Multiplex into the Phase Encoded (PE) mode. The TCCM Write Multiplex and Write Buffer operate together to perform this function.

The output of the Write Multiplex is clocked into the Write Buffer. In NRZI mode, this clock occurs once for every character written on tape. In PE mode, the clock occurs twice for every character written: once when normal data is output from the Write Multiplex, and once again when inverted data is output from the Write Multiplex. It is this operation that produces phase encoding in PE mode. Figure 2-5 shows the timing of Write Multiplex-Write Buffer operation for PE and NRZI modes. Note that for NRZI mode the output of the Write Buffer is still in binary form. The output of the TCCM Write Buffer is then applied to signal drivers that transmit the data via the slave bus to the TU45.

In order to write tape mark (TM) characters or IDB, appropriate codes are obtained by clearing selected bits in the Write Buffer and forcing the data lines to their desired values.

The slave bus Write Data line signals are received by slave bus receivers on the MTA module and passed on to the TU45.

Timing for TCCM and Bit Fiddler write operations is derived from WRT CLK, which is generated in the TU45 (M8921) and transmitted to the TM02. WRT CLK is also gated in the TM02 to produce REC pulses, which are transmitted back to the MTA and to the TU45
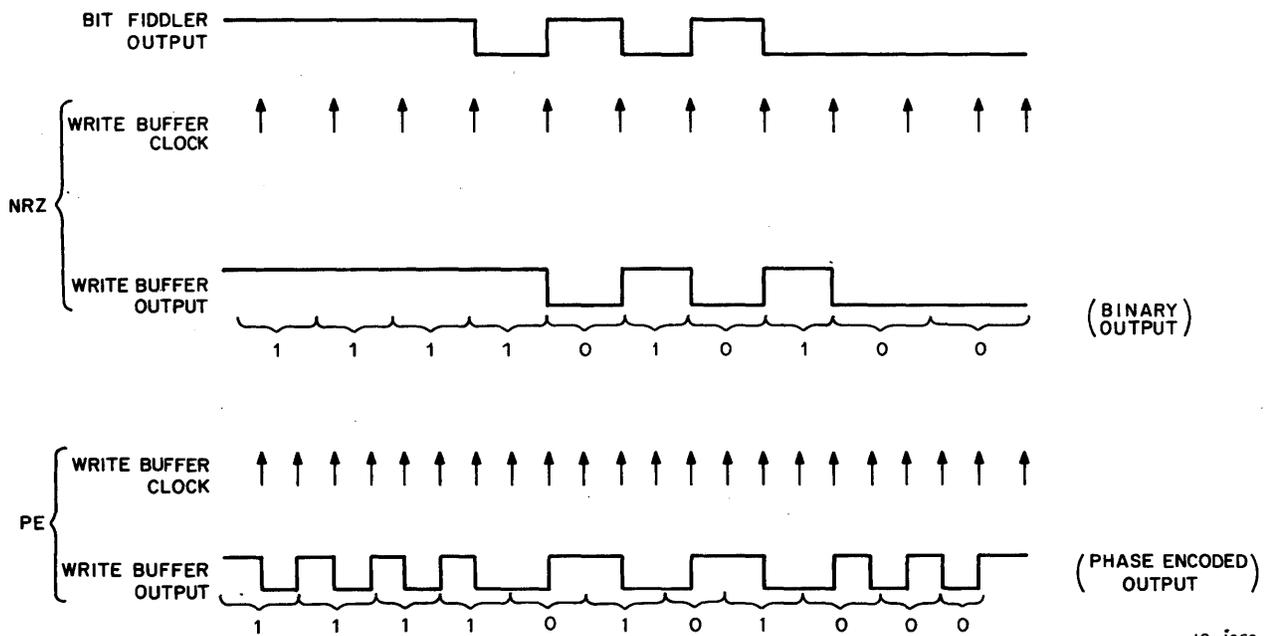
Figure 2-5 TCCM Write Timing

2.4 READ DATA PATH

The read data path, shown in the MTA and TU45/TM02 block diagram (Figure 2-3), is discussed in this section in greater detail (Figure 2-6).

As tape moves past the read heads, flux transitions on the tape cause the read heads to produce positive and negative current pulse outputs. These current pulses are processed in the Read Amplifers of the TU45 to yield voltage levels of the form shown in Figure 2-7. The voltage levels are transmitted by Line Drivers in the MTA across the slave bus Read Data lines to the TM02 TCCM module. The read data is passed through the TCCM Read Multiplex to the three Data Sync (PE) modules and the Tape Control-NRZI module. However, the operation of one of these modules will be disabled, depending on whether the TM02 is operating in PE or NRZI mode.

In NRZI mode, the Tape Control-NRZI module is enabled, and data is strobed from the TCCM Read Multiplex into the Tape Control-NRZI Read Latch by RDS (Read Data Strobe). RDS, generated from RSDO (Read Strobe Delay Over) transmitted from the TU45 occurs when a valid tape character is known to be at the output of the TCCM Read Multiplex. RDS also clocks the CRCC and LRCC Generator, so that the data being read off the tape can be validated at the end of the read operation by comparing the generated CRCC/LRCC against the CRCC and LRCC read off the tape. The contents of the Tape Control-NRZI Read Latch are available to the Maintenance Register module (M8905-YA) multiplex.

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In PE mode, the Tape Control-NRZI circuitry is disabled while the Data Sync and Tape Control-PE modules are enabled. The phase encoded data is input to the Data Sync modules (each module processes three data bits), which sync onto the frequency of the data during the preamble. The PE data on each track is then decoded and stored in the Deskew register. Only when all the bits of a character are available in the Deskew register is the character read from the register. Because the Deskew register has a capacity of 9X8 bits, a skew of 8-1=7 characters can be accommodated by the TM02.

The output of the Deskew register is input to error correction circuitry. If a vertical parity error occurs along with a single dead track error, the data on the dead track is corrected on the fly. The data (minus parity) is then output to the Maintenance Register module multiplex.

The Maintenance Register Multiplex passes the data character through to the Bit Fiddler, were it is loaded into position in the Bit Fiddler Read Data Buffer. When the Read Data Buffer is full (this will require two or more tape characters), the Bit Fiddler issues SCLK to the Massbus Controller.

Read data and SCLK are driven to the Massbus Controller By the Massbus Drivers (M5903 or M5903-YA). When the controller receives SCLK, it strobes in the word on the Data lines of the Massbus.

Figure 2-6 Read Data Path (sheet 1 of 2)
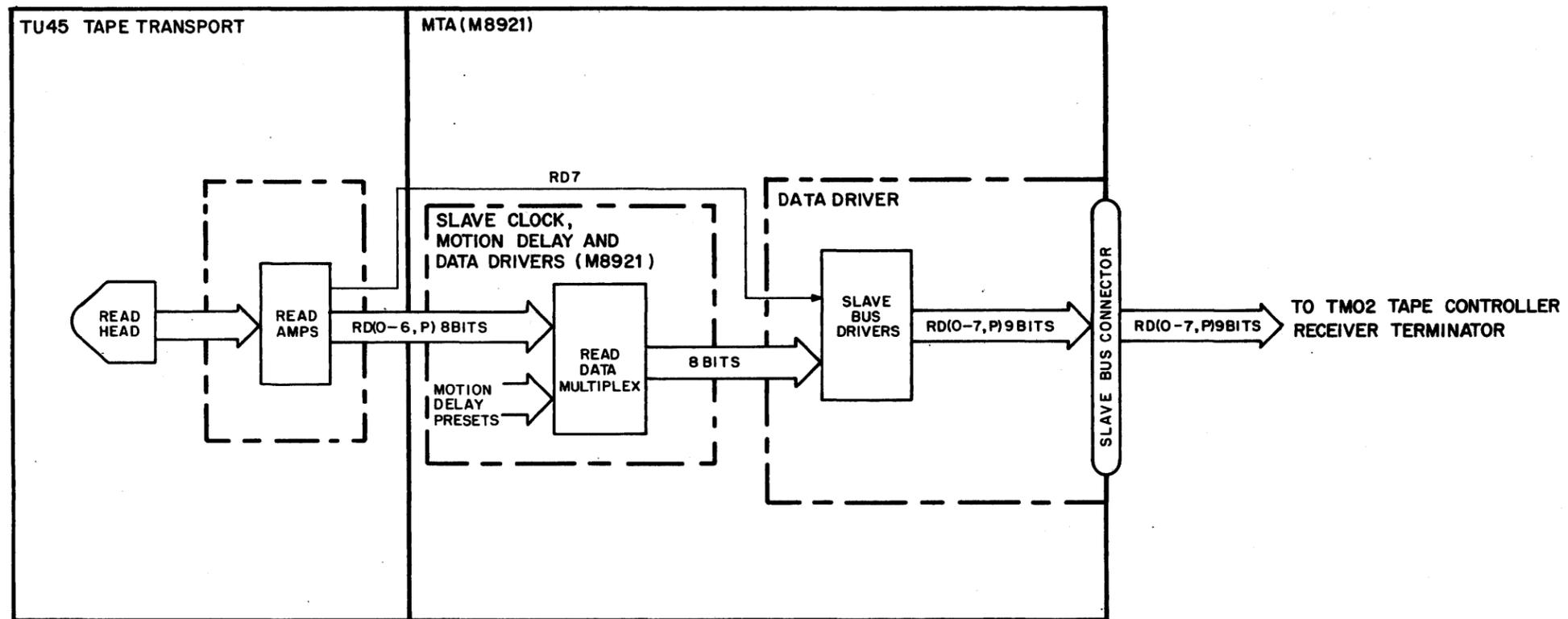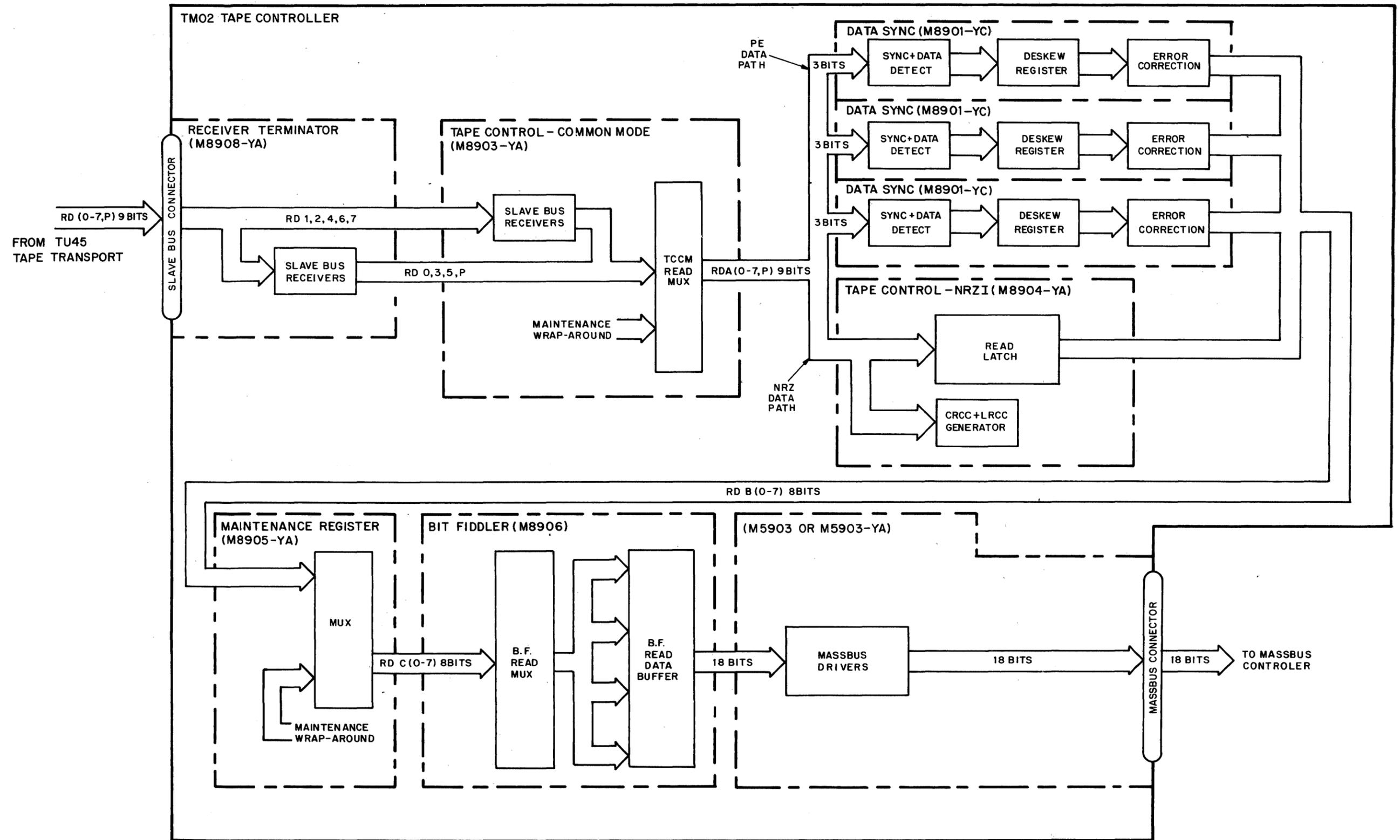
CS-1600

Figure 2-6 Read Data Path (sheet 2 of 2)

CS-1601
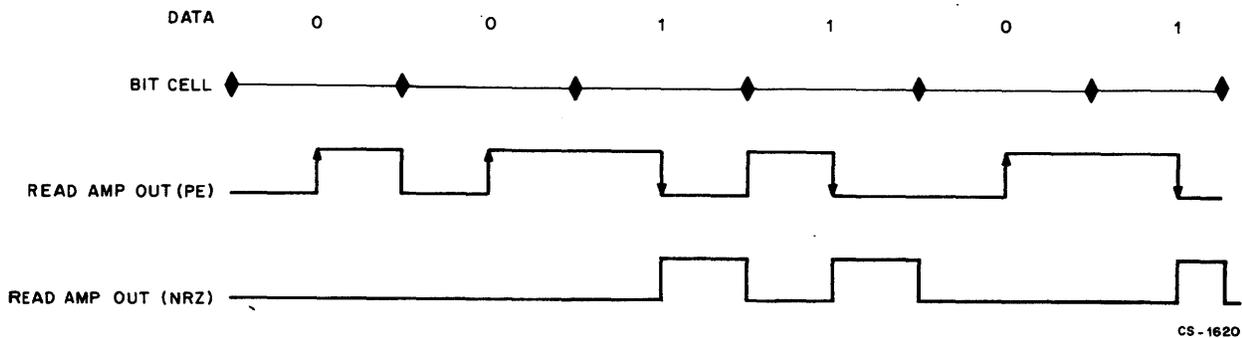
Figure 2-7 Read Amplifier Outputs

2.5   REGISTER FUNCTIONS AND FORMATS

The TM02 contains ten registers, some of which have been mentioned in previous discussions. A summary of the TM02 registers is provided in Table 2-3. Any of the TM02 registers may be read to determine the status of the TU45/TM02 Tape Drive. Some of the registers may be written into, thereby controlling TU45/TM02 functions and operating parameters.

The TM02 registers are read and written into by performing "handshake" operations on the control bus of the Massbus. A register is loaded by the Massbus Controller in the following manner:

1. The controller places the select code of the desired TM02 on the Drive Select lines.

2. The controller places a register select code on the Register Select lines.

3. It asserts CTOD H (Controller To Drive).

4. It places data on the Control lines.

5. The controller then asserts DEM H.

The selected TM02 responds to DEM H and CTOD H asserted by loading the selected register with the data on the Control lines. It then asserts TRA H. The controller responds by negating DEM H, which causes the TM02 to negate TRA H; the write operation is thereby terminated.

A TM02 register is read in a similar manner except that CTOD H is negated (step 3) and step 4 is eliminated. The selected TM02 responds to DEM H asserted and CTOD H negated by gating out the contents of the selected register onto the Control lines. It then asserts TRA H, which, when received by the controller, causes it to strobe in the data on the Control lines and negate DEM H. The TM02 responds by negating TRA H, thereby terminating the operation.

The remainder of Section 2-5 provides a more detailed description of
the TM02 registers and their contents. It is primarily for reference,
and may be skipped during a first reading.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
				DVA*						F/5	F/4	F/3	F/2	F/1	F0/GO

DEFINED BY MASS BUS CONTROLLER   FUNCTION CODE
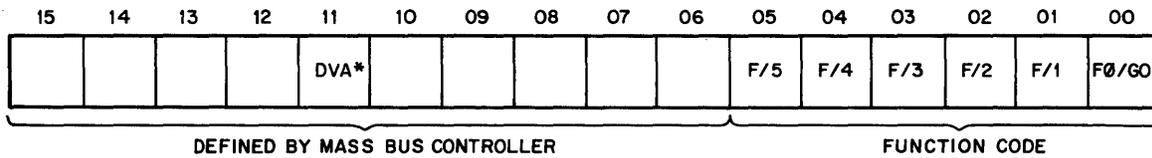
*DRIVE AVAILABLE, HARDWIRED SET

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Figure 2-8 Control Register Format

Table 2-3
TM02 Registers

ADDRESS CODE (OCTAL)	NAME	TYPE	DESCRIPTION
00	Control I (CS1)	Read/write	Contains the function code including the GO bit.
01	Status (DS)	Read only	Contains all non-error status information plus the Error Summary bit.
02	Error (ER)	Read only	Contains all error indications.
03	Maintenance (MR)	Read/write	Controls diagnostic functions.
04	Attention Summary (AS)	Read/write	Indicates the Attention Active status of each TM02 (one bit/TM02).
05	Frame Count (FC)	Read/write	For a data transfer operation, contains the number of tape characters to be transferred. For a space operation, contains the number of records to be spaced.

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06	Drive Type (DT)	Read only	Indicates that transport type and status (e.g., existing TU45 with power applied).
07	Check Character (CK)	Read only	For an NRZI operation, contains the CRC error character.
			For a PE operation, contains the dead track indications.
10	Tape Control (TC)	Read/write	Contains the transport selection and configuration codes.
11	Serial Number (SN)	Read only	Contains the last four digits of the transport serial number.

2.5.1 Control Register (Register 00(8))

The Control register is a read/write register (Figure 2-8) which receives operational commands from the Massbus Controller via the control bus. This register operates in conjunction with the Tape Control register to control the operation of the selected transport.

The TU45/TM02 responds to the 14 function codes listed in Table 2-4. If the Control register is loaded with a fuction code (with GO bit set) that does not agree with those listed in the table, an Illegal Function Error (ILF) is generated. Thus, an ILF is generated for codes 05(8), 12(8), 37(8), but not for 00(8), 02(8), 06(8), 10(8), 20(8), 24(8), 30(8), etc

2.5.2 Status Register (Register 01(8))

The Status register is a 16-bit, read-only register which stores the tape system status information. Figure 2-9 ilustrates the Status register format and Table 2-5 defines the bit positions. Although the Status register multiplexor is located in the TM02, inputs to this multiplexor may be generated either by a selected transport, any transport, or the TM02 logic itself. Because of this fact, each bit position in Table 2-5 is identified by one or more of the following designators to indicate the origin of the input signal.

        (SS) = Selected transport
        (S) = Any transport
        (M) = TM02 logic

2.5.3 Error Register (Register 02(8))

There are 16 different error conditions that can be detected in the TU45/TM02 Tape Drive System. The Error register is a 16-bit, read-only register which stores all of the tape system error indications.

TU45/TM02 errors are categorized as Class A and Class B. A Class B error will terminate an in-progress data transfer; a Class A error will not. However, the Massbus Controller is notified of any error during a data transfer by the immediate assertion of EXC H on the Massbus. If the TU45/TM02 is not performing any operation, or is performing a rewind (i.e., the GO bit is clear), the controller is immediately notified of an error condition by the assertion of ATTN H on the Massbus.

Figure 2-10 illustrates the Error register format and Table 2-6 lists the error bit indicators.

2.5.4 Maintenance Register (Register 03(8))

The Maintenance register(M8905-YA)is a 16-bit, read/write register (Figure 2-11) which allows complete diagnostic testing of the TM02 data paths and error detection circuitry. The Maintenance register can configure the data paths into four wrap-around loops, each loop testing certain TM02 circuits. The Maintenance register data field is part of these loops, and is used to read or write test data into the TM02. The wrap-around modes are discussed in more detail in the Maintenance Modes pamphlet (Section 3.1). Table 2-7 briefly describes the bits of the Maintenance register.

2.5.5 Attention Summary Register (Register 04(8))

The Attention Summary register (M8909, sheet 3) is a read/write "pseudo-register" which consists of from one to eight bits, depending on the number of TM02s in the system. The term "pseudo-register" refers to the fact that only one register bit position is physically contained in each TM02. This bit position reflects the state of the ATA status bit for that TM02. Hence, bit position 0 of the Attention Summary register is generated by the ATA bit of TM02 0, bit position 1 is generated by the ATA bit of TM02 1, and so on to bit 7. Bits 8 through 15 are not used.

Unlike the other drive registers, the Attention Summary register is directly selected by the controller without first addressing a particular TM02. Thus, for a single Attention Summary register read operation, every TM02 in the system responds by placing the state of its ATA bit in the appropriate bit position on the control bus and disabling its remaining 15 control bus transmitters. This control bus configuration appears as a single register output which collectively informs the controller of all TM02s that require attention (i.e., ATA = 1). The controller can then selectively examine the Error or Status registers of each of the affected TM02s to determine the cause of the individual attention conditions.

The controller can also write into the Attention Summary register; however, the significance of the bits being written is unique. Writing a 1 into a bit position resets the ATA bit in the TM02 assigned to that bit position; however, writing a 0 has no effect. This unique writing scheme allows the controller to reset, after inspection, all summary bits that were set, without accidentally resetting those bits that may have become set in the meantime. The following table illustrates the effects of writing into an attention summary bit position:

ATA Bit Before	Summary Bit Written	ATA Bit After
0	0	0
1	0	1
0	1	0
1	1	0

Table 2-4
Command Function Codes

FUNCTION CODE F(0-5) (OCTAL)	OPERATION	DESCRIPTION
01	No Op	Performs no operation. Clears GO bit in Control register.
03	Rewind Off-line*	1. Initiates a rewind on selected transport then places it off-line, and unloads the tape.
		2. Clears GO bit.
		3. Sets the following bits in the Status register:

* Requires manual intervention to return transport on-line.

Drive Ready (DRY)
Slave Status Change (SSC)
Attention Active (ATA)

07	Rewind	1. Initiates a rewind to BOT marker on selected transport and clears the GO bit.
		2. Sets DRY, PIP, and ATA bits in the Status register during rewind.
		3. When BOT is sensed, sets SSC and clears PIP.
11	Drive Clear	Similar to Initialize. Resets all TM02 and selected transport logic only. Does not affect unselected transports.
21	Read-In Preset	Presets the Tape Control register (R10) to select slave 0, odd parity, and 800 bpi NRZI, then causes slave 0 to rewind. It also sets the Format Select bits (bits 04-07 in the Tape Control register) to zeros. (Format Code 0000 is undefined for the 8906 Bit Fiddler. These bits should be loaded with a defined code (Table 2-10) before loading another GO =1).
25	Erase	Erases approximately 3 in. of tape. Clears GO bit and sets ATA on termination.
27	Write Tape Mark	Writes a special tape record on the selected transport. Clears GO bit and sets ATA bit on termination.
31	Space Forward	Moves tape forward (toward EOT) on the selected transport over the number of records specified by the Frame Count register. Aborts space operation if TM or EOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination.

33	Space Reverse	Moves tape in reverse (toward BOT) on the selected transport over the number of records specified by the Frame Count register. Aborts space operation if TM or BOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination.
51	Write Check Forward	Same as Read Forward.
57	Write Check Reverse	Same as Read Reverse.
61	Write Forward	Writes forward one tape record on the selected transport. Record length is determined by Frame Count register. Clears GO bit on command termination.
71	Read Forward	Reads forward one tape record on the selected transport. Clears GO bit on command termination.
77	Read Reverse	Reads reverse one tape record on the selected transport. Clears GO bit on command termination.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	EOT		DPR	DRY	SSC	PES	SDWN	IDB	TM	BOT	SLA

NOT USED
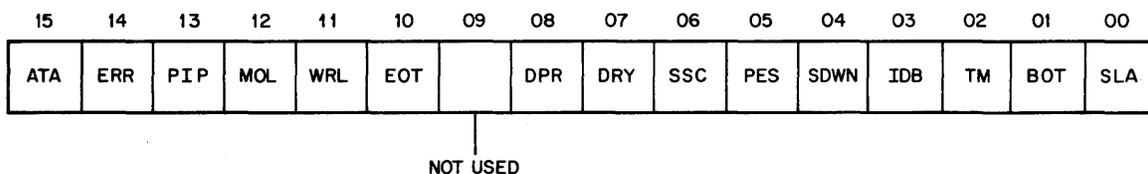
10-1275

Figure 2-9 Status Register Format

Table 2-5
Status Register Bit Positions

BIT POSITION	NAME	DESCRIPTION
00 (SS)	Slave Attention (SLA)	Indicates that a selected transport has come on-line.

01 (SS)	Beginning of Tape (BOT)	Indicates that a selected transport has detected the BOT marker.
02 (M)	Tape Mark (TM)	Indicates that a tape mark has been detected. Remains asserted until the next tape motion operation is initiated.
03 (m)	Identification Burst (IDB)	Indicates that a Phase Encoded (PE) identification burst has been detected. Asserted until a subsequent tape motion command is initiated.
04 (SS)	Settle Down (SDWN)	Indicates that tape motion on the selected transport is stopping.
05 (SS)	Phase Encoded Status (PES)	Indicates that the selected transport is configured for PE operation. Is negated during \NRZI operation.
06(S)	Slave Status Change (SSC)	Indicates that any transport has just gone on-line or off-line, or has completed a rewind operation.
07 (M)	Drive Ready (DRY)	Indicates that both the TM02 and the selected transport are ready to accept a command.
08 (M)	Drive Present (DPR)	Hardwired set.
09	Not used	
10 (SS)	End of Tape (EOT)	Indicates that the selected transport has detected the EOT marker during forward tape motion. Is negated when the EOT marker is detected during reverse tape motion.
11 (SS)	Write Lock (WRL)	Indicates that the selected transport is write protected.
12 (SS)	Medium On-Line (MOL)	Indicates that the selected transport has tape loaded and is on-line.

13 (M/SS)	Positioning in Progress (PIP)	Indicates that the selected transport is performing a tape motion operation. This bit is asserted by the TM02 (M) during a space or by the selected transport (SS) during a rewind.
14 (M)	Composite Error (ERR)	Indicates that an error condition has occurred. Is asserted whenever any bit in the Error register is set.
15 (M)	Attention Active (ATA)	Is asserted whenever the ATTN L interface signal is generated. Indicates one of the following:

1. The TM02 and the selected transport require servicing.

2. The TM02 and the selected transport have become ready after a nontransfer operation.

3. A transport status change has occurred.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
COR/CRC	UNS	OPI	DTE	NEF	CS/ITM	FCE	NSG	PEF/LRC	INC/VPE	DPAR	FMT	CPAR	RMR	ILR	ILF

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Figure 2-10 Error Register Format

**Table 2-6
Error Register Bit Indicators**

BIT POSITION	NAME	TYPE	DESCRIPTION
00	Illegal Function(ILF)	Class B	Indicates that an illegal function code has been transmitted.

01	Illegal Register(ILR)	Class A	Indicates that a read or write from a nonexistent register is attempted.
02	Register Modification Refuse(RMR)	Class A	Indicates that during a transport operation (GO = 1), a write into one of the registers is attempted. (Does not apply for the Maintenance or Attention Summary register).
03	Control Bus Parity (CPAR)	Class A	Indicates that incorrect control bus parity is detected.
04	Format(FMT)	Class B	Indicates that a data transfer with an incorrect format code was attempted.'
05	Data Bus Parity Error (DPAR)	Class A	Indicates that incorrect data bus parity has occurred.
06	Incorrectable Data Error or Vertical Parity Error (INC/VPE)	Class A	During a PE read operation, indicates that one of the following has occurred:

1. Multiple dead tracks
2. Dead tracks without parity errors
3. Parity errors without dead tracks
4. Skew overflow

During an NRZI read operation, indicates that a verical parity error has occurred.

07	Format Error or LRC (PEF/LRC)	Class A	During a PE read operation, indicates that an incorrect preamble or postamble is detected.
		Class A	During an NRZI write operation, indicates that the read-after-write LRCC does not match the LRCC computed during the write.

08	Nonstandard Gap(NSG)	Class A	Indicates that a tape character is detected during the first half of the EOR.
09	Frame Count Error(FCE)	Class A	Indicates that a space operation has terminated and the Frame Counter is not cleared. Also asserted when the Massbus Controller fails to negate RUN when the TM02 asserts EBL.
10	Correctable Skew or Illegal Tape Mark (CS/ITM)	Class A	During a PE read operation, indicates that excessive but correctable skew is detected. (This condition is only a warning and does not indicate bad data).
			During an NRZI read, indicates that characters not legally a tape mark have been read and recognized as a tape mark.
11	Nonexecutable Function (NEF)	Class B	Indicates one of the following:

1. A write operation is attempted on a write-protected transport.

2. A space reverse, read reverse, or write check reverse is attempted when the tape is at BOT.

3. The DEN2 bit in the Tape Control register does not agree with the PES status bit.

4. A space or write operation is attempted when FCS=0 in the Tape Control register.

			5. A read or write operation is attempted with DEN2=0 in the Tape Control register and the 2's complement of a number less than 13 is in the Frame Count register.
12	Drive Timing Error (DTE)	Class B	Indicates one of the following:
			1. During a write operation, WCLK was not received from the Massbus Controller in time to provide a valid tape character.
			2. A data transfer (read/write) was attempted when the data bus of the Massbus was already occupied.
13	Operation Incomplete (OPI)	Class B	During a read or space operation, indicates that a tape record has not been detected within 4.2 sec from command initiation (25 feet).
			During a write operation, indicates that a read-after-write tape record has not been detected within 0.42 sec from command initiation (31 inches).
14	Unsafe(UNS)	Class B	Indicates one of the following:
			1. A program-controlled operation is attempted on a selected transport which is not on-line.
			2. An imminent power failure is detected (AC LO L).

15   Correctable Data Error   Class A   During a PE read operation,
            or CRC Error(COR/CRC)   indicates that a single
                                                    dead track has occurred.

                                                    During an NRZT operation,
                                                    indicates that the CRCC
                                                    read off the tape does not
                                                    match the CRCC computed
                                                    from the data read off the
                                                    tape.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MDF8	MDF7	MDF6	MDF5	MDF4	MDF3	MDF2	MDF1	MDF0	SWC2	MC	MOP3	MOP2	MOP1	MOP0	MM

MAINTENANCE DATA FIELD   SWC   MODE OF OPERATION
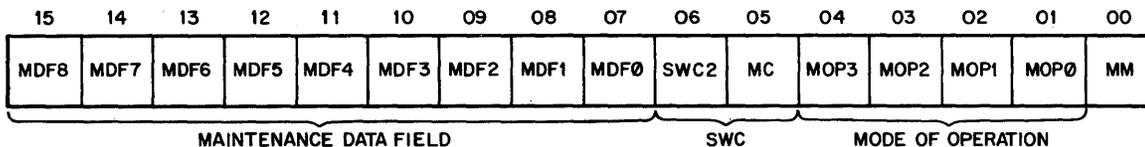
10-1277

Figure 2-11 Maintenance Register Format

Table 2-7
Maintenance Register Bit Positions

BIT POSITION	NAME	DESCRIPTION
00	Maintenance Mode(MM)	When set, configures the TM02 for maintenance mode operation.
01	Maintenance Operation Code (MOP0-3)	Controls command execution during the maintenance mode. (MM and MOP function together to alter normal command execution during maintenance mode operation).
05	Maintenance Clock(MC)	Controls data sequencing through the TM02 data path in maintenance mode.
06	Selected Slave Clock(SWC)	This is the WRT CLK signal generated by the selected slave.

07-15   Maintenance Data Field   Buffers the data
                   (MDF0-8)   generated   during
                                                     wrap-around operations.

                                                     At the end of normal NRZI
                                                   transfers, contains the
                                                   LRC of the last record.

2.5.6 Frame Count Register (Register 05(8))

The Frame Count register (M8909, sheet 8) is a 16-bit, read/write register that counts tape events. During a data transfer operation (read/write), this register is incremented each time a tape character is transferred to or from the tape. However, during a space operation, this register is incremented each time a record is detected. The register output may be read by the controller at any time; but the controller can only write into this register when the transport is not performing a space or data transfer (GO negated).

For a write operation, the Frame Count register is loaded, prior to write initiation, with the 2s complement of the number of tape characters to be written. During the writing process, the Frame Count register is incremented each time a tape character is recorded. Normal write data transfer termination is accomplished when the Frame Count register overflows to zero. For a space operation, the Frame Count register functions similarly to a write, except it is loaded with the 2s complement of the number of records to be spaced and is then incremented each time a record is detected. Space termination is accomplished when the register overflows to zero. For a read operation, this register is automatically reset prior to read initiation. The register is then incremented each time a tape character is read. Thus, at the end of the read operation, the Frame Count register contains a count of the number of characters read.

2.5.7 Drive Type Register (Register 06(8))

The Drive Type register (M8903-YA) is a 16-bit, read-only register, the contents of which identifies the pariticular type of storage device (transport) being used. When a read from the Drive Type register is performed, the register output is applied to the appropriate multiplexor bit positions. The remaining bit positions are forced reset, and hence the 8-bit output of the Drive Type register presents a 16-bit format to the controller.

Bits 0 through 8 (DT0-8) of the Drive Type register identify the type and status of the selected transport. If a nonexistent transport is selected or if the selected transport is not powered up, DT0-8 will contain 010(8). If the selected transport is powered up, but is not a TU45, DT0-8 will contain 011(8) or 013(8) to 017(8), depending on the type of transport. If the selected transport is a TU45 and is powered up, these bit positions will contain 012(8).

Figure 2-12 illustates the Drive Type register format and Table 2-8 briefly describes each bit position.

2.5.8 Check Character Register (Register 07(8)).

The Check Character register (M8905-YA) is a nine-bit, read-only register which permits the programmer to check the validity of a data transfer. At the end of an NRZI read operation, this register contains the CRCC for that operation. Hence, the programmer can determine if the CRCC generator logic is functioning properly. At the end of PE read operation, however, this register contains a dead track indication (DT=1) of any track which may have dropped one or more bits during the operation.

Figure 2-13 illustrates the Check Character register format for both NRZI and PE modes.

2.5.9 Tape Control Register (Register 10(8))

The Tape Control register (M8905-YA) is a 16-bit, read/write register which selects an existing transport and configures it to a particular operational mode.

Figure 2-14 illustrates the Tape Control register and Table 2-9 briefly describes each bit position.

2.5.10 Serial Number Register (Register 11(8))

The Serial Number register (M8921) is a 16-bit, read-only register which contains a BCD representation of the four least-significant digits of the transport serial number. This register is located on the MTA module and the register inputs are hardwired to the BCD configuration of the least-significant serial number digits. The Serial Number register does not function during the test mode.

Figure 2-15 illustrates the Serial Number register format

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
NSA	TAP	MOH	7CH	DRQ	SPR										

NOT USED (09)

DRIVE TYPE (0-8)

10-1278
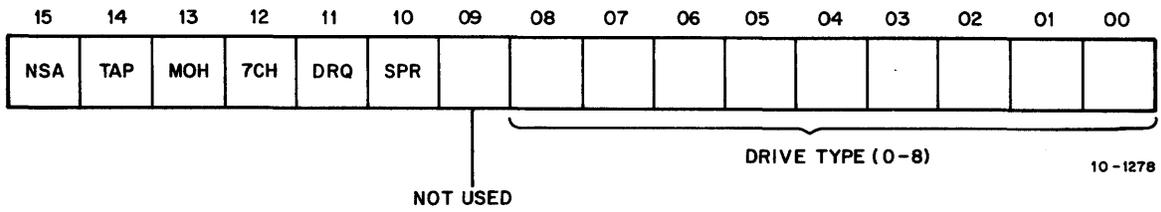
Figure 2-12 Drive Type Register Format

A. NRZ FORMAT

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
							CRC PAR	CRC 7	CRC 6	CRC 5	CRC 4	CRC 3	CRC 2	CRC 1	CRC 0

NOT USED

B. PE FORMAT

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
							DT4 PAR	DT7-	DT6	DT5	DT3	DT9	DT1	DT8	DT2

NOT USED

10-1273
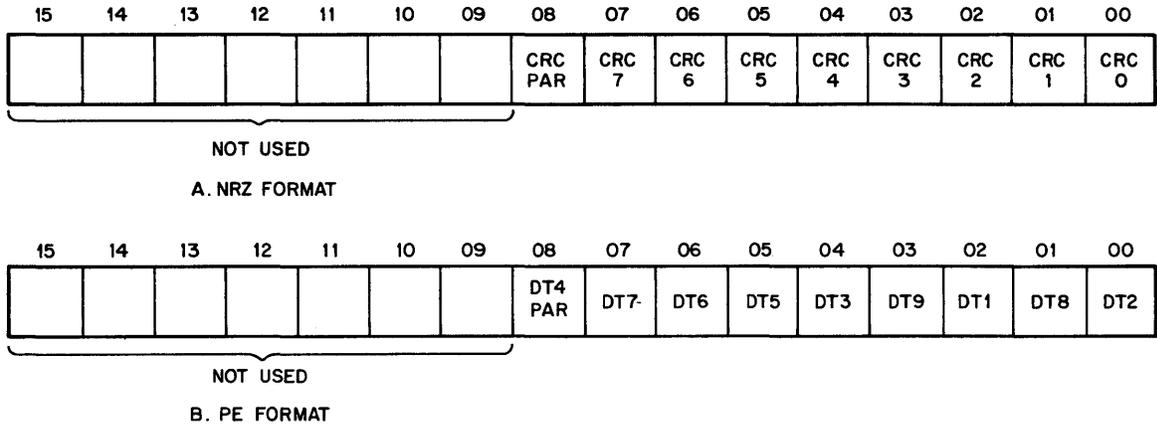
Figure 2-13 Check Character Register Format

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ACCL	FCS	TCW	EAO DTE		DEN 2	DEN 1	DEN 0	FMT SEL 3	FMT SEL 2	FMT SEL 1	FMT SEL 0	EV PAR	SS2	SS1	SS0

NOT USED (11)

10-1279
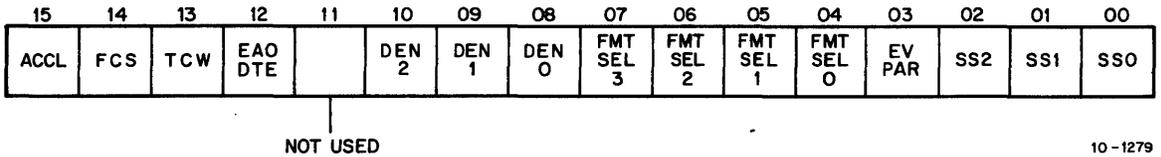
Figure 2-14 Tape Control Register Format

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SN15	SN14	SN13	SN12	SN11	SN10	SN9	SN8	SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0

4th DIGIT | 3rd DIGIT | 2nd DIGIT | 1st DIGIT

10-1272
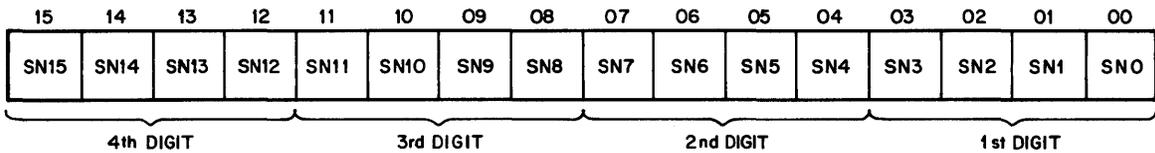
Figure 2-15 Serial Number Register Format

Table 2-8
Drive Type Register Bit Positions

BIT POSITION	NAME	DISCRIPTION
00-08	Drive Type(DT0-8)	Specifies the drive type (012(8) = TU45).
10	SLAVE PRESENT(SPR)	Asserted when a transport is powered up and has been assigned the selection code contained in the Tape Control register.
11	Drive Request Required(DRQ)	Always negated to indicate that the device is a single-port unit.
12	7-Channel(7-CH)	Asserted if the selected transport is a 7-channel unit. Negated if the selected transport:

1. Is a 9-channel unit.
2. Does not have power applied.
3. Is disconnected from the slave bus.

13	Moving Head(MOH)	Always negated to indicate that the device is not a moving head unit.
14	Tape Drive(TAP)	Always asserted to indicate that the device is a tape transport.
15	Not Sector Addresses(NSA)	Always asserted to indicate that the device is not sector addressable.

Table 2-9
Tape Control Register Bit Positions

BIT POSITION	NAME	DESCRIPTION
00-02	Slave Select(SS0-2)	Specifies the unit number of the transport to be used.
03	Even Parity(EV PAR)	When set for NRZI operation, even parity is written or read from tape. Ignored during PE operation.
04-07	Format Select (FMT SEL0-3)	Specifies Massbus-to-tape character formatting during a write operation, or tape character-to-Massbus formatting during a read (Table 2-10).
08-10	Density Select(DEN0-2)	Specifies the tape character density during read or write operations as follows:

DEN2 DEN1 DEN0 Density
                     (bpi)

DEN2	DEN1	DEN0	Density (bpi)	
0	0	0	200	
0	0	1	556	NRZI
0	1	0	800	
1	0	0	1600	PE
1	0	1		
1.	1	0		Reserved
1	1	1		

BIT POSITION	NAME	DESCRIPTION
11	Not used	
12	Enable Abort on Data Transfer Errors(EAODTE)	When set, immediately aborts a write or read operation for one of the following errors:

1. COR/CRC - Error register bit 15.
2. FMT/LRC - Error register bit 7.
3. INC/VPI - Error register bit 6.
4. DPAR - Error register bit 5.

13	Frame Count Status(FCS)	Is normally set at the end of a write into the Frame Count register. However, if FCS=0, and a space or write command with GO=1 is loaded, a nonexecutable function (NEF) error is generated and the command is not executed. Is reset when Frame Count register overflows.
14	Tape Control Write(TCW)	Is set when Tape Control register is written into. Is cleared with any tape motion command.
15	Acceleration(ACCL)	This read-only bit is asserted when the transport is not actively reading or writing data.

Table 2-10
Format Select Codes

Code	Description
1100	Normal
1101	Core Dump
1110	15 Normal

See Notes.

NOTES

Codes 1100-1110 use an M8906 Data Formatting module.

An invalid code causes a Format Error (FMT - Error register bit 4) when a data transfer command with GO = 1 is loaded.

2.6 OPERATIONAL SEQUENCES

This section discusses the sequencing that occurs when the TU45/TM02 performs functional operations. Each operation is described separately to simplify the presentation. However, this does cause considerable redundancy, especially for similar operations. If the equipment is down and time is critical, it is recommended that only applicable portions of this section be read.

2.6.1 Rewind

A program-controlled rewind operation may be initiated by one of two commands from the processor. One of these commands (07(8)) performs the rewind operation and retains the transport on-line. The other command (03(8)) places the transport off-line immediately after command initiation. Following completion of the 03(8) command, the operator must reload tape and use the ON-LINE/OFF-LINE switch on the transport status bit indicators (Table 2-5), both rewind commands function identically.

Figure 2-16 illustrates the major functional sequences of a rewind operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.
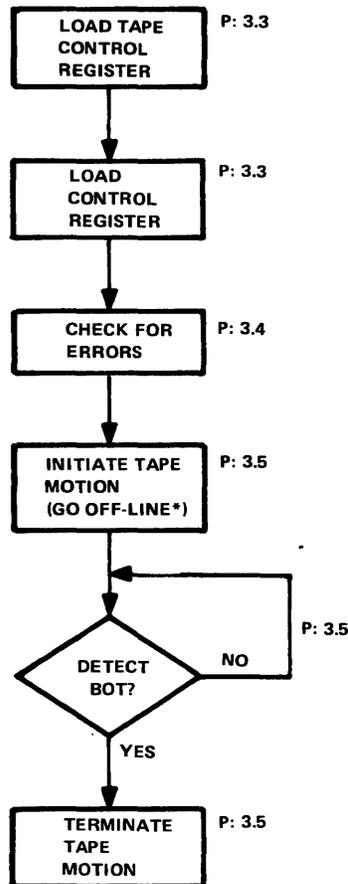
Figure 2-16 Rewind Operation Flowchart

2.6.1.1 Command Initiation - To initiate a program-controlled rewind operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register (R10), selecting the slave desired to perform the rewind operation. The TM02 places the Slave Select bits of the Tape Control register on the slave bus. The Massbus Controller then writes the operational function code of the rewind command (03(8) or 07(8)) into the Control register (R00). The TM02 decodes the fuction code and asserts RWND L on the slave bus. (If a rewind-off-line operation has been specified, the TM02 also asserts WRITE L). It then checks for errors, and, if there are none, issues SLAVE SET Pulse and STOP L to the TU45, and clears the GO bit in the Control register.

2.6.1.2 Command Execution - The TU45, enabled by its address code on the Slave Select lines (SS 0-2), responds to SLAVE SET Pulse by setting a Rewind Status flip-flop (if WRITE L is also asserted, it also places itself off-line), which activates the capstan drive for a high-speed (250 in/sec) operation independently, and the Massbus Controller and TM02 may divert attention to other transports.

2.6.1.3 Command Termination - When the refective beginning-of-tape (BOT) marker is detected, the TU45 terminates its high-speed reverse motion, but will overshoot the BOT marker. The TU45 then inititates forward tape motion at read/write speed (75 in/sec). When it encounters the BOT marker again, the Rewind Status flip-flop is reset and the capstan motor is deactivated. When the TU45 has completed its rewind operation, it asserts SET SSC (Slave Status Change) on the slave bus. This causes the attention bit in the TM02 to be set, which results in ATTN H being asserted on the Massbus, thereby notifying the Massbus controller.

2.6.2 Space

Figure 2-17 illustrates the major functional sequences of a space operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.

2.6.2.1 Command Initiation - To initiate a space operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register, selecting the slave desired to perform the space operation. The TM02 places the Slave Select bits of the Tape Control register on the slave bus.

The Massbus Controller then loads the 2's complement of the number of
tape records to be spaced into the TM02 Frame Count register.
Following this, the controller loads the Control register with the
operational fuction code of the space command (31(8) for space
forward, 33(8) for space reverse). The TM02 decodes the fuction code
and asserts FWD L or REV L on the slave bus. It then checks for
errors, and, if there are none, issues SLAVE SET Pulse and EMD to the
TU45.

2.6.2.2 Command Execution - The TU45 which is enabled by its address
code on the Slave Select lines (SS 0-2), responds to SLAVE SET Pulse
by setting a motion control flip-flop (forward or reverse) in MTA
module (M8921), which activates the capstan drive for forward or
reverse motion (75 in/sec).

The selected TU45 also responds to EMD from MTA, multiplexing motion
delay presets onto the Read Data lines of the slave bus. The TM02
uses the presets to generate a motion delay, at the end of which the
read heads will detect a record. (As the tape moves under the read
heads, tape characters are detected exactly as they are during a read
operation; however, Bit Fiddler operation is suppressed).

When the end of the record, i.e., IRG (Interrecord Gap), is detected,
a signal (RECORD H) from the TCCM module increments the Frame Count
register, and another motion delay is generated. At the end of this
motion delay, STOP L is asserted on the slave bus and causes the
motion control flip-flop in the MTA module to be reset. Soon after,
however, another SLAVE SET Pulse from the TM02 sets this flip-flop
again, as another motion delay is generated. At the end of this
motion delay, the read heads will detect the next record. At the end
of this record, the Frame Count register is again incremented and
another motion delay occurs. This sequence continues for all the
records spaced. Because the resetting and setting of the MTA motion
control flip-flops takes place within approximately 1 microsecond, the
space operation will be performed at a constant speed (75 in/sec).

2.6.2.3 Command Termination - After the last record has been spaced,
the Frame Count register will overflow to zero. This will inhibit a
SLAVE SET Pulse to the TU45; the motion control flip-flop will not be
reset. The capstan will remain deactivated, and tape motion will be
terminated. If BOT, EOT, or TM are detected before the Frame Count
regster overflows, tape motion will also be terminated. Upon
detection of BOT, EOT, TM or frame count overflow, the GO bit of the
Control register is cleared.
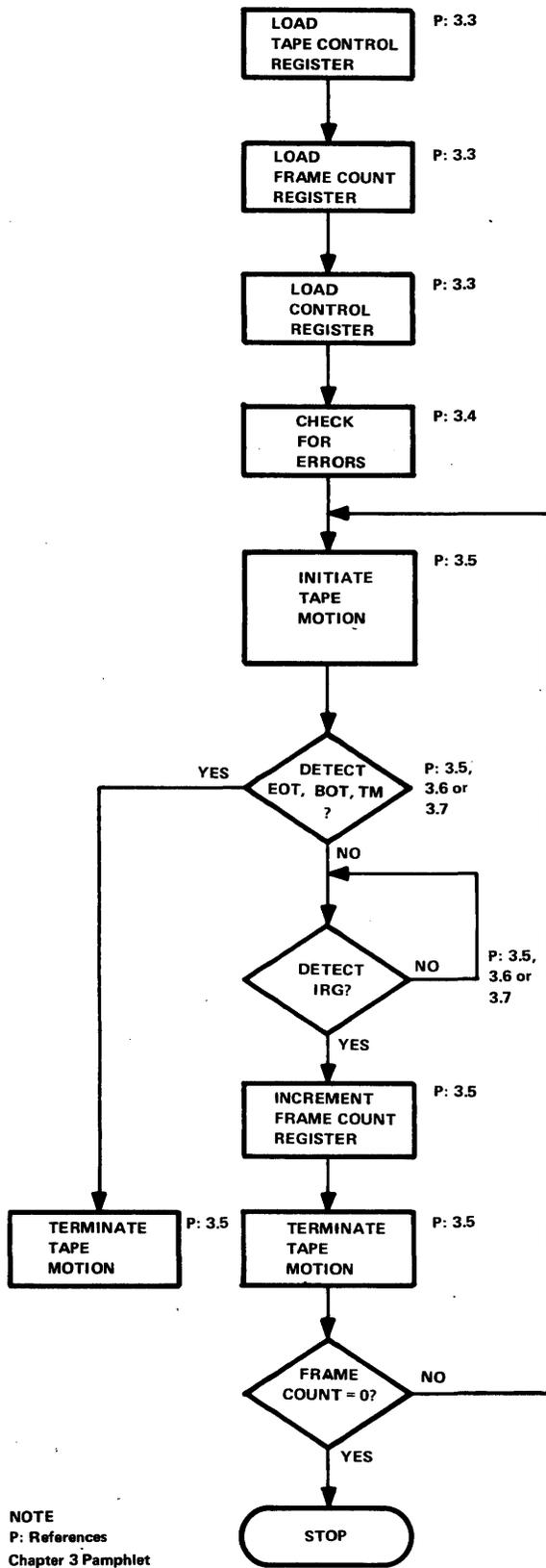
Figure 2-17 Space Operation Flowchart

2.6.3 Erase

Figure 2-18 illustrates the major functional sequences of an erase operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.
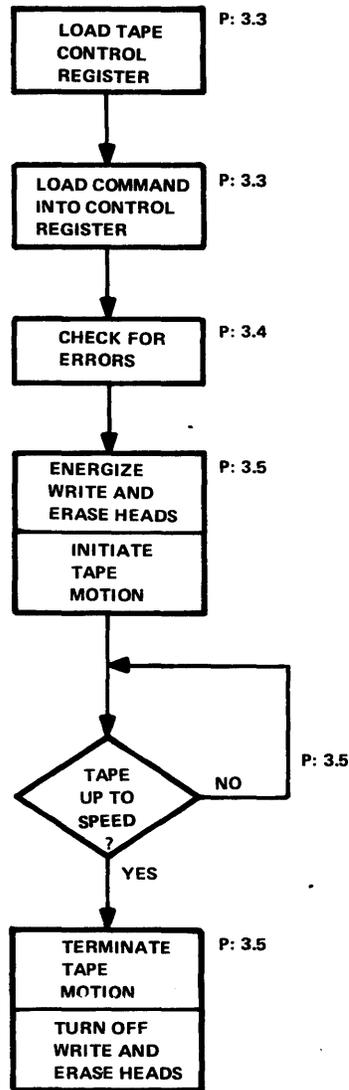
```
        ┌─────────────────┐  P: 3.3
        │   LOAD TAPE      │
        │   CONTROL        │
        │   REGISTER       │
        └─────────────────┘
                 │
                 ▼
        ┌─────────────────┐  P: 3.3
        │ LOAD COMMAND     │
        │ INTO CONTROL     │
        │ REGISTER         │
        └─────────────────┘
                 │
                 ▼
        ┌─────────────────┐  P: 3.4
        │   CHECK FOR      │
        │   ERRORS         │
        └─────────────────┘
                 │
                 ▼
        ┌─────────────────┐  P: 3.5
        │   ENERGIZE       │
        │   WRITE AND      │
        │   ERASE HEADS    │
        ├─────────────────┤
        │   INITIATE       │
        │   TAPE           │
        │   MOTION         │
        └─────────────────┘
                 │        ◄──────────┐
                 ▼                    │
              ╱─────╲                 │
             ╱ TAPE  ╲                │  P: 3.5
            ╱ UP TO   ╲   NO          │
            ╲ SPEED   ╱──────────────┘
             ╲   ?   ╱
              ╲─────╱
                 │ YES
                 ▼
        ┌─────────────────┐  P: 3.5
        │   TERMINATE      │
        │   TAPE           │
        │   MOTION         │
        ├─────────────────┤
        │   TURN OFF       │
        │   WRITE AND      │
        │   ERASE HEADS    │
        └─────────────────┘

NOTE
P: REFERENCES
CHAPTER 3 PAMPHLET

                     10-1251
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Figure 2-18 Erase Operation Flowchart

2.6.3.1 Command Initiation - To initiate an erase operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register, selecting the slave desired to perform the erase operation. The TM02 places the Slave Select bits of the Tape Control register on the slave bus. The Massbus Controller then loads the TM02 Control register with the operational function code (25(8)) of the erase command. The TM02 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, issues SLAVE SET Pulse and EMD (Enable Motion Delay) to the TU45.

2.6.3.2 Command Execution - The TU45 which is enabled by its address code on the Slave Select lines, responds to SLAVE SET Pulse by setting its Forward motion and Write Enable flip-flops, which activate the capstan drive (starting forward tape motion) and the write and erase heads. It also responds to EMD by gating out a motion delay preset onto the slave bus Read Data lines. The preset is loaded into a counter in the TCCM module, which is then counted up. When a count of 2 to the 14th power is reached. tape motion is considered to be up to speed.

Since the erase head is activated and the write heads receive no data input during an erase operation, all the tape moving past the erase head will be dc erased.

2.6.3.3 Command Termination - When the start motion delay is over, another motion delay is started. At the end of this second (stop) motion delay, the TM02 asserts STOP L on the slave bus. STOP L causes the Forward motion control flip-flop to be reset, thereby deactivating the capstan motor. STOP L also causes the GO bit of the Control register to be cleared. When tape motion has ceased, the Write Enable flip-flop is cleared, de-energizing the write and erase heads.

2.6.4 PE Data Read

Figure 2-19 illustrates the major functional sequences of a PE read operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.

2.6.4.1 Command Initiation - To initiate PE read operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register, specifying selected slave TU45, tape character format, and tape data density (1600 bpi for PE).

2-48

LOAD TAPE CONTROL REGISTER — P: 3.3

LOAD COMMAND INTO CONTROL REGISTER — P: 3.3

CHECK FOR ERRORS — P: 3.4

RECEIVE RUN H

INITIATE TAPE MOTION — P: 3.5

TAPE UP TO SPEED ? — NO / YES

DETECT/READ PREAMBLE — P: 3.6

READ n DATA* CHARACTERS — P: 3.6

CONVERT DATA CHARACTERS INTO 18 BIT WORD TRANSMIT WORD — P: 3.8 or 3.9

DETECT POSTAMBLE ? — P: 3.6 — NO / YES

TERMINATE TAPE MOTION — P: 3.5
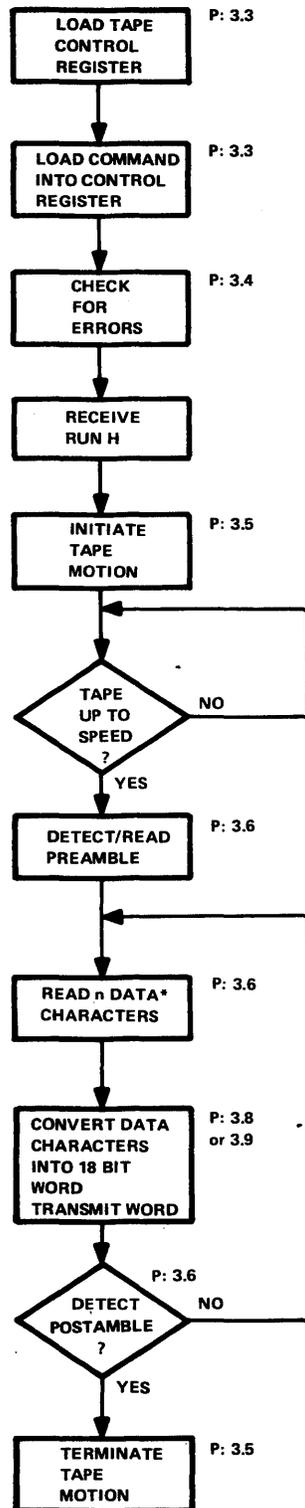
NOTE   *n depends on selected format
P: REFERENCES
CHAPTER 3 PAMPHLET   10-1248

Figure 2-19 PE Read Operation Flowchart

The TM02 places the slave select (SS 0-2) and density (DEN 0-2) bits of the Tape Control register on the slave bus. The Massbus Controller then loads the TM02 Control register with the operational function code of a read operation (71(8) read forward, 77(8) read reverse, 51(8) write check forward, or 57(8) write check reverse) and asserts RUN on the Massbus. The TM02 decodes the function code and asserts FWD L or REV L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus. The TM02 then transmits SLAVE SET Pulse to the SLAVE and initiates a motion delay.

2.6.4.2 Command Execution - The TU45, which is enabled by its address code on the Slave Select lines (SS 0-2) of the slave bus, responds to SLAVE SET Pulse by setting a motion control flip-flop (forward or reverse), thereby activating the capstan drive motor and tape motion.

As the tape accelerates, the TM02 PE read circuitry checks for a PE Identification Burst (IDB) and begins looking for a preamble. When the tape is at speed, the preamble will be detected and read; the tape characters immediately after the preamble all-1's character are data characters. These are deskewed in the Data Sync (M8901-YC), and Tape Control-PE (M8902-YA logic), and sent to the Bit Fiddler (via the Maintenance Register module), which assembles the characters into 18-bit data words and places them on the data bus. When a data word is assembled, the Bit Fiddler notifies the Massbus Controller, which then strobes in the data on the data bus. The Bit Fiddler continues this assembly of data characters into 18-bit words until the first character of the postamble is detected.

2.6.4.3 Command Termination - The TM02 reads the postamble, which signifies the end of the record and asserts EBL H (End of Block) on the Massbus. When the postamble has been read, a motion delay sequence is initiated, at the end of which STOP L is asserted on the slave bus. STOP L resets the motion flip-flop in the TU45 and terminates tape motion. It also clears the GO bit in the Control register, which causes OCC to be negated on the Massbus.

2.6.5 NRZI Read

Figure 2-20 illustrates the major functional sequences of an NRZI read operation and the following paragraphs describe this operation in slightly greater depth. Each functinal box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.

```
          P: 3.3
    ┌─────────────┐
    │ LOAD TAPE   │
    │ CONTROL     │
    │ REGISTER    │
    └─────────────┘
          │
          ▼           P: 3.3
    ┌─────────────┐
    │ LOAD COMMAND│
    │ INTO CONTROL│
    │ REGISTER    │
    └─────────────┘
          │
          ▼           P: 3.4
    ┌─────────────┐
    │ CHECK  FOR  │
    │ ERRORS      │
    └─────────────┘
          │
          ▼
    ┌─────────────┐
    │ RECEIVE     │
    │ RUN H       │
    └─────────────┘
          │
          ▼           P: 3.5
    ┌─────────────┐
    │ INITIATE    │
    │ TAPE        │
    │ MOTION      │
    └─────────────┘
          │
          ▼
         ╱╲
        ╱  ╲    NO
       ╱TAPE╲──────┐
       ╲UP TO╱     │
        ╲SPEED     │
         ╲?╱       │
          │        │
         YES       │
          │
          ▼           P: 3.7
    ┌─────────────┐
    │ READ n DATA*│
    │ CHARACTERS  │
    └─────────────┘
          │
          ▼           P: 3.8
    ┌─────────────┐   or 3.9        ┌─────────────┐
    │ CONVERT DATA│                 │ GENERATE    │  P: 3.7
    │ CHARACTERS TO│                │ CRCC LRCC   │
    │ 18-BIT WORD AND│              └─────────────┘
    │ TRANSMIT WORD │
    └─────────────┘
          │
          ▼
         ╱╲
    NO  ╱END╲
   ─────╲OF DATA╱
        ╲RECORD?╱
          │
         YES
          │
          ▼           P: 3.7
    ┌─────────────┐
    │ READ        │
    │ CRCC        │
    │ LRCC        │
    └─────────────┘
          │
          ▼           P: 3.5
    ┌─────────────┐
    │ TERMINATE   │
    │ TAPE MOTION │
    └─────────────┘
```

*n is determined
by selected format
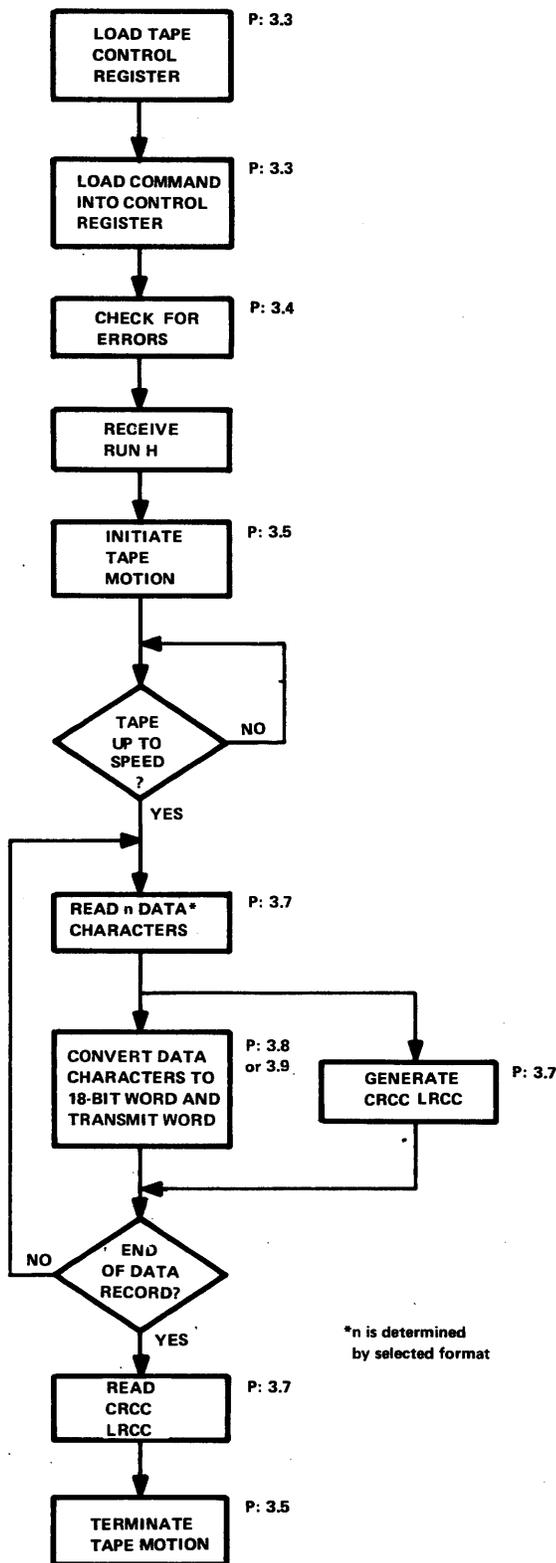
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Figure 2-20 NRZI Read (Forward) Operation Flowchart

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2.6.5.1 Command Initiation - To initiate an NRZI read operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register, specifying selected slave TU45, tape character format, and tape data density. The TM02 places the Slave Select (SS 0-2) and Density (DEN 0-2) bits of the Tape Control register on the slave bus. The Massbus Controller then loads the TM02 Control register with the operational function code of a read operation (71(8) read forward, 77(8) read reverse 51(8) write check forward, or 57(8) write check reverse) and asserts RUN H on the Massbus. The TM02 decodes the function code and asserts FWD L or REV L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus. The TM02 then transmits SLAVE SET Pulse to the SLAVE, and initiates a motion delay.

2.6.5.2 Command Execution - The TU45, which is enabled by its address code on the Slave Select lines (SS 0-2) of the slave bus, responds to SLAVE SET Pulse by setting a motion control flip-flop (forward or reverse), thereby activating the capstan drive motor and tape motion. When the motion delay has timed out, the TM02 negates ACCL L on the slave bus.

When a tape character is determined by the MTA, RSDO (Read Strobe Delay Over) is transmitted via the slave bus to the TM02 Tape Control-NRZI module, and the tape character is multiplexed onto the slave bus Read Data lines. RSDO causes the Tape Control-NRZI module to strobe in the tape character, via the TCCM module, from the slave bus. The character (minus the vertical parity bit) now becomes available to the Bit Fiddler. LRCC and CRCC are generated from the data as it passes through the Tape Control-NRZI module. These will later be used to check the validity of the data read.

The Bit Fiddler assembles the characters into 18-bit data words and places them on the data bus. When a data word is assembled, the Bit Fiddler notifies the Massbus Controller, which then strobes in the data word off the data bus. The Bit Fiddler continues this assembly of data characters into 18-bit words until the end of the data record as represented by an all-0s tape character.

During a forward read, the rest of the read circuitry continues its operation, reading the CRCC and strobing it into the Check Character register, and then reading the LRCC. Discrepancies between generated CRCC/LRCC and detected CRCC/LRCC cause their respective error bits to be set.

During a reverse read, the LRC character is encountered first at the start of the read operation, but is ignored. The CRCC is encountered next, and strobed into the Check Character register, but otherwise it is ignored. No CRC or LRC error is generated. Then the data is read; assembly of characters into data words may differ when reading in the reverse direction, but this depends on the data format selected.

2.6.5.3 Command Termination - When the data and LRCC/CRCC have been read, the read heads will encounter the IRG. This absence of tape characters causes a motion delay, at the end of which STOP L is asserted on the slave bus and EBL (End of Block) is asserted on the Massbus. STOP L resets the motion flip-flop in the TU45 and terminates tape motion. It also clears the GO bit in the Control register, which causes OCC to be negated on the Massbus.

2.6.6 PE Data Write

Figure 2-21 illustrates the major functional sequences of a PE data write operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.

2.6.6.1 Command Initiation - To initiate a PE write operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register, specifying the selected slave TU45, tape character format, and tape data density (PE - 1600 bpi). The TM02 places the Slave Select (SS 0-2) and Density (DEN 0-2) bits of the Tape Control register on the slave bus. The Massbus Controller then loads the 2's complement of the number of tape characters to be written into the TM02 Frame Count register. Following this, the controller loads the Control register with the operational function code (61(8)) of the data write command. The TM02 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus.

When the controller has data available for transfer, it asserts RUN H on the Massbus. The TM02 responds by asserting SLAVE SET Pulse on the slave bus and accepting the first data word from the controller.

2.6.6.2 Command Execution - The TU45 which is enabled by its address code on the Slave Select lines (SS 0-2) of the slave bus, responds to SLAVE SET Pulse by setting its Forward motion control and Write Enable flip-flops on its MTA module. These flip-flops activate the capstan drive motor for forward tape motion and turn on the write and erase heads.

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After a motion delay during which the TU45 erases tape while it comes up to speed, the TM02 negates ACCL L on the slave bus. This notifies the TU45 that it is at speed, and enables it to transmit WRT CLK to the TM02. Upon receipt of WRT CLK, the TM02 begins generating a preamble. When forty all-0 characters and one all-1s character have been written, the Bit Fiddler begins disassembling the first data word into characters. When it has disassembled the first data word, it requests the next data word from the Massbus Controller, and continues to do so until all the data words have been transferred. Each time the Bit Fiddler generates a character, the Frame Count register is incremented, a vertical parity bit is generated, and the tape character is converted to PE mode and transmitted to the write circuitry of the TU45. When the Frame Count register overflows to zero, the TM02 asserts EBL (End of Block) to the controller and generates a postamble which is written on the tape. During the entire operation, the TU45/TM02 read operation is active and reads the record

2.6.6.3 Command Termination - When the TU45/TM02 read circuitry detects the end of the record, a motion delay is generated at the end of which the TM02 asserts STOP L on the slave bus, resetting the TU45 Forward motion flip-flop, thereby terminating tape motion. STOP L also clears the GO bit of the Control register, which causes OCC to be negated. When tape motion ceases, the Write Enable flip-flop is cleared, and the write and erase heads are de-energized.

2.6.7 NRZI Data Write

Figure 2-22 illustrates the major functional sequences of an NRZI data write operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description pamphlet in Chapter 3.

2.6.7.1 Command Initiation - To initiate an NRZI write operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register, specifying selected slave TU45, tape character format, and tape data density. The TM02 places the Slave Select (SS 0-2) and Density (DEN 0-2) bit of the Tape Control register on the slave bus. The Massbus Controller then loads the 2's complement of the number of tape characters to be written into the TM02 Frame Count register. Following this, the controller loads the Control register with the operational function code (61(8)) of the data write command. The TM02 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus.

When the controller has data available for transfer, it asserts RUN H on the Massbus. The TM02 responds by asserting SLAVE SET Pulse on the slave bus and accepting the first data word from the controller.

2.6.7.2 Command Execution - The TU45, which is enabled by its address code on the Slave Select lines (SS 0-2) of the slave bus, responds to SLAVE SET Pulse by setting its Forward motion control and Write Enable flip-flops. These flip-flops activate the capstan drive motor for forward tape motion and turn on the write and erase heads.

After a motion delay during which the TU45 erases tape while it comes up to speed, the TM02 negates ACCL L on the slave bus. This notifies the TU45 that it is at speed, and enables it to transmit WRT CLK to the TM02.

Upon receipt of WRT CLK by the TM02, the Bit Fiddler begins disassembling the first data word into characters. When it has disassembled the first data word, it requests the next data word from the Massbus Controller, and continues to do so until all the data words have been transferred. Each time the Bit Fiddler generates a character, the Frame Count register is incremented. A verical parity bit is generated, the CRCC is generated, and the tape character is transmitted to the write circuitry of the TU45 where it is converted from binary to NRZI mode (1's become transitions) and written on the tape. When the Frame Count register overflows to zero, the TM02 transmits EBL (End of Block) to the controller. It then generates the timing to write the generated CRCC and the LRCC.

During the time that the tape is moving at speed (ACCL L negated), the TU45/TM02 performs a read-after-write operation.

2.6.7.3 Command Termination - When the TU45/TM02 read circuitry detects the end of the record, a motion delay is generated, at the end of which the TM02 asserts STOP L on the slave bus, resetting the Forward motion flip-flop on MTA module thereby terminating tape motion. STOP L also clears the GO bit of the Control register, which causes OCC to be negated. When tape motion ceases, the Write Enable flip-flop on MTA module is cleared and the write and erase heads are de-energized.
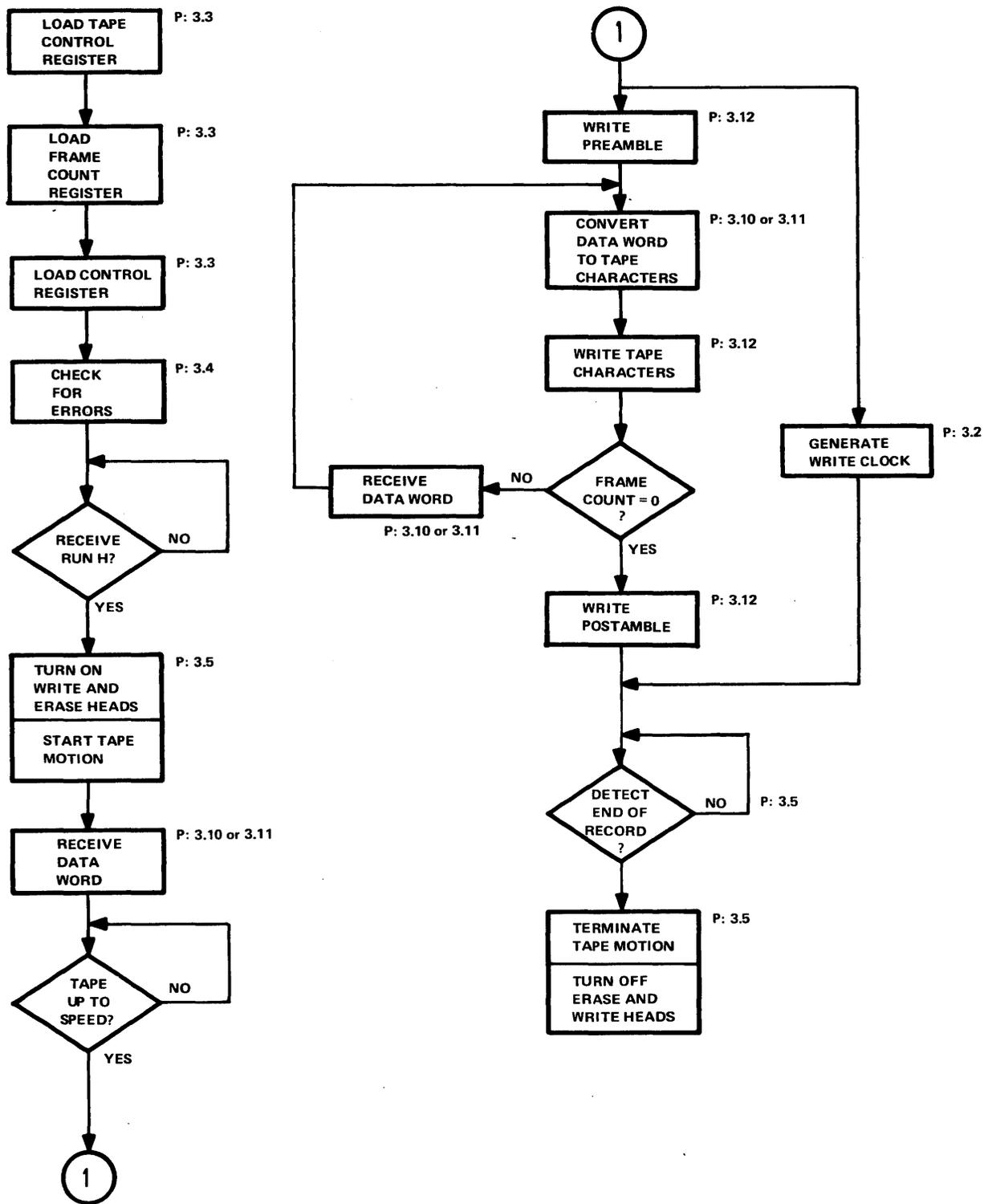
Figure 2-21 PE Data Write Operation Flowchart

LOAD TAPE CONTROL REGISTER — P: 3.3
LOAD FRAME-COUNT REGISTER — P: 3.3
LOAD CONTROL REGISTER — P: 3.3
CHECK FOR ERRORS — P: 3.4
RECEIVE RUN H? — NO / YES
TURN ON WRITE AND ERASE HEADS / INITIATE TAPE MOTION — P: 3.5
RECEIVE DATA WORD — P: 3.10 or 3.11
NO
1

1
CONVERT DATA WORDS TO TAPE CHARACTERS — P: 3.10 or 3.11
WRITE TAPE CHARACTERS — P: 3.13
GENERATE CRC CHARACTER — P: 3.13
RECEIVE DATA WORD — P: 3.10 or 3.11
FRAME COUNT = 0 ? — NO / YES
SPACE 3 CHARACTERS AND WRITE CRCC — P: 3.13
SPACE 3 CHARACTERS AND WRITE LRCC — P: 3.13
TERMINATE TAPE MOTION / ERASE IRG / TURN OFF ERASE AND WRITE HEADS — P: 3.5

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Figure 2-22 NRZI Data Write Operation Flowchart

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2.6.8 Write Tape Mark

The tape mark is a special tape record used to separate data on tape. Although a write tape mark command may be issued at any time, the most common use of this command is as a "software bookmark" to designate the end of a group of related records. It is possible to quickly locate the beginning of a group of related data records by searching the tape for written tape marks. This is accomplished by loading the Frame Count register with a record count larger than the number of records in any existing group of records, and then issuing a space command. The transport will space to the tape mark and terminate, motion despite the fact that frame count overflow does not occur.

Figure 2-23 illustrates the major functional sequences of a write tape mark operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description in Chapter 3.

2.6.8.1 Command Initiation - To initiate a write tape mark operation, the Massbus Controller first places the address code of the desired TM02 on the Drive Select lines of the Massbus. It then performs a register write into the Tape Control register, selecting the slave desired to perform the write tape mark operation and the density at which the tape mark characters are to be written. The TM02 places the Slave Select (SS 0-2) and Density Select (DEN SEL 0-3) bits of the Tape Control register on the slave bus.

The Massbus Controller then loads the TM02 Control register with the operational function code (27(8)) of the write tape mark command. The TM02 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, issues SLAVE SET Pulse to the TU45 and generates a motion delay.

2.6.8.2 Command Execution - The TU45, which is enabled by its address code on the Slave Select lines, responds to SLAVE SET Pulse by setting its Forward motion and Write Enable flip-flops on MTA module which activate the capstan drive (starting tape motion) and the write and erase heads. As tape moves past the heads, it is erased. Then, when the motion delay is over, the TCCM module generates the tape mark.

If the TM02 is operating in PE mode, slave bus write lines WD 3, 4, 6, and 7 are forced low while PE 0s are generated for WD 0, 1, 2, 5, and P. At the same time, Record pulses (40X2 = 80) are transmitted to the TU45. This results in forty 0s being written in tracks 1, 2, 4, 5, and 8 (See Figure 1-4 for Digital to Pertec Designation Conversion), and erasure of the remaining tracks.
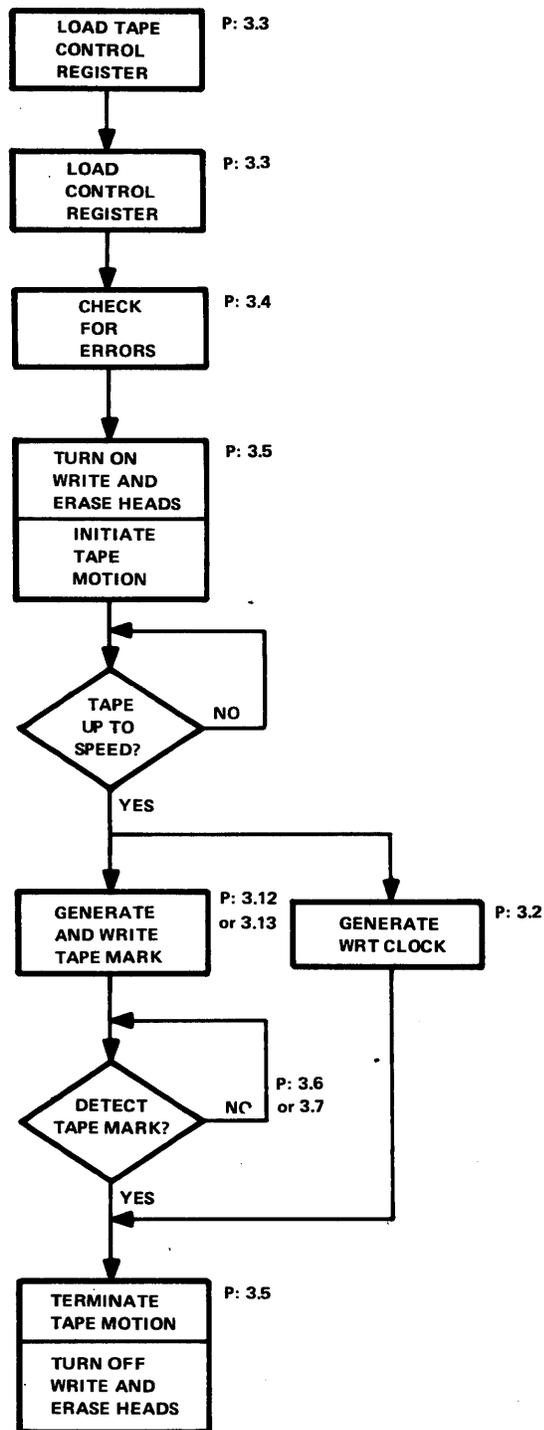
```
        ┌──────────────┐
        │ LOAD TAPE    │   P: 3.3
        │ CONTROL      │
        │ REGISTER     │
        └──────┬───────┘
               │
        ┌──────▼───────┐
        │ LOAD         │   P: 3.3
        │ CONTROL      │
        │ REGISTER     │
        └──────┬───────┘
               │
        ┌──────▼───────┐
        │ CHECK        │   P: 3.4
        │ FOR          │
        │ ERRORS       │
        └──────┬───────┘
               │
        ┌──────▼───────┐
        │ TURN ON      │   P: 3.5
        │ WRITE AND    │
        │ ERASE HEADS  │
        ├──────────────┤
        │ INITIATE     │
        │ TAPE         │
        │ MOTION       │
        └──────┬───────┘
               │
             ╱   ╲
            ╱ TAPE╲     NO
           ╱ UP TO ╲───────┐
           ╲ SPEED?╱       │
            ╲     ╱        │
             ╲   ╱         │
              │ YES        │
              │            │
        ┌─────▼──────┐  ┌──▼───────┐
        │ GENERATE   │  │ GENERATE │  P: 3.2
        │ AND WRITE  │  │ WRT CLOCK│
        │ TAPE MARK  │  └──┬───────┘
        └─────┬──────┘     │
   P: 3.12         │       │
   or 3.13         │       │
              ╱   ╲        │
             ╱DETECT╲  NO  │
             ╲TAPE  ╱──────┤
             ╲MARK? ╱ P:3.6│
              ╲   ╱  or 3.7│
               │ YES       │
               │◄──────────┘
        ┌──────▼───────┐
        │ TERMINATE    │   P: 3.5
        │ TAPE MOTION  │
        ├──────────────┤
        │ TURN OFF     │
        │ WRITE AND    │
        │ ERASE HEADS  │
        └──────────────┘

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Figure 2-23 Write Tape Mark Operation Flowchart

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If the TM02 is operating in NRZI mode, the tape mark character is forced onto the slave bus WD lines and a Record pulse is transmitted to the TU45. The TU45 is then allowed to erase seven character lengths of tape at which time it receives LRC STROBE on the slave bus, and writes an LRCC (which will be the same as the tape mark character).

After writing the NRZI or PE tape mark, the TU45/TM02 continues to erase tape. As the write tape mark operation is performed, the read circuitry performs a read-after-write.

2.6.8.3 Command Termination - When the read circuitry has detected the written tape mark, a motion delay is generated by the TM02, at the end of which STOP L is transmitted to the TU45. STOP L resets the TU45 Forward motion flip-flop on MTA module which deactivates the capstan motor, thereby terminating tape motion. When tape motion has ceased, the write and erase heads are de-energized. STOP L also resets the TM02 Control register GO bit.

CHAPTER 3

SERVICING

MAINTENANCE MODES

CONTENTS

3.1 INTRODUCTION

This section discusses TU45/TM02 on-line testing capabilites (Paragraph 3.1.1) and diagnostics (Paragraph 3.1.2).

3.1.1 Maintenance Register

The Maintenance register (R3) facilitates on-line diagnostic testing of the TU45/TM02, and allows testing of the TM02 data paths and error discrimination circuitry. A discussion of the Maintenance register bits and their functions follows.

1. Bit 0 - Maintenance Mode (MM) - Must be loaded set when any maintenance mode function is desired.

2. Bits 1 to 4 - Maintenance Op Code (MOP 0 to 3) - These four bits determine the maintenance function that will occur if the MM bit is set and the TM02 is loaded with the appropriate command. The op codes that are implemented are:

   o 0000 - Null code

   o 0001 - Interchange Read (IRD)
      In PE mode, this op code suppresses on-the-fly correction of data errors.

      0010 - Even Parity
      Causes even parity to be used on the Control lines of the Massbus.

o   0011 - Global Data Wrap-Around (WRP 0)
    Configures the TM02 data paths as shown in Figure 3.1-1.
    This causes write data command to be executed as follows.
    Data is brought in on the data lines, divided into bytes
    using the algorithm defined by the format code resident
    in the Tape Control register, formatted as either NRZI or
    PE write data, multiplexed into the read circuitry, and
    deposited in the Maintenance Register Data Field.

o   0100 - Partial Data Wrap-Around (WRP 1)
    Configures the TM02 data path as shown in Figure 3.1-2.
    This causes a write data command to be executed as
    follows. Data is brought in on the data lines, divided
    into bytes using the algorithm defined by the format code
    resident in the Tape Control register, formatted as
    either NRZI or PE write data, and deposited in the
    Maintenance Register Data Field.

o   0101 - Formatter Write Data Wrap-Around (WRP 2)
    Configures the TM02 data path as shown in Figure 3.1-3.
    This causes a write data command to be executed as
    follows. Data is brought in on the data lines, divided
    into bytes using the format code resident in the Tape
    Control register, and deposited in the Maintenance
    Register Data Field.
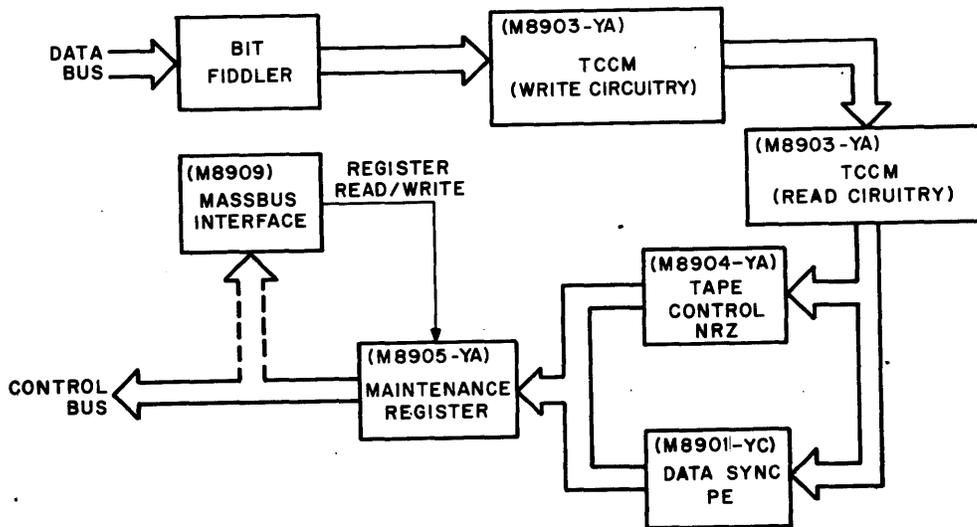
CS-1610

Figure 3.1-1 Global Wrap-Around (WRP 0)

Figure 3.1-2   Partial Wrap-Around (WRP 1)

Figure 3.1-3   Formatter Wrap-Around (WRP 2)

o   **0110 - Formatter Read Data Wrap-Around (WRP 3)**
Configures the TM02 data path as shown in Figure 3.1-4.
This causes a read data command to be executed as
follows. Data is taken from the Maintenance Register
Data Field, multiplexed into the formatting logic byte by
byte, formed into data bus words using the algorithm
defined by the format code resident in the Tape Control
register, and transmitted to the controller.

In addition, this op code suppresses reception of the
Massbus WCLK signal. Thus, an attempt to perform a write
operation with this op code in the Maintenance register
will result in detection of DTE.

3-4

o   0111 - Cripple Reception of OCC
    An attempt to perform any data transfer operation with
    this op code in the Maintenance register will result in
    detection of DTE.


```
                    ┌──────────┐
     DATA  ⟵────────│   BIT    │⟵────────────────┐
     BUS            │ FIDDLER  │⟵──────────┐     │
                    └──────────┘           │     │
                                           │     │
                    ┌──────────┐           │     │
                    │ (M8909)  │ REGISTER  │     │
                    │ MASSBUS  │ READ/WRITE│     │
                    │ INTERFACE│           │     │
                    └──────────┘           │     │
                       ↑  ↑      │         │     │
                       :  :      │         │     │
                       :  :      ↓         │     │
                    ┌──────────┐           │     │
     CONTROL ──────────╲  │ (M8905-YA)│────────────┘     │
     BUS     ──────────╱  │MAINTENANCE│──────────────────┘
                    │ REGISTER │
                    └──────────┘
                         CS-1608
```
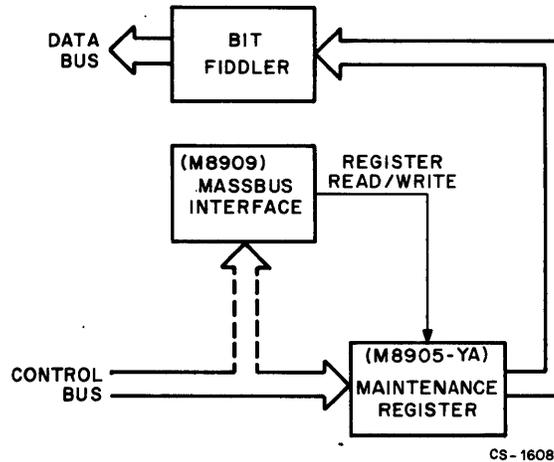
Figure 3.1-4   Formatter Read Wrap-Around (WRP 3)

o   1000 - Illegal Check Character (ILCC)
    In NRZI mode, this op code suppresses initialization of
    the CRC checking logic, resulting in CRC errors. In PE
    mode, this op code suppresses detection of data in
    logical track 1.

o   1001 - Incorrect Tape Mark
    In NRZI mode, this op code causes bit 5 of tape data
    bytes to remain in the negated state. In PE mode, this
    op code suppresses detection of data in logical tracks 1
    and 2.

o   1010 - Maintenance Mode End of Record (MMEOR)
    This op code is used to signal the end of a maintenance
    mode operation, thus causing the GO bit to become
    negated.

o   1011 - Incorrect Preamble (INC PREAMBLE)
    This code causes logical bit 1 of a PE preamble and
    postamble to be inverted during a write data command,
    resulting in generation of invalid preambles and
    postambles.

3. Bit 5 - Maintenance Mode Clock (MC) - This bit controls the
    sequencing of data through the TM02 data paths when operating
    in a maintenance mode.

4. Bit 6 - Selected Slave Clock (SWC) - This bit displays a clock signal which is transmitted to the TM02 from the selected slave. The frequency of this clock depends both on the Density Select bits located in bits 8-10 of the Tape Control register and on the operating speed of the selected slave. Its purpose is to enable a check on the proper decoding of the Density Select bits by the selected slave, and to allow monitoring of drive functions during maintenance mode operation.

5. Bit 7 to 15 - Maintenance Data Field (MDF 0-8) - These bits act as buffers for data generated during checks of the TM02 data paths.

3.1.2 Diagnostics

This section introduces the diagnostics supplied with the TU45/TM02 Tape Drive System. For detailed information, refer to the documentation supplied with the diagnostics.

1. Control Logic Test

   a. Tests control logic; isolates malfunctions to the module level.

   b. Tests the data paths utilizing the maintenance wrap-arounds; isolates malfunctions to the module level.

   c. Tests TU45/TM02 function (read/write/space etc).

2. TU45 Data Reliability - Writes and reads user-determined data patterns, and thereby tests TU45 and TM02 circuitry. The program provides printouts whenever any errors occur.

3. Drive Function Timing - Tests for proper tape motion timing (speed, acceleration, deceleration) and data transfer rate.

4. Basic Functions Test - Exercises the TM02 read/write circuitry utilizing the maintenance wrap-arounds while using programmer-determined random data.

5. TU45 Utility Driver (BRUTUS - Brute Force Subroutine) - Performs up to 15 operational functions determined by the user.

6. Data Tape Create - Utility Program Supplement to Random Data Exerciser. Creates a paper tape containing a desired data pattern for use as Pattern 0 of the Data Reliability Program.

CLOCKS

CONTENTS

3.2.1   System Clocks

All free-running system clock waveforms used in the TU45/TM02 are
generated from a 3.84-MHz, crystal controlled clock located on the MTA
module M8921. The 3.84-MHz clock is divided down to 240 kHz, and is
transmitted to the TM02 via the slave bus [CLOCK (SB)] by an on-line,
selected transport loaded with tape. On the Tape Control Common Mode
(TCCM) module (M8903), this 240-kHz clock is further divided to
provide:

```
        DATA HALF       120 kHz
        800 BPI CLK      60 kHz
        200 BPI CLK      15 kHz
```

These clocks perform various housekeeping functions in the TM02.   For
example, 800 BPI CLK clocks the Motion Delay Counter (M8903-YA, sheet
3); 200 BPI CLK counts the IDB Counter, Write End Counter, and
Shutdown Counter.

DATA HALF is essentially a 1600-bpi clock, and is used in functions
pertaining to PE mode. For instance, it clocks the Character Counter
on the Tape Control-PE module (M8902-YA, sheet 4).

3.2.2 Write Clock

The TM02 is capable of reading and writing data at several bit densities. To do this, a separate clock signal, whose frequency depends on the tape data density, must be developed; WRT CLK is this signal. WRT CLK is transmitted to the TM02 by a selected, powered TU45 loaded with tape and running at speed (except during a rewind). It is used in the TM02 to produce the following clock signals:

WB CK   Clocks the TCCM Write Buffer (M8903-YA), sheet 2).

ST CLK   Used to generate PE write data states in the Tape Control-PE module (M8902-YA, sheet 2).

PE CLK   Used in PE mode to control TCCM Write Multiplex (M8903-YA, sheet 2).

WRT CLK is generated in the following manner. A number is preset into a 74161 (synchronously loaded) binary counter (M8921, MTA module), which is then upcounted at 960kHz. When the counter overflows, WRT CLK H is asserted and causes the counter to be preset at the leading edge of the next 960-kHz clock pulse. With the counter preset, WRT CLK will be negated by the trailing edge of that same 960-kHz clock pulse. The counter will be clocked up as before, until overflow, and the cycle is repeated.

The presets of the 74161 counter are determined by various signals and conditions. These are listed in Table 3.2-1, along with the resulting counter presets, WRT CLK frequency, and density. Note that WRT CLK frequency for 1600 bpi is four times that of 800 bpi. This is because 1600 bpi is used only in PE mode, and PE mode requires a double frequency WRT CLK.

Obviously, the frequency of the cycle will vary with the magnitude of the preset. Figure 3.2-1 shows timing diagrams for presets of -1 (-n = 2's complement of n), -2, and -3. Note that for a preset of -n, the frequency of WRT CLK, $f(WRT\ CLK) = [960/(n+1)]$ kHz.

3.2.3 Performance Checks

Refer to the Acceptance Procedure in the appropriate system manual (TJU45 or TWU45) whichever is applicable.

3.2.4 Adjustments

None.

Table 3.2-1

Write Clock Frequencies

	DEN 2	DEN 1	DEN 0	Test PE	Test DEN	WRT CLK Counter Presets	Frequency kHz (bpi)
						LSB MSB	
	0	0	0	1	1	10000011	15(200)
	0	0	1	1	1	01010111	41.7(556)
	0	1	0	1	1	10001111	60(800)
	0	1	1	1	1	10001111	60(800)
On-Line	1	0	0	1	1	10111111	240(1600)
	1	0	1	1	1	00111111	192(1277)Reserved
	1	1	0	1	1	10001111	60(800)Reserved
	1	1	1	1	1	10111111	240(1600)Reserved
	x	x	x	0	0	01010011	17.5(233)
Off-Line	x	x	x	0	1	10001111	60(800)
	x	x	x	1	0	00111111	192(1277)
	x	x	x	1	1	10000011	15(200)
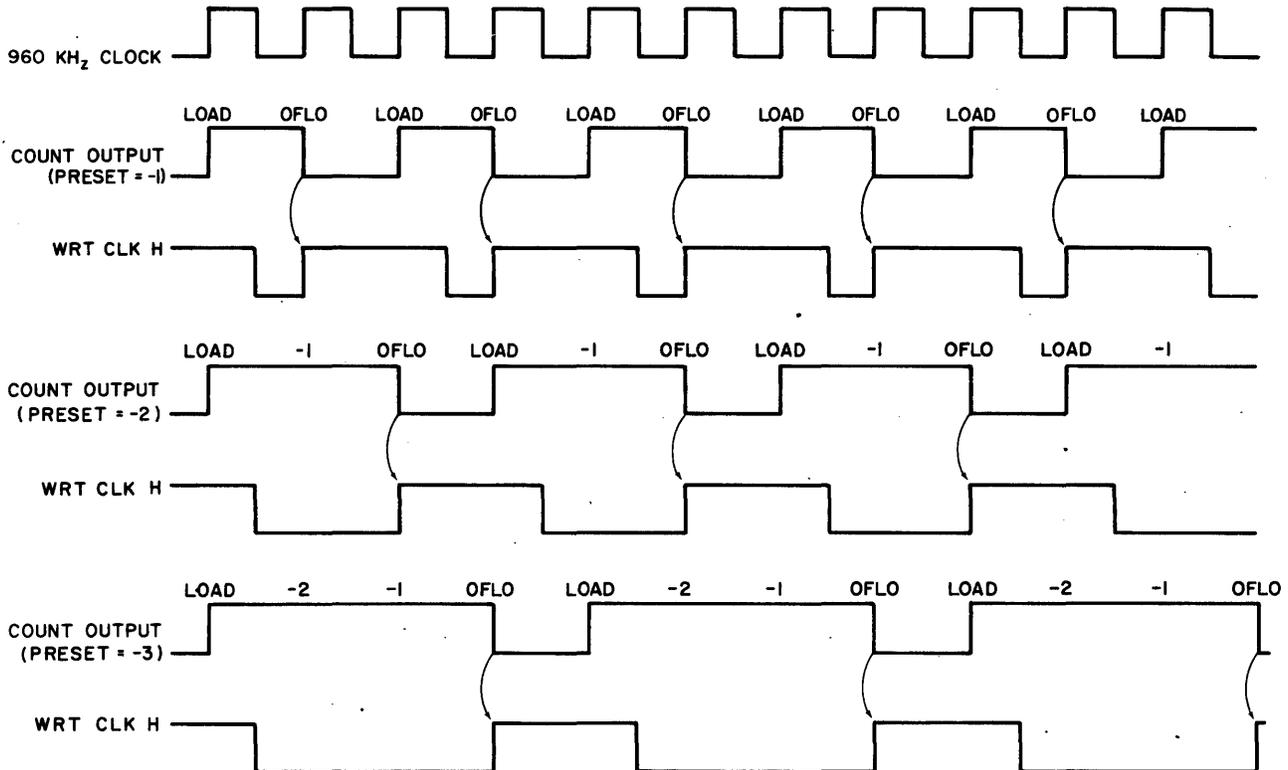
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Figure 3.2-1   WRT CLK Generation Timing (MTA-M8921)

CONTENTS

3.3 INTRODUCTION

The Massbus Controller performs register transfers to control and determine the status of the TU45/TM02. These register transfers are performed on the control bus of the Massbus.

3.3.1 Register Write

The Massbus Controller writes into TM02 registers to control TU45/TM02 operations. To accomplish a register write (Figures 3.3-1 and 3.3-2), the controller simultaneously:

> Places a five-bit address code on the Drive (TM02) Select lines.

> Places the five-bit register select code of the desired register on the Register Select lines.

> Places the information to be written on the Control lines.

> Places a parity bit (odd parity) on the CPA line. This parity bit is associated with the data on the Control lines.

> Asserts CTOD H.

The controller now waits for these signals to settle (325 ns) and then asserts DEM H.

All drives diasy-chained on the Massbus examine the Drive (TM02) Select lines (M8909, sheet 2), but only the drive whose unit select jumper block configuration corresponds to the signals on the Drive (TM02) Select lines is conditioned to respond to DEM H. All drives decode the Register Select lines, but only the selected drive will utilize the information on these lines.

When DEM H is received by the selected TM02, a 70-ns PULSE H is generated, which produces ASYC WRT L (also of 70-ns duration).

In the meantime:

1. The TM02 has checked for control bus parity (M8909, sheet 4) and, if detected, a parity error SET CMB PE L has been asserted.

2. The TM02 has decoded the Register Select lines and generated Rn L (where n designates the selected register). If Rn is a nonexistent register, SET ILR (Set Illegal Register) is generated.

3. If Rn is not R3 (Maintenance register) or R4 (Attention Summary register) and GO L is asserted (i.e., an operation other than rewind is being executed), then the TM02 generates SET RMR (Set Register Modification Refused).

If neither SET ILR or SET RMR has been asserted, ASYC WRT L generates REG WRT L. REG WRT L, along with Rn L, load the selected register with the data on the Control lines. If SET CMBPE, SET ILR, or SET RMR were asserted, the corresponding bits in the Error register are set.

The trailing edge of PULSE L triggers a 20-ns one-shot. When the 20-ns one-shot times out, TRA is asserted and transmitted to the Massbus Controller. This signal, when received by the Massbus Controller, notifies it that the write sequence in the TM02 is over. The controller therefore negates DEM H and this in turn negates TRA (M8909, sheet 1); the register transfer is over.

START

SELECT DRIVE (TM02)	SELECT REGISTER	ASSERT CTOD H	PLACE DATA ON CONTROL LINES	PLACE CPA ON CONTROL BUS
RH *	RH	RH	RH	RH

BUS SETTLE DELAY

ASSERT DEM H		SELECTED TM02 ENABLED	REGISTER SELECT DECODED
RH			

PULSE H ↑	ASSERT ASYC WRT L	Rn L ASSERTED (n=SELECTED REGISTER)

SET RMR

YES — ATTEMPTED WRITE INTO ANY REGISTER BUT 3 OR 4 WHILE "GO" SET ?

NO

YES — ILLEGAL REGISTER ? — NO

SET PARITY ERROR

YES — C-BUS PARITY ERROR ? — NO

SET ILR

ASSERT REG WRT L

LOAD REGISTER

PULSE H ↓

ASSERT TRA H

NEGATE DEM H	MASSBUS SIGNALS MAY NOW BE ALTERED
RH	

NEGATE TRA H

*RH indicates that the operation is performed by the Massbus Controller.

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Figure 3.3-1   Register Write Flowchart

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```
DRIVE (TMO2) ▨━━━〰━━━━━━━━━━━〰━━━━━━━▨
   SELECT

   REGISTER ▨━━━〰━━━━━━━━━━━〰━━━━━━━▨
   SELECT

DATA + PARITY ━━━━┌──〰━━━━━━━━━━━〰━━━━━━┐━━━

   CTOD  H  ▨━┐━〰━━━━━━━━━━━〰━━━━━━━▨

  DEMAND  H  ━━━━━〰━┌────────────〰────────────┐━━

   PULSE  H  ━━━━━〰━┌──────┐━━━━━〰━━━━━━

ASYC WRT L /  ━━━━━〰━┌──────┐━━━━━〰━━━━━━
REGISTER WRITE L

         REGISTER  LOADED

  E4  PIN  12 ━━━━━〰━━━━━━━┌──┐━━〰━━━━━━

  TRANSFER  L ━━━━━〰━━━━━━━┌────────〰────────┘━━

                                          CS - 1618
```
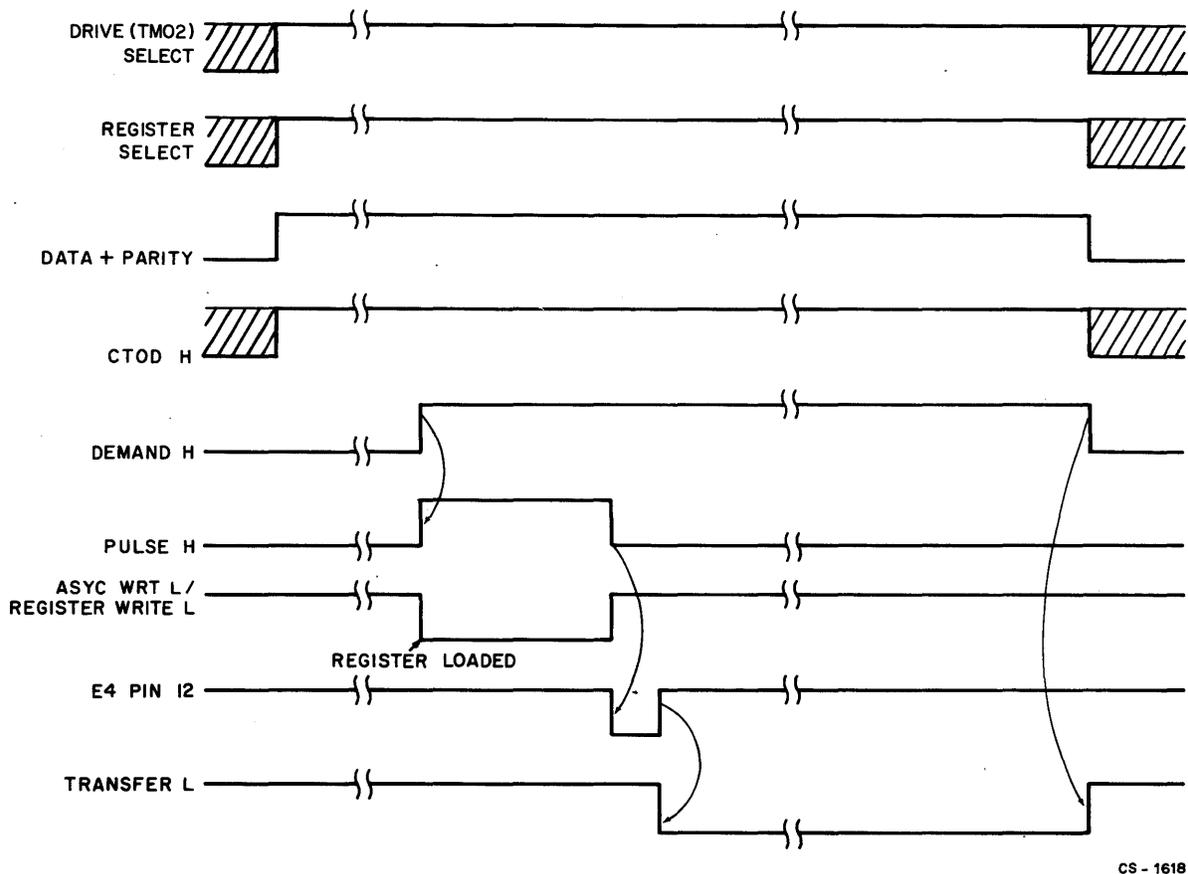
Figure 3.3-2 Register Write Timing Diagram

3.3.2 Register Read

The Massbus Controller can read any TM02 register to determine the
status of the TU45/TM02. To do so (Figures 3.3-3 and 3.3-4), the
controller simultaneously:

> Places a five-bit drive address code on the Drive Select
> lines.

> Places the five-bit register select code of the desired
> register on the Register Select lines.

> Negates CTOD H.

The controller now waits 325 ns for these signals to settle on the
Massbus and then asserts DEM H.

Drive (TM02) select recognition and register select recognition occur
in the same way as for a register write (M8909, sheet 2); only the
selected TM02 will respond.

When DEM H is received by the selected TM02, a 70-ns PULSE H is generated. If a nonexistent register is decoded on the Register Select lines, SET ILR H will be generated, and, on the leading edge of PULSE H, the ILR bit of the Error register will be set. If a legal register has been addressed, Rn L (as decoded from the Register Select lines, where n is the selected register) will multiplex the bits of the selected register to the Control Line Latches (M8905-YA, sheet 4 and Figure 3.3-5).

The register multiplexers are located on several of the TM02 logic modules, but their outputs are "common collectored". Table 3.3-1 lists the location in the engineering drawing set of the various multiplexers.

The trailing edge of PULSE L triggers a 20-ns one-shot, which causes LCTOD L to be asserted. LCTOD loads the Control Line Latches with the multiplexed register contents and gates the register contents onto the Control lines.

When the 20-ns one-shot times out, TRA is asserted and transmitted to the Massbus Controller. Upon receipt of TRA H, the controller strobes in the data on the control lines and negates DEM H. DEM H, a low, negates TRA L in the TM02, and also negates LCTOD L. With LCTOD L negated, the type 74173 Control Line Latches produce high level (+5V), high impedance outputs.

3.3.3. Attention Summary Register (R04)

The Attention Summary register is shared by all TM02s (and other drives) that are connected to a particular Massbus Controller. Therefore, when reading or writing this register, it is not required to place any address code on the Drive Select lines of the Massbus. Each TM02 is enabled to respond when it decodes R4 L from the Register Select lines. It should be noted, however, that the DEMAND-TRANSFER "handshake" is carried on in the normal manner by the TM02.

3.3.3.1 Register 04 Read - To read the Attention Summary register, the Massbus Controller performs its usual register read sequence; however, no particular TM02 address code need be placed on the Drive Select lines. When each TM02 decodes R4 L from the Register Select lines, it places its ATA (Attention Active) status bit on one of the Control lines of the Massbus; which Control line is determined by the unit select plug configuration (unit number) of the particular TM02.

```
       ┌─────────────┐       ┌──────────────┬──────────────┬──────────────┐
       │    START    │       │   SELECT     │   NEGATE     │   SELECT     │
       └──────┬──────┘       │   DRIVE      │   CTOD H     │   REGISTER   │
              │              │   (TM02)     │              │              │
       ═══════╪═══════       │ RH *         │ RH           │ RH           │
              │              └──────────────┴──────────────┴──────────────┘
            BUS
          SETTLE
          DELAY
       ═══════╪═══════
              │
       ┌──────┴──────┐       ┌──────────────┬──────────────┐
       │   ASSERT    │       │  SELECTED    │  REGISTER    │
       │   DEM H     │       │  TM02        │  SELECT      │
       │             │       │  ENABLED     │  DECODED     │
       │ RH          │       │              │              │
       └──────┬──────┘       └──────────────┴──────────────┘
              │
       ┌──────┴──────┐       ┌──────────────┬──────────────┐
       │   PULSE H   │       │ Rn L ASSERTED │  MULTIPLEX   │
       │      ↑      │       │ (n=SELECTED   │  SELECTED    │
       │             │       │  REGISTER)    │  REGISTER    │
       └──────┬──────┘       └──────────────┴──────────────┘
              │
┌─────────┐  ╱╲
│  SET    │ ╱  ╲   ILLEGAL
│  ILR    │◄─── YES   REGISTER
│         │ ╲  ╱      ?
└────┬────┘  ╲╱
     │        │ NO
     └────────┼────────┐
              │
       ┌──────┴──────┐
       │   PULSE H   │
       │      ↓      │
       │             │
       └──────┬──────┘
              │
       ┌──────┴──────┐       ┌──────────────┐
       │   ASSERT    │       │ LOAD C-LINES │
       │   LCTOD L   │       │ OUTPUT       │
       │             │       │ LATCH        │
       └──────┬──────┘       └──────────────┘
              │
       ┌──────┴──────┐
       │   ASSERT    │
       │   TRA H     │
       │             │
       └──────┬──────┘
              │
       ┌──────┴──────┐       ┌──────────────┐
       │   NEGATE    │       │  STROBE IN   │
       │   DEM H     │       │  C-LINES     │
       │             │       │  DATA        │
       │ RH          │       │ RH           │
       └──────┬──────┘       └──────────────┘
              │
       ┌──────┴──────┐       ┌──────────────┐
       │   NEGATE    │       │   NEGATE     │
       │   TRA H     │       │   LCTOD L    │
       │             │       │              │
       └─────────────┘       └──────────────┘
```
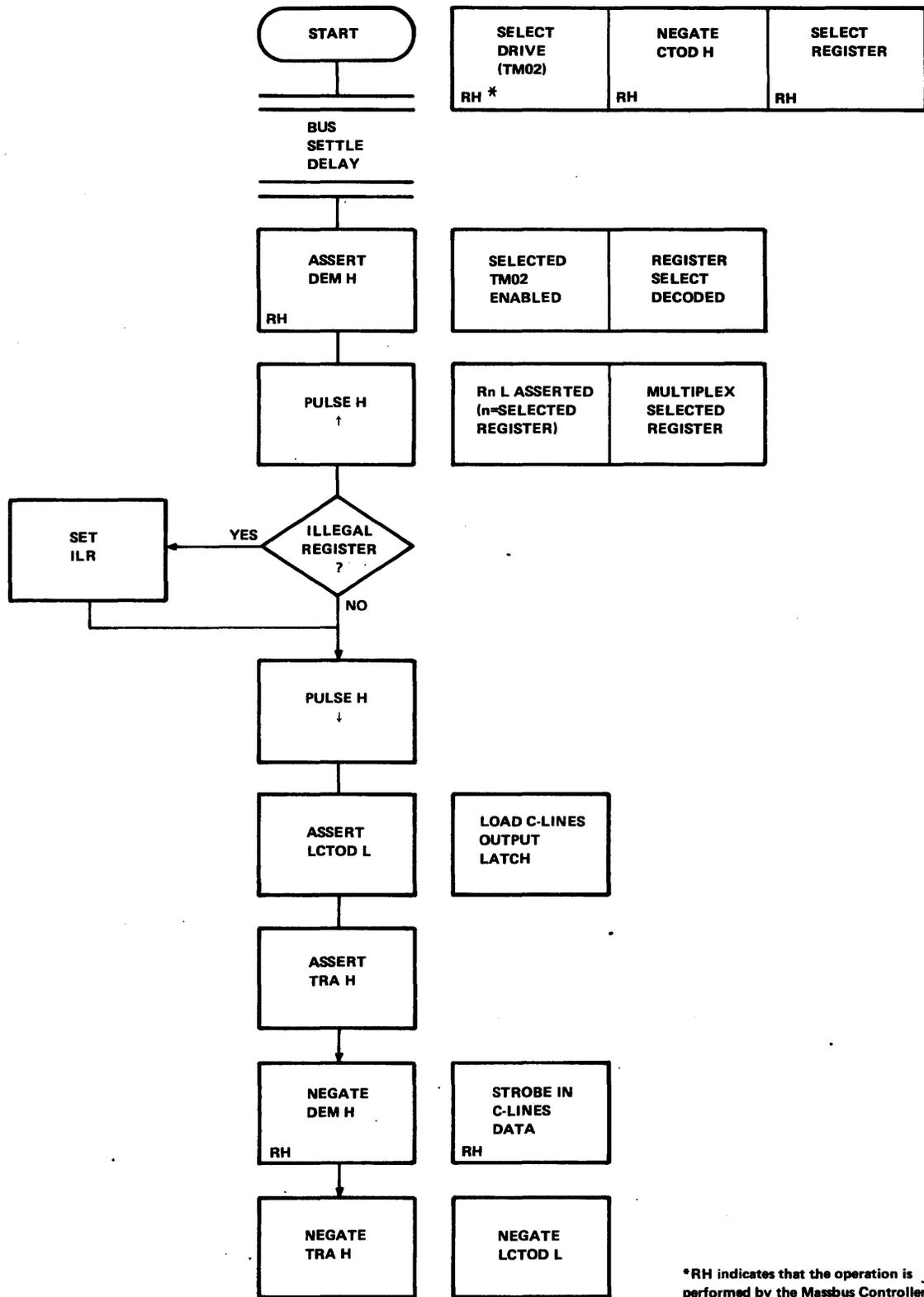
*RH indicates that the operation is
performed by the Massbus Controller.

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Figure 3.3-3 Register Read Flowchart

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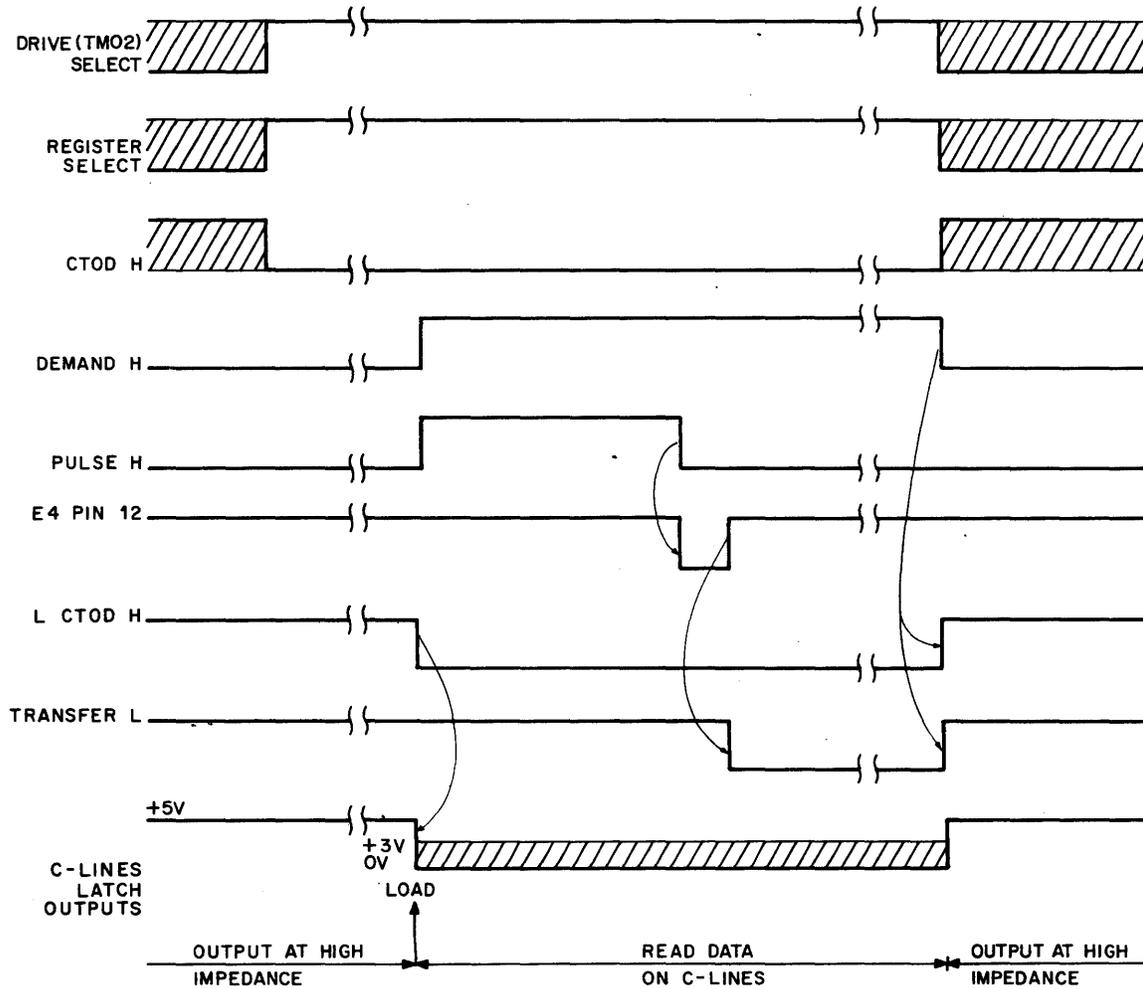
Figure 3.3-4 Register Read Timing Diagram

CS-1613
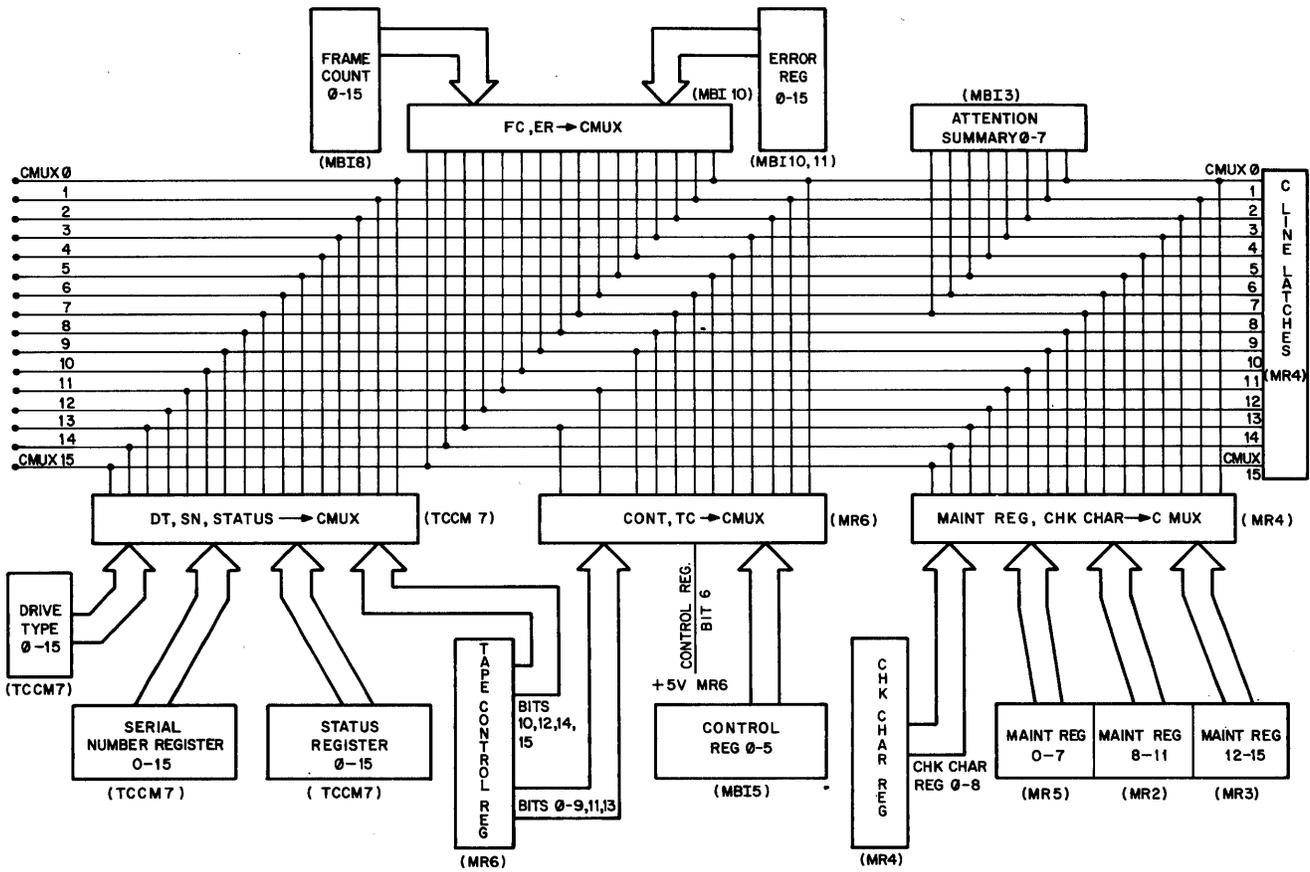
Figure 3.3-5 Register Read Multiplexing

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Table 3.3-1
Register Locations

Register	Bit Source Drawing	Sheet	Multiplexer Drawing	Sheet
00 Control	M8909	5	M9805-YA	6
01 Status			M8903-YA	7
02 Error	M8909	11	M8909	10
03 Maintenance	M8905-YA	2,3,5	M8905-YA	4
04 Attention Summary	M8909	3		
05 Frame Count	M8909	8	M8909	10
06 Drive Type			M8903-YA	7
07 Check Character	M8905-YA and M8901-YC	3 3,5,7	M8905-YA	4
10 Tape Control	M8905-YA	6	M8903-YA and M8905-YA	7 6
11 Serial Number	MTA(M8921)	2	M8903-YA	7

A type 74145 BCD decoder (M8909, sheet 3 and Figure 3.3-6) multiplexes the ATA bit onto the proper Control line. Inputs D0, D1, and D2 of the decoder are the unit select (US0-2) configuration of the TM02. If register 4 is being read and the ATA bit is asserted, input D3 is low (units 0 and 2 in Figure 3.3-6). The input to the BCD decoder is therefore the unit select configuration; the appropriate output is asserted low, but is later inverted by the Massbus Drivers.

If the ATA bit is not asserted (unit 1 in Figure 3.3-6), D3 is high and the decoder decodes 8 or higher (8+n for unit n). Since only outputs 0-7 of the decoder are used, this condition will not produce a high on the Control lines.

3.3.3.2 Register 04 Write - To write the Attention Summary register, the Massbus Controller performs the usual register write sequence. However, it need not specify a particular TM02 on the Drive Select lines. The DEMAND-TRANSFER handshake is caried out in the normal manner, but TM02 internal operation is slightly different.

When REG WRT L is generated, one of the Control lines is multiplexed (M8909, sheet 3) into the TM02. If the signal on the Control line is high, it resets the ATA flip-flop; if it is low, it has no effect. The Control line is selected by the unit select configuration (US0-2) of the particular TM02, input to a type 74151 multiplexer.

3.3.4 Performance Checks

Refer to the Acceptance Procedure in the appropriate system manual (TJU45 or TWU45) whichever is applicable.

3.3.5 Adjustments

None.
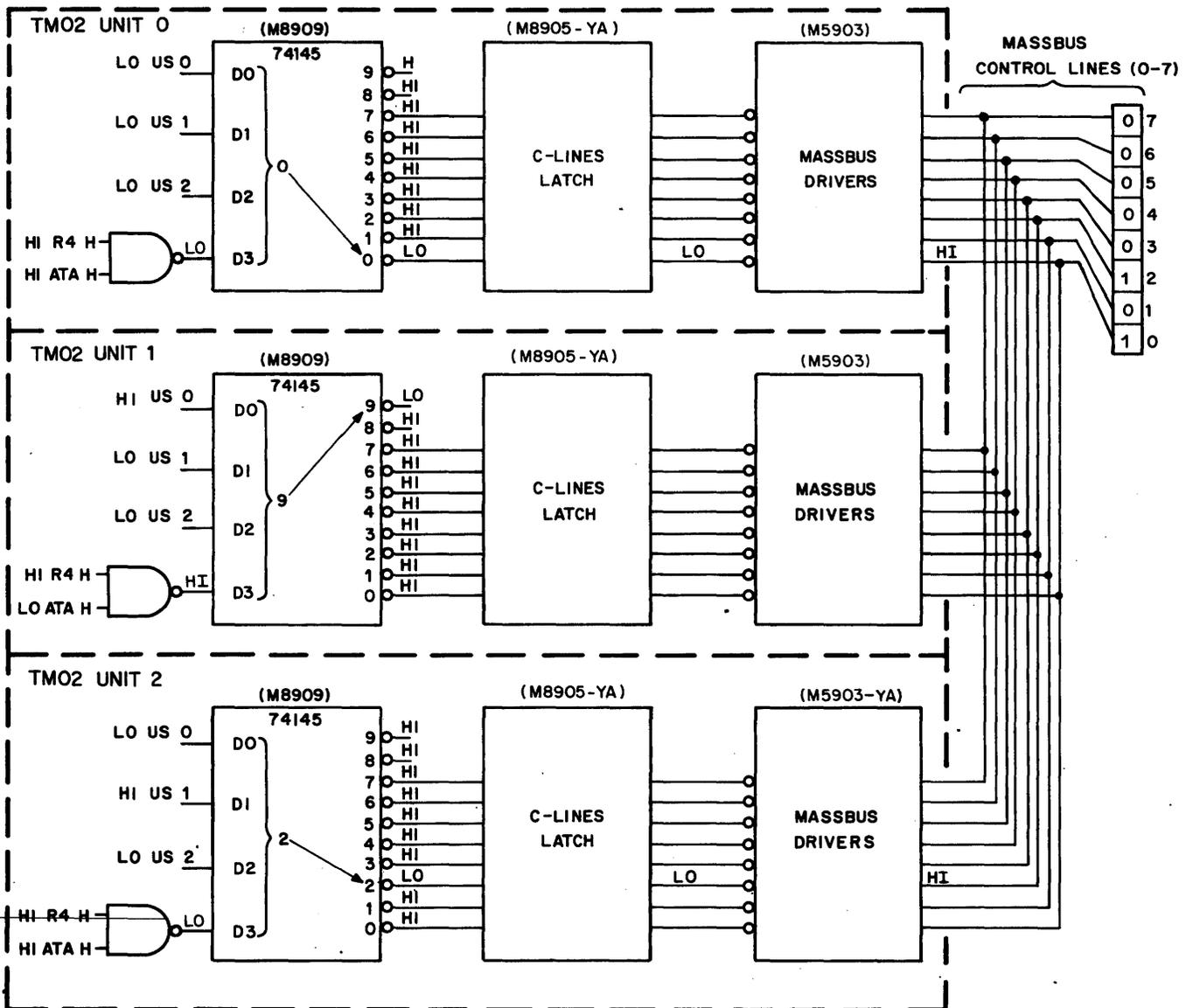
Figure 3.3-6 Attention Summary Register Read

CONTENTS

3.4   INTRODUCTION

This |section | discusses the error check sequence performed by the
TM02, as well as TM02 and system responses to error conditions (ATTN
and EXC asserted). For a detailed discussion of the Error register
bits, refer to Chapter 2, Paragraph 2.5.3.

3.4.1   Error Check

Whenever the Control register is loaded, setting the GO bit, an error
check is performed. If an error condition exists, the operation
specified by the function code in the Control register is inhibited.

If any bit in the Error register is asserted, COMPER H (Composite
Error) is asserted (MBI 10). If the Control register is loaded while
this signal is asserted, PREV ER H (Previous Error) is generated and
prevents the assertion of OCC (Occupied) on the Massbus (MBI 7). This
clears the Control register GO bit, which in turn sets the TM02 ATA
bit and asserts ATTN on the Massbus.

3.4.2 Attention (ATTN)

Attention (ATTN) is asserted on the Massbus by any drive that requires servicing. ATTN is asserted (MBI 3) under the following conditions:

1. At the completion of an erase, space, or write tape mark operation

2. Upon initiation of rewind command

3. Upon loading a 1 into the GO bit of the Control register while an error condition exists

4. Upon termination of an operation during which an error occurred or SSC was asserted

5. Upon termination of any operation during which END POINT was asserted

When the Massbus Controller senses that the ATTN line of the Massbus is asserted, it must read the Attention Summary register (R04) to determine which drive(s) require(s) servicing. It will service each drive whose ATA bit is asserted, and will clear the ATA bit of the drive upon completion of servicing.

To service a TM02, the Massbus Controller first reads the Status register (R01) to determine why servicing is required. If the ERR (Composite Error) bit of the Status register is asserted, it will read the Error register (R02) to determine which error has occurred, and will then proceed accordingly. If the SSC (Slave Status Change) bit of the Status register is set, the Massbus Controller will poll all of the slaves controlled by the TM02 to determine which one requires servicing and why.

3.4.3 Exception (EXC)

The EXC line of the Massbus is immediately asserted (MBI 9) by the TM02 whenever any error occurs during a data transfer operation (OCC TM asserted).

If during a write data operation, an error which is serious enough to invalidate data occurs, then the TM02 asserts EBL on the Massbus. It also terminates the write operation (WRITE END L asserted), stopping tape motion after erasing IRG.

The following error conditions cause the TM02 to assert EBL:

1. A data transfer operation is attempted while an error condition exists in the TM02.

2. An error condition occurs while the data transfer is being initiated.

3. A Class B error (UNS, OPI, DTE) or an ILF error occurs while a data transfer command is being executed.

4. A data error (INC/VPE, DPAR, PEF/LRC, COR/CRC) occurs during the data transfer operation, while bit 12(EAODTE) of the Tape Control register is set.

3.4.4 Performance Checks

Refer to the Acceptance Procedure in the appropriate system manual (TJU45 or TWU45) whichever is applicable.

3.4.5 Adjustments

None.

3.4.6 Troubleshooting

When troubleshooting the error detection circuitry of the TU45/TM02, it is preferable to start at the Error register itself. Most of the Error register flip-flops are located in the Massbus Interface (MBI-11). The rest are located as follows:

1. INC/VPE, PEF/LRC, and COR/CRC are on TCPE-2/CNRZ-2.

2. CS/ITM is on TCPE-2/CNRZ-4.

3. NSG is on TCCM-5.

Table 3.4-1 lists errors which could be detected during certain operations and remain asserted after the operation is completed. If errors other than those indicated occur, the TU45/TM02 error detection circuitry should be suspect.

Table 3.4-1
TU45/TM02 Operations and Possible Errors

Operations \ Errors	ILF	ILR	RMR	CPAR	FMT	DPAR	INC/VPE	PEF/LRC	NSG	FCE	CS/ITM	NEF	DTE	OPI	UNS	COR/CRC
Write to any register*		X	X	X												
Read fromm any register		X														
Load CS1 with "NO-OP"	X	X	X	X								X			X	
Load CS1 with "REWIND-OFF LINE"	X	X	X	X								X			X	
Load CS1 with "REWIND"	X	X	X	X								X			X	
Load CS1 with "DRIVE CLEAR"	X	X	X	X											X	
Load CS1 with "WRITE TAPE MARK"	X	X	X	X			X	X	X		X	X		X	X	
Load CS1 with "ERASE"	X	X	X	X					X		X	X			X	
Load CS1 with "SPACE FWD"	X	X	X	X						X		X		X	X	
Load CS1 with "SPACE REV"	X	X	X	X						X		X		X	X	
Load CS1 with "WRITE CHECK FWD"	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Load CS1 with "WRITE CHECK REV"	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Load CS1 with "WRITE FWD"	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Load CS1 with "READ FWD"	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Load CS1 with "READ REV"	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MASSBUS INIT															X	
Write into AS or MT register		X		X												

*Except AS or MT.

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CONTENTS

3.5   SEE PERTEC MANUAL

3.5.1   Tape Unit Status Sensors

The tape status (EOT/BOT) and write lock sensor features are discussed in this section.

EOT/BOT Sensor - To locate the beginning and end of the recording area on the tape, the load and end points are marked by reflective strips mounted on the nonoxide side of the tape. The dimensions and placement of these strips are shown in Figure 3.5-1.

The strips are detected by the phototransistors of the EOT/BOT sensor assembly. It consists of an EOT sensor phototransistor, located to detect light reflected from the EOT strip; a BOT sensor phototransistor, located to detect light reflected from the BOT strip. The outputs of the EOT and BOT signals are amplified, filtered, and converted to logic levels, producing signals BOT (SB) L, END PT H, and END PT (SB) L.

The assertion of END PT H sets a flip-flop, which remains set until either the tape is rewound or EOT is negated while the tape is traveling in the reverse direction. Thus, if the tape is moved forward past the EOT marker, the END PT flip-flop remains set even after the marker is passed and is cleared only by rewinding or reversing the tape back past the EOT marker. Setting the END PT flip-flop has the following effects:

1. If the TU45 is off-line forward tape motion stops and the transport does not accept manual forward commands until the tape is rewound or reversed off the EOT marker.

2. If the TU45 is on-line and selected by the TM02, the TU45 signal END PT (SB) L is asserted, indicating to the TM02 that it has passed the end point.

NOTE

Notice that if TU45 is on-line, it does not stop automatically upon detecting EOT. It is permissable to write data up to 10 ft. past the end point. It is up to the programmer to ensure that he does not run past this point.

The assertion of BOT H has the following effects:

1. The TU45 accepts no new rewind commands.

   The LD PT indicator is lit.

2. If the TU45 is on-line and selected by the TM02, it asserts the transport bus signal BOT (SB) L, indicating to the TM02 that it is at BOT.

Write Lock - To protect tapes from inadvertent erasure, tape reels are provided with a write enable ring. If a reel of tape is mounted on the TU45 Tape Transport with its write enable ring removed, this condition is sensed and the transport refuses to honor any write commands. Further, if the transport is on-line and selected by its controller, it asserts WRL (SB) L to the TM02 Tape Controller, indicating to the TM02 that it is write-locked.

RECORDING AREA
SEE NOTE 2

PHOTO REFLECTIVE MARKERS
SEE NOTE 1

0.03-IN. MAX

EOT

0.498
±0.002 IN.

HUB END

RIM END

REFERENCE
EDGE

10 FT.

BOT

0.03-IN. MAX

25 FT. +5 FT.
-0 FT.

15 FT. ±1 FT.

BACK SIDE

0.0019
±0.0003 IN.

MAGNETIC SIDE

HUB END

RIM END

MAGNETIC SIDE

BACK SIDE

FRONT VIEW
SCHEMATIC OF TAPE WINDING

NOTES:
(1) Photo reflective markers shall not protrude beyond edge of tape and shall be free of wrinkles and excessive adhesive. Marker dimensions: length, 1.2 ± 0.2 inch; width, 0.19 ± 0.02 inch; thickness, 0.0005 ± 0.0001 inch.
(2) Minimum for test area; maximum for recording.
(3) Tape shall not be attached to the hub.

CP-0223

Figure 3.5-1 Tape Markers, Recording Area, and Tape Wind

Principally, the assembly consists of the write-lock solenoid and the write-lock switch. When no write enable ring is inserted in the file reel, a feeler attached to the end of the solenoid shaft extends into the write-lock slot on the back of the reel. This feeler puts the write-lock switch in its normally closed position, asserting WRL (SB) L. When a write enable ring is inserted in the file reel, the ring pushes back the solenoid shaft, actuating the write-lock switch and negating WRL (SB) L. If the write enable switch is actuated the write-lock solenoid is engaged to withdraw the write-lock feeler from contact with the ring. This keeps the write-lock switch actuated until the tape is unloaded and reduces wear of the write-lock assembly and write enable ring during tape unit operation.

3.5.2 On-Line Operation

When the TU45 is on-line all transport operations are directed by the TM02 via the slave bus. The slave bus connects the TM02 Tape Controller to up to eight TU45 Tape Transports.

3.5.2.1 Transport Selection and Status Reporting - All of the tape transports in a system are wired to the same slave bus, but only one transport can be logically connected to the bus at one time, i.e., only one transport can transmit its status to the TM02 Tape Controller and respond to commands, and only one transport can be reading or writing data at a given time.

To select the particular tape transport to converse with the tape controller, the controller transmits a binary code on bus lines SS00 (SB) L, SS01 (SB) L, and SS02 (SB) L. Each transport on the bus compares this code to the transport number determined by the unit select switch. If the selection code transmitted by the TM02 Tape Controller matches the transport number, and the transport is on-line, the transport logically connects itself to the slave bus. All other transports remain logically disconnected and neither transmit nor respond to bus signals.

When a particular transport is logically connected to the slave bus, it transmits status information to the tape controller as follows:

7CH (SB) L   Always negated in the Tape Transport.

BOT (SB) L   Asserted when the tape is positioned at load point (beginning of tape).

END PT (SB) L   Asserted when the End Point flip-flop is set.

WRL (SB) L   Asserted when the Tape Transport is write-locked.

RWS (SB) L   Asserted when the Rewind Status (RWS) flip-flop is set.

SDWN (SB) L   Asserted when the transport is settling down following an operation, i.e., asserted for about 5.0 ms following the command to terminate an operation while the capstan is coming to a halt.

TUR (SB) L   Asserted when the tape unit is ready to receive any command; i.e., when the transport is neither performing an operation nor settling down following an operation.

3.5.3 Tape Motion Initiation (On-Line)

When DRV SET PLS is generated by the Massbus Interface module (MBI 6), the TM02 negates STOP L (TCCM 3) and asserts SLAVE SET PLS L (TCCM 4) and EMD L (TCCM 3) on the slave bus (Figures 3.5-2 and 3.5-3). During a read or write data operation, this is a consequence of the assertion of RUN H by the Massbus Controller. During nondata transfer operations that require tape motion, this is a consequence of loading the corresponding function code (GO bit set) into the Control register (R00).
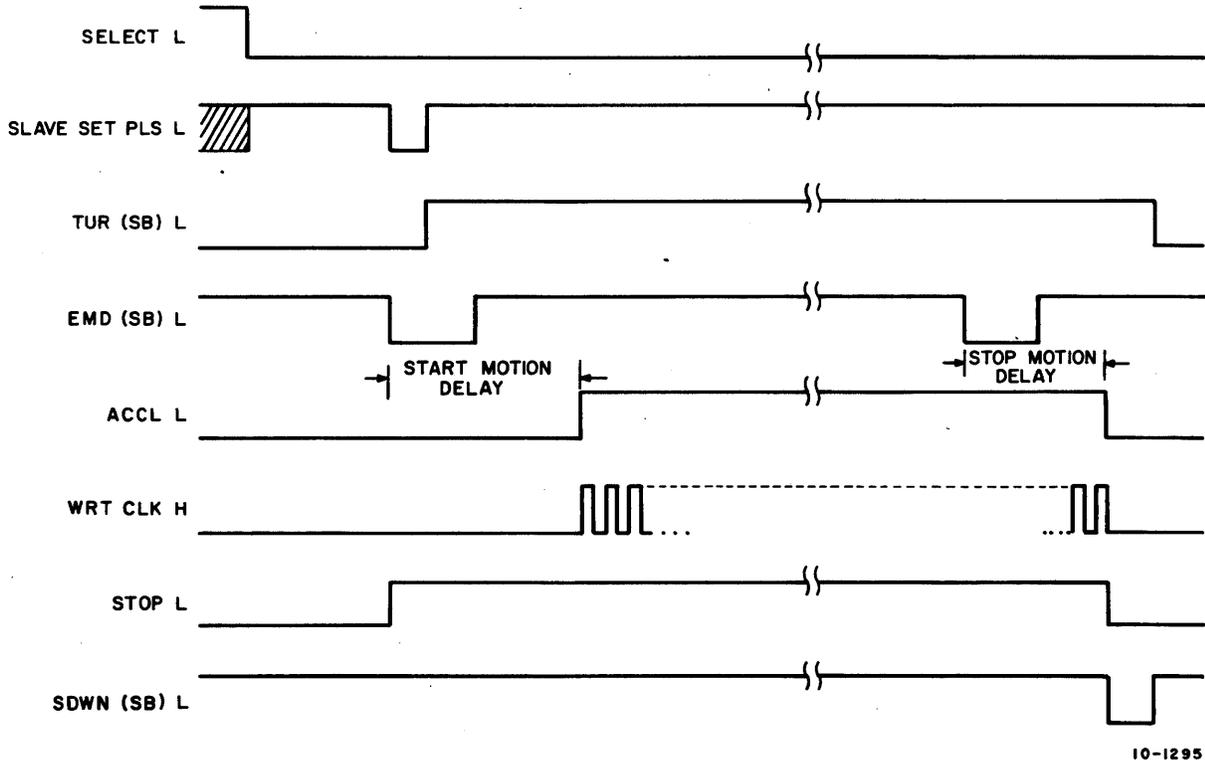
Figure 3.5-2 Tape Motion Timing

If a TU45 is selected, on-line, and loaded with tape (MOL H asserted), it responds to SLAVE SET PLS and the FWD, REV, and RWND command lines of the slave bus by setting the corresponding motion control flip-flops [i.e., FWD, REV, and RWND flip-flops]. If the WRITE command line is asserted, along with the RWND command line, SET OFFLINE L is generated. If WRITE is asserted but RWND is not, SLAVE SET PLS sets WRITE H (MTA) and is transmitted to the TU45 to activate WRITE and ERASE circuits.

Motion control signals (FWD(1) H, REV(1) H & RNND H) within the MTA
control the capstan servo and drive circuits as described in the TU45
Manual. At the same time, WRITE(1) H (IN MTA), if set, causes tape to
be erased, generating IRG as the tape comes up to speed and the start
motion delay times out. Simultaneously with motion initiation, EMD L
gates the motion delay presets onto the Read Data lines of the slave
bus (SC 2) and loads them into the Motion Delay Counter in the TM02
(TCCM 3). When EMD L is negated, the counter is upcounted by 800 BPI
CLK until it reaches a count of 2 to the 14th power, at which time
ACCL H and READING L are asserted, and further clocking is inhibited.
The presets of the counter determine the time interval necessary to
reach a count of 2 to the 14th power, and hence the duration of the
motion delay. When an erase or write tape mark operation is
performed, the presets to the motion delay may be modified.
Modification occurs only when starting in the forward direction, not
from BOT (E60 pins 3, 4, 5, and 6), and adds 48 ms to the start motion
delay; this produces an extended IRG on tape. The presets depend on
the type of operation performed (read/write), the direction of tape
motion, and other parameters. Table 3.5-1 lists the motion delays
generated under the various conditions. READING L enables the read
circuitry in the TM02. ACCL L is transmitted to the TU45, where it
enables generation of WRT CLOCK and other read and write functions.

Once forward or reverse tape motion is initiated, it continues (unless
a TU45 mechanical or power failure is sensed) until the TM02 transmits
STOP L asserted to the transport.

If a rewind operation is being performed, STOP L is asserted as soon
as DRV SET PLS is negated. Once the Rewind Status flip-flop is set,
the TU45 performs the rewind operation independently. The TU45
notifies the TM02 that it is performing a rewind by asserting RWS L on
the slave bus. When the rewind control sequence is over, motion
terminates automatically and the TM02 is notified when the TU45
asserts SET SSC L (Slave Status Change) on the slave bus.

Table 3.5-1

Start and Stop Motion Delays

Start/Stop	Direction of Motion	Operation		
		Read/Space	Write	Erase/Write Tape Mark
	Reverse	1.6 ms		
Start Motion Delays	Forward	1.6 ms	4.8 ms	53.3 ms
	Forward from BOT	8.5 ms	72.5 ms	72.5 ms
	Reverse	1.0 ms		
Stop Motion Delays	Forward	0	.53 ms	.53 ms

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SLAVE (MTA, M8921)

DATA-TRANSFER OPERATION   NON DATA-TRANSFER OPERATION

RECEIVE RUN H ASSERTED

CONTROL REGISTER LOADED (GO BIT SET)

SB FWD ASSERTED ? — NO / YES

SB REV ASSERTED ? — NO / YES

SB RWND ASSERTED ? — NO / YES

SB WRITE ASSERTED ? — NO / YES

SB WRITE ASSERTED ? — NO / YES

DRIVE SET PULSE

SLAVE SET PULSE

ENABLE MOTION DELAY

SET FWD FF

SET REV FF

SET RWND FF

SET FF OFF-LINE

SET WR ENAB FF

PLACE SLAVE OFF-LINE

ENERGIZE WRITE & ERASE HEADS

GATE OUT MOTION DELAY PRESETS

GENERATE MOTION

TU45

LOAD MOTION DELAY COUNTER

DRIVE CAPSTAN SERVO

COUNT UP TO 2^{14}

NEGATE ACCL L

ASSERT READING L

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Figure 3.5-3   Tape Motion Initiation Flowchart

3.5.4   Tape Motion Termination (On-Line) STOP L

The TU45 terminates tape motion when a pulse clears the motion control flip-flops (M8921). Several sequences cause this to happen, depending on the type of operation being performed (Figure 3.5-4). The various sequences are discussed in the following paragraphs.

3.5.4.1   Read - During a read operation, the motion termination sequence begins when the read circuitry negates RST SHDN CNTR+ this occurs when the read heads presumably encounter the IRG after reading a data record or tape mark.

When a tape mark or data record (24 preamble characters for PE, 10 data characters for NRZI) is encountered, ENBL SHDN CNTR L is asserted (TCPE 5 and CNRZ 4) because the Gap Detection Timer (TCCM 5) will be inactive, and E35 pin 8 will be low. This allows ENBL SHDN CNTR L to gate 200 BPI CLK H to shutdown Counter (E51).

When no envelopes are detected in PE mode, (ANY ENV H negated), or when no RSDO pulses are received from the TU45 in NRZI mode, RST SHDN CNTR L is negated. This allows the Shutdown Counter to be upcounted. If the counter reaches a count of 15, EOR PLS and EOR CLR L are produced. EOR CLR L asserts EMD L, (TCCM 3) and thereby initiates a stop motion delay. EMD L loads the motion delay counter with presets gated by the TU45 onto the Read Data lines of the slave bus, just as occurred during motion initiation (Paragraph 3.5.3). The presets will, however, be different during start and stop delays.

Note that because ACCL H was negated (E15, pin 2, a high), the two most significant bits of the motion delay counter are preset high, asserting DECL H and negating READING L. The counter is upcounted until overflow, at which time DECL H is negated and ACCL H is asserted. The leading edge of ACCL H clocks the Stop flip-flop (E57), causing STOP L asserted to be transmitted to the TU45. STOP L clears the FWD or REV motion control flip-flop, and thereby causes the capstan activating signal to be removed. As tape motion slows down, SDWN L is asserted by the TU45 and transmitted to the TM02. When tape motion stops, TUR L is asserted and transmitted to the TM02.

3.5.4.2 Write - Termination during a write is almost identical to that during a read. Note the difference:

1. The Gap Detection Timer (TCCM 5) is active, because WRT CLK ENBL L is asserted during the write. Thus ENBL SHDN CNTR L cannot gate clock pulses to the Shutdown Counter until 1.6 ms (24 200 BPI CLK pulses) after the last character is written.

3.5.4.3 Erase - Termination during an erase follows a sequence similar to that of a write. The sequence starts as soon as the start motion delay is over (READING L asserted). This activates TCCM 5 E41 (pins 8, 9, and 10), and causes the Shutdown Counter to be upclocked immediately, because RST SHDN CNTR L remains unasserted. Thus the stop motion delay follows the start motion delay almost immediately, and tape (approximately 3 in.) is erased throughout.

WRITE

RECORD DETECTED ? — NO

YES

ASSERT ENBL SHDN CNTR L

GAP DETECTION TIMEOUT — NO

YES

READ

RECORD DETECTED ? — NO

YES

ASSERT ENBL SHDN CNTR L

OPI

ERASE

START MOTION DELAY OVER ? — NO

YES

REWIND

DETECT BOT ? — NO

YES

DRIVE CAPSTAN FORWARD

SET FWD MOTION CONTROL FF

DETECT BOT ? — NO

YES

GATE CLOCK TO SHUTDOWN COUNTER

RESET SHUT-DOWN COUNTER — YES — TAPE CHARACTERS DETECTED ?

NO

COUNT SHUT-DOWN COUNTER

SHDN=15 ? — NO

YES

GENERATE END OF RECORD PULSE

1

1

ENABLE MOTION DELAY

GATE MOTION DELAY PRESETS ONTO READ DATA LINES

| ASSERT DECL H | NEGATE READING L | LOAD MOTION DELAY COUNTER |
| NEGATE DECL H | ASSERT ACCL L | COUNT TO OVERFLOW |

ASSERT STOP L

| ASSERT SDWN L | CLEAR MOTION CONTROL FFs |

STOP TAPE MOTION

NEGATE SDWN L

CLEAR WR ENAB F.F. (IF SET)

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Figure 3.5-4   Tape Motion Termination Flowchart

3.5.4.4 Space - Termination during a space is similar to that of a read. Each time an IRG is detected, a stop motion delay is generated and STOP L is transmitted to the MTA (TU45) and clears the motion control flip-flop. However, as soon as SDWN L asserted is received by the TM02, a DRV SET PLS is generated, which produces a start motion delay and a SLAVE SET PLS. This causes the motion control flip-flop to be set once again. Thus, start motion delays and stop motion delays are produced as each record is spaced.

Each time a record is detected, the Frame Count register is incremented. When the Frame Count register overflows, or when a tape mark is detected, further DRV SET pulses are inhibited; the motion control flip-flop remains cleared, and tape motion ceases.

3.5.4.5 Rewind - Once the RWND flip-flop in the TU45 is set, the transport performs the rewind operation independently. The transport rewinds past the BOT marker, then spaces forward until it encounters the BOT marker again. RWND STATUS H will go low. It also causes RWD STATUS to change (MTA) and assert SSC PULSE on the slave bus.

3.5.4.6 Operation Incomplete (OPI) - The OPI bit of the Error register is set when the end of a record is not detected within 4.2 sec of the initiation of a read or a space operation, or if the end of a record is not detected within .42 sec after the initiation of a write operation. If OPI H is asserted, 200 BPI CLK H is gated to the Shutdown Counter. The shutdown sequence begins if or when RST SHDN CNTR L is negated. Thus, if a record has not been detected, shutdown begins immediately. If a record is being detected, the shutdown sequence begins at the end of the record.

3.5.5 Performance Checks

Refer to the Acceptance Procedure in the appropriate system manual (TJU45 or TWU45) whichever is applicable.

READ (PE)

CONTENTS

3.6   INTRODUCTION

This section discusses the operation of the TM02 read circuitry when operating in PE mode. The PE read data path (reference Figure 2.6) is covered from the digital read to the inputs of the Bit Fiddler. Bit Fiddler read operation is described in section 3.8 (M8906).

3.6.1   Read Heads and Amplifiers

The outputs of the TU45 Read Amplifier are routed to the slave bus via a type 8266 multiplex on the MTA module M8921. The read data signals are then transmitted to the TCCM module in the TM02, where they are multiplexed to the three Data Sync modules (M8901-YC)*.

* The M8901-YA is used in some earlier TM02's, however the M8901-YC is the most current revision and is the only module currently being shipped.

The output of the SLAVE Read Data flip-flop follows the polarity of the magnetic field on the tape; it contains the data in phase encoded form.

3.6.2 Data Sync

The Data Sync module (M8901-YC) contains three sections, each of which processes a single track of read data (Figure 3.6-1). Each of these sections contains a data discriminator, a phase-locked clock, a Deskew Buffer, error detection circuitry, and error correction circuitry (Figure 3.6-2). To process nine tracks of data, three Data Sync modules are required.

NOTE

Operation of all sections of the M8901-YC Data Sync module is identical. Therefore, all discussions of Data Sync operation reference section A schematics (DS 2 and 3), unless otherwise specified.

3.6.2.1 Phase-Locked Clock - Conversion of phase encoded data into binary data requires generation of a data window for each track in sync with the data transitions in the track. The direction of the data transition within the data window determines whether a 1 or a 0 bit is detected.

The phase-locked clock (DS 3) operates to generate the data window and to keep it in sync with the incoming data stream. The heart of the phase-locked clock is a voltage controlled oscillator (VCO) and a phase detector (type 4044). The phase detector senses the phase relationship between incoming data transitions (BIT STRB) and the VCO output signal divided by 32 (TP3). If the frequency of data transitions increases (decreases), BIT STRB begins to lead (lag) TP3. This increases (decreases) the VCO output frequency and brings the two signals back in phase. Thus, the frequency of TP3 becomes the same as the frequency of BIT STRB. The data window (WINDOW) is generated 90 degrees out of phase with TP3 (DS 2 and Figure 3.6-3).

3.6.2.2 Data Discriminator - The data discriminator converts the phase encoded data on its track into binary form: 1 = high, 0 = low. To do so, the data window must first be synchronized to the frequency of the incoming data. It is for purposes of synchronization that the preamble is used.

READ DATA

```
TRK #      DEC BIT
  1  ------- 2 --->  M8901-YC  SECTION A  --->
                     (SLOT 1)
  2  ------- 0 --->            SECTION B  --->
  3  ------- 4 --->            SECTION C  --->

  4  ------- P --->  M8901-YC  SECTION A  --->
                     (SLOT 2)
  5  ------- 5 --->            SECTION B  --->
  6  ------- 6 --->            SECTION C  --->

  7  ------- 7 --->  M8901-YC  SECTION A  --->
                     (SLOT 3)
  8  ------- 1 --->            SECTION B  --->
  9  ------- 3 --->            SECTION C  --->
```

                                        CS-1617
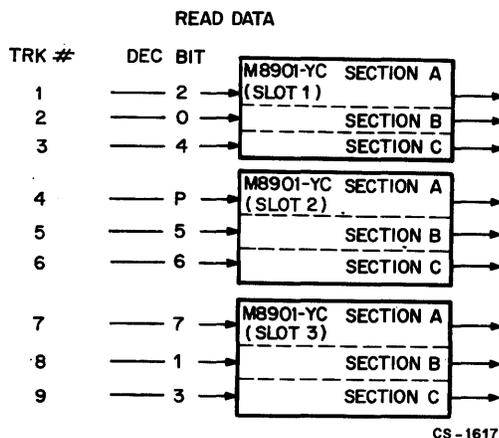
Figure 3.6-1 Data Sync Channels

To understand the operation of the data discriminator, it should be
noted that the data discriminator operates in three modes (Figure
3.6-4):

1. During the start motion delay, READING H is negated, causing
    ANY TRANS L (Any Transition) to be asserted (TCPE 5). During
    this condition, IDB may be detected (Paragraph 3.6.7).

2. When the motion delay times out, ANY TRANS is negated.
    During this condition, preamble 0's may be detected
    (Paragraph 3.6.3).

3. When 24 preamble 0's are detected, RECORD ACTIVE and ANY
    TRANS are asserted. During this condition, the preamble 1's
    character and data are detected (Paragraph 3.6.4).

3.6.2.3 Deskew Buffer - The Deskew Buffer stores the binary data
detected by the data discriminator until a whole tape character
becomes available. Because eight bits of data can be stored for each
track, a skew of up to seven tape characters can be accommodated.

The Deskew Buffer is implemented by nine type 74172 2 by 8 random
access registers. Each register buffers data (RD BUFFER I) and flux
reversal information (BIT STRB OCCURRED) for a single track. Each
register is loaded as data bits become available. The output of the
register depends on its RD ADDR input (common to all the registers
that make up the Deskew Buffer), and is read when a whole tape
character becomes available. The RD ADDR is then incremented, and the
read circuitry waits for the next tape character to become available.
Deskew Buffer operation is described in more detail in Paragraph
3.6.4.1.

3.6.2.4 Error Detection - The error detection circuitry senses when a data transition fails to occur. Error detection is described in more detail in Paragraph 3.6.4.2.

3.6.2.5 Error Correction - The error correction circuitry performs on-the-fly error correction. Error correction is described in more detail in Paragraph 3.6.4.2.

3.6.3 Preamble Detection

Because all sections of the Data Sync modules operate in the same manner, this discussion describes the operation of one section: M8901-YC, Section A, (DS 2 and 3). Reference Figures 3.6-5 and 3.6-6.

The preamble 0's are input to XOR gate E35. If tape motion is in the forward direction (REV L negated), E35 inverts A RDA H; thus, the output of E35 is of proper polarity for both forward and reverse read operations. E15, E14, and their associated circuitry function to produce a positive pulse (BIT STRB H) each time the output of E35 transitions. However, because ANY TRANS is negated and E14 and E24 are "common collectored," BIT STRB H pulses are produced only on negative-going transitions. (The negative-going transition corresponds to the data transition of preamble 0's).

BIT STRB H asserts WINDOW H if it was not already asserted. This operation synchronizes WINDOW H with the incoming data. On its trailing edge, BIT STRB H asserts BIT STRB OCCURRED. Since BIT STRB OCCURRED H is asserted when WINDOW H is negated, ENV H is generated (DS 3, E30). Each time the output of E35 transitions low, BIT STRB H is asserted; ENV H remains asserted as long as BIT STRB occurs at the expected data rate.
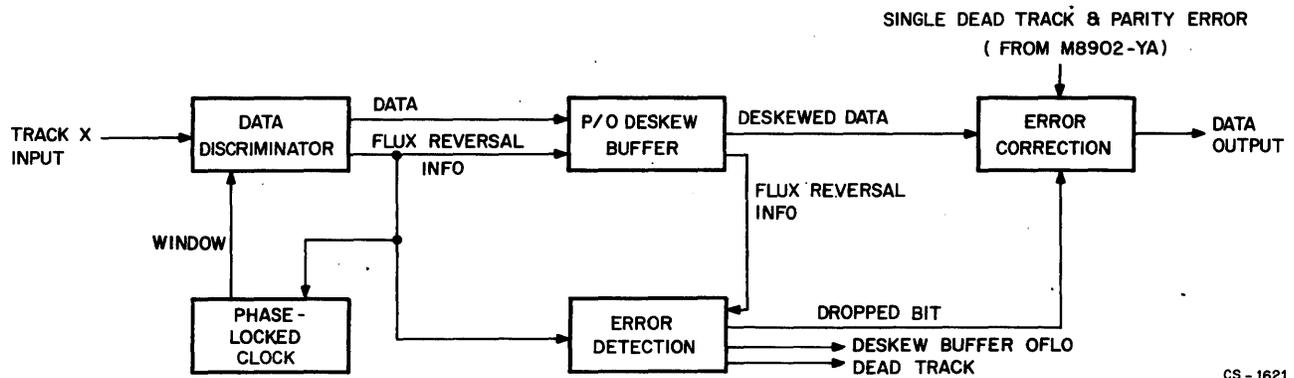
Figure 3.6-2 One Section of the Data Sync Module

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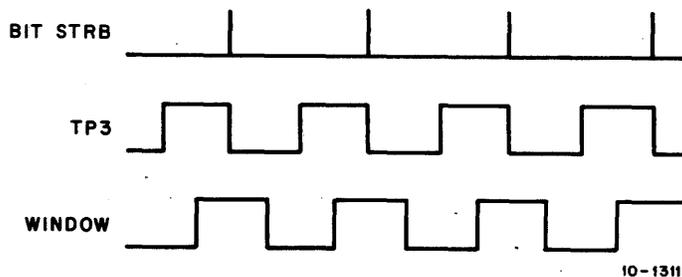
Figure 3.6-3 Data Window Generation
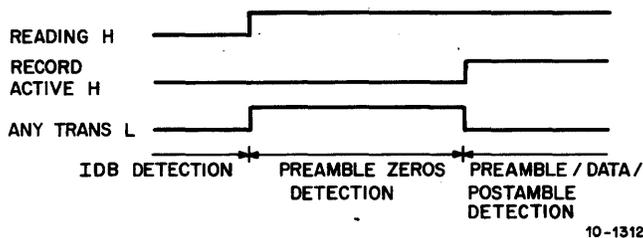
Figure 3.6-4 Data Discriminator Modes

When ENV H is detected on a sufficient number of tracks (TCPE 4), a clear input is removed from the character counter (E9 and E14), allowing it to be upcounted by DATA HALF H. Because DATA HALF occurs at the PE data rate, the outputs of the character counter represent the number of preamble 0's read. When the character counter reaches a count of eight (CT 3 H asserted), the Preamble flip-flop is set (TCPE 5). When the character counter reaches a count of 24 (CT3 H and CT 4 H asserted), the Record Active flip-flop is set. With RECORD ACTIVE asserted, ANY TRANS L is asserted, and the data discriminator operates in its third mode. By this time, the phase-locked clock is synchronized to produce WINDOW H in sync with the data being read.

As preamble 0's continue, WINDOW H is always asserted at the time E35's output transitions low. This transition produces a BIT STRB H pulse which clocks the Read Buffer. But because E35's output is already low, the buffer remains reset.

3.6.4 Data Detection

When the preamble 1's character appears (Figure 3.6-5), BIT STRB H is produced at the positive transition of E35's output (DS 2), thereby setting the Read Buffer flip-flop. Because WINDOW H has been synchronized to the PE data transition time, BIT STRB H occurs only during the data transition time, and will set or clear the Read Buffer depending on the direction of transition. Therefore, the binary output of the Read Buffer is a decode of the RDA phase encoded data.

3.6.4.1 Deskew Buffer - Whenever WINDOW H is negated, the Deskew Buffer (DS 3, E33) is loaded with the contents of the Read Buffer and Bit Strobe Occurred flip-flops. However, during the preamble, only location 000 is loaded each time. When the preamble 1 bit is detected, ONE DETECTED (1) H is asserted (E47 on DS 3). ONE DETECTED (1) H enables the Write Address Generator (E42) to increment the Deskew Buffer write address. Thus, the preamble 1's bit is loaded into address 000. The next bit, i.e., the first data bit, is also loaded into address 000 (Figure 3.6-7). The address is now incremented on each leading edge of WINDOW H, so that the second data bit is loaded into 001, the third into 010, etc. After the eighth data bit, the write address becomes 000 again, and the cycle continues.

With ONE DETECTED asserted, counter E34 (DS 2) is enabled to determine Deskew Buffer status. Each time a data bit is loaded into the Deskew Buffer, the count of E34 is decremented. Each time the Deskew Buffer is read, the count is incremented. Thus, the counter keeps track of how many unread data bits are in the Deskew Buffer.

When the Deskew Buffer contains an unread data bit in each track, BIT READY H (common collectored) is asserted.BIT READY H causes CHAR SHIFT H and ENB RDS L to be asserted (TCPE 3). CHAR SHIFT generates RD SYNC (0) H, which upcounts the Deskew Buffer read address (TCPE 4). ENB RDS L enables generation of RDS H by succeeding BIT READY H pulses. RDS H causes the output of the Data Sync modules [i.e., the contents of Buffer B (Paragraph 3.6.4.2)] to be read and assembled by the Bit Fiddler.

If skew of more than seven characters occurs during the read operation, the Deskew Buffer Status Counter of the leading track will be downcounted to seven, causing OVERFLOW L to be asserted. This sets the INC/VPE error bit in the Error register. A skew of three or more characters causes the CS/ITM bit of the Error register to be set.
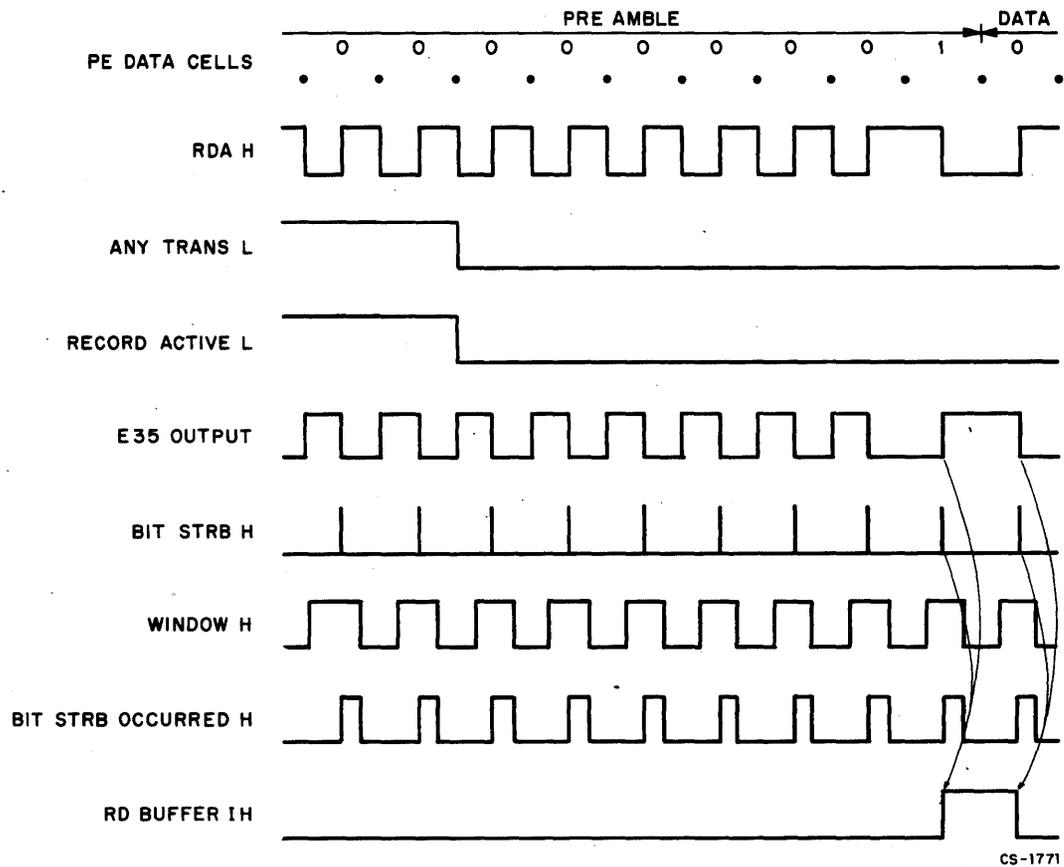
Figure 3.6-5   Data Discriminator Timing Diagram

3.6.4.2   Error Detection and Correction - If BIT STRB does not occur during any data cell, ENV H is negated and the DD TRK (Dead Track) flip-flop (E39) is set. When the data of this data cell is read from the Deskew Buffer and loaded into Buffer A (E22), DROPPED BIT H will be generated as well. The outputs of Buffer A of each track are input to a Parity Generator/Checker (TCPE 2). If there is only one dropped bit and a parity error is detected, PERR AND ONE DD TR H is generated; this means that the content of Buffer A of the dead track is of the wrong polarity. When the next CHAR SHIFT H is generated, this bit is corrected as it is clocked into Buffer B; thus, on-the-fly error correction is achieved.

The outputs of Buffer B are gated by PES B H (Phase Encoded Status Buffered), and become RD B (Read Data B). The RD B lines are multiplexed in the Maintenance Register module (MR 2) and become RD C (Read Data C), and are then transmitted to the Bit Fiddler.
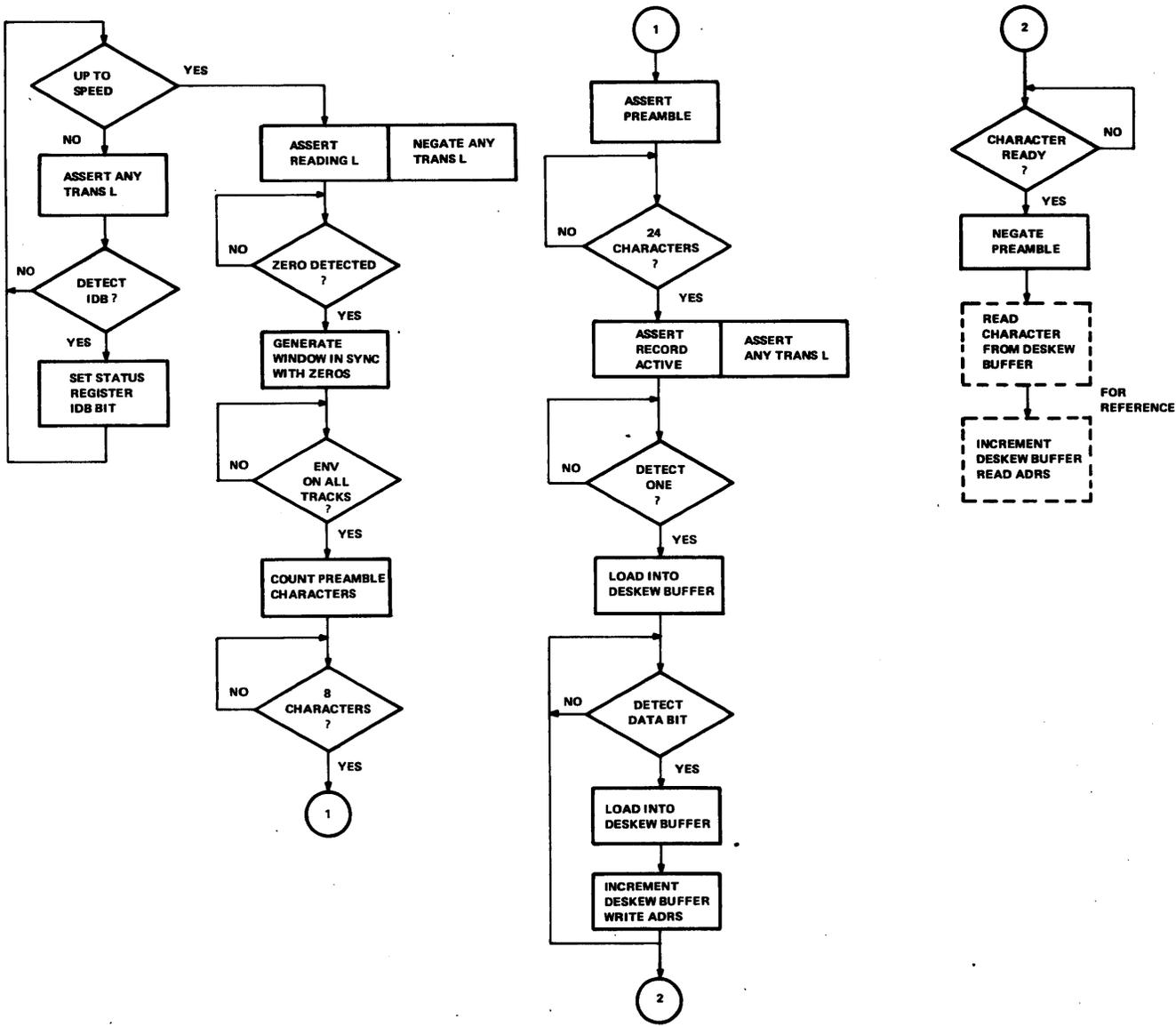
Figure 3.6.6 Preamble/IDB Detection Flowchart

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```
                    ┌─────────────┐
              NO    ╱  DETECT   ╲
             ◄──────╲ DATA BIT  ╱
                     ╲─────────╱
                         │ YES
                         ▼
                ┌──────────────────┐
                │ LOAD INTO        │
                │ DESKEW BUFFER    │
                └──────────────────┘
                         │
                         ▼
        ┌──────────────────┬──────────────────┐
        │ INCREMENT        │ DOWN COUNT       │
        │ DESKEW BUFFER    │ DESKEW BUFFER    │
        │ LOAD ADRS        │ STATUS           │
        │                  │ COUNTER          │
        └──────────────────┴──────────────────┘
                         │
                         ▼
                     ╱─────────╲   NO
                    ╱ CHARACTER  ╲─────►
                    ╲  READY ?   ╱
                     ╲─────────╱
                         │ YES
                         ▼
                ┌──────────────────┐
                │ READ CHAR FROM   │
                │ DESKEW BUFFER    │
                └──────────────────┘
                         │
                         ▼
        ┌──────────────────┬──────────────────┐
        │ INCREMENT        │ UP COUNT         │
        │ DESKEW BUFFER    │ DESKEW BUFFER    │
        │ READ ADDRESS     │ STATUS           │
        │                  │ COUNTER          │
        └──────────────────┴──────────────────┘
                                     │
                                     ▼
                              ╱─────────────╲
                             ╱ TRACK, PARITY ╲
                             ╲ ERROR, AND    ╱
                              ╲ MISSED BIT  ╱
                               ╲──────────╱
                                    │ YES
                                    ▼
                           ┌──────────────────┐
                           │ CORRECT          │
                           │ ERROR            │
                           └──────────────────┘
                                    │
                                    ▼
                           ┌──────────────────┐
                           │ CHARACTER        │
                           │ ROUTED THROUGH   │
                           │ MAINTENANCE      │
                           │ REGISTER BOARD   │
                           │ TO BIT FIDDLER   │
                           └──────────────────┘
```

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Figure 3.6.7 Data Sync Data Read Flowchart

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3.6.5   POSTAMBLE DETECTION

If on any track, a 1 bit followed by a 0 bit is read, POST PAT L is
asserted (DS 3 E28).   If this occurs simultaneously on all tracks,
POST DETECT A, B, C, H is asserted, and the Postamble flip-flop (TCPE
5) is set.

If for any reason, the all-1's postamble character was read or written
improperly, the Postamble flip-flop will nevertheless be set by 8 ZERO
CHARS H. This signal is asserted by the Missed Postamble Detector
(TCPE 4) when eight all-0 characters of the postamble are detected.

With the Postamble flip-flop set, the character counter is further
upcounted, and, when a count of 32 is reached (CT 5 H asserted), MID
POSTAMBLE (1) is asserted. This signal loads the Check Character
register (R07) with dead track information MR 4).

3.6.6   IRG DETECTION

If the read heads are passing over a portion of erased tape, no
envelopes will be detected, and ANY ENB H will be negated. This also
causes RS SHDN CNTR L (reset Shutdown Counter) to be negated (TCPE 5),
and allows the Shutdown counter (E51 on TCCM 5) to be upcounted by 200
BPI CLK H. When a count of 15 is reached, EORS H and RECORD H are
asserted. RECORD H indicates that an IRG is detected, while EORS H
causes a stop motion delay to be generated.

3.6.7   IDB Detection

When the IDB is encountered, the parity read line contains alternate
1's and 0's; no other read lines transition.

The parity line (A RDA) is input to pin 9 of XOR gate E35 (DS 2 and
Figure 3.6.8) on the Data Sync module in slot C02. If tape is moving
in the forward direction (REV L negated), RDA in inverted. Thus, the
output of E35 is of proper polarity for both forward and reverse tape
motion.

Gates E15 and E14 and their associated circuitry produce a narrow
pulse BIT STRB H each time the output of gate E35 transitions. BIT
STRB H sets WINDOW H and, on its trailing edge, sets BIT STRB
OCCURRED.

BIT STRB OCCURRED (1) H is input to the Envelope flip-flop (DS 3).
When WINDOW H is negated while BIT STRB OCCURRED is asserted, this
flip-flop is set, generating ENV H (Envelope). ENV H will remain
asserted throughout the IDB.

RDA P H

WINDOW H

BIT STRB H

BIT STRB OCCURRED H

ENV 4 H

IDB H
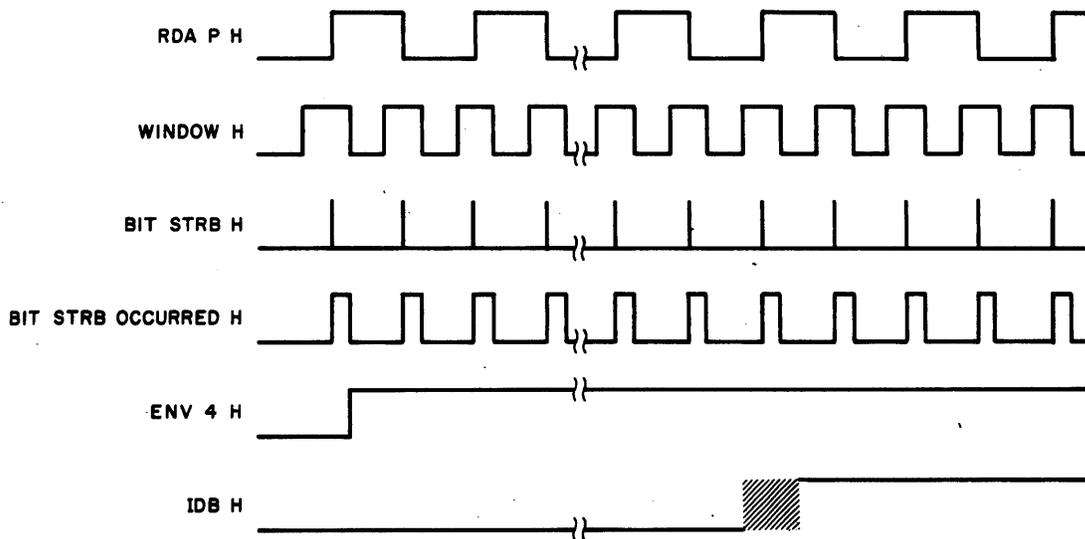
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Figure 3.6.8 IDB Detection Timing Diagram

During the IDB, the only track generating ENV H will be the parity track (track 4). This condition is recognized by circuitry on the Tape Control-PE module (TCPE 4), and allows the IDB Timer to be upcounted by 200 BPI CLK H. When the IDB Timer reaches a count of 8, IDB H is asserted; this prevents further counting of the IDB Timer, and asserts the IDB bit of the Status register (R01).

3.6.8 Tape Mark Detection

A PE tape mark is defined as 0s in tracks 1, 2, 4, 5, and 8, while tracks 3, 6, 7, and 9 are erased. (See Figure 1-3 for Digital to Pertec track designation conversion). This pattern is recognized in the TM02 by the generation of ENV H in tracks 1, 2, 4, 5, and 8, while tracks 3, 6, 7, and 9 do not generate ENV. When this condition is detected, (TCPE 4) FMK PATTERN is asserted, and the corresponding bit in the Status register (R01) is set.

3.6.9 PERFORMANCE CHECKS

Refer to the Acceptance Procedure in the appropriate system manual (TJU45 or TWU45) whichever is applicable.

READ (NRZI)

CONTENTS

3.7   INTRODUCTION

This section discusses the operation of the TM02 read circuitry when operating in NRZI mode. The NRZI read data path (reference Figure 2-6) is covered from the digital read to the inputs of the Bit Fiddler. Read operation is described in section 3.8 (M8906).

3.7.1   Tape Control-NRZI

When RSDO H is received in the TM02, it is used to generate (CNRZ 4) a 390-ns ERDS L pulse (Enable Read Strobe) and RDS H (Read Strobe). ERDS L loads the NRZ Read Latch (CNRZ 2) with the tape character data. The Read Latch outputs are then gated (CNRZ 3) by PES B L (phase Encoded Status Buffered) negated to the Maintenance Register module. The data inputs (RD B) to the Maintenance Register module are multiplexed to the Bit Fiddler. ERDS L also clocks the Read LRCC register (CNRZ 3). Thus, a Longitudinal Parity Check Character and a Cyclic Redundancy Check Character are developed as data is read. This is discussed in more detail in Sections 3.7.3 and 3.7.4.

3.7.2 CRCC Generation and Read

The Read CRCC Generator (CNRZ 3) is clocked at the start of an operation by DRV SET PLS H. The register is then clocked by ERDS H each time a tape character is read, and the Read CRCC is thus developed. Just before the CRCC is read from tape, the register should already contain the CRCC. It should therefore be cleared when the CRCC is read from tape; if not, a CRCC error has occurred. This is detected by E48 and E45 or CNRZ 3, and CRCE ENBL L is asserted. If the read is in the forward direction, CORCRC L is asserted (CNRZ 2), and the corresponding bit is set in the Error register.

During a reverse read, when the second RDS H pulse is produced, REV CRCS L is asserted. During a forward read, FWD CRCS L is asserted when Binary Counter E16 on CNRZ 4 reaches a count of three; this occurs three character cells after the last data character has been read (i.e., when the CRCC is read).

REV CRCS L or FWD CRCS L generate CHK CHAR L. The negative-going edge of this signal clocks the Check Character register (R07) with the CRCC just read from tape.

3.7.3 LRCC Generation and Read

The Read LRCC register (CNRZ 3) is cleared at the start of an operation by DRV SET PLS H. The register is then clocked by ERDS L each time a tape character is read. Each time a one-bit is read on a track, the corresponding bit in the register is toggled. Therefore, just before the LRC tape character is read, the register should contain the LRCC. When the LRC tape character is read, the register should contain all 0's; if it does not an LRCC error has occurred. This is detected by E43, E49, E45, and E13, and LRCE ENBL H is generated. Note that during a reverse read (FWD L negated), LRCC error is inhibited. This is because the LRCC is ignored during a reverse read. LRCE ENBL H causes the PEF/LRC flip-flop (CNRZ 2) to be set, thereby setting the corresponding bit in the Error register.

Because the LRCC is the last character read in a record, it is preserved in the Data Field of the Maintenance register (R03). It can therefore be checked by performing a register read of R03.

3.7.4 IRG Detection

As data is read off the tape and RSDO is transmitted from the TU45 to the TM02, RST SHDWN CNTR L (CNRZ 4) constantly keeps resetting the Shutdown Counter (TCCM 5). If RSDO pulses terminate, the Shutdown Counter is enabled for counting by 200 BPI CLK H. [During a write operation, the Gap Detection Timer (TCCM 5) must first time-out before the Shutdown Counter is enabled.] When the Shutdown Counter reaches a count of 15, EORS H and RECORD H are asserted. EORS H causes a Stop tape motion delay to be generated. RECORD H signifies that IRG has been detected.

If data is again detected after a count of SHDN=8, and before the stop motion delay, a Nonstandard Gap error (NSG) is generated, and the corresponding bit in the Error register is set.

3.7.5 Tape Mark Detection

A set of two isolated characters, separated from each other by six to eight character lengths of erased tape is recognized as an NRZI (nine-channel) tape mark by the TM02.

Refer to the NRZI tape mark detection logic located on CNRZ 4. The Short Record flip-flops E17 were initially cleared by READING H negated, during the start of motion delay. As the read heads pass over the IRG, no RSDO H pulse sets the Tape Mark Window flip-flop, because NO CHAR RD L is asserted. The same RSDO pulse also sets the Short Record I flip-flop, which negates NO CHAR RD L and enables the Binary Counter (E19) to be upcounted by WRT CLK.

If the next RSDO H pulse occurs while the Binary Counter is at a count of 12 through 15, TPMK WINDOW (1) L will remain asserted. At the same time, SHORT REC I (1) H will be negated, and SHORT REC II (0) L will be asserted.

These three conditions activate E13 (pins 1, 2, and 13), and generate ENBL SHDN CNTR L. If no other characters are soon detected, the Shutdown Counter will assert SHDN=8 H, which will cause the NRZ TMRK flip-flop to direct set.

In nine-track tape units, the Binary Counter is preset to 6. Therefore, the tape mark is valid if the second character arrives six to nine character lengths after the first.

3.7.6 Performance Checks

Refer to the Acceptance Procedure in the appropriate system manual (TJU45 or TWU45) whichever is applicable.

BIT FIDDLER READ (M8906)

CONTENTS

3.8 INTRODUCTION

This section discusses the operation of the M8906 Bit Fiddler during a read data operation (reference Figure 2-6). The M8906 Bit Fiddler is used in PDP-11 systems.

3.8.1 M8906 Bit Fiddler Operating Modes

When OCC is asserted on the Massbus, the Bit Fiddler is enabled (BF ENABLE H asserted).[Reference the M8906 schematics and the M8906 Bit Fiddler Read Operation flowchart (Figure 3.8-1).] When DRIVE SET Pulse is generated, tape motion is started and the Bit Fiddler is initialized by P BF RUN H (generated by signal AEMD). The initial state of the Bit Fiddler during a read operation is determined by the tape data format and the direction of tape motion. These parameters determine the initial states of the Select A and Select B flip-flops. The format also determines the manner in which these flip-flops will be toggled (see Table 3.8-1). The Format Select bits (FMT0-3) of the Tape Control Register are decoded in the Bit Fiddler (BF3) as follows:

	FMT(0-3)			Mode
BIT 3	2	1	0	
1	1	0	0	Normal Mode (low order byte first)
1	1	0	1	Core Dump (high order byte first)
1	1	1	0	15 Mode (high order byte first)

Any other combination produces a Bit Fiddler Format Error (BFFMTE).

3.8.2   M8906 Bit Fiddler Read Opertion

When a tape data character becomes available on the Read Data C lines (RDC 0-7), the Bit Fiddler receives RDS. This causes one or two of the Read Latches (E1, E2, E5, and E6 on BFS) to be loaded by CLK A and/or CLK B, or by CLK C and/or CLK D, depending on the states of SELECT A, SELECT B, and CORE DUMP. The states of SELECT B and/or SELECT A are now altered, and, when the next tape data character becomes available and RDS is received, one or two other Read Latches are loaded. The Bit Fiddler thus assembles 18-bit data words (bits 16 and 17 forced set) for transfer to the Massbus Controller. Table 3.8-2 shows CLK A B C D sequences for the different formats and tape motion directions.

After each CLK A B C D cycle, an 18-bit data word, ready for transmission to the Massbus Controller, is sitting on the Data lines. The Bit Fiddler (BF3) generates a parity bit DPA TM which will be transmitted with the data word.

When the data word is assembled, the Massbus Transfer (MB XFR) flip-flop is clocked set. This produces a 1 microsecond pulse SCLK, which is transmitted to the Massbus Controller and causes it to strobe in the word on the Data lines. SCLK also resets the MB XFR flip-flop. Consecutive tape data characters are assembled in the same manner, and each time a data word is ready, SCLK is generated to the Massbus Controller.

Figure 3.8-2 is a timing diagram of Bit Fiddler operation in core dump mode during a read forward operation.

3.8.3   Performance Checks

Refer to the Acceptance Procedure in the appropriate system manual (TJU45 or TWU45) whichever is applicable.

3.8.4   Adjustments

None.

Figure 3.8-1 M8906 Bit Fiddler Read Operation

Flowchart (Sheet 1 of 2)

Column 1 (connector 1):

| MUX CHARACTER | RECEIVE DATA CHARACTER |

| LOAD READ BUFFER | RECEIVE R D S |

| CLOCK FRAME-COUNT REGISTER | TOGGLE SELECT B |

| MUX CHARACTER | RECEIVE DATA CHARACTER |

| · LOAD READ BUFFER | RECEIVE R D S . |

| CLOCK FRAME-COUNT REGISTER | TOGGLE SELECT B |

| | GENERATE S CLK |

Column 2 (connector 2):

| MUX CHARACTER | RECEIVE DATA CHARACTER |

| LOAD READ BUFFER | RECEIVE R D S |

| CLOCK FRAME-COUNT REGISTER | |

| MUX CHARACTER | RECEIVE DATA CHARACTER |

| LOAD READ BUFFER | RECEIVE R D S |

| CLOCK FRAME-COUNT REGISTER | TOGGLE SELECT A & SELECT B · |

| MUX CHARACTER | RECEIVE DATA CHARACTER |

(to connector 3)

Column 3 (connector 3):

| LOAD READ BUFFER | RECEIVE R D S |

| CLOCK FRAME-COUNT REGISTER | TOGGLE SELECT A |

| MUX CHARACTER | RECEIVE DATA CHARACTER |

| LOAD READ BUFFER | RECEIVE R D S |

| CLOCK FRAME-COUNT REGISTER | TOGGLE SELECT A & SELECT B |

| | GENERATE S CLK |

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Figure 3.8-1 M8906 Bit Fiddler Read Operation
Flowchart (Sheet 2 of 2)

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Table 3.8-1

Bit Fiddler Initialization/Operation

Format Mode		Select A		Select B	
		Initial	Toggled By	Initial	Toggled By
Forward	Normal Mode	Clear	Toggling inhibited	Clear	RDS
Tape	Core Dump	Clear	RDS	Clear	Alternate RDS
Motion	15 Mode	Clear	Toggling inhibited	Set	RDS
Reverse	Normal Mode	Clear	Toggling inhibited	Set	RDS
Tape	Core Dump	Clear	RDS	Set	Alternate RDS
Motion	15Mode	Clear	Toggling inhibited	Clear	RDS

Table 3.8-2

CLK A B C D Sequences

Mode	Direction of Tape Motion	Sequence
Normal Mode	Forward	A&B-C&D-A&B-C&D-etc.
	Reverse*	C&D-A&B-C&D-A&B-etc.
Core Dump	Forward	A-B-C-D-A-B-C-D-etc.
	Reverse	C-D-A-B-C-D-A-etc.
15 Mode	Forward	C&D-A&BC&D-A&Betc.
	Reverse*	A&B-C&D-A&B-C&Detc.

*Only normal mode and 15 mode provide proper reassembly in read reverse.
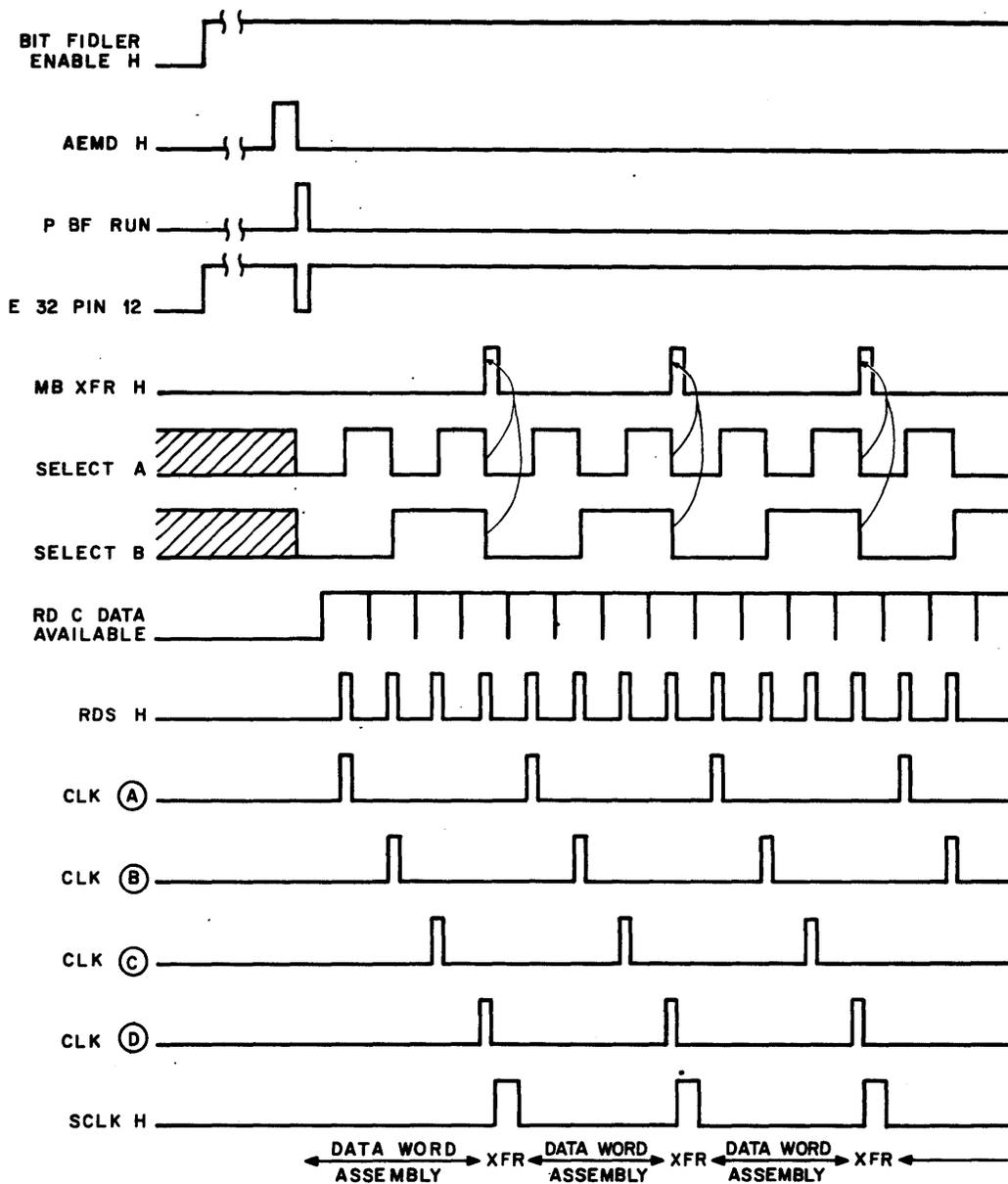
Figure 3.8-2 Bit Fiddler Read Forward Operation
in Core Dump Mode

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BIT FIDDLER WRITE (M8906)

CONTENTS

3.9   INTRODUCTION

This section discusses the operation of the M8906 Bit Fiddler during a write data operation (reference Figure 2-4). The M8906 Bit Fiddler is used in PDP-11 systems.

3.9.1   Bit Fiddler Initialization

Reference the M8906 Bit Fiddler schematics and the Bit Fiddler Write Operation flowchart (Figure 3.9-1).

When the TM02 decodes a data transfer function code in the Control register, OCC TM is asserted (MBI 7); this enables the Bit Fiddler (BF ENABLE H). When the Massbus Controller is ready to transmit data, it places an 18-bit data word on the Data lines of the data bus, places a parity bit associated with the Data lines on the DPA line, and then asserts RUN H.

When the TM02 receives RUN H, DRV SET PLS is generated in the Massbus Interface module (M8909). DRV SET PLS produces AEMD H (TCCM3), a pulse which, on its trailing edge, triggers a one-shot (BF2, E29) and generates P BF RUN H. P BF RUN H initializes the Bit Fiddler by setting or clearing the Select A and Select B flip-flops. Because WRITE L is asserted during a write data operation, P BF RUN H is gated by E25 and also sets the MB XFR (Massbus Transfer) flip-flop. MB XFR H produces a 1 microsecond SCLK pulse, which resets the MB XFR flip-flop and is transmitted to the Massbus Controller.

When the Massbus Controller receives SCLK, it transmits WCLK to the TM02 and then places the next data word and its corresponding parity bit on the data bus. WCLK, enabled by BF ENABLE, produces CLK WRT BUF H, which loads the Bit Fiddler Write Buffer (BF 4). Thus, in a data write operation, the first data word is transferred soon after, and as a consequence of, the assertion of RUN H. Subsequent data words are transferred only after the first data word has been converted to tape characters, i.e., after the motion delay is over (and in PE Mode, after the preamble is written).

3.9.2 Bit Fiddler Formatting

The mode of Bit Fiddler operation during a data write is determined by the selected data format. The Format Select bits (FMT 0-3) of the Tape Control register are decoded in the Bit Fiddler (BF 3) as follows:

	FMT(0-3)				
Bit	3	2	1	0	Mode
	1	1	0	0	Normal Mode
	1	1	0	1	Core Dump
	1	1	1	0	15 Mode

Any other combination produces a Bit Fiddler Format Error (BFFMTE). The selected format determines the initial states of the Select A and Select B flip-flops, and also the manner in which the flip-flops are toggled (refer to Table 3.9-1). SLCT A and SLCT B are inputs to multiplexers E16, E16, and E19 (BF4), and determine the manner in which a data word stored in the Write Buffer is disassembled. Note that in core dump mode, BFO 4-7 are forced low. As SLCT A and/or SLCT B toggle, the data word is multiplexed into characters as indicated in Figure 3.9-2.
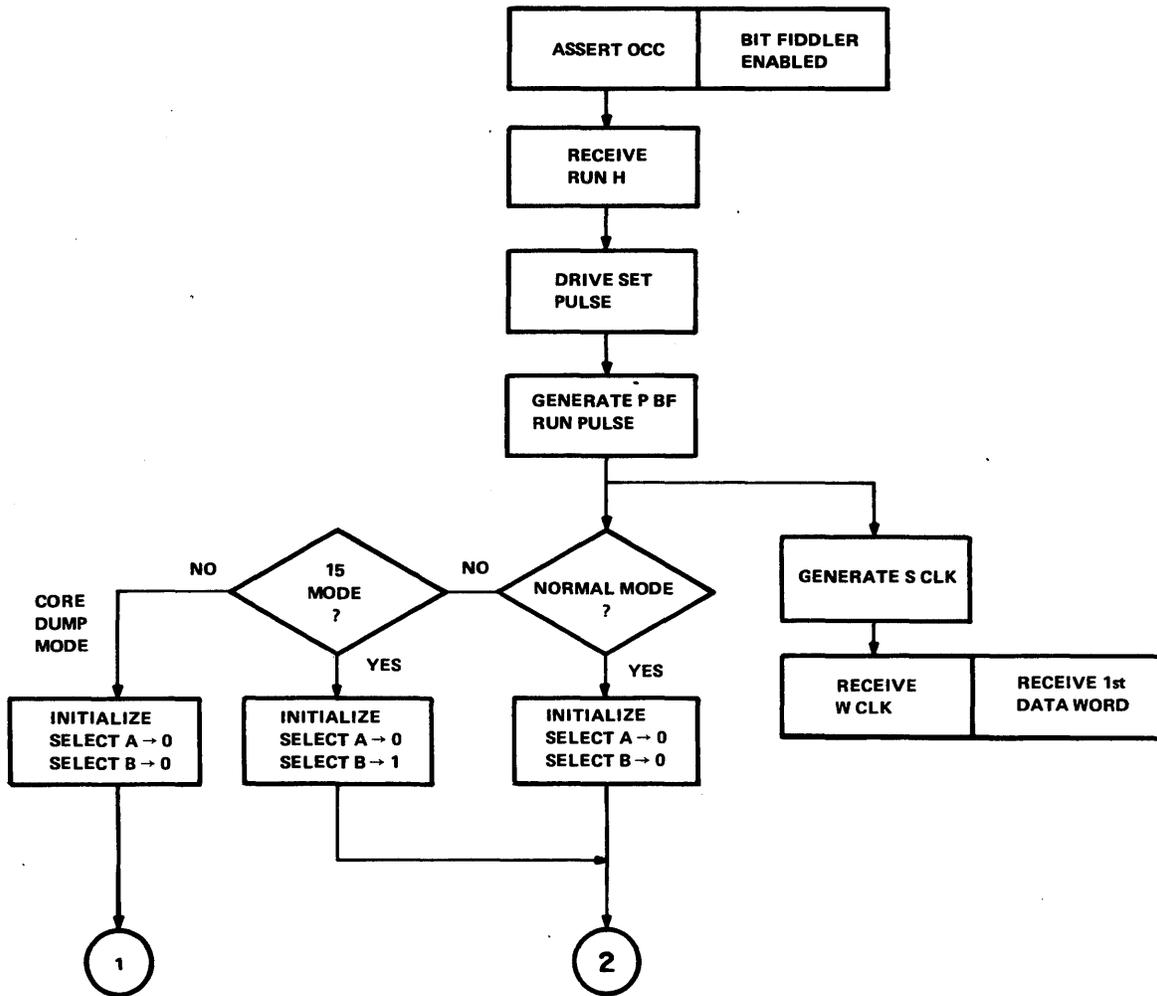
Figure 3.9-1 M8906 Bit Fiddler Write Operation
Flowchart (Sheet 1 of 2)
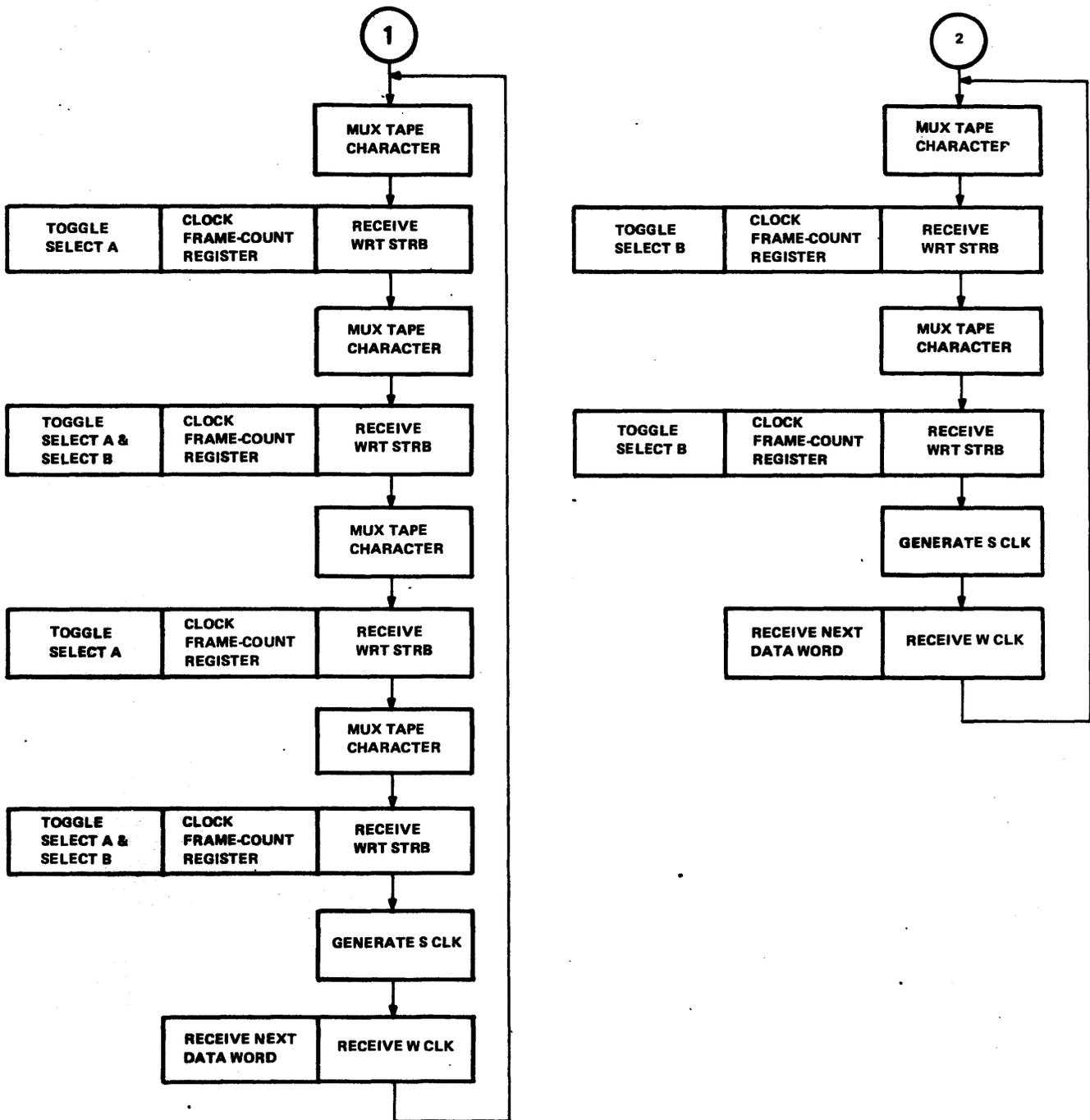
Figure 3.9-1 M8906 Bit Fiddler Write Operation
Flowchart (Sheet 2 of 2)

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Table 3.9-1

Bit Fiddler Initialization/Operation

Format Mode	Select A Initial	Toggled By	Select B Initial	Toggled By
Normal Mode	Clear	Toggling inhibited	Clear	WRT STRB
Core Dump	Clear	WRT STRB	Clear	Alternate WRT STRB
15 Mode	Clear	Toggling inhibited	Set	WRT STRB

3.9.3 Bit Fiddler Timing

When WRT STRB H pulses are received by the Bit Fiddler, it begins disassembling the data word stored in the Write Buffer. In NRZI mode, this occurs immediately after the start motion delay, when the TU45 is at speed and transmits WRT CLK to the TM02. In PE mode, WRT STRB pulses are generated after the preamble has been written.

WRT STRB H is generated on the Tape Control Common Mode module (TCCM 4). When DRV SET PLS H is asserted during a write data operation, the Write Data Record flip-flop (E42) is set, generating WDR H. In NRZI mode, (PESB L negated), this produces a high at E25 pin 6 and E46 pin 8, and enables generation of WRT STRB H when WRT CLK is produced by the TU45. WRT STRB and WRT CLK will be at the same frequency. In PE mode, WRT STRB H is also derived from WRT CLK; however, PE WRT ENABLE L and DATA CLK H must be asserted. This occurs when the data portion of a record is written. Because the frequency of DATA CLK H is half that of WRT CLK, WRT STRB H will also be at half the frequency of WRT CLK H (Figure 3.9-3).

Figure 3.9-4 is a timing diagram for a Bit Fiddler write operation in core dump mode. Each time a WRT STRB H pulse is generated, the Select B and/or Select A flip-flops are toggled. The Frame Count register is also incremented (FCCLK H asserted) at each WRT STRB H. For each combination of SLCT A and SLCT B, a separate character is multiplexed onto the Bit Fiddler output lines; this character becomes available to the write circuitry in the TCCM module.

In core dump (or normal) mode, completion of data word disassembly is detected by E21 (pins 3, 4, 5, and 6) (in 15 mode, E23 pins 1, 2, 12, and 13 detect this condition), and the MB XFR flip-flop is clocked set. MB XFR H generates a 1 microsecond SCLK pulse, which clears the MB XFR flip-flop, and is transmitted to the Massbus Controller. The controller responds to SCLK with a WCLK pulse which loads the Bit Fiddler Write Buffer with the data word on the Data lines. The controller then places a new data word on the Data lines, places a data parity bit on the DPA lines, and waits for the next SCLK pulse, In the meantime, the Bit Fiddler performs its disassembly process on the new word in its Write Buffer. When this word is disassembled, another SCLK is transmitted to the controller; this cycle continues until all the data has been transferred.

Each time the Write Buffer is loaded, a data bus parity check is performed. If there is a parity error, the Parity Error flip-flop (BF 3) is set and SET DPAR H is generated. This causes the DPAR bit in the Error register to be set.

If a WRT STRB H pulse occurs before the Bit Fiddler receives a WCLK response from the Massbus Controller, SET DTE L (Set Data Timing Error) is asserted. This causes the DTE bit in the Error register to be set.

3.9.4 Performance Checks

Refer to the Acceptance Procedure in the appropriate system manual (TJU45 or TWU45) whichever is applicable.

3.9.5 Adjustments

None.
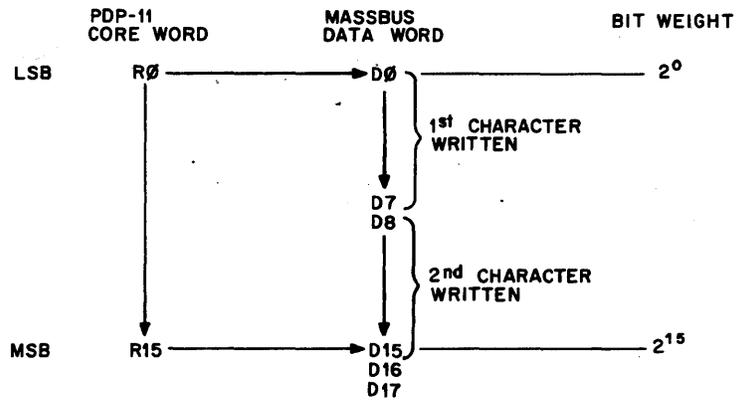
a. Normal Mode
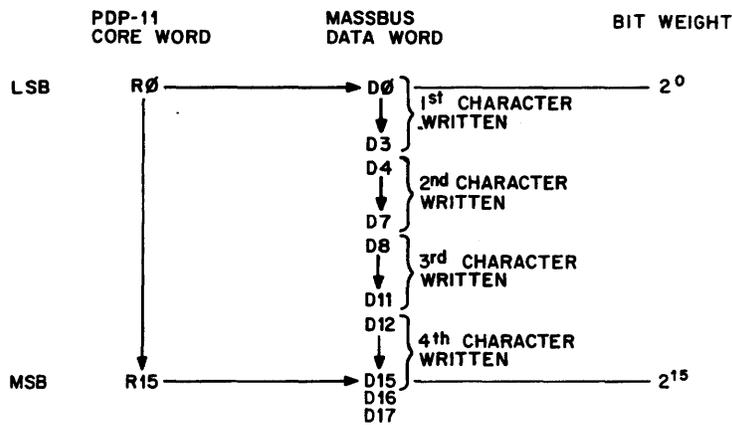
b. Core Dump Mode
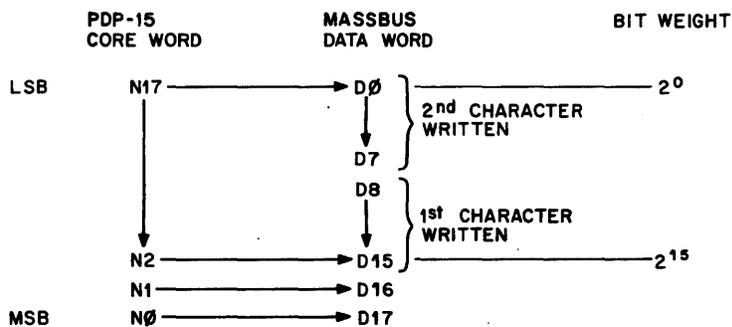
c. 15 Mode

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Figure 3.9-2 M8906 Bit Fiddler Write Formats

WRT CLK H
and WB CLK H

PE CLK L
and DATA CLK H

WRT STRB H
(for PE)

WRT STRB H
(for NRZ)

CS-1884
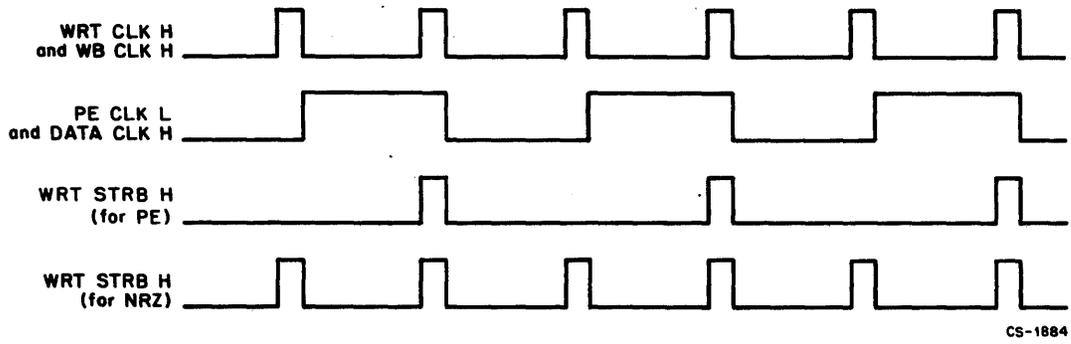
Figure 3.9-3 WRT STRB Timing

BIT FIDDLER
ENABLE H

AEMD H

P BF RUN H

SELECT A

SELECT B

MB XFR H

SCLK H

WRT STRB H

1st XFR
AND
DISASSEMBLY

2nd XFR
AND
DISASSEMBLY

3rd XFR
AND
DISASSEMBLY

ETC.

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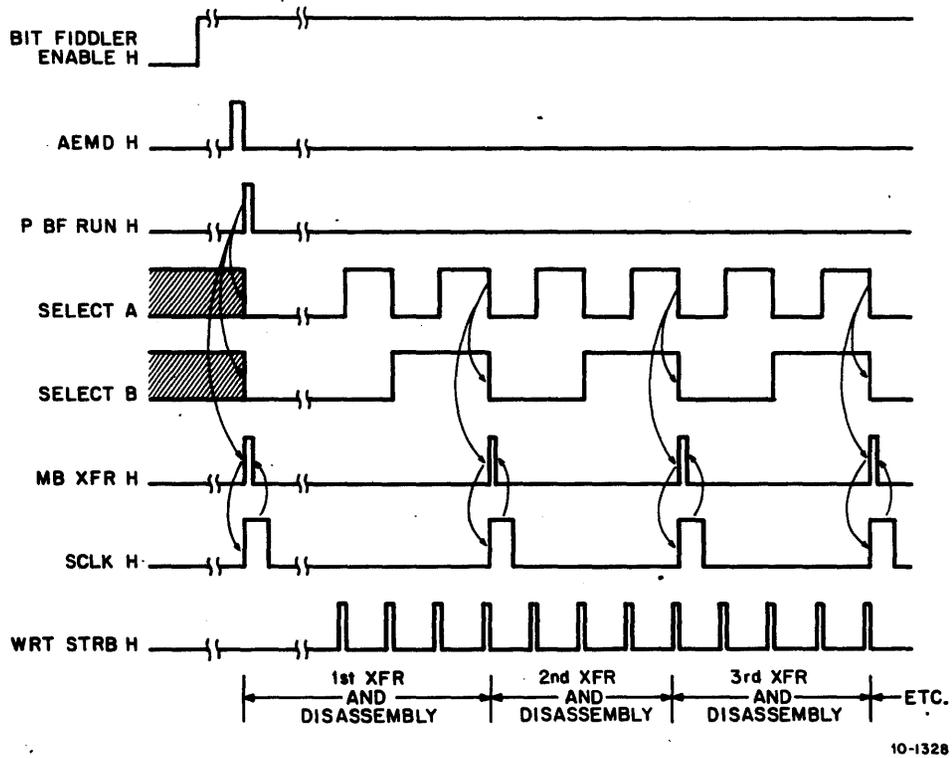
Figure 3.9-4 Bit Fiddler Write Operation in Core Dump Mode

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CONTENTS

3.10   INTRODUCTION

This section discusses the operation of the TM02 write circuitry when operating in PE mode. The write data path (reference Figure 2-4) is covered from the output of the Bit Fiddler to the slave bus. Bit Fiddler write operation is described in section: 3.9 (M8906).

3.10.1   PE Data write

The characters multiplexed by the Bit Fiddler into the Write Data Bit Fiddler Output lines (WDBFO 0-7) are transmitted to the TCCM module. In the TCCM module, the WDBFO lines are input to a parity tree (TCCM 2 E44) and generate a vertical parity bit (odd or even, as determined by the program). The character (parity bit included) is applied to the A inputs of the TCCM Write Multiplex (TCCM 2), and multiplexed to the TCCM Write Buffer.

When the Write Buffer receives WB CLK H, it is loaded with the output of the Write Multiplex. The complemented outputs of the Write Buffer are applied to the D inputs of the Write Multiplex, and loaded into the Write Buffer at alternate WB CLK H pulses. This operation phase encodes the binary data output of the Bit Fiddler.

The uncomplemented outputs of the TCCM Write Buffer are driven across the slave bus to the TU45. The Write Data (WD) lines of the slave bus are received by MTA module (M8921) of the TU45.

3.10.2 PE Data Write Timing

When the TM02 decodes a Write Data function code, it places the WRITE and FWD commands on the slave bus. When the Massbus Controller asserts RUN, the TM02 generates DRV SET Pulse, which sets the WDR (Write Data Record) flip-flop (TCCM 4); this enables generation of WB CLK and REC L pulses when WRT CLK is received from the TU45. The TM02 also transmits SLAVE SET Pulse to the TU45 (MTA). This initiates tape motion and sets the slave in write mode. Since no flux reversals can be effected until WRT CLK Pulses are produced, the tape is dc erased as it accelerates.

When the transport is up to speed (ACCL H negated), the PE Write Major States circuitry (TCPE 3) is enabled; at the same time, the TU45 (MTA) begins to transmit WRT CLK to the TM02. The Write Major States circuitry enables the various segments of a PE data record (preamble 0's, preamble 1's, data postamble 1's, and postamble 0's) to be written. While the preamble is being written, WRT CLK generates WB CLK and REC L pulses (RCCM 4). WB CLK is used in the TCCM write circuitry (TCCM 2) to phase encode the preamble (Figure 3.10-1). REC L is transmitted to the TU45 and causes the phase-encoded characters generated by the TCCM Write Buffer to be transferred to tape.

When the preamble has been written, the Write Major States circuitry asserts DATA H. This enables the generation of WRT STRB in addition to WB CLK and REC L, and changes the mode of the TCCM Write Multiplex operation so that it gates data characters from the Bit Fiddler to the TCCM Write Buffer. The WRT STRB pulses cause the Bit Fiddler to generate tape characters from the data words it receives from the Massbus Controller. WB CLK pulses clock the TCCM Write Buffer and phase encode the Bit Fiddler outputs, while the RECC L pulses, transmitted to the TU45 cause the data to be transferred to tape. The writing of the data portion of a PE record terminates with Frame Count register (R05) overflow.
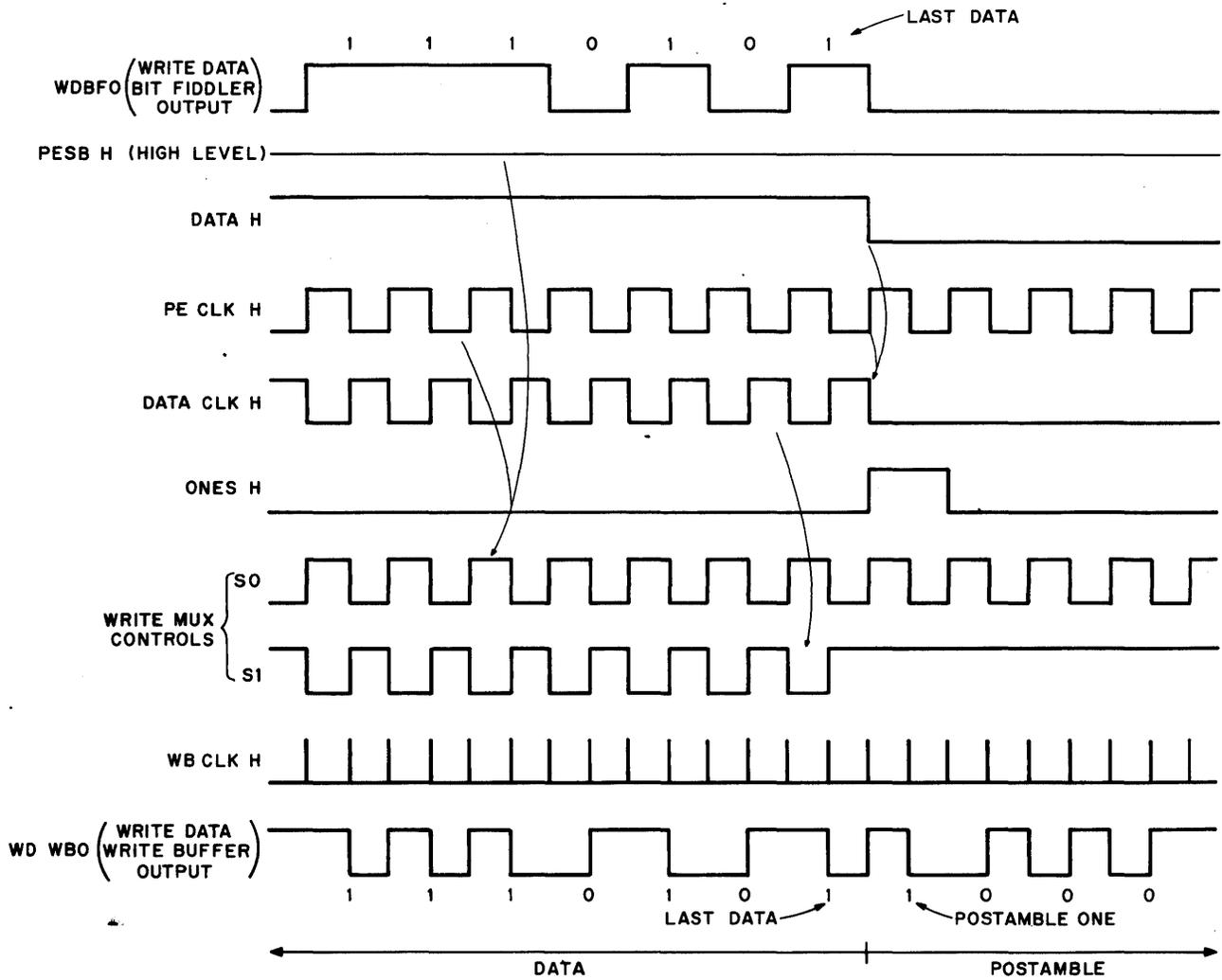
Figure 3.10-1 TCCM Write Operation Timing (PE)

3.10.3 Preamble Write Timing

The Write Major States circuitry on TCPE 3 controls various stages of a PE write data operation. At the beginning of a write data operation in PE mode, WDR H (TCCM 4) enables the PRE 0 flip-flop (TCPE 3) to be clocked set by ST CLK (State Clock). However, Write Major States circuitry operation is inhibited until the end of the start motion (acceleration) delay. When the start motion delay is over (ACCL negated), the PRE 0 flip-flop is set; PRE 0 asserts PE WRT ENB L. At the same time, WRT CLK pulses received by the TM02 produce PE CLK, WB CLK H, and REC L pulses (TCCM 4). PE CLK and PESB (Phase Encoded Status Buffered) cause the S0 and S1 inputs of the TCCM Write Multiplex (TCCM 2) to toggle as illustrated in Figure 3.10-1. Because ONES H is not asserted, phase-encoded 0's are loaded into the TCCM Write Buffer by WB CLK. (The operation is identical to the manner in which postamble 0's are produced, illustrated in Figure 3.10-1.)

The number of preamble 0's generated is counted by E5 and E6 on TCCM 3. (The motion delay counter, of which E5 and E6 are a part, thus serves a dual purpose.) When forty 0's have been generated, FORTY H causes the PRE 0 flip-flop to be cleared and the PRE 1 flip-flop to be set; this asserts ONES L, causing the TCCM Write Bufer to be loaded with a phase-encoded 1's character. REC L pulses are continuously transmitted to the TU45 and cause the forty 0's and the 1's character to be transferred to tape.

After the preamble 1's character is written, the PRE 1 flip-flop is cleared, and the Data flip-flop is set. DATA H asserted causes the data portion of the PE record to be written, as described in Paragraph 3.10.2.

3.10.4 Postamble Write Timing

When the Frame Count register overflows (indicating that the data has been written), WRITE END L is generated (MBI 9) and clears the write Data Record flip-flop (TCCM 4). WDR H negated clears the Data flip-flop (TCPE 3) and causes the POS 1 flip-flop to set. This asserts ONES L, and changes the mode of TCCM Write Multiplex operation (Figure 3.10-1), so that a phase-encoded 1's character is generated and written on tape. The next ST CLK pulse clears the POS 1 flip-flop. This negates ONES L and enables the postamble 0's to be written on tape. The ST CLK pulse that follows sets the POS 0 flip-flop. While POS 0 is asserted, E5 and E6 of the Binary Counter on TCCM 3 are upcounted from 40 to 80, during which time 40 postamble 0's are written on tape. When EIGHTY L is asserted, the POS 0 flip-flop is cleared; this completes the PE record.

3.10.5 PE Tape Mark Generation

When the DRV SET PLS is produced, the write and erase heads are energized and cause the tape to be erased throughout the start motion delay. DRV SET PLS also causes the TMWIP (Tape Mark Write In Progress) flip-flop (TCCM 4 E42) to be set.

When the start motion delay is over, the Write Major States circuitry (TCPE 3) is enabled, and TMWIP H allows the PRE 0 flip-flop to set. This causes the assertion of PE WRT ENB L, which enables generation of PE CLK, WB CLK, and REC L pulses (TCCM 4).

With PRE 0 asserted, almost the same situation exists as when preamble 0's are written (Paragraph 3.12.3). Forty tape characters will be written on tape, as determined by E5 and E6 on RCCM 3. However, because WFMK L is asserted and input to E33 pin 12 on TCCM 2, bits 3, 4, 6, and 7 of the TCCM Write Buffer are force cleared. Thus, instead of all-0 tape characters, only tracks 1, 2, 4, 5, and 8 will contain 0s; tracks 3, 6, 7, and 9 (corresponding to bits 3, 4, 6, and 7) will be erased.

When the 40 characters comprising the tape mark have been written, FORTY H (TCCM 3) causes the PRE 0 flip-flop (TCPE 3) to be cleared; this inhibits further WB CLK and REC L pulses.

3.10.6 IDB Generation

The IDB is written on tape automatically when the TU45 operating in PE mode, is commanded to perform a write operation while at BOT. The circuitry that detects this condition is located on TCCM 3. The count in the motion delay counter (E5, E6, E14 and E15) is used to activate the Write IDB circuitry. During a write from BOT operation, the start motion delay is 74ms. Approximately 0.02ms into the delay, the Write IDB flip-flop (E26) is forced set and asserts WRT ID BURST L. It remains set for 64ms, during which time the identification burst is written.

WRT ID BURST L asserted negates ACCL (SB) L (TCCMM 3); this enables the TU45 (MTA) to transmit WTRT CLK to the TM02. WRT ID BURST also generates PE WRT ENB L (TCPE 3), which enables generation of PE CLK, WB CLK, and REC (TCCM 4). At the same time, WRT ID BURST is input to E33 pin 13 on TCCM 2, and force clears all the bits of the TCCM Write Buffer except for the parity bit. WRT ID BURST H, input to E83 pin 13 on TCCM2, enables PARITY DATA SET UP H, which causes the Write Buffer parity bit to produce alternate 1's and 0's. The net result is alternate 1's and 0's on the parity track (track 4) while all other tracks are erased.

3.10.7 Performance Checks

Refer to the Acceptance Procedure in the appropriate system manual (TJU45 or TWU45) whichever is applicable.

CONTENTS

3.11   INTRODUCTION

This section discusses the operation of the TM02 write circuitry when operating in NRZI mode. The write data path (reference Figure 2-4) is covered from the output of the Bit Fiddler to the slave bus.   Bit Fiddler write operation is described in section 3.9 (M8906).

3.11.1   NRZI Data Write

The characters, multiplexed by the Bit Fiddler onto the Write Data Bit Fiddler Output lines (WDBFO 0-7), are transmitted to the TCCM module. In the TCCM module, the WDBFO lines are input to a parity tree (TCCM 2 E44), and generate a vertical parity bit (odd or even, as determined by the program). The character (parity bit included) is applied to the A inputs of the TCCM Write Multiplex (TCCM 2), and multiplexed to the TCCM Write Buffer.

When the Write Buffer receives WB CLK H, it is loaded with the outputs of the Write Multiplex.   The outputs of the Write Buffer are then driven by type 75451 drivers across the slave bus to the TU45.

The Write Data (WD) lines of the slave bus are received by the MTA module (8921) of the TU45.

3.11.2 NRZI Data Write Timing

When the TM02 decodes a Write Data function code, it places the WRITE and FWD commands on the slave bus. When the Massbus Controller asserts RUN, the TM02 generates DRV SET pulse which sets the WDR (Write Data Record) flip-flop (TCCM 4); this enables generation of WB CLK and REC L pulses when WRT CLK is received from the TU45. The TM02 also transmits TU45 SET Pulse to the TU45 (MTA). This initiates tape motion and sets the TU45. Since no flux reversals can be effected until WRT CLK pulses are produced, the tape is dc erased as it accelerates.

When the transport is up to speed, WRT CLK pulses are transmitted to the TM02 and generate WRT STRB, WB CLK, and REC L pulses. WB CLK is used to load the TCCM Write Buffer with the outputs of the TCCM Write Multiplex (Figure 3.11-1). REC L is transmitted by the TM02 to the TU45, where it causes the tape character presently in the TCCM Write Buffer to be transferred to tape. WRT STRB activates the Bit Fiddler to generate the next character.

WB CLK, WRT STRB, and REC L pulses continue until the WDR flip-flop is cleared. This occurs when the Frame Count register overflows and generates WRITE END (MBI 9).

3.11.3 CRCC Generation

Data input to the TCM is also input to the CRCC Generator (CNRZ 2). The generator, clocked by WB CLK, produces the CRCC by a series of shifts and XORs. The outputs of the CRCC Generator (CRC 0-7, P) are applied to the B inputs of the TCCM Write Multiplex. After the data portion of the record is written, the CRCC is transmitted to the TU45 and written on tape.

3.11.4 CRCC and LRCC Writing Timing

When the data portion of an NRZI record has been written, the WDR flip-flop is cleared; this enables Binary Counter E27 (TCCM 4) to be upcounted by WRT CLK. The counter, initially preset to a count of 8, generates CRC STRB H when it reaches a count of 11, and LRC STRB L when it reaches a count of 15. At a count of zero, further clocking is inhibited. Therefore, three clock pulses increment the counter to 11; another four clock pulses increment it to 15, so that CRC STRB H is produced three character spaces after the data, and LRC STRB L is generated seven character spaces after the data.
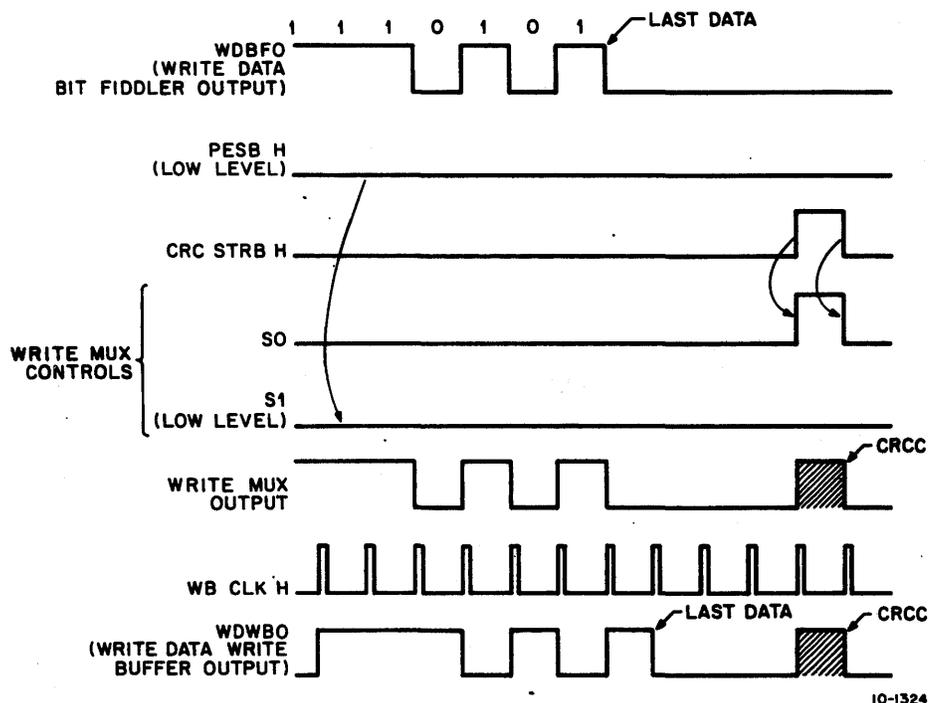
Figure 3.11-1 TCCM Write Operation Timing

(NRZI, 1 of 9 Tracks)

Whenever LRC STRB or CRC STRB occur, WRT CLK ENBL H is momentarily asserted, and gates out one WB CLK H pulse and one REC L pulse.

When CRC STRB H is asserted, the TCCM Write Multiplex (TCCM 2) gates the outputs of the CRCC Generator (CNRZ 2) to the TCCM Write Buffer (Figure 3.11-1). The WB CLK produced at CRC STRB time loads the buffer with the CRCC. The character is driven to the MTA module in the TU45, and applied to the TU45. When REC L is received by the TU45, the Write Buffer in TU45 is clocked, and the CRCC is transferred to tape, three character lengths past the last data character (Figure 3.11-2).

LRC STRB L, input to E38 pin 2 on TCCM 2, clears the entire TCCM Write Buffer and causes 0's to be transmitted to the Write Buffer in the TU45. This signal clears all nine buffers.
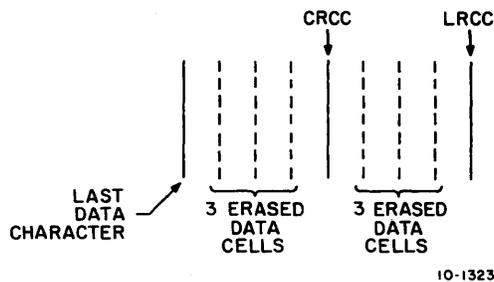
Figure 3.11-2 CRCC and LRCC Timing

3.11.5 NRZI Tape Mark Generation

During a write tape mark operation, WFMK is asserted. WFMK L is input to E24 pin 12 on TCCM 2, and causes all the bits of the TCCM Write Buffer to be cleared, while at the same time NRZ WTMK L, 7CH TM 1 and 7 CH TM 0 are generated. These signals are input to slave bus drivers E13 (pins 6 and 7), E21 (pins 2 and 6), and E12 (pin6), thereby forcing the tape mark character onto the Write Data (WD) lines of the slave bus. The tape mark character forced on the WD lines is 23(8) (nine-channel NRZI format).

3.11.6 Tape Mark Writing Timing

When the DRV SET PLS is produced, the write and erase heads are energized, and cause tape to be erased throughout the start motion delay. DRV SET PLS also causes the TMWIP (Tape Mark Write In Progress) flip-flop (TCCM 4 E42) to set. This loads the type 74197 Binary Counter (E27) and also allows WRT CLK H to be gated by E49 (pins 8, 9, and 10) to produce WB CLK H and REC L.

When the start motion delay is over and the first WRT CLK pulse is received by the TM02, the first WB CLK H produced clears the TMWIP flip-flop; thus, further WB CLK and REC L pulses are temporarily inhibited. The REC L pulse produced, along with the WB CLK H pulse, cause the Write Buffer in the TU45 to be clocked, and transfer the tape mark character to tape.

With the TMWIP flip-flop now clear, the type 74197 Binary Counter is enabled. It operates in the same manner as during a CRCC and LRCC write, except that WFMK H asserted, input to E41 pin 3 on TCCM 4, inhibits the production of CRC STRB H. However, LRC STRB is produced in the normal manner, and occurs seven character spaces after the tape mark character.

LRC STRB L, input to pin 2 of AND gate E8 on TCCM 2, removes the tape mark character forced on the WD lines of the slave bus; this causes 0s to be input to the Write Buffer in the TU45. LRC STRB L, is transmitted to the TU45, and causes the Write Buffer to clear, thereby transferring the LRCC of the tape mark character (which is identical to the tape mark character) to tape.

3.11.7 Performance Checks

Refer to the Acceptance Procedure in the appropriate system manual (TJU45 or TWU45) whichever is applicable.