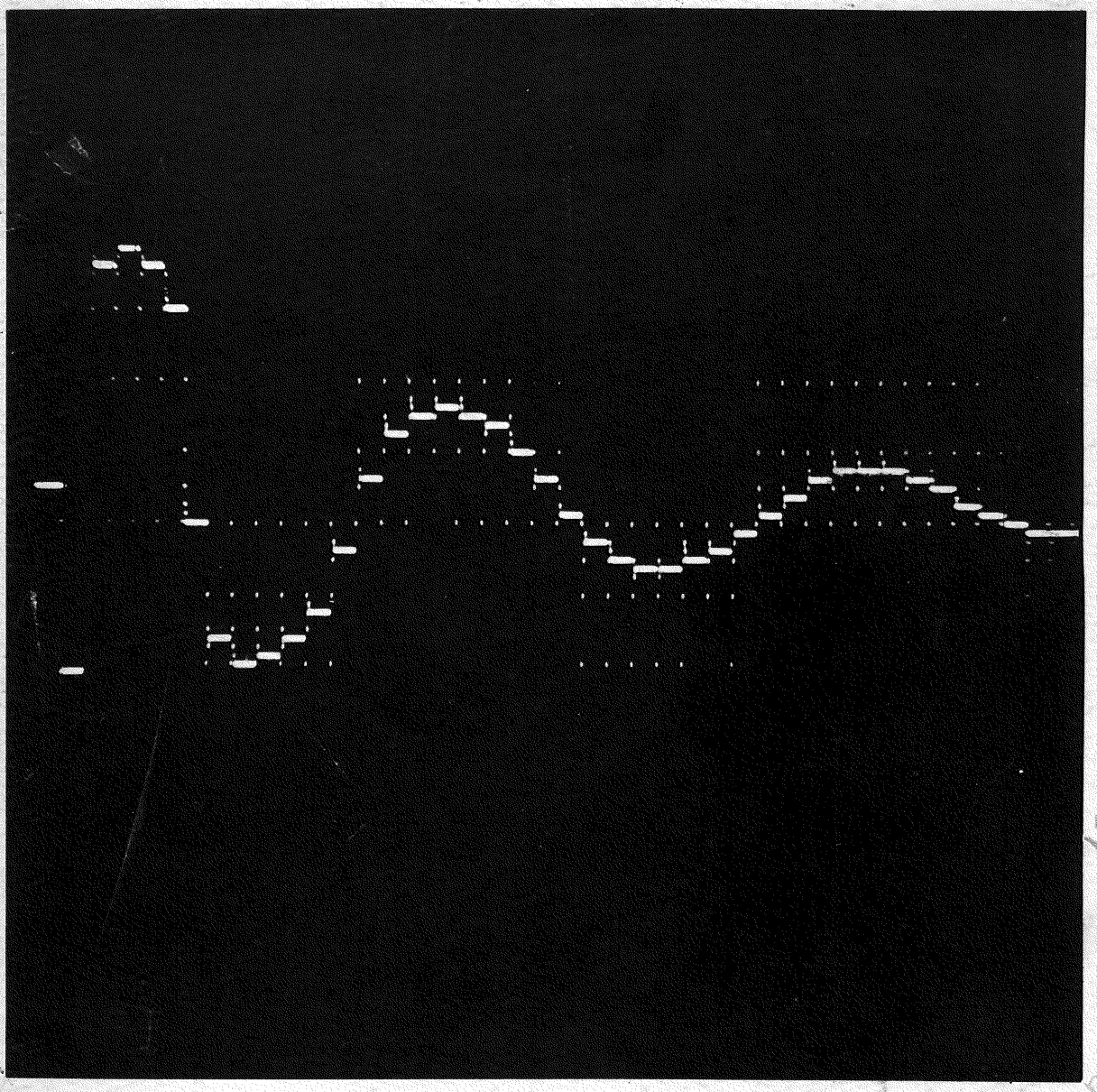
E-5100
7/64



ANALOG ⟷ DIGITAL CONVERSION HANDBOOK

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

The Digital Equipment Corporation makes no representation that the interconnection of its modular circuits in the manner described herein will not infringe on existing or future patent rights. Nor do the descriptions contained herein imply the granting of licenses to make, use, or sell equipment constructed in accordance therewith.

E-5100
7/64

ANALOG—DIGITAL CONVERSION HANDBOOK

Barbera W. Stephenson

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

PREFACE

The Analog-Digital Conversion Handbook represents the first attempt in the data processing industry to assemble comprehensive information on this subject in a form that makes it immediately useful to beginner or expert. All phases of conversion are covered, from concepts to calibration. Many diagrams supplement the text; and tabular summaries of terms, methods, and performance characteristics are included for comparison and reference. Circuit modules and other equipment manufactured by Digital Equipment Corporation are mentioned specifically, so after choosing the conversion method most appropriate to his needs, the reader can construct his system directly.

The use of circuit modules in constructing analog-digital converters yields several advantages. First, they are flexible. Converter systems have widely varying requirements, from pulse height analysis, where differential linearity is of utmost importance, to time-locked averaging in biomedical work, where resolution is more critical than repeatability or even accuracy. Modules permit the construction of the exact type of converter needed and, should requirements change, the same modules can be used later to build a different kind of system.

Second, modules are economical. Aside from the interchangeability mentioned above, savings are gained in the cost of construction. The typical cost of a digital-to-analog converter is about $1,000; of an analog-to-digital converter, about $2,000. If several systems are built, the cost per converter decreases since the same power supplies and mounting panels are used for the additional units. If the speed requirement is exceptionally high, costs will be higher.

A third advantage of using modules is that the completed converter need never go back to the factory for recalibration. Procedures for calibration and adjustment are included in this handbook. Recalibration can be carried out quickly and easily by the user.

Those modules designed exclusively for use in conversion systems are specified in detail in this handbook. The general purpose logic modules also needed are mentioned by name and type number. Complete specifications for these and over 200 other kinds of circuit modules and accessories are contained in the Digital Module Catalog, available at any Digital Equipment Corporation office. The catalog also contains much information helpful in designing and assembling digital systems.

CONTENTS

ILLUSTRATIONS

TABLES

CHAPTER I

BASIC ELEMENTS OF CONVERSION

Introduction

This chapter describes the general technique used to convert, to sample and hold, and to multiplex.

For digital-to-analog conversion, just one technique is described. Though there may be some variations, the same technique is generally applicable for all digital-to-voltage or digital-to-current converters.

Analog-to-digital conversion is somewhat more complex and thus a variety of different methods is commonly used. In this chapter, the four most common methods are described. Of these, the successive approximation converter is most generally used since it provides good performance over a wide range of applications at a reasonable cost. However, if the converter is to be used only in a single application, various other methods may be preferred for better performance or lower cost.

It is suggested that this chapter be read as a brief development of the principles of conversion, rather than a delineation of specific methods. Detailed descriptions of conversion systems will be given in Chapters 3 and 4.

Digital-to-Analog Conversion

To convert from a digital number to an analog voltage, a resistive divider network is connected to the flip-flop register which holds the digital number (see Figure 1). The divider network is weighted so that each bit of the register will contribute to the output voltage in proportion to its value.

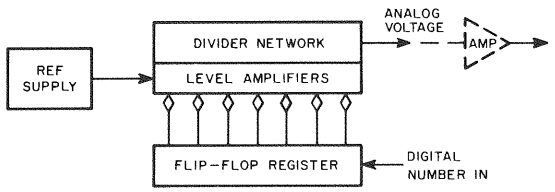


Figure 1 Digital-to-Analog Conversion

The digital input signal determines the analog output voltage, since the divider network is simply a passive element. However, because digital voltage levels are not usually as precise as required in an analog system, level amplifiers are placed between the flip-flops and the divider network. The amplifiers switch the divider network between ground and a

reference voltage supplied by a precision reference supply. The output voltage range is between these two voltage levels. In Digital systems, the range is normally 0 to —10 volts. If the digital-to-analog converter is to drive long cable or a heavy load, an operational amplifier or emitter follower is usually put on the output of the circuit to lower the output resistance.

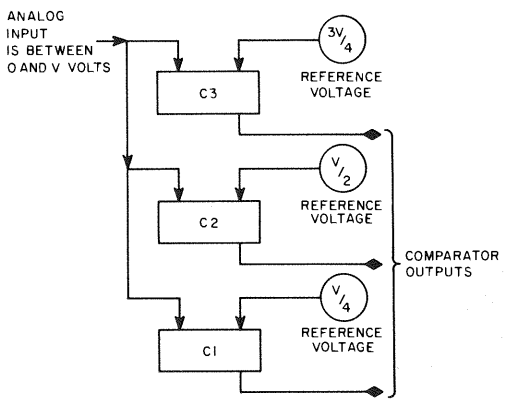
The level amplifiers, divider network, and reference supply shown in Figure 1 are basic to a digital-to-analog converter and are described under those headings in Chapter 5.

Analog-to-Digital Conversion

The basis of analog-to-digital conversion is the comparator circuit. This circuit compares an unknown voltage with a reference voltage and indicates which of the two is larger.

SIMULTANEOUS METHOD

Figure 2 shows how a simple simultaneous analog-to-digital converter can be built using several comparator circuits. Each comparator has a reference input signal. The other input terminal of the comparators is driven by the unknown input analog signal, which is between 0 and V volts. The comparator is called "ON" if the analog input is larger than the reference input. Then, if none of the comparators are on, the analog input must be less than $\frac{V}{4}$. If C-1 is on, and C-2 and C-3 are off, the input must be between $\frac{V}{4}$ and $\frac{V}{2}$. Similarly, if C-1 and C-2 are on, and C-3 off the voltage is between $\frac{V}{2}$ and $\frac{3V}{4}$; and if all the comparators are on, the voltage is greater than $\frac{3V}{4}$.



C_1	C_2	C_3	Input Voltage
off	off	off	0 to V/4
on	off	off	V/4 to V/2
on	on	off	V/2 to 3V/4
on	on	on	3V/4 to V

Figure 2 Simultaneous Analog-to-Digital Converter

Here, the voltage range is divided into four parts, which can be coded to give two binary bits of information. Seven comparators would give three bits of binary information. Fifteen comparators would give four bits. In general, 2^N—1 comparators will give N bits of binary information.

The simultaneous method is extremely fast for small resolution systems. For large resolution systems (a large number of bits), this method requires so many comparators that it becomes unwieldly and prohibitively costly.

FEEDBACK METHODS

If the reference voltage were variable, only one comparator would be needed. Each of the possible reference voltages could be applied in turn to determine when the reference and the input were equal. But a digitally controlled variable reference is simply a digital-to-analog converter. Thus the generalized analog-to-digital converter shown in Figure 3 is actually a closed-loop feedback system. The main components are the same as a digital-to-analog converter plus the comparator and some control logic. With a digital number in the DAC (digital-to-analog converter) the comparator indicates whether the corresponding voltage is larger or smaller than the input. With this information, the digital number is modified and compared again.

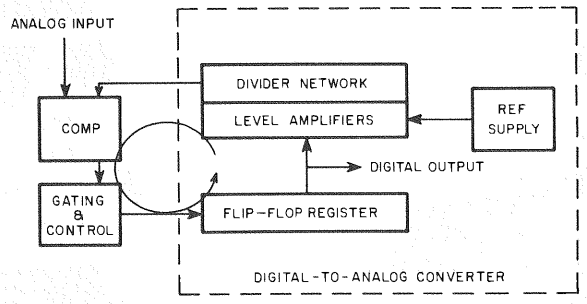


Figure 3 Analog-to-Digital Converter Incorporating a Digital-to-Analog Converter

COUNTER METHOD

Numerous methods may be used for controlling the conversion. The simplest way is to start at zero and count until the DAC output equals or exceeds the analog input.

Figure 4 shows a converter in which the DAC register is a counter, and a pulse source has been added. The gate stops pulses from entering the counter when the comparator indicates that the conversion is complete.

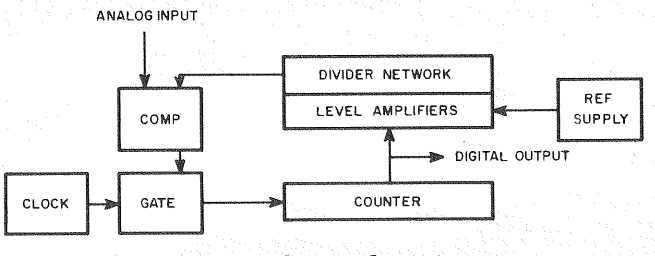


Figure 4 Counter Converter

The counter method is good for high resolution systems: As the number of bits is increased, very little additional circuitry is needed. Multiple inputs can easily be converted simultaneously (as described under Multiplexing later in this chapter). However, conversion time increases rapidly with the number of bits, since an N-bit converter must allow time for 2^N counts to accumulate. The average conversion time will, of course, be half this number.

CONTINUOUS METHOD

A slight modification of the counter method is to replace the simple counter with an up-down counter as in Figure 5. In this case, once the proper digital representation has been found, the converter can continuously follow the analog voltage, thus providing readout at an extremely rapid rate. This method, called continuous conversion, is particularly useful when a single channel of information is to be converted. The converter starts running, and the digital equivalent of the input voltage can be sampled at any time.

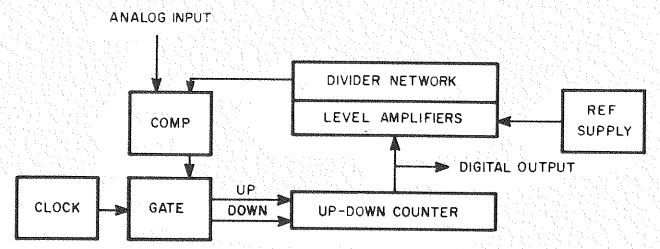
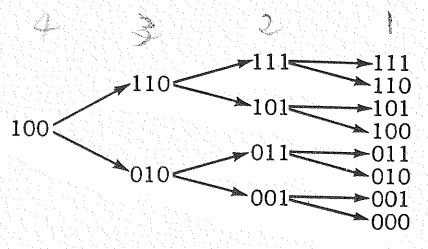


Figure 5 Continuous Converter

The continuous method is less effective for multiple inputs or for inputs that change faster than the converter can change. Each time the input makes a large change, the converter may require as many as 2^N steps to catch up. However, if a rapid rate of change is necessary, extra comparators may be added so that the up-down counter can count in units of 2, 3, 4,or more (see Chapter 3).

SUCCESSIVE APPROXIMATION METHOD

For higher speed conversion of many channels, the successive approximation converter is used. This method requires only one step per bit to convert any number. The successive approximation analog-to-digital converter operates by repeatedly dividing the voltage range in half as follows:



Thus, the system first tries 100, or half scale. Next it tries either quarter scale (010) or three-fourths scale (110) depending on whether the first approximation was too large or too small. After three approximations, a 3-bit digital number is resolved.

Successive approximation is a little more elaborate than the previous methods since it requires a control register to gate pulses to the first bit, then the second bit, and so on. However, the additional cost is small and the converter handles all types of signals about equally fast.

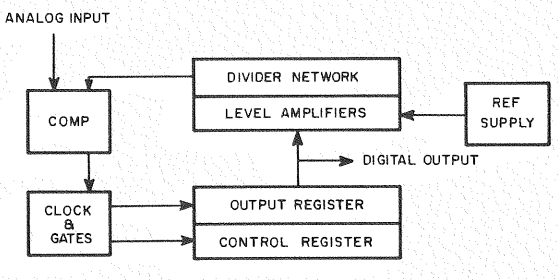


Figure 6 Successive Approximation Converter

The successive approximation method is good for general use. It handles many continuous and discontinuous signals and large and small resolution conversions at a moderate speed and moderate cost.

Sample and Hold

A sample and hold circuit is used in an analog-to-digital converter whenever it is desirable to make a measurement on a signal and to know precisely when the input signal corresponded to the results of the measurement. It is also used to increase the duration of a signal.

The sample and hold circuit can be represented as shown in Figure 7. When the switch is closed, the capacitor is charged to the value of the input signal; then it follows the input. When the switch is opened, the capacitor holds the same voltage that it had at the instant the switch was opened.

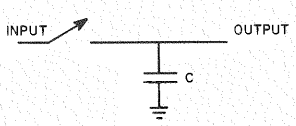


Figure 7 Sample and Hold

It is possible to build a sample and hold circuit just as shown here. Often, the same circuit is used with a high gain amplifier to increase the driving current available into the capacitor

or to isolate the capacitor from an external load on the output. In some cases, this sample and hold is made entirely differently; but from a logical point of view, it acts as the ideal component shown.

The acquisition time of a sample and hold is the time required for the capacitor to charge up to the value of the input signal after the switch is first shorted. The aperture time (see definition, Chapter 2) is the time required for the switch to change state and the uncertainty in the time that this change of state occurs. The holding time is the length of time the circuit can hold a charge without dropping more than a specified percentage of its initial value.

Multiplexing

Often it is desirable to multiplex a number of analog channels into a single digital channel or conversely a single digital channel into a number of analog channels. Multiplexing can take place in the digital realm, the analog realm, or in the conversion process.

DIGITAL-TO-ANALOG

In digital-to-analog conversion, a common problem is to take digital information which is arriving sequentially from one device, such as a digital computer, and to distribute this information to a number of analog devices. Usually it is necessary to hold the information on the analog channel even when it is not being addressed from the digital device. There are two ways to multiplex. A separate digital-to-analog converter may be used for each channel as shown in Figure 8.

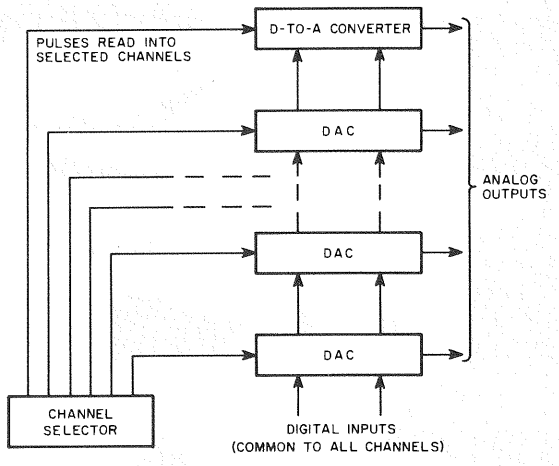


Figure 8 Digital-to-Analog Systems

In this case, the storage device is the digital buffer associated with the converter. Or, a single digital-to-analog converter may be used, together with a set of multiplexing switches and a sample and hold circuit on each analog channel. The cost of the first method is

slightly more than the cost of the second method, but it has the advantage that the information can be held on the analog channel for an indefinite period of time without deteriorating; whereas with the multiple sample and hold technique, it is necessary to renew the signal on the sample and hold at periodic intervals.

ANALOG-TO-DIGITAL

In analog-to-digital conversion, it is more common to multiplex the inputs in the analog realm. Here switches, either relays or solid state, are used to connect the inputs to a common bus. This bus goes into a single analog-to-digital converter which is used for all channels (see Figure 9). If simultaneous time samples from all channels are required, a sample and hold circuit can be used ahead of each multiplexer switch. In this way, all channels would be sampled simultaneously and then switched to the converter sequentially. The multiplex switches and sample and holds will introduce some error into the system. However, it is usually less expensive to go to higher quality sample and hold and multiplex circuits than add extra converters.

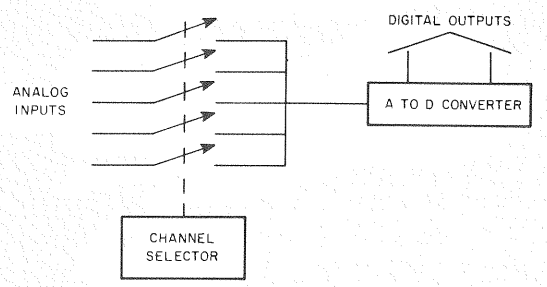


Figure 9 Multiplexed Analog-to-Digital Conversion System

In a simple analog-to-digital converter with a single comparator circuit, it is also possible to multiplex by using a separate comparator for each analog channel. One input of each comparator is tied to the voltage generating device in the converter. The other inputs are tied to the separate analog channels. The comparator to be used can be selected digitally. This method is particularly good when a small number of channels is to be multiplexed since it is quite simple and requires little additional control. For a large number of channels, separate multiplexer switches are usually less expensive and more accurate as they do not put any load on the voltage generating device of the converter.

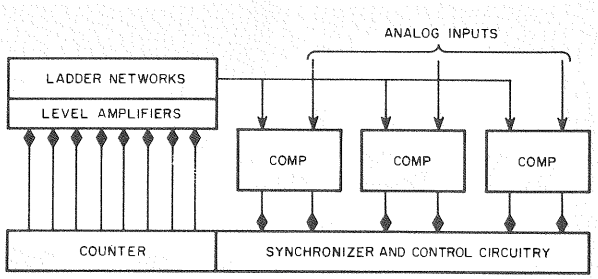


Figure 10 Counter Type Analog-to-Digital Converter with Multiplexed Input

The comparator multiplexing technique is particularly useful with the counter type analog-to-digital converter. This technique is shown in Figure 10. Several comparators are attached to one converter. The counter is cleared; then count pulses are applied. When one of the comparators signals that the digital-to-analog output is greater than the input voltage on that channel, the contents of the counter are read out. Counting is then resumed until the next signal is received.

CHAPTER 2
MEASURES OF CONVERTER PERFORMANCE

Accuracy

Since the end result of conversion is the representation of a given value in different terms, it is important to know how accurate the representation is. In systems where accuracy requirements are not too stringent, say in the order of 1 percent, an overall accuracy specification is usually sufficient. In cases where the desired accuracy is 0.1 percent or greater, it is necessary to isolate the various sources of error; and since a converter is a hybrid device, both digital and analog sources must be taken into account.

In high accuracy systems particularly, accuracy figures given in the general specifications may not include isolated sources of error, e.g., noise. Thus, it is important to know the various types of errors, their causes, how they are measured and specified, and when they are important. Figure 11 shows a breakdown of various types of errors.

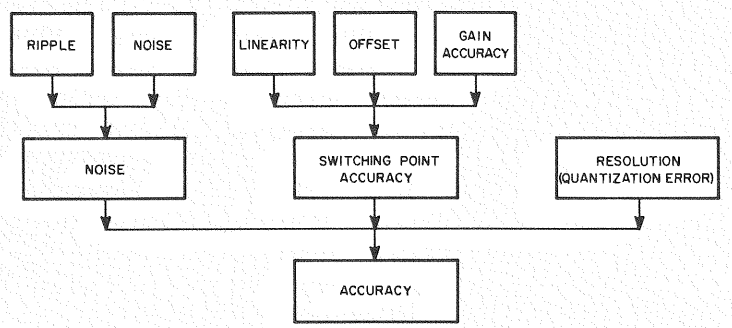


Figure 11 Measures of Cumulative Error

DIGITAL ERROR SOURCES

When a continuous signal is quantized, there is an error which is equal in magnitude to the smallest quantum. For a linear converter, the smallest quantum is the least significant bit. In most converters the quantization error is centered so that it is equal to $\pm$½ the least significant bit, written as $\pm$½ LSB.

In a continuous converter or digital voltmeter, accuracy may not be as important as avoiding chatter. That is, if the input is right on the dividing line between two quantization states, the output should not oscillate. If hysteresis is introduced so that the quantization error is just under $\pm$1 LSB, then oscillations will normally be avoided and the accuracy will not be greatly impaired.

The digital-to-analog converter reproduces exactly all the digital input information which it accepts. Hence digital error is not included in its accuracy specifications. However, if the input has more bits than the converter, there will be a quantization error in the readin process which should be taken into account. If desired, a ½ LSB offset can be built into the converter so that the readin will round off, rather than truncate, more precise digital information.

ANALOG ERROR SOURCES

The dc accuracy of the converter (or switching point accuracy) depends on the offset, the gain calibration, and the linearity. Nonlinearities are due to the variation in gain (or common mode effect) in going from the smallest input to the largest input. Some of these will be long-term, because of the common mode effect of the comparator circuit in the analog-to-digital converter, for example. Some will be shorter term, because of discontinuities in the divider network or insufficient settling time of the comparator. The offset and the gain can be adjusted in the calibration until their effects are essentially negligible.

The measurement of analog error in a digital-to-analog converter is easily made by putting in a digital number (the same word length as the converter) and observing the output. In an analog-to-digital converter, the analog error is difficult to locate since the quantization error is always present. However, the point where the output oscillates approximately equally between two neighboring digital numbers is fairly well-defined. This point, called the switching point, can be measured and compared with the theoretical value.

The ripple on the reference supply and other sources of noise are often measured separately since one or the other can sometimes be neglected in the final result. The two can be separated by measuring the ripple in the reference supply and subtracting it from the measured noise, or by running the input source in the converter from the same reference, thereby giving a direct measurement of all noise sources except the reference supply ripple. In a digital-to-analog converter the noise and ripple can be measured by observing the output with a scope. In an analog converter they can be measured by observing the input range which causes the output to oscillate between two states.

DIFFERENTIAL LINEARITY

Differential linearity is the variation in the size of the required voltage change that causes an analog-to-digital converter to go from one switching point to another. That is, it is the variation in the size of the states and is generally quoted as a percent of the size of the states. It is a part of the overall linearity discussed above, but deserves special mention because of its importance when an analog-to-digital converter is being used in histogram applications. For example, when plotting the number of inputs versus the digital state, if one of the states is twice as big as its neighbor, it will tend to accumulate twice as many counts. Naturally, a very misleading output results.

Differential linearity is one of the few accuracy characteristics which is affected by the conversion technique. The differential linearity tends to be best when the converter goes

through all the states sequentially as in the counter type converter described in Chapter 1 or the ramp variation described in Chapter 3. In an approximation converter, such as the successive approximation type, the large transients which result in going from, say, half scale to quarter scale require a long time to settle down, and any hysteresis in the comparator circuit causes relatively large variations in the state size. However, the differential linearity of an approximation converter can be improved by running it at very low speed. Differential linearity is also affected by variations in the divider networks (although they are relatively small). It can be avoided by using a ramp converter.

The shorter the converter word length, of course, the better the differential linearity will tend to be. However, this gain may well be compromised, since small resolution could result in the loss or the smoothing of very sharp peaks in the histogram.

Techniques commonly used to overcome difficulties with differential linearity are: changing the offset on the converter (or equivalently the bias on the input signal) and changing the word length of the converter. Switches can be mounted on the converter for this purpose, or the change can be made programmable so that the controlling device can make the change automatically.

DISTRIBUTION OF ERROR

How much of the total error should be in the digital circuitry and how much in the analog portion? For converters in the range of up to 10 or 11 bits, the digital error generally accounts for about ⅓ to ½ of the total. Thus, a typical 10-bit system would have a quantization error of $\pm$½ LSB and an analog error of $\pm$1%.

If the accuracy requirement is low, the word length may be the major source of error. The total error may then be treated simply as round-off. If the accuracy requirements are stringent, it is desirable to minimize all sources of error, analog and digital. The digital error is quite simple to minimize by extending the number of bits within practical limits. A converter with an overall error of 0.1% and a word length of 20 bits would be unjustified, as for all intents and purposes the least significant bit could have been generated by a random number generator.

Requiring monotonicity is one way to assure that all the bits are meaningful. This means that all states must exist and they must be in the correct order. In terms of converter operation, as the number going into the digital-to-analog converter is increased, the output voltage must also increase; it should never dip back down at any point. Similarly, if the input voltage to an analog-to-digital converter is increased, the digital output should stay at the same value or increase and should not skip over any states.

The converter is most likely to lose monotonicity when switching between digital states such as 0111 and 1000. If the weighting of the bits is not quite correct, in a digital-to-analog converter the higher state might correspond to a lower voltage, and in the analog-to-digital converter the output might jump directly from 0110 to 1000.

Measures of Speed

DIGITAL-TO-ANALOG CONVERSION

The maximum conversion rate is theoretically limited only by the minimum time between readins to the converter flip-flops, and can easily be as high as 10 megacycles. However, such a figure may be misleading. The desired ratio of settling time to non-settling time usually determines the maximum usable conversion rate.

The settling time of a converter is measured from the time the digital readin is performed to the time when the analog output has settled to within the specified limits of accuracy. How the output approaches its final value depends on the output circuit, as discussed below.

The divider output will have high frequency transients before it begins to settle. If the output is going to a low frequency device, the transients can be ignored. In some applications, it is more desirable to smooth the transition between states than to minimize the total time, in which case the oscillations can be damped with the capacitor or a low pass filter.

If the output is from an amplifier circuit, the settling time will be determined by the maximum rate of change of the amplifier. Thus, the first readin may take longer to settle than subsequent readins, which usually do not change the converter by such a percentage of the full scale.

ANALOG-TO-DIGITAL CONVERSION

Conversion time is measured from when a request is given to when a digital output is available. In converters like the successive approximation type, where all conversions are completely independent, time must be allowed for completion of entire steps in the conversion process. In the continuous converter, the conversion time is usually just that time required to synchronize the request and get the number.

The conversion rate is usually the inverse of the conversion time. In some systems, an amplifier or comparator recovery time is required between conversions; thus the rate is lower. However, comparators manufactured by Digital Equipment Corporation do not have a recovery time. The conversion rate will also be slower if logical operations must be carried out between conversions. In some cases, such as the counter converter performing a number of simultaneous conversions or the synchronous sequential converter, the conversion rate is actually faster than the inverse of the conversion time.

If the input signal is changing with respect to time, it is very important to know when the signal had the value given by the output. The uncertainty in this time measure is called the aperture time (sometimes also called window or sample time). The size of the aperture and the time when the aperture occurs vary depending on the conversion method.

Figures 12 through 15 illustrate how the aperture varies with different conversion techniques. In each case, the upper portion of the figure shows how the converter arrives at an output. The lower portion of each figure shows how the input might be reconstructed from the Digital data.

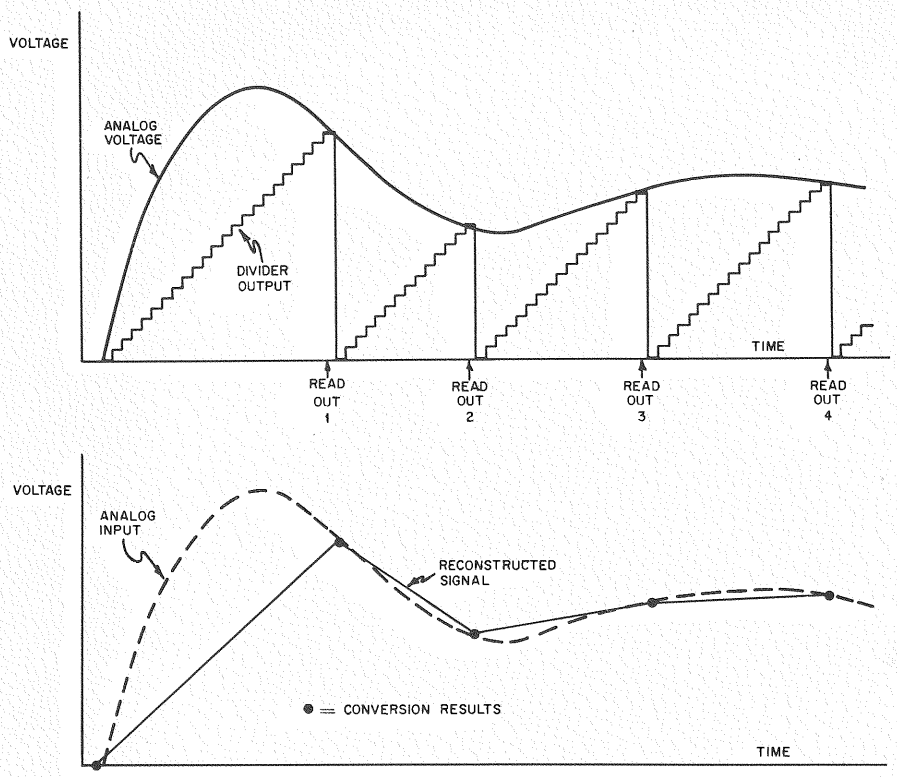


Figure 12 Counter Converter

In the counter converter (Figure 12) the aperture occurs at the end of the conversion. This is not constant with respect to the beginning of the conversion, but it may be calculated from the digital output.

For the continuous converter (Figure 13) the aperture is the time for the last step. Here the assumption is made that the input signal does not change more than ± 1 LSB between conversion steps. To meet this requirement, the maximum rate of change of the input voltage must not exceed the maximum rate of change of the converter. This is $V_{ref}/2^N\Delta T$ where V reference is the full scale voltage, N is the number of bits, and ΔT is the time per step. The maximum rate of change of the sine wave is $2\pi V_p f$, or $\pi V_{pp} f$. Thus, if the converter is to follow the input, the maximum frequency components in the input must satisfy the following equation:

$$\pi V_{pp} f = V_{ref}/2^N\Delta T$$

and if the peak-to-peak voltage is assumed equal to the converter reference, then the maximum frequency is:

$$f = \frac{1}{2^N\Delta T\pi}$$

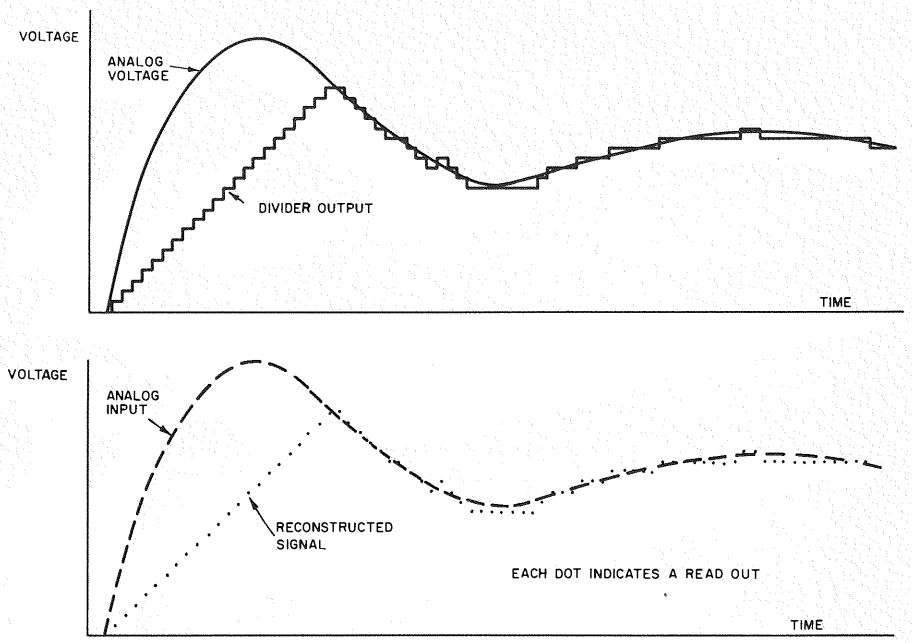


Figure 13 Continuous Converter

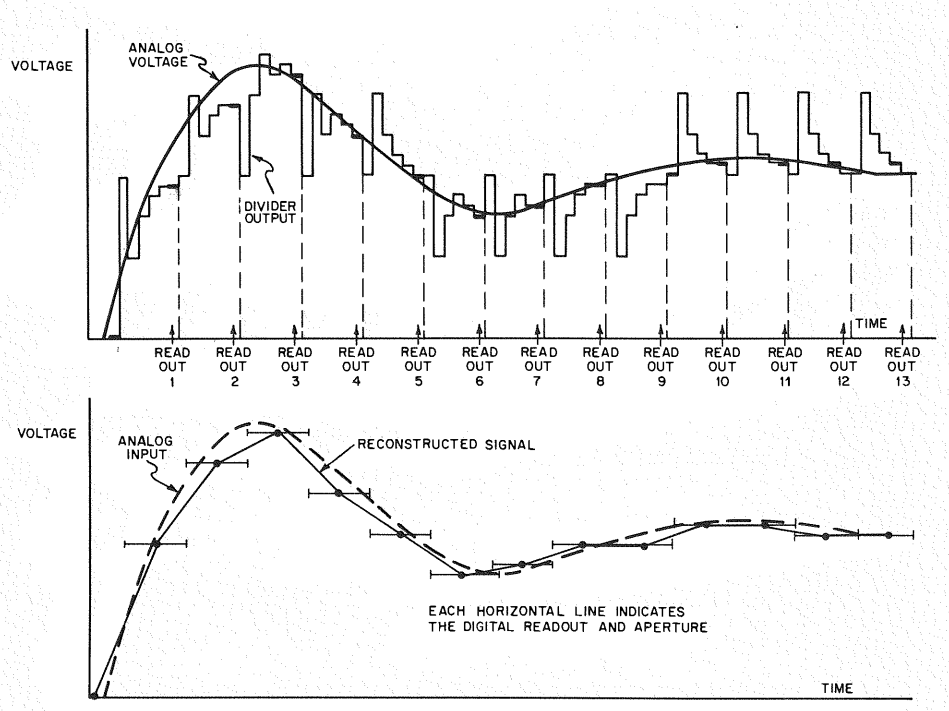


Figure 14 Successive Approximation Converter

For a successive approximation converter (Figure 14) the digital output corresponds to some value the analog input had during the conversion. Thus, the aperture is equal to the total conversion time. Aperture time of the successive approximation converter can be reduced by using the redundancy techniques outlined in Chapter 3 or by using a sample and hold circuit. The sample and hold is illustrated in Figure 15.

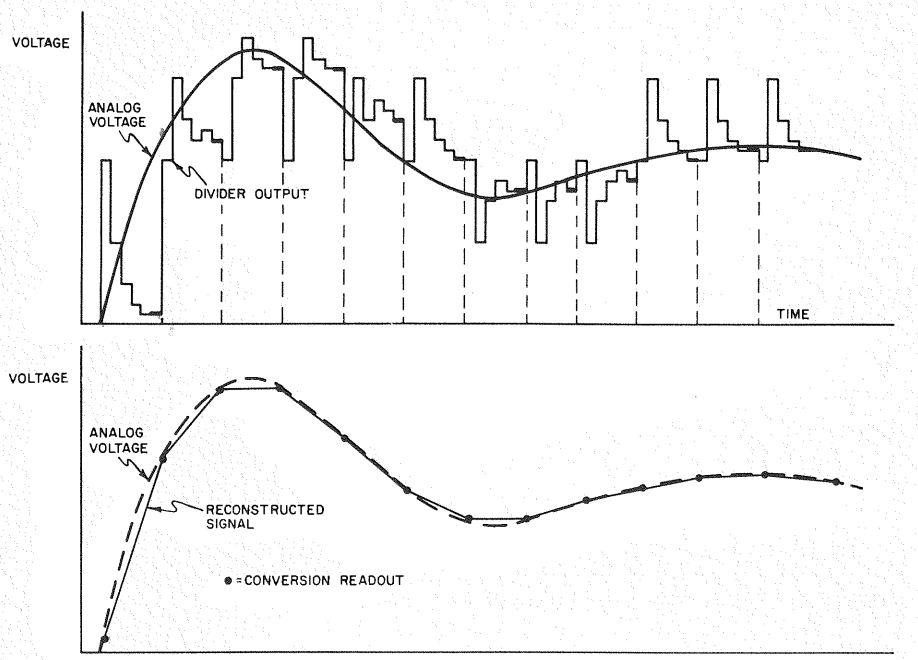


Figure 15 Successive Approximation Converter with Sample and Hold

SELECTING A CONVERSION METHOD

Chapters 1 and 2 have summarized several methods of conversion and the performance characteristics that may be expected from them. These criteria for choosing a specific conversion method are condensed in Table 1. The table is organized like the handbook with applicable chapters called out for quick reference to detailed descriptions of the methods.

The decision to choose one converter over another is principally a matter of speed, aperture, cost, and whether multiplexing or a single continuous input is to be used. Exact conversion times, aperture times, and cost depend on the number of bits, type of circuitry,

TABLE 1 ANALOG TO DIGITAL CONVERSION TECHNIQUES

Method	Best for Multiplexed or Continuous Input?	Conversion Time* 5 Bits (μsec)	Conversion Time* 10 Bits (μsec)	Aperture Time* 5 Bits (μsec)	Aperture Time* 10 Bits (μsec)	Constant Time of Aperture?	Relative Cost	Remarks
BASIC METHODS (Chap. 1 & 4)								
Simultaneous	Both	Not Applicable				Yes	Depends on resolution	Excellent for low resolution systems — operates in about 100 nanoseconds
Counter	M	24 av.	1792 av.	1.5	3.5	No	Low	Allows many conversions simultaneously
Continuous								Extremely high speed for continuous input but falls behind on sharp rate of change
Continuous Input	C	1.5	2	1.5	2	Yes	Low to Medium	
Discontinuous Input	C	24 av.	1024 av.			Yes		
Successive Approximation	M	7.5	36	7.5	36	Yes	Medium	General purpose — good speed/dollar
VARIATIONS ON BASIC METHODS (Chap. 3)								
Ramp	M	16 av.	512 av.	1	1	No	Depends on resolution	Good differential linearity — low cost for low resolution systems
Section Counter	M	18	112-224	1.5	3.5	No	Low to medium	Used with digital voltmeter
Continuous with add. comp.								
Continuous Input	C	1.5	2	1.5	2	Yes	Medium to High	Similar to continuous but has faster responses to discontinuous or high speed signals
Discontinuous Input	C	6-12 av.	32-512 av.	1.5	2	Yes		
Successive Approximation with Redundancy	M	9	27	1.5	3	Yes	Medium to High	Good speed per dollar in high resolution systems. Small aperture, good differential linearity
ADVANCED (Chap. 3)								
Subranging	M	3-4	10-20	3-4	10-20	Yes	High	Excellent for 5 to 8 bits
Subranging with Redundancy	M	2.5	6-9	1.5	3	Yes	High	Excellent for 7 bits or more
Seq. Approx. (Non-Synchronous)	M	7.5	25			Yes	High	May make errors. Requires sample and hold
Seq. Approx. (Synchronous)	C	1.5/9†		1.5		Yes	High	†Time between conversions/total time
Quantizing								Excellent for both multiplexed and continuous inputs. Automatically follows fast input with low resolution and slow input with high resolution
Continuous Input	Both	2	3	2	3	Yes	High	
Discontinuous Input	Both	6	18	2	3	Yes	High	

*See text

and variations in system design. The speeds given in the table were derived assuming that the system was designed for maximum speed per dollar. Actual speeds will usually be within a factor of 2 for basic conversion methods and within a factor of 5 for the others.

The basic conversion methods, as described in Chapters 1 and 4, will satisfy most requirements. If Table 1 confirms the choice of one of the basic methods, the reader can go directly to Chapter 4 for specific information on the equipment required. The other methods are variations of basic methods and advanced techniques primarily for increased speed. They are described in general terms in Chapter 3.

CHAPTER 3

SPECIAL ANALOG-TO-DIGITAL CONVERSION TECHNIQUES

The analog-to-digital conversion techniques described in Chapter 1 are the most commonly used methods but not necessarily the only ones. There is an extremely large variety of techniques, not all of which have been investigated. Some of the other methods are described in the following section.

Variations In Basic Techniques

SECTION COUNTER

The counter converter is a simple technique for performing conversions. However, if the digital word becomes long, the 2^N steps required to complete the conversion may be too many.

One way to decrease the time at a minimum of cost is to divide the counter into sections. For example, a 10-bit converter could be divided into 2 sections of 5 bits each. At the beginning of the conversion the least significant counter is set to all ones and counts are inserted into the most significant counter until the comparator idicates that the input has been exceeded. The least significant counter is cleared and counted up until the correct value is reached. The maximum number of steps required to complete a conversion is 2^5 for the most significant counter and 2^5 for the least significant counter, giving a total of 2^6 steps. This is a maximum of 64 counts versus 1024 counts for the standard counter converter.

Other types of section counters might use more parts and operate by counting one counter up and the next down. The total conversion time, of course, depends on the number of sections.
The section counter technique is frequently used in digital voltmeters where the output is to be in decimal: Each section of the section counter thus represents one decimal digit.

RAMP METHOD

In the counter converter, each count input is increasing the voltage out of the DAC by one step, effectively generating a ramp out of the DAC. Thus the level amplifiers, reference supply, and divider network could be replaced by an external ramp generator circuit. If accuracy is not too important, the ramp can be made by charging a capacitor with a current source and using the linear part of the exponential. In higher resolution converters, the ramp might be made by using the operational amplifier as an integrator.

The ramp technique is somewhat faster than the counter technique because carry and DAC set up time is not required before gating the next count pulse. The differential linear-

ity, over a short span of a ramp converter, is bound to be fairly good, since the ramp is a continuous signal. Although there may be some noise, the general slope will not change significantly over a short span.

Both the ramp method and the counter technique approach the final value in small steps and from one direction only. This puts considerably less strain on the comparator circuit than a technique such as subranging or successive approximation where the comparator is receiving large input voltage changes in different directions and being asked to resolve small differences. In general, all smooth conversion techniques (the counter, ramp, and continuous converters) generally operate at a considerably faster time-per-step and produce better differential linearity than the approximation methods (subranging, successive approximation, sequential approximation, etc.).

CONTINUOUS CONVERTERS WITH ADDITIONAL COMPARATORS

A continuous converter is an extremely fast and relatively inexpensive device for following a continuous signal. However sometimes the input rate of change exceeds that of the converter. To close this gap determine if the differential error exceeds a specified amount and add or subtract a correction count in a more significant bit. For example, a small amount of logic added to a 10-bit continuous converter could measure large differences between the input and the contents of the converter. If the difference is more than +8 counts, it adds a count in the third flip-flop from the least significant end. If the

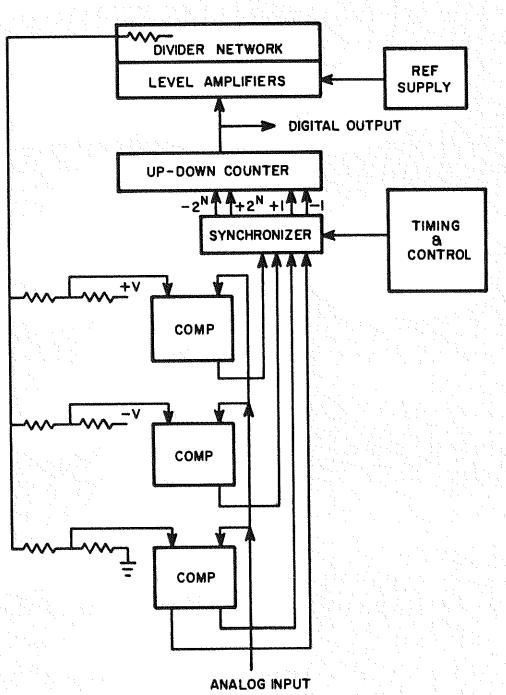


Figure 16 High Speed Continuous Converter

difference is more negative than —8 counts, it subtracts a count from this stage. Thus the converter operates on high frequency signals with reduced accuracy and on low frequency signals with the full accuracy.

A continuous converter with additional comparators is shown in Figure 16. Two comparators and additional gating and synchronizing logic have been added to a basic continuous converter.

SUCCESSIVE APPROXIMATION CONVERTER WITH REDUNDANCY

Redundancy is useful where high resolution and high speed are both required. It can also be used to improve differential linearity and aperture.

The successive approximation converter is extremely efficient; but, since the results of each step are irrevocable, each step must be allowed to settle to within the total system accuracy. For high resolution systems, the settling time can be quite long. With redundancy, the first steps are done with a limited accuracy; then a correction step is inserted to improve the accuracy. Only the correction step and the following steps need to settle to final accuracy. Steps before correction need only settle within $\pm\frac{1}{2}$ of the correction amount.

The correction can be implemented by adding or subtracting one bit, as in a continuous converter. If the steps preceding the correction are offset, only add circuitry is necessary. For fastest operation, a special divider with redundant inputs can be used so that the addition can be done without generating carries. The digital summing can be done in an output buffer where the carries will not interfere with the analog-to-digital feedback loop.

The correction step can also be used to compensate for changes in the input analog signal during earlier steps, thereby reducing the aperture. It also improves the differential linearity of the converter since a large part of the variation in state size is due to the large transients during the early conversion steps.

Advanced Techniques

SUBRANGING

This method is very good for converting a large number of input channels since the conversion begins without assuming anything regarding the previous state of the input. It also converts quite rapidly and allows a trade-off between cost and complexity and speed. Thus, if extremely high speed is required, numerous comparators are used and not many steps are required. In the case where less speed is required, perhaps only one comparator circuit would be used.

The subranging method operates by dividing the total input signal range by the number of subranges, selecting the appropriate subrange and then dividing this into subranges as before, repeating until the desired resolution is achieved.

Figure 17 shows how subranging works. At the start of the conversion, the only information available about the input signal is that it lies somewhere in the range of zero to the full scale voltage, V_{FS}. The first step of the conversion divides the full scale voltage into

subranges, in this case four. Simultaneously, comparisons are made between the input voltage and the three subrange boundaries, V_1, V_2, and V_3. It can be determined whether the input voltage is higher than or lower than each of these boundaries. If the input signal is lower than all of the boundaries, it must fall in the lowest range. If it is higher than V_1 but lower than V_2 and V_3, it must fall in the next to the lowest range, and so forth. Once this information is determined, the selected subrange can be divided into four more subranges and the process repeated.

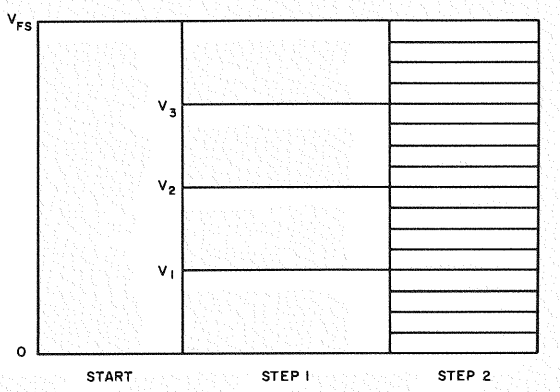


Figure 17 Subranges for a Converter with Four Subranges Per Step

If there are M ranges per step and S steps, the total resolution of this conversion will be $(\frac{1}{M})^S$. For example, a 12-bit system requiring a total resolution of $\frac{1}{4096}$ could be implemented in 12 steps [$(\frac{1}{2})^{12} = \frac{1}{4096}$], in six steps [$(\frac{1}{4})^6 = \frac{1}{4096}$], in four steps [$(\frac{1}{8})^4 = \frac{1}{4096}$], or in three steps [$(\frac{1}{16})^3 = \frac{1}{4096}$]. The step resolution does not have to be an integer power of two. However, except in a binary coded decimal system where it is useful to make M equal to 10, the saving in control circuitry is usually sufficient to justify increasing the step resolution to the next power of 2.

Figure 18 shows a subranging converter. Here two digital-to-analog converters and a number of comparators are referenced at equally spaced intervals in the range between the value of the two converters. The technique is similar to the simultaneous method. The system starts with the lower DAC (digital-to-analog converter) at zero, the upper one at the maximum voltage. The output of the comparators indicates which range contains the input, say between the reference applied at C_K and the reference applied at C_{K+1}. Then the reference voltage from C_K is applied to the lower DAC, and the reference voltage that was at C_{K+1} is applied to the upper DAC. A new, smaller set of ranges is produced. The process is then repeated.

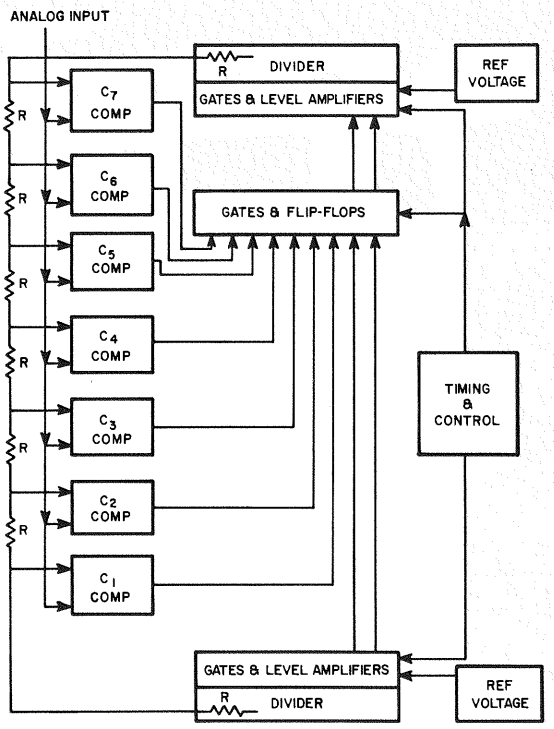


Figure 18 Subranging Converter

If the number of subranges obtained in a single step is equal to the total system resolution, this method becomes the simultaneous method described in the introduction. If the number of subranges per step is reduced to two, this method becomes the successive approximation conversion.

SUBRANGING WITH REDUNDANCY

Redundancy, as described for the successive approximation converter, can be applied in the same manner to a subranging converter. It is particularly useful here as the capacitance of many comparators in parallel causes the settling time to be quite long.

SEQUENTIAL APPROXIMATION

Sequential approximation, also called parallel approximation, uses a separate analog-to-digital converter for each binary bit of information to be obtained. There are two methods of operation, synchronous and non-synchronous.

Figure 19 shows how the non-synchronous type operates. In one example shown at the top of the figure, the analog input comes into a comparator which compares the input with half scale. If the input is larger, the comparator applies a voltage to the most significant bit of each of the DAC circuits down the line. As soon as the first comparator has

settled, the second comparator can start to make its decision. Speed is gained because there is no flip-flop delay in this system. But more important, most comparators will make decisions relatively quickly, since the analog input cannot be very close to the boundaries of more than two subranges (the last one and one other). Thus, the average amount of time required per decision is considerably less than the maximum. In a clocked system, the maximum required time must be allowed for each step. Here, only the average time is allowed.

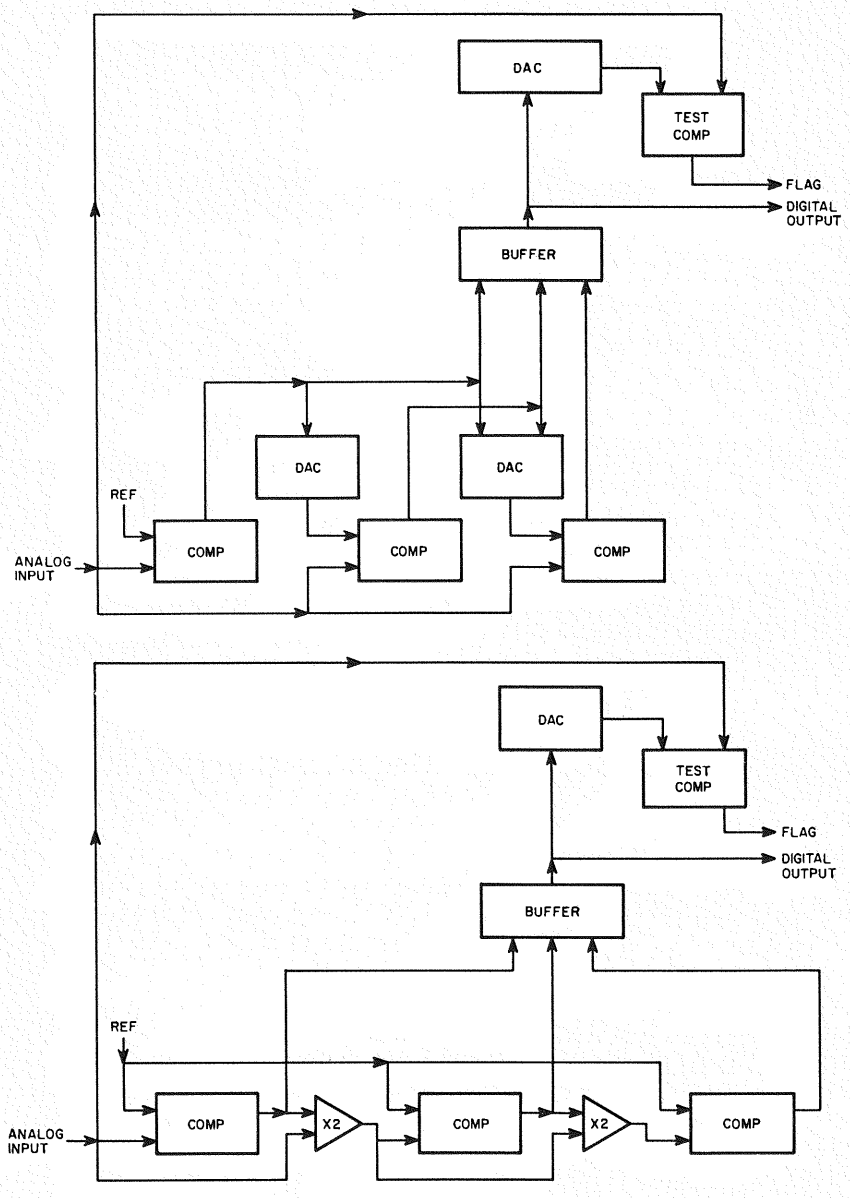


Figure 19 Non-synchronous Sequential Approximation

The converter shown at the lower half of Figure 19 is quite similar except that the individual DAC networks are replaced by operational amplifiers. The analog input goes to the first comparator. If the input is above half-scale, the comparator produces a voltage corresponding to half scale. This is subtracted from the input signal, and the result is multiplied by two and passed on to the next comparator.

In both examples, speed is gained by the fact that full settling time is not needed by those comparators which are not making a critical decision. On the other hand, some difficulties are encountered if the input signal should change slightly before the digital readout has occurred. One of the comparators may change value, but the results may not carry to the end of the chain before readout. Thus, the comparator should have built-in hysteresis so that small noise spikes will not cause an error, and the digital output should always be read into a buffer and double checked with the input.

In synchronous sequential approximation, the time required to perform a complete conversion is essentially the same as in a successive approximation converter; however, the conversion rate is much faster. Erroneous readout is eliminated, since the converter is buffered and synchronous. This type of converter is particularly useful for systems with a single input.

The synchronous or clocked type sequential approximation converter also uses one converter per bit. It differs from the non-synchronous type because there is a delay line between each converter (see Figure 20). The analog information arrives at the first comparator, which makes a decision and stores the information in a shift register for use by later converters. By the time the second converter is set up and ready to make a decision, the same analog information is just arriving at the second comparator. This converter decides on the second bit of the output word, based on exactly the same analog voltage as was at the first converter when the first bit decision was made. This process is continued for however many bits are necessary.

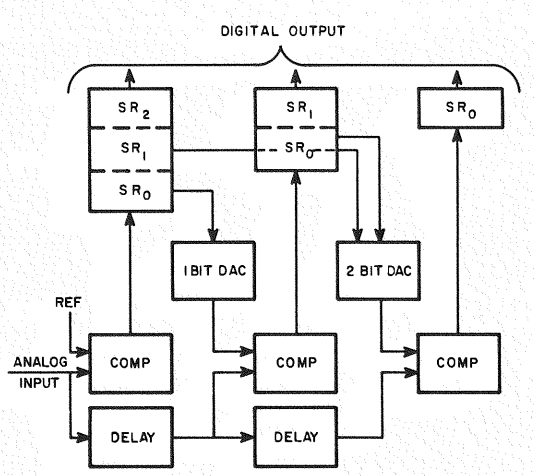


Figure 20 Sequential Approximation (Synchronous)

QUANTIZING ENCODER

The quantizing encoder was developed by Dr. Jerome Cox and Donald Glaser at the Central Institute for the Deaf. It is the most general purpose, high speed converter because it is fast for both continuous and multiplexed inputs.

The quantizing encoder uses one digital-to-analog converter, a number of amplifiers, and a number of comparators. It examines the difference between the input voltage and the DAC output, quantizes the difference to the nearest power of 2, and adds or subtracts this from the DAC. Thus, the quantizing encoder can follow a continuous signal, staying within one bit of the correct value for low frequencies. For high frequencies, it will always be within the nearest possible power of 2 of the correct answer. (Thus, if the input signal should suddenly change, the quantizing encoder will make a similar jump corresponding to the nearest power of 2 change, while the standard continuous converter could increase by only one count.)

For multiplexed input, the quantizing encoder will operate similar to a successive approximation converter but twice as fast. It requires only one step for each two binary bits (or fraction thereof). In addition, since it includes a self-correcting ability, the time per step can be quite fast.

Figure 21 shows how the quantizing encoder could arrive at the result when used as a 4-bit encoder. In the left-hand example, it is used with a multiplex input. At the start

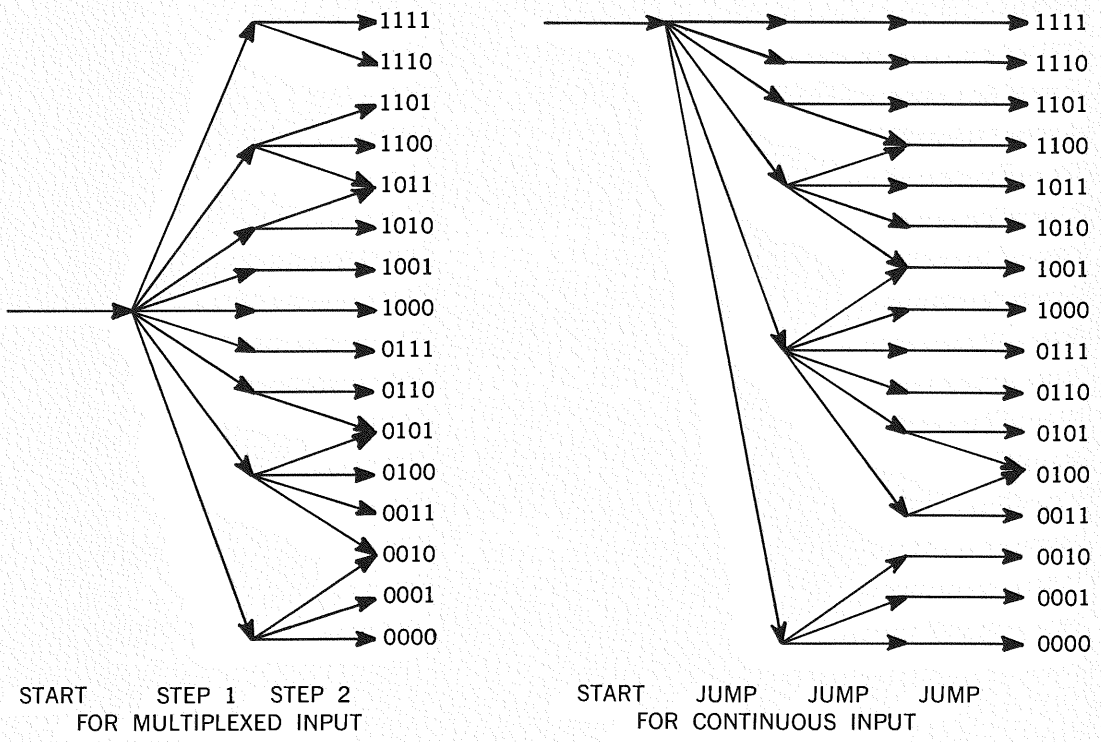


Figure 21 Quantizing Encoder Method

of the conversion the converter is set to mid-scale. At the end of the first step it will go to any of the points shown, and at the end of the second step it always has arrived at the correct answer.

The right-hand example, Figure 21, shows how the converter would react if it were holding its maximum value and the input suddenly dropped to a much lower value. If the new value were within 1 or 2 counts, it would immediately arrive at the exact answer. Otherwise, it would make a power of 2 jump to the nearest correct value.

CHAPTER 4

TYPICAL CONVERTER LOGIC

Digital-to-Analog Conversion

Figure 22 shows a typical digital-to-analog converter. The basic components of this circuit are a flip-flop register, level amplifiers, a divider network, and a reference supply. The digital signals are brought in with a pair of complementary levels for each bit. This information is jammed simultaneously into all the flip-flops and is automatically converted to the appropriate analog voltage by the divider network.

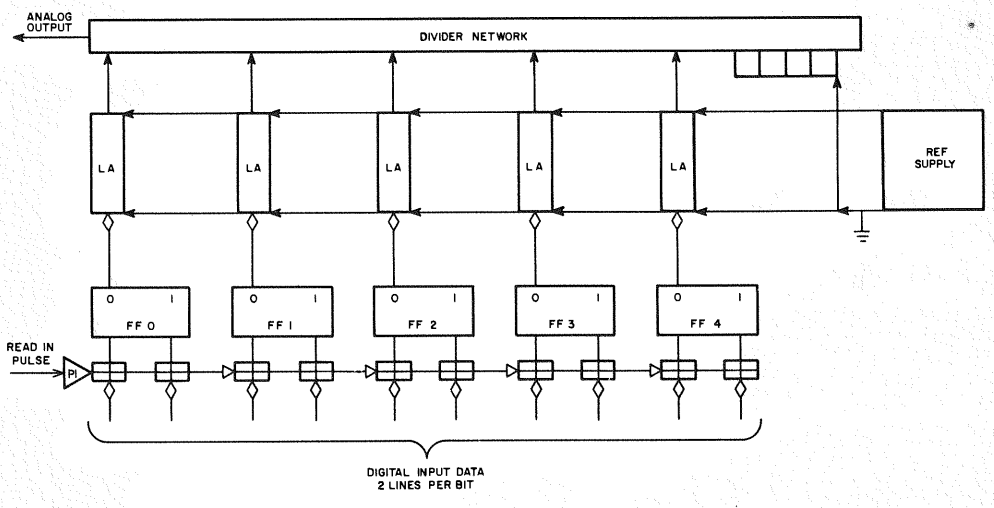


Figure 22 Digital-to-Analog Converter

The settling time of the digital-to-analog converter depends on the number of flip-flops that change, as well as the voltage difference between the two states involved. For example, in switching from a number such as 0111 to a number such as 1000, all of the flip-flops change state. Even though the two final values of the analog voltage are very close, transients occur on the divider output for the following reasons: variation in transition times from flip-flop to flip-flop and from level amplifier to level amplifier; transient current drawn from the reference supply; the fact that the flip-flops have a slower fall than rise time; and the fact that signals must propagate through the divider network. The worst case is switching from mid-scale (1000 . . .) to one count less (0111 . . .). Here the transients are as much as 1 volt, and even more with the Inverter Amplifiers Type 1667 and 4677. However, the transients are quite short in duration and return to within ½ LSB of their final value within at most 2.5 microseconds for the medium speed combinations listed in the table. In most cases, these transients will be faster than the load can respond and hence can be ignored. For minimum transients, the Type 4679 Level Amplifiers and the metal film ladders are recommended. These units will settle to within 0.05 per cent within 2.5 microseconds.

Table 2 lists the modules which are recommended for systems of different word length. Since a digital-to-analog converter is by nature a relatively fast device, the recommended modules were selected principally on the basis of economy and accuracy consistent with the word length. The maximum conversion rate is 1 megacycle.

TABLE 2

RECOMMENDED MODULES FOR MEDIUM SPEED D TO A CONVERTER

No. of Bits	Flip-Flops	Level Amp.	Divider	Ref Supply
up to 4	4218	4667* or 1667	1563	1562**
5	4219	4667* or 1667	1563	1562**
6	4218	4679	1563	1562
8	4218	4679	1563	1562
10	4219	4678	1574	1704
12	4218	4679	1574	1704

*longer operating time for high voltage levels
**or external reference of −3 to −10 volts

If high speed transients are a problem, the Type 6227 Flip-Flop should be used to drive the divider. A small choke can be used between the flip-flop output and the level amplifier input on the more significant bits to equalize the switching times. This will reduce the transients to about a 0.5 microsecond duration on high accuracy systems. If further smoothing is desired, a low pass voltage should be used on the output.

Analog-to-Digital Conversion

SIMULTANEOUS CONVERSION

The simultaneous conversion technique is simple, inexpensive, and extremely fast for a small resolution system. Figure 23 illustrates a simultaneous converter with a resolution of 3 bits. It uses Level Standardizers Type 1501 as comparator circuits for the input. These units have a resolution of 0.1 volts and are therefore suitable for a simultaneous converter of up to 4 bits. The reference voltages for the level standardizers are made by dividing a +10 volt reference with a series of identical resistors. Although the tolerance on these resistors is not wide, in systems of 3 or 4 bits small trimming potentiometers should be put in series with the resistors so that the reference voltages can be adjusted to offset the common mode effects and the zero offset of the level standardizers. Since the level standardizers also draw a current through the resistors, the potentiometers can trim the value of the resistors to compensate for this current.

The outputs of the level standardizers are coded in a Gray code and jammed into a simple flip-flop register, made by cross-coupling inverters and diode gates. A Gray-to-binary decoder on the output produces standard binary notation.

For higher speed operation, the gates used should be Type 6115, 6113, and 6112. The clear and readin pulses can then be DEC Standard 70 nanosecond Pulses and can occur 100 microseconds apart (thus performing a conversion every 200 nanoseconds).

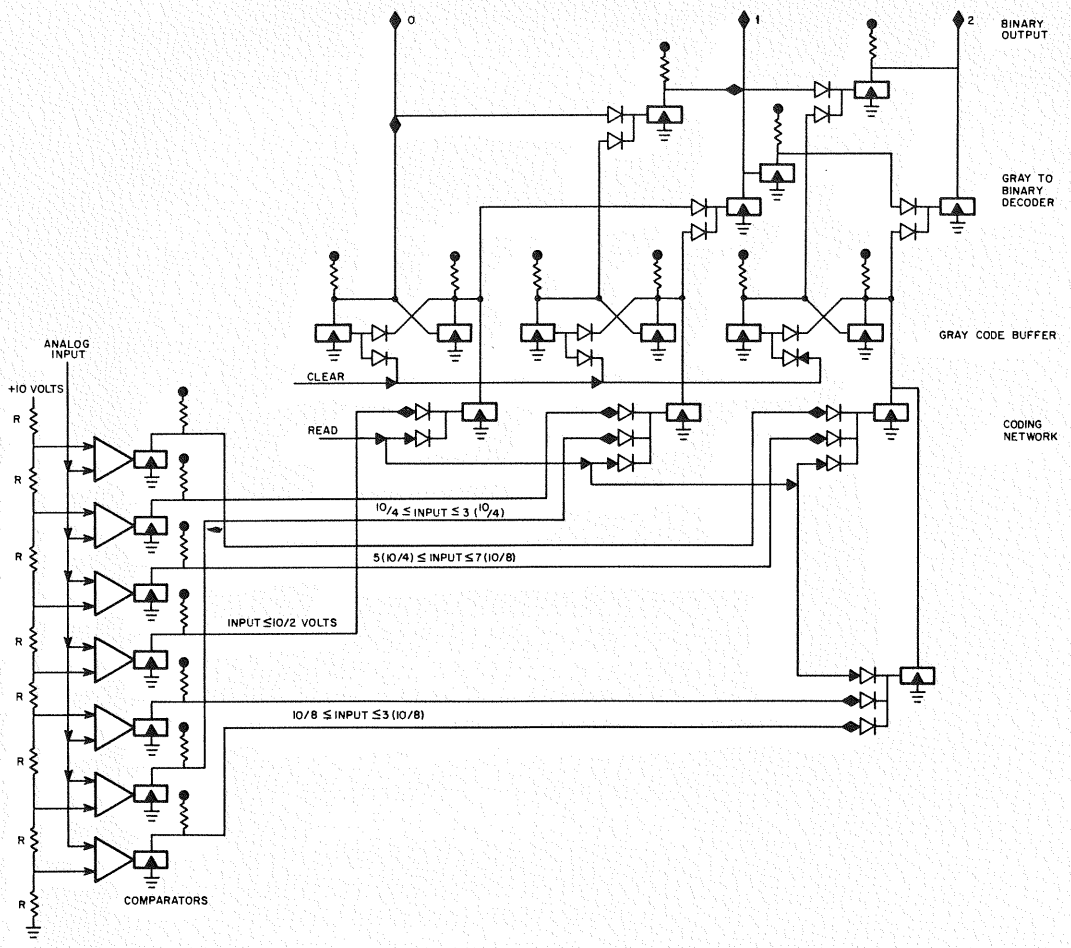


Figure 23 Simultaneous Converter

For lower speed systems, Type 4115, 4113, and 4112 gates can be used with DEC Standard 400 nanosecond Pulses. With these gates, pulses can occur 1 microsecond apart, thus giving a conversion every 2 microseconds.

For maximum speed operation the buffer register can be made with Type 6202 or 6208 Flip-Flops. The standardizer information can be jammed into the buffer with DEC Standard 40 nanosecond Pulses. In this case, conversion could be completed every 100 nanoseconds.

There are two factors which limit extending this system to large resolution systems. One factor is cost of so many comparators. The other factor is the current drawn and the input capacitance, which become extremely large if too many comparators are tied in parallel. For this reason it is recommended that the Type 1501 be used for systems of up to four bits only. Detailed information on the Type 1501 is included in the Module Catalog published by Digital Equipment Corporation.

TABLE 3 RECOMMENDED MODULES FOR SIMULTANEOUS CONVERTER UP TO 4 BITS

Maximum Conversion Frequency (Less Readout Time)	Delay Through System (nsec)	Pulse Inputs (nsec)	Comparator	Flip-Flops	Gates
10 mc	delayed FF, read & pulse simultaneous	40	1501	6202 or 6208	6106
5mc	250	70	1501	6112, 6113, 6115	
500kc	620	400	1501	4112, 4113, 4115	

COUNTER METHOD

Figure 24 illustrates a typical circuit for the counter type analog-to-digital converter. The start signal clears the counter and inserts a single pulse in the delay chain. Each time the pulse goes around the chain, one count is added to the flip-flop register. When the divider output is equal to the analog input, the comparator will switch. The next pulse sets the control flip-flop, indicating the end of conversion and inhibiting the pulse from circulating. The circuit shown in Figure 24 uses Type 4215 or 4225 unbuffered flip-flops for the counter. The control flip-flop may be any unbuffered flip-flop such as the Type 4214 or 4215. At the end of conversion, this flip-flop will be set by grounding the ZERO output terminal.

The Pulse Amplifiers Type 4604 perform pulse standardization as well as amplification. The clear pulse should be 1 microsecond in duration.

The type of delay unit depends upon the number of bits in the counter, since this determines the maximum time required between counts. If either Type 1304 or 4301 Delays are used, at least two units must be in the loop to provide the required recovery time. The Type 4303 and the delay lines do not have a recovery time requirement.

The two inputs to the 1310 Delay line pass through two diodes acting as an OR circuit. One diode is in the 1310 connected to pin X. An external high speed diode (such as the Type 1N994) should be connected to pin W.

A complete conversion requires 2^N steps, where N is the number of bits in a counter. The average number of steps is 2^{N-1}. Calculations of the time per step must take into account the following:

Carry propagate time of the flip-flops

Total transition time of the flip-flops

Delay of the level amplifiers

Delay through the ladder network

Transition time of the comparator and settling time (0.15 + 0.05N microseconds)

Gating time

Synchronization time (if required)

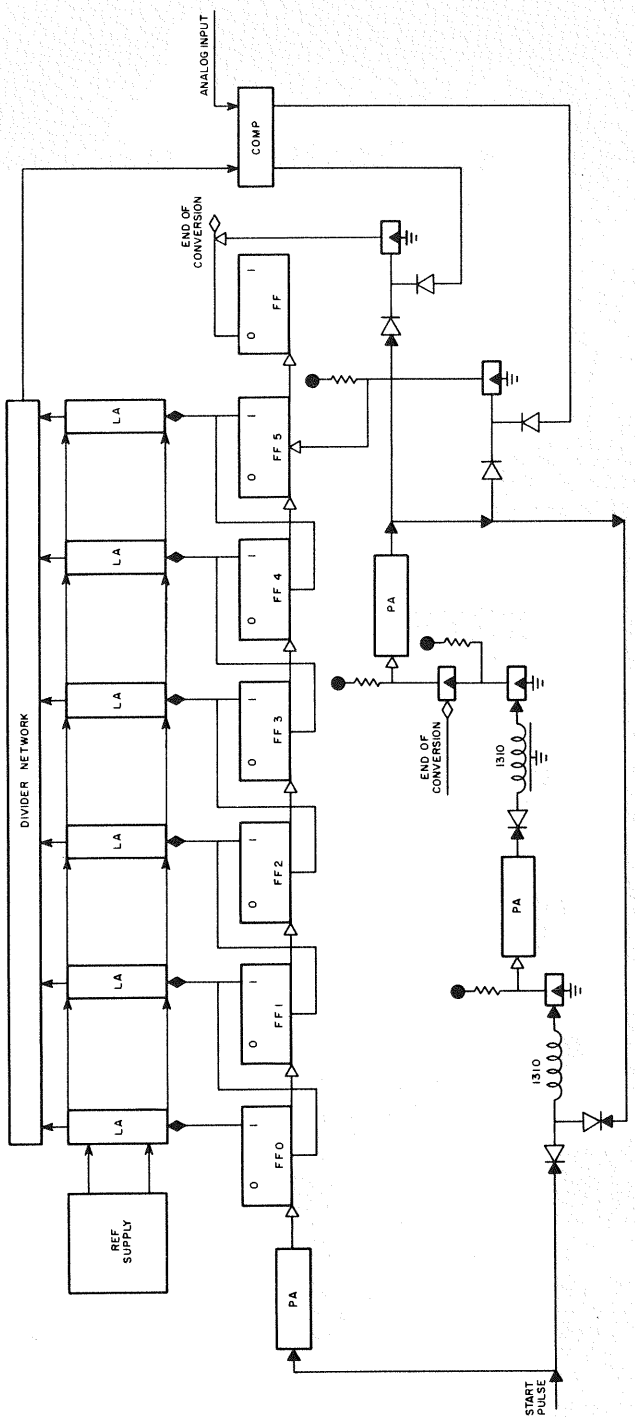


Figure 24 Typical Counter Converter

Typical speeds for the method illustrated are given in Table 4.

TABLE 4 COUNTER CONVERTER CONVERSION TIME

No. of Bits	Level Amplifier	Diode Gates	Divider Network	ΔT Time/Step (μsec)	$2^N \Delta T$ Total Time (μsec)
6	4678	4113	1574	2.2	140.8
6	4679	1113	1574	1.5	96.0
8	4678	4113	1574	2.4	614.4
8	4679	1113	1574	1.7	505.2
10	4678	4113	1564	3.3	3379.2
10	4679	1113	1574	1.9	1945.6

Alternatively, Type 4201 and Type 1201 Flip-Flops can be used in this circuit. However, the Type 4201 will not be as fast as the Type 4215, and the Type 1201 will be only slightly faster.

If buffered flip-flops are used, the control flip-flop should also be buffered and would be set through the input terminal. Also the comparator signal should not gate the counter input directly. Any noise on either the analog input or the ladder output could cause the comparator input to be in a transient state at the time the out pulse occurs. This could result in a split or partial pulse which might not propagate fully. To avoid this possibility the gating inverter on the counter may be either synchronized or eliminated, since the pulse will be inhibited from continuing through the loop.

CONTINUOUS CONVERSION

Continuous analog-to-digital conversion can be performed using an up-down counter. At each step the counter output is compared with the analog input, and a pulse is added to or subtracted from the counter, as necessary. By proper adjustment of the comparator, it is also possible to inhibit counts when the analog signal is approximately equal to the digital number. The inhibit signal is formed by adjusting the comparator outputs so that they do not switch simultaneously. For ideal operation, the two outputs should be in the same state whenever the digital feedback signal is within $\pm$½ part in 2^N of the appropriate input signal.

Synchronization (the use of control flip-flops) is required in all continuous converters. Any noise on the inputs to a comparator could cause the outputs to be in a transient state at the time they were sampled. Thus, if the signals are not synchronized, add and subtract pulses could enter the counter at the same time.

Two continuous converters are illustrated. These systems are identical except that the system shown in Figure 25 uses buffered flip-flops with pulse carry techniques for the up-down counter, while the system in Figure 26 uses the 4000 series unbuffered flip-flops with level change carry propagate.

Both illustrations consist of four basic parts: the up-down counter, the DAC, the comparator, and the synchronizer and control logic. Two control pulses are formed by a clock and

a delay unit. The synchronizer pulse sets the up-sync flip-flop if the enable level from the comparator indicates that the feedback signal is smaller than the input signal. Similarly, the down-sync flip-flop is set if the analog input is larger than the feedback input. Two sets of diode gates are used to inhibit counting which would cause the counter to overflow.

The outputs of the set flip-flops are exclusive ORed together to assure that no count signals will be generated if both flip-flops are set. After these signals have had time to set up, the clock generates a count pulse which samples the levels and produces a count up pulse or a count down pulse. At the same time the up- and down-sync flip-flops are reset so that the enable signals can be read in the next time. All of the synchronizer and control logic should be from the same speed line. The flip-flops illustrated here are Type 1209's, the clock is a Type 1401, the delay a Type 1403, and the inverters and diode gates can be either 5 megacycle or 10 megacycle logic.

The counter can be a lower speed logic than the synchronizer if desired. In this case, the up and down count pulses should be stretched with Type 4604 Pulse Amplifiers to produce pulses of appropriate duration. In the illustration using Type 4215 Flip-Flops, the outputs are buffered since the flip-flop outputs drive a capacitor diode gate level input, a capacitor diode gate pulse input, and a diode gate input, as well as providing the signals to the DAC. The inverters used for buffering are 10 megacycle units which have a minimum of capacitance. Readout from the counter register should take place from the output of the inverter buffers so as not to exceed the loading on the flip-flops.

The continuous conversion method is applicable when the maximum rate of change of the analog voltage is less than the fastest possible rate of change in the converter. That is:

$$\left(\frac{\Delta V}{\Delta t}\right)_{\text{input}} \leq \frac{\text{Vref}}{2^N \Delta T}$$

where

$$\left(\frac{\Delta V}{\Delta t}\right)_{\text{input}}$$

is the rate of change of the input analog voltage, V_{ref} is the full scale voltage of the converter, N is the number of bits, and ΔT is the time per step. ΔT is the sum of:

Carry propagate time for the flip-flops

Total transition time of the flip-flops

Delay of the level amplifiers

Delay through the divider network

Transition time of the comparator and settling time
(0.15 $\pm$0.05N microseconds)

Total transition time for the synchronizer
(2 microseconds with 4209 flip-flops)
(0.2 microseconds with 1209 flip-flops)

Delay through gates and pulse amplifiers if in feedback loop

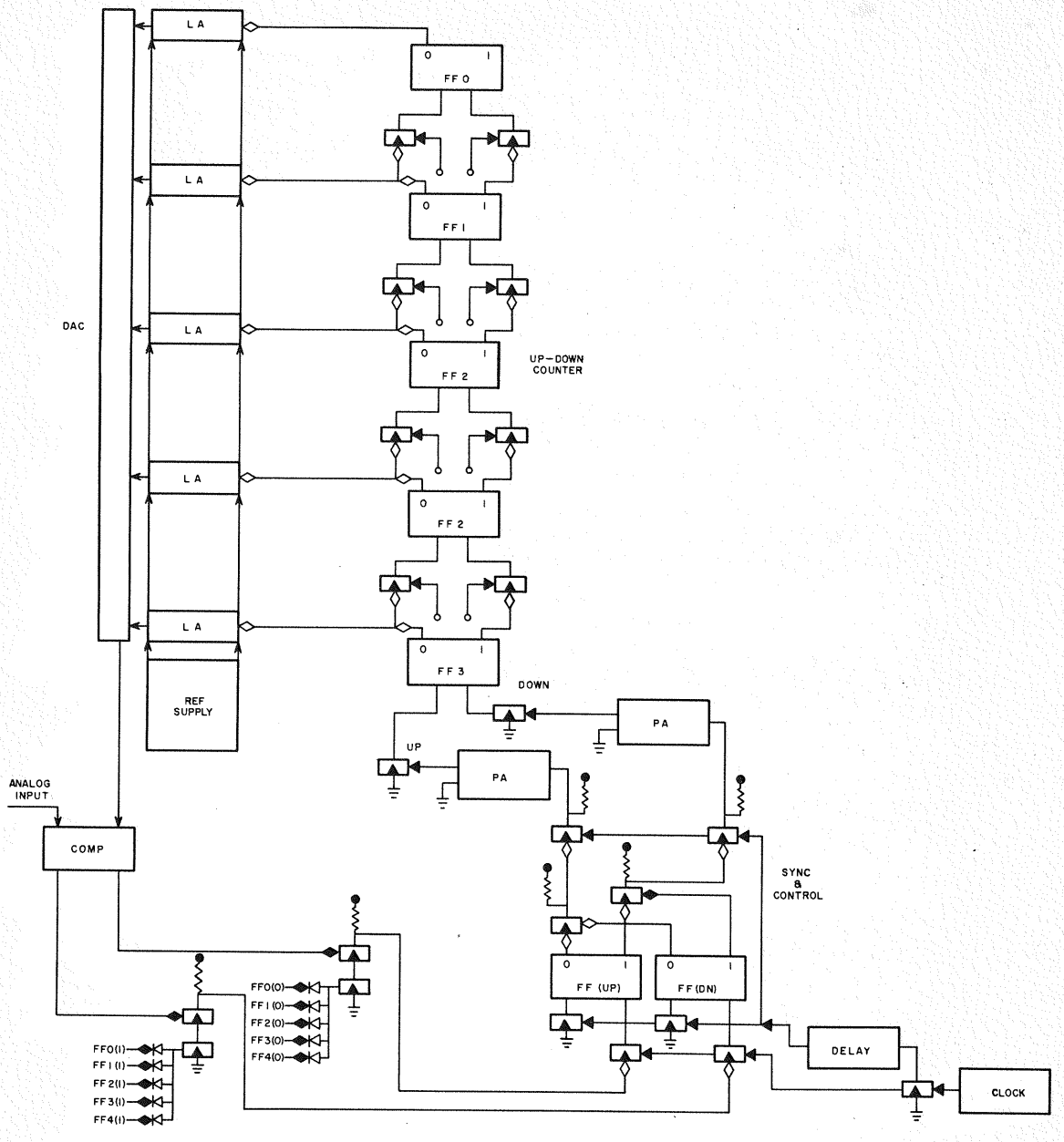


Figure 25 Continuous Converter with Buffered Flip-Flops

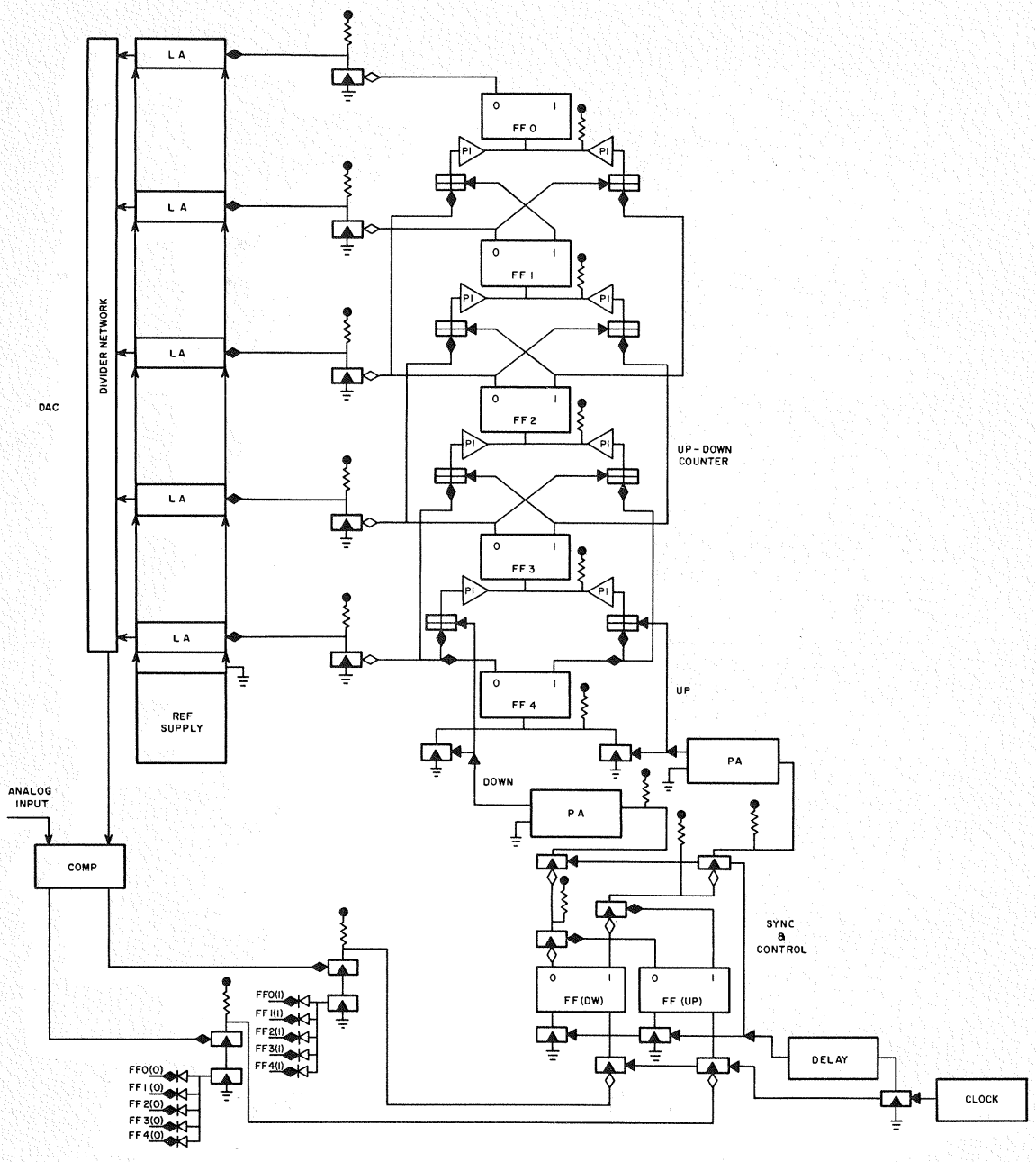


Figure 26 Continuous Converter with Unbuffered Flip-Flop

Carry propagate time may be reduced splitting the carry chain. For example, if flip-flops 2, 3, and 4 are in the ONE state, the count-up signal can be gated to complement flip-flop 1 as well as flip-flop 4. Of course, the normal carry input to flip-flop 1 is not used. Typical times required for the method shown are given in Table 5.

TABLE 5 CONTINUOUS CONVERTER CONVERSION TIMES

No. of Bits	Level Amplifiers	Buffers	FFs	Sync FF	Divider Network	ΔT Time/ Step (μsec)	$2^N \Delta T$ Total/ Time (μsec)	$\frac{V \text{ ref}}{2^N \Delta T}$ (volts/ sec)
6	4679		4201	1209	1574	2.85	182.4	54,824
8	4679		4201	1209	1574	3.05	780.8	12,807
10	4678		4201	1209	1574	3.95	4044.8	2,472
10	4679		4201	1209	1574	3.25	3328.0	3,005
6	4679		1201	1209	1574	1.3	83.2	120,192
8	4679		1201	1209	1574	1.44	368.7	27,393
10	4679		1201	1209	1574	1.58	1618.0	6,180
6	4679	6109	4215	1209	1574	2.05	131.2	76,211
8	4679	6109	4215	1209	1574	2.35	601.6	16,622
10	4679	6109	4215	1209	1574	2.55	2611.2	3,822

SUCCESSIVE APPROXIMATION CONVERTER

This method repeatedly approximates the input voltage. At each step, the possible range of the input signal is divided in half. The converter uses a digital register with gatable ONE and ZERO inputs, a digital-to-analog converter, a comparison circuit, a control timing loop, and a flip-flop distributor register that determines which step is taking place (see Figure 27). The distributor register is like a ring counter with a single ONE circulating to indicate which step is taking place. At the beginning of the conversion, both the digital register and the distribution register are set with a ONE in the most significant bit and a ZERO in all bits of lesser significance.

At the same time, a pulse enters the delay chain. When this pulse has had sufficient time to make one complete loop through the chain, the digital-to-analog converter and the comparator have settled and the comparator output determines whether the next digital approximation should be larger or smaller. At this time, the next most significant bit of the digital register is set to a ONE, and the most significant bit either remains in the ONE state or is reset to a ZERO, depending on the comparator output. The single ONE in the distribution register is shifted to the next position. This procedure is repeated until the final approximation has been corrected, making a total of N steps, plus settling time for the last flip-flop.

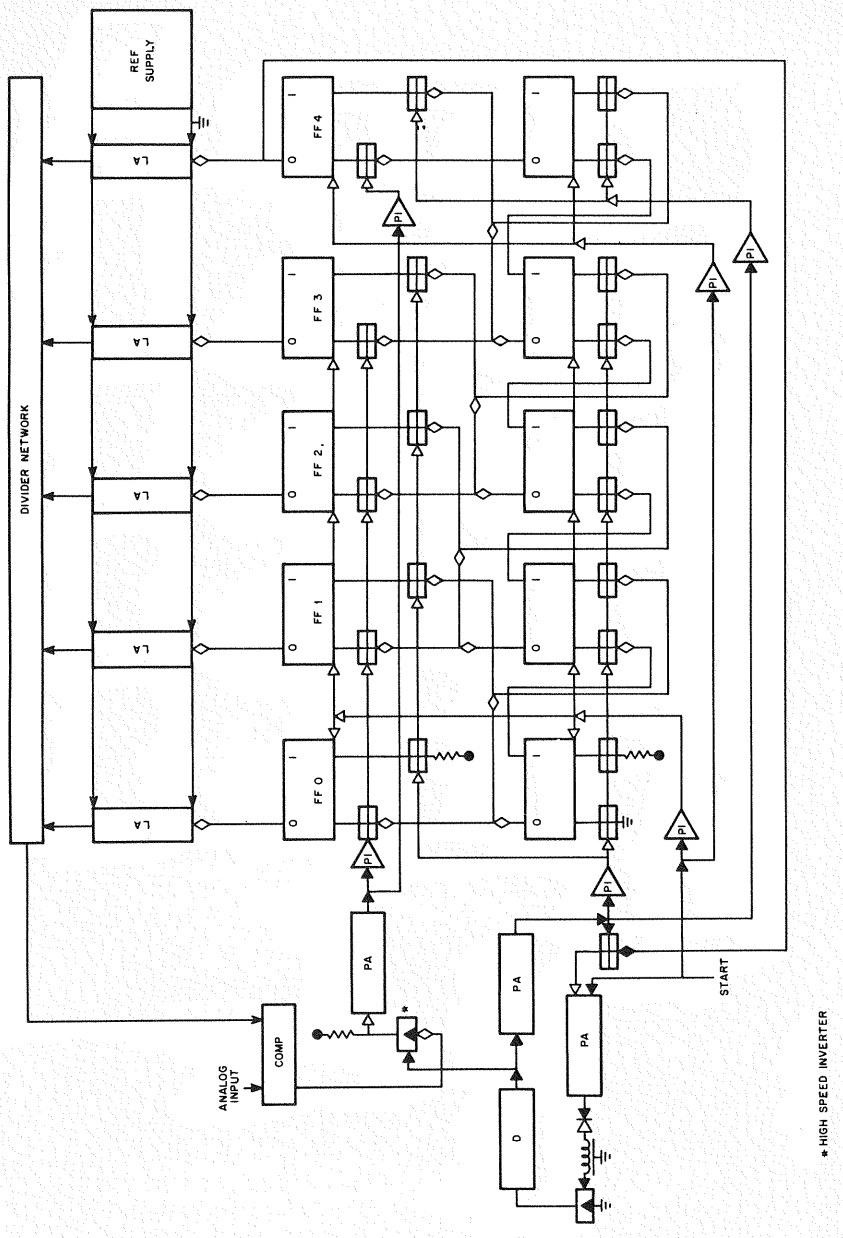


Figure 27 Successive Approximation Counter

The total time required is N ΔT, where ΔT, the time per step, is at least as large as the sum of:

Total transition time for the flip-flops

Delay of the level amplifiers

Delay through the divider network

Transition time of the comparator and settling time
1 microsecond for $N<5$,
0.2 N microseconds for $5<N<8$,
2.4 microseconds for $N=9$,
3.0 microseconds for $N=10$

Delay through pulse amplifier and gates

No synchronization time is required for this method since the comparator never controls the action of more than one flip-flop.

The digital register and the distribution register use the Type 4226 Serial to Parallel Assembler. Due to the set up time of the internal gates, the time per step must be at least 1 microsecond.

The control delay chain uses a Type 1304 delay and a delay line. Gating the comparator with a 70-nanosecond pulse avoids the possibility that the results of the pulse might be fed back through the DAC to the comparator before the pulse when complete. The 70-nanosecond pulse goes through a 1000 or 6000 series inverter; then the Type 4604 Pulse Amplifier is used to increase the pulse duration to 0.4 microseconds for driving the flip-flops. Typical times for the circuit illustrated are given in Table 6.

TABLE 6 SUCCESSIVE APPROXIMATION CONVERSION TIMES

No. of Bits	Level Amplifiers	Divider	ΔT Time/Step (μsec)	Total Time (ΔT (N) + 0.2 μsec for readout) (μsec)
6	4679	1574	1.83	11.18
7	4679	1574	2.03	14.41
8	4679	1574	2.23	18.04
9	4679	1574	3.03	27.47
10	4679	1574	3.63	36.50

CHAPTER 5

BASIC CIRCUITS

This chapter includes general information on the use and importance of various characteristics of converter circuits. Detailed performance characteristics are given for specific Digital modules. Definitions of symbols and terminology are included in the appendix.

Any of the appropriate modules described in the Digital Module Catalog can be used for the flip-flop registers and the control and gating logic in a converter. The choice is governed by speed requirements in the system.

Divider Networks

The Digital binary divider is a ladder as shown in Figure 28. The open circuit output voltage is one-half the voltage at input A, plus one-fourth the voltage at B, plus one-eighth the voltage at E, and so on. Thus, the resulting open circuit output voltage is a properly weighted sum of the individual binary bits.

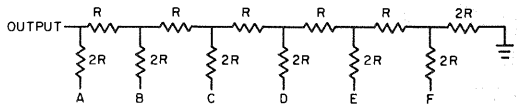


Figure 28 Binary Ladder

INPUT IMPEDANCE

The input impedance is important because of its effect on the driving source. Ladder networks made by Digital have potentiometers in the most significant bits; so the size of the input resistors can be adjusted according to the output impedance of the driving source (see Level Amplifiers).

If the ladder output is terminated in 2R, the input impedance of all bits is 3R. (For Digital ladders, this value is 3000 ohms.) If the ladder output is open circuited or terminated with some other impedance, the input impedance of the most significant bits is changed.* In most cases, it is sufficient to assume all inputs are 3000 ohms.

LOADING THE OUTPUT

Looking back into the output, the open circuit voltage is in series with an output resistance of R. Thus, if the output is loaded, the output voltage will be reduced by the drop

*Input resistance for the most significant bit is $2R + \frac{2R \times Z}{2R + Z}$, where Z is the load resistor and R, for Digital ladders, is 1000 ohms.

through R. Loading the output with a constant impedance does not destroy the binary weighting, and thus the relative accuracy of the digital-to-analog converter, but loading with a variable impedance does destroy it.

The output impedance of a Digital binary divider is 1000 ohms with a tolerance of 0.1 percent to 0.5 percent (see Figure 29 for specific numbers). If the load is heavy, the tolerance on the output impedance can be adjusted with a trimming potentiometer or by changing the reference voltage. With loads heavier than 2000 ohms, second order effects come in to play because of the increased load on the level amplifiers in the more significant bits. The error, in percent of full scale, can be approximated as $\Delta r\ (2000+Z)/20Z$, where Δr refers to the level amplifiers and Z is the load resistance in ohms.

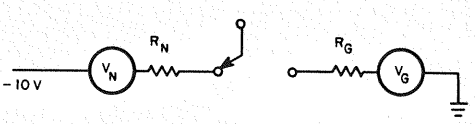
RESISTOR DIVIDER MODULES

The individual characteristics of Digital divider networks are shown in Figure 29. The output impedance of all binary dividers is 1000 ohms. The nominal input impedance is 3000 ohms. The more significant bit inputs have trimpots for fine adjustment. (See Chapter 6 for the procedure.) Unused inputs should be grounded or connected to a voltage source.

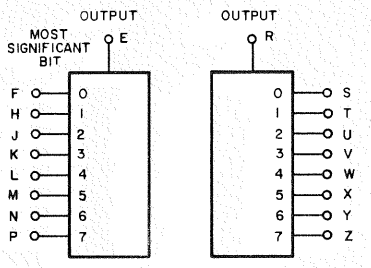
On the Type 1574, the terminating resistor is brought out to pin Z. This pin is normally grounded, but it may be used to add a small amount of positive bias to offset the voltage drop in the ladder drivers. A bias resistor (10,000 ohms including a 150 ohm trimpot) is brought out to pin W and may be used to obtain equal positive and negative excursion. The bias should be a positive voltage equal to 5 times V ref. The output voltage excursion is then $\pm$V ref/2.2. If the biasing terminal is used, the output impedance is 909.09 ohms $\pm$0.35%.

Level Amplifiers

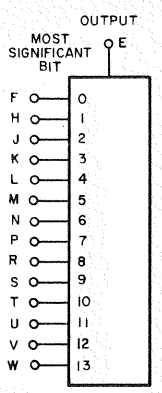
Level amplifiers are used to switch the divider inputs between two precision voltage levels. For Digital amplifiers these are normally ground and -10 volts. Since the voltage comes from an external source, an important characteristic of the amplifiers is how well they approximate an ideal switch. Normally the switch has an equivalent output circuit as follows:



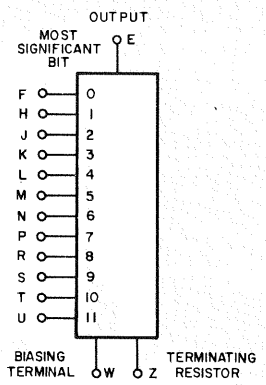
The offset voltages (V_N and V_G) are adjusted for in the converter calibration. If $R_N = R_G$, these are also calibrated for. However, the difference between the two equivalent resistances will produce an error. The equivalent offsets, resistances, and corresponding errors are shown below in Table 7 for Digital amplifiers driving a Digital binary divider.



Type 1563 Digital-to-Analog Converter



Type 1564 Digital-to-Analog Converter

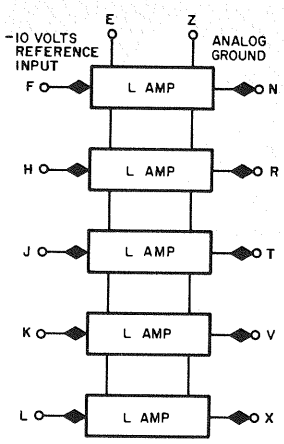


Type 1574 Digital-to-Analog Converter

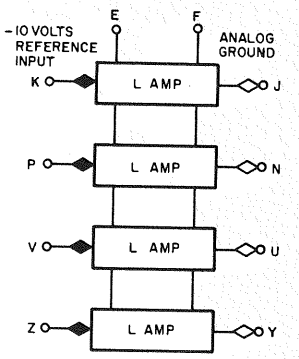
Module Type	Type	No. of Circuits	No. of Bits	T.C. ppm/°C	Speed* μsec	Resistor Type	Tolerance R out.
1563	Binary	2	8	20	1.0	ww	.1%
1564	Binary	1	14	20	1.0	ww	.1%
1574	Binary	1	12	14	0.3	mf	.35%

*Speed listed is the propagate time. Output settling time will depend on how the inputs are changed and the accuracy desired. At high accuracies, the time is approximately the same for all networks. For specific applications see Chapter 4.

Figure 29 Ladder Network Specifications



Type 4678 Level Amplifier



Type 4679 Level Amplifier

Module Type	No. of Circuits	Speed to 90% of Output (μsec)	Input Load (ma $\mu\mu$f)	Inverting	Integral Error % of full scale	Differential Error % of full scale
4678	5	0.8	0.5 330	No	±.01%	±.0013%
4679	4	0.1	±1.3 762	Yes	±.004%	±.0005%

	Output Characteristics				Power Requirements			
Module Type	Nominal Output Resistance (ohms)	Variation in R	V_G (mv)	V_N (mv)	−15v (ma)	+10v(A) (ma)	+10v(B) (ma)	−10v (ma)
4678	2	1.2	0 to −1.0	−0.5 to −1.5	145	0.42	31	20
4679	4–9	0.5	3.2 to 9.7	−0.3 to −3.2	45	0.6	0.6	20

Figure 30 Precision Level Amplifier Specifications

Two precision level amplifiers are available. The Type 4679 is the fastest and most accurate. Type 4678 presents a lighter load to the flip-flop driving it. Type 4678's are matched from circuit to circuit (as well as within the two sides of the switch) so that they may be interchanged without recalibrating the converter.

For systems of about six bits or less, inverter amplifiers may be used instead of the precision level amplifiers. These are standard inverters with the clamp diodes brought out to separate pins so that an external reference may be used. Two types, the 1667 and the 4667 are available; both have six circuits per module. The speed and accuracy will depend on the clamp voltage as shown in Table 7.

TABLE 7 INVERTER AMPLIFIERS SPEED AND ACCURACY

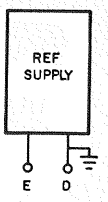
Module Type	−3 volts			−10 volts		
	Differential Error % of full scale	Integral Error % of full scale	Speed μsec	Differential Error % of full scale	Integral Error % of full scale	Speed μsec
1667	±.035%	±.3%	.05	±.11%	±.9%	.15
4667	±.05%	±.4%	.2	±.12%	±1%	.5

In some cases, the accuracy requirements will permit the ladder network to be driven directly from Digital flip-flops or standard inverters. This method is applicable only for converters using a very small number of bits, because the tolerance on Digital standard flip-flop levels is approximately 0 to −0.15 volts and −3.0 to −3.8 volts, although inverters in a single module may have less variation. Additional information — pin connections, etc. for standard inverters and inverter amplifiers — is given in the Digital Module Catalog.

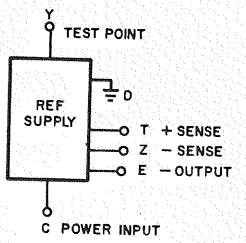
Reference Supplies

The reference supply determines the voltage range of the converter. It is important that the supply be of good quality, since any error in the reference voltage will translate directly into error in the converter. That is, a 0.1 percent ripple in the reference produces a 0.1 percent ripple in the analog output.

Digital manufactures two reference supplies: the Type 1562, which may be used for systems of seven bits or less; and the Type 1704, a precision supply that should be used for more accurate systems and any system with a distributed load. Both supplies are mounted on Digital modules and are driven by Digital standard power voltages. The characteristics are shown in Figure 31.



Type 1562 Reference Supply



Type 1704 Precision Power Supply

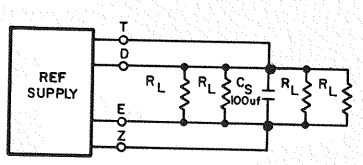
Module Type	Output	Current	Stability	Regulation	Ripple Peak to Peak
1562	−10v	±60 ma	2 mv/°C	30 mv, no load to full load	10 mv
1704	−10v	−90 to +40 ma	1 mv/8 hrs 1 mv/15 to 35°C 4 mv/0 to 0°C	0.1 mv, no load to full load	0.1 mv

Module Type	Adjustment Resolution	Input Power	Use	Output Impedance
1562	80 mv	−15 volts/100 ma +10 volts (B)/ 10 ma	Load with 5000 pf at load. May also pre-load if desired	0.5 ohms
1704	0.01 mv	−15±2 volts/ 250 ma	See below for sensing and preloading	.0025 ohms

TYPE 1704 PRECISION POWER SUPPLY

REMOTE SENSING

The input to the regular circuits of the 1704 is connected at sense terminals T (+) and Z (—). Connection from these points to the load voltage at the most critical location provides maximum regulation at a selected point in a distributed or remote load. When the sense terminals are connected to the load at a relatively distant location, a capacitor of approximately 100 microfarads should be connected across the load at the sensing point.



PRELOADING

The supplies may be preloaded to ground or —15 volts to increase the current available in either direction.

Figure 31 Reference Supply Specifications

Comparators

The comparator is an unusual circuit because it is a hybrid, partially analog and partially digital. Basically, it is a very high gain difference amplifier. The outputs "saturate" quickly so that they do not exceed standard levels. (For Digital equipment these are 0 and —3 volts.) The comparator, Type 1572, has an input range of 0 to —10 volts. When the input differential is large, the dual outputs are complementary Digital levels.

The time required for the comparator to switch states depends on the desired system resolution and the conversion method. That is, the comparator takes longer to respond to a 10-millivolt differential input than for a 100-millivolt differential input. A 7-bit system, for example, seldom requires information about 10-millivolt differentials. Similarly, the comparator switches faster in a counter or continuous converter system, where the differential input is being reduced gradually, than in a successive approximation converter, where the differential voltage may go from 5 volts to 0 in one step.

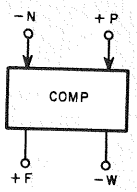
FACTORS AFFECTING COMPARATOR ACCURACY

As the input to the comparator circuit varies from 0 to —10 volts, the switching point may vary also. That is, one of the inputs may have to go somewhat more negative than the other before the outputs switch. A similar effect occurs with changes in temperature. In the Type 1572, the switching point does not move more than 5 millivolts as the input voltage changes from 0 to —10 volts and the temperature changes over a range of 20°C (around room temperature). Power supply fluctuations of the Type 722 or an equivalent supply change the switching point by less than 0.6 millivolts.

Both outputs will not switch simultaneously unless the amplifier is in perfect balance. If the switching point changes mentioned above affect both outputs equally, the effect is referred to as a shift in the common switching level. If one of the outputs is affected more than the other, there is an offset between the two sides of the amplifier.

USE OF THE COMPARATOR

Illustrations of the use of the comparator are included in Chapter 4. In other uses, it must be remembered that the comparator is a hybrid circuit. If the differential input is small, but balance is not quite right, the outputs may not be complementary. If there is a small amount of ripple on the input, the outputs may oscillate. Normally this effect is of no concern because the errors have already been taken into account in the common mode and resolution specifications. However, if the results are to be read into more than one flip-flop, output oscillations can cause different information to be read into the different flip-flops. Thus, the outputs must be synchronized before being read into more than one flip-flop. Similarly, the comparator level changes should not be used as information unless it is certain that transient signals (such as those that occur when a DAC switches) will not cause false outputs.



Type 1572 Comparator

Specifications:

Input Range: 0 to —10 volts

Input Impedance: 1 microampere, 75 picofarads (The input current depends on the relative polarity of the two inputs. The more positive input may draw up to 1 microampere and the more negative input may supply up to 1 microampere. The maximum current difference between states is 1 microampere.)

Outputs: Two outputs, 0 and —3 volt levels

Output Loading: 7 units base load at dc, 1 unit for maximum speed

Resolution: 1 millivolt at dc

Common Mode & Temperature: 5-millivolt maximum equivalent input offset for 10-volt common mode change and 20°C change

Speed:

Depends on application, principally on the ratio of the voltage difference before passing through the switching point (V_B) to the voltage afterward (V_A). Speed is affected to a lesser degree by the length of time the input difference is at V_B, by the magnitude of V_A, by the source impedance, and by the load. Typical speeds in an analog-to-digital converter system where the source is a ladder network and level amplifiers, and the load is a 1 unit base load, are listed below. (These speeds include allowances for extra divider settling times at high accuracies.) For more information on specific applications, see Chapter 4.

V_B/V_A	V_A in mv	Time in μsec
—512	10	3.0
—128	40	1.6
—32	160	1.2
—2	20	0.6
—2	80	0.5
—1/512	10	0.15

Adjustment:

Two potentiometers control zero set and common balance. See Chapter 6 for adjustment.

Power: —15 volts/55 ma; +10 volts (A)/0; +10 volts (B)/21 ma.

Figure 32 Comparator Specifications

When the comparator is used in a digital voltmeter or a continuous converter, it is usually desirable to have built-in hysteresis which is just slightly less than ±½ LSB. The hysteresis avoids converter chatter (switch back and forth between two states) when the input voltage lies on a boundary between the two states. It is possible to introduce some hysteresis into the 1572 by adjusting the common switching level and offset control so that the two outputs do not switch simultaneously. In a continuous converter, counting would then take place only when the two outputs were of opposite polarity. No action would take place when both outputs had the same polarity. The same type of logic would be applied in a digital voltmeter, the exact action depending on the conversion method used to arrive at the results.

Multiplexer Switches

ANALOG MULTIPLEX SWITCHES

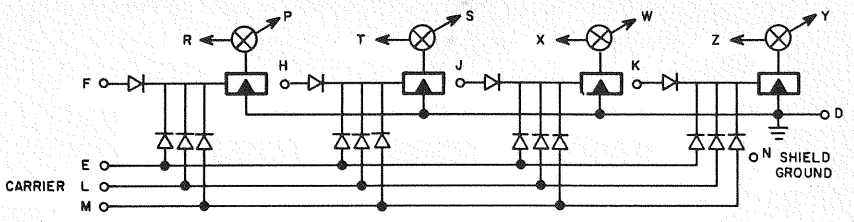
An analog multiplex switch is like a relay, in that two points are opened or shorted on command from an external source. Digital manufactures a relay switch, Type 1807, for low speed operations, and a solid state switch, Type 1578, for high speed operations. Each module contains four switching circuits. The control inputs to these switches are 3-input AND gates, each with a separate control input and all with two inputs in common. If the control inputs are driven from binary to octal decoders, up to 512 switches can be placed in parallel. The accuracy and speed limitations are the switch capacitance and the amount of leakage current back through the switches.

The Type 1578 is available with different performance characteristics (see Figure 33). A fifth digit on the model number indicates the characteristics. However, the basic logic of all is the same. Each contains four switches. Both inputs are available so the switches can be tied in parallel, cascaded to give double level multiplexing for large systems, or used in other applications such as the sample and hold circuitry. Besides the control level inputs, there is a carrier signal which should be driven with a 5-megacycle square wave.

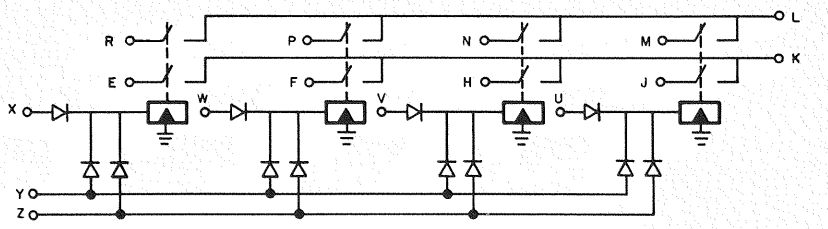
The speed depends on three variables: the delay of the switch, the synchronization time with the carrier, and the time required for the input signal to charge any stray capacitance once the switch has been closed. Synchronization requires a maximum of 100 nanoseconds. The time to charge the capacitance can be figured on an RC basis. The capacitance is the input capacitance of the load circuit plus 10 picofarads per switch. The resistance is the output resistance of the source plus the "on" impedance of the switch. Table 8 shows useful logs for calculating the time constant error. Thus, after three time constants, the error is 5 percent; after 4 time constants it is 1.8 percent, etc.

USE OF THE TYPE 1578 SWITCH

In the off position, most types of 1578 switches can have up to 12 volts across them, generally 10 volts for signal and 2 volts for margin. The control input is transformer coupled so that the 10 volts may be centered at any voltage; for example, it may be 0 to +10 or 0 to −10.



Type 15780, 15781, and 15782 Solid State Switches



Type 1807 Relay Switch

TYPE NUMBER	15780	15781	15782	1807
Type of Switch	Solid state			Relay
Number of Circuits	4, single pole, independent			4, double pole, outputs bussed
Control				
Signals	Digital levels & 5 mc square wave			Digital levels
Enable	−3 v (5 mc sq. wave pin E)			−3 v
Load	1/8 unit emitter load shared among grounded inputs			1/8 unit emitter load shared among gnd inputs
Signal				
Max. voltage	12 v			250 v
Max. current	1 ma			125 ma dc
"On" offset (max.)	200 μv	100 μv	300 μv	
"On" resistance (max.)	50Ω	50Ω	100Ω	0.2Ω
"Off" resistance, leakage	2 na, 10 μμf	2 na, 10 μμf	10 na, 10 μμf	$5 \times 10^8 \Omega$
Speed				
50% input to tolerance output	Delay + sync + charging time			Delay + bounce setting
Turn on delay	400 nsec	600 nsec	600 nsec	0.9 msec
Turn off delay	200 nsec	400 nsec	400 nsec	0.06 msec
Synchronization	100 nsec	100 nsec	100 nsec	None
Bounce setting				0.3 msec
Life				20,000,000 operations at low loads

Figure 33 Multiplexer Switch Specifications

TABLE 8 USEFUL LOGS

t/T	$1 - e^{-t/T}$	$e^{-t/T}$
3	0.95021	0.04979
4	0.98168	0.01832
5	0.99326	0.00674
6	0.99752	0.00248
7	0.99909	0.00091
8	0.99966	0.00034
9	0.99988	0.00012
10	0.99995	0.00005

The switch is turned on when the three control level inputs are negative voltage (or open) and the carrier input is receiving a 5 megacycle square wave. This square wave can be made using a 10 megacycle clock and a 10 megacycle flip-flop.

When changing the state of the switches, care should be taken that two switches tied to a common node are never turned on simultaneously. If the control levels come from 10-megacycle flip-flops which are all changed simultaneously and which are decoded by 5-megacycle binary octal decoders, the switching is fast enough so that there is no danger of shorting. If low speed circuitry is used to drive the switch, or if the controlling flip-flops are not all changed simultaneously, the carrier input or one of the enabling inputs should be grounded before the state of the switches is changed. This will put all of the switches in the off position and assure that there will never be a make before break situation.

When a single switch multiplexer switch is used, the output voltage will probably remain the same for a long period of time since the RC time constant is determined by the leakage of the switch plus the impedance of the load, rather than the impedance of the source.

RELAY MULTIPLEXER TYPE 1807

The Type 1807 contains four double pole switches which can be used for differential multiplexing. The switch outputs are connected to pairs of output busses. The speed of the relay is determined by the delay in turn-on plus the bounce settling time. For the Type 1807 this delay is 1.2 milliseconds. There are three control level inputs for each relay; two of these are common to all relays in the module, and one is independent. The relay is turned on when all of its control inputs are negative.

The 4000 series unbuffered flip-flops are particularly good for converters since the delay is built into the level inputs of the associated capacitor diode gates instead of the flip-flop outputs. Thus, the time between pulsing the input and the switching of the outputs is short. The 6000 series inverters are also good for any units important to the timing of the system, that is, as buffers for the flip-flops and for gating the comparator. These inverters switch extremely fast and present only a small capacitive load; thus they do not slow the switching time of the device that is driving them.

TABLE 9 TRANSITION TIMES FOR DIGITAL MODULES

Module	Transition Time (nsec)	Carry Propagate Time (nsec)
Inverters		
1000 series	20	
4000 series	300	
6000 series	12	
6000 dual inverter gates	17	
Diode Gates		
1000 series gatable emitter (1110, 1111)	50	
1000 series gnded emitter neg AND (1113, 1115, 1117)	90	
4000 series gatable emitter (4110, 4111)	400	
4000 series gnded emitter	160	
neg AND (4113, 4115, 4117)	300	
neg OR (4112, 4114, 4118)	160	
6000 series	50	
Capacitor Diode Gates		
4000 series negative gates	50	
Flip-Flops (includes input gate)		
1000 series	150	17
4000 buffered (4201, 4209)	1300	100
4000 unbuffered (4214, 4227)	180	50
4000 series counter with cap. diode gates (4215 with 4127)		100
6000 series buffered	80	15
6000 series unbuffered	70	
Pulse Amplifiers		
1000 series	25	
4000 series	50	
4000 series standardizing PA's (4604)	75	
6000 series	25	

The switching times to be used in calculating converter timing are summarized in Table 9. Complete circuit descriptions are in the Digital Module Catalog. Little else need be said about them here except to mention the Type 4226 Flip-Flop, expressly designed for use in the successive approximation analog-to-digital converter. This unit contains two 4-bit registers. The lower one is for use as part of a ring counter. A single ONE is

inserted into the first flip-flop in the chain, and each shift pulse moves it down the chain. The location of the ONE in the chain provides timing information for the successive approximation converter. The upper register serves as a buffer for the converter. The set line is tied to the shift line of the lower register; and the gating is arranged in such a way that as a ONE is shifted into one of the flip-flops in the lower register, the corresponding flip-flop in the upper register will also be set to the ONE state. The clear line is separate, and if it is pulsed simultaneously with the shift line, it will clear that flip-flop in the upper register which corresponds to the flip-flop being cleared in the lower register.

Analog Amplifiers

Amplifiers are sometimes used at the input of an analog-to-digital converter to shift the input range, scale the input range, provide a differential input, or isolate the input signal from the converter. Amplifiers are used on the output of digital-to-analog circuits to shift or scale the output range, to reference the output signal to the external ground, and to lower the output impedance. The last two features are important when the two pieces of equipment are separated by a distance that makes noise pick up likely. In this case, it is best to put the amplifiers at the driving source end, that is, at the output of the divider network in a digital-to-analog conversion or at the signal source for analog-to-digital.

High input impedance is the advantage of the follower configuration. An advantage of the operational amplifier configuration is the ease with which the scale can be changed by switching the input resistances.

A typical configuration for using operational amplifiers circuit on the output of a digital-to-analog converter is shown in Figure 34. The bias voltage and the ratio of R3 to R2 determine the offset. The ratio of R3 to R1 determines the scaling factor. The inverter ground reference coming in provides a means of referencing the signal to an external ground. On the input from the converter, the resistor has a value of R1 — 1000 ohms because the output impedance of the divider, 1000 ohms, is taken into account.

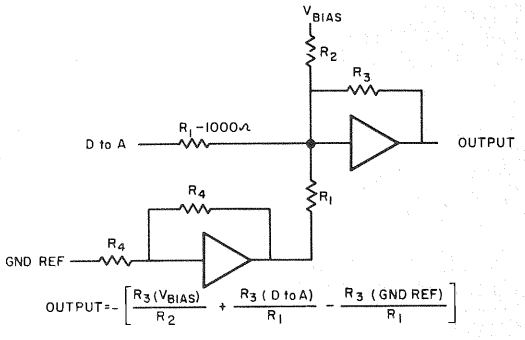


Figure 34 Typical Amplifier Configuration
for Scaling and Biasing Digital-to-Analog Outputs

Scaling, offsetting and differential input to an analog-to-digital circuit follow exactly the same method. The input resistor would be R1 minus the appropriate output impedance of the driving signal.

When amplifiers are required on converters, it is generally best to use the same type of amplifier as is being used in the analog portion of the circuitry to keep the performance characteristics the same. When an amplifier is being used internally in the converter, such as between a group of multiplexer switches and an analog-to-digital converter, a higher performance amplifier is required, since it will be asked to take full scale changes and settle within a very short time.

The Type 1751 is a linear dc amplifier with a voltage gain of 10,000 and a current gain of up to 40,000 at low frequencies. It can operate in the presence of common mode signals between ±10 volts. Its maximum output voltage is ±10 volts; it can deliver as well as accept up to 20 ma. of output current. Output is short circuit proof.

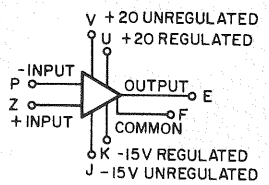


Figure 35 Type 1751 Operational Amplifier

SPECIFICATIONS

Bandpass (3 db down)	1.5 kc
Gain-Bandwidth Product	15 mc
Offset Voltage Temperature Coefficient	±25 μv/°C between +55°C and −20°C
Offset Voltage/Supply Voltage Stability Coefficient	±5 μv per 1% of supply voltage change
Offset Voltage/Common Mode Stability Coefficient	±60 μv/v common mode between ±10v
Input Current Per Side	±500 na
Differential Input Current	±200 na
Input Current Temperature Coefficient	±10 na/°C between −20°C and +55°C
Differential Current Temperature Coefficient	±4 na/°C between −20°C and +55°C
Open Loop Voltage Gain	10,000
Differential Input Impedance (Z in)	100 KΩ
Open Loop Output Impedance	2Ω (typical)
Output Rise and Fall Times (follower configuration)	3 μsec

CHAPTER 6

INTERCONNECTION AND CALIBRATION

Grounding and Shielding

If the converter system operates with eight bits or more, care should be taken with the system wiring to avoid noise pickup and ground potential differences between the analog equipment and the converter. Since the digital voltages are low level, the major noise source within the converter is fast-switching transients, particularly pulses. Their effects can be minimized by isolating the analog portions (the divider network, level amplifier, reference supply and comparator) from the digital portions of the converter. Pulse-generating devices, such as clocks and pulse amplifiers, should be farthest away from the major analog components.

Single wires can be used within a mounting panel or between two panels if no noise sources are nearby. Coaxial cable is best, of course, for long leads. However, a twisted pair is usually sufficient, even in high accuracy systems, if pulse lines and other fast transients are avoided. The shield conductors of the coaxial or twisted pair should be tied down at one end only, and this end should go to a good ground, not near a pulse transformer or other high frequency device.

On the precision level amplifiers, there is a separate input for the high quality ground. These inputs can be tied together and fastened to chassis ground at a good solidpoint. On a large system excessive ground loops should be avoided, but in a single converter of 10 bits they normally cause no error.

Similarly, in large systems sense wires from the reference voltage supply should be brought to a point near the load so that the supply will regulate the voltage as seen by the load, not the voltage as generated at the power supply. If the load is distributed, capacitors at the main load points will reduce transients caused by the rapid switching of the level amplifiers. A separate ground-shield is brought out on the Type 1578 Multiplexer Switch. It isolates the analog signal from noise transients generated by the multiplexer control signals. Any solid ground source can be used here, but this analog signal is not a ground reference for the system.

Signals from a high impedance output are more sensitive to noise pickup than those from a low impedance output. Thus, if a digital-to-analog converter is to drive long leads where noise could be picked up, the output should be buffered with an amplifier having a low output impedance.

The size of the ground potential differences which can occur between the converter and the analog input or output signal should also be minimized. If it is not possible to place the two pieces of equipment close to each other with the grounds tied tightly together, a

heavy ground strap can be run between them. Alternatively, the ground potential differences can be subtracted out. In an analog-to-digital converter this is done by using a differential amplifier at the input, or by using two standard operational amplifiers. In the latter case, one of the amplifiers is used to invert the ground; then the signal and inverted ground are summed. In digital-to-analog conversion, the ground from the signal destination is brought back to the converter, inverted with an operational amplifier, and summed with the signal.

CAUTION

The precision level amplifiers and the multiplexer switches are low impedance switching circuits. Precautions should be taken against possible shorting of the analog inputs and outputs of these circuits to any other low impedance source, including ground. Such shorting could damage either the circuits or the signal sources.

Calibration

EQUIPMENT NEEDED

The adjustment and calibration procedures outlined here are designed to be as simple as possible. Four pieces of equipment are needed, as follows:

1. A Digital Module Extender, Type 1954.
2. An oscilloscope with a high gain ac-coupled vertical amplifier and a dual trace amplifier.
3. A low-frequency sine wave generator with variable amplitude (10 to 100 millivolts) transformer coupled output. Stepped down ac power may be used if it is clean. This equipment is needed for analog-to-digital converters only.
4. A reference for determining proper gain setting. Can be a standard voltage or a reference from the analog equipment.

GENERAL PROCEDURE

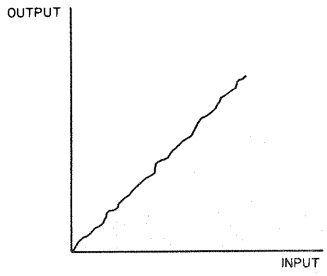
There are six kinds of calibration needed for basic conversion systems. They apply to digital-to-analog converters and to three types of analog-to-digital converters: the counter, continuous, and successive approximation types. Other conversion systems require basically the same kind of adjustments, with certain steps added or omitted depending upon the circuits used. In this chapter, the six general procedures for calibration are presented as follows:

Steady State Calibration
- Divider Network
- Comparators (analog-to-digital conversion only)
- Offset and Gain

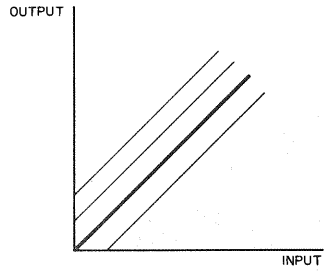
Speed
- Noise and Ripple
- Digital-to-Analog Adjustment
- Analog-to-Digital Adjustment

Calibration should follow in the same order as the procedure given. In steady state calibration particularly, the divider, offset, and gain adjustments carried out in that order make it unnecessary to repeat previous adjustments for fine trimming. The effects of these adjustments can be seen easily if output is plotted against input. Normally, with the digital number 0 in, the output should be 0 volts out, and vice versa. Similarly, maximum input should yield full scale output. Intermediate points should fall on a straight line between these two points.

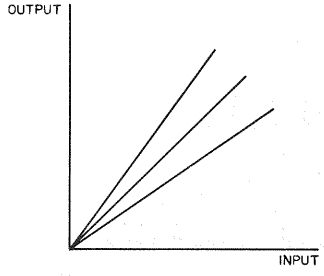
An uncalibrated converter, however, produces the non-linear plot shown below.



By adjusting the divider network, the irregularities are removed from the curve and it becomes a straight line. Next a small amount of offset is added to the network, shifting the curve up and down, as shown below, until the zero input gives a zero output.



Finally the gain is adjusted until a relatively large input produces the correct output. The slope of the curve will change as follows:



DIVIDER ALIGNMENT

The divider is aligned to compensate for variations in resistors in the divider network and for variations in the output impedance of the level amplifiers. The output voltage from the bit to be calibrated is compared with the output voltage resulting from all of the bits of lesser significance. The difference is trimmed so that it is equal to one least significant bit. A simple setup for making this adjustment is shown in Figure 36. The clock, delay one-shot, and inverter simulate a digital input to the converter. Here they are shown switching the inputs between 00100000 and 00011111. Thus, the bit under test is the third bit, and the adjustment is made with the trimpot on that bit.

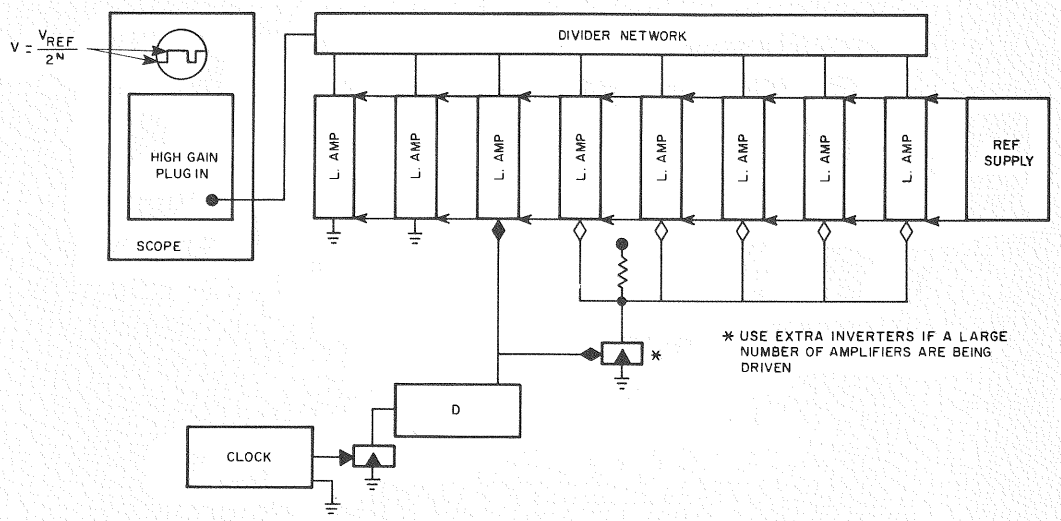


Figure 36 Divider Adjustment

The output should be monitored by an oscilloscope with a high gain, ac coupled vertical amplifier. The amplitude of the output should be one least significant bit voltage contribution. Since this alignment also adjusts for variation in output impedance of the level amplifiers, the level amplifiers should be driving the same divider inputs in the alignment setup as in the final system. Any unused bits of lesser significance should be grounded in the test setup just as in the system. Inputs to level amplifiers in more significant positions may be either grounded or connected to —3 volts, as long as they remain constant throughout the alignment.

In starting the alignment, it is advisable to check a non-adjustable bit first to make sure that the setup is correct. Using this method, the adjustment of bits of lesser significance is independent of the adjustment of bits of more significance. Therefore, the least significant adjustable bit should be checked first, then the next in order, and so on toward the most significant bit. The alignment is then completed in one step, without the need of going back to realign any portion.

The sensitivity to the trimpot motion depends on the number of bits being used. In a 1574, for example, there are eight adjustable bits. In a 10-bit system, where the voltage differential being observed is approximately 9.8 millivolts, the motion of the eighth potentiometer is barely seen on the scope. Working toward the most significant bit, the adjustment range will become larger and larger until it may be possible to invert the relative values of the outputs. To avoid such inversion, note whether the longer portion of the rectangular wave corresponds to the more negative part of the signal or to the more positive part of the signal. Be sure that this relationship continues the same for all of the bits.

Some of the ladder networks use fine resolution wire-wound trimpots. Ascertain that they are in a stable position and that the slider arm is not resting on a single wire where it could jump away, possibly in the wrong direction. After trimming, tap the pot once or twice with the end of a screwdriver and, if the output changes, retrim to the stable position closest to the ideal value.

CAUTION

Some of the trimpots are hermetically sealed. Since the input end is connected to a near short circuit of either ground or —10 volts, be careful not to short the other end to any voltage, as this could greatly exceed the wattage rating and the trimpot seal would explode.

There are two advantages of this particular method of alignment. As the trimpot is changed, the dc level will move up and down. However, since the levels are being observed simultaneously, and only the difference is being monitored, the scope can be put on ac and the picture will stay in the center of the scope face. Also, since the adjustment is made on the differential between two states, a 10 per cent error in the adjustment will give an error in the system of only 10 per cent divided by 2^N.

An ohmmeter should not be used to adjust the ladder network, since it will not take into account the output impedance of the level amplifiers. Do not try to adjust the output with a voltmeter since the dc level shift would require switching between the two states, and the measurements would be extremely confusing and time-consuming.

NEED FOR REALIGNMENT

Realignment should not be necessary under normal conditions. The system should be checked if the modules have been subjected to a drastic change of temperature or to a mechanical shock sufficient to change the trimpot settings. If Type 4679 Level Amplifiers or inverter amplifiers are used, realignment should be done if one of these modules is changed. Replacing Type 4678 modules does not require readjustment because the output impedance is matched for all modules.

THE COMPARATOR TYPE 1572

The comparator can be adjusted easily with a transformer and a dual trace oscilloscope. A sine wave, in the range of a few hundred cycles, should be applied to the comparator through a transformer which is center-tapped or end-tapped at —5 volts. Stepped-down 60 cycles is also suitable if the signal is relatively clean and noise-free. The peak-to-peak voltage should equal the change of the few least significant bits.

The two outputs of the 1572 are viewed simultaneously on a dual trace oscilloscope. With both traces synchronized to a single point, the two signals will appear as roughly complementary square waves. For most applications the comparator should be balanced; that is, both outputs change simultaneously when the relative polarity of the inputs changes. For continuous converters or digital voltmeters, however, such adjustment would cause the converter to oscillate around a dc level. In this application it is desirable to delay switching of the outputs until the input analog signal is almost ½ LSB away from the divider input. The small amount of hysteresis introduced prevents converter chatter.

ADJUSTMENT FOR BALANCE

The comparator should be adjusted so that the two outputs are perfect complementary square waves. Adjust the upper potentiometer to make the two waveforms complementary. Adjust the lower potentiometer for equal positive and negative portions of the square wave. These controls are somewhat interdependent, so it is necessary to repeat the adjustments until the optimum symmetry is observed. The resolution can be increased by reducing the size of the input sine wave and repeating the adjustment.

COMPARATOR WITH HYSTERESIS

Begin the adjustment with a relatively large (several least significant bits) peak-to-peak voltage on the input sine wave, and make sure that the outputs observed on the scope are very close to being complementary sine waves. Then reduce the input amplitude to the equivalent of about 2 LSB. Observe the amount of time during which the two inputs to the comparator are within $\pm$½ LSB of each other. Then without changing the time setting on the scope, adjust the two output signals so that both are the same voltage level for the period of time previously measured. Be sure that the output level of the comparators during the "equality" time period is the same level as was assumed in designing the system logic; that is, if they are assumed to be at ground for equality in the system, be sure that they are both at ground for equality when adjusting the comparator.

WHEN TO READJUST

The comparator adjustment can change with time, temperature, or a mechanical shock severe enough to jar the potentiometers. The need for readjustment depends on the accuracy required and the environment. Usually a monthly check is more than sufficient. Testing can be done by taking the comparator out of the converter and employing the above method or by testing the overall system, as described in the next chapter.

If the comparator has been badly misaligned, it can easily be brought back to alignment with a relatively large input sine wave (50 to 100 millivolts). Adjust the outputs for maximum symmetry with this large input swing; then reduce the swing, and repeat the adjustment until the desired sensitivity is reached.

OFFSET AND GAIN

Offsetting and gain adjustments should be made on the assembled system. In a digital-to-analog converter, a digital number is put in and the output is observed with a voltmeter. In an analog-to-digital system, a voltage is put in and the switching points are observed. Offset and gain adjustment are necessary to compensate for the open-circuit voltage drop of the level amplifiers, which can be as high as 10 millivolts in precision converters. In an analog-to-digital converter offsetting is also necessary to center the quantization error; that is, if the state zero corresponds to 0 volts and the state one corresponds to 10 millivolts, the converter should switch between states zero and one at an input of 5 millivolts.

OFFSET

The calibration should begin with the offset. A positive voltage is applied either to bits in the ladder that are of lesser significance than those used, or through a large resistor (usually on the order of 1 to 10 megohms) attached to the digital-to-analog converter output, or both. The number of inputs, the size of the bias resistor, or the amplitude of the bias voltage can be varied until the offset is correct. For digital-to-analog conversion, zero in gives zero out. For analog-to-digital, an input of ½ LSB produces the first switching point.

The offset voltage source can be the standard +10 volts (for systems of up to 10 bits). The percentage variations in the voltage supply for the offset signal are scaled according to the amount of bias obtained. That is, a 10 percent ripple on the bias supply produces a 10 percent ripple in the offset; so if the offset is 10 millivolts, a 10 percent ripple would be 1 millivolt.

GAIN

The gain adjustment on a digital-to-analog converter is made by setting the digital number to half-scale or full-scale and adjusting the reference voltage supply until the output has the correct value. The Type 1562 has one trimming potentiometer for this adjustment. The Type 1704 has both a fine and a coarse adjustment. In checking the output voltage, remember that the output impedance of the divider network is about 1000 ohms. Thus, loading the output with one megohm would reduce the output voltage by 0.1 percent. This adjustment should be done with the same load as in the final system.

The gain adjustment for an analog-to-digital converter differs only in that the common mode effect of the comparator must be taken into account. The comparator has been balanced with a −5 volt common mode. The offset has been applied so that the lowest switching point is correct. Therefore, the reference adjustment which gives the correct half-scale switching point is different from that which gives the correct full-scale switching point. Generally, maximum accuracy is desired in the lower part of the scale, so the mid-scale point should be used. Alternatively, the reference may be adjusted for the best fit between half-scale and full-scale points. In calculating the switching points for these measurements, be sure to remember the quantization offset that has been introduced. This adjustment should be made at low speed (10 to 20 microseconds per step).

Speed Adjustments

NOISE AND RIPPLE

When the level amplifiers switch, a transient current is drawn from the reference supply. Normally this supply is loaded with a capacitor to reduce noise (see power supplies, Figure 31), but it may also be desirable to place small capacitors at the reference inputs of the individual level amplifiers and possibly also between the high quality ground and the chassis ground. Older models of level amplifiers have internal by-pass capacitors between —10 volts and ground. For maximum speed, these should be clipped out and the external capacitor, if needed, should be matched to the system. The voltage at the load can be monitored on a scope with a high-gain dc-coupled plug-in unit.

Care should be taken that the noise being observed is actually there and not introduced through the scope or by a ground lead attached to the wrong point. The reference and the ground tend to move together. If the input signal source is referenced to this ground, it also moves. Thus, the scope should generally be disconnected from the power at ground and connected to the converter ground at a good solid point, and the cable running to this scope should be prevented from introducing additional noise.

ANALOG-TO-DIGITAL ADJUSTMENTS

As mentioned previously, the speed and accuracy of an analog-to-digital converter are interrelated. That is, if the converter is run too fast, level amplifiers, ladder networks, and especially the comparators do not have enough time to settle to final value. Chapter 4 shows the speeds at which systems are run for the type of accuracy that is normally desired with different numbers of bits. In the range of 6 to 10 bits, even a tenth of a microsecond per step can make a considerable difference in the system accuracy. Thus, the speed may be adjusted for the maximum allowable time and hence the maximum accuracy, or it may be adjusted for the minimum time required to give the required accuracy.

Test for speed should be made by checking the major switching points. For most converters (including the counter, continuous, and successive approximation types) these are around one-fourth, one-half, and three-fourths of full scale, as shown below.

Area Being Checked	From	To
1/4	0011...110	0011...111
	0011...111	0100...000
	0100...000	0100...001
1/2	0111...110	0111...111
	0111...111	1000...000
	1000...000	1000...001
3/4	1011...110	1011...111
	1011...111	1100...000
	1100...000	1100...001

For a more detailed check, the switching points around 1/8, 7/8, 1/16, etc., might also be included.

DIGITAL-TO-ANALOG ADJUSTMENTS

The digital-to-analog converter output contains transients when many bits are changed simultaneously, such as in going from 01111 to 10000. These transients are caused by variation in flip-flop transient times and propagation time through the divider.

Transients can be reduced by adding a small choke in series between the flip-flop and level amplifier, or by loading the flip-flop with a resistor to —15 volts. Further reduction can be made with a low pass filter on the output (remember that the digital-to-analog output impedance is 1000 ohms.)

CHAPTER 7

TESTING AN ANALOG-TO-DIGITAL CONVERTER

The adjustment and calibration procedures detailed in the previous chapter should result in a converter that operates correctly over the whole range. To make sure the converter meets specific accuracy requirements, testing may be desired, and simple operating checks should be repeated at regular intervals to assure continued correct operation.

If the converter is part of a general purpose computing facility, complete testing can be performed easily under program control. If, on the other hand, the converter is part of a specialized system or is to be tested before installation in such a system, manual or semi-automatic testing is necessary and will probably cover only the worst cases. For most converters (counter, continuous, and successive approximation) the worst cases are seen at the major switching points; namely, one-fourth, one-half, and three-fourths full scale (see Chapter 6).

The following sections describe tests that can be performed to measure the various converter characteristics either manually or by computer. The equipment required depends on the tests to be performed. Some of the tests require very specialized equipment, while others can be performed with quite simple equipment.

MONOTONICITY

This simple test requires a minimum of precision equipment. It does not guarantee a specific accuracy but gives a good indication. If a converter with a ladder-type divider passes a monotonicity check, the relative error in the DAC will be small, probably less than ± 1 LSB.

DIGITAL-TO-ANALOG — Monotonicity can be checked by driving the converter from a counter and observing the output on a high gain scope. The output should be a staircase pattern.

ANALOG-TO-DIGITAL — The input can be any noise-free power supply (such as a battery) and a potentiometer of less than 2000 ohms. In testing high resolution systems, potentiometers should have a coarse and fine control with overlapping ranges. Starting at zero, increase the input voltage and check that each state exists and that these states are in the correct order. A similar computer-controlled test can be done using a saw tooth generator as the input signal.

STEADY STATE ACCURACY

DIGITAL-TO-ANALOG — Set an input to a known digital number and observe the output with a high accuracy meter. Compare with the theoretical value.

ANALOG-TO-DIGITAL — The input can be a high accuracy voltage reference or a stable, ripple-free, variable power supply with a high accuracy meter. When the converter is run at a rapid rate, the indicator lights will show quite clearly where the switching points are.

The input voltage at the switching point is measured and compared with the theoretical value. Computer controlled checking can be done in a similar manner using a precision programmable reference as the input signal.

NOISE

DIGITAL-TO-ANALOG — Noise can be measured on a scope with a high gain, ac-coupled plug-in unit.

ANALOG-TO-DIGITAL — The noise appears as a band around the switching point, where the converter output is oscillating between two neighboring states.

INTERMITTENT ERRORS

Intermittent errors can be caused by pickup or loss of a bit in the digital section or by noise picked up in the analog section. The test for intermittent errors should be done with automatic or semi-automatic equipment where the converter is run at full speed for an extended period of time. The equipment should be installed in its final configuration so that the transmission of the information is included in the test. It is important to check the states where there is only a single 0 or a single 1 for possible pickup or loss of information in the digital transfer.

In a general purpose system which includes two-way conversion, an intermittent error check can be run in a closed loop. The computer can generate a pattern wave of digital numbers which are converted to analog, then reconverted to digital. The results are checked to see that the two numbers agree within their specified tolerance.

DIGITAL-TO-ANALOG — In a general-purpose system, limits for two specific numbers can be set up with two comparators, and the state of the comparators can be sampled by the computer after the corresponding number has been brought in. Where other numbers are read in, the comparator outputs would not be sampled, of course. For semi-automatic testing, a similar system might be set up with a counter driving some of the bits of the converter and toggle switches driving other bits.

ANALOG-TO-DIGITAL — In a general purpose system, a dc voltage input would be applied and the computer would monitor it to make sure that all the readouts produced the same number or two adjacent numbers.

To test semi-automatically, set a dc voltage input that is as far as possible from any switching point and insert the equivalent number into a bank of toggle switches. The Type 4139 or 4141 Diode Gate can be used to compare the output with the toggle switches. A clock and a few gates can be set up so the converter runs at its maximum rate and stops if the toggle switches and the analog-to-digital converter do not agree.

SETTLING TIME (DIGITAL-TO-ANALOG)

In most applications, the digital-to-analog converter is asked to go through small changes at a time. The worst case transients occur when all the flip-flops change, that is, when the

states change from 0111 to 1000. The transients involved can be measured quite easily using the same setup as described for adjusting the ladder network. (see Chapter 6).

The settling time with respect to large transients is most important when the converter output is being multiplexed. It can be observed by looking at the signal on a single channel with a high gain scope.

In a system where the multiplexing is done digitally, or where there is only a single channel, the response to large transients is only important when a group of conversions is started; after which the converter will be changing in relatively small steps. If an analog-to-digital converter had been constructed with the same modules, then the response to large transients can be inferred from previous operation. For example, in a successive approximation converter, the settling time for a quarter-scale step must be less than the time per step of the converter.

To observe the settling time more directly, a comparator can be used with one input set to the desired threshold of the dc value of the digital-to-analog converter. The Digital-to-Analog can be switched back and forth, and the comparator output can be monitored on the scope.

RESPONSE TO TRANSIENTS (ANALOG-TO-DIGITAL)

Transient response is extremely important in a converter with multiplexed inputs. The response can be tested in the same way that switching point accuracy is tested. Alternate the input between a test channel and an offset channel. Vary the voltage on the test channel until a switching point is found, and compare this with the switching point that was observed in the steady state test. If the output is observed visually on indicator lights, the voltage on the offset channel should be one which gives all zeros or all ones, so that the alternate voltage can be read clearly.

If the output is being monitored by a computer, the steady state and transient switching points can be measured simultaneously by performing several conversions before changing the channel. The first conversion will give the transient results, the last conversion will give the steady state results. A check should be made with the offset and test channels at nearly opposite ends of the voltage range. Do not use end points, as the converter saturates and overshoot would not be detected. The first decision point should be tested. In a successive approximation converter, for example, the first decision is whether the input is above or below half-scale.

In a single channel system, the transient response is only important for the first conversion. It can be checked manually, running the converter from a push-button and changing the input voltage manually. The general approach would be the same as for a multiplexed system.

Operating Checks

Operating checks are made to assure that the equipment has not been damaged, wires have not been pulled off, or other catastrophic failures have not occurred. If properly set up, the check also detects drift, so that the converter will never actually reach a point where it needs realignment. Generally the test should be simple and should be a part of

the overall preventative maintenance routine for the equipment. In a general purpose computing facility with both types of conversion systems, a closed loop test can be run very simply by plugging the digital-to-analog converter into the analog-to-digital converter and comparing the results that come back with the original number.

If a converter is being tested separately, a simple test can be made on the worst case points. If precision equipment is not readily available for the test, the converter can be checked against a divided-down value of its own internal reference.

APPENDIX 1

SIGNED DIGITAL NUMBERS

In the foregoing chapters, the most significant bit represents —5 volts, the next most significant bit, —2.5 volts, and so on. Thus, the all ZERO state corresponds to 0 volts and the all ONE state corresponds to 1 LSB less —10 volts. This conversion can be reversed simply by using the opposite side of the flip-flop to drive the divider.

If only the most significant bit is reversed, the numbers are signed, 2's complement, as shown below. Since more numbers are negative than positive, the negative numbers are used for 0 to —5 volts and the positive numbers go from —5 to slightly less than —10 volts.

Voltage	Unsigned	Signed
0	000000	100000
	000001	100001
	.	.
	.	.
	.	.
	.	.
	011110	111110
	011111	111111
−5	100000	000000
	100001	000001
	.	.
	.	.
	.	.
<−10	111110	011110
	111111	011111

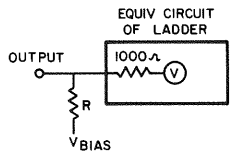
In 1's complement, the weighting of the sign bit is reduced so that +0 equals —0. (Thus, it cannot be used in a system with redundancy, a variable word length or any other feature which does not give a constant one to one correspondence between voltage and number.) Weighting is done by increasing the resistance of the MSB (most significant bit), and for a system of 9 or 10 bits the ladder potentiometer is sufficient. For low resolution systems, add a small resistor (about 16 ohms for an 8-bit system, 32 ohms for 7 bits, etc.) in series with the MSB input. It need not be precise (since the potentiometer will adjust for it) nor have a low temperature coefficient (since a large change in this resistor will have a small effect on the output voltage). Use the standard divider adjustment procedure and look for a straight line instead of a square wave on the most significant bit.

APPENDIX 2

BIPOLAR VOLTAGES

BIPOLAR D TO A OUTPUTS

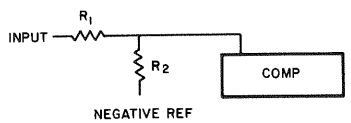
Binary weighted ladder networks made by Digital have an output impedance of 1000 ohms. The external load can reach 2000 ohms without any noticeable effect on the linearity of the system. Thus the output can be made bipolar with a large resistor to a positive bias voltage. The equivalent circuit is shown below.



With a —10 volt reference driving the digital-to-analog converter, the output voltage swing is reduced to $\frac{\pm 5R}{R + 1000}$ volts. The output voltage swing is centered when the bias voltage equals +R/200. The bias voltage, of course, should be stable and noise free.

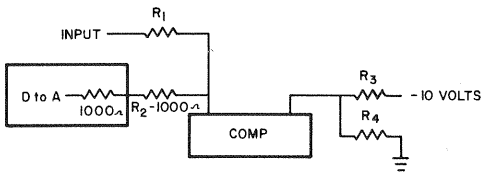
BIPOLAR A TO D INPUTS

If multiplexing is being done or if the input signal cannot drive a heavy load, an amplifier should be used for signal conversion as described in Chapter 5. In other cases, a simple divider can be used in front of the comparator. The basic circuit is shown below.



The impedance level should be kept low since the comparator will draw some current even at balance (a fraction of a microampere). The input, as seen by the comparator, should be as near as possible to the full 0 to —10 volt range.

An alternative to the above scheme is to buck the input against the digital-to-analog converter in the feedback loop, as follows:



The range seen by the comparator is reduced, but common mode effects are avoided since balance is always at the same point. R_2 should be less than 1000 ohms, and R_3 plus R_4 should be about 500 ohms or less.

APPENDIX 3

TABLE OF VOLTAGES

Octal Numbers		Voltage
Signed 2's Comp.	Unsigned	(Negative)
4000	0000	0.
4001	0001	0.00244140625
4002	0002	0.0048828125
4004	0004	0.009765625
4010	0010	0.01953125
4020	0020	0.0390625
4040	0040	0.078125
4100	0100	0.15625
4200	0200	0.3125
4400	0400	0.625
5000	1000	1.25
6000	2000	2.5
0000	4000	5.
2000	6000	7.5
3000	7000	8.75
3400	7400	9.375
3600	7600	9.6875
3700	7700	9.84375
3740	7740	9.921875
3760	7760	9.9609375
3770	7770	9.98046875
3774	7774	9.990234375
3776	7776	9.9951171875
3777	7777	9.99755859375
—	10000	10.

APPENDIX 4

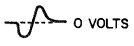
DIGITAL SYMBOLS AND STANDARDS

"DIGITAL STANDARD LEVELS" are 0 and —3 volts. The tolerance on the more positive level is 0 to —0.3 volts. The tolerance on the more negative level is —3 volts to —4 volts.

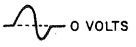
"DIGITAL STANDARD NEGATIVE PULSES" are —2.5 volts in amplitude with a positive overshoot of similar amplitude. These pulses are referenced to ground.

The "DIGITAL STANDARD POSITIVE PULSES" are identical to the Negative Pulses except that the polarity is reversed.

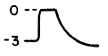
Inverter output pulses are similar to positive logic levels but have a duration equal to pulses.



Standard Negative Pulse



Standard Positive Pulse



Inverter Output Pulse

The timing characteristics of Digital Standard Pulses are commensurate with the speed line. For the 3000 and 4000 Series, pulses have a duration of 0.4 microseconds. For the 100 and 1000 Series, the pulse duration is 70 nanoseconds. For the 5000 and 6000 Series, pulse duration is 40 nanoseconds. A detailed description of the requirements for external input signals which may be used as the equivalent of Digital Standard Pulses is outlined for each series under the pulse amplifier descriptions of that series in the Digital Module Catalog.

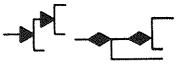
Negative Logic Level

Positive Logic Level

Standard Negative Pulse

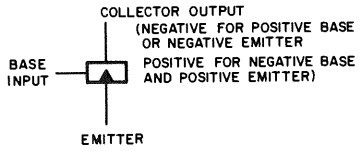
Standard Positive Pulse
or Inverter Output Pulse

Nonstandard Signal

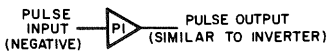


Branch Points

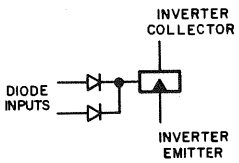
BASIC LOGIC UNITS



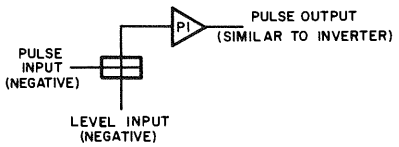
Inverter



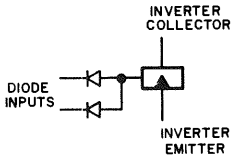
Pulse Inverter



Diode Gate
Negative NAND
Positive NOR

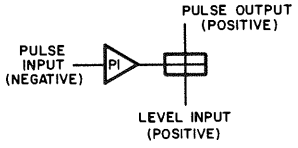


Negative Capacitor Diode Gate

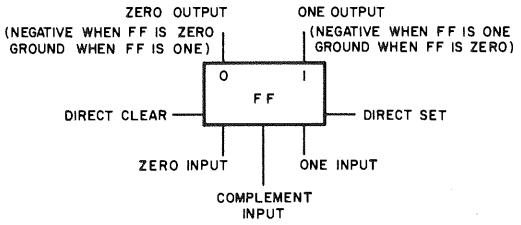


Diode Gate
Negative NOR
Positive NAND

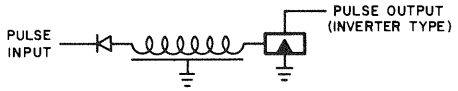
Clamped Load



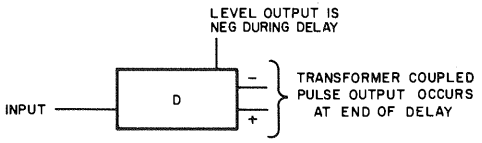
Positive Capacitor Diode Gate



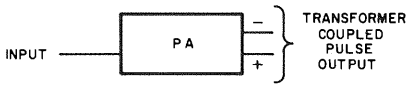
Flip-Flop



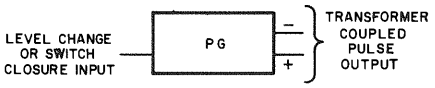
Delay Line



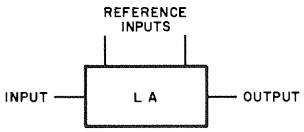
Delay One-Shot



Pulse Amplifier



Pulse Generator

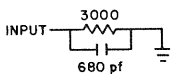


Level Amplifier

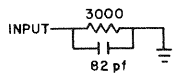
Clock

LOAD DEFINITIONS

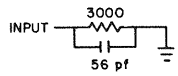
A BASE LOAD is a load to ground. It draws 1 milliampere when the input is at —3 volts and no current when the input is at ground. The transient current depends on the speed line being used. Normally the input circuit can be approximated as follows:



3000 + 4000
Series

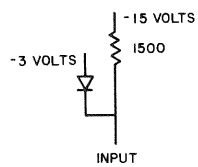


100 + 1000
Series



5000 + 6000
Series

An EMITTER LOAD is a load to a more negative voltage. It draws 10 milliamperes when the input is at ground and no current when the input is at —3 volts. This type of load is normally independent of the speed line.



digital

25028 PRINTED IN U.S.A. 250-7/64