digital
LOGIC HANDBOOK

DEC
FLIP CHIP

THE

digital

LOGIC HANDBOOK
FLIP CHIP™ MODULES
1968 EDITION

PREFACE

GENERAL PURPOSE MODULES

The first section defines the characteristics of the FLIP-CHIP™ line of modules which cover the spectrum of application in five series:

1. The M Series of high-speed TTL monolithic integrated circuit modules
2. The K Series of deliberately slowed and virtually noise-immune modules designed for industrial applications
3. The A Series of analog-to-digital and digital to analog conversion modules
4. The W series modules for interfacing with various types of external equipment
5. The R series which operates from DC to Two Megahertz
6. The B series which operates from DC to Ten Megahertz

In addition to these module lines, a new approach to subsystem design, OCTAIDS and PANELAIDS, are described in detail. These design aids provide the user with a fast, accurate method of assembling such common elements as A to D converters, binary counters, and real time clocks.

ANALOG-DIGITAL CONVERSION

The second section of the Digital Logic Handbook is concerned with Analog-Digital Conversion. A primer on conversion techniques prefaces this section and the complete line of A to D converters follow. The system designer is provided with the necessary information to select either a complete A to D converter or the various analog modules. Application notes are included to further aid in the design of special systems.

HARDWARE

A section which describes Digital's complete line of hardware is included in the Handbook. New in this issue are the 4096 x 13 bit memory and paper tape punch and reader units. All of the hardware necessary for the fabrication of a complete system are included, and each piece of hardware has been field-proven in Digital's PDP series computers.

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Discrete components are positioned and crimped in place at rates up to 30 per minute on pantograph controlled inserting machine.

To insure reliability, a wide variety of dynamic tests are performed on-line by
a computer controlled system.

PART I: DIGITAL LOGIC PRIMER

NUMBER SYSTEMS

Early number systems were crude and awkward to use. A simple system, using a mark for each unit, cannot be used to express large quantities such as a thousand. Later systems, such as Roman numerals, were a great improvement, but still extremely difficult to manipulate in ordinary arithmetic. With the Arabic, or decimal, number system, common arithmetic operations, which correspond to true to life operations, can be defined and easily used.

The decimal number system uses ten symbols representing the quantities 0 through 9. Other numbers are constructed by assigning different values (or weights) to the position of the symbol relative to the decimal point. For example, the number 008 (more commonly written simply 8) represents eight units, while the number 080 (again more commonly written just 80) represents a quantity of eighty, and the number 800 represents a quantity of eight hundred.

Each position in a decimal number has a value which is ten times the value of the next position to the right. In other words, every positional weight is a multiple of ten and can be expressed by ten raised to some power. The tens position is 10^1, the hundreds position is 10^2, the thousands position is 10^3, etc.

Simple exponential arithmetic shows that the ones position is $10^0 = 1$ (in fact, any number raised to the 0 power, except 0, is equal to 1). This progression of increasing exponents can be continued as far as desired to the left of the decimal point. The same progression can also be extended to the right of the decimal point, but here the exponents will be negative. For example, the first position to the right of the decimal point is the tenths position, it has a weight of 10^{-1} or $1/10^1$.

Figure 1 represents a general skeleton for any decimal number. The symbol which is placed in any of the positions indicates how many multiples of that power of 10 are in the total quantity represented by the number.

10^N		10^3	10^2	10^1	10^0	•	10^{-1}	10^{-2}	10^{-3}		10^{-N}
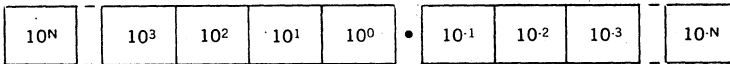
Figure 1

Ten is not a particularly magical number; there is no reason for the number of symbols to be extended to ten (or limited to ten). It would be just as simple to have twelve symbols or eight symbols or two symbols, or any other number of symbols. However, one of the features of the decimal system is that there is only one way in which any given number can be written, and on seeing a number written, there is only one value which can be ascribed to it. In order to keep this feature in a number system with a different number of symbols, it is necessary to change the weights of the different positions. The values which must be assigned, in fact, turn out to be powers of the

number of symbols available. The number of symbols used is called the radix of the number system. Figure 2 shows the skeleton of a general number system with a radix R.

| R^N | | R^3 | R^2 | R^1 | R^0 | • | R^{-1} | R^{-2} | R^{-3} | | R^{-N} |
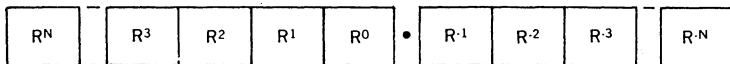
Figure 2

Examples of counting in different number systems are illustrated in Figure 3. The duodecimal number system has a radix of 12 and the symbols A and B are used here to represent the quantities 10 and 11, respectively. The octal number system has a radix of 8 and the binary number system has a radix of 2. The positional weights are given in decimal at the top of each column.

COUNTING IN DIFFERENT NUMBER SYSTEMS

DECIMAL		DUODECIMAL		OCTAL		BINARY				
tens	ones	twelves	ones	eights	ones	sixteens	eights	fours	twos	ones
	0		0		0					0
	1		1		1					1
	2		2		2				1	0
	3		3		3				1	1
	4		4		4			1	0	0
	5		5		5			1	0	1
	6		6		6			1	1	0
	7		7		7			1	1	1
	8		8	1	0		1	0	0	0
	9		9	1	1		1	0	0	1
1	0		A	1	2		1	0	1	0
1	1		B	1	3		1	0	1	1
1	2	1	0	1	4		1	1	0	0
1	3	1	1	1	5		1	1	0	1
1	4	1	2	1	6		1	1	1	0
1	5	1	3	1	7		1	1	1	1
1	6	1	4	2	0	1	0	0	0	0
1	7	1	5	2	1	1	0	0	0	1
1	8	1	6	2	2	1	0	0	1	0
1	9	1	7	2	3	1	0	0	1	1
2	0	1	8	2	4	1	0	1	0	0
2	1	1	9	2	5	1	0	1	0	1
2	2	1	A	2	6	1	0	1	1	0
2	3	1	B	2	7	1	0	1	1	1
2	4	2	0	3	0	1	1	0	0	0

Figure 3

3

BINARY NUMBER SYSTEM

Since the binary number system uses two symbols, it has a radix of 2 and the positional weights are powers of 2. Examination of the binary counting sequence, Figure 3, shows that the binary number system follows the same number system skeleton which was previously outlined. Because of this, the method of performing arithmetic operations in binary numbers is the same as the methods used for decimal numbers. For example, $0 + 0 = 0$, and $0 + 1 = 1$. Since there is no symbol for two, however, $1 + 1 = 0$ and 1 to carry. The tables for performing arithmetic operations are given in Figure 4. Since there are only two symbols, the tables are considerably simpler than those required to outline the same operations in the decimal number system. This, of course, leads to considerably simpler computer circuitry also. Some typical examples of arithmetic operations in binary are shown in Figure 5.

Binary Addition

$A + B = S$ (Sum)
$0 + 0 = 0$
$0 + 1 = 1$
$1 + 0 = 1$
$1 + 1 = 0$ & 1 to carry

Binary Subtraction

$A - B = D$ (Difference)
$0 - 0 = 0$
$0 - 1 = 1$ & 1 to borrow
$1 - 0 = 1$
$1 - 1 = 0$

Binary Multiplication

$A \times B = P$ (Product)
$0 \times 0 = 0$
$0 \times 1 = 0$
$1 \times 0 = 0$
$1 \times 1 = 1$

Binary Division

$A \div B = Q$ (Quotient)
$0 \div 0 = ?$
$0 \div 1 = 0$
$1 \div 0 = ?$
$1 \div 1 = 1$

Figure 4

Addition

```
 1
  101101        101101
+  1010        + 1100
 110111        111001
```

Subtraction

```
  101101        101101
 - 1100          11001
  100001         10100
```

Multiplication

```
    101101
  ×   101
    101101
   00000
  101101
  11100001
```

Division

```
              1001
    101 √101101
           101
           0001
           0000
             10
             00
            101
            101
```

Figure 5

4

BINARY-DECIMAL CONVERSION

Numbers can be converted from binary to decimal and vice versa by hand by using the methods outlined in Figure 6. As shown, a binary number is converted to decimal simply by adding the positional weights of all those positions where a 1 appears. Decimal to binary conversion is more a process of trial and error. First, subtract the largest power of 2 which will go into the number that is being converted. This process is repeated on the remainder until the remainder is equal to 0. The binary number then has ones in those positions with the values corresponding to the powers of 2 which were subtracted; all other positions are 0.

BINARY TO DECIMAL CONVERSION

32	16	8	4	2	1		
1	0	1	1	0	1	= 32 + 8 + 4 + 1 = 45	
		1	0	1	0	= 8 + 2 = 10	
1	1	0	1	1	1	= 32 + 16 + 4 + 2 + 1 = 55	

DECIMAL BINARY CONVERSION

```
              32  16  8  4  2  1
  45
 -32 ───────→  1   0  1  1  0  1
  13
 - 8
   5
 - 4
   1
 - 1
   0
```

Figure 6

BINARY-CODED-DECIMAL NUMBERS

Since computer inputs and outputs must often be in decimal notation, a variety of special codes are used. These hybrid number systems are referred to as binary-coded-decimal or BCD.

An example of BCD is the 8421 code. This is often referred to as simply BCD since the weights of the positions are the same as in the binary number system, as illustrated below.

Decimal	8421 Code
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

The 8421 code employs four bits to represent each decimal digit. For instance, the number 987 may be represented by the 12-bit number 1001 1000 0111. Although this number contains only ones and zeros, it is not a true binary number since it does not follow the rules previously established. Arithmetic operations with BCD would be quite involved. However, it is relatively easy for the computer to convert to true binary, perform the necessary calculations, and reconvert to BCD.

BCD numbers do not always follow the pure binary number system. Special purpose number systems such as Excess Three Code, Gray Code, and Biquinary Code are often used.

OCTAL NUMBER SYSTEM

As the name implies, the octal number system has a radix of 8, i.e., it uses eight discreet symbols: 0, 1, 2, 3, 4, 5, 6, and 7. The positional weights in the octal number system are powers of 8.

The octal number system is widely used by digital engineers and computer programmers since it can easily be converted to binary. At the same time, it is considerably easier to work with, or to record, octal numbers than to use a long string of binary zeros and ones.

The binary-octal conversion may be performed quite simply due to the fact that 8 is the third power of 2. This produces a direct correlation between the successive 3-bit groups in a binary number and the octal digits. That is, an octal number may be converted to binary digit by digit, while with a decimal number the entire number must be converted to binary. The table for octal to binary conversion is shown in Figure 7.

OCTAL TO BINARY CONVERSION

Octal	Binary
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Figure 7

Using this table, the octal number 777, for example, could be easily and directly converted to the binary number 111111111. Going in the opposite direction, the binary number 110101110 can be converted directly to 656. (As in other number systems, zeros are always assumed in the most significant bits. For example, the number 1110110 converts to 166 in octal.)

Arithmetic operations in octal are quite similar to the operations in decimal. A more detailed discussion of this can be found in some of the reference books in the bibliography.

NOTATION

When there may be some doubt as to the number system being employed, it is customary to indicate this by writing the radix of the number system (in decimal) as a subscript to the number. For example, 777_8 indicates that this is the number 777 written in the octal number system. The same number in the decimal system would be 511_{10}.

In working with different number systems it is extremely important to be certain which system is being used. For example, take that tricky little question, "what's two and two?"

$$2 + 2 = \text{(meaningless for radix of 2)}$$

$$2 + 2 = 11_3$$

$$2 + 2 = 10_4$$

$$2 + 2 = 4_5 \text{ or more.}$$

BOOLEAN ALGEBRA

Boolean algebra was introduced in 1847 by an English mathematician, George Boole. The purpose of the algebra was to find a shorthand notation for the system of logic originally set forth by Aristotle. Aristotle's system dealt with statements which were considered to be either true or false, but never partially true or false. Boole's algebra was based on a single valued function with two discrete possible states.

Boolean algebra lay almost dormant until recent times. Today, however, it is gaining widespread recognition as an efficient method for handling any single valued function with only two possible states. When it is applied to binary arithmetic, the two states are 0 and 1. When discussing a switch, the two values are open and closed.
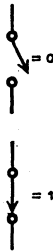
Figure 8   Switch Analogy

The convention used will be that the open state corresponds to the 0 state, while the closed state corresponds to the 1 state.

OR FUNCTION

A + B = C
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 1
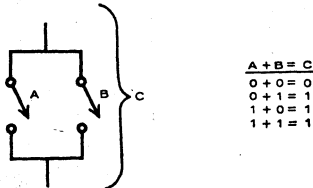
Figure 9   OR Function

If two switches, A and B, are connected in parallel to form a gate, inspection shows that the gate can only transmit information if A or B or both are in the transmitting state,

8

i.e., closed. This is written in equation form as

$$A + B = C$$

$$(A \text{ or } B \text{ equals } C)$$

Figure 2 shows the parallel combination of two switches along with a table giving the value of C for all possible values of A and B.

(A+B)+C   =   A+(B+C)   =   A+B+C
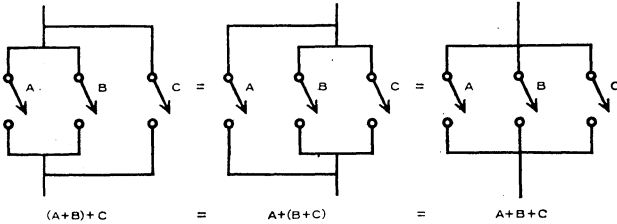
Figure 10   Compound OR Functions

By adding a third gate in parallel, as in Figure 10 it becomes obvious how the OR function may be extended to any number of variables. This figure also serves to illustrate that the communicative and associative laws are valid for the OR function, i.e.,

$$A + B = B + A$$

$$(A + B) + C \equiv A + (B + C) \equiv A + B + C$$

AND FUNCTION

A B = C
0 0 = 0
0 1 = 0
1 0 = 0
1 1 = 1
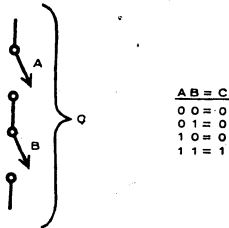
Figure 11   AND Function

If two or more gates are placed in series, the result is known as an AND gate. Inspection of the arrangement in Figure 11 shows that the resulting gate will transmit only if both A and B are closed, i.e., equal to 1. The equivalent equation in Boolean form is

$$AB = C$$

$$(A \text{ and } B \text{ equals } C)$$

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A(BC) ≡ ABC ≡ CBA
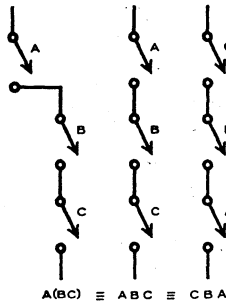
Figure 12 Compound AND Functions

Figure 12 demonstrates how the AND function is applied to more than one variable. The commutative and associative laws also hold.

$$AB = BA$$

$$A(BC) \equiv (AB)C \equiv ABC$$

IDENTITIES

1+A≡1   0+A=A   1A=A   0A=0

A(B+C)   =   AB+AC

Figure 13 Indentities

10
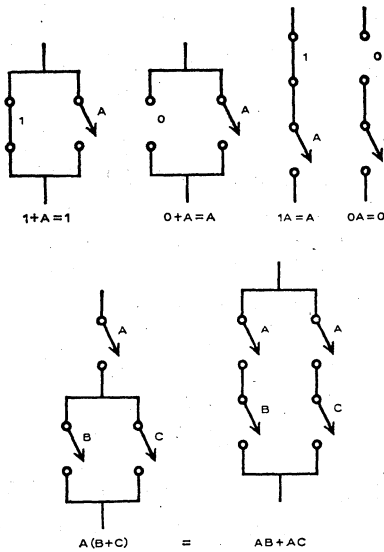
To enable the simplification of Boolean functions, there are many identities which are helpful. In Figure 13 the combination of switches and corresponding equations demonstrate these identities.

COMPLEMENT

If two gates are connected so that the same signal will open both of them or close both of them simultaneously, the switches are given the same symbol. If two gates are connected so that a single signal will open one gate while closing the other gate, and vice versa, these gates are said to be the complement of each other. Thus, if one gate is labeled A, the other gate will be labeled $\overline{A}$ (read "not A" or "A not").

An entire function may also be complemented. For example,

if
$$D = A(B + C)$$

then
$$\overline{D} = \overline{A(B + C)}$$

The use of one label for more than one gate makes the following identities helpful:

$$A + A = A \qquad\qquad A + \overline{A} = 1 \qquad\qquad \overline{\overline{A}} = A$$
$$AA = A \qquad\qquad A\overline{A} = 0$$

DE MORGAN'S LAWS

Two unique laws which can be applied only to Boolean algebra are known as De Morgan's laws.

$$\overline{A + B + C + \ldots + N} = \overline{A}\overline{B}\overline{C} \ldots \overline{N}$$
$$\overline{ABC \ldots N} = \overline{A} + \overline{B} + \overline{C} \ldots + \overline{N}$$

These laws may be verified by constructing a table of various possible values.

BOOLEAN ALGEBRA FOR USE WITH VOLTAGE LEVELS

Since DEC voltage levels have only two possible values, Boolean algebra can also be useful in the study of these levels.

Diode-Capacitor-Diode Gate	Clamped Load
Inverter	Diode Gate Negative NAND Positive NOR

OUTPUT
PULSE INPUT
LEVEL INPUT

COLLECTOR OUTPUT
(NEGATIVE FOR POSITIVE BASE
OR NEGATIVE EMITTER
POSITIVE FOR NEGATIVE BASE
AND POSITIVE EMITTER)
BASE INPUT
EMITTER

COLLECTOR
DIODE INPUTS
EMITTER
NODE INPUT

ZERO OUTPUT
(NEGATIVE WHEN FF IS ZERO
GROUND WHEN FF IS ONE)
ONE OUTPUT
(NEGATIVE WHEN FF IS ONE
GROUND WHEN FF IS ZERO)
DIRECT CLEAR
DIRECT SET
ZERO INPUT
ONE INPUT
O   1   F F

Flip-Flop

LEVEL OUTPUT IS
NEG DURING DELAY
INPUT
D

Delay
(One-Shot)

INPUT
OUTPUT

General Element

Device Symbols

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Figure 15   Inverter

An inverter or single input diode gate may be used to perform a complement. If the emitter is at ground and a signal is applied to the base, the resulting output is the complement of the base input as shown in Figure 15.

NEGATIVE AND GATE
ABCDEF = G
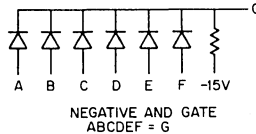
Figure 16   Diode AND Gate

R, B, and W Series Standard levels are defined as −3 volts = 1, and 0 volts = 0, hence a simple AND gate is formed by diodes shown in Figure 16. Only if A and B and C and D and E and F are negative will the resulting output G be negative.

Inspection of these diode units shows that the AND gate becomes an OR gate if the levels are defined in the opposite manner; i.e., if ground is defined as a 1 and −3 volts is defined as a 0. This is a demonstration of De Morgan's law.

The use of symbols for signal definitions helps the designer keep track of these definitions if he wants to change conventions in a system. The symbols used are shown in Figure 17. Figure 18 shows the basic diode gate with its corresponding negative and positive logic. definitions.
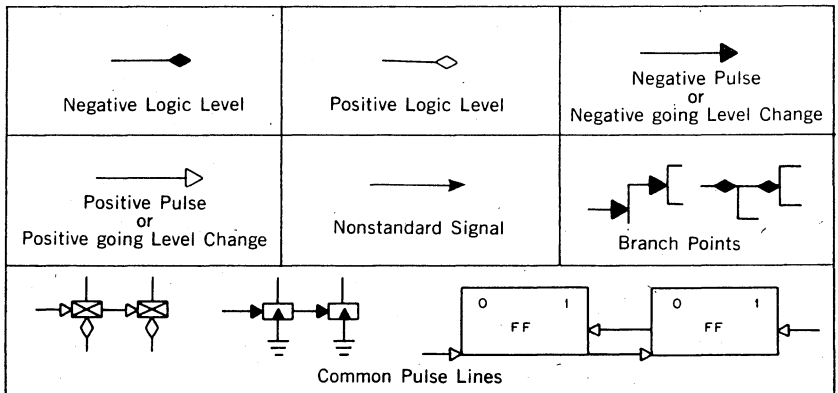
Figure 17 Symbols for Standard Signals

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$$C = \overline{A \cdot B} = (\overline{A} + \overline{B})$$

NEGATIVE NAND

$$C = \overline{A + B} = (\overline{A} \cdot \overline{B})$$

POSITIVE NOR
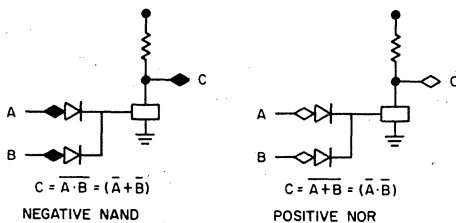
Figure 18   Diode Gate Definitions

Regardless of level convention chosen, there is only one unique state which indicates coincidence of inputs for the diode gate shown. That is, if, and only if both inputs are —3 volts, the output will be at ground. This means that in a decoding situation, the only active decoder output is ground in either definition of logic levels.

The circuit design is such that a number of gates may be connected together at a common point to produce a positive OR function. In Figure 19, if either gate output goes to ground, the output of the logic will be ground. Thus a convenient function is derived.

$$F = \overline{AB + CD} = (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})$$

NEGATIVE DEFINITION

$$F = \overline{(A + B)(C + D)} = \overline{A}\,\overline{B} + \overline{C}\,\overline{D}$$

POSITIVE DEFINITION
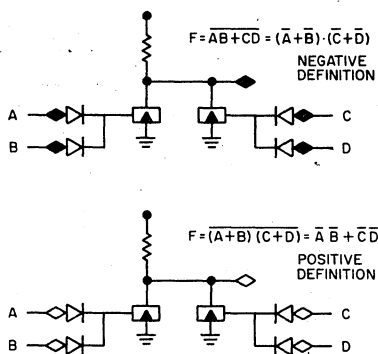
Figure 19   OR Gate Definitions

The DCD gate performs a positive AND function. If the DCD gate could be used as a separate logic element (not in conjunction with pulse amplifiers or flip-flops) its positive and negative definitions would be as shown in Figure 20.
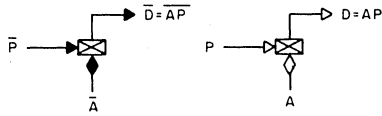
Figure 20   DCD Gate Definitions

When DCD gates are used in conjunction with an R602 Pulse Amplifier, for example, the functions of the combined elements are defined as shown in Figure 21.
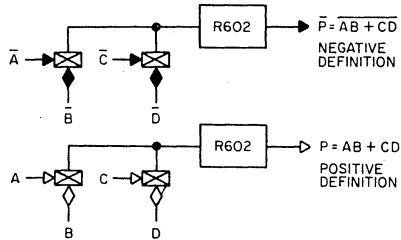
Figure 21   Definitions, DCD Gates with Pulse Amplifier

BINARY-CODED DECIMAL CODES

The digital computer can be thought of as an assemblage of two-state devices because it manipulates the ones and zeros of the binary number system. People, on the other hand, are more accustomed to decimal numbers, and for this reason it is often desirable to build a computing system which can be operated in decimal.

To build a decimal computer with two-state devices, it is necessary to encode the decimal digits with binary bits. Four binary bits are needed. Although only 10 of the 16 permutations possible with the 4-bit decade will be used, all are available. The number of codes that can be generated is calculated as follows:

$$\frac{16!}{6!} \simeq 2.9 \times 10^{10}$$

The choice of a code is obviously important. Desirable features of the code are: ease in performing arithmetic operation, economy of storage space, economy of gating operations, error detection and correction, and simplicity. Several possible codes are shown below, followed by a detailed explanation of arithmetic operations using two especially convenient codes, the 8 4 2 1 and the Excess 3.

FOUR-BIT CODES

The 8 4 2 1 code is commonly referred to simply as binary-coded decimal because the weights of the positions are the same as in the binary number system. Arithmetic operations are easily performed using the same basic method as in binary since the number sequence is the same.

In the Excess 3 code, a decimal number D is represented by the binary equivalent of the number D + 3. The Excess 3 code is not a weighted code, but since it follows the same number sequence as binary, it is useful in arithmetic operations. Addition is facilitated since the need for a correction factor is easily detected and easily implemented. Because it is self-complementing, the Excess 3 code is also useful in subtraction.

The 2 4 2 1 is a self-complementing weighted code which is commonly employed in counting systems. Other examples of four-bit weighted codes include the 5 4 2 1, the 5 3 1 1, and the 7 4 −2 −1 code. All of these codes are shown in Figure 22 .

More than four bits may be used in each decade to provide additional special features such as the detection of errors and the simplification of decoding.

DECIMAL	8421	Excess 3	2421
0	0000	0011	0000
1	0001	0100	0001
2	0010	0101	0010
3	0011	0110	0011
4	0100	0111	0100
5	0101	1000	1011
6	0110	1001	1100
7	0111	1010	1101
8	1000	1011	1110
9	1001	1100	1111

DECIMAL	5421	5311	7421
0	0000	0000	0000
1	0001	0001	0111
2	0010	0011	0110
3	0011	0100	0101
4	0100	0101	0100
5	1000	1000	1010
6	1001	1001	1001
7	1010	1011	1000
8	1011	1100	1111
9	1100	1101	1110

Figure 22 Four-bit decimal codes

ARITHMETIC OPERATIONS WITH THE 8 4 2 1 OR EXCESS 3 CODES

Because the 8 4 2 1 and the Excess 3 codes follow the same number sequence as the binary number system, standard binary methods may be used. However, in binary notation sixteen states are represented with four bits. In binary-coded decimal only ten of these states are used; therefore, special correction factors must be added to account for the six unused states.

Counting

In a binary-coded decimal (BCD) counter, the corrective action is very simple. The counter is divided into four-bit decades, and special gating is added to each decade. This gating detects the number 9 and reroutes the next count pulse so that it will reset the decade to 0 and generate a carry to the next decade.

In a down counter, the same approach is used. Starting with a standard binary down counter, the number 0 is detected, and the next count input resets the counter to the appropriate 9 designation and produces a borrow.

A reversible BCD counter may be implemented by combining the techniques for the individual up and down counters. Such a counter, however, is more difficult to construct than a single direction counter since provision must be made for isolating the carry and borrow chains and for assuring that count up and count down signals do not occur simultaneously.

Addition

A common method of performing BCD addition is to add two numbers in the binary adder and, if necessary, add or subtract an appropriate correction factor (see Figure A19). When addition is to be performed in a decade by decade fashion (serial addition with parallel decades), either code is useful. If addition is performed in parallel, however, the Excess 3 code is superior to the 8 4 2 1 code.

In 8 4 2 1 code the sum will be correct if it does not exceed 9. If the decimal sum is between 10 and 15, it is necessary to add +6 to the binary sum and generate a carry to the next decade. If the decimal sum exceeds 15, a carry signal is generated by the initial addition, but the correction factor +6 must still be added to the binary sum.

Addition of 8 4 2 1 coded numbers has the disadvantage that a carry signal can be generated during the correction process. For this reason each decade in the adder has to be corrected individually. Therefore it is not a desirable code in a parallel adder (see Figure 23).

No correction necessary
(Sum ≤ 9)

0100 = 4 dec.
0011 = 3 dec.
0111 = 7 dec.

Initial sum in forbidden state
(10 ≤ sum ≤ 15)

1000 = 8 dec.
0100 = 4 dec.
1100 = forbidden state
0110 = correction factor of +6
1 ◄— 0010 = 2 dec. plus carry   —

Initial sum in incorrect notation
(16 ≤ sum ≤ 18)

1001 = 9 dec.
1000 = 8 dec.
1 ◄— 0001 = 1 plus carry
0110 = correction factor of +6
0111 = 7 dec. (plus carry from first addition)

Multiple decade addition

```
0101  0101  1000     = 558 dec.
0010  0100  0011     = 243 dec.
0111  1001  1011
              + 0110  ⎫
        1 ◄ 0001      ⎪
         1010         ⎪
         0110         ⎬ = 801 dec.
  1 ◄ 0000            ⎪
1000                  ⎭
```

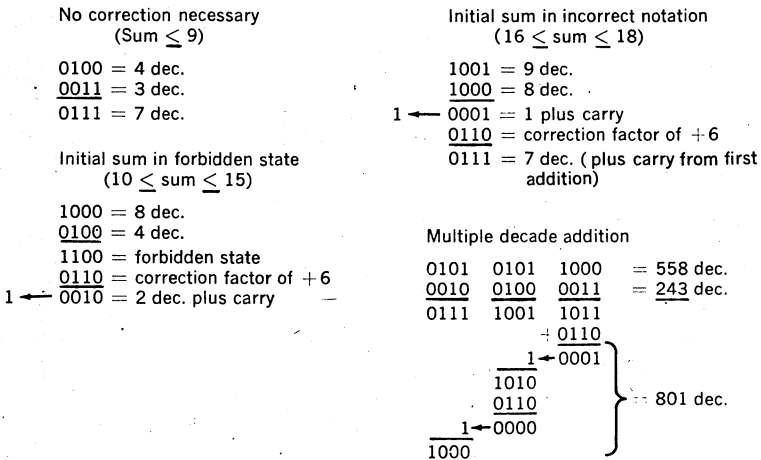Figure 23 Addition with the 8 4 2 1 code

When two Excess 3 numbers are added, the sum will contain an excess 6; if the decimal sum is 9 or less, it is necessary to subtract 3 in order to return to Excess 3 notation; if the decimal sum is greater than 9, the excess 6 contained in the sum cancels the effect of the six unused binary states, but it is necessary to add 3 to return to the Excess 3 notation.

Whether the correction factor is +3 or −3 is determined by whether or not a carry signal appears during the initial addition. An initial carry requires a positive correction; no carry, a negative correction. The correction process will never yield an additional carry, thus simultaneous correction of all decades is possible.

The steps for performing Excess 3 addition are:

1. Add the two BCD numbers in binary fashion

2. Check each decade for a carry signal

3. Subtract 3 from each decade in which a carry has not occurred, while simultaneously adding 3 to each decade in which the carry signal has occurred.

The +3 correction is made by adding 0011 to the appropriate decade. Subtracting 3 from a decade is done by adding 1100 and using the end around carry from the most significant bit of the decade. This is a method of 9's complement subtraction, described under subtraction below.

Sum ≤ 9		Sum ≥ 10	
0111	= 4 dec.	1011	= 8 dec.
0110	= 3 dec.	0111	= 4 dec.
1101	= uncorrected sum	1 ← 0010	= uncorrected sum
−0011	= correction factor of −3	0011	= correction factor of + 3
1010	= 7 dec.	0101	= 2 dec., plus carry from initial addition

Multiple Decade Addition

1000	1000	1011		558 dec.
0101	0111	0110	=	243 dec.
1110 ←	0000 ←	0001		
−0011	+0011	+0011		
1011	0011	0100	=	801 dec.

Figure 24 Addition with the Excess 3 code

Subtraction

Since subtraction is the inverse of addition, the same circuits may be used for both operations. Subtractions by this process is known as the system of adding complements. The 9's complement of any number is that number which is obtained by subtracting each individual digit from 9. With a self-complementing BCD code, such as Excess 3, the 9's complement of any number can be easily obtained by changing all zeros to ones and all ones to zeros. Figure 25 illustrates Excess 3 code with 9's complement notation.

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DECIMAL		EQUIVALENT CODE	
	sign	tens decade	ones decade
+99	0	1100	1100
+98	0	1100	1011
+10	0	0100	0011
+3	0	0011	0110
+2	0	0011	0101
+1	0	0011	0100
+0	0	0011	0011
−0	1	1100	1100
−1	1	1100	1011
−2	1	1100	1010
−3	1	1100	1001
−10	1	1011	1100
−98	1	0011	0100
−99	1	0011	0011

Figure 25 Nines complement, Excess 3 code

To subtract with Excess 3, 9's complement code, the subtrahend is first complemented then added to the minuend. During the first step of the addition process the individual bits (in the decimal decades and in the sign bits) are added just as in binary. Carries propagate from each digit to the digit of more significance and from the most significant digit to the sign bit. If the sign bit produces a carry, it is added to the least significant decade, a process known as end around carry.

```
0        1000     0100     51 dec.                        +51 dec.
1        1001     1000     (complement of 34 dec.)        −34 dec.
0  ←──── 0001     1100
                    →1     end around carry

0        0001     1101
         0011     1100     correction factor
         0100   ⌐ 1001
                    →1     end around carry

0        0100     1010     17 dec.                        +17 dec.
```

```
0        0110     0111     34 dec.                        +34 dec.
1        0111     1011     (complement of 51 dec.)        −51 dec.
1        1110  ←── 0010
         1100     0011     correction factor
       ⌐ 1010     0101
          →1              end around carry

1        1011     0101     −17 dec.                       −17 dec.
```

Figure 26 Subtraction with the Excess 3 code, 9's complement notation

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After this initial portion of the subtraction, a correction factor must be applied just as in addition. That is, a binary 3 (0011) must be added to each decade in which a carry signal has occurred, and binary 3 must be subtracted from each decade in which a carry signal did not occur.

Subtraction of the correction factor may be performed in the same way as well as the overall subtraction. However, the subtraction in this case operates only on the individual digits. Thus, if a carry occurs from the most significant bit of the digit, it is not carried out to the next digit; rather, it is added into the least significant bit of the same digit.

A second method of performing subtraction is through the use of the 10's complement notation. The 10's complement of any number may be obtained by adding 1 to the 9's complement. Operations are similar to those used in the 9's complement notation except that the end around carry is not required. Hence this is useful in systems where a feed back loop would be particularly time consuming.

CODES GREATER THAN FOUR BITS

DECIMAL	BIQUINARY							RING COUNTER CODE									
	5,	0	4,	3,	2,	1,	0	9,	8,	7,	6,	5,	4,	3,	2,	1,	0
0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
2	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0
3	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0
4	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
5	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
6	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0
7	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
8	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
9	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0

DECIMAL	SWITCH TAIL RING COUNTER CODE					DECODING	
	A	B	C	D	E		
0	0	0	0	0	0	A	E
1	0	0	0	0	1	D	E
2	0	0	0	1	1	C	D
3	0	0	1	1	1	B	C
4	0	1	1	1	1	A	B
5	1	1	1	1	1	A	E
6	1	1	1	1	0	D	E
7	1	1	1	0	0	C	D
8	1	1	0	0	0	B	C
9	1	0	0	0	0	A	B

Figure 27 Codes greater than four bits

Codes greater than four bits are often used for error detection and simplicity in decoding (Figure 27). The biquinary code is commonly used when error detection is required. It is a 7-bit weighted code in which two ones and five zeros appear in the representation of any number; thus it is always possible to detect single errors, and it is often possible to detect multiple errors.

The ten-bit weighted code shown in Figure 27 allows any number to be represented with a single 1 and nine zeros. This code is often used in counting operations; the counter is a ten-stage shift register with the final stage connected to the initial stage. This counter, often given the name of ring counter, requires no carrying propagate time and the numbers may be decoded into ten lines without additional gates.

The switch-tail ring counter is a five-stage ring counter with reversed feed-back from the initial stage to the final stage. It requires fewer flip-flops than the ring counter and has the same advantage that no carry propagate time is required. Any state may be decoded by a two-input gate conditioned by two neighboring flip-flops.

PART II: FLIP CHIP MODULES

M
SERIES

INTRODUCTION

The development of monolithic integrated circuits has had an impact on the design of digital module systems. Advantages of small size and high operating speeds made these circuits initially attractive. However, a lower price/performance ratio compared to hybrid or discrete component modules offset the advantages. Recently, significant price reductions in both TTL (transistor-transistor logic) and DTL (diode-transistor logic) integrated circuits indicated a re-evaluation was needed.

DIGITAL EQUIPMENT CORPORATION undertook a study of both types of logic, their performance in large and small systems, and their ease of use in system design. The result of this study is the M Series Integrated Circuit FLIP-CHIP™ Module.

M Series modules contain high speed TTL logic in both general purpose and functional logic arrays. TTL was chosen for its high speed, capacitance drive capability, high noise immunity and choice of logical elements. High performance integrated circuit modules are now available at approximately one-half the price of their discrete or hybrid counterparts.

In addition to the reduced cost of integrated circuits, Digital's advanced manufacturing methods and computer controlled module testing have resulted in considerable production cost savings, reflected in the low price of all M Series Modules.

BASIC CIRCUITS

M Series high-speed, monolithic integrated circuit logic modules employ TTL (transistor-transistor logic) integrated circuits for high speed, high fan out, large capacitance drive capability, excellent noise margins, and a superior power-speed characteristic. M Series includes a full digital system complement of basic modules, designed with sufficient margins for reliable system operation at frequencies up to 6 MHz. Specific modules may be operated at frequencies up to 10 MHz.

All integrated circuits are in 14-lead, dual in-line packages. The printed circuit boards used are identical in size to standard FLIP-CHIP™ modules, except that the M Series module uses a double-sided printed-circuit board with 36 pins instead of 18. 36-pin sockets (H803) and mounting panels (H910 and H911) are available for use with M Series modules. For additional information about applicable hardware, see the hardware section of this handbook.

M Series modules are fully compatible with K Series and, through the use of level converters, are compatible with all of Digital's other standard FLIP CHIP™ modules.

OPERATING CHARACTERISTICS

Speed: M Series monolithic integrated circuit modules are conservatively rated for operation in a system environment at frequencies up to 6 MHz. Specific modules may be operated at higher frequencies. (See the individual module specifications).

Logic Levels: Logic 1 or High (H):   +2.4 to +3.6 volts

Logic 0 or Low (L):   0 to + 0.4 volts

This catalog assumes positive logic purely for the purpose of description.

Input and Output Loading: In order to simplify system design using M Series modules, input loading and output drive capability are specified in terms of a unit load. In the logic 0 state, one unit load causes the driver to draw 1.6 milliamps (maximum) from the load's input circuit. In the logic 1 state, the driver supplies only a leakage current of approximately .40 microamps.

Input loading is typically one or two unit loads per input. (See the individual module specifications).

Output drive capability is 10 unit loads per module, unless otherwise specified.

Noise Immunity: Typical DC noise margin is 1 volt at either the logic 1 or logic 0 level. Absolute worst case noise margin is 400 millivolts at either level.

Timing: M Series pulse sources provide sufficient pulse duration to trigger any M Series flip-flop operating within maximum propagation delay specifications. Detailed timing information appears later in this manual.

Power Supply Voltage: 5 volts ± 5%

Operating Temperature Range: 0° to 70°C

TTL NAND GATE

The basic gate of the M Series is a TTL NAND gate. Operation of the TTL gate is similar in many respects to the familiar DTL (diode-transistor logic) NAND gate. The two circuits are compared in Figure 1.
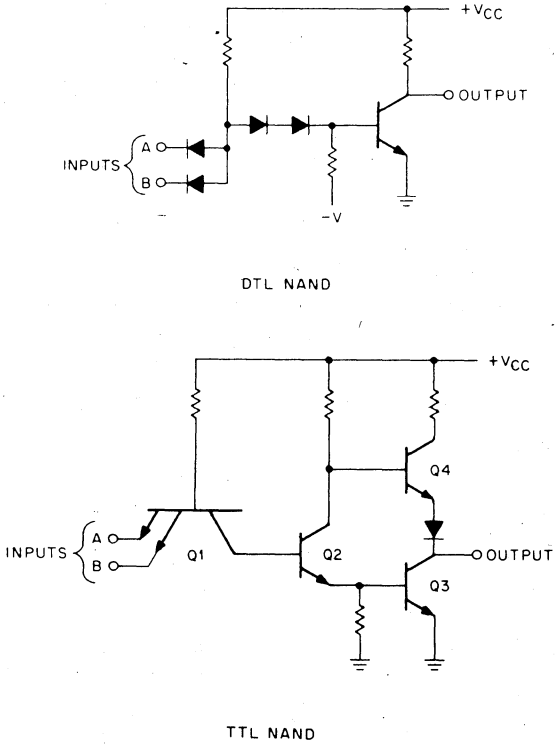

DTL NAND

TTL NAND

Figure 1. Schematic Comparison of DTL and TTL NAND gates

Both approaches provide the NAND function, in which the output, C, is low when both inputs (A and B) are high.

Logic Levels: Operating from a power supply voltage of $+5$ vdc $\pm 5\%$, the TTL NAND gate develops the following nominal logic levels at the loading extremes:

Logic Level	Voltage, No Load	Voltage, Full Load
1 (High) (H)	$+3.6$	$+2.4$
0 (Low) (L)	0.1	$+0.4$

Circuit Operation: The input element of the TTL gate is a multiple-emitter transistor which performs the same basic function as the input diodes of the DTL gate. When both inputs are high, the collector of transistor Q1 is high, turning on the phase-splitter, Q2. The phase-splitter turns on output switching transistor Q3, which permits the flow of load current. During the power driving state, the output is clamped near ground potential. Transistor Q4 is turned off during this state and is effectively out of the circuit.

When either of the inputs returns to the low level, the collector of the input transistor goes low, turning off the phase-splitter. The output transistor, Q3, is turned off, ending the load current drain, and transistor Q4 is turned on to return the output line rapidly toward Vcc. Leakage current through the emitter of the driven gate is supplied by Q4 during the off state.

A number of advantages inherent in the TTL circuit provides superior speed, high capacitance drive, and noise rejection. The multiple-emitter transistor is fabricated on less area than the corresponding diodes, resulting in lower capacitance and higher speed.

Output recovery time is speeded by the "totem pole" output circuit, which provides a practical output impedance of about 100 ohms compared to the typical DTL "pullup" resistor of 4 to 6 K ohms. This feature significantly reduces noise pickup through capacitive or inductive coupling.

NAND Logic Symbol: Logic symbology used to describe M Series modules is based on widely accepted standards. Logic symbols and a truth table for the NAND gate are shown in Figure 2.

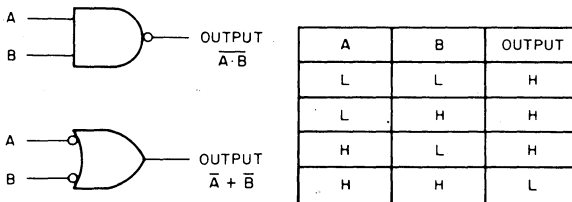| A	B	OUTPUT
L	L	H
L	H	H
H	L	H
H	H	L

Figure 2. NAND Gate Logic Symbol and Truth Table

The first symbol is visually more effective in applications where two high inputs are ANDed to produce a low output. The second symbol better represents an application where low inputs are ORed to produce a high output.

TTL AND/NOR GATE

With a few modifications, the basic TTL NAND gate can perform an AND/NOR function useful in exclusive OR, coincidence, line selection and NOR gating operations. The modified circuit is shown in simplified form in Figure 3.
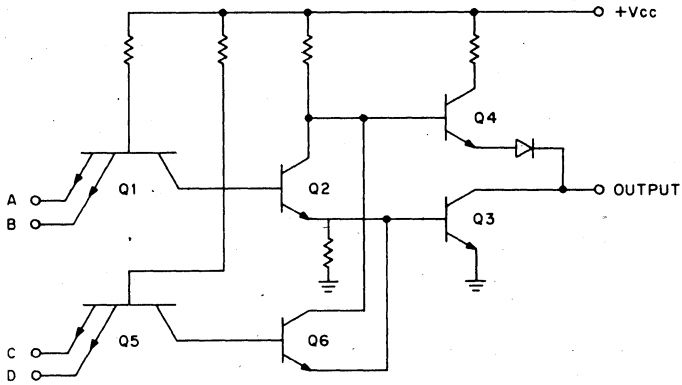
Figure 3. TTL AND/NOR Gate Simplified Schematic

Circuit Operation: The basic elements of the TTL NAND gate are used without modification. The phase-splitter (Q2) is paralleled with an identical transistor (Q6), also controlled by multiple-emitter input transistor which receives two additional inputs, C and D. When either of the input pairs are high, the phase inverter operates to switch the output voltage low. Circuit performance is essentially identical to the TTL NAND circuit.

AND/NOR Logic Symbol: The logic symbols for the AND/NOR gate are shown and defined in Figure 4.
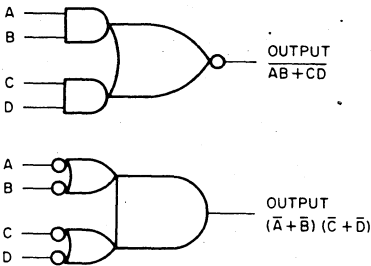
A	B	C	D	OUTPUT
H	H	ANY		L
ANY		H	H	
L	H	L	H	
L	H	H	L	H
H	L	H	L	
H	L	L	H	

Figure 4. AND/NOR Gate Logic Symbols and Truth Table

NOR Configuration: The AND/NOR gate can perform a straight NOR function if the AND gate inputs are tied together as shown in Figure 5:

AND/NOR INPUTS TIED   RESULTING NOR SYMBOL
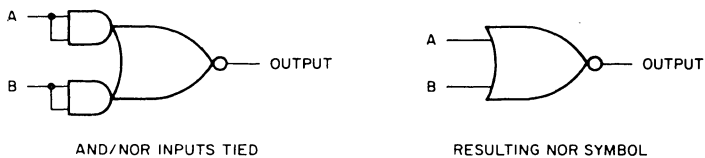
Figure 5. NOR Connection of AND/NOR Gate

NAND GATE FLIP-FLOPS

RS Flip-Flop: A basic Reset/Set flip-flop can be constructed by connecting two NAND gates as shown in Figure 6.

PREVIOUS STATE		INPUT CONDITION		RESULT	
1	0	SET	RESET	1	0
L	H	L	H	H	L
H	L	H	L	L	H
L	H	H	H	NO CHANGE	
H	L	H	H	NO CHANGE	
H	L	L	H	NO CHANGE	
L	H	H	L	NO CHANGE	
L	H	L	L	H	H*
H	L	L	L	H	H*
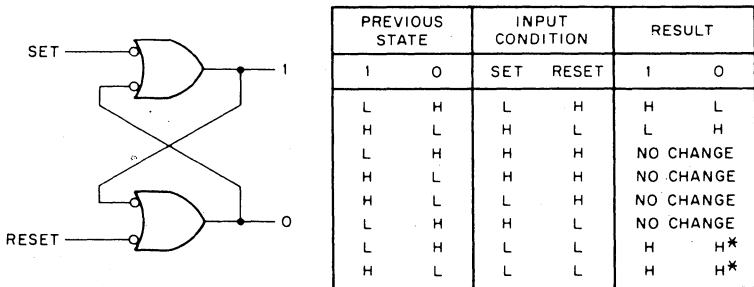
*Ambiguous state: In practice, the input that stays low longest will assume control.

Figure 6. RESET/SET NAND Gate Flip-Flop

CLOCKED NAND-GATE FLIP FLOPS

The Reset-Set flip-flop can be clock-synchronized by the addition of a two-input NAND gate to both the set and the reset inputs. (See Figure 7.) One of the inputs of each NAND is tied to a common clock or trigger line.
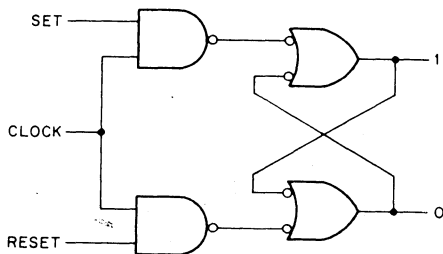
Figure 7. Clocked NAND Gate Flip-Flop

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A change of state is inhibited until a positive clock pulse is applied. The ambiguous case will result if both the set and reset inputs are high when the clock pulse occurs.

M SERIES GENERAL-PURPOSE FLIP-FLOPS

Two types of general-purpose flip-flops are available in the M Series, both of which have built-in protection against the ambiguous state characteristic of NAND gate flip-flops.

D Type Flip-Flop: The first of these is the D type flip-flop shown in Figure 8. In this element, a single-ended data input (D) is connected directly to the set gate input. An inverter is provided between the input line (D) and the reset input. This ensures that the set and reset levels cannot be high at the same time.

LOGIC SYMBOL

SIMPLIFIED NAND GATE EQUIVALENT
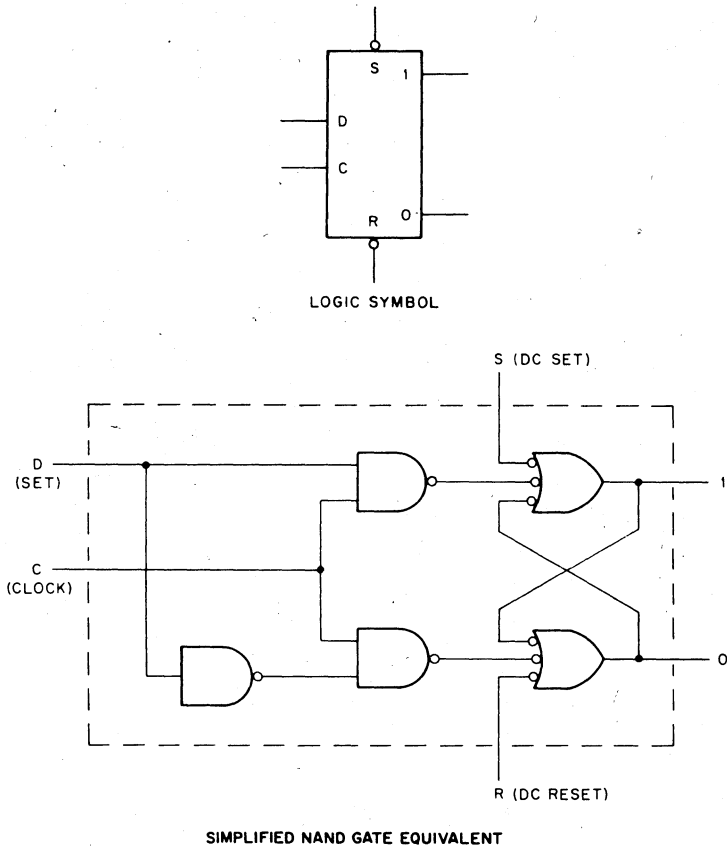
Figure 8. D Type General Purpose Flip-Flop

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The flip-flop proper employs three-input NAND gates to provide for dc set and reset inputs.

D type flip-flops are especially suited to buffer register, shift register, and binary ripple counter applications. Note that D type devices trigger on the leading (or positive going) edge of the clock pulse. Once the clock has passed threshold, changes on the D input will not affect the state of the flip-flop due to a lockout circuit (Not shown).

J-K Flip-Flop: The second type of clocked general-purpose flip-flop is the J-K or complementing flip-flop. An idealized version of the J-K flip-flop is made by substituting three-input NAND gates for the two-input NAND gates of the D type flip-flop. (See Figure 9.)

LOGIC SYMBOL

* IN ACTUAL MASTER - SLAVE CONFIGURATION, THESE
CROSS CONNECTIONS ARE TIED TO SLAVE OUTPUTS.

NAND GATE EQUIVALENT (INPUT BANK ONLY)
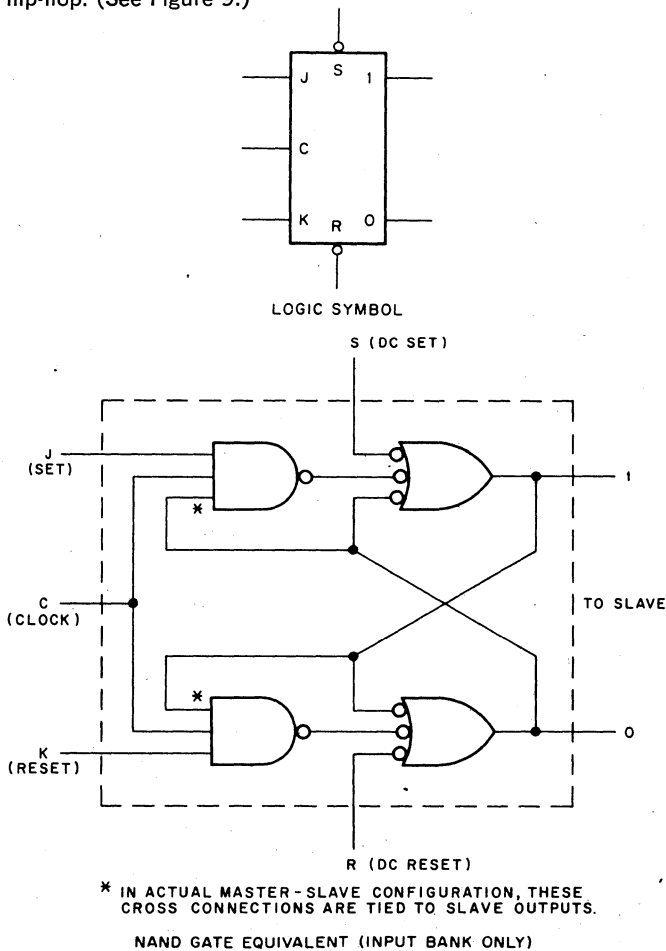
Figure 9. J-K Type General Purpose Flip-Flop

The ambiguous condition is avoided, and complementing action is achieved by cross connection of outputs to the added gate inputs. Either the J or K gate can be enabled but not both. For example, assume that the flip-flop is reset ("0"output is high), and both J and K are high. When the clock pulse occurs, only the J gate is enabled (the"1"output is low, inhibiting the K gate) and the flip-flop is set. With the reverse situation(output"1" initially high), the flip-flop is reset. Therefore, raising both the J and K inputs causes the flip-flop to complement when the clock goes high.

The J-K flip-flop shown in Figure 9 is representative of the logical operation of a flip-flop of this type. It is not, however, the actual circuit configuration of the integrated circuit package. The actual flip-flop is a master-slave type in which a master flip-flop is enabled during the positive level of the clock pulse and a slave (or output) flip-flop is set with the contents of the master flip-flop on the trailing (or negative going) edge of the clock pulse. Timing factors are discussed in detail in the section entitled "Timing Considerations".

UNUSED INPUTS (GATES AND FLIP-FLOPS)

As explained previously, the input circuit of the TTL circuits is quite different from that of ordinary DTL circuits. Since the input of a TTL device is an emitter of a multiple-emitter transistor, care must be exercised when an input is not to be used for logic signals. These emitters provide excellent coupling into the driving portions of the circuit when left unconnected. To insure maximum noise immunity, it is necessary to connect these inputs to a source of Logic 1 (High). Two methods are recommended to accomplish this:

1. Connect these inputs to a well filtered and regulated source of +3 volts. Pins U1 and V1 are provided on the M113, M117, M119, M121, M617, and M627 for this purpose.

2. Connect these inputs to one of the active inputs on the same gate. This results in a higher leakage current due to the parallel emitters and should be considered as an additional unit load when calculating the loading of the driving gate.

Connection of unused inputs to the supply voltage, Vcc, is not advisable, since power supplies are subject to transients and voltage excursions which could damage the input transistor.

TIMING CONSIDERATIONS

Standard Timing Pulse: In digital system design, a reference for system timing is required. In the M Series, a standard timing pulse generated by the M401 Variable Clock, provides such a reference. A standard pulse may also be obtained from a level transition through the use of the M602 Pulse Amplifier. Output pulses from each of these units are identical. The standard pulse derived from these two module types is shown in Figure 10.
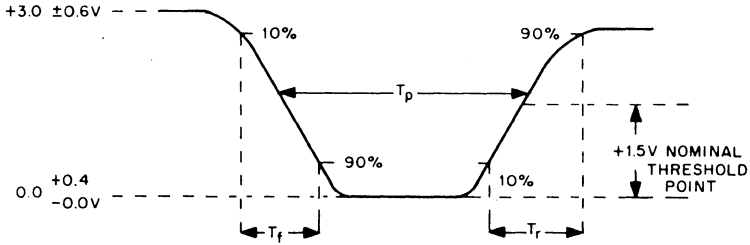
Figure 10. Standard Pulse

NAND Gate and Power Amplifier Propagation Delays: The standard pulse (Figure 10) is distributed throughout a system in negative form to maintain the leading edge integrity. (Since the TTL gate drives current in the logic 0 state, the falling edge is more predictable for timing purposes.) However, the standard pulse is of the wrong polarity for use as a clocking input to the type D and J-K flip-flops, requiring the use of a local inverter. Ordinarily, a NAND inverter is adequate. Where high fan-out is necessary, a M617 Power NAND is preferred.

For applications requiring both high fan-out and critical timing the M627 Power Amplifier is available. This module contains extremely high-speed gates which exhibit turn-on times differing by only a few nanoseconds. Simultaneity is desirable in clock or shift pulses distributed to extended shift registers or synchronous counters.

Delays introduced by inverting gates and power amplifiers are illustrated in Figure 11. (Delays are measured between threshold points.)

DELAY (NANOSECONDS)			
t_{on}		t_{off}	
TYP.	MAX.	TYP.	MAX.
18	29	8	15
7	—	5	—
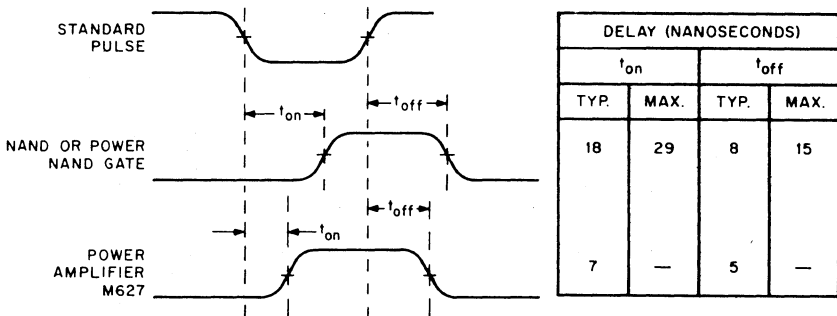
Figure 11. NAND Gate and Power Amplifier Delays

Flip-Flop Propagation Delays: D type flip-flops trigger on the leading or rising edge of a positive clock pulse; the propagation delay is measured from the threshold point of this edge. The set-up time of the D flop is also measured from this threshold point. Data on the D input must be settled at least 20 nanoseconds prior to the clock transition. The advantage of the D-flip-flop, however, is that the leading edge triggering allows the flip-flop AND gates to propagate while the clock pulse is still high. Figure 12 illustrates this situation.
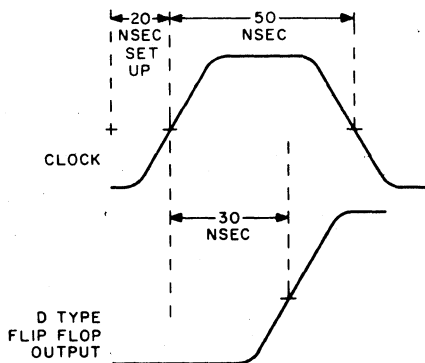
Figure 12. D Type Flip-Flop Timing

JK type flip-flops are, in effect, trailing edge triggering devices as explained previously. The only restriction on the J and K inputs is that they must be settled by the time that the rising edge occurs. Timing is shown in Figure 13.
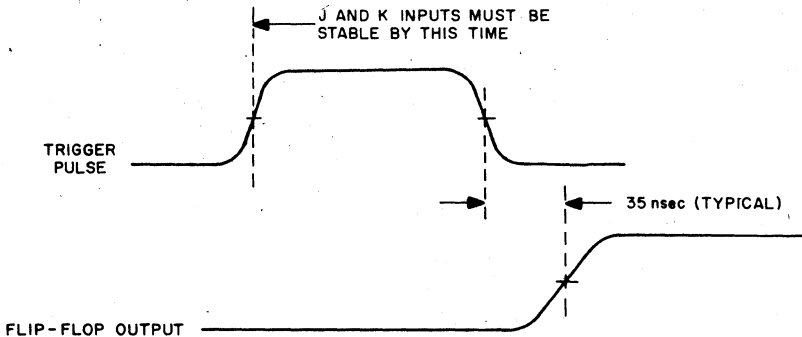
Figure 13. J-K Flip-Flop Timing

When using the dc Set or Reset inputs of either flip-flop type, propagation delays are referenced to the falling edge of the pulse. This is due to the inverted sense of these inputs. When resetting ripple type counters (where the output of one flip-flop is used as the trigger input to the next stage) the reset pulse must be longer than the maximum propagation delay of a single stage. This will ensure that a slow flip-flop does not introduce a false transition, which could ripple through and result in an erroneous count.

One-Shot Delay: Calibrated time delays of adjustable duration are generated by the M302 Delay Multivibrator. When triggered by a level change from a logical one to a logical zero, this module produces a positive output pulse that is adjustable in duration from 50 to 750 nsec with no added capacitance. Delays up to 7.5 milliseconds are possible without external capacitance. (See M302 specification.) Basic timing and the logic symbol are shown in Figure 14. The 100 picofarad internal capacitance produces a recovery time of 30 nsec. Recovery time with additional capacitance can be calculated using the formula;

$$t_r \text{ Nanoseconds} = \frac{30 \text{ C Total (Picofarads)}}{100}$$
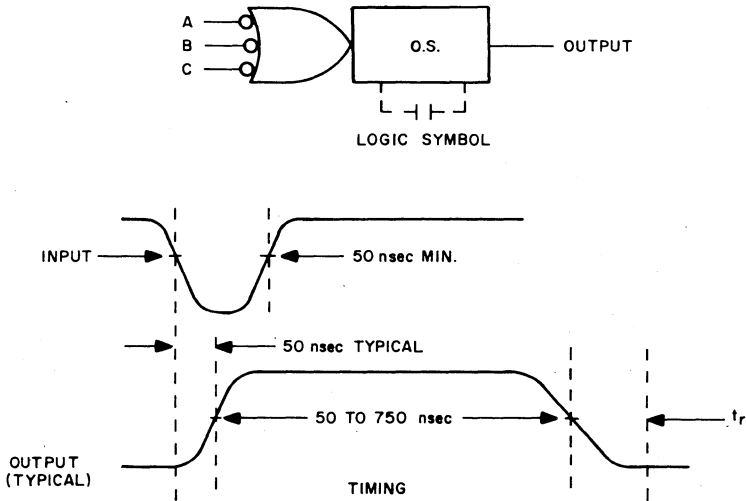
LOGIC SYMBOL

Figure 14. One-Shot Delay Timing and Logic Symbol

SYSTEM OPERATING FREQUENCY

Although individual propagation delays are significant in the design of digital logic, even more important is the maximum operating frequency of a system which is composed of these individual modules. Specifically designed systems may be operated at 10 MHz, but a more conservative design may result in a somewhat lower operating speed. M Series modules can be designed into a system with a 6 MHz clock rate with relative ease. This system frequency is derived by summing the delays in a simple logic chain:

1. A standard clock pulse width of 50 nsec is assumed. This period is measured from the threshold point of the leading edge to the threshold point of the trailing edge.

2. One flip-flop propagation delay of 35 nsec from the trailing edge of the clock pulse to the threshold point of the final state of the flip-flop is allowed.

3. Two gate-pair delays of 30 nsec each are assumed. (A gate-pair consists of two inverting gates in series.) Two gate-pair delays are usually required to perform a significant logic function with a minimum of parallel operations. The two gate-pair delays total 60 nsec.

The time necessary to perform these operations before the next occurrence of the clock pulse is the sum of the delays; 50 + 35 + 60, or 145nsec. Allowing 20 nsec for variations within the system, the resulting period is 165 nsec, corresponding to a 6 MHz clock rate. This timing is demonstrated in Figure 15.
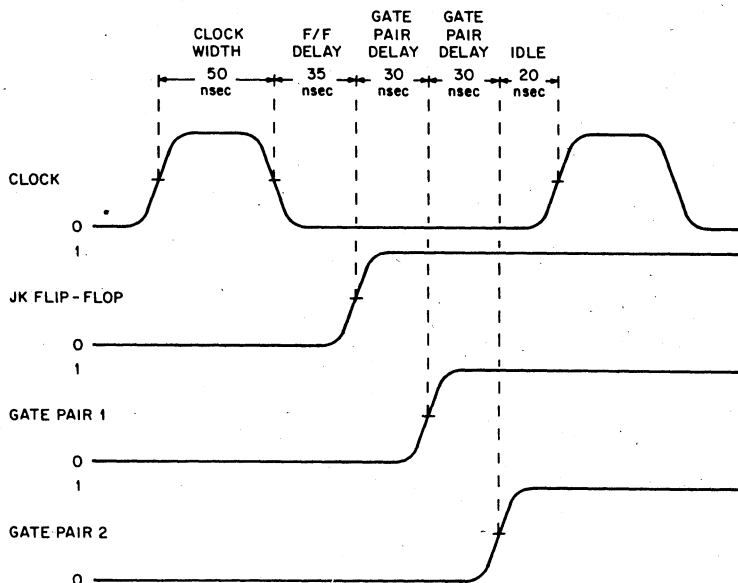
Figure 15. Delays Determining System Operating Frequency

Substitution of a D type flip-flop results in a similar timing situation. In a system using both D and J-K flip-flops, note that the D flip-flop triggers on the leading edge of the clock pulse and the J-K flip-flop triggers on the trailing edge. When calculating system timing using D flip-flops, remember that the flip-flop inputs must be settled at least 20 nsec prior to the occurrence of the clock pulse.

Preparation of a timing diagram that considers delays introduced by all logic elements will aid the designer in achieving predictable system performance.
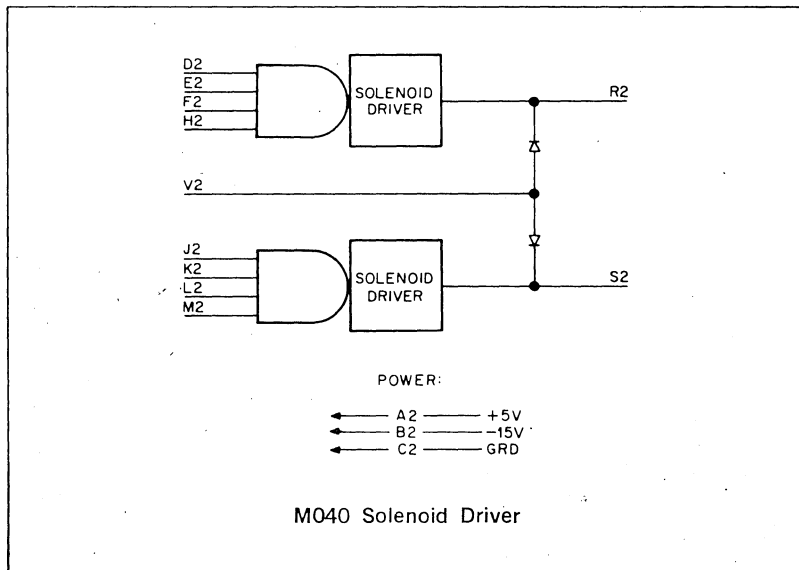
M040 Solenoid Driver

These high current drivers can drive relays, solenoids, stepping motor windings, or other similar loads. The output levels are -2 volts and a more negative voltage determined by an external power supply. One terminal of the load device should be connected to the external power source, the other to the driver output. There are two drivers per module.

Pin V of the driver module must be connected to the external supply so that the drivers will be protected from the back voltage generated by inductive loads. If the wire to the power supply is more than 3 feet long it may have to be by-passed at the module with an electrolytic capacitor to reduce the short over-shoot caused by the inductance of the wire. If pin V is connected to the supply through a resistor, the recovery time of inductive loads can be decreased at a sacrifice in maximum drive voltage capability. Maximum rated supply voltage less actual supply voltage should be divided by load current to find the maximum safe resistance. When both circuits on a module are used, the load current for the above calculation is the sum of the currents.
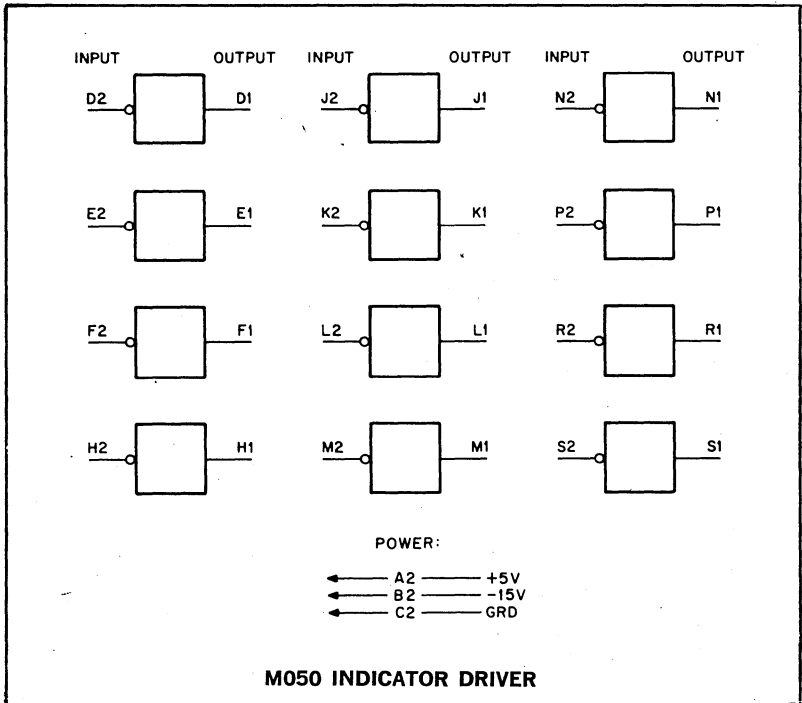
Inputs: Each input presents one unit load.

39

Outputs: The M040 has maximum ratings of −70 volts and 0.6 amp. Typical delay for the circuit is 5 μsec. No more than two circuits should be paralleled to drive loads beyond the current capabilities of single circuits.

Grounding: High current loads should be grounded at pin C2 of the M040.

Power: +5 volt, 13.6 ma; −15 volts, 7.6 ma.
The external voltage supply must provide the output current of the two drivers (1.2 amps max.)

M040 — $39.00

INPUT		OUTPUT	INPUT		OUTPUT	INPUT		OUTPUT
D2		D1	J2		J1	N2		N1
E2		E1	K2		K1	P2		P1
F2		F1	L2		L1	R2		R1
H2		H1	M2		M1	S2		S1

POWER:

```
← A2 ——— +5V
← B2 ——— −15V
← C2 ——— GRD
```

M050 INDICATOR DRIVER

The M050 contains twelve transistor inverters that can drive miniature in-candescent bulbs such as those on an indicator panel. It is used to provide drive current for a remote indicator, such as Drake 11-504, Dialco 39-28-375, or Digital Indicator type 4908, or level conversion to drive 4917 and 4918 indicator boards (See the Hardware Section.) A low level on the input of the driver causes current to flow in the output.

INPUTS: Each input presents two unit loads.

OUTPUTS: Each output is capable of driving 50 ma. into an external load connected to any voltage between ground and −20 volts.

POWER: +5 volts, 40 ma (max); −15 volts, 12 ma (max)

M050 — $31.00

POWER:
A2 ——————— +5V
C2, T1 ——— GRD
+3V ——— U1, V1 ——► UNUSED INPUTS
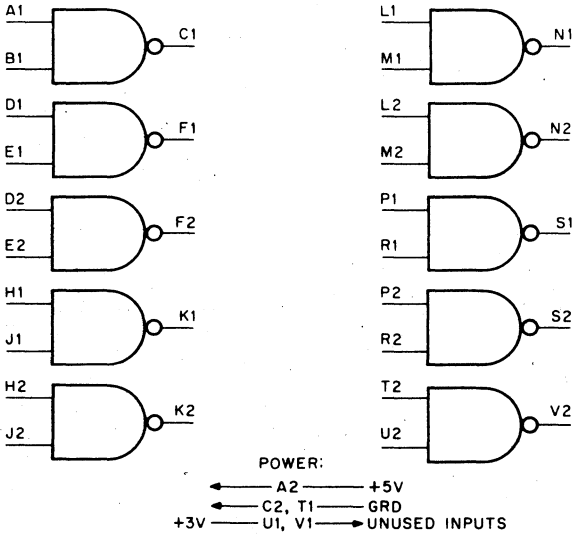
M113 2-INPUT NAND GATES

POWER:
A2 ——————— +5V
C2, T1 ——— GRD

M115 3-INPUT NAND GATES

A1
B1
C1
D1
E1

D2
E2
F2
H2
J2

F1
H1
J1
K1
L1

K2
L2
M2
N2
P2

M1
N1
P1
R1
S1

R2
S2
T2
U2
V2

POWER:

⟵ A2 ⟶ +5V

⟵ C2, T1 ⟶ GRD

+3 VOLTS ⟶ U1, V1 ⟶ UNUSED INPUTS

M117 4-INPUT NAND GATES

A1
B1
C1
D1
D2
E2
F2
H2
J2

F1
H1
J1
K1
K2
L2
M2
N2
P2

M1
N1
P1
R1
R2
S2
T2
U2
V2

POWER:

⟵ A2 ⟶ +5V

⟵ C2, T1 ⟶ GRD

+3 VOLTS ⟵ U1, V1 ⟶ UNUSED INPUTS
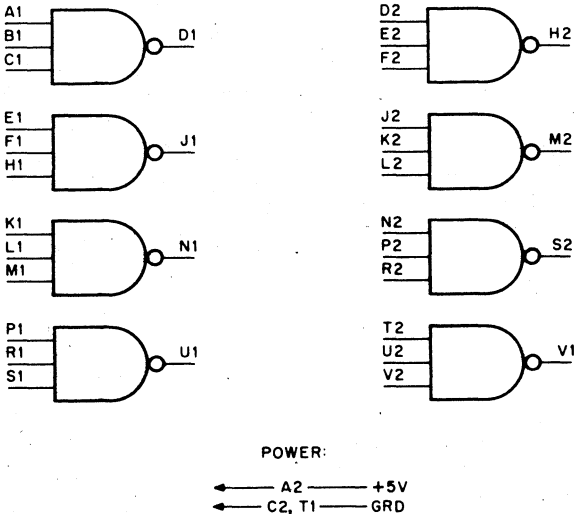
M119 8-INPUT NAND GATES
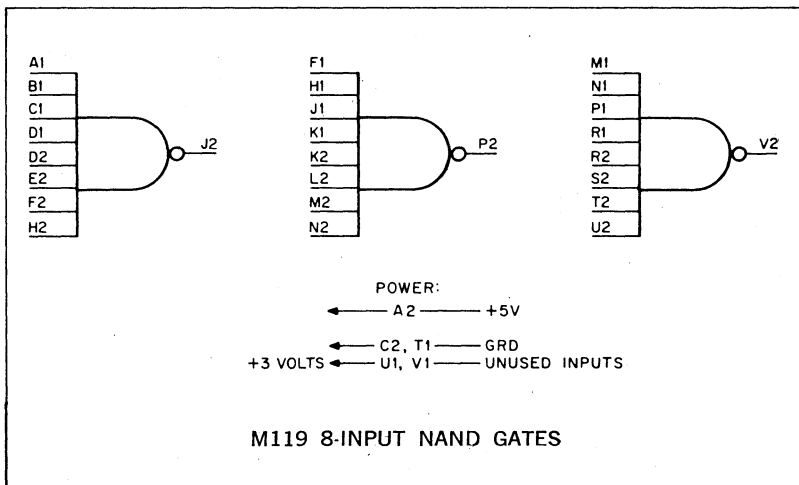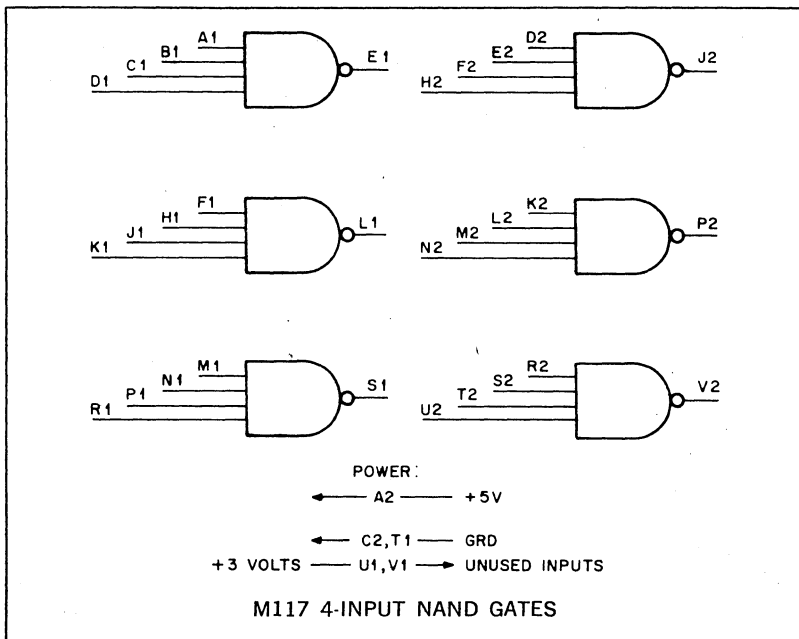
These modules provide general-purpose gating for the M Series, and are most commonly used for decoding, comparison, and control. Each module performs the NAND function $\overline{A \cdot B \text{---------} N}$, depending upon the number of inputs.

M113 — Ten, two-input NAND gates that
also may be used as inverters.
M115 — Eight, three-input NAND gates.
M117 — Six, four-input NAND gates.
M119 — Three, eight-input NAND gates.

Unused inputs on any gate must be returned to a source of logic 1, for maximum noise immunity. In the M113, M117 , M119, M121, M617 and M627 modules, two pins are provided (U1 and V1) as source of +3 volts for this purpose. Each pin can supply up to 25 unit loads.

Typical propagation delay of M Series gates is 15 nsec.

Inputs: Each inputs presents one unit load.

Outputs: Each output is capable of driving 10 unit loads.

Power: M113: 30 ma (avg)

M115: 28 ma (avg)

M117: 18 ma (avg)   at +5 volts

M119: 9 ma (avg)

M113 — $23.00
M115 — $24.00
M117 — $24.00
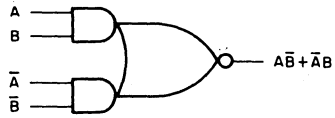M119 — $24.00
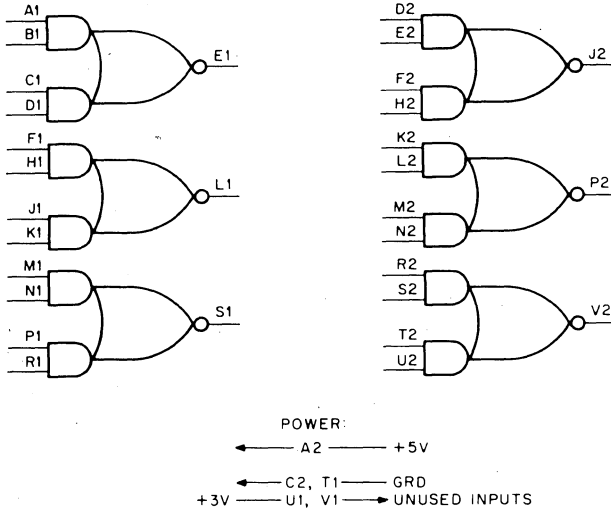
M121 AND/NOR GATES

The M121 module contains six AND/NOR gates which perform the function $\overline{AB + CD}$. By proper connection of signals to the AND inputs, the exclusive OR, coincidence, and NOR functions can be performed.
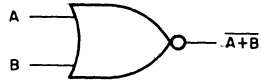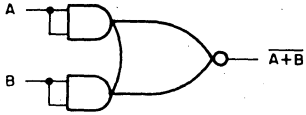
Typical propagation delay of an M121 gate is 15 nsec.

Inputs: Each input presents one unit load to the driving module.

Outputs: Each output is capable of driving up to 10 unit loads.
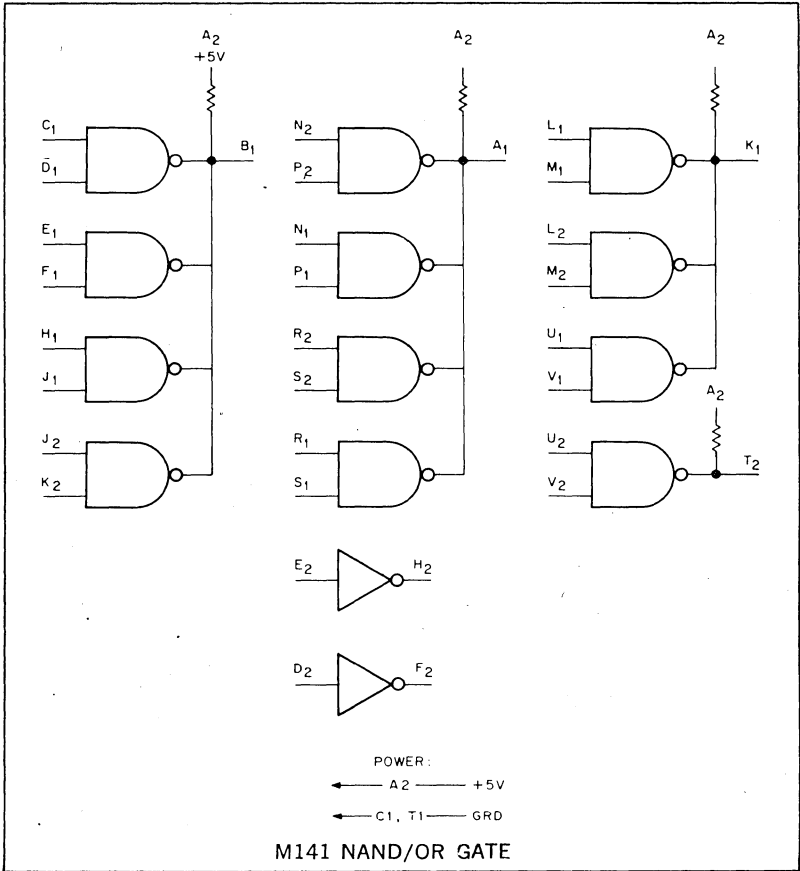
Power: +5 volts, 21 ma (avg.)
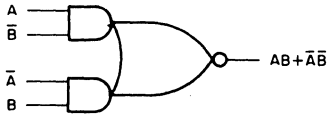
A
$\overline{B}$

$\overline{A}$
B
$AB + \overline{A}\overline{B}$

COINCIDENCE

A
B

$\overline{A}$
$\overline{B}$
$A\overline{B} + \overline{A}B$

EXCLUSIVE OR

A

B
$\overline{A+B}$

NOR FUNCTION

A

B
$\overline{A+B}$

M141 NAND/OR GATE

The M141 NAND/OR gate performs two levels of logic. The first is the NAND function which is identical to the M113 NAND gate. The second level is that of a wired OR for low logic levels. The two input NAND gate which is used in the M141 does not have the standard TTL output circuit, but only the lower half of the totem pole output. This allows the outputs of these gates to be connected together and to share a common pull-up resistor. Propagation delay through these gates is a maximum of 70 nsec.

The NAND/OR gates are arranged in four groups consisting of 4, 4, 3, and 1 two input NAND gates respectively. The outputs in each group are connected together which provide a wired OR for low levels. The function of these gates can be shown as:
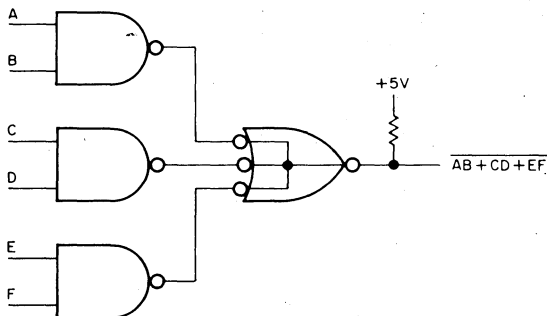
By using one of the two inverters provided, a true AND/OR function can be realized. A maximum of four groups of gates can be connected together. Connection is made by merely connecting output pins together.

Inputs: Each input presents one unit load.

Outputs: Four gate outputs, each capable of driving 7 unit loads. The load resistor of each output presents 2 unit loads when connected to another output. For example, four groups are connected together, therefore 3 groups present two unit loads each to the fourth group, totalling 6 unit loads. This leaves 1 unit load capability. Each inverter output is capable of driving up to 10 unit loads.
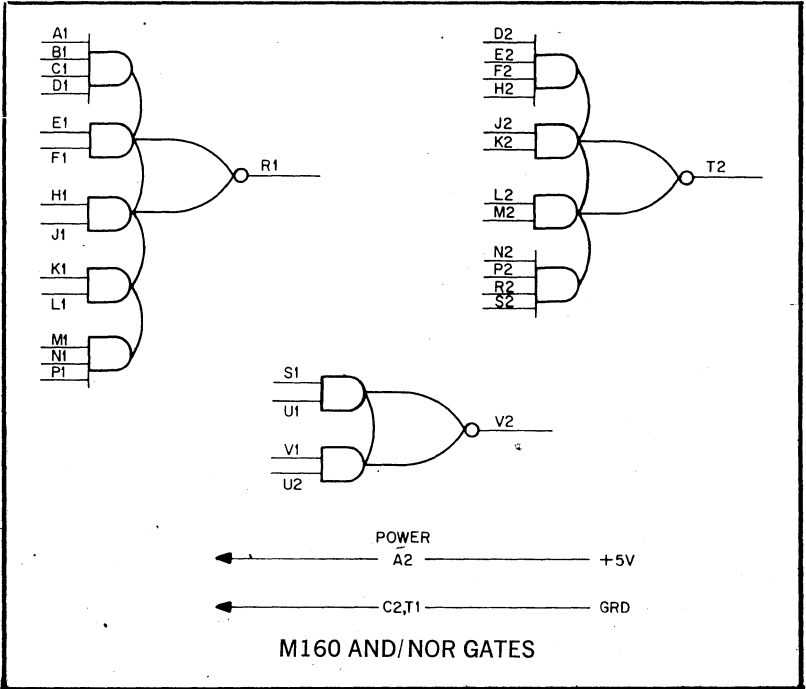
Power: +5 volts, 55 ma (avg.)

Propagation delay of the NAND/OR gate with 100 pf capacitance on its output is 70 nsec.

M141—$30.00

AND/NOR GATE
M160

M
SERIES

M160 AND/NOR GATES

The M160 module contains three general purpose AND/NOR gates which perform functions similar to the M121. By connecting signals to the AND inputs, these gates can be used to select and place on a single output any of several input signals.

Typical propagation delay of an M160 gate is 20 nsec.

INPUTS: Each input presents one unit load

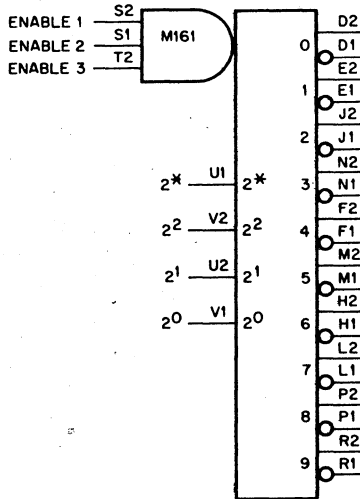**OUTPUTS:** Each output is capable of driving 10 unit loads

POWER: +5 volts, 12 ma (average)

M160 — $35.00

ENABLE 1 — S2
ENABLE 2 — S1 M161
ENABLE 3 — T2

2^* — U1 — 2^*
2^2 — V2 — 2^2
2^1 — U2 — 2^1
2^0 — V1 — 2^0

0 — D2, D1, E2
1 — E1, J2
2 — J1, N2
3 — N1, F2
4 — F1, M2
5 — M1, H2
6 — H1, L2
7 — L1, P2
8 — P1, R2
9 — R1

M161 BINARY TO OCTAL/DECIMAL DECODER

The M161 is a functional decoding module which can be used as a binary-to-octal or binary-coded decimal (8421 or 2421 codes) to decimal decoder. In the binary-to-octal configuration, up to eight M161's can be linked together to provide decoding of up to six bits. Three ENABLE inputs are provided for selective enabling of modules in decoders of more than one digit. In the octal mode, the bit 2^* input is connected to ground, which automatically inhibits the 8 and 9 outputs. Connections for a 5-bit binary/octal decoder (4 modules) are shown below. The figure assumes that the inputs to the decoder are the outputs of flip-flops such as FF2° (1), 1 output side; and FF2° (0), 0 output side.

The 2^* input may be of decimal value 2, 4, 6, 8 as long as illegal combinations are inhibited before connections to the inputs, and the 4-2-1 part of the code is in binary.

The propagation delay through the decoder is typically 55 nsec in the binary-to-octal mode, and 75 nsec in the BCD-to-decimal mode. The maximum delay in the BCD-to-decimal mode is 120 nsec, frequency-limiting this module to 8HMz when used in this fashion. The enable inputs can be used to strobe output data providing inputs 2° — 2^* have settled at least 50 nsec prior to the input pulse.

Inputs: 2° through 2^*, 1 unit load each; ENABLE 1 through ENABLE 3, 2 unit loads each.

Outputs: Each positive output is capable of driving 10 unit loads, and each negative output, 9 unit loads.

Power: +5 volts, 80 ma (avg.)
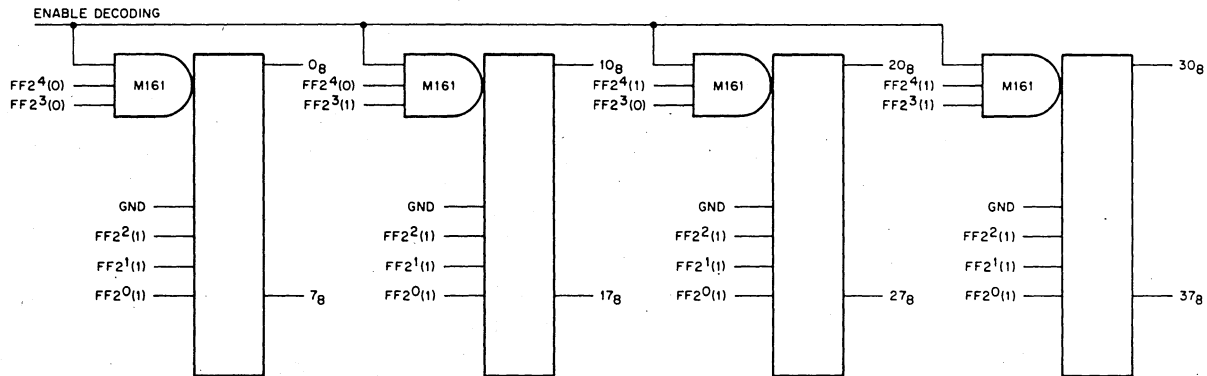
5-BIT BINARY/OCTAL DECODER
(OUTPUTS ARE REPRESENTED IN
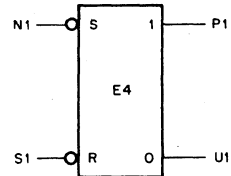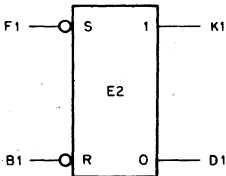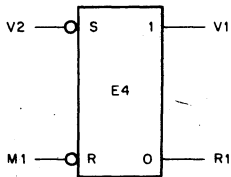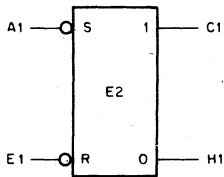OCTAL 37_8 = 31_{10})

5-BIT BINARY/OCTAL DECODER
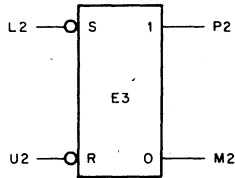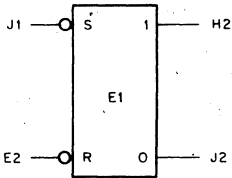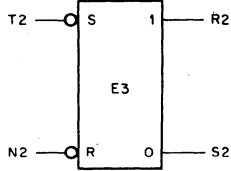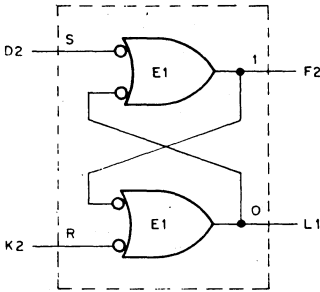
M203 8-R/S FLIP-FLOPS

The M203 is made up of 8 R/S type flip-flops. Each flip-flop is made up of two 2-input NAND gates whose outputs are cross coupled. R/S flip-flops provide an inexpensive method of storage but care must be taken to inhibit placing the Set and Reset inputs low at the same time. In this case, the last of the inputs to be removed will control the final state of the flip-flop.

The propagation delay of the M203 is approximately 30 nsec.

INPUTS: All inputs present 1 unit load

OUTPUTS: All outputs are capable of driving 9 unit loads.

POWER: +5 volts, 35 ma (avg.)

M203 — $32.00

M204 GENERAL-PURPOSE BUFFER AND COUNTER

The M204 contains four J-K type flip-flops, augmented by multiple-input AND gates, for general use as gated control flip-flops or buffers. The gating scheme permits the formation of counters of most moduli up to .16, by simple connector wiring. Clock, trigger and input lines for each flip-flop are independent. A common CLEAR input is provided.

Logical operation of the J-K flip-flops used in this module is identical to the M207 (described in detail) except for the addition of dc set inputs.

Two typical counting configurations are shown below:

54
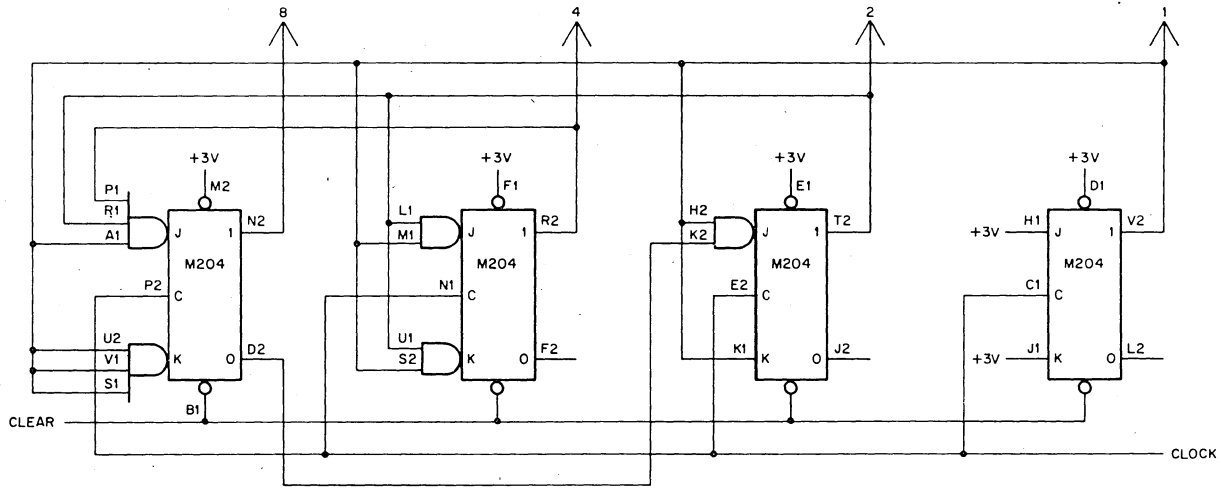
8-4-2-1 BCD UP COUNTER
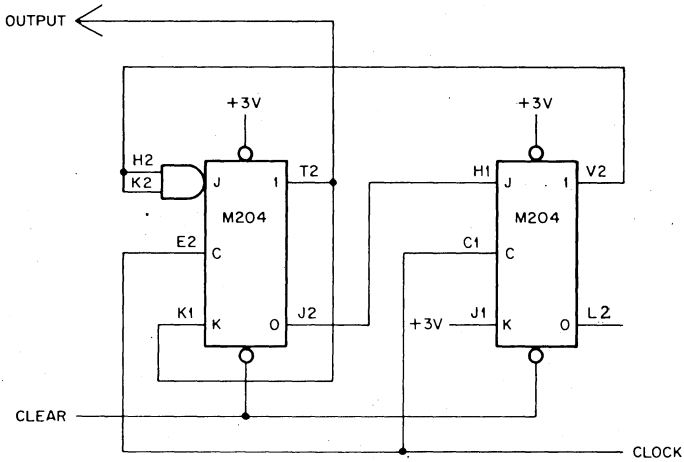
MODULUS 3

Other combinations for counter construction are explained thoroughly in application note AP-M-01 which may be obtained from the nearest DIGITAL EQUIPMENT Sales Office.

Inputs: The "C" inputs present two unit loads each to the source. The dc set ("S") inputs present two unit loads each. The common CLEAR line presents 8 unit loads. All other inputs present one unit load to the source.

Outputs: Each output, before interconnection as a counter, is capable of driving 10 unit loads.

Power: +5 volts, 40 ma (avg.)

M204 — $36.00

M206 D TYPE FLIP-FLOPS
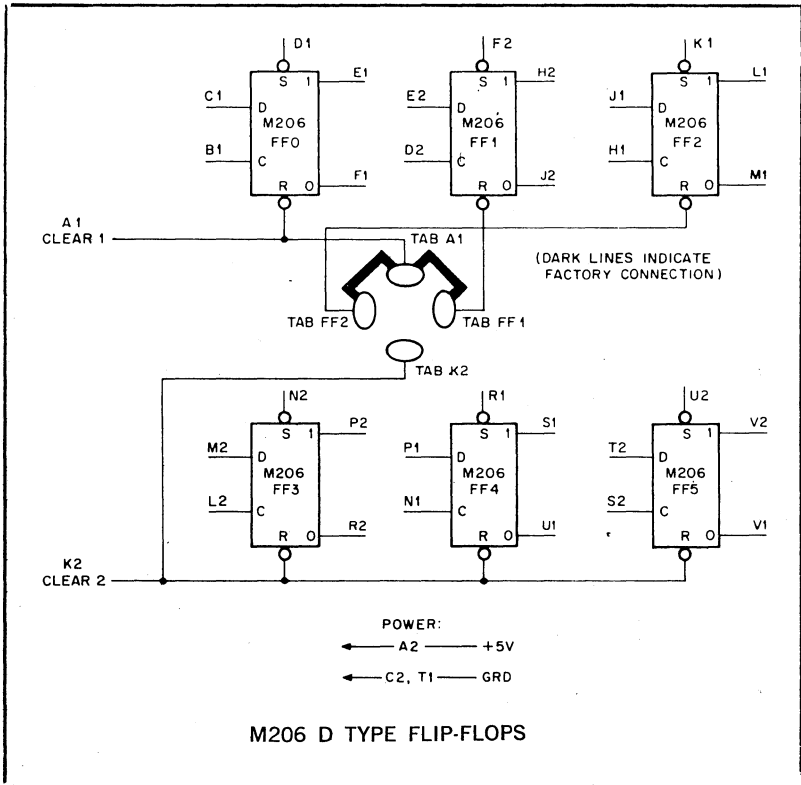
The M206 contains six separate D-Type flip-flops. Each flip-flop has independent gated data, clock, and dc set inputs.

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flops. All M206 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

CONFIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1, & 2	FF3, 4, & 5		
4-2	FF0 & 1	FF2, 3, 4, & 5	A1 to FF2	K2 to FF2
5-1	FF0	FF1, 2, 3, 4, & 5	A1 to FF2	K2 to FF2
			A1 to FF1	K2 to FF1

Information must be present on the D input 20 nsec (max) prior to a standard clock pulse and should remain at the input at least 5 nsec (max) after the clock pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop will be stable at the output within 50 nsec, maximum. Typical width requirement for the clock, dc reset and dc set pulses is 30 nsec each.

Inputs: D inputs present 1 unit load each.

            C inputs present 2 unit loads each.

            CLEAR lines present 3 unit loads per connected flip-flop.

            S inputs present 2 unit loads each.

Outputs: Each output is capable of driving 10 unit loads.

Power: +5 volts, 51 ma (avg.)

A common clear for all six flip-flops can be obtained by wiring pins A1 and K2 together externally. **CAUTION:** The loading of each clear line is calculated on the basis of 3 unit loads per flip-flop. For example, the 4-2 configuration results in 12 unit loads at input K2 and 6 unit loads at input A1.

M206 — $42.00

M207 J-K FLIP FLOPS
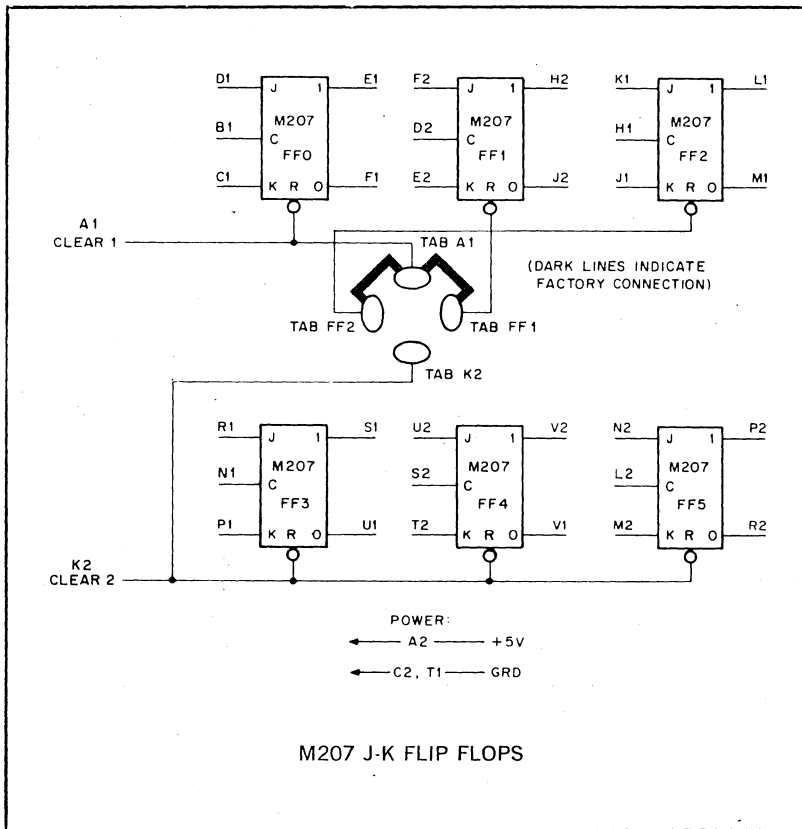
The M207 contains six J-K type flip-flops which can be used as buffers, control flip-flops, shift registers, and counters. A truth table for clocked set and reset conditions appears below. Note that when the J and K inputs are both high, the flip-flop complements on each clock pulse.

STARTING CONDITION (OUTPUT)		INPUT CONDITION		RESULT AT END OF STANDARD CLOCK PULSE (OUTPUT)	
1	0	J	K	1	0
L	H	L	L	No change	
		L	H	No change	
		H	L	H	L
		H	H	H	L
H	L	L	L	No change	
		L	H	L	H
		H	L	No change	
		H	H	L	H

Application of a low level to an R input for at least 25 nsec resets the flip-flop unconditionally. Two CLEAR inputs are provided, with jumper terminals for optional clearing in groups of 3 and 3 (standard), 4 and 2, 5 and 1, or 6 and 0.

J and K inputs must be stable during the leading-edge threshold of a standard clock input and must remain stable during the positive state of the clock. Data transferred into the flip-flop will be stable at the output within 30 nsec (typical) of the clock pulse trailing edge threshold.

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flop. All M207 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

CONFIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1, & 2	FF3, 4, & 5		
4-2	FF0 & 1	FF2, 3, 4, & 5	A1 to FF2	K2 to FF2
5-1	FF0	FF1, 2, 3, 4, & 5	A1 to FF2 A1 to FF1	K2 to FF2 K2 to FF1

Inputs: J or K inputs present 1 unit load each.
C inputs present 2 unit loads each.
CLEAR lines present 2 unit loads per connected flip-flop.

Outputs: Each output is capable of driving 10 unit loads.

Power: +5 volts, 48 ma (avg)

M207 — $42.00

M208 8-BIT BUFFER/SHIFT REGISTER

TWO REPRESENTATIVE STAGES

*NOTE THAT THESE TYPE "D" FLIP-FLOPS HAVE HAD THEIR OUTPUT TERMINALS REDEFINED. COMPARE THESE PIN CONNECTIONS WITH THOSE IN M206 DESCRIPTION.
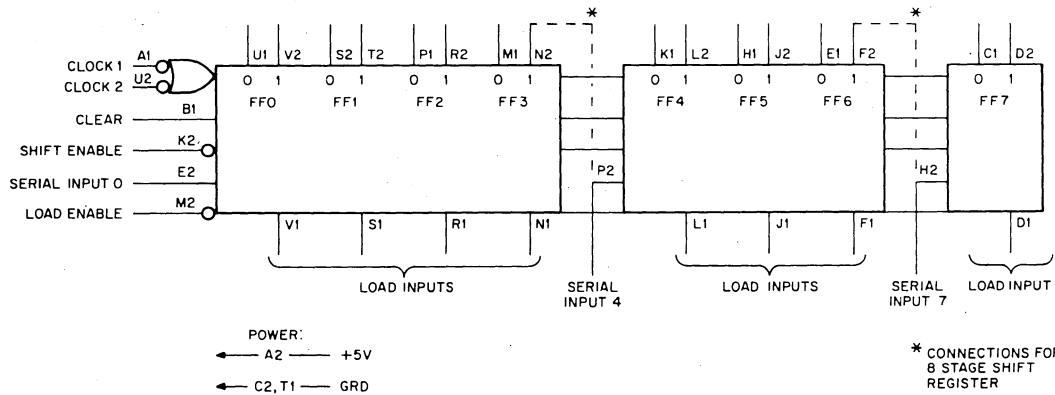
The M208 is an internally connected 8-bit buffer/shift register. Provisions are made for gated single-ended parallel load, bipolar parallel output, and serial input. The shift register is divided into three segments:

Bits 0 through 3: Serial input to bit 0, bipolar outputs from bits 0 through 3.

Bits 4 through 6: Serial input to bit 4, bipolar outputs from bits 4 through 6.

Bit 7: Serial input to 7, bipolar outputs from bit 7.

Each of these groups shares a common shift line (the ORed CLOCK 1 and CLOCK 2 inputs) and a common parallel load line (LOAD ENABLE). To form a 6-bit shift register, for example, the true output of bit 3 is connected to the serial input of stage 4. A shift register of 8 bits may be constructed from a single module. Modules may be cascaded to form shift registers of any desired length. A few additional stages may be formed more economically from NAND and AND/NOR gates plus a D-type flip-flop. A representative stage of this type is illustrated.

Two clock inputs are provided so that individual Load and Shift clock sources may be used. Care must be taken that the clock inputs remain in the high state in the off condition because either input going to the low state will produce a positive edge at the output of the NAND gate and trigger the D type flip-flop. Data shifted or parallel loaded into the M208 will appear on the outputs within 55 nsec (max) of the clock pulse leading edge threshold. Load or Shift Enable levels and parallel data must be present at least 50 nsec prior to a clock pulse. Propagation delay from the leading edge of a CLEAR pulse to the outputs is 40 nsec max.

Inputs: Serial data, dc set, and enable inputs present one unit load each to the source module. Each clock input presents $2\frac{1}{2}$ unit loads. The CLEAR input presents two unit loads.

Outputs: Parallel outputs are capable of driving 10 unit loads each.

Power: +5 volts, 112 ma (avg)

M208 — $84.00
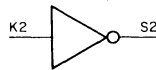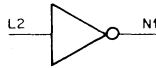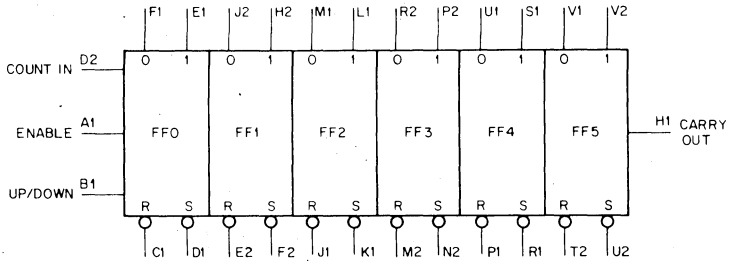
M211 BINARY UP/DOWN COUNTER

The M211 is a 6 bit binary UP/DOWN counter. It can switch counting mode (UP or DOWN) without disturbing the contents of the counter. Maximum count rate is 10 MHz. SET/RESET inputs are available for each bit. Maximum carry propagation time is 80 ns per bit.

The Enable input must be negated before the Up/Down level is switched. Maximum settling time between control level change is 75 ns. The enable input must be asserted 60 ns before the first count. Up count is a high level and down count is a low level. The Carry Out will generate a positive level change whenever a carry or borrow occurs, depending respectively on an up or down counting mode.

Inputs: Count In—positive transition or pulse with less than
           400 nsec risetime.
           Count In presents 2 unit loads.
           Reset — Each reset input presents 3 unit loads
           Set — Each set input presents 2 unit loads
           All other inputs present 1 unit load

Outputs: Each flip flop output (1 or 0) can drive 8 unit loads.
Carry Out can drive 10 unit loads
Each inverter output can drive 30 unit loads

Power: +5.0 volts, 130 ma (avg)

M211 — $75.00
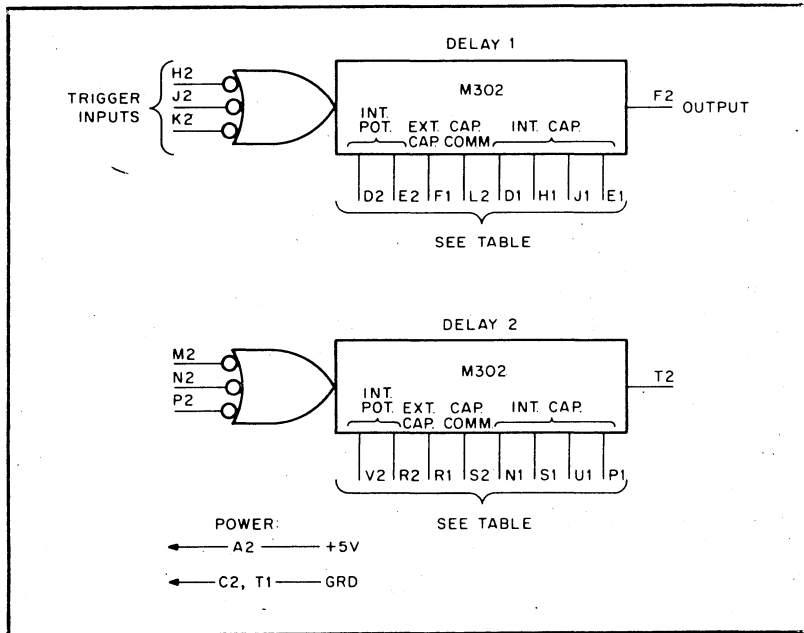
The M302 contains two delays (one-shot multivibrators) which are triggered by the trailing edge of a positive pulse or by a level change from high to low. When the input is triggered, the output changes from low to high for a predetermined, adjustable period of time and then returns to low. The DELAY RANGE is determined by an internal capacitor, or a parallel combination of internal and external capacitors. An internal potentiometer can be connected for fine delay adjustment within each range. Fall time of the input trigger should be less than 400 nsec. Typical transition time between the trigger and output rise threshold is 50 nsec. The delay time is adjustable from 50 nsec to 7.5 milliseconds using the internal capacitors and can be extended by adding an external capacitor. The minimum internal capacitance of 100 picofarads produces a recovery time of 30 nsec. Recovery time with additional capacitance can be calculated using the formula:

$$T_R \text{ Nanoseconds} = \frac{30 \text{ C Total (In Picofarads)}}{100}$$

Inputs: Each input presents $2\frac{1}{2}$ unit loads.

Outputs: Each output is capable of driving 25 unit loads.

Power: $+5$ volts, 130 ma (avg)

| Delay Range | Capacitor Value | Interconnections Required | |
		Delay 1	Delay 2
50 nsec — 750 nsec	100 pf (internal)	None	None
500 nsec — 7.5 nsec	1000 pf (internal)	D1 — L2	N1 — S2
5 usec — 75 usec	0.01 uf (internal)	H1 — L2	S1 — S2
50 usec — 750 usec	0.10 uf (internal)	J1 — L2	U1 — S2
500 usec — 7·5 msec	1.0 uf (internal)	E1 — L2	P1 — S2
Above 7.5 msec	Add external capacitors between specified pins	F1 — L2	R1 — S2

Adjustable Delays: connect pins to add internal adjustment potentiometer. Without a potentiometer, the delay will not recover. An external potentiometer of less than 10KΩ can be used by connecting it between E2 or R2 and ground pin C2. Use of an external adjustment resistor will cause some increase in jitter. It is recommended that leads to an external potentiometer be twisted pairs and as short as possible.
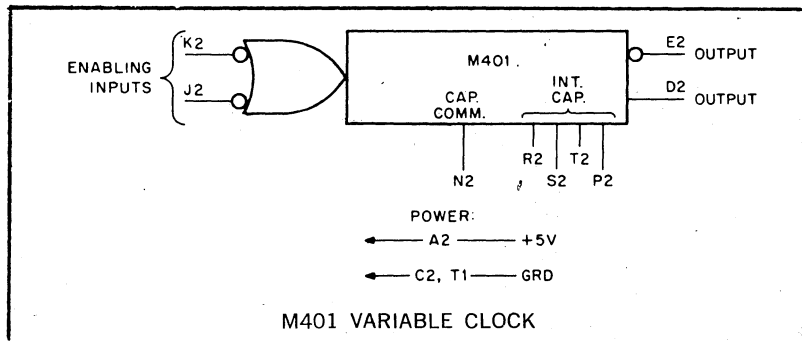
D2 — E2   V2 — R2

M302 — $46.00

M401 VARIABLE CLOCK

The M401 Variable Clock is a stable RC-coupled multivibrator which produces standard timing pulses at adjustable repetition rates.

The module is intended for use as the primary source of timing signals in a digital system. Repetition rate is adjustable from 175 Hz to 10 MHz in five ranges. Internal capacitors, selected by jumper pin connections, provide coarse frequency control. An internal potentiometer provides continuously variable adjustment within each range.

A two-input OR gating input is provided for start-stop control of the pulse train. A level change from high to low with fall time less than 400 nsec is required to enable the clock. Propagation delay from the low transition of the input to the leading edge of the first output pulse is typically 50 nsec. for the negative output pulse and 80 nsec for the positive output pulse. A 5% power supply deviation changes the PRF by less than 1.5%.

Frequency Range	Interconnections Required	
1.5 MHz to 10 MHz	(100 pf)	NONE
175 KHz to 1.75 MHz	(1000 pf)	N2 — R2
17.5 KHz to 175 KHz	(.01 μfd)	N2 — S2
1.75 KHz to 17.5 KHz	(0.1μfd)	N2 — T2
175 Hz to 1.75 KHz	(1.0 μfd)	N2 — P2

Fine Frequency Adjustment: Controlled by an internal potentiometer. No provision is made for any external connections.	External capacitor may be added by connection between pin N2 and ground.

Inputs: Each enable input presents 1 unit load.

Outputs: The positive output can drive 10 unit loads; the negative output, 9 unit loads.
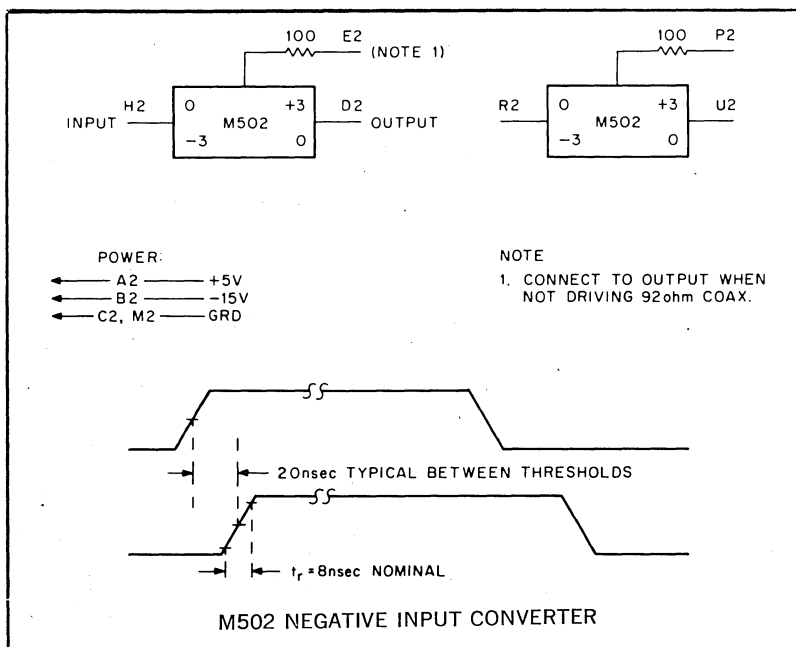
Power: +5 volts, 75 ma (avg)

M401 — $55.00

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```
            100   E2
            ᴡᴡ   (NOTE 1)

     H2   ┌──────────────┐ D2              R2   ┌──────────────┐ U2
INPUT ────┤ O        +3  ├──── OUTPUT      ─────┤ O        +3  ├────
          │    M502      │                      │    M502      │
          │ -3        0  │                      │ -3        0  │
          └──────────────┘                      └──────────────┘

                                               100   P2
                                               ᴡᴡ
```

```
    POWER:                          NOTE
◄──── A2 ──────── +5V               1. CONNECT TO OUTPUT WHEN
◄──── B2 ──────── -15V                 NOT DRIVING 92 ohm COAX.
◄──── C2, M2 ──── GRD
```



```
              ┤├  20nsec TYPICAL BETWEEN THRESHOLDS

              ┤├  tᵣ = 8nsec NOMINAL
```

M502 NEGATIVE INPUT CONVERTER

The M502 contains two non-inverting high-speed signal converters which interface standard negative (−3v and ground) DIGITAL logic levels or pulses with M and K Series positive logic modules. These converters provide sufficient current drive at a low output impedance for system interconnections by means of terminated 92-ohm coaxial cable. The converters operate at frequencies up to 10 MHz, with typical output rise and fall times of 8 nsec. Propagation times for output rise and fall are typically 20 nsec.

INPUT	OUTPUT
0v	+3v
−3v	0v

Inputs: Input loading is equivalent to a 3 ma clamped load.

Outputs: Each output can drive terminated 92-ohm coaxial cable, and supply an additional 30 ma at +3 volts or sink an additional 30 ma at ground. Output rise and fall times depend on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds are increased by connecting the 100 ohm resistor to the output.
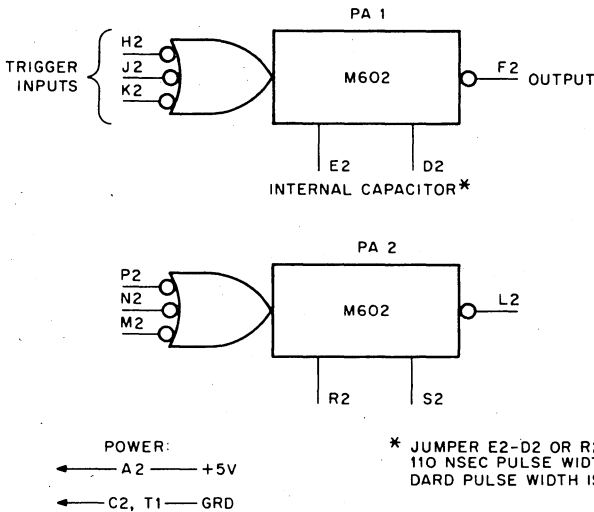
Power: +5 volts, 150 ma; −15 volts, 20 ma (avg)

M502 — $26.00

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M602 PULSE AMPLIFIER

The M602 contains two pulse amplifiers which provide power amplification, standardize pulses in amplitude and width, and transform level changes into a standard pulse. A negative pulse output is produced when the input is triggered by a transition from high to low. Propagation time between input and output thresholds is 30 nsec maximum. An internal capacitor is brought out to pin connections to permit the standard 50 nsec output pulse to be increased to 110 nsec (nominal). Recovery time is equal to that of the output pulse width. The input must have a fall time (10% to 90% points) of less than 400 nsec and must remain below 0.8 volts for at least 30 nanoseconds. Maximum PRF is 10 MHz.

Inputs: Each input presents 2½ unit loads.

Outputs: Each output is capable of driving 30 unit loads.

Power: +5 volts, 200 ma (avg)

M602 — $28.00

POWER:

$\longleftarrow$ A2 $\longrightarrow$ + 5 V

$\longleftarrow$ C2, T1 $\longrightarrow$ GRD

+3 VOLTS $\longrightarrow$ U1, V1 $\longrightarrow$ UNUSED INPUTS
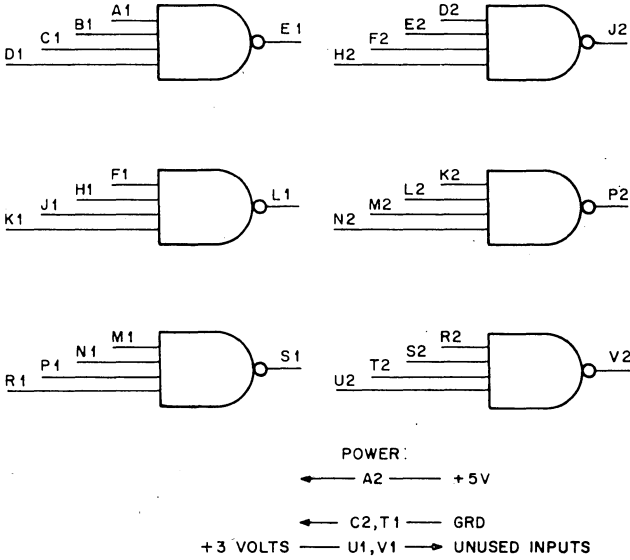
M617 POWER NAND GATE

The M617 contains 6 four-input NAND gates each capable of driving up to 30 unit loads. Typical gate propagation delay is 15 nsec. Physical configuration and logical operation are identical to the M117.

Inputs: Each input presents 1 unit load.

Outputs: Each output is capable of driving 30 unit loads.

Power: +5 volts, 52 ma (avg)

M617 — $27.00

M627 NAND POWER AMPLIFIER
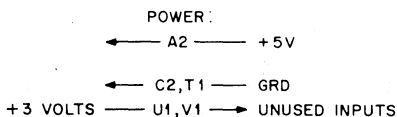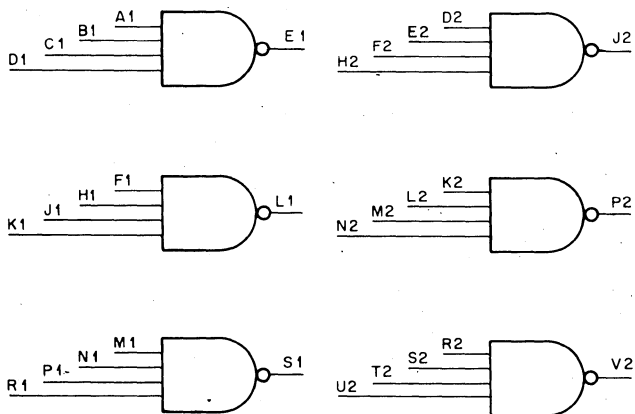
The M627 combines power amplification with high-speed gating, specifically for high fan-out of clock or shift pulses to expanded counters and shift registers. Propagation time between input and output transitions is typically 6 nsec. To utilize the timing accuracy of this module, wire runs of minimum length are recommended.

The module may also be used as a four-input NAND gate. In the pulse amplifier application, unused inputs should be connected to the +3 volt pins provided.

Inputs: Each input presents $2\frac{1}{2}$ unit loads.

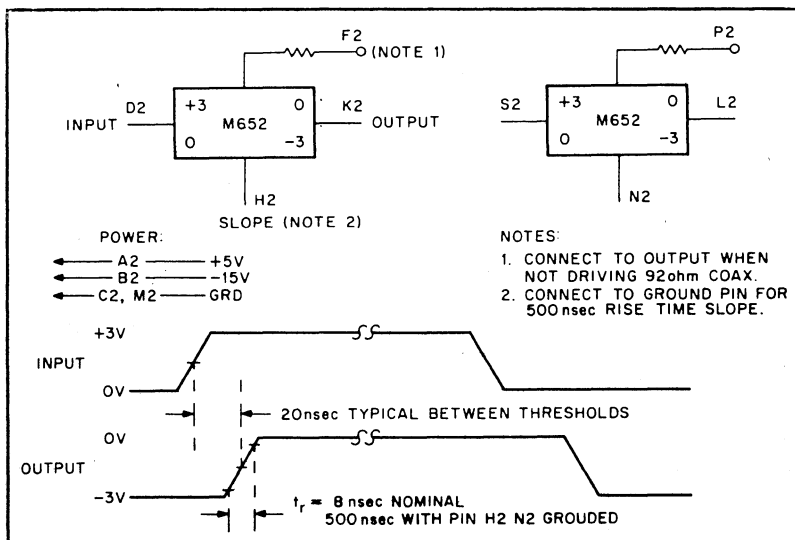**Outputs:** Each output is capable of driving 40 unit loads.

Power: +5 volts, 120 ma (avg)

M627 — $32.00

F2
P2
(NOTE 1)

D2
INPUT

+3	0	K2
M652		OUTPUT
0	-3	

S2

+3	0	L2
M652	
0	-3	

H2
SLOPE (NOTE 2)

N2

POWER:
A2 ——— +5V
B2 ——— -15V
C2, M2 ——— GRD

NOTES:
1. CONNECT TO OUTPUT WHEN NOT DRIVING 92 ohm COAX.
2. CONNECT TO GROUND PIN FOR 500 nsec RISE TIME SLOPE.

+3V
INPUT
0V

20nsec TYPICAL BETWEEN THRESHOLDS

0V
OUTPUT
-3V

t_r = 8 nsec NOMINAL
500 nsec WITH PIN H2 N2 GROUNDED

The M652 contains two non-inverting high-speed signal converters which can be used to interface the positive logic levels or pulses of the K and M Series to DIGITAL negative logic levels of −3 volts and ground. These converters provide current drive at a low output impedance so that system interconnections can be made using terminated 92-ohm coaxial cable. The converters operate at frequencies up to 10 MHz with typical output rise and fall times of 8 nsec. Propagation times for output rise and fall are typically 20 nsec. The slope of the output transition can be decreased by grounding an internal RC network, to avoid ringing on exceptionally long lines. The converter then operates at frequencies up to 1MHz.

INPUT	OUTPUT
0v	−3v
+3v	0v

Inputs: Positive logic levels of 0 and +3 volts (nominal). Input loading is 2 unit loads. Input signals more positive than +6 volts will damage the circuit.

Outputs: Each output can drive terminated 92 ohm coaxial cable and supply an additional 20 ma at ground or sink an additional 20 ma at −3 volts. Output rise and fall times are dependent on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds will be increased by connecting the 100-ohm resistor to the output.

Power: +5 volts, 20 ma; −15 volts, 150 ma (avg)

M652 — $26.00

K
SERIES

K SERIES

INTRODUCTION

High-speed, noise-sensitive computer electronics or awkward relay substitutes often impose limits in process control design, from the simplest transfer machine to the most sophisticated numerically controlled system. Digital Equipment Corporation's new low-speed industrial modules (K Series) eliminate this condition economically and reliably.

Computer-oriented logic, by its very nature, is high speed (1 MHz and above), and provides noise immunity far below that required in a process control environment. The upper frequency range of the K-Series modules is 100 KHz, with provision for reduction to 5 KHz for maximum noise immunity. These modules incorporate all silicon diodes, transistors, and integrated circuits, deliberately slowed.

Either English (non-inverting) logic or NAND/NOR logic is compatible with the K Series. The hardware for this series is specifically designed for standard NEMA enclosures. FLIP CHIP™ mounting hardware can likewise be used for rack-mounting, inasmuch as K-Series modules fit standard DEC sockets.

Proven FLIP CHIP™ connectors, used for years in applications from steel mills to lathe controls, provide modularity. Even the connection between terminal strips and electronics can be plugged for installing the logic after field wiring is complete, and removing it quickly for modifications or additions.

Checkout and trouble shooting is easy with K-Series logic. Every system input and output has an indicator light at its screw terminal. A special test probe provides its own local illumination and built-in indication of transients, as well as steady states. Every point in the system is a test point, and consistent pin assignments reduce the need to consult prints.

Construction materials and methods are the same as for other high-production FLIP CHIP™ modules, including a computer-controlled operating test of each complete module. K-series modules further offer the size reduction, reliability, flexibility, and low cost of solid state logic, with an added bonus of easy interconnection. FLIP CHIP™ industrial modules are ideal for interfacing high speed M-series or computer-systems to machinery and processes.

Sensing and output circuits operate at 115v ac for full electromechanical capability. Inputs from contact devices see a moderate reactive load to assure normal contact life. Solid state ac switches are fully protected against false triggering, and include provisions for interlocking. Voltage from the external environment are excluded from the wire-wrap connections within the logic.

SPECIFICATIONS

SUMMARY

Frequency range: DC to 100 KHz. Control points on each module allow reduction to 5 KHz for maximum noise immunity for critical functions. Signal levels: Ov and +5v, regardless of format used.

Fan-out: 15 ma available from all outputs; typical inputs 1-3 ma.

Waveforms: Trapezoidal. No fast transients to cause cross talk. External capacitive loading affects speed only; no risetime dependence.

Temperature Range: 20°C to +65°C on modules using silicon diodes and transistors. Modules using monolithic integrated circuits operate from 0°C.

Noise immunity: False 1:20 ma at 1.6v for 1.5 μsec typical. False "0":3 ma at 3v for 1.5 μsec typical. Time thresholds can be increased by a factor of 20 for critical points by wiring the slowdown control pins.

Power requirements: Single voltage supply, +5v ±10%. Dissipation typically 120 mw per counting or shifting flip-flop, 30 mw per control flip-flop, 25 mw per two-stage diode gate.

Control system voltage: 120 VAC, 50 or 60 hertz.
Mounting provisions: Standard NEMA industrial enclosures. May also be used in 19″ electronics cabinets.

GENERAL SPECIFICATIONS

Construction Features

K-Series modules include the quality features of the lines of FLIP CHIP modules: flame-resistant epoxy-glass laminates, all-silicon semiconductors, gold plated fingers and solid gold connector contacts. K-Series modules are constructed on module boards with the same dimension as the other lines of the FLIP-CHIP series and fit the standard DEC sockets. Thorough testing of each module is by computer operated automatic tester for most modules, or by specialized equipment for those which are not amenable to automatic test. A test specification sheet or data sheet is packaged with each module, including a circuit schematic for that type. Monolithic or hybrid integrated circuits are included wherever they can improve the performance-cost ratio. Versatile mounting hardware imposes as few physical constraints as practicable.
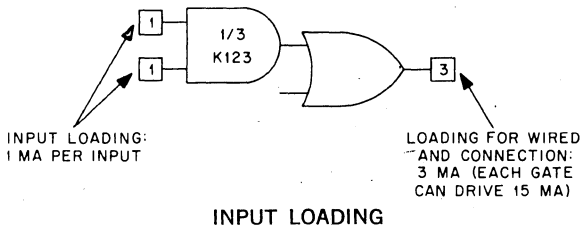
Logic Signals
There are no ultra-fast transients at any K-Series output. Logic signal "1" and "0" levels are essentially independent of fanout. Rise and fall transitions have controlled slopes which are not strongly influenced by normal changes in fanout, lead length, temperature, or repetition rate. The fastest K-Series trapezoidal logic signal can be fully analyzed with a 500KC oscilloscope. Logic "1" or "true" is +5 volts and logic "0" or "false" is zero volts except where redefined by logic designer. Counters and shift registers advance at the "1" to "0" transition and are cleared by a "0" level. Any unused input may be left open.

M-Series Compatibility
M-Series outputs can drive K-Series logic gates and output converters K604 and K644 directly, and any K-Series input after passing through a K-Series gate, provided they meet timing requirements.

Fanout and Fanin

K-Series fanout capabilities are sufficient to relegate fanout calculations to the final checking phases of logic design. Logic outputs from any module type can drive up to 15 milliamperes. Logic gate inputs consume 1 milliampere per input. Other loadings range from 1 to 4 milliamperes as indicated by the loading numbers enclosed in squares on each specification diagram.

INPUT LOADING:
I MA PER INPUT

LOADING FOR WIRED
AND CONNECTION:
3 MA (EACH GATE
CAN DRIVE 15 MA)

INPUT LOADING

Expandable gates give K-Series a fanin capability well beyond typical logic requirements. The most restrictive fanin limitation in K-Series logic concerns the wired AND configuration, for which several logic outputs are simply wired in common: the wired AND fanout capability is reduced to three milliamperes when the maximum of 5 outputs are tied together. The second level of logic (the OR node) within K113 and K123 gates is limited to less than 10 OR inputs to preserve output falltime control. The input AND gates of K113 or K123 modules may be extended with K003 expanders up to a maximum of 100 inputs, well beyond any practical requirement.

Operating Temperature

K-Series modules are designed for operation in free-air ambient temperatures between $-20°C$ and $+65°C$ (0°F to 150°F) except the following types which are restricted to 0°C 32°F minimum: K202, K210, K220, K230.

Speed

Many applications for K-Series modules involve operation at rates lower than relay speeds. Even at speeds many times faster than relay capabilities, timing need not be considered unless the logic includes a "loop". A flip-flop constructed of logic gates is such a loop, in which the output at a given point feeds back to influence itself, thus demanding input durations longer than total loop delay. Proper operation of such loops should be verified by calculation using the specifications below. For a complex loop an experiment should be made if possible to look for flaws in the calculations.

When anticipated repetition rates will be of the same order of magnitude as rated logic frequency, more care is required in timing design. K-Series circuits are intentionally slowed to the maximum extent practicable for 100 KHz operation, and the resulting propagation delays can limit complex logic systems to 50 KHz or even 30 KHz repetition rates. In addition, timing loops must be examined just as carefully in fast logic as in slow. If K-Series speed appears marginal or insufficient for the job at hand, use M-Series high speed logic modules.

Timing Characteristics for K113, K123, K202, K210, K220, K230	Min.	Time (μsec) Typ.	Max.
Logic Gate Propagation Delay, Output Rise (0V to +5V)	0.5	2.0	3.0
Output D only, when connected to pin B	7.5	40	180
Logic Gate Propagation Delay, Output Fall (+5V to 0V)	0.3	1.0	6.0
Output D only, when connected to Pin B	4.5	20	180
Count/Shift Input Propagation Delay, Output Rise	2.0	5.0	9.0
As above, but pin B grounded to pin C	10	30	100
Count/Shift Input Propagation Delay, Output Fall	1.0	4.0	9.0
As above, but pin B grounded to Pin C	10	30	100
Rise time, all unslowed outputs	2.0	5.0	9.0
Pin D outputs only, when connected to pin B	30	100	240
Falltime, all unslowed outputs	0.5	1.0	4.0
Pin D outputs only, when connected to pin B	7.5	20	120
Minimum time between successive input transitions on any module which has one or more Count/Shift inputs	4		
As above, but pin B grounded to pin C	10		

NOTE: Count Shift inputs are included in types K202, K210, K220 and K230 Exceptions: Input transitions at pins J and K may follow other input transitions with delays down to zero; For characteristics not listed above, see timing information on individual data pages.

Noise Immunity
Two properties of electrical interference often overlooked in evaluating logic noise immunity are its source impedance and its frequency distribution. Unless the digital logic is spread over several feet or yards so that high potentials can be induced in the ground system, most noise will be injected via very small stray capacitances and hence will have a high source impedance. The voltages at the noise source itself are usually measured in thousands of volts. Consequently, voltage thresholds alone cannot provide adequate noise rejection. On the contrary, the noise appears to come from a current source, so that logic circuit current thresholds are also an important measure of noise immunity.

Capacitance-coupled interference is strongest at the highest frequencies that can travel over wires to the logic from the noise source. Logic circuits which respond slowly can reject high frequency interference peaks that exceed dc current and voltage thresholds. K-Series modules get their outstanding noise immunity from a balanced combination of current, voltage, and time thresholds.

Important as good noise thresholds are, practical noise environments are only vaguely predictable, so that the following design features are probably still more important:

1. All field wiring is isolated from K-Series logic wiring pins.

2. Logic power is not transmitted outside the logic environment for contact sensing, etc.

3. W994 electrostatic shields may be plugged in to further isolate pilot circuit noise: see Construction Recommendations.

4. Plug-in module compactness keeps logic wiring short, to reduce noise injection capacitance, and confines the ground mesh for reduced ground noise.

5. Every third logic gate has optional slowdown control, ample for slow-down of all control flip-flops.

6. If all else fails, lack of risetime dependence permits any K-Series output to be loaded with 0.001 mfd to ground to further reduce imped-ance and speed of response.

K-Series Typical Noise Thresholds

False "1": 20 milliamperes, 1.6 volts, 1.5 μsec or 30 μsec.

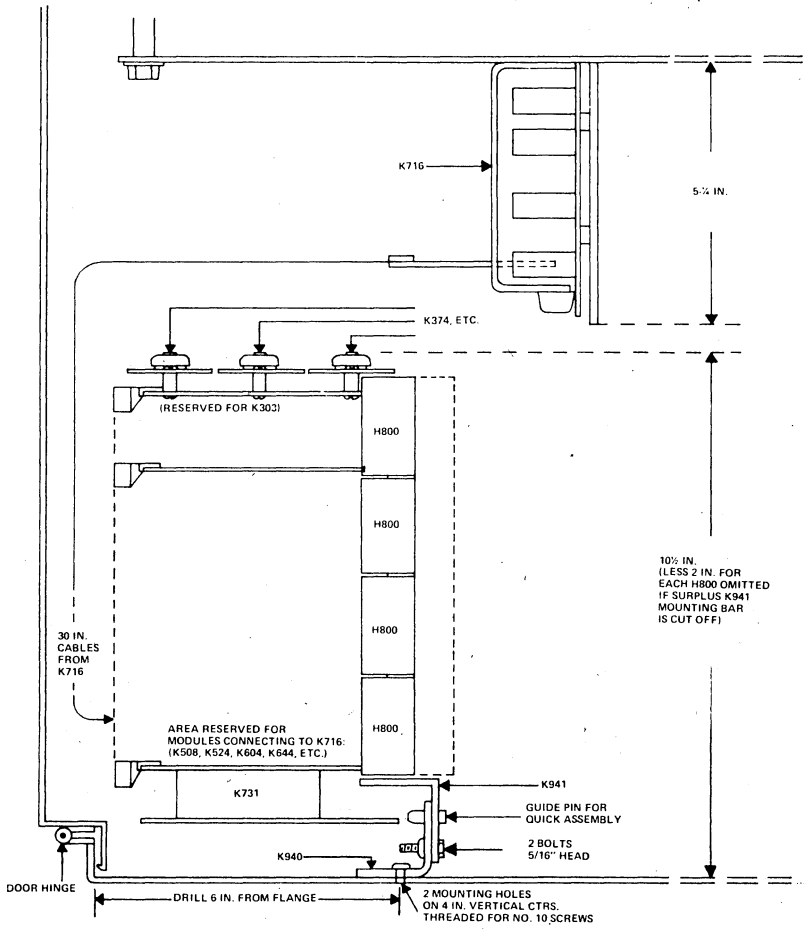False "0": 3 milliamperes, 3 volts, 1.5 μsec or 30 μsec.

NOTE: Both time and one other threshold must be exceeded simultaneously to produce a logic error.

Power Requirements

A simple 5 volt supply operates any K-Series system. Tolerance at room temperature: $\pm 10\%$. K-Series regulators K731 and K732 have a built-in temperature coefficient of approximately minus 1% for 3°C(5°F) to obtain full logic fanout over a wide temperature range and to minimize the tem-perature coefficient of K303 timers. Both regulators run from a nominal 12.6 volt center-tapped transformer secondary, with hash removed. See Construc-tion Recommendations for information about alternate sources of logic power. Logic power is not used for contact sensing; 120 VAC is specified to provide full compatibility with silver contacts and noisy environments.

Mounting

Mounting dimensions of K716, K731, K940 and K941 and a suggested arrangement in a NEMA 12 enclosure are illustrated below.
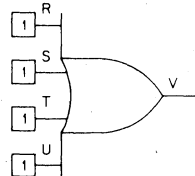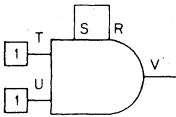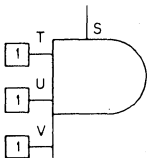
K716

5¼ IN.

K374, ETC.

(RESERVED FOR K303)

H800

H800

H800

H800

10½ IN.
(LESS 2 IN. FOR
EACH H800 OMITTED
IF SURPLUS K941
MOUNTING BAR
IS CUT OFF)

30 IN.
CABLES
FROM
K716

AREA RESERVED FOR
MODULES CONNECTING TO K716:
(K508, K524, K604, K644, ETC.)

K731

K941

GUIDE PIN FOR
QUICK ASSEMBLY

2 BOLTS
5/16" HEAD

K940

DOOR HINGE

DRILL 6 IN. FROM FLANGE

2 MOUNTING HOLES
ON 4 IN. VERTICAL CTRS.
THREADED FOR NO. 10 SCREWS

K-SERIES LOGIC IN A NEMA-12 ENCLOSURE, 16 IN. DEEP
TOP VIEW
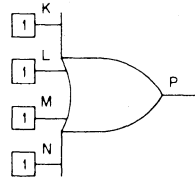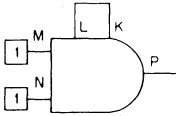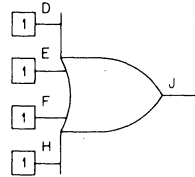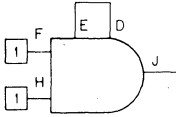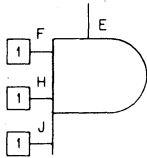
K003	K003	K012
AS EXPANDERS FOR	AS INDEPENDENT GATES	AS EXPANDERS FOR
INPUT AND GATES	FOR AND/OR EXPANSION	OR GATING IN K113
OF K113 OR K123	OF K113 OR K123	OR K123

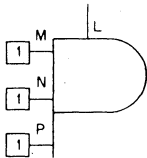These inexpensive gate expanders offer great logic flexibility and versatility without a proliferation of module types. Logic functions performed by expanders are illustrated in combination with the K113 and K123 gates.

K003 — $4.00
K012 — $7.00

Together with the K003 and K012 expanders, these gates perform any desired logic function, including AND, OR, AND/OR, NAND, NOR, exclusive OR, and wired AND.

Logic gate type K123 is an AND/OR non-inverting gate subject to expansion at either the AND or the OR node. Logic symbols and equivalents schematics are compared in the following illustrations. Typical pin connections are shown.

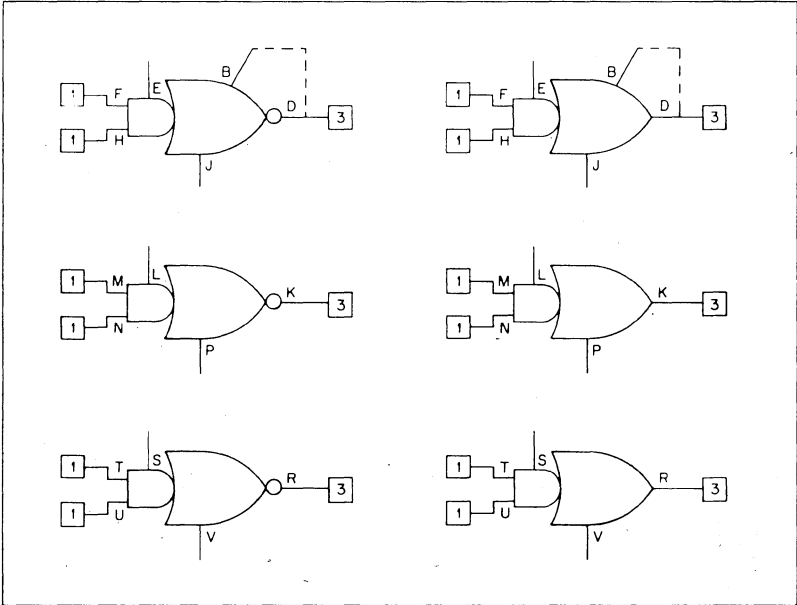The AND input can be expanded up to 100 inputs total. The OR input can be expanded, either by K003 and K012 expanders, up to 9 inputs total. More OR inputs can be added if faster fall times are acceptable.

Expansion of the K113 inverting gate is identical. The equivalent circuit is the same except for inversion in the output amplifier.

Both gate types include a slowdown capacitor that can be connected to the output of one circuit to increase its noise rejection when gates are interconnected to make control flip-flops. Use of this capacitor increases rise and fall time by approximately a factor of 20.
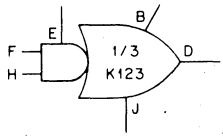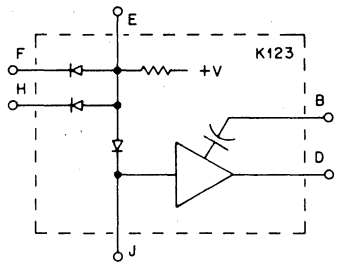
BASIC GATE
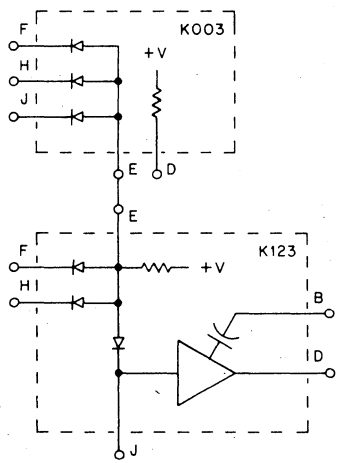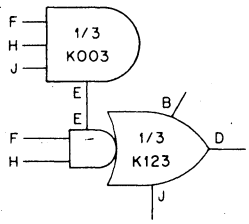
K003 AND EXPANSION
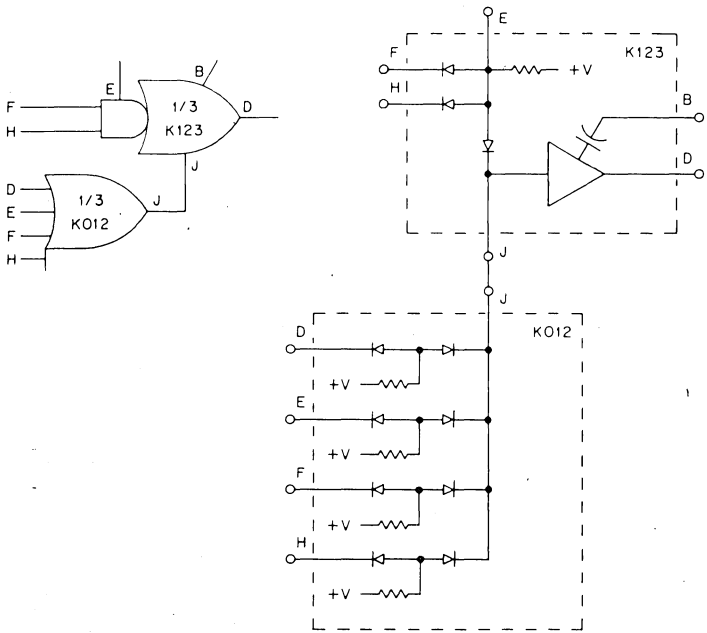
K012 OR EXPANSION

LOGIC   SCHEMATIC
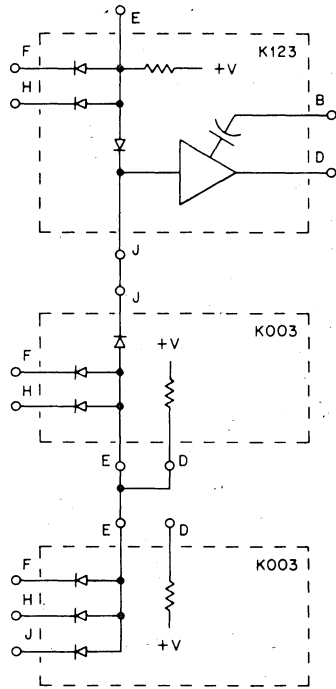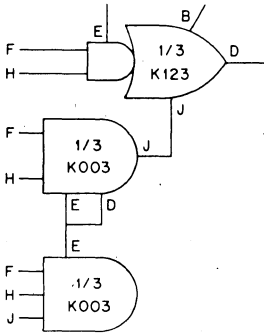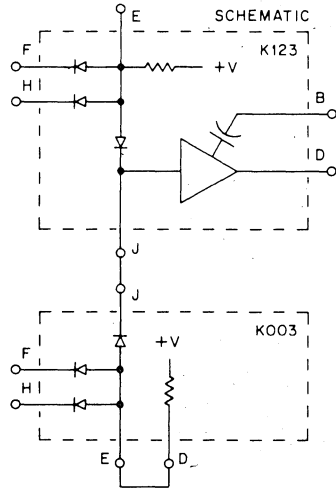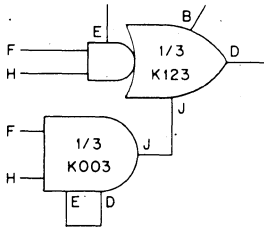
K003 AND/OR EXPANSION

86

The basic types of logic function obtainable by expansion are shown below for the K123 non-inverting gate. Logic functions for the expanded K113 inverting gate are identical except for inversion of the output. Letters refer to logic signal names rather than module pin numbers.

BASIC NON INVERTING GATE

AND/OR EXPANSION COMBINATIONS
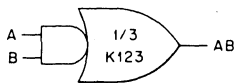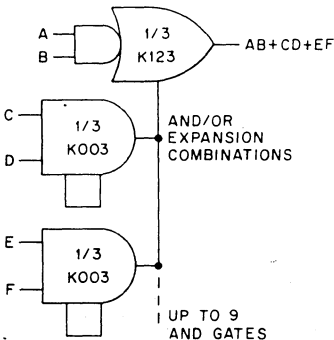
UP TO 9 AND GATES
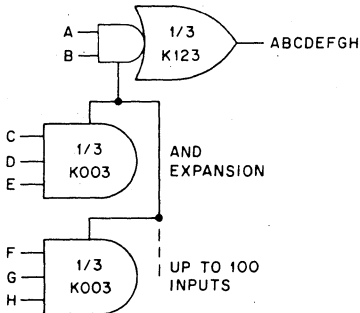
AND EXPANSION

UP TO 100 INPUTS
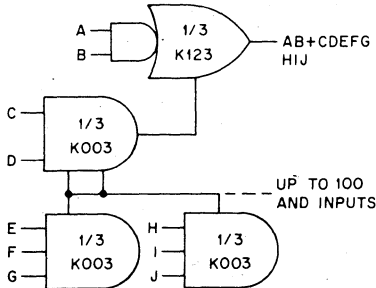
UP TO 100 AND INPUTS
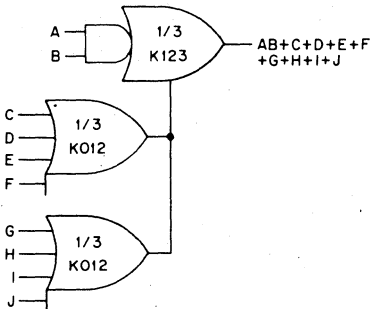
OR EXPANSION
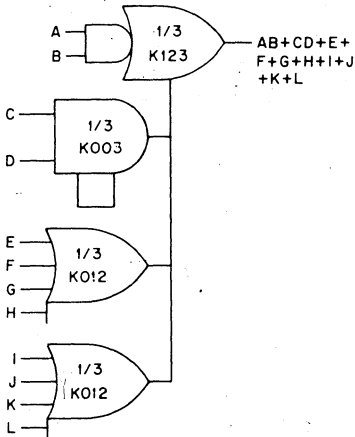
LOGIC FUNCTIONS WITH GATE EXPANSION

87

NAND, NOR, EXCLUSIVE OR

The K113 inverting gate performs the NAND function directly, and performs the NOR function when combined with a K003 expander.

With proper input connections and a K003 expander, the K123 non-inverting gate performs the exclusive OR function.

A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

NAND FUNCTION OF BASIC INVERTING GATE

UNUSED INPUTS
ACT AS ONES
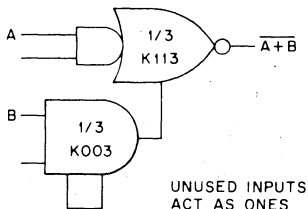
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

NOR FUNCTION OF BASIC INVERTING GATE
WITH EXPANDER
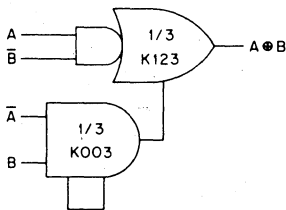
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

EXCLUSIVE OR CONNECTION OF BASIC
NON-INVERTING GATE WITH EXPANDER
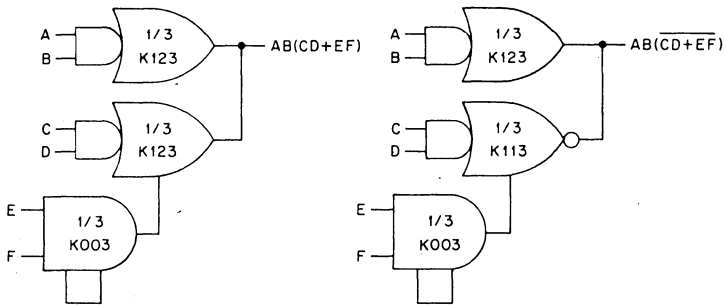
WIRED AND EXAMPLES

WIRED AND

Wired AND functions can be obtained by connecting K123 outputs to other K123 or K113 outputs as shown.

CONTROL FLIP-FLOPS FROM GATES

Control flip-flops can be formed by interconnection of gates as shown below.

INVERTING GATE CONTROL FLIP-FLOP

*USE SLOWDOWN
CONNECTIONS
IN FLIP-FLOPS
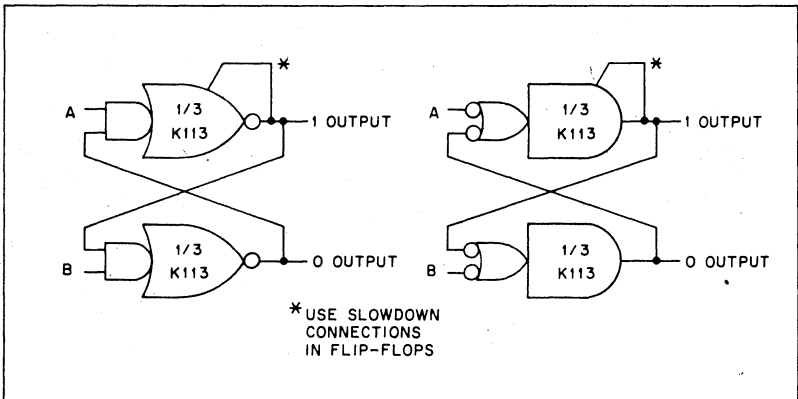
The flip-flops above, made from two inverting gates, provide complementary 1 and 0 outputs. A truth table is shown below.

TRUTH TABLE

A	B	1 OUTPUT	0 OUTPUT
0	0	1	1
0	1	1	0
1	0	0	1
1	1	NO CHANGE	

NON-INVERTING GATE CONTROL FLIP-FLOP
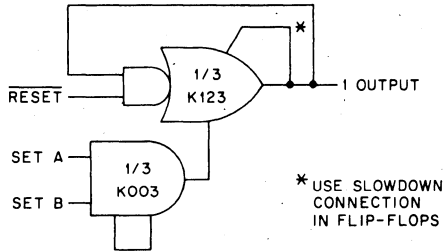
The output of the flip-flop above is set to a ONE when the two SET inputs are both ONEs. A ZERO at the RESET input returns the output to ZERO, provided at least one of the SET inputs is also ZERO.

PULSE GENERATOR FROM NAND GATES

An effective pulse generator is formed by adding a capacitor to the OR node of a K113 inverting gate, as shown below. The circuit converts positive level transitions to pulses for clearing flip-flops, etc. Pulse width is slightly greater than 1000 C: 1.0 microfarad produces 1.0 to 1.5 millisecond pulses, 0.01 microfarad produces 10 to 15 microsecond pulses. The input must remain low for several times the pulse width for reasonable pulse width consistency.
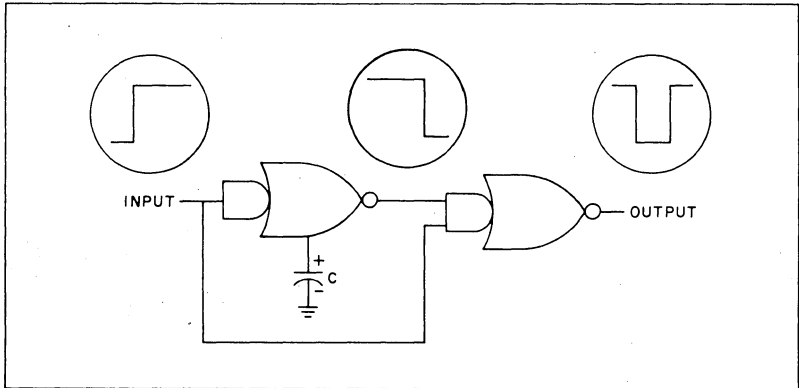
NAND GATE PULSE GENERATOR

K113 — $11.00
K123 — $12.00

FOR ZERO VOLTS DEFINED AS LOGIC ZERO standard definition			
Logic Function	No. of Inputs	Expanders	Gates
AND	2	none	1/3 K123
	3-5	1/3 K003	1/3 K123
	6-8	2/3 K003	1/3 K123
OR	2	1/3 K003 or 1/3 K012	1/3 K123
	3-5	1/3 K012	1/3 K123
	6-9	2/3 K012	1/3 K123
NAND	2	none	1/3 K113
	3-5	1/3 K003	1/3 K113
	6-8	2/3 K003	1/3 K113
NOR	2	1/3 K003 or 1/3 K012	1/3 K113
	3-5	1/3 K012	1/3 K113
	6-9	2/3 K012	1/3 K113

FOR ZERO VOLTS DEFINED AS LOGIC ONE (inverted definition)			
Logic Function	No. of Inputs	Expanders	Gates
AND	2	1/3 K003 or 1/3 K012	1/3 K123
	3-5	1/3 K012	1/3 K123
	6-9	2/3 K012	1/3 K123
OR	2	none	1/3 K123
	3-5	1/3 K003	1/3 K123
	6-8	2/3 K003	1/3 K123
NAND	2	1/3 K003 or 1/3 K012	1/3 K113
	3-5	1/3 K012	1/3 K113
	6-9	2/3 K012	1/3 K113
NOR	2	none	1/3 K113
	3-5	1/3 K003	1/3 K113
	6-8	2/3 K003	1/3 K113
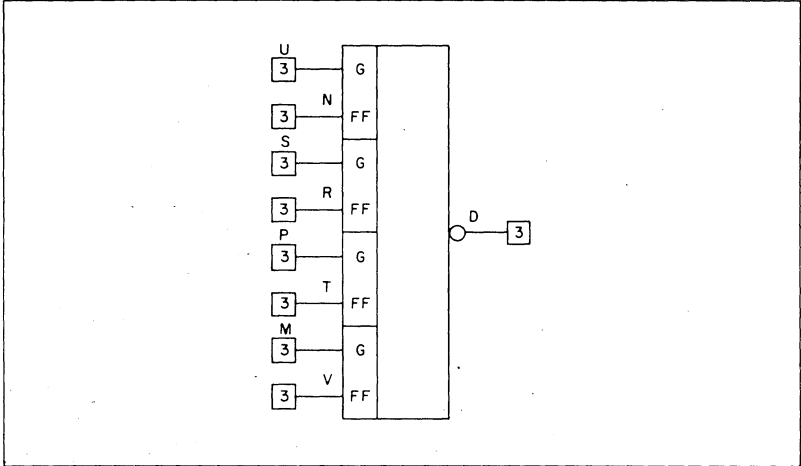
If the four outputs of K210 counter are wired to K184 "F" inputs, and a four bit binary fraction presented in reverse order to the corresponding "G" inputs, a pulse train is emitted at an average rate equal to the product of the K210 input rate and the binary fraction. Each transition from "0" to "1" at an EF input produces a 5 μsec output pulse to ground, if the corresponding "G" input has been high for 5 microseconds or more. Inputs are not rise-time sensitive. Outputs from several rate multipliers may be combined to give any desired precision. Rate multipliers are primarily useful for numerical control applications.

K184 — $18.00

93
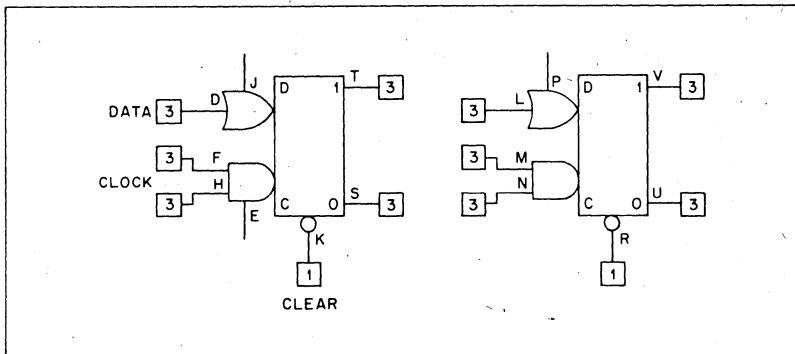
K202 flip-flops do shifting, complementing, counting, and other function beyond the capabilities of simple set-reset flip-flops built up from logic gates. They also may be used to extend K210 counters or K230 shift registers.

When the output of the CLOCK gate falls from high to low, the information at the OR input (pins D-J, L-P) is transferred into the flip-flop.

Pin J (or P) is ORed with the pin D (or L) input.

Like pins J and P of a logic gate, these pins can be driven only from a K003 or K012 expander.

Time is required for flip-flops and delayed inputs to adjust to new signals. The CLOCK gate output must not fall to zero sooner than 4 μsec after its own rise, the end of a CLEAR signal, or a change on associated SET input pins.

A K202 flip-flop is cleared by grounding the CLEAR input pin. The flip-flop is held in the zero state as long as the clear input is zero volts, regardless of other inputs.

K202 — $27.00
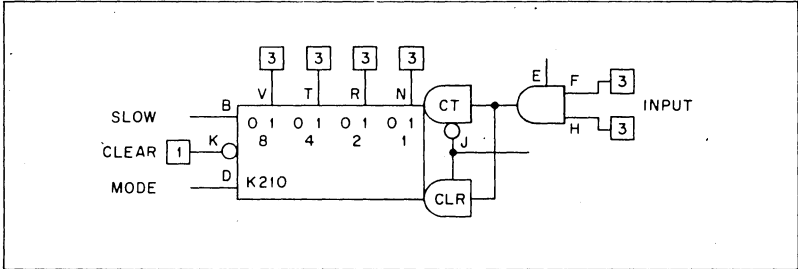
The K210 is a binary or BCD counter that can be wired to return to zero after any number of input cycles from 2 to 16. Count-up occurs when the COUNT gate output steps to zero. Decimal counting logic is built in; when pin D is unused, the counter resets to zero on the next count after nine. When pin D is grounded, the counter overflows to zero, after a count of 15. (Pin D is not intended for dynamic switching between binary and BCD counting.)

The counter is reset by grounding the CLR input for 4 microseconds or more. A positive level at the J input from a K003 expander also resets the counter when the COUNT gate output steps to zero.

Wire the K003 as a decoder to detect one count less than the desired modulus. (Detect 5 for a count-of-6 counter, etc.)
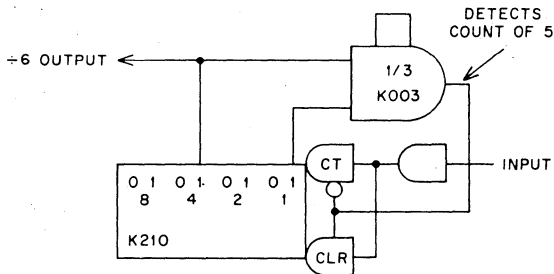
1/3 K003 AS 2-INPUT DECODER

For counts above 10, ground pin D. Combine two K003 expanders as shown below, where three counter outputs must be sensed (to divide by 12, 14, or 15).
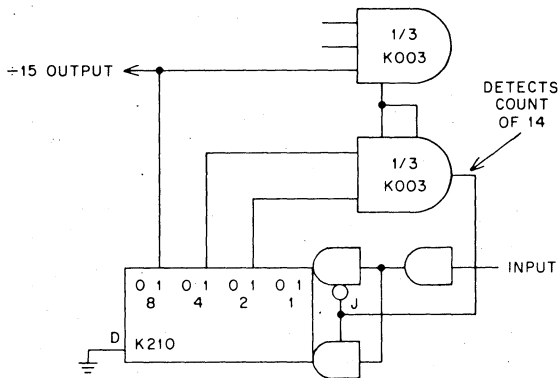
2/3 K003 AS 3-INPUT DECODER

Time is required for flip-flops and pin J reset logic to adjust to new inputs. The count gate output must not step to zero sooner than 4.0 μsec after its own rise, a change at pin J, or the end of a clearing signal at pin K. When pin B is grounded, the count gate output must not step to zero sooner than 50 μsec after its own rise or a change at pin J.

Larger counters are obtained by cascading K210's or adding K202 flip-flops. To cascade K210 modules, wire the most significant output of one counter to the input gate of the next. Inputs to the least significant stage can be either pulses or logic transitions to ground; risetime is not important.

Any transducer such as a switch, photocell, pulse tachometer, thermistor probe, or others compatible with K508 or K524 input converters can generate the signal which is to be counted. The lack of input risetime restrictions may allow transducer outputs to drive K210 counters directly if damaging transients can be avoided, as when the transducer shares the logic system environment.

For visual readout of binary-coded decimal counters, the four outputs from each K210 may be connected to corresponding input pins on a K671 decoding driver and display.

K210 — $27.00

Four flip-flops and all the gates needed for binary-coded decimal up counting, down counting, presetting, and clearing are built into the K220. Up-down counters are useful for many digital position readout and feedback applications.

The direction of counting is established by the signal at pin L, high for up counting and low for down counting. Pin L count direction changes should finish no later than 4.0 μsec before next count input.

When K220 counters are cascaded, a single connection from the "8" output of one K220 to the count input gate of the next establishes both carry and borrow propagation.

CASCADED K220 COUNTER

Up-counts occur when input makes the transition from high to low (± 5 v to 0 v), as in K210 and K230. Down-counts, however, take place on the transition from low to high (0 v to $+5$ v). Thus both carry and borrow signals propagate via the simple connection from 8-weight output to 10-weight input.

ONEs present at readin gate pins U,S,P, or M are read into the respective flip-flops when pin D makes the transitions from low to high. The transition at pin D should finish not later than 4.0 μsec before next count input. Transition from low to high at pin D should also begin no sooner than 4.0 μsec after any previous transition at pins D,M,P,S, or U. Ground any unused readin gate inputs to prevent readin of undesired ONEs.

Grounding pin J or K forces all flip-flops to zero for as long as either clear input remains low.

Time is required for flip-flops, counting logic, or readin gates to adjust to new inputs. No counter input may be changed within 4 μsec of a transition at any other input. (Refers to output of count gate). When pin B is grounded for slowdown, allow 50 μsec.

All connections are made on the upper connector.

K220 — $52.00

SHIFT REGISTER
TYPE K230

K
SERIES

SLOW

CLEAR

B

V T R N E F

SHIFT

0 1 0 1 0 1 0 1
8   4   2   1

K230

H

L

SERIAL
INPUT

U   S   P   M   D

READ IN

(DOUBLE-HEIGHT BOARD, ALL
CONNECTIONS ARE TO UPPER SOCKET)

Information presented to pin L of this four stage flip-flop register is shifted toward pin V with each transition from "1" to "0" at the shift input gate.

ONEs present at readin gate input pins M,P,S, or U are read into the respective flip-flops when pin D makes the transition from low to high. The pin D transition should finish no later than 4.0 μsec before the next count input. Transition from low to high at pin D should also begin no sooner than 4.0 μsec after any previous transition at pins D,M,P,S, or U. Ground any unused readin gate inputs to prevent readin of undesired ONEs.

Grounding pin J or K forces all flip-flops to zero for as long as the either clear input remains low.

Shift registers up to 20 bits long can be formed by tying pin V of one K230 to pin L of the next, and operating all shift gates together. Supply all shift pulses from the same device to maintain synchonism. The propagation delay of even one gate is too large a difference between two shift inputs on the same register. If more than 20 bits are required, duplicate the shift-generating logic and tie the outputs in parallel to all K230 shift gate inputs.

Time is required for flip-flops, shifting logic or readin gates to adjust to new inputs. No register input may be changed within 4 μsec after a transition at any other input. When pin B is grounded for slowdown no register input may be changed within 50 μsec after a transition at the shift, clear or serial input terminals.

K230 — $36.00

99

(DOUBLE THICKNESS MODULE)

Three magnetically latched mercury wetted contact relays in the K273 follow logic-level input information at rates up to 100 Hz, when pin E is grounded. Normally the OK Level output from a K731 source module drives pin E. When a line voltage failure is detected, pin E rises and each relay mechanically stores the last valid input data until full power returns.

K273 — $72.00
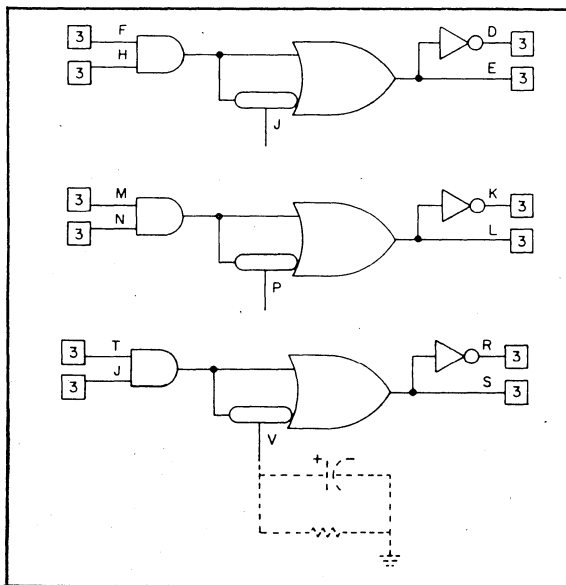
K303 timers provide time delays from 10 microseconds to 30 seconds and can be interconnected to form clocks with periods covering the same intervals. Fixed or adjustable delays and frequencies are obtainable. Calibrated controls are available (K371 through K378) for mounting directly on the K303. Remote controls can be added, if desired. A simplified schematic of the K303 is shown below. Note that the comparator has hysteresis, increasing the rejection of false "1" noise peaks at the input.
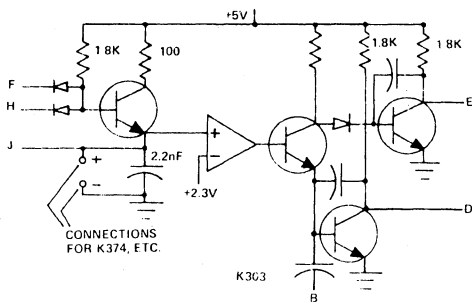
K303 TIMER SIMPLIFIED SCHEMATIC

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When a K303 input gate steps to zero, the uninverted output falls after a controlled interval, while the inverted output rises. The interval can be as little as 10 μsec or as long as 30 seconds, depending on the size of the R and C connected to pin J,P, or V. Recovery begins when the input gate rises to 1. Allow recovery time of at least 0.3% of the maximum delay obtainable from the capacitor, in order to guarantee 95% repeat accuracy in the delay.

NOTE
K374, K376, K378 PROVIDE
TIMING COMPONENTS FOR
THIS CIRCUIT.
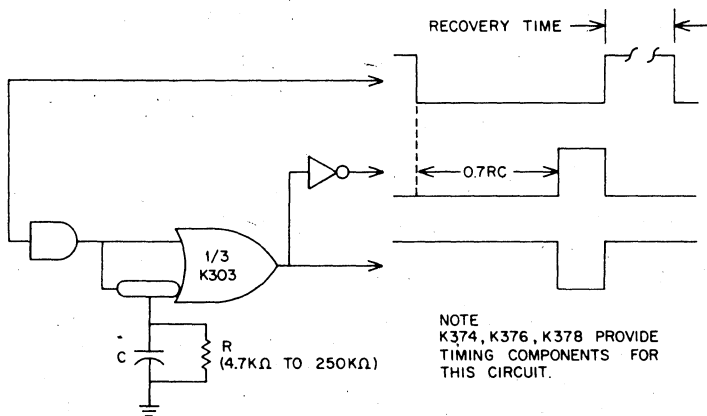
1/3 K303 AS OFF DELAY

A positive step at the input gate resets the K303 timer outputs. If the step occurs before a timeout is complete, the timeout is terminated and no change appears at the outputs. This property is sometimes convenient for establishing a pulse repetition rate threshold.

A built-in 2.2 nanofarad timing capacitor assures adequate noise rejection when external capacitors are mounted several inches from the timer. Time threshold for resetting is always several percent of rated recovery time, so that noise rejection time increases in proportion to the size of the timing capacitor. Remote rheostats and timing capacitors may be used, but noise rejection will be degraded. If several timing capacitors will be switch selected, wire in the smallest near the module and switch the others in parallel with it.

Variable or fixed timing resistors used with K303 timers may be any carbon composition, film, or wirewound rheostat or potentiometer. Delay time is linearly proportioned to resistance from 250KΩ down to a few thousand ohms, falling to zero (reset inhibited) below a few hundred ohms. Momentary shorting to ground of control pins will not cause damage, but a padding resistor of at least 300Ω in series with variable controls is advisable both to prevent continuous grounding and to avoid confusion which may arise if resetting is inhibited.

Timing capacitors may be any ordinary mica, paper, ceramic, or low leakage electrolytic type. For delays above a few seconds, wet slug tantalum electrolytic capacitors are advisable to avoid leakage induced drift at high temperatures. Temperature coefficient of delay has been optimized for the carbon composition potentiometers and tantalum electrolytic capacitors used in the controls described below, and is typically less than $\pm 1\%$ in 5°C (9°F) using K731 and K732 regulators for power.

K303 — $27.00

K371

PROVIDES TIMING COMPONENTS
FOR OPERATION OF 3/3 K303
AS CLOCK FROM 6 K Hz to
200 K Hz.

K373
K375

PROVIDE TIMING COMPONENTS
FOR OPERATION OF 2/3 K303 AS
CLOCK:

K373: 600 Hz to 20 Hz
K375: 60 Hz to 2 Hz

K374
K376
K378

PROVIDE TIMING COMPONENTS
FOR INDIVIDUAL (1/3) K303
DELAYS:

K374: 0.01 to 0.3 SEC
K376: 0.1 to 3.0 SEC
K378: 1.0 to 30 SEC
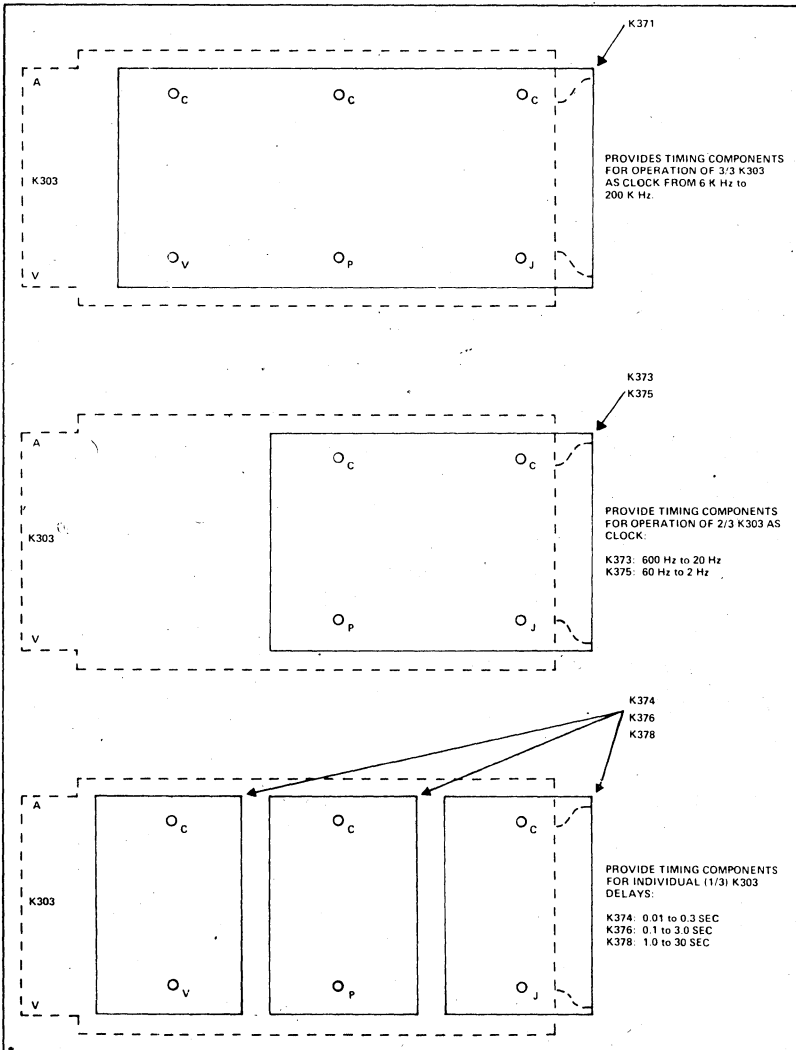
Calibrated controls for timers and clocks are available in several ranges. They mount to the K303 module by two screws per circuit, providing both mechanical and electrical connections. Each control includes a logarithmic potentiometer for easy settling over the full 30:1 calibrated range. Calibrations are approximate, meant for quick setup and easy control identification. Accurate time settings require the use of an oscilloscope, stopwatch, or other reliable time standard. These controls are intended for use at the end of K941 mounting bars; see Construction Recommendations.

K371 — $8.00
K373 — $8.00
K374 — $7.00
K375 — $8.00
K376 — $7.00
K378 — $9.00

SCREW TERMINALS

SOCKET B

K716 INTERFACE BLOCK

CONNECTOR BOARD

K508

RIBBON CABLE

120 VAC

120-VOLT INDICATORS

CHASSIS GROUND

AC/DC CONV.
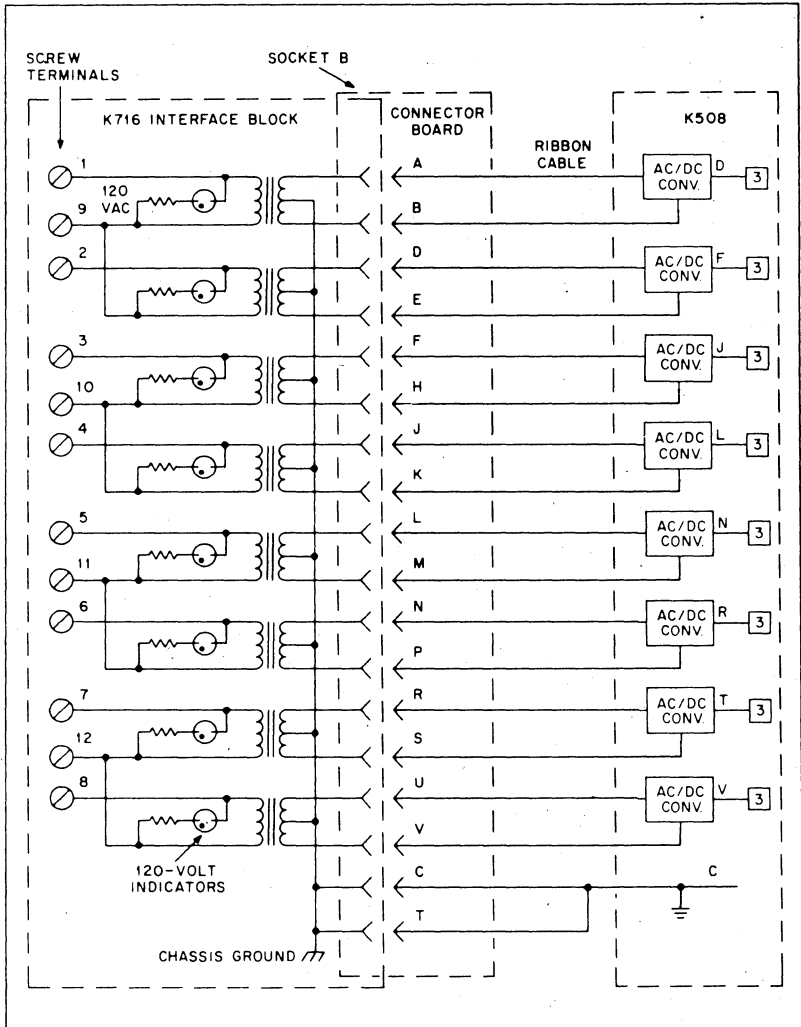
The K508 AC input converter, operating through the K716 interface block, is designed for use with ordinary silver contacts in limit switches, pressure switches, pushbuttons and the like. Each input terminal presents a reactive load of 1.5 volt-amperes, which together with an external 120 volt AC pilot circuit voltage inhibits contamination buildup at the contact surface.

Electrical noise riding on pilot circuit wiring is attenuated in the input transformers and by hash filters at the K508 module. Contact bounce filtering is designed to respond to the first signal, and to leave the logic output in the "1" state in spite of skips lasting up to 100 milliseconds.

K508 output circuits have hysteresis, so that no intermediate output state can result from an ill-defined input condition. No separate Schmitt-triggers are required. Outputs are at ground for no input, at +5 volts when energized. All connections use upper connector.

K508 — $44.00

SENSOR CONVERTER
TYPE K524

K
SERIES
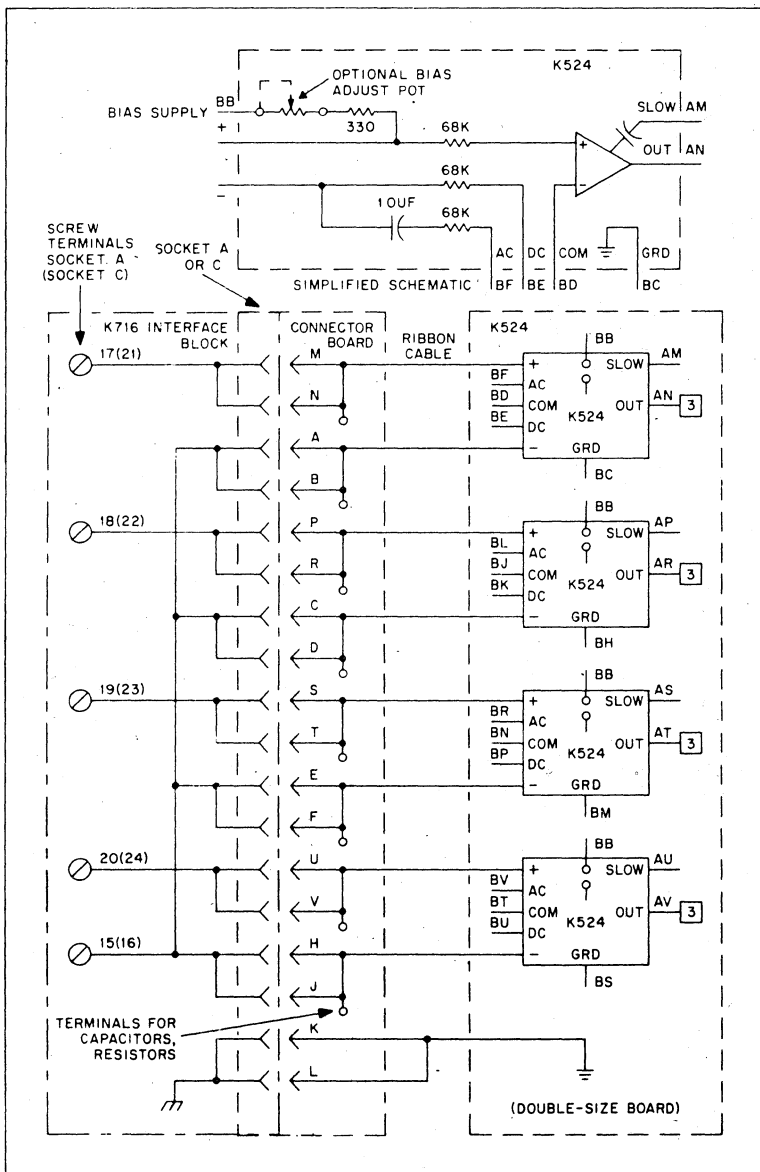
*See application section

The K524 Sensor Converter, operating through the K716 interface block, senses voltage transitions or resistance thresholds by noise-rejecting differential simplification. A choice of AC or DC coupling is provided.

Output transitions occur when input voltage differentials are within 0.3 volts or less. When the "+" input is more positive, the output is a ONE. When the "+" input is more negative, the output is a ZERO.

Both direct and AC-coupled positive feedback are included in the amplifiers to neutralize the effects of noise and insure well-defined logic level outputs.

Component terminals on the connector board accept capacitors or resistors across input lines to aid in removing noise or ringing.

Noise voltages common to both sides of the sensor leads are reduced more than ten times compared to the sensor output itself when AC input coupling is selected, and at least twenty times when direct coupled. Negative amplifier inputs in the range from -5 volts to $+10$ volts can be converted without error, even though the positive input swings as far as ± 30 volts. Accidental contact of K524 inputs with the 120-volt AC line is harmless.

When a resistive sensor is used, pin BB (pin B on lower connector) must be connected to an independent bias supply, such as separate K731 operated from a separate transformer, to insure against damaging currents through the bias circuits to the logic in case of accidental high voltages at K524 inputs. This precaution is most essential in systems containing K604 or K644 output converters, since inadvertent use of the wrong K716 socket is possible. This problem does not arise with self-generating sensors or where bias is supplied externally to variable-resistance sensors.

K524 — $98.00
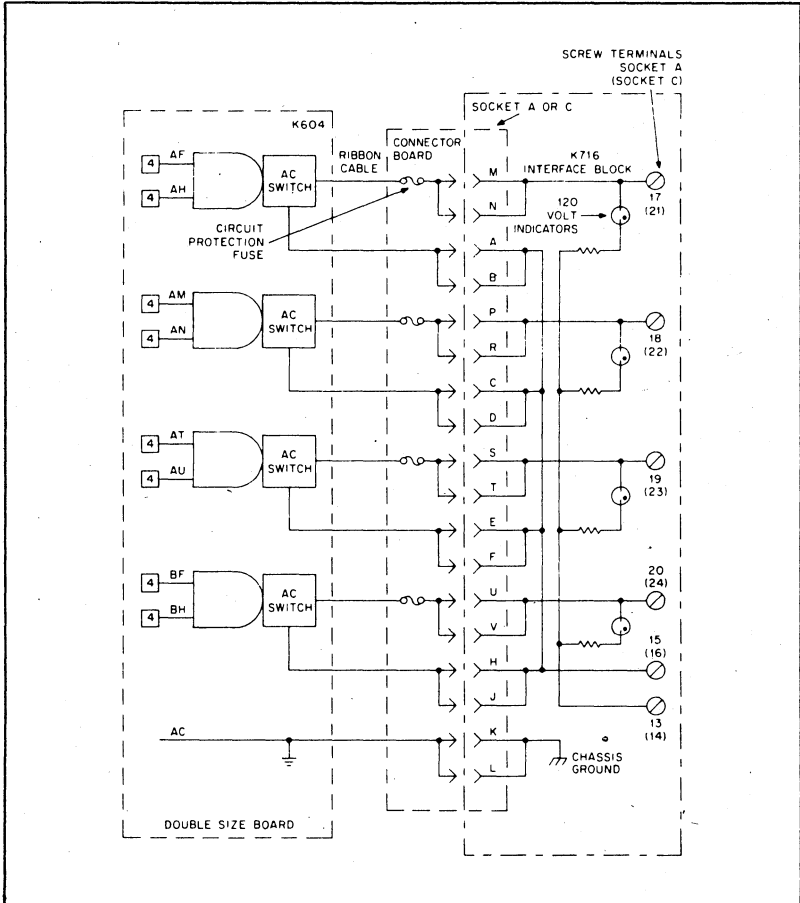
Operating in conjunction with the K716 Interface Block, the K604 permits AC operated valves, solenoids, small motors, motor starters and the like to be controlled directly from K-Series logic. Each circuit can handle up to 250 volt-amperes continuously. Total for any module, however, should not exceed 500 volt-amperes averaged over one minute. Ratings below include maximum horsepower based on use of Allen-Bradley type K^R motor starters. Less sensitive starters or relays may have significantly reduced capacity.

Maximum Capacity, each K604 circuit (120 v AC lines)						
Condition	Continuous V.A.	Inrush V.A.	Motor Direct	Type K Starter	208/220 Max. H.P.	480/600 Max. H.P.
With Fuse	250	600	1/20 H.P.	Size 3	30	50
No Fuse	250	1800	1/10 H.P.	Size 4	50	100

Littelfuze[R] type 275005 fuses provide fault protection for the triac output circuits. The fuses are mounted by clips on the connector board for easy replacement. Without the fuses, short circuits will destroy the module. The no-fuse information above is for reference only, and operation without fuse protection cannot be recommended. Circuits cannot be paralleled to increase ratings.

AC switch turnon takes place within 500 microseconds after input logic gate goes high. Turnoff takes place at zero crossings of the current. Maximum "off" leakage: 10 ma RMS at 140 VAC. Line voltage rating: 100 to 140 VAC, 50 to 60 Hz. Each triac output circuit has 400-volt breakdown rating. Shunt capacitor and shunt clipping devices inhibit false triggering on line transients.

Two special precautions are made necessary by the presence of AC line voltages on the K604 module. First, always disconnect the ribbon cable connector before inserting or removing a K604 or an adjacent module, to avoid shocks or component damage. Second, W993 copper-clad boards ($4 each) should be installed between K604 modules and all other types except K508 or K644. With the pin A connection cut away, on either the board or the socket, the W993 copper clad board acts as an electrostatic shield. If this added interface protection is later found to be unnecessary, the sockets reserved for shield boards can be used to add logic features, modifications, etc. Refer to Construction Recommendations.

K604 — $82.00

SCREW
TERMINALS
SOCKET A
(SOCKET C)

SOCKET
A OR C

K644

RIBBON
CABLE

CONNECTOR
BOARD

K716
INTERFACE
BLOCK

4 AF
4 AH
DC
DRIVER
M
N
17
(21)

A
B

4 AM
4 AN
DC
DRIVER
P
R
18
(22)

C
D

4 AT
4 AU
DC
DRIVER
S
T
19
(23)

E
F

4 BF
4 BH
DC
DRIVER
U
V
20
(24)

AB
AC
BB
BC
H
15
(16)

J

K

L

CHASSIS
GROUND
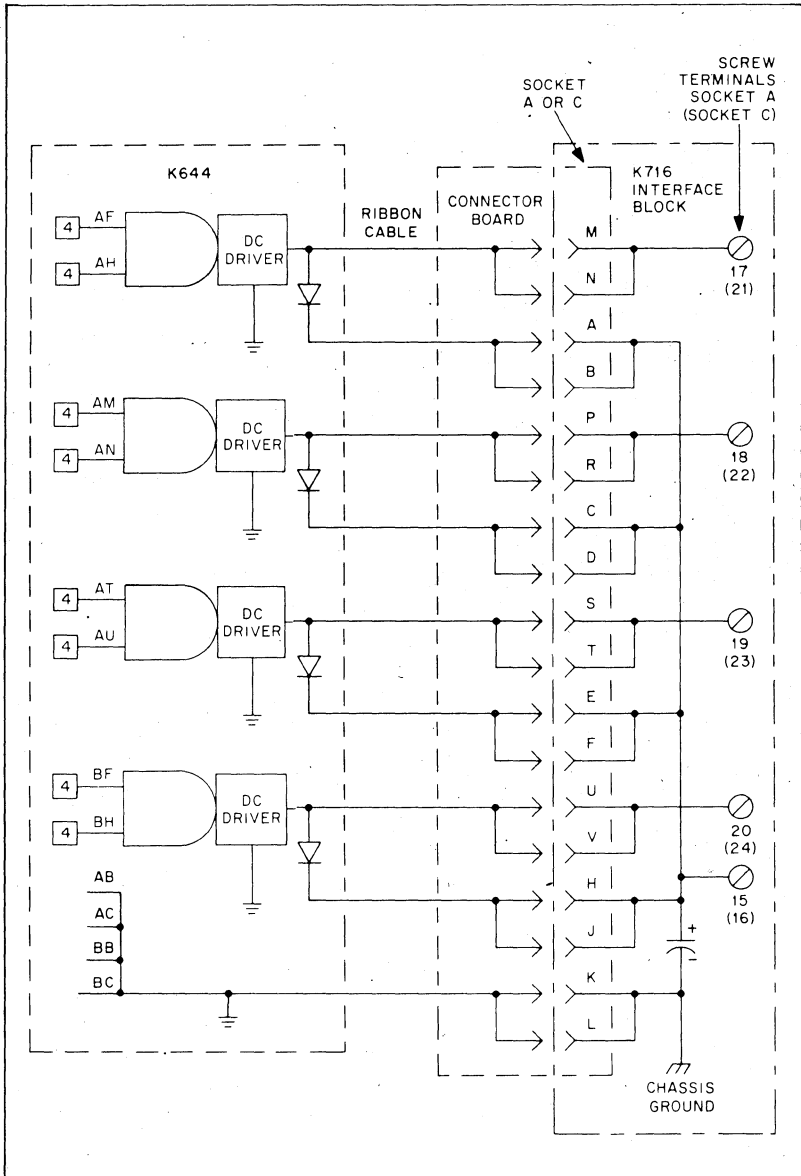
Operating through the K716 Interface Block, the K644 DC Driver permits stepping motors, dc solenoids, and similar devices rated up to 2.5 amperes at 48 volts to be driven directly from K series logic. Built-in clamping diodes protect switching transistors from transient over-voltage.

Total output circuit current for the K644 module must not exceed 4 amperes averaged over any 1 minute period. The ribbon connector should be unplugged before inserting or removing a K644 module.

Moving the parts of a magnetic device changes the winding inductance. To equalize magnetic field turnoff and turnon times, the ratio of inductance to total circuit resistance must be held constant. This demands more resistance in the circuit during turnoff, when the inductance is higher. Resistance may be inserted between K716 terminal 15 (or 16) and the load supply to achieve this, provided the K644 output voltage will not exceed 55 volts. Whether resistance is added or not, these clamp return terminals must be connected to the load supply to protect the module from overvoltage during turnoff.

K644 — $66.00
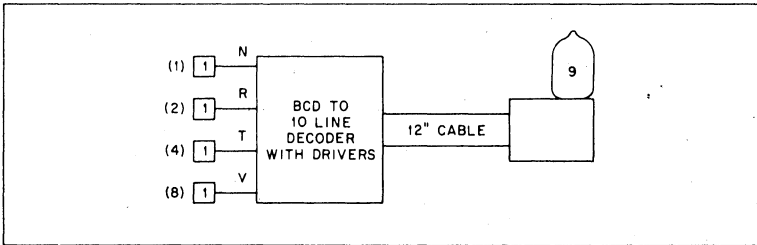
This module has two parts separated by a 1-foot ribbon cable. One part plugs into any module socket, the other contains a side-viewing Burroughs type B-5440 long life NIXIE glow tube on a mounting board. Four connections to corresponding module socket pins of a K210 or K220 binary-coded decimal counter completes the input wiring. The display tube board attaches with two screws to a K771 supply for both mechanical mounting and power supply electrical connections. Displays up to 6 digits long can be stacked on each K771 supply. Stacked digits have 0.8" mounting centers. See Construction Recommendations before assigning module locations.

K671 — $43.00
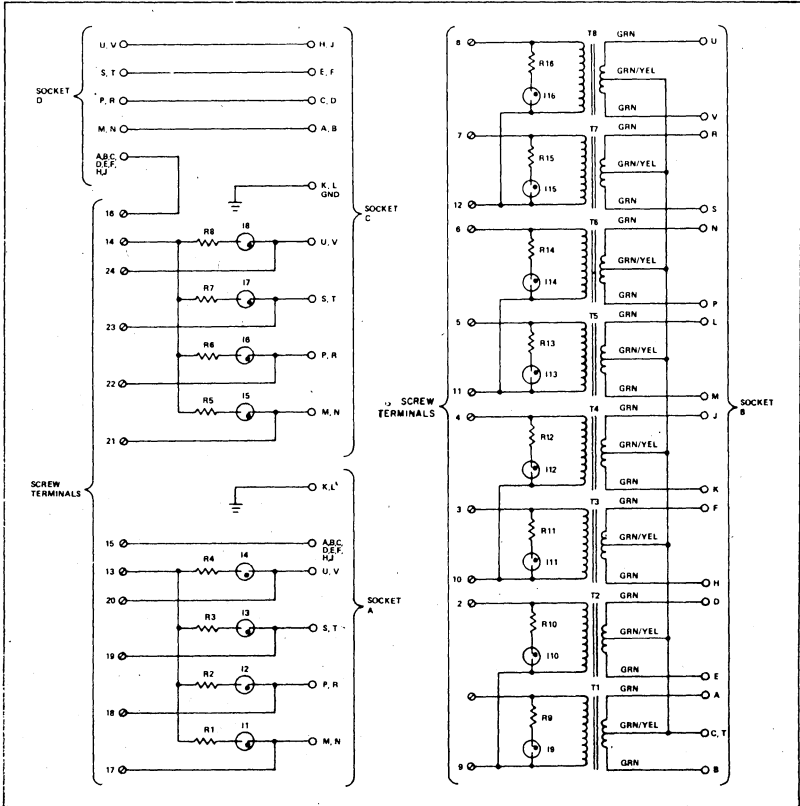
K716 INTERFACE BLOCK
SCHEMATIC

PROJECTS 5 1/2"
ABOVE MOUNTING
SURFACE

FROM THIS SIDE

RIBBON
CABLES
FROM
MODULES

CONNECTOR
MODULES:
A IN FRONT,
B,C,D BEHIND

SPACE
FOR
TERMINAL
MARKING

WIRES APPROACH

12 1/2"
MTG.
CTRS.

13"
OVERALL

1
2
3
4
5
6
7
8
9
10
11
12

13
14
15
16
17
18
19
20
21
22
23
24

1"
CLEARANCE
REQUIRED

2"

4"
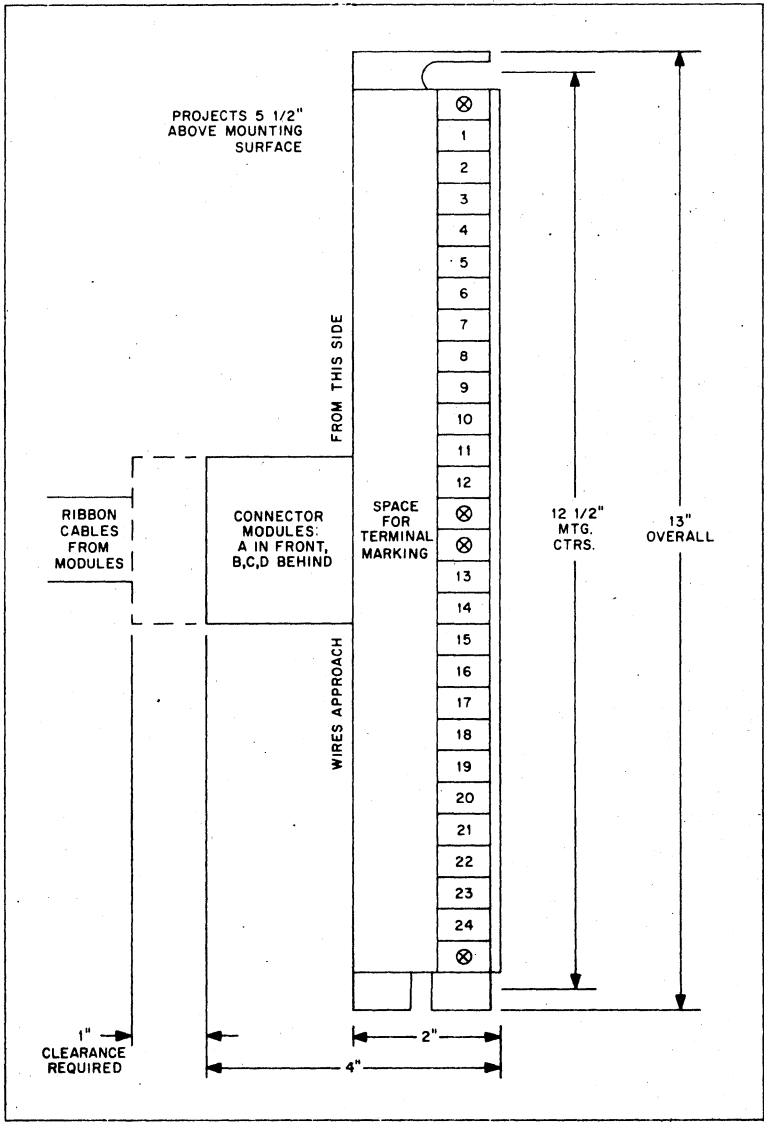
K716 INTERFACE BLOCK
FRONT VIEW

The K716 Interface Block serves as an interconnection interface for those K-Series modules that communicate with external equipment. External field wiring terminates at a 24-terminal screw connection block that accepts plain stripped wire up to 14 gauge. No separate crimped or soldered terminals are required.

Ribbon cables from the K-Series interface modules connect to printed circuit board sockets on the K716. This allows the K716 terminal block to mount on the rear panel of a NEMA enclosure for the convenience of electricians, while the digital system itself mounts on the door for easy access to both modules and logic wiring. The ribbon cable makes neat, simple wiring layouts and easy flexing at the hinge.

The three sockets in the K716 terminal block contain the same module-connector system used for the modules themselves, permitting quick disconnect of the entire logic system without affecting reliability. This arrangement, together with the K940-K941 bolt-on mounting hardware, allows initial checkout of control systems away from the site, as well as minimizing downtime in case of failure. (See Construction Recommendations.) The cable sockets have the same reliable gold contacts as K-Series module sockets.

Socket B, for use with the K508 AC input converter, is fed by eight isolation, stepdown and contact loading transformers contained within the aluminum shell of the K716. The transformer primaries receive 120-volt pilot signals from external contact closures. Each input is monitored by a neon indicator.

Sockets A and C are for use with K524, K604, and K644. Neon indicators are provided to monitor the outputs of the K604 Isolated AC Switch module.

All neon indicators are located within the K716 shell, visible at the rear of the associated screw terminals.

Socket D, normally terminated by a shorting plug, runs all return lines from connector C to a common point. If the shorting plug is removed, independent wiring of connector C return leads for K524 or K604 modules is possible. A W021-06R-W021 cable connector ($8.60) must be installed between socket D and socket A. An extra 2-inch clearance is required by this connector board. Independent wiring provides connections for four two-wire circuits instead of 8 circuits with bussed ground.

The drawing above shows approximate dimensions of the K716. Mounting slots clear no. 10 screws and allow compensation for mounting screw location tolerances.

(See Construction Recommendations.)

Below is a recommended mounting pattern for combining many interface blocks. This pattern can be extended provided the 30" reach of ribbon is not exceeded.

K716 Mounting Dimensions

Height:	13"
Width:	2"
Depth:	$5\frac{1}{4}$"
Mounting Centers:	$12\frac{1}{2}$"
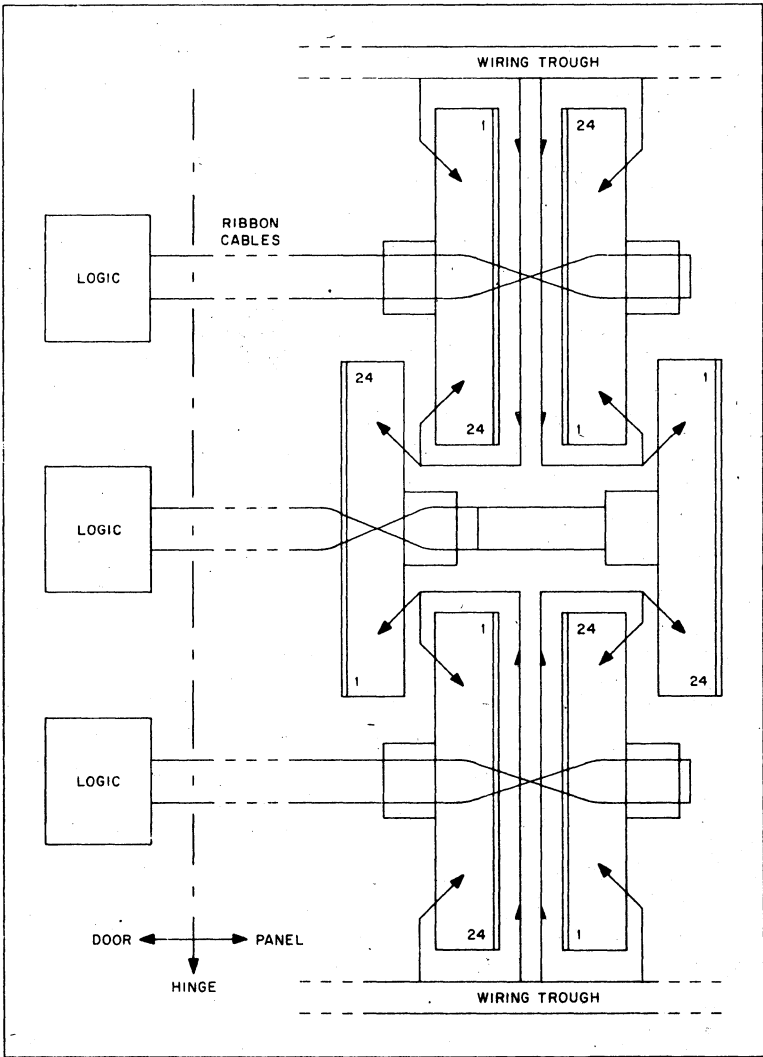
K716'S IN INDUSTRIAL ENCLOSURE

K716 — $90.00

```
        12.6VCT
     TRANSFORMER
     ┌─────┐                    C ┌──────────────┐ A
     │ 120 │                      │              │ ──► +5VDC, 1 AMPERE
     │ VAC │                    U │  RECTIFIER AND│ D
     └─────┘                      │   REGULATOR  │ ○─► TURN ON
                                  │     K731     │ E
                                  │              │ ○─► OK LEVEL
                                V │              │ F
                                  └──────┬───────┘ ──► LINE SYNC
                                         S
                                  SENSING OUTPUT
                                    (TO K732)

                            (TRIPLE. THICKNESS MODULE)
```
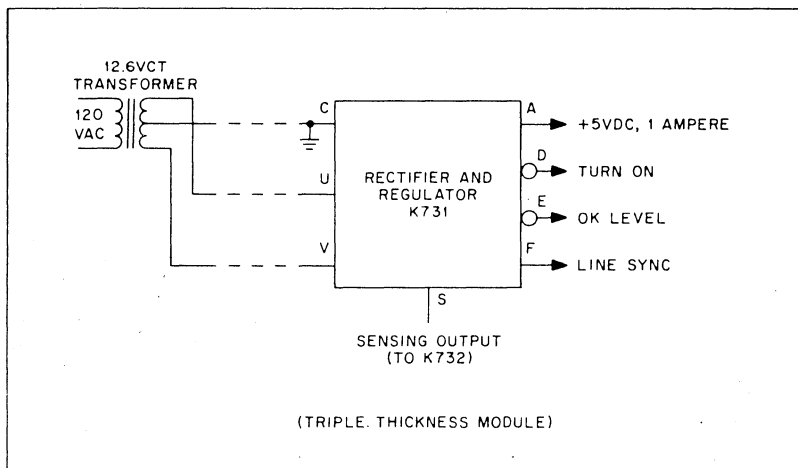
The K731 supplies +5 volt dc power to pin A of all K-Series modules and provides several specialized once-per-system control functions. Any source of center-tapped 12.6 v (50 or 60 Hz) allows the K731 to deliver up to 1 amp dc, which is sufficient to operate most typical control systems of up to 32 modules. The K731 is short-circuit proof.

This module is normally plugged into one of the innermost sockets on a K941 mounting bar, where its large components occupy space otherwise unused.

The TURN-ON output goes to ground during the power-up transient, and remains at ground until after the supply voltage has fully reached its quiescent value. It may be used to initialize flip-flops to a known starting condition.

The OK level output goes to ground when the supply voltage reaches 90% of its final value, and returns positive when less than 90% of full voltage is available. It is normally used as an enabling input to the K273 Retentive Memory module.

The line sync output allows a K113 or K123 gate to switch in synchronism with ac supply zero-crossings. This permits the line frequency to drive a real-time clock, or serve as the standard in a phase-locked loop with K303 timers, where higher frequencies must be synchronized with the line. Line sync fan-out is limited to 1 ma (for high fanout, use K113 or K123 for distribution). None of the K731 logic outputs may be used to obtain the OR function, and they may not be wired to any other output.

K731 delivers up to 1 ampere when used with a 12.6 volt transformer rated for 105-130 volt line; calculate loading from module data below. For 5% input voltage reduction (12.0v transformer or 100 volt line) the output current capability decreases 10%. Output voltage temperature coefficient is typically minus 0.1%/°C.

NOTE: For Module current requirements, see K Series Module Summary.

K731 — $24.00

K SERIES MODULE CURRENT REQUIREMENTS

Type	Current	Type	Current
K003	3 ma	K303	30 ma
K012	12 ma	K508	65 ma
K113	17 ma	K524 (transducer bias plus)	
K123	18 ma		45 ma
K184	60 ma	K604 (all circuits off)	40 ma
K202	110 ma	(additional per enabled circuit)	20 ma
K210	150 ma	K644 (all circuits off)	20 ma
K220	220 ma	(additional per enabled circuit)	100 ma
K230	150 ma		
K273	50 ma	K671	13 ma

```
                                              A    +5VDC, 3 AMPS
12.6VAC                      U                      (TO PIN A,
   CT                                              ALL MODULES)

                             C    K731            TURN ON
120
VAC
                             V                    OK LEVEL

                                 S               LINE SYNC
                      SENSING
                      LEVEL                       GROUND
                             U    S               (TO PIN C,
                                  A               ALL MODULES)

                             C    K732
                                  SLAVE
                                  REGULATOR

                             V
   * HASH FILTERS
     (SEE CONSTRUCTION
     RECOMMENDATIONS)


              (FOUR MODULES THICK)
```

This module is normally tied to corresponding pins A,C,S,U, and V of a K731 Source. For each unit of current emitted by the K731, the K732 emits two. Up to three K732 slaves can be controlled by a single K731 for a total system current of 7 amperes. Since K731 modules may not be paralleled, systems demanding more than 7 amperes require separation of pin A wiring.

In high-current systems, use short heavy wires for transformer secondary connections. Loss of 5% of secondary voltage in either ground return or transformer output leads will reduce regulator current ratings more than 10%.

K732 — $28.00

3/8"

2"

2 3/4"

2 3/4"

(SHOWN WITH 3 K671'S)

Shown above from the viewing side, the K771 supplies power and a conveni-
ent two-screw mounting for up to 6 K761 display tubes. Display tubes are
stacked to the left, the first tube board being attached to the K771. The
second tube board attaches to the first, and so on. Board mounting screws
provide both mechanical mounting and electrical power connections. The two
panel mounting screw locations dimensioned above have no. 6 steel threaded
inserts. Several 1" holes using a standard chassis punch may be cut on 0.8"
centers for viewing display tubes. To seal opening against dust, a 3" by 3-6"
piece of Lucite® or Plexiglas® may be assembled between display and mount-
ing surface. Power (120v AC) enters the supply from a terminal strip at the
rear. Total depth behind mounting surface: 4"
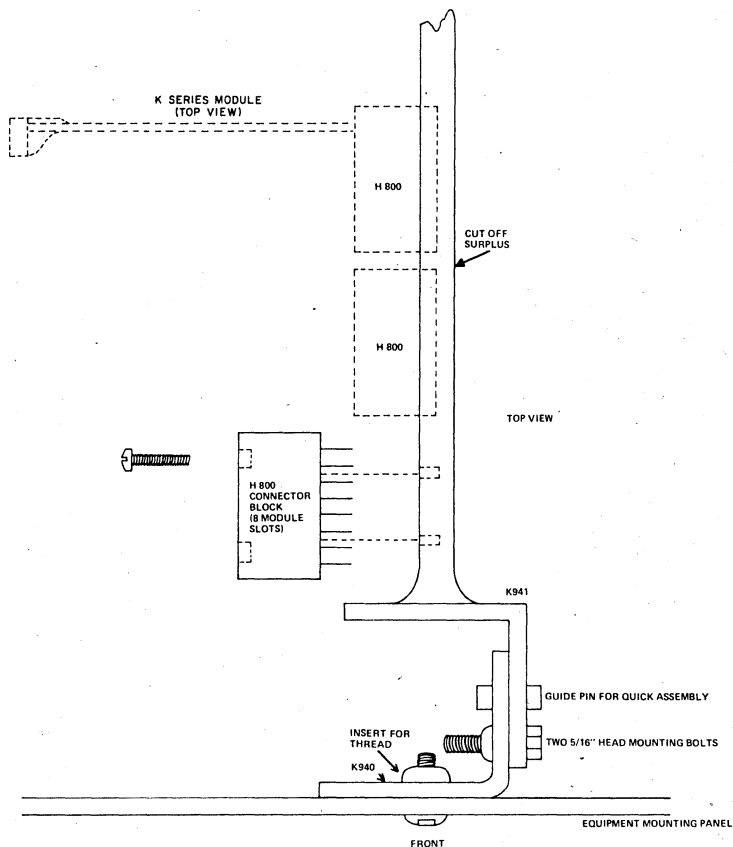
K771 — $26.00
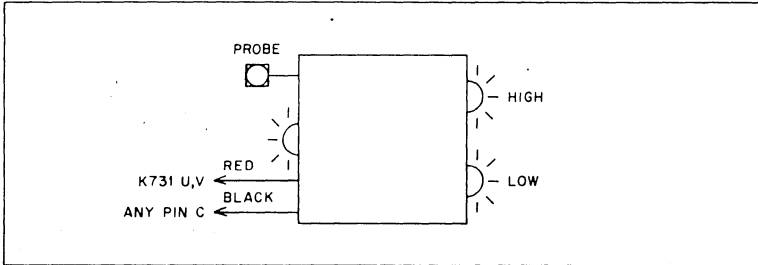
K791 TEST PROBE

This pocket test probe contains two pulse-stretching lamp drivers for visual indication of both transient and steady-state conditions. Neither indicator lights on an open circuit. A built-in test point illuminator adds convenience. The probe introduces negligible loading of the point under observation. The black wire connects to any pin C. The red wire gets ac power from the system supply transformer, pin U or V of K731. Probe is hollow and fits unwrapped end of H800W pins for hands-off use if desired.

K791 — $27.00

K SERIES MODULE
(TOP VIEW)

H 800

CUT OFF
SURPLUS

H 800

TOP VIEW

H 800
CONNECTOR
BLOCK
(8 MODULE
SLOTS)

K941

GUIDE PIN FOR QUICK ASSEMBLY

INSERT FOR
THREAD

K940

TWO 5/16" HEAD MOUNTING BOLTS

EQUIPMENT MOUNTING PANEL

FRONT

This convenient mounting hardware permits logic connector pin wiring to be done before logic is installed in the enclosure.

K940 is a mounting support that attaches to the enclosure. K941 is a removable bracket that mounts up to four H800 connector blocks. Any connections to external equipment are made through the ribbon connectors of interface signal modules (K508, K524, K604, K644) to the K716 Interface Block.

An installation of K-Series equipment in a NEMA-12 Enclosure is illustrated earlier in this section.

K940 — $3.00
K941 — $6.00

K-SERIES CONSTRUCTION RECOMMENDATIONS

A high percentage of all failures in electronic systems result directly from hasty planning of nonelectronic aspects. Much time and trouble can be saved by planning mechanical assembly before construction begins. Wiring methods and lead dress, heat distribution and temperature control, power supply reliability and line fault contingencies, and the attitudes and habits of people working near the system all merit forethought. Important opportunities for reliability, maintainability, and convenience will be lost if early and consistent attention is not given the topics below.

Environment

a. Temperature

Module temperature ratings are $-20°C$ to $65°C$ ($0°F$ to $150°F$) except K202, K210, K220, and K230 which are limited to $0°C$ ($32°F$) minimum. These ratings are for average air temperature at the printed board, and take local heating by high dissipation components into account. Free, unobstructed air convection is required for reliable operation; the plane of each module must be essentially vertical for this reason.

Convection is required not only to remove heat but also to distribute it, and movable louvres or baffles used to obtain self-heating under frigid conditions must not interfere with air movement within and around modules.

b. Motion

Transport or use in trucks or aboard ships can vibrate modules sufficiently to work them out of their sockets. K273, K604, K644, K731, K732, and K303 modules with K374 or similar controls attached are most subject to disturbance.

If modules are mounted in a 19-inch panel such as type 1943, use a 1945 hold-down bar. If modules are mounted on the hinged door of an enclosure, position the K941 so a support bolted to the side of the enclosure will contact the modules when the door is closed, taking care not to let the support interfere with ribbon cable on K508, K524, K604, and K644.

Mercury contact relays in K273 modules should be maintained within 30° of vertical while operating to insure correct logic output.

Controls such as K374, etc. will hold their setting in vibration, but are easily disturbed by repeated contact with loose wiring, etc.

c. Contaminants

Sulphurous fumes will attack exposed copper or silver; their presence demands the coating of ribbon connections and K731 heatsink cladding with suitable insulating varnish or plastic. A combination of high humidity and contaminated atmospheres requires such treatment on all printed wiring of K303 timers and controls, since at maximum settings even a few microamperes of leakage will affect their timing. Varnish or coatings are neither required nor recommended in less hostile conditions, and in any case it is desirable to exclude contaminants.

d. Convenience

Adjustments should be mounted so the least critical are easiest to reach. Calibrated controls such as K374, etc. should be positioned in a logical pattern before K303 sockets are wired. Ruggedness and feel should govern the selection of remote timer controls likely to be operated in moments of preoccupation or alarm.

During initial field wiring, the K716 interface blocks, K940 mounting feet, and the regulator supply transformers are easily interconnected by electricians. Pluggable connections have been provided to simplify later installation of the electronics package. K941 mounting bars are pin-indexed to K940 mounting feet, minimizing the chance of dropping the electronics package during assembly or disassembly.

Logic Wiring

a. General Information

Wire wrapping is the most suitable technique for the sockets used with K series modules. Some prefer AMP Termi-Point (trademark) but neither AMP nor DEC can guarantee full compatibility for this system. Solder fork connectors are optional; wrapped connections may also be soldered. For large volume repetitive systems using 1943 mounting panels, DEC offers a machine-wrapping service.

Never solder or wire wrap with any tool if there are modules installed, unless the tool is grounded to the frame to drain static charges, and unless AC operated devices work from isolation transformers. It is safest to avoid AC operated wire wrap tools together. Hand-operated pistol-grip wire wrapping tools are surprisingly efficient and easy to use. If automatic machine wrapping is contemplated, plan for only two wraps per pin.

b. Wire Types

Teflon (trademark) insulation over size 22 tinned solid copper wire is best for soldering. Size 24 tinned solid copper wire must be used for wrapping H801 and 1943 pins. Teflon (trademark) insulation may be used, but some prefer to sacrifice high temperature performance by using Kynar (trademark), to get greater resistance to cut-through where soldering is not involved.

Type 932 bussing strip allows module power and ground pins A and C to be connected conveniently, and is also helpful if several modules have common pin connections.

c. Procedures

First solder in all bussing strips. Next tie all grounds and grounded pins together. Finally point-to-point wire all other connections.

Run all wires diagonally or vertically. Do not run wires horizontally except to adjacent pins or along mounting bar between modules. Horizontal zig-zag wiring interferes with checking and is prone to insulation cut-through. Leave wires a bit slack so they can be pushed aside for probing. Cabling is definitely not recommended. Wires should be more or less evenly distributed over the wiring area.

When wrapping, avoid chains of top-wrap-to-bottom-wrap sequences which entail numerous unwrappings if changes must be made. Properly sequenced wraps require no more than three wires to be replaced for any one change in two-wraps-per-pin systems. Never re-wrap any wire. For best reliability, do not bend or stress wrapped pins, for this may break some of the cold welds. Follow tool supplier's recommendations on tool gauging and maintenance etc. As a convenience, DEC stocks three Gardener-Denver tools under numbers H810, H811, and H812. See specifications pages.

Field Wiring

a. AC Pilot Circuits

K716 terminals accept one or two wires up to size 14. Connections have been arranged so AC inputs all go to one end of the interface block, and AC outputs all go to the other end. The eight terminals nearest the center are typically connected only to each other and to a few return and AC supply wires.

Input and output leads should be segregated so they do not block entry to the ribbon connector sockets. If sockets face to the left, AC inputs will be above and all other connections below. Wires should be routed down the connector side of K716 blocks to cable clamps or wiring ducts placed parallel with K716s. (See diagrams on K716 data page.)

Plan the logical arrangement of field wiring terminals and indicators before module locations are selected to avoid excessive folding or twisting of ribbon cables. (See recommendations on module locations below.)

b. DC and Transducer circuits

All signals except line voltage AC inputs use the straight-through connections of K716 terminals 15 through 24. Within the K716, leads are shortest to terminals 15, 17, 18, 19, and 20; use these terminals for minimum noise on K524 low level signals.

DC outputs from K644 and AC outputs from K604 are high level; wiring is noncritical. Low level inputs to K524, however, may require special treatment to avoid false indications. Low level signals should at least be isolated from AC line and DC output signals throughout the field wiring system, and, as a minimum, individual twisted pairs should be used for signals and return connections.

For lower signal levels or longer wiring runs, shielded pairs may be required, with the shield grounded only at one point, preferably at the logic system end unless one side of the transducer is unavoidably grounded. Conduit which may be grounded indiscriminately is not an effective substitute for shielded, insulated wiring.

Module Locations

a. End Sockets

The first sockets to assign are those for K731 and K732 regulators, and for K303 timers. If possible, mount regulators nearest the foot of a K941 mounting bar, so their extra bulk projects into the space between the mounting surface and the first H800 block on the bar. Controls mounted on the same mounting surface opposite K731 source modules may be as much as ⅝" deep without touching modules.

Sockets at the outer end of K941 mounting bars are the only locations where K303 timers can have integral controls mounted. Even where the use of K370-group controls is not initially planned, assignment of K303 modules to these outer locations is recommended. Also, these sockets should be the first reserved as spares if any unused locations are available. This way maximum flexibility will be preserved for possible design changes or additions.

b. Interface Modules

AC and DC interface modules such as K508, K524, K604, and K644 should be assigned locations that simplify cabling. Ribbon cables can be twisted by a succession of 45° folds, but a neat installation should be planned. Assign the location and position of K716 interface blocks first. Consider such features as logical arrangement of indicator lights for trouble shooting, ease of routing and tracing field wiring, and directness and length of ribbon cable runs back to the logic modules.

After K716 locations and assignments have been selected, assign socket positions for interface modules (K508, etc.). The order should be coordinated so the combined ribbon cables will lie flat together. Excess ribbon cable can be easily and neatly folded away. Lengths other than 30" are not available since these modules cannot be tested and stocked until cables are cut and soldered. This should cause no difficulty if module locations are assigned thoughtfully.

c. Display Modules

If K671 decade displays are required, select their locations after regulator and interface modules have been assigned sockets. The 12" cables on these modules are oriented for convenient assembly of displays above logic modules, to be viewed from outside the door or enclosure in which K940 and K941 hardware is mounted. Used this way, the digits of lower significance have cables below those of more significant digits.

For neatest cabling and quickest module wiring, counter and display modules should be arranged so the counter input will be nearest the K940 mounting surface. Notice that pin connections on K671, K210, and K220, and K230 modules are coordinated, so that a side-by-side pairing of flip-flop and associated K671 modules will result in short, neat, easy wiring. Ribbon cable passes easily between modules, so it is not necessary to restrict K671 modules to the topmost row. However, the limited cable length will usually restrict them to the top mounting bar in systems using more than one K941.

Do not fold or arrange ribbon cables so that they lie flat on the upper edges of modules, as this will restrict the flow of cooling air.

System Power

a. Supply Transformer

Any filament or "control" transformer rated at 12 v or 12.6 v RMS on nominal 120 v line voltage may be used to supply power to K series logic

Transformer current rating should be for capacitor-input filter, about 50% higher than the rating required for resistive loads. Thus a single K731 1 amp regulator requires a center-tapped transformer with $3/4$ ampere rating on resistive loads at 12 v, or with two 6 v windings rated $3/4$ ampere each.

b. Noise Filtering

Hash filter capacitors cf 0.1 mf each are recommended from each side of the power transformer secondary to chassis ground. In environments where the AC line may carry unusually large amounts of noise, line filters such as Sprague Filterols (trademark) are advisable. K series systems must not share 12 volt power with any electromechanical device, since the transformer itself is the primary filter for medium-frequency line noise rejection.

c. Power Wiring

In systems not requiring full use of the quick-change features of the K716 and K940, transformer secondaries can be wired directly to pins U and V of regulator modules. If power connections are to be removed with maximum speed, a W021 connector board may be used to bring 12 VAC power into the system. It is best to limit current through any pin to about 2 amperes, so in large systems several W021 pins are needed for each side of the secondary.

Outputs of K731 modules may not be parallel, so +5 v bussing must be broken into two sections where two K731 Source Modules are required. This is not advisable when using one K731 and one or more K732 slave regulators.

d. Alternate Power Supplies

Any source of 5 VDC ± 10% may be used for K series systems at ordinary room temperatures, provided noise, hash, spikes, turnon-overshoot, etc. are reasonably well controlled. K series modules are far less sensitive to noise on power lines than computer-speed circuits, but it is still possible to cause malfunction or damage if extreme noise is present.

Temperature coefficient of the K731 regulator is selected to compensate for that of timers and other circuits, so operation over temperature extremes with constant-voltage supplies involves a sacrifice in timing consistency. Output fanouts are also degraded if constant voltage supplies are used at extreme low temperatures. Derate linearly from 15 ma at room temperature to 12 ma at −20°C (0°F) for constant-voltage power supplies.

e. Line Failure

When unscheduled shutdown of a K-series system cannot be tolerated in spite of AC power failure, some form of local energy storage is required. To withstand short-term failures it is possible to add extra capacitance from pin A to pin C. However, manual grounding of pin D (turnon level) may be required to start the system, since the external capacitance will appear to the regulator as a short and output current will be limited to a low value. For each ampere millisecond of dc power storage beyond the rise of K731 OK level, 10,000 mfd is required. The supply itself provides one half ampere-millisecond internally. K732 slave regulators each provide one ampere-millisecond internally

A 5 volt battery, or a 6 volt battery with series diode(s) to drop the voltage to 5 volts, may be used as an alternate source of power in case of line voltage failure. In very small systems (with some types of batteries) it may be practical to use the battery itself as a shunt regulator, charging it through a simple full-wave rectifier and dropping resistor circuit from the same kind of transformer used with K-series regulators. Unless the current is very low with respect to battery size, however, some means of switching the battery connection will be required. Below is shown a circuit which can be used for

129

current requirements to 1 ampere. The same principle can be extended to larger systems with slightly more complex circuitry.

6 VOLT BATTERY
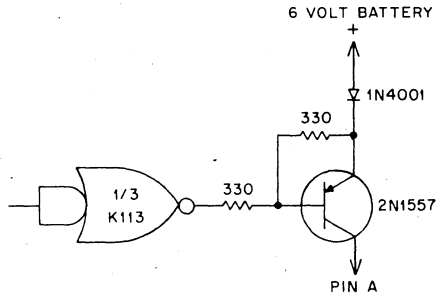
POWER FAILURE SWITCH FOR EMERGENCY BATTERY

R
SERIES

R SERIES MODULE FEATURES

COMPLETENESS OF LINE
A full selection of high-volume standard modules with sufficient types and accessory hardware for building complete systems.

SIGNAL LEVELS
0 volts and —3 volts.

FAN-OUT
70 ma from pulse amplifiers
18 ma from diode gates
15 ma from typical flip-flops

CLAMPED LOGIC
Signal voltages are independent of loading. All signals clamped to —3 volts.

WIDE TEMPERATURE RANGE
FLIP CHIP silicon modules operate over a temperature range of —20°C to +65°C.

GOOD NOISE IMMUNITY
All R Series modules have diode isolated inputs. Typical noise rejection for diode gates:
at 0v — 1.0v
at —3v — 1.5v

LOW POWER DISSIPATION
Typically: 150 mw per flip-flop
40 mw per diode gate

SIMPLE POWER REQUIREMENTS
Two supply voltages required: +10v and —15v. All modules have standard power connections. Complete line of power supplies available as standard items.

ULTIMATE IN LOGICAL FLEXIBILITY
Extremely flexible flip-flop configuration permits JK, RS, RST, or T memory elements to be constructed without modifying modules.
Gates and power amplifiers may be paralleled for performing positive OR functions.
A wide range of interfacing modules are available for converting standard DEC levels to external equipment reuirements.

FREQUENCY RANGES
Dc to 2 MHz

LOGIC LEVELS
0v to —0.3 upper level
3.2 v to —3.9v lower level

HIGH FAN-IN
Low input current requirements. Typically 1 ma to 3 ma. Diode gate inputs may. be
expanded as high as 25 inputs with gate expander modules.

ALL LOGIC LEVELS DIODE CLAMPED
Signal voltages are diode clamped at —3v independent of fan-out and independent of
other input conditions at the load.

CONSERVATIVE DESIGN
All circuits can tolerate at least ±20% variations in power supply voltage.

NOISE IMMUNITY

NOISE IMMUNITY	At 0 volts	At —3 volts
Diode Gates	1.0v	1.5v
DCD Gates	0.7v	Totally insensitive

TEMPERATURE RANGE
—20°C to +65°C on all silicon R and W FLIP CHIP modules. A few W-Series power
driving accessory modules include germanium semiconductors as indicated on their
data sheets, reducing their upper limit to +55°C.

POWER REQUIREMENTS
+10v nominal, module pin A
—15v nominal, module pin B
ground, module pin C

BOARD SPECIFICATIONS
Material — G10 FR4 Glass Epoxy
Copper Coating — 2 oz. (0.0028 inches)
Thickness — 0.055 ±.003 inches overall
Gold Plated Contacts — 0.00015 inch gold on copper

STANDARD R SERIES FLIP CHIP WAVEFORM

STANDARD PULSE

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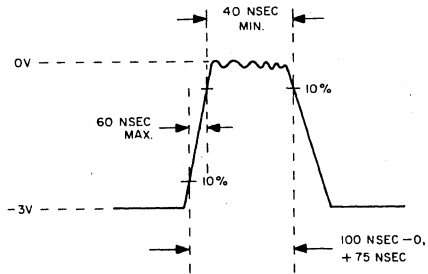
R-SERIES
BASIC CIRCUITS

DIODE GATE

The basic element of digital logic described in this chapter is the diode gate. The diode gate is used in the R (2-megahertz) series to combine, amplify, invert, and standardize the signals which represent various logic functions. Figure 1 is a schematic of a simple diode gate with one input.
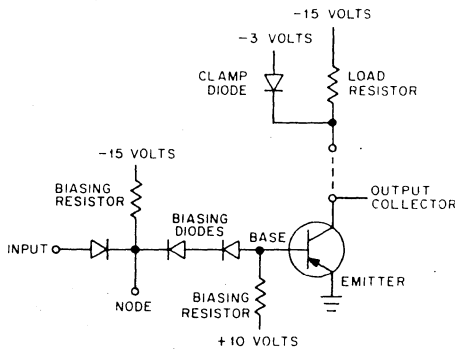

Figure 1   Single Input Diode Gate

When the input is negative, the node point is also negative and current flows from the transistor emitter through the biasing diodes and the biasing resistor to minus 15 volts (−15v). As a result, the PNP transistor is turned on, forming a short circuit between the collector and the emitter. Thus, when the input voltage is negative, the output voltage is ground. Since the output is from a saturated transistor, it has a low output impedance and good driving power.

When the diode gate input voltage is ground, the biasing diodes and the resistor, which is connected to the 10v supply, hold the transistor base more positive than the emitter, and the transistor is turned off. The output is then an open circuit, and it will follow the voltage of any other circuit connected to it.

If the load resistor and clamp diode are attached to the transistor collector, they serve as a voltage source and hold the output at   3v while the transistor is off. When the transistor is on, the diode is cut off and the load resistor follows the output to ground.

The single-input diode gate therefore has three functions. First, it inverts the input signal. Second, it standardizes the output voltage to   3v or ground (if the clamped load diode and resistor are connected). Third, since the output current available from the transistor is much greater than the required input current, the diode gate amplifies.

A fourth function, gating, is obtained by adding more diode inputs to the node point, as shown in Figure 2.
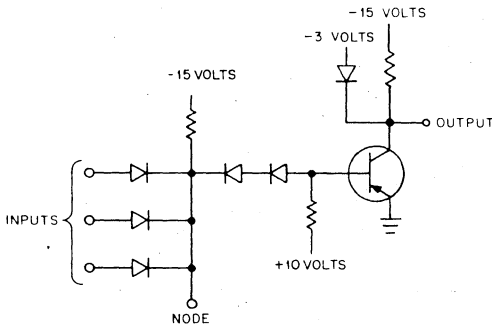
Figure 2   Multiple Input Diode Gate

The node terminal in this diagram will be at approximately the same voltage as the most positive input. Thus, when any input terminal is grounded, the node terminal is also at ground and the circuit output is at − 3v. If all of the inputs are negative, the node terminal will be negative and the circuit output will be at ground.

Gating functions may also be performed by wiring together two or more diode gate outputs and one load resistor, as shown in Figure 3. When any input is negative, it saturates the corresponding transistor and forces the output line to ground. If all inputs are at ground, all of the transistors are open circuits and the output voltage, determined by the clamped load resistor, is   3v.
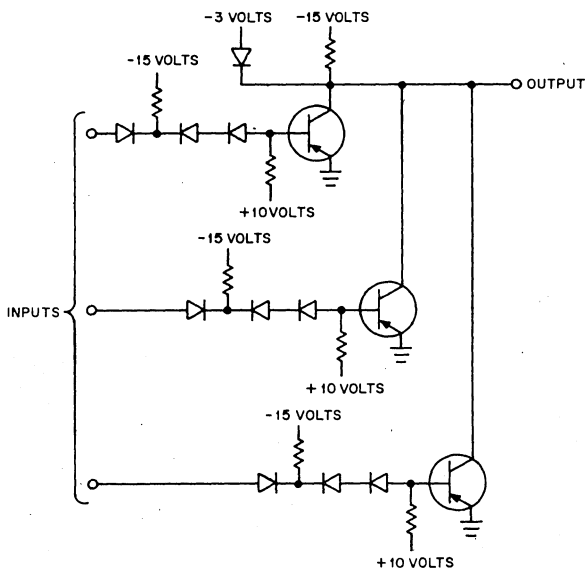
Figure 3   Diode Gates in Parallel

The basic diode gate can be used to construct very complex logical functions. A drawing that showed all of the circuit components, however, would be tedious to draw and difficult to read. For this reason, the diagrams that follow use a shorthand notation which represents one or more components as a single functional unit. Referring to Figure 4, diodes are shown in the conventional way. The transistor circuit, including the biasing resistors and diodes, is shown as a simple rectangle with an arrowhead indicating the direction of the transistor emitter. This part of the circuit is called an inverter because of the function it performs. The load resistor is shown as a resistor with a large dot at the top indicating that it is diode clamped to −3v. With these symbols, one can easily and quickly draw complex logical functions.
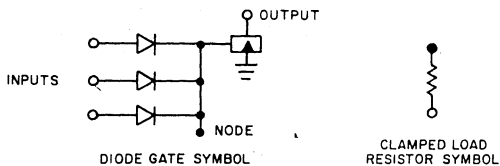

Figure 4   Diode Gate and Clamped Load Resistor Symbols

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Assertion input and output voltage levels are shown by diamonds. A solid diamond indicates a --3v level, and an open diamond indicates a ground level. In the 2-input diode gate of Figure 5, for example, if input A and input B are both negative, the output will be at ground. If either A or B is at ground, the output will be negative.
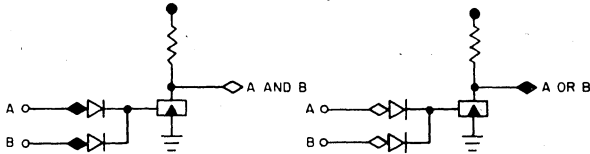

Figure 5   Diamonds Indicating the Voltage Levels

DIODE-CAPACITOR-DIODE GATES

The diode-capacitor-diode (DCD) gate is used to standardize the input to various units such as flip-flops, delays, and pulse amplifiers. It provides logical isolation between pulse and level inputs and produces a logical delay which is essential for sampling flip-flops at the same time they are being changed. It also acts as a logical AND gate since both pulse and level inputs must meet certain requirements for a signal to appear at the output. Either positive pulses or positive-going level changes (both —3v to ground) may be used as the pulse input.
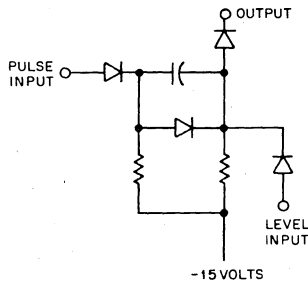

Figure 6   Diode-Capacitor-Diode Gate Circuit

A schematic drawing of a DCD gate is shown in Figure 6. If the level input is held at ground and the pulse input is held at —3v, the capacitor will become charged after the setup time has passed. If the pulse input then suddenly goes to ground, a positive-going pulse will appear at the output. There is delay at the level input, but the pulse input goes to the output without delay. Even if the level input changes simultaneously with a positive transition at the pulse input, the delay acts as a temporary memory: the pulse input is gated according to the level input that existed during the interval before the pulse.
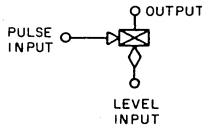
Figure 7   Diode-Capacitor-Diode Gate Symbol

The symbol for the DCD gate (Figure 7) is distinguished from the diode gate by an X in the rectangle. The output is at the top, the delayed (level) input is at the bottom, and the differentiating (level change or pulse) input is on the side. The input signal to be differentiated, whether a level change or a pulse, is indicated by an arrowhead, rather than a diamond. The pulse symbols are hollow when positive-going and solid when negative-going. In the DCD gate, the pulse input must be positive-going.

Since many DCD gates may be driven by the same pulse, the side of the rectangle opposite the pulse may be used to show a continuation of the same line, as in Figure 8. The illustration on the left below is a simplified version of the identical logical configuration on the right.
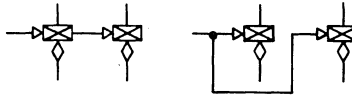

Figure 8   Pulse Lines to Multiple Gates

FLIP-FLOPS

The flip-flop provides a convenient means of storing logical conditions within a digital system. It has two stable states representing 0 and 1, and remains in one of these states until an appropriate command to change state is received. Three commands may be given: set, which puts the flip-flop in the 1 state; clear, which puts the flip-flop in the 0 state; and complement, which changes the state of the flip-flop regardless of its previous state.

TABLE 1   FLIP-FLOP COMMANDS

Command	State Before Command	State After Command
Set	1 0	1 1
Clear	1 0	0 0
Complement	1 0	0 1

Figure 9 shows a schematic diagram and the symbolic equivalent of an R series flip-flop. The flip-flop consists of two diode gates, connected "back-to-back." When transistor Q1 is off, its output is negative. This holds transistor Q2 on, which in turn maintains the off condition of transistor Q1. Direct set and direct clear inputs are provided for operation of the flip-flops directly from external logical elements. When the flip-flop is set to the 1 state, the 1 output is at —3v.
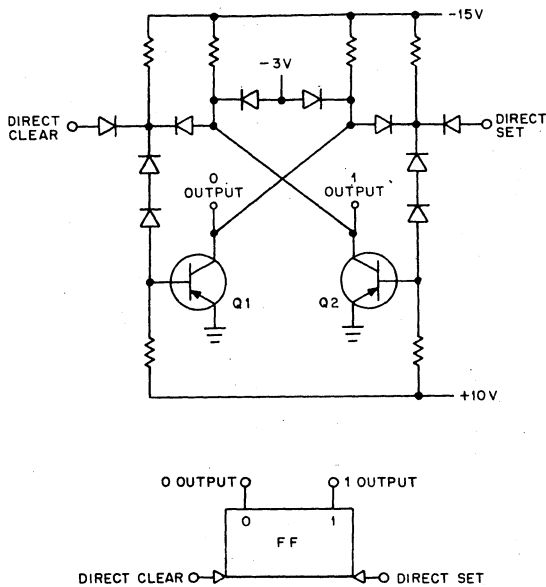

Figure 9   Flip-Flop Schematic and Symbol

Inputs to this flip-flop are often made through DCD gates as shown in Figure 10. The gates provide sufficient delay so that information may be read out of one flip-flop and into another at the same time that the first flip-flop receives a command to change state. The DCD gate can also be used to perform additional logical operations, since it is basically an AND gate. That is, both the pulse and level inputs of the DCD gate must meet the proper input requirements for an output signal to occur.
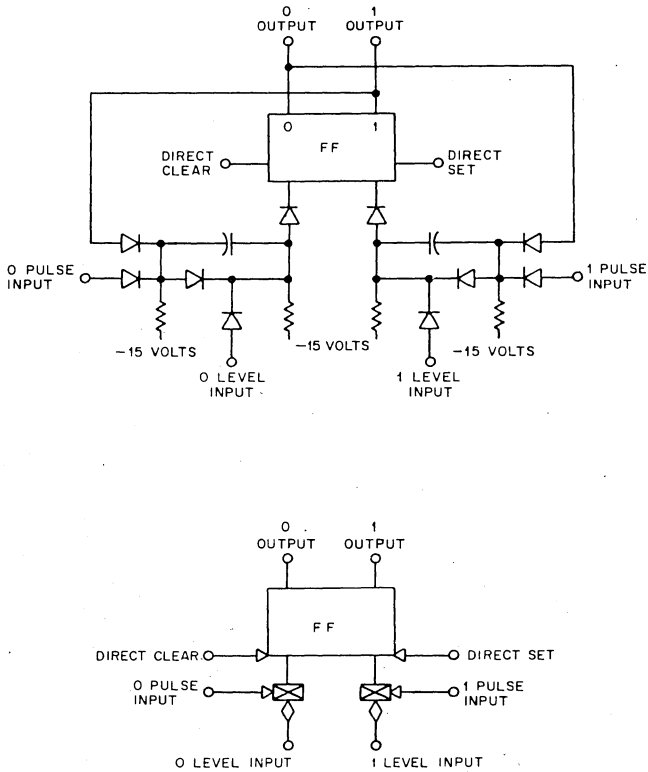
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Figure 10 Flip-Flop with DCD Gates, Schematic and Symbol

As can be seen from the schematic in Figure 10, the DCD gate level inputs are conditioned by the flip-flop outputs. Thus, a set signal will reach the flip-flop only if the flip-flop was previously in the 0 state. Similarly, a clear command reaches a flip-flop only if it was previously in the 1 state. For simplicity, this conditioning is not shown on the symbol but should be remembered because it is a very powerful element of the flip-flop.

A complement terminal can be made simply by tying the set and clear pulse inputs together as shown in Figure 11. The gate inputs are still available for external enables. This technique allows a flip-flop with its DCD gates to be used in such varied applications as up counter, down counter, up-down counter, shifting, multiple source buffering, jam transfer register, ring counter, BCD counting, and special counts of 2^n ($2^n + 1$) all without need for additional gate modules.
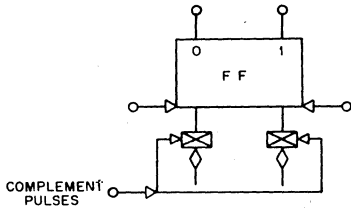

Figure 11   Complementing

Flip-flops may be collector-triggered by tying a flip-flop output to the output of one or more diode gates. As illustrated in Figure 12, when the output of either diode gate D_1 or D_2 is asserted (at ground), the corresponding flip-flop is cleared (put to 0). If the gates are attached to the flip-flop through diode networks (Figure 12a), the diode gate outputs (D_1 and D_2) can be logically independent. If they are attached in parallel without diode networks (Figure 12b), the ouputs will be dependent. That is, if any output is at ground, the output of all gates connected in parallel with it will be at ground.
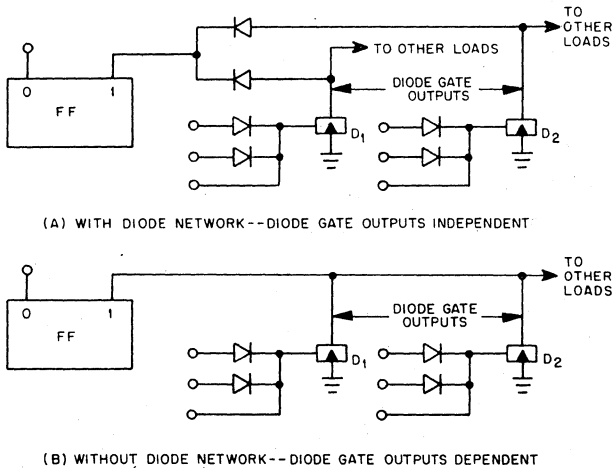

(A) WITH DIODE NETWORK--DIODE GATE OUTPUTS INDEPENDENT

(B) WITHOUT DIODE NETWORK--DIODE GATE OUTPUTS DEPENDENT

Figure 12   Collector Triggering of a Flip-Flop

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DELAYS

The delay one-shot, or monostable multivibrator, is a basic timing element. The input to the delay, like that of the flip-flop, is through a DCD gate (see Figure 13). When the gate is properly enabled, and when its pulse input terminal is brought to ground by a positive pulse or a positive-going level change, the output of the delay changes from its normal ground level to a −3v level for a fixed, but adjustable, period of time. After the fixed time has elapsed, the output returns to ground. This delayed output is suitable for driving many R series modules. A pulse output can be obtained with the addition of a pulse amplifier to the delay output.
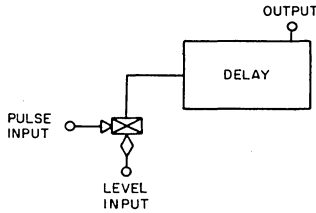

Figure 13   Delay One-Shot

Delay units are particularly useful in generating delayed pulses or signals of arbitrary width. The network of delays in Figure 14a will produce the waveform shown in Figure 14b.
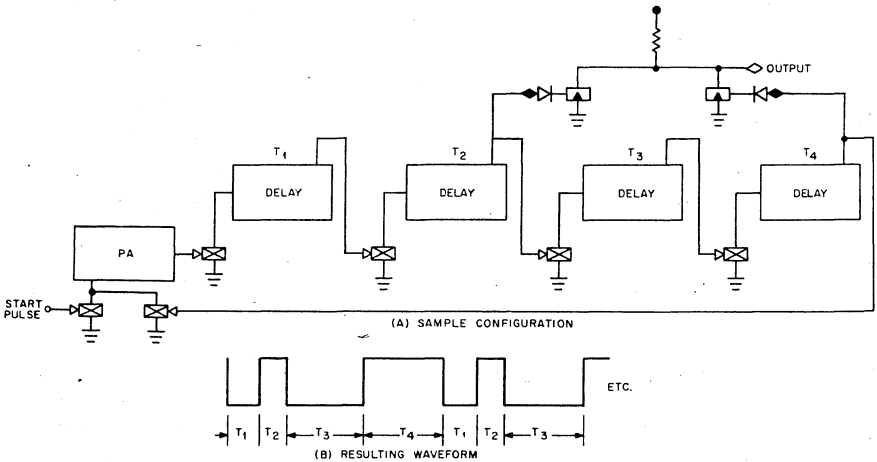

Figure 14   Typical Application of Delay Units

PULSE AMPLIFIERS

Pulse amplifiers are extremely versatile elements since they not only amplify and standardize various signals into standard 100-nanosecond pulses ($-3v$ to ground), but they may also be used to carry the results of gating to many units. For example, when the same gating is to be done on an entire register of flip-flops, it is most economically performed at the input to the pulse amplifier which drives the register.
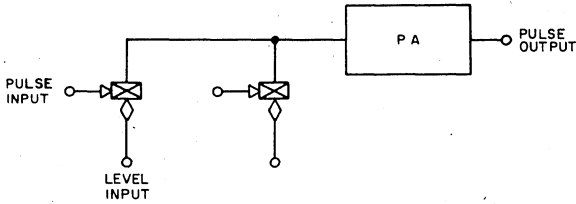

Figure 15   Pulse Amplifier with Gates

Several pulse amplifier outputs may be ORed together by simply connecting their outputs in parallel (Figure 16). Thus two levels of logic can be performed by pulse amplifiers.
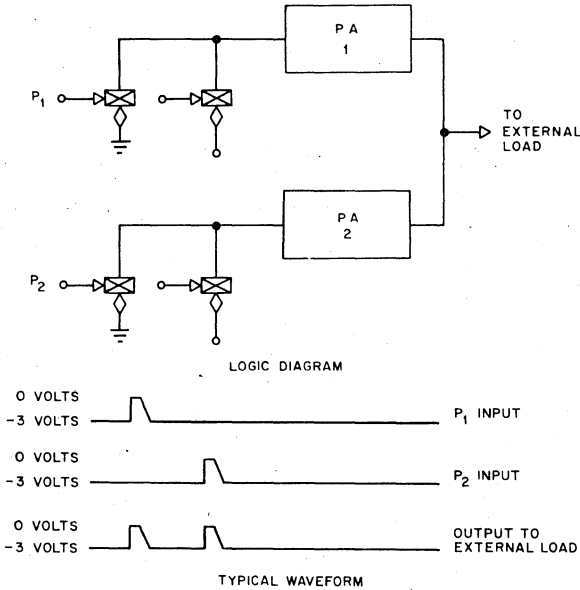

Figure 16   ORed Pulse Amplifiers

Flip-flops may be collector-triggered by connecting the output of one or more pulse amplifiers to the output terminals of the flip-flop (Figure 17). This connection may be made directly or through the diode networks, as with the diode gates shown in Figure 12.
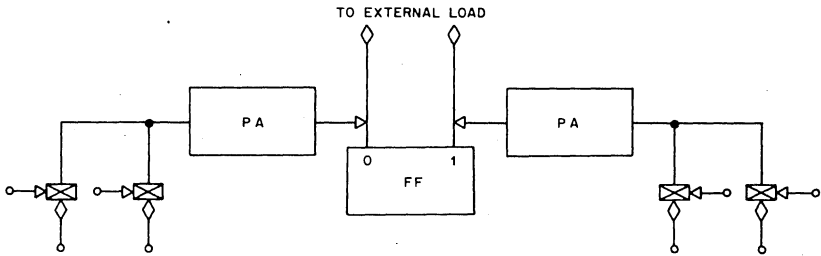

Figure 17   Collector Triggering of Flip-Flops

CLOCKS

Variable R series clocks produce standard, 100-nsec pulses (—3v to ground) from stable RC-coupled oscillators. These clocks are often used as a primary source of timing for large systems (Figure 18).
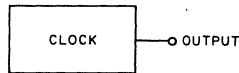

Figure 18   Clock

Where precise timing is required, a clock with a single frequency crystal oscillator may be used.

LOADING RULES

When interconnecting basic circuits to perform logical operations, it is important to keep the load on each circuit within its driving ability. The R series loading rules are simple because all inputs draw current from the same direction and because all inputs are either diode gate circuits or DCD circuits.

Each diode gate input draws 1 ma (milliampere) and the output drives 20 ma. The load resistor draws 2 ma; so a diode gate with a clamped load resistor tied to it can drive 18 ma.

A flip-flop is two slightly modified diode gates cross-connected. The direct set and clear terminals draw 1 ma. The output will drive 21 ma less 3 ma for the load resistor permanently connected in the flip-flop and less 1 ma for conditioning the opposite side of the flip-flop for a remainder of 17 ma.

The single shot delay has a similar output circuit with a built-in load resistor. It will drive 20 −2 or 18 ma.

The pulse amplifiers will drive loads of up to 70 ma.

The DCD gates on flip-flops, delays, and pulse amplifiers draw 2 ma at the level inputs and 3 ma at the pulse inputs. When two DCD gates are driving both sides of the same flip-flop, the load on both pulse inputs totals only 4 ma. When the level inputs are tied together as in a complement configuration, the total input load is only 3 ma, as shown in Figure 19.
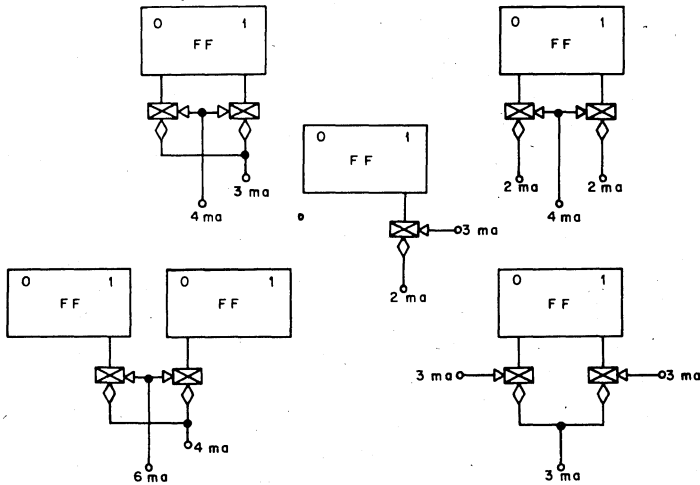
Figure 19   Flip-Flop Input Loads

On flip-flops which have built-in DCD gates, the output driving ability is less because the internal diode capacitor gate draws current from the flip-flop. Table 2 lists the output driving capability for each of the six types of flip-flops.

Table 2 Flip-Flop Output Driving Capability

Flip-Flop	0 Output	1 Output
R200	17	17
R201	11	13
R202	15	15
R203	15	17
R204	17	17
R205	13	15

R001 DIODE NETWORK
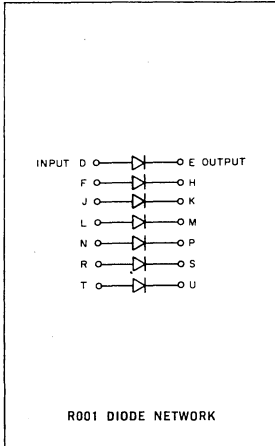
R002 DIODE NETWORK

Diode networks can expand the logic capability of any R-Series, W-Series, or A-Series module which has one or more node inputs, such as the R111 diode g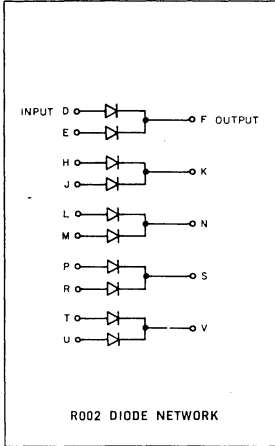ate. They can also make it possible to OR into an R-Series flip-flop output terminal for setting or clearing from several sources.

Diode networks cannot be cascaded to perform other logic operations.

Propagation delay of R-Series gates expanded by R001 or R002 diodes will increase typically 15-30 nsec when gate output rises from —3v to 0v, but will not change noticeably when gate output falls from 0v to —3v. Diodes used are similar to type IN3606.

R001 — $4.00
R002 — $5.00

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R107 INVERTER

The R107 Inverter contains seven inverter circuits with single-input diode gates. Six of the circuits are used for single-in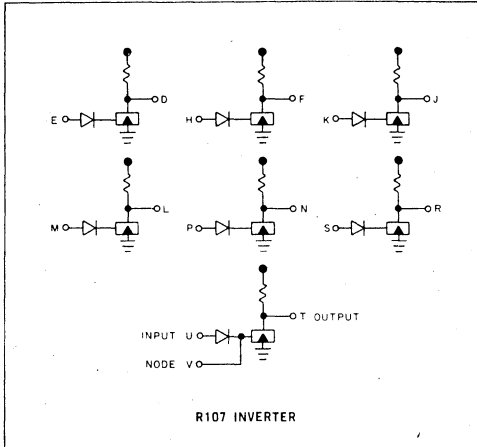put inversion; the seventh circuit can be used for gating by tying additional diode input networks to its node terminal. Clamped load resistors of 2 ma are a permanent part of each inverter.

INPUT: Diode — Standard levels of —3v and ground, 100-nsec minimum duration. Input load is 1 ma, shared among the inputs that are at ground. **Node Terminal** — Accepts only R001 or R002 Diode Networks or their equivalent. The combined length of all leads attached to the node terminal must not exceed 6 in. Input signal and load characteristics for diode networks are the same as those given for the diode input above.

OUTPUT: Standard levels of —3v and ground. Each inverter can drive 18 ma of load at ground. Output terminals of inverters may be connected in parallel.

Some typical propagation delays are shown below. High frequency logic designs may benefit from the application note "Estimating Propagation Delays."

Fan-out	4	10	16
Output Rise	30 nsec	35 nsec	40 nsec
Output Fall	60 nsec	100 nsec	140 nsec

POWER: + 10 v(A)/0.7 ma, —15 v(B)/30 ma.

R107 — $24.00

EXPANDABLE NAND/NOR GATE
TYPE R111

R
SERIES

CLAMPED LOAD RESISTORS

OUTPUT

DIODE INPUTS

NODE TERMINAL F

R111
EXPANDABLE NAND/NOR GATE

The R111 contains three diode gates, each connected to a transistor inverter. The gate operates as a NAND for negative inputs, and as a NOR for ground inputs. Each gate has three input terminals: two are connected to diodes, a third is connected directly to the node point of the diode gate. The third terminal allows the number of input diodes to be increased by adding external diode networks such as the R001 or R002. External diodes must be connected in the same direction as the diodes in the R111. Unused inputs may be left open.

INPUT: Diodes — Standard levels of —3v and ground, 100·nsec minimum duration. Input load is 1 ma, shared among the inputs that are at ground. **Node Terminal** — Accepts only R001 or R002 networks or their equivalent. The combined length of all leads attached to the node terminal must not be greater than 6 in. Input signal and load characteristics for the diode networks are the same as those given for the diode above.

OUTPUT: Standard levels of —3v and ground. Each output can drive 20 ma of load at ground. Clamped load resistors are included in the module. Each clamped load resistor represents 2 ma of load. The output terminals of diode gates may be connected in parallel. Two gates in parallel (driven by the same signal) can drive 38 ma at ground (20 ma each, less the 2-ma clamped load). If they are not driven by the same signal, gates in parallel drive 20 ma at ground minus 2 ma for each clamped load used. Some typical propagation delays are shown below. High frequency logic designs may benefit from the application note "Estimating Propagation Delays."
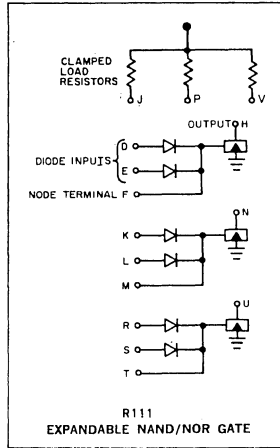
Fan-out	4	10	16
Output Rise	30 nsec	35 nsec	40 nsec
Output Fall	60 nsec	100 nsec	140 nsec

POWER: +10 v(A)/0.3 ma, —15 v(B)/18 ma.

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R113 NAND/NOR GATE
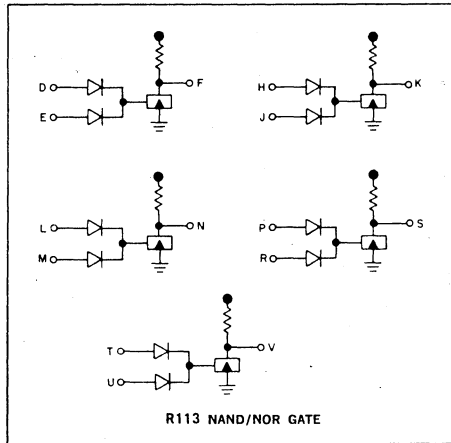
The R113 contains five diode gates, each connected to a transistor inverter. The gate operates as a NAND for negative inputs, and as a NOR for ground levels.

INPUTS: Standard levels of - 3v and ground. 100-nsec minimum duration. Input load is 1 ma, shared among the inputs at ground. Unused inputs may be left open.

OUTPUT: Standard levels of 3v and ground. Each output can drive 18 ma of load at ground. Output terminals may be connected in parallel. Clamped loads includ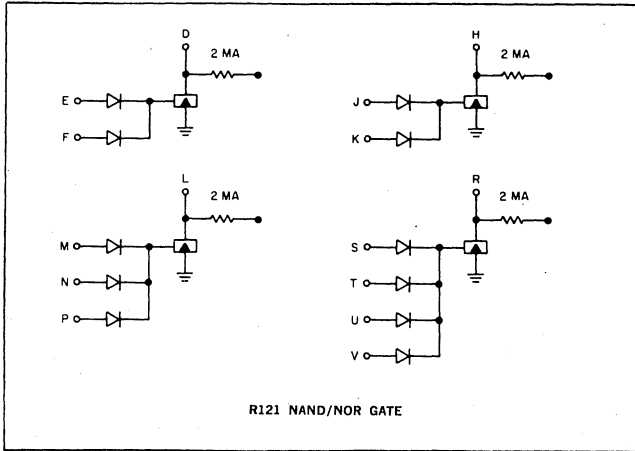ed in the module are 2 ma each. Some typical propagation delays are shown below. High frequency logic designs may benefit from the application note "Estimating Propagation Delays."

Fan-out	4	10	16
Output Rise	30 nsec	35 nsec	40 nsec
Output Fall	60 nsec	100 nsec	140 nsec

POWER REQUIREMENTS: : 10V (A) 0.5 ma. —15V (B) 23 ma.

R113 — $20.00

150

R121 NAND/NOR GATE

The R121 contains four R111-type circuits with 2-ma loads internally connected to each output. This module increases density at the expense of flexibility, since gate expanders R001 and R002 cannot be used.

INPUT: Standard levels of —3v and ground, 100 nsec, minimum duration. Input load is 1 ma, shared among the inputs that are at ground.

OUTPUT: Standard levels of —3v and ground. Each output has a permanently attached 2 ma clamped load resistor. Each output can drive 18 ma of load at ground. Delays are similar to R111 delays. See application note "Estimating Propagation Delay" for more information.

POWER: +10v(A)/0.4 ma, —15v/20 ma.

R121 — $17.00

NOR / NAND GATE
TYPE R122

R122 NOR/NAND GATE
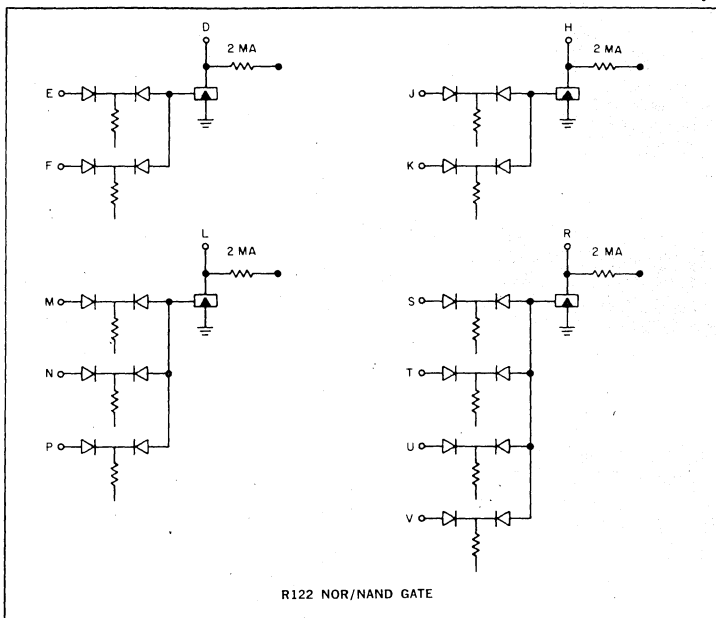
Provides the logical complement to the R121 NAND Gate at some sacrifice of speed and economy.

INPUT: Standard levels of —3v and ground. Minimum duration: 400 nsec at ground, 100 nsec at —3v. Input load is 1 ma at each input.

OUTPUT: Standard levels of —3v and ground. Each output has a permanently attached 2 ma clamped load resistor. Each output can drive 18 ma of load at ground. Propagation delays for output rise are similar to R111 delays. Propagation delays for output fall are typically 75 nsec longer than R111 delays.

POWER: + 10v(A)/3 ma, —15v/31 ma.

R122 — $26.00
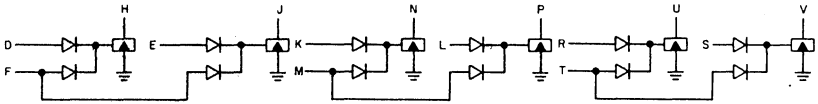
R123 INPUT BUS GATE

This module contains six R111-type diode gates arrayed for convenient driving of the PDP-8 computer input bus, and for other matrix-like applications. Clamped loads are not provided on this module, and must be obtained from some module in the associated logic.

INPUT: Standard levels of −3v and ground, 100-nsec, minimum duration. Each of the six gates is a 1 ma load shared among its grounded inputs; thus inputs F, M, and T may be loaded with up to 2 ma at ground.

OUTPUT: Standard levels of −3v and ground. Each output can drive up to 20 ma at ground. A 2 ma or heavier clamped load must be used at each group of paralleled collector outputs, chosen to provide fall times fast enough for the use intended. Delays are similar to R111 delays. See application note "Estimating Propagation Delay" for more information.

POWER: +10v(A)/.6 ma, −15v/15 ma.

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R131 EXCLUSIVE OR
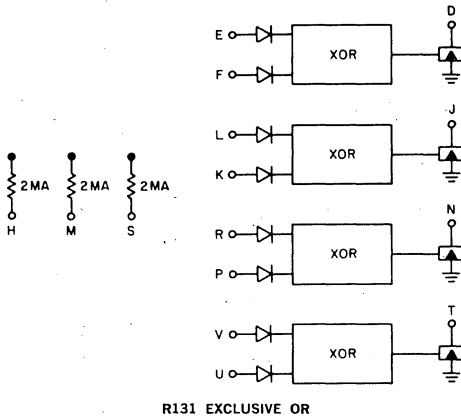
This module provides a convenient way to compare two binary numbers or patterns. The output of each circuit is negative if its inputs are the same, and ground if they are different. If the outputs of several circuits are tied together, the common output line will be negative if every input pair matches, ground if any pair doesn't match.

During the transition from one input pattern to another with the same output, there is an interval during which the R131 output may be wrong for both patterns. Transitions between unequal inputs have a relatively short settling time, but transitions between equal inputs may produce transients to ground lasting 250 nsec or more.

INPUTS: Standard levels of —3v and ground. Each input is a 2 ma load at ground.

OUTPUTS: Standard levels of —3v and ground. Each output can drive 18 ma at ground. Propagation delay for output rise is similar to R111 delay. Propagation delay for output fall is typically 300 nsec longer than R111 delay.

POWER: +10v(A)/0.8 ma; —15v(B)/36 ma.

TRUTH TABLE

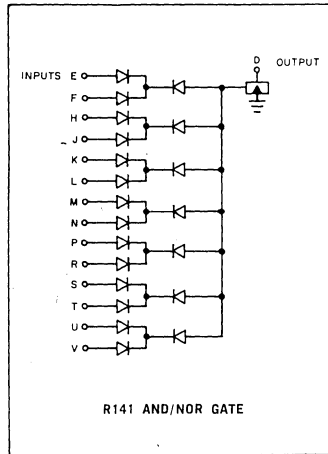| Input E(K, P, U)	Output D(J, N, T)	Input F(L, R, V)
0v	0v	—3v
—3v	0v	0v
0v	—3v	0v
—3v	—3v	—3v

R131 — $35.00

R141 AND/NOR GATE

The R141 AND/NOR Gate performs two levels of gating. The module contains a multiple-input diode gate with a transistor inverter for signal amplification. For negative input signals the R141 is seven 2-input AND gates which are NORed together. For ground inputs, it is seven 2-input OR gates NANDed together. This module is frequently used to mix multiple inputs to a pulse amplifier, or to compare the contents of two flip-flop registers.

The back-to-back diode circuits are possible because of an internal bias resistor connected to the input of each second stage diode. The bias holds the input of the second stage at —3v unless one of the first stage inputs is grounded. Propagation delay for output rise is similar to R111 delay. For output fall, delay is typically 100 nsec longer than R111 delay

under similar loading conditions, assuring sufficient pulse stretching to allow 70 nsec inputs. Output is typically too wide, however, to allow 2 mc rates. Maximum rate depends upon R141 loading, and may be as low as 1 mc.

INPUT: Standard 100-nsec pulses, standard levels of —3v and ground, or 70-nsec negative pulses such as those generated by the W607 Pulse Amplifier. Input load is 1 ma per input pair shared by the grounded inputs. When any pair of inputs is not being used, at least one of the two must be grounded.

OUTPUT: Standard levels of —3v and ground. The output can drive 20 ma of external load at ground. It has no internal load.
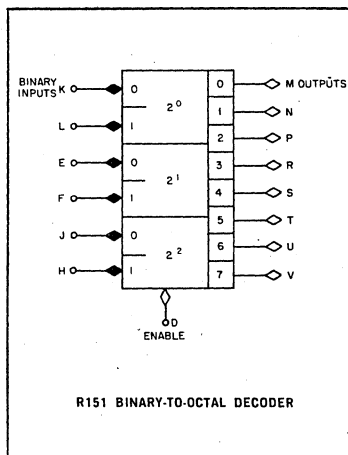
POWER: +10 v(A)/0.5 ma, —15 v(B)/19 ma.

155

R141 — $13.00

BINARY-TO-OCTAL DECODER
TYPE R151

R151 BINARY-TO-OCTAL DECODER

TRUTH TABLE

INPUTS							OUTPUTS							
J	H	E	F	K	L	D	M	N	P	R	S	T	U	V
-3v	0v	-3v	0v	-3v	0v	0v	0v	-3v	-3v	-3v	-3v	-3v	-3v	-3v
-3v	0v	-3v	0v	0v	-3v	0v	-3v	0v	-3v	-3v	-3v	-3v	-3v	-3v
-3v	0v	0v	-3v	-3v	0v	0v	-3v	-3v	0v	-3v	-3v	-3v	-3v	-3v
-3v	0v	0v	-3v	0v	-3v	0v	-3v	-3v	-3v	0v	-3v	-3v	-3v	-3v
0v	-3v	-3v	0v	-3v	0v	0v	-3v	-3v	-3v	-3v	0v	-3v	-3v	-3v
0v	-3v	-3v	0v	0v	-3v	0v	-3v	-3v	-3v	-3v	-3v	0v	-3v	-3v
0v	-3v	0v	-3v	-3v	0v	0v	-3v	-3v	-3v	-3v	-3v	-3v	0v	-3v
0v	-3v	0v	-3v	0v	-3v	0v	-3v	-3v	-3v	-3v	-3v	-3v	-3v	0v
						-3v	-3v	-3v	-3v	-3v	-3v	-3v	-3v	-3v
-3v	-3v	-3v	-3v	0v	-3v	0v	-3v	0v	-3v	0v	-3v	0v	-3v	0v
-3v	-3v	-3v	-3v	-3v	0v	0v	0v	-3v	0v	-3v	0v	-3v	0v	-3v
-3v	-3v	0v	-3v	-3v	-3v	0v	-3v	-3v	0v	0v	-3v	-3v	0v	0v
-3v	-3v	-3v	0v	-3v	-3v	0v	0v	0v	-3v	-3v	0v	0v	-3v	-3v
0v	-3v	-3v	-3v	-3v	-3v	0v	-3v	-3v	-3v	-3v	0v	0v	0v	0v
-3v	0v	-3v	-3v	-3v	-3v	0v	0v	0v	0v	0v	-3v	-3v	-3v	-3v

The R151 decodes binary information from three flip-flops into octal form. When the enable input is at ground, the selected output line is at ground and the other seven outputs are at —3v. When the enable input is at —3v, all outputs are at —3v. The internal gates are similar to those in the R111. The enable input is the common emitter connection of the output inverters. Typical total transition times are 75 nsec for output rise and 60 nsec for output fall.

INPUT: Binary — Standard levels of —3v and ground, 100 nsec minimum duration. Input load is

2.3 ma per grounded input when the inputs are binary, as in the first 8 lines of the truth table. The input current is 4 ma at ground when only one input is grounded, as in the last 6 lines of the truth table. **Enable** — Standard levels of —3v and ground, 100 nsec minimum duration. Input load at ground is 3 ma plus the current required by the load on the selected output when the inputs are binary, as in the

first 8 lines of the truth table. For other inputs, the load is 3 ma per selected output plus the loads on those selected outputs. The maximum input current is 10 ma when driven from an inverter collector. No more than one inverter can be placed in series with this pin and ground. If any external circuit brings an R151 output to ground, any gate being used to enable pin D must not drive anything else.

OUTPUT: Standard levels. Each octal output has a permanently attached 2-ma clamped load resistor. Each output can drive 7 ma of load at ground. If the enable input is permanently grounded, each output can drive 18 ma of load at ground. The length of the wire used to ground the enable input (pin D) should be kept as short as possible. Note: Simultaneous switching of R151 outputs is not assured. If adjacent R151 outputs are ORed together for example, the gate output may contain spikes.

POWER: +10 v(A)/0.9 ma, —15 v/32 ma.

R151 — $33.00
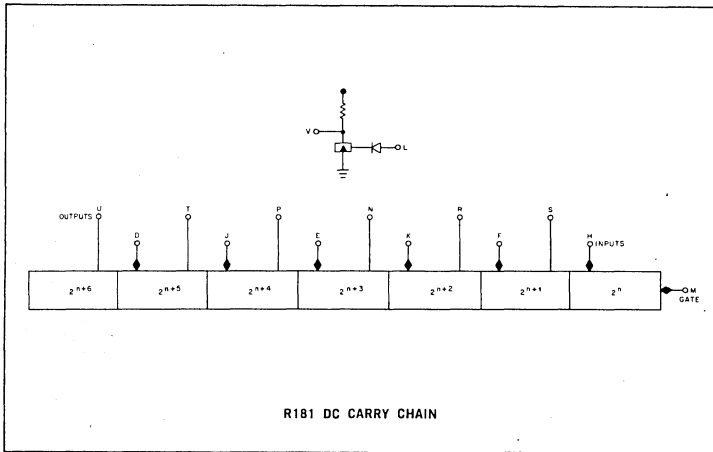
R181 DC CARRY CHAIN

The R181 DC Carry module is designed for building counters with no carry propagate delay. A 2-mc counter of any size, with all flip-flops switching simultaneously, can be constructed using the dc carry modules interconnected as in Figures 1 and 2 on the next page. The pulse amplifier interconnection of Figure 1 should be used between the first pair of dc carry modules. The dc carry interconnection of Figure 2 may be used between all following pairs of stages.

If the time between input count pulses is greater than $400 + 100(N-1)$ nsec (where N is the number of dc carry modules), the pulse amplifier connection is not necessary and the dc interconnection may be used between all dc carry modules.

The carry module contains an independent 1-input diode gate and six interconnected diode gates with two, three, four, five, six, and seven inputs respectively. The outputs are all similar to the Type R107.

INPUT: Inputs are DEC standard levels. The input loads on Pins M and H are 6 ma each. The load on Pin F is 5 ma; on Pin K it is 4 ma; on Pin E, 3 ma, etc. The loads presented by Pins D and L are 1 ma each. All loads are at ground, there is no load at $-3v$.

OUTPUTS: Each output is at ground only when the input to the common gate and all inputs to gates of lesser significance are at -3 v. Each output circuit can supply 18 ma at ground and has an internal load of 2 ma.
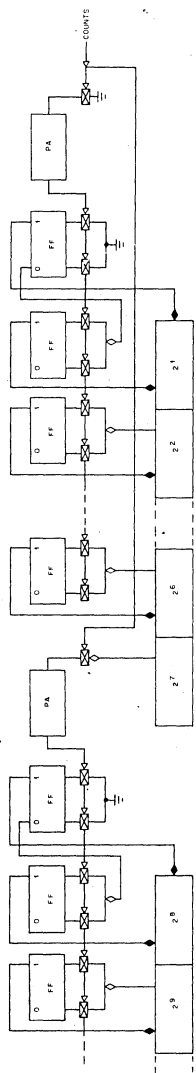
POWER: $+10$ v(A)/0.7 ma, -15 v(B)/26.2 ma.
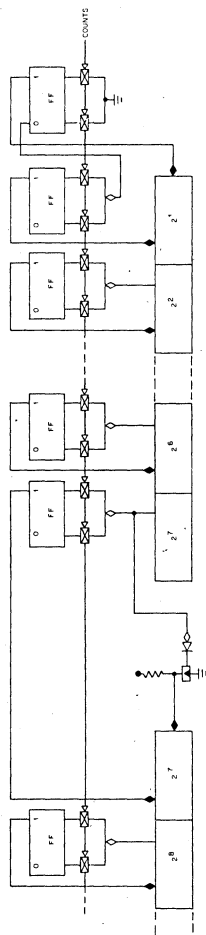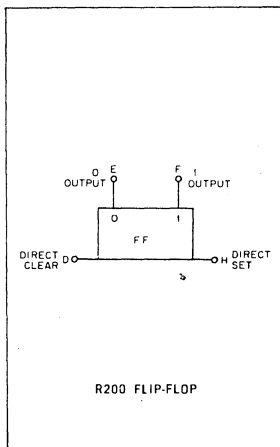
R181 — $35.00

Figure 1   Pulse Amplifier Interconnection

Figure 2   DC Interconnection

FLIP-FLOP
TYPE R200

```
            O  E        F  1
        OUTPUT o       o OUTPUT
            ┌──────────────┐
            │  O        1  │
            │     F F      │
DIRECT   D o─┤              ├─o H  DIRECT
CLEAR       └──────────────┘      SET
                   ↘
```

R200 FLIP-FLOP

The R200 is a basic flip-flop for use in set-reset applications. It can be set and cleared at any frequency up to 2 mc. A set input makes the 1 output go to —3v and the 0 output to ground; a clear input makes the 0 output go to —3v and the 1 output to ground.

INPUT: Direct Set and Clear — A standard 100-nsec pulse or a ground level of 100 nsec minimum duration activates the input; the load at ground is 1 ma. When not in use, the direct set and clear terminals must be at —3v. If both inputs are held at ground, both outputs are at —3v. **Collector Triggering** — The flip-flop can also be set or cleared through its output by a diode gate or a diode network. The triggering circuit load is the external load on the output terminal being driven plus the internal load.

OUTPUT: Standard levels. Each output can drive 17 ma of external load at ground. The internal load is 4 ma. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output fall time. The load is sufficient if the positive transition at the opposite terminal reaches —1v within 80 nsec after the flip-flop is pulsed.
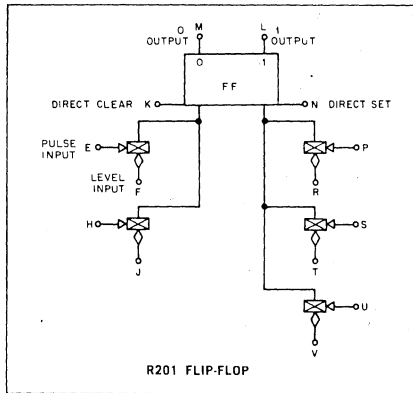
Note: Additional driving capability at 3 v is required by some circuits outside the R series. Auxiliary clamped loads W002 and W005 are available for this purpose.

POWER: +10 v(A)/0.3 ma, —15 v(B)/16 ma.

R200 — $9.50

FLIP-FLOP
TYPE R201

R201 FLIP-FLOP

The R201 Flip-Flop has direct set and clear inputs and five diode-capacitor-diode (DCD) gates. Because of this large number of inputs, the R201 can be used in any of the following applications without additional gating:

1. Any two of the following as well as conditional read-in from an external source: up counter, shift register, jam transfer buffer, ring counter, and switch tail ring counter. Down counters or up-down counters can also be implemented if conditional read-in is not required

2. BCD counter with read-in from two sources.

3. Buffer register or control flip-flop with readin from five sources.

4. Special Counts of 2^k ($2^k + 1$).

INPUT: Direct Set and Clear — A standard 100-nsec pulse or a ground level of 100 nsec minimum duration activates the input; the load at ground is 1 ma. When not in use, the direct set and clear terminals must be at —3v. If both inputs are held at ground, both outputs will be at —3v. If the flip-flop is used in an up counter with carry gates enabled, the direct clear pulse must be at least 400 nsec long to suppress carry propagation. Similarly, if the down counter gates are enabled, the direct set pulse must be 400 nsec long. DCD Gates, Level — Standard levels of —3v and ground. DCD gates are internally conditioned by the state of the flip-flop, complement inputs may be formed by tying 1 and 0 DCD gate inputs together. A DCD gate is enabled by a ground level and disabled by a —3v level. The conditioning level must be present for at least 400 nsec before the gate is pulsed. The level input represents

2 ma of load at ground. When 1 and 0 DCD gates are connected in parallel to form a complement input, the total level load is 3 ma at ground. Pulse — Standard 100-nsec pulses (—3v to ground) at any frequency up to 2 mc. It can also be driven by positive-going level changes (—3v to ground) with rise times of 60 nsec max and duration of 100 nsec min. Prior to operation the input must have been at —3v for at least 400 nsec. The pulse input represents 3 ma of load at ground. When a pair of 1 and 0 DCD gates have a common pulse input, as in complementing or shifting, the total pulse load is 4 ma at ground. Collector Triggering — The flip-flop can also be set or cleared from its outputs by a diode gate circuit or a diode network. The triggering circuit load is the external load on the terminal being driven by the circuit plus the internal load on that terminal.

OUTPUT: Standard levels of —3v and ground. The carry propagate time is 70 nsec. The 0 terminal can drive 11 ma of external load at ground. The internal load is 10 ma. The 1 terminal can drive 13 ma of external load at ground. The internal load is 8 ma. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output fall time. The load is sufficient if the positive transition at the opposite terminal reaches —1v within 80 nsec after the flip-flop is pulsed.
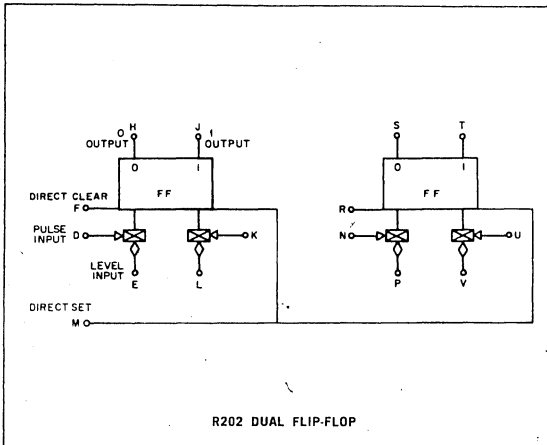
Note: Additional driving capability at —3v is required by some circuits outside the R series. Auxiliary clamped loads W002 and W005 are available for this purpose.

POWER: +10 v(A)/0.2 ma, —15 v(B)/27 ma.

R201 — $22.00

R202 DUAL FLIP-FLOP

The R202 Dual Flip-Flop contains two identical flip-flops. Each has a direct clear input, a common set input, and two DCD gates. The R202 can perform in any one of the following applications without additional gating: up counter, down counter, shift register, ring counter, jam transfer buffer, and switch tail ring counter.

INPUT: Direct Set and Clear — A standard 100 nsec pulse or a ground level of 100 nsec minimum duration activates the input; the load at ground is 1 ma for each clear input, and 2 ma for the set input. When not in use, the direct terminals must be at —3v. If the flip-flop is in an up counter with carry gates enabled, direct clear pulses must be at least 400 nsec long to suppress carry propagation. In like manner, a 400 ns set pulse must be used when the flip-flops are arranged as a down counter. If both inputs are held at ground, both outputs are at —3v. **DCD Gates, Level** — Standard levels of —3v and ground. Because DCD gates are internally conditioned by the state of the flip-flop, a complement input may be formed by tying the 1 and 0 DCD gate inputs together. A DCD gate is enabled by a ground level and disabled by a —3v level. The conditioning level must be present for at least 400 nsec before the gate is pulsed. The level input represents 2 ma of load at ground. When 1 and 0 DCD gates are connected in parallel to form a complement input, the total level load is 3 ma at ground. **Pulse** — Standard 100-nsec pulses (—3v to ground) at any

frequency up to 2 mc. It can also be driven by positive-going level changes (—3v to ground) with rise times of 60 nsec max and duration of 100 nsec min. Prior to operation the input must have been at —3v for at least 400 nsec. The pulse input represents 3 ma of load at ground. When a pair of 1 and 0 DCD gates have a common pulse input, as in complementing or shifting, the total pulse load is 4 ma at ground. **Collector Triggering** — The flip-flop can also be set or cleared through its outputs by a diode gate circuit or a diode network. The triggering circuit load is the external load on the terminal being driven by the circuit plus the internal load on that terminal (6 ma each).

OUTPUT: Standard levels. The carry propagate time is 70 nsec. Each terminal can drive 15 ma of external load at ground and has an internal load of 6 ma. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output fall time. The load is sufficient if the positive transition at the opposite terminal reaches —1 v within 80 nsec after the flip-flop is pulsed.

Note: Additional driving capability at —3v is required by some circuits outside the R series. Auxiliary clamped loads W002 and W005 are available for this purpose.

POWER: +10 v(A)/0.5 ma, —15 v(B)/34 ma.

TRIPLE FLIP-FLOP
TYPE R203

R203 TRIPLE FLIP-FLOP
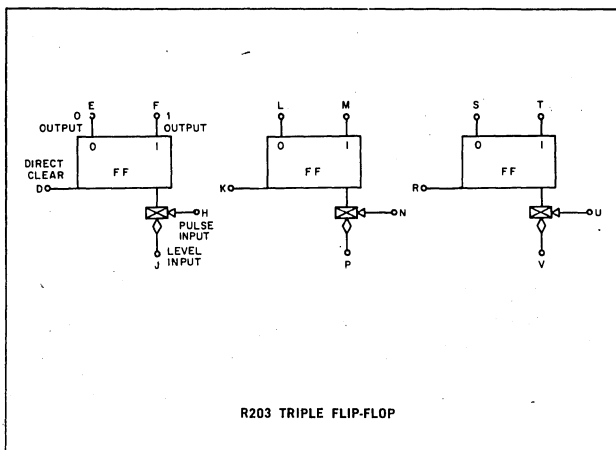
The R203 Triple Flip-Flop contains three identical flip-flops. Each flip-flop has a direct clear input and a DCD gate for conditional read-in.

INPUT: Direct Clear — A standard 100-nsec pulse or a ground level of 100 nsec minimum duration activates the input; the load at ground is 1 ma. When not in use, the direct clear terminal must be at —3v. **DCD Gates, Level** — Standard levels of —3v and ground. A DCD gate is enabled by a ground level and disabled by a —3v level. The conditioning level must be present for at least 400 nsec before the gate is pulsed. The level input represents 2 ma of load at ground. **Pulse** — Standard 100-nsec pulses (—3v to ground) at any frequency up to 2 mc. The flip-flop can also be driven by positive-going level changes (—3v to ground) with rise times of 60 nsec max and duration of 100 nsec min. Prior to operation the input must have been at —3v for at least 400

nsec. The pulse input represents 3 ma of load at ground. **Collector Triggering** — The flip-flop may also be set or cleared from its outputs by a diode gate circuit or a diode network. The triggering circuit load is the external load on the terminal being driven by the circuit plus the internal load on that terminal.

OUTPUT: Standard levels of —3v and ground. The 0 terminal can drive 15 ma of external load at ground. The internal load is 6 ma. The 1 terminal can drive 17 ma of external load at ground. The internal load is 4 ma. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output fall time. The load is sufficient if the positive transition at the opposite terminal reaches —1v within 80 nsec after the flip-flop is pulsed.

POWER: +10 v(A)/0.7 ma, —15 v(B)/40 ma.

R203 — $28.00

QUADRUPLE FLIP-FLOP
TYPE R204

R204 QUADRUPLE FLIP-FLOP
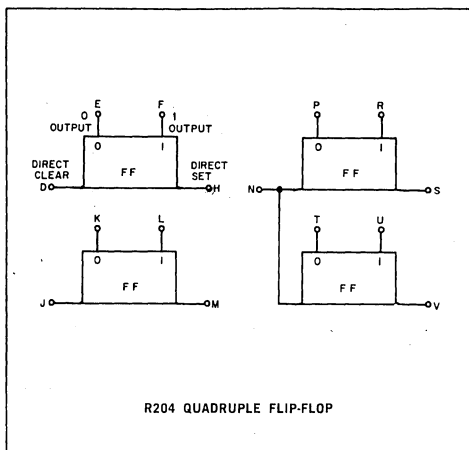
The R204 Quadruple Flip-Flop contains four flip-flops. Each has direct set and direct clear inputs. Two of the flip-flops share a common direct clear input. The R204 is used in general control applications. A set input makes the 1 output —3v and the 0 output ground; a clear input makes the 0 output —3v and the 1 output ground.

INPUT: Direct Set and Clear — A standard 100-nsec pulse or a ground level of 100 nsec minimum duration activates the input; the load at ground is 1 ma per flip-flop. When not in use, the direct set and clear terminals must be at —3v. If both inputs are held at ground, both outputs will be at —3v. **Collector Triggering** — The flip-flop can also be set or cleared through its outputs by a diode gate circuit or a diode network. The triggering circuit load is the external load on the terminal being driven by the circuit plus the internal load on that terminal. The internal load is 4 ma for each terminal.

OUTPUT: Standard levels of —3v and ground. Each terminal can drive 17 ma of external load at ground, and has an internal load of 4 ma. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output fall time. The load is sufficient if the positive transition at the opposite terminal reaches —1v within 80 nsec after the flip-flop is pulsed.

Note: Additional driving capability at —3v is required by some circuits outside the R series. Auxiliary clamped loads W002 and W005 are available for this purpose.

POWER: +10 v(A)/0.9 ma, —15 v(B)/42 ma.

R204 — $28.00
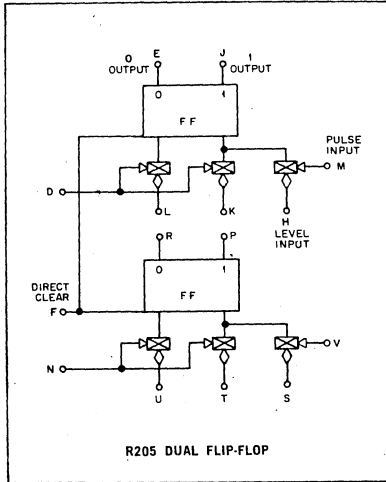
R205 DUAL FLIP-FLOP

The R205 contains two identical flip-flops with a common direct clear input. Each has three DCD gates, and can be collector-triggered at either output by a diode-transistor gate or a diode network. The R205 can be used in any of the following applications without additional gating: up counter, down counter, shift register, ring counter, or jam transfer register.

INPUT: Direct Clear — A standard 100-nsec pulse or a ground level of 100 nsec minimum duration activates the input; the load at ground is 1 ma. When not in use, the direct clear terminal must be at —3v. If the flip-flop is used in an up counter with carry gates enabled, direct clear pulses must be at least 400 nsec long to suppress carry propagation. **DCD Gates** — DCD gates are standard levels of —3v and ground. Because DCD gates are internally conditioned by the state of the flip-flop, complement inputs may be formed by tying 1 and 0 DCD gate inputs together. A DCD gate is enabled by a ground level and disabled by a —3v level. The conditioning level must be present for at least 400 nsec before the gate is pulsed. The level input represents 2 ma of load at ground. When 1 and 0 DCD gates are connected in parallel to form a complement input, the total load is 3 ma at ground. **Pulse** — Standard 100-nsec pulses (—3v to ground) at any frequency up to 2 mc. It can also be driven by positive-going level changes (—3v to ground) with rise times of 60 nsec

max and duration of 100 nsec min. Prior to operation the input must have been at —3v for at least 400 nsec. The pulse input represents 3 ma of load at ground. When a pair of 1 and 0 DCD gates have a common pulse input as in complementing or shifting, the total pulse load is 4 ma at ground. **Collector Triggering** — Triggering circuit load is the external load on the terminal being driven plus the internal load on that terminal. Internal load for the 1 terminal is 6 ma; for the 0 terminal, 8 ma.

OUTPUT: Standard levels. Carry propagation time is 70 nsec. The 0 terminal can drive a 13-ma external load at ground; the 1 terminal, 15 ma at ground. Internal load on the 1 terminal is 6 ma; for the 0 terminal, 8 ma. If more than 18 in. of wire is attached to an output, additional clamped loads (see the W002, W005) should be connected to decrease the output fall time. The load is sufficient if the positive transition at the opposite terminal reaches —1v within 80 nsec after the flip-flop is pulsed.
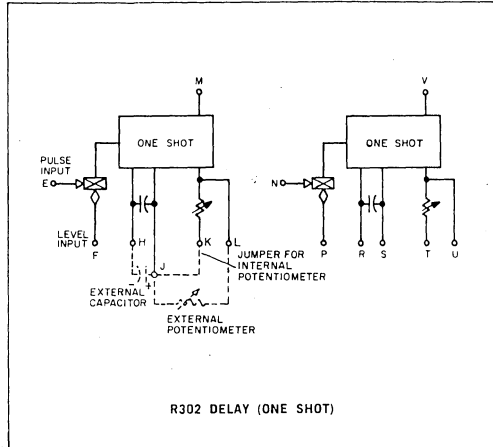
Note: Additional driving capability at —3v is required by some circuits outside the R series. Auxiliary clamped loads W002 and W005 are available for this purpose.

POWER: +10 v(A)/0.5 ma, —15 v(B)/36 ma.

DELAY (ONE SHOT)
TYPE R302

R
SERIES

R302 DELAY (ONE SHOT)

The R302 contains two delays (one-shot multivibrators) which are triggered by DCD gates. Each delay is independent and can be externally or internally controlled. When the input is triggered, the output changes from its normal ground level to −3v for a predetermined, adjustable period of time and then returns to ground. The length of the delay is determined by the capacitor and potentiometer. External capacitors can be attached between terminals H and J (or R and S), J (S) being the more positive terminal. The 20-kilohm internal potentiometer can be used by putting a jumper between terminals J and K (or S and T). External potentiometers can be attached between terminals J and L (S and U). The total resistance between these terminals must not exceed 20 kilohm. A 20% change in power supply voltage will change the delay less than 2%. Delay jitter due to power supply ripple is less than 0.2%.

The expected delay of any combination (with more than a 500-pf capacitance) can be estimated by the following formula:

$$\text{Delay} \quad RC$$

where the delay time is in nsec, R in kilohm and C in pf. The total capacitance, C, equals 220 pf of internal capacitance plus any external capacitance used. The resistance, R, is equal to the resistance of the potentiometer plus 1 kilohm of internal resistance. The minimum delay is 400 nsec. The minimum delay in nsec for a given external capacitor is C where C is equal to the external capacitance in pf plus a 220-pf internal capacitance. The recovery time is twice the minimum delay.

The delay range for typical capacitors used with the internal potentiometer is given in the table that follows:

DELAY RANGES

Total Capacitance Used (External + 220 pf Internal)	Minimum Delay Range	Recovery Time
Internal 220 pf only	400-4000 nsec	800 nsec
2000 pf	4-40 μsec	8 μsec
20 nf	40-400 μsec	80 μsec
200 nf	0.4-4 msec	0.8 msec
2000 nf	4-40 msec	8 msec
20 μf	40-400 msec	80 msec
200 μf	400-4000 msec	800 msec

R302 — $44.00

165

Large electrolytic capacitors can have internal leakage enough to substantially modify time delay. For best results, use wet-slug tantalum electrolytics for delays of several seconds or more. Four volt ratings are adequate in most cases, but 6 or 8 volt ratings may be desirable to further reduce leakage in some cases.

Remote Control Wiring: Noise picked up on wires leading to remote timing capacitors or rheostats tends to synchronize the end of the delay period (or it could cause false triggering in extreme cases). Even for 1 ft control wires, a grounded shield may be advisable if smooth control and freedom from jitter are essential.

INPUT: Level — Standard levels of —3v and ground. A DCD gate is enabled by ground level and disabled by a —3v level. The conditioning level must be present for at least 400 nsec before the gate is pulsed. The level input represents 2 ma of load at ground. **Pulse** — Standard 100-nsec pulses (—3v to ground). It can also be driven by positive-going level changes (—3v to ground) with rise times of 60 nsec max and duration of 100 nsec min. Prior to operation the input must have been at —3v for at least 400 nsec. The pulse input represents 3 ma of load at ground. The delay cannot be set from its output terminal.

OUTPUT: Standard Level of —3v for the duration of the delay time. The output can drive 18 ma of external load at ground. The internal load is 2 ma.

POWER: +10 v(A)/0.6 ma; —15 v(B)/88 ma.

R303 INTEGRATING ONE SHOT
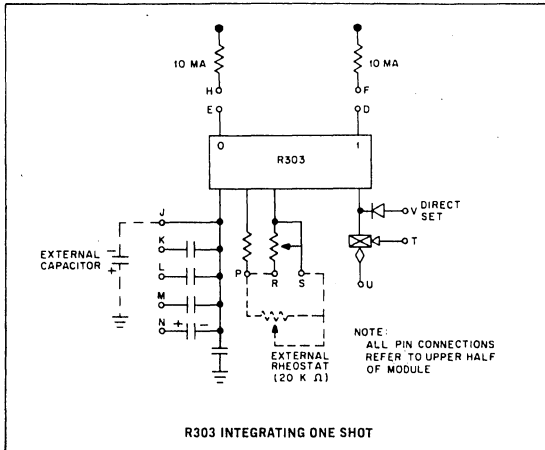
The R303 contains a zero recovery time multivibrator and complementary output buffers. Its unusual characteristics include the ability to respond to inputs even while in the ONE state, so that successive inputs above a preset frequency can postpone the return to ZERO indefinitely. This characteristic can be used, for example, to detect gaps in an otherwise continuous pulse train, or to determine whether an input pulse rate is above or below a preset frequency threshold. If the delay setting of this module exceeds the time it takes +10 and —15 to reach 90% of their final valves on power turn-on, this module will initially go to the ONE state. The above conditions allow the R303 to be used for system initialization on power turn-on.

Delay is 3.5 microseconds to 0.7 second. Jitter is less than 1.4% peak-to-peak. Precision: Delay time will change less than 2% for a change of 20% in supply voltage.

INPUTS: Direct Set — A standard 100 nsec pulse or a ground level of at least 100 nsec duration starts the delay. The load at ground is 1 ma. At least 90% to 99.5% of total delay (for 0 and 20 kilohm rheostat setting, respectively) will not be measured out until —3v is restored, a fact which may be important if this input is grounded for longer than 300 nsec. DCD Gate — Same as R302.

OUTPUTS: Each output can drive 18 ma at ground, 0 ma at —3v. Extra 10 ma clamped loads may be connected to change the driving capability at each output to 8 ma at ground, 7 ma at —3v. The ONE output will be at —3v during the delay period and ground otherwise. The ZERO output is grounded during the delay period and —3v otherwise.

POWER: +10v(A)/6 ma; —15v/75 ma.

CONTROLS: To choose desired range of delay, ground the appropriate capacitor pin K through N (for minimum delay range, ground none of these). Ranges are separated by approximately a factor of ten. For extra long delays, connect an external capacitor from pin J to ground. To use the internal rheostat, connect pin P to pin R. For external control, connect a variable resistance no larger than 20,000 ohms from pin P to pin S.

EXTERNAL CONTROL: Delay times may be controlled by external R and C in the same manner as described for R302. Substantially the same R and C are required in the R303 as in the R302 for a given delay, taking into account the ten times larger minimum capacitance built into the R303. If electrolytic capacitors are used, at least a 6-volt rating is required.

Capacitor Values (MFD): Internal – 0.0022, Pin K – 0.027, Pin L – 0.39, Pin M – 3.9, Pin N – 39.0.

R401 VARIABLE CLOCK
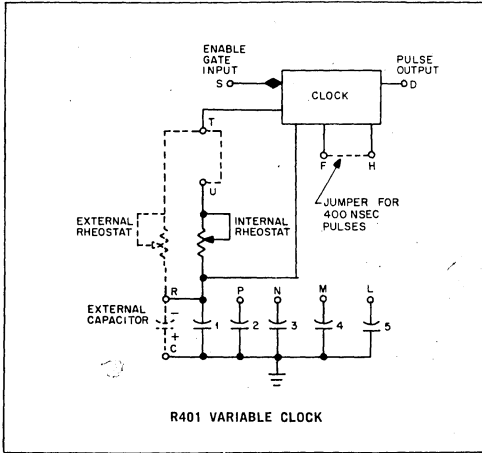
The R401 Variable Clock is a gateable clock that produces standard 100-or 400-nsec pulses from a stable RC-coupled oscillator. The variable clock is often used as a primary source of timing for large systems.

The frequency of the R401 Clock is variable from 30 cps to 2.0 mc. Five capacitors provide coarse frequency control, and a built-in 20,000-ohm potentiometer permits fine adjustment. Terminals for an external potentiometer or capacitor are available. The maximum size of the external potentiometer to be used is 20,000 ohms.

FREQUENCY SELECTION

Select Pin R	C_1 = 82 pf	300 kc to 2.0 mc
Pin P	C_2 = 1200 pf	30 kc to 375 kc
Pin N	C_3 = 0.015 MFD	3.5 kc to 40 kc
Pin M	C_4 = 0.15 MFD	300 cps to 4.5 kc
Pin L	C_5 = 2.2 MFD	30 cps to 340 cps

Lower frequencies may be obtained by adding an external capacitor between pins R and C. A 20%

change in power supply voltage will change the prf less than 1%. The pulse-to-pulse jitter is less than 0.2%.

INPUT: The clock is enabled by a -3 v level or an open circuit at its enable gate input. The total transition time from the time the gate is enabled until the first pulse reaches 90% of its amplitude is approximately 45 nsec. The pulses that follow appear at the frequency selected. The clock may be disabled by applying a ground level at the enable gate pin S. The enable gate loading is 4 ma at ground. Disable duration must exceed the period to which the clock is set.
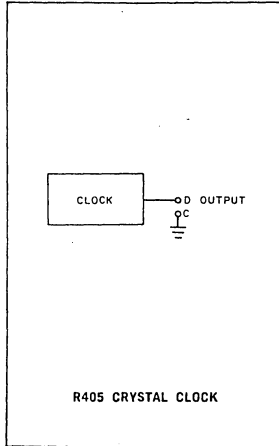
OUTPUT: The output is a standard 100 nsec pulse -3 volts to ground and may be changed to a 400 nsec pulse by connecting pin F to pin H. The output can drive 70 ma of external load at ground. The internal load is 3 ma.

POWER: $+10$ v(A)/1.3 ma; -15 v(B)/19 ma.

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R401 — $45.00

R405 CRYSTAL CLOCK

The Type R405 employs a series resonant crystal oscillator, squaring circuit, and output pulse amplifier. The crystal clock's output frequency remains within 0.01% of specified value between 0°C and +55° C. The clock frequency is specified anywhere in the 5 kc to 2 mc range by the customer and is stamped on the crystal can.
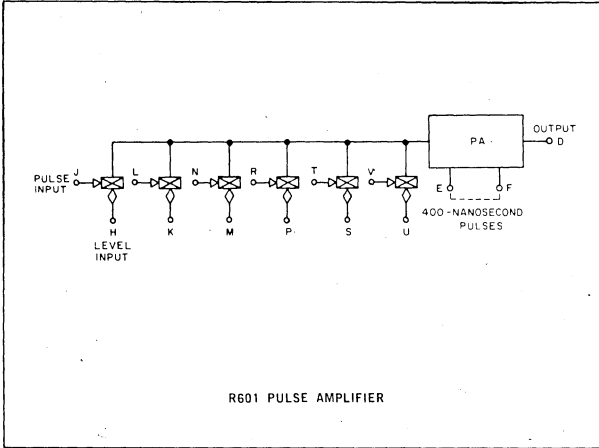
OUTPUT: 100-nsec pulse, —3v to ground. The output can drive 70 ma of external load at ground. Internal load is 3 ma.

POWER: +10 v(A)/5.4 ma; —15 v(B)/50 ma.

R405 — $100.00

R601 PULSE AMPLIFIER

The R601 is a pulse amplifier that standardizes pulses in amplitude and width. Outputs may be either standard 100- or 400-nsec pulses (—3v to ground). It has six DCD gates so that inputs from as many as six sources may be mixed. Input pulses can occur at any frequency up to 2 mc for 100-nsec pulse outputs and up to 1 mc for 400-nsec outputs. Delay through the pulse amplifier is approximately 50 nsec.

DCD GATE INPUTS: Level — Standard levels of —3v and ground. A DCD gate is enabled by a ground level and disabled by a —3v level. The conditioning level must be present for at least 400 nsec before the gate is pulsed. The level input represents 2 ma of load at ground. **Pulse** — 100 nsec or longer pulses, —3v to ground, at any frequency up to 2 mc. It can also be driven by positive-going level changes (—3v to ground) with rise times of 60 nsec max, and dura-

tion of 40 nsec min. The input must have been at —3v for at least 400 nsec prior to operation of any input. The pulse input represents 3 ma of load at ground.

OUTPUT: With terminals E and F connected together, the output is a standard 400-nsec pulse (—3v to ground). With E and F open, the output is a standard 100-nsec pulse, —3v to ground. The output (for either 100- or 400-nsec pulses) can drive 70 ma of external load at ground. The internal load is 3 ma.

Pulse amplifier outputs may be paralleled for a logical OR.

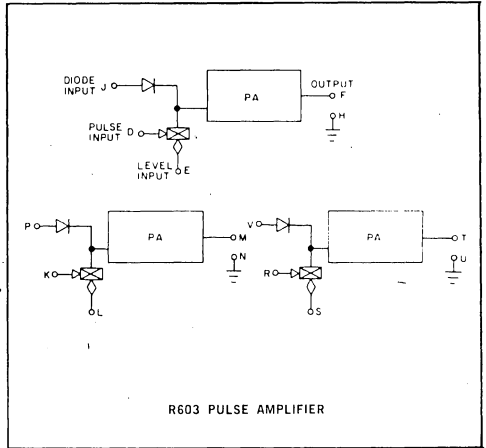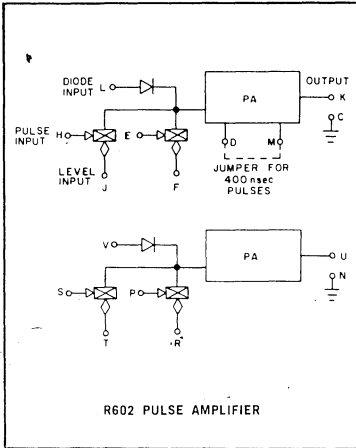Pulse lines and ground lines should be kept as short as possible.

POWER: +10 v(A)/1.1 ma; —15 v(B)/33 ma.

R601 — $25.00

PULSE AMPLIFIERS
TYPES R602, R603

R602 PULSE AMPLIFIER

R603 PULSE AMPLIFIER

The R602 and R603 contain pulse amplifiers for power amplification and for standardizing pulses in amplitude and width. Each amplifier produces standard 100-nsec pulses and one section of the R602 can also produce 400 nsec pulses. DCD gates and a single diode input permit inputs from many sources to be mixed. Input pulses can occur at any frequency up to 2 mc for 100 nsec pulses, and up to 1 mc for 400 nsec pulses. Delay through the pulse amplifier is approximately 50 nsec.

INPUTS: Level and Pulse — Same as R601. **Diode** — Standard 100-nsec pulses (—3v to ground) or

positive-going level changes (—3v to ground) with a rise time of 60 nsec max. The input level must be

returned to —3v for at least 400 nsec before another input may occur at either the diode or the DCD gate input. The diode input represents a 1-ma load at ground.

OUTPUTS: Outputs are standard 100 nsec pulse, —3v to ground (except pin K of R602, which may be changed to 400 nsec pulses by connecting pin D to pin M). Each output can drive up to 70 ma load at ground. The internal load is 3 ma. Pulse amplifier outputs may be paralleled to obtain a logical OR. Pulse lines and grounds should be kept as short as possible.

POWER: R602: + 10 v(A)/2.2 ma; —15 v(B)/45 ma.
R603: + 10 v(A)/3.3 ma; —15 v(B)/57 ma.

R602 — $22.00
R603 — $28.00

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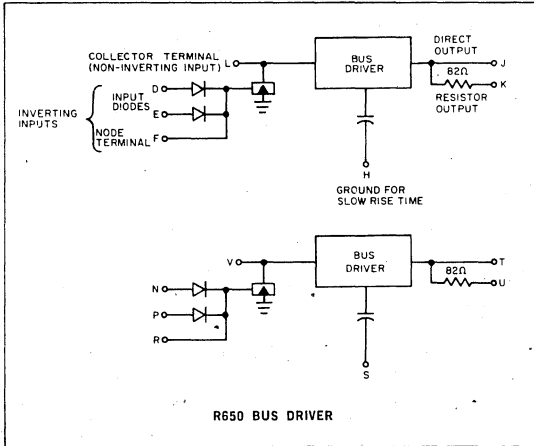
R650 BUS DRIVER

The R650 contains two inverting bus drivers for driving heavy current loads to either ground or negative voltages. The four input terminals make the R650 a versatile logic element as well. The diode inputs D and E (N and P) are the principal inputs. They form a NAND gate for negative inputs or a NOR gate for ground inputs. Gate inputs, such as the R001 or R002, can be added through the node terminal F (R). Other gating sources may be mixed with the gate inputs by using collector terminal L (V).

The bus drivers operate at frequencies up to 2 mc with typical rise and fall times of 25 nsec. The typical total transition times are 60 nsec for output rise and 65 nsec for output fall.

By grounding pin H (S) the rise and fall time can be increased to avoid ringing on exceptionally long lines. The driver then operates at frequencies up to 500 kc with typical rise delay of 50 nsec, fall delay of 50 nsec, and total transition time of 800 nsec for

output rise and 700 nsec for output fall. Terminal K (U) can be used for driving coaxial cable.

INPUT: Standard levels at frequencies up to 2 mc (up to 500 kc with H or S grounded). The diode inputs, including any diodes attached to the node terminal, represent 1 ma of load, shared by all grounded inputs. Collector terminal L (V) represents 10 ma of load at ground. External clamped loads should not be connected to this terminal. The combined length of all leads attached to the node terminal should not exceed 6 in. The combined length of all leads attached to the collector terminal should not exceed 18 in.

OUTPUT: Direct — Standard levels. The output can drive 20 ma of external load at either ground or —3v. **Resistor** — Standard levels. The resistor output drives 90-ohm coaxial cable such as RG-62-U. The output can drive 5 ma of external load at either ground or —3v.

POWER: +10 v(A)/50 ma; —15 v(B)/81 ma.

W
SERIES

W SERIES
INTRODUCTION

The W series provides input-output compatibility between FLIP CHIP Modules and other digital devices. The range of W series inputs and outputs is wide. Inputs up to ± 48v, outputs up to ± 135v or up to 10 amp, inputs from source impedances as high as 100 KΩ, floating systems, bouncing contacts, long transmission lines, all can be handled easily by one or more of these modules. A few of their uses are listed below.

Clamped Loads

The inputs of all R series circuits draw current only when the input voltage is at ground. Other DEC circuits may require input current to be supplied at the negative voltage level. The use of additional clamped load resistors allows an R series module to be preloaded so that it is able to supply higher currents at the --3v level.

It is also possible to obtain higher drive capability at ground from DEC circuits which normally supply current at 3v. In this case the normal clamped load resistor would be replaced by one which is a lighter load at ground. The Type W002 contains clamped load resistors of this type. Care should be exercised when such a lighter load is used since an increased fall time will result.

A clamped load can also be used as a short-circuit proof, --3v supply for toggle switches or patchboards.

Cable Connectors

Cable connectors provide a convenient means for going from one section of logic to another. They may also be used to hold series isolation resistors or shunt termination resistors. They allow large systems to be broken into pluggable subsystems for efficiency in checkout and field maintenance.

Drivers

The Types W050 and W051 provide signals for indicator lights, relays, and solenoids. W051 outputs go to ground and can therefore be used to drive R111 or similar diode inputs. W061 can drive NIXIE tubes, or other loads returned to positive voltages. W061 outputs supply sufficient current for most projection type numerical displays as well, and for relays and solenoids too large for W051 circuits. W040 is the next larger driver, and has sufficient output capability for most electromechanical devices. Stepping motors and other exceptionally high current devices may require the use of a W042. Line voltage can be controlled by the W080 module, and if a Triac is added to its output this module allows up to 1 kilowatt of AC power to be solid-state controlled by FLIP CHIP logic.

Input Converters

The W501 allows external low frequency or noisy signals to be converted to DEC standard levels. The Type W510 converts positive signals of a few volts amplitude into DEC levels. Other external levels that are noise-free and have a swing greater than 3v can usually be biased so that they can be brought directly into the logic modules. Pulses, which are noise-

free and fast, can usually come directly into the pulse amplifiers. Small signals, with amplitudes of a few millivolts or more, can be brought into the logic system using W520 or A501 comparators. Floating-battery signals such as those in process controls can be converted by W502 modules. The W500 buffers inputs from photocells, vacuum-tube equipment, and other high-impedance sources. Some types of computer interface can use the W590 module. W700 filters bounce from contact signals not requiring W501 standardization.

Output Converters

The W600 and W601 provide a means of driving low power digital devices requiring signals in the range of —15 to +20v. Most drivers can be used as output converters under some circumstances. Some types of computer interface can use the W690 module. Many types of output pulse requirements can be met by W607 or W640 pulses.

Communications Interface Modules

The W706, W707, and W708 are functional modules which are used to provide Teletype communications system interfaces to computers and other parallel devices. These units contain serial to parallel and parallel to serial conversion for 5-bit and 8-bit communication systems.

Accessory Modules

The accessory modules include blank boards for constructing special circuits, a module extender, which allows access to the module while it is connected to the mounting panel, and a system module adapter, which allows DEC system modules to be connected into a FLIP CHIP mounting panel. Related are the A series amplifier boards A990 and A992, for mounting operational amplifiers of various types.

Pulse Conversion

See the application note with the above heading for a table of pulse conversions between FLIP CHIP and earlier System Modules and Laboratory Modules made by DEC. All modules use logic levels of ground and —3v, so in many cases no conversion at all is required.

W002 CLAMPED LOAD
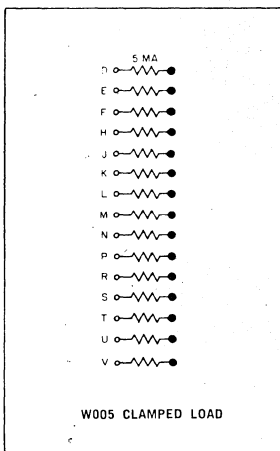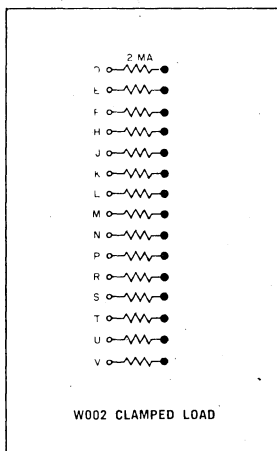
W005 CLAMPED LOAD

The W002 contains 15, 2-ma clamped loads. These can be used for clamping voltages at the output of inverter collectors in R-series modules, or for converting B-series modules to work with R-series.

OUTPUT: When the clamped load output is grounded, it draws 2 ma. When it is at —3v, it can supply up to 1.4 ma.

POWER: —15 v(B)/46 ma.

The W005 contains 15, 5-ma clamped loads. These can be used for clamping voltages at the output of inverter collectors in B-series modules, or for converting R-series modules to work with B-series. Two of these clamped loads in parallel are equivalent to one B-series clamped load.

OUTPUT: When the clamped load terminal is grounded, it draws 5 ma. When at —3v, it can supply up to 3.5 ma.

POWER: —15 v(B)/91 ma.

W002 — $13.00
W005 — $15.00

The W018 and W023 provide 18 line ribbon cable connections to FLIP CHIP mounting panels. In the W018 connection to each pin is through a series low leakage silicon diode. The W023 provides unbroken signal lines from the cable to the connector pin.

When these cables are used with 4917 or 4918 indicators, the W018 must be located at the FLIP CHIP panel and the W023 inserted in the indicator socket connector. Cables may be ordered with connector modules on both ends or on one end only. Cable length may be specified in increments of 1 inch.

For ordering information, see W021, W022, and W028 on next page.
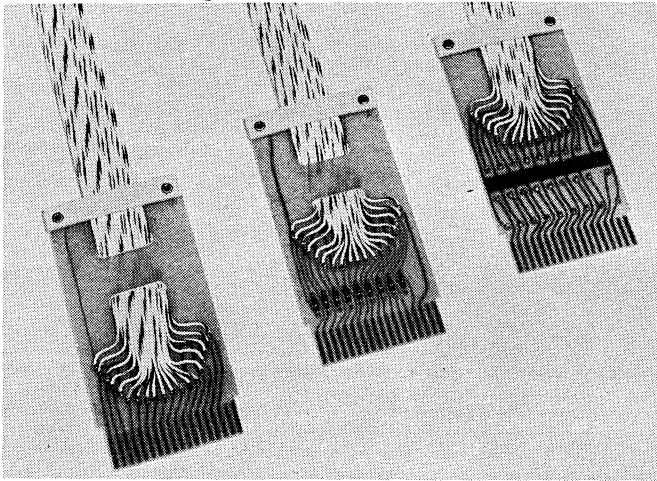
Care should be taken when using the W023 for other purposes, since the Power Pins (A, B) are unprotected.

Type	Price with Cable Attached	Type	Price without Cable
W018	$18.00*	W018U	$9.00
W023	$13.00*	W023U	$4.00
*Ribbon Cable: Add $.60 per foot, or fraction			

The W021, W022, and W028 provide cable connections to the FLIP CHIP mounting panel. The cable is a 19-conductor ribbon with nine signal leads and ten shields. The signal leads are connected to pins D, E, H, K, M, P, S, T and V. The shields are internally connected together and to pins C, F, J, L, N, R, and U.

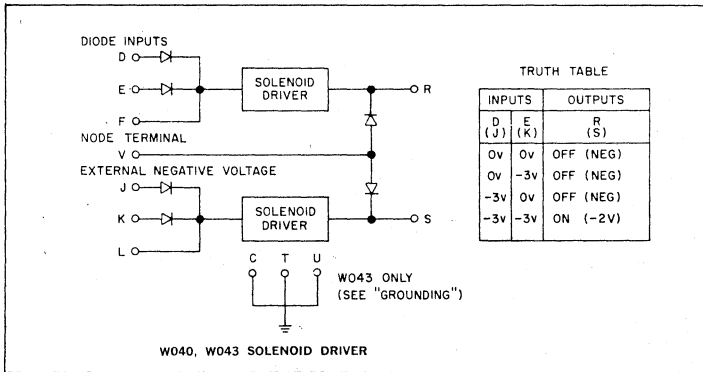In the W021, the signal leads are connected directly to the signal pins. In the W028, jumpers are available for series or shunt terminators. The Type W022 has a 100-ohm shunt terminator from each signal wire to the shield.

Connectors may be ordered in like or unlike pairs. They may also be ordered separately, in which case the other end of the cable is left free. Cable length may be specified in increments of 1 in.

ORDERING INFORMATION: To insure clear communication, use the format below.

$$\underline{\textbf{W02X}} \quad - \quad \textbf{XXX} \quad - \quad \underline{\textbf{W02X}}$$

first connector

second connector (if any)

type of cable
R = RIBBON
C = CO-AXIAL
(Z_O = 93Ω)

inches of cable

EXAMPLE: W028-24C two feet of co-axial cable attached, no second connector

	Ribbon Cable Connectors				Coaxial Cable Connectors†		
Type	Cable Attached	Type	No Cable	Type	Cable Attached	Type	No Cable
W021R	$13.00*	W021RU	$4.00	W021C	$31.00**	W021CU	$ 4.50
W022R	$13.50*	W022RU	$4.50	W022C	$33.00**	W022CU	$6.50
W028R	$13.00*	W028RU	$4.00	W028C	$31.00**	W028CU	$4.50
	*Ribbon Cable: Add $.60/ foot.				**Coaxial Cable: Add $1.50/foot.		

SOLENOID DRIVERS
·TYPES W040, W043

W
·SERIES

DIODE INPUTS

TRUTH TABLE

INPUTS		OUTPUTS
D (J)	E (K)	R (S)
Ov	Ov	OFF (NEG)
Ov	-3v	OFF (NEG)
-3v	Ov	OFF (NEG)
-3v	-3v	ON (-2V)

NODE TERMINAL
EXTERNAL NEGATIVE VOLTAGE

W043 ONLY
(SEE "GROUNDING")

W040, W043 SOLENOID DRIVER

These high current drivers can drive relays, solenoids, stepping motor windings, or other similar loads. The output levels are −2 volts and a more negative voltage determined by an external power supply. One terminal of the load device should be connected to the external power source, the other to the driver output. There are two drivers per module and both modules use the same pin connections.

Pin V of the driver module must be connected to the external supply so that the drivers will be protected from the back voltage generated by inductive loads. If the wire to the power supply is more than 3 feet long it may have to be by-passed at the module with an electrolytic capacitor to reduce the short over-shoot caused by the inductance of the wire. If pin V is connected to the supply through a resistor, the recovery time of inductive loads can be decreased at a sacrifice in maximum drive voltage capability. Maximum rated supply voltage (see below) less actual supply voltage should be divided by load current to find the maximum safe resistance. When both circuits on a module are used, the load current for the above calculation is the sum of the currents.

INPUTS: Standard DEC levels or equivalent. The maximum input load is 3 ma. per driver, shared by all grounded inputs. Additional diode inputs may be added by connecting diode networks such as R001 or R002 to the node terminal.

OUTPUTS: The table below shows maximum ratings for individual circuits. No more than two circuits should be paralleled to drive loads beyond the current capabilities of single circuits. For larger loads use the W042. When both circuits on a W043 are used with a duty cycle exceeding 35%, use the

current derating curve shown below.

GROUNDING: The W043 has three ground terminals C, T, U, which should be wired together externally to limit current through each connector pin to safe levels. (High current loads should be grounded at the W040 or W043 modules to avoid noise due to high pulse currents in ground conductors.)

MODULE	MAXIMUM VOLTAGE	MAXIMUM CURRENT	TYPICAL DELAY
W040	−70 V	0.6 amp.	5 μsec
W043	−35 V	2.0 amp.	10 μsec

W043 DERATING CURVE
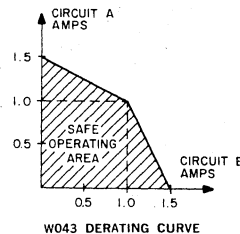
POWER: W040: + 10v (A)/ 0 MA, −15v (B)/24 MA. The external voltage supply must supply the output current of the two drivers (1.2 amp max.)

W043: +10v (a)/0.25 MA, −15v (B) /6 MA. The external voltage supply must supply the output current (2.0 amp max.)
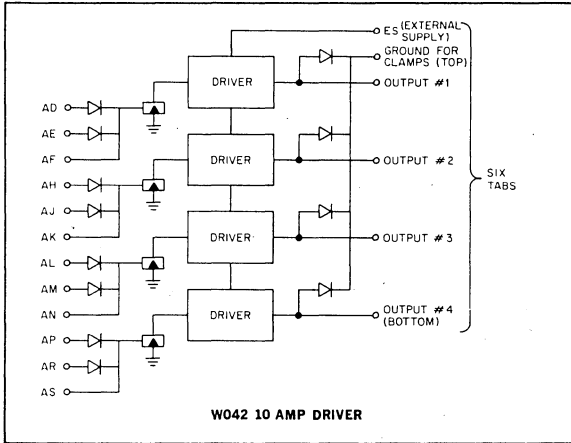
W040 — $36.00
W043 — $35.00

10 AMP DRIVER
TYPE W042
(DOUBLE-HEIGHT, DOUBLE-WIDTH MODULE)

W042 10 AMP DRIVER

This module has four germanium transistor drivers each capable of providing up to ten amperes of DC drive at ambients up to 40°C for heavy loads such as paper tape punches, card punches, hydraulic servo valves, or high-torque stepping motors like Responsyn (T.M. United Shoe) or Slo-Syn (T.M. Superior Electric). In 55°C ambients, up to 8 amps total current may be obtained. AMP "Faston" tabs at the handle end of the module provide high current connections for ground, ES , and the four outputs. Loads are to be connected between the outputs and external ground. Due to the fact that this module may dissipate as much as 20 watts when operated at rated output, special consideration should be given to an unobstructed flow of cooling air. It is recommended that no modules be mounted directly above any W042 operating at more than 4 amps average current. Typical delay: 20 microseconds. Load current decay time may be much longer, if its inductance is large.

INPUTS: Each input requires 2 ma at ground. Negative input brings corresponding output to ES . Input gates may be expanded with R001 or R002 diode modules, if no more than 6″ of wire is connected to each node. All connections are made to the A half (upper) of the module.

OUTPUTS: Total DC current from the W042 may be up to 10 amp, and may be distributed at will among the four outputs. Even higher currents may be obtained briefly by taking into account the 4 minute (approx.) time constant of the heat sink. For example, four 10 amp solenoids can be activated together, as long as they are on only a few seconds and at low duty factors. Outputs are not short circuit protected if shorted to ground. Shorts to output supply voltage are harmless. Clamp diodes are provided from each output to ground to damp transients when turning off inductive loads. Damping-diode ground and all ES power is connected only by tab terminals. Logic ground and +10v power use standard connector pins. Output circuit power supply must be grounded to digital system power externally. Power jumpers Type 914 may be used to make connections. Outputs may not be paralleled to increase short duty peak current, unless 0.1Ω current-sharing resistors are connected in series with each output.
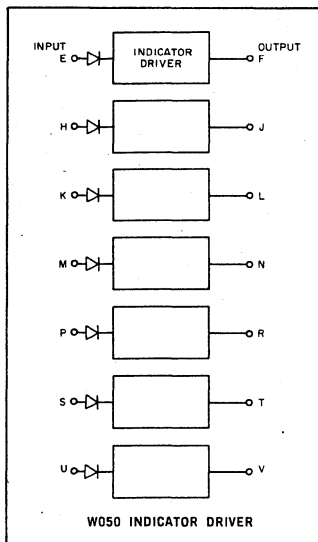
The negative supply voltage (ES) must be between --12 and --25 volts.

POWER: +10v(A)/180ma; ES/270ma plus output current.

W042 — $80.00

INPUT
E ○─▷├   INDICATOR DRIVER   ○ OUTPUT F

H ○─▷├   ○ J

K ○─▷├   ○ L

M ○─▷├   ○ N

P ○─▷├   ○ R

S ○─▷├   ○ T

U ○─▷├   ○ V

W050 INDICATOR DRIVER

The W050 contains seven transistor amplifiers that can drive miniature incandescent bulbs, such as those on an indicator panel. It is used to provide remote indicators for R- or B-Series flip-flops. If the input is at —3v, the output is at —1v.

INPUT: Standard levels of —3v and ground. Each input represents 1 ma of load at ground.

OUTPUT: The output is capable of supplying 30 ma

at —1v. The external load may be connected to any voltage between —1v. and —20 v. The output is capable of driving an indicator light, such as Drake 11-504, Dialco 39-28-375, or Eldema CF2-WT-1762, returned to —15 v.
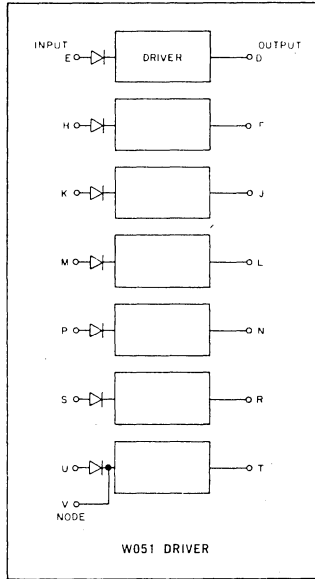
POWER: +10 v(A)/1.1 ma; —15 v(B)/7 ma.

NOTE: An additional 210 ma is drawn from the indicator supply when all remote lights are on. This power is not drawn from the module.

W050 — $13.00

100 MA INDICATOR AND RELAY DRIVER
TYPE W051

INPUT   OUTPUT
E ○—▷|— DRIVER —○ D

H ○—▷|—   —○ F

K ○—▷|—   —○ J

M ○—▷|—   —○ L

P ○—▷|—   —○ N

S ○—▷|—   —○ R

U ○—▷|—   —○ T

V ○—
NODE

W051 DRIVER

The W051 contains seven inverter amplifiers suitable for driving indicators, relays, and other medium power devices. The amplifiers can supply up to 100 ma at ground, and each output is diode clamped to 15v to prevent overvoltage when the current is interrupted in an inductive load. If the input is at —3v, the output is at ground.

INPUT: Diode — Standard levels of 3v and ground. The input load is 3 ma at ground. **Node** — Other inputs may be connected here through diodes such as those in the R002. The 3-ma load is shared among the grounded inputs.

OUTPUT: The output is capable of supplying 100 ma at ground. The external load may be connected to any voltage between 0 and 15v. The negative output is diode clamped to prevent it from going more negative than 15v. Typical delay for circuit alone: 1 microsecond. Decay time of current in inductive loads may be much longer.
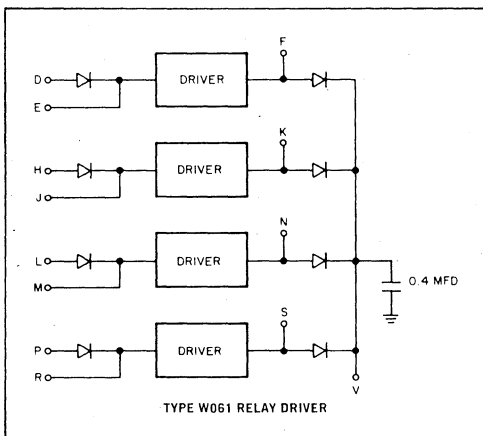
POWER: +10 v(A)/3 ma; —15 v(B)/23 ma.

NOTE: An additional 700 ma will be drawn from 15v when all circuits are on. This power is not drawn from the module.

W051 — $22.00

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RELAY DRIVER
TYPE W061

TYPE W061 RELAY DRIVER

The W061 Relay Driver has four all-silicon 250 ma drivers with gateable inputs; it can drive relays and solenoids with positive voltage supplies up to 55v.

INPUTS: 2 ma at ground, no load at 3v. Use diodes for ungated input. Multiple-input AND gate may be obtained by connecting R001 or R002 diodes to node inputs.

OUTPUTS: The loads are to be connected between the outputs and an external positive supply. Each output can supply a quarter-amp load at ground when the input(s) is (are) negative. Pin V must be connected to the positive voltage supply so inductive loads will not cause output transistor breakdown. Supply voltage should be between 2 and 55v positive. Typical delay for circuit alone: 1 μsec. Decay time of current in inductive loads may be much longer.
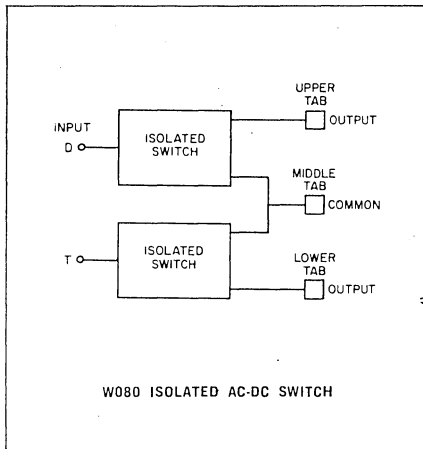
POWER: $+ 10v(A)/70$ ma; $-15v/8$ ma.

OTHER POWER: Inductive loads cause clamp currents at pin V tending to drive supply voltage more positive when drivers are turned off.

W061 — $35.00

ISOLATED AC-DC SWITCH
TYPE W080

W
SERIES

W080 ISOLATED AC-DC SWITCH

This module contains two photon-coupled transistor switches with bridge rectifiers. Both turnon and turnoff are slow enough to minimize output noise. Output tabs are at handle end of module for maximum isolation. Drives relays, solenoids, panel lamps, small motors directly. Larger AC loads can be driven by the use of SCR or Triac* buffers. For example, one SC45B Triac with a W080 circuit tied from gate to anode 2 and a 100Ω resistor from gate to anode 1 can switch AC loads up to one kilowatt.

INPUT: Each input is a 30 ma load returned to 10v. A W061 driver is suitable. Switching rate must not exceed one hertz per second. Grounding an input turns on the switch, and an open circuit at the input turns off the switch.

OUTPUT: Each circuit can switch up to ¼ ampere from supplies up to 135 volts DC or AC (RMS) into resistive or inductive loads, or 30 va maximum at 120 volts. Can drive up to 40 va intermittently; up to 5 seconds on 50% duty factor. Derate by half for driving incandescent lamps. Typical "on" voltage drop: 8 volts. Typical switching time: 1/10 second.
*G.E. trademark

Not designed for series or parallel operation.

WIRING: Three AMP "Faston" tabs replace module handle. Type 914 Power Jumpers can be used to connect these to a nearby terminal block, etc. Use caution on high voltage.

NOISE: W080 is designed to generate little or no switching noise. However, power lines often carry noise from distant sources. Some types of loads generate noise, such as bush-type motors and power relays. Even SCR and Triac circuits generate fast transients on each turnon cycle. For these reasons, it is important to locate W080 modules and their output leads away from logic and logic wiring. If a W080 module must be used close to a logic module, put a W992 or W993 copper clad board with pins A and B cut away between them to form an electro-static shield. In some cases line filters may also be necessary.
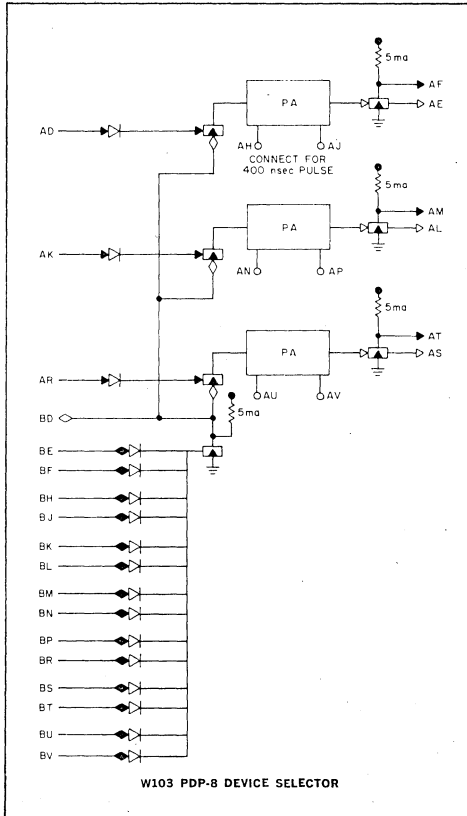
POWER: 10v(A)/60 ma; 15v(B)/0.

W103 PDP-8 DEVICE SELECTOR

This module is used to decode the six device selector bits transmitted in complement pairs on the PDP-8 or PDP-8/S I/O bus, and it provides standard pulses to the selected device. The device code is selected by cutting one diode of each pair, BE or BF, etc., off the board. Device coding can also be accomplished by selective wiring of the bus inputs to the diode pairs.

INPUTS: Diodes — Standard levels of −3v and ground. Input load is 1 ma shared among the inputs that are at ground. **Pulse Input** — Standard 100 nsec negative pulse or any pulse at least 100 nsec wide with an amplitude of 2.5 volts.

OUTPUTS: With terminals AH and AJ or the corresponding terminals on other sections connected together, the output is a standard 400 nsec pulse. With these terminals open the output is a standard 100 nsec pulse. Both positive (−3v to ground) and negative pulses are available. Each positive output can drive 65 ma of external load at ground and each negative output 15 ma.
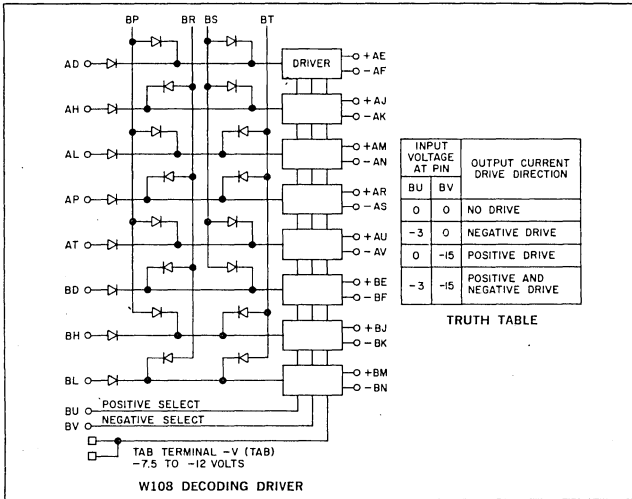
POWER: +10 v(A)/6.4 ma; −15 v/57 ma.

W103 — $52.00

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DECODING DRIVER
TYPE W108
(DOUBLE HEIGHT)

INPUT VOLTAGE AT PIN		OUTPUT CURRENT DRIVE DIRECTION
BU	BV	
0	0	NO DRIVE
−3	0	NEGATIVE DRIVE
0	−15	POSITIVE DRIVE
−3	−15	POSITIVE AND NEGATIVE DRIVE

TRUTH TABLE

W108 DECODING DRIVER

This driver provides up to 300 ma bipolar drive currents for use in memory systems including core memories, such as the H201, and magnetic tape systems. There are eight drivers on a module, each of which can be selected either by one of eight address lines or by using the built-in binary-to-octal decoding matrix. The drive current direction is selected by one of two input select lines and will be the same for all drivers on a module. Drive current can be varied from 160 ma to 300 ma by adjusting the external negative voltage reference connected to a tab terminal on the module handle.

INPUTS: Address selection diode inputs have a 2 ma at ground load shared between all inputs used on each driver. Positive output drive can be selected by a −3 volt signal at pin BU. When pin BU is brought to ground, the input driving source must supply 35 ma per addressed driver. The negative output drive current is selected by a −15 volt signal at Pin BV. This input requires a 25 ma drive at ground independent of driver addressing.

For a complete description of drive current direction selection see the truth table.

The negative voltage reference applied to the tab terminal input may have a voltage range of −7.5 to −15 volts with the current amplitude approximately

determined by the formula

$$I \text{ (ma)} = \frac{\text{Tab Voltage}}{0.048 + \text{External Series Resistance in Kilohms}}$$

This external source must be able to sink the maximum negative drive currents used in the W108. For tab voltages more negative than −12 volts the duty cycle of each negative driver should be such that the average drive current per driver is less than 200 ma. Momentary shorts to the negative drive outputs will cause no module damage.

OUTPUTS: All negative current outputs sink current as controlled by the tab voltage. Typical turn-on and turn-off times for the negative current are, respectively, 100 nsec and 1.5 μsec. The positive current driver output must be used in series with a negative current driver, the latter then controls the positive drive current. Each positive output is diode-protected to −15v against inductive backswing.

POWER: −15(B)/16 ma plus 35 ma per selected driver
−V(TAB)/maximum of 250 ma per negative current driver used.

HIGH IMPEDANCE FOLLOWER
TYPE W500

W500 HIGH IMPEDANCE FOLLOWER
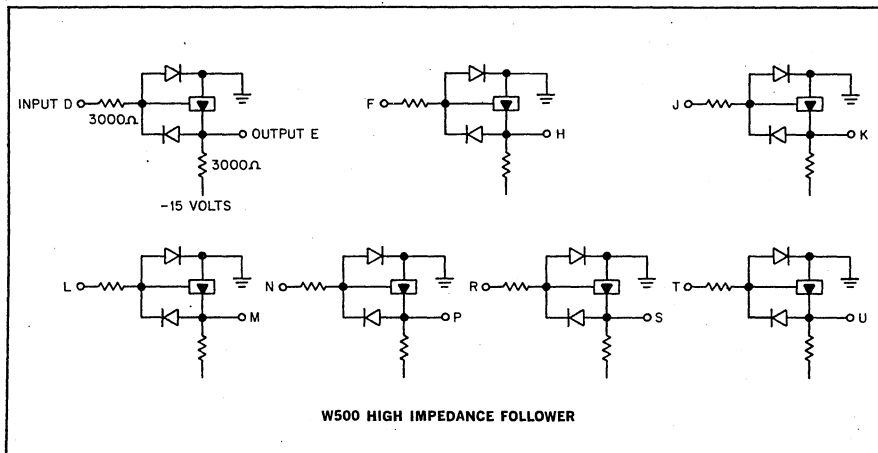
High impedance signal sources such as photocells and low-current instrumentation amplifiers can drive Schmitt Trigger W501 or logic gates through a W500 circuit. The module contains 7 fault-protected circuits, each comprising two cascaded emitter-follower amplifiers. Input voltage excursions up to ±30v or short-circuits from output to ground are harmless. Outputs can go as negative as −15v with very light loading, but will not exceed −10v when driving a W501 input.

INPUTS: Excursions Between —0 and —3v: Input currents of 100 μa or less (typically 50) flow toward the driving source, tending to bring it more positive. Low frequency equivalent input resistance exceeds 10KΩ even while the output voltage is passing through the input threshold region of a Schmitt circuit or diode gate. Voltage offset between input and output: less than ±1/3v.
Larger Excursions: A diode shorts the active components of the follower circuit if the input voltage goes more positive than ground or more negative

than −15v, and the input equivalent circuit changes to 3000Ω returned to the limiting voltage. If the output is connected to a clamped load for driving grounded loads such as B-series inverters, the limiting negative voltage changes from −15 to −3v.

OUTPUTS: Excursions Between 0 and —3v: Each circuit can drive up to 15 ma at ground. Driving capability at −3v is 3 ma more than that of any clamped load attached. If the output is brought to ground by a paralleled transistor collector, not only the internal 5 ma load and the external load must be driven, but also the current demanded by the input 3000Ω resistance returned to the negative input voltage present. 10 mc emitters may not be driven. **Larger Excursions:** If no clamped load is attached, each output will follow its input as far negative as its internal 3000Ω resistor to −15 v will drive the load. Output voltage cannot go more positive than ground.

POWER: +10v(A)/18 ma; −15v/35 ma.

W501 SCHMITT TRIGGER
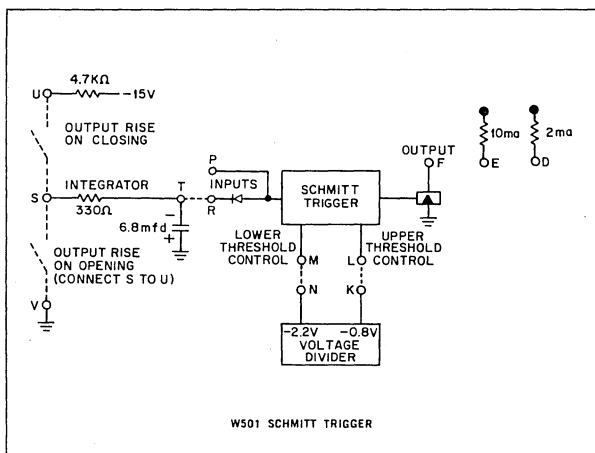
The W501 contains a Schmitt trigger circuit which produces standard levels as a result of some outside activity such as the closure of a switch or relay. A ground level input produces a −3v level output, and a negative level input produces a ground level output. Nominal switching thresholds of −2.2v and −0.8v are obtained by connecting terminal L to terminal K and terminal M to terminal N. The switching thresholds can be varied over the range of 0 to −2.5v by applying external voltage levels to terminals M and L. Terminal M controls the lower level threshold, and terminal L controls the upper level threshold. The module also contains an integrating circuit to filter contact bounce when a switch or relay is used to generate the levels.

INPUTS: Diode — Any signal at pin R between ±10v will not cause damage to the circuit. The input impedance is 7500 ohms to +10v when the input is more negative than the lower threshold, and is an open circuit when the input is more positive than the upper threshold. The output will switch from −3v to ground if the input voltage goes more negative than the lower threshold after having been more positive than the upper threshold. The output switches from ground to −3v if the input voltage goes more positive than the upper threshold after having been more negative than the lower threshold. Upper and lower thresholds must be at least ½v apart. The 2 ma clamped load at pin D cannot be used to bring this

input to −3v since it sinks insufficient current.

Direct: — Pin P provides a bypass of the diode connected at pin R. This node input can be used with R001 diodes to form a NANDed input to the W501 as shown in Fig. 1 below. In addition, this input can be used to obtain an integrated input when many contacts or switches are connected as shown in Fig. 2 below. This latter scheme gives an output rise when contacts close.

Integrating — The input to the integrating circuit is a switch or relay contact. To obtain output rise when contacts close connect contacts between pin S and U and connect pins R and T. To obtain output rise when contacts open, connect contacts between pin S and ground, connect pin U to pin S, and connect pin R to pin T.

OUTPUT: Direct — The output is ground for negative inputs and — 3v for ground inputs. When attached to the 2-ma clamped load, the output can drive 18 ma of external load at ground. When attached to the 10-ma clamped load, the output can drive 10 ma at ground, and 7 ma at —3v. Output rise time is 50 nsec or less. Typical delays for output rise and fall are 100 nsec and 200 nsec, respectively. **Integrating** — Using threshold voltages provided, integration time for output rise is approximately 8 msec total closed time for path S-to-U, or 8 msec continuous open time for path S-to-ground.
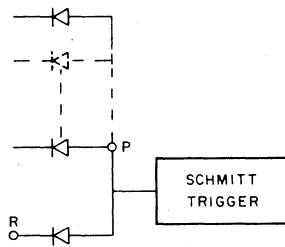
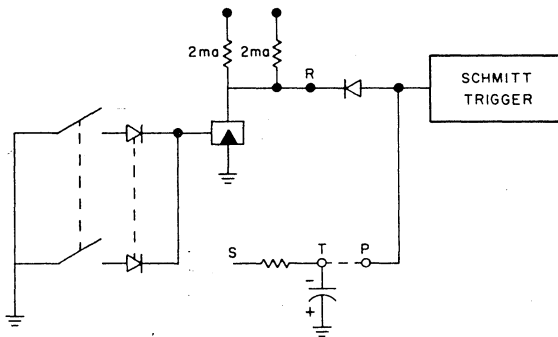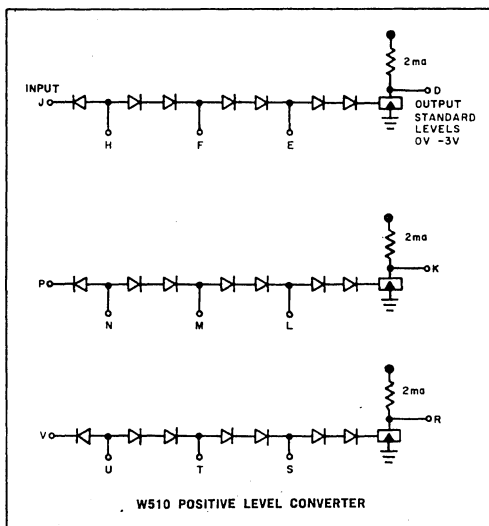**POWER:** +10 v(A)/12 ma; — 15 v(B)/27 ma.

Figure 1. NANDed Input

Figure 2. Integrated Input

POSITIVE INPUT CONVERTER
TYPE W510

W510 POSITIVE LEVEL CONVERTER

The Type W510 Positive Level Converter contains three circuits that convert positive levels to DEC standard levels of ground and −3v. Each circuit consists of a grounded-emitter inverter with a diode string between its input and the base of the inverter. By shorting out sections of the diode string, the switching threshold may be varied to either +2v, +1v, or 0v (see the following table). When the input is more positive than the switching threshold by 1v, the inverter is cut off and the output is at −3v. When the input is more negative than the switching threshold by 1v, the inverter is saturated and the output is at ground.

Threshold	Connections	Output = −3 v	Output = 0 v
+2v	none	Input ≥ +3.0 v	Input ≤ +1.0 v
+1v	H.& F, N & M, U & T	Input ≥ +2.0 v	Input ≤ 0.0 v
0v	H & E, N & L, U & S	Input ≥ +1.0 v	Input ≤ −1.0 v

In jumpering pins together to obtain the desired switching point, it is very desirable to use the shortest possible wire. Under no condition may anything else be tied to these pins.

Maximum frequency is 2 mc. Maximum TTT for output fall is 200 nsec. Maximum TTT for output rise is 100 nsec.

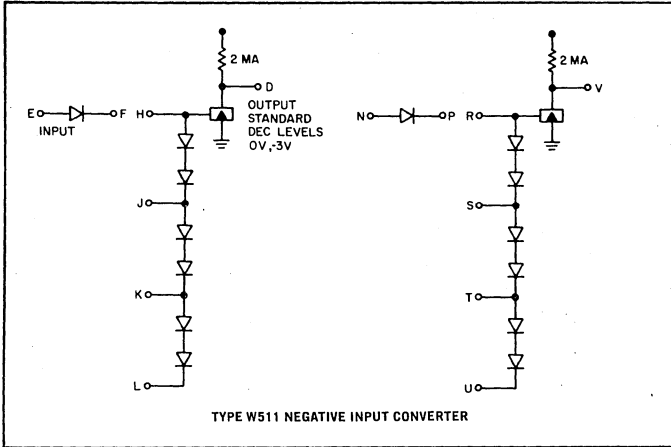INPUTS: Voltage levels must not exceed +25v or go below −15v. For inputs more negative than the switching threshold by 1v or more, the input load is equivalent to 3900 ohms returned to +10v. For inputs which are more positive than the switching threshold by +1.5v the input leakage is 100 μa or less.

OUTPUTS: The output is an inverter with a 2-ma clamped load. It can drive 18 ma at ground.

POWER: + 10 v(A)/8.0 ma; −15 v(B)/17 ma.

W510 — $17.00

TYPE W511 NEGATIVE INPUT CONVERTER

The Type W511 Negative Level Converter contains two circuits that convert negative levels to DEC standard levels of ground and −3v. Each circuit consists of a grounded emitter inverter with a string of bias diodes between its base and the input pins. A separate input diode is also provided. By connecting the input diode to various points on the diode string, the switching threshold can be set at 0v, −1v, −2v, or −3v (see the table below). When the input is more positive than the switching threshold by 1v, the inverter is cut off and the output is at −3v. When the input is more negative than the switching threshold by 1v, the inverter is saturated and the output is at ground.

Threshold	Connections	Output = − 3v	Output = 0v
0v	F & H, P & R	Input $\geq$ +1.0v	Input $\leq$ −1.0v
−1v	F & J, P & S	Input $\geq$ 0.0v	Input $\leq$ −2.0v
−2v	F & K, P & T	Input $\geq$ −1.0v	Input $\leq$ −3.0v
−3v	F & L, P & U	Input $\geq$ −2.0v	Input $\leq$ −4.0v

In connecting input diodes to the bias string, use short, direct wire. Under no conditions should anything but the input diode be connected to a bias string pin. Inputs must be connected only to pins E and N.

INPUTS: Voltage levels must not exceed +25v or go below −50v. Input current required is approximately 1 ma when the input is slightly more positive than the threshold, rising to a maximum of 4 ma when the input is at +25v. Input leakage is 100 μa or less when the input is more negative than the threshold.

OUTPUTS: The output is an inverter with a 2 ma clamped load. It can drive 18 ma at ground. Output rise and fall TTT are less than respectively 95 and 200 nsec.

POWER: +10v(A)/3 ma; −15v(B)/24 ma.

W511 — $17.00
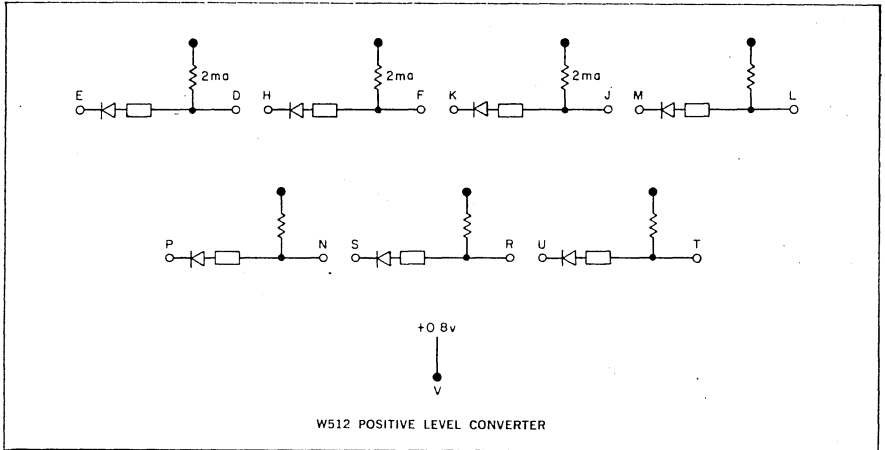
192

W512 POSITIVE LEVEL CONVERTER

Positive logic systems, such as those using monolithic integrated circuits, can use the W512 to make available standard accessory modules in the W and A series.

Input threshold voltage to each converter is normally 1.6 volts for compatibility with DTL and TTL levels. This theshold can be set at 0.8 volts by grounding pin V for RTL level conversion.

**INPUTS:** Input current 1 ma or less for input voltages between 0.3 volts and the threshold, 100 μa for inputs above the threshold. Input voltages must not exceed 6.0 volts with pin V open, or 5.3 volts with pin V grounded. Inputs must exceed nominal thresholds by at least 0.4 volts for full switching with minimum noise rejection.

OUTPUTS: Each output can supply up to 8 ma at ground. Grounded inputs provide grounded outputs and positive inputs provide negative outputs. Output rise and fall TTT are less than respectively 70 and 200 nsec.

POWER: 10v (A)/104 ma; 15v (B)/30 ma.

W512 — $25.00

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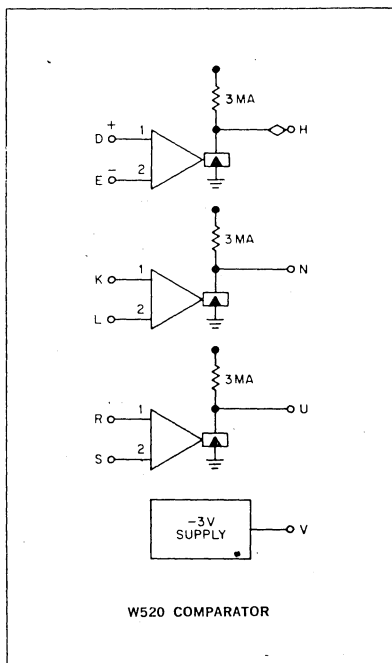
W520 COMPARATOR

This module is useful as an inexpensive comparator for A/D work, or as a general-purpose input level converter. The W520 contains three four-transistor difference amplifiers which give DEC Standard levels at the output. The state of the output is determined by the relative polarity of the input voltages.

Max delay for output fall:
75 ns, 50% to 50%
Max delay for output rise:
150 ns, 50% to 50%
Typical rise time 10%
to 90%: 25 ns

for 200 mv square wave about a fixed reference voltage

The W520 is tested for 100 mv differences minimum. It is not a replacement for the more precise A502.

INPUTS: High impedance inputs to the amplifier are provided. The more positive input appears as 100 K ohms to 15v; the more negative input supplies a maximum of 0.5 μa from 10v at room temperature. For proper operation of the module, input 2 voltage must remain between 5v and −10v, and input 1 between 10v and 15v. Input excursions beyond 10v or 15v will cause damage.

**OUTPUTS:** Standard DEC levels of 0 and −3v; capable of driving 17 ma at ground. The internal load is 3 ma. If input 1 is more positive than input 2, the output will be zero. The −3v output should be lightly loaded (less than 1 ma current) by any external path to ground unless an external resistor is added between pin V and −15 volts. Up to 50 ma may be drawn by external path from pin V to −15v.

POWER: 10v(A)/37 ma; 15v/32 ma.
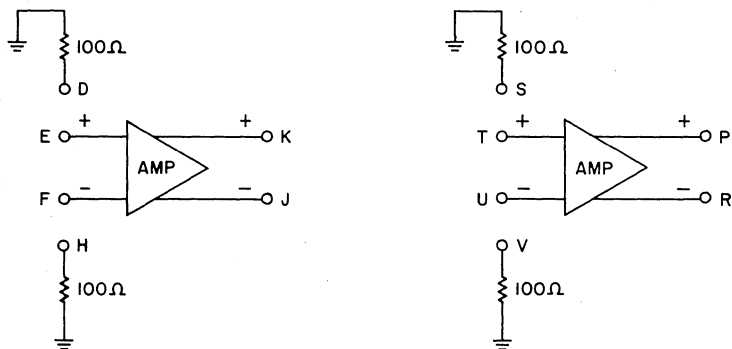
W532 DUAL AMPLIFIERS

The W532 contains two AC-coupled differential amplifiers for use with many magnetic sense systems, including the H201 core memory. These amplifiers provide the high differential gain and common mode noise rejection necessary to amplify information signals in a system using a single sense line per plane for a memory or per channel for a tape system.

INPUTS: Pins E, F, T, U require an input current of 0.15 ma or less and must be terminated to ground through the internal 100Ω resistor or an external resistor or transformer of nominal impedance 1000Ω or less. These terminations bias the inputs at ground. In the absence of common mode signals, the difference signals must not exceed 80 mv for linear amplification. For positive common mode signals the maximum differential input must be reduced by 5mv per half volt of common mode input. Negative common mode voltages allow an increase in maximum differential input by the same ratio. See Table 1 below for additional specifications.

OUTPUTS: The output voltage with no input signal is nominally at −11.5 volts so that a W533 can be used

with a W532 to detect differential signals above a preset threshold. Output impedance is 1000Ω. Due to power supply ripple it is recommended that the output be AC-coupled to other modules. See Table 1 for additional specifications.

TABLE 1. MODULE SPECIFICATIONS

Specifications	Minimum	Maximum
Output Voltage (no signal)	−11.0	−12.0
Common Mode Input Voltage	−5	+5
Common Mode Voltage Gain	—	0.37
Difference Mode Voltage Gain	88	96
Output Rise Time Square Wave Input	—	250 ns
Output Fall Time Square Wave Input	—	400 ns
3db Bandpass	1 kHz	0.8 MHz

POWER: +10(A)/40 ma, −15(B)/40 ma

W532 — $30.00

<table>
<tr><td>

DUAL RECTIFYING SLICER
TYPE W533

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W
SERIES

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W533 DUAL SLICER

W533 AS USED WITH A W532
IN A H201 MEMORY
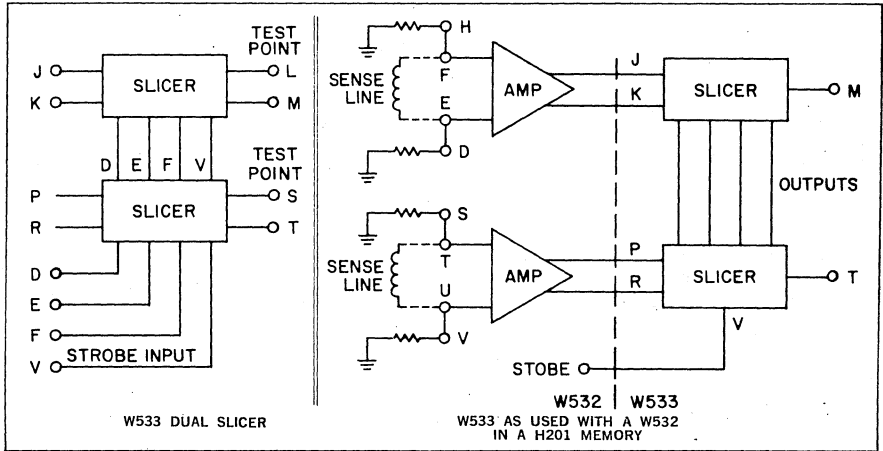
This module is used to detect amplified magnetic system sense signals from a W532 (see above diagram) and convert them to positive DEC pulses. Detection of signals as narrow as 100 nsec is possible over a wide range of detection thresholds. There are two slicer circuits on each W533. Two input terminals per circuit permit rectification so that bipolar difference signals can be sliced and standardized.

INPUTS: AC-coupled inputs J, K, P, and R have an input impedance of 10kΩ and a 1 μsec coupling network time constant. When any negative going input exceeds its threshold and a -3 volt to ground strobe pulse is applied at pin V, the output M or T corresponding to the input used will rise to ground. Provided that the strobe pulse is narrower than the time during which the detection threshold is exceeded, the output pulse will be of the same width as the strobe pulse. Input load on pin V is 1 ma to ground. The threshold level is preset at -1 volt, but can be varied by paralleling resistors as shown below. The maximum threshold is -1.5 volts. Pins L and S are test points which will go negative when the

threshold is exceeded. No connections should be made to these points.

THRESHOLD ADJUSTMENT
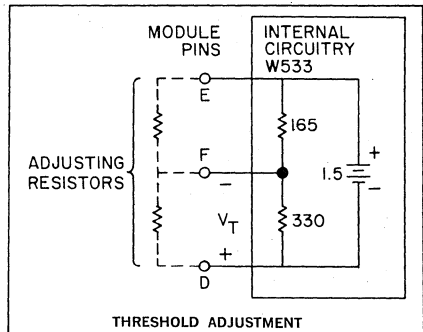
OUTPUTS: Identical to those of a R111 or R123. Drive capability is 20 ma to ground and outputs may be paralleled. Delay from input to output is 50 nsec, from strobe to output 70 nsec.
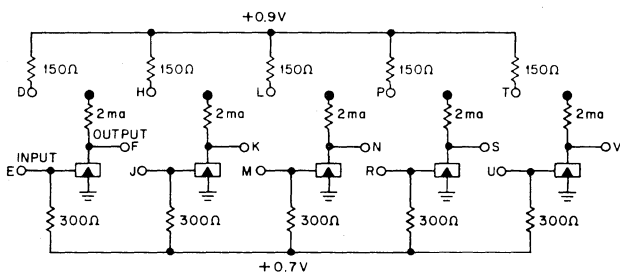
POWER: $+10$(A)/4 0ma., -15(B)/28 ma.

W533 — $30.00

IBM N LINE TO DEC CONVERTER
TYPE W590

W590 IBM N LINE TO DEC CONVERTER

Each of the 5 inverting amplifiers on this module provides input characteristics compatible with three types of IBM N Lines. Input impedance is nominally 300 ohms, with 100 ohm impedance available by connecting 150 ohm shunts provided. Each circuit has a switching threshold near zero volts, with input biasing included to maintain a definite output state when the input is open-circuited.

Unshunted inputs will tolerate input excursions up to +4v and —6v, so these circuits may also be used to convert IBM T, D, or Q lines if the IBM circuits involved can safely drive the W590 input loads.

INPUTS:

IBM Line	Floating Input	Lower Level	Input Impedance
N Transmission	+0.8v	(@ —23 ma) —1.5v	(shunted) 100 Ω
C Line	+0.7v	(@ —12 ma) —2.6v	300 Ω
N Logic	+0.7v	(@ —6 ma) —0.8v	300 Ω

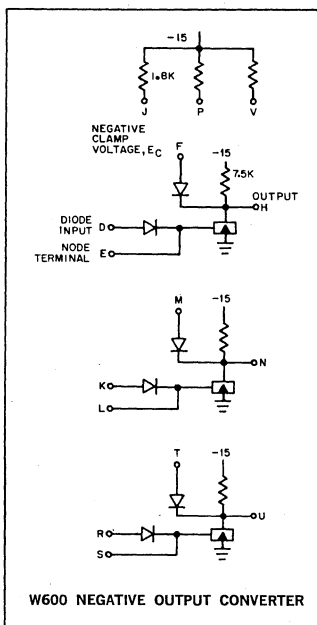Maximum input voltages: Unshunted (300 Ω) inputs: +4v, —6v; Shunted (100 Ω) inputs: ±4v.

OUTPUTS: 18 ma at ground. 1 ma at —3v.

POWER: +10v(A)/40 ma; —15v(B)/23 ma.

W600 NEGATIVE OUTPUT CONVERTER

The W600 contains three inverting amplifiers that convert standard levels to outputs of ground and an externally supplied negative voltage. The external clamp voltage is applied to terminal F (M, T) and must be between -1 and -15 v. Additional inputs may be added by tying diode networks, such as those contained on the R001 or R002, to the node terminal. These inputs form a NOR gate for ground levels and a NAND gate for negative levels. That is, if any input diode is at ground, the output is at the external clamp voltage; and if all inputs are at -3 v, the output is at ground. Output rise and fall TTT are less than respectively 100 and 200 nsec.

INPUT: Standard levels. The input load is 1 ma shared by all grounded inputs, including those attached through diode networks to the node terminal.

CLAMP VOLTAGE: The external voltage E_c applied to terminals F, M, and T may be any voltage between -1 and -15 v. The load is 2500 ohms to -15 v without the extra load resistors or 500 ohms to -15 with the extra loads.

OUTPUT: The output voltage levels are ground and the negative external clamp voltage, V_c. Driving depends on the external clamp voltage and is given in the following table.

	Maximum Output Current	
	At Ground	At Clamp Voltage
Without additional resistor	18 ma	$\dfrac{15 + E_c}{7.5}$ ma
With additional resistor (H, N, or U connected to J, P, or V)	10 ma	$\dfrac{15 + E_c}{1.5}$ ma

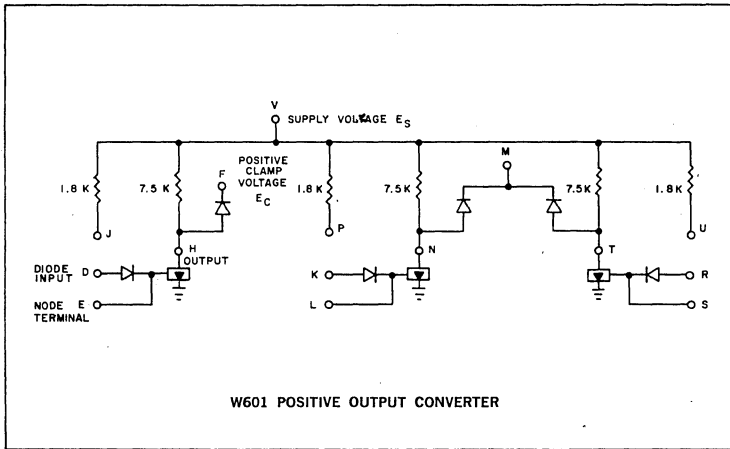E_c = external clamp voltage, -1 to -15 v. It is therefore a negative number in the above equations.

POWER: $+10$ v(A)/0.3 ma; -15 v(B)/33 ma.

W600 — $12.00

W601 POSITIVE OUTPUT CONVERTER

The W601 contains three amplifiers for converting DEC standard levels to outputs of ground and an externally supplied clamp voltage level, E_C. This external clamp voltage is applied to terminal F (M) and must be between +1 and +20v. Additional inputs can be added by tying diode networks, such as the R001 or the R002, to the node terminal. These inputs form a NOR gate for ground levels and a NAND gate for negative input levels. That is, if any input diode is at ground, the output will be at ground, and if all inputs are at −3v, the output will be at E_C. A positive supply voltage E_S greater than E_C should be tied to terminal V. If E_C is less than +10v, the +10v supply on terminal A may be used at the supply voltage on terminal V. Output rise and fall TTT are less than respectively 150 and 100 nsec.

INPUT: Standard levels. The input load for each amplifier is 2 ma shared by all grounded inputs including those attached through diode networks to the node terminal.

EXTERNAL VOLTAGE: Terminal F (M) — The external clamp voltage E_c applied to terminal F (M) can be between +1 and +20v. The load is 500 ohms to $+E_S$ (if the 1800-ohm resistors are used)

or 2500 ohms to $+E_S$ (if the 1800-ohm resistors are not used). **Terminal V** — The supply voltage E_S on terminal V should be greater than E_c but not greater than +20v. The load is 500 ohms (if the 1800-ohm resistors are used) or 2500 ohms (if the 1800-ohm resistors are not used) to ground.

OUTPUT: Output levels are ground and a positive external clamp voltage, E_c. Output drive depends on the two external voltages. They are given in the table below.

EXTERNAL DRIVING CAPABILITIES OF W601

	OUTPUT CURRENT	
	AT GROUND	AT CLAMP VOLTAGE
Without additional resistor	$\left(20 - \dfrac{E_s}{7.5}\right)$ma	$\left(\dfrac{E_s - E_c}{7.5}\right)$ma
With additional resistor, i.e. H (N, T) connected to J, P, or U.	$\left(20 - \dfrac{E_s}{1.5}\right)$ma	$\left(\dfrac{E_s - E_c}{1.5}\right)$ma

POWER: +10 v(A)/3 ma; −15 v(B)/6 ma.

W602 BIPOLAR OUTPUT CONVERTER
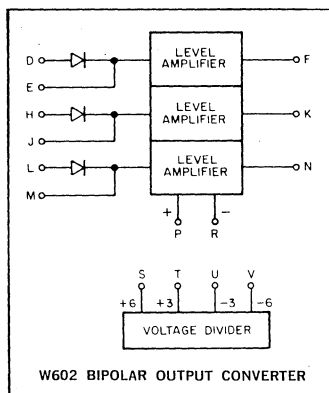
For driving EIA standard communication lines and other applications demanding levels both positive and negative with respect to ground, the W602 provides up to · 15 ma at up to · 6v. There are three inverting amplifiers on the module. To control noise on long transmission lines the output rise and fall times are intentionally slowed to roughly 50 nsec/v, and at low repetition rates capacitance may be connected externally from outputs to ground to further increase rise and fall times. Output upper levels can be set at · 6v, · 3v, or 0v, and lower levels can be set at 6v, 3v, or 0v using clamp voltage supplies provided.

INPUTS: Signals — Diode inputs require 1 ma drive at ground. Input gating can be achieved b· ¬onnecting R001 or R002 diodes at node inputs. Clamp Voltages — Voltages from 0v to ¦ 6v may be applied to pin P to establish the upper output level for all

three amplifiers. Each circuit whose output is high supplies 4 ma tending to make pin P more positive. Voltages from 0v to 6v may be applied to pin R to establish the lower output level for all three amplifiers. Each circuit whose output is low supplies 2 ma tending to make pin R more negative.

OUTPUTS: Signals — Maximum output current from each circuit is · 15 ma. Outputs are high when inputs are low, and vice versa. Momentary shorts from outputs to ground will not cause damage. If switching speed must be reduced to reduce noise generation, capacitance to ground sufficient to extend transient times to 50% duty factor may be added from outputs to ground. Clamp Voltages — Voltage supplies are adequate for use with the three circuits on the module.
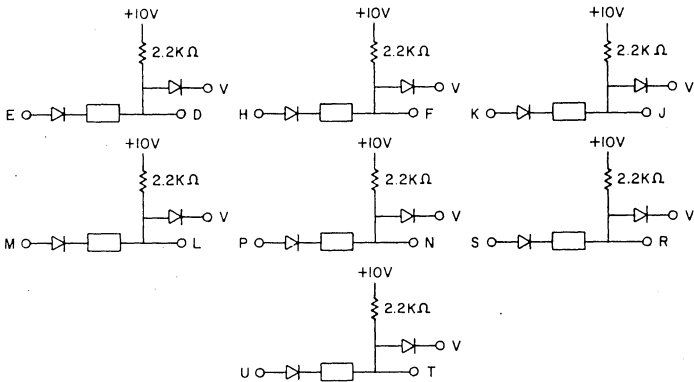
POWER: ¦ 10v(A)/32 ma; 15v/31 ma .

POSITIVE LEVEL AMPLIFIER
TYPE W603

W
SERIES

W603 POSITIVE LEVEL AMPLIFIER

Positive logic systems such as those using RTL, DTL, or TTL monolithic integrated circuits can be driven from FLIP CHIP systems through the W603. Clamped load resistors at the output of each circuit permit output levels to be adjusted to the type of circuit being driven. Normally the clamp voltage at pin V is provided by the logic supply voltage used with the monolithic circuits. This clamp voltage is common to all seven converters on the module.

INPUTS: 1 ma at ground.

OUTPUTS: Each output can supply up to 5 ma at ground. Drive capability at the positive output voltage is provided by internal 2200-ohm resistors returned to $\pm$ 10 volts. The upper positive level will be no more than 0.8 volts above the clamp voltage.

Grounded inputs provide grounded outputs; negative inputs produce positive outputs. Output rise and fall TTT are less than respectively 100 and 150 nsec.
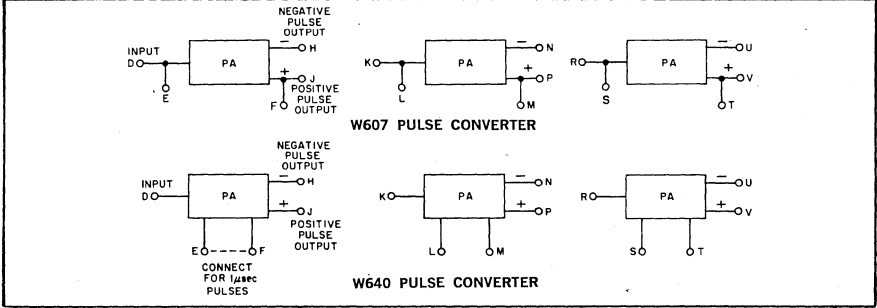
POWER: +10(A)/35 ma, —15(B)/7 ma.

W603 — $23.00

W607 PULSE CONVERTER

W640 PULSE CONVERTER

These pulse converters were designed primarily to facilitate the use of Flip Chip modules in conjunction with Digital Laboratory and System Modules. In addition, the W607 can be useful in setting or clearing B series unbuffered flip-flops via inverters such as B104 or gates such as B113.

Outputs from these pulse converters are taken from floating pulse-transformer windings. In addition to allowing data transmission independent of ground system integrity, this feature permits two or three outputs to be series-connected for larger pulse amplitudes when inputs are driven simultaneously.

For purposes other than driving Digital Laboratory and System Modules, it may be important to consider the effect of pulse transformer backswing at the end of each pulse. When the load is light, this transformer recovery spike approaches the amplitude of the pulse itself.

INPUT: Standard Digital positive pulses or a level change from −3 volts to ground. See table below

for other characteristics. Unless wider than standard output pulses are acceptable, W607 inputs must not be paralleled with clamped loads, such as those internally tied to R107 outputs. W640 output pulse-width is not affected by input loads. No connections should be made to W640 pins E or F (L or M, S or T) other than shorting them together to obtain 1 μsec output pulses.

OUTPUT: A standard 2.5v pulse. To obtain a negative output, ground the positive output terminal. To obtain a positive output, ground the negative output terminal. Each output can drive up to 10 ma of load, in addition to a terminating resistor. A terminating resistor must be used. Its value should be about 47Ω for lightest loads, and about 150Ω for heaviest loads. Reactances in loads and leads cause pulses to grow in transmission, and optimum values must be determined empirically. See table for other characteristics.

POWER: W607. 10v(A)/0 ma; −15v(B)/35 ma.
W640: +10v(A)/0 ma; −15v(B)/25 ma.

Module	Input				Output			Laboratory Series	System Series
	Load	Ground	Rise Times	−3 volts	Delay	Width	Max. Freq.		
W607	10 ma	≅40 nsec	100 nsec	≅330 nsec	20 nsec	70 nsec	2.5 mc	100	1000
W640	2 ma	≅70 nsec	200 nsec	≅1 μsec	10 nsec	400 nsec	500 kc	3000	4000
W640 E to F, etc.	2 ma	≅70 nsec	200 nsec	≅3 μsec	40 nsec	1 μsec	200 kc	3000	4000

W607 — $42.00
W640 — $42.00

DEC TO IBM N LINE CONVERTER
TYPE W690

W690 DEC TO IBM N LINE CONVERTER
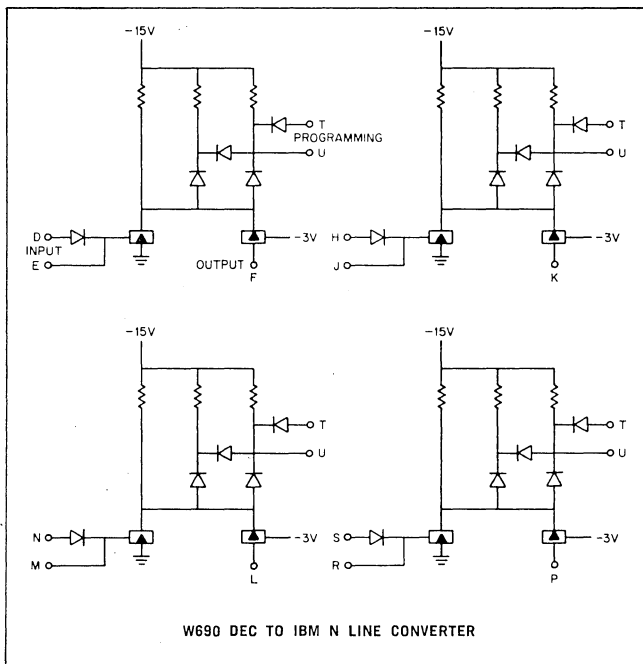
Each of the four inverting drivers on this module provides outputs compatible with the three types of IBM N lines, depending upon what output currents are programmed by grounds or open circuits at pins T and U. Node points are provided at each input. Maximum delay: 100 nanoseconds driving N transmission lines.

Outputs will drive loads returned to voltages as high as -12, so this module will also drive T, D, or Q lines with suitable biasing networks added.

INPUTS: 2 ma at ground, 0 ma at -3v in. Node input provided for connection to R001 or R002 diode gate expander cards.

**OUTPUTS:** Outputs are open for negative inputs. Table below shows nominal output currents for grounded input. Maximum negative output excursions: -3.5v (clamped). Shorting outputs to ground will not cause damage.

POWER: +10v(A)/0 ma; -15v(B)/150 ma.

IBM LINE	NEGATIVE OUTPUT	OUTPUT PROGRAMMING
N Transmission	26 ma	T Open U Open
————	20 ma	T Ground U Open
C Line	14 ma.	T Open U Ground
N Logic	8 ma	T Ground U Ground

W690 — $36.00

SWITCH FILTER
TYPE W700

W700 SWITCH FILTER
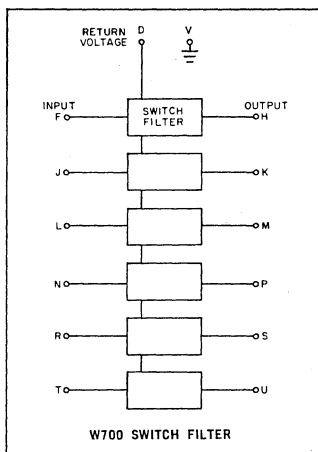
The W700 contains six switch filters for reducing contact closures to standard levels. The output drive of the switch filter is determined by the voltage to which the switch contact is returned. For maximum output drive at ground level, terminal D should be connected to —15v and the external contacts should be returned to +10v. In this case, open contacts produce a —3v output, and closed contacts produce a ground output. For maximum output drive at the —3v level, terminal D should be connected to +10v and the external contacts should be returned to —15v. In this configuration, open contacts produce a ground output and closed contacts produce a —3v output. Typical rise and fall times are given in the table below.

INPUT: When terminal D is connected to —15v, 6 ma flows through a closed contact. When terminal D is connected to +10v, 7 ma flows through a closed contact.

OUTPUT: See table below.

POWER: Terminal D connected to —15v: +10v(A)/-0 ma; —15v(B)/31 ma. Terminal D connected to +10v: +10v(A)/8 ma; —15v(B)/22 ma.

	Typical Rise Time	Typical Fall Time	Contact Current	Output Drive	
				at gnd	at —3 v
D connected to —15 v, switch contact returned to +10 v	5 msec (switch contacts closing)	20 msec (switch contacts opening)	6 ma	4 ma (switch contacts closed)	1 ma (switch contacts open)
D connected to +10 v, switch contact returned to —15 v	25 msec (switch contacts opening)	3 msec (switch contacts closing)	7 ma	1 ma (switch contacts open)	5 ma (switch contacts closed)

W700 — $20.00

POWER
SUPPLY — +3.6 VOLTS
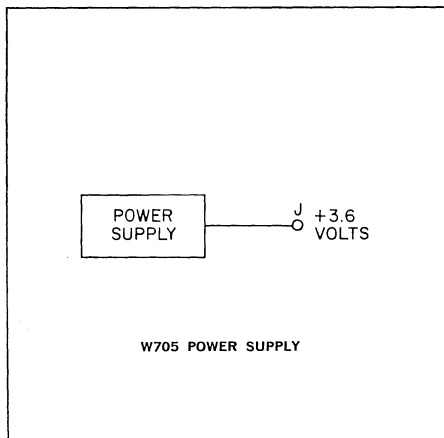
W705 POWER SUPPLY

This inexpensive power supply is of primary use in conjunction with the W706 and W707 teletype modules. The output can supply up to 1.5 amp at a nominal voltage of 3.6 volts. Voltage regulation for variable loading is provided and output ripple is less than 40 mv.

It is recommended that this supply be located where air flow is not restricted. Power dissipation is a maximum of 15 watts, depending on load current.
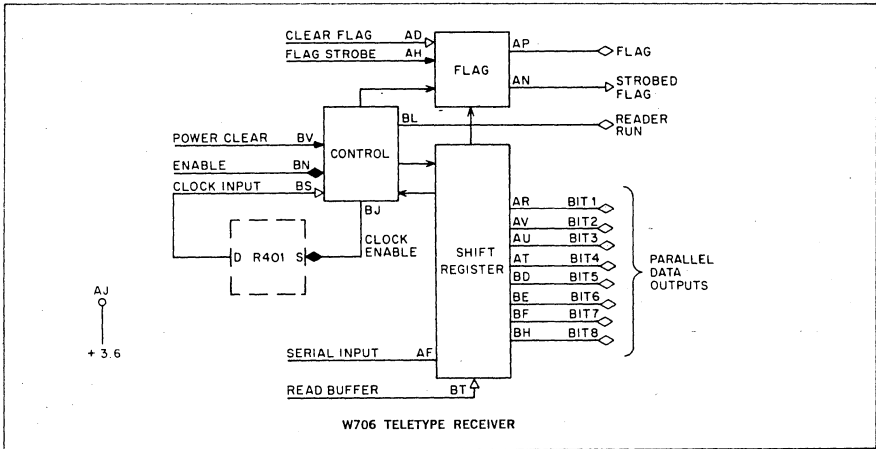
POWER: +10(A), 200 ma. plus load current

W705 — $15.00

TELETYPE RECEIVER
TYPE W706
(DOUBLE HEIGHT)

W
SERIES

W706 TELETYPE RECEIVER

The W706 Teletype Receiver is an integrated-circuit, serial-to-parallel Teletype code converter, self contained on a double-height module. This unit includes all of the serial to parallel conversion, buffering, gating, and synchronizing necessary to transfer information between an incoming asynchronous serial teletype line and a parallel binary device. Either a 5-bit serial character consisting of 7.0, 7.5, or 8.0 units or an 8-bit serial character of 10.0, 10.5, or 11.0 units can be assembled into parallel form by the W706 through the use of selective jumpers on the module. The serial input for one character is expected to be in sequence; a one unit −3 volt start signal, the five or eight character bits, a ground level stop signal of 1.0, 1.5, or 2.0 units. When the conversion is complete, the start and stop elements accompanying the serial character are removed. A logical 1 for a character bit is a ground level and a logical 0 is −3 volts. The first bit received on the serial line is Bit 1 at the parallel output.
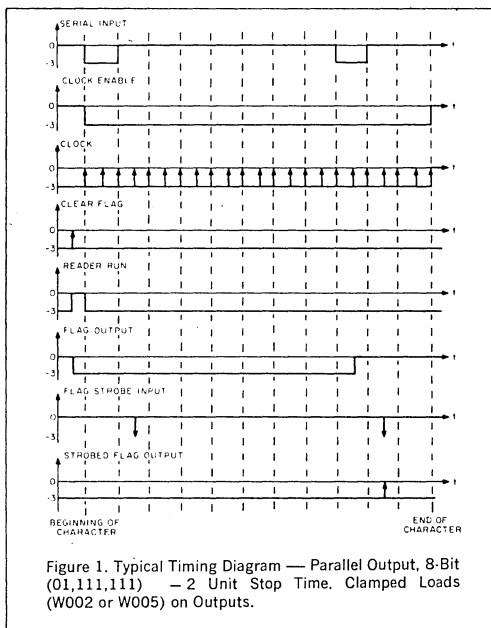
To perform the serial to parallel conversion, the re-

ceiver continuously examines the serial input line, and when a start element is recognized, the receiver enables the external clock through the Clock Enable Output and synchronizes with the incoming signal.

When the last character bit, either bit 5 or bit 8, is received, the flag is set and a ground level appears at the Flag Output. At this time, the Parallel Data Outputs of the W706 can be examined by a Read Pulse, and if desired, the flag can be cleared by a pulse on the Clear Flag Input. A new serial character must not be put on the Serial Input until the stop time of the previous character is counted out and so indicated by a ground level on the Clock Enable Output. For additional timing information see Figure 1. The W706 may be connected to devices other than a Teletype, providing that their serial output is similar to a Teletype code. Start element noise rejection of the W706 is approximately one volt from ground, requiring a line filter or use of the W708 on noisy teletype lines. To obtain additional Teletype applications data, write for Applications Note AP-W-001.

INPUTS: Standard Digital levels of −3 volts and ground or 400 nsec pulses as generated by module types R602 and R401. Input pins are shown on the diagram above.
CLOCK: 400 nsec positive pulses with a maximum receiver input frequency of 200 kHz. The clock fre-

quency must be twice the required serial input frequency thus defining one unit of character time as two clock periods. Input loading is 2.8 ma at −3 volts. The clock used must be externally gateable and similar to a R401 unless the W706 is used with a W708.

W706 — $150.00

Figure 1. Typical Timing Diagram — Parallel Output, 8-Bit (01,111,111) — 2 Unit Stop Time. Clamped Loads (W002 or W005) on Outputs.

ENABLE: A diode input, which if brought to ground, will disable the clock through clock enable. Disabling (or enabling) the clock during a serial input character can result in incorrect character reception.

CLEAR FLAG: A ground level or Digital standard 400 nsec positive pulse will clear the flag. If a level is used, it must be returned to --3 volts before the flag can be set. Loading is 1.4 ma at −3 volts. Typically the flag is sensed through one of the flag outputs and then cleared.

FLAG STROBE: Digital standard 400 nsec negative pulse or a --3 volt level. Loading is 1.4 ma at −3 volts. This input is NANDed with the flag and provides a ground level Strobed Flag Output signal when the flag is set.

READ BUFFER: A 400 nsec positive pulse provides parallel information from the W706. During this pulse, any bit which is a logical 1 will generate a 400 nsec positive pulse at the corresponding bit output. This input can be held at ground for continuous monitoring of bit outputs. Typically, this pulse is generated after a Flag Output has been sensed so that no incorrect character will be received on the parallel lines. Loading is 2.8 ma at --3 volts.

POWER CLEAR: Same input signals and loading as for Flag Strobe. Initialization of module components by a Power Clear signal is not necessary if the first

character received after power turn-on is insignificant. When not used, Power Clear can be left disconnected.

SERIAL INPUT: Digital standard levels of --3 volts and ground. A ground level during a bit input represents a logical 1. The first character bit to come in on this input appears at Bit 1 output. Loading is 2.8 ma at --3 volts.

OUTPUTS: All outputs are capable of supplying 20 ma at ground. The external load may be connected to any voltage between ground and −20 volts. Clamped loads such as W002 and W005 can also be used.

BITS 1 THRU 8: Buffered outputs generated by NANDing the internal bit and the Read Buffer. A ground level or positive pulse output represents a logical 1 for that bit. Unused outputs can be left open.

FLAG OUTPUT: Ground level output when the flag is set.

STROBED FLAG OUTPUT: Ground level output or pulse output when Flag Strobe is at −3 volts and the flag is set.

CLOCK ENABLE: Used with R401 clock or equivalent to synchronize the clock to incoming serial data. The output is an open circuit whenever a serial input is

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present and at ground at all other times. When used with a R401, this output is connected to the enable input of the R401.

READER RUN: Of use in teletypes equipped with relay controlled paper tape readers. The Reader Run Output is enabled (ground level) by a Clear Flag pulse and disabled by the W706 circuitry when a start pulse is received on the serial input. For ad-ditional information see Figure 1.

JUMPERS: Jumper positions are indicated on the top view physical sketch shown in Figure 2. The W706 is shipped with 8 bit, 2 unit shop jumpers in position.

POWER: —15 (B) 12 ma: +3.6 volts. 550 ma. This power is available from a W705 or any commercial supply that has an output regulation of ±10%.
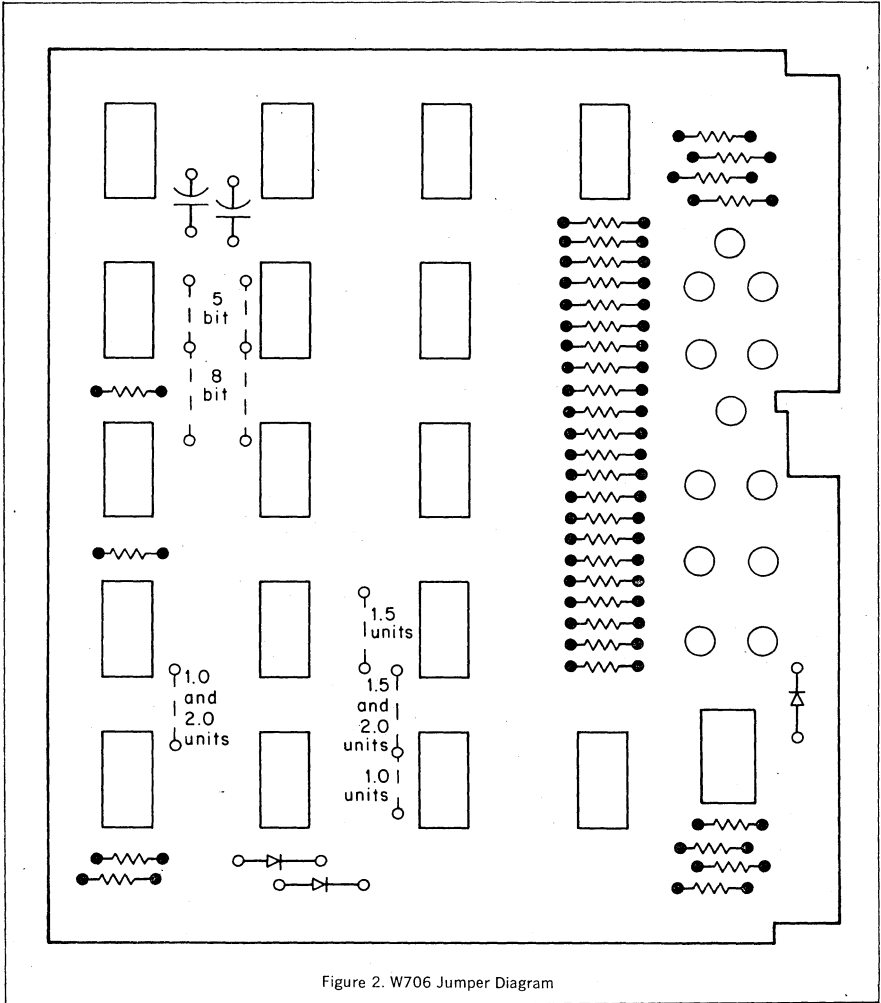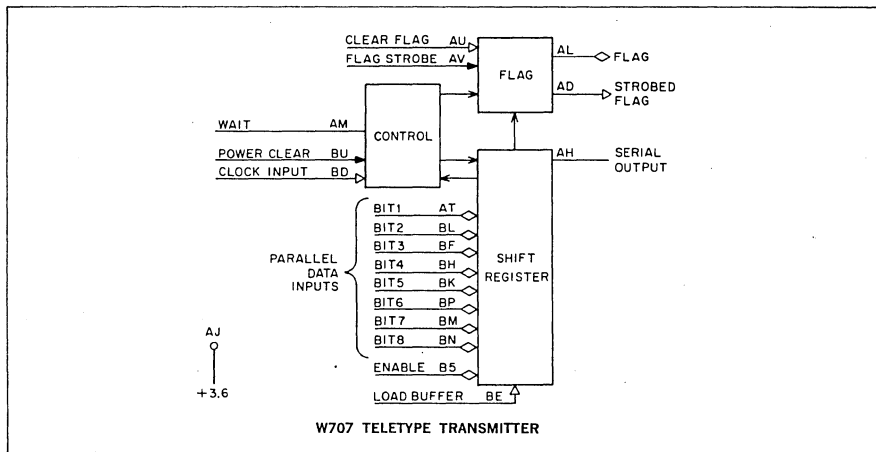

Figure 2. W706 Jumper Diagram

TELETYPE TRANSMITTER
TYPE W707
(DOUBLE HEIGHT)

W
·SERIES

W707 TELETYPE TRANSMITTER

The W707 Teletype Transmitter is an integrated-circuit parallel-to-serial teletype code converter, self contained on a double-height module. This unit includes all of the parallel to serial conversion, buffering, gating, and timing necessary to transfer information in an asyncronous manner between a parallel binary device and a serial teletype line. Either a 5-bit or 8-bit parallel character can be assembled into a 7.0, 7.5, or 8.0 unit serial character or a 10.0, 10.5, or 11.0 unit serial character, respectively, by the W707 through the use of selective jumpers on the module. When the conversion is complete, the necessary one unit negative voltage start signal and a ground level stop signal of 1.0, 1.5, or 2.0 units have been added to the original parallel character and transmitted over the serial line. The serial character is transmitted with the start signal first, followed by bits 1 through 8 in that order, and completed by the stop signal. One-half unit after the stop signal is put on the serial line, the flag is set indicating that the previous character has been transmitted and that a new parallel character can now be loaded into the W707. Transmission of this character will not occur until the stop time from the previous character is completed. See the timing diagram (Figure 1) for additional information.

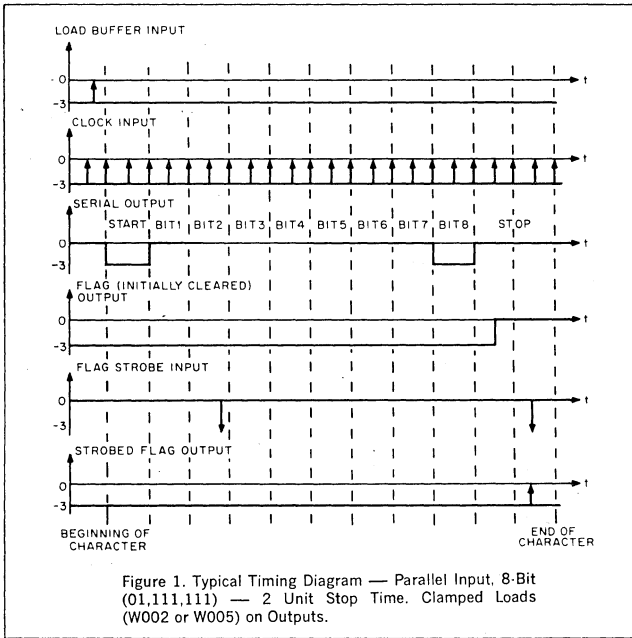The W707 may be connected to devices other than a Teletype. For example, two computer systems can be connected using a serial line as shown in Figure 2. To obtain additional Teletype applications data write for Applications Note AP-W-001.

INPUTS: Standard Digital levels of −3 volts and ground or 400 nsec pulses as generated by modules types R602 or R401. Input pins are shown on the module diagram above.

CLOCK — 400-nsec positive pulses with a maximum transmitter output frequency of 200 kHz. The clock frequency must be twice the required serial output frequency thus defining one unit of character time as two clock periods. Input loading is 2.8 ma at −3 volts.

LOAD BUFFER — A 400-nsec positive pulse which loads the parallel character into the W707. Typically this pulse is generated after a Flag Output has been sensed so that no incorrect characters will be transmitted. Loading is 2.8 ma at −3 volts.

BITS 1 THROUGH 8 AND ENABLE — Digital standard levels or equivalent with input loading 1.4 ma at −3 volts. When an 8-bit character is to be transmitted, all bit inputs are connected to data lines with bit 1 the least significant bit. For 5-bit characters, bits 1 through 5 are connected to data lines with bit 1 the least significant bit. Bit 6 is now used as the

Figure 1. Typical Timing Diagram — Parallel Input, 8-Bit
(01,111,111) — 2 Unit Stop Time. Clamped Loads
(W002 or W005) on Outputs.

Enable input, and bits 7, 8, and Enable are tied together and either returned to −15 volts through a 2.7K resistor or individually connected to W002 clamped loads. If the Enable input (Enable or bit 6 depending on character length) is at −3 volts during a Load Buffer Pulse, the parallel character information is loaded into the W707, but no serial transmission will occur. The Enable input must be at ground during a Load Buffer Pulse for serial information transmission. Ground levels on bit inputs represent a logical 1 or a Teletype "mark," and generate a ground output on the serial line at the corresponding bit times.

CLEAR FLAG: A ground level or DEC standard 400 nsec positive pulse will clear the flag. If a level is used, it must be returned to −3 volts before the flag can be set. Loading is 1.4 ma at −3 volts. Typically the flag is sensed through one of the flag outputs and then cleared.

FLAG STROBE: DEC standard 400 nsec negative pulse or a −3 volt level. Loading is 1.4 ma at −3 volts. This input is NANDed with the flag and provides a ground level Strobed Flag Output signal when the flag is set.

POWER CLEAR: Same input signals and loading as for Flag Strobe. Initialization of module elements by a Power Clear signal is not necessary if the first serial character transmitted after power turn-on need not be correct. When not used, Power Clear can be left disconnected.

WAIT: This input is available for use with the W708 in half duplex operation. Internal logic levels of +3.6 and ground appear at this input. It must not be connected to any signal but the WAIT output of the W708. If not used, this input must be left disconnected.

OUTPUTS: All outputs are capable of supplying 20 ma at ground. The external load may be connected to any voltage between ground and −20 volts. Clamped loads such as W002 and W005 can also be used.

SERIAL OUTPUT: Provides the teletype code serial output during character transmission. A logical 1 output is a ground level. If inductive loads are driven by this output, diode protection must be provided by connecting the cathode of a diode to the output and the anode of this diode to the negative supply used at the output.

FLAG OUTPUT: Ground level output when the flag is set.

STROBED FLAG OUTPUT: Ground level output when Flag Strobe is at −3 volts and the flag is set.

INVERTER: Pins BJ and AP are the input respectively of an inverter that can be used for any needed buffering. Input load is 1.8 ma at −3 volts.

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JUMPERS: Jumper positions are indicated on the top view physical sketch shown in Figure 3. The W707 is shipped with 8 bit, 2 unit stop jumpers in position.

POWER: —15(B)/3 ma; +3.6 volts/550 ma. This power is available from a W705 or any commercial supply that has an output regulation of ±10%.

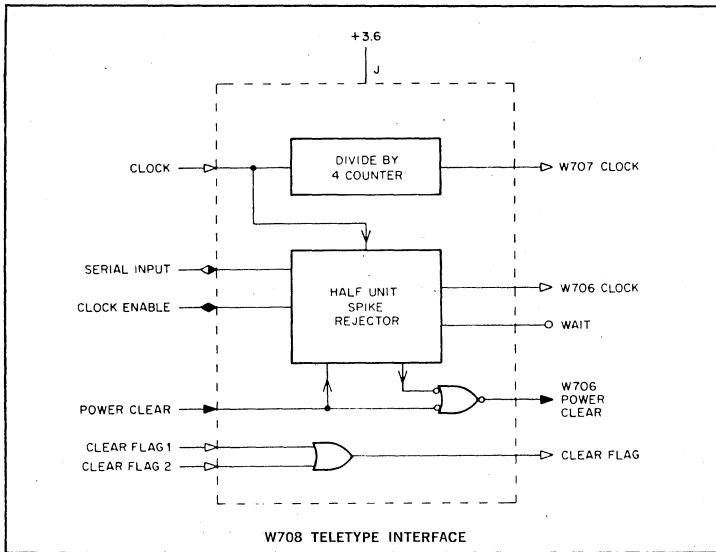Figure 2. Computer-to-Computer Serial Transmission.

Figure 3. W707 Jumper Diagram.
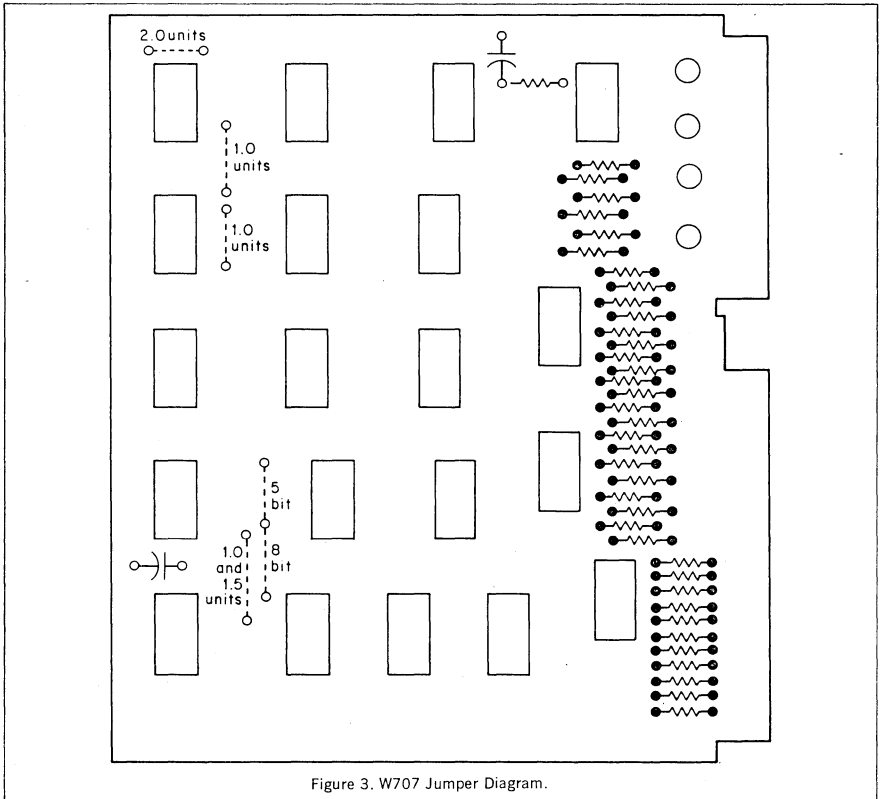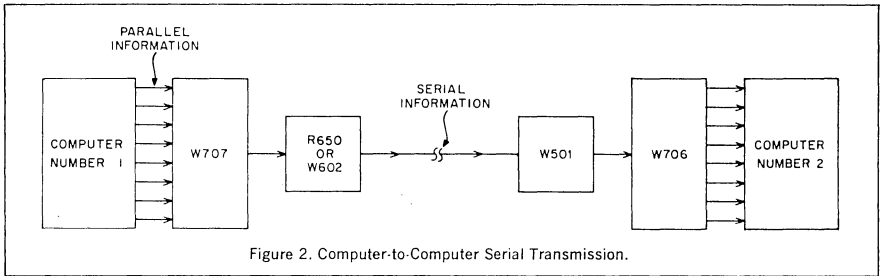
W708 TELETYPE INTERFACE

The W708 provides special gating controls and clock synchronization for teletype and data communications systems when used with the W706 and W707 Teletype modules. Such system features as half-duplex operation, half-unit start bit spike rejection, and single clock operation are possible when W706, W707, and W708 modules are used in a system. DIGITAL's Application Note AP-W-001 shows several system interconnections using a W708.

INPUTS: Standard Digital levels of 3 volts and ground or 400 nsec pulses as generated by module types R401 and R602.

CLEAR FLAG 1 and CLEAR FLAG 2: Input load is 2 ma at ground for each input. If either clear flag input is brought to ground, the clear flag output rises to ground. These inputs can be used to clear the flag of either a W706 or W707, or they can be used wherever a positive OR gate is necessary. In most half-duplex systems with echo characteristics, two clear flag inputs are needed on the W706.

CLOCK: Input load is 2 ma at ground. This input requires a 400 nsec positive pulse occurring at a repetition rate of eight times the serial data input frequency (baud rate). The maximum clock frequency is 1MHz.

SERIAL INPUT: Input load is 2 ma at ground. This input expects to see a serial input in teletype code format, with a space (binary zero) at 3 volt signal.

CLOCK ENABLE: Input load is 2 ma at ground. When the spike rejection feature of the W708 is used to reduce noise effects from long serial data lines, this input is connected to the Clock Enable Output of a W706. To reduce effects of long line signal distortion on reception of serial data, the stop time of the W706 module should be reduced by one-half unit. This change allows the W708 to sample the serial line three-eights of a bit time before the next start bit is expected. This input enables the W706 clock when at --3 volts.

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POWER CLEAR: Input load is 2.8 ma at 3 volts. Initialization of the W708 is accomplished by pulsing this input to 3 volts. When initialization is not required and an error in the first character received can be tolerated, this input can be left disconnected.

OUTPUTS: Levels or 400 nsec pulses between 15 volts and ground. All outputs have correct collector resistor for connections in systems with W706 and W707 modules. All outputs drive 15 ma to ground.

W707 clock: 400 nsec positive pulses with frequency one-quarter of the input clock frequency. This output is continuous if the clock input is connected and should be connected to the clock input of the W707.

W706 clock: 400 nsec positive pulses with frequency one-quarter of the input clock frequency. This pulse output is present only if the Clock Enable input is low. When used, this output should be connected to the clock input of a W706.

W706 POWER CLEAR: 500 nsec negative pulse occurs at this output whenever the Power Clear input is pulsed or a spike occurs in a start bit of the incoming serial data. This output should be connected to the Power Clear input of a W706.

CLEAR FLAG: If either Clear Flag 1 or Clear Flag 2 input is brought to ground, Clear Flag rises to ground.

POWER: ─ 15 (B) 25 ma; + 3.6 volts/300 ma. This power is available from a W705 or any commercial supply that has an output regulation of ±10%.

W708 — $55.00

W709 DIVIDE BY 16164 COUNTER
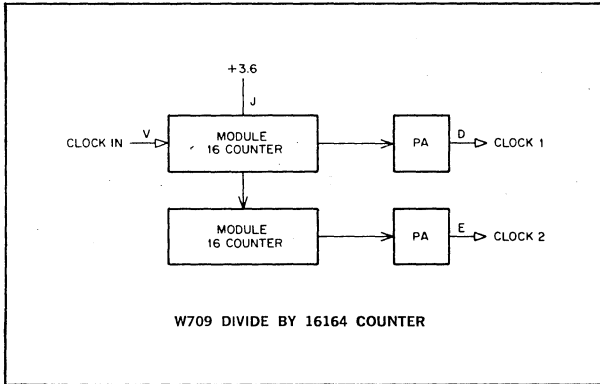
The W709 module provides the count-down circuitry for conversion of stable crystal clock frequencies to low frequencies common to teletype and data communications systems.

INPUT: CLOCK IN: Input load is 5 ma at ground. The input must be a 400 nsec or wider positive pulse occurring at a frequency not greater than 1 MHz.

OUTPUTS: Each output can drive 45 ma to ground during an output 400 nsec pulse. Normal levels at outputs are 3 volts.
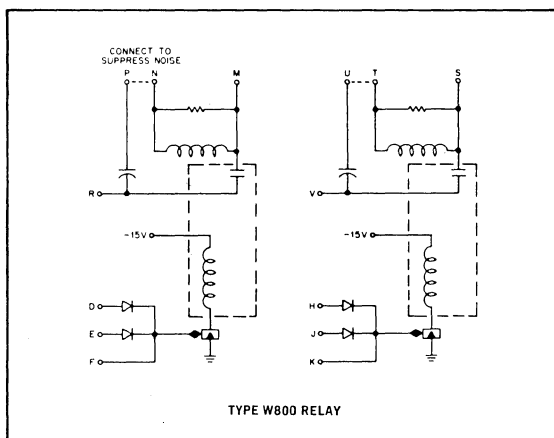
CLOCK 1: One positive 400 nsec pulse per sixteen input pulses.

CLOCK 2: One positive 400 nsec pulse per sixty-four input pulses.

POWER: —15 (B) 27 ma; +3.6 (J) 180 ma. This power is available from a W705 or any commercial supply that has an output regulation of ±10%.

CONNECT TO
SUPPRESS NOISE

TYPE W800 RELAY

The Type W800 Relay consists of two separate Form A reed relays, each with an optional protecting circuit. When the protecting circuit feature is desired, N and P (T, U) should be connected together, and the external circuit connected to P and R (U, V). To use the relay without the protecting circuit, the external circuit should be connected between M and R (S, V). The protecting circuit consists of a capacitor and a parallel combination of an inductor and a resistor. The protection circuit slows down current and voltage rise time at the time of contact closure or opening in order to minimize undesirable effects on sensitive logic in the vicinity of the relay. The

Type W800 is used to drive heavy loads on computer or logic command. The frequency limit is 100 cps. Maximum relay operating time is 2 msec.

INPUT: A Standard Level of 3v operates the relay. Input load is 1 ma at ground, 0 ma at 3v, shared by inputs at ground. Pins F and K are for use only with diodes such as R001 and R002. A maximum of 6 in. of wire may be attached to these points.

OUTPUT: The relay contacts close when the input requirements are met. Maximum contact ratings are 250v. 500 ma, 10 watts maximum.
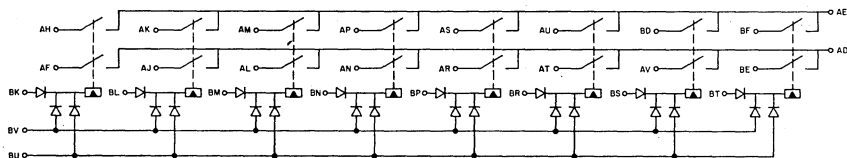
POWER: 15v/124 ma; +10v(A)/0.6 ma.

W800 — $45.00

W802 RELAY MULTIPLEXER

The W802 Relay Multiplexer contains eight double-pole, normally open reed relays. One of its uses is to address memory lines in memory testers. It can also be used as a low-speed multiplex switch where the grounded, low-noise performance of the A111 multiplexer is not required. Maximum closing time: 1.5 msec; typical opening time: 500 μsec.

INPUTS: Each driver is a 1 ma load shared among its grounded inputs. Contacts close when inputs are negative.
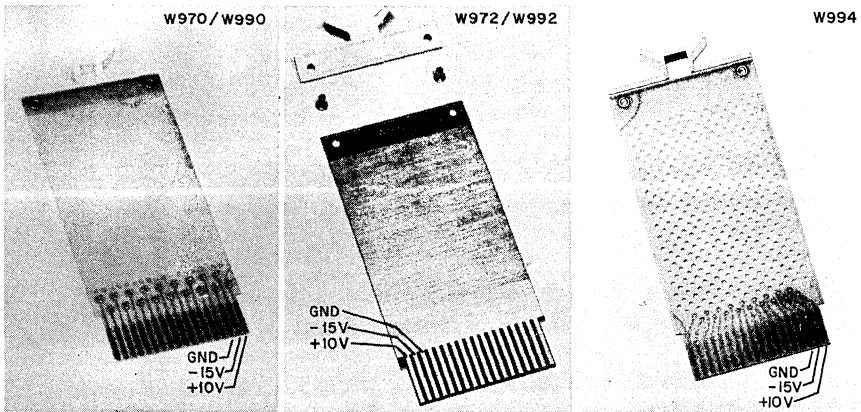
OUTPUTS: Relay contacts rated at 250v, 500ma, 10 watts maximum. Contact resistance typically 250 milliohms.

POWER: +10v(A)/2 ma; −15v(B)/20 ma plus 25 ma per energized relay (220 ma max for all relays energized).

W802 — $160.00

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W970/W990   W972/W992   W994

These 10 blank modules offer convenient means of integrating special circuits and even small mechanical components into a FLIP CHIP system, without loss of modularity. Both single- and double-size boards are supplied with contact area etched and gold plated. The W990 Series modules provide connector pins on only one module side for use with H800 connector blocks. W970 series modules have etched contacts on both sides of the module for use with double density connectors Type H803.

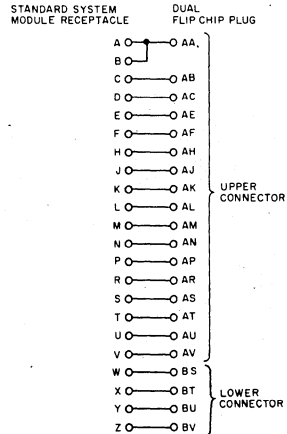| Type	Pins	Description	Handle	Price
W990	18	Bare board, split-lug terminals	attached	$ 2.50
W991	36	Bare board, split-lug terminals	attached	$ 5.00
W992	18	Copper clad, to be etched by user	separate	$ 2.00
W993	36	Copper clad, to be etched by user	separate	$ 4.00
W994	18	Perforated, 0.052" holes, 18 with etched lands. The holes are on 0.1" centers, both horizontally and vertically.	attached	$ 4.50
W995	36	Perforated, 0.052" holes, 36 with etched lands. The holes are on 0.1" centers, both horizontally and vertically.	attached	$ 9.00
W970	36	Bare board, no split lugs, similar to W990, contact both sides	attached	$ 4.00
W971	72	Bare board, no split lugs, similar to W991, contact both sides	attached	$ 8.00
W972	36	Copper clad, similar to W992, no hole pattern	separate	$ 4.00
W973	72	Copper clad, similar to W993, no hole pattern	separate	$ 6.00
W974	36	same as W994, contact both sides	attached	$ 9.00
W975	72	same as W995 contact both sides	attached	$18.00
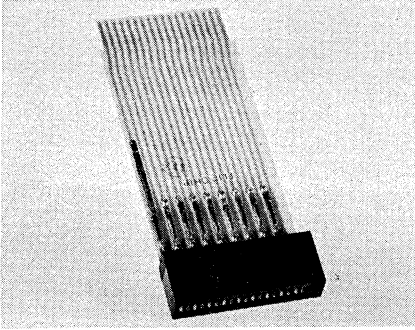
The W980 Module Extender allows access to the module circuits without breaking connections between the module and mounting panel wiring.

| W | SYSTEM MODULE ADAPTER |
| SERIES | TYPE W985 |
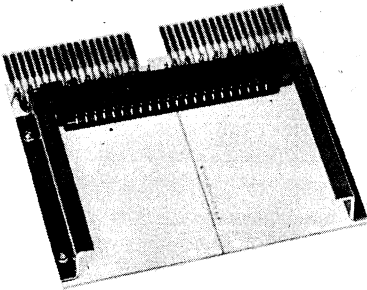
The W985 is an adapter which permits DEC system modules to be plugged into a FLIP CHIP mounting panel. It requires a block of four (two high and two wide) FLIP CHIP module spaces. The pin connections are made in two vertical slots with all pins being used on the upper connector and only pins S, T, U, and V being used on the lower connector. The two connectors on the component side of the module (to the left as you face the wiring) must be left vacant to accommodate the extra width of the system module. Built on a W991 board.

```
STANDARD SYSTEM        DUAL
MODULE RECEPTACLE      FLIP CHIP PLUG
        A O——————O AA
        B O
        C O——————O AB
        D O——————O AC
        E O——————O AE
        F O——————O AF
        H O——————O AH
        J O——————O AJ
        K O——————O AK    UPPER
        L O——————O AL    CONNECTOR
        M O——————O AM
        N O——————O AN
        P O——————O AP
        R O——————O AR
        S O——————O AS
        T O——————O AT
        U O——————O AU
        V O——————O AV
        W O——————O BS
        X O——————O BT    LOWER
        Y O——————O BU    CONNECTOR
        Z O——————O BV
```

W980 — $14.00
W985 — $34.00

A
SERIES

A100, A103 MULTIPLEXER SWITCHES

A121
MULTIPLEXER SWITCH
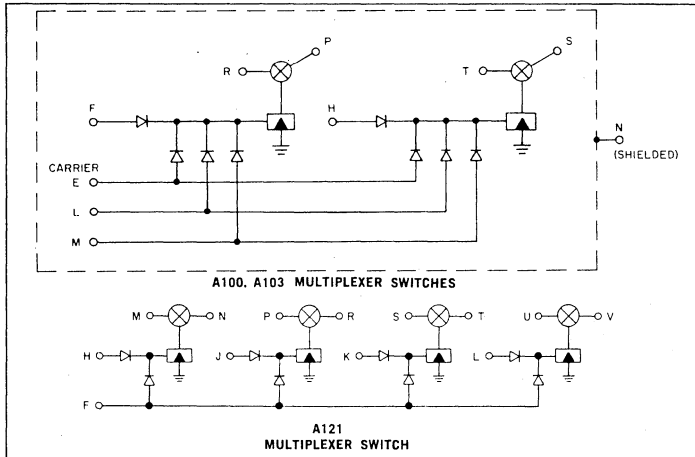
	A100	A103	A121
Control			
Signals	Digital levels and 5-mc square wave		
Enable	-3 v (5-mc square wave pin E)		3v
Load	$1\frac{1}{4}$ ma shared among grounded inputs		
Signal			
Max voltage	12v	30v	±10v
Max current	1 ma	1 ma	1 ma
"On" offset (max.)	200 μv	300 μv	0
"On" resistance (max.)	50Ω	50Ω	450Ω
"Off" leakage, capacitance	2 na, 10 pf	10 na, 10 pf	2 na, 10 pf
Carrier cross talk (with light filtering)	10 mv p-p	10 mv p-p	0
Speed			
50% input to tolerance output	Delay + sync + charging time (RC)		
Turn on delay	400 nsec	600 nsec	150 nsec
Turn off delay	200 nsec	1000 nsec	250 nsec
Synchronization	100 nsec	100 nsec	100 nsec

The A100 and A103 multiplexer modules contain two, single–pole, high–speed, solid–state switches. The switch drive is transformer-coupled so that the switch may be completely isolated from ground. The switch is turned on when the three control inputs are at −3v (or open-circuited) and the carrier is receiving a 5-mc square wave. The square wave can be made using a 10-mc clock and a 10-mc flip-flop. Since the switches are low impedance, care should be taken to avoid shorting signal terminals to ground or to each other, or simultaneously turning on two switches which have a common connection. There is a shield on Pin N that should be grounded. In newer modules, this connection is made internally. Better performance results if Pin N is also grounded externally.

The A121 multiplexer module contains four single pole, high-speed, insulated-gate FET switches. The switch is turned on when its two inputs are at −3 volts.

NOTE: A121 POWER REQUIREMENTS

1. The positive power source must be at least equal to or greater than the most positive excursion of the signal.

2. The negative power source must be at least 10 volts more negative then the most negative ex-excursion of the signal.

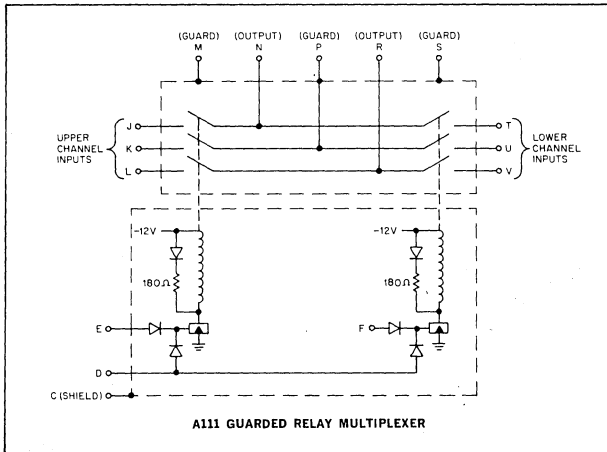3. The differential signal may not exceed 10 volts.

A100 — $100.00
A103 — $ 78.00
A121 — $ 65.00

GUARDED RELAY MULTIPLEXER SWITCH
TYPE A111
(Standard height, double width)

A111 GUARDED RELAY MULTIPLEXER

At low levels, multiplexing of analog signals must usually include guarding and shielding provisions to control noise pickup. Fortunately, transducers having low-level outputs are often slow speed devices like thermocouples, so that the limited speed of a relay multiplexer is not a serious problem, and the superiority of relay contacts for ultra-low-offset switching can be fully utilized. The two James Microscan 3-pole relays in the A111 are specially designed for this purpose, and are mounted on a double-clad circuit board which shields the analog from the digital circuitry and provides guarded contact wiring. The large size of the special relays used requires that two module slots be allowed for each A111 module.

INPUTS: Each relay driver requires 3 ma drive at ground, shared among grounded inputs. A shield on the component side of the board covers the driver circuitry and is connected to pin C. Another shield covering the area under the relay coils is connected independently to pin C. Contacts close when inputs are at −3v.

OUTPUT: Signal Contacts — 10v and 1 ma, max. Contacts switch within 1 msec. Life expectancy — 10^9 operations. Limits can be extended to 30v and 10 ma below 25 cps at short duty cycles. **Guard Contacts** — Designed for high voltage, high current transients. Guard contacts close before signal contacts close, open after signal contacts open.

POWER: +10 v(A)/0 ma; −15v (B)/85 ma.

SIGNAL
Max. voltage: $\pm$ 10 VDC
Max. current: 1 ma
Max. common mode voltage: 200 VDC
"ON" Resistance: 0.025 Ω (nominal)
"OFF" Resistance: 5 x $10^8 \Omega$

SPEED: Delay + Operate Time
Turn "ON" < 1 millisecond
Turn "OFF" < 1 millisecond

A111 — $93.00

The A200 is an operational amplifier mounted on an A990 amplifier board. Provisions are made on the board for the mounting of potentiometers for gain trim and balance. Mounting holes are also provided for input and feedback networks, and rolloff capacitor.

OPEN LOOP GAIN:	2×10^6
RATED OUTPUT	
Voltage:	± 11v
Current:	20 ma
FREQUENCY RESPONSE	
Unity gain, small signal:	10 MHz
Full output voltage:	300 kHz
Slewing rate:	30v/μsec
Overload recovery:	200 μsec
INPUT VOLTAGE OFFSET (Adjustable to Zero)	
Average vs. Temperature:	20 μv/°C
Average vs. Supply voltage:	15 μv/%
Average vs. Time:	10 μv/day
INPUT CURRENT OFFSET:	± 2 na
Average vs. Temperature:	0.4 na/°C
Average vs. Supply voltage:	0.15 na/%
INPUT IMPEDANCE	
Between inputs:	6 megohm
Common mode:	500 megohm
INPUT VOLTAGE	
Maximum:	± 15 volts
Maximum common mode:	± 10 volts
Common mode rejection:	20,000
POWER	
Voltage:	± 15 volts
Current at rated load:	35 ma

*REFER TO A990 FOR CONNECTIONS

A 200 — $130.00
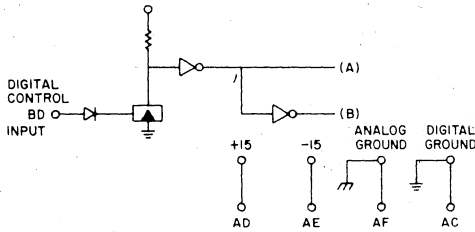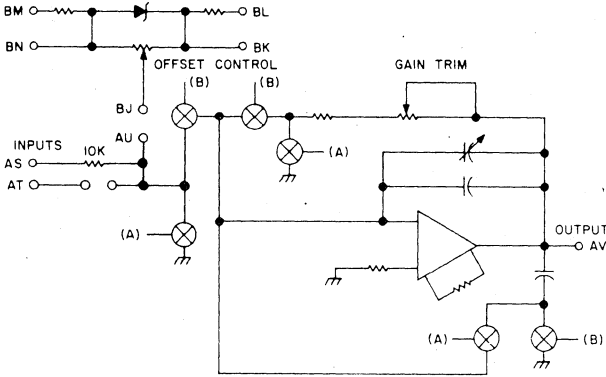
The A400 is an accurate sample and hold amplifier capable of tracking a full scale excursion in 12 micro-seconds to 0.025% accuracy. In the hold mode, the droop (decay) is less than 1 millivolt per millisecond. Two analog inputs are provided. Pin AS is connected to a 10KΩ resistor which provides for unity gain. Pin AT is connected to a point which allows for the insertion of different resistors to effect a gain change. The resistor connected to this point must be a precision 1% resistor with a temperature coefficient of 25 ppm.

An optional internal offset network which uses the ± 15 volt supply can be included. Connections are made according to the following table:

TO OFFSET OUTPUT

PIN	NEGATIVE	POSITIVE
BK	NO CONNECTION	ANALOG GROUND
BL	+15 VOLT SUPPLY	NO CONNECTION
BM	NO CONNECTION	-15 VOLT SUPPLY
BN	ANALOG GROUND	NO CONNECTION
AU	BJ	BJ

Offsets of up to 6 volts can be achieved in this manner. The digital control input (BD) requires the standard -3 volt level to sample (track) and ground to hold.

The A400 can be used to sample fast time varying wave forms and produce a time invariant output sufficient for analog to digital conversion. Several sample and holds may be used to simultaneously sample a number of inputs and be multiplexed into an A to D converter. The A-400 is mounted on a double height double width board. Therefore, the unit requires 4 card slots (2 x 2).

TRACK TIME TO 0.025%:	12 μsec
APERTURE:	Less than 150 nanosec
DROOP:	Less than 1 volt/sec
GAIN:	1.000 (Adjustable to 0.025%)
INPUT IMPEDANCE:	10KΩ $\pm$ 0.1% (AS)
FULL SCALE INPUT:	$\pm$ 10 Volts
OUTPUT CURRENT:	10 MA
TEMPERATURE COEFFICIENT (IN SAMPLE):	20 μvolt/°C Offset
TEMPERATURE COEFFICIENT (IN HOLD):	0.10 Volt/Sec/°C
POWER REQUIREMENTS:	$\pm$ 15 Volts/50 MA

A400 — \$330.00
Optional Offset — 50.00

225

OUTPUTS
+F   −V

COMP.

−N   +P
INPUTS
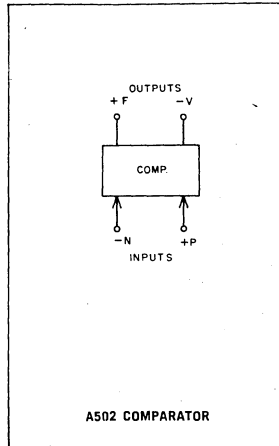
A502 COMPARATOR

The A502 Comparator is a high speed difference amplifier which compares two input voltages and indicates which of the two is the more negative. The comparator has a resolution of 1 mv, and an input range of 0 to −10v. The maximum combined error due to a change in the common input voltage from 0 to −10v and a 20°C temperature change is 5 mv equivalent input offset. Two potentiometers allow adjustment of the zero set and common balance.

As seen in the module diagram, when the input polarity of pins N and P are − and +, respectively, then the output polarity of pins F and V are + and −, respectively.

The comparator switching time is less than 250 nsec for a ±10 mv square wave. The switching time is also less than 250 nsec when one input is at −5.00v and the other is switched from ground to −5.02v. For finer resolution, the switching time is increased. When the comparator is driven from a high impedance, fast switching source, such as a digital-to-analog converter, time should also be allowed for

transients to settle. The analog-digital conversion application notes show illustrations of various combinations of divider networks and comparators in typical converter applications.

INPUT: 0 to −10v. The input draws up to 1 μa, depending on the relative polarity of the two voltage inputs. The maximum current difference between positive and negative input voltages is 1 μa. The difference input capacitance is 75 pf.
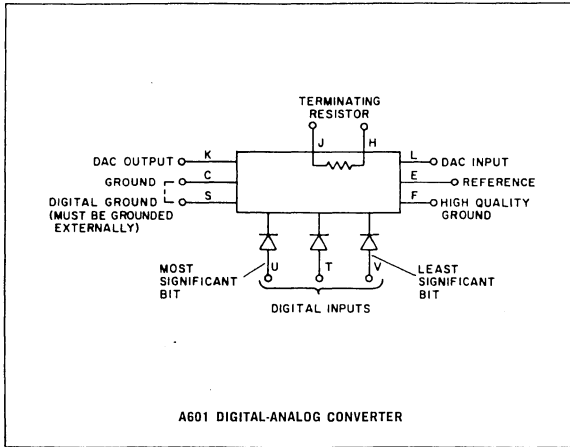
OUTPUT: The outputs produce standard levels of ground and −3 v. Each output will supply 5 ma (2 ma at maximum speed) at ground, and 14 ma (2 ma at maximum speed) at −3 v.

POWER: +10 v(A)/21 ma; −15 v(B)/55 ma.

NOTE: See "WIRING" section of reference supplies data sheet.

A502 — $110.00

A601 DIGITAL-ANALOG CONVERTER

The A601 is a three-bit digital-to-analog conversion module utilizing a star-type divider network and three precision germanium-transistor level amplifiers. It may be connected in series with other converters to form higher resolution converters. The accuracy of the A601 is suitable for up to eight bits of conversion. For higher resolution, it should be combined with the Types A604 and A605.

ACCURACY*: ±0.25% of expected value or ±0.5 mv, whichever is greater.

TEMPERATURE COEFFICIENT: ±100 ppm/°C max from +10°C to +45°C

OUTPUT IMPEDANCE: 1000 ohms ±0.1%

SWITCHING TIME: 300 nsec

SETTLING TIME: The settling time is determined by the capacitive loading at the output. Approximately 10 nsec/pf should be allowed in addition to the switching time.

DIGITAL INPUT: DEC standard levels. A —3v input signal at all digital inputs produces ground out. The input load is 1 ma at ground. If all inputs are not required, the most significant inputs should be used, and the least significant ones should be left open

circuited. **Converter Input** — The converter input may be driven from the converter output of another module in order to provide higher resolution. If not driven from another unit, it should be terminated with 1000 ohms to ground. A termination resistor is included in the module. **Reference Input** — The reference input requires a —15 ma DEC Type A702 or A704 Supply. The supply should be adjusted to approximately —10.01v to overcome the saturation resistance in the level amplifiers. **High Quality Ground** — This is the ground return for the reference supply and should be connected to the supply terminal and eventually to chassis ground at a noise-free location.

OUTPUT: The output is the analog equivalent of the digital input. The most positive output is 0v. The most negative output is —10v less the value of the least significant bit. The output impedance is 1000 ohms. If a bipolar or reduced output swing is required, the output may be loaded with 1000 ohms or more without affecting the accuracy.
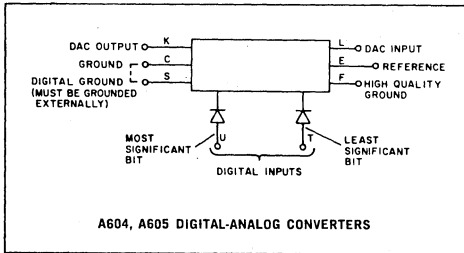
POWER: +10 v/1 ma; —15 v/40 ma; —10 v ref/ —9 ma.

* At 25°C includes tolerance of ±1.5 v on the +10 v and —15 v power supplies.

See **CAUTION** on A606 specifications.

A601 — $60.00

DIGITAL-ANALOG CONVERSION MODULES
TYPE A604, 605

```
DAC OUTPUT o——K                    L—o DAC INPUT
      GROUND ┌o——C                 E——o REFERENCE
DIGITAL GROUND └o——S               F——o HIGH QUALITY
(MUST BE GROUNDED                        GROUND
  EXTERNALLY)

         MOST        ┌U      T┐    LEAST
    SIGNIFICANT      o        o    SIGNIFICANT
         BIT                       BIT
                   DIGITAL INPUTS
```

A604, A605 DIGITAL-ANALOG CONVERTERS

The A604 and A605 are two-bit digital-to-analog conversion modules for use with the A601 in forming high resolution, high accuracy converters. Inputs and outputs are identical to the A601 except that a terminating resistor is not included. Germanium transistors are used.

	A604	A605
ACCURACY:*	±0.025% of expected value or ±0.25 mv whichever is greater	±0.005% of expected value or ±0.05 mv whichever is greater
TEMPERATURE COEFFICIENT:	±25 ppm/°C (from +10°C to +45°C)	±10 ppm/°C (from +10°C to +45°C)
OUTPUT IMPEDANCE:	1000 ohms ±0.1%	1000 ohms ±0.01%
SWITCHING TIME:	300 nsec	1.5 μsec

* At 25°C includes tolerances of ±1.5 v on the +10 v and —15 v supplies.

SETTLING TIME: The settling time is determined by the capacitive loading at the output. Approximately 10 nsec/pf should be allowed in addition to the switching time.

The following combinations of modules are recommended.

Resolutions (bits)	% of Full Scale	Analog Accuracy (% of Full Scale)	Units (quantity-type)
up to 8	down to 0.39%	0.25%	3-A601
9-10	0.195% to 0.098%	0.082%	1-A604, 3-A601
11	0.049%	0.038%	2-A604, 3-A601
12	0.024%	0.014%	1-A605, 2-A604, 2-A601
13	0.012%	0.01%	2-A605, 2-A604, 2-A601

These modules have been factory aligned; however, for maximum accuracy, the assembled system should be calibrated as a whole. Offset compensation has been made for standard digital-to-analog conversion. Additional offset may be added for analog-to-digital conversion.

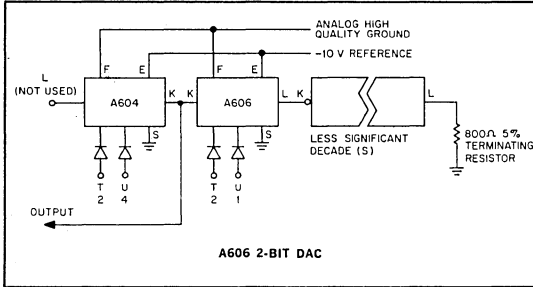Note: See "WIRING" section of reference supplies data sheet.

POWER: A604: +10 v/1 ma; +15 v/30 ma; —10 v ref/—10 ma. **A605:** +10 v A/1 ma; —15 v/30 ma; —10 v ref/—9 ma.

See **CAUTION** on A606 specifications.

A604 — $62.00
A605 — $78.00

A606 2-BIT DAC

TRUTH TABLE:

Decimal Number	8	4	2	1	A 2	B 4	C 2	D 1
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	0	1	1	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1

This module is similar to the A604 but with different values of ladder resistors. It is designed to be used in conjunction with an A604 to form one decade of BCD Digital to Analog conversion. The digital inputs of the decade must be 2-4-2-1 weighing (a conversion scheme from an 8-4-2-1 flip-flop register to a satisfactory 2-4-2-1 code is shown). Overall accuracy and other characteristics are the same as for A604, except as shown in the logic diagram.

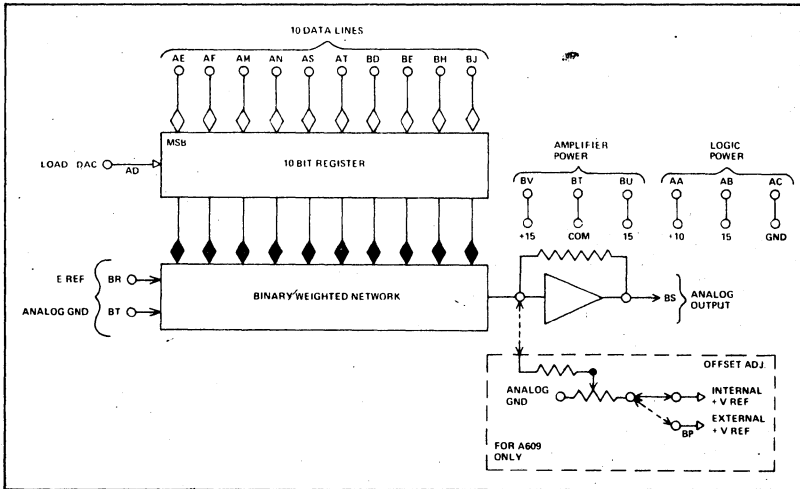**POWER:** +10v(A)/1.0 ma; −15v/30 ma; +10v ref./−9 ma.

CAUTION

Care should be taken when using power supplies with separate +10v and −15v on-off controls. If this is the case, the −15v must be turned off first and on last; otherwise, damage to the DACs may result.

8-4-2-1 FLIP FLOP REGISTER

A606 — $62.00
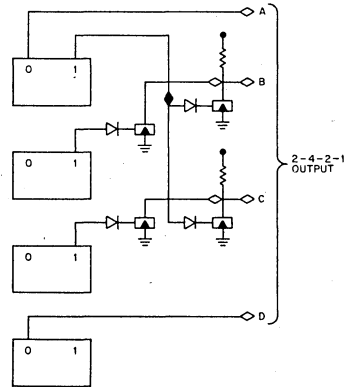
10-BIT D/A CONVERTER
SINGLE BUFFERED
TYPES A608 and A609

A SERIES

The A608 and the A609 Digital to Analog Converters (DAC) are contained on one DEC double Flip-Chip™ Module. These modules are also double width in the lower (B section) half. The converters are complete with 10-bit buffer registers, level converters, a precision divider network, and a current summing amplifier capable of driving external loads up to 10 ma. The reference voltage is externally supplied for greatest efficiency and optimum scale factor matching in multi-channel applications.

The A609 DAC output voltage is bi-polar while the A608 DAC output voltage is uni-polar.

Binary numbers are represented as shown (right justified) in Table 1:

TABLE 1

Binary Input	Analog Output (Standard)	
	A608	A609
0000_8	0v	-10v or -5v
0400_8	$+2.5$v	-5v or -2.5v
1000_8	$+5.0$v	0 volts
1400_8	$+7.5$v	$+5$v or $+2.5$v
1777_8	$+10.0$v	$+10$v or $+5$v

OUTPUT:

Voltage: (A608 — Standard)	0 to +10 volts
Voltage: (A609 — Standard)	±5 or ±10 volts
Current:	10 ma MAX.
Impedance:	<0.1 μsec
Settling Time:	
(Full scale step, resistive load)	<5.0 μsec
(Full scale step, 1000 pf)	<10.0 μsec
Resolution:	1 part in 1024
Linearity:	±0.05% of F.S.
Zero Offset:	±1.0 mv MAX.
Temperature Coefficient:	<0.1 mv/°C
Temperature Range:	0 to 50°C

INPUT:

Level:
Logical "1" = —◇   = +3.0v ±.6 volts
Logical "0" = —◆   = 0, +0, −.4 volts
Pulse: —▷
Amplitude: +4 volts @ 2 ma
Rise and Fall Time: 20 to 100 nsec
Width: ≥50 nsec
Rate: 10^6 Hz max.
Timing:
Data lines must be settled 40 nsec before the "LOAD DAC" pulse (transition) occurs.

POWER REQUIREMENTS:

Reference Power:	−10.06 volts, 60 ma
Amplifier Power:	±15 volts, 25 ma (plus output loading)
Logic Power:	+10 volts, 135 ma
	−15 volts, 160 ma

NOTES:
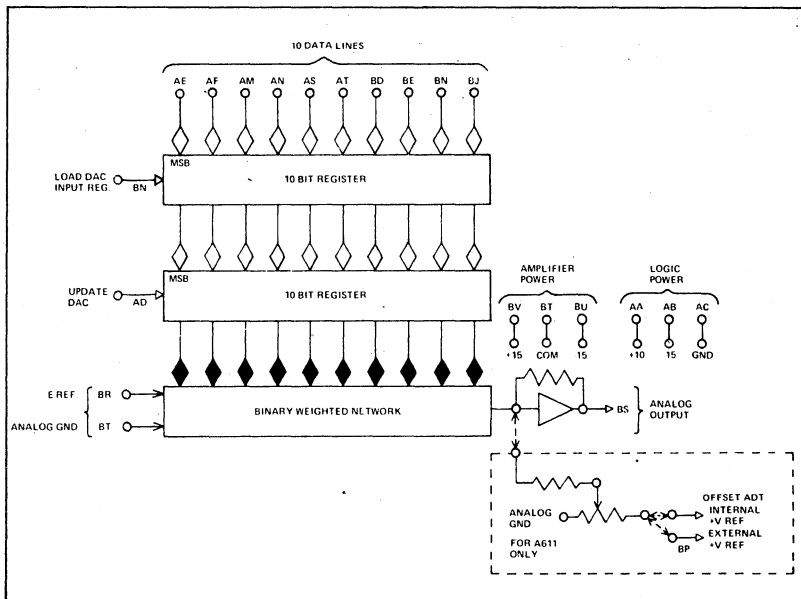*Voltage — A609: Full scale voltage (±5 or ±10) must be specified at time of purchase.
**Price: Price stated is for standard output voltage and current. Other output characteristics are available on request.

A608 — $350.00**
A609 — $375.00**

10 DATA LINES

AE AF AM AN AS AT BD BE BN BJ

LOAD DAC
INPUT REG.   BN

MSB   10 BIT REGISTER

UPDATE
DAC   AD

MSB   10 BIT REGISTER

AMPLIFIER POWER   LOGIC POWER

BV BT BU   AA AB AC

+15 COM 15   +10 15 GND

E REF   BR

ANALOG GND   BT

BINARY WEIGHTED NETWORK

BS   ANALOG OUTPUT

OFFSET ADT
ANALOG GND   INTERNAL +V REF
FOR A611 ONLY   EXTERNAL +V REF
                  BP

The A610 and the A611 Digital-to-Analog Converters (DAC) are contained on one DEC double Flip-Chip Module. These modules are also double-width in the lower (B section) half. The converters are complete with two 10-bit buffer registers, level converters, a precision divider network, and a current summing amplifier, capable of driving external loads up to 10 ma. The reference voltage is externally supplied for greatest efficiency and optimum scale-factor matching in multi-channel-application.

The A611 DAC output voltage is bi-polar while the A610 DAC output voltage is uni-polar.

The double-buffered DAC's are offered to satisfy those applications where it is imperative to update several analog output simultaneously. When DAC's deliver input to a multi-channel analog tape system or update the constants of an analog computer, the double-buffer feature may be necessary to prevent skew in the analog data.

Binary numbers are represented as shown (right justified) in Table 1:

TABLE 1

Binary Input	Analog Output (Standard)	
	A610	A611
0000₈	0v	−10v or −5v
0500₈	+2.5v	−5v or −2.5v
1000₈	+5.0v	−0 volts
1500₈	+7.5v	+5v or +2.5v
1777₈	+10.0v	+10v or +5v

OUTPUT:

Voltage: (A610 — Standard)	0 to 10 volts
Voltage: (A611 — Standard*)	±5 or ±10 volts
Current:	10 ma MAX.
Impedance:	<0.1 ohms
Settling Time:	
(Full scale step, resistive Load)	<5.0 μsec
(Full scale step, 1000 pf)	<1.0 μsec
Resolution:	1 part in 1024
Linearity:	$\pm0.005\%$ of full scale
Zero Offset:	±1.0 mv MAX.
Temperature Coefficient:	<0.1 mv/°C
Temperature Range:	0 to 50°C

INPUT:

Level:
  Logical "1" $= \longrightarrow\diamond$ $= +3$ volts $\pm.6$ volts
  Logical "0" $= \longrightarrow\blacklozenge$ $= 0, -0, +.4$ volts
Pulse: $\longrightarrow\triangleright$

Amplitude:	+4 volts @ 1 ma
Rise and Fall Time:	20 to 100 nsec
Width:	≥50 nsec
Rate:	10^6 Hz MAX.

Timing:
1. Data lines must be settled 40 nsec before the "LOAD DAC" pulse (transition) occurs.
2. The "Update DAC" pulse must occur more than 100 nsec after the "LOAD DAC" pulse.

POWER REQUIREMENTS:

Reference Power:	−10.6 volts, 60 ma
Amplifier Power:	±15 volts, 25 ma (plus output loading)
Logic Power:	+10 volts, 150 ma
	−15 volts, 60 ma

Notes:
*Voltage — A611:   Full scale voltage (±5 or ±10) must be specified at time of purchase.
**Price: Price stated is for standard output voltage and current. Other output characteristics are available on request.
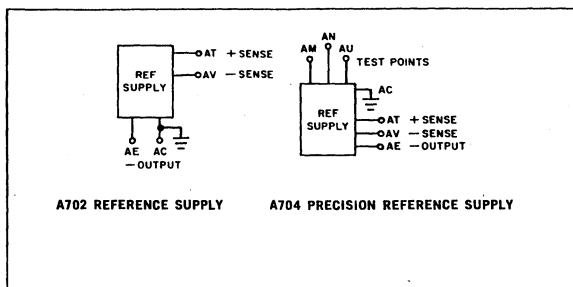
A610 — $400.00**
A611 — $425.00**

A702 REFERENCE SUPPLY   A704 PRECISION REFERENCE SUPPLY

Module Type	Output	Current	Temperature Coefficient	Regulation	Ripple Peak to Peak
A702	−10 v	±60 ma	1mv/°C	30 mv, no load to full load	10 mv
A704	−10 v	−90 to +40 ma	1 mv/8 hrs 1 mv/15° to 35°C 4 mv/0° to 50°C	0.1 mv, no load to full load	0.1 mv

Module Type	Adjustment Resolution	Input Power	Use	Output Impedance
A702	5 mv	−15 v/100 ma +10 v (B)/10 ma	Load with 500 μf at load. May also be preloaded if desired	0.5 ohms
A704	0.01 mv	−15 ±2 v/250 ma	See below for sensing and preloading	0.0025 ohms

REMOTE SENSING: The input to the regulating circuits of the A704 is connected at sense terminals AT (+) and AV (−). Connection from these points to the load voltage at the most critical location provides maximum regulation at a selected point in a distributed or remote load. When the sense terminals are connected to the load at a relatively distant location, a capacitor of approximately 100 μf should be connected across the load at the sensing point.

PRELOADING: The supplies may be preloaded to ground or −15v to change the amount of current available in either direction. For driving DEC Digital-Analog Converter modules, −125 ma maximum can be obtained by connecting a 270Ω±5% 1 watt resistor from the −10v pin AE reference output to pin AC ground (A704 only).

**PIN CONNECTIONS:** The A704 is a double-sized module. The top pin letters are prefixed A.

Wiring: Digital-analog and analog-digital converters perform best when module locations and wiring are optimized. All Digital-Analog Converter modules should be side-by-side, with Type 932 bus strip used to bus pins E and pins F together on all converter modules. In an analog-digital converter, the comparator should be mounted next to the converter module for the bits of most significance. The reference supply module should be mounted nearby, and if the A704 is used, its sense terminals should be wired to pins E and F of the most-significant-bits converter module. The high quality ground must be connected to the common ground only at pin AC of the reference supply module, and this point should also be the common ground for analog inputs to analog-digital converters. Do not mount A-series modules closer than necessary to power supply transformers or other sources of fluctuating electric or magnetic fields.

A702 — $ 58.00
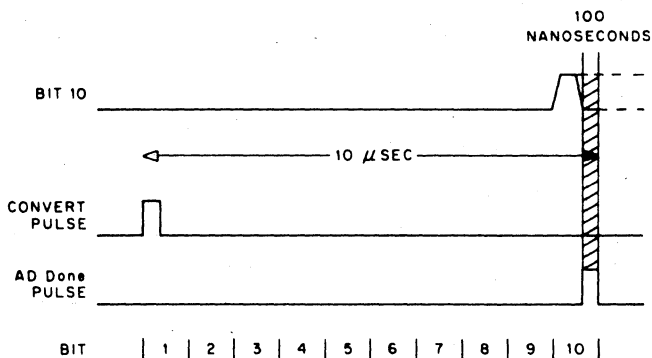A704 — $184.00

A801 10-BIT ANALOG-TO-DIGITAL CONVERTER
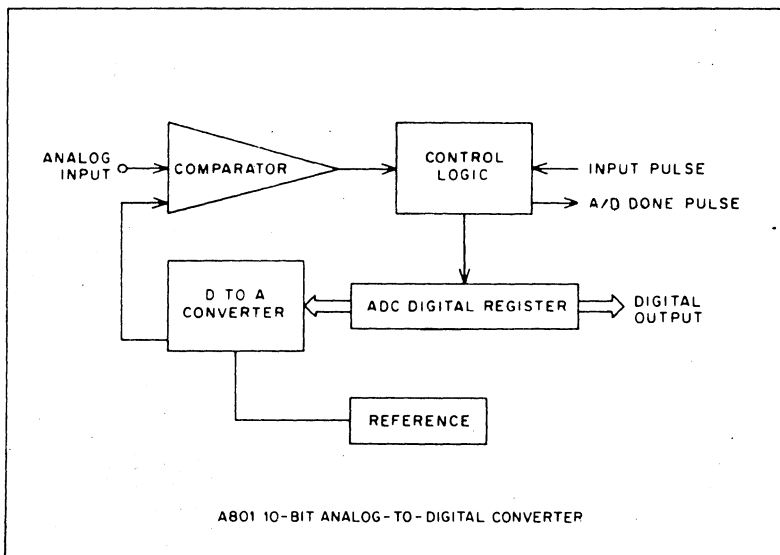
A801 10-BIT ANALOG-TO-DIGITAL CONVERTER

The A-801 is a complete, 10-bit successive approximation, analog to digital converter with a built in reference supply. The complete converter is contained on one DEC double FLIP CHIP™ logic module. Conversion is initiated by raising the Convert input to logic 1 (+4 volts). The digital result is available at the output within 10 microseconds. An A/D Done Pulse is generated when the result is valid. The A-801 uses monolithic integrated circuits for control logic, output register, and comparator.

The A-800 is identical with the A-801 except that no internal reference is included. A −10.06 volt external reference will produce +10.00 volts full scale and a −10.290 volt reference will produce +10.230 volts full scale (10 mv resolution).

100
NANOSECONDS

BIT 10

◁──────────── 10 μ SEC ────────────▶

CONVERT
PULSE

AD Done
PULSE

BIT | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |

TIMING

SPECIFICATIONS:

	Max.	Min.
Convert Pulse Input:		
Pulse Amplitude	+4v	+2v
Pulse Width	500 nsec	100 nsec
Pulse Rise Time	250 nsec	—
Pulse Current	1 ma	—
A/D Done Pulse Output:		
Pulse Amplitude	+4v	+2v
Pulse Width	300 nsec	100 nsec
Pulse Current	1.5 ma	—
Digital Output:		
Logical "0"	+0.4v	0v
Logical "1"	+3.6v	+2.4v
Output Current "0"	16 ma	—
Output Current "1"	−0.4 ma	0v
Input:		
Input Voltage	0 to +10v	
Input Impedance	1000 ohms	
Resolution:	10 bits	
Accuracy:	0.1% of full scale	
Temperature Coefficient:	0.5 mv/°C	
Operating Temperature:	0°C to 50°C	
Conversion Rate:	100 KHz MAX.	
Output Format:	Parallel Binary Uni-polar	

Power:
+15 volts ±1% 20 ma
−15 volts ±1% 160 ma
+10 volts ±1% 300 ma
Reference Power: (A800 only)
−10.060 volts at 60 ma for +10 volts full scale.
−10.290 volts at 60 ma for +10.230 volts full scale.
Options:
The input impedance of the A/D converter can be raised to greater than 100 megohms by adding an A200 input amplifier module. An A400 sample and hold amplifier module may also be included. The impedance of the converter with sample and hold is 10,000 ohms. Both options may be included simultaneously if high impedance and narrow aperture are both required.

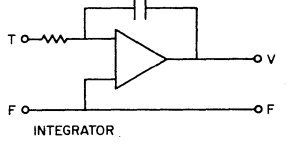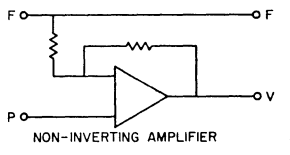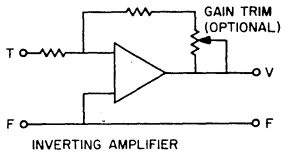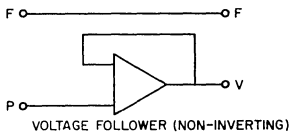|	
A-800	— $700.00
A-801	— 750.00
A200 (Input Amplifier)	— 130.00
A400 (Sample and Hold)	— 385.00
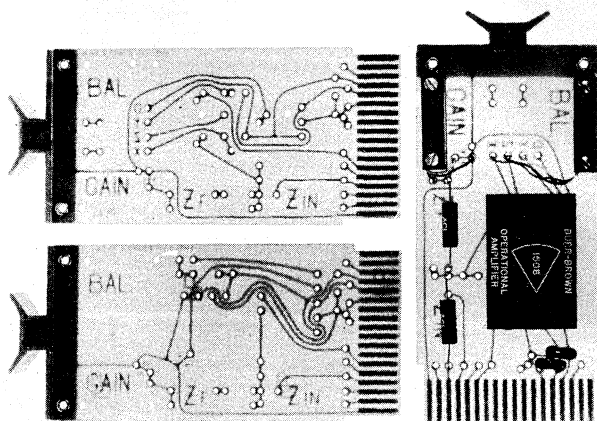
Many types of commercially available operational amplifiers can be mounted in the holes provided on these predrilled etched boards. Mounting holes and printed wires provide for balance, trim, gain trim, and feedback networks required to build such common operational devices as voltage followers, inverting or non-inverting amplifiers, integrators, differentiators, summers and subtractors. Most amplifiers listed in the table below require ±15v regulated supplies which are readily available from the amplifier manufacturers. Notable exceptions are Analog Devices' Models 101, 103, and 104 which may be used with standard DEC +10v, −15v supplies at some sacrifice in voltage range (+5, −10v) and noise.

POWER: Positive at pin D, negative at pin E, common at pin F for all types. Space is provided for mounting bypass capacitors used with some high frequency amplifiers.

TRIMMING: Mounting holes on 1″ centers at the handle end accept wirewound potentiometers for balance and feedback (gain) trimming. Gain rheostat may be connected in series with feedback components to allow precise adjustment of gain using inexpensive 1% feedback resistors. Board is etched to allow for use without gain trimming, and one printed conductor must be cut at caret marks to put a rheostat in the circuit. Gain rheostat stray capacitance to ground is driven by amplifier output.

Amplifier Supplier	Types accepted by A990	Types accepted by A992 (boosters too)
Analog Devices	101, 102, 104, etc.	103, 106, 107, etc.
Burr-Brown*	1500-46, 1500-68	—
Data Device Corp.	—	most types, except boosters
Nexus	Case K or Case L	Case Q
Philbrick	—	Case PP
Union Carbide	—	most types
Zeltex	—	Case A

*Except Burr-Brown differential output and chopper stabilized types. Perforated board W994 or other blank module may be used to mount non-standard configurations.

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F o————————o F

VOLTAGE FOLLOWER (NON-INVERTING)

GAIN TRIM
(OPTIONAL)

INVERTING AMPLIFIER

NON-INVERTING AMPLIFIER

INTEGRATOR

DIFFERENTIATING
CAPACITOR

GAIN
LIMITER

HIGH-FREQUENCY
ROLL-OFF NETWORK

DIFFERENTIATING
RESISTOR

DIFFERENTIATOR WITH DOUBLE BAND STOPS

FOUR-INPUT SUMMER

MATCHING TRIMMER CAN BE
USED TO OPTIMIZE COMMON-
MODE REJECTION. ALSO
EFFECTS GAIN.

SUBTRACTOR AND COMMON-MODE REJECTOR

B
SERIES

B-SERIES

INTRODUCTION

B-series FLIP CHIP modules operate at frequencies from dc to 10 mc. They are electrically and mechanically compatible with all other R & W series FLIP CHIP modules.

The B-series circuits described below are somewhat different from the R-series circuits described earlier.

B SERIES MODULE SUMMARY
INVERTERS
TYPES B104, B105, B123, B124

Each inverter is analogous to a switch. If the inverter base is at -3 v and the inverter emitter is at ground, the transistor is saturated and a conducting path is established between the emitter and collector of the inverter. If the base is at ground, or if both base and emitter are at -3 v, the emitter-collector path is open circuited (i.e., will not allow current to flow).

Delay through the inverter is approximately 12 nsec for lightly loaded inverters driven by a pulse.

The B104 contains three standard 10-ma clamped loads and four transistor inverters, each with its base, emitter, and collector brought to connector pins.

The B105 has five standard 10-ma clamped loads and five transistor inverters, with each emitter grounded, and with each base and collector brought out.

The B123 has three standard 10-ma clamped loads and eight transistor inverters. The inverters are tied together in series groups of two.

The B124 has three standard 10-ma clamped loads and nine transistor inverters, each with emitter grounded, and with each base and collector brought to terminals. The collectors are tied together in groups of three.

B104 — $17.00
B105 — $21.00
B123 — $31.00
B124 — $31.00

NAND/NOR GATES
TYPES B113, B115, B117, B171

The B113, B115, B117, and B171 are positive NOR diode gates; they form NOR gates for ground inputs and NAND gates for -3 v inputs. The outputs of the diode gates drive inverters similar to the B105, for power amplification. The typical total transition time is 40 nsec for output fall and 60 nsec for output rise. (Because the rise and fall delays differ, these diode gates may shorten negative input pulses markedly; see below.)

The B113 provides three standard 10-ma clamped loads and four diode gates, each with two diode inputs and the collector brought out.

The B115 has three standard 10-ma clamped loads and three diode gates, each with three diode inputs and the collector brought out.

The B117 has two diode gates, each with six diode inputs and the collector brought out. In addition, the emitter of one of the inverters is available.

The B171 is a single gate with twelve diode inputs. In addition to the positive NOR output, another inverter has been added at the output; using the inverted output makes the B171 an OR gate for ground inputs and an AND gate for — 3 v inputs.

POWER: B113: +10 v(A)/0.7 ma; −15 v(B)/43 ma. **B115:** +10 v(A)/0.5 ma; −15 v(B)/42 ma. **B117:** +10 v(A)/0.3 ma; −15 v(B)/2.5 ma. **B171** +10 v(A)/0.3 ma; −15 v(B)/31 ma.

B113 — $23.00
B115 — $21.00
B117 — $14.00
B171 — $18.00

THREE-BIT PARITY CIRCUIT
TYPE B130

This special logic module has two levels of high speed logic and complementary outputs. It is designed to compute the parity (odd or even) of the contents of a flip-flop register with a minimum of time delay, but it can be used wherever there is a need for four 3-input·negative diode AND gates feeding a 4-input OR gate.

Delay is typically 15 nsec from 50% of the input transition to 50% of the output transitions when output capacitive loading is very small.

POWER: +10 v(A)/49 ma; −15 v (B)/92 ma.

B130 — $50.00

HALF BINARY-TO-OCTAL DECODER
TYPE B155

The B155 module is used alone as a 2-bit decoder with two enable inputs, or it is used with another B155 to form a full 3-bit (binary-to-octal) decoder, using one combined enable line. Either way, each binary input combination results in one selected output held at ground if the decoder is enabled. No output will be selected if an enable input is held at ground. The decoder consists of four 4-input diode gates with appropriate input interconnections. All of the output transistor emitters are connected to pin D, providing a third enabling point. Also included are four standard 10-ma clamped loads.

POWER: +10(A)/0.6 ma; −15(B)/53 ma.

B115 — $21.00

FLIP-FLOP
TYPE B200

Most 10 mc registers can be built with B200 buffered flip-flops. The delay from pulse input to flip-flop output is short, suiting the B200 for unidirectional counting and shifting applications in which comparators are used to stop the action. Delayed level inputs are conditional, providing JK characteristics. Some typical operations the B200 can perform at 10 mc input rates are: gated shifting, parallel-serial conversion, jam transfer, and simultaneous-transition counting. Typical delay: 30 nsec. Typical output rise time: 35 nsec. See "B Series — Logic Configurations" for examples of B200 applications.

POWER: $+10v(A)/11$ ma; $-15v(B)/45$ ma.

B200 — $25.00

FLIP-FLOP
TYPE B201

Some 10 mc operations require a greater variety of pulse inputs than the B200 can provide. For example, read-in from several sources, bi-directional shifting, and arithmetic operations all require the greater flexibility of the B201.

In order to allow the outputs to be sampled by the same pulse that is changing the state of the internal flip-flop, the buffers include a controlled amount of delay.

The B201 has nine built-in inverters for accomplishing such operations as set, clear, jam-transfer, shift, and complement without the need for additional gating. The B201 can also be used in counters. Logic diagrams for these operations are shown under "B Series Logic Configurations."

POWER: $+10(A)/5$ ma; $-15(B)/63$ ma.

B201 — $56.00

QUADRUPLE FLIP-FLOP
TYPE B204

Module B204 contains four bits of unbuffered flip-flop memory. Each flip-flop comprises two B105-type inverters, two 10-ma clamped loads, a common clear input, and an indicator driver resistor.

POWER: $+10(A)/0$ ma; $-15(B)/94$ ma.

B204 — $29.00

DELAY (ONE SHOT)
TYPE B301

A delay (one shot) is a monostable multivibrator. When the input terminal is grounded, either through the inverter or externally, the level output switches from its normal ground level to -3 v for a pre-determined, but adjustable, period of time; then it switches back to ground. Simultaneously with the final transition, a standard 40-nsec pulse is generated at the pulse output.

The B301 contains three capacitors for delay range selection, and a screwdriver-adjustable rheostat for fine control. Typical level output duration ranges are 60 to 700 nsec, 0.5 to 10 μsec ,and 7 to 150 μsec using pins J, L, and V respectively. To increase the range further, connect an external capacitor between pins J and K. When pins U and P are jumpered together, fine adjustments are made with the internal control. For external control, a rheostat of about 5000 ohms can be connected between pins S and P.

The circuit recovery time using a given timing capacitor is approximately 10% of the maximum delay available with that capacitor. This limits the maximum input frequency to about 6.5 mc.

A 20% change in power supply voltage will change the delay typically 1%. Delay jitter (due to power supply ripple) is less than 0.3%.

POWER: $+10$ v(A)/2 ma; -15v(B)/110 ma.

B301 — $73.00

DELAY
TYPE B310 Double Height Board

The B310 contains four delay lines, each producing maximum delay of 50 nsec in 12.5 nsec steps. The output of each line is connected to a transistor inverter whose emitter is grounded. The collector terminal is available for logical gating. The 15 nsec delay through the inverter must be added to the delay of the line.

POWER: None required.

B310 — $66.00

DELAY WITH PULSE AMPLIFER
TYPE B360

The B360 contains a delay line which may be varied from 25 nsec to 250 nsec, and a standardizing pulse amplifier similar to one half of a B602. The length of the delay is adjusted by means of a slotted screw accessible from the handle-end of the module. The high resolution of the delay line (approxi-

mately $\frac{1}{4}$ nsec) makes it ideal for high-speed timing chains. By connecting the delay and pulse amplifier together with suitable logic in a feedback loop, a stable gateable clock may be obtained (see Application Section).

POWER: $+10$ v(A)/5 ma; -15 v(B)/50 ma.

B360 — $84.00

CLOCKS
TYPES B401, B405

The B401 Variable Clock produces standard pulses from a stable, RC-coupled oscillator with a wide range of frequencies. The variable clock is often used as a primary source of timing for large systems. Where very precise timing is needed, the B405 Crystal Clock, which contains a single-frequency crystal oscillator, may be used.

The frequency of the B401 is variable from 10 kc to 10 mc. Three capacitors determine the frequency range, and a potentiometer provides fine control. For lower frequencies, an external capacitor may be used. When terminals U and P are connected together, the internal rheostat provides fine control. If desired, an external rheostat can be connected between terminals P and C. A 20% change in power supply voltage will change the frequency less than 1%. Pulse-to-pulse jitter is less than 0.3%.

The B405 contains a series resonant crystal oscillator circuit and a pulse-shaping buffer amplifier which produces standard 40-nsec pulses. The frequency, specified by the customer, can be between 2 and 10 mc. The frequency is stamped on the crystal. Stability is 0.01% over the temperature range of -20 to $+55°C$.

POWER: B401: $+10$ v(A)/0 ma; -15 v(B)/70 ma. **B405:** $+10$ v(A)/51 ma; -15 v(B)/25 ma.

B401 — $ 57.00
B405 — $100.00

PULSE AMPLIFIER
TYPE B602

The B602 contains two pulse amplifiers which are used for power amplification, for standardizing pulses in amplitude and width, and for transforming a level change to a pulse. Delay from the input of an inverter that drives the PA to the PA output is approximately 20 nsec. Input pulses may occur at any frequency up to 10 mc.

POWER: $+10$ v(A)/2 ma; -15 v(B)/75 ma.

B602 — $36.00

CARRY PULSE AMPLIFIER
TYPE B620

Module B620 supplements the B201 for 10-mc counting applications. It supplies the circuitry to complement two B201 Flip-Flops and propagate their carry pulses. One B620 and one B201 can also be combined to form one bit of an up-down counter. The B620 contains two pairs of inverters for complementing 10-mc flip-flops with conditional set and clear inputs, and two standardizing pulse amplifiers each capable of driving three inverter bases. The propagation delay is approximately 10 nsec. Maximum pulse repetition frequency is 5 mc for pulse amplifiers.

POWER: +10 v(A)/6 ma; −15 v(B)/20 ma.

B620 — $47.00

POWER INVERTER
TYPE B681

The B681 Power Inverter contains four high current inverters, each with separate emitter connections. A 20-ma clamped load is permanently connected to each collector. Four additional 10-ma clamped loads are supplied. Input and output current ratings are double those of a standard inverter.

POWER: +10 v(A)/0 ma; −15 v/130 ma.

B681 — $25.00

BUS DRIVER
TYPE B684

The B684 contains two dual-purpose, non-inverting bus drivers and a −3 v supply. Each bus driver provides standard levels either to a large number of inverter base and diode loads, or to a terminated 90-ohm cable. All logic terminals are available at the connector. Delay through a bus driver is approximately 30 nsec.

POWER UNLOADED: +10 v(A)/80 ma; −15 v(B)/120 ma.

POWER FOR LOAD: Current to bring loads to ground must be added to the total demanded from +10(A); current to bring loads negative must be added to the total current from −15(B).

B684 — $52.00

APPLICATION NOTES

The chart below shows the effect of logical complexity of R-Series gate delay for output fall. Fall time is often the main source of delay, even though two-thirds of the rise time and only one third of the fall time elapses before the input threshold is reached. This is because the 2 ma load alone must charge wiring and input capacitance during output fall. Ample excess gate output current accelerates rise times, so propagation delay for output rise remains typically 30-40 nsec regardless of fan-out. Gate expansion at node inputs adds 15-30 nsec delay.

If speed is important, excess fanout capability may be traded to obtain it. The dotted line on the chart shows how adding a W005 clamped load affects propagation delay.

There are many factors that influence propagation delay: wiring capacitance, node expansion, enabling of connected gates, even ambient temperature. Since all of these factors together can account for substantial variations, the chart is a guide only.

PROPAGATION DELAY VS NUMBER OF OUTPUT CONNECTIONS
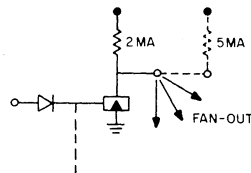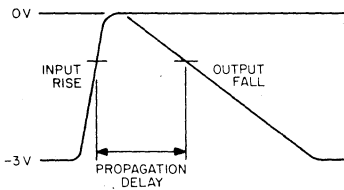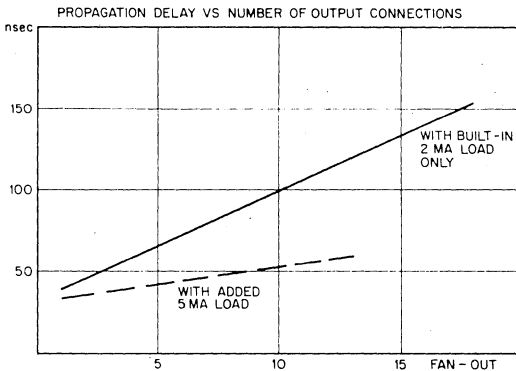
Figure 1   Propagation Delay

BCD COUNTING

It is sometimes preferable to represent binary numbers as decimal, especially when ease or speed of recognition by an operator is an important consideration. Familiar examples are elapsed time measurements, event recording, digital volt meters, and digital servo systems. The Application Note, General Purpose Digital Clock, describes one specific use of BCD counting.

The Application Note on Binary Coded Decimal Codes lists various popular codes in use today. Four of the most commonly used codes are implemented in this application note as single digit (decade) elements. These elements can be cascaded to provide long counting chains by simply connecting the proper carry out of the most significant bit in the decade to the proper carry input of the least significant bit of the next decade. In using the decades as elements in a system, it must be remembered that the longest carry propagation time may not be the time for propagating carries between successive digits (decades) in the counter. In a three digit, 8421 up counter, there are only two such carries between digits and one carry within each digit, as shown.

COUNTER STATE

Present	Next
099_{10}	100_{10}

Carries to propagate

0000   1001   1001   0001   0000   0000
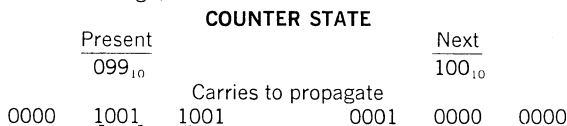
When one decade is changing from a decimal 7 to a decimal 8 there are three carries which must propagate within the decade itself.

DECADE STATE

Present	Next
7_{10}	8_{10}

Carries to propagate

0111   1000
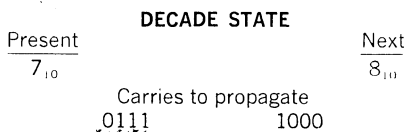
One of the most common BCD codes is 8421 code. Figure 1 is an up counter for this code. The inhibit decade input may be used to turn a counter off from a control level rather than shutting off the pulse train. Note that the level should change at least 400 nsec prior to the next pulse occurring at the pulse input in order for that pulse to be excluded from being counted. Figure 2 is an 8421 down decade. It is more expensive than an up counter because it requires a pair of gates in addition to the DCD gates on the R202's.

Figure 3 is a bi-directional 8421 counter decade that requires level control of the direction of count. The least significant decade of such a counter requires only a single pulse source, so on this digit the up and down pulse inputs may be tied together. It is important that direction levels do not conflict with one another. A ground level enables the direction, so the opposite direction must be at a —3v level. Changes in the direction level should occur at least 400 nsec prior to the next pulse. A single flip-flop may be used to furnish the direction levels in order to prevent conflicts from occurring.

Figure 4 is an 8421 up down counter with pulse control of direction. Here, two separate pulses must be furnished to the least significant digit. Changes in direction should occur no closer than 500 nsec.

Another popular decimal code is 2421. Figure 5 is a 2421 up decade. Figures 6 and 7 are up decade counters for the 5421 and XS3 (excess 3) decimal codes.

When interconnecting decades in a counter configuration it is the positive going edge of a pulse or level that causes the decade to increment or decrement. Figure 8 shows block diagram interconnections for up, down, and up/down decades.
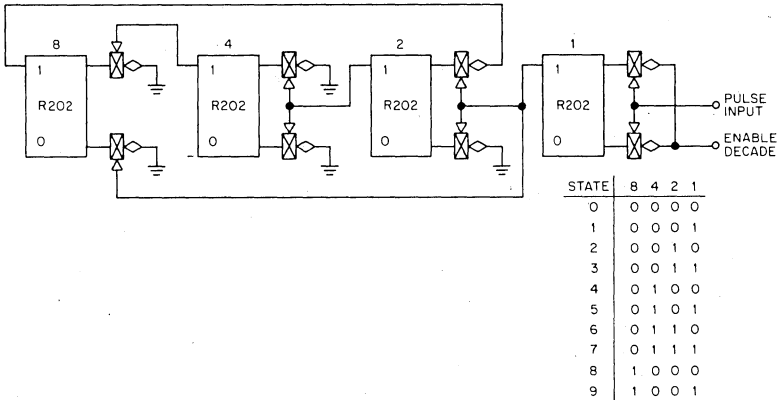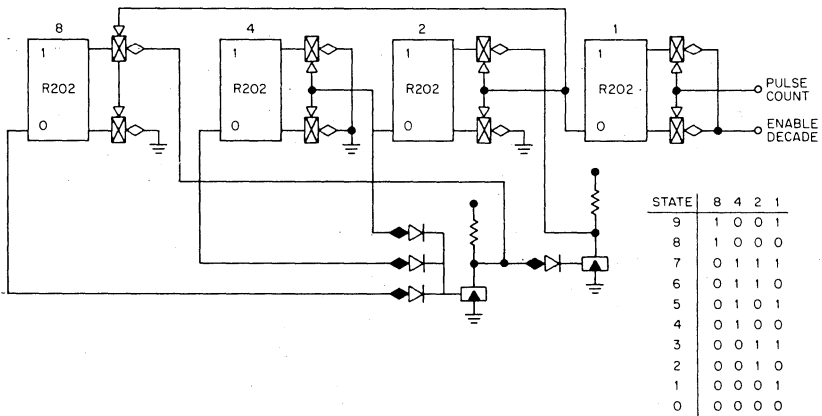

STATE	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Figure 1 8421 Up Decade

STATE	8	4	2	1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

Figure 2 8421 Down Decade
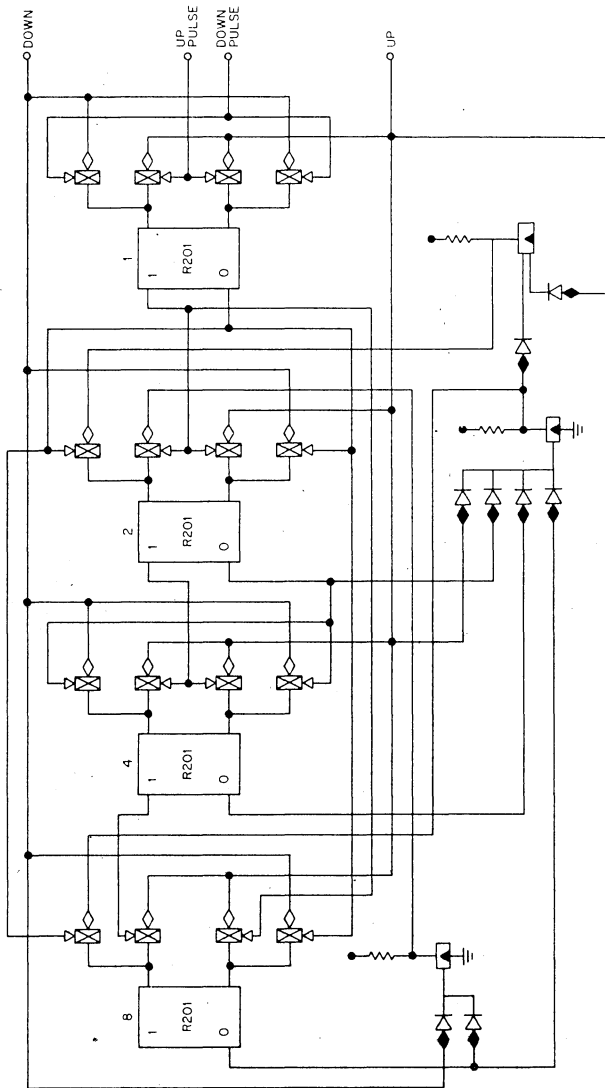
Figure 3 8421 Up/Down Decade, Level Control

253
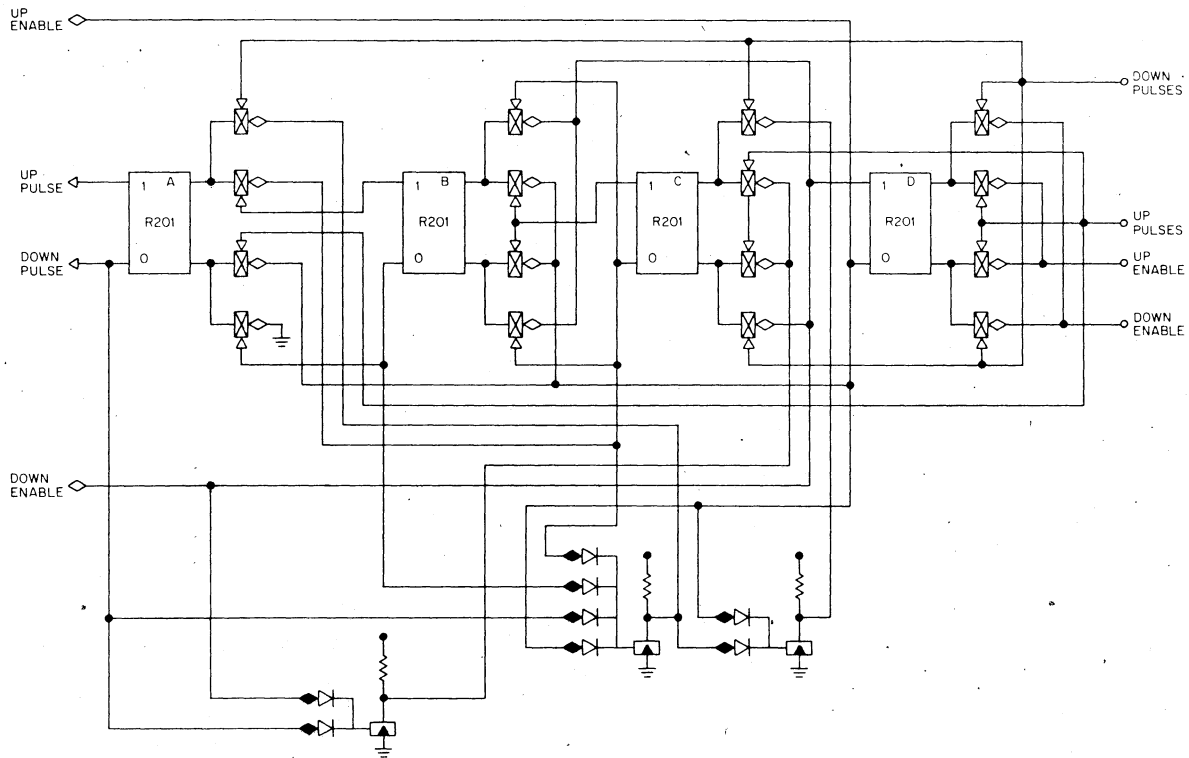
Figure 4 8421 Up/Down Decade, Pulse Control

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STATE	2	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1

Figure 5 2421 Up Decade

STATE	5	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0

Figure 6 5421 Up Decade

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STATE	A	B	C	D
0	0	0	1	1
1	0	1	0	0
2	0	1	0	1
3	0	1	1	0
4	0	1	1	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0
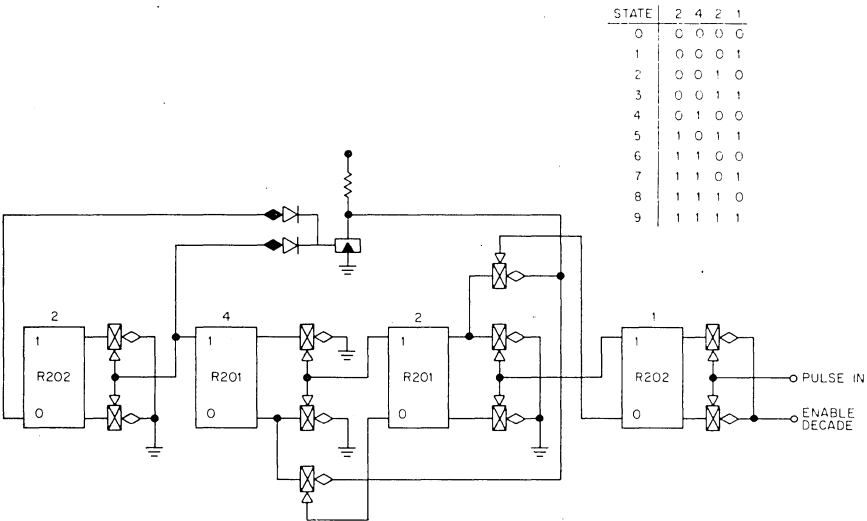
Figure 7 XS3 (Excess 3) Up Decade

UP/DOWN DECADES (LEVEL CONTROL OF DIRECTION)

UP/DOWN DECADES (PULSE CONTROL OF DIRECTION)
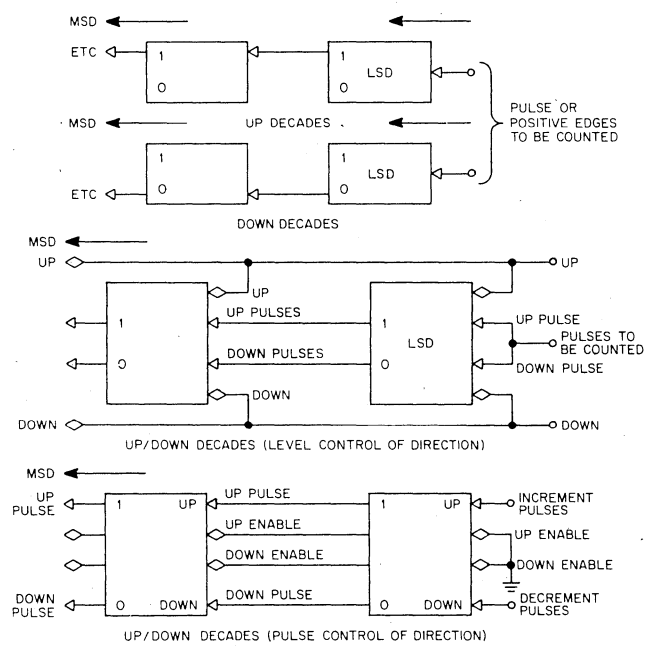
Figure 8 Interconnecting Decades

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PARTS LIST

	Type	Quantity	Description
8421 Up Decade (Figure 1)	R202	2	2 Flip-Flops
8421 Down Decade (Figure 2)	R202	2	2 Flip-Flops
	R111	1	3 Diode Gates
	R001	1	Diode Network
8421 Up/Down Decade, Level Control (Figure 3)	R201	4	Flip-Flop
	R111	1	3 Diode Gates
	R002	1	Diode Network
8421 Up/Down Decade, Pulse Control (Figure 4)	R201	4	Flip-Flop
	R111	1	3 Diode Gates
	R002	1	Diode Network
2421 Up Decade (Figure 5)	R202	1	2 Flip-Flops
	R201	2	Flip-Flop
	R111	1	3 Diode Gates
5421 Up Decade (Figure 6)	R202	2	2 Flip-Flops
XS-3 Up Decade (Figure 7)	R202	1	2 Flip-Flops
	R201	2	Flip-Flop
	R111	1	3 Diode Gates

GENERAL PURPOSE DIGITAL CLOCKS | APPLICATION NOTE

In most digital systems which collect data or record events, it is often desirable to have a general purpose digital clock from which real time of day may be read for recording along with measurements. The clock is also useful for generating periodic time signals which may be used to interrupt a computer when performing periodic scans of inputs, etc.

Such clocks most often derive their base frequency from the line frequency. The rest of the clock is usually a decimal divider chain which keeps track of the hours, minutes, seconds, and any smaller desired increments. The block diagram of the clock is shown in Figure 1.
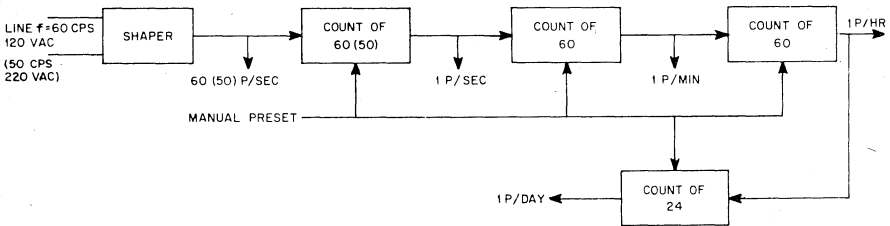
Figure 1 Block Diagram of Clock

Desirable features of such a clock are that it provide 24 hour time, may be preset to any time, may be read as a binary or BCD word, and that single pulses may be derived at periodic intervals for use as an auxiliary signal.

Two designs are offered here are:
    120v, 60 cps line, BCD clock, and
    220v, 50 cps line, BCD clock.

The only differences between the clocks are whether or not the first stage is a count of 60 or a count of 50. The count of 60 produces output changes at a 1 pps rate from a 60 cps source, while the count of 50 derives a 1 pps rate from a 50 cps source.

The input network consists simply of a 6.3v rms filament transformer, a small integrator to minimize high frequency noise, and a Schmitt Trigger (W501) to shape the negative portion of the cycle between -0.75v and -2.25v into a pulse which drives between 3v and ground. The positive edge of the output pulse occurs when the input reaches -2.25v. Figure 2 shows the shaper.
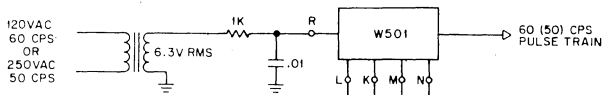
Figure 2 Line Frequency Shaper

The first counter is either for a 60 cps source (Figure 3), or a 50 cps source (Figure 4). The output of this chain is 1 pulse per second. Following this are two counts of 60 providing minute and hourly pulses, and finally, a count of 24 providing daily pulses. (Figure 5).

The preset logic is the same for each counter unit. Figure 6 shows typical preset logic for two digits. Only the bits required for the counter unit are implemented. A block diagram showing the pulse logic for presetting the clock is shown in Figure 7. The one shot (R302) provides a delay between clearing and presetting the bits of the clock, which should be ones. The PA's must generate 400-nsec pulses to insure proper clock clearing.

PARTS LIST

Type	Quantity	Description
R202	14	Counter
W002	1	Preset Logic
R111	5	Diode Gate
R601	1	Pulse Amplifier
R302	1	Delay (One Shot)
W501	1	Schmitt Trigger
W501	1	Line Frequency Shaper

Additional Hardware

1	6.3v̇ fil XFMR
1	1K-¼ watt res
1	.01 µf cap
4	decade switches
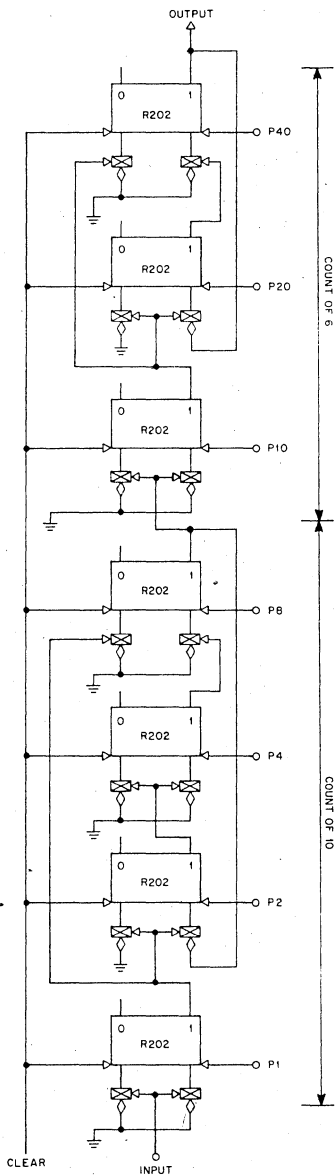
Figure 3 BCD Count of 60 Logic Counts 0 through 59   Figure 4 BCD Count of 50 Logic Counts 0 through 49
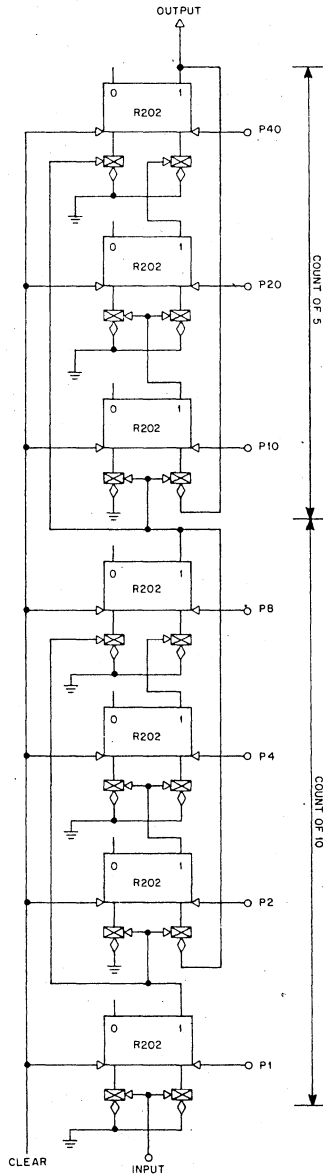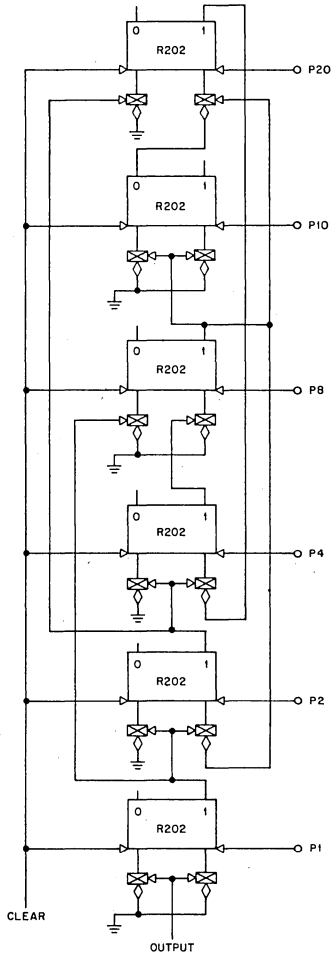
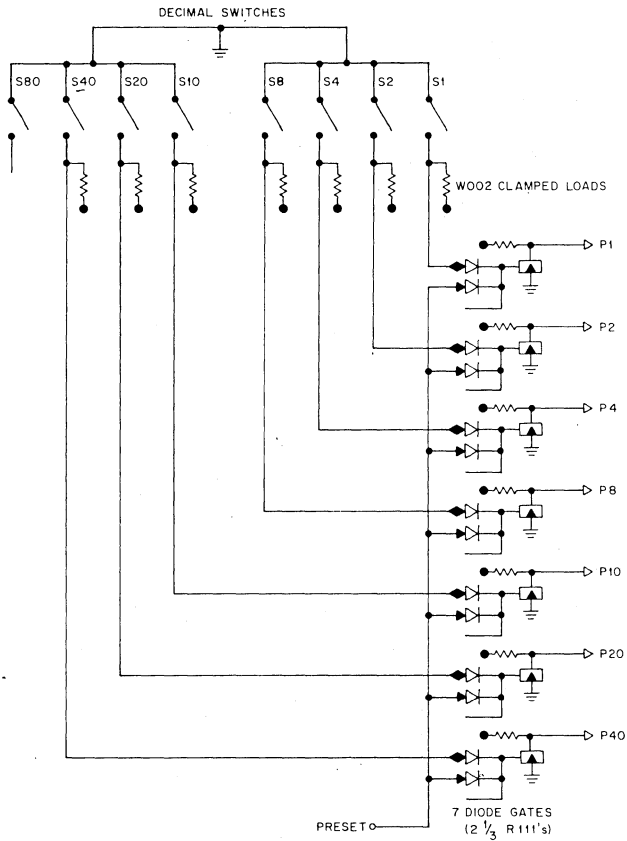Figure 5 BCD Count of 24 Logic Counts 0 through 23

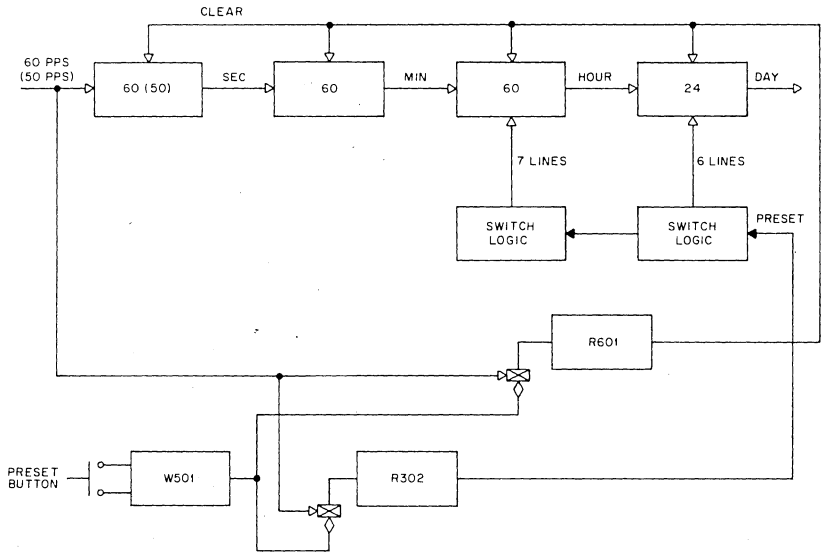Figure 6 Preset Switch Logic (Hours or Minutes)

Figure 7 Clock Preset Logic

Parallel adders can be used to add two binary numbers. The augend is called the resident number and is stored in the accumulator register (AC_{0-7}). The addend, or incident number, is stored in the incident register (I_{0-7}). The sum appears in the accumulator. R series Type R201 Flip-flops can be used as shown in the logic diagram, Figure 1. Addition is performed in two steps. The first step is a half-add. Each digit of the accumulator is complemented (made negative) if the corresponding digit of the incident number is 1 (inner pair of DCD gates on AC_{0-7}). The second step is a carry. A carry is generated if a digit in the accumulator is 0 and the corresponding incident number is 1 (R111 gates). A carry is also propagated if an accumulator digit is 1 and it receives a carry pulse from the next less significant accumulator digit (upper DCD gate on each pulse amplifier). Each stage will propagate one carry at most. After all carries have been propagated, addition is complete and the accumulator contains the sum of the incident and the resident numbers.

When the most significant bit is used as a sign bit, a carry pulse amplifier is provided on the input to AC_7 (least significant bit) to provide for End Around Carry (EAC). EAC only occurs when dealing with negative numbers (AC_0 and I_0 are considered the sign bits). If the full 8 bits of the AC are to be used as a positive accumulator, the EAC pulse amplifier must be disabled so that end carries will not affect bit AC_7.

Overflow can occur only in adding two positive numbers or two negative numbers together (in the latter case it sometimes is referred to as underflow). Overflow is characterized as a carry out of the most significant bit when adding two positive numbers, or a lack of a carry out of the most significant bit when adding two negative numbers. In the case of the unsigned adder (where AC_0 is the most significant bit) the overflow is the EAC pulse. In this case the output of the unused EAC pulse amplifier may be used to set an overflow flip-flop.

Subtraction

An adder may also be used for subtraction. To subtract a number from the accumulator, the AC is complemented and added to the incident number. The result is then recomplemented as the final step.

The steps involved in performing a subtraction depend on whether the 1's complement or the 2's complement number system is used to represent a negative number. Since the 1's complement number system is easiest to implement, it is the one described here. To subtract a number from the accumulator, the steps are (1) complement the AC by means of the complement pulse input, (2) half-add, (3) carry, and (4) recomplement the AC. With this number system, it is necessary to use the end around carry into AC_7 as shown in Figure 1. One's complement subtraction may also be performed by (1) complementing the incident number, (2) half-add, and (3) carry. Note that in 1's complement arithmetic, there are two possible zeros. This is because the 1's complement of $+0$ is -0 (11111111).

When subtraction is included in the arithmetic capability of the unit, the AC and incident numbers must be considered as signed numbers (bits AC_0 and I_0 being the sign bits). Overflow and underflow detection is quite important here, for one of the properties of 1's
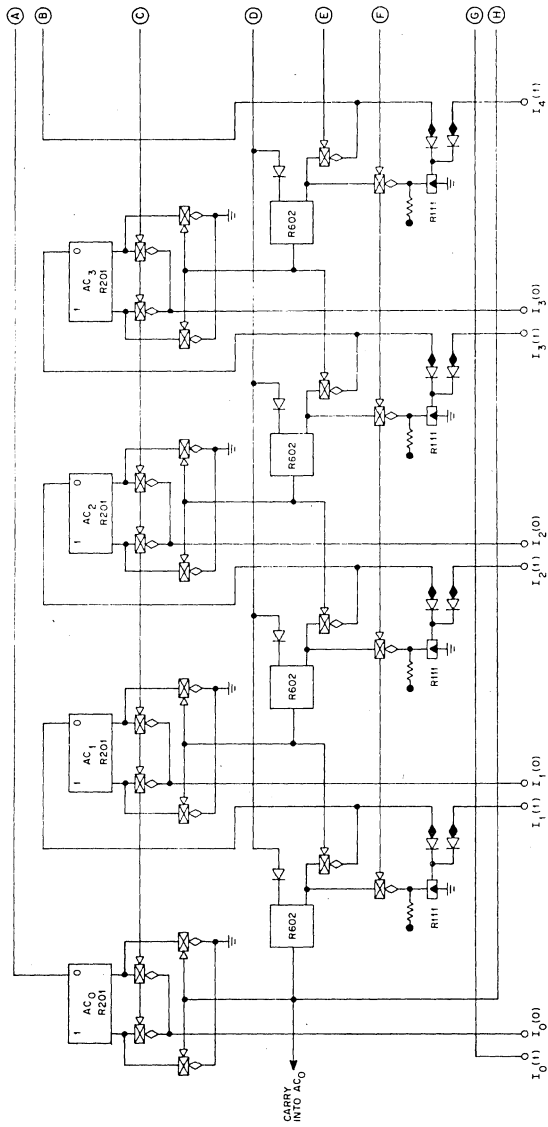
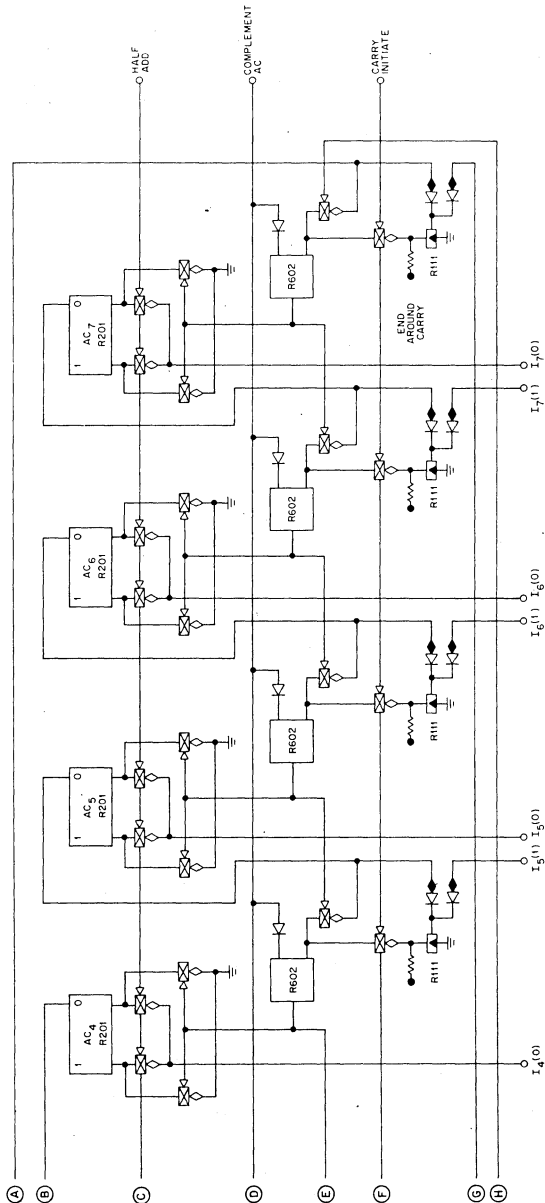Figure 1a 8-Bit Parallel Adder (4 Most Significant Bits)

Figure 1b   8-Bit Parallel Adder (4 Least Significant Bits)

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complement arithmetic is that the sign of the result is incorrect if overflow or underflow has occurred. Detection of overflow is simply derived from the previous definition of 1's complement overflow. If the result of the sign bit after the half-add is a 0, then the carry into bit AC_0 is allowed to set the overflow flip-flop (see Figure 2). Precautions must be taken to prevent this carry from setting overflow when performing a complement of the AC. This may be done by gating AC_0 with a status level to indicate that an addition is being performed.
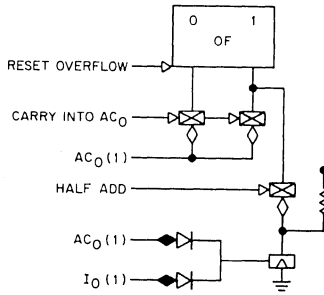
Figure 2 Overflow Logic

Underflow is detected by implementing the rule that no carry into the sign bit occurs. We allow the overflow to set on the half-add step if I_0 and AC_0 are both ones. When the carry into AC_0 occurs if AC_0 is a 0 (after half-add), the overflow flip-flop will reset. If there is no carry into AC_0, the overflow flip-flop remains set indicating an underflow. The overflow flip-flop must not be looked at until after the addition is completed (after carries have rippled). The overflow bit must be reset before the next addition.

The timing for the adder is as follows:

1. Time between half-add pulse and carry initiate: ≥ 500 nsec

2. Time for settling after carry initiate: 560 nsec maximum (EAC initiating a ripple down the length of the counter)

PARTS LIST

Adder and Control System		
Type	Quantity	Description
R201	8	Flip Flop
R602	4	2 Pulse Amplifiers
R111	3	3 Diode Gates

Buffer Register for Incident
Number where required

Type	Quantity	Description
R203	3	3 Flip Flops

Overflow Detection		
Type	Quantity	Description
R201	1	Flip Flop
R111	1	3 Diode Gates (use spare in adder)

A five-bit binary number can be decoded into its 32 permutations by using 32 five-input NAND gates made from: eleven R111, five R001, and six R002, a total of 22 modules. Various classical techniques of decoding can be used to achieve different degrees of simplicity and/or economy. In applying these techniques to the decoding problem the degree of simplicity and/or economy that may be attained is a function of the module configurations available, such as packing density, optimum number of inputs per gate, special matrix configurations of gates, etc.

One of the classical techniques employs a matrix. This method may be used to minimize the number of inputs per gate, but at the expense of increasing the number of gates. In logic configurations which are input limited, this technique may be the only economical solution to the problem. In pure diode logic systems (true AND functions) the technique actually produces more economical results.

In the DEC FLIP CHIP line, the R151 module performs a binary to octal conversion. That is, given both sides of three flip-flops, the module produces eight mutually exclusive outputs which represent the eight permutations of the three flip-flops. Figure 1 shows the truth table for the R151 Binary to Octal decoder.

Truth Table for R151 Binary to Octal Decoder (1 = —3v; 0 = 0v)

Inputs						Outputs							
H	J	F	E	L	K	0	1	2	3	4	5	6	7
2^2		2^1		2^0									
0	1	0	1	0	1	0	1	1	1	1	1	1	1
0	1	0	1	1	0	1	0	1	1	1	1	1	1
0	1	1	0	0	1	1	1	0	1	1	1	1	1
0	1	1	0	1	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	1	1	0	1	1	1
1	0	0	1	1	0	1	1	1	1	1	0	1	1
1	0	1	0	0	1	1	1	1	1	1	1	0	1
1	0	1	0	1	0	1	1	1	1	1	1	1	0

In addition to the six input lines for the complementary outputs of three flip-flops, there is one additional input which is a control line. When the control line is at 0 (0 volts), the decoder is enabled and functions according to the truth table. When at 1 (—3 volts), the decoder is disabled and all output lines produce a 1 regardless of input. Note that input pairs (HJ, FE, and LK) represent the 1 and 0 sides of a flip-flop respectively and that the zeros of the truth table on the output lines may be used for the assertion of each of the eight states of the three flip-flops.
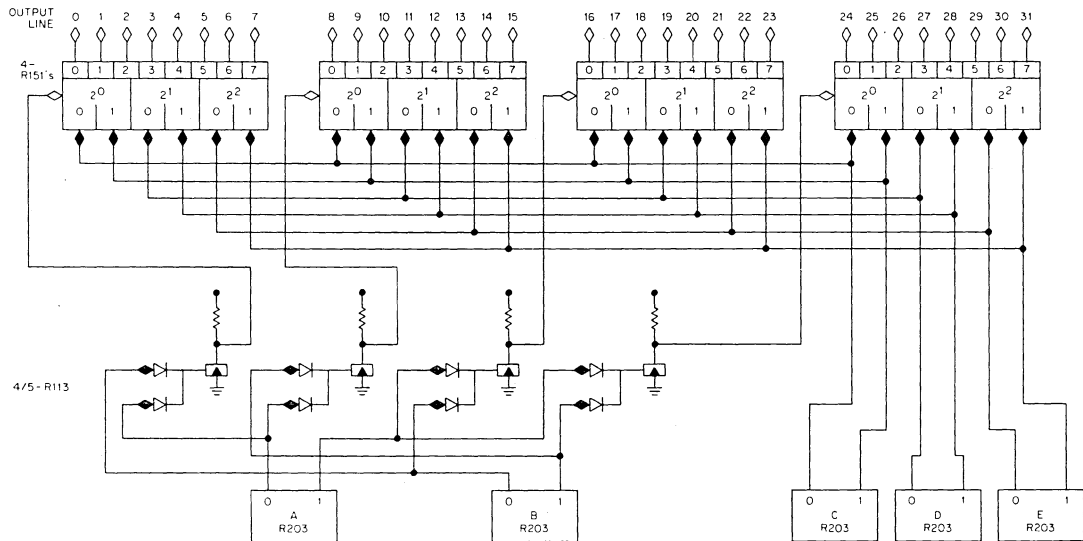
Figure 1 32-Position Decoder

The minimization technique applied in this case to make optimum use of the R151 module involves breaking the five bit binary number into two groups of three bits and two bits each. The least significant three bits may be considered one octal digit. If we now consider the two most significant bits we find that there are only four permutations of these bits. For each of these permutations, the least significant three bits may assume eight unique states for a total of 32 permutations which, of course, is the correct number of combinations of five bits.

To implement this technique, we use four R151's which all have parallel inputs from the least significant three bits. Thus, there will be four out of the 32 lines at ground for each of the eight combinations of the least significant three bits. All that remains now is to turn off three of the four active lines as a function of the most significant two bits. A two bit decoder made from four two-input gates will cause one out of its four output lines to be at ground for each of the four permutations of the two input bits. Remembering that the R151 inhibit inputs are enabled by a ground signal, the four unique ground outputs of the two bit decoder furnish the necessary four disabling signals for the four R151's.

PARTS LIST

	Type	Quantity	Description
Decoder	R151	4	Binary to Octal decoder
5-Bit Buffer	R203	2	3 Flip Flops

STEPPING MOTOR DRIVES (TRANSLATORS)

The W042 driver card was designed to handle a variety of high power driving applications, including stepping motors. Stepping motors come in a variety of types, but the two we will deal with here are the Superior Electric Slo-Syn (model SS50-1001) and the United Shoe Machinery Responsyn (model HDUM-16-100-161). The phasing of the pulses that drive the steppers is varied. Three different phasing requirements and simple methods for deriving them are described in this application note.

Most stepping motors have four leads plus a common lead. To make the motors step, a sequence of pulses on the four leads is required. Three of the desired pulse timings are shown in Figure 1. To reverse the direction of either motor, simply reverse the sequence of pulses.
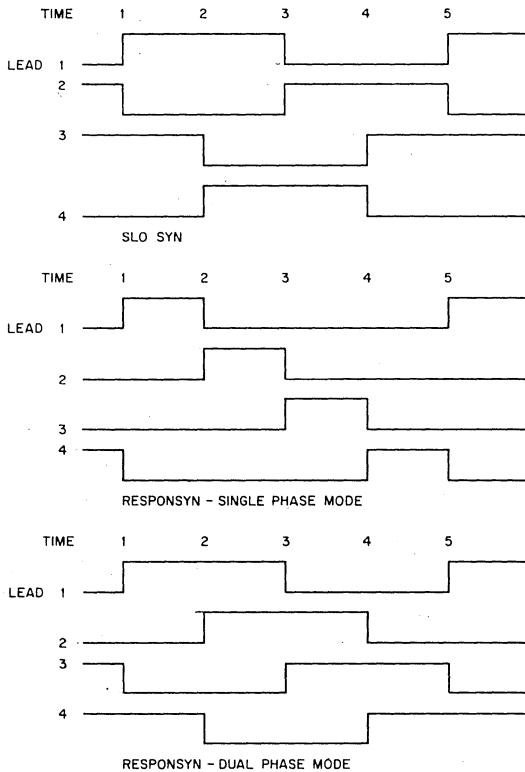
Figure 1 Pulse Timing for Stepping Motors (Positive Level means on)

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All of these timing sequences can be generated with two R201's in a switch tail ring counter configuration and the diode gate on the W042 driver card (two diodes per driver). The basic counter is shown in Figure 2.

COUNT	SEQUENCE (FWD)		SEQUENCE (REV)	
T	A	B	A	B
1	0	0	0	0
2	1	0	0	1
3	1	1	1	1
4	0	1	1	0
5	0	0	0	0
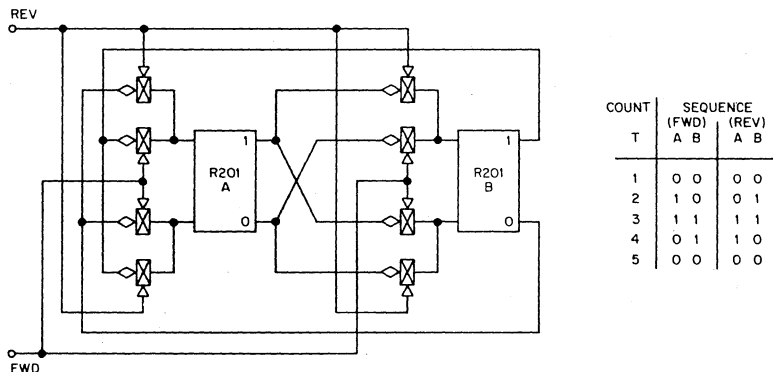
Figure 2 Basic Counter

By using the diode gating, the three different sequences shown in Figure 1 can be decoded from the one counter. Figures 3, 4, and 5 show the pulse sequences and logic diagram for each configuration. The decoding requirements have been simplified to one input per driver in the Slo-Syn and Responsyn single phase mode configurations.
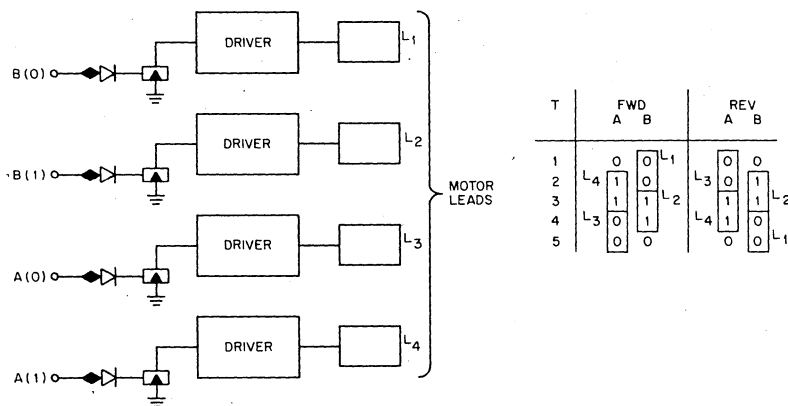
Figure 3 Slo-Syn Configuration

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T	FWD A	B		REV A	B	
1	0	0	L_1	0	0	L_1
2	1	0	L_2	0	1	L_4
3	1	1	L_3	1	1	L_3
4	0	1	L_4	1	0	L_2
5	0	0	L_1	0	0	L_1

Figure 4 Responsyn Single Phase Mode Configuration

Figure 5 Responsyn Dual Phase Mode Configuration

T	FWD A	B		REV A	B	
1		0	0 L_1	L_4	0	0
2	L_2	1	0		0	1 L_3
3		1	1 L_3	L_2	1	1
4	L_4	0	1		1	0 L_1
5		0	0		0	0

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The W042 driver board supplies current from —15v to the motor leads. Generally, some external resistance will be required. The Slo-Syn motor SS50-1001 is rated at 14 v and requires little to no external resistance. The time constant of the motor coils is smaller than its minimum pulse period and does not require external resistance to decrease it (only to insure proper motor dissipation).

The Responsyn HDUM-16-100-161, however, is a 4 v motor and has a time constant which is larger than the minimum pulse period. It requires the external resistance and higher supply voltage to insure maximum running rate. The values of external resistance depend upon the motor parameter and coil configuration. Two such configurations are shown in Figures 6 and 7. Also, the dissipation requirements of the W042 driver must be obeyed. See the W042 data sheet for use restrictions.
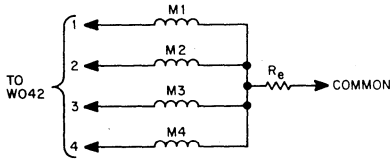
Figure 6 External Resistance for Slo-Syn and Responsyn (dual phase mode only)
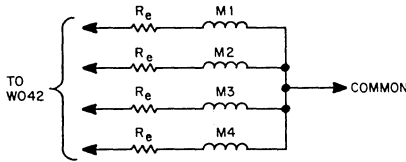
Figure 7 External Resistance for Responsyn (single phase or dual phase modes)

Stepping Motor Characteristics

Motor	DC Volts	Amps/Winding
Slo-Syn Motors		
SS50 -1010	2.0	3.3
SS50 -1009	5.5	1.3
SS50 -1008	8.0	0.85
SS50 -1001	14.0	0.53
SS150-1023	1.4	8.5
SS150-1009	2.5	4.0
SS150-1010	10.0	1.25
SS250-1006	2.5	5.0
SS250-1002	9.0	1.55

Responsyn Motor

HDUM-16-100-161	4	7.3

Slo-Syn SS150 series:

Static Holding Torque	310 oz.-in.
Resolution	1 part in 200 (1.8°)

Speed	50 s/sec	100 s/sec	150 s/sec	200 s/sec
Torque	156 oz. in.	125 oz. in.	100 oz. in.	62 oz. in.

Responsyn HDUM-16-100-161

Static Holding Torque	375 oz. in.
Resolution	1 part in 800 (0.4°)

Speed	200 s/sec	400 s/sec	800 s/sec
Torque	100 oz. in.	100 oz. in.	75 oz. in.

The Slo-Syn motor has a solid, conventional motor rotor, and hence a high inertia.

The Responsyn motor has a thin wall cup rotor with essentially negligible inertia.

PARTS LIST

Type	Quantity	Description
R201	2	Flip Flop (Translator)
W042	1	10-amp Driver (Driver/decoder)

In transmitting information digitally, it is often desirable to code it in such a way that a single bit of data is represented by a burst of pulses. Such techniques are useful in combatting noise and interference of the type encountered in sonar, radar, and high-frequency communications. Codes having special autocorrelation properties are widely used for this purpose. Receiving systems can be constructed which will produce an analog output whose shape is similar to the autocorrelation function of the coded signal. This analog output signal is developed as the code train passes through a filter which is "matched" to the coded sequence. The signal out of such a filter is usually a narrow pulse similar in shape to the single bit of information which was encoded originally.

BARKER CODE

One of the earliest codes used for this purpose was the Barker code, which was seven bits long. It is a bipolar signal as follows:

$$+1, +1, +1, -1, -1, +1, -1$$

A digital matched filter for receiving such a code could be implemented as shown in Figure 1. It will be observed that a signal coded in this fashion and having a peak amplitude of E will be compressed into a single spike having a peak amplitude of 7E.
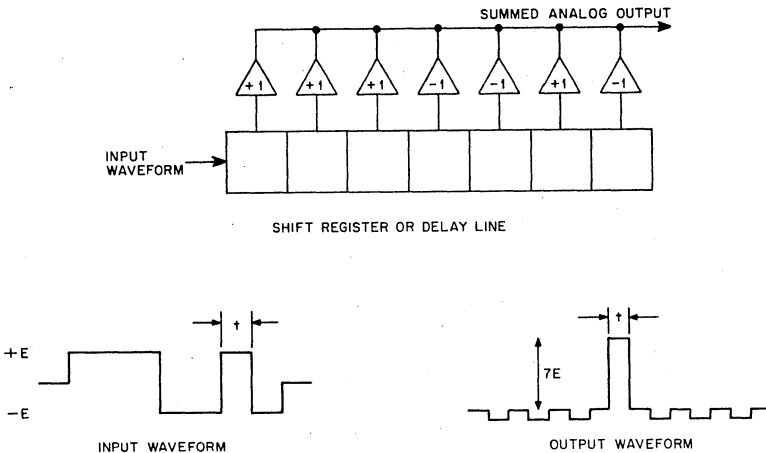

Figure 1 Barker Sequence

In addition, various sidelobe signals having an amplitude of E will be present. The width of both the main lobe and the side lobes is equal to t, the sub-interval used in the pulse sequence. In order to identify the position of the received bit of information in time, it is necessary to detect it at a threshold above the sidelobe level. The peak-to-sidelobe ratio is therefore a characteristic of some importance in the choice of a sequence for pulse compression. The Barker Code is one of a family of sequences having such properties. They are commonly referred to as maximal-length, or merely M-sequences. This reference is to the fact that a code of length 2^n 1 can be generated by using a shift register only n bits long. Because of the ease with which these codes can be generated and detected, they are becoming widely used in communications and control systems.

31-BIT SEQUENCE GENERATOR

Figure 2 shows a five-bit shift register and the necessary control electronics to generate a sequence which is 31 bits long. It is a slight modification of a ring counter in that it uses an exclusive OR condition of the state of the third and the fifth flip-flops to determine whether a 1 or a 0 is to be set into the first flip-flop on each shift operation. The state of the fifth flip-flop may be used to generate the code shown.

A filter matched to this sequence could be constructed either from a linear tapped delay line or its digital equivalent, a shift register. In either case, a resistive summing network could be used to produce an analog output which should be similar in shape to the autocorrelation function of the sequence. The following module list includes the modules necessary to construct an N-sequence generator and also a 31-bit shift register to receive it. The control electronics will include a clock which will sample the incoming waveform at a rate at least twice the bit rate used in sending the compressed signal.
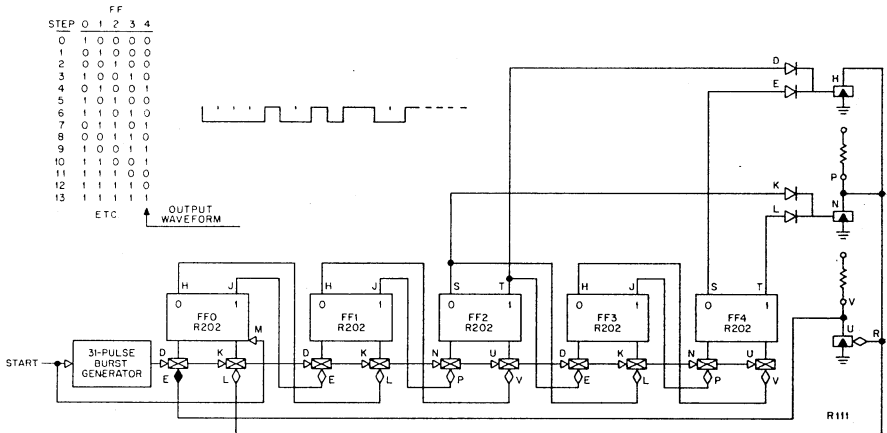

Figure 2 M-Sequence Generator

PARTS LIST

	Type	Quantity	Description
Shift Register	R202	3	2 Flip-Flops
	R111	1	3 Diode Gates
Burst-of-31	R202	3	2 Flip-Flops
	R302	1	2 Delays (oneshot)
	R602	1	2 Pulse Amplifiers
Matched Digital Filter	R202	17	2 Flip-Flops
	R401	1	Variable Clock

PART III: LOGIC LABORATORY

INTRODUCTION

The DEC Logic Laboratory is a low cost device for use in laboratory training, function breadboarding, and testing. When used in conjunction with the Logic Laboratory Workbook, a student who is not completely familiar with digital logic can quickly learn to construct operating logical networks and understand their function. In addition to the training function, the Logic Laboratory can be used to breadboard complex algorithms in order to verify the logic design prior to its inclusion in a system.

The Laboratory is also a very effective tool for testing individual logic modules as is evidenced by the fact that each DEC field service office uses a Logic Laboratory for computer module testing and maintenance.

The Logic Laboratory is a completely self-contained system consisting of a power supply, pulse generator, controls, indicators, mounting hardware, and a basic complement of logic modules necessary to construct a working system.

Education And Training

Flexibility is the key to the excellence of the Logic Laboratory as a training device. Far from a complicated do-it-yourself kit, the Laboratory is a well-conceived and implemented teaching aid. The Workbook provides a step-by-step approach to building an understanding of various digital logic functions. With only three module types, the student is taught to use the operations of NAND and NOR to perform the basic AND, OR, NOT, and EXCLUSIVE OR (Half add) functions. In the process of constructing these, the student learns by doing, as opposed to learning by rote.
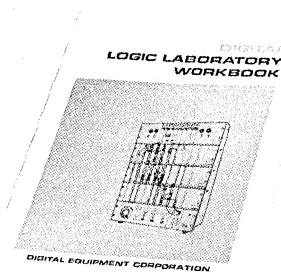
Experiments contained in the Workbook are designed so that experiments can be short and simple, or extended by the numerous possibilities suggested by additional problems contained in the Workbook. The Logic Laboratory is designed to teach universal logic principles rather than a narrow system, rigidly tied to a company's product line. The logic symbology used in the Workbook closely resembles the generally accepted standard. These symbols have been field-tested by leading training directors and found to be easily understood.
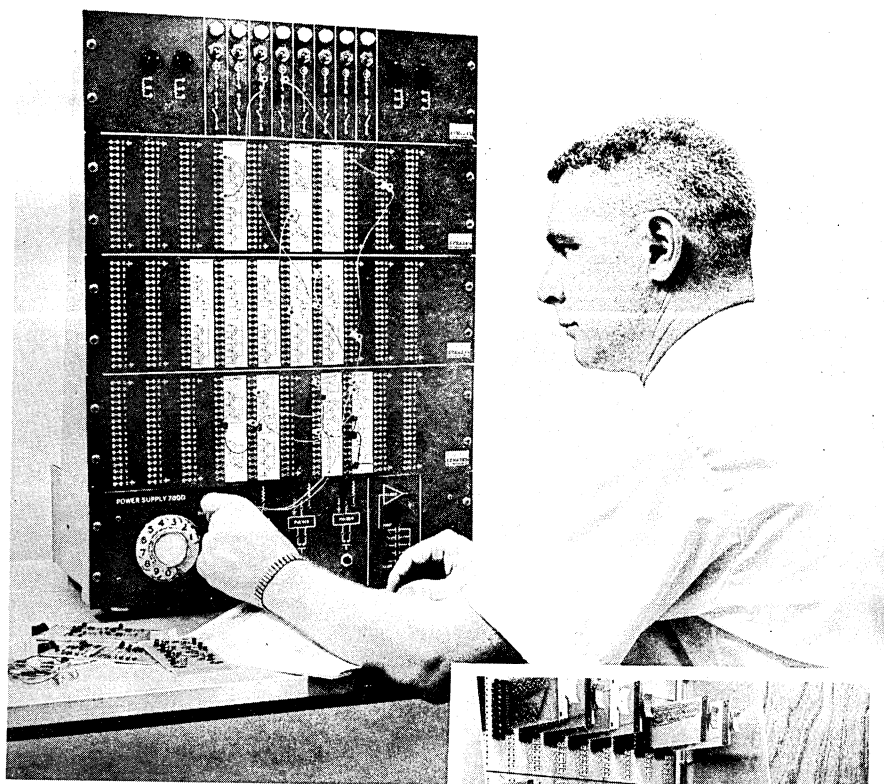
The Workbook was prepared specifically for use with the Logic Laboratory. It contains 15 graded experiments, or laboratory sessions, each of over three hours duration. No prior knowledge of electronics or digital logic is required, although the experiments should be performed in conjunction with a course in logic design or textbook study (a number of texts are recommended). All basic logic elements and techniques are covered, and all can be carried out with the basic Laboratory. Each chapter or laboratory session of the Workbook contains tutorial text and projects to be performed. A considerate amount of latitude is allowed in the assignment of projects, so that a given chapter can stimulate well over three hours of experimentation. The Workbook is also arranged so that various material may be omitted by the instructor, should he desire a less thorough coverage.

One of the most valuable features of the Logic Laboratory is its Analog-Digital Converter section. Two chapters are allocated to the techniques of analog to digital (ADC) and digital to analog (DAC) conversion. Since most of the measuring devices which exist today are analog in form, an understanding of the techniques and operation of A/D conversion equipment is absolutely necessary. In addition to the data acquisition problem, an understanding of the conversion of digital values to analog outputs for control and display (strip charts, meters, etc.) is essential for an overall understanding of data processing.

The following list of chapter titles indicate the scope of the material covered.

1.	Binary Numbers	9.	Binary Coded Decimal Arithmetic
2.	Binary Coded Decimal	10.	Code Conversion
3.	Basic Digital Circuits — Gates	11.	Control
4.	Flip-Flops and DCD Gates	12.	Timing
5.	From Boolean Equations to Gating Networks	13.	Introduction to Analog-Digital Conversion
6.	Boolean Equations and Flip-Flops	14.	Advanced Studies in Analog-Digital Conversion
7.	Addition		
8.	Parallel Addition and Subtraction	15.	Computer Design

The Standard Logic Laboratory contains the necessary equipment to perform experiments 1 through 10. The Advanced Logic Laboratory, when added to the Standard, contains the necessary equipment to perform experiments 11, 12, and 15. The Advanced Logic Laboratory with Analog-Digital Conversion provides the equipment for experiments 13 and 14.

Breadboarding And Testing

The Logic Laboratory is much more than a training device when used by a competent logic designer or technician. It is designed and manufactured to the same high quality as DEC modules and computers as well as being electrically and physically compatible with all Flip Chip modules. The Logic Laboratory power supply is capable of supplying drive to about 100 modules. There is no restriction on the size of the system which can be implemented since additional equipment can be ordered and Logic Laboratories interconnected directly. Many logic problems are complex enough to require assurance beyond the level of the Boolean equation before the final implementation. There is no substitute for actually building the system and verifying the logic using the Laboratory. The inherent flexibility and ease of interconnection modification results in a checkout time which is faster than building a complete prototype. The Laboratory is also very useful in building

A digital computer is an assemblage of extremely simple circuits. Consider the familiar elements in the logic laboratory — the toggle switches and push buttons. Examine these elements in detail. Compare them.

Each has only two states. The switch may be up or down. The button may be depressed or released. Digital circuits also have two states, a negative voltage level and a positive level. In the logic laboratory the negative level is —3 volts; the more positive level is ground.

Note the differences. The button makes contact only when depressed. When released, it always returns to its original position. The switch, by contrast, always remains where last positioned. It remembers. In this same sense, digital circuits are divided into two classes, those which remember and those which follow.

A BINARY COUNTER

In this experiment, you will study the binary number system by constructing a counter, using the Flip-Flop Type R201. The flip-flop is the circuit equivalent of the toggle switch. It remembers.

The flip-flop circuit is shown symbolically in Figure 1. The two outputs are always in opposite states. That is, if one output is at – 3 volts, the other is at ground and vice versa. To see this, connect the two flip-flop outputs to indicator lights. One will be on while the other is off.

To change the state of the flip-flop, connect a push-button pulser to each of the direct inputs. Notice that the flip-flop always re-members which button was depressed last.
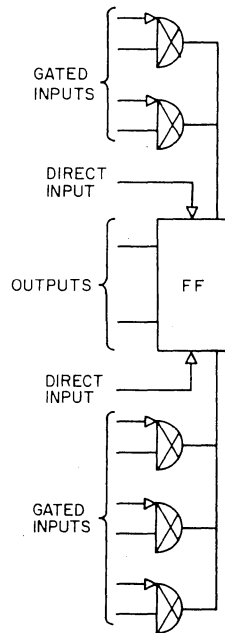
"one of a kind" systems for experimentation when the system is used for a single pass operation.

Some common uses of the Logic Laboratory are listed below. Many of these are described in detail near the back of this catalog under the heading Application Notes. The uses to which the Laboratory can be put are without limit. Digital's highly trained field engineers are always available to assist customers with logic design problems.

Peak Amplitude and Zero
  Crossing Measurements
Computer Controlled
  Communications Systems
Generation of Pseudo-Random
  Sequences
Digital Filtering of Analog Signals
Highly Accurate Timing Systems
Stepping Motor Drives (Translators)
Teletype Send-Receive Logic
Real-Time Computer Interfaces

General Purpose Digital Clocks
Analog Signal Multiplexing
Decoding
Sequence Control
Data Acquisition
Hybrid Computation
Pulse Train Techniques
Typewriter Drive Logic
Voltage-Time Conversion
Digital Spectrum Analyzers
Elapsed Time Measurements

Basic Equipment Lists

STANDARD LOGIC LABORATORY

The following equipment is sufficient to study the basic principles of digital logic, as set forth in Experiments 1 through 10 in the Logic Laboratory Workbook. Total price is $845.30

1	H901	Module Mounting Panel
1	H902	Indicator-Switch Panel (complete with WO52 module)
6	R201	Flip-Flops
3	R121	Four NOR Gates
1	R122	Four NAND Gates
4	911-2″	Box of 2″ Patch Cords
5	911-4″	Box of 4″ Patch Cords
2	911-8″	Box of 8″ Patch Cords
1	911-16″	Box of 16″ Patch Cords
1	700D	Power Supply and Signal Generator Panel (with modules)
1	4913	Mounting Rack

ADVANCED LOGIC LABORATORY

Added to the standard equipment above, the following items permit the study of control, timing, and computer design, as covered in Experiments 11, 12, and 15 of the Workbook. Price of added equipment is $311.50. Total price is $1156.80

1	H901	Module Mounting Panel
3	R201	Flip-Flops
1	R121	Four NOR Gates
2	R302	Two Delay One-Shots
1	R602	Two Pulse Amplifiers
1	911-4″	Box of 4″ Patch Cords
1	911-8″	Box of 8″ Patch Cords
1	911-16″	Box of 16″ Patch Cords
1	911-32″	Box of 32″ Patch Cords

## ADVANCED LOGIC LABORATORY WITH ANALOG-DIGITAL CONVERSION

The converter listed below opens up the large and varied field of interfacing digital logic with external analog equipment. As described in Experiments 13 and 14 of the Wookbook, analog-to-digital converts can convert analog outputs from thermometers, pressure gauges, flowmeters, etc. into digital values for processing, and digital-to-analog converters can convert the resulting digital numbers into analog signals to control devices such as motors, oscilloscopes, and valve actuators. Converter price $143.00. Total price is $1299.80

1	H903	Analog-Digital Conversion Panel (Provides D to A and A to D Conversion. Complete with modules)

POWER SUPPLIES AND INPUT PANEL
TYPES 700D, 700DA

LOGIC LABORATORY COMPONENTS
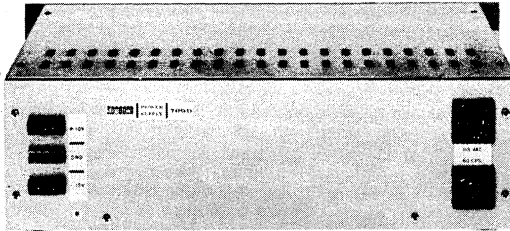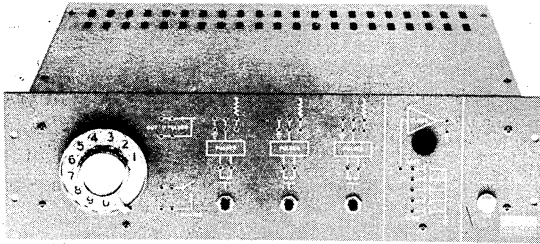
The 700D is a combination power supply and input panel. The input devices include a dial, three push buttons and pulsers, and a clock. The power supply can drive approximately ten Type H901 Panels of R-series FLIP CHIP logic, or up to 10 basic Logic Laboratories. Details on the pulser circuits are given in the module description of the Type W501. Details on the clock are given on the module description of the Type R401. The 700D is a combination of the 900 Control Panel plus an H701 Power Supply.

ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE: Power Supply — 700D: 115v, 60 cps, 700DA: 112.5, 123.5, 195, 220, 235v, 50 cps. See "50 cps power."

OUTPUT VOLTAGE: ±10v, −15 vdc, floating

OUTPUT CURRENT: +10v: 0 to 0.4 amp; −15v: 0.5 amp to 3 amp.

LINE AND LOAD REGULATION: The output voltage remains between −15.5 and −16.5v for the −15v output and within +9.2 and +11.5v for the +10v output, when load varies from minimum to maximum and line voltage varies from 105 to 125 vdc.

P-P RIPPLE: Less than 0.6v. for +10v output; less than 0.6v for −15v output (20% more ripple on the 50-cps type).

LINE FREQUENCY TOLERANCE: ±2% of line frequency

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19 in.

PANEL HEIGHT: 5-3/16 in.

DEPTH: 12 in.

FINISH: Chassis: Chromicoat; Panel: DEC Blue
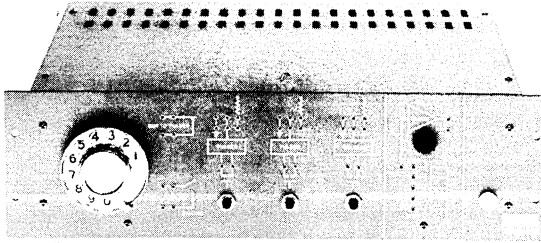
POWER UNIT CONNECTION: Amphenol 160-5 Socket

POWER OUTPUT CONNECTION: Hayman Tab Terminals which fit AMP "Faston" receptacle series 250, part 41774 or Type 914 Power Jumpers.

700D	— $288.00
700DA	— $308.00

The Type 900 Control Panel uses the same chassis and input controls as the 700D but does not contain a power supply. It is designed for multi-student installations of DEC Logic Laboratory units powered by a single 700D Power Supply. Connections are available on the rear of the 900 to accept power from the master 700D Power Supply.

The input devices include a dial, three pulsers with pushbuttons, and a variable clock. Details of the Type W501 Pulser Circuits and the Type R401 Clock can be found in the module description section of the catalog.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19 in.
PANEL HEIGHT: 5-3/16 in.
DEPTH: 12 in.
FINISH: Chassis: Chromicoat; Panel: DEC Blue
AC POWER CONNECTION: Amphenol 160-5 Socket

is provided, but not wired
DC POWER INPUT CONNECTION: Hayman Tab Terminals which fit AMP "Faston" receptacle series 250, part 41774 or Type 914 Power Jumpers.

900 — $214.25

MISCELLANEOUS ACCESSORIES
TYPES H901, 911
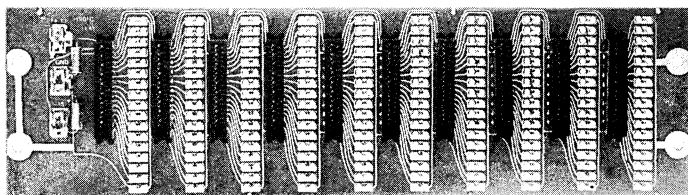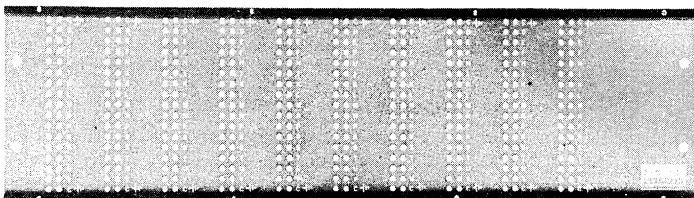
H901 PATCHCORD MOUNTING PANEL

This panel provides up to ten FLIP CHIP modules with power and patch connections. Space between patching sockets allows insertion of logic diagrams. Logic diagrams are printed on all FLIP CHIP module data sheets. More permanent plastic diagrams are available for those modules required to complete the logic laboratory workbook experiments.

PANEL WIDTH: 19 in.

PANEL HEIGHT: 5-3/16 in.

DEPTH: 6½ in. with FLIP CHIP modules inserted

FINISH: DEC Blue

POWER INPUT CONNECTIONS: Tabs which fit AMP "Faston" receptacle series 250, part 41774.

911 PATCHCORDS

DEC Type 911 Banana-Jack Patchcords are supplied in color-coded lengths of 2 in. (brown), 4 in. (red), 8 in. (orange), 16 in. (yellow), 32 in. (green), and 64 in. (blue). Patchcords may be stacked to permit multiple connections at any circuit point on the graphic panels of the DEC H901 Mounting Panel. The cords are supplied in snap-lid plastic boxes of ten for handy storage.
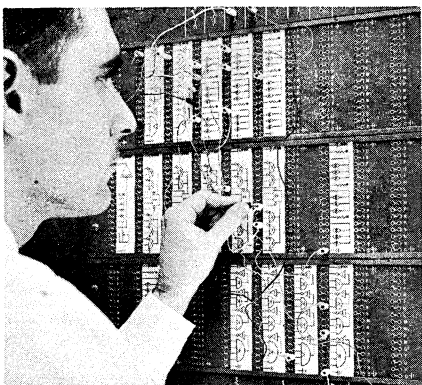
H901 — $82.50
911 — $9.00/pkg. of 10

INDICATOR SWITCH PANEL
TYPE H902
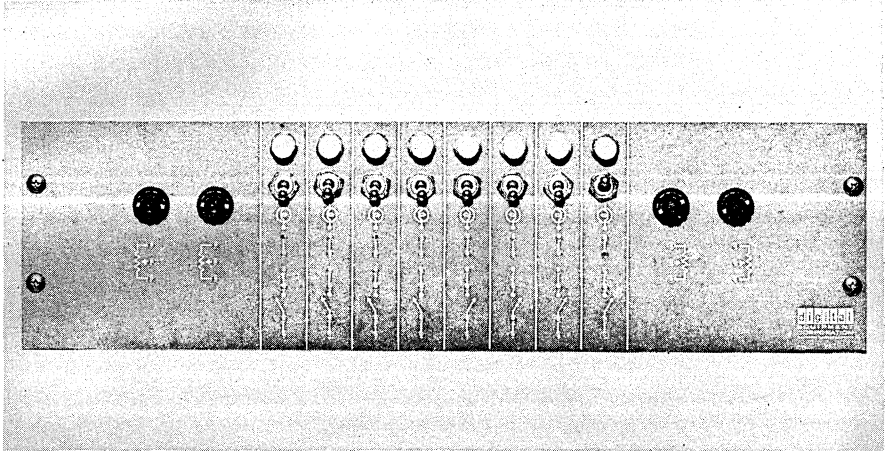
The H902 Panel provides facilities for control and observation of the Logic Laboratory. It contains eight indicator lights and a lamp driver module, eight toggle switches and four potentiometers. Connections to these devices are made with Type 911 Stacking Banana-Jack Patchcords.

INDICATORS: Indicators inputs accepts signals of —3v and ground. A ground input lights the indicator. If the input is returned to —3v or open circuited, the indicator will not light. The load is 1 ma.

TOGGLE SWITCHES: The toggle switches are single pole, single throw with a logic diagram to show the open and closed positions.

POTENTIOMETERS: The potentiometers are 20,000 ohms. They may be used to control the frequency of delay one-shots or clock circuits in the H901 Mounting Panel.
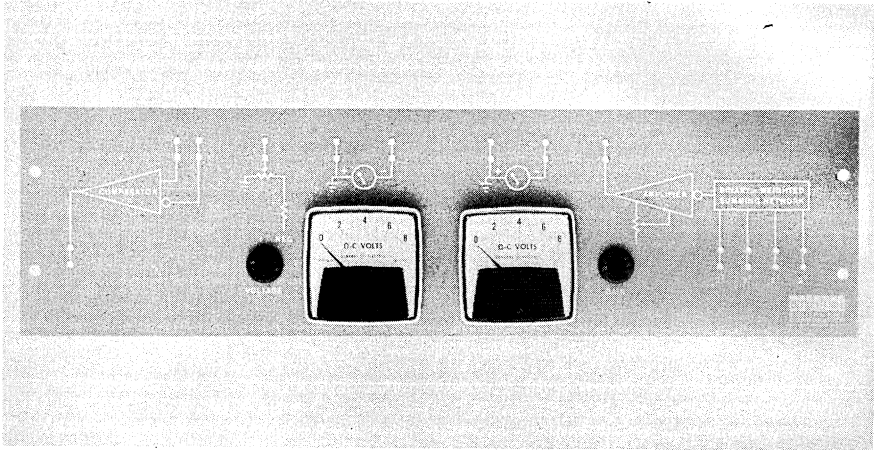
MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19 in.
PANEL HEIGHT: 5-3/16 in.
DEPTH: 6½ in.

FINISH: DEC Blue
POWER INPUT CONNECTIONS: Tabs which fit AMP "Faston" receptacle series 250, part 41774.

H902 — $112.80

ANALOG-DIGITAL PANEL
TYPE H903

LOGIC LABORATORY COMPONENTS

This panel provides facilities for experimenting with analog-digital techniques. It contains a 4 bit variable output D-A converter and a comparator circuit. Also includes two 8 volt panel meters and a potentiometer for producing 0 to —8v test signal. Connections to these devices are made with Type 911 Stacking Banana-Jack Patchcords.

ELECTRICAL CHARACTERISTICS

D-A CONVERTER ZERO OFFSET: ±0.4v or less

LINEARITY: ±3% of full scale

ALL ONES OUTPUT (FULL SCALE): adjustable from —7v to —8v driving 3000 ohm load

D-A CONVERTER OUTPUT IMPEDANCE: typically less than 100Ω

COMPARATOR OFFSET: ±0.2v or less

COMPARATOR INPUT CURRENT: typically less than 100 μa.

INPUT VOLTAGE OPERATING RANGE: 0 to —10v

INPUT: D-A converter inputs each require 1 ma at ground. No load at —3v.

OUTPUT: D-A converter output may be shorted to ground accidentally without harm. Comparator output supplies up to 8 ma at ground; 1 ma at —3v. Because the inputs may pass through the switching region slowly or hesitantly in most A-D converter applications, the comparator output transition is not suitable for driving DCD gate pulse inputs.

POWER: +10 v(A)/8 ma; —15 v/30 ma.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19 in.
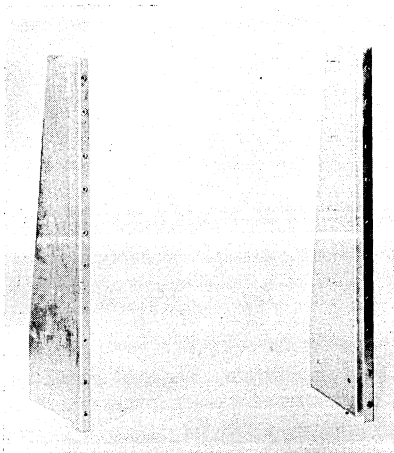PANEL HEIGHT: 5-3/16 in.
DEPTH: 6½ in. with FLIP CHIP modules inserted

FINISH: DEC Blue
POWER INPUT CONNECTIONS: Tabs which fit AMP "Faston" receptacle series 250, part 41774.

H903 — $143.00

4913 MOUNTING RACK

The 4913 Mounting Rack provides support for a 700D Power Supply and up to four H901 Patchcord Mounting Panels, for a total of up to 40 FLIP CHIP modules ready to be patched together for experiments. It may also be used to mount general purpose mounting panels such as the 1943 for use with the H700 Power Supply. The power supply must be mounted at the bottom for stability.

Height: 26¼ in.

Threads for mounting panels: 10-32

914 POWER JUMPERS

For interconnections between power supplies, mounting panels, and logic lab. Panels these jumpers use AMP "Faston" receptacles series 250. Specify 914-7 for interconnecting adjacent mounting panels, or 914-19 for other runs of up to 19 inches. 914-7 contains 10 jumpers; 914-19 contains 5.

4913	—	$10.00
914-7	—	$ 4.00
914-19	—	$ 4.00

ORDER FORM

DIGITAL
LOGIC
LABORATORY
WORKBOOK
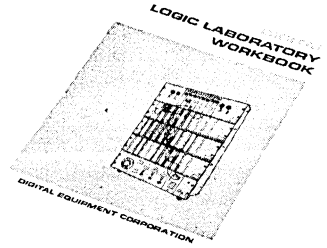
DIGITAL EQUIPMENT CORPORATION
Technical Publications Dept.
146 Main Street
Maynard, Mass. 01754

GENTLEMEN: Please send me_____copy(s) of The DIGITAL LOGIC LABORATORY
WORKBOOK B-250 at $5.00 per copy postpaid.

Enclosed is my check or money order for $_____

Name_____Title_____

Company_____

Street_____

City_____State_____Zip Code_____

Type of Business_____

☐ I would like a demonstration of the Logic Laboratory. Please have a salesman call.

(left margin, vertical text) CUT ALONG DOTTED LINE

PART IV: HARDWARE, OCTAIDS AND PANELAIDS

INTRODUCTION

Digital manufactures a complete line of hardware accessories in support of its module series. Module connectors are available for as few as one module and as many as 64. A complete line of cabinets is available to house the modules and their connector blocks, as well as providing a convenient means for system expansion. Power supplies for both large and small systems as well as marginal check and reference supplies are also available.

A major new addition to the hardware line is the H201 Core Memory. The H201 gives the logic designer the capability of designing a complete random access storage system for off-line storage, programming automatic equipment, or controlling of a general-purpose computer.

Coupled with the recent additions to the hardware line, Digital has made every effort to maintain or improve the high standards of reliability and performance of its present line. Through the availability of a wide range of basic accessories, DEC feels that it is offering the logic designer the necessary building blocks which he requires for complete system design.

MARGINAL CHECKING

The use of variable output power supply Type 786 and marginal check switches on the mounting panels allow preventive maintenance routines to be established on systems that must not become inoperative without warning, even after years of use. Varying the power supply voltages is an excellent way to determine the safety margins and can also help in pinpointing a logic design or wiring mistake that causes baffling sporadic errors with normal voltage applied. All systems built by Digital are tested under conditions of varying $+10$ and -15 supply voltages before shipment, and standard practice on large computers is to make margin checks at regular intervals, to detect any deteriorating components before they threaten an unscheduled shutdown.

50-CYCLE POWER

Because of the demand for Digital's products in areas where 115-v, 60-cps power is not available, each of the power supplies with a frequency-sensitive regulating transformer is also available in a multi-voltage 50-cps version. All 50-cps supplies have the same input connections. The line input is on pins 3 and 4. Jumpers should be connected depending on the input voltage. These connections are shown below along with a schematic.

WIRING HINTS

These suggestions may help reduce mounting panel wiring time. They are not intended to replace any special wiring instructions given on individual module data sheets or in application notes. For fastest and neatest wiring, the following order is recommended.

(1) All power wiring (pins A, B, and C) and any horizontally bussed signal wiring. Use Horizontal Bussing Strips Type 932.

(2) Vertical grounding wires interconnecting each chassis ground with pin C grounds. Start these wires at the uppermost mounting panel and continue to the bottom panel. Space the wires 2 inches apart, so each of the chassis-ground pins is in line with one of them. Each vertical wire makes three connections at each mounting panel.

(3) All other ground wires. Always use the nearest pin C above the pin to be grounded, unless a special grounding pin has been provided in the module.

(4) All signal wires in any convenient order. Point-to-point wiring produces the shortest wire lengths, goes in the fastest, is easiest to trace and change, and generally results in better appearance and performance than cabled wiring. Point-to-point wiring is strongly urged.

The recommended wire size for use with the H800 mounting blocks and 1943 mounting panel is 24 for wire wrap, and 22 for soldering. The recommended size for use with H803 block and H911 mounting panel is #30 wire. Larger or smaller wire may be used depending on the number of connections to be made to each lug. Solid wire and a heat resistant spaghetti (Teflon) are easiest to use when soldering.

Adequate grounding is essential. In addition to the connections between mounting panels mentioned above, there must be continuity of grounds between cabinets and between the logic assembly and any equipment with which the logic communicates.

When soldering is done on a mounting panel containing modules, a 6-v (transformer) soldering iron should be used. A 110-v soldering iron may damage the modules.

When wire wrapping is done on a mounting panel containing modules, steps must be taken to avoid voltage transients that can burn out transistors. A battery- or air-operated tool is preferred, but the filter built into some line-operated tools affords some protection.

Even with completely isolated tools, such as those operated by batteries or compressed air, a static charge can often build up and burn out semiconductors. In order to prevent damage, the wire wrap tool should be grounded except when all modules are removed from the mounting panel during wire wrapping.

AUTOMATIC WIRING

Significant cost savings can be realized in quantity production if the newest automatic wiring techniques are utilized. Every user of FLIP CHIP modules benefits from the extensive investment in high-production machinery at Digital, but some can go a step further by taking advantage of programmed wiring for their FLIP CHIP digital systems.

While the break-even point for hand wiring versus programmed wiring depends upon many factors that are difficult to predict precisely, there are a few indications:

1. One-of-a-kind systems will probably not be economical with automatic wiring, even when the size is fairly large; programming and administrative costs are likely to outweigh savings due to lower costs in the wiring itself.

2. At the other end of the spectrum, production of 50 or 100 identical systems of almost any size would be worth automating, not only to lower the cost of the wiring itself but also to reduce human error. At this level of volume, machine-wired costs can be expected to be less than the cost of hand wiring.

3. For two to five systems of several thousand wires each, a decision on the basis of secondary factors will probably be necessary: ease of making changes, wiring lead time, reliability predictions, and availability of relevant skills are factors to consider.
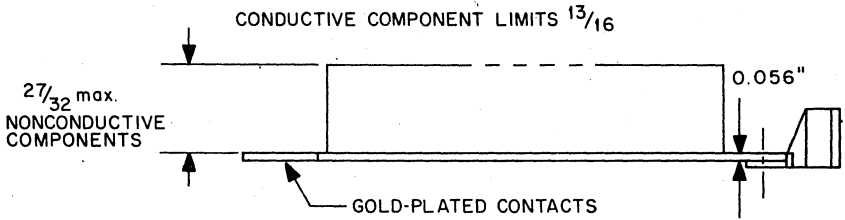
The Gardner-Denver Corporation, and Digital can supply further information to those interested in programmed wiring techniques. At Digital, contact the Module Sales Manager, Sales Department.
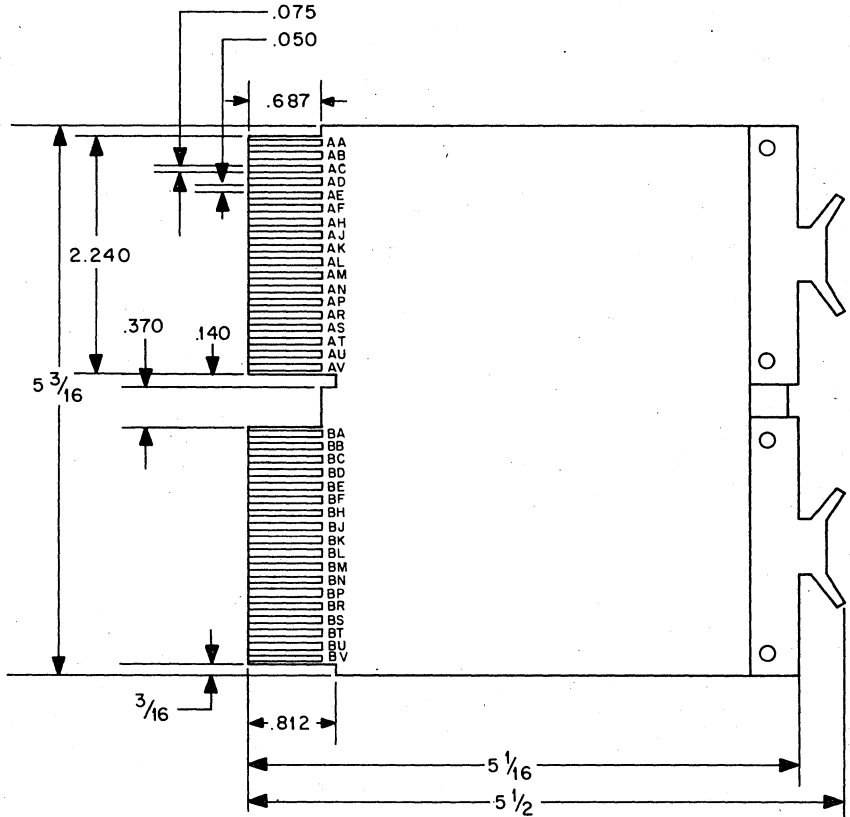

COOLING OF FLIP CHIP MODULES

The low power consumption of R-series modules results in a total of only about 25 watts dissipation in a typical 1943 Mounting Panel with 64 modules. This allows up to six panels of R-series modules to be mounted together and cooled by convection alone, if air is allowed to circulate freely. In higher-dissipation systems using modules in significant quantities from the W, B, and A series, the number of mounting panels stacked together must be reduced. For example, no more than three panels of B-series modules may be mounted together without forced-air cooling. In general, total dissipation from all modules in a convection-cooled system should be 150 watts or less (about 9-amp total current at —15v).

The regulating transformers used in most DEC power supplies have nearly constant heat dissipation for any loading within the ratings of the supply. Power dissipated within each supply will be roughly equal to half its maximum rated output power. If power supplies are mounted below any of the modules in a convection-cooled system, this dissipation must be included when checking against the 150 watt limit.

STANDARD MODULE SIZES

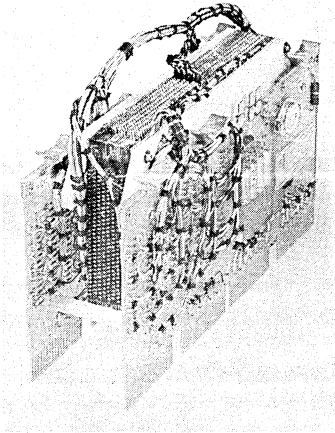SINGLE-WIDTH FLIP CHIP MODULE

CONDUCTIVE COMPONENT LIMIT $^{11}/_{32}$

NONCONDUCTIVE COMPONENTS $^3/_8$ max.

0.056"

$^1/_{16}$ MAXIMUM HEIGHT
OF SOLDERED
COMPONENT LEADS

GOLD-PLATED CONTACTS

ETCHED WIRING SURFACE

SINGLE-HEIGHT FLIP CHIP MODULE

$\sim ^1/_2{}''$

.687

A
B
C
D
E
F
H
J
K
L
M
N
P
R
S
T
U
V

$2^7/_{16}$ 2.240

.050

.075

.812

$5^1/_{16}$

$5^1/_2$

299

DOUBLE-WIDTH FLIP CHIP MODULE

CONDUCTIVE COMPONENT LIMITS $^{13}/_{16}$

0.056"

$^{27}/_{32}$ max.
NONCONDUCTIVE
COMPONENTS

GOLD-PLATED CONTACTS

DOUBLE-HEIGHT FLIP CHIP MODULE

.075

.050

.687

AA
AB
AC
AD
AE
AF
AH
AJ
AK
AL
AM
AN
AP
AR
AS
AT
AU
AV

2.240

.370   .140

$5\,^3/_{16}$

BA
BB
BC
BD
BE
BF
BH
BJ
BK
BL
BM
BN
BP
BR
BS
BT
BU
BV

$^3/_{16}$

.812

$5\,^1/_{16}$

$5\,^1/_2$

The H201 Core Memory can store 4096, 13-bit words. By combining with other modules, a complete random access memory storage system with a cycle time of 8 μs can be built. This system may be used to provide off-line data storage, program automatic equipment, or control a general-purpose computer.

SPECIFICATIONS

ADDRESS:	4096	RISE TIME:	0.5 μs nominal
BITS:	13	$_u V_1$ (UNDISTURBED "1"):	50 mv typical
ORGANIZATION:	4 wire, 3D	$_d V_Z$ (DISTURBED "0"):	8 mv typical
SELECTION:	2 diodes per line, 8x8 "X" matrix, 8x8 "Y" matrix	PEAKING TIME:	0.7 us typical
		PHYSICALLY:	Occupies 24 module locations, 4 vertically by 6 horizontally. Note mounting panels must be aligned to permit core to plug in.
1/2 SELECT CURRENT:	200 ma nominal		
SELECTION PULSE WIDTH:	2 μs nominal		

H201 — $2,000.00

301

DUAL POWER SUPPLY
TYPE H704
±15 VOLTS
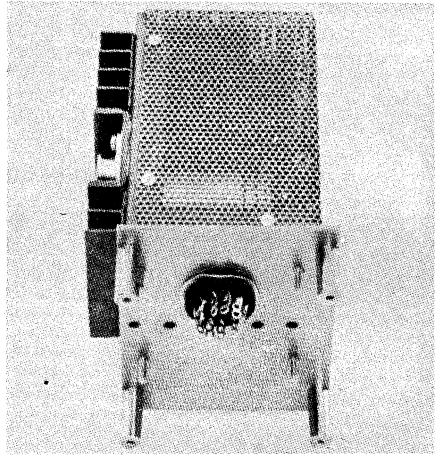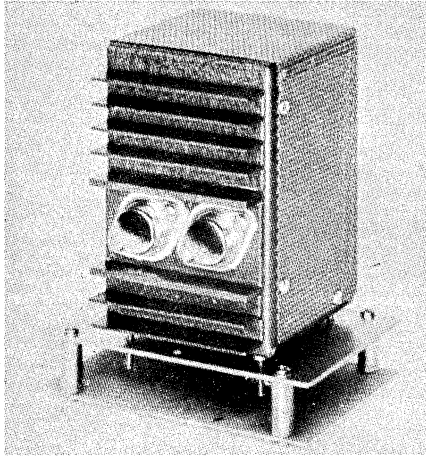
The Type H704 Power Supply (±15v) is a precision unit designed to supply the voltage requirements for up to six operational amplifier modules. It is an all silicon modular supply capable of delivering 400 ma on both outputs. Remote sensing terminals are provided.

The H704 is supplied with all the hardware required for computer cabinet, 1943, or H900 mounting. When the H704 is installed in a 1943 or H900 Mounting Panel, it takes the place of two module connector blocks.

MECHANICAL CHARACTERISTICS

DIMENSIONS: 3¼ x 3⅜ x 5 in. height
CONNECTIONS: All input-output wires must be soldered to octal socket at the base of the power supply.
OPERATING TEMPERATURE: —20 to +71°C ambient

ELECTRICAL CHARACTERISTICS
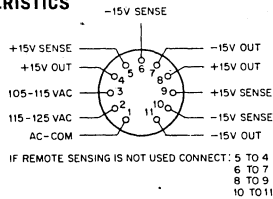
INPUT VOLTAGE: 105 to 125 vac; 47-420 cps.
OUTPUT VOLTAGE: floating ±15v at 400 ma
OUTPUT VOLTAGE ADJUSTMENT: ±1v each output
REGULATION: 0.05% line, 0.1% load for both voltages
RIPPLE: 1 mv rms max for both outputs
OVERLOAD PROTECTION: The power supply is capable of withstanding output short circuits indefinitely without being damaged.

-15V SENSE

+15V SENSE — — -15V OUT
+15V OUT — — +15V OUT
105-115 VAC — 3   9 — +15V SENSE
115-125 VAC — — -15V SENSE
AC-COM — — -15V OUT

IF REMOTE SENSING IS NOT USED CONNECT: 5 TO 4
6 TO 7
8 TO 9
10 TO 11

IF REMOTE SENSING IS NOT USED, CONNECT: 5 TO 4
6 TO 7
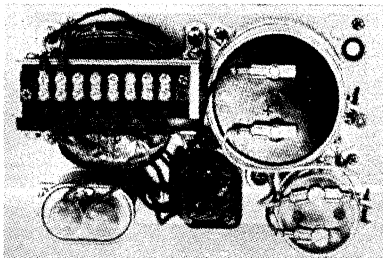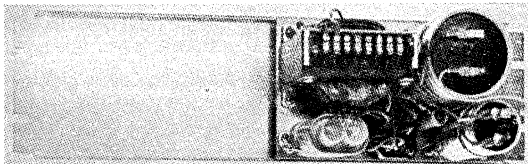
H704 — $200.00

POWER SUPPLIES
TYPES H701, H701A, 782, 782A
+10, −15 VOLTS

TYPE H701 DESIGNED FOR PLENUM OR COMPUTER CABINET MOUNTING

TYPE 782 DESIGNED FOR 19 INCH RACK MOUNTING

The 782 and 782A power supplies are ruggedly built, low cost units that fit into a standard 19-inch rack. The H701 and H701A are identical to these units, except they can be mounted on a chassis or panel in applications where space is added to an existing device. The basic supply can be mounted in various configurations and is identical to the power supplies used in models 700D and H900. The Types 782A and H701A are Power Supplies with 50 Hertz transformers.

ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE: H701: 115 v 60 cps. H701A: 112.5, 123.5, 195, 220, 235 v, 50 cps. See "50 cps power"

OUTPUT VOLTAGE: +10 v, −15 vdc, floating

OUTPUT CURRENT: −15 v: ½ to 3 amp; +10 v: 0 to 0.4 amp.

LINE AND LOAD REGULATION: The output voltage remains between −14.5 and −16.5 v for the −15

output, and within + 9.2 and +11.5 v for the +10 output, when load varies from minimum to maximum and line voltage varies ±10%.

P-P RIPPLE: Less than 0.6 v for +10 output. Less than 0.6 v for −15 output; 20% more ripple on the 50-cps type.

LINE FREQUENCY TOLERANCE: ±2% of line frequency.

MECHANICAL CHARACTERISTICS

LENGTH: 8″

WIDTH: 4-15/16″

HEIGHT: 5¾″

FINISH: Chromicoat

POWER CONNECTIONS: Screw terminals are provided on transformer for input power connections. Output power connections are made via tab terminals which fit the AMP "Faston" receptacle series 250, part #41774 or Type 914 power jumpers. All required mounting hardware is supplied with this unit.
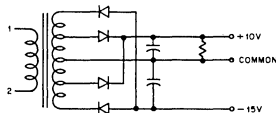
H701	— $116.00
H701A	— $136.00
782	— $128.00
782A	— $148.00

POWER SUPPLY
TYPE H710

The H710 power supply is a ruggedly built, low cost, regulated, floating output, five volt power supply that can be mounted in an H920 chassis drawer or used as a free standing unit. Remote sensing to correct for loss due to long lines is provided. When shipped from the factory, the remote sensing inputs are jumpered to their respective outputs.

ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE:
105-125 VAC or 210-250 VAC 47-63 HZ
OUTPUT VOLTAGE:
5 vdc.
OUTPUT CURRENT:
0-5 amps. short-circuit protected for parallel supply operation.

LINE AND LOAD REGULATION:

The output voltage will not vary more than 50 mv over the full range of load current and line voltage.

P-P RIPPLE:

Less than 20 mv.

OVERVOLTAGE PROTECTION:

The output is protected from transients which exceed 6.9 Volts for more than 10nsec. However, the output is not protected against long shorts to voltages above 6.9 Volts.

MECHANICAL CHARACTERISTICS

Length: 8"
Width: 5"
Height: 6"
Finish: Chromicoat

POWER CONNECTIONS:
Input power connections are made via tab terminals which fit the AMP "Faston" receptacle series. Output power is supplied to solder lugs. All required mounting hardware is supplied with this unit.
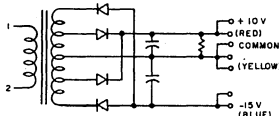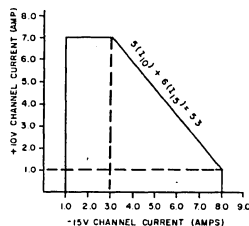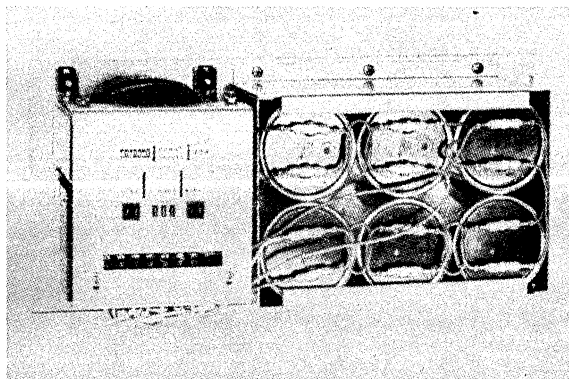
H710—$200.00

POWER SUPPLIES
TYPES 728, 728A
+10, −15 VOLTS

DESIGNED FOR COMPUTER CABINET MOUNTING

The Types 728 and 728A (+10, −15 v) Power Supplies are capable of withstanding wide line and load variations for general system use. When used singly, the 10-v channel can supply 0 to 7.5 amp, or the 15-v channel can supply 1.0 to 8.5 amp. The 728 Power Supply is electrically identical to the 783 but is made on a shorter chassis specifically designed for mounting on the plenum door of a DEC computer cabinet.

ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE: 728: 115 v, 60 cps, 728A: 112.5, 123.5, 195, 220, 225 v, 50 cps. See "50 cps power"

OUTPUT VOLTAGE: +10 v, −15 vdc, floating.

OUTPUT CURRENT: 1) When only one output is loaded: +10 v: 0 to 7.5 amp −15 v: 1.0 to 8.5 amp. 2) When both outputs are loaded: +10 v: 0 to 7 amp* −15 v: 1.0 to 8.0 amp.* At least 1.0 amp must be drawn from the −15 v channel to assure proper load regulation.

LINE AND LOAD REGULATION: The output voltage remains between −14.5 to −16.5 v for the −15 v channel and within +9.5 to +11.5 v for the +10 v channel, when load varies from minimum to maximum and line voltage varies from 105 to 125 vac.

P-P RIPPLE: Less than 0.7 v for +10 v output; less than 0.7 v for −15 v output (20% more ripple on the 50 cps type).

LINE FREQUENCY TOLERANCE: ±2% of line frequency.

*The sum of the output currents is limited by the following equation: $5(I_{10}) + 6(I_{15}) = 53$ (see Figure).

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 16⅝ in.

PANEL HEIGHT: 8¾ in.

DEPTH: 5⅜ in.

FINISH: Chromicoat.
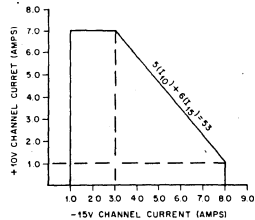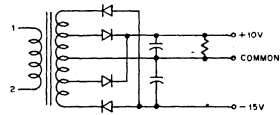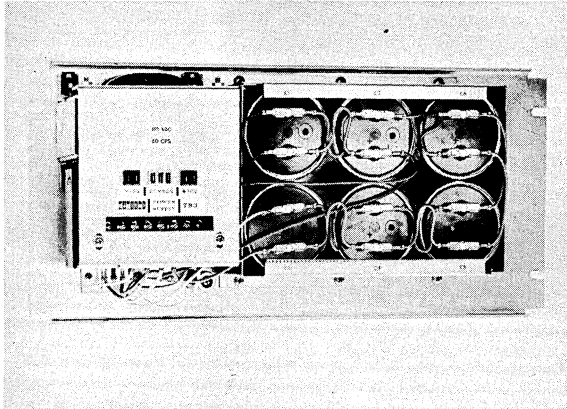
POWER INPUT CONNECTION: Screw terminals on transformer.

POWER OUTPUT CONNECTION: Heyman tab terminals to fit with AMP "Faston" receptacles series 250, part 41774 or Type 914 power jumpers.

728 — $240.00
728A — $260.00

305

POWER SUPPLIES
TYPES 783, 783A
+10, −15 VOLTS

DESIGNED FOR 19 INCH RACK MOUNTING

The Type 783 Power Supply (+10, −15 v) is a simple, rugged supply capable of withstanding wide line and load variation for general system use. The graph above shows the permissible region of operation when both outputs are used. When used singly, the 10-v output can supply 0 to 7.5 amp, or the 15-v output can supply 1.0 to 8.5 amp. It is designed for mounting in a standard 19-in. rack. The Type 783A is a 783 Power Supply with a 50-cps transformer.

ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE: 783: 115 v, 60 cps. 783A: 112.5, 123.5, 195, 220, or 235 v, 50 cps. See "50 cps power"

OUTPUT VOLTAGE: +10 v, −15 vdc, floating.

OUTPUT CURRENT: 1) When only one output is loaded: +10 v: 0 to 7.5 amp, −15 v: 1.0 to 8.5 amp; 2) When both outputs are loaded: +10 v: 0 to 7.0 amp*, −15 v: 1.0 to 8.0 amp*. At least 1.0 amp must be drawn from the −15 v channel to assure proper load regulation.

LINE AND LOAD REGULATION: The output voltage remains between −14.5 and −16.5 v for the −15 v

output and within +9.5 and +11.5 v for the +10 v output, when load varies from minimum to maximum and line voltage varies from 105 to 125 vac.

P-P RIPPLE: Less than 0.7 v for +10 v output. Less than 0.5 v for −15 v output. (20% more ripple on the 50-cps type.)

LINE FREQUENCY TOLERANCE: ±2% of line frequency.

*The sum of the output currents is limited by the following equation: $5(I_{10}) + 6(I_{15}) = 53$

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19 in.

PANEL HEIGHT: 8¾ in.

DEPTH: 5⅜ in.

FINISH: Chromicoat

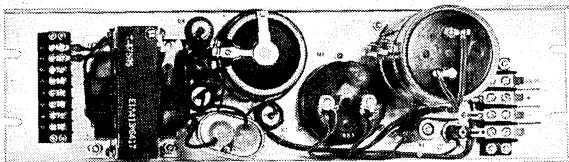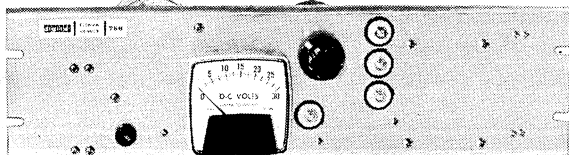POWER INPUT CONNECTION: Screw terminals on transformer.

OUTPUT POWER CONNECTION: Heyman tab terminals designed to mate with AMP "Faston" receptacles series 250, part #41774 or Type 9144 power jumpers.

783	$240.00
783A	$260.00

POWER SUPPLIES
TYPES 786, 786A
VARIABLE 0 TO 24 VOLTS

DESIGNED FOR MARGINAL CHECK APPLICATIONS

The 786 is a floating variable power supply for mounting on a standard 19 in. rack. A resonant input transformer isolates the output from line voltage variations, while the variable transformer and 0 to 30 v meter allow precise control of output voltage. Although designed for marginal checking of digital systems, this rugged supply will fill many other laboratory needs.

ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE: 786: 115 v, 60 cps; 786A: 112.5, 123.5, 195, 220, or 235 v, 50 cps. See "50 cps power."

OUTPUT VOLTAGES: 0 to 24 vdc continuously variable.

MAX. OUTPUT CURRENT: 2.5 amp.

LINE REGULATION: 2% for input variation ±10%.

LOAD REGULATION: Maximum 3.0 v drop at 20 v going from no load to full load.

RIPPLE: ≤1.0 v, p-p at 20 v and 2.5 amp (20% more on 50-cps model).

LINE FREQUENCY TOLERANCE: ±2% of line frequency.

OVERLOAD PROTECTION: 4-amp fuse accessible from front panel.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19 in.

PANEL HEIGHT: 5-3/16 in.

DEPTH BEHIND PANEL: 5 in.

FINISH: Chromicoat

POWER INPUT CONNECTION: Screw terminal strip provided on panel.

POWER OUTPUT CONNECTION: Barrier strip with screw terminals and tabs which fit AMP "Faston" receptacle series 250, part 41774 or Type 914 power jumpers.
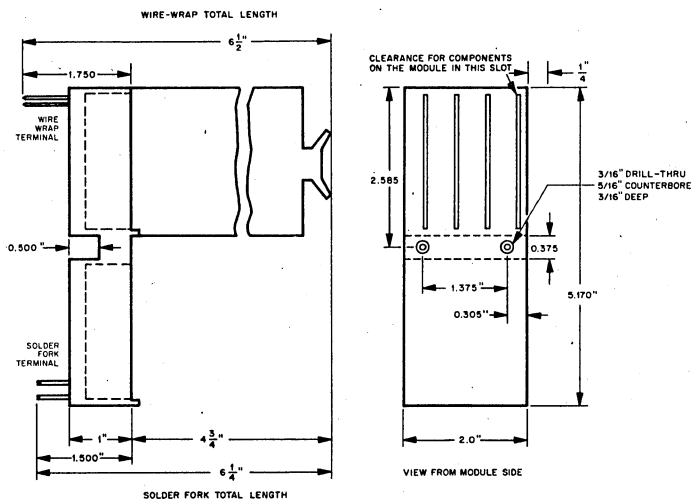
786 — $215.00
786A — $235.00

CONNECTOR BLOCKS
TYPES H800-W, H800-F

This is the 8-module molded socket assembly used in FLIP CHIP mounting panels. Aside from its function as a replacement part, there may be times when a special mounting fixture with one or more

H800 blocks must be made by a manufacturer who wishes to fit a few modules into a confined or irregular space. The drawings below show the pertinent dimensions.

WIRE-WRAP TOTAL LENGTH

$6\frac{1}{2}$"

1.750

WIRE WRAP TERMINAL

0.500"

SOLDER FORK TERMINAL

1"

1.500"

$4\frac{3}{4}$"

$6\frac{1}{4}$"

SOLDER FORK TOTAL LENGTH

CLEARANCE FOR COMPONENTS ON THE MODULE IN THIS SLOT

$\frac{1}{4}$"

2.585

3/16" DRILL–THRU
5/16" COUNTERBORE
3/16" DEEP

0.375

1.375"

0.305"

5.170"

2.0"

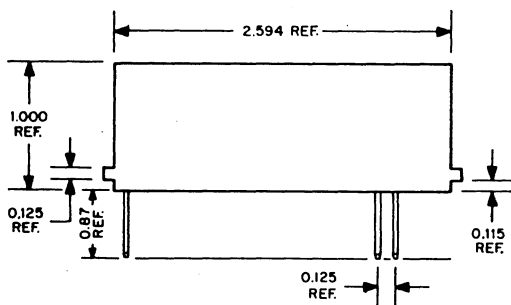VIEW FROM MODULE SIDE
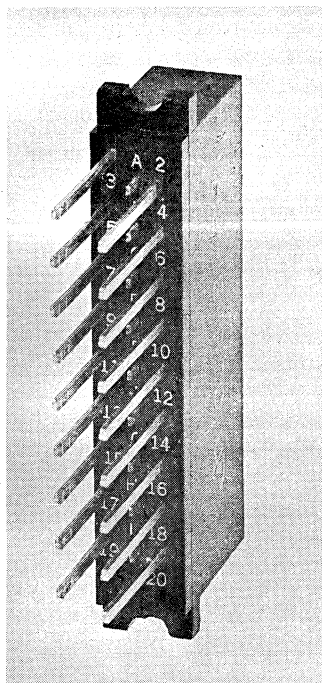
REPLACEMENT CONTACTS TYPES H801-W, H801-F

These contacts are offered in packages of 18 for replacement purposes. In each package, nine straight and nine offset contacts are included, enough to replace all contacts in one socket.

H801-W is for wire-wrap connectors; H801-F is for solder-fork connectors.

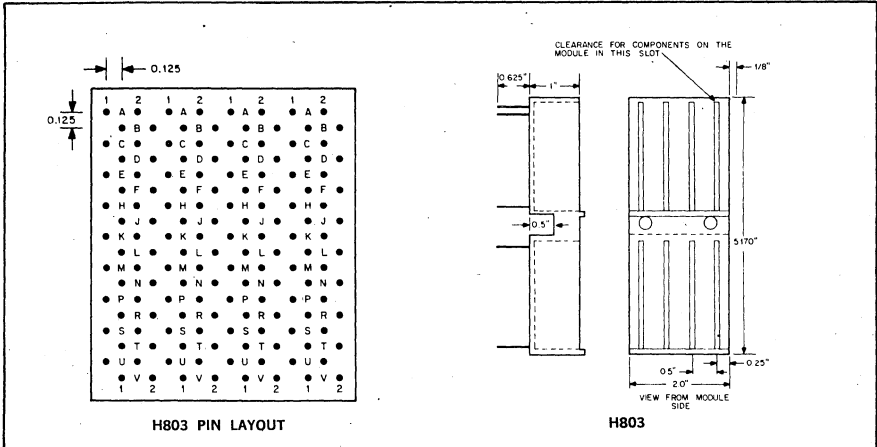|	
H800F	$8.00
H800W	$8.00
H801F	$4.00
H801W	$4.00

This is a connector block for a single flip-chip module like the H800, the H802 can be used to fit a single module in a confined or irregular space. Often the H802 is used as a connector for a cable at some remote location. The H802 is only available with wire wrap pins.

H802 — $4.00

H803 PIN LAYOUT

H803

The H803 is the 8-module molded Jacket Assembly used in the H910 and H911 mounting panels. For each of the eight modules, it provides a 36-pin connector with the wirewrap pins forming a 0.125-inch staggered grid as shown above. This connector is designed to be used with M Series modules; however, it can also be used with all other series listed in this handbook.

The blocks have the same physical dimensions as the H800 with the exception of pin length. These blocks are only available with wire wrap pins which are designed to be wrapped with number 30 wire. Pin dimensions are 0.025 inches square.

The H805 Package of 18 pins for use as spares and replacements for those used in H803. The package contains nine each straight and off-set pins.

R, B, W, and other 18 pin modules will make contact with only the 2-side pins (A2, B2, etc.).

H803 — $13.00
H805 — $ 4.00

POWER CONTROL
TYPE 831
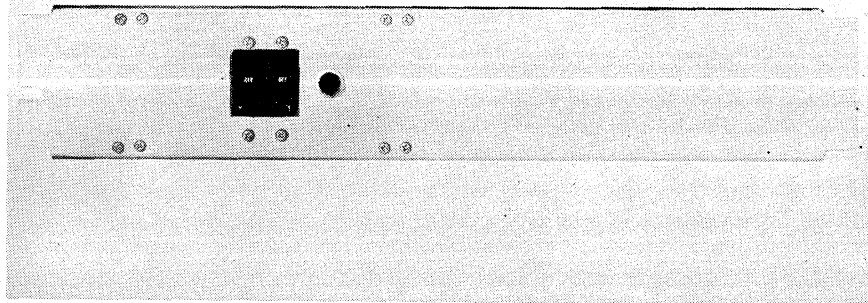
The Type 831 Power Control Panel features a 2-pole circuit breaker which provides convenient 1-step control and protection for entire systems, including auxiliary equipment. The panel fits standard 19-in. racks and is finished with a protective aluminum coating. Available in 4-, 10-, 20-, or 30-amp. capacity.

PANEL HEIGHT: 3-7/16 in.

PANEL WIDTH: 19 in.

Space available for mounting other controls and indicators: 3 in. by 8 in.

831 — $51.00

TYPES H900 AND H900A

This dual function mounting panel offers a way to build complete digital systems of up to 32 FLIP CHIP modules into only 5¼ in. of rack spac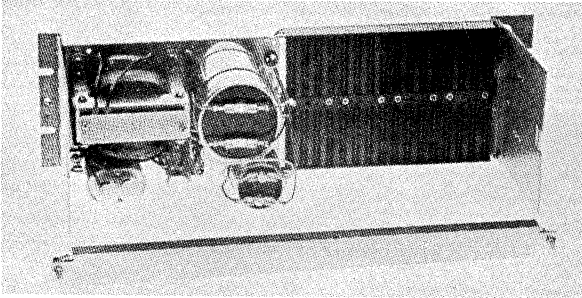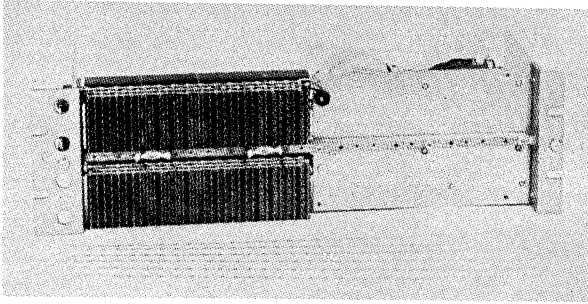e. More power is available than is ever likely to be consumed in a 32 module system; a typical mix of as many as 96 R and W series modules (one H900 and one 1943) can be adequately supplied. Power in excess of that required for 32 modules can be obtained at the terminal block, which is convenient to the input terminal block on any adjacent 1943 Mounting Panel.

ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE: H900: 115 v, 60 cps. H900A: 112.5, 123.5, 195, 220, 235 v, 50 cps. See "50 cps power".

OUTPUT VOLTAGE: +10 v, −15 vdc.

OUTPUT CURRENT: −15 v: ½ to 3 amp; +10 v: 0 to 0.4 amp.

LINE AND LOAD REGULATION: The output voltage remains between −14.5 and −16.5 v for the −15v output and within +9.2 and +11.5 v for the +10 v output, when load varies from minimum to maximum and line voltage varies ±10%.

P-P RIPPLE: Less than 0.6 v for +10 v output; less than 0.6 v for −15 v output (20% more ripple on the 50-cps type).

LINE FREQUENCY TOLERANCE: ±2% of line frequency.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19 in.

PANEL HEIGHT: 5-3/16 in.

DEPTH: 6-3/4 in.

FINISH: Chromicoat

POWER INPUT CONNECTIONS: Screw terminals pro-
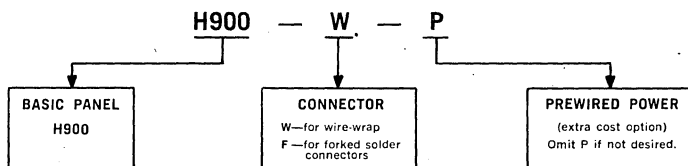
vided on transformer.

MODULES ACCOMMODATED: 32

POWER OUTPUT CONNECTIONS: Barrier strip with screw terminals and tabs which fit AMP "Faston" receptacle series 250, part no. 41774 or Type 914 power jumpers.

H900, H900A
OPTIONS AND ORDERING

There are two kinds of sockets available for FLIP CHIP modules: wire-wrap and solder fork. Prewiring of pins A, B, and C for +10 v, −15 v, and ground is also optional. The example below shows how to specify wire-wrap connectors and prewired power:

$$H900 \quad - \quad W \quad - \quad P$$

BASIC PANEL	CONNECTOR	PREWIRED POWER
H900	W—for wire-wrap F—for forked solder connectors	(extra cost option) Omit P if not desired.

1945-19 HOLD DOWN BAR: Secures modules for shipping, or other vibrational environments.

932 BUS STRIP: Simplifies wiring of register pulse busses, power, and grounds.

TYPE H910

The H910 is similar in appearance to the H900 mounting panels. The differences being that the H910 panels are built from four H803 connector blocks and a 5 volt regulated supply. Wire wrap connectors for =30 awg wire only are present on the H910. The panel will hold 32, 36 pin modules. In addition, the panel is bussed with 933 bus strips on pins A2, C2, and T1 and all power wiring to the supply is connected. Power in excess of that required for the 32 modules can be obtained at the terminal block, which is convenient to the input terminal block on any adjacent H911 Mounting Panel.

ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE:
105-125 VAC or 210-250 VAC 47-63 HZ
OUTPUT VOLTAGE:
5 vdc.
OUTPUT CURRENT:
0-5 amps. short-circuit protected for parallel supply operation.

LINE AND LOAD REGULATION:

The output voltage will not vary more than 50 mv over the full range of load current and line voltage.

P-P RIPPLE:

Less than 20 mv.

OVERVOLTAGE PROTECTION:

The output is protected from transients which exceed 6.9 Volts for more than 10nsec. However, the output is not protected against long shorts to voltages above 6.9 Volts.

H900	— $180.00
H900A	— $200.00
Option P	— $5.00
H910	— $280.00
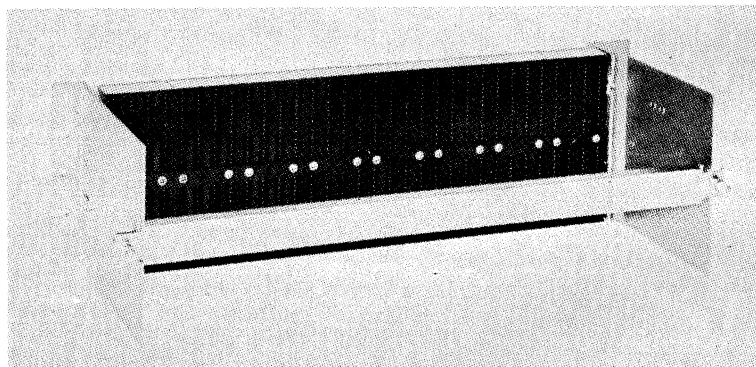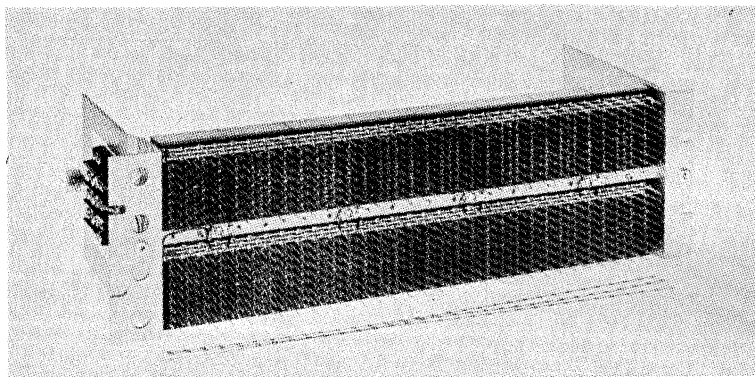
TYPE 1943 MOUNTING PANEL

The 1943 Mounting Panel houses 64 modules. It is designed for mounting in a standard 19-in. rack. The mounting panel is finished with an aluminum conversion coating (Chromicoat). Filter capacitors are included on all power supply lines.

Available options are solder or wire-wrap connectors, power input via terminal strip or marginal check switches, and power wiring. The chart below shows how the options are indicated when ordering.

1943 — F — B — P

```
                                    ┌──────────────┐
                                    │ Power Wiring │
                                    │   Option*    │
                                    └──────────────┘
```

BASIC PANEL	CONNECTOR	POWER CONNECTION
1943	F —Forked-pin solder type connectors. OR W—Wire-wrap connectors.	B —Power input via terminal block. Both conventional screw connections and taper tabs can be used. M—Marginal check switches on all voltage inputs allow selection of fixed or variable power*.

*Additional charge.
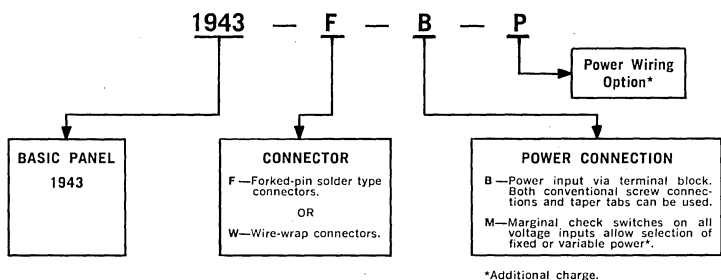
EXAMPLE: If you require a Type 1943 Mounting Panel with wire-wrap connectors, marginal check switches on the power connection, and prewired power, you would order:

1943 — W — M — P

BASIC PANEL   CONNECTOR   POWER CONNECTION   POWER WIRING

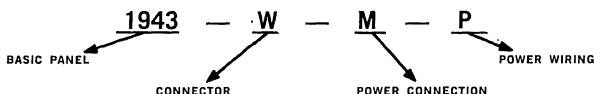MECHANICAL DIMENSIONS: 19 in. wide; 5-3/16 in. high; 6-3/4 in. deep. Tabs for power connections fit AMP "Faston" receptacles, series 250, part 41774 or Type 914 power jumpers.

1945-19 HOLD DOWN BAR: Reduces vibration and keeps modules securely mounted when panel or system is moved. Adds 1/2 in. to depth of mounting panel.

932 BUS STRIP: Makes wiring power and register pulse busses easy.

H911 MOUNTING PANEL

The H911 mounting panel is similar to the 1943. It houses 64, 36 pin connectors. Mechanical dimensions are identical to those of the 1943 with the exception of the pin length. Pins on the H803 blocks are 0.626" long while those on the H800 are 0.75 inches long. The H911 is available with wire wrap pins only. Marginal check and power wiring options are available on the H911.

933 BUS STRIP — For H911 mounting panel, makes wiring power and register pulse busses easy.

H911B	— $151.00
H911BP	— $161.00
H911-M	— $172.00
H911-MP	— $182.00
932	— $ .60
933	— $ 1.00
1943-F-B	— $111.00
1943-W-B	— $111.00
1943-F-B-P	— $121.00
1943-W-B-P	— $121.00
1943-F-M	— $132.00
1943-W-M	— $132.00
1943-F-M-P	— $142.00
1943-W-M-P	— $142.00
1945-19	— $ 15.00

MODULE DRAWER AND ACCESSORIES

TYPES H920, H921, H923
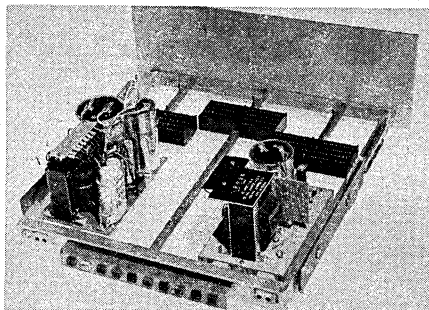
Shown above are the H920 module drawer, the H921 front panel, and the slide half of the H923 slide tracks. Mounted on this assembly are H701 and H710 power supplies, and three H800 connector blocks.

The H920 Module Drawer provides a convenient mounting arrangement for a complete digital logic system. The drawer has sufficient room to house up to 16 mounting blocks in addition to the H701 and H710 power supplies. Power supplies are not included in the H920 but must be ordered separately. When used without the power supplies, there is room for up to 24 mounting blocks. The drawer accepts both H800 and H803 mounting blocks and fits a standard 19" relay rack and all DEC cabinets. Width of the module drawer is 16¾" and depth is 19". When used with the H921 Panel, the height is 6¾". The module drawer comes equipped with a power bracket for distribution of power within the drawer, to other drawers or to mounting panels. The H920 comes with convenient mounting arrangements for both the H921 front panel and the H923 slide tracks. The H921 is a front panel designed to be used primarily with the H920 Module Drawer. It provides convenient mounting arrangements for switches, indicators, and other accessories which may be required in a logic system. The H921 comes predrilled and ready to mount to the H920. Height of the panel is 6¾" and width is 19".

The H923 chassis slides are designed to be used with the H920 Mounting Drawer. These slides allow the user to slide the drawer out of the cabinet or rack and tilt the drawer to any angle. H923 tracks may also be ordered directly from Chassis Trak, Inc., Indianapolis, Indiana, part number CTD 120.

H920—	$170.00
H921—$	5.00
H923—$	75.00
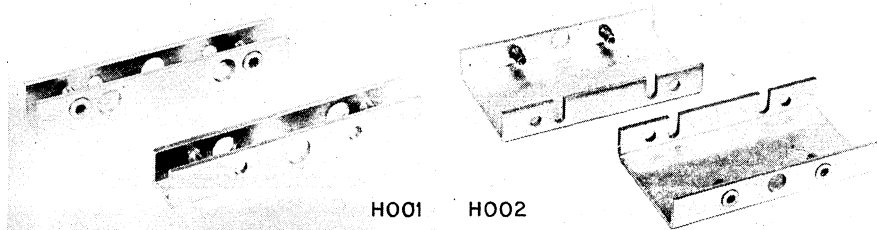
H001   H002
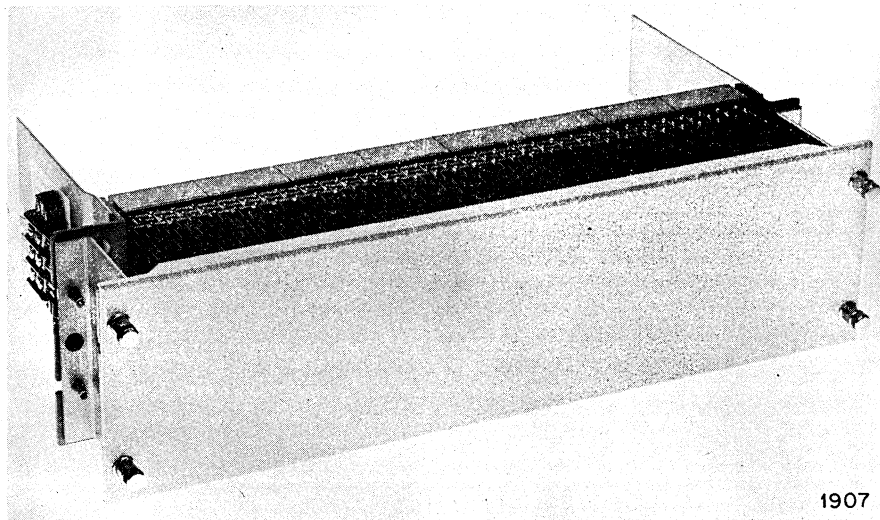
1907

H001 PANEL COVER BRACKET

The H001 consists of a pair of U-brackets that fit under the mounting screws of a 1943, H900, H910, or H911 FLIP CHIP mounting panel, providing a way to mount 1907 cover panels. The ¾" standoff obtained makes these cover plates approximately flush with DEC cabinet edges.

H002 PANEL SETBACK BRACKET

The H002 consists of a pair of U-brackets which are used to setback a power supply or mounting panel from a 1907 panel cover. The H002 permits the use

of controls on the 1907 cover plate with protrusions up to 2".

DEPTH: 3 in. (bridges DEC cabinet mounting rails)

1907 MOUNTING PANEL COVER

The Type 1907 Mounting Panel Cover is designed to cover the logic and power wiring for the 1943, H900, H910, or H911 Mounting Panels. The 1907 should be used with the H001 or H002 Panel set back brackets and is finished in brown "tweed" or blue. Dimensions are 5¼ by 19 in. Specify color when ordering.

|	
H001 — $8.00
H002 — $8.00
1907 — $9.00

4908 PANEL INDICATOR ASSEMBLY

Consists of lamp, spring clip, and terminal. Facilitates panel mounting of individual indicator lamps. Power required is −15 v at 30 ma. Requires a 5/16 in. hole for mounting. Wires can be any length, since their capacitance is isolated from the logic by a driver such as W050.
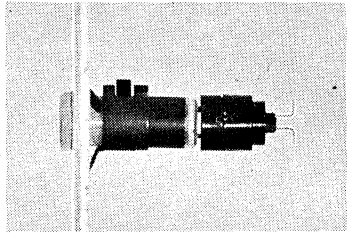

4906 INDICATOR WITH AMPLIFIER

Single indicator lamp with transistor driver. May be panel mounted in ⅜ in. hole; bulb is replaceable from the front. Power required is −15 v at 30 ma. Overall dimensions are 2½ in. x ⅝ in. x ⅞ in. The input to the transistor driver requires DEC standard levels or equivalent. The input load is 1 ma at −3 v. Minus 3 v lights the lamp; 0 v turns it off.
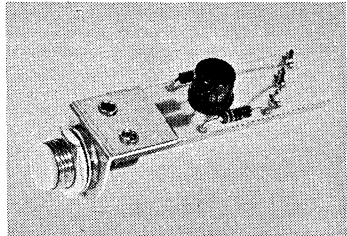
4917, 4918 Indicators with Amplifiers

The 4917 is a 9-bit indicator and the 4918 is an 18-bit indicator both of which can be driven directly from R series logic without additional buffering or clamped loads. The indicators must be used in conjunction with a W018 connector. All 18 pins of the cable connector are used for signal leads. Ground and −15v are brought to the module through quick disconnect jumpers. Plugging the W018 into a connector slot with +10v and −15v on pins A and B will not damage the indicators. A −3v or open circuit turns the indicator on. A ground input turns the indicator off. Load at ground is 1ma. The W018 should be plugged into the logic mounting and panel and a W023 should be used on the end of the cable that connects to the 4917 or 4918.
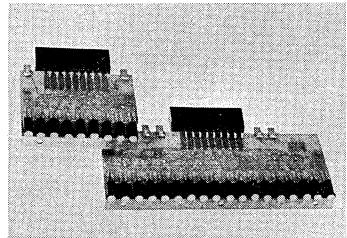
Power required is 540 ma at −15v (4918). Overall dimensions are 9 1/2 in. x 15/16 in. Bulbs are on 7/16 centers and each requires a 5/16 in. hole.

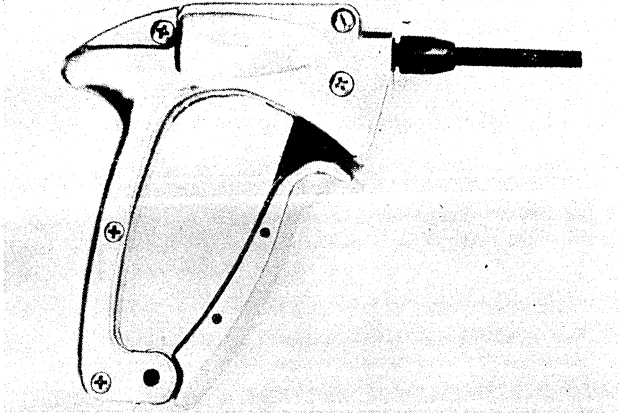All indicators utilize 28-v bulbs which are operated at 15 v. This provides more than adequate illumination and greatly extends the life of the bulbs. When driving type 4906 from R-series flip-flops, one or more W002 or W005 clamped loads must be added to supply the current at −3 v demanded by these circuits.

4908 —	$ 3.00
4906 —	$ 9.50
4917 —	$73.00
4918 —	$96.00

H810 PISTOL GRIP HAND WIRE WRAPPING TOOL

The type H810 Wire Wrapping Tool is designed for wrapping #24 or #30 solid wire on Digital-type connector pins. The H810 Kit includes the proper sleeves and bits. It is recommended that five turns of bare wire be wrapped on these pins. This tool may also be purchased from Gardner-Denver Co. (Gardner-Denver part No. 14H-1C) with No. 26263 bit and No. 18840 sleeve for wrapping #24 wire. Specify bit #504221 and sleeve #500350 for wrapping #30 wire. When ordering from Digital specify the sleeve and bit size desired for #24 and #30 wire.
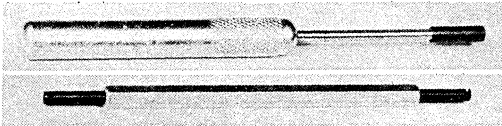
H811 WRAPPING AND TYPE H812 UNWRAPPING TOOLS

The Type H811 Hand Wrapping tool is useful for service or repair applications. It is designed for wrapping #24 solid wire on DEC Type H800-W connector pins. This tool may also be purchased from Gardner-Denver Co. as Gardner-Denver Part #A20557-12.

Wire wrapped connections may be removed with the Type H812 Hand Unwrapping tool. This tool may also be purchased from Gardner-Denver Co. as Gardner-Denver Part #500130.

The H811A and H812A are equivalent to the H811 and the H812 except that the A versions are designed for #30 wire. Both tools may be purchased from Gardner-Denver directly under the following part numbers: H811A A-20557-29; H812A 505 244-475. The H813 is a ≠24 bit; H813A, a ≠30 bit. The H814 is a ≠24 sleeve; H814A, a ≠30 sleeve.

H810(24)	$ 99.00		H812(24)	$ 10.50
H810A	$ 99.00		H812A(30)	$ 10.50
H810B	$150.00		H813(24)	$ 30.00
H811(24)	$ 21.50		H813A(30)	$ 30.00
H811A(30)	$ 21.50		H814(24)	$ 21.00
			H814A(30)	$ 21.00

913 AND 915 PATCHCORDS

These patchcords provide slip-on connections for FLIP CHIP mounting panels and are available in color-coded lengths of 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, and 64 inches. All cords are shipped in quantities of 100 in handy polystyrene boxes. Type 913 patchcords are for 24 gauge wirewrap and use AMP Terminal Type #60530-1. Type 915 patchcords are for 30 gauge wirewrap and use AMP Terminal Type #85952-3.

H820 AND H821 GRIP CLIPS FOR SHIP-ON PATCHCORDS

The type H820 and H821 GRIP CLIPS are identical to slip-on connectors used in respectively the 913 and 915 patchcords. These connectors are shipped in packages of 1000 and permit fabrication of patchcords to any desired length. H820 GRIP CLIPS will take size 24-20 awg. wire and may be purchased from AMP, Inc. as AMP part #60477-2. H821 GRIP CLIPS will take size 30-24 awg. wire and are AMP part #85952-3.

H825 HAND CRIMPING TOOL

Type H825 hand crimping tool may be used to crimp the type H820 GRIP CLIP connectors. Use of this tool insures a good electrical connection. This tool may also be obtained from AMP, Inc. as AMP part #90084.

H826 HAND CRIMPING TOOL

Type H826 hand crimping tool may be used to crimp the type H821 GRIP CLIP connectors. This tool is identical to AMP part #90191-1.

913—$	18.00/pkg. of 100
915—$	33.00/pkg. of 100
H820—$	47.80/pkg. of 1000
H821—$	75.00/pkg. of 1000
H825—$146.00	
H826—$210.00	
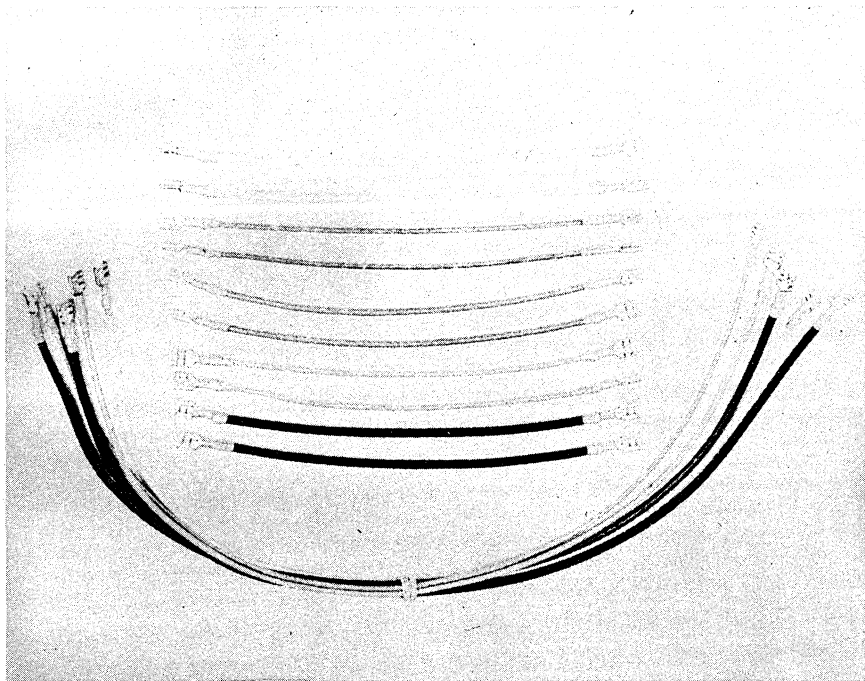
For interconnections between power supplies, mounting panels, and logic lab. panels these jumpers use AMP "Faston" receptacles series 250. Specify 914-7 for interconnecting adjacent mounting panels, or 914-19 for other runs of up to 19 inches. 914-7 contains 10 jumpers per package; 914-19 contains 10 jumpers per package.

914-7 — $4.00/pkg.
914-19 — $4.00/pkg.

```
FLIP        SYSTEM
CHIP        MODULE
 A ───────── A
             B
 B ───────── C
 C ───────── D
┌D
│E ───────── E
│F ───────── F
│H ───────── H
│J ───────── J
│K ───────── K
│L ───────── L
│M ───────── M
│N ───────── N
│P ───────── P
│R ───────── R
│S ───────── S
│T ───────── T
│U ───────── U
│V ───────── V
│            W
│            X
│            Y
└─────────── Z
```
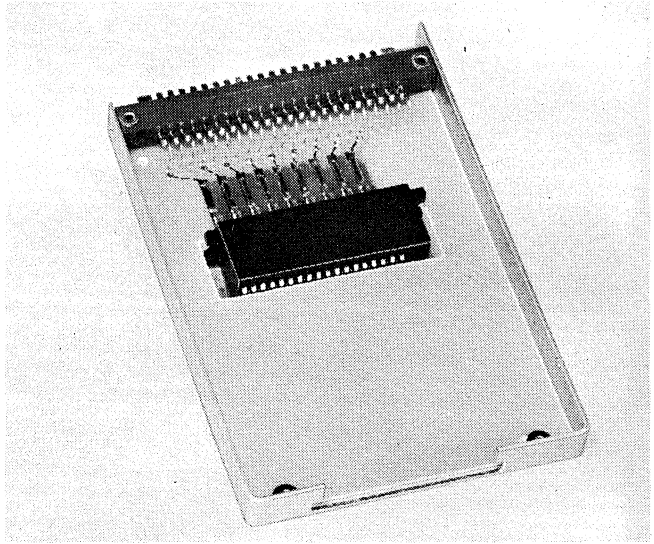
This accessory occupies one slot of a system module mounting panel, allowing a FLIP CHIP module to be plugged in. The $+10$ v for the FLIP CHIP module is taken from pin A of the system module connector. The handle of a FLIP CHIP module plugged into the adapter projects $1\frac{1}{2}$ in. beyond a standard System Module handle. Because components on the FLIP CHIP module project above the normal limit of components on system modules, some care should be taken to see that these components do not contact adjacent printed boards while power is applied.

4912 — $28.00
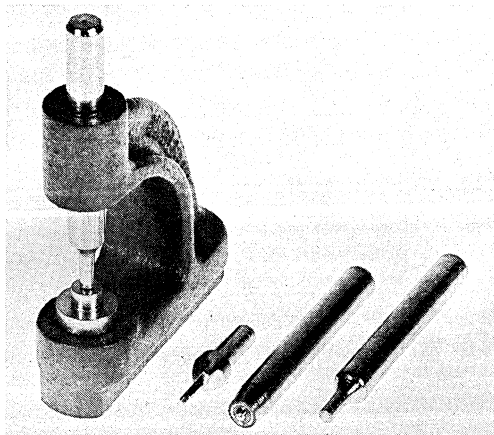
The H830 is designed for clinching on rivets on the 1951, W992, and W993 blank modules. Fits into any vise and once the module and eyelet are positioned, a slight tap of the hammer will clinch the eyelet.

The unit has a 3½″ height and weighs 1 lb.

H830 — $10.00

Digital offers a variety of cabinets which can be used to build up special systems.

The Type CAB-1 can be used alone or in multicabinet systems where only one control cabinet or indicator cabinet is desired. The standard cabinet has full length French doors for access to logic wiring.

The Type CAB-2 cabinet is used where many controls and indicators are required. No French doors are provided in front.

The Type CAB-3 is intended as an expander cabinet for the PDP-8. The cabinet has a wood panel in the front above the table top. The wood panel comes down to the table and the bottom of the panel can be removed to add accessories from the table up. In addition to use as an expander cabinet, the CAB-3 provides a means of ready access to the front of the system.

The Type CAB-6 can be used with other cabinets or as a remote indicator cabinet. The French doors give access to logic wiring. The brushed aluminum, clear anodized panel is placed at a convenient height for viewing indicators.

All cabinets are alike with the exception of end panels and the French door configuration. All cabinets come, as shown, with fan, fan housing, and filter. A plenum door for mounting power supplies is provided in the rear behind full length French doors. Casters are provided for mobility. All cables enter through an access cutout in the bottom of the cabinet.

The CAB-8A is a free-standing cabinet, with a winged table with legs. The logic modules are housed beneath this table and enclosed with short French doors. The CAB-8A is not expandable and, therefore,

not recommended for systems that have multiple bays bolted together.

The CAB-8B is similar to the CAB-8A with the exception of the table. The table is rectangular and is positioned so that other cabinets may be placed adjacent to the cabinet. The CAB-1 will normally be bolted to the left on the CAB-8B and the CAB-3 will normally be bolted to the right of the CAB-8B.

Cabinets can be factory assembled into multicabinet groups. Cabinet types can be mixed in one group except for the CAB-2, which has different end panel and trim details.

The cooling fan built into the bottom of each cabinet is adequate to ventilate up to $5\frac{1}{4}$ in. mounting panels of B-series FLIP CHIP modules mounted near the bottom of the cabinet. If the lower dissipation R-series modules of W or A series modules make up a significant portion of the system, more modules can be installed. Four-hundred watts is the maximum total power that should be dissipated in all of the modules mounted in any one cabinet. The top panel of each cabinet must be removed when FLIP CHIP modules are installed, and all side panels and plenum doors should be closed except during system checkout.

The price of the first cabinet includes end panels. The price of each additional cabinet includes the cabinet joining hardware. Cabinets are shipped assembled and on skids with the tables packed separately.

DIMENSIONS
Cabinet
42 in. wide
27-1/16 in. deep
69⅛ in. high

SERVICE CLEARANCE
8¾ in. front
14⅞ in. rear
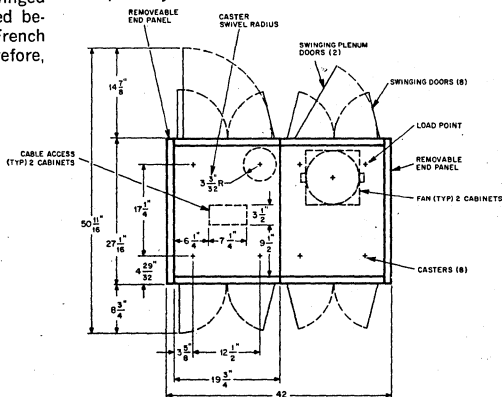
In addition to the 728 power supply, there are several other items especially designed for plenum door mounting. For example, there are the 1946 mounting

panel and the 734B marginal checking supply. Your nearest DEC sales office can supply details.

CAB-1 —	$700.00 $500.00	CAB-6 —	$800.00 $600.00
CAB-2 —	$700.00 $500.00	CAB-8A —	$1,100.00
CAB-3 —	$650.00	CAB-8B —	$1,000.00
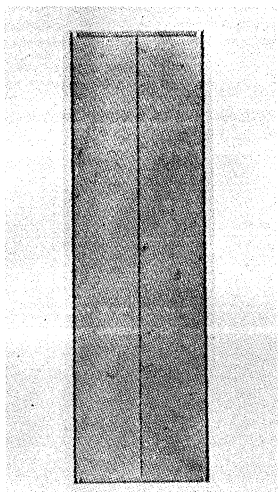
CAB-1
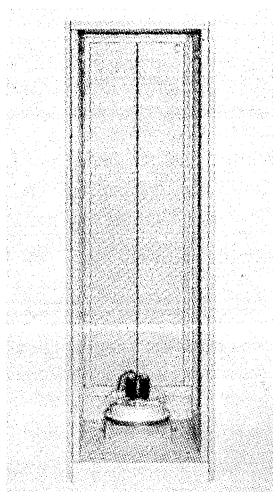
CAB-2
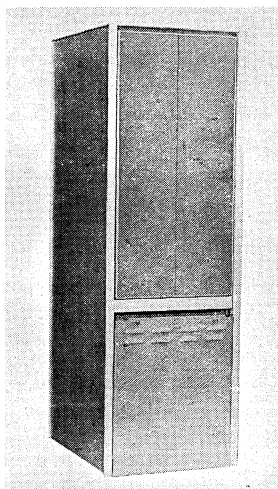
CAB-3
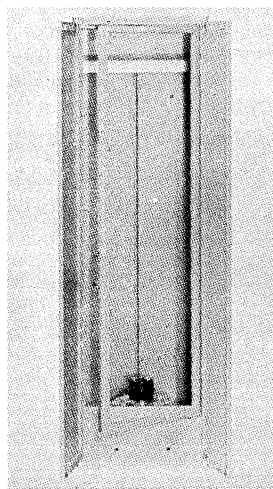
CAB-6 (Inside view)

EXPANDER CABINETS
(No End Panels)

CAB-1

CAB-3
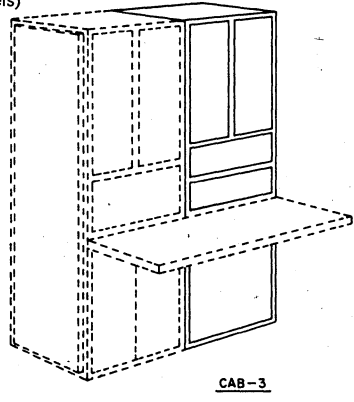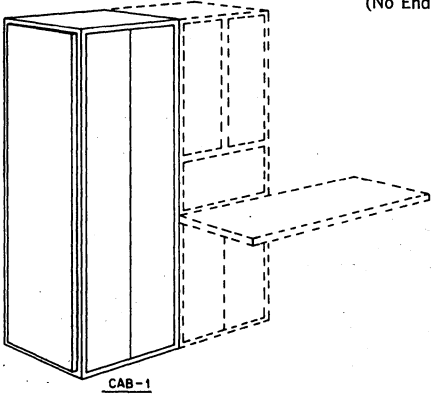
FREE-STANDING
CABINETS

CAB-8A

CAB-8B
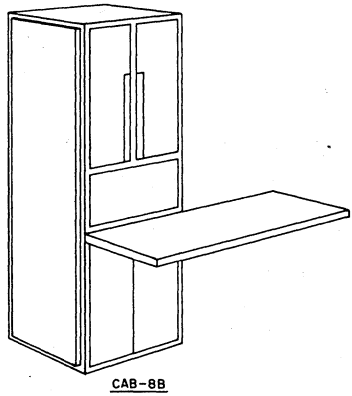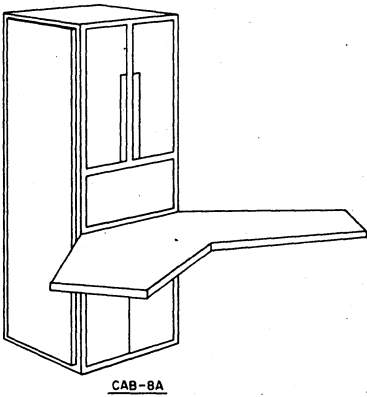
OCTAIDS™ AND PANELAIDS™

Digital's new OCTAID and PANELAID kits are designed to provide the logic user with an easy-to-assemble, time-saving group of components to achieve common logic functions, such as up-down counting, decoding digital-to-analog and analog-to-digital conversion, and computer interfaces. Standard FLIP-CHIP modules and connectors are used in conjunction with special purpose printed circuit interconnectors.

The OCTAID series has up to eight standard FLIP-CHIP modules, and the PANELAID series has up to 64 modules. Each kit includes the necessary modules, connectors, and specially designed printed-circuit, back-panel wiring eliminating the necessity for hand-wiring. Since hand-wiring and trouble shooting are eliminated, a significant reduction in the amount of manufacturing time can be achieved.

Input/Output Buffer kits are designed to interface between Digital's PDP-8 or PDP-8/S computers and other OCTAID kits or specially designed systems. PANELAID kits, in general, can be interfaced directly to the PDP-8 or PDP-8/S.

OCTAID KIT

A–D PANELAID KIT
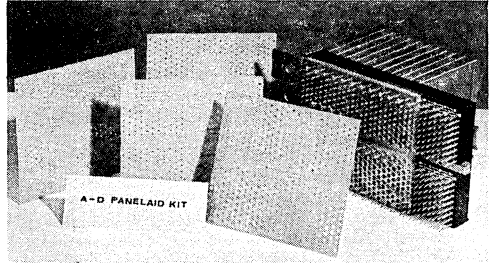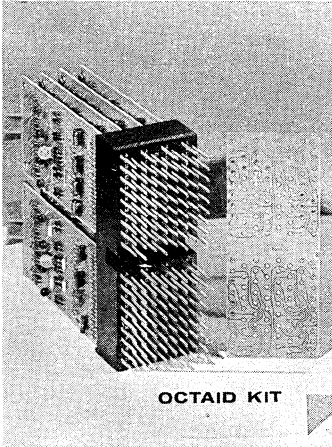
DIGITAL-ANALOG CONVERTER KITS
KITS D001A-F

Each converter can have from 8 to 13 bits depending upon the module and input pin combination. Each D001 kit includes two printed-circuit boards (F728 and F843) that are used for all digital-analog converter common connections, one H800W connector block, one A704 reference supply, and the necessary converter modules.

MODULE LOCATION AND TYPES VERSUS BITS (KIT)*

BITS (KIT)	8(A)	9(B)	10(C)	11(D)	12(E)	13(F)
A02	A601	A601	A601	A601	A601	A601
A03	A601	A601	A601	A601	A601	A601
A04	A601	A601	A601	A601	A604	A604
B02	—	A604	A604	A604	A604	A604
B03	—	—	—	A604	A605	A605
B04	—	—	—	—	—	A605

*The double height A704 fills locations A01 and B01 for all converters.

MODULE LOCATION DIAGRAM (WIRING SIDE)

328
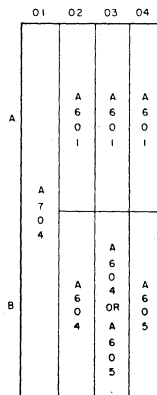
The following table illustrates the digital input pins and analog output pin as specified for each size of converter. Bit 0 is designated the most significant bit.

INPUT/OUTPUT PINS FOR CONVERTERS

SIGNAL	8(A)	9(B)	10(C)	11(D)	12(E)	13(F)
Analog Output	A04K	B02K	B02K	B03K	B03K	B04K
Bit 0 in	A04U	B02U	B03U	B03U	B03U	B04U
Bit 1 in	A04T	B02T	B02T	B03T	B03T	B04T
Bit 2 in	A04V	A04U	A04U	B02U	B02U	B03U
Bit 3 in	A03U	A04T	A04T	B02T	B02T	B03T
Bit 4 in	A03T	A04V	A04U	A04U	A04U	B02U
Bit 5 in	A03V	A03U	A03U	A04T	A04T	B02T
Bit 6 in	A02U	A03T	A03T	A04V	A03U	A04U
Bit 7 in	A02T	A03V	A03V	A03U	A03T	A04T
Bit 8 in	—	A02U	A02U	A03T	A03V	A03U
Bit 9 in	—	—	A02T	A03V	A02U	A03T
Bit 10 in	—	—	—	A02U	A02T	A03V
Bit 11 in	—	—	—	—	A02V	A02U
Bit 12 in	—	—	—	—	—	A02T

INPUT: Standard Digital levels of —3 volts or ground are required. Loading for all digital inputs is 1 ma each at ground. If all inputs on a module are not required, the most significant inputs should be used and the least significant ones should be left open-circuited.

OUTPUT: The analog output is the equivalent of the digital input. The most negative output is —10 volts, less the value of the least significant bit. The most positive output is ground. The offset of the least significant bit may be overcome by adjusting the —10 volt reference to —10 volts plus the value of the LSB to obtain a full scale value. Output impedance is.1000 ohms.

D001A (8 bits) — $376.50
D001B (9 bits) — $438.50
D001C (10 bits) — $438.50
D001D (11 bits) — $500.50
D001E (12 bits) — $518.50
D001F (13 bits) — $596.50

BCD UP-COUNTER
KIT D002

The D002 has four binary-coded decimal (8-4-2-1) up-counters. Each counter is operated independently or in series to form a four-digit counter. All inputs conform to standard DEC pulse and level requirements. Each kit includes one printed-circuit board type F723, one H800 connector block, and two R202 decade modules per decade.
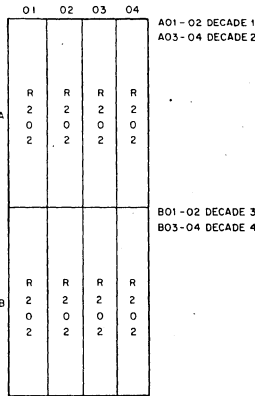
MODULE LOCATION DIAGRAM (WIRING SIDE)
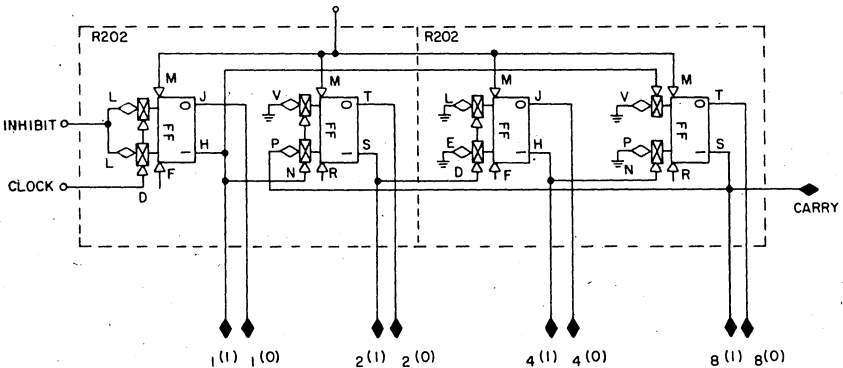
BCD Up-Counter

| Single Decade — $ 62.50 |
| Quad Decade – $ 212.50 |

BI-DIRECTIONAL DECADE COUNTER
KIT D004

The D004 is primarily a one-digit 8-4-2-1 up-down counter that can optionally be used for decimal decoding and 8421-2421 conversion. The counter is level-controlled. All blocks are wired for the counting, decoding and conversion functions. If decoding or conversion functions are not desired, the associated modules need not be ordered. The basic up-down counter kit includes two printed-circuit boards (F861 and F862), one H800 connector block four R201 flip-flops, and one R121 gate. To add the decimal decoding function, one R151 binary-to-octal decoder and one R111 gate are included. To add the 8421-2421 conversion function,* one R121 gate is included. The following figures show module location; define the inputs, outputs, and control connections for interconnection to other devices; and schematically illustrate the completed counter.
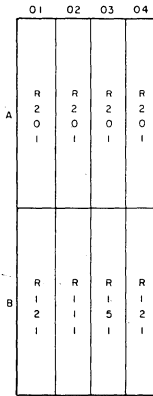
MODULE LOCATION DIAGRAM (WIRING SIDE)

*8421 to 2421 Conversion — Wiring has been provided for 8421 to 2421 conversion for use in a digital-to-analog converter. The most and least significant bits (2 - - 1) are derived directly from the 0 sides of the up down counter. The remaining bits (- 4 2 -) are derived from the outputs of two R121 gates connected as NOR gates.
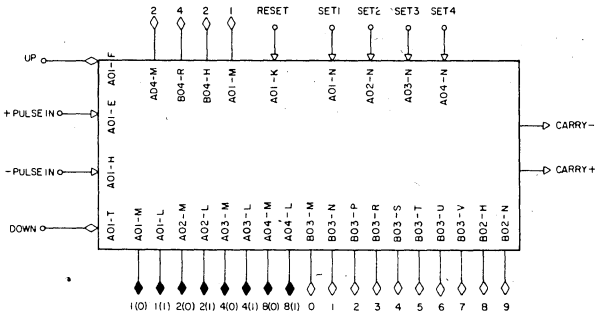
UP/DOWN DECADE DECODER AND CONVERTER INPUTS, OUTPUTS, AND CONNECTIONS

D004	— $124 40
Decoding Option	— $ 47.00
Conversion Option	— $ 17.00
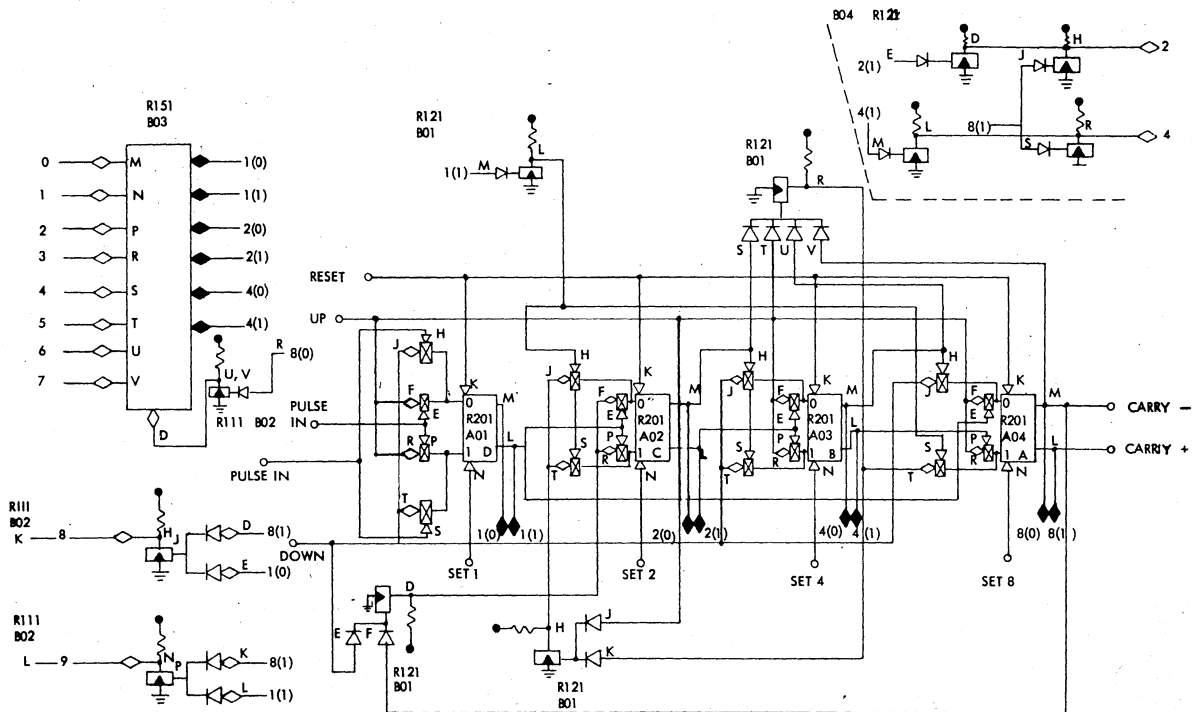
UP-DOWN COUNTER, DECODER, AND CONVERTER

PDP-8/S OUTPUT BUFFER REGISTER
KIT D006

This kit provides a convenient means of sampling, storing, and transferring to the outside world the contents of the Central Processor's Accumulator Register during an IOT instruction.

Four R203 triple flip-flop boards are used for storage, making a total of twelve flip-flops. The kit also includes two printed-circuit boards (types F001 and F004), one H800W connector block, and W103 device selector, on R111 gate, and one R202 dual flip-flop. The flip-flops are gated by the corresponding AC bits (0 - 11) being set to the "one" state (positive conditioning levels) and by a positive enabling pulse (supplied by IOP 4 and the chosen device select code). A strobe pulse input is required to the R202 (pin D) when data is strobed out of the R203's.

OUTPUT: The contents of the output buffer register may be sampled or transferred where desired by taking the bit information directly from the output pins of the flip-flops. R202 output (pin J B04) provides a negative level to indicate new data has been deposited in the buffer.
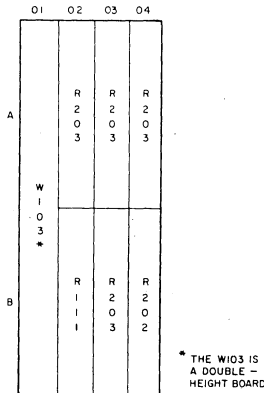
MODULE LOCATION DIAGRAM (WIRING SIDE)

D006 — $215.50

LOCATION NUMBERS FOR R203's ARE: A02, A03, A04, B03.

OUTPUT BUFFER REGISTER

DUAL 8-BIT SHIFT REGISTER
KIT D007

This kit has two independent 8-bit shift registers with the enable inputs of the first flip-flop left floating. By appropriate connection of the floating inputs, operation as a shift register, ring-counter, or switch-tail ring counter can be attained. In addition, the two 8-bit circuits can be operated in series to provide a 16-bit capability. Each kit includes two printed-circuit boards(types F005 and F006), one H800 connector block, and either one or two shift registers. Each shift register includes four R205 flip-flop modules (8 flip-flops) with the "0" and "1" enable inputs connected, respectively, to the "1" and "0" outputs of the preceding stage.

All pulse inputs are bussed together to form a common shift line. A common direct clear line is also brought out for simultaneous clearing of all flip-flops in the shift register. Loading a "1" into the shift register is accomplished by grounding any enable input at least 400 nsec prior to initiation of a load pulse. Individual load pulses are also bussed together to form a common load or strobe input. All pulse and level inputs must conform to the standard DEC configuration.

	O1	O2	O3	O4
A	R 2 0 5	R 2 0 5	R 2 0 5	R 2 0 5
B	R 2 0 5	R 2 0 5	R 2 0 5	R 2 0 5

MODULE LOCATION, DIAGRAM (WIRING SIDE)

335
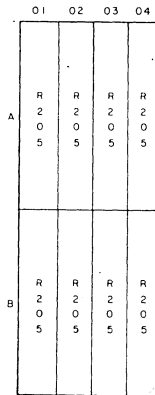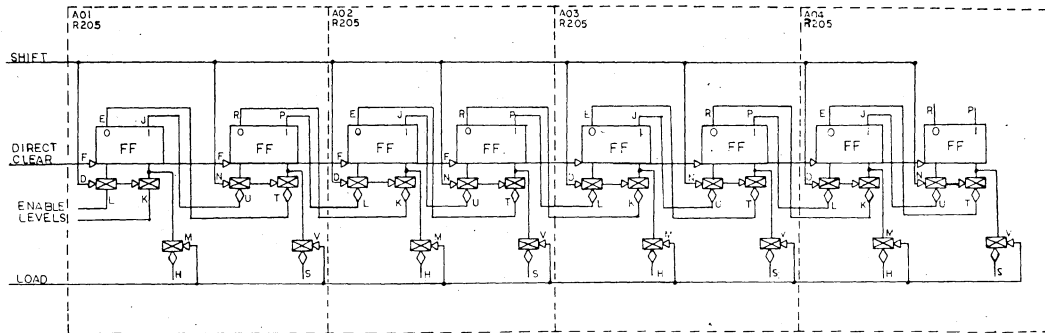
DUAL 8-BIT SHIFT REGISTER

Note: Loading for registers #1 and #2 are identical. For location of inputs and outputs for register #2, substitute row B in place of row A.

336

DUAL 8-BIT UP-COUNTER
KIT D008

This kit includes two independent eight-bit up-counters (four R202 flip-flops for each counter), two printed-circuit boards (types F007 and F008), and one H800 connector block. Each counter can be operated independently, or should more than eight bits be required, the counters can be connected in series to provide a 16-bit counter.

Each counter has an independent direct clear, count enable, and pulse or count input line. In addition, each bit of either counter can be individually set so that the counter can start counting at some preselected number other than zero. All pulses and levels should conform to DEC standards.

	01	02	03	04
A	R 2 0 2	R 2 0 2	R 2 0 2	R 2 0 2
B	R 2 0 2	R 2 0 2	R 2 0 2	R 2 0 2
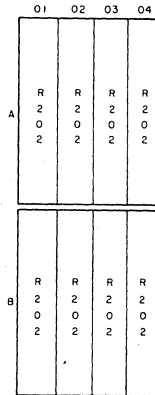
MODULE LOCATION DIAGRAM

Single —	$117.00
Dual —	$217.00
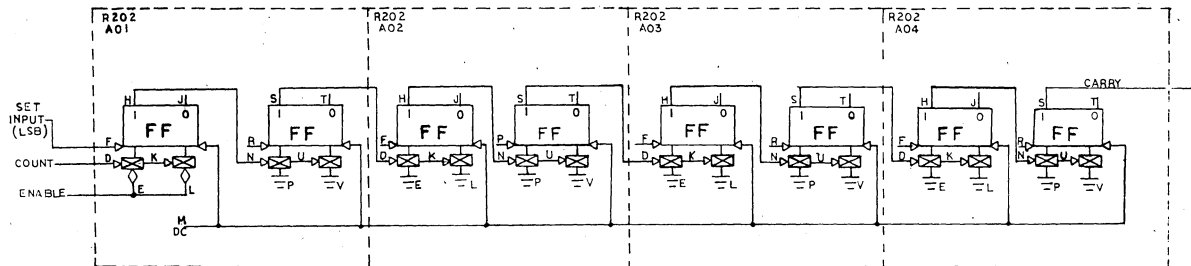
DUAL 8-BIT UP-COUNTER

ANALOG-DIGITAL CONVERTER KITS
KITS C001, C001A, C002

There are three 10-Bit, successive-approximation, analog-digital converters in the Panelaid TM series. The C001 is supplied with 60-Hertz power, the C001A with 50-Hertz power, and the C002 is available without AC power. All three converters accept any analog value from 0 to —10.23v (full scale) and convert this to a 10-bit absolute value. Each unit has an accuracy of 0.1 percent ($\pm\frac{1}{2}$ least significant bit) and a resolution of 1 part in 1024 (10 millivolts). The maximum conversion rate is 30 kh for low-impedance sources with a maximum input current drain of 1 μamp. All digital input and output signals are compatible with DEC standard pulses and levels. The C001 and C001A are housed on a H900 mounting panel, while the C002 is mounted on a 1943 panel.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
A		A704	A601	A601	A601	A502	R202	R202	R202	R202	R202							
B		A704	R202	R602	R602	R302		R202	R202	R202	R202	R202						
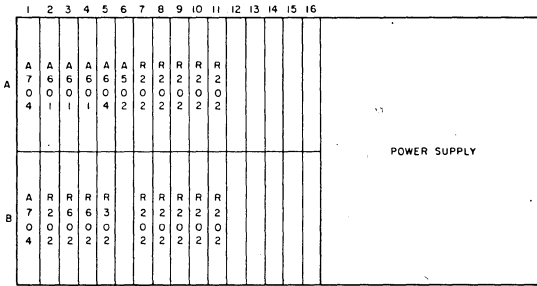
POWER SUPPLY

MODULE LOCATION DIAGRAM

PARTS LIST

1 — H900 — W — P*		power supply and mounting panel
11 — R202		dual flip-flop
2 — R602		dual pulse amplifier
1 — R302		dual delay
1 — A502		comparator
3 — A601		D to A converter
1 — A604		D to A converter
1 — A704		reference supply
1 — E724		Panelaid
1 — E725		Panelaid
1 — E726		Panelaid
1 — E727		Panelaid
1 — W980		module extender

*1943 supplied with the C002, H900A-W-P is supplied in C001A

Kit #C001 — $1,139.00
Kit #C001A — $1,159.00
Kit #C002 — $1,080.00
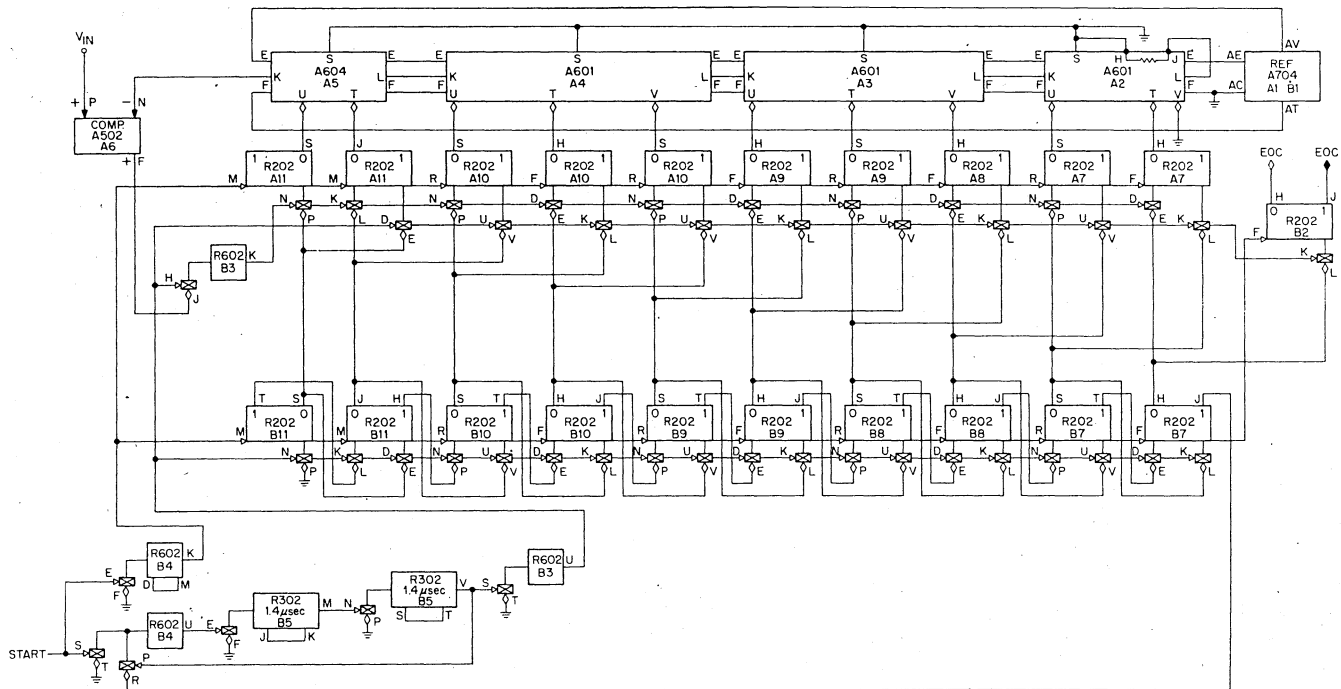
10-BIT ANALOG-DIGITAL CONVERTER

50/60 HERTZ BCD REAL TIME CLOCK
KIT C003

This kit is useful for applications in which it is desired to maintain a time of day reading, or to measure the time lapse of events, to provide time synchronizing signals, etc. The clock has built-in gating to permit connection of switches to preset the clock to the correct time of day; or for elapsed time measurements to clear the clock before use.

	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
									X X				X X X			
A	R 2 0 2	R 2 0 2	R 2 0 2	R 2 0 2	R 2 0 2	R 2 0 2	R 2 0 2	R 2 0 2	W 0 0 8	R 2 0 2	R 2 0 2	R 2 0 2	W 0 1 8	R 2 0 2	R 2 0 2	R 2 0 2
B	R 6 0 1	R 3 0 2	W 5 0 1	W 5 0 1	W 0 2 3	W 0 2 3	W 0 0 5	R 1 1 1	R 1 1 1	R 1 1 1	R 1 1 1	R 1 1 1	W 0 2 3	W 0 0 5	R 1 1 1	R 1 1 1
							x	x	x	x						

X	MODULES OMITTED IF SECOND SET NOT DESIRED
XX	MODULES OMITTED IF CABLE OUTPUTS OF SECOND COUNTER NOT DESIRED
XXX	MODULES OMITTED IF CABLE OUTPUTS OF HOUR AND MINUTE COUNTERS NOT DESIRED

MODULE LOCATION DIAGRAM (WIRING SIDE)

The following figure illustrates the required relative positioning of the three printed-circuit boards to each other when installed on a mounting panel. However, the boards need not occupy these particular socket positions.

bd. no. E869

bd. no. E870

bd. no. E007
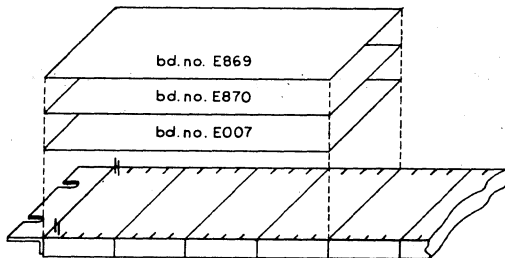
RELATIVE BOARD POSITIONS

It is suggested that the PANELAID boards be positioned approximately ½ inch apart and as close to the mounting panel as possible. This facilitates attachment of testing equipment or wiring to other devices.

The radix of the hertz counter may be set to either 50 or 60 by jumpers installed on the outer layer board. For a 50-hertz clock a jumper is installed between each pair of lugs with a "50" between them or for a 60-hertz clock a jumper is installed between lugs which have a "60" between them. These lugs are shown on the logic diagram.

CLOCK INPUTS: Should come from a network consisting of a small filament transformer, and a small integrator to filter high frequency noise from the line voltage. A cable socket input is provided. The input network must be supplied by the customer.

PRESET LEVEL INPUTS: Inputs are clamped to —3 volts which cause assertions of "ones" at the input gates. Decade switches used to generate preset levels must provide contact closures to ground to the level inputs to negate bits not to be set; connection to these inputs is via W023 boards in sockets provided.

PRESET PUSH BUTTON INPUT: A momentary contact closure presented between pins S and U of the W051 in B14 will generate the signals to read the contents of the preset switches into the hour, minute and second counters.

OUTPUT CABLING: The "1" side negative outputs of the hour, minute, and second counters are connected to two sockets to enable driving of indicators, connecting to other devices etc.
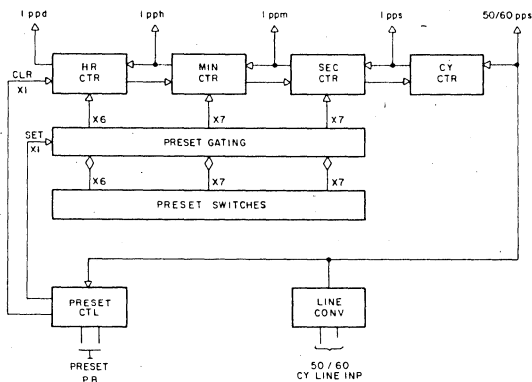
REAL TIME CLOCK BLOCK DIAGRAM

Equipment required and prices; excluding mounting panels, power supplies, and cabling are:

1 — E007	PANELAID for C003		1 — R302	Dual Delay
1 — E869	PANELAID for C003		1 — R601	Pulse Amplifier
1 — E870	PANELAID for C003		2 — W005	Clamped Loads
7 — R111	Diode Gates		2 — W501	Schmitt Trigger
14 — R202	Dual Flip-flop		2 — W018	Cable Connector

C003 — $639.00
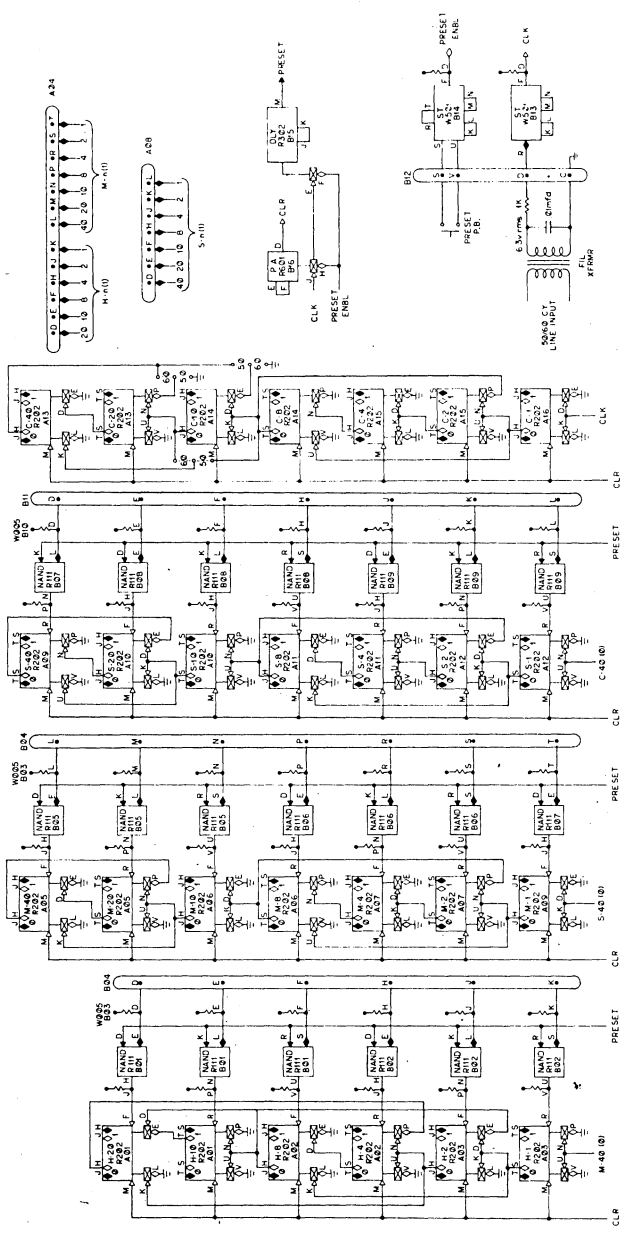
REAL TIME CLOCK

PDP-8/S I/O BUS INTERFACE
KIT C005

PANELAID
SERIES

This kit provides an interface for a grouping of six cables that parallel connect each peripheral device. Each device must have associated sockets to facilitate interconnection of peripheral gear and continuation of the I/O Bus cables. Six sockets must be provided for input cables and six for output cables.
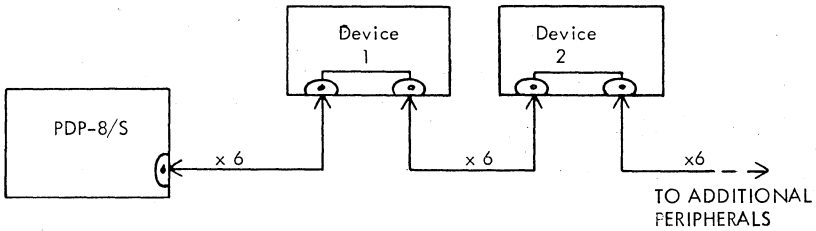
I/O BUS CONFIGURATION

The kit includes two printed-circuit boards, each six sockets wide by two sockets high. One board provides all the ground connections, the other all the wiring to parallel the two sockets for each cable.

The PANELAID boards should be positioned as close to the mounting panel surface (and each other) as possible, for easy attachment of test equipment or wiring to input-output devices.

PARTS LIST
1 — E001 PANELAID
1 — E002 PANELAID

C005 — $12.00

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PDP-8 or PDP-8/S
INPUT/OUTPUT BUFFER REGISTER
KIT C006

This kit includes a 12-bit register that may be loaded from the computer's accumulator register (AC); two device-selector modules to decode and generate the control or transfer pulses; input gating to the AC input lines; a flip-flop with one output connected to I/O Skip and Program Interrupt facilities; and a free flip-flop which may be used for enabling or controlling functions. A C005 PANELAID TM interface is used with each C006 to provide connections for the PDP-8 or PDP-8/S I/O Bus cables.

The following figures illustrate the required relative positioning of the C005 and C006 boards when installed on a mounting panel. Although relative board location is critical, the exact positioning of the kit, with respect to the mounting panel, is not.

	07	06	05	04	03	02	01	06	05	04	03	02	01
A	R205	R205	R205	R123	R202			I/O CABLE 5	I/O CABLE 5	I/O CABLE 3	I/O CABLE 3	I/O CABLE 1	I/O CABLE 1
						W I/O 3	W I/O 3						
B	R205	R205	R205	R123	R201			I/O CABLE 6	I/O CABLE 6	I/O CABLE 4	I/O CABLE 4	I/O CABLE 2	I/O CABLE 2

C006   C005

MODULE LOCATION DIAGRAM (WIRING SIDE)

E005
E004
E001   E003
E002

RELATIVE BOARD POSITIONS
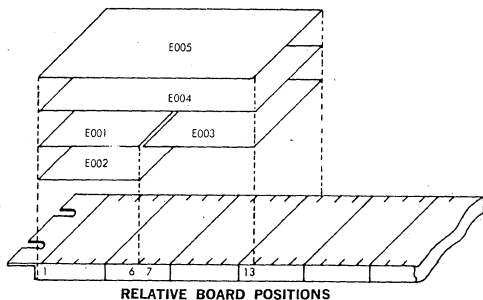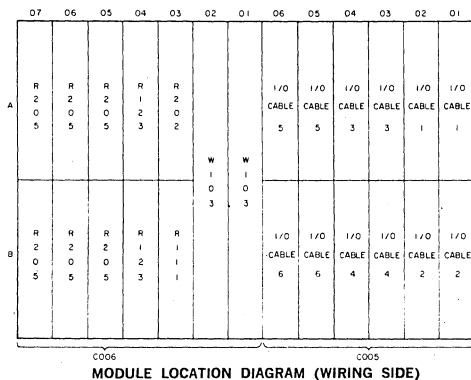
NOTE:

E001 and E002 are board numbers for kit C005

E003, E004, and E005 are board numbers for kit C006

The equipment required and prices, — excluding mounting panels and power supplies are:

1 — E001 PANELAID for C005
1 — E002 PANELAID for C005
1 — E003 PANELAID for C006
1 — E004 PANELAID for C006
1 — E005 PANELAID for C006

1 — R111 Diode Gate
2 — R123 Diode Gate
1 — R202 Dual Flip-flop
6 — R205 Dual Flip-flop
2 — W103 PDP-8 Device Selector

C006 — $397.00

Input/Output Buffer Register

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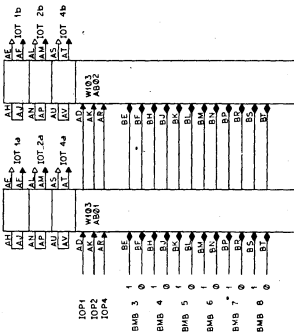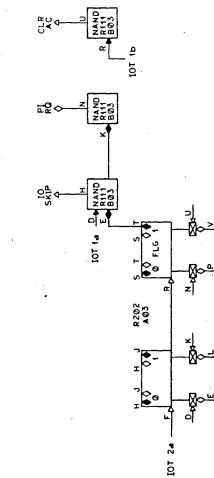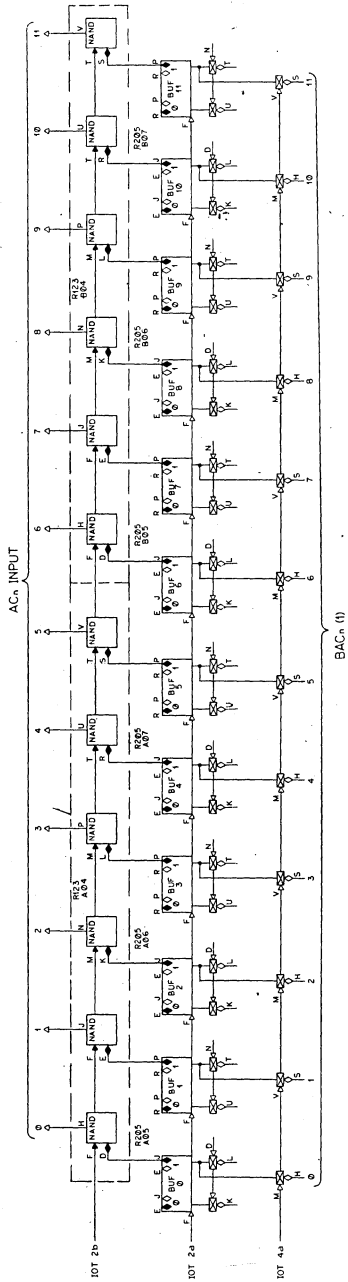
PDP 8/S INPUT INTERFACE
KIT C007

This kit provides cable connection sockets, device selection pulses, data input gates, and interrupt and skip facilities for interfacing two twelve bit words to the PDP-8/S.

In operation, the PDP-8/S will provide a device selection code and three I/O transfer pulses. These are decoded by a W103 device selector module, after the pre-selected device number is asserted, to generate the IOT 1, 2 and 4 pulses for local device usage.

Device number decoding is performed by selectively removing diodes from the input AND gate detect only the desired code.

Each set of input gates has its own flip-flop which should be set when data is ready to be transferred to the computer. This flip-flop enables the local device interrupt gate. The skip facility may be sampled by generating the appropriate device selector code and IOP1. IOP2 will clear the data transfer flop and IOP4 will strobe the data into the accumulator of the computer.

To interface only 1 set of 12 bit words, the standard kit should be ordered but with one W103 and two R123 modules deleted.

External Inputs Required: Data present pulse: —3 v to ground pulse with a maximum rise time of 60 ns. and a minimum duration of 100 ns. Load is 1 ma. at ground. Data input levels: —3 v level on the input to the R123 gate will be strobed into the computer as a logical one. A ground level represents a zero. Loading is 1 ma. at ground.

External Outputs: No outputs are required; however, information may be taken from the outputs of the Data Present flip-flops. A level of —3 v from either pin J or T of the R202 indicates data is present at the appropriate gate. A ground level signifies no data present. Each output can drive 13 ma. of external load at ground.
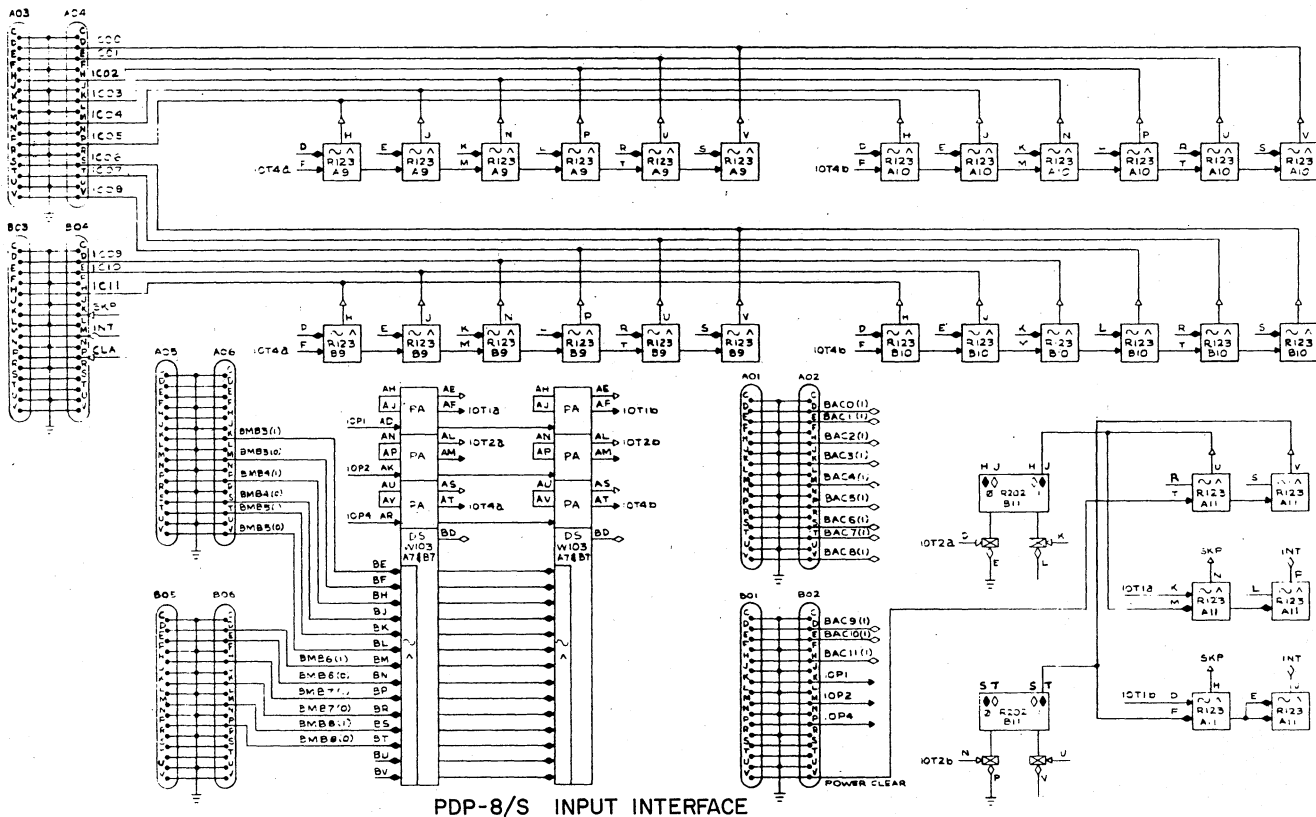
PDP-8/S INPUT INTERFACE

MODULE LOCATION DIAGRAM

1	2	3	4	5	6	7	8	9	10	11	
B A C 0 ↓ 8	B A C 0 ↓ 8	I A C 0 ↓ 8	I A C 0 ↓ 8	B M B 3 ↓ 5	B M B 3 ↓ 5	W 1 0 3	W 1 0 3	R 1 2 3	R 1 2 3	1 2 3 R	
B A C 9 ↓ 11	B A C 9 ↓ 11	I A C 9 ↓ 11	I A C 9 ↓ 11	B M B 6 ↓ 8	B M B 6 ↓ 8			R 1 2 3	R 1 2 3	R 2 0 2	

INPUT CONNECTIONS

	IAC0	IAC1	IAC2	IAC3	IAC4	IAC5	IAC6	IAC7	IAC8	IAC9	IAC10	IAC11	DATA PRESENT
BUFFER #1	A09S	A09R	A09L	A09K	A09E	A09D	B09S	B09R	B09L	B09K	B09E	B09D	B11K
BUFFER #2	A10S	A10R	A10L	A10K	A10E	A10D	B10S	B10R	B10L	B10K	B10E	B10D	B11U

PRICE

MODULE	QTY.	UNIT	TOTAL
R123	5@	19.00	95.00
R202	1@	25.00	25.00
W103	2@	52.00	104.00
H800	3@	8.00	24.00
C005	1@	12.00	12.00
E008	1@	9.50	9.50
E009	1@	9.50	9.50
			$279.00

Kit C009 contains an eight bit shift register made of four R202 flip-flops, one R401 clock, one R302 delay (one shot) one R602 pulse amplifier, one R113 NAND/NOR gate, one R111 expandable NAND/NOR gate, and one R002 diode board.

The C009 kit is primarily intended for use in providing the necessary timing and control functions for memory systems using the type H201 core memory.

The functional inputs (read request, write request, and memory power clear (—MPC)) as well as the functional outputs (read, strobe, inhibit 1, inhibit 2, write, and memory done) are brought to a common input/output point at location B06 on the mounting block. Location B06 has been designed so that the input/output signals may be taken to and from the C009 by a W021 or W011 cable connector, or hard wired directly to the pins. The cable connector and cable are offered as an option, and are not included in the price of the C009 kit.

All wiring connections are made on two printed circuit boards.

All pulse and level inputs to the C009 must be DEC standard pulses and levels of —3v and ground (Ov).

A common direct clear line (—MPC) is available for simultaneous clearing of all flip-flops in the shift register.

CIRCUIT OPERATION

Upon receipt of a read request or a write request, the memory done level goes negative to enable the R401 clock, which drives the switch tail ring counter through a total of 16 discrete counts. If the clock is set for a 2 MHS rate, one entire cycle of the counter will result in a memory cycle time of eight microseconds.

The decoding for the memory control signals, read, write, etc., are derived by looking at sets of outputs from the ring counter. (Example: write —⟨⟩ = FF/C (1)—◆ and FF/H (1)—◆)

With no read request or write request signal present, and the counter in all zero condition, memory done goes positive disabling the R401, leaving the counter in an all zero state at the end of each memory cycle.
For a complete description of timing, operation, and circuit adjustments, refer to the enclosed application note AP-H-001, and the attached timing diagram.

INPUT LOAD REQUIREMENTS

—MPC = ma at ground
R113 and R111 diode gate inputs = 1 ma at ground
R401 enable gate input (pin S) = 4 ma at ground
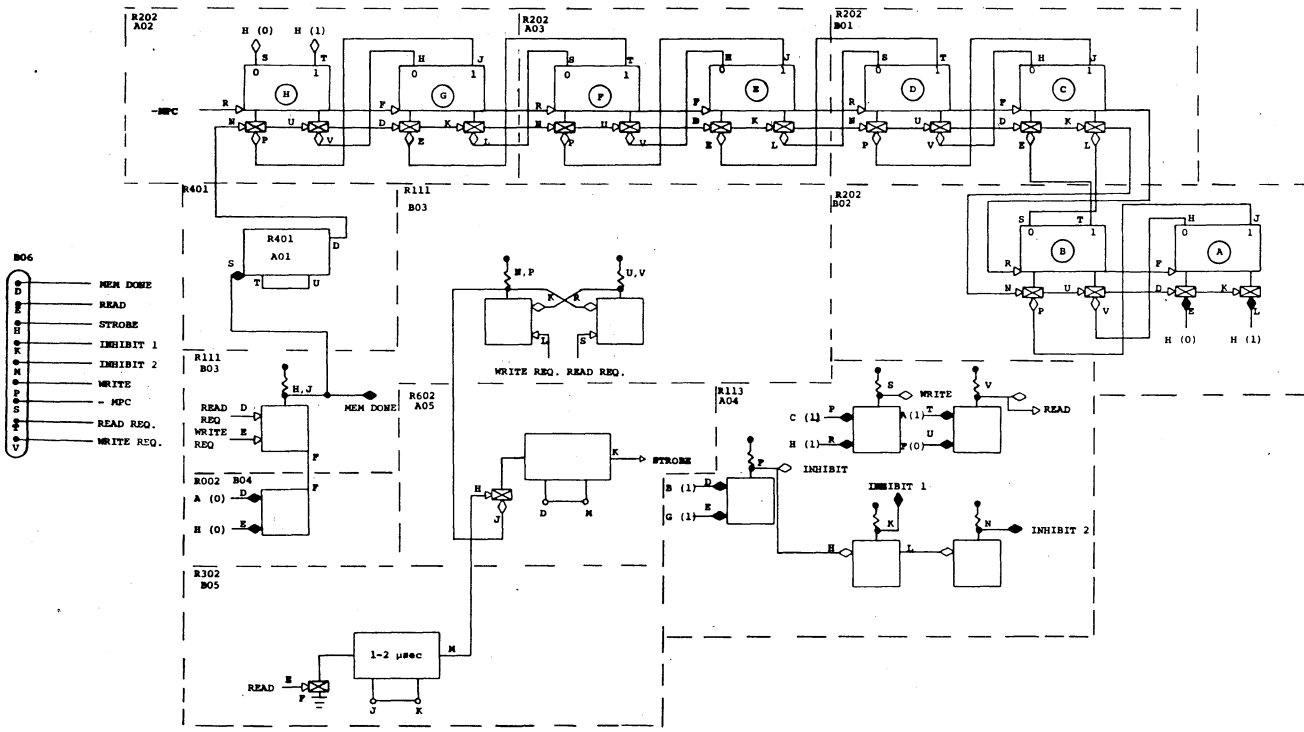
MEMORY TIMING AND CONTROL

TIMING DIAGRAM

|← 8 μSEC. →|

0 V
READ/WRITE
REQUEST
-3V

0 V
MEMORY
DONE
-3V

01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16

0 V
CLOCK
-3V

0 V
READ
-3V

2.5 μSEC.

0 V
STROBE
-3V

1 μSEC. | 2 μSEC.

0 V
INHIBIT
-3V

* 5
μSEC.

1.5 μSEC.

0 V
WRITE
-3V

1.5 μSEC.

|← 3 μSEC. →|
ALLOTTED FOR
W108 & W532
RECOVERY
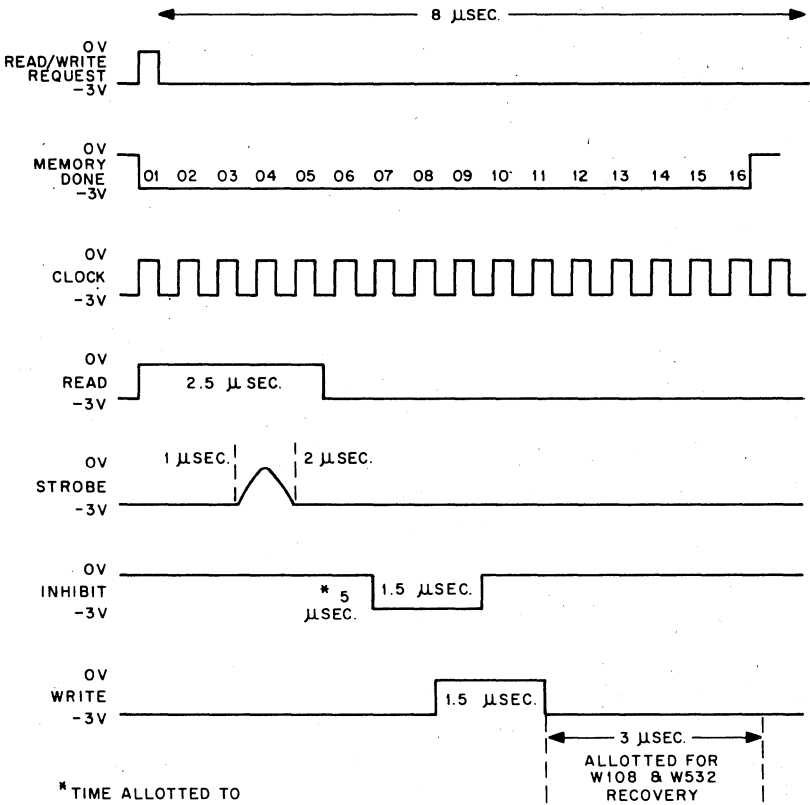
* TIME ALLOTTED TO
UPDATE MEMORY BUFFER

KEY: EACH SQUARE EQUALS .5 μSEC.

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	A	B	C	D	E	F	G	H
1	0	0	0	0	0	0	0	0
2	1	0	0	0	0	0	0	0
3	1	1	0	0	0	0	0	0
4	1	1	1	0	0	0	0	0
5	1	1	1	1	0	0	0	0
6	1	1	1	1	1	0	0	0
7	1	1	1	1	1	1	0	0
8	1	1	1	1	1	1	1	0
9	1	1	1	1	1	1	1	1
10	0	1	1	1	1	1	1	1
11	0	0	1	1	1	1	1	1
12	0	0	0	1	1	1	1	1
13	0	0	0	0	1	1	1	1
14	0	0	0	0	0	1	1	1
15	0	0	0	0	0	0	1	1
16	0	0	0	0	0	0	0	1

READ

WRITE

INHIBIT

MEMORY DONE

OUTPUT DRIVE CAPABILITIES

R202 "one" side output = 15 ma at ground
R202 "zero" side output = 15 ma at ground
R113 output terminal = 18 ma at ground
R111 output terminal = 18 ma at ground
R401 output terminal = 70 ma at ground
R602 output terminal = 70 ma at ground
R302 output terminal = 18 ma at ground

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MODULE LOCATION DIAGRAM

(CO 09)

	01	02	03	04	05	06	07	08
A	R 4 O 1	R 2 O 2	R 2 O 2	R 1 1 3	R 6 O 2			
B	R 2 O 2	R 2 O 2	R 1 1 1	R O O 2	R 3 O 2	W021 MEM DONE READ STROBE INHIBIT 1 INHIBIT 2 WRITE −MPC READ REQ WRITE REQ		

PRICING

MODULE	QUANTITY	UNIT PRICE	TOTALS
R401	1	$ 45.00	$ 45.00
R202	4	25.00	100.00
R113	1	20.00	20.00
R111	1	14.00	14.00
R002	1	5.00	5.00
R602	1	22.00	22.00
R302	1	44.00	44.00
H800W*	2	8.00	16.00
Panelaid	2	9.50	19.00
		$192.50	$285.00

NOTE: If the panelaid is to be used on a customer's existing type 1943 or H900 mounting panel, the price of the H800W connector block may be deleted from the kit.

PRINTED CIRCUIT BOARDS

E and F SERIES

The E and F series are the printed circuit back panels used in the OCTAID and PANELAID Kits. These back panels may be ordered separately by those who already have the required Flip-Chip modules and connectors. Where a kit includes more than one board, all boards must be used to perform the indicated functions.

PRICE LIST

KIT NUMBER	KIT NAME		PRICE*
C001	Analog-Digital Converter Kits	E724	$11.50
C001A		E725	11.50
C002		E726	11.50
		E727	11.50
		TOTAL	$46.00
C003	50/60 Hertz BCD Real Time Clock	E869	16.00
		E007	16.00
		E870	16.00
		TOTAL	$48.00
C005	PDP-8/S IO Bus Interface	E001	6.00
		E002	6.00
		TOTAL	$12.00
C006	PDP-8 and PDP-8/S Input Output Buffer Register	E001	6.00
		E002	6.00
		E003	10.00
		E004	10.00
		E005	10.00
		TOTAL	$42.00
C007	PDP-8/S Input Interface	E008	$ 9.50
		#009	9.50
		TOTAL	$19.00
C009	Memory Timing and Control	E010	$ 9.50
		E011	9.50
		TOTAL	$19.00

*If the board fits over only one H800 connector block it will be identified by an F and three digits. If the board fits over more than one H800 it will be identified by an E and three digits. Any Octaid kit (D series) can contain only F series boards. However, any Panelaid kit may contain both E and F series boards.

KIT NUMBER	KIT NAME		PRICE*
D001A-F	Digital-Analog Converter	F728	2.25
		F843	-2.25
	TOTAL		$ 4.50
D002	BCD Up-Counter	F723	4.50
D004	Bi-Directional Decode Counter	F861	$ 5.70
	(Converter and Decoder Options)	F862	5.70
	TOTAL		$11.40
D006	PDP-8/S Output Buffer Register	F001	2.25
		F004	2.25
	TOTAL		$ 4.50
D007	Single or Dual 8-Bit Shift Register	F005	4.50
		F006	4.50
	TOTAL		$ 9.00
D008	Single or Dual 8-Bit Up-Counter	F007	4.50
		F008	4.50
	TOTAL		$ 9.00

PART V: ANALOG - DIGITAL CONVERSION HANDBOOK

PREFACE

The Analog-Digital Conversion Handbook represents the first attempt in the data processing industry to assemble comprehensive information on this subject in a form that makes it immediately useful to beginner or expert. All phases of conversion are covered, from concepts to calibration. Many diagrams supplement the text; and tabular summaries of terms, methods, and performance characteristics are included for comparison and reference. Circuit modules and other equipment manufactured by Digital Equipment Corporation are mentioned specifically, so after choosing the conversion method most appropriate to his needs, the reader can construct his system directly.

The use of circuit modules in constructing analog-digital converters yields several advantages. First, they are flexible. Converter systems have widely varying requirements, from pulse height analysis, where differential linearity is of utmost importance, to time-locked averaging in biomedical work, where resolution is more critical than repeatability or even accuracy. Modules permit the construction of the exact type of converter needed and, should requirements change, the same modules can be used later to build a different kind of system.

Second, modules are economical. Aside from the interchangeability mentioned above, savings are gained in the cost of construction. The typical cost of a digital-to-analog converter is about $1,000; of an analog-to-digital converter, about $2,000. If several systems are built, the cost per converter decreases since the same power supplies and mounting panels are used for the additional units. If the speed requirement is exceptionally high, costs will be higher.

A third advantage of using modules is that the completed converter need never go back to the factory for recalibration. Procedures for calibration and adjustment are included in this handbook. Recalibration can be carried out quickly and easily by the user.

Those modules designed exclusively for use in conversion systems are specified in detail in this handbook. The general purpose logic modules also needed are mentioned by name and type number. Complete specifications for these and over 200 other kinds of circuit modules and accessories are contained in another part of this handbook.

CHAPTER I

BASIC ELEMENTS OF CONVERSION

Introduction

This chapter describes the general technique used to convert, to sample and hold, and to multiplex.

For digital-to-analog conversion, just one technique is described. Though there may be some variations, the same technique is generally applicable for all digital-to-voltage or digital-to-current converters.

Analog-to-digital conversion is somewhat more complex and thus a variety of different methods is commonly used. In this chapter, the four most common methods are described. Of these, the successive approximation converter is most generally used since it provides good performance over a wide range of applications at a reasonable cost. However, if the converter is to be used only in a single application, various other methods may be preferred for better performance or lower cost.

It is suggested that this chapter be read as a brief development of the principles of conversion, rather than a delineation of specific methods. Detailed descriptions of conversion systems will be given in Chapters 3 and 4.

Digital-to-Analog Conversion

To convert from a digital number to an analog voltage, a resistive divider network is connected to the flip-flop register which holds the digital number (see Figure 1). The divider network is weighted so that each bit of the register will contribute to the output voltage in proportion to its value.

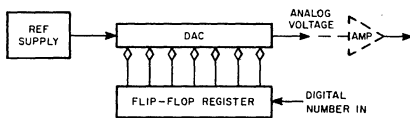
Figure 1. Digital-to-Analog Conversion

The digital input signal determines the analog output voltage, since the divider network is simply a passive element. However, because digital voltage levels are not usually as precise as required in an analog system, level amplifiers are placed between the flip-flops and the divider network. The amplifiers switch the divider network between ground and a

reference voltage supplied by a precision reference supply. The output voltage range is between these two voltage levels. In Digital systems, the range is normally 0 to —10 volts. If the digital-to-analog converter is to drive a long cable or a heavy load, an operational amplifier or emitter follower is usually put on the output of the circuit to lower the output resistance. The digital-to-analog converter and reference supply shown in Figure 1 are basic to a digital-to-analog converter and are described under those headings in Chapter 5.

Analog-to-Digital Conversion

The basis of analog-to-digital conversion is the comparator circuit. This circuit compares an unknown voltage with a reference voltage and indicates which of the two is larger.

SIMULTANEOUS METHOD

Figure 2 shows how a simple simultaneous analog-to-digital converter can be built using several comparator circuits. Each comparator has a reference input signal. The other input terminal of the comparators is driven by the unknown input analog signal, which is between 0 and V volts. The comparator is called "ON" if the analog input is larger than the reference input. Then, if none of the comparators are on, the analog input must be less than $\frac{V}{4}$. If C-1 is on, and C-2 and C-3 are off, the input must be between $\frac{V}{4}$ and $\frac{V}{2}$. Similarly, if C-1 and C-2 are on, and C-3 off the voltage is between $\frac{V}{2}$ and $\frac{3V}{4}$; and if all the comparators are on, the voltage is greater than $\frac{3V}{4}$.

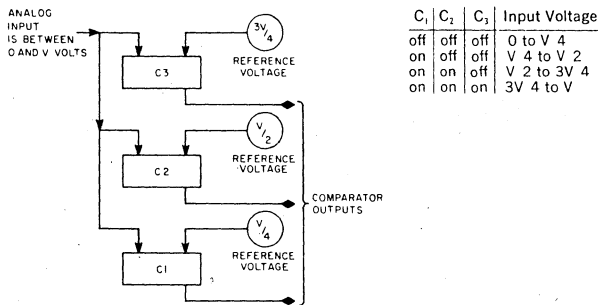| C_1	C_2	C_3	Input Voltage
off	off	off	0 to V 4
on	off	off	V 4 to V 2
on	on	off	V 2 to 3V 4
on	on	on	3V 4 to V

Figure 2. Simultaneous Analog-to-Digital Converter

Here, the voltage range is divided into four parts, which can be coded to give two binary bits of information. Seven comparators would give three bits of binary information. Fifteen comparators would give four bits. In general, $2^N - 1$ comparators will give N bits of binary information.

The simultaneous method is extremely fast for small resolution systems. For large resolution systems (a large number of bits), this method requires so many comparators that it becomes unwieldly and prohibitively costly.

FEEDBACK METHODS

If the reference voltage were variable, only one comparator would be needed. Each of the possible reference voltages could be applied in turn to determine when the reference and the input were equal. But a digitally controlled variable reference is simply a digital-to-analog converter. Thus the generalized analog-to-digital converter shown in Figure 3 is actually a closed-loop feedback system. The main components are the same as a digital-to-analog converter plus the comparator and some control logic. With a digital number in the DAC (digital-to-analog converter) the comparator indicates whether the corresponding voltage is larger or smaller than the input. With this information, the digital number is modified and compared again.
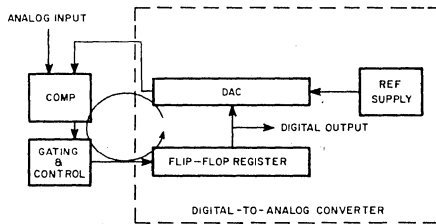
Figure 3.   Analog-to-Digital Converter Incorporating Digital-to-Analog Conversion Modules

COUNTER METHOD

Numerous methods may be used for controlling the conversion. The simplest way is to start at zero and count until the DAC output equals or exceeds the analog input.

Figure 4 shows a converter in which the DAC register is a counter, and a pulse source has been added. The gate stops pulses from entering the counter when the comparator indicates that the conversion is complete.
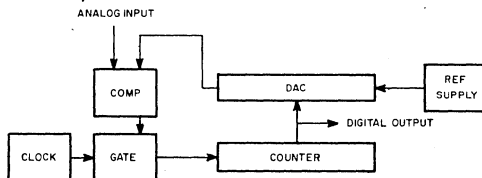
Figure 4. Counter Converter

The counter method is good for high resolution systems: As the number of bits is increased, very little additional circuitry is needed. Multiple inputs can easily be converted simultaneously (as described under Multiplexing later in this chapter). However, conversion time increases rapidly with the number of bits, since an N-bit converter must allow time for 2^N counts to accumulate. The average conversion time will, of course, be half this number.

CONTINUOUS METHOD

A slight modification of the counter method is to replace the simple counter with an up-down counter as in Figure 5. In this case, once the proper digital representation has been found, the converter can continuously follow the analog voltage, thus providing readout at an extremely rapid rate. This method, called continuous conversion, is particularly useful when a single channel of information is to be converted. The converter starts running, and the digital equivalent of the input voltage can be sampled at any time.
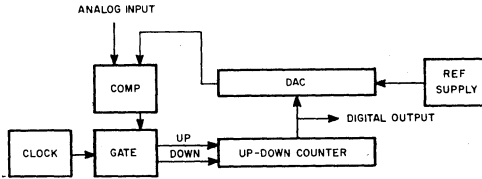
Figure 5. Continuous Converter

The continuous method is less effective for multiple inputs or for inputs that change faster than the converter can change. Each time the input makes a large change, the converter may require as many as 2^N steps to catch up. However, if a rapid rate of change is necessary, extra comparators may be added so that the up-down counter can count in units of 2, 3, 4, or more (see Chapter 3).

SUCCESSIVE APPROXIMATION METHOD

For higher speed conversion of many channels, the successive approximation converter is used. This method requires only one step per bit to convert any number. The successive approximation analog-to-digital converter operates by repeatedly dividing the voltage range in half as follows:
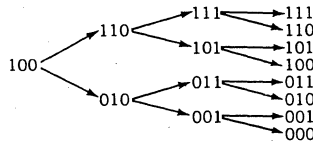
Thus, the system first tries 100, or half scale. Next it tries either quarter scale (010) or three-fourths scale (110) depending on whether the first approximation was too large or too small. After three approximations, a 3-bit digital number is resolved.

Successive approximation is a little more elaborate than the previous methods since it requires a control register to gate pulses to the first bit, then the second bit, and so on. However, the additional cost is small and the converter handles all types of signals about equally fast.
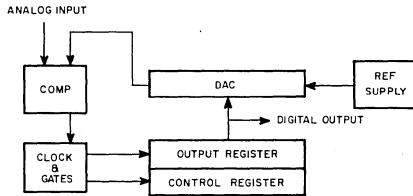
Figure 6. Successive Approximation Converter

The successive approximation method is good for general use. It handles many continuous and discontinuous signals and large and small resolution conversions at a moderate speed and moderate cost.

Sample and Hold

A sample and hold circuit is used with an analog-to-digital converter when it is necessary to convert a signal which changes too rapidly to allow an accurate conversion. A digital signal from some timing device can signal the sample and hold to hold the analog voltage present on its input until a time when the converter has completed its operation. The sample and hold is basically an operational amplifier which charges a capacitor during the track or sample mode, and retains the value of the charge of the capacitor during the hold mode.

The acquisition time of a sample and hold is the time required for the capacitor to charge up to the value of the input signal after the switch is first shorted. The aperture time (see definition, Chapter 2) is the time required for the switch to change state and the uncertainty in the time that this change of state occurs. The holding time is the length of time the circuit can hold a charge without dropping more than a specified percentage of its initial value.

The sample and hold circuit can be represented as shown in Figure 7. When the switch is closed, the capacitor is charged to the value of the input signal; then it follows the input. When the switch is opened, the capacitor holds the same voltage that it had at the instant the switch was opened.
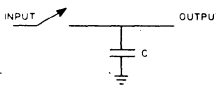
Figure 7 Sample and Hold

It is possible to build a sample and hold circuit just as shown here. Often, the same circuit is used with a high gain amplifier to increase the driving current available into the capacitor or to isolate the capacitor from an external load on the output. In some cases, this sample and hold is made entirely differently; but from a logical point of view, it acts as the ideal component shown.

Figure 8 shows a sample and hold built with an A200 amplifier board and an A121 multiplexer switch.

In Track sample, the hold capacitor is charged up by the operational amplifier; in Hold, the capacitor is switched into the feedback loop. The input resistor and the feedback resistor are switched to ground. Since the input to the amplifier remains within a few microvolts of ground (except during switching), the input impedance is 10,000 ohms to ground both in Track and Hold. The offset input allows a precise dc level to be added to the input so that the output of the sample and hold is shifted by this value.

These principles have been incorporated into the A400 sample and hold.
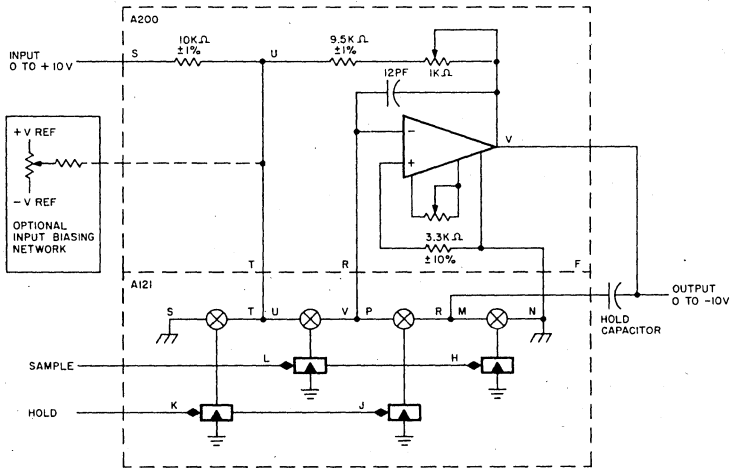
Figure 8.   Sample And Hold System

TYPICAL SAMPLE AND HOLD PERFORMANCE

INPUT: 0 to +10 volts
OUTPUT: 0 to −10 volts
ACCURACY: ±0.05% for 10 μs
      sample, 5 ms — hold
INPUT IMPEDANCE: 10KΩ
Higher resistances in A200 will increase input inpedance at the cost of increased acquisition time, reduced accuracy or both.
OUTPUT IMPEDANCE: <10Ω

NOTE: For best noise rejection keep amplifier negative input lead short and add two 0.01 mfd capacitors from supply pins to analog ground (pin F) within A200.

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REDUCING THE APERTURE OF AN A/D CONVERTER A400

In the process of quantizing dynamic signals, an area of uncertainty exists which is a function of the aperture time of the analog to digital converter. Aperture time, as used in this case, is the amount of time which the converter must see the input signal to perform a complete conversion. The uncertainty arises when the input signal changes by an amount greater than the resolution of the analog to digital converter during the aperture time. A sample and hold is used to decrease the effective aperture time and increase the effective bandwidth of the converter. The maximum frequency that an analog to digital converter or sample and hold circuit can handle can be calculated by determining the maximum rate of change of voltage with respect to time.

This is illustrated in Figure 1.

$$e(t) = E_p \sin wt$$

$$\frac{de}{dt} = wE_p \cos wt$$

The derivative is maximum at zero.

$$\left.\frac{de}{dt}\right|_0 = E_p w \qquad \text{where } E_p = \text{peak voltage}$$

$$w = 2\pi f \text{ (Hz)}$$

The aperture, $\triangle T$ is approximately equal to dt and the resolution $\triangle E$ is approximately equal to de.

Substituting and rearranging,

$$f = \frac{\triangle E}{2\pi E_p \triangle T}$$

Figure 2 is a chart showing the relationship between resolution (in percent of full scale), aperture, and frequency based on the above relationship.

The following table compares the performance of several Digital Equipment Corporation Analog to Digital Converters with and without the A400 Sample and Hold.

A/D Converter	Aperture	Resolution	Frequency
AF01, ADC-1	35 usec	0.025%	2.2 cps
AF01, ADC-1	9 usec	1.56 %	520 cps
A801	10 usec	0.1 %	30 cps
With A400 Sample and Hold			
AF01, ADC-1	150 nsec	0.025%	540 cps
AF01, ADC-1	150 nsec	1.56 %	60,000 cps
A801	150 nsec	0.1 %	25,000 cps

Figure 3 shows the output of a Sample and Hold circuit sampling a sine wave at 30° intervals.
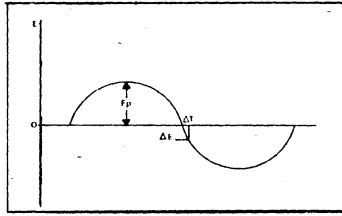
FIGURE 1

GRAPH OF E_ρ Sin ωt SHOWING THE RELATIONSHIP
OF RESOLUTION, APERTURE AND FREQUENCY
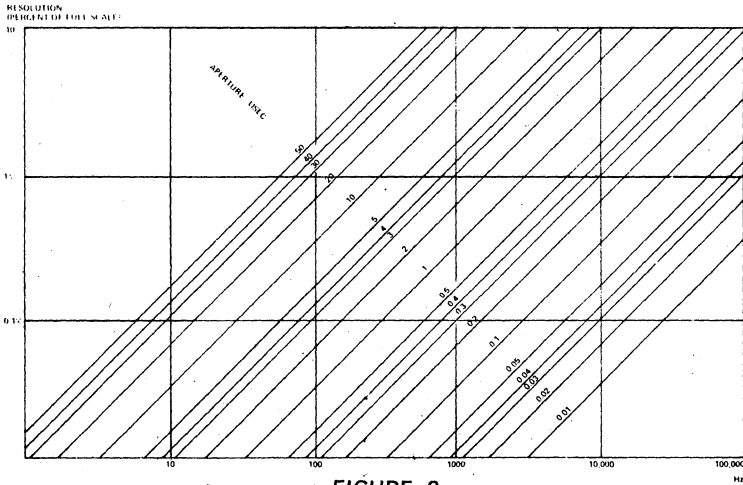
FIGURE 2

CHART OF UPPER FREQUENCY VS. RESOLUTION
AS A FUNCTION OF APERTURE
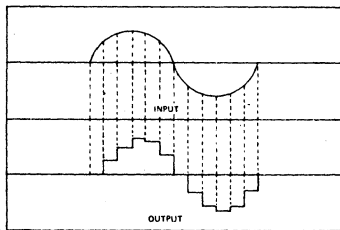
FIGURE 3

THE A400 OUTPUT FOR A SINGLE CYCLE
SINEWAVE INPUT, SAMPLED AT 30° INTERVALS

Effect of Bandwidth on Accuracy A400

It is common to use the frequency domain to characterize signals to be processed. Generally, one speaks of the bandwidth requirement. It is necessary to consider the effect of all the elements in the signal path to determine overall accuracy which is to be attained.

Figure 1 shows the frequency characteristics of the A400 in "TRACK" or Sample.

At DC it displays unity gain, rolling off 6 db/octave (20 db/decade) at 110 KHz. It can therefore be considered a single-pole lag network, or more simply a low-pass RC circuit.

Most applications of this circuit will be in low bandwidth situations and it is of interest to be able to calculate the attenuation of the A400 at low frequencies. This can be done easily by the following approximation:

$$E = \frac{e_{in} - e_{out}}{e_{in}} \cong \frac{1}{2} \left(\frac{f}{110 \ KHz} \right)^2$$

Where E is the error and f is the input frequency. The approximation is accurate to better than 0.012% below 10 KHz, and is accurate to 21.7% at the 6 db point (110 KHz).

Multiplying E by 100 will give the percent of error. Note also that if the equation is rewritten,

$$E = \frac{1}{2} \left(\frac{f}{110 \ KHz} \right)^2 e_{in}$$

the E will be in millivolts if e_{in} is in millivolts. This is convenient since converter accuracies are often in millivolts or in percentage of full scale. (Since DEC A/D converters are usually 10 volts full scale, the two numbers turn out to be the same; 0.025% is 0.0025 volts or 2.5 mv.)
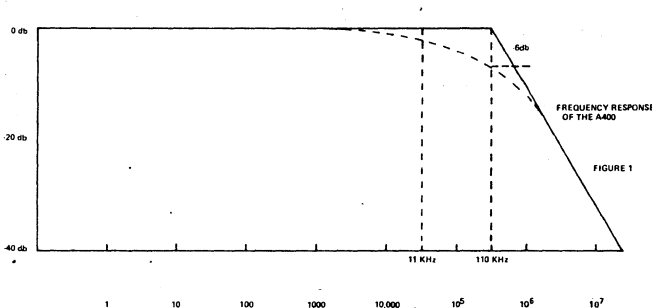
FREQUENCY RESPONSE OF THE A400
FIGURE 1

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Rise time — Bandwidth relationships A400

The bandwidth of sample and hold circuits is not normally specified. But this parameter can be inferred from the rise time specification as it is assumed that the frequency characteristic rolls off at 6db/octave. Then a simple low-pass RC circuit serves as a model. This bandwidth, which is defined as the point where the response is 6db down from DC, is given by $f = f_0 = \dfrac{1}{2\pi RC}$.

The product of R and C also determines the rise time of the circuit.

From these two statements it follows that:

$$f_0 = \frac{K}{2\pi T}$$

where f_0 = corner frequency
T = rise time
K is a constant

The constant is required because of the way in which rise times are specified (that is, the rise time is specified as the time required to achieve a certain accuracy). Therefore K can be obtained from the log-log scales of the slide rule or from log tables. They are given here for the most common accuracy specifications:

accuracy (%)	K
1 -	4.6
0.1	6.9
0.025	8.3
0.01	9.2

Example: From the following specifications on ·sample and hold circuits, calculate the band width:

Type A rise time, 5 usec to 0.01%
Type B rise time, 1 usec to 0.1%
Type C rise time, 12 usec to 0.025%

Type A:
$$f_0 = \frac{9.2}{2\pi \times 5 \times 10^{-6}} = 293 \text{ KHz}$$

Type B:
$$f_0 = \frac{6.9}{2\pi \times 1 \times 10^{-6}} = 1.085 \text{ MHz}$$

Type C:
$$f_0 = \frac{8.3}{2\pi \times 12 \times 10^{-6}} = 110 \text{ KHz}$$

Note that the time constants of the circuits are:

$$\frac{T}{K}$$

For the A400, the time constant is:

$$\frac{12}{8.3} = 1.45 \ \mu\text{sec}$$

Multiplexing

Often it is desirable to multiplex a number of analog channels into a single digital channel or conversely a single digital channel into a number of analog channels. Multiplexing can take place in the digital realm, the analog realm, or in the conversion process.

DIGITAL-TO-ANALOG

In digital-to-analog conversion, a common problem is to take digital information which is arriving sequentially from one device, such as a digital computer, and to distribute this information to a number of analog devices. Usually it is necessary to hold the information on the analog channel even when it is not being addressed from the digital device. There are two ways to multiplex. A separate digital-to-analog converter may be used for each channel as shown in Figure 9.
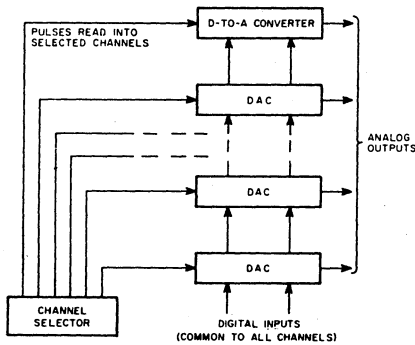
Figure 9. Digital-to-Analog Systems

In this case, the storage device is a digital buffer associated with the d-a convertor. Or, a single digital-to-analog convertor may be used, together with a set of analog multiplexing switches and a sample and hold circuit on each analog channel. The cost of the first method is slightly more than the cost of the second method, but it has the advantage that the information can be held on the analog output for an indefinite period of time without deteriorating. With the multiple sample and hold technique, however, it is necessary to renew the signal on the sample and hold at periodic intervals.

ANALOG-TO-DIGITAL

In analog-to-digital conversion, it is more common to multiplex the inputs in the analog realm. Here switches, either relays or solid state, are used to connect the inputs to a common bus. This bus goes into a single analog-to-digital converter which is used for all channels (see Figure 10). If simultaneous time samples from all channels are required, a sample and hold circuit can be used ahead of each multiplexer switch. In this way, all channels would be sampled simultaneously and then switched to the converter sequentially. The multiplex switches and sample and holds will introduce some error into the system. However, it is usually less expensive to go to higher quality sample and hold and multiplex circuits than add extra converters.
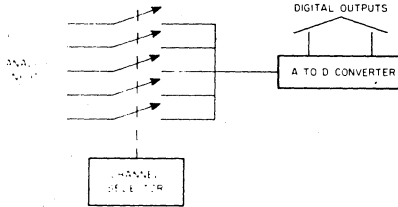
Figure 10. Multiplexed Analog-to-Digital Conversion System

In a simple analog-to-digital converter with a single comparator circuit, it is also possible to multiplex by using a separate comparator for each analog channel. One input of each comparator is tied to the voltage generating device in the converter. The other inputs are tied to the separate analog channels. The comparator to be used can be selected digitally. This method is particularly good when a small number of channels is to be multiplexed since it is quite simple and requires little additional control. For a large number of channels, separate multiplexer switches are usually less expensive and more accurate as they do not put any load on the voltage generating device of the converter.
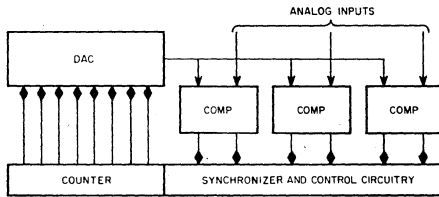
Figure 11. Counter Type Analog-to-Digital Converter with Multiplexed Input

The comparator multiplexing technique is particularly useful with the counter type analog-to-digital converter. This technique is shown in Figure 11. Several comparators are attached to one converter. The counter is cleared; then count pulses are applied. When one of the comparators signals that the digital-to-analog output is greater than the input voltage on that channel, the contents of the counter are read out. Counting is then resumed until the next signal is received.

CHAPTER 2
MEASURES OF CONVERTER PERFORMANCE
Accuracy

Since the end result of conversion is the representation of a given value in different terms, it is important to know how accurate the representation is. In systems where accuracy requirements are not too stringent, say in the order of 1 percent, an overall accuracy specification is usually sufficient. In cases where the desired accuracy is 0.1 percent or greater, it is necessary to isolate the various sources of error; and since a converter is a hybrid device, both digital and analog sources must be taken into account.

In high accuracy systems particularly, accuracy figures given in the general specifications may not include isolated sources of error, e.g., noise. Thus, it is important to know the various types of errors, their causes, how they are measured and specified, and when they are important. Figure 12 shows a breakdown of various types of errors.
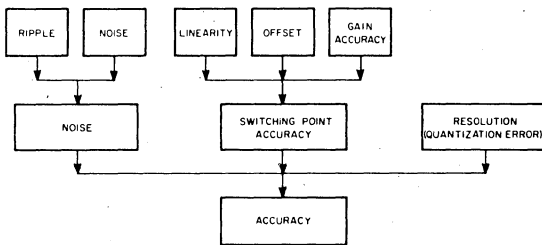
Figure 12. Measures of Cumulative Error

DIGITAL ERROR SOURCES

When a continuous signal is quantized, there is an error which is equal in magnitude to the smallest quantum. For a linear converter, the smallest quantum is the least significant bit. In most converters the quantization error is centered so that it is equal to $-\frac{1}{2}$ the least significant bit, written as $-\frac{1}{2}$ LSB.

In a continuous converter or digital voltmeter, accuracy may not be as important as avoiding chatter. That is, if the input is right on the dividing line between two quantization states, the output should not oscillate. If hysteresis is introduced so that the quantization error is just under -1 LSB, then oscillations will normally be avoided and the accuracy will not be greatly impaired.

The digital-to-analog converter reproduces exactly all the digital input information which it accepts. Hence digital error is not included in its accuracy specifications. However, if the input has more bits than the converter, there will be a quantization error in the readin process which should be taken into account. If desired, a ½ LSB offset can be built into the converter so that the readin will round off, rather than truncate, more precise digital information.

ANALOG ERROR SOURCES

The dc accuracy of the converter (or switching point accuracy) depends on the offset, the gain calibration, and the linearity. Nonlinearities are due to the variation in gain (or common mode effect) in going from the smallest input to the largest input. Some of these will be long-term, because of the common mode effect of the comparator circuit in the analog-to-digital converter, for example. Some will be shorter term, because of discontinuities in the divider network or insufficient settling time of the comparator. The offset and the gain can be adjusted in the calibration until their effects are essentially negligible.

The measurement of analog error in a digital-to-analog converter is easily made by putting in a digital number (the same word length as the converter) and observing the output. In an analog-to-digital converter, the analog error is difficult to locate since the quantization error is always present. However, the point where the output oscillates approximately equally between two neighboring digital numbers is fairly well-defined. This point, called the switching point, can be measured and compared with the theoretical value.

The ripple on the reference supply and other sources of noise are often measured separately since one or the other can sometimes be neglected in the final result. The two can be separated by measuring the ripple in the reference supply and subtracting it from the measured noise, or by running the input source in the converter from the same reference, thereby giving a direct measurement of all noise sources except the reference supply ripple. In a digital-to-analog converter the noise and ripple can be measured by observing the output with a scope. In an analog-to-digital converter they can be measured by observing the input range which causes the output to oscillate between two states.

DIFFERENTIAL LINEARITY

Differential linearity is the variation in the size of the required voltage change that causes an analog-to-digital converter to go from one switching point to another. That is, it is the variation in the size of the states and is generally quoted as a percent of the size of the states. It is a part of the overall linearity discussed above, but deserves special mention because of its importance when an analog-to-digital converter is being used in histogram applications. For example, when plotting the number of inputs versus the digital state, if one of the states is twice as big as its neighbor, it will tend to accumulate twice as many counts. Naturally, a very misleading output results.

Differential linearity is one of the few accuracy characteristics which is affected by the conversion technique. The differential linearity tends to be best when the converter goes

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through all the states sequentially as in the counter type converter described in Chapter 1 or the ramp variation described in Chapter 3. In an approximation converter, such as the successive approximation type, the large transients which result in going from, say, half scale to quarter scale require a long time to settle down, and any hysteresis in the comparator circuit causes relatively large variations in the state size. However, the differential linearity of an approximation converter can be improved by running it at very low speed. Differential linearity is also affected by variations in the divider networks (although they are relatively small). It can be avoided by using a ramp converter.

The shorter the converter word length, of course, the better the differential linearity will tend to be. However, this gain may well be compromised, since small resolution could result in the loss or the smoothing of very sharp peaks in the histogram.

Techniques commonly used to overcome difficulties with differential linearity are: changing the offset on the converter (or equivalently the bias on the input signal) and changing the word length of the converter. Switches can be mounted on the converter for this purpose, or the change can be made programmable so that the controlling device can make the change automatically.

DISTRIBUTION OF ERROR

How much of the total error should be in the digital circuitry and how much in the analog portion? For converters in the range of up to 10 or 11 bits, the digital error generally accounts for about $\frac{1}{3}$ to $\frac{1}{2}$ of the total. Thus, a typical 10-bit system would have a quantization error of $\pm\frac{1}{2}$LSB and an analog error of $\pm$ 0.1%.

If the accuracy requirement is low, the word length may be the major source of error. The total error may then be treated simply as round-off. If the accuracy requirements are stringent, it is desirable to minimize all sources of error, analog and digital. The digital error is quite simple to minimize by extending the number of bits within practical limits. A converter with an overall error of 0.1% and a word length of 20 bits would be unjustified.

Requiring monotonicity is one way to assure that all the bits are meaningful. This means that all states must exist and they must be in the correct order. In terms of converter operation, as the number going into the digital-to-analog converter is increased, the output voltage must also increase; it should never dip back down at any point. Similarly, if the input voltage to an analog-to-digital converter is increased, the digital output should stay at the same value or increase and should not skip over any states.

The converter is most likely to lose monotonicity when switching between digital states such as 0111 and 1000. If the weighting of the bits is not quite correct, in a digital-to-analog converter the higher state might correspond to a lower voltage, and in the analog-to-digital converter the output might jump directly from 0110 to 1000.

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Measures of Speed

DIGITAL-TO-ANALOG CONVERSION

The maximum conversion rate is theoretically limited only by the minimum time between readins to the converter flip-flops, and can easily be as high as 10 megacycles. However, such a figure may be misleading. The desired ratio of settling time to non-settling time usually determines the maximum usable conversion rate.

The settling time of a converter is measured from the time the digital readin is performed to the time when the analog output has settled to within the specified limits of accuracy. How the output approaches its final value depends on the output circuit, as discussed below.

The divider output will have high frequency transients before it begins to settle. If the output is going to a low frequency device, the transients can be ignored. In some applications, it is more desirable to smooth the transition between states than to minimize the total time, in which case the oscillations can be damped with the capacitor or a low pass filter.

If the output is from an amplifier circuit, the settling time will be determined by the maximum rate of change of the amplifier. Thus, the first readin may take longer to settle than subsequent readins, which usually do not change the converter by such a percentage of the full scale.

ANALOG-TO-DIGITAL CONVERSION

Conversion time is measured from when a request is given to when a digital output is available. In converters like the successive approximation type, where all conversions are completely independent, time must be allowed for completion of entire steps in the conversion process. In the continuous converter, the conversion time is usually just that time required to synchronize the request and get the number.

The conversion rate is usually the inverse of the conversion time. In some systems, an amplifier or comparator recovery time is required between conversions; thus the rate is lower. However, comparators manufactured by Digital Equipment Corporation do not have a recovery time. The conversion rate will also be slower if logical operations must be carried out between conversions. In some cases, such as the counter converter performing a number of simultaneous conversions or the synchronous sequential converter, the conversion rate is actually faster than the inverse of the conversion time.

If the input signal is changing with respect to time, it is very important to know when the signal had the value given by the output. The uncertainty in this time measure is called the aperture time (sometimes also called window or sample time). The size of the aperture and the time when the aperture occurs vary depending on the conversion method.

Figures 13 through 16 illustrate how the aperture varies with different conversion techniques. In each case, the upper portion of the figure shows how the converter arrives at an output. The lower portion of each figure shows how the input might be reconstructed from the digital data.
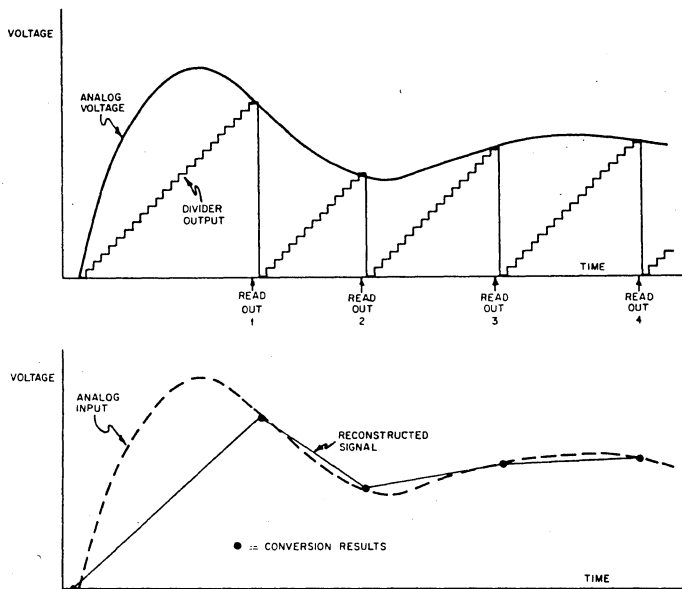
Figure 13. Counter Converter

In the counter converter (Figure 13) the aperture occurs at the end of the conversion. This is not constant with respect to the beginning of the conversion, but it may be calculated from the digital output.

For the continuous converter (Figure 14) the aperture is the time for the last step. Here the assumption is made that the input signal does not change more than ± 1 LSB between conversion steps. To meet this requirement, the maximum rate of change of the input voltage must not exceed the maximum rate of change of the converter. This is $V_{ref}/2^N\Delta T$ where V reference is the full scale voltage, N is the number of bits, and ΔT is the time per step. The maximum rate of change of the sine wave is $2\pi V_p f$, or $\pi V_{pp} f$. Thus, if the converter is to follow the input, the maximum frequency components in the input must satisfy the following equation:

$$\pi V_{pp} f = V_{ref}/2^N \Delta T$$

and if the peak-to-peak voltage is assumed equal to the converter reference, then the maximum frequency is:

$$f = \frac{1}{2^N \Delta T \pi}$$
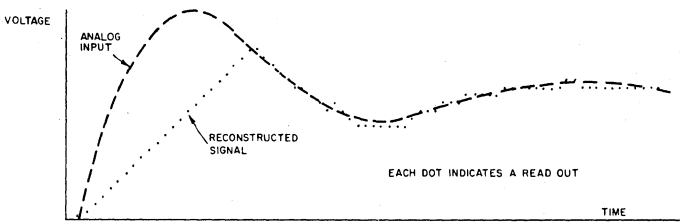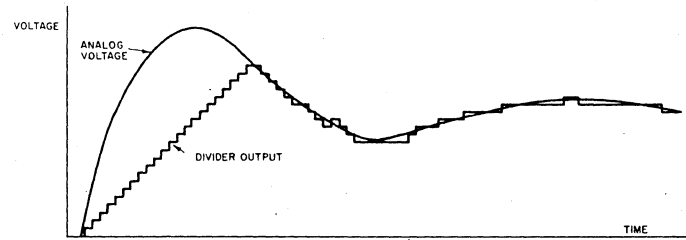
Figure 14. Continuous Converter
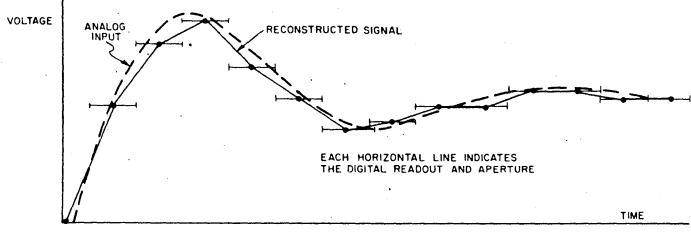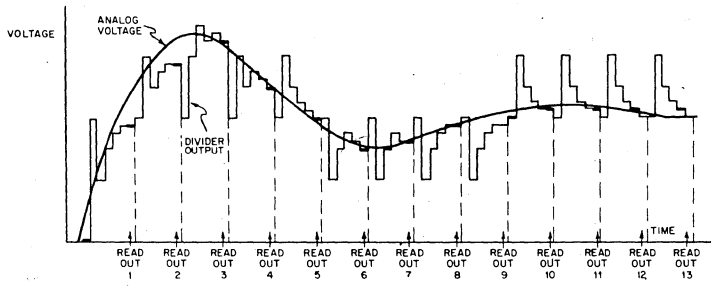
Figure 15. Successive Approximation Converter

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For a successive approximation converter (Figure 15) the digital output corresponds to some value the analog input had during the conversion. Thus, the aperture is equal to the total conversion time. Aperture time of the successive approximation converter can be reduced by using the redundancy techniques outlined in Chapter 3 or by using a sample and hold circuit. The sample and hold is illustrated in Figure 16.
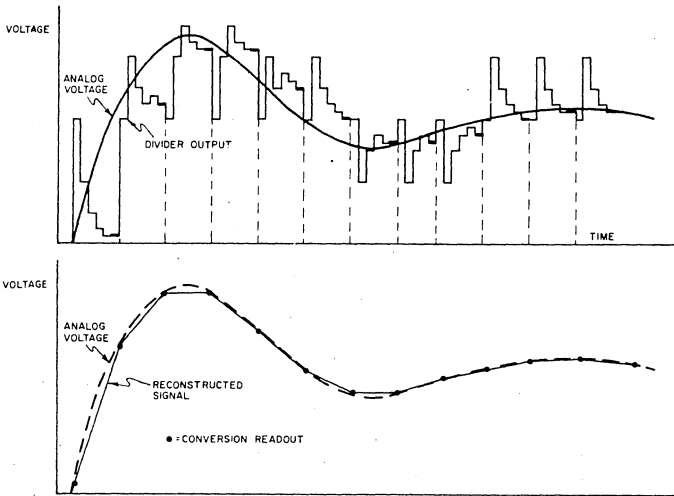
Figure 16 . Successive Approximation Converter with Sample and Hold

SELECTING A CONVERSION METHOD

Chapters 1 and 2 have summarized several methods of conversion and the performance characteristics that may be expected from them. These criteria for choosing a specific conversion method are condensed in Table 1. The table is organized like the handbook with applicable chapters called out for quick reference to detailed descriptions of the methods.

The decision to choose one converter over another is principally a matter of speed, aperture, cost, and whether multiplexing or a single continuous input is to be used. Exact conversion times, aperture times, and cost depend on the number of bits, type of circuitry,

TABLE 1   ANALOG TO DIGITAL CONVERSION TECHNIQUES

Method	Best for Multiplexed or Continuous Input?	Conversion Time* 5 Bits (μsec)	Conversion Time* 10 Bits (μsec)	Aperture Time* 5 Bits (μsec)	Aperture Time* 10 Bits (μsec)	Constant Time of Aperture?	Relative Cost	Remarks
BASIC METHODS (Chap. 1 & 4)								
Simultaneous	Both	———— Not Applicable ————				Yes	Depends on resolution	Excellent for low resolution systems — operates in about 100 nanoseconds
Counter	M	24 av.	1792 av.	1.5	3.5	No	Low	Allows many conversions simultaneously
Continuous Continuous Input Discontinuous Input	C C	1.5 24 av.	2 1024 av.	1.5	2	Yes Yes	Low to Medium	Extremely high speed for continuous input but falls behind on sharp rate of change
Successive Approximation	M	7.5	36	7.5	36	Yes	Medium	General purpose — good speed dollar
VARIATIONS ON BASIC METHODS (Chap. 3)								
Ramp	M	16 av.	512 av.	1	1	No	Depends on resolution	Good differential linearity — low cost for low resolution systems
Section Counter	M	18	112-224	1.5	3.5	No	Low to medium	Used with digital voltmeter
Continuous with add. comp. Continuous Input Discontinuous Input	C C	1.5 6-12 av.	2 32-512 av.	1.5 1.5	2 2	Yes Yes	Medium to High	Similar to continuous but has faster responses to discontinuous or high speed signals
Successive Approximation with Redundancy	M	9	27	1.5	3	Yes	Medium to High	Good speed per dollar in high resolution systems. Small aperture, good differential linearity
ADVANCED (Chap. 3)								
Subranging	M	3-4	10-20	3-4	10-20	Yes	High	Excellent for 5 to 8 bits
Subranging with Redundancy	M	2.5	6-9	1.5	3	Yes	High	Excellent for 7 bits or more
Seq. Approx. (Non-Synchronous)	M	7.5	25			Yes	High	May make errors. Requires sample and hold
Seq. Approx. (Synchronous)	C	1.5 9†		1.5		Yes	High	†Time between conversions total time
Quantizing Continuous Input Discontinuous Input	Both Both	2 6	3 18	2 2	3 3	Yes Yes	High High	Excellent for both multiplexed and continuous inputs. Automatically follows fast input with low resolution and slow input with high resolution

*See text

and variations in system design. The speeds given in the table were derived assuming that the system was designed for maximum speed per dollar. Actual speeds will usually be within a factor of 2 for basic conversion methods and within a factor of 5 for the others.

The basic conversion methods, as described in Chapters 1 and 4, will satisfy most requirements. If Table 1 confirms the choice of one of the basic methods, the reader can go directly to Chapter 4 for specific information on the equipment required. The other methods are variations of basic methods and advanced techniques primarily for increased speed. They are described in general terms in Chapter 3.

Signed Digital Numbers

In the following chapters, the most significant bit represents   5 volts, the next most significant bit,   2.5 volts, and so on. Thus, the all ZERO state corresponds to 0 volts and the all ONE state corresponds to 1 LSB less — 10 volts. This conversion can be reversed simply by using the opposite side of the flip-flop to drive the divider.

If only the most significant bit is reversed, the numbers are signed, 2's complement, as shown below. Since more numbers are negative than positive, the negative numbers are used for 0 to   5 volts and the positive numbers go from   5 to slightly less than   10 volts.

Voltage	Unsigned	Signed
0	000000	100000
	000001	100001
	.	.
	.	.
	.	.
	011110	111110
	011111	111111
5	100000	000000
	100001	000001
	.	.
	.	.
	.	.
10	111110	011110
	111111	011111

In 1's complement, the weighting of the sign bit is reduced so that   0 equals   0. (Thus, it cannot be used in a system with redundancy, a variable word length or any other feature which does not give a constant one to one correspondence between voltage and number.) Weighting is done by increasing the resistance of the MSB (most significant bit), and for a system of 9 or 10 bits the ladder potentiometer is sufficient. For low resolution systems, add a small resistor (about 16 ohms for an 8-bit system, 32 ohms for 7 bits, etc.) in series with the MSB input. It need not be precise (since the potentiometer will adjust for it) nor have a low temperature coefficient (since a large change in this resistor will have a small effect on the output voltage). Use the standard DAC adjustment procedure and look for a straight line instead of a square wave on the most significant bit.

Bipolar Voltages

BIPOLAR D TO A OUTPUTS

Binary weighted DAC modules made by Digital have an output impedance of 1000 ohms. The external load can reach 2000 ohms without any noticeable effect on the linearity of the system. Thus the output can be made bipolar with a large resistor to a positive bias voltage. The equivalent circuit is shown below.
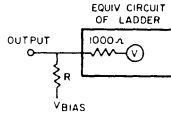
With a 10 volt reference driving the digital-to-analog converter, the output voltage swing is reduced to $\frac{5R}{R \cdot 1000}$ volts. The output voltage swing is centered when the bias voltage equals R 200. The bias voltage, of course, should be stable and noise free.

BIPOLAR A TO D INPUTS

If multiplexing is being done or if the input signal cannot drive a heavy load, an amplifier should be used for signal conversion as described in Chapter 5. In other cases, a simple divider can be used in front of the comparator. The basic circuit is shown below.
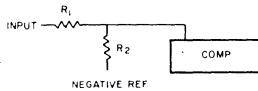
The impedance level should be kept low since the comparator will draw some current even at balance (a fraction of a microampere). The input, as seen by the comparator, should be as near as possible to the full 0 to 10 volt range.

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An alternative to the above scheme is to buck the input against the digital-to-analog con-
verter in the feedback loop, as follows:
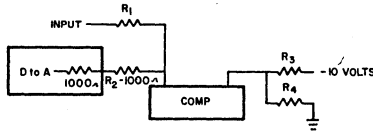
The range seen by the comparator is reduced, but common mode effects are avoided
since balance is always at the same point. R_2 should be less than 1000 ohms, and R_1 plus
R_4 should be about 500 ohms or less.

Table of Voltages

Octal Numbers		Voltage
Signed 2's Comp.	Unsigned	(Negative)
4000	0000	0.
4001	0001	0.00244140625
4002	0002	0.0048828125
4004	0004	0.009765625
4010	0010	0.01953125
4020	0020	0.0390625
4040	0040	0.078125
4100	0100	0.15625
4200	0200	0.3125
4400	0400	.0.625
5000.	1000	1.25
6000	2000	2.5
0000	4000	5.
2000	6000	7.5
3000	7000	8.75
3400	7400	9.375
3600	7600	9.6875
3700	7700	9.84375
3740	7740	9.921875
3760	7760	9.9609375
3770	7770	9.98046875
3774	7774	9.990234375
3776	7776	9.9951171875
3777	7777	9.99755859375
—	10000	10.

CHAPTER 3

SPECIAL ANALOG-TO-DIGITAL
CONVERSION TECHNIQUES

The analog-to-digital conversion techniques described in Chapter 1 are the most commonly used methods but not necessarily the only ones. There is an extremely large variety of techniques, not all of which have been investigated. Some of the other methods are described in the following section.

Variations In Basic Techniques

SECTION COUNTER

The counter converter is a simple technique for performing conversions. However, if the digital word becomes long, the 2^N steps required to complete the conversion may be too many.

One way to decrease the time at a minimum of cost is to divide the counter into sections. For example, a 10-bit converter could be divided into 2 sections of 5 bits each. At the beginning of the conversion the least significant counter is set to all ones and counts are inserted into the most significant counter until the comparator indicates that the input has been exceeded. The least significant counter is cleared and counted up until the correct value is reached. The maximum number of steps required to complete a conversion is 2^5 for the most significant counter and 2^5 for the least significant counter, giving a total of 2^6 steps. This is a maximum of 64 counts versus 1024 counts for the standard counter converter.

Other types of section counters might use more parts and operate by counting one counter up and the next down. The total conversion time, of course, depends on the number of sections.

The section counter technique is frequently used in digital voltmeters where the output is to be in decimal. Each section of the section counter thus represents one decimal digit.

RAMP METHOD

In the counter converter, each count input is increasing the voltage out of the DAC by one step, effectively generating a ramp out of the DAC. Thus the level amplifiers, reference supply, and divider network could be replaced by an external ramp generator circuit. If accuracy is not too important, the ramp can be made by charging a capacitor with a current source and using the linear part of the exponential. In higher resolution converters, the ramp might be made by using the operational amplifier as an integrator.

The ramp technique is somewhat faster than the counter technique because carry and DAC set up time is not required before gating the next count pulse. The differential linear-

ity, over a short span of a ramp converter, is bound to be fairly good, since the ramp is a continuous signal. Although there may be some noise, the general slope will not change significantly over a short span.

Both the ramp method and the counter technique approach the final value in small steps and from one direction only. This puts considerably less strain on the comparator circuit than a technique such as subranging or successive approximation where the comparator is receiving large input voltage changes in different directions and being asked to resolve small differences. In general, all smooth conversion techniques (the counter, ramp, and continuous converters) generally operate at a considerably faster time-per-step and produce better differential linearity than the approximation methods (subranging, successive approximation, sequential approximation, etc.).

CONTINUOUS CONVERTERS WITH ADDITIONAL COMPARATORS

A continuous converter is an extremely fast and relatively inexpensive device for following a continuous signal. However sometimes the input rate of change exceeds that of the converter. To close this gap determine if the differential error exceeds a specified amount and add or subtract a correction count in a more significant bit. For example, a small amount of logic added to a 10-bit continuous converter could measure large differences between the input and the contents of the converter. If the difference is more than 8 counts, it adds a count in the third flip-flop from the least significant end. If the
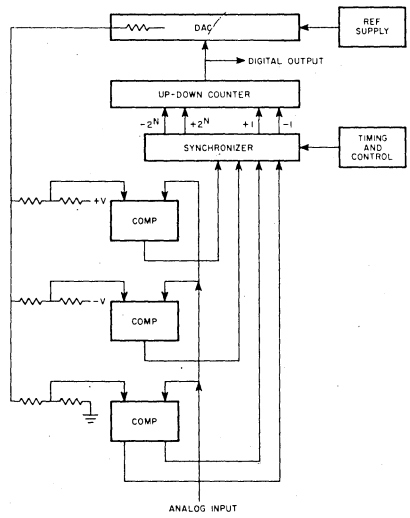

Figure 17 . High Speed Continuous Converter

difference is more negative than   8 counts, it subtracts a count from this stage. Thus the converter operates on high frequency signals with reduced accuracy and on low frequency signals with the full accuracy.

A continuous converter with additional comparators is shown in Figure 17. Two comparators and additional gating and synchronizing logic have been added to a basic continuous converter.

SUCCESSIVE APPROXIMATION CONVERTER WITH REDUNDANCY

Redundancy is useful where high resolution and high speed are both required. It can also be used to improve differential linearity and aperture.

The successive approximation converter is extremely efficient; but, since the results of each step are irrevocable, each step must be allowed to settle to within the total system accuracy. For high resolution systems, the settling time can be quite long. With redundancy, the first steps are done with a limited accuracy; then a correction step is inserted to improve the accuracy. Only the correction step and the following steps need to settle to final accuracy. Steps before correction need only settle within $\pm\frac{1}{2}$ of the correction amount.

The correction can be implemented by adding or subtracting one bit, as in a continuous converter. If the steps preceding the correction are offset, only add circuitry is necessary. For fastest operation, a special divider with redundant inputs can be used so that the addition can be done without generating carries. The digital summing can be done in an output buffer where the carries will not interfere with the analog-to-digital feedback loop.

The correction step can also be used to compensate for changes in the input analog signal during earlier steps, thereby reducing the aperture. It also improves the differential linearity of the converter since a large part of the variation in state size is due to the large transients during the early conversion steps.

Advanced Techniques

SUBRANGING

This method is very good for converting a large number of input channels since the conversion begins without assuming anything regarding the previous state of the input. It also converts quite rapidly and allows a trade-off between cost and complexity and speed. Thus, if extremely high speed is required, numerous comparators are used and not many steps are required. In the case where less speed is required, perhaps only one comparator circuit would be used.

The subranging method operates by dividing the total input signal range by the number of subranges, selecting the appropriate subrange and then dividing this into subranges as before, repeating until the desired resolution is achieved.

Figure 18 shows how subranging works. At the start of the conversion, the only information available about the input signal is that it lies somewhere in the range of zero to the full scale voltage, V_{FS}. The first step of the conversion divides the full scale voltage into

subranges, in this case four. Simultaneously, comparisons are made between the input voltage and the three subrange boundaries, V_1, V_2, and V_3. It can be determined whether the input voltage is higher than or lower than each of these boundaries. If the input signal is lower than all of the boundaries, it must fall in the lowest range. If it is higher than V_1 but lower than V_2 and V_3, it must fall in the next to the lowest range, and so forth. Once this information is determined, the selected subrange can be divided into four more subranges and the process repeated.
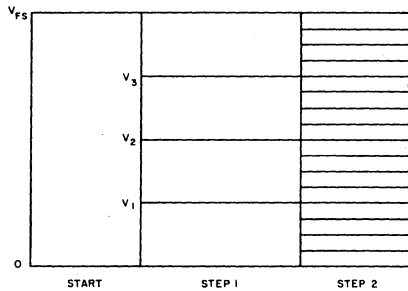
Figure 18 . Subranges for a Converter with Four Subranges Per Step

If there are M ranges per step and S steps, the total resolution of this conversion will be $(\frac{1}{M})^S$. For example, a 12-bit system requiring a total resolution of $\frac{1}{4096}$ could be implemented in 12 steps [$(\frac{1}{2})^{12} = \frac{1}{4096}$], in six steps [$(\frac{1}{4})^6 = \frac{1}{4096}$], in four steps [$(\frac{1}{8})^4 = \frac{1}{4096}$], or in three steps [$(\frac{1}{16})^3 = \frac{1}{4096}$]. The step resolution does not have to be an integer power of two. However, except in a binary coded decimal system where it is useful to make M equal to 10, the saving in control circuitry is usually sufficient to justify increasing the step resolution to the next power of 2.

Figure 19 shows a subranging converter. Here two digital-to-analog converters and a number of comparators are referenced at equally spaced intervals in the range between the value of the two converters. The technique is similar to the simultaneous method. The system starts with the lower DAC (digital-to-analog converter) at zero, the upper one at the maximum voltage. The output of the comparators indicates which range contains the input, say between the reference applied at C_K and the reference applied at C_{K+1}. Then the reference voltage from C_K is applied to the lower DAC, and the reference voltage that was at C_{K+1} is applied to the upper DAC. A new, smaller set of ranges is produced. The process is then repeated.

ANALOG INPUT

C₇ COMP

C₆ COMP

C₅ COMP

C₄ COMP

C₃ COMP

C₂ COMP

C₁ COMP

R DAC

REF VOLTAGE

GATES & FLIP-FLOPS

TIMING & CONTROL

DAC R

REF VOLTAGE
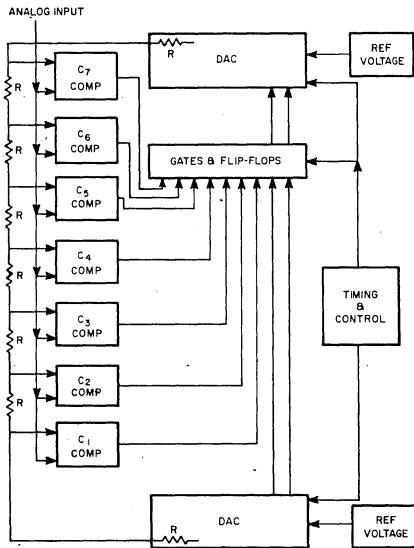
Figure 19. Subranging Converter

If the number of subranges obtained in a single step is equal to the total system resolution, this method becomes the simultaneous method described in the introduction. If the number of subranges per step is reduced to two, this method becomes the successive approximation conversion.

SUBRANGING WITH REDUNDANCY

Redundancy, as described for the successive approximation converter, can be applied in the same manner to a subranging converter. It is particularly useful here as the capacitance of many comparators in parallel causes the settling time to be quite long.

SEQUENTIAL APPROXIMATION

Sequential approximation, also called parallel approximation, uses a separate analog-to-digital converter for each binary bit of information to be obtained. There are two methods of operation, synchronous and non-synchronous.

Figure 20 shows how the non-synchronous type operates. In one example shown at the top of the figure, the analog input comes into a comparator which compares the input with half scale. If the input is larger, the comparator applies a voltage to the most significant bit of each of the DAC circuits down the line. As soon as the first comparator has

settled, the second comparator can start to make its decision. Speed is gained because there is no flip-flop delay in this system. But more important, most comparators will make decisions relatively quickly, since the analog input cannot be very close to the boundaries of more than two subranges (the last one and one other). Thus, the average amount of time required per decision is considerably less than the maximum. In a clocked system, the maximum required time must be allowed for each step. Here, only the average time is allowed.

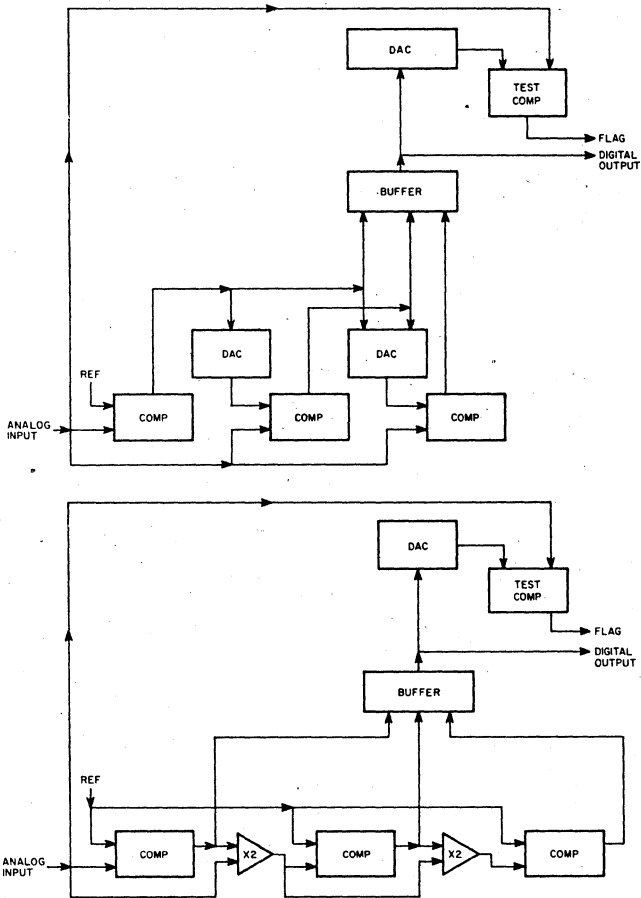

Figure 20. Non-synchronous Sequential Approximation

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The converter shown at the lower half of Figure 20 is quite similar except that the individual DAC networks are replaced by operational amplifiers. The analog input goes to the first comparator. If the input is above half·scale, the comparator produces a voltage corresponding to half scale. This is subtracted from the input signal, and the result is multiplied by two and passed on to the next comparator.

In both examples, speed is gained by the fact that full settling time is not needed by those comparators which are not making a critical decision. On the other hand, some difficulties are encountered if the input signal should change slightly before the digital readout has occurred. One of the comparators may change value, but the results may not carry to the end of the chain before readout. Thus, the comparator should have built·in hysteresis so that small noise spikes will not cause an error, and the digital output should always be read into a buffer and double checked with the input.

In synchronous sequential approximation, the time required to perform a complete con-version is essentially the same as in a successive approximation converter; however, the conversion rate is much faster. Erroneous readout is eliminated, since the converter is buffered and synchronous. This type of converter is particularly useful for systems with a single input.

The synchronous or clocked type sequential approximation converter also uses one converter per bit. It differs from the non·synchronous type because there is a delay line between each converter (see Figure 21). The analog information arrives at the first comparator, which makes a decision and stores the information in a shift register for use by later converters. By the time the second converter is set up and ready to make a decision, the same analog information is just arriving at the second comparator. This converter decides on the second bit of the output word, based on exactly the same analog voltage as was at the first converter when the first bit decision was made. This process is continued for however many bits are necessary.
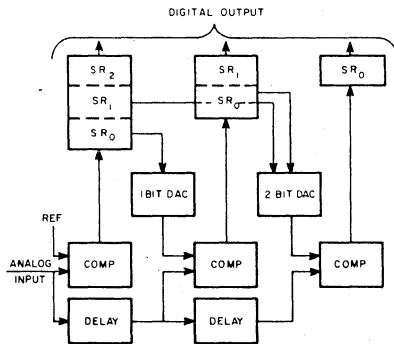
Figure 21. Sequential Approximation (Synchronous)

QUANTIZING ENCODER

The quantizing encoder was developed by Dr. Jerome Cox and Donald Glaser at the Central Institute for the Deaf. It is the most general purpose, high speed converter because it is fast for both continuous and multiplexed inputs.

The quantizing encoder uses one digital-to-analog converter, a number of amplifiers, and a number of comparators. It examines the difference between the input voltage and the DAC output, quantizes the difference to the nearest power of 2, and adds or subtracts this from the DAC. Thus, the quantizing encoder can follow a continuous signal, staying within one bit of the correct value for low frequencies. For high frequencies, it will always be within the nearest possible power of 2 of the correct answer. (Thus, if the input signal should suddenly change, the quantizing encoder will make a similar jump corresponding to the nearest power of 2 change, while the standard continuous converter could increase by only one count.)

For multiplexed input, the quantizing encoder will operate similar to a successive approximation converter but twice as fast. It requires only one step for each two binary bits (or fraction thereof). In addition, since it includes a self-correcting ability, the time per step can be quite fast.

Figure 22 shows how the quantizing encoder could arrive at the result when used as a 4-bit encoder. In the left-hand example, it is used with a multiplex input. At the start
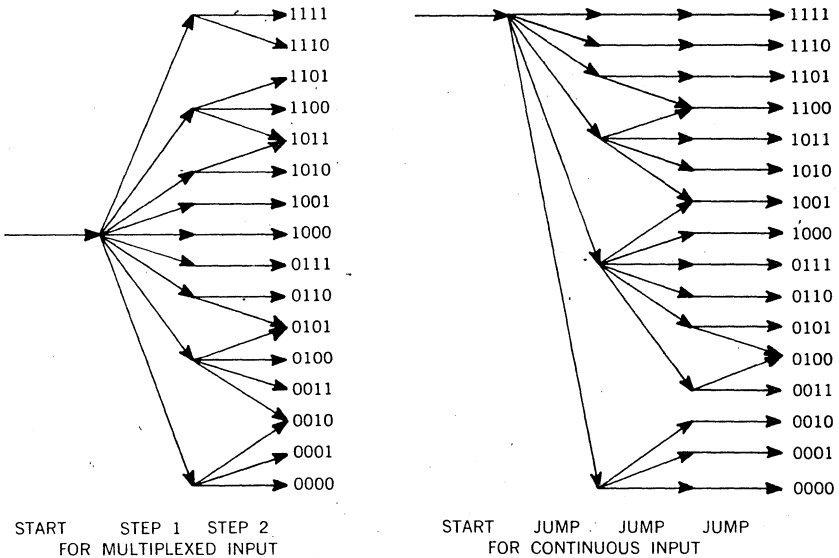
Figure 22. Quantizing Encoder Method

of the conversion the converter is set to mid-scale. At the end of the first step it will go to any of the points shown, and at the end of the second step it always has arrived at the correct answer.

The right-hand example, Figure 22, shows how the converter would react if it were holding its maximum value and the input suddenly dropped to a much lower value. If the new value were within 1 or 2 counts, it would immediately arrive at the exact answer. Otherwise, it would make a power of 2 jump to the nearest correct value.

CHAPTER 4

TYPICAL CONVERTER LOGIC

Digital-to-Analog Conversion

Figure 23 shows a typical digital-to-analog converter. The basic components of this circuit are a flip-flop register, DAC modules, and a reference supply. The digital signals are brought in with a pair of complementary levels for each bit. This information is jammed simultaneously into all the flip-flops and is automatically converted to the appropriate voltage by the divider network.
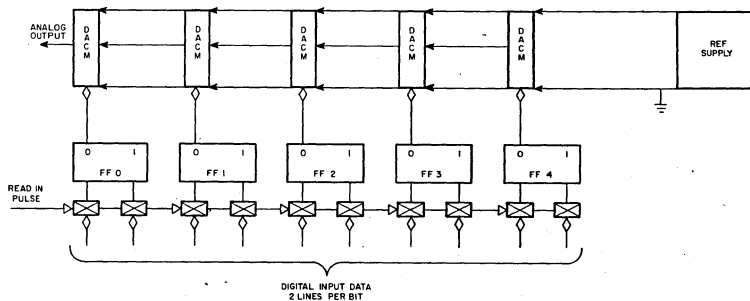
Figure 23. Digital-to-Analog Converter

The settling time of the digital-to-analog converter depends on the number of flip-flops that change, as well as the voltage difference between the two states involved. For example, in switching from a number such as 0111 to a number such as 1000, all of the flip-flops change state. Even though the two final values of the analog voltage are very close, transients occur on the divider output for the following reasons: variation in transition times from flip-flop to flip-flop and from level amplifier to level amplifier; transient current drawn from the reference supply; the fact that the flip-flops have a slower fall than rise time; and the fact that signals must propagate through the divider network. The worst case is switching from mid-scale (1000 . . .) to one count less (0111 . . .). Here the transients are as much as 1 volt.

However, the transients are quite short in duration and return to within ½ LSB of their final value within at most 2.5 microseconds for the medium speed combinations listed in the table. In most cases, these transients will be faster than the load can respond and hence can be ignored.   These units will settle to within 0.05 per cent within 2.5 micro-seconds.

RECOMMENDED MODULES FOR MEDIUM SPEED DIGITAL-TO-ANALOG CONVERTER

No. of Bits	Flip-Flops			Digital-to-Analog Conversion Module	Reference Supply
Up to 4	R200	R202	R203	A601	A702
5	R200	R202	R203	A601	A702
6	R200	R202	R203	A601	A702
8	R200	R202	R203	A601	A702
10	R200	R202	R203	A604	A704
12	R200	R202	R203	A604, A605	A704

A small choke can be used between the flip-flop output and the DAC input on the more significant bits to equalize the switching times. This will reduce the transients to about a 0.5 microsecond duration on high accuracy systems. If further smoothing is desired, a. low pass filter should be used on the output.

Analog-to-Digital Conversion

SIMULTANEOUS CONVERSION

The simultaneous conversion technique is simple, inexpensive, and extremely fast for a small resolution system. Figure 24 illustrates a simultaneous converter with a resolution of 3 bits. It uses Type W520 as comparator circuits for the input. These units have a resolution of 0.1 volts and are therefore suitable for a simultaneous convertor of up to 4 bits. The reference voltages for the level standardizers are made by dividing a +10 volt reference with a series of identical resistors. Although the tolerance on these resistors is not wide, in systems of 3 or 4 bits small trimming potentiometers should be put in series with the resistors so that the reference voltages can be adjusted to offset the common mode effects and the zero offset of the comparators. Since the comparators also draw a current through the resistors, the potentiometers can trim the value of the resistors to compensate for this current.

The outputs of the comparators are coded in a Gray code and jammed into a simple flip-flop register, made by cross-coupling inverters and diode gates. A Gray-to-binary decoder on the output produces standard binary notation.
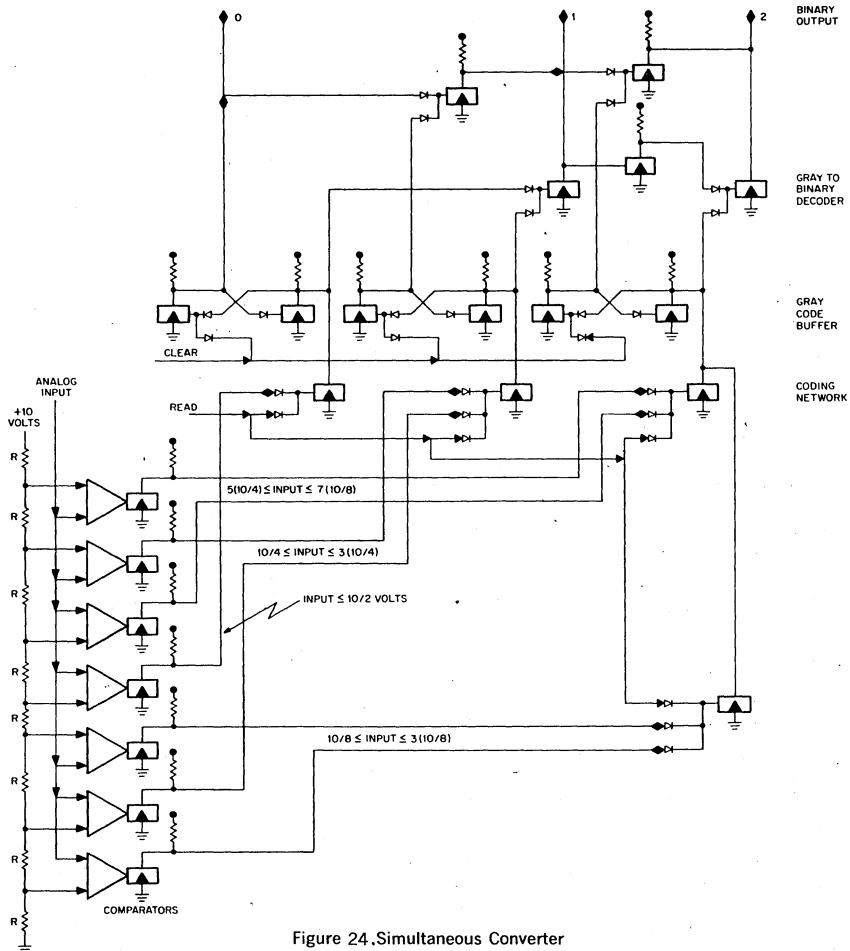
Figure 24. Simultaneous Converter

For medium speed systems, Type R111, R113, R121 and R122 gates can be used with DEC Standard 100 nanosecond pulses. With these gates, pulses can occur 0.5 microsecond apart, thus giving a conversion every 1 microseconds.

There are two factors which limit extending this system to large resolution systems. One factor is cost of so many comparators. The other factor is the current drawn and the input capacitance, which become extremely large if too many comparators are tied in parallel. For this reason it is recommended that the Type W520 be used for systems up to four bits only. Detailed information on the Type W520 is included in the W Series Section of this handbook.

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COUNTER METHOD

Figure 25 illustrates a typical circuit for the counter type analog-to-digital converter. The start signal clears the counter and inserts a single pulse in the delay chain. Each time the pulse goes around the chain, one count is added to the flip-flop register. When the divider output is equal to the analog input, the comparator will switch. The next pulse sets the control flip-flop, indicating the end of conversion and inhibiting the pulse from circulating. The circuit shown in Figure 25 used Type R201. R202. R205 flip-flops for the counter. The control flip-flop may be any unbuffered flip-flop such as the Type R200, R202, R203, R204. At the end of conversion, this flip-flop will be set by grounding the ZERO output terminal.

The Pulse Amplifiers Type R602 perform pulse standardization as well as amplification. The clear pulse should be 400 nanoseconds in duration.

The type of delay unit depends upon the number of bits in the counter, since this determines the maximum time required between counts. If an R302 Delay is used, at least two units must be in the loop to provide the required recovery time. The Type R303 does not have a recovery time requirement.

A complete conversion requires 2 steps, where N is the number of bits in a counter. The average number of steps is 2 '. Calculations of the time per step must take into account the following:

Carry propagate time of the flip-flops

Total transition time of the flip-flops

Delay of the level amplifiers

Delay through the ladder network

Transition time of the comparator and settling time (0.15 0.05N microseconds)

Gating time

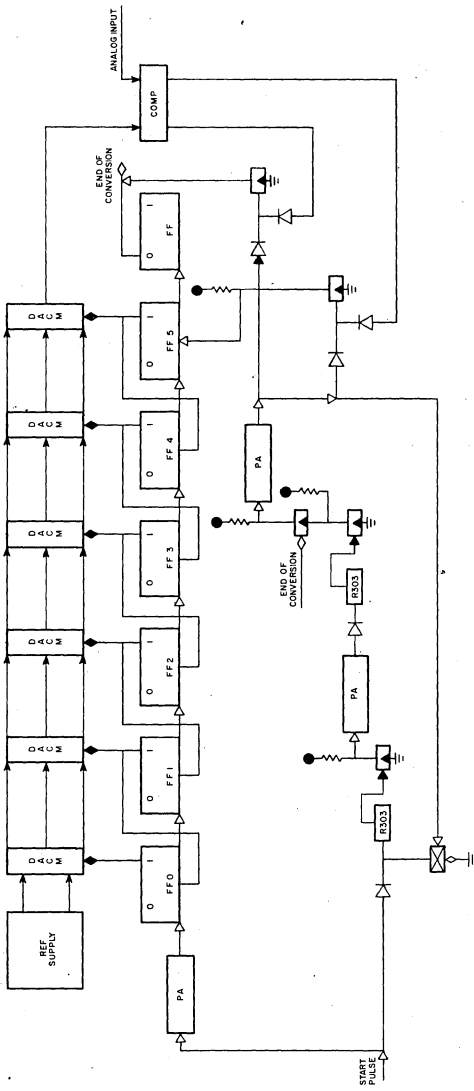Synchronization time (if required)

Figure 25. Typical Counter Converter

If buffered flip-flops are used, the control flip-flop should also be buffered and would be set through the input terminal. Also the comparator signal should not gate the counter input directly. Any noise on either the analog input or the ladder output could cause the comparator input to be in a transient state at the time the out pulse occurs. This could result in a split or partial pulse which might not propagate fully. To avoid this possibility the gating inverter on the counter may be either synchronized or eliminated, since the pulse will be inhibited from continuing through the loop.

CONTINUOUS CONVERSION

Continuous analog-to-digital conversion can be performed using an up-down counter. At each step the counter output is compared with the analog input, and a pulse is added to or subtracted from the counter, as necessary. By proper adjustment of the comparator, it is also possible to inhibit counts when the analog signal is approximately equal to the digital number. The inhibit signal is formed by adjusting the comparator outputs so that they do not switch simultaneously. For ideal operation, the two outputs should be in the same state whenever the digital feedback signal is within $+\frac{1}{2}$ part in 2^n of the appropriate input signal.

Synchronization (the use of control flip-flops) is required in all continuous converters. Any noise on the inputs to a comparator could cause the outputs to be in a transient state at the time they were sampled. Thus, if the signals are not synchronized, add and subtract pulses could enter the counter at the same time.

A continuous converter is illustrated in Figure 26. This system uses the R series unbuffered flip-flops with level change carry propagate. The illustration consist of four basic parts: the up-down counter, the DAC, the comparator, and the synchronizer and control logic. Two control pulses are formed by a clock and a delay unit. The synchronizer pulse sets the up-sync flip-flop if the enable level from the comparator indicates that the feedback signal is smaller than the input signal. Similarly, the down-sync flip-flop is set if the analog input is larger than the feedback input. Two sets of diode gates are used to inhibit counting which would cause the counter to overflow.

The outputs of the set flip-flops are exclusive ORed together to assure that no count signals will be generated if both flip-flops are set. After these signals have had time to set up, the clock generates a count pulse which samples the levels and produces a count up pulse or a count down pulse. At the same time the up- and down-sync flip-flops are reset so that the enable signals can be read in the next-time. All of the synchronizer and control logic should be from the same speed line. The flip-flops illustrated here are Type R202s, the clock is a Type R401, the delay a Type R302, and the inverters and diode gates are 2 megacycle logic.

The counter can be a lower speed logic than the synchronizer if desired. In this case, the up and down count pulses should be stretched with Type R602 Pulse Amplifiers to produce pulses of appropriate duration. In the illustration using Type R202 Flip-Flops, the outputs are buffered since the flip-flop outputs drive a capacitor diode gate level input, a capacitor diode gate pulse input, and a diode gate input, as well as providing the signals to the DAC. The inverters used for buffering are 10 megacycle units which have a minimum of capacitance. Readout from the counter register should take place from the output of the inverter buffers so as not to exceed the loading on the flip-flops.

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The continuous conversion method is applicable when the maximum rate of change of the analog voltage is less than the fastest possible rate of change in the converter. That is:

$$\left(\frac{\Delta V}{\Delta t} \right)_{input} \leq \frac{V_{ref}}{2^N \Delta T}$$

where

$$\left(\frac{\Delta V}{\Delta t} \right)_{input}$$

is the rate of change of the input analog voltage, V_{ref} is the full scale voltage of the converter, N is the number of bits, and ΔT is the time per step. ΔT is the sum of:

Carry propagate time for the flip-flops

Total transition time of the flip-flops

Delay of the level amplifiers

Delay through the divider network

Transition time of the comparator and settling time
    (0.15 ±0.05N microseconds)

Total transition time for the synchronizer

    15 microseconds

Delay through gates and pulse amplifiers if in feedback loop

Figure 26.Continuous Converter with Unbuffered Flip-Flop

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Carry propagate time may be reduced splitting the carry chain. For example, if flip-flops 2, 3, and 4 are in the ONE state, the count-up signal can be gated to complement flip-flop 1 as well as flip-flop 4. Of course, the normal carry input to flip-flop 1 is not used.

SUCCESSIVE APPROXIMATION CONVERTER

This method repeatedly approximates the input voltage. At each step, the possible range of the input signal is divided in half. The converter uses a digital register with gatable ONE and ZERO inputs, a digital-to-analog converter, a comparison circuit, a control timing loop, and a flip-flop distributor register that determines which step is taking place (see Figure 27). The distributor register is like a ring counter with a single ONE circulating to indicate which step is taking place. At the beginning of the conversion, both the digital register and the distribution register are set with a ONE in the most significant bit and a ZERO in all bits of lesser significance.

At the same time, a pulse enters the delay chain. When this pulse has had sufficient time to make one complete loop through the chain, the digital-to-analog converter and the comparator have settled and the comparator output determines whether the next digital approximation should be larger or smaller. At this time, the next most significant bit of the digital register is set to a ONE, and the most significant bit either remains in the ONE state or is reset to a ZERO, depending on the comparator output. The single ONE in the distribution register is shifted to the next position. This procedure is repeated until the final approximation has been corrected, making a total of N steps, plus settling time for the last flip-flop.

The total time required is $N \cdot \backslash T$, where $\backslash T$, the time per step, is at least as large as the sum of:

> Total transition time for the flip-flops
>
> Delay of the level amplifiers
>
> Delay through the divider network
>
> Transition time of the comparator and settling time
>> 1 microsecond for $N < 5$,
>> 0.2 N microseconds for $5 < N < 8$,
>> 2.4 microseconds for $N \quad 9$,
>> 3.0 microseconds for $N \quad 10$
>
> Delay through pulse amplifier and gates

No synchronization time is required for this method since the comparator never controls the action of more than one flip-flop.

The digital register and the distribution register use the Type R202 flip-flops. Due to the set up time of the internal gates, the time per step must be at least 1 microsecond.

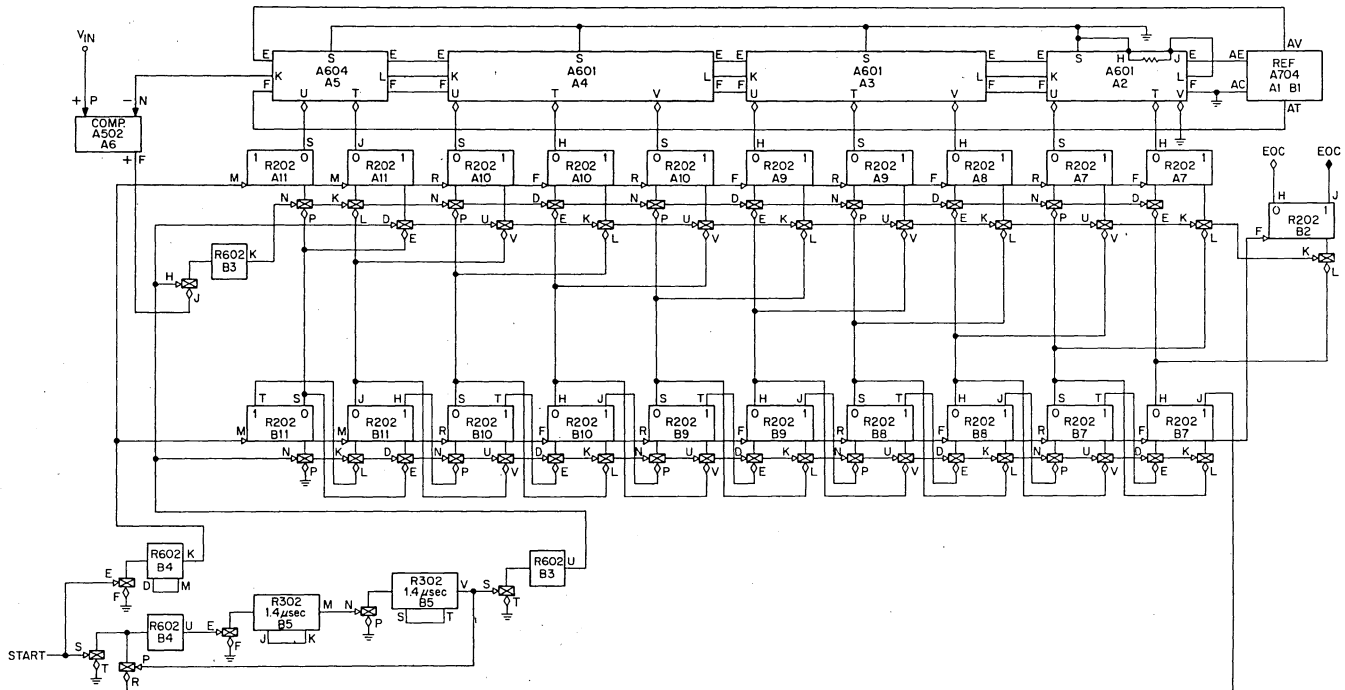The control delay chain uses Type R302 delays and R602 pulse amplifiers.

Figure 27 Logic Diagram of Successive Approximation

CHAPTER 5

BASIC CIRCUITS

This chapter includes general information on the use and importance of various characteristics of converter circuits. Detailed performance characteristics are given for specific Digital modules. Definitions of symbols and terminology are included in the appendix.

Any of the appropriate modules described in the Digital Module Catalog can be used for the flip-flop registers and the control and gating logic in a converter. The choice is governed by speed requirements in the system. For specifications on the A Series Analog-to-Digital Conversion Modules, see the FLIP-CHIP section of this catalog.

DIGITAL - ANALOG CONVERSION MODULES

The A601 (Figure 28) is a three-binary-bit digital-to-analog converter utilizing a star-type divider network and three precision germanium-transistor level amplifiers. It may be connected in series with other converters to form higher resolution converters. The accuracy of the A601 is suitable for up to eight bits of conversion. For higher resolution, it should be combined with the Types A604 and A605.

A —3v input signal at all digital inputs produces ground out. The input load is 1 ma at ground. If all inputs are not required, the most significant inputs should be used, and the least significant ones should be left open circuited. The converter input may be driven from the converter output of another module in order to provide higher resolution. If not driven from another unit, it should be terminated with 1000 ohms to ground. A termination resistor is included in the module. The reference input requires a —15 ma DEC A704 supply. The supply should be adjusted to approximately —10.01v to overcome the saturation resistance in the level amplifiers. High Quality Ground is the ground return for the reference supply and should be connected to the supply terminal and eventually to chassis ground at a noise-free location.

The output is the analog equivalent of the digital input. The most positive output is 0v. The most negative output is —10v less the value of the least significant bit. The output impedance is 1000 ohms. If a bipolar or reduced output swing is required, the output may be loaded with 1000 ohms or more without affecting the accuracy.

The A604 and A605 (Figure 29) are two-binary-bit digital-to analog converters for use with the A601 in forming high resolution, high accuracy converters. Inputs and outputs are identical to the A601 except that a terminating resistor is not included. Germanium transistors are used.
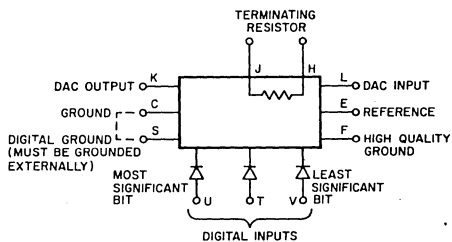
Figure 28. A601 DIGITAL-ANALOG CONVERTER
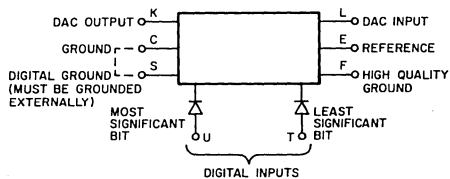
Figure 29. A604, A605 DIGITAL-ANALOG CONVERTERS

	A601	A604	A605
ACCURACY:*	±0.25% of expected value or ±0.5 mv, whichever is greater	±0.025% of expected value or ±0.25 mv, whichever is greater	±0.005% of expected value or ±0.05 mv, whichever is greater
TEMPERATURE COEFFICIENT:	±100 ppm/°C max (from +10°C to +45°C)	±25 ppm/°C (from +10°C to +45°C)	±10 ppm/°C (from +10°C to +45°C)
OUTPUT IMPEDANCE:	1000 ohms ±0.1%	1000 ohms ±0.1%	1000 ohms ±0.1%
SETTLING TIME:	300 nsec	300 nsec	1.5 μsec

*At 25°C includes tolerance of ±1.5 v on the ±10 v and −15 v supplies.

The following combinations of modules are recommended.

Resolutions (bits)	% of Full Scale	Analog Accuracy (% of Full Scale)	Units (quantity-type)
up to 8	down to 0.39%	0.25%	3-A601
9-10	0.195% to 0.098%	0.082%	1-A604, 3-A601
11	0.049%	0.038%	2-A604, 3-A601
12	0.024%	0.014%	1-A605, 2-A604, 2-A601
13	0.012%	0.01%	2-A605, 2-A604, 2-A601

Reference Supplies

The reference supply determines the voltage range of the converter. It is important that the supply be of good quality, since any error in the reference voltage will translate directly into error in the converter. That is, a 0.1 percent ripple in the reference produces a 0.1 percent ripple in the analog output.

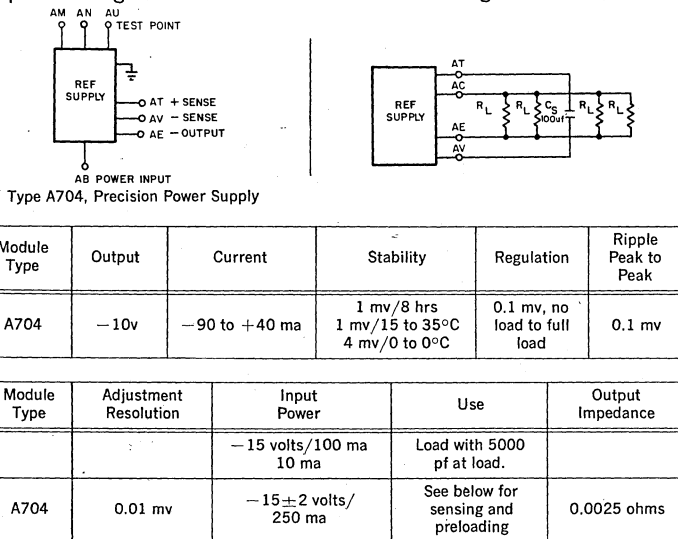Digital manufactures a reference supply: The Type A704, which may be used for systems of 13 bits or less. The supply is mounted on a Digital module and is driven by Digital standard power voltages. The characteristics are shown in Figure 30.

Type A704, Precision Power Supply

Module Type	Output	Current	Stability	Regulation	Ripple Peak to Peak
A704	−10v	−90 to +40 ma	1 mv/8 hrs 1 mv/15 to 35°C 4 mv/0 to 0°C	0.1 mv, no load to full load	0.1 mv

Module Type	Adjustment Resolution	Input Power	Use	Output Impedance
		−15 volts/100 ma 10 ma	Load with 5000 pf at load.	
A704	0.01 mv	−15±2 volts/ 250 ma	See below for sensing and preloading	0.0025 ohms

TYPE A704 PRECISION POWER SUPPLY

REMOTE SENSING

The input to the regular circuits of the A704 is connected at sense terminals at (+) and AV (−). Connection from these points to the load voltage at the most critical location provides maximum regulation at a selected point in a distributed or remote load. When the sense terminals are connected to the load at a relatively distant location, a capacitor of approximately 100 microfarads should be connected across the load at the sensing point.

PRELOADING

The supplies may be preloaded to ground or −15 volts to increase the current available in either direction. −125 ma maximum can be obtained by connecting a 270Ω ±5%, 1 watt, resistor from the −10 v pin AE reference output to pin AC ground.

Figure 30. Reference Supply Specifications

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Comparators

The comparator is an unusual circuit because it is a hybrid, partially analog and partially digital. Basically, it is a very high gain difference amplifier. The outputs "saturate" quickly so that they do not exceed standard levels. (For Digital equipment these are 0 and —3 volts.) The comparator, Type A502, has an input range of 0 to —10 volts. When the input differential is large, the dual outputs are complementary Digital levels.

The time required for the comparator to switch states depends on the desired system resolution and the conversion method. That is, the comparator takes longer to respond to a 10-millivolt differential input than for a 100-millivolt differential input. A 7-bit system, for example, seldom requires information about 10-millivolt differentials. Similarly, the comparator switches faster in a counter or continuous converter system, where the differential input is being reduced gradually, than in a successive approximation converter, where the differential voltage may go from 5 volts to 0 in one step.

FACTORS AFFECTING COMPARATOR ACCURACY

As the input to the comparator circuit varies from 0 to —10 volts, the switching point may vary also. That is, one of the inputs may have to go somewhat more negative than the other before the outputs switch. A similar effect occurs with changes in temperature. In the Type A502, the switching point does not move more than 5 millivolts as the input voltage changes from 0 to —10 volts and the temperature changes over a range of 20°C (around room temperature). Power supply fluctuations of the Type 728 or an equivalent supply change the switching point by less than 0.6 millivolts.

Both outputs will not switch simultaneously unless the amplifier is in perfect balance. If the switching point changes mentioned above affect both outputs equally, the effect is referred to as a shift in the common switching level. If one of the outputs is affected more than the other, there is an offset between the two sides of the amplifier.

USE OF THE COMPARATOR

Illustrations of the use of the comparator are included in Chapter 4. In other uses, it must be remembered that the comparator is a hybrid circuit. If the differential input is small, but balance is not quite right, the outputs may not be complementary. If there is a small amount of ripple on the input, the outputs may oscillate. Normally this effect is of no concern because the errors have already been taken into account in the common mode and resolution specifications. However, if the results are to be read into more than one flip-flop, output oscillations can cause different information to be read into the different flip-flops. Thus, the outputs must be synchronized before being read into more than one flip-flop. Similarly, the comparator level changes should not be used as information unless it is certain that transient signals (such as those that occur when a DAC switches) will not cause false outputs.
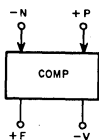
Type A502 Comparator

Specifications:

Input Range: 0 to —10 volts

Input Impedance: 1 microampere, 125 picofarads (The input current depends on the relative polarity of the two inputs. The more positive input may draw up to 1 microampere and the more negative input may supply up to 1 microampere. The maximum current difference between states is 1 microampere.)

Outputs: Two outputs, 0 and —3 volt levels

Output Loading: 7 units base load at dc, 1 unit for maximum speed

Resolution: 1 millivolt at dc

Common Mode & Temperature: 5-millivolt maximum equivalent input offset for 10-volt common mode change and 20°C change

Speed:

Depends on application, principally on the ratio of the voltage difference before passing through the switching point (V_s) to the voltage afterward (V_A). Speed is affected to a lesser degree by the length of time the input difference is at V_s, by the magnitude of V_A, by the source impedance, and by the load. Typical speeds in an analog-to-digital converter system where the source is a ladder network and level amplifiers, and the load is a 1 unit base load, are listed below. (These speeds include allowances for extra divider settling times at high accuracies.) For more information on specific applications, see Chapter 4.

V_s/V_A	V_A in mv	Time in μsec
—512	10	3.0
—128	40	1.6
—32	160	1.2
—2	20	0.6
—2	80	0.5
—1/512	10	0.15

Adjustment:

Two potentiometers control zero set and common balance. See Chapter 6 for adjustment.

Power: —15 volts/55 ma; +10 volts (A)/0; +10 volts (B)/21 ma.

Figure 31. Comparator Specifications

When the comparator is used in a digital voltmeter or a continuous converter, it is usually desirable to have built-in hysteresis which is just slightly less than $\pm\frac{1}{2}$ LSB. The hysteresis avoids converter chatter (switch back and forth between two states) when the input voltage lies on a boundary between the two states. It is possible to introduce some hysteresis into the A502 by adjusting the common switching level and offset control so that the two outputs do not switch simultaneously. In a continuous converter, counting would then take place only when the two outputs were of opposite polarity. No action would take place when both outputs had the same polarity. The same type of logic would be applied in a digital voltmeter, the exact action depending on the conversion method used to arrive at the results.
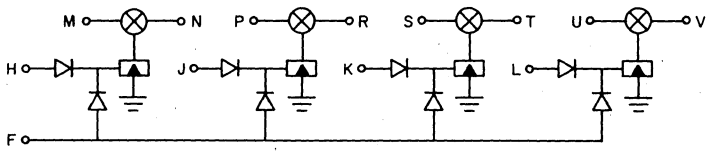
Multiplexer Switches

ANALOG MULTIPLEX SWITCHES

An analog multiplex switch is like a relay, in that two points are opened or shorted on command from an external source. Digital manufactures a relay switch, Type A111, for low speed operations, and a solid state switch, Type A121, for high speed operations. The control inputs to these switches are 2-input AND gates, each with a separate control input and all with one input in common. If the control inputs are driven from binary to octal decoders, up to 512 switches can be placed in parallel. The accuracy and speed limitations are the switch capacitance and the amount of leakage current back through the switches.

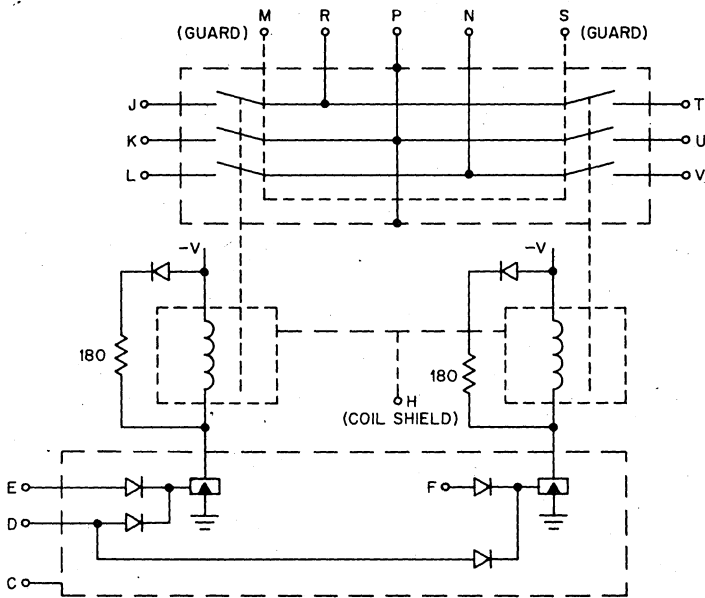The switches can be tied in parallel, cascaded to give double level multiplexing for large systems, or used in other applications such as the sample and hold circuitry.

USE OF THE TYPE A121 SWITCH

In the off position, most types of A121 switches can have up to 15 volts across them, ranging from $+10$ volts to -5 volts referenced to ground.

A121 Solid State Switch

A111 Relay Switch

Figure 32. Multiplexer Switchs

Multiplexer Switch Specifications

TYPE NUMBER	A121	A111
Type of Switch	Solid state	Relay
Number of Circuits	4, single pole, independent	2, double pole, outputs bussed
Control		
Signals	Digital levels	Digital levels
Enable	$-3v$	$-3v$
Load	1.3 ma load shared among grounded inputs	3 ma load shared among ground inputs
Signal		
Max. voltage	$\pm 10v$	$\pm 10v$
Max. common mode voltage	N/A	200 VDC
Max. current	1 ma	1 ma
"On" offset (max.)	0	
"On" resistance (max.)	450Ω	$(0.025\Omega$ nominal)
"Off" resistance, leakage	10 na	$5 \times 10^8 \Omega$
Speed		
50% input to .01% of output	Delay + charging time	Delay + operate time
Turn on delay	150 nsec	1 msec (max.)
Turn off delay	250 nsec	1 msec (max.)
Life		10^9 operations at low loads

TABLE 8   USEFUL LOGS

t/T	$1 - e^{-t/T}$	$e^{-t/T}$
3	0.95021	0.04979
4	0.98168	0.01832
5	0.99326	0.00674
6	0.99752	0.00248
7	0.99909	0.00091
8	0.99966	0.00034
9	0.99988	0.00012
10	0.99995	0.00005

The switch is turned on when the two control level inputs are negative voltage (or open). When changing the state of the switches, care should be taken that two switches tied to a common node are never turned on simultaneously. If the control levels come from 10-megahertz flip-flops which are all changed simultaneously and which are decoded by 5-megahertz binary octal decoders, the switching is fast enough so that there is no danger of shorting. If low speed circuitry is used to drive the switch, or if the controlling flip-flops are not all changed simultaneously, one of the enabling inputs should be grounded before the state of the switches is changed. This will put all of the switches in the off position and assure that there will never be a make before break situation. If the switches are turned on

simultaneously, no damage will occur if the voltage ratings are observed, but large signal and transients will occur. It should be noted that the fall time of the output waveform of a single multiplexer switch is almost entirely determined by the load impedance and may be quite long for high load impedances.

RELAY MULTIPLEXER TYPE A111

The Type A111 contains two double pole switches which can be used for differential multiplexing. The switch outputs are connected to an output bus. The speed of the relay is determined by the delay in turn-on plus the bounce settling time. For the Type A111 this delay is 1.2 milliseconds. There are two control level inputs for each relay; one of these is common to both relays on the module, and one is independent. The relay is turned on when both of its control inputs are negative.

Analog Amplifiers

Amplifiers are sometimes used at the input of an analog-to-digital converter to shift the input range, scale the input range, provide a differential input, or isolate the input signal from the converter. Amplifiers are used on the output of digital-to-analog circuits to shift or scale the output range, to reference the output signal to the external ground, and to lower the output impedance. The last two features are important when the two pieces of equipment are separated by a distance that makes noise pickup likely. In this case, it is best to put the amplifiers at the driving source end, that is, at the output of the divider network in a digital-to-analog conversion or at the signal source for analog-to-digital.

The most useful amplifier for these applications is the operational amplifier. Its high input impedance and high gain make it a building block just as a flip-flop or nor gate is a digital building block.

Usually an operational amplifier is designed to roll off at 6 db per octave. This ensures less than 180 degrees additional phase shift so that the amplifier will not oscillate. This also produces a simplification in calculating the dynamic aspects of putting an amplifier in the system, although for a rigorous analysis, much more detail about the characteristics of the amplifier must be known, and the calculations are far more complex.

The approximation of infinite input impedance and infinite gain can be used in designing with good quality operational amplifiers with negligible error.

Figure 33a shows the amplifier operating as a simple inverter. The gain is $\frac{R_f}{R_i}$. The imput impedance is R_i and is returned to virtual ground (within microvolts of true ground). The gain accuracy and stability is that of R_f and R_i. The output impedance depends on the difference between open loop gain and closed loop gain. Typically, the closed loop gain is not very high, less than 100, and the open loop gain is in the order of 10^6. Under these circumstances, the output impedance is less than one ohm.
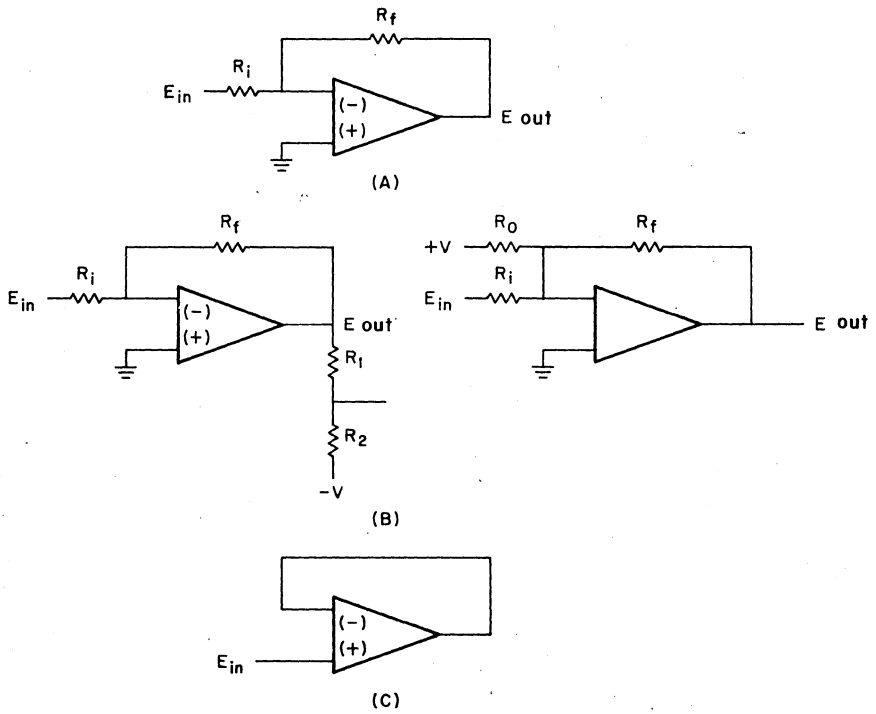
Figure 33. Typical Amplifier Configuration for Scaling and Biasing
Digital-to-Analog or Analog-to-Digital Inputs

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Figure 33b shows how a signal may be offset with a negative or positive reference voltage. In b, the positive reference is summed with the input voltage, E in. The amplifier will keep the turning point at ground so that a sample calculation of resistances and currents is all that is required to determine the offset. Since the summing point is at ground, each input is independent of the other. If a half scale offset is required,

$$\frac{+V}{R_o} = \frac{2R_f}{E_o}$$

the input signal current applied thru R_i will be superimposed on the above dc level. Figure a utilizes a gain of two and a times ½ alternator. If the input voltage swings from —5 volts to +5 volts, the alternator output will vary from zero to —10 volts.

Figure 34c shows a non-inverting "potentiometric" amplifier configuration. The output will equal the input and the gain will approach +1. The current drawn by the non-inverting input will be nearly zero. The input impedances achieved can approach 500 megohms.

Scaling, offsetting and differential input to an analog-to-digital circuit follow exactly the same method. The input resistor would be R1 minus the appropriate output impedance of the driving signal.

When amplifiers are required on converters, it is generally best to use the same type of amplifier as is being used in the analog portion of the circuitry to keep the performance characteristics the same. When an amplifier is being used internally in the converter, such as between a group of multiplexer switches and an analog-to-digital converter, a higher performance amplifier is required, since it will be asked to take full scale changes and settle within a very short time.

The A200 consists of a DEC amplifier (part #1505379) mounted on an A990 amplifier board and includes a gain trim and balance potentiometer. Mounting holes are provided for input and feedback networks and roll off capacitor. The amplifier is supplied to Digital by Analog Devices and is identical with the Analog Devices 102 A.

|	
Open Loop Gain:	2×10^6
Rated output voltage (a20 ma)	$\pm$ 11v
Frequency response	
Unity gain, small signal	10 mc
Full output voltage	300 kc
Slewing rate	30v/μsec
Overload recovery	200 μsec
Input voltage offset	Adjustable to Zero
Average vs temp.	20 uv/°C.
Vs supply voltage	15 uv/%
Vs time	10 uv/day
Input current offset	$\pm$ 2 na
Average vs temp.	0.4 na/°C.
Vs supply voltage	0.15 na/%
Input inpedance	
Between inputs	6 megohm
Common mode	500 megohm
Input voltage	$\pm$ 15 volts
Max common mode	$\pm$ 10 volts
Common mode rejection	20,000
Input	8 μvolts
Power	
Voltage	$\pm$ 15 to 16 volts
Current at rated load	35 ma
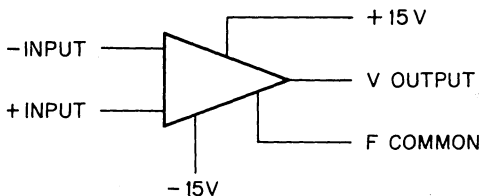
Figure 34.   A200 Operational Amplifier

CHAPTER 6

INTERCONNECTION AND CALIBRATION

Grounding and Shielding

If the converter system operates with eight bits or more, care should be taken with the system wiring to avoid noise pickup and ground potential differences between the analog equipment and the converter. Since the digital voltages are low level, the major noise source within the converter is fast-switching transients, particularly pulses. Their effects can be minimized by isolating the analog portions (the divider network, level amplifier, reference supply and comparator) from the digital portions of the converter. Pulse-generating devices, such as clocks and pulse amplifiers, should be farthest away from the major analog components.

Single wires can be used within a mounting panel or between two panels if no noise sources are nearby. Coaxial cable is best, of course, for long leads. However, a twisted pair is usually sufficient, even in high accuracy systems, if pulse lines and other fast transients are avoided. The shield conductors of the coaxial or twisted pair should be tied down at one end only, and this end should go to a good ground, not near a pulse transformer or other high frequency device.

On the precision level amplifiers, there is a separate input for the high quality ground. These inputs can be tied together and fastened to chassis ground at a good solid point. In general, excessive analog ground loops should be avoided.

Similarly, in large systems sense wires from the reference voltage supply should be brought to a point near the load so that the supply will regulate the voltage as seen by the load, not the voltage as generated at the power supply. If the load is distributed, capacitors at the main load points will reduce transients caused by the rapid switching of the DAC's. A separate ground-shield is brought out on the Type A111 Multiplexer Switch. It isolates the analog signal from noise transients generated by the multiplexer control signals. Any solid ground source can be used here, but this analog signal is not a ground reference for the system.

Signals from a high impedance output are more sensitive to noise pickup than those from a low impedance output. Thus, if a digital-to-analog converter is to drive long leads where noise could be picked up, the output should be buffered with an amplifier having a low output impedance.

The size of the ground potential differences which can occur between the converter and the analog input or output signal should also be minimized. If it is not possible to place the two pieces of equipment close to each other with the grounds tied tightly together, a

heavy ground strap can be run between them. Alternatively, the ground potential differences can be subtracted out. In an analog-to-digital converter this is done by using a differential amplifier at the input, or by using two standard operational amplifiers. In the latter case, one of the amplifiers is used to invert the ground; then the signal and inverted ground are summed. In digital-to-analog conversion, the ground from the signal destination is brought back to the converter, inverted with an operational amplifier, and summed with the signal.

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CAUTION

The multiplexer switches are low impedance switching circuits. Precautions should be taken against possible shorting of the analog inputs and outputs of these circuits to any other low impedance source, including ground. such shorting could damage either the circuits or the signal sources.

</div>

CALIBRATION

EQUIPMENT NEEDED

The adjustment and calibration procedures outlined here are designed to be as simple as possible. Three pieces of equipment are needed, as follows:

1. A digital module extender.
2. An oscilloscope with a high gain ac-coupled vertical amplifier and a dual trace amplifier.
3. A reference for determining proper gain setting. Can be a standard voltage or a reference from the analog equipment.

GENERAL PROCEDURE

There are six kinds of calibration needed for basic conversion systems. They apply to digital-to-analog converters and to three types of analog-to-digital converters: the counter, continuous, and successive approximation types. Other conversion systems require basically the same kind of adjustments, with certain steps added or omitted depending upon the circuits used. In this chapter, the six general procedures for calibration are presented as follows:

Steady State Calibration
   DAC Networks
   Comparators (analog-to-digital conversion only)
   Offset and Gain
Speed
   Noise and Ripple
   Digital-to-Analog Adjustment
   Analog-to-Digital Adjustment

Calibration should follow in the same order as the procedure given. In steady state calibration particularly, the DAC, offset, and gain adjustments carried out in that order make it unnecessary to repeat previous adjustments for fine trimming. The effects of these adjustments can be seen easily if output is plotted against input. Normally, with the digital number 0 in, the output should be 0 volts out, and vice versa. Similarly, maximum input should yield full scale output. Intermediate points should fall on a straight line between these two points.

An uncalibrated converter, however, produces the non-linear plot shown below.
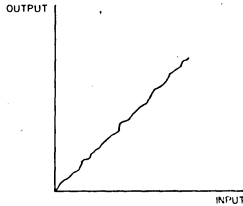
By adjusting the DAC networks, the irregularities are removed from the curve and it becomes a straight line. Next a small amount of offset is added to the network, shifting the curve up and down, as shown below, until the zero input gives a zero output.
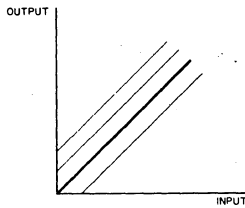
Finally the gain is adjusted until a relatively large input produces the correct output. The slope of the curve will change as follows:
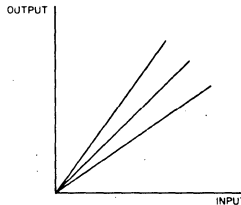
DIVIDER ALIGNMENT

The DAC is aligned to compensate for variations in resistors in the divider network and for variations in the output impedance of the level amplifiers. The output voltage from the bit to be calibrated is compared with the output voltage resulting from all of the bits of lesser significance. The difference is trimmed so that it is equal to one least significant bit. A simple setup for making this adjustment is shown in Figure 35. The clock, delay one-shot, and inverter simulate a digital input to the converter. Here they are shown switching the inputs between 00100000 and 00011111. Thus, the bit under test is the third bit, and the adjustment is made with the trimpot on that bit.
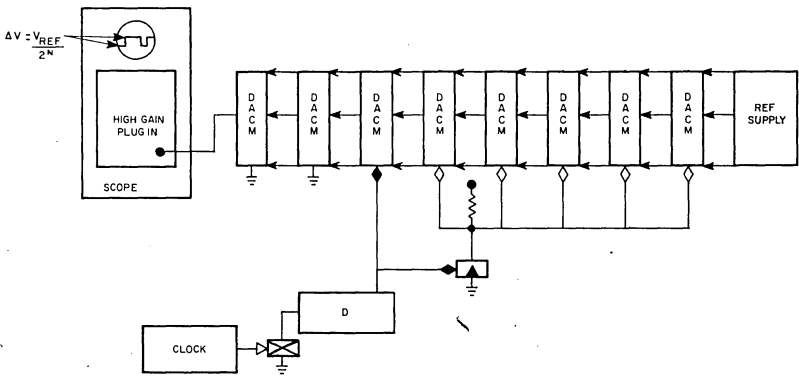

Figure 35. DAC Adjustment

The output should be monitored by an oscilloscope with a high gain, ac coupled vertical amplifier. The amplitude of the output should be one least significant bit voltage contribution. Since this alignment also adjusts for variation in output impedance of the DAC's, the level DAC's should be aligned in the same relative order as in the final system. Any unused bits of lesser significance should be connected to —3v. in the test setup just as in the system. Inputs to DAC's in more significant positions may be either grounded or connected to −3 volts, as long as they remain constant throughout the alignment.

In starting the alignment, it is advisable to check a non-adjustable bit first to make sure that the setup is correct. Using this method, the adjustment of bits of lesser significance is independent of the adjustment of bits of more significance. Therefore, the least significant adjustable bit should be checked first, then the next in order, and so on toward the most significant bit. The alignment is then completed in one step, without the need of going back to realign any portion.

The sensitivity to the trimpot motion depends on the number of bits being used. In a 10-bit system, where the voltage differential being observed is approximately 9.8 millivolts, the motion of the least significant potentiometer is barely seen on the scope. Working toward the most significant bit, the adjustment range will become larger and larger until it may be possible to invert the relative values of the outputs. To avoid such inversion, note whether the longer portion of the rectangular wave corresponds to the more negative part of the signal or to the more positive part of the signal. Be sure that this relationship continues the same for all of the bits.

Since the DAC's use fine resolution wire-wound trimpots, ascertain that they are in a stable position and that the slider arm is not resting on a single wire where it could jump away, possibly in the wrong direction. After trimming, tap the pot once or twice with the end of a screwdriver and, if the output changes, retrim to the stable position closest to the ideal value.

There are two advantages of this particular method of alignment. As the trimpot is changed, the dc level will move up and down. However, since the levels are being observed simultaneously, and only the difference is being monitored, the scope can be put on ac and the picture will stay in the center of the scope face. Also, since the adjustment is made on the differential between two states, a 10 per cent error in the adjustment will give an error in the system of only 10 per cent divided by 2^N.

An ohmmeter should not be used to adjust the ladder network, since it will not take into account the output impedance of the level amplifiers. Do not try to adjust the output with a voltmeter since the dc level shift would require switching between the two states, and the measurements would be extremely confusing and time-consuming.

NEED FOR REALIGNMENT

Realignment should not be necessary under normal conditions. The system should be checked if the modules have been subjected to a drastic change of temperature or to a mechanical shock sufficient to change the trimpot settings. Realignment should be done if one of the DAC modules is changed.

THE COMPARATOR TYPE A502

The comparator can be adjusted easily with a dual trace oscilloscope and a clean-SN dc source applied simultaneously to the inputs.

The two outputs of the A502 are viewed simultaneously on a dual trace oscilloscope. With both traces synchronized to a single point, the two signals will appear as roughly complementary square waves. For most applications the comparator should be balanced; that is, both outputs change simultaneously when the relative polarity of the inputs changes. For continuous converters or digital voltmeters, however, such adjustment would cause the converter to oscillate around a dc level. In this application it is desirable to delay switching of the outputs until the input analog signal is almost ½ LSB away from the divider input. The small amount of hysteresis introduced prevents converter chatter.

The comparator should be adjusted so that the two outputs are perfect complementary square waves. Adjust the upper potentiometer to make the two waveforms complementary. Adjust the lower potentiometer for equal positive and negative portions of the square wave. These controls are somewhat interdependent, so it is necessary to repeat the adjustments until the optimum symmetry is observed. The resolution can be increased by reducing the size of the input sine wave and repeating the adjustment.

COMPARATOR WITH HYSTERESIS

Begin the adjustment with a difference voltage, applied to the input, that is equal to the amount of hysteresis desired. Proceed to adjust the comparator as above, under Adjustment For Balance.

The comparator adjustment can change with time, temperature, or a mechanical shock severe enough to jar the potentiometers. The need for readjustment depends on the accuracy required and the environment. Usually a monthly check is more than sufficient. Testing can be done by taking the comparator out of the converter and employing the above method or by testing the overall system, as described in the next chapter.

OFFSET AND GAIN

Offsetting and gain adjustments should be made on the assembled system. In a digital-to-analog converter, a digital number is put in and the output is observed with a voltmeter. In an analog-to-digital system, a voltage is put in and the switching points are observed. Offset and gain adjustment are necessary to compensate for the open-circuit voltage drop of the DAC's, which can be as high as 10 millivolts in precision converters. In an analog-to-digital converter offsetting is also necessary to center the quantization error; that is, if the state zero corresponds to 0 volts and the state one corresponds to 10 millivolts, the converter should switch between states zero and one at an input of 5 millivolts.

OFFSET

The calibration should begin with the offset. A positive voltage can be applied through a large resistor (usually on the order of 1 to 10 megohms) to the digital-to-analog converter output. The size of the bias resistor, or the amplitude of the bias voltage can be varied until the offset is correct. For digital-to-analog conversion, zero in gives zero out. For analog-to-digital, an input of ½ LSB produces the first switching point.

The offset voltage source can be the standard $+10$ volts (for systems of up to 10 bits). The percentage variations in the voltage supply for the offset signal are scaled according to the amount of bias obtained. That is, a 10 percent ripple on the bias supply produces a 10 percent ripple in the offset; so if the offset is 10 millivolts, a 10 percent ripple would be 1 millivolt.

GAIN

The gain adjustment on a digital-to-analog converter is made by setting the digital number to half-scale or full-scale and adjusting the reference voltage supply until the output has

the correct value. The Type 1562 has one trimming potentiometer for this adjustment. The Type A204 has both a fine and a coarse adjustment. In checking the output voltage, remember that the output impedance of the divider network is about 1000 ohms. Thus, loading the output with one megohm would reduce the output voltage by 0.1 percent. This adjustment should be done with the same load as in the final system.

The gain adjustment for an analog-to-digital converter differs only in that the common mode effect of the comparator must be taken into account. The comparator has been balanced with a —5 volt common mode. The offset has been applied so that the lowest switching point is correct. Therefore, the reference adjustment which gives the correct half-scale switching point is different from that which gives the correct full-scale switching point. Generally, maximum accuracy is desired in the lower part of the scale, so the mid-scale point should be used. Alternatively, the reference may be adjusted for the best fit between half-scale and full-scale points. In calculating the switching points for these measurements, be sure to remember the quantization offset that has been introduced. This adjustment should be made at low speed (10 to 20 microseconds per step).

SPEED ADJUSTMENTS

NOISE AND RIPPLE

When the DAC's switch, a transient current is drawn from the reference supply. Normally this supply is loaded with a capacitor to reduce noise (see power supplies, Figure 30), but it may also be desirable to place small capacitors at the reference inputs of the individual DAC's and possibly also between the high quality ground and the chassis ground. The voltage at the load can be monitored on a scope with a high-gain dc-coupled plug-in unit.

Care should be taken that the noise being observed is actually there and not introduced through the scope or by a ground lead attached to the wrong point. The reference and the ground tend to move together. If the input signal source is referenced to this ground, it also moves. Thus, the scope should generally be disconnected from ground at the power and connected to the converter ground at a good solid point, and the cable running to this scope should be prevented from introducing additional noise.

ANALOG-TO-DIGITAL ADJUSTMENTS

As mentioned previously, the speed and accuracy of an analog-to-digital converter are interrelated. That is, if the converter is run too fast, the DAC's and the comparators do not have enough time to settle to final value. In the range of 6 to 10 bits, even a tenth of a microsecond per step can make a considerable difference in the system accuracy. Thus, the speed may be adjusted for the maximum allowable time and hence the maximum accuracy, or it may be adjusted for the minimum time required to give the required accuracy.

Test for speed should be made by checking the major switching points. For most converters (including the counter, continuous, and successive approximation types) these are around one-fourth, one-half, and three-fourths of full scale, as shown below.

Area Being Checked	From	To
¼	0011...110	0011...111
	0011...111	0100...000
	0100...000	0100...001
½	0111...110	0111...111
	0111...111	1000...000
	1000...000	1000...001
¾	1011...110	1011...111
	1011...111	1100...000
	1100...000	1100...001

For a more detailed check, the switching points around 1/8, 7/8, 1/16, etc., might also be included.

DIGITAL-TO-ANALOG ADJUSTMENTS

The digital-to-analog converter output contains transients when many bits are changed simultaneously, such as in going from 01111 to 10000. These transients are caused by variation in flip-flop transient times and propagation time through the divider.

Transients can be reduced by adding a small choke in series between the flip-flop and level amplifier, or by loading the flip-flop with a resistor to 15 volts. Further reduction can be made with a low pass filter on the output (remember that the digital-to-analog output impedance is 1000 ohms.)

CHAPTER 7

TESTING AN ANALOG-TO-DIGITAL CONVERTER

The adjustment and calibration procedures detailed in the previous chapter should result in a converter that operates correctly over the whole range. To make sure the converter meets specific accuracy requirements, testing may be desired, and simple operating checks should be repeated at regular intervals to assure continued correct operation.

If the converter is part of a general purpose computing facility, complete testing can be performed easily under program control. If, on the other hand, the converter is part of a specialized system or is to be tested before installation in such a system, manual or semi-automatic testing is necessary and will probably cover only the worst cases. For most converters (counter, continuous, and successive approximation) the worst cases are seen, at the major switching points; namely, one-fourth, one-half, and three-fourths full scale (see Chapter 6).

The following sections describe tests that can be performed to measure the various converter characteristics either manually or by computer. The equipment required depends on the tests to be performed. Some of the tests require very specialized equipment, while others can be performed with quite simple equipment.

MONOTONICITY

This simple test requires a minimum of precision equipment. It does not guarantee a specific accuracy but gives a good indication. If a converter with a star / type divider passes a monotonicity check, the relative error in the DAC will be small, probably less than ± 1 LSB.

DIGITAL-TO-ANALOG — Monotonicity can be checked by driving the converter from a counter and observing the output on a high gain scope. The output should be a staircase pattern.

ANALOG-TO-DIGITAL — The input can be any noise-free power supply (such as a battery) and a potentiometer of less than 2000 ohms. In testing high resolution systems, potentiometers should have a coarse and fine control with overlapping ranges. Starting at zero, increase the input voltage and check that each state exists and that these states are in the correct order. A similar computer-controlled test can be done using a saw tooth generator as the input signal.

STEADY STATE ACCURACY

DIGITAL-TO-ANALOG — Set an input to a known digital number and observe the output with a high accuracy meter. Compare with the theoretical value.

ANALOG-TO-DIGITAL — The input can be a high accuracy voltage reference or a stable, ripple-free, variable power supply with a high accuracy meter. When the converter is run at a rapid rate, the indicator lights will show quite clearly where the switching points are.

The input voltage at the switching point is measured and compared with the theoretical value. Computer controlled checking can be done in a similar manner using a precision programmable reference as the input signal.

NOISE

DIGITAL-TO-ANALOG — Noise can be measured on a scope with a high gain, ac-coupled plug-in unit.

ANALOG-TO-DIGITAL — The noise appears as a band around the switching point, where the converter output is oscillating between two neighboring states.

INTERMITTENT ERRORS

Intermittent errors can be caused by pickup or loss of a bit in the digital section or by noise picked up in the analog section. The test for intermittent errors should be done with automatic or semi-automatic equipment where the converter is run at full speed for an extended period of time. The equipment should be installed in its final configuration so that the transmission of the information is included in the test. It is important to check the states where there is only a single 0 or a single 1 for possible pickup or loss of information in the digital transfer.

In a general purpose system which includes two-way conversion, an intermittent error check can be run in a closed loop. The computer can generate a pattern wave of digital numbers which are converted to analog, then reconverted to digital. The results are checked to see that the two numbers agree within their specified tolerance.

DIGITAL-TO-ANALOG — In a general-purpose system, limits for two specific numbers can be set up with two comparators, and the state of the comparators can be sampled by the computer after the corresponding number has been brought in. Where other numbers are read in, the comparator outputs would not be sampled, of course. For semi-automatic testing, a similar system might be set up with a counter driving some of the bits of the converter and toggle switches driving other bits.

ANALOG-TO-DIGITAL — In a general purpose system, a dc voltage input would be applied and the computer would monitor it to make sure that all the readouts produced the same number or two adjacent numbers.

To test semi-automatically, set a dc voltage input that is as far as possible from any switching point and insert the equivalent number into a bank of toggle switches. The Type R121 AND/NOR Gate can be used to compare the output with the toggle switches. A clock and a few gates can be set up so the converter runs at its maximum rate and stops if the toggle switches and the analog-to-digital converter do not agree.

SETTLING TIME (DIGITAL-TO-ANALOG)

In most applications, the digital-to-analog converter is asked to go through small changes at a time. The worst case transients occur when all the flip-flops change, that is, when the states change from 0111 to 1000.

The settling time with respect to large transients is most important when the converter output is being multiplexed. It can be observed by looking at the signal on a single channel with a high gain scope.

In a system where the multiplexing is done digitally, or where there is only a single channel, the response to large transients is only important when a group of conversions is started; after which the converter will be changing in relatively small steps. If an analog-to-digital converter had been constructed with the same modules, then the response to large transients can be inferred from previous operation. For example, in a successive approximation converter, the settling time for a quarter-scale step must be less than the time per step of the converter.

To observe the settling time more directly, a comparator can be used with one input set to the desired threshold of the dc value of the digital-to-analog converter. The Digital-to-Analog can be switched back and forth, and the comparator output can be monitored on the scope.

RESPONSE TO TRANSIENTS (ANALOG-TO-DIGITAL)

Transient response is extremely important in a converter with multiplexed inputs. The response can be tested in the same way that switching point accuracy is tested. Alternate the input between a test channel and an offset channel. Vary the voltage on the test channel until a switching point is found, and compare this with the switching point that was observed in the steady state test. If the output is observed visually on indicator lights, the voltage on the offset channel should be one which gives all zeros or all ones, so that the alternate voltage can be read clearly.

If the output is being monitored by a computer, the steady state and transient switching points can be measured simultaneously by performing several conversions before changing the channel. The first conversion will give the transient results, the last conversion will give the steady state results. A check should be made with the offset and test channels at nearly opposite ends of the voltage range. Do not use end points, as the converter saturates and overshoot would not be detected. The first decision point should be tested. In a successive approximation converter, for example, the first decision is whether the input is above or below half-scale.

In a single channel system, the transient response is only important for the first conversion. It can be checked manually, running the converter from a push-button and changing the input voltage manually. The general approach would be the same as for a multiplexed system.

Operating Checks

Operating checks are made to assure that the equipment has not been damaged, wires have not been pulled off, or other catastrophic failures have not occurred. If properly set up, the check also detects drift, so that the converter will never actually reach a point where it needs realignment. Generally the test should be simple and should be a part of the overall preventative maintenance routine for the equipment. In a general purpose computing facility with both types of conversion systems, a closed loop test can be run very simply by plugging the digital-to-analog converter into the analog-to-digital converter and comparing the results that come back with the original number.

If a converter is being tested separately, a simple test can be made on the worst case points. If precision equipment is not readily available for the test, the converter can be checked against a divided-down value of its own internal reference.

GENERAL-PURPOSE ANALOG-TO-DIGITAL CONVERTER AND MULTIPLEXER CONTROL

Digital is now offering its general-purpose analog-to-digital converter (ADC-1) and multiplexer control (AMX-1) as separate units or as a combined converter-multiplexer (CMX 1). Optional equipment includes input amplifiers to obtain high impedance or "standardize" the input signal, sample and hold circuitry, and interfacing for the PDP-8, PDP-8/S, or PDP-9 computers.

ADC-1 CONVERTER SPECIFICATIONS

The ADC-1 converts an analog voltage to a binary number. Three convenient switches are mounted on the INDICATOR/CONTROL PANEL; a POWER ON/OFF switch is a 117-volt input power disconnect. The ADC switch is a normally open pushbutton that initiates an A/D conversion whenever the switch is activated. The WORD LENGTH control is a rotary switch used to select the word length, the conversion accuracy, and the conversion time. The WORD LENGTH switch selects the following characteristics:

TABLE 1. CONVERSION ACCURACY AND
TIME AT SELECTED WORD LENGTHS

Word Length (No. of bits)	Max Switching Point Error*	Conversion Time (μsec)
6	±1.6%	9.0
7	±0.8%	10.5
8	±0.4%	12.0
9	±0.2%	13.5
10	±0.1%	18.0
11	±0.05%	25.0
12	±0.025%	35.0

*±½ LSB for quantizing error.

A completely wired back panel includes an A/D Converter, interfacing for the PDP computers, an optional multiplexer control with up to 64 input channels and amplifier output, and provisions for a sample and hold amplifier (A400).

If the converter is used with a PDP computer, conversions are initiated by an IN/OUT Transfer instruction. If the converter is used separately, a CONVERT A-D PULSE is necessary to initiate conversion.

ACCURACY: See Table 1.

CONVERSION TIME: See Table 1.

APERTURE TIME: Same as conversion time.

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CONVERTER RECOVERY TIME: None.

INPUT: 0 to $-10v$ standard. Input scaling may be specified using the amplifier option.

INPUT LOADING: $\pm 1\mu 2$ amp and 125 pf for 0 to $-10v$ input signal.

OUTPUT: Binary number of 6 to 12 bits, with negative numbers represented in 2's complement notation. A 0v input gives a 4000_8; a $-5v$ input a 0000_8 and a $-10v$ (minus 1 LSB) input gives 3777_8 number.

CONTROLS: Power ON/OFF switch, ADC switch, binary readout indicators and a seven position rotary switch which selects word length and conversion rate are provided.

The convert A/D pulse input requires a negative pulse (0 to $-3v$) of at least 150-nsec duration. The pulse loading is 1 ma at ground.

At the completion of the conversion process, two complementary A/D DONE levels initiate external reading of the converted data. This level remains in the A/D DONE state until an external clear flag pulse is generated or another convert A/D pulse is given. If used with a PDP computer, the flag is cleared when the read buffer command is given.

The clear flag requires a negative pulse (0 to $-3v$) of at least 100-nsec duration. The pulse loading is 1 ma at ground.

POWER: Module power is supplied through one H701 power supply and one H704 regulated power supply. Input power; 117 volts at less than ½ amp.

OPERATING TEMPERATURE RANGE: 0°C to 50°C

MECHANICAL: Panel Width: 19 inches
Panel Height: 8¹¹⁄₁₆ inches
Depth: 22 inches

AMX-1 MULTIPLEXER CONTROL SPECIFICATIONS

The AMX-1 Multiplex Control can include from 1 to 16 A121 Multiplex Switch Modules. The user, therefore, may select any multiple of 4 channels to a maximum of 64.

The AMX-1 may be used in either the Random Access or Sequential modes. In the Random Mode the controller routes the analog signal from any selected channel to a single (bussed) output. In the sequential address mode, the controller advances its channel address by one each time an "Index" command is received. After indexing through the maximum number of channels implemented, the address is returned to zero. When in the sequential mode, the conditioning levels for random addressing are ignored.

The on-resistance of the A121 Multiplexer switch is as high as 450 ohms. Therefore, it is suggested that the device which monitors the multiplexer output have an input impedance of greater than 10^6 ohms. A high input impedance minimizes offset error.

The AH03 Amplifier option may be used to raise the multiplexer input impedance and/or to scale the input signal.

Four convenience switches are mounted on the control/indicator panel: a power switch to control the AC power to the Type AMX-1 Multiplier, an ADC pushbutton switch to initiate a conversion manually; a CLR pushbutton to set the Multiplexer address to channel 0 manually; and an index pushbutton to increment the multiplexer address manually. The ADC pushbutton is not used on the AMX-1.

The control indicator panel also contains six indicators to display the current multiplexer address, and a power off-on indicator.

Multiplexer Switches

The multiplexer can include from 1 to 16 Type A121 Switch Modules. Each module contains four single-pole, high speed, insulated gate FET switches with appropriate gating. The Type A121 Switches are arranged as a 64-channel group of series-switched single-pole switches with a separate continuous ground wire for each signal input. The switched signal input wire and the continuous ground for each channel are run as twisted pairs to the input connectors mounted on the rear panel. The continuous grounds for all channels are to be terminated at the high quality ground at the user's analog source.

SPECIFICATIONS: (Measured at input connector)

Input signal (max)	$\pm10v$
Input current (max)	1.0 ma
"On" offset voltage	0
"On" resistance (max)	450 ohms
"Off" leakage (max)	10 na
Turn-on delay	150 nsec
Turn-off delay	250 nsec
Settling time to 1-LSB (source $Z \leq 1$ ohm)	≤ 2 μsec

POWER: Module power is supplied through one H701 Power Supply and one H702 Regulated Power Supply. Input power is 117 v at less than $\frac{1}{2}$ amp.

OPERATING TEMPERATURE RANGE: 0 to 50° C

MECHANICAL: Panel width, 19 inches; Panel height, $8\frac{11}{16}$ inches; Depth $19\frac{1}{2}$ inches; Weight, 25 lbs.; BTU/hr., 188.

AH03 AMPLIFIER OPTION

The AH03 consists of a DEC amplifier (part #1505379) mounted on an A990 Amplifier Board with appropriate scaling networks and gain trim and balance potentiometers.

Interface Options

Interface options are offered so that the AMX-1 may function as a peripheral device on PDP Computers or data logging equipment. Standard interface options for the PDP-8, PDP-8/S, and the PDP-9 computers are designed to operate on the computer Input-Output (I/O) Bus. The necessary IOT commands and diagnostic programs are supplied with these interfaces.

IF 8 — 8/S:
This option interfaces the AMX-1 to the PDP-8 or PDP-8/S computer.

IF 9:
This option interfaces the AMX-1 to the PDP-9 Computer.

Information on special interfaces is available on request.

CMX-1 CONVERTER AND MULTIPLEXER

The CMX-1 combination with computer interface is available as the AF01A (PDP-8, 8/S) AF01B (PDP-9) interface. As such, it is considered a computer peripheral, and check out and installation is included in the price if purchased and delivered with a computer system.

The computer interface options also may be purchased as modules and cables from this catalog and installed by the customer who takes responsibility for check-out.

Modules required for PDP-8 and 8/S interface:

1	R111
2	R123
2	W103
Bus Cables	

Modules for PDP-9 Interface:

3	W103
1	W500
1	R202
1	R107
4	R123
2	W640
Bus Cables	

A/D Converter (ADC 1)	— $2,000.00
64 Channel Multiplexer (AMX-1) Plus $16.25 per channel	— $2,250.00
Converter-Multiplexer (CMX-1) Plus $16.25 per channel	— $3,300.00
Options	
Input Amplifier	— $ 300.00
Sample and Hold	— $ 500.00
IF8-8/S	— $1,200.00
IF9	— $1,265.00
AF01A, AF01B	— $4,500.00

PART VI: COMPUTER CATALOG

PDP COMPUTERS

PDP general-purpose digital computers are used for a wide variety of data processing and control functions. PDP's are constructed of highly reliable FLIP-CHIP digital circuit modules, and include built-in provisions for marginal checking. The resulting overall reliability has earned PDP's a reputation for trouble-free performance. An exceptionally varied line of input-output devices are available, and versatile facilities are provided in the computers to handle these and other devices.

A complete, well-documented package of programming aids accompanies each PDP computer. The package includes a FORTRAN compiler, a symbolic assembler, on-line debugging routines, an editor, and utility, arithmetic, and maintenance routines. Editing and on-line debugging programs use the same symbolic language as the assembly systems. This means that debugging is carried out in the same language as the program being debugged, eliminating the creation and reassembly of new symbolic tapes each time an error is found.

The arithmetic subroutines include a floating point package. Input-output subroutines are prepared for most of Digital's standard optional devices. Extensive maintenance routines are provided. Supporting these programming aids are free training courses at Digital and membership in DECUS, the Digital Equipment Computer Users Society. DECUS provides a means for users to exchange ideas and programs through regularly scheduled symposia. A library of fully documented programs is maintained.

PDP-8/I

The PDP-8/I is the newest member in Digital's Family-of-Eight computers. These include the PDP-8, PDP-8/S, DISPLAY-8, TYPESETTING-8, MULTI-ANALYZER-8, and the LINC-8.

The PDP-8/I offers the power, speed, and expandability of the highly successful PDP-8, but at a significantly lower price. It provides a new ease of interfacing with a wide range of DEC peripherals, including the new random access disk file. It offers a programming system field-proven in nearly 2000 Family-of-Eight installations.

The basic PDP-8/I system features a 1.5 microsecond random access core memory and includes 4096 words of 12-bit ferrite core memory, with a plug-in capability of 8192 words in the basic machine; keyboard printer and tape reader punch. Pre-wiring is also included for a high speed paper tape reader and punch, a 100 card-per-minute card reader, an incremental plotter and a scope display as well.

In addition to Digital's new DECdisk, the PDP-8/I operates with a number of other optional devices such as DECtape, high speed perforated tape readers and punches, card equipment, a line printer, analog-to-digital converters, cathode ray tube displays and magnetic drum systems.

### SPECIFICATIONS:
Word Length: 12 bits
Memory: 4096 to 32,768 words; cycle time 1.5 microseconds
Add Time: 3.0 microseconds
In-Out Transfer Rates: 7,992,000 bits per second
Standard I/O Devices: Printer-keyboard with paper tape punch and reader

PDP-8

The PDP-8 is a general-purpose, stored-program computer, featuring a 1.5 microsecond random access core memory, a fast arithmetic processor, and a buffered input-output control. These features combine to make the PDP-8 one of the most popular on-line computers for physics and biomedical analysis and process control. The PDP-8 is also used in large systems as a control element and as a training computer.

The PDP-8 is easy to install, maintain, and use, with comprehensive software, customer-tested in over 1000 installations. The basic system includes 4096 words of 12-bit ferrite core memory, keyboard-printer and tape reader-punch, eight auto-index registers, wired-in analog-to-digital converter, program interrupt, data interrupt, and indirect addressing.

A partial list of central processor options includes the Extended Arithmetic Element for high speed, double precision arithmetic; Memory Modules and Control for increasing memory size in increments of 4096 words to 32,768 words; a Data Channel Multiplexer providing direct memory access for seven external devices; a Serial Drum for storage of 65,536 to 262,144 words and a 32,768 word random access memory disc.

The applications success of the PDP-8 has led Digital to develop a series of computers based on the PDP-8 to meet a number of special needs, resulting in a unique family of small computer products. These include the DISPLAY 8, the LINC-8, the TYPESETTING-8, the MULTIANALYZER-8, the PDP-8/S, and the new PDP-8/I.

SPECIFICATIONS:
Word Length: 12 bits
Memory: 4096 to 32,768 words; cycle time 1.5 microseconds
Add Time: 3.0 microseconds
In-Out Transfer Rates: 7,992,000 bits per second
**Standard I/O Devices:** Printer-keyboard with paper tape punch and reader
Instructions: 49 with standard equipment, expandable to over 100 as optional equipment is added.
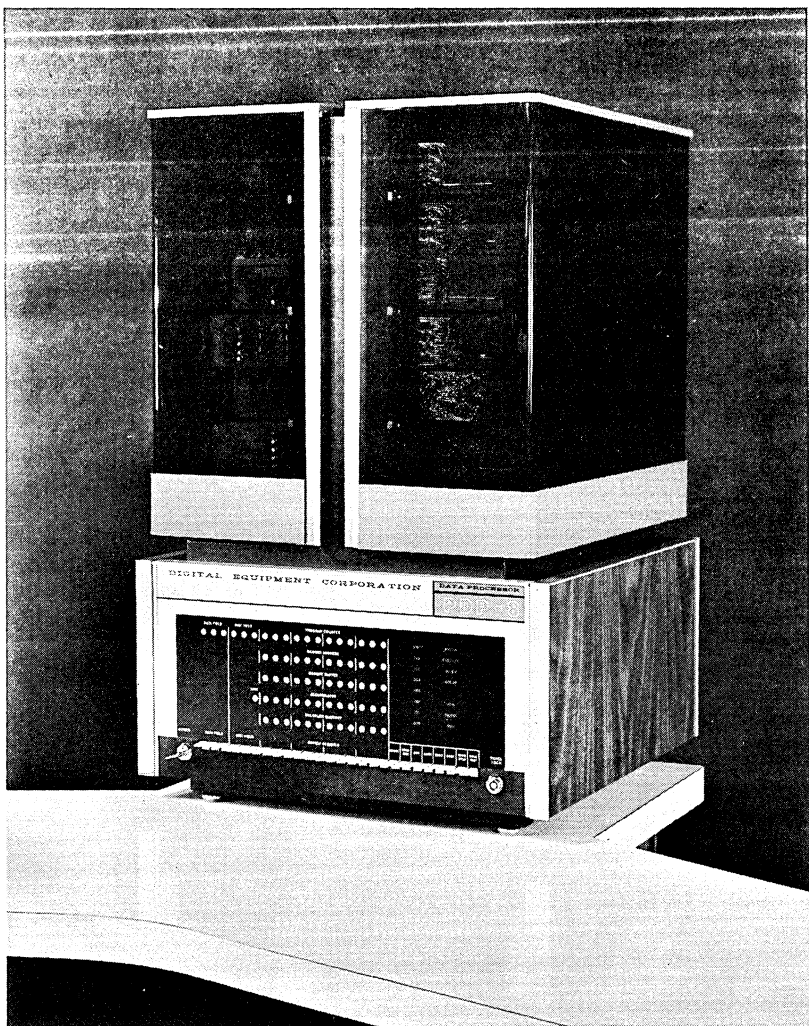
PDP-8/S

The PDP-8/S is the first full-scale, general-purpose, core-memory digital computer selling for under $10,000; it is designed for data handling and for controlling complex process system.

The PDP-8/S has the same size memory, the same input/output capabilities, the same extensive set of standard options as the PDP-8. Both use the same software. The difference between the two machines is in speed and physical size. The PDP-8/S adds in 36 microseconds compared with an add time of 3.0 microseconds for the PDP-8. The basic 12-bit-word PDP-8/S features an 8-microsecond, 4096-word, expandable core memory; a comprehensive software package, including FORTRAN; and an ASR-33 Teletype. Although the PDP-8/S combines a fully parallel core memory and input/output facility with a serial arithmetic unit, the machine appears to be fully parallel to the user. Flexible, high capacity, input/output capabilities of the computer operate a variety of peripheral equipment. In addition to the standard teletype and perforated tape equipment, the system can operate in conjunction with most of the optional devices offered in the PDP-8 family line. Equipment of special design is easily adapted for connection into the PDP-8/S system. The computer need not be modified to add peripheral devices.

SPECIFICATIONS:

Word length: 12 bits
Memory: 4096 to 32,768: cycle time 8.0 microseconds
Add Time: 36 microseconds
In-Out Transfer Rate: 1,500,000 bits per second
Standard I/O Devices: Printer-keyboard with paper tape punch and reader.
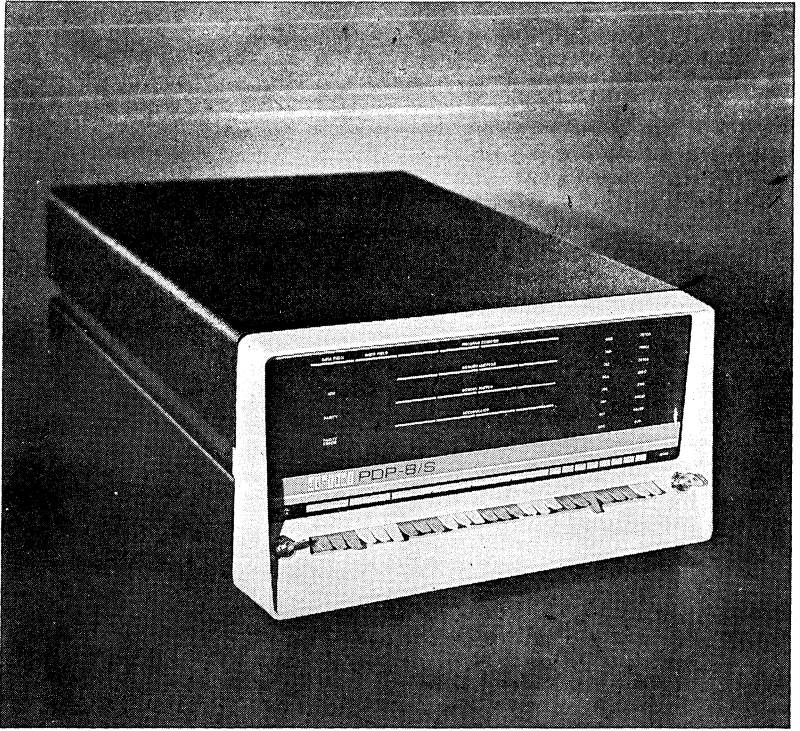
LINC-8

The LINC-8 is a computer-based system designed to control experiments and collect and analyze data in the laboratory. The system combines the features of the PDP-8 and the LINC computers, and allows the researcher to choose between the two programming systems available. The researcher simply uses one of the two consoles in the system. Typical biomedical applications for the new system are: arterial shock wave measurements in-phase triggering of stimuli from EEG alpha waves, processing of single-unit data from the nervous system. EKG processing, and operative conditioning applications.

Other applications for the LINC-8 include research in physics, chemistry, meteorology, oceanography, psychology, radiation, seismology, and acoustics.

The original LINC hardware and software were developed for on-line, real-time laboratory research under grants from the National Institutes of Health and the National Aeronautics and Space Administration. Development began at Massachusetts Institute of Technology and continued at Washington University in St. Louis.

The LINC-8 system includes: a built-in multiplexed analog to digital input facility, a relay register, dual digital LINCtape transports, an alphanumeric oscilloscope display and an ASR-33 teletypewriter. The LINC-8 takes advantage of the PDP-8's input/output bus for additional convenience in interfacing other laboratory instrumentation to the LINC-8 system.

With the LINC-8, the researcher has the option of using the LINC software which has been designed to allow the researcher to write his own programs after minimum instruction or he may use the more advanced PDP-8 programming system which includes FORTRAN. The LINC-8 system "talks" with researchers by displaying instructions and results on the oscilloscope display. Displays combine English language with data displays. To familiarize customers with the new system, Digital offers four courses in programming and maintenance of the LINC-8. These are included in the basic system purchase price.
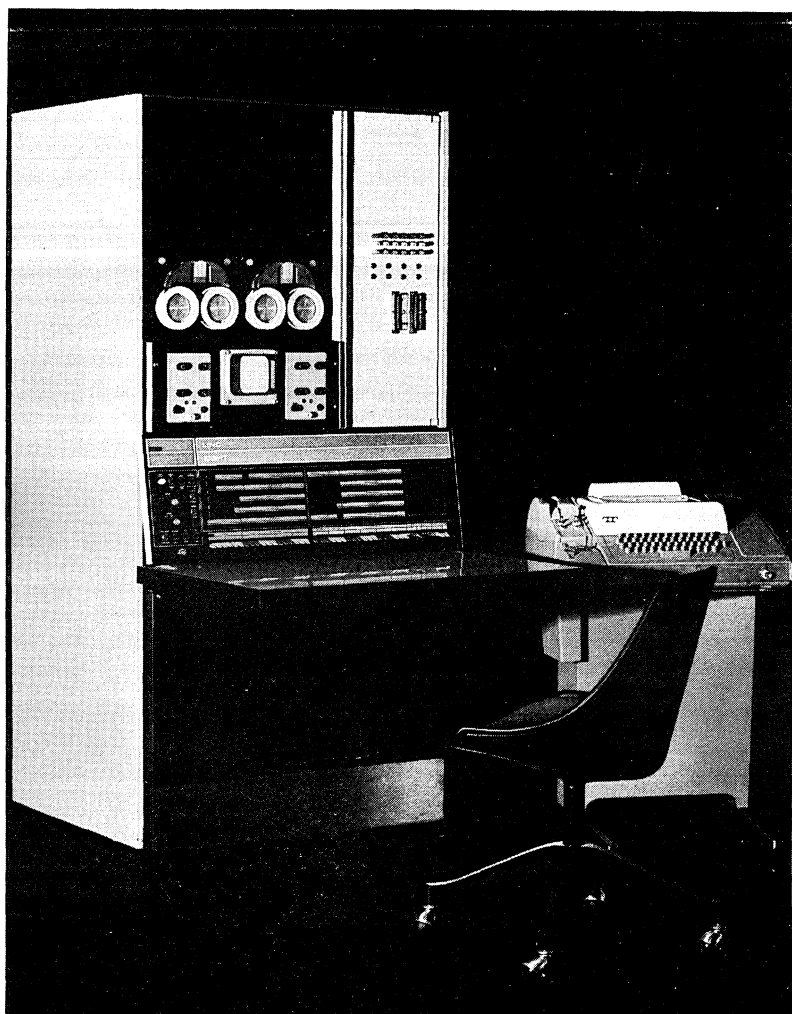
DISPLAY-8

The DISPLAY-8 (Type 338 Programmed Buffered Display) is an integrated cathode-ray-tube system containing its own general-purpose computer. It is capable of precisely displaying points lines, and characters, and of performing extensive computation using the computer order code and a complete software package.

The computer is a PDP-8. It is fast enough to perform 2,000,000 additions per second while displaying 300,000 points, 600 inches of vector, or 700 characters flicker free at the same time. The highly flexible character generator produces alphabetical characters or special symbols, similar to those used on electronic circuit schematic, with equal ease.

The 338 can be used as a self-contained display system or as a buffered display station in a large computer system. The 338 can control interfaces to external data sources, such as the central computer in a large system, and can handle real time requests, such as data phone interrupts. The 338 can be programmed to view selected small areas of a large stored drawing: 10 by 10 inch window can be moved randomly about a 6 by 6 foot drawing for detailed examination and modification.

The system contains the following features for general purpose computations: An extensive software package that includes FORTRAN, symbolic assembler, debugging programs, floating point arithmetic, and display maintenance programs; 4096 words of core memory; program interrupt; and keyboard-printer and 10-hertz paper-reader punch. The 338 ﹐ ﹐be expanded using any standard PDP-8 plug-in units.
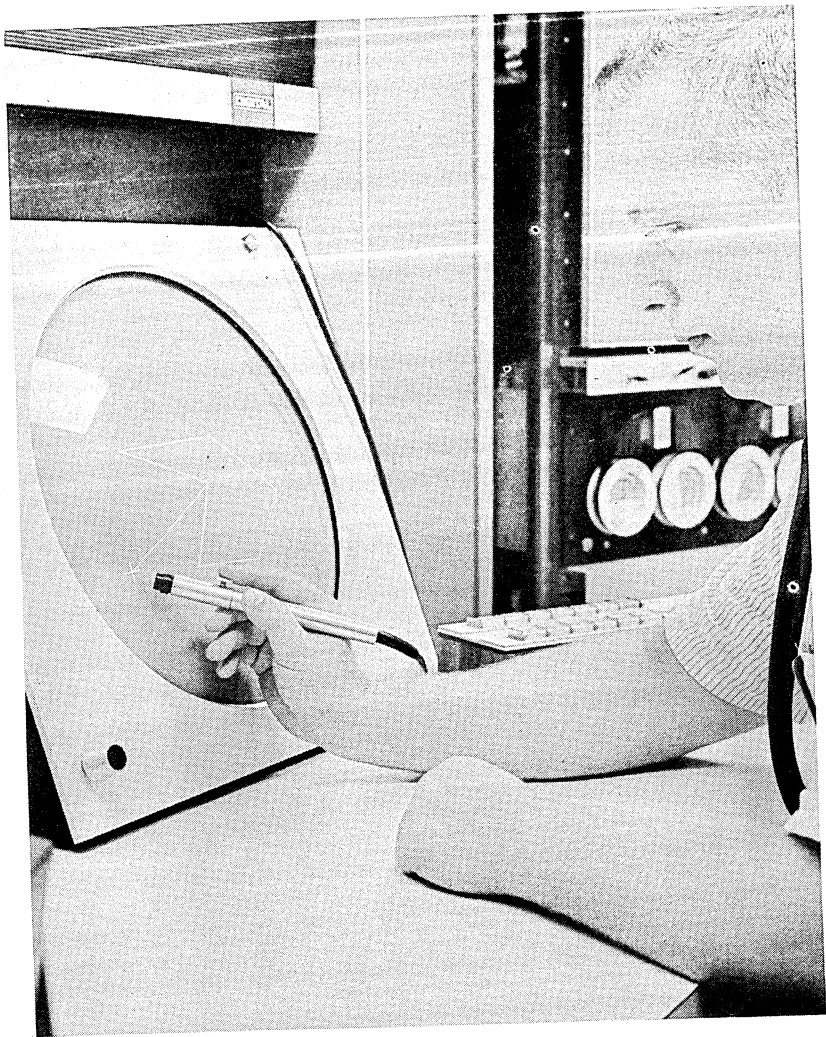
PDP-9

The PDP-9 is a stored-program, general-purpose digital computer, designed to handle a variety of on-line and real-time scientific applications calling for more computation power than offered by the PDP-8. The basic PDP-9 features a 2-microsecond add time; 8,192 words of 18 bit (plus optional parity bit) core memory; a real-time clock; a 300-character-per-second paper tape reader; a 50-character-per-second tape punch; and input-output teleprinter (Teletype Model KSR-33), Input/Output can be via programmed transfers, data channel transfers, or direct memory access. The maximum I/O transfer rate is 18,000,000 bits-per-second.

Single address instructions are used, with auto-indexing and one level of in-direct addressing permitted. A single memory reference instruction can directly address any location in a block of 8,192 words of memory. PDP-9 has a Direct Memory Access channel plus four built-in Data Channels.

The memory can be expanded in 8,192-word increments to a total of 32,768 words. Mass storage devices, such as DECtape, IBM compatible magnetic tape, disks and drums are available as options for the PDP-9, as are a wide variety of other input-output devices and central-processor additions.

A comprehensive software package including FORTRAN IV, a MACRO Symbolic Assembler, a monitor system, and diagnostic routines is provided with the basic machine. With the modular software package, PDP-9 users can program in a device-independent environment to take full advantage of configurations with mass storage devices and central processor options.

Applications for the PDP-9 include its use in biomedicine, process control, chemical instrumentation, display processing, hybrid systems and data communications. A special configuration, the PDP-9 MULTIANALYZER, has been designed for physics applications.

SPECIFICATIONS:

Word length: 18 bits
Memory: 8,192 to 32,768 words in 8,192 word increments
Cycle time: 1.0 microseconds
Add Time: 2 microseconds
In-Out Transfer Rate: Up to 18,000,000 Bits per second
Standard I/O Devices: A 300 character-per-second paper tape reader, a 50 character-per-second paper tape punch and a 10 character-per-second KSR-33 teletype.
Options: DEC Tape, IBM Compatible magnetic tape, drums, CTRS, A/D con verters, line printers, card readers, plotters, etc.

PDP-10

PDP-10 is an expandable, 36-bit computer system available in five configurations (PDP-10/10, 10/20, 10/30, 10/40, and 10/50) and offering optimum power and versatility in the medium price range.

The PDP-10 includes an extremely powerful processor with 15 index registers, 16 accumulators, and 8,192 words of 36-bit core memory, a 300-character-per-second paper tape reader, a 50-character-per-second paper tape punch, a console teleprinter, and a two-level priority interrupt subsystem. PDP-10/20 adds two DEC tapes. PDP-10/30 includes 16,384 words of memory and additional I/O devices. PDP-10/40 adds an extended order code and a memory protection and relocation feature. And PDP-10/50 permits swapping between 32,768 words or more of memory and fast access disc file via the multiplexer/selector channel, and includes multiprogramming time-sharing software.

The PDP-10 is designed for on-line and real-time applications such as physics and biomedical research, process control, as a departmental computation facility, in simulation and aerospace, chemical instrumentation, display processing and as a science teaching aid.

The software package includes real-time FORTRAN IV, a control monitor, a macro assembler, a context editor, a symbolic debugging program, an I/O controller, a peripheral interchange program, a desk calculator and library programs. All software systems assure upward compatibility from the standard 8,192 words of memory through the multiprogramming and swapping systems at both the symbolic and relocatable binary level.

PDP-10 features a 1-microsecond cycle time, a 2.1-microsecond add time, I/O transfer rates up to 7,200,000 bits per second and a modular, proven software package that expands to make full use of all hardware configurations. Memory can be expanded in 8,192 word increments to the maximum directly addressable 262,144 words.
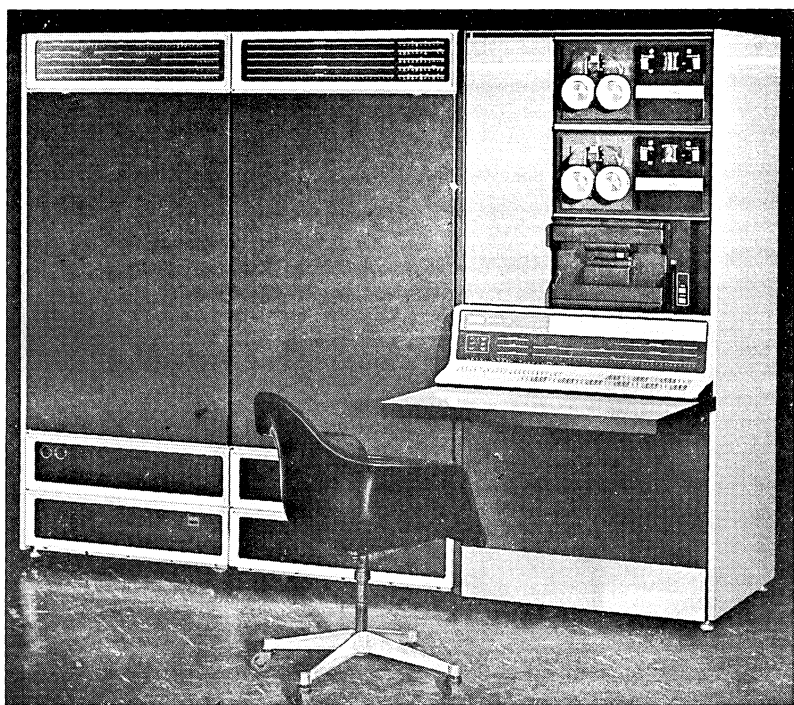
DIGITAL TEST SYSTEMS

DEC designs and manufactures a variety of devices for testing computer components and similar products. The Company uses these products in its own operations and also markets them to a regularly growing list of customers.

DEC memory test products are used by nearly every major manufacturer of core memories (memories such as the ones DEC uses in its computers). This equipment is used to check each stage of the computer memory assembly from the single core to the completed unit.

DEC has recently announced a memory test system, the PMA-8 (Programmable Memory Analyzer-8), which incorporates the PDP-8 as its control element. The speed and versatility of the PMA-8 is a major contribution to the memory testing field.

Automatic Module Testers are another Digital Test System product. Equipment such as the tester shown in the photo, is used by DEC and other companies who manufacture large quantities of their own modules to perform functional tests on completed modules. The tester controlled by a PDP computer, can perform from 10 to 100 different static and dynamic tests on a module in one second.

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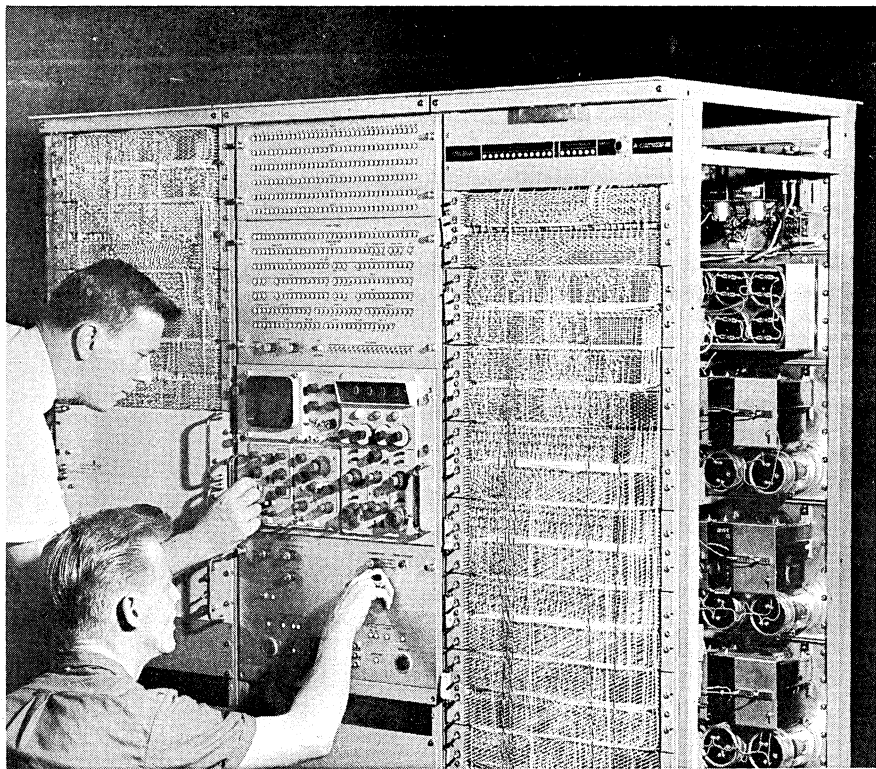
GENERAL PURPOSE ANALOG-DIGITAL
CONVERTER/MULTIPLEXERS

Digital offers a wide range of analog-digital and digital-analog converters from a 10-bit single-buffered D/A Converter contained on one double-width FLIP-CHIP™ Module card to a multiplexed integrating digital voltmeter with guarded reed relay scanner providing 140db of common mode rejection and expandable to 2,000 input channels.

Digital's analog-digital converter/multiplexer system is a combined unit with interface for the PDP-8, PDP-8/S and PDP-9 computers. The converter and multiplexer are available either as separate units or as a combined unit without computer interfacing. Optional equipment includes input amplifiers and sample and hold circuitry. The converter offers seven front panel selections of speed and word length. Maximum speed: 6 bits, 1.6% accuracy, 9 microseconds. Maximum accuracy: 12 bits, 0.025% accuracy, 35 microseconds. The multiplexer includes from one to 16 multiplexer switch modules, depending on the number of channels required. Any multiple of four channels may be selected to a maximum of 64. The time required to switch from one channel to another is 10 microseconds to within 1 millivolt of the final voltage. The multiplexer/converter combination is conveniently packaged in a single chassis 19 inches wide by 8-11/16 inches high by 19-1/2 inches deep.

DIGITAL also offers a new analog-digital converter for use with the PDP-8 or PDP-8/S computers to convert an analog input signal to a ten-bit binary number. The A/D Converter is a general purpose successive-approximation type with an accuracy of 0.1% of full scale ±1/2 LSB and a conversion time of 10 μsec. The converter includes cables for connection to the PDP-8 or PDP-8/S I/O Bus and a complete software package with IOT's and diagnostics.
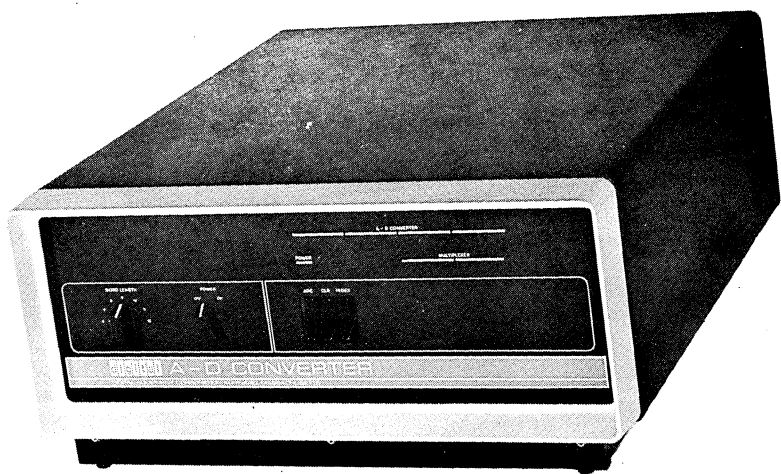
INPUT-OUTPUT OPTIONS

MAGNETIC TAPE EQUIPMENT

DECtape, a unique fixed address magnetic tape system, allows on-line program debugging or high speed loading and readout. Density is 375 ± 60 bpi; tape speed is 80 ips with a 15 kc character rate. Reads and writes in both directions: redundant tracks allow less than one transient error in 10^{10} characters. Total storage, the equivalent of 4000 feet of perforated tape, is three million bits per reel.

Other magnetic tape systems include automatic and programmed controls and high or low density transports. Formats are IBM compatible at recording densities of 200, 556, and 800 bpi. Transfer rates range from 15 to 90 thousand characters per second. Transports include an electro-pneumatic design of high performance and low tape stress and wear.

RANDOM ACCESS DISC

A new DECdisc random access memory storage device significantly expands the memory capacity of the PDP-8/I, PDP-8, and PDP-8/S computers. The DF 32 has a capacity of 32,768 thirteen bit words (12 bits plus parity) with capability of expansion to 131,072 words. It is a fixed disc with one head per track. Transfer rate is 66 microseconds per 12 bit word. Average access time is 16.67 milliseconds.

MAGNETIC DRUM SYSTEMS

Drums provide auxiliary mass storage with direct access to memory. Sizes range from a 32,768 word drum to 262,144 words.

DISPLAY AND PLOTTING EQUIPMENT

Precision and incremental cathode ray tube displays convert digital data into graphic and tabular form. Light Pen detects plotted points to initiate computer action; Symbol Generator plots alphanumeric or special symbols in four sizes on scope face. Incremental Plotters give hard-copy graphs and histograms.

PRINTERS

Automatic line printers produce hard-copy output data from 300 to 1000 lines per minute with 120 or 132 column lines and any of 64 characters per column. Teleprinters permit on line inputs and outputs from the computer console or remote stations at 10 characters per second. Character sets are ACSII.

ANALOG-DIGITAL CONVERTERS

General purpose analog to digital converters offer seven front-panel selections of speed and word length. Maximum speed: 6 bits 1.6%. 9 microseconds. Maximum accuracy: 12 bits 0.025% 35 microseconds. Digital-to-analog equipment has maximum conversion time to an accuracy of one least significant bit of 2 μsec. Speeds may be limited by the repetition rate of the associated equipment.

PERFORATED TAPE AND CARD EQUIPMENT

Paper tape punches operate at 10 to 63 characters per second; readers at 10,300, and 400. Card punch controls permit operation at 100 or 300 cards per minute; card readers at 100, 200, or 800.

APPENDIX 1
MIL-STD-806B AND DEC SYMBOL COMPARISON

This comparison of MIL-STD and DEC Symbology relates MIL-STD symbols to the DEC logical equivalents or combination of equivalents which perform the same function. Designations of high (H) and low (L) are used instead of "1's" and "0's" to avoid the problem of positive and negative assertion.

DEC R-series FLIP-CHIP modules also are related to the appropriate MIL-STD equivalent. In cases where many input gates are provided (such as flip-flops), only a few of the many methods of input connections are illustrated. Output triggering of flip-flops is not shown, but is one of the possible methods of clearing and setting.

MIL-STD-806B gating symbols use a small circles(s) at the input(s) of the logic element to indicate that a relatively low (L) input signal activates the function. The absence of a circle indicates that a relatively high (H) signal activates the function. The presence or absence of a circle at the output of an element indicates that the output is low (L) or high (H) respectively in the activated state.

DEC's high and low level symbology uses this same principle except for a difference in signal indication. A solid diamond (————◆) indicates DEC's low (L) signal level (—3 volts), whereas open diamond (————◇) indicates the high (H) signal level (0 volts or ground). Correspondingly, for pulse signals, a solid arrowhead (————▶) signifies a negative (low) pulse, and open arrowhead (————▷). a positive (high) pulse.

The MIL-STD-806B logic symbols with their DEC equivalents are listed in Table 1. Logically equivalent AND and OR elements for each system with the appropriate Table of Combinations are included.

MIL-STD-806B logic symbols, with their DEC counterpart, for flip-flops, one-shot multivibrators, inverters, etc., are illustrated in Table 2. It should be noted that the input connections of the DEC elements correspond to the MIL-STD operation, symbolically described.

In most cases, the DEC element is capable of greater flexibility of operation if maximum use of input/output gating is utilized.

MIL-STD nomenclature for flip-flop inputs is, set (S), clear (reset) (C), and toggle (trigger) (T). DEC terminology is identical except for the "toggle" input which is termed "complement".

R-series module elements are shown in Table 3 with their MIL-STD symbol. For gating functions, two logically equivalent MIL-STD symbols are compared with the appropriate DEC symbol (shown without the polarity indicators). A table of combinations is included in instances where clarification may be necessary.

DEC R series flip flops, pulse amplifiers, and one shots use diode-capacitor-diode gates to generate and steer pulses to these elements. Operation of the DCD gate is explained in the R-Series section of the handbook. The DCD gate can be represented by symbols listed in MIL-STD-806B as shown below:
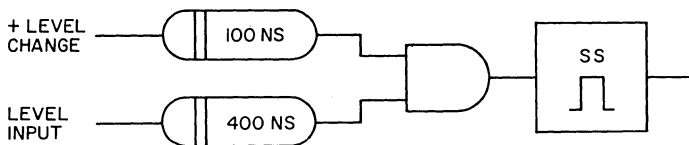
The 400 nanosecond level input represents the set up time of the gate and the + level change delay of 100 nanosecond represents the minimum duration of the positive level. The DEC symbol is:
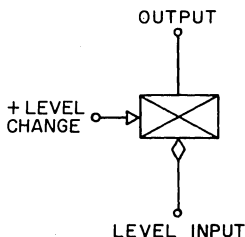
In order that the unwieldy MIL representation need not be shown in the following representations, a new symbol is defined as being the equivalent of the DCD gate.
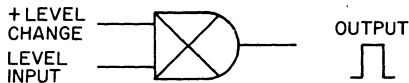
The inputs are defined in the positions shown above, regardless of the orientation of the gate.

In cases where a large number of connections may cause confusion, terminal points are letter referenced for both symbologies.

TABLE 1. GATING SYMBOL EQUIVALENTS

AND	OR	AND	OR	A B X
A B → X	A B → X	(circuit)	(circuit)	H H H H L H L H H L L L
A B → X	A B → X	(circuit)	(circuit)	H H L H L L L H L L L L
A B → X	A B → X	(circuit)	(circuit)	H H L H L L L H L L L L
A B → X	A B → X	(circuit)	(circuit)	H H L H L L L H L L L L
A B → X	A B → X	(circuit)	(circuit)	H H H H L L L H L L L L
A B → X	A B → X	(circuit)	(circuit)	H H L H L H L H H L L H
A B → X	A B → X	(circuit)	(circuit)	H H H H L H L H H L L L
A B → X	A B → X	(circuit)	(circuit)	H H L H L H L H H L L H

EXCLUSIVE OR	EXCLUSIVE OR	A B X
A B → X	A ⊕ B → X	L L L L H H H L H H H L

TABLE 1. GATING SYMBOL EQUIVALENTS

454
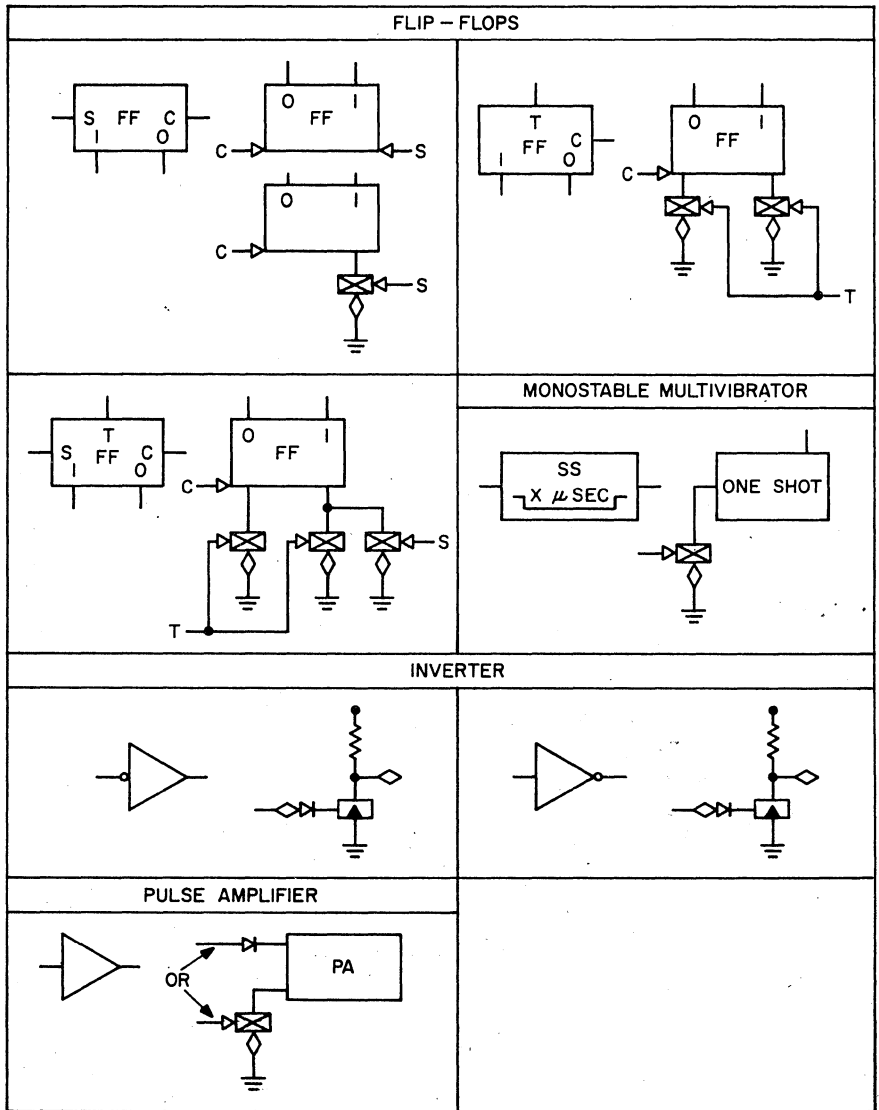
TABLE 2. LOGIC SYMBOL EQUIVALENTS

TYPE	DEC	MIL-STD-806B	A B C D	X
R107 INVERTER			H L	L H
R121 NEGATIVE NAND POSITIVE NOR			H H H L L H L L	L H H H
R111 WITH R001 NEGATIVE NAND POSITIVE NOR			H H H H L H H H L L H H L L L H L L L L ETC	L L L L H
R141 NEGATIVE AND / NOR POSITIVE OR / NAND			H H H H L H L H H L H L H H L L L L H H L L L L ETC	L L L H H H
R122 NEGATIVE NOR POSITIVE NAND			H H H L L H L L	L H H H

TABLE 3. R-SERIES MODULE SYMBOL EQUIVALENTS
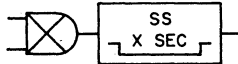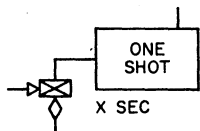
FLIP — FLOPS

R200
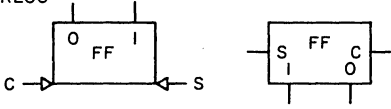
R203
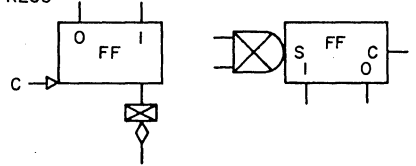
R202

R202

R205

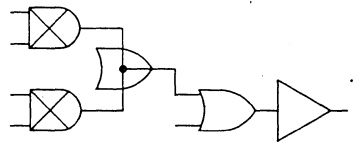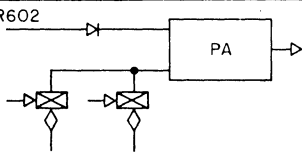R205

457
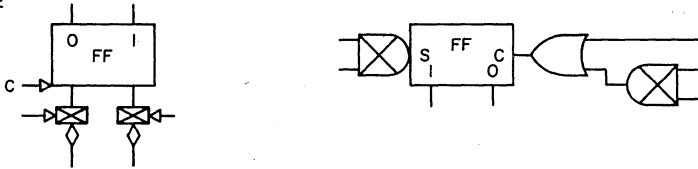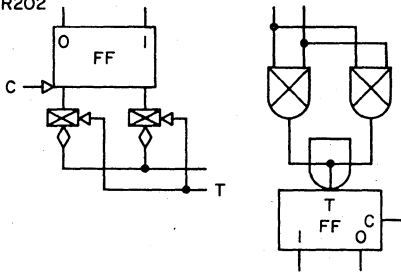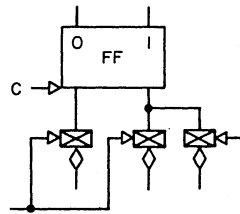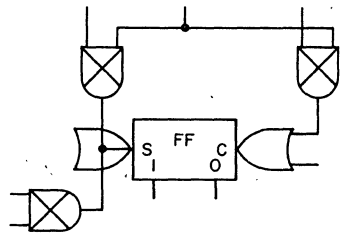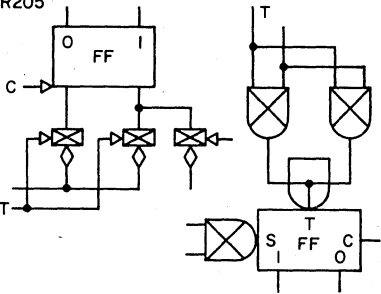
FLIP — FLOPS
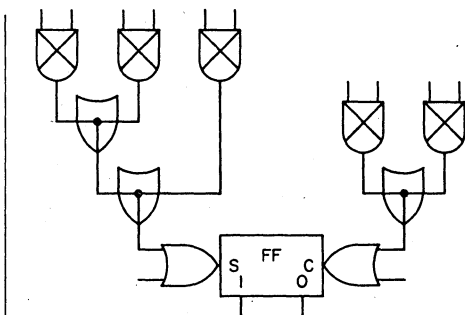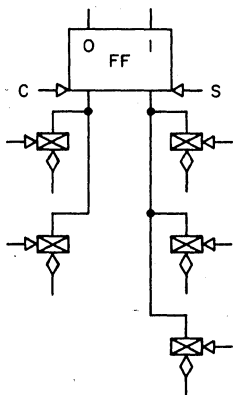
R201

R201
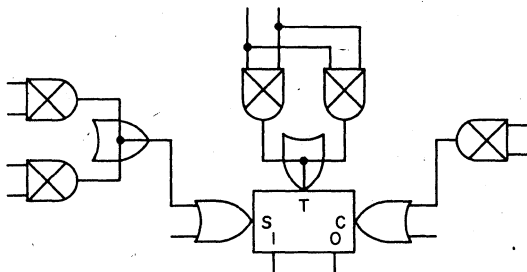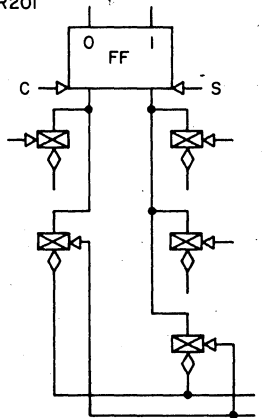
MONOSTABLE MULTIVIBRATOR
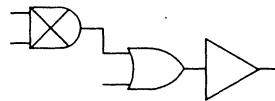
R302

ONE SHOT
X SEC

SS
X SEC

458

PULSE AMPLIFIERS

R601
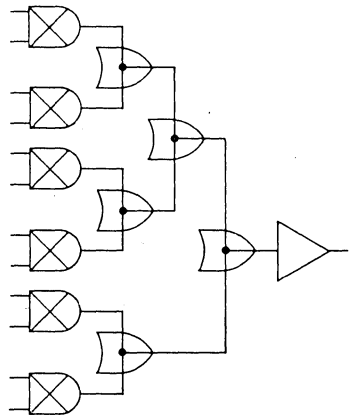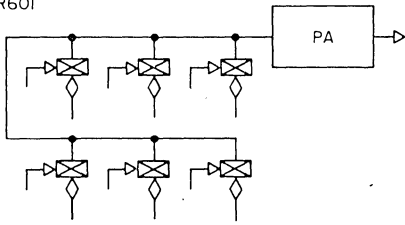
R602

R603

BUS DRIVER

R650

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APPENDIX 2
POWERS OF TWO

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125
1 099 511 627 776	40	0.000 000 000 000 909 494 701 772 928 237 915 039 062 5
2 199 023 255 552	41	0.000 000 000 000 454 747 350 886 464 118 957 519 531 25
4 398 046 511 104	42	0.000 000 000 000 227 373 675 443 232 059 478 759 765 625
8 796 093 022 208	43	0.000 000 000 000 113 686 837 721 616 029 739 379 882 812 5
17 592 186 044 416	44	0.000 000 000 000 056 843 418 860 808 014 869 689 941 406 25
35 184 372 088 832	45	0.000 000 000 000 028 421 709 430 404 007 434 844 970 703 125
70 368 744 177 664	46	0.000 000 000 000 014 210 854 715 202 003 717 422 485 351 562 5
140 737 488 355 328	47	0.000 000 000 000 007 105 427 357 601 001 858 711 242 675 781 25
281 474 976 710 656	48	0.000 000 000 000 003 552 713 678 800 500 929 355 621 337 890 625
562 949 953 421 312	49	0.000 000 000 000 001 776 356 839 400 250 464 677 810 668 945 312 5
1 125 899 906 842 624	50	0.000 000 000 000 000 888 178 419 700 125 232 338 905 334 472 656 25
2 251 799 813 685 248	51	0.000 000 000 000 000 444 089 209 850 062 616 169 452 667 236 328 125
4 503 599 627 370 496	52	0.000 000 000 000 000 222 044 604 925 031 308 084 726 333 618 164 062 5
9 007 199 254 740 992	53	0.000 000 000 000 000 111 022 302 462 515 654 042 363 166 809 082 031 25
18 014 398 509 481 984	54	0.000 000 000 000 000 055 511 151 231 257 827 021 181 583 404 541 015 625
36 028 797 018 963 968	55	0.000 000 000 000 000 027 755 575 615 628 913 510 590 791 702 270 507 812 5
72 057 594 037 927 936	56	0.000 000 000 000 000 013 877 787 807 814 456 755 295 395 851 135 253 906 25
144 115 188 075 855 872	57	0.000 000 000 000 000 006 938 893 903 907 228 377 647 697 925 567 626 953 125
288 230 376 151 711 744	58	0.000 000 000 000 000 003 469 446 951 953 614 188 823 848 962 783 813 476 562 5
576 460 752 303 423 488	59	0.000 000 000 000 000 001 734 723 475 976 807 094 411 924 481 391 906 738 281 25
1 152 921 504 606 846 976	60	0.000 000 000 000 000 000 867 361 737 988 403 547 205 962 240 695 953 369 140 625
2 305 843 009 213 693 952	61	0.000 000 000 000 000 000 433 680 868 994 201 773 602 981 120 347 976 684 570 312 5
4 611 686 018 427 387 904	62	0.000 000 000 000 000 000 216 840 434 497 100 886 801 490 560 173 988 342 285 156 25
9 223 372 036 854 775 808	63	0.000 000 000 000 000 000 108 420 217 248 550 443 400 745 280 086 994 171 142 578 125
18 446 744 073 709 551 616	64	0.000 000 000 000 000 000 054 210 108 624 275 221 700 372 640 043 497 085 571 289 062 5
36 893 488 147 419 103 232	65	0.000 000 000 000 000 000 027 105 054 312 137 610 850 186 320 021 748 542 785 644 531 25
73 786 976 294 838 206 464	66	0.000 000 000 000 000 000 013 552 527 156 068 805 425 093 160 010 874 271 392 822 265 625
147 573 952 589 676 412 928	67	0.000 000 000 000 000 000 006 776 263 578 034 402 712 546 580 005 437 135 696 411 132 812 5
295 147 905 179 352 825 856	68	0.000 000 000 000 000 000 003 388 131 789 017 201 356 273 290 002 718 567 848 205 566 406 25
590 295 810 358 705 651 712	69	0.000 000 000 000 000 000 001 694 065 894 508 600 678 136 645 001 359 283 924 102 783 203 125
1 180 591 620 717 411 303 424	70	0.000 000 000 000 000 000 000 847 032 947 254 300 339 068 322 500 679 641 962 051 391 601 562 5
2 361 183 241 434 822 606 848	71	0.000 000 000 000 000 000 000 423 516 473 627 150 169 534 161 250 339 820 981 025 695 800 781 25
4 722 366 482 869 645 213 696	72	0.000 000 000 000 000 000 000 211 758 236 813 575 084 767 080 625 169 910 490 512 847 900 390 625

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APPENDIX 3
ABBREVIATIONS

Frequency

Hz = Hertz = cycles per second
KHz = 10^3 Hertz
MHz = 10^4 Hertz

Time

msec = millisecond = 10^{-3} second
μsec = microsecond = 10^{-6} second
nsec = nanosecond = 10^{-9} second

Current

amp = ampere
ma = milliampere = 10^{-3} ampere
μa = microampere = 10^{-6} ampere
na = nanoampere = 10^{-9} ampere

Voltage

v = volt
mv = millivolt = 10^{-3} volt
μv = microvolt = 10^{-6} volt

Resistance

K = kilohm = 10^3 ohms
meg = megohm = 10^6 ohm

Capacitance

μf = microfarad = 10^{-6} farad
nf = nanofarad = 10^{-9} farad
pf = picofarad = 10^{-12} farad

Other

ac = alternating current
BD = bus driver
CD = capacitor-diode
D = delay
dc = direct current
DCD = diode-capacitor-diode
DEC = Digital Equipment Corporation
FF = flip-flop
LA = level amplifier
MP = mounting panel
PA = pulse amplifier
PG = pulse generator
P-P = peak to peak
PS = power supply

APPENDIX 4
DEFINITIONS

TIMING DEFINITIONS

Level Delay Time is the time delay between the point of 10% input change and the point of 10% output change in a given circuit. The input is assumed to be the output of a flip-flop of the same frequency series as the circuit under discussion, or a level change with similar characteristics. This is also referred to as delay for output fall or delay for output rise.

Pulse Delay Time is the time delay between the point of 10% input change and the point of 10% output change in a given circuit, when the input is a standard pulse of the same frequency line as the circuit under discussion.

Propagation Delay is the average signal delay per stage for many similar circuits connected in cascade.

Rise Time and Fall Time are the time delay between the 10% and 90% points of a voltage change.

Total Transition Time is the time delay between the point of 10% input change and the point of 90% output change in a given circuit. It is the sum of delay time and rise (or fall) time. Rise TTT is total transition time for rising output. Fall TTT is total transition time for falling output.

Set-up Time is the time required for a diode-capacitor-diode gate to open or close after a change of input level. This time is measured from the point of 10% input change.

APPENDIX 5
BIBLIOGRAPHY OF DIGITAL LOGIC

INTRODUCTORY BOOKS

A large number of books are currently becoming available on the principles of digital computers and digital logic. The following four are particularly well written and concise. They are on a level which would be suitable for an undergraduate course, an industrial training course, or for self-study. Only a knowledge of algebra, trigonometry and basic electronics is assumed.

Siegel, Paul, **Understanding Digital Computers**
New York: John Wiley & Sons, Inc., 1961.

> Discusses logic and arithmetic, components and circuits used in logical building blocks, and the functional units of the digital computer.

Bartee, Thomas C., **Digital Computer Fundamentals**
New York: McGraw-Hill, 1960.

> Includes a discussion of computer operations, programming, number systems, basic logical circuits and logical design, and the functional elements of a general purpose computer.

Irwin, Wayne C., **Digital Computer Principles**
Princeton, New Jersey: D. Van Nostrand Company, 1960.

> Puts slightly more emphasis on logic and less on circuitry. It includes a discussion of number systems, a brief discussion of the circuitry, timing, and digital arithmetic, as well as Venn diagrams, Karnaugh maps, and Harvard minimizing chart.

Smith, Charles V. L., **Electronic Digital Computers**
New York: McGraw-Hill, 1959.

> Discusses digital computer arithmetic, instruction codes, basic logic circuits, and functional elements of computers. It includes a variety of specific examples, principally from the parallel direct-coupled asynchronous machine developed at the Institute for Advanced Study at Aberdeen Proving Ground.

LOGICAL DESIGN

The following texts provide a more theoretical treatment of switching theory and machine design. They are suitable for a fourth year undergraduate course, a first year graduate course, or home study by a practicing design engineer or research scientist. The reader should be familiar with college mathematics and basic electronics.

Bartee, Thomas C., Lebow, Irwin L., and Reed, Irving S., **Theory and Design of Digital Machines** New York: McGraw-Hill, 1962

> Combines switching theory and machine design. Including the design of general purpose, special purpose, and sequential machines.

Chu, Yaohan, **Digital Computer Design Fundamentals** New York: McGraw-Hill, 1962

> Discusses arithmetic operations in binary, BCD, floating point, and residue numbers. Also describes circuitry, using different types of modern circuit elements. The text leads to the design of a simple computer.

Ledley, Robert S., **Digital Computer and Control Engineering** New York: McGraw-Hill, 1960

> A thick book that includes programming, systems design, logic design, and circuit design. A simple computer, Pedagac, is designed from start to finish.

Phister, Montgomery, Jr., **Logical Design of Digital Computers** New York: John Wiley & Sons, Inc., 1958

> Develops the design of a computer from boolean equations. It covers all subjects, including circuits, memory, and input output, from a strictly mathematical approach.

Scott, Norman R., **Analog and Digital Computer Technology** New York: McGraw-Hill, 1960

> Excellent basic book on principles and applications of analog and digital computers. Analog topics include general approach to problem solving, representation of nonlinear functions, and amplifier design. Digital topics covered are problem solving approach (very little on programming), number systems, switching and logic circuits and their design, arithmetic and control circuits, and memory elements. Written for graduate and advanced undergraduate electrical engineers.

REFERENCE WORKS

These books are intended primarily as an aid to the practicing designer. Each section is prepared by a specialist in the field, and contains detailed, concise information.

Grabbe, Ramo and Wooldridge (editors)
Handbook of Automation, Computation and Control
New York: John Wiley & Sons, 1959.

> Volume 1 — **Control Fundamentals.** Emphasizes mathematics including sets and relations, Boolean algebra, probability, and statistics, as well as numerical analysis, operations serearch, and information theory.

> Volume 2 — **Computers and Data Processing.** Discusses computer terminology, digital computer programming, the design and use of digital computers, data processors, analog computers, and unusual computer systems. Included in this is a discussion of digital computer circuits, logical design, and techniques for reliability.

> Volume 3 — **Systems and Components.** Includes systems engineering, manufacturing process control, chemical process control, and industrial control. The component section treats selection, mathematical description, and integration of components into systems.

Huskey, Harry D., & Korn, Granino A., **Computer Handbook** New York: McGraw-Hill, 1962

> Section 1 discusses analog computers including terminology, basic building blocks, design of computer systems, and computer applications. Section 2 deals with digital computers, including definitions, components, circuits, logic design, programming, system design, and applications.

NUMERICAL INDEX

PRICE LIST*

Effective February 1, 1968

M Series

M040	SOLENOID DRIVER	Two drivers per module — maximum ratings of 70 watts and 0.6 amp.	$ 39.00
M050	INDICATOR DRIVER	Twelve transistor inverters to drive miniature incandescent bulbs.	$ 31.00
M113	NAND GATES	Ten 2-input NAND gates that also may be used as inverters.	$ 23.00
M115	NAND GATES	Eight 3-input NAND gates.	$ 24.00
M117	NAND GATES	Six 4-input NAND gates.	$ 24.00
M119	NAND GATES	Three 8-input NAND gates.	$ 24.00
M121	AND/NOR GATE	Six AND/NOR gates — can also perform exclusive OR, coincidence, and NOR functions.	$ 25.00
M141	NAND/OR GATES	Two 4-input, one 3-input and one 1-input NAND gates to perform NAND and wired OR functions.	$ 30.00
M160	EXPANDER	Three general purpose AND/NOR gates to select and put on a single output any of several input signals.	$ 35.00
M161	BINARY TO OCTAL/ DECIMAL DECODER	Functional decoding module or a binary-to-octal or binary-coded decimal-to-decimal decoder for up to six bits.	$160.00
M203	8 R/S FLIP-FLOPS	Eight R/S type flip-flops, each with two 2-input cross-coupled NAND gates.	$ 32.00
M204	GENERAL PURPOSE BUFFER & COUNTER	Four J-K type flip-flops augmented by multiple-input AND gates.	$ 36.00
M206	GENERAL PURPOSE FLIP-FLOPS	Six separate D-type flip-flops with independent gated data, clock and dc set inputs.	$ 42.00
M207	GENERAL PURPOSE FLIP-FLOPS	Six J-K type flip-flops for use as buffers, control flip-flops, shift registers and counters.	$ 42.00
M208	8-BIT BUFFER/ SHIFT REGISTER	Internally connected 8-bit buffer/shift register with provisions for gated single-ended parallel load, bipolar parallel output and serial input.	$ 84.00
M211	BINARY UP/DOWN COUNTER	Six bit binary up/down counter that can shift counting mode without disturbing the contents of the counter.	$ 75.00
M302	DUAL DELAY MULTIVIBRATOR	Two delays (one-shot multivibrator) triggered by trailing edge of positive pulse or level change from high to low.	$ 46.00
M401	VARIABLE CLOCK	Stable RC-coupled multivibrator which produces standard timing pulses at adjustable rates.	$ 55.00
M502	NEGATIVE INPUT CONVERTER	Two non-inverting high-speed signal converters.	$ 26.00
M602	PULSE AMPLIFIER	Two pulse amplifiers for power amplification, pulse amplitude and width standardization and pulse formation from level changes.	$ 28.00
M617	POWER NAND GATE	Six 4-input NAND gates capable of driving up to 30 unit loads each.	$ 27.00
M627	NAND POWER AMPLIFIER	Six 4-input NAND gates with power amplification and high speed gatings. Each output can drive 40 unit loads.	$ 32.00
M652	NEGATIVE OUTPUT CONVERTER	Two non-inverting high-speed signal converters providing current drive at low output impedance.	$ 26.00

K Series

K003	GATE EXPANDER	Three 3-input gates for expansion of K113 and K123.	$ 4.00
K012	GATE EXPANDER	Three 4-input OR gate expanders for K113 and K123.	$ 7.00
K113	LOGIC GATES	Three 2-input inverting gates expandable at either the NAND or NOR modes.	$ 11.00
K123	LOGIC GATES	Three 2-input non-inverting gates expandable at either the AND or OR modes.	$ 12.00
K184	RATE MULTIPLIER	Four-bit rate multiplier which emits a pulse train equal to the product of signals presented at inputs "FF" and "G".	$ 18.00

*Normal delivery off-the-shelf for all items listed.

K202	FLIP-FLOP	Two general-purpose gated flip-flops which can shift, complement, count and expand K210 counters or K230 shift registers.	$ 27.00
K210	COUNTER	Four-bit binary-coded-decimal or binary counter that can return to zero after any number of input cycles from 2 to 16.	$ 27.00
K220	BCD UP/DOWN COUNTER	Four-bit binary coded decimal up/down counter.	$ 52.00
K230	SHIFT REGISTER	Four-bit shift register can form a shift register up to 20 bits long by tying 5 K230's together.	$ 36.00
K273	RETENTIVE MEMORY	Three-bit retentive memory has three magnetically latched mercury wetted contact relays.	$ 72.00
K303	TIMER	Three remotely controllable timers provide time delays from 10 micro-seconds to 30 seconds.	$ 27.00
K371	TIMER CONTROL	Calibrated control for 6 KHz to 200 Hz.	$ 8.00
K373	TIMER CONTROL	Calibrated control for 60 Hz to 20 Hz.	$ 8.00
K374	TIMER CONTROL	Calibrated control for .01 to 0.3 sec.	$ 7.00
K375	TIMER CONTROL	Calibrated control for 60 Hz to 2 Hz.	$ 8.00
K376	TIMER CONTROL	Calibrated control for 0.1 to 3 sec.	$ 7.00
K378	TIMER CONTROL	Calibrated control for 1 to 30 sec.	$ 9.00
K508	AC INPUT CONVERTER	Eight AC input converters each presenting a reactive load of 1.5 volt-amperes.	$ 44.00
K524	SENSOR CONVERTER	AC or DC coupled converter senses voltage transitions or resistance thresholds by noise-rejecting differential simplification.	$ 98.00
K604	ISOLATED AC SWITCH	Four 250 volt-ampere AC switches can drive a Type K Size 3 motor starter directly.	$ 82.00 ,
K644	DC DRIVER	Can drive directly devices rated up to 2.5 amperes at 48 volts.	$ 66.00
K671	DECIMAL DECODER AND NIXIE DISPLAY	Decodes and displays outputs of K210 or K220 binary-coded decimal counters.	$ 43.00
K716	INTERFACE BLOCK	Interconnection interface for K Series modules that communicates with external equipment.	$ 90.00
K731	SOURCE MODULE	Source module with 1 amp regulator supplies +5 volt DC power to operate up to 32 modules.	$ 24.00
K732	SLAVE REGULATOR	For each unit of current emitted by K731, the K732 emits two; up to three K732 slaves can be controlled by a single K731.	$ 28.00
K771	DISPLAY SUPPLY	Power and support for six K671 displays.	$ 26.00
K791	TEST PROBE	Pocket test probe with two pulse-stretching lamp drivers.	$ 27.00
K940	MOUNTING HARDWARE	Mounting foot for K941.	$ 3.00
K941	MOUNTING HARDWARE	Mounting bar for up to four H800 connector blocks.	$ 6.00

R SERIES

R001	DIODE NETWORK	Seven diodes for adding inputs to gates and flip-flops.	$ 4.00
R002	DIODE NETWORK	Five 2-input diode networks; OR for ground AND for negative signals, when connected to diode-gate node points.	$ 5.00
R107	INVERTER	Seven one-input diode gates. One inverter also has node input.	$ 24.00
R111	EXPANDABLE NAND/NOR GATE	Three 2-input diode-transistor gates. NOR's for ground and NAND's for negative inputs. Node terminal provided for additional inputs.	$ 14.00
R113	NAND/NOR GATE	Five 2-input diode transistor gates. NOR's for ground and NAND's for negative inputs.	$ 20.00

R121	NAND/NOR GATE	Four R111-type gates with loads internally connected and without nodes.	$ 17.00
R122	NOR/NAND GATE	Logical complement of R121, but somewhat slower. One ma input and 18 ma outputs like R121.	$ 26.00
R123	INPUT BUS GATE	Six two-input R111-type gates without loads or nodes. Each gate shares one input with another.	$ 19.00
R131	EXCLUSIVE OR	Four gates which perform exclusive OR function.	$ 35.00
R141	AND/NOR GATE	Seven 2-input gates. OR's NAND'ed together for ground inputs; AND's NOR'ed together for negative inputs.	$ 13.00
R151	OCTAL DECODER	One of eight outputs is grounded for each combination of states in three pairs of complementary inputs.	$ 33.00
R181	DC CARRY CHAIN	Six cascaded AND gates for counting without carry delay.	$ 35.00
R200	FLIP-FLOP	Two-transistor flip-flop is set or cleared from its own outputs or direct set and clear inputs. Operates at up to 2 megacycles.	$ 9.50
R201	FLIP-FLOP	Flip-Flop with direct set and clear inputs and five diode capacitor-diode gates. Can be set or cleared from its outputs.	$ 22.00
R202	DUAL FLIP-FLOP	Two flip-flops, each with clear input and two diode-capacitor-diode input gates. Can be set or cleared from its outputs.	$ 25.00
R203	TRIPLE FLIP-FLOP	Three flip-flops, each with direct clear input and diode-capacitor-diode gate. Can be set or cleared from its outputs.	$ 28.00
R204	QUADRUPLE FLIP-FLOP	Four flip-flops, each with direct clear and set inputs. Two flip-flops share each direct-clear input. Can be set or cleared from its outputs.	$ 28.00
R205	DUAL FLIP-FLOP	Two flip-flops with common clear and each having three diode-capacitor-diode gates. Can be set or cleared from its outputs.	$ 29.00
R302	DELAY	Two one-shot multivibrators triggered by capacitor-diode gates. Independent delays controlled internally or externally.	$ 44.00
R303	INTEGRATING ONE SHOT	Zero recovery time multivibrator with complementary output buffers. Delays controlled externally or internally.	$ 45.00
R401	VARIABLE CLOCK		$ 45.00
**R405	CRYSTAL CLOCK	Please specify frequency	$100.00
R601	PULSE AMPLIFIER	Pulse amplifier and six capacitor-diode input gates. Driven by 40 to 100-nanosecond, positive-going pulses at up to 2 megacycles or 400-nanosecond pulses at up to 1 megacycle.	$ 25.00
R602	PULSE AMPLIFIER	Two pulse amplifiers, each with two diode-capacitor-diode gates and one ungated input. Input frequency up to 2 megacycles.	$ 22.00
R603	PULSE AMPLIFIER	Three pulse amplifiers, each with one diode-capacitor-diode gate and one ungated input. Input frequency up to 2 megacycles.	$ 28.00
R650	BUS DRIVER	Two inverting bus drivers, each with 2-input NOR or NAND diode-transistor gate. Node terminal provided for additional inputs.	$ 23.00

W SERIES

W002	CLAMPED LOAD	Fifteen 2-milliampere clamped loads.	$ 13.00
W005	CLAMPED LOAD	Fifteen 5-milliampere clamped loads.	$ 15.00
W018	CONNECTOR MODULE	For 18-line, ribbon-cable connections. For each foot of cable or fraction.	$ 18.00 $ .60
W018U	CONNECTOR MODULE	Without cable.	$ 9.00

**2mc only off-the-shelf delivery.

W021-R	CONNECTOR MODULE	For 9 direct ribbon-cable connections: For each foot of cable, or fraction:	$ 13.00 $ .60
W021-RU	CONNECTOR MODULE	Without cable.	$ 4.00
W021-C	CONNECTOR MODULE	For 9 direct co-axial connections: For each foot of cable, or fraction:	$ 31.00 $ 1.50
W021-CU	CONNECTOR MODULE	Without cable.	$ 4.50
W022-R	CONNECTOR MODULE	For 9 terminated ribbon connections: For each foot of cable, or fraction:	$ 13.50 $ .60
W022-RU	CONNECTOR MODULE	Without cable.	$ 4.50
W022-C	CONNECTOR MODULE	For 9 terminated co-ax connections: For each foot of cable, or fraction:	$ 33.00 $ 1.50
W022-CU	CONNECTOR MODULE	Without cable.	$ 6.50
W023	CONNECTOR MODULE	For 18-line, ribbon-cable connections. For each foot of cable or fraction.	$ 13.00 $ .60
W023U	CONNECTOR MODULE	Without cable.	$ 4.00
W028-R	CONNECTOR MODULE	For 9 jumperable ribbon connections: For each foot of cable, or fraction:	$ 13.00 $ .60
W028-RU	CONNECTOR MODULE	Without cable.	$ 4.00
W028-C	CONNECTOR MODULE	For 9 jumperable co-ax connections: For each foot of cable, or fraction:	$ 31.00 $ 1.50
W028-CU	CONNECTOR MODULE	Without cable.	$ 4.50
W040	SOLENOID DRIVER	Two high-current-drive amplifiers, each with a diode NOR or NAND gate. Node terminal provided for additional inputs.	$ 36.00
W042	10 AMP DRIVER	Four germanium transistor drivers which can provide up to 10 amps of DC drive.	$ 80.00
W043	SOLENOID DRIVER	Two high-current-drive amplifiers, each with a diode NOR or NAND gate. Node terminal provided for additional inputs.	$ 35.00
W050	INDICATOR DRIVER	Seven amplifiers for miniature, incandescent indicators.	$ 13.00
W051	100ma DRIVER	Seven higher-current circuits.	$ 22.00
W061	RELAY DRIVER	Four quarter-amp, 55 volt, all-silicon drivers for loads returned to positive voltage.	$ 35.00
W080	ISOLATED AC-DC SWITCH	Two floating switches controlled by light beams. Allows isolated control of line-operated devices. One-quarter amp at 125v AC or DC.	$ 60.00
W103	DEVICE SELECTOR	For PDP-8.	$ 52.00
W108	DECODING DRIVER	300-ma, bipolar drive with 8 drivers.	$ 75.00
W500	HIGH IMPEDANCE FOLLOWER	Seven fault-protected circuits, each comprising two cascaded emitter-follower amplifiers. Up to ±30v in.	$ 25.00
W501	LEVEL CONVERTER AND SCHMITT TRIGGER	Produces standard pulses from contact closures or non-standard negative logic levels. Switching thresholds can be 0 to −2.5 volts. Contact-bounce integrator included.	$ 13.00
W510	POSITIVE LEVEL CONVERTER	Three inverters with input thresholds which can be set at 0, +1v, or +2v.	$ 17.00
W511	NEGATIVE LEVEL CONVERTER	Two circuits for converting inputs between −50 volts and +25 volts to 3 volt levels. Switching point can be set to 0, −1, −2, or −3 volts.	$ 17.00
W512	POSITIVE LEVEL CONVERTER	W and A Series Interface for Positive Logic Systems.	$ 25.00

W SERIES (Cont.)

W520	COMPARATOR	An inexpensive comparator for A/D work, or a general purpose input level converter. Three circuits, each is a 4-transistor difference amplifier, DEC Standard levels at the output.	$ 43.00
W532	DUAL AMPLIFIERS	Two AC-coupled differential amplifiers.	$ 30.00
W533	DUAL RECTIFYING SLICER	Two slicers that amplifies signals from a W532 and converts them to DEC signal.	$ 30.00
W590	IBM N LINE TO DEC CONVERTER	Each of five inverting amplifiers provides inputs compatible with three types of IBM N lines.	$ 26.00
W600	NEGATIVE LEVEL AMPLIFIER	Three diode-transistor inverting amplifiers convert standard levels to outputs of ground and −1 to −15 volts. Node terminals provide for additional inputs.	$ 12.00
W601	POSITIVE LEVEL AMPLIFIER	Three diode-transistor inverting amplifiers convert standard levels to ground and 1 to 20-volt outputs. Additional gates added through node terminals.	$ 13.00
W602	BIPOLAR LEVEL AMPLIFIER	Three inverting amplifiers for output levels at +6, +3, 0, −3, or −6 volts.	$ 40.00
W603	POSITIVE LEVEL AMPLIFIER	Amplifier drives positive logic systems from FLIP CHIP systems.	$ 23.00
W607	PULSE AMPLIFIER	Three pulse amplifiers. Input: 40-nanosecond (or wider) pulses at up to 2.5 megacycles.	$ 42.00
W640	PULSE AMPLIFIER	Three standardizing amplifiers with transformer-coupled outputs of 400 nsec at up to 500 kc, or 1 μsec at up to 200 kc.	$ 42.00
W690	DEC TO IBM N LINE CONVERTER	Each of four inverting drivers provides outputs compatible with three types of IBM N lines.	$ 36.00
W700	SWITCH FILTER	Six switch filters reduce the effects of contact bounce.	$ 20.00
W705	POWER SUPPLY (+3.6v)	Supplies up to 1 amp at +3.6 volts.	$ 15.00
W706	TELETYPE RECEIVER	Integrated-circuit, serial-to-parallel Teletype code converter.	$150.00
W707	TELETYPE TRANSMITTER	Integrated-circuit, parallel-to-serial Teletype code converter.	$150.00
W708	TELETYPE INTERFACER	Provides special gating controls and clock synchronization for Teletype and data communications systems, when used with the W706 and W707.	$ 55.00
W709	COUNTER	Divide by 16/64 counter for conversion of stable crystal clock frequencies to low teletype frequencies.	$ 30.00
W800	RELAY	Two normally open reed relays for up to ⅛ amp, 200 volts with contact protection provided.	$ 45.00
W802	RELAY MULTIPLEXER	Eight double-pole, normally open relays, their drivers and a gating circuit.	$160.00
W970	BLANK BOARD	36-pins	$ 4.00
W971	BLANK BOARD	Double-height W970, 72 pins	$ 8.00
W972	CLAD BOARD	36-pins	$ 4.00
W973	CLAD BOARD	Double-height W972, 72 pins	$ 6.00
W980	MODULE EXTENDER	Allows access to circuits without breaking connections.	$ 14.00
W985	ADAPTER	Puts a System Module in four FLIP CHIP slots.	$ 34.00
W990	BLANK BOARD	18-Pins	$ 2.50
W991	BLANK BOARD	Double-height W990, 36-pins	$ 5.00
W992	CLAD BOARD	18-pins	$ 2.00
W993	CLAD BOARD	Double-height W992, 36-pins	$ 4.00
W994	PERFORATED BOARD		$ 4.50
W995	PERFORATED BOARD	A double-height W994.	$ 9.00

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A SERIES

A100 A103 A121	MULTIPLIER SWITCHES	Solid-state analog switches. Transition time: less than one microsecond; offset; 100 to 300 microvolts. Controlled by standard levels and high frequency carrier. Transformer-coupled for isolation.	$100.00 $ 78.00 $ 65.00
A111	MULTIPLEXER SWITCH	Low level relay multiplexer with guarded contact wiring. Two three-pole relays.	$ 93.00
A200	OPERATIONAL AMPLIFIER	15 volt amplifier with a 2x10⁶ open-loop voltage gain and a 15-megahertz unity gain. Differential inputs accept up to 10-volt common-mode signals.	$130.00
A400	SAMPLE AND HOLD AMPLIFIER	± 10 volt sample and hold able to track a full scale excursion in 12 microseconds to 0.25% accuracy.	$330.00
A502	COMPARATOR	Difference amplifier for signals as small as one millivolt. Standard output drives R- or B-series modules.	$110.00
A601	DIGITAL-TO- ANALOG CONVERTER	Three-bit star networks with drivers and terminating resistor.	$ 60.00
A604	DIGITAL-TO- ANALOG CONVERTER	Two-bit network with drivers for more accuracy.	$ 62.00
A605	DIGITAL-TO- ANALOG CONVERTER	Two-bit wirewound network with drivers for maximum accuracy.	$ 78.00
A606	DIGITAL-TO- ANALOG CONVERTER	Two-bit network used with A604 to form one decade of BCD D to A conversion.	$ 62.00
A608 A609	DIGITAL-ANALOG CONVERTERS	Ten-bit single buffered Digital-to-Analog converters — A609 output is bi-polar, A608 output is uni-polar.	$350.00 $375.00
A610 A611	DIGITAL-ANALOG CONVERTERS	Ten-bit double buffered Digital-to-Analog converters — A611 output is bi-polar, A610 output is uni-polar.	$400.00 $425.00
A702 A704	REFERENCE SUPPLIES	Both — 10-volt references. A702: 10-millivolt ripple, 30-millivolt load regulation. A704: 0·1-millivolt ripple, 0.1-millivolt load regulation.	$ 58.00 $184.00
A800 A801	ANALOG-DIGITAL CONVERTERS	Complete 10-bit successive approximation analog-to-digital converter; A801 has built in reference supply.	$700.00 $750.00
A990	AMPLIFIER BOARD	Predrilled etched board on which can be mounted one of several dozen types of operational amplifiers manufactured by three different companies.	$ 4.00
A992	AMPLIFIER BOARD	Similar to A990, and also receives booster amplifiers. Accepts even more different types, from many manufacturers.	$ 4.00

B SERIES

B104	INVERTER	Four 10-megacycle inverters and three clamped load resistors.	$ 17.00
B105	INVERTER	Five 10-megacycle inverters and five clamped load resistors.	$ 21.00
B113	NAND/NOR GATE	Four 2-input diode-transistor NOR or NAND gates with three clamped load resistors.	$ 23.00
B115	NAND/NOR GATE	Three 3-input diode-transistor NOR or NAND gates and three clamped load resistors.	$ 21.00
B117	NAND/NOR GATE	Two 6-input diode-transistor NOR or NAND gates.	$ 14.00
B123	INVERTER	Three 10-ma clamped loads, 4 pairs transistor inverters.	$ 31.00
B124	INVERTER	Three groups of three inverters, and three clamped load resistors. Logically complementary to B115.	$ 31.00
B130	3-BIT PARITY CIRCUIT	Two levels of gating at high speed, with complementary outputs.	$ 50.00

B155	HALF BINARY-TO-OCTAL DECODER	One output is grounded for each of four input combinations, if each of three auxiliary inputs is also enabled.	$ 25.00
B171	NAND/NOR GATE	One 12-input diode gate with two transistors. NOR and OR for ground signals; AND and NAND for negative signals.	$ 18.00
B200	FLIP-FLOP	For building simple 10 mc registers at low cost. Short delay from pulse input to flip-flop output.	$ 25.00
B201	FLIP-FLOP	General purpose flip-flop and nine input transistors.	$ 56.00
B204	QUADRUPLE FLIP-FLOP	Four flip-flops with an inverter for common clear. Can be set or cleared from their outputs.	$ 29.00
B301	DELAY	One shot multivibrator with both pulse and level outputs.	$ 73.00
B310	DELAY	Four delay lines, each with maximum delay of 50 nanoseconds in 12.5 nanosecond steps.	$ 66.00
B360	DELAY (WITH PULSE AMPLIFIER)	Adjustable delay line (250 nanoseconds, maximum) and a pulse amplifier.	$ 84.00
B401	VARIABLE CLOCK		$ 57.00
B405	CRYSTAL CLOCK	Please specify frequency	$100.00
B602	PULSE AMPLIFIER	Two pulse amplifiers for negative or positive pulses.	$ 36.00
B620	CARRY PULSE AMPLIFIER	Two stages for long B201 counters.	$ 47.00
B681	POWER INVERTER	Four inverters each equivalent to two paralleled B105-type inverters. Includes a 20 ma clamped load internally connected to each collector, and four separate 10 ma loads.	$ 25.00
B684	BUS DRIVER	Two 40 ma drivers for direct or terminated connection.	$ 52.00

HARDWARE ACCESSORIES

CAB-1	CABINET	Includes End Panels Additional Cabinets	$ 700.00† $ 500.00†
CAB-2	CABINET	Includes End Panels Additional Cabinets	$ 700.00† $ 500.00†
CAB-3	CABINETS	Expander cabinet for PDP-8.	$ 650.00†
CAB-6	CABINET	Includes End Panels Additional Cabinets	$ 800.00† $ 600.00†
CAB-8A	CABINETS	Free standing with winged table.	$1,100.00†
CAB-8B	CABINETS	Free standing with rectangular table.	$1,100.00
H001	BRACKETS	One pair brackets to mount a 1907 cover plate on a 19″ mounting panel. Provides ¾ inch standoff, cover plate flush with cabinet.	$ 8.00
H002	BRACKETS	One pair brackets to mount a 1907 cover plate on a 19 inch mounting panel. Provides 2 inch setback to leave room for lights, controls.	$ 8.00
H201	CORE MEMORY	4096 x 13 bit core memory (90 day guarantee)	$2,000.00
H701 H701A	POWER SUPPLIES	Small, chassis mounted supplies electrically similar to 782A.	$ 116.00 $ 136.00
H704	POWER SUPPLY	Will drive six operational amplifier modules. All silicon, regulated, floating supply providing ±15 volts at up to 400 ma on both outputs.	$ 200.00†
H710	POWER SUPPLY	Regulated, floating output 5-volt power supply with provisions for remote sensing.	$200.00
H800F H800W	CONNECTOR BLOCKS	Unmounted 144 pin connectors for 8 FLIP CHIP modules.	$ 8.00 $ 8.00
H801F H801W	CONNECTOR PINS	Set of 18 spare pins to fit FLIP CHIP sockets.	$ 4.00 $ 4.00
H802	CONNECTOR BLOCK	For single FLIP CHIP modules.	$ 4.00

†Non-discountable

H803	MODULE SOCKETS	Unmounted 288 pin connectors for 8-36 pin modules.	$	13.00
H805	CONNECTOR PINS	Set of 18 spare pins to fit H803 and H804 connectors.	$	4.00
H810 (24)	PISTOL GRIP HAND WIRE WRAPPING TOOL	For wrapping #24 solid wire on DEC Type H800-W Connector Pins.	$	99.00†
H810 (30)	PISTOL GRIP HAND WIRE WRAPPING TOOL	For wrapping #30 solid wire on DEC Type H800-W Connector Pins.	$	99.00
H810 (24 & 30)	PISTOL GRIP HAND WIRE WRAPPING TOOL	For wrapping #24 and 30 wire on DEC type H800W and H803 Connector Pins.	$	150.00†
H811 (24)	HAND WRAPPING TOOL	For wrapping #24 wire on Connector Pins in service or repair applications.	$	21.50†
H811A (30)	HAND WRAPPING TOOL	For wrapping #30 wire on Connector Pins in service or repair applications.	$	21.50†
H812 (24)	HAND UNWRAPPING TOOL	For removing #24 wire wrapped connections.	$	10.50†
H812A (30)	HAND UNWRAPPING TOOL	For removing #30 wire wrapped connections.	$	10.50†
H813 H813A	BITS	H813 is a #24 bit; H813A is a #30 bit.	$ $	30.00 30.00
H814 H814A	SLEEVES	H814 is a #24 sleeve; H814A is a #30 sleeve.	$ $	21.00 21.00
H820 H821	GRIP CLIPS	**Identical to slip-on connectors used on Type 913 and 915 patchcords. Shipped in packages of 1000.**	$ $	**47.80†** **75.00†**
H825 H826	HAND CRIMPING TOOL	For crimping Type H820 Grip Clips. Insures a good electrical connection.	$ $	146.70† 210.00†
H830	STACK-ON RIVETING TOOL		$	10.00
H900 H900A	MOUNTING PANELS WITH POWER	For up to 32 modules. Power supplies electrically similar to 782, 782A. **P option $5.00 add'l.**	$ $	180.00 200.00
H901	MOUNTING PANEL	For patching up to 10 modules.	$	82.50
H902	SWITCH AND INDICATOR PANEL	5-in. panel for experimental use. Eight switches, eight indicator lamps with ground-enabled drivers, four rheostats for controlling clocks and delays. Complements H901 and 700D. Complete with indicator driver module.	$	112.80
H903	ANALOG-DIGITAL PANEL	D-A converter and comparator (including module).	$	143.00
H910		36-pin equivalent of H900.	$	280.00
H911B H911BP H911M H911MP	MOUNTING PANEL MOUNTING PANEL MOUNTING PANEL MOUNTING PANEL	Similar to the 1943 but uses H803 and H804 connectors. Following options available as indicated by the suffix letters: Marginal Check Switches (M) or terminal block (B), prewired power (P) or not.	$ $ $ $	151.00 161.00 172.00 182.00
H920	MODULE DRAWER	Can house up to 16 mounting blocks in addition to power supplies; can be slide mounted.		**$170.00**
H921	FRONT PANEL	Front panel for H920 provides mounting arrangements for switches, indicators and other accessories.	$	5.00
H923	CHASSIS SLIDES	Allow H920 to be slide mounted.	$	75.00
700D	POWER SUPPLY WITH DIAL	5-in. panel for powering and pulsing experimental logic systems patched together on H901 panels. Contains a variable clock, three pulsers, with a telephone dial and three push-buttons for driving the pulsers. Designed especially for educational use.	$	288.00
700DA		50-cycle version of 700D.	$	308.00
728 728A	POWER SUPPLIES	+10 v @ 0.7 amp, −15 v @ 1.8 amp, for 17" DEC cabinet plenum-door mounting.	$ $	240.00 260.00

†Non-discountable

782 782A	POWER SUPPLIES	Rack-mounted power supplies with regulated +10 and −15 volt output at up to 0.4 and 3 amperes, respectively. Input: 782: 115 volts, 60 cycles. 782A: 112.5 to 235 volts, 50 cycles.	$ 128.00 $ 148.00
783 783A	POWER SUPPLIES	Rack-mounted power supplies with electrical characteristics similar to 728 and 728A.	$ 240.00 $ 260.00
786 786A	VARIABLE POWER SUPPLIES	Standard rack mounting 0-24 volt variable supplies, 0-2.5 amp.	$ 215.00 $ 235.00
831	POWER CONTROL	Specify 4, 10, 20, or 30 amp circuit-breaker.	$ 51.00
900	CONTROL PANEL	A front panel and chassis exactly duplicating 700D but without power. For multi-student installations on a Logic Laboratory.	$ 214.25
911	BANANA PATCHCORDS	Ten each 2, 4, 8, 16, 32, or 64 inches. One box.	$ 9.00
913	WIRE WRAP PATCHCORDS	Hundred each 2, 4, 8, 16, 32 or 64 inches. One pkg.	$ 18.00
915			**$ 33.00**
914-7	POWER JUMPERS	Ten each 7 inches long. One pkg.	$ 4.00
914-19	POWER JUMPERS	Ten each 19 inches long. One pkg.	$ 4.00
932	BUSSING STRIP		$ .60
933			**$ 1.00**
1907	MOUNTING PANEL COVER	5¼ by 19 inch cover plate to protect power and logic wiring and permit installation of lights and control switches on a 19 inch mounting panel. Use with one pair of brackets, H001 or H002 (order separately).	$ 9.00
1943-F-B 1943-W-B 1943-F-B-P 1943-W-B-P 1943-F-M 1943-W-M 1943-F-M-P 1943-W-M-P	MOUNTING PANEL	Houses 64 modules in a standard 19-inch rack. Following options available as indicated by the suffix letters: Forked-pin solder (F) or wire-wrap (W) connectors; marginal-check switches (M) or terminal block (B); prewired power (P) or not.	$ 111.00 $ 111.00 $ 121.00 $ 121.00 $ 132.00 $ 132.00 $ 142.00 $ 142.00
1945-19	HOLD DOWN BAR	For 1943 mounting panel (19-inch).	$ 15.00
4906	SINGLE INDICATOR	With amplifier.	$ 9.50
4908	SINGLE INDICATOR	Lamp and mounting hardware.	$ 3.00
4912	ADAPTER	Puts a FLIP CHIP module in 2 system module slots.	$ 28.00
4913	MOUNTING RACK	For a power supply and four 5½″ panels.	$ 10.00
4917	INDICATORS	9 bit indicators with amplifiers.	$ 73.00
4918	INDICATORS	18 bit indicator with amplifiers.	$ 96.00

OCTAIDS and PANELAIDS⌃

D001A	D-A CONVERTER	8 Bits	$ 376.50
D001B	D-A CONVERTER	9 Bits	$ 438.50
D001C	D-A CONVERTER	10 Bits	$ 438.50
D001D	D-A CONVERTER	11 Bits	$ 500.50
D001E	D-A CONVERTER	12 Bits	$ 518.50
D001F	D-A CONVERTER	13 Bits	$ 596.50
D002	BCD UP-COUNTER	Single Decade · Quad Decade	$ 62.50 **$ 212.50**
D004	BI-DIRECTIONAL DECADE COUNTER	Decoding Option Conversion Option	$ 124.40 $ 47.00 $ 17.00
D006	OUTPUT BUFFER INTERFACE	For PDP-8/S	$ 215.50

D007	DUAL SHIFT REGISTER	8 Bits	$ 249.00
		Single Register	$ 133.00
D008	DUAL UP-COUNTER	8 Bits	$ 217.00
		Single Up-Counter	$ 117.00
C001	A-D CONVERTER	10 Bits, 60 Hertz	$1,139.00
C001A	A-D CONVERTER	10 Bits, 50 Hertz	$1,159.00
C002	A-D CONVERTER	10 Bits, without AC power.	$1,080.00
C003	BCD REAL TIME CLOCK	50/60 Hertz	$ 639.00
C006	I/O BUFFER REGISTER	For PDP-8 or PDP-8/S	$ 397.00
C007	PDP-8/S INPUT INTERFACE	Provides cable sockets, device selection pulses, data input gates and chip facilities to interface two twelve-bit words to the PDP-8/S.	$279.00
C009	MEMORY TIMING AND CONTROL	Provides the necessary timing and control functions for memory systems using the type H201 core memory.	$285.00

△See Printed Circuit Board Price List on Page 355.

All shipments are F.O.B. Maynard, Massachusetts, and prices do not include state or local taxes.
Prices and specifications are subject to change without notice.
QUANTITY DISCOUNTS
$5,000 — 3%; $10,000 — 5%; $20,000 — 10%; $40,000 — 15%;
$70,000 — 18%; $100,000 — 20%; $250,000 — 22%; $500,000 — 25%
Discounts apply to any combination of FLIP CHIP Modules , Cabinets are not discountable.

WARRANTY

WARRANTY-1. B, R, W, MODULES — All B, R, W modules shown in Catalog C-105, as revised from time to time, are warranted against defects in workmanship and material under normal use and service for a period of ten years from date of shipment. DEC will repair or replace any B, R, W modules found to be defective in workmanship or material within ten years of shipment for a $5.00 per unit handling charge. Handling charges will be applicable from one year after delivery.

WARRANTY-2. SYSTEM MODULES, LABORATORY MODULES, HIGH CURRENT PULSE EQUIPMENT, A, G, K, M, S, NON-CATALOG FLIP-CHIP MODULES AND ACCESSORIES — All items referenced are warranted against defects in workmanship and material under normal use and service for a period of one year from date of shipment. DEC will repair or replace any of the above items found to be defective in workmanship or material within one year of shipment. Handling charges will be applicable from one year after delivery with handling charges varying depending on the complexity of the circuit.

The Module Warranty outside the continental U.S.A. is limited to repair of the module and excludes shipping, customer's clearance or any other charges.

Modules must be returned prepaid to DEC. Transportation charges covering the return of the repaired modules shall be paid by DEC. DEC will select the carrier, but by so doing will not thereby assume any liability in connection with the shipment nor shall the carrier be in any way construed to be the agent of DEC. Please ship all units to:

> **Digital Equipment Corporation**
> **Module Marketing Services**
> **Repair Division**
> **146 Main Street**
> **Maynard, Mass. 01754**

No module will be accepted for credit or exchange without the prior written approval of DEC, plus proper Return Authorization Number (RA#).

PERHAPS YOU HAVE A FRIEND WHO WOULD LIKE TO

RECEIVE A FREE COPY OF THE 1968

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COMPUTER HANDBOOK, OR THE NEW

INDUSTRIAL CONTROL HANDBOOK.

IF SO, PLEASE FILL OUT THE CARD BELOW.

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Maynard, Mass. 01754

GENTLEMEN:

Please send a free copy of: ☐ Digital Logic Handbook
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FOR MORE MODULE INFORMATION

INFORMATION REQUEST

☐ Please add my name to your mailing list

☐ Please send technical literature on the following DIGITAL products:

    ☐ PDP-8   ☐ PDP-8/S   ☐ PDP-8/I   ☐ LINC-8   ☐ PDP-9   ☐ PDP-10

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NOTES

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146 Main Street, Maynard, Massachusetts 01754
Telephone: From Metropolitan Boston: 646-8600
Elsewhere: (617)-897-8821
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Telephone: (713)-523-2529   TWX: 910-881-1651

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DENVER OFFICE:
Suite 406 — 5200 South Quebec Way, Englewood, Col. 80110
Telephone: (303)-771-1180   TWX: 910-935-0711

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CANADA
Digital Equipment of Canada, Ltd.
150 Rosamond Street, Carelton Place, Ontario, Canada
Telephone: (613)-257-2615   TWX: 610-561-165

Digital Equipment of Canada, Ltd.
39 Dundas Road East, Cooksville, Ontario, Canada
Telephone: (416)-279-1690   TWX: 610-492-4381

Digital Equipment of Canada, Ltd.
640 Cathcart Street, Suite 205, Montreal, Quebec, Canada
Telephones (514)-861-5018, (514)-861-5179

GERMANY
Digital Equipment GmbH
5 Koeln, Neue Weyerstr. 10, West Germany
Telephone 23 55 01   Telegram Flip Chip Koeln

Digital Equipment GmbH
8 Muenchen, 2 Theresienstr. 29, West Germany
Telephone: 28 30 53   Telex: 841-24226

ENGLAND
Digital Equipment Corporation (U.K.) Ltd.
Arkwright Road, Reading, Berkshire, England
Telephone: Reading 85131   Telex: 851-84327

Digital Equipment Corporation (U.K.) Ltd.
13/15 Upper Precinct
Bolton Road, Walkden, Worsley, Manchester, England
Telephone: (061) 790 2274

FRANCE
Equipement Digital
22, rue du Champ de l'Alouette, Paris 13e, France
Telephone: 336-0384   Telex: 842-26705

SWEDEN
Digital Equipment Aktiebolag
Vretenvagen 2, Solna 1, Stockholm, Sweden
Telephone: 98 13 90
Telex: Digital Stockholm 17050
Cable: Digital Stockholm

AUSTRALIA
Digital Equipment Australia Pty. Ltd.
89 Berry Street
North Sydney, New South Wales 2060, Australia
Telephone: 92-0919   Telex: 790AA-20740

Cable: Digital, Sydney
Digital Equipment Australia Pty. Ltd.
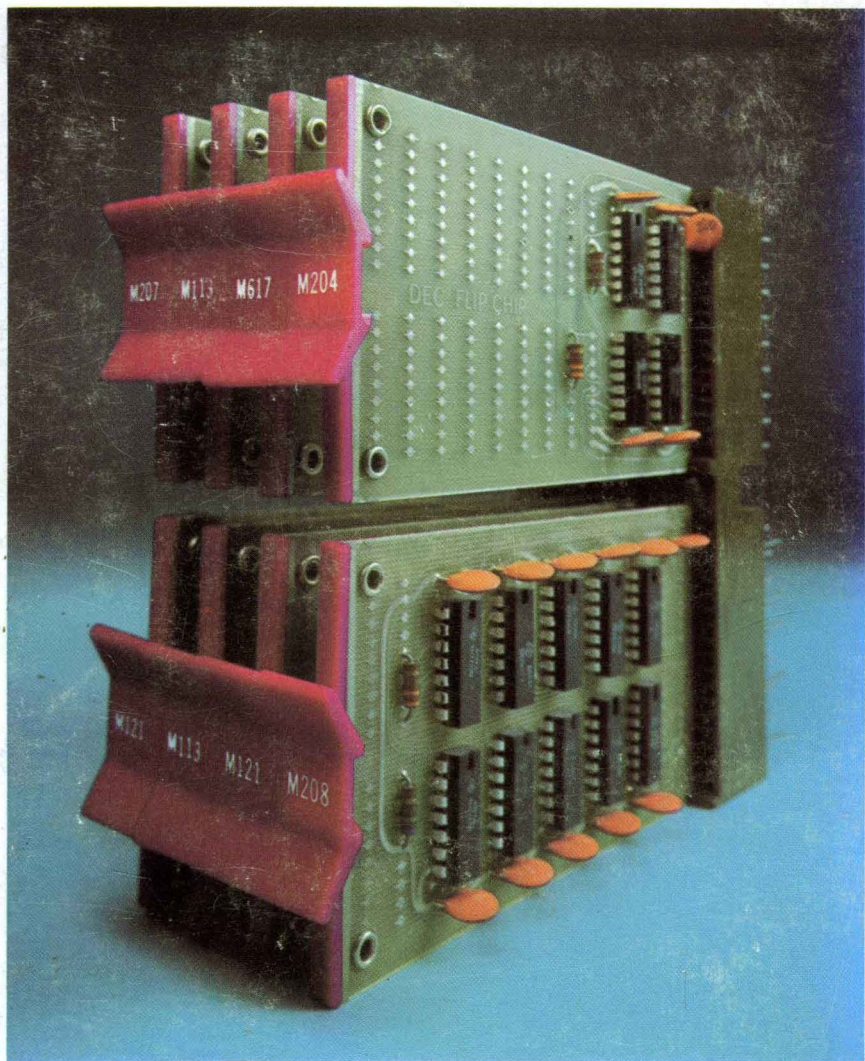69 Outram Street
West Perth 6005, Western Australia
Telephone: 214-993   Telex: 790 921 40

JAPAN
Rikei Trading Co., Ltd.
Kozato-Kaikan Bldg.
No 18-14, Nishishimbashi 1-chome
Minato-Ku, Tokyo, Japan
Telephone: 5915246   Telex: 7814208

This edition of the Logic Handbook features DIGITAL's two newest logic module lines: M Series and K Series. The M Series modules (shown above) contain high speed integrated circuit TTL logic and provide the best cost/performance ratio in the industry. K Series modules, specifically designed for industrial control applications, feature high noise immunity, ease of design and installation, and hardware compatible with standard NEMA enclosures.