RM02/03 Adapter Technical Description Manual

digital

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RM02/03 Adapter
Technical Description Manual

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PREFACE

The *RM02/03 Adapter Technical Description Manual* is designed to provide a detailed description of the adapter portion of the RM02/03 Disk Drive Subsystem. It is contained in the same cabinet as the vendor-built RM02 or RM03 drive and provides an interface to the Massbus.

The first three chapters of this book give the reader information on the drive subsystem as a prerequisite to understanding the adapter. Chapter 1 contains some general information on the subsystem including specifications, options, and typical system configurations as well as a description of the RM03P disk pack and data formatting on the pack. Chapter 2 describes the susbsystem on an interface level, describing the cables that connect the adapter to the controller (the Massbus) and the adapter to the drive itself. Chapter 3 contains information relevant to programming a system containing an RM02 or RM03 drive, such as a description of the 16 command operations the drive can execute and a summary of the registers in the drive subsystem and associated controller. Chapter 3 also describes the available diagnostics, error correcting code (ECC), and dual-port operation of the drive subsystem.

The technical description of the adapter itself is contained in Chapter 4. There are several block diagrams to illustrate the operation of various circuit elements, and the manual uses flowcharts to enhance the detailed descriptions of command exections. The information in Chapter 4 was designed to be used in conjunction with the *RM02/03 Field Maintenance Print Set,* and the chapter makes frequent reference to specific pages of the print set.

Paragraph 1.4 contains a list of other documentation relevant to the RM02/03 Disk Drive Subsystem.

CHAPTER 1
INTRODUCTION

1.1 GENERAL

This chapter contains the information necessary to familiarize maintenance personnel with the RM02 or the RM03 Disk Drive Subsystem. The chapter is divided into three major subsections that contain general information, system descriptions, and performance specifications.

1.1.1 Description

The RM02 or RM03 Disk Drive (Figure 1-1) is an 80M byte (unformatted; 67M byte formatted) random-access, mass storage device. The RM02 or RM03 is housed in a free-standing cabinet and is compatible with the following disk drive controllers: RH10, RH20, RH70, and, in specific instances, the RH11. Either a 16-bit data word or 18-bit data word format can be utilized, allowing the RM02 or RM03 to be configured in DECsystem-10, PDP-11, or DECSYSTEM-20 computer based systems. In the 16-bit format, the maximum storage capacity is 33,710,080 data words per disk pack and 31,603,200 data words per pack in the 18-bit format. The transfer rate is 1.65 μs per word for a 16-bit word or 1.86 μs for an 18-bit word. The platters in the RM03P pack spin at 3600 rev/min in an RM03, and at 2400 rev/min in an RM02.

A type 9877 removable disk pack is used with the RM02 or RM03. This 85.5 cm (14 in) diameter pack has five platters; the top and bottom platters are non-functional and only provide protection for the three inner disks. These three disks have six surfaces which are divided into five data storage surfaces and one servo track surface. This pack is interchangeable between an RM03 and an RM03 drive.

All RM02s or RM03s have error detection and error isolation operations performed on all information (data and header) read from the disk. This feature permits the software to correct detected errors and recover this data which would normally be incorrect.

The RM02 and RM03 also have the ability to accept offset commands that cause the heads to move off the track centerline in a program-controlled attempt to recover data that is not normally recoverable. The offset distance is 200 microinches on either side of the track centerline.

Data is recorded on the disk in fixed-number sector blocks, depending on the word length used. There are always 30 sectors per track for 18-bit formats and 32 sectors for 16-bit formats. Each sector contains unique cylinder, sector, and track information encoded in a header block. This block also has provisions for accepting manufacturer- or user-specified codes to indicate that the sector is unacceptable for data storage.

The RM02 and RM03 incorporate a unique integrated backplane that permits dual-port, matched-impedance Massbus connections to be made directly onto the backplane, thus eliminating requirements for multiple internal flat cables for the interface. This integrated backplane also simplifies the interconnections of Massbus cables, since up to eight RM02s or RM03s can be "daisy-chained" from a controller.

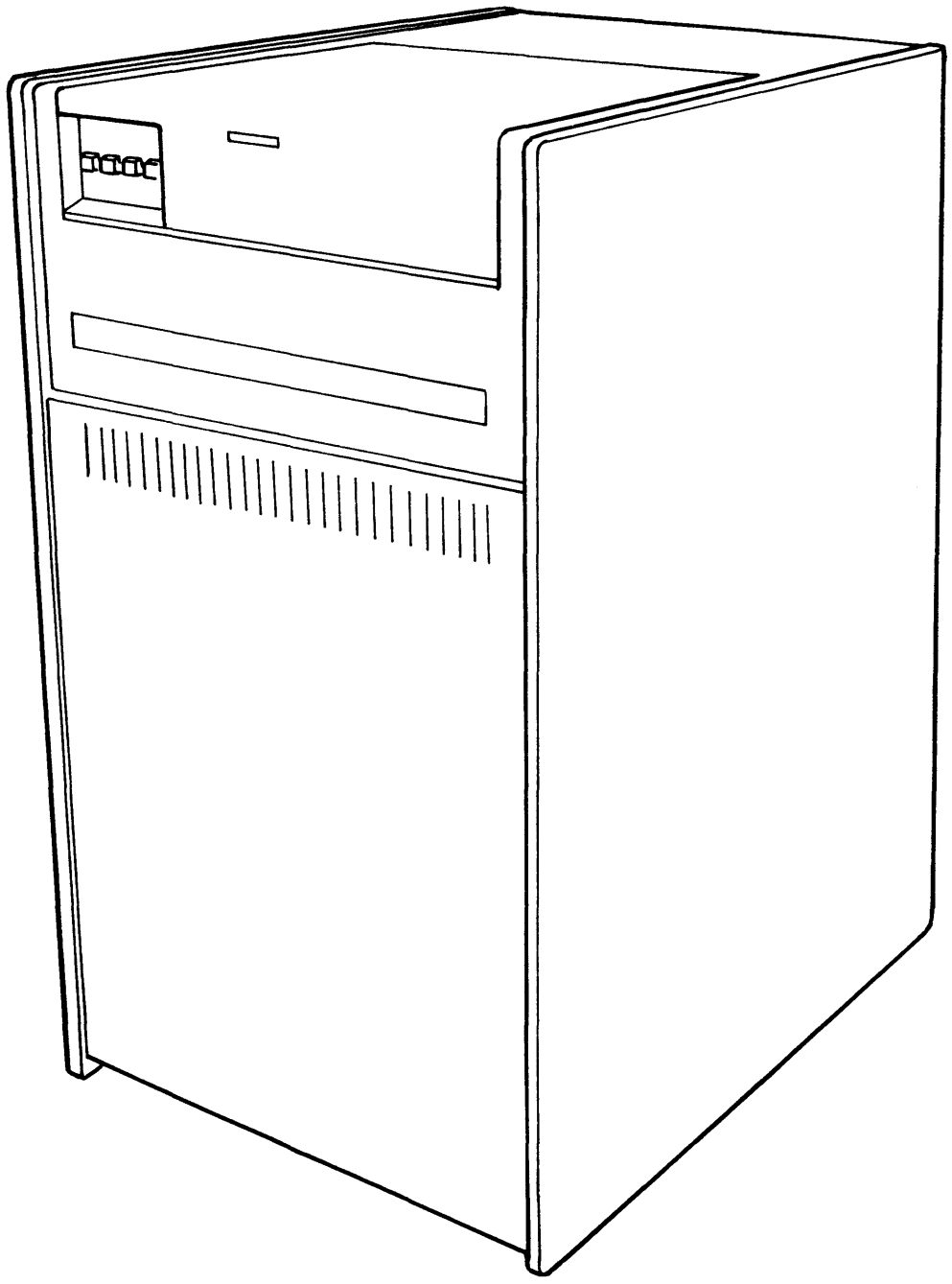

Figure 1-1 RM02/03 Disk Drive

Extensive diagnostic programs are available for maintenance procedures. An off-line tester (the TB3A2 field test unit) is also available that is used to isolate drive-associated faults.

Recording on the disk is by the three-frequency or modified frequency modulation (MFM) method, commonly referred to as the Miller Encoded Recording Technique.

1.1.2 Options

The option designations for the RM02 or RM03 are listed in Table 1-1.

NOTE

A single-port RM02 or RM03 is field upgradable to dual-port capabilities.

1.2 TYPICAL CONFIGURATIONS

Two typical system configurations incorporating RM02s or RM03s are shown in Figures 1-2 and 1-3. In the most basic configuration, the controller provides the interface between the computer bus from the central processor and the Massbus that connects to the RM02 or RM03. If the control processor is a DECsystem-10, DECSYSTEM-20, or PDP-11, the controller must be the appropriate Massbus controller (RH10, RH20, RH70, or RH11) to interface this processor to the RM02 or RM03.

Figure 1-2 depicts the RM02 or RM03 in the maximum multidrive configuration. Here, up to eight drives are serviced by a single controller.

The optional dual-port RM02 or RM03 configuration is shown in Figure 1-3. In this configuration, two processors can access up to eight drives. Each RM02 or RM03 contains additional transceiver modules permitting another Massbus connection. The RM02s or RM03s also have the arbitration logic required to switch from one port to the other. These RM02s or RM03s can be locked on port A, locked on port B, or in the programmable state.

The processors shown in Figure 1-3 can operate on the same or different word length format (16 bits/word for PDP-11, 18 bits/word for DECsystem-10 and DECSYSTEM-20) as long as there is no attempt to mix these unique formats on the same track.

1.3 DATA FORMATTING

1.3.1 Pack Format

Each disk pack is divided into individually addressable locations as shown in Figure 1-4. The five read/write data surfaces (designated 0 through 4) are sectioned into 823 (0 through 822) concentric rings called cylinders. These cylinders consist of fixed-length sectors (consecutively numbered 0 to 29 for formats using 18 bits per word or numbered 0 to 31 for formats using 16 bits per word).

Each sector is divided into two information fields with gaps or spaces between these fields. The header field contains address information and the data field stores the 256 data words. The gaps between these fields permit the following actions.

1. Compensation for drive mechanical tolerances
2. Compensation for a decision or command change
3. Compensation for head switching from write to read or vice versa
4. Synchronization of the VFO (variable frequency oscillator)

The RM02 or RM03 generates the sector gaps, and the controller supplies the header and data information during a pack-formatting operation.

Table 1-1 RM02 or RM03 Option Designations

Single-Port Options	
Option Number	**Line Voltage/Frequency**
RM02-AA or RM03-AA	120 V/60 Hz
RM02-AD or RM03-AD	240 V/50 Hz
RM03-AE	100 V/60 Hz
RM03-AF	100 V/50 Hz
Dual-Port Options	
Option Number	**Line Voltage/Frequency**
RM02-BA or RM03-BA	120 V/60 Hz
RM02-BD or RM03-BD	240 V/50 Hz
RM03-BE	100 V/60 Hz
RM03-BF	100 V/50 Hz

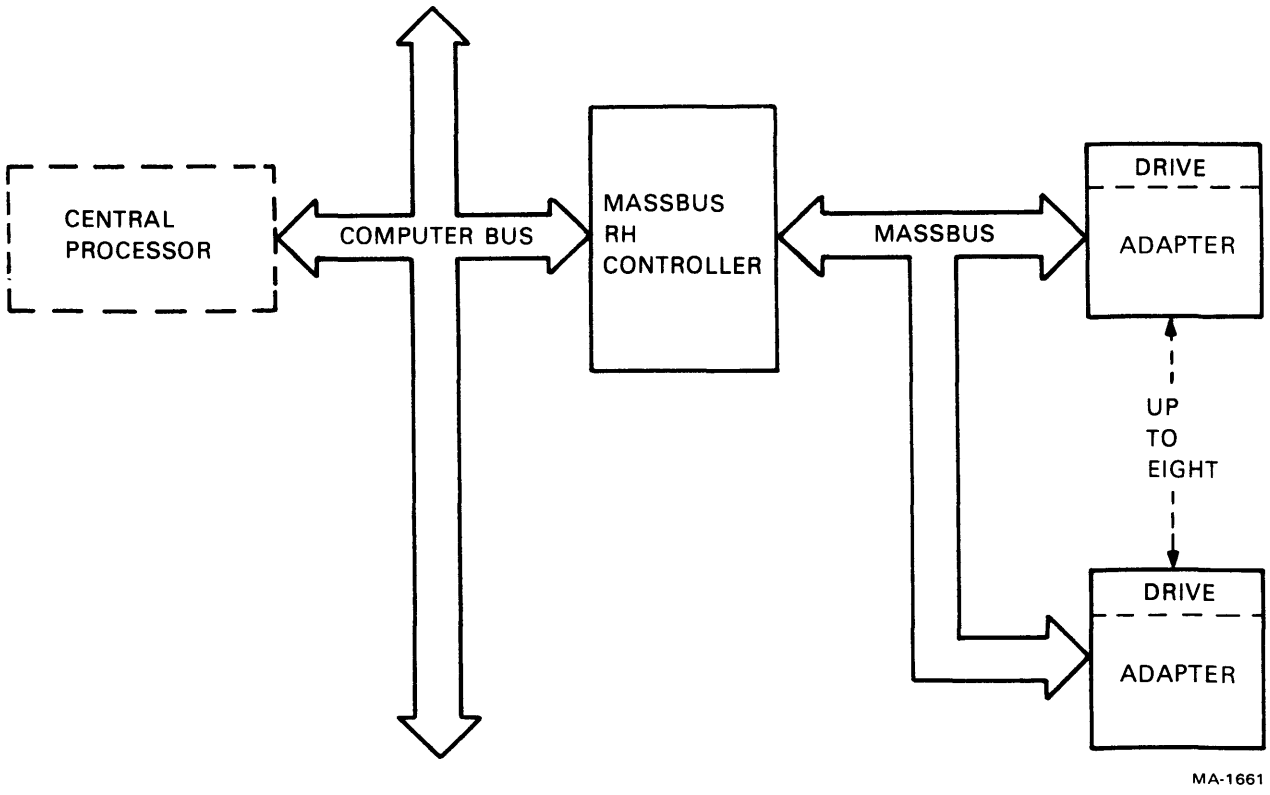

Figure 1-2 Typical 8-Drive Configuration

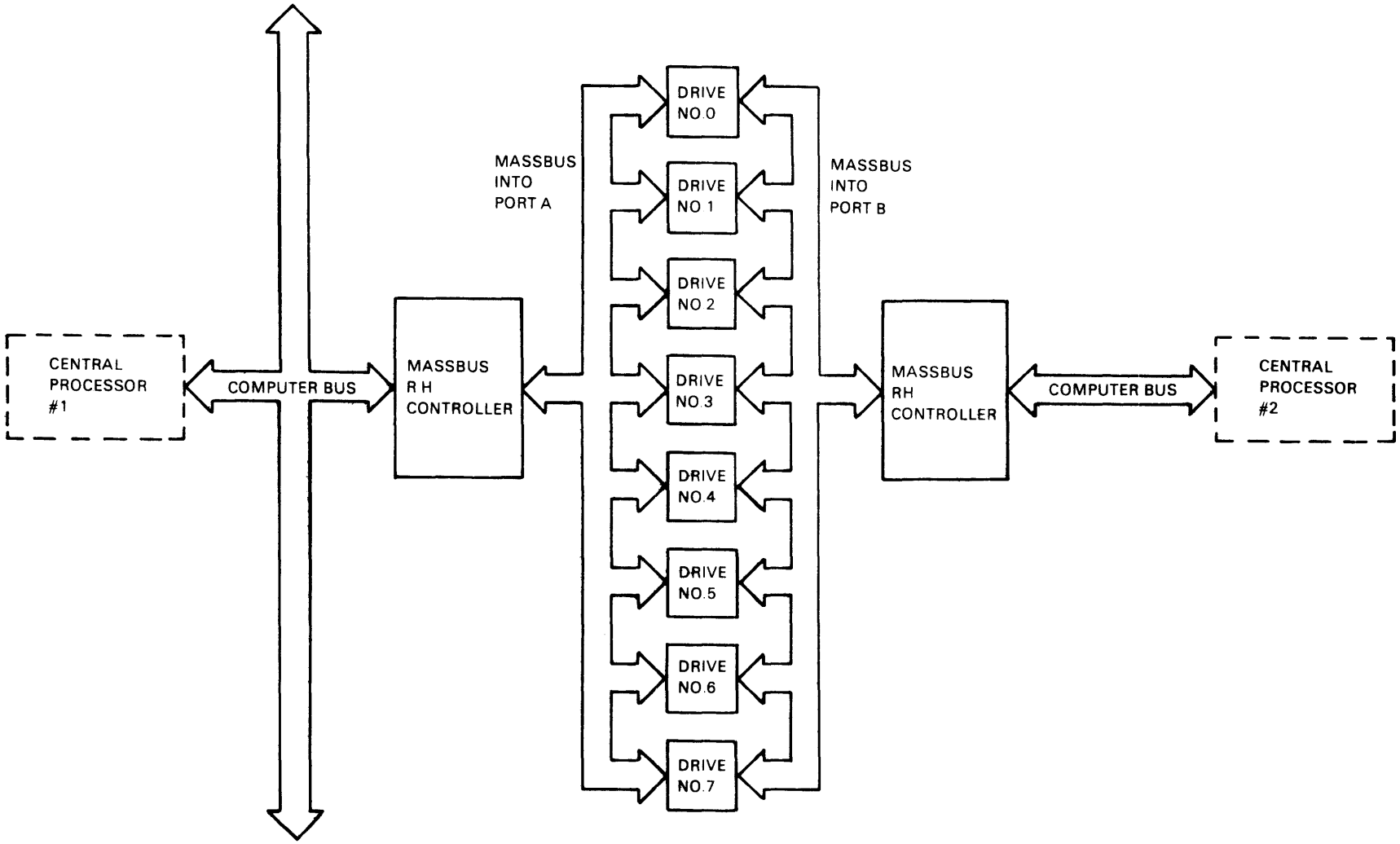

Figure 1-3 Dual-Port RM02 or RM03 Configuration

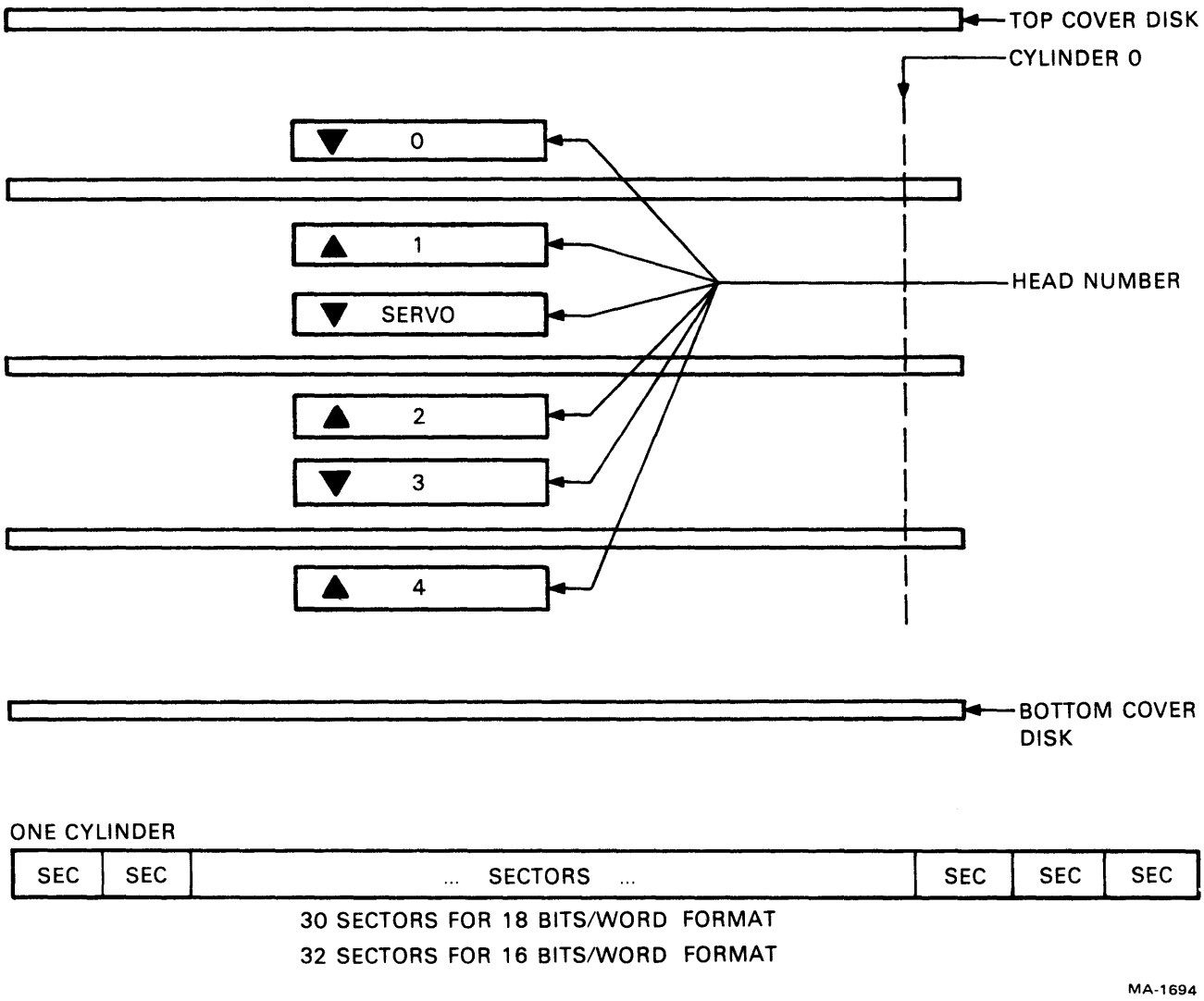

Figure 1-4 Disk Pack Format

The disk surface is prerecorded by the manufacturer with positioning signals used by the servo tracking circuits. This track is a read-only surface.

Each disk pack has a maximum formatted capacity of 663,667,200 bits. Table 1-2 shows how these bits are utilized.

1.3.2 Sector Format

The five major divisions of a sector are shown in Figure 1-5. Table 1-3 contains the overall bit/byte assignments for sectors of each data word format.

Sector Gap – This gap, which is generated by the RM02 or RM03, contains 28 bytes of 0s and 1 sync byte. The sync byte, which marks the beginning of valid information, is shown in Figure 1-6.

Table 1-2 RM02 or RM03 Pack Capacity Allocation

Data Word Format	18-Bit Format	16-Bit Format
No. of Sectors/Data Track	30 sectors	32 sectors
Bits/Sector	5,376 bits/sector	4,864 bits/sector
Total Formatted Capacity (Note 1)	663,667,200 bits/pack	640,491,520 bits/pack
Formatted Data (Note 2)	568,857,600 data bits/pack	539,361,280 data bits/pack
Total Number of Words (Note 3)	31,603,200 words/pack	33,710,080 words/pack

NOTES

1. **(Bits/sector)× (sectors/track) × (823 cylinders/pack) × (5 tracks/cylinder) = Bits/pack**
2. **(Bits/data word) × (256 words/sector) × (sectors/track) × (823 cylinders/pack) × (5 tracks/cylinder) = Formatted data word bits/pack**
3. **(Formatted data word bits/pack) ÷ (bits/word) = Words/pack**

Table 1-3 Assignment of Bits/Bytes in Sectors

	18-Bit/Word Format		16-Bits/Word Format	
Sector Location	**Bytes**	**Bits**	**Bytes**	**Bits**
Sector Gap	29	232	29	232
Header Field	6	48	6	48
Header Gap	18	144	18	144
Data Field	580	4640	516	4128
Data Gap (fixed) undefined	2 37	16 296	2 59	16 472
Total Per Sector	672	5376	630	5040

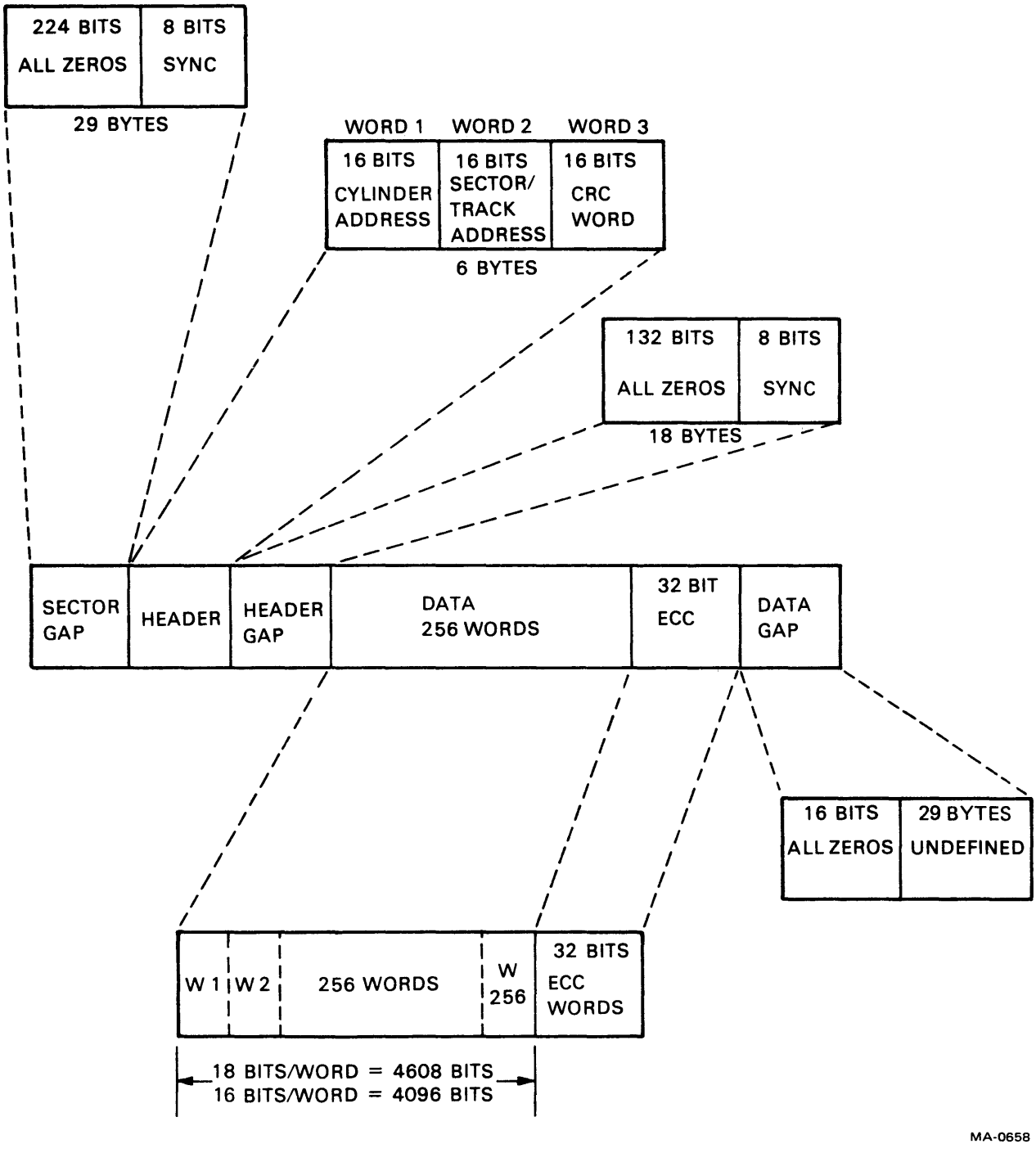

Figure 1-5 Sector Format

Header Field – The header field is divided into three words as follows.

1. Cylinder Address Word 1 – The 16 bits of this controller-generated word are shown in Figure 1-6 and described in Table 1-4.

2. Sector/Track Address Word 2 – The 16 bits of this controller-generated word are shown in Figure 1-6 and described in Table 1-5.

3. CRC Word 3 – This 16-bit word is generated by the cycle redundancy check (CRC) circuits of the RM02 or RM03. These circuits utilize the data in the first two header words to establish this CRC word. This provides a method for error detection in the reading or writing of the header data.

Table 1-4 Cylinder Address Bit Assignments

Bit	Name	Description
0–9	CYL	Ten bit locations for the address of the cylinder. Any decimal number from 0 to 822 is valid. Bit 0 is the least-significant bit.
10, 11	Unused	Always 0s.
12	FMT	The format bit that establishes whether the sector is formatted using 18-bit words or 16-bit words. When a 0, 18-bit; when a 1, 16-bit.
13	Unused	Always 0.
14	UF	The location where the user can identify this sector as being bad so that data is not recorded here. A 0 indicates a bad sector; 1, a good sector.
15	MF	The location used by the disk pack manufacturer to indicate a bad sector. A 0 indicates bad; a 1, good.

Table 1-5 Sector/Track Address Bit Assignments

Bit	Name	Description
0–4	SA	These five bits contain the address of the sector. Valid decimal numbers are 0–29 for 18-bit formats and 0–31 for 15-bit formats.
5–7	Unused	Always 0s.
8–10	TA	These three bits contain the track address. Valid numbers are: 0–4.
11–12	Unused	Reserved for future use.
13–15	Unused	Always 0s.

SYNC BYTE FORMAT

7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	1

CYLINDER ADDRESS FORMAT (FIRST HEADER WORD)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MF	UF	0	FMT	0	0	CYL 512	CYL 286	CYL 128	CYL 84	CYL 32	CYL 16	CYL 8	CYL 4	CYL 2	CYL 1

SECTOR/TRACK ADDRESS FORMAT (SECOND HEADER WORD)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	*TA 16	*TA 8	TA 4	TA 2	TA 1	0	0	0	SA 16	SA 8	SA 4	SA 2	SA 1

*RESERVED FOR FUTURE USE (ARE NORMALLY ZERO)

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Figure 1-6 Sync Byte and Header Format

Header Gap – This gap, which is generated by the RM02 or RM03, contains 17 bytes of 0s and 1 sync byte. The sync byte, which marks the beginning of valid information, is shown in Figure 1-6.

Data Field – The data field is composed of 516 bytes, 512 of which are provided by the controller and 4 of which are generated by the error correction code (ECC) circuits of the RM02 or RM03. The 512 data words are in either 18-bit or 16-bit format. The 32 bit ECC word, which is derived from the 512 data words, is considered part of the data field and is used to detect errors in the reading of the data words.

Data Gap – This gap consists of 2 0-bytes which are generated by the RM02 or RM03 and 29 bytes that are undefined.

1.4 RELATED DOCUMENTATION

Table 1-6 lists the related documentation that supplements the information in this manual.

Table 1-6 Related Documentation

Manual Title	Control Number
RM03 Disk Drive Illustrated Part Breakdown	EK-RM03-IP*
RM03 Disk Drive Technical Manual Volume I	EK-1RM03-TM*
RM03 Disk Drive Technical Manual Volume II (RM03 Print Set)	EK-2RM03-TM
RM02 Disk Drive Illustrated Parts Breakdown	EK-RM02-IP*
RM02 Disk Drive Technical Manual Volume I	EK-1RM02-TM*
RM02 Disk Drive Technical Manual Volume II (RM02 Print Set)	EK-2RM02-TM
RM02/03 Disk Subsystem User's Guide	EK-RM023-UG
RM02/03 Disk Subsystem Service Manual	EK-RM023-SV*
RM02 Field Maintenance Customer Print Set (Adapter Print Set)	MP-00456
RM03 Field Maintenance Customer Print Set (Adapter Print Set)	MP-00350

*These documents are also available on microfiche. Order as EP-XXXXX-XX.

CHAPTER 2
INTERFACE-LEVEL DESCRIPTION

2.1 SYSTEM OVERVIEW

This chapter describes the primary signal interfaces of an RM02 or an RM03 installation and discusses how both drive commands and data are routed through these interfaces. There are two major interface areas. The connection between the RM02 or RM03 and the controller is the Massbus interface and the internal connection between the adapter and the drive is the internal interface. Figure 2-1 shows these RM02 or RM03 interfaces. Figure 2-1 does not depict interfaces for either a dual-port or multidrive configuration because, while there is a considerable increase in external cabling, there is no difference in the actual Massbus signals and no difference in the internal RM02 or RM03 cabling.

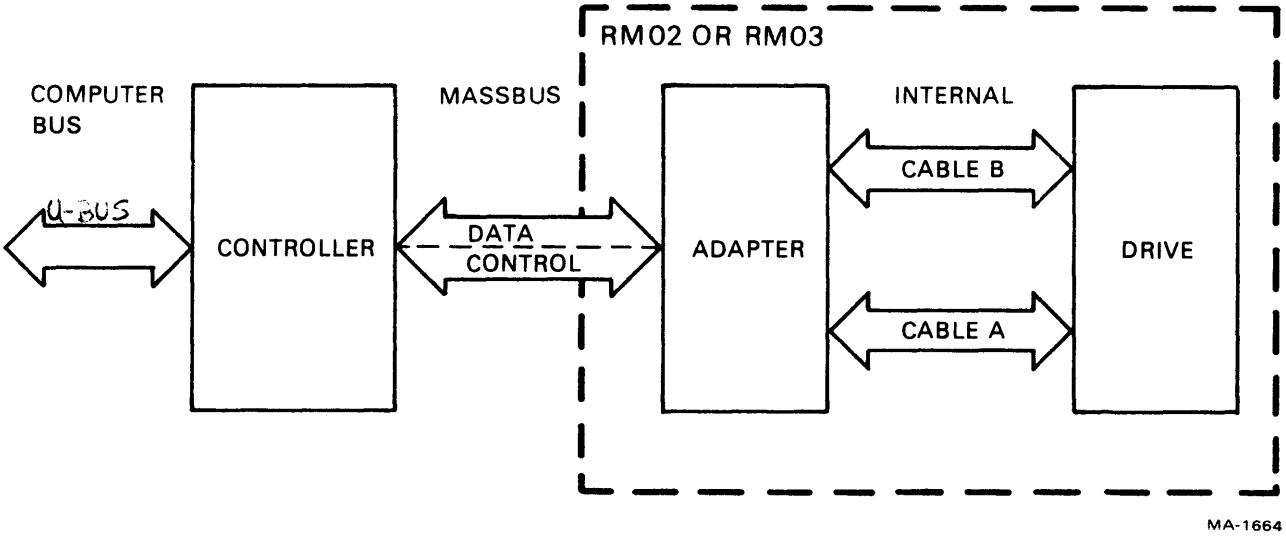


Figure 2-1 RM02 or RM03 Interfaces

2.2 PHYSICAL CABLE LOCATIONS

Figure 2-2 shows the routing of all the cables connecting the controller, adapter, and drive in the RM02 or RM03 Disk Drive Subsystem. The Massbus interface cable is described in Paragraph 2.3. The drive interface cables (cable A and cable B) are described in Paragraph 2.4, and Paragraph 2.5 contains a description of the power sequence cabling.

The steps necessary to install these cables are listed in both the *RM02/03 Disk Subsystem User's Guide* (EK-RM023-UG) and the *RM02/03 Disk Subsystem Service Manual* (EK-RM023-SV).

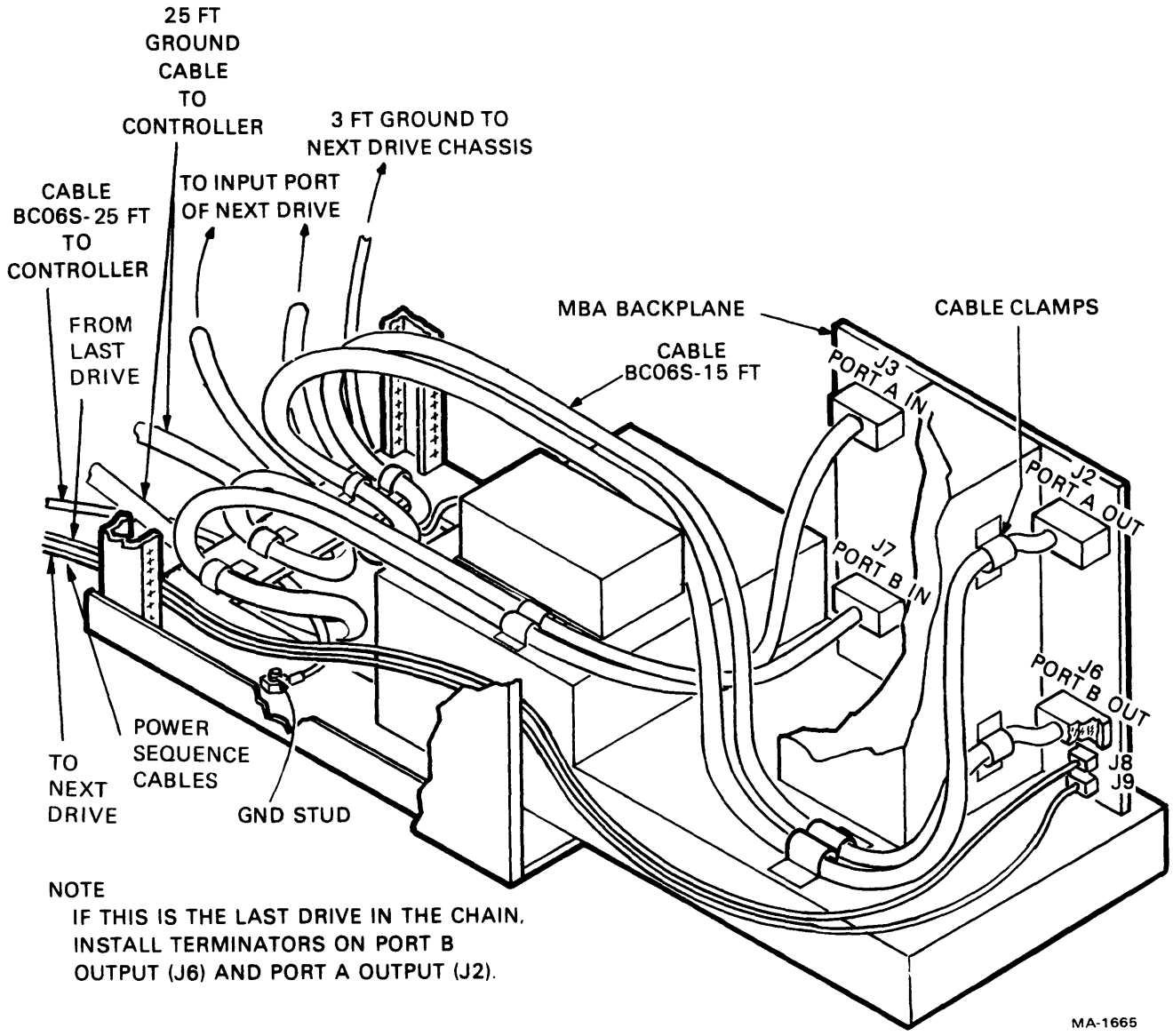


Figure 2-2 RM02 or RM03 Subsystem Cabling

2.3 MASSBUS INTERFACE

The controller-to-drive interface, or Massbus (Figure 2-3), consists of two sections: data bus lines and control bus lines.

NOTE

The RM02 and RM03 are both Massbus subsystems and operate in exactly the same manner as all other Massbus peripherals.

2.3.1 Data Lines

The data bus section of the Massbus consists of a 19-bit (18 data bits plus parity bit) parallel data path and 6 control lines (Figure 2-3). The data bus lines are described in the following six paragraphs.

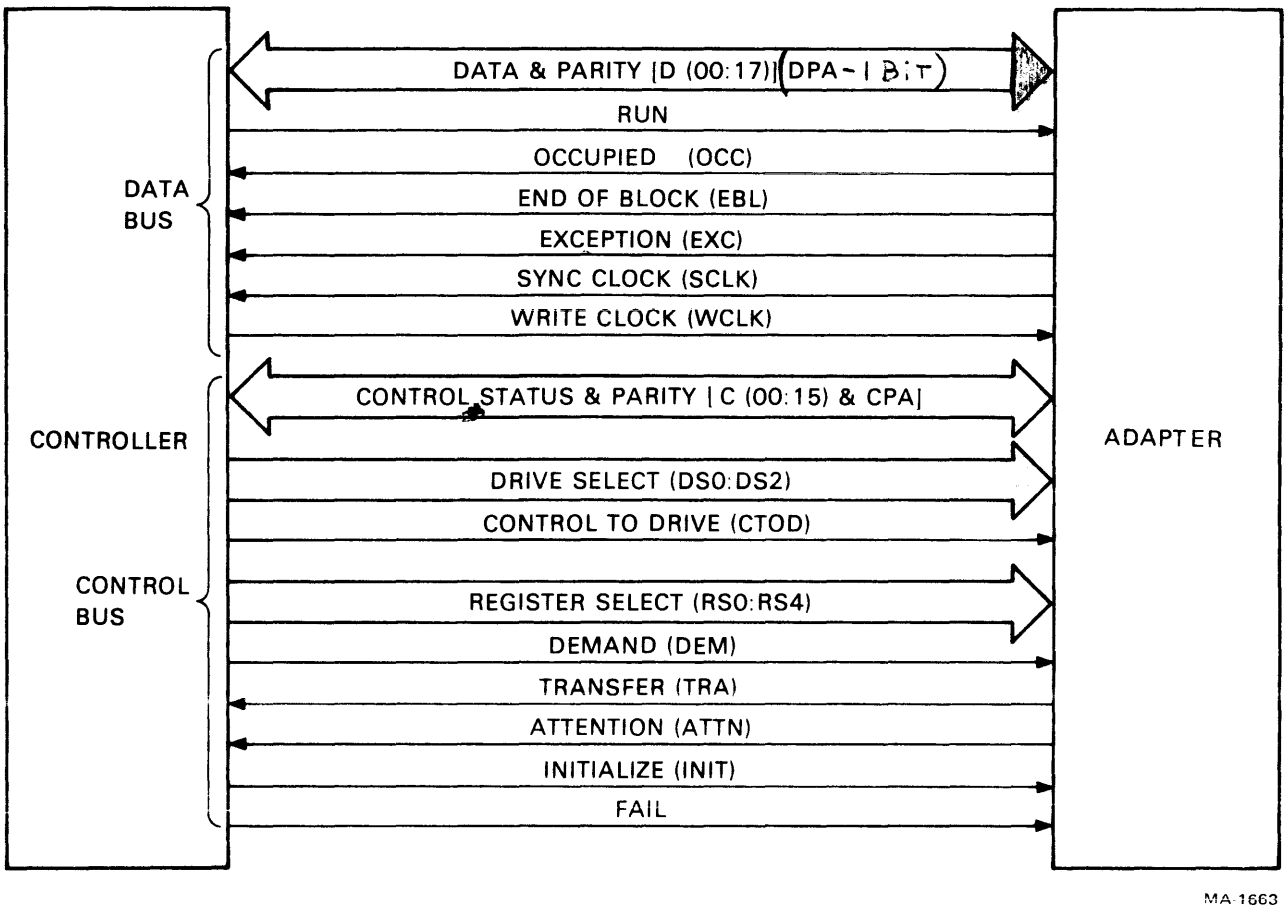


Figure 2-3 Massbus Interface Lines

Parallel Data Path – The parallel data path consists of an 18-bit data path designated D00 through D17 and an associated parity bit (DPA). The data path is bidirectional and employs odd parity. Data is transmitted synchronously, using a clock generated in the adapter.

RUN – After a transfer command has been written into the control register of the RM02 or RM03, the RM02 or RM03 connects to the data bus. The controller asserts the RUN line to initiate the function. At the end of each sector, on the trailing edge of the EBL (end of block) pulse, RUN is strobed by the RM02 or RM03. If it is still asserted, the function continues for the next sector; if it is negated, the function is terminated.

Occupied (OCC) – This signal is generated by the drive to indicate "data bus busy." As soon as a valid data transfer command is written into a RM02 or RM03, and the RUN line is asserted, the drive asserts OCC. Various errors may prevent an RM02 or an RM03 from executing a command. The controller times out in these cases due to no assertion of OCC or of SCLK (sync clock), and the MXF (missed transfer) error will be set in the controller. OCC is negated at the trailing edge of the last EBL pulse of a transfer.

End of Block (EBL) – This signal is asserted by the RM02 or RM03 for 2 μs at the end of each sector (after the last SCLK pulse). For certain error conditions where it is necessary to terminate operations immediately, EBL is asserted prior to the normal time for the last SCLK. In this case, the data transfer is terminated prior to the end of the sector.

Exception (EXC) – This signal is asserted by the RM02 or RM03 when an abnormal condition occurs in the RM02 or RM03 during a data transfer. The RM02 or RM03 asserts this signal to indicate an error during a data transfer command (read, write, or write-check). EXC is asserted at or prior to assertion of EBL and is negated at the negation of EBL.

Sync Clock (SCLK), Write Clock (WCLK) – These signals are the timing signals used to control the strobing of the data in the controller and/or in the RM02 or RM03. During a read operation, the controller strobes the data lines on the negation of SCLK and the RM02 or RM03 changes the data on the assertion of SCLK. During a write operation, the controller receives SCLK and echos it back to the RM02 or RM03 as WCLK. On the assertion of WCLK, the drive strobes the data lines; on the negation of WCLK, the controller changes the data on the data lines.

2.3.2 Control Lines

The control bus section of the Massbus consists of a 17-bit (16 bits plus parity bit) parallel control and status data path, and 14 control lines (Figure 2-3). The control bus lines are described in the following nine paragraphs.

Parallel Control – The parallel control path consists of a 16-bit parallel data path designated C00 through C15 and an associated parity bit (CPA). The control lines are bidirectional and employ odd parity.

Drive Select [DS (0:2)] –These three lines trnasmit a 3-bit binary code from the controller to select a particular RM02 or RM03. The RM02 or RM03 responds when the select (unit) number plug on the front panel of the RM02 or RM03 corresponds to the transmitted binary code.

Controller-to-Drive (CTOD) – This signal is generated by the controller and indicates the direction in which control and status information is to be transferred. For a controller-to-drive transfer, the controller asserts CTOD. For a drive-to-controller transfer, the controller negates this signal.

Register Select [RS (0:4)] – These five lines transmit a 5-bit binary code from the controller to the selected RM02 or RM03. The binary code selects one of the RM02 or RM03 registers.

NOTE

Sixteen registers are contained in the RM02 or RM03 adapter and are designated by RM codes 00_8 through 17_8. Six registers are contained in the controller. Table 2-1 lists the registers and their locations. If a register code higher than 17_8 is detected by the RM02 or RM03 hardware, an illegal register (ILR) error occurs in the RM02 or RM03.

Demand (DEM) – This signal is asserted by the controller to indicate that a transfer is to take place on the control bus. For a controller-to-drive transfer, DEM is asserted by the controller when data is present and settled on the control bus. For a drive-to-controller transfer, DEM is asserted by the controller to request data and is negated when the data has been strobed off the control bus. In both cases, the RS, DS, and CTOD lines are generated and allowed to settle before assertion of DEM.

Transfer (TRA) – This signal is asserted by the selected RM02 or RM03 in response to DEM. For a controller-to-drive transfer, TRA is asserted after the data has been strobed and is negated after DEM is negated. For a drive-to-controller transfer, TRA is asserted after the data has been gated onto the bus and negated after the negation of DEM is received.

Table 2-1 Controller/Drive Registers

Massbus Address (Octal)	Register	Mnemonic	Type
	Drive Registers		
00	Control (shared)	RMCS1	Read/write
01	Drive Status	RMDS	Read only
02	Error Register 1	RMER1	Read/write
03	Maintenance 1	RMMR1	Read/write
04	Attention Summary	RMAS	Read/write
05	Desired Sector/Track Address	RMDA	Read/write
06	Drive Type	RMDT	Read only
07	Look-Ahead	RMLA	Read only
10	Serial Number	RMSN	Read only
11	Offset	RMOF	Read/write
12	Desired Cylinder Address	RMDC	Read/write
13	Holding	RMHR	Read only
14	Maintenance 2	RMMR2	Read only
15	Error Register 2	RMER2	Read/write
16	ECC Position	RMEC1	Read only
17	ECC Pattern	RMEC2	Read only
	Controller Registers		
	Control (shared)	RMCS1	Read/write
	Word Count	RMWC	Read/write
	Bus Address	RMBA	Read/write
	Status	RMCS2	Read/write
	Data Buffer	RMDB	Read/write
	Bus Address Extension	RMBAE	Read/write
	Control and Status 3	RMCS3	Read/write

Attention (ATTN) – This line is shared by all eight RM02s or RM03s attached to a controller; it may be asserted by any RM02 or RM03 as a result of an abnormal condition or status change in the RM02 or RM03. An ATA status bit in each drive is set whenever that drive is asserting the ATTN line. ATTN may be asserted due to any of the following conditions:

1. An error while no data transfer is taking place (asserted immediately)

2. Completion of a data transfer command if an error occurred during the data transfer (asserted at the end of the data transfer)

3. Completion of a mechanical motion command (seek, recalibrate, etc.) or of a search command

4. As a result of the medium-on-line (MOL) bit changing states (except in the unload operation). In the dual-controller configuration, a change in state of MOL causes the assertion of ATTN to both controllers.

The ATA bit in an RM02 or an RM03 is cleared by the following actions:

1. Asserting initialize (INIT) on the Massbus (affects all eight drives)
2. Executing a drive clear command
3. Causing Unibus A INIT by a console operation
4. Writing a 1 into the attention summary register (in the bit position for this RM02 or RM03), which clears the ATA bit, but does not clear the error
5. Writing a valid command (with the GO bit asserted) into the RMCS1 register if no error occurs. Note that clearing the ATA bit of one RM02 or RM03 does not always cause the ATTN line to be negated because other RM02s or RM03s may also be asserting the line.

NOTE

There are three cases in which ATA is not reset when a command is written into the control register (with the GO bit set). These are: (1) if there is a control bus parity error on the write, (2) if an error was previously set, or (3) if an illegal function (ILF) code is written.

Initialize (INIT) – This signal is asserted by the controller to perform a system reset of all the RM02s and RM03s. It is asserted when a 1 is written into the CLR bit (bit 05 of RMCS2) and when Unibus INIT is asserted on Unibus A. When an RM02 or RM03 receives the INIT pulse, it immediately aborts the execution of any current command and performs all actions described for the drive clear command.

NOTE

In the dual-controller configuration, an RM02 or an RM03 honors an INIT pulse only from the controller that has seized the RM02 or RM03, or from either controller if the RM02 or RM03 is in the unseized state. In addition, the ATA and VV bits, which exist independently on each port of the RM02 or RM03, can be cleared only from their respective controller.

FAIL – When asserted, this signal indicates that a power-fail condition has occurred in the controller. While FAIL is asserted, the RM02 or RM03 inhibits reception of the INIT and DEM signals at the RM02 or RM03.

2.4 DRIVE INTERFACE

The internal signal interface between the adapter and the drive is accomplished through two cables as shown in Figure 2-1. These cables, designated cable A and cable B, route both data and command signals between the units.

2.4.1 Interface Cable A

The cable A signal lines are shown in Figure 2-4 and described in the following 12 paragraphs.

Select Address (1, 2, 4) – These three lines are binary encoded with a logical number that represents the address of one of the eight possible RM02s or RM03s. The address value (0 through 7) is front-panel selectable by using a removable logic plug.

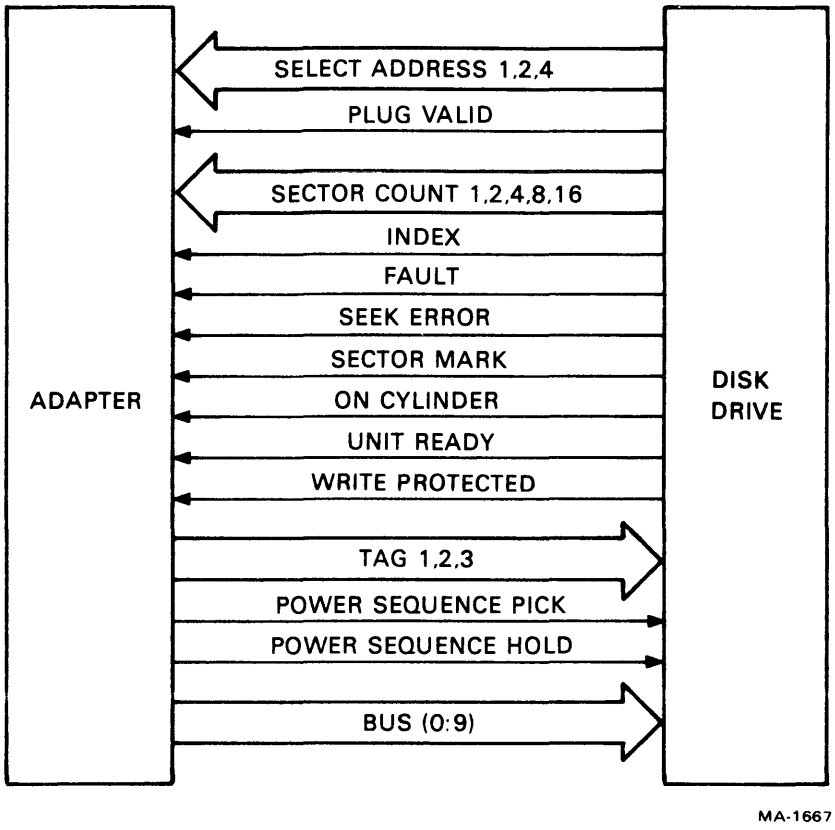


Figure 2-4 Cable A Interface Lines

The binary code on these lines is present at least 200 ns prior to the plug valid signal becoming asserted and remains present until at least 200 ns after the logic plug is removed.

Plug Valid – When asserted, this signal indicates that a logic plug is inserted in the front panel.

Sector Count 1, 2, 4, 8, 16 – These five lines contain the binary value of the sector presently under the heads. The value changes on the leading edge of the sector pulse and clears to 0 on the leading edge of the index pulse. Maximum count is 29_{10} in 18-bit format or 31_{10} 16-bit format.

Index – This signal occurs once per revolution and its leading edge is considered the leading edge of the sector 0 (typically 2.5 μs wide).

Fault – When asserted, this signal indicates that one or more of the following five faults occurred in the drive.

1. DC power fault
2. Head select fault
3. Write fault
4. Write or read while off cylinder
5. Write command during a read operation

A fault condition immediately inhibits the write capability to prevent data destruction. The dc power fault indicates a below-normal voltage from the positive or negative power supplies. The head select fault indicates that more than one head is selected. The write fault indicates low (or the absence of) write current as well as the absence of write data. The drive does not write or read while off cylinder, and generates a fault condition. The drive also generates a fault if it receives a write command during a read operation.

The fault condition may be cleared by a drive clear command or the FAULT CLEAR switch on the operator panel, or master fault clear on the fault card (providing the fault no longer exists). Faults are stored in individual flip-flops as maintenance aids, and may be cleared by the INIT signal, by powering down dc power, or by means of the switch on the fault card.

Seek Error – When asserted, this signal indicates that a seek error has occurred in the drive. The error is cleared by performing a return-to-zero or initialize. This signal indicates that the unit was unable to complete a move within 500 ms, or that the carriage has moved to a position outside the recording field, or that an address greater than 822 tracks has been selected. If an address greater than 822 tracks is selected, the seek error signal asserts within 100 ns of the cylinder select tag, and the carriage movement is inhibited to not more than one track.

A return-to-zero seek command clears the seek error condition, returns the heads to cylinder 0, and enables an on cylinder signal to the controller.

Sector Mark – This signal occurs once per sector. It is typically 1.25 μs wide.

On Cylinder – This signal is asserted when the servo has positioned the heads over a track. It is cleared with any seek instruction causing carriage movement, or a zero-track seek. A carriage offset results in loss of on cylinder for a period of 2.75 ms (nominal). For a zero-track seek, the on cylinder signal is removed for 30 μs (nominal).

Unit Ready – When asserted, this signal indicates that the following three drive conditions have occurred.

1. Pack is revolving at correct speed.
2. Heads are loaded.
3. No drive fault condition exists.

Write Protected – This signal is asserted when the front panel's WRITE PROTECT switch is pressed. It prevents data from being written onto disk. Attempting any write function causes a write lock error (WLE) indication.

Tag 1, 2, 3 – These three lines select one of three functions and also permit the bit pattern on the 10 bus lines to be decoded. Only one tag line at a time is asserted. When tag 1 is asserted, the bus lines contain a binary number that represents the cylinder address to which the heads are to move. (Only decimal numbers 0 through 822 are valid.) Tag 2 decodes bits 0 through 2 of the bus lines to select the drive head. (Only decimal numbers 0 through 4 are valid.) Tag 3 selects one of the eight possible drive control commands as follows.

Bit 0 (Write Gate)	When asserted, enables the write driver and allows data to pass through the selected head onto the disk.
Bit 1 (Read Gate)	When asserted, enables the read circuits and allows data read by the head to be sent to the controller.

Bit 2 (Servo Offset Plus) — When asserted, the head actuator is offset from the nominal on cylinder position to a position 200 microinches toward the spindle.

Bit 3 (Servo Offset Minus) — When asserted, the head actuator is offset from the nominal on cylinder position to a position 200 microinches away from the spindle.

Bit 4 (Fault Clear) — When asserted, clears the drive fault flip-flop if the fault condition no longer exists.

Bit 5 — Not used.

Bit 6 (RTZ) — When asserted, causes a return-to-zero (RTZ) condition where the heads position over track 0, the head register resets, and the seek error flip-flop clears.

NOTE

This seek takes significantly longer than a normal seek to track 0, and should only be used for recalibration.

Bit 7 — Not used.

Bit 8 — Not used.

Bit 9 — Not used.

Table 2-2 contains the tag line and bus bit decoding arrangement.

Table 2-2 Tag Line and Bus Bit Decoding Arrangement

	Tag 1 Asserted	**Tag 2 Asserted**	**Tag 3 Asserted**
Bus Bit	**Cylinder Address**	**Head Select**	**Control Select**
0	1	1	Write Gate
1	2	2	Read Gate
2	4	4	Servo Offset Plus
3	8	Not used	Servo Offset Minus
4	16	Not used	Fault Clear
5	32	Not used	Not used
6	64	Not used	Return to Zero
7	128	Not used	Not used
8	256	Not used	Not used
9	512	Not used	Not used

Power Sequence Pick and Power Sequence Hold – A ground on both of these lines causes the drive to energize if the following conditions have already been met.

1. AC and dc power on
2. START/STOP switch in START position
3. REMOTE/START switch in REMOTE position

2.4.2 Interface Cable B

The cable B signal lines are shown in Figure 2-5 and described in the following eight paragraphs.

Servo Clock – The phase-locked 9.677 MHz clock generated from the servo track dibits is present on this line.

Read Data – The data read from the disk is available on this line.

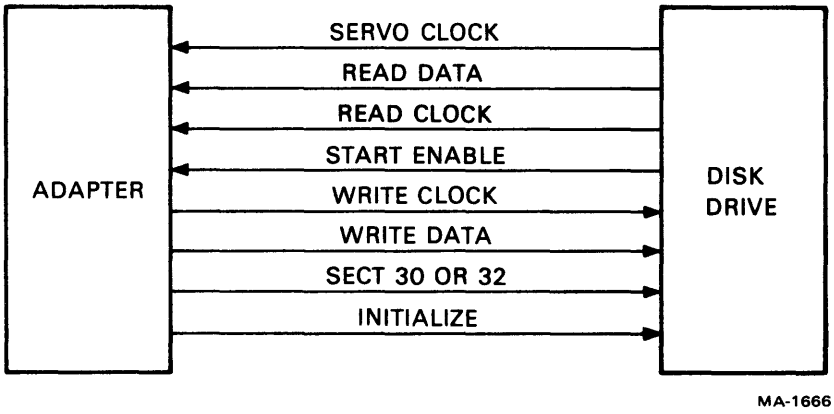


Figure 2-5 Cable B Interface Lines

Read Clock – This line contains the 9.677 MHz read clock pulses. The negative-going edge of the read clock pulse is synchronous with the data being read from the disk.

Start Enable – When asserted, this line indicates that the STOP/START switch is in the START position. When low, the switch is in the STOP position.

Write Clock (WCLK) – This line contains the signal, which is actually the servo clock signal that has been retransmitted back to the drive by the controller during a write operation. The write clock is synchronous with the data that is to be written on the disk.

Write Data – This line contains the data that is to be written on the disk.

SEC 30 or 32 – When asserted, this line configures the disk into 32 sectors per revolution. When low, the configuration is 30 sectors. This line is clocked with the leading edge of the index mark.

Initialize (INIT) – When asserted, this line clears all drive fault latches and seek error flip-flops (providing the fault no longer exists).

2.5 POWER SEQUENCE CABLE

The main purpose of the power sequence cable is to prevent two or more drives from starting up simultaneously. This could happen, for example, if there is a power failure while several drives are running. If the power is restored before the drives are shut down, the current drawn by all the drives starting up could be enough to overload the building circuit breakers. The power sequence cable (Figure 2-6) prevents this.

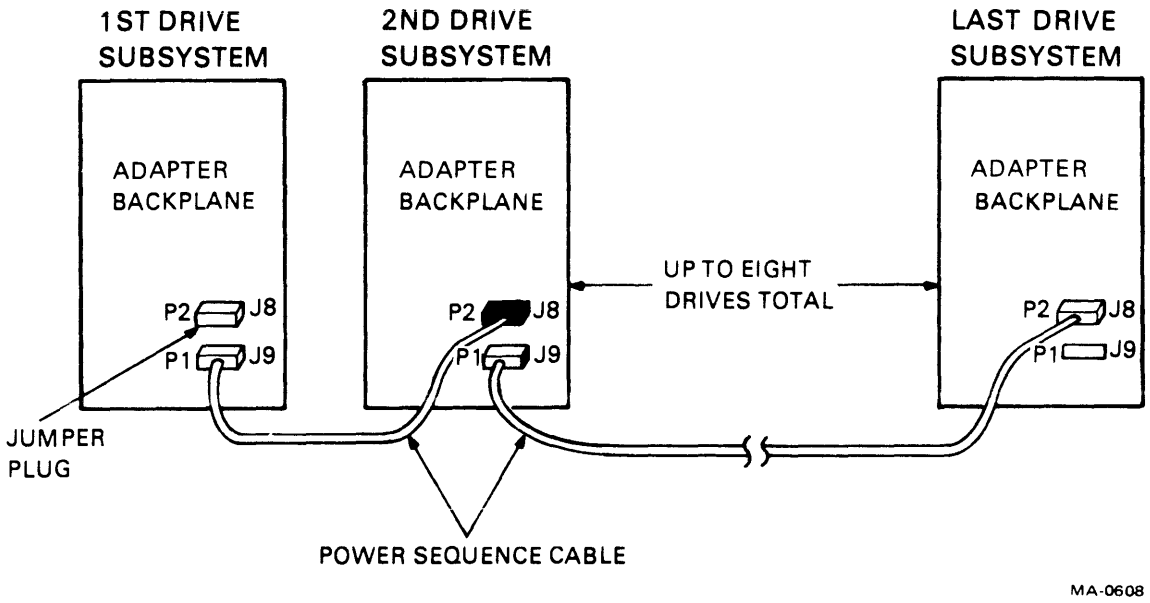


Figure 2-6 Power Sequence Cable Configuration

The cable consists of three lines: start in progress (SIP), grant, and ground. The SIP line is a parallel connection to all the drives on the power sequence cable. It is normally high. When a drive starts up, however, the drive pulls the SIP line low. Any other drive attempting to start while the SIP line is low will be unable to do so.

The grant line is connected serially through all the drives on the power sequence cable. The signal coming into a drive (from the previous drive) on this line is called grant-in, and the signal leaving a drive (and entering the next drive) is called grant-out. If a drive in the sequence is powered down, the grant line passes directly through that drive, so that grant-out always matches grant-in. The first drive in the sequence has a jumper plug (Figure 2-6) that ties this drive's grant-in to ground. When a drive sees a low grant-in, it can start if instructed to do so (assuming SIP is high).

While the first drive is going through its start cycle, it pulls its grant-out high. This is interpreted by the next drive in the sequence as a high grant-in, and thus the next drive cannot start up until the first drive has gone through its start-up cycle.

Any drive in the sequence may be stopped (to change the disk cartridge, etc.) and then restarted, but only if all the drives before it are either running or powered down.

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 INTRODUCTION

The first part of this chapter (Paragraph 3.2) describes the 16 different command operations that the RM02 or RM03 can execute. The command operations are divided into three categories: positioning commands, data transfer commands, and housekeeping commands. The names and descriptions for each of the 16 commands are given in Paragraph 3.2.

The second part of this chapter (Paragraph 3.3) is a summary of the 22 registers used by the RM02 or RM03 and the controller to communicate control commands, status data, error conditions, and maintenance information.

Paragraph 3.4 contains a bit-by-bit description of each of the 22 registers. The registers used by the controller are described in Paragraph 3.4.1; the registers used by the drive are detailed in Paragraph 3.4.2. Detailed bit descriptions can be found in the *RM02/03 Disk Subsystem User's Manual.*

This chapter ends with Paragraph 3.5 which provides a brief functional description of the RM02 and RM03 subsystem diagnostics.

3.2 COMMAND OPERATIONS

3.2.1 Positioning Commands

Positioning commands are mechanical movement commands used to position the heads over the disk pack; they take milliseconds to complete. These commands assert the ATTN line after their normal completion. The positioning commands are described below.

Seek – A seek causes the heads to be moved to the cylinder address specified by the desired cylinder register (RMDC). The current cylinder is made equal to the desired cylinder address following the completion of the command.

Recalibrate – A recalibrate positions the heads over cylinder 0 and sets the current cylinder address register to 0.

Offset – An offset allows the heads to be moved off the track centerline. It is used in error recovery processing and moves the heads 200 microinches either toward the spindle (positive offset) or away from the spindle (negative offset).

Return-to-Centerline – Return-to-centerline is used to explicitly return to the track centerline after an offset operation.

Search – A search combines the seek command for the desired sector address and can be considered a synchronization command between the software and the desired disk address.

3.2.2 Data Transfer Commands

These commands involve the transfer of data to or from the disk. They usually require the completion of: (1) a positioning command by either a seek or search command or (2) an implied seek as part of the read data command. The data transfer commands are described in the following six paragraphs.

Read Header and Data – A read header and data command transfers two words of header information and 256 data words per sector from the disk pack to the RH controller.

Read Data – A read data command transfers 256 data field words from the disk pack to the RH controller for each sector. If an error is detected in the header, this command aborts immediately following the CRC check and there is no data transferred.

Write Check Header and Data – A write check header and data command transfers the first two words of the header and 256 words of data to the RH controller. Errors in the header, however, cause termination of the command after the CRC word of the header is checked in the adapter.

Write Check Data – This command is identical to a read data command.

Write Header and Data – A write header and data command, also referred to as a "format" command, writes all gaps, headers, and data for the sector(s). The RM02 or RM03 generates the gaps including the sync byte, CRC, and ECC. The RH controller supplies 2 header words and 256 data words for each sector.

Write Data – A write data command transfers 256 words of data for each specified sector from the RH controller to the drive. This data field is preceded by a sync byte and followed by a 32-bit ECC, both generated by the RM02 or RM03. A header error causes the command to abort immediately after checking the CRC word.

3.2.3 Housekeeping Commands

Housekeeping commands are used to place the drive logic into a known or initial state. ATTN is not raised at the completion of the housekeeping commands unless there is a persistent error condition. The five housekeeping commands are listed below.

No-Op – Upon recognizing this code in the control (RMCS1) register and the GO bit, the RM02 or RM03 resets the GO bit. This command is considered a filler command.

Drive Clear – A drive clear command clears bits in the following registers in the adapter:

Status (RMDS)	Bit 14 (ERR) Bit 15 (ATA)
Error 1 (RMER1)	All bits
Error 2 (RMER2)	All bits
Attention Summary (RMAS)	Respective bit
Maintenance 1 (RMMR1)	All bits
ECC Pattern (RMEC2)	All bits

This command also clears all error indications in the drive (provided the error condition no longer exists). A pulse on the Massbus INIT line performs the same functions as the drive clear command.

Release – The release command performs a drive clear function and releases the drive for use by the other port.

Read-In Preset – The read-in preset command sets the volume valid (VV) bit (06) in the status (RMDS) register for the port that issued the command. This command also clears all bits in the desired sector/track address (RMDA) register and all bits in the desired cylinder address (RMDC) register. It also clears the offset mode and the following bits in the offset (RMOF) register.

- OFD (bit 07) – Offset Direction
- HCI (bit 10) – Header Compare Inhibit
- ECI (bit 11) – Error Correction Code Inhibit
- FMT 16 (bit 12) – Format

Pack Acknowledge – The pack acknowledge command sets the volume valid (VV) bit (06) in the status (RMDS) register for the port that issued the command. This command must be issued before any data transfer or positioning commands can be given if the pack has gone off-line and then on-line (i.e., MOL changes state). It is primarily intended to avoid unknown pack changes on a dual-controller RM02 or RM03 configuration.

3.2.4 Command Codes

The programmer initiates operations by selecting an RM02 or an RM03, addressing the control register (776700), and loading the register with a function code and setting the GO bit. The function code specifies a specific command. Upon assertion of the GO bit, the RM02 or RM03 proceeds to execute the command. The commands can be divided into three categories: positioning commands, data transfer commands, and housekeeping operations. These commands and their corresponding octal function codes are listed in Table 3-1.

Table 3-1 Command Codes

Command	Function Codes (Octal)
Positioning Commands	
Seek	5
Recalibrate	7
Offset	15
Return-to-Centerline	17
Search	31
Data Transfer Commands	
Write Check Data	51
Write Check Header and Data	53
Write Data	61
Write Header and Data (Format)	63
Read Data	71
Read Header and Data	73
Housekeeping Operations	
No-Op	1
Drive Clear	11
Release	13
Read-In Preset	21
Pack Acknowledge	23

NOTE
The function codes include the GO bit.

3.3 REGISTER SUMMARY

The names, mnemonics, and addresses of the 22 RM02 or RM03 subsystem registers are given in Paragraph 3.3.1. Figure 3-1 shows an illustration of all the registers. Paragraph 3.4 contains a list of the names of each bit in each register.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
RMDT (776726) 06	0	0	MOH 1	0	DRQ	0	0	DT 8	DT 7	DT 6	DT 5	DT 4	DT 3	DT 2	DT 1	DT 0	R
RMSN (776730) 10	SN 8000	SN 4000	SN 2000	SN 1000	SN 800	SN 400	SN 200	SN 100	SN 80	SN 40	SN 20	SN 10	SN 8	SN 4	SN 2	SN 1	R
RMOF (776732) 11	0	0	0	FMT 16	ECI	HCI	0	0	OFF DIR	0	0	0	0	0	0	0	R/W
RMDC (776734) 12	0	0	0	0	0	0	DC 512	DC 256	DC 128	DC 64	DC 32	DC 16	DC 8	DC 4	DC 2	DC 1	R/W
RMHR (776736) 13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W
RMMR2 (776740) 14	RQA	RQB	TAG	TEST BIT	CIC	CIH	BB 9	BB 8	BB 7	BB 6	BB 5	BB 4	BB 3	BB 2	BB 1	BB 0	R
RMER2 (776742) 15	BSE	SKI	OPE	IVC	LSC	LBC	0	0	DVC	0	0	0	DPE	0	0	0	R/W
RMEC1 (776744) 16	0	0	0	P 4096	P 2048	P 1024	P 512	P 256	P 128	P 64	P 32	P 16	P 8	P 4	P 2	P 1	R
RMEC2 (776746) 17	0	0	0	0	0	PAT 11	PAT 10	PAT 9	PAT 8	PAT 7	PAT 6	PAT 5	PAT 4	PAT 3	PAT 2	PAT 1	R
RMBAE (776750) RH	0	0	0	0	0	0	0	0	0	0	A21	A20	A19	A18	A17	A16	R/W
RMCS3 (776752) RH	APE	DPE HI	DPE LO	WCE HI	WCE LO	DBL	0	0	0	IE	0	0	IPCK 3	IPCK 2	IPCK 1	IPCK 0	R/W

MA-0652

Figure 3-1 Register Summary (Sheet 1 of 2)

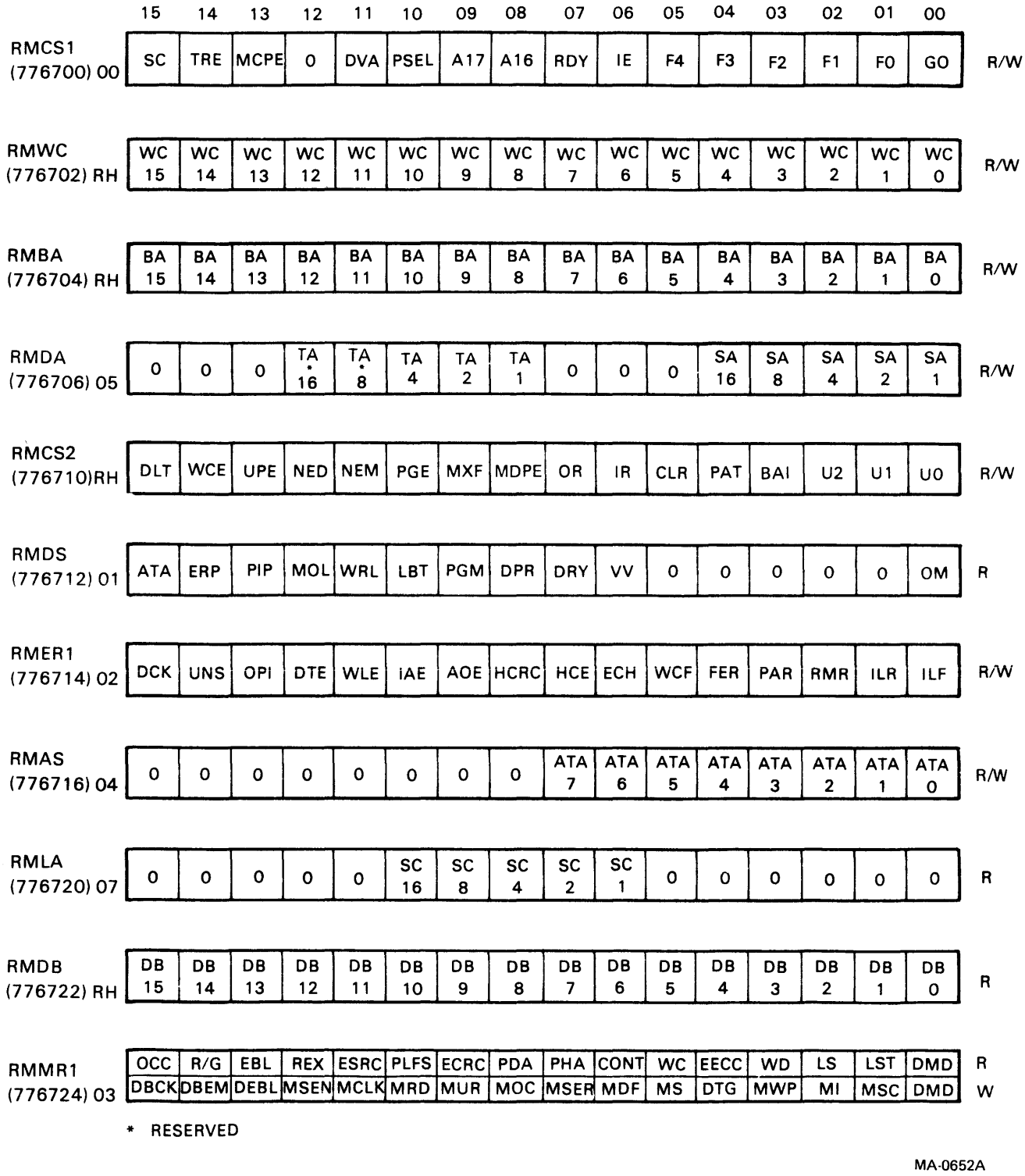


Figure 3-1 Register Summary (Sheet 2 of 2)

3.3.1 Register Names and Addresses

Table 3-2 contains a list of the 22 RM02 or RM03 device register names, mnemonics, and addresses.

Table 3-2 Controller and Drive Device Registers

Mnemonic	Register Name	Unibus Address	Massbus Address	Mode	Function
RMCS1	Control	776700	00*	Read/write	Contains function Code, GO bit
RMWC	Word Count	776702	†	Read/write	Contains 2's complement of number of words to be transferred
RMBA	Bus Address	776704	†	Read/write	Contains memory address of location where data transfer is to begin
RMDA	Desired Sector/Track Address	776706	05	Read/write	Contains disk sector and track address where transfer is to occur
RMCS2	Status	776710	†	Read/write	Contains controller status indication
RMDS	Drive Status	776712	01	Read only	Contains all non-error status plus error summary bit
RMER1	Error No. 1	776714	02	Read/write	Contains individual error indications
RMAS	Attention Summary	776716	04	Read/write	Contains 1 bit per drive attention summary status
RMLA	Look-Ahead	776720	07	Read only	Contains current sector address under heads
RMDB	Data Buffer	776722	†	Read/write	Contains input and output connection to silo for maintenance

*RMCS1 is shared by drive and controller.
†Controller registers.

Table 3-2 Controller and Drive Device Registers (Cont)

Mnemonic	Register Name	Unibus Address	Massbus Address	Mode	Function
RMMR1	Maintenance No. 1	776724	03	Read/write	Contains diagnostic test functions
RMDT	Drive Type	776726	06	Read only	Contains drive type/options
RMSN	Serial Number	776730	10	Read only	Contains lowest four digits of drive serial number
RMOF	Offset	776732	11	Read/write	Contains bit for control of offset of drive heads
RMDC	Desired Cylinder	776734	12	Read/write	Contains address cylinder for seek operation
RMHR	Holding	776736	13	Read/write	Used only by diagnostic software
RMMR2	Maintenance No. 2	776740	14	Read only	Contains diagnostic test functions
RMER2	Error No. 2	776742	15	Read/write	Contains drive error bits
RMEC1	ECC Position	776744	16	Read only	Contains position of burst error
RMEC2	ECC Pattern	776746	17	Read only	Contains the burst error
RMBAE	Bus	776750	‡	Read/write	Contains the bus address extension bits
RMCS3	Control and Status	776752	‡	Read/write	Contains status and error indications

*RMCS1 is shared by drive and controller.
†Controller registers.
‡RH10, RH20, and RH70 only.

3.3.2 Register Summary

Figure 3-1 illustrates all 22 of the RM02 or RM03 subsystem registers, as listed, bit-by-bit, in Paragraph 3.4.

3.4 REGISTER BIT LISTING

3.4.1 Controller Registers

3.4.1.1 Control Register 1 (as used by controller) (RMCS1)

Table 3-3 RMCS1 Bit Assignments

Bit	Name	Type
00–05	Not Used by RH Controller (Table 3-9)	–
06	Interrupt Enable (IE)	R/W
07	Ready (RDY)	R
08, 09	Bus Address Extension Bits (A16, A17)	R/W
10	Port Select (PSEL)	R/W
11	Not Used by RH Controller (Table 3-9)	–
12	Not Used; always 0	–
13	Massbus Control Bus Parity Error (MCPE)	R
14	Transfer Error (TRE)	R/W
15	Special Condition (SC)	R

3.4.1.2 Word Count Register (RMWC)

Table 3-4 RMWC Bit Assignments

Bit	Name	Type
00–15	Word Count (WC)	R/W

3.4.1.3 Address Register (RMBA)

Table 3-5 RMBA Bit Assignments

Bit	Name	Type
0	Not used; always 0	–
01–15	Bus Address (BA)	R/W

3.4.1.4 Status Register 2 (RMCS2)

Table 3-6 RMCS2 Bit Assignments

Bit	Name	Type
00–02	Unit Select (U)	R/W
03	Bus Address Increment Inhibit (BAI)	R/W
04	Parity Test (PAT)	R/W
05	Controller Clear (CLR)	W
06	Input Ready (IR)	R
07	Output Ready (OR)	R
08	Massbus Data Bus Parity Error (MDPE)	R
09	Missed Transfer (MXF)	R/W
10	Program Error (PGE)	R
11	Nonexistent Memory (NEM)	R
12	Nonexistent Drive (NED)	R
13	Unibus Parity Error (UPE)	R/W
14	Write Check Error (WCE)	R
15	Data Late (DLT)	R

3.4.1.5 Data Buffer Register (RMDB)

Table 3-7 RMDB Bit Assignments

Bit	Name	Type
00–15	Data Buffer (DB)	R/W

3.4.1.6 Bus Address Extension Register (RMBAE)

Table 3-8 RMBAE Bit Assignments

Bit	Name	Type
00–05	Bus Address (A00–A05)	R/W
00–15	Not Used; Always 0s	–

3.4.1.7 Control and Status Register 3 (RMCS3)

Table 3-9 RMCS3 Bit Assignments

Bit	Name	Type
00–03	Inverted Parity Check (IPCK)	R/W
04–05	Not Used; Always 0s	–
06	Interrupt Enable (IE)	R/W
07–09	Not Used; Always 0s	–
10	Double Word (DBL)	R
11	Write Check Error – Even Word (WCE LO)	R
12	Write Check Error – Odd Word (WCE HI)	R
13	Data Parity Error – Even Word (DPE LO)	R
14	Data Parity Error – Odd Word (DPE HI)	R
15	Address Parity Error (APE)	R

3.4.2 Drive Registers

3.4.2.1 Control Register 1 (as used by drive) (RMCS1)

Table 3-10 RMCS1 Bit Assignments

Bit	Name	Type
00	Go Bit (GO)	R/W
01	Function Bit 0 (F0)	R/W
02	Function Bit 1 (F1)	R/W
03	Function Bit 2 (F2)	R/W
04	Function Bit 3 (F3)	R/W
05	Function Bit 4 (F4)	R/W
06–10	Not Used by Drive (Table 3-3)	–
11	Drive Available (DVA)	R
12–15	Not Used by Drive (Table 3-3)	–

3.4.2.2 Drive Status Register (RMDS)

Table 3-11 RMDS Bit Assignments

Bit	Name	Type
00	Offset Mode (OM)	R
01–05	Not Used; Always 0s	–
06	Volume Valid (VV)	R
07	Drive Ready (DRY)	R
08	Drive Present (DPR)	R
09	Programmable (PGM)	R
10	Last Block Transferred (LBT)	R
11	Write Lock (WRL)	R
12	Medium On-Line (MOL)	R
13	Positioning in Progress (PIP)	R
14	Error (ERR)	R
15	Attention Active (ATA)	R

3.4.2.3 Error Register 1 (RMER1)

Table 3-12 RMER1 Bit Assignments

Bit	Name	Type
00	Illegal Function (ILF)	R/W
01	Illegal Register (ILR)	R/W
02	Register Modification Refused (RMR)	R/W
03	Parity Error (PAR)	R/W
04	Format Error (FER)	R/W
05	Write Clock Fail (WCF)	R/W
06	ECC Hard Error (ECH)	R/W
07	Header Compare Error (HCE)	R/W
08	Header CRC Error (HCRC)	R/W
09	Address Overflow Error (AOE)	R/W
10	Invalid Address Error (IAE)	R/W
11	Write Lock Error (WLE)	R/W
12	Drive Timing Error (DTE)	R/W
13	Operation Incomplete (OPI)	R/W
14	Drive Unsafe (UNS)	R/W
15	Data Check Error (DCK)	R/W

3.4.2.4 Maintenance Register 1 (RMMR1)

Table 3-13 RMMR1 Bit Assignments (Read-Only Section)

Bit	Name	Type
00	Diagnostic Mode (DMD)	R
01	Last Sector and Track (LST)	R
02	Last Sector (LS)	R
03	Write Data (WD)	R
04	Enable ECC Out (EECC)	R
05	PROM Strobe	R
06	Continue (CONT)	R
07	Header Area (PHA)	R
08	Data Area (PDA)	R
09	Enable CRC Out (ECRC)	R
10	Looking for Sync (PLFS)	R
11	Enable Search (ESRC)	R
12	Exception (REX)	R
13	End of Block (EBL)	R
14	Run and Go (R/G)	R
15	Occupied (OCC)	R

Table 3-14 RMMR1 Bit Assignments (Write-Only Section)

Bit	Name	Type
00	Diagnostic Mode (DMD)	W
01	Sector Compare (MSC)	W
02	Index Pulse (MI)	W
03	Write Protect (MWP)	W
04	Not Used; Always 0	-
05	Sector Pulse (MS)	W
06	Drive Fault (MDF)	W
07	Seek Error (MSER)	W
08	On Cylinder (MOS)	W
09	Unit Ready (MUR)	W
10	Read Data (MRD)	W
11	Maintenance Clock (MCLK)	W
12	Search Timeout Disable (MSEN)	W
13	Diagnostic EBL (DEBL)	W
14	Debug Clock Enable (DBEM)	W
15	Debug Clock (DBCK)	W

3.4.2.5 Attention Summary Register (RMAS)

Table 3-15 RMAS Bit Assignments

Bit	Name	Type
00–07	Attention Active (ATA 00:07)	R/W
08–15	Not used	-

3.4.2.6 Desired Sector/Track Address Register (RMDA)

Table 3-16 RMDA Bit Assignments

Bit	Name	Type
00–04	Sector Address (SA 1,2,4,8,16)	R/W
05–07	Not Used; Always 0s	-
08–12	Track Address (TA 1,2,4,8,16) (Note: TA 8, TA 16 are reserved for future expansion)	R/W
13–15	Not Used; Always 0s	-

3.4.2.7 Drive Type Register (RMDT)

Table 3-17 RMDT Bit Assignments

Bit	Name	Type
00–08	Drive Type (DT00:08)	R
09–10	Not Used; Always 0s	-
11	Drive Request Required (DRQ)	R
12	Not Used; Always 0	-
13	Moving Head (MOH)	R

3.4.2.8 Look-Ahead Register (RMLA)

Table 3-18 RMLA Bit Assignments

Bit	Name	Type
00–05	Not Used; Always 0s	–
06–10	Sector Count (SC 1,2,4,8,16)	R
11–15	Not Used; Always 0s	R

3.4.2.9 Serial Number Register (RMSN)

Table 3-19 RMSN Bit Assignments

Bit	Name	Type
00–15	Serial Number (SN00:15)	R

3.4.2.10 Offset Register (RMOF)

Table 3-20 RMOF Bit Assignments

Bit	Name	Type
00–06	Not Used; Always 0s	–
07	Offset Direction (OFD)	R/W
08–09	Not Used; Always 0s	–
10	Header Compare Inhibit (HCI)	R/W
11	Error Correction Inhibit (ECI)	R/W
12	Format (FMT 16)	R/W
13–15	Not Used; Always 0s	–

3.4.2.11 Desired Cylinder Register (RMDC)

Table 3-21 RMDC Bit Assignments

Bit	Name	Type
00–09	Desired Cylinder	R/W
10/15	Not Used; Always 0s	–

3.4.2.12 Holder Register (RMHR) – This is an addressable register with no drive function. It is used only by diagnostic software. When writing into this register, all bits remain unchanged and new information is lost. When reading this register (or any illegal register), the complement of the register contents is read. Whenever writing any legal register, this holding register is concurrently written.

3.4.2.13 Maintenance Register 2 (RMMR2)

Table 3-22 RMMR2 Bit Assignments

Bit	Name	Type
00–09	Bus in Lines (BB00:09)	R
10	Control or Head Select (CIH)	R
11	Control or Cylinder Select (CCH)	R
12	Test Bit (TEST BIT)	R
13	Tag (TAG)	R
14	Request B (RQB)	R
15	Request B (RQA)	R

3.4.2.14 Error Register 2 (RMER2)

Table 3-23 RMER2 Bit Assignments

Bit	Name	Type
00–02	Not Used; Always 0s	–
03	Data Parity Error (DPE)	R/W
04–06	Not Used; Always 0s	–
07	Device Check (DVC)	R/W
08–09	Not Used; Always 0s	–
10	Loss of Bit Check (LBC)	R/W
11	Loss of System Clock (LSC)	
12	Invalid Command (IVC)	R/W
13	Operator Plug Error (OPE)	R/W
14	Seek Incomplete (SKI)	R/W
15	Bad Sector Error (BSE)	R/W

3.4.2.15 ECC Position Register (RMEC1)

Table 3-24 RMEC1 Bit Assignments

Bit	Name	Type
00–12	Position Bit (P)	R
13–15	Not Used; Always 0s	–

3.4.2.16 ECC Pattern Register (RMEC2)

Table 3-25 RMEC2 Bit Assignments

Bit	Name	Type
00–10	Pattern Bit (PAT00:10)	R
11–15	Not Used; Always 0s	–

3.5 RM02 AND RM03 DIAGNOSTICS

The diagnostic tests described in this paragraph may be used to demonstrate system performance or to help pinpoint problem areas. Ten RM02 and RM03 diagnostics are described in the following paragraphs.

3.5.1 RM02/RM03 Formatter (MAINDEC-ZZ-CZRMA)

This program provides the facilities to format or check the header and data fields of each data block on the disk pack.

In the format operation, the program writes the header of each data block with a cylinder number, track number, and sector number. It also writes the data field with a selected data pattern. The program then verifies the written data blocks by executing the write check head and data command.

In the check operation, the program repeats the format operation three times while the data pattern is rotated one bit at each pass. This diagnostic also allows access to the Bad Sector File.

3.5.2 RM02/RM03 Performance Exerciser (MAINDEC-ZZ-CZRMB)

This program performs an interactive test on RM02 or RM03 disk drives connected to a Massbus system. It is used to verify that the drives under test are performing to their data error rate.

The program exercises a mixed system of dual-port and single-port drives and monitors the performance of each. It reports the statistics for each drive being exercised either on request from the operator or automatically at intervals determined by the operator.

3.5.3 RM02/RM03 Functional Test

The test is comprised of three parts, which would normally be run in sequence starting with Part I. Briefly, Part I tests housekeeping and mechanical positional operations. Part II tests write, read, and write-check operations using header and data. Part III tests write, read, and write-check operations using data.

3.5.3.1 Part I (MAINDEC-ZZ-CZRMC) – The functional test is a stand-alone program that uses functional means to verify the operability of the RM02 or RM03 Disk Drive Subsystem. It is used to establish confidence in the basic operations of the disk drive, including mechanical positioning and data transfer operations.

3.5.3.2 Part II (MAINDEC-ZZ-CZRMD) – Part II of the functional test performs write, read, and write check operations using header and data. Note that Part II of the functional test leaves two header errors on the media and the pack must be reformatted after running this test.

3.5.3.3 Part III (MAINDEC-ZZ-CZRME) – Part III of the funtional test performs write, read, and write-check operations using data. Note that Part III of the functional test leaves two header errors on the media and the pack must be reformatted after running this test.

NOTE

Although the functional test, Parts II and III, leaves header errors on the pack, the Revision B or higher versions will correct the errors. Revision A of the functional test requires reformatting after each use.

3.5.4 RM02/RM03 Extended Drive Test (MAINDEC-ZZ-CZRMF)

This program contains a series of tests to verify that the disk drive is capable of performing seeks and that the access times are within tolerance. It also verifies that the track and sector addressing circuitry operates properly and that the data storage and retrieval capabilities are functioning.

3.5.5 RM02/RM03 Dual-Port Logic Test, Part I (MAINDEC-ZZ-CZRMG)

This program performs tests on the dual-port control logic. During this test, both parts of the drive are cabled to the same Massbus by a special adapter cable. This arrangement allows the dual-port logic to be tested from a single RH controller.

3.5.6 RM02/RM03 Dual-Port Logic Test, Part II (MAINDEC-ZZ-CZRMH)

Part II of the dual-port logic program is used to test the PORT SELECT switch. The special cable is used during this test also to permit operation from a single RH controller.

3.5.7 RM02/RM03 Drive Compatibility Test (MAINDEC-ZZ-CZRMI)

This program is used to verify the compatibility of up to 16 RM02 or RM03 drives that may reside on one or more RH controller. It tests the ability of a drive to write data that can be successfully read by all other drives, and to over-write data written by all other drives. The following causes of incompatibility can be detected.

1. Head misalignment
2. Positioner lateral misalignment
3. Spindle cartridge interface runout
4. Improper levels of write current
5. Incorrect addressing of read/write heads

3.5.8 RM02/RM03 Diskless Diagnostic (MAINDEC-ZZ-CZRMJ)

This stand-alone program is used to verify the operability of the RM02 or RM03 disk subsystem independently of the disk drive. It is used to resolve hardware failures in the RM02 or RM03 Massbus adapter to field-replaceable modules.

3.6 OPERATION OF ERROR CORRECTING CODE (ECC)

The RM02 or RM03 contains error correcting code (ECC) logic which has the capability to detect errors in the data being read off the disk and provide information to the software to permit data recovery.

The ECC code employed, called burst error correcting code, locates an error that falls within an 11-bit burst.

Any errors outside this 11-bit burst length are detected but not correctable. For uncorrectable errors, the ECC logic generates an ECC hard error (ECH) indication.

An uncorrectable error is defined as any error field *larger* than the 11-bit burst. Isolated dropped bits are, for example, 1 bit in word 0 and 1 bit in word 225.

If the above conditions occur, the drive indicates the ECC uncorrectable error to the software by setting the ECC hard error bit (ECH) in error register 1 (RMER1).

The ECC logic performs the following.

1. Finds the 11-bit burst where the read error is located
2. Determines the exact location of the burst within the data field

This error information is provided to the controller through two registers.

Pattern Register (RMEC2)	Contains the actual 11-bit error burst
ECC Position Register (RMEC1)	Contains the address of the first bit of the error burst within the data field.

The actual correction of the data field is done by the software using the data contained in these two registers.

In the event of an ECC hard error, the contents of the ECC pattern and ECC position registers are of *no significance*.

3.6.1 ECC Operation During a Data Write

The ECC generation is started with the first bit following the sync pattern for the data field and continues for the entire data field, ending with the last bit of the data field. This ECC (32 bits) is then shifted out unaltered immediately following the last data word (word 256) and placed onto the disk sector.

3.6.2 ECC Operation During a Data Read

The ECC field in the sector block always follows the 256-word data block. The data block is guaranteed to be 256 words in length, regardless of whether the 16- or 18-bit mode is employed. After transmitting the required 256 data words, the logic inhibits communication with the controller until the ECC field is shifted through the ECC register for a possible read error detection.

3.6.3 Error Detection and Isolation

The ECC operation stops as soon as the last bit of the 32-bit ECC field is read in from the disk. At this point, the ECC register (by nature of the code used) should contain all 0s. A non-zero result in these bits indicates a data error and causes a data check error indication [bit 15 of error register 1 (RMER1) sets].

If no error is detected in the data field after the last word has been read, the read command normally terminates without any time delay.

If an error has been detected in the data field (and ECC hardware is enabled), the procedure to correct this error is accomplished by the ECC hardware, which goes through a routine to isolate the 11-bit error burst in the data field. The exact location of this burst is available to the software.

NOTE

If an error has occurred and has been detected by the ECC hardware following transmission of the data block, the data check (DCK) error bit remains set throughout the entire correction process (providing the ECI bit is reset).

The software then takes the ECC burst pattern and proceeds to find the bits in error and correct them.

3.6.4 ECC Inhibit/Enable Function

Error correction in the drive is enabled or inhibited by the error correction inhibit (ECI) bit (RMOF, bit 11). If this bit is asserted, the drive logic inhibits error correction when an error is detected. The read operation continues as if no error occurred. If this bit is negated, the drive logic enables the ECC circuitry when a read error is detected.

3.7 DUAL-PORT OPTION

The dual-port option for the RM02 or RM03 provides the capability for two controllers to access the same drive. Figure 3-2 shows the dual-controller configuration. Note that the eight drives are daisy-chained and that the two controllers can be attached to the same or to two different central processors.

NOTE

Since both the PDP-11 and PDP-10 processors have the capability (through RH11 and RH10 controllers, respectively) to interface to the Massbus, it is possible for both of these processors to be connected (through their respective controllers) into the configuration in Figure 3-2. In this configuration, both processors can operate in their separate format modes (16 bits/word for the PDP-11, 18 bits/word for the PDP-10) as long as there is no attempt to mix formats on the same track.

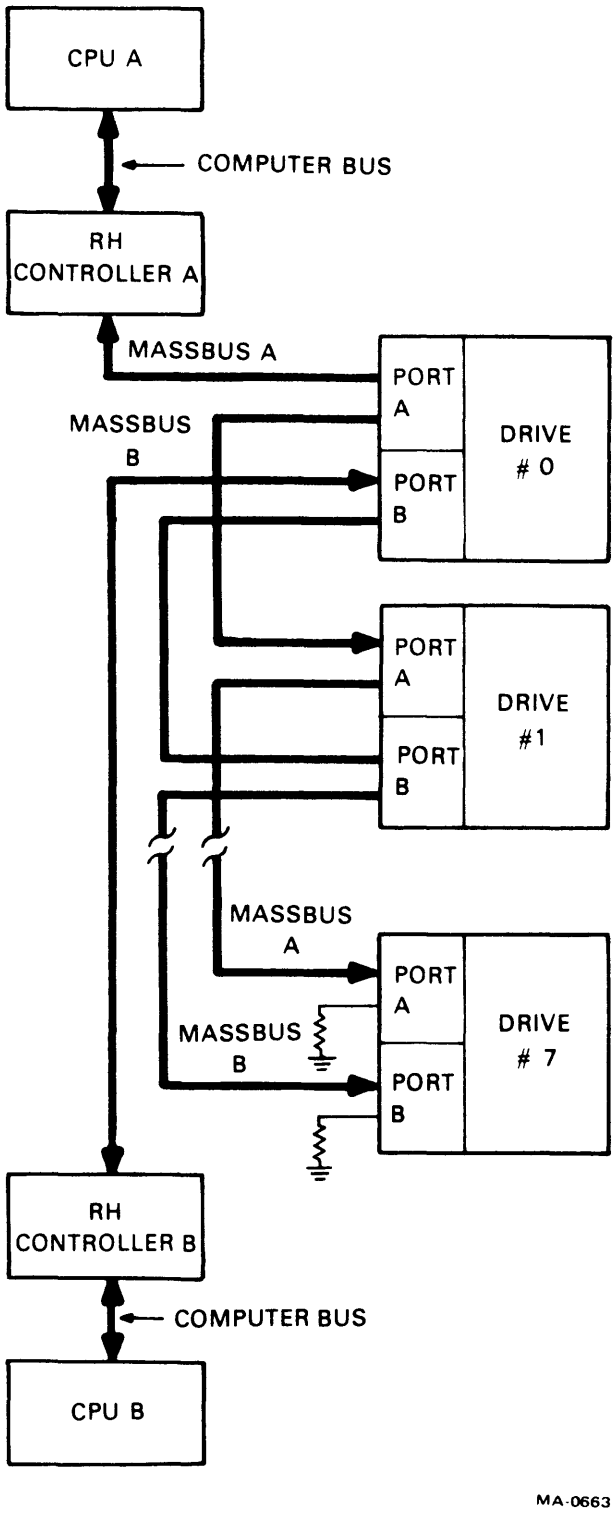


Figure 3-2 Dual-Port Configuration

The PORT SELECT switch (a 3-position switch located on the integrated backplane) establishes the operational condition of a dual-ported drive. The operational condition is set when the drive powers up from a not-ready state to the ready state. These dual-port conditions are as follows.

Locked on Port A – This condition exists if the switch is in position A when the drive becomes ready. In this condition, the drive is effectively single ported to port A. A request on port B does not result in a response from the drive.

Locked on Port B – This condition exists if the switch is in position B when the drive becomes ready. In this condition, the drive is effectively single ported to port B. A request on port A does not result in a response from the drive.

Programmable – This condition exists if the switch is in the A/B position when the drive becomes ready. In this condition, the drive is capable of responding to both port A and port B.

NOTE

Changing the position of the PORT SELECT switch after the drive becomes ready does not change the operational condition of the drive. To accomplish a change, the drive must be powered down, then re-started after a new condition has been selected by the position of the PORT SELECT switch. For single-controller operation, the switch is interlocked to controller A; manipulating the switch has no effect on the system.

In the programmable condition, the drive is always in one of three states. These states are:

- Seized on port A
- Seized on port B
- Neutral; not seized on either port.

Seized on Port A – In this state, the RH controller connected to port A can access all the drive registers. The RH controller connected to port B can read and write the attention summary (RMAS) register, but it cannot write any other register in the drive, and when reading any other register, it reads all 0-bits (with a 1 parity bit).

Seized on Port B – In this state, the RH controller connected to port B can access all the drive registers. The RH controller connected to port A can read and write the attention summary (RMAS) register, but it cannot write any other register, and when reading any other register, it reads all 0-bits (with a 1 parity bit).

Neutral State – In this state, the drive is not occupied by either port A or port B, but is equally available to either port on a first-come, first-served basis.

3.7.1 Dual-Port Register Bits

The following bits in the status (RMDS) register and control (RMCS1) register are used in dual-port operations.

Status Register

Volume Valid (VV) – The drive implements two volume valid bits: VV-A and VV-B. These are used to indicate when a disk pack has been changed; therefore, the program should not assume anything about the identity of the pack. VV-A is accessible to controller A only; VV-B is accessible to controller B only. The status of either bit is displayed in bit location 06. This bit can be examined by each controller and indicates the pack status for that controller. If controller A issues a pack acknowledge command, the VV bit for controller A is set. If controller B does not issue a pack acknowldge command, the VV bit for controller B is reset.

Drive Ready (DRY) – This bit (07) is reset by the controller that has seized the drive and is set on the completion of an operation. The DRY bit is the complement of the GO bit. If the second controller attempts to access the status register, the drive transmits all 0s (accompanied by the TRA pulse) and causes the DRY bit to appear reset (indicating device busy).

Drive Present (DPR) – This bit (08) is set for the controller that has seized the drive. If the second controller attempts to access the status register, the drive transmits all 0s (accompanied by the TRA pulse) and causes the DPR bit to appear reset. The DPR bit indicates that the drive is ready to communicate with the controller that has seized it.

Programmable (PGM) – This bit (09) is set when the drive is in the programmable condition and reset when the drive is locked on port A or locked on port B. During startup of the drive, the PGM bit is always set from the time power is applied until the medium-on-line (MOL) bit (12) sets.

Attention Summary (ATA) – This bit (15) consists of two ATA flip-flops: ATA-A and ATA-B. When controller A has seized the drive, the ATA-A bit is displayed in the ATA position of the status register; ATA-A is accessible to controller A only. When controller B has seized the drive, the ATA-B bit is displayed in this bit position; ATA-B is accessible to controller B only.

The ATA-A bit is always accessible to controller A, regardless of the setting of the PORT SELECT switch; similarly, the ATA-B bit is always accessible to controller B.

Reading the attention summary register by either controller produces the normal response. Even though controller A is selected, controller B can read the drive registers; however, 0s will be read back to controller B, indicating that this controller is not logically connected to the drive.

Control Register

Device Available (DVA) – This bit (11) appears set to the port that has seized the drive and reset to the other port. If the second controller attempts to access the status register, the drive transmits all 0s (accompanied by the TRA pulse). This causes the DVA bit to appear reset to the second controller.

3.7.2 Dual-Port Commands

The following commands are used in dual-port operations.

Pack Acknowledge – Sets volume valid (VV) bit in status register for the port that issued the pack acknowledge command.

Read-In Preset – Sets volume valid (VV) bit in status register for the port that issued the read-in preset command.

Release – With the drive seized on a port, a release command to that port causes the drive to release to the neutral state (if the other port has not requested use of the drive). If the other port has requested use of the drive, it switches to the other port rather than to neutral.

Initalize (INIT) line – The drive responds to an INIT issued separately from either port under the following conditions:

- An INIT issued by port A clears the port A ATA bit but does not affect the port B ATA bit. The converse is true for port B.
- If the drive is seized on port A and an INIT is initiated by port B, the INIT from port B is ignored. The converse is true for a drive seized on port B.
- When the drive is in the neutral state, an INIT from either port is accepted.

NOTE

In the above three conditions, an INIT clears all other registers and functions in a normal manner.

3.7.3 Dual-Port Unseized Status

The unseized state occurs when the drive is not connected to either controller and the PORT SELECT switch is in the A/B position.

The drive is switched to the alternate controller by the PORT SELECT switch, or, if in the unseized state, when:

1. The alternate controller writes into any register (including illegal registers).
2. The alternate controller reads the control register.
3. The alternate controller writes the ATA bit associated with a specific drive in the attention summary register.

As an example, if the drive is in the unseized state and controller A reads the control register, it seizes the drive.

3.7.4 Dual-Port Seized Status

Seized operation occurs when the drive is logically connected to one controller through a port.

NOTE

The drive is seized by controller A when the PORT SELECT switch is in A position, by controller B when the PORT SELECT switch is in B position, or by either controller when the PORT SELECT switch is in A/B position.

If the drive is seized by controller B, for example, writing any control register from controller A is ignored by the logic; however, the drive stores the fact that controller A has requested use of the drive in the port request flip-flop. Every request by controller A to read the control register (RMCS1) causes the drive to send 0s (accompanied by the TRA pulse) to the controller, indicating that the device is reserved by the other controller. Since the system operates with odd parity, the drive forces a 1 parity bit with each transmission of 0s though port A.

NOTE

If the drive is seized by controller B, the drive present (DPR) bit is set for controller B and reset for controller A. No special handling is required by the drive to process the DPR bit, because, if controller A requests a read of the control register (RMCS1), the drive sends all 0s (accompanied by the TRA pulse). The same situation occurs for the DRY bit (0s sent to controller A, indicating that the device is busy).

If, upon cycling up (indicated by setting the MOL bit), the drive determines that the PORT SELECT switch is in the A/B position, it sets the programmable (PGM) bit. Although the drive is occupied by one controller or the other, the status of the PGM bit is not physically altered.

3.7.5 Switching from Unseized to Seized Status

When the drive is not seized by either controller, it is equally available to both. If a controller reads a drive register (including illegal registers), the drive immediately connects to that controller for the duration of the register read operation. This constitutes a momentary transition.

If a controller writes any register (including illegal registers), the drive immediately connects to that controller and remains seized to that controller until a release command or a 1-second timeout is received.

3.7.6 Switching from Seized to Unseized Status

Upon recognizing the release command from controller B, the drive checks the port A request flip-flop to determine if the drive has been requested by controller A. If this flip-flop is not set, the logic returns to the unseized state (PGM is already set) and the DVA bit is set in the control register. If the flip-flop is set, controller A seizes the drive and bypasses the unseized state.

NOTE

The drive times out if it is occupied by a controller, and a release command is not received from that controller 1 second after termination of the last command transmitted to the drive. In this case, the drive returns to the unseized state. The 1-second timeout does not apply if the controller is selected by the position of the PORT SELECT switch.

For example, assume that controller B has seized the drive and controller A has requested it. When controller B issues the release command, the drive:

1. Sets the PGM bit in the drive status register
2. Maintains the DRP bit set to controller A
3. Sets the drive available (DVA) bit for controller A
4. Sets the ATA bit to controller A.

Upon recognizing the assertion of the ATTN line, controller A takes advantage of the interupt and initiates a command to the drive. With the drive seized by controller A, controller B receives the same response that controller A received when it requested the drive.

3.7.7 Dual-Port Register Access

Table 3-26 shows the controller action and the corresponding drive responses to each action. For example, if controller A attempts to read the control register and the drive is in the unseized state with the PORT SELECT switch in the A/B position, the drive immediately switches to controller A, sets the DVA bit, and reads the function code. If the drive is already seized by controller B, controller A reads all 0s.

Table 3-26 Register Accesses on Dual-Controller Operation

Action Performed by	Drive Response with Respect to Controller A		
Controller A	Drive in programmable state	Drive seized by A	Drive seized by B
Read the control register	Immediately switches to state A; reads the function code	DVA = 1; reads the function code	DVA = 0; reads all 0s
Write the control register	Immediately switches to state A; loads the function code	Loads the function code (switches to neutral if the function is release)	The function code is ignored.
Read the status register	Reads the status bits; PGM = 0; DPR = 1. No change of state	Reads the status bits; PGM = 1; DPR = 1.	Reads all 0s; PGM = 1; DPR = 0.
Read any other drive register	Reads the register; no change of state	Reads the register	Reads all 0s
Write any other drive register	Immediately switches to state A; loads the register	Loads the register	The word is ignored.

NOTES

1. **It is assumed that the PORT SELECT switch is in A/B position.**

2. **If controller A has seized the drive, and controller B requests it, the drive switches to controller B as soon as a release command is issued. When this occurs, the port B ATTN line is asserted.**

3.7.8 Error Handling in Dual-Port Operations

If an error condition exists, a drive clear command or INIT must be issued to the seized port before a Release command can be executed.

If the error is persistent, neither the drive clear command nor INIT clears the condition. For this condition, the 1-second timeout circuit releases the seized port.

Following release from a persistent error condition, the next port that seizes the drive sees the ATA and ERR bits set, indicating that the error condition occurred.

For example, assume that the drive is seized by controller A and a persistent error occurs that cannot be cleared by a drive clear or an INIT command.

If controller B has requested the drive, the drive eventually is seized by controller B through the 1-second timeout. The ATA bit is set, but it has a double meaning. Controller B determines that an error condition also exits by reading the status register and discovering the ERR bit set.

If controller B has not requested the drive, the drive reverts to the unseized state through the 1-second timeout. In this case, controller B receives no ATTN when the drive goes to the unseized state from controller A. Controller B is notified of the error condition when it attempts to seize the drive (by writing the drive registers).

NOTE

In the event of a persistent error, the software can clear the ATTN bit by writing a 1 into it.

Subsequent addressing of the attention summary register by the controller does not cause the ATTN bit (belonging to the drive with the persistent error) to be asserted. Any attempt to write on any of the other drive registers, however, causes the ATTN line to be asserted.

CHAPTER 4
TECHNICAL DESCRIPTION

4.1 INTRODUCTION

This chapter provides a technical description of the RM02/03 adapter. Detailed block diagrams are used to illustrate the operation of various circuit elements. Command execution is described in detail with the aid of command flowcharts. The entire chapter is organized to be used along with the field maintenance print set. To accomplish this, every block diagram uses numerous references to pages of actual circuit schematics. For example, "Command Sequencer Schematic page 7" is abbreviated CS7, etc. Block diagrams, flowcharts, timing diagrams, PLA, and PROM maps are all found in the latest RM02 or RM03 Field Maintenance Print Set (MP-00456 or MP-00350, respectively).

4.2 ADAPTER PHYSICAL DESCRIPTION

The RM02/03 adapter consists of a backplane and several modules that plug into this backplane. The location of the modules relative to the backplane is shown in Figure 4-1. (The various cables and jumpers on the backplane are described in the *RM02/03 Disk Subsystem User's Manual.)*

There are six different types of modules in the adapter. Two of these, the port A Massbus transceiver board (M5922) and the port B Massbus transceiver board (M5923), are used in pairs. The other four modules, the control interface board (M7686), the data sequencer board (M7685), the command sequencer board (M7684), and the drive interface (M7687) board, are used only once in an adapter. Each of these boards is briefly described in the next several paragraphs.

4.2.1 Control Interface (IF)

The control interface module is used primarily for asynchronous Massbus handshaking and register transfer control. It also contains several registers: the RMAS, RMER1, RMER2, RMCS1, RMDT, RMDS, RMOF, and RMHR registers.

4.2.2 Data Sequencer (DS)

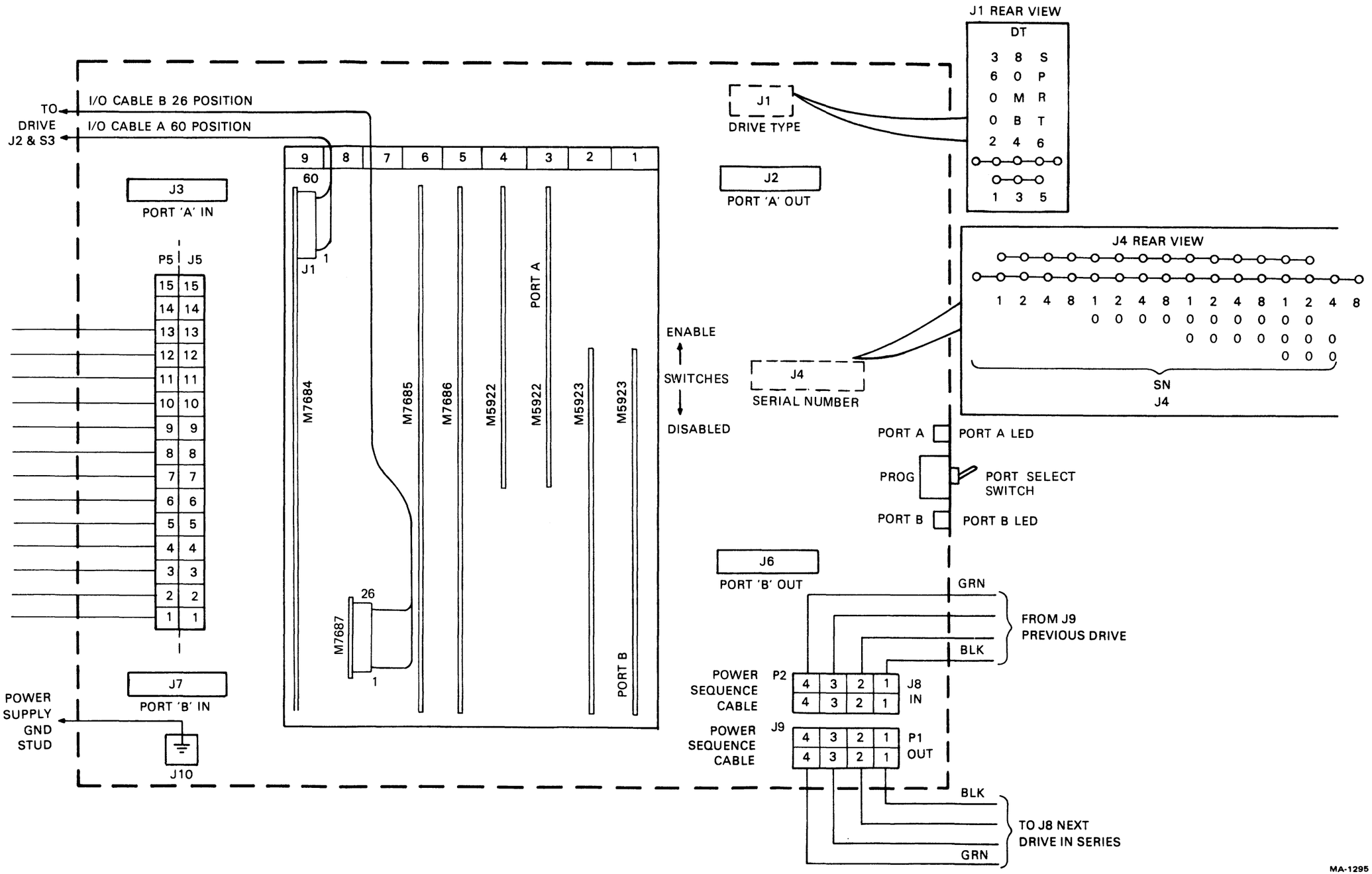
The data sequencer module controls the flow of data being read from, or written onto, the disk. The logic on this module includes bit- and word-clock generation; error correcting code and cycle redundancy check logic; and the RMDC, RMEC1, RMEC2, and RMDA registers.

4.2.3 Command Sequences (CS)

The command sequencing logic on the command sequencer board handles all command execution. Read/write sequencing also occurs on this board, and the CS module contains the differential drivers and controls to handle data on cable A, which goes to the drive itself. The registers RMMR1, RMMR2, RMSN, and RMLA are located on the CS.

4.2.4 Drive Interface

The drive interface board is used primarily as an interface for information on the adapter-drive cable B, including read and write clocks and the data being transmitted.



MA-1295

Figure 4-1 Adapter Backplane

4.2.5 Port A Massbus Transceiver

As stated above, there are two port A transceiver modules in the adapter. One of these boards handles asynchronous information – it transmits control signals between the Massbus and the IF module. The other board handles synchronous information – it handles data between the Massbus and the DS board.

4.2.6 Port B Massbus Transceiver

The two port B transceiver modules function exactly as the port A modules, except that they only function when the drive is in port B mode.

4.3 POWER-UP SEQUENCE

In a multidrive installation, the power sequence cable that is connected between the backplanes carries three signals used to control the power-up sequence. The power sequence cable is described in Paragraph 2.5 of this manual. As described in Chapter 2, the three power sequence cable signals are grant-in, grant-out, and start in progress (SIP).

Figure 4-2 shows a typical system configuration. The grant line, which handles the grant-in and grant-out signals, is connected serially through each drive. The SIP line is common to all the drives. The drive physically closest to the controller has pin 1 of J8 on the backplane grounded by a jumper plug (Figure 2-6). Thus, the grant signal initially appears low to all the drives on the power sequence cable.

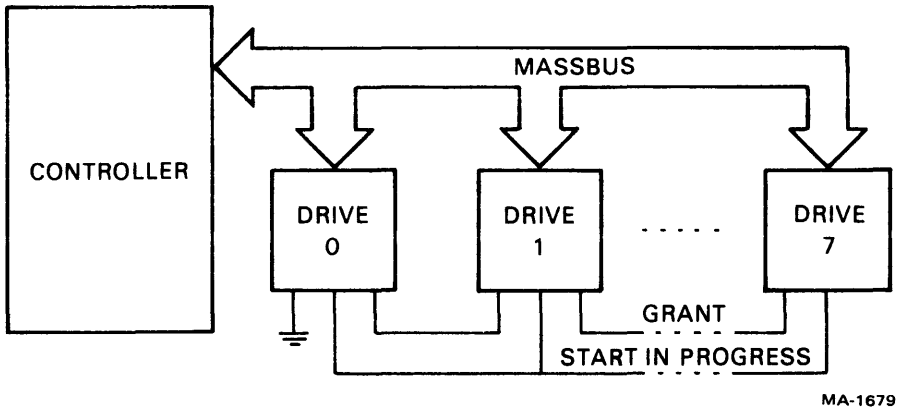


Figure 4-2 Typical Power-Up Configuration

The presence of a low grant signal is one of the two prerequisites for a drive to be able to start up. The other prerequisite (with respect to the power sequence cable) is that the SIP line be high. Normally, it is high, but when a drive begins its power-up sequence, it pulls the SIP line low. A low SIP line prevents all the other drives from starting up.

Figure 4-3 shows the flow diagram for the power-up sequence and Figure 4-4 depicts the functional block diagram. The sequence of events in the power-up sequence is as follows.

1. With the LOCAL/REMOTE switch of the A2–A10 board in the REMOTE position, pressing the front panel START switch causes the start enable line on cable B to assert.

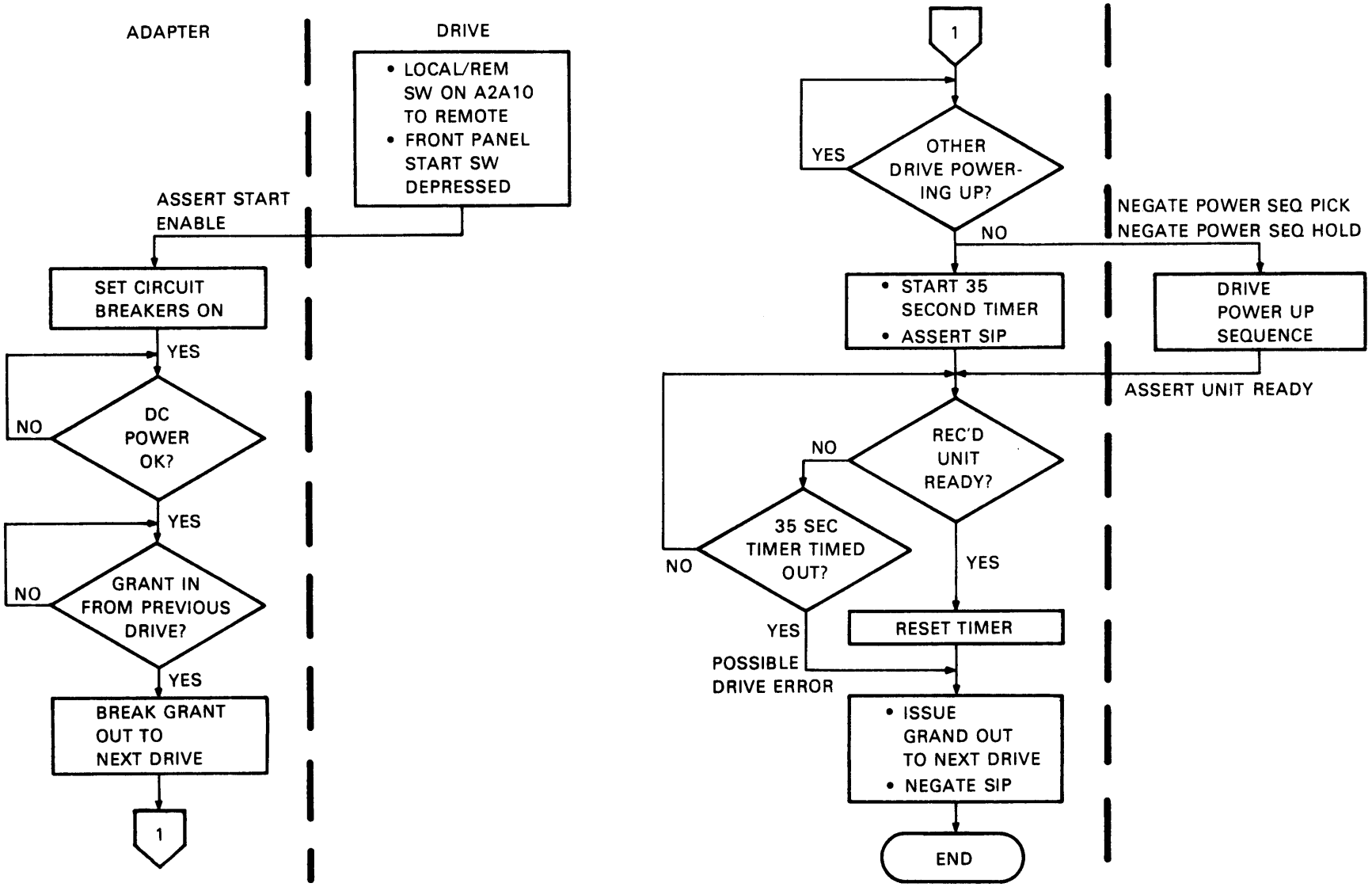


Figure 4-3 Power-Up Sequence Flow Diagram

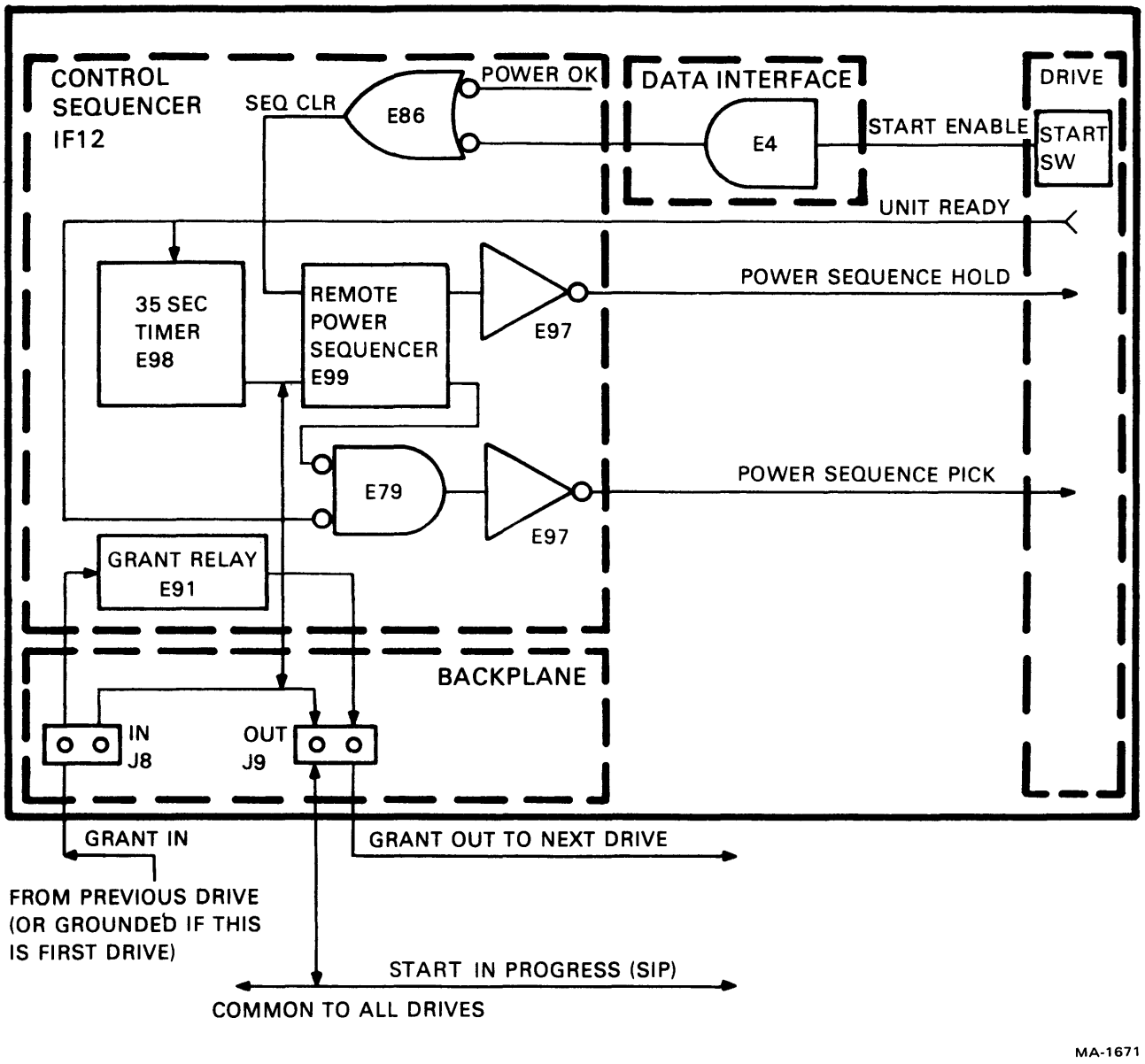


Figure 4-4 Power-Up Sequence
Functional Block Diagram

2. In the adapter, the following conditions are needed to start the sequence:

   a. Circuit breakers CB1 and CB2 set to ON

   b. DC power OK (from CS4)

   c. A grant-in signal from the drive closer to the controller than the drive trying to power up. If this is the first drive in the string, grant-in will always be present because the line is grounded at the backplane.

3. The sequence starts by energizing E91, which breaks the grant line to the other drives.

4. The drive attempting to start tests the SIP line to see if another drive further up the line is in its power-up sequence. If it is, the drive attempting to start will wait for the other to finish its sequence.

5. If no other drive is powering up, this drive initiates the following four actions:

   a. Negates power sequence pick line to drive
   b. Negates power sequence hold line to drive
   c. Starts the 35-second timer
   d. Asserts the SIP line to prevent other drives from trying to power up.

6. When the drive has completed its power-up cycle, it asserts the unit ready line to indicate that the pack is up to speed, the heads are loaded, and no faults exist in the drive.

7. During the time the drive is powering up, the drive constantly tests the 35-second timer for a timeout. If the timer times out before receiving the unit ready from the drive, it assumes that the drive did not fully complete the power-up sequence.

8. At the end of the 35 seconds or upon receipt of the unit ready signal, the adapter issues the grant-out to the next drive and negates the SIP line.

When unit ready is asserted, the drive has finished its power-up sequence, and is considered "powered up." If the drive did not start, for some reason, it sends grant-out to the other drives to allow them a chance to start. It continues sending grant-out until the fault that prevented its startup is cleared. Then, a new power-up sequence commences in the drive.

After a drive has been powered up and is running, it may be stopped to change a disk pack by pressing the front panel START switch. The following action occurs.

1. The start enable line is negated and both pick and hold lines are asserted.

2. The start relay de-energizes but the grant-out signal is still passed along to the next drive.

3. After the new pack is loaded and the START switch is pressed again, the drive powers up in the normal manner.

NOTE

Even though this drive is powered down, other drives further out on the string can power up because the grant line is passed right through the powered-down drive on the de-energized contacts of E91.

4.4 INITIALIZE SEQUENCE

The initialize sequence starts with the receipt of a Massbus INIT signal from either port A or B. This sequence is used to condition both the adapter and drive circuits to a known reset state. The functional block diagram for the initialize command is shown in Figure 4-5.

The Massbus INIT signal (whether coming from port A or B) clears the ATA bit in the attention summary register in the IF module. In the CS module, it is converted to the MBA clear signal which performs the following:

1. Clears the enable search latch
2. Sets the on latch
3. Clears bit 00 of maintenance register 2 (RMMR2)
4. Clears ECC pattern register (RMEC2)
5. Clears both error registers (RMER1 and RMER2)
6. Clears any drive faults (if the fault condition has been removed).

It is important to note that either the power OK condition (occurring at power-up) or a drive clear command also generates the MBB clear signal and performs the same functions as the Massbus INIT.

4.5 DEVICE SELECTION

The three device select lines (DS0–DS2) of the control bus contain the unique code for one of the eight possible drives that can be connected via the Massbus to the controller. Each drive has a coded logic plus numbers 0–7 that insert into a socket on the front panel. A code representing the plug's number is sent over cable A through the CS module and is applied to the drive address comparator on the IF module. If both addresses compare, a signal is sent to the handshake control circuits to allow the handshake sequence to commence.

Figure 4-6 contains the functional block diagram for the device selection circuits.

4.6 REGISTER SELECTION

The five register select lines (RS0–RS4) in the Massbus contain the addresses that select the 16 registers in the RM02/03 adapter. Figure 4-7 is a block diagram showing the register selection circuits, indicatting the location of the registers.

Paragraph 3.3 of this manual provides a summary of the registers, including a brief description of each bit assignment. Table 4-1 gives the location of each register as it appears in the *RM02/03 Field Maintenance Print Set.*

Table 4-1 Register Locations in Print Set

Mnemonic	Page	Mnemonic	Page
RMAS	IF7	RMEC2	DS8
RMCS1	IF8	RMEC1	DS9
RMOF	IF8	RMDA	DS11
RMDS	IF9	RMDC	DS12
RMDT	IF9		
RMER1	IF10		
RMER2	IF11	RMLA	CS7
RMHR	IF	RMSN	CS7
		RMMR1	CS8
		RMMR2	CS9

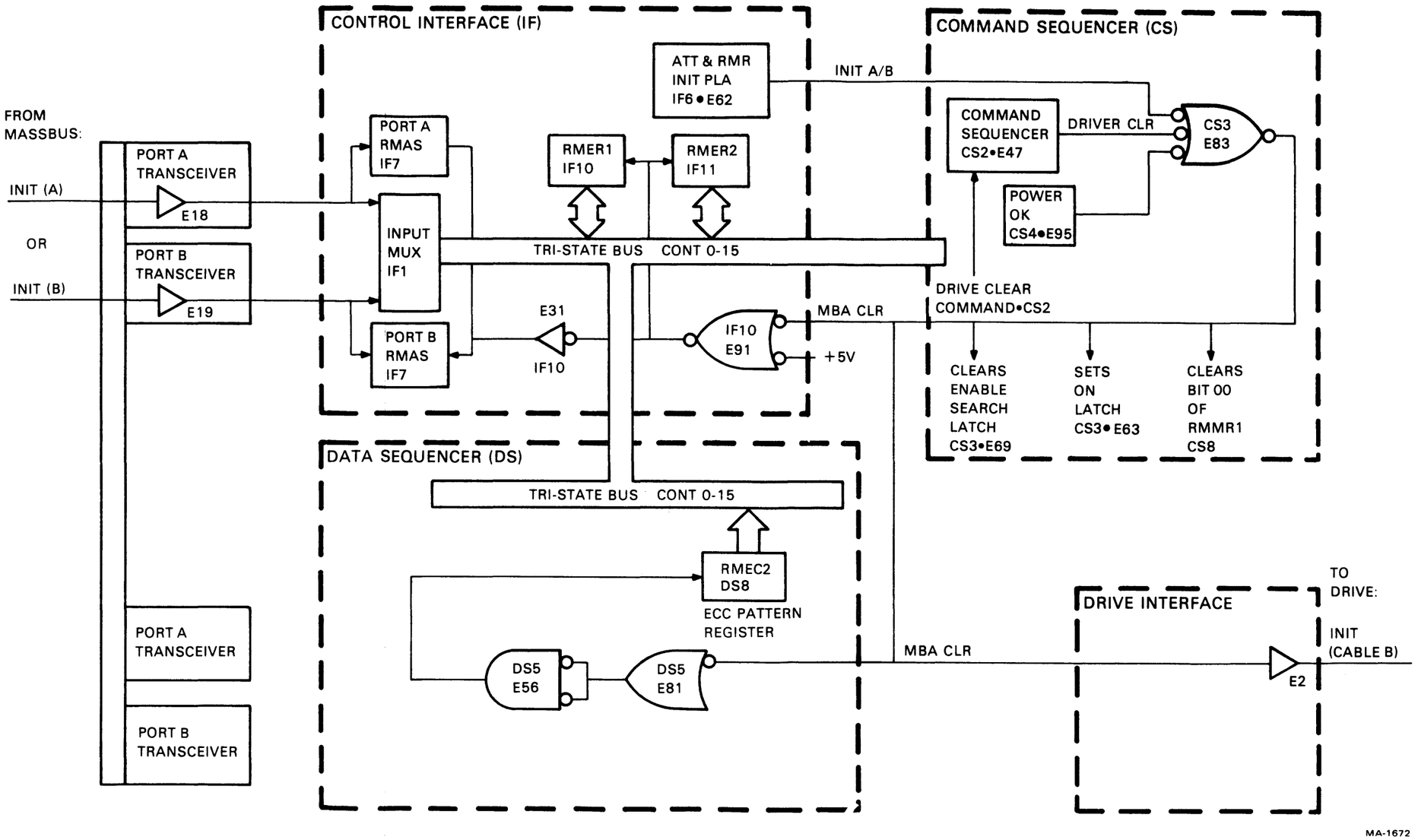


Figure 4-5 Initialize Sequence
Functional Block Diagram

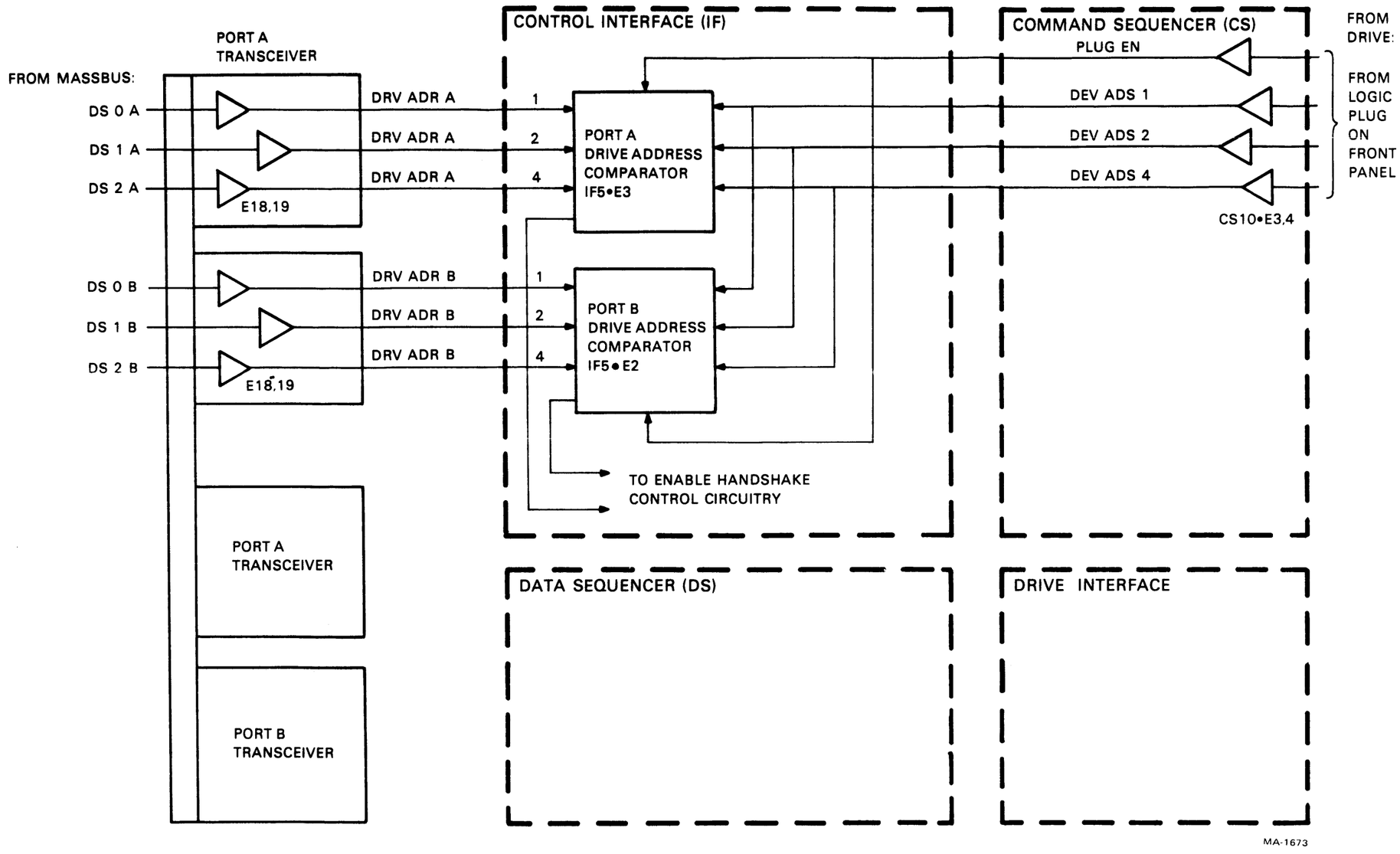


Figure 4-6 Drive Selection
Functional Block Diagram

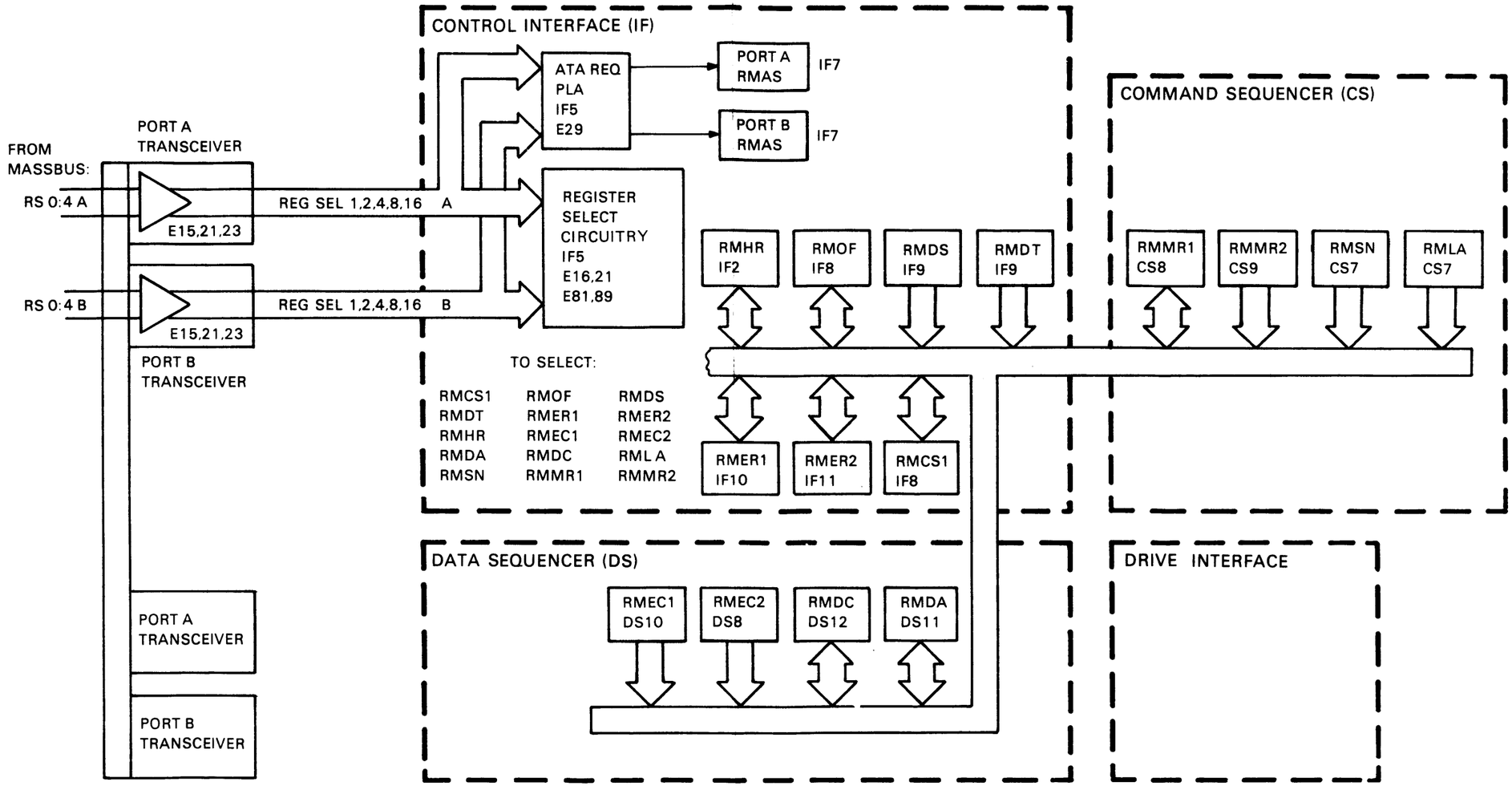


Figure 4-7 Register Selection
Functional Block Diagram

4.7 HANDSHAKE CONTROL

The functional block diagram of the handshake control circuits is shown in Figure 4-8. These circuits establish the timing required whenever a register write or read is performed.

Prior to the actual handshake sequence, the device selection circuits have determined that this is the correct drive and the port selection circuits have established the port through which the register information is to pass.

The register information is routed to and from the drive on the control bus which has 16 data bits and a parity bit. The control bus functional block diagram is shown in Figure 4-9.

4.7.1 Register Write

When the controller writes information into a drive, the following sequence occurs.

1. The drive is selected using the device select lines (Figure 4-6).
2. The register that the information is to be written into is selected (Figure 4-7).
3. The information is placed on the 16 lines of the control bus. The controller asserts the CTOD line.
4. The controller asserts the demand (DEM) line (Figure 4-8) and initiates the handshake. The timing for this register write is shown in Figure 4-10.
5. The grey code counter accesses a new location in the handshake PROM every cycle of the system clock.
6. The handshake takes 6 clock cycles and cannot be interrupted during this time. The other port is inhibited by the too-late signal from the PROM.
7. The LD BUF signal loads the information on the 16 control bus lines into the control line buffer as shown in Figure 4-9.
8. The ASY WRT signal loads the information in the control line buffer into the selected register. If the control and status register 1 was written, the GO bit sets on the next clock cycle. (This would be if a command code is being written.)
9. The TRA signal is generated at the end of the handshake to indicate to the controller that the sequence be completed.
10. When the controller receives TRA from the drive, it drops the DEM.
11. When the disk drive sees that the controller has dropped DEM, the drive drops TRA. The handshake sequence is complete.

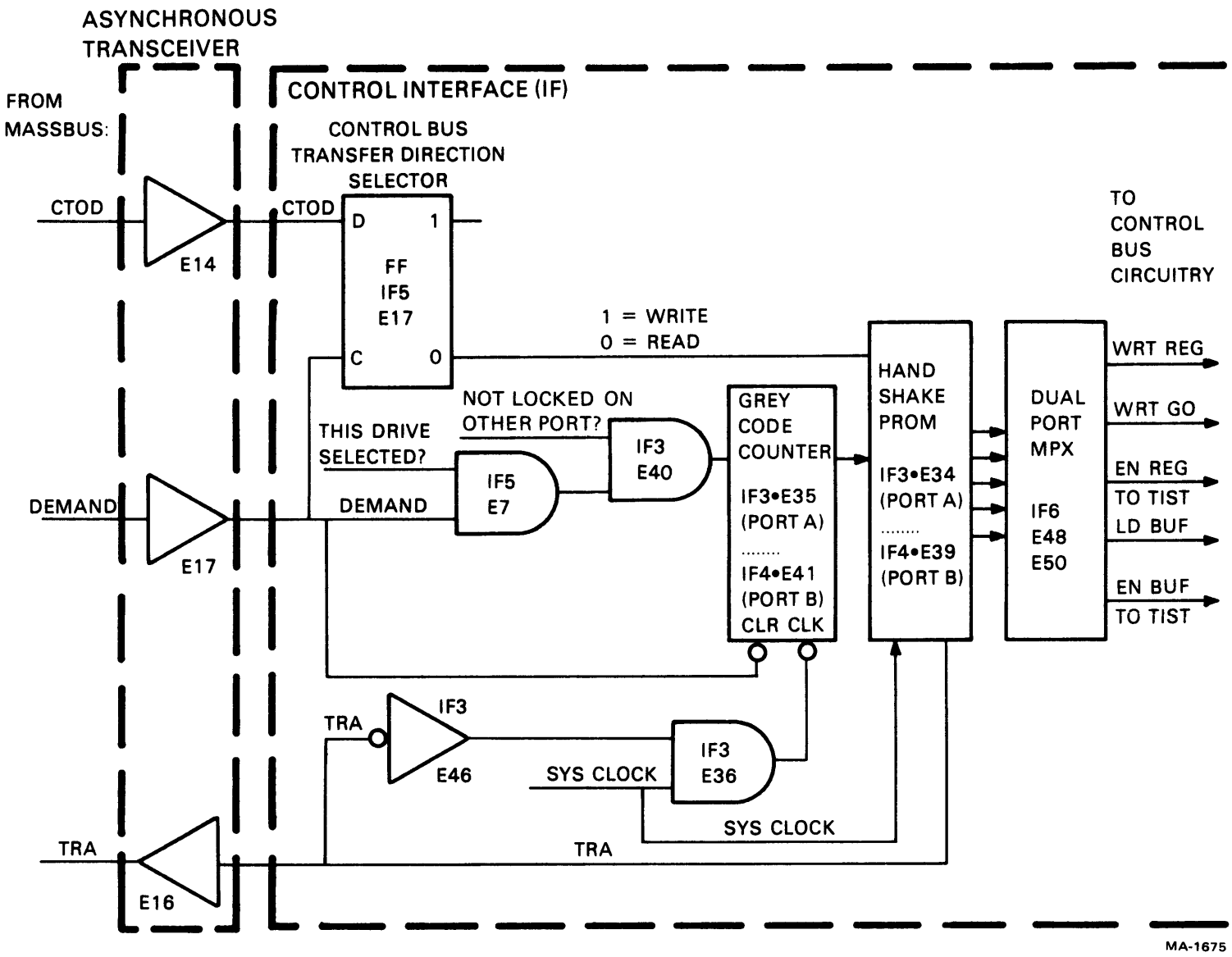


Figure 4-8 Handshake Control Functional Block Diagram

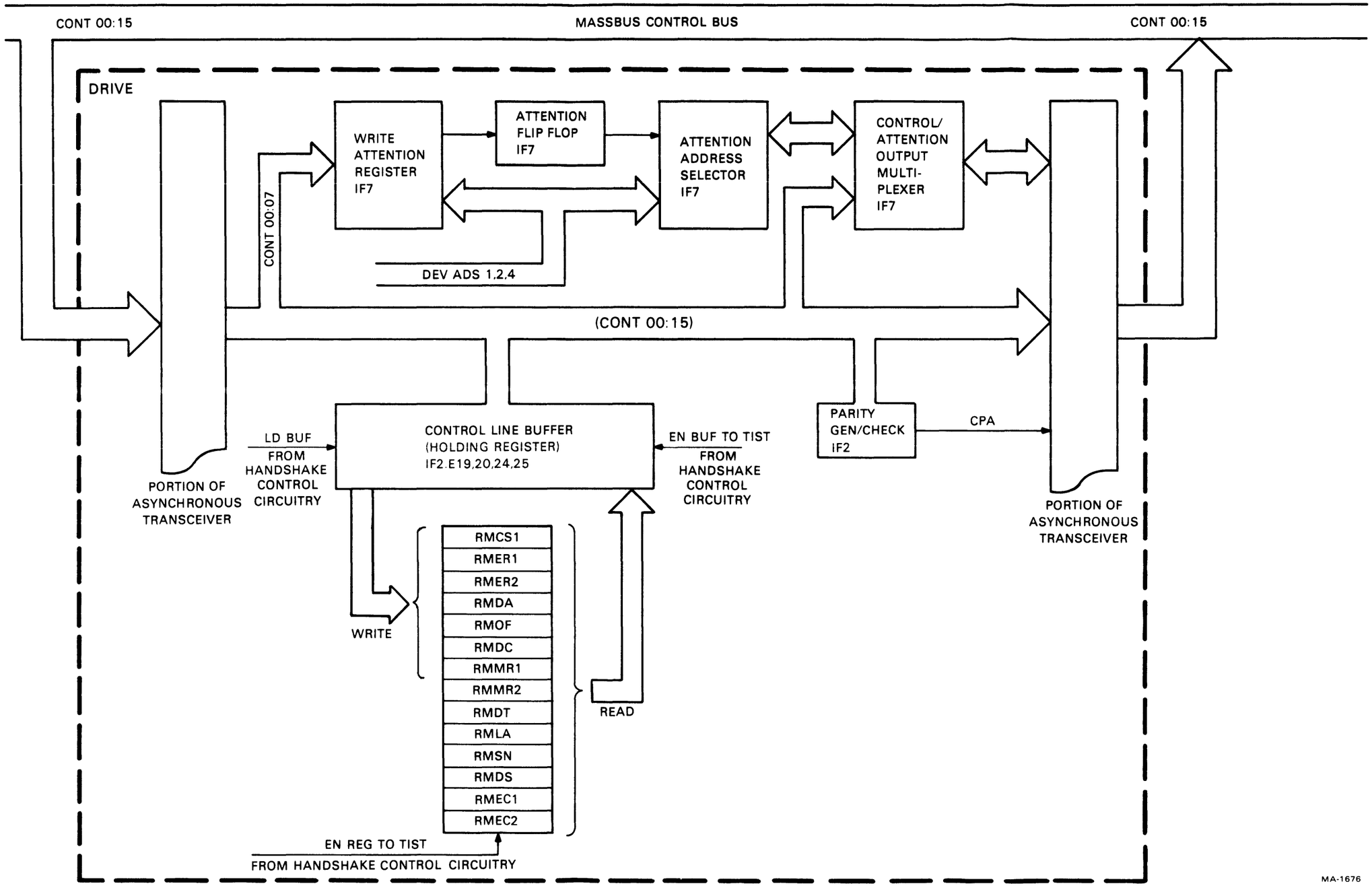


Figure 4-9 Control Bus Functional Block Diagram

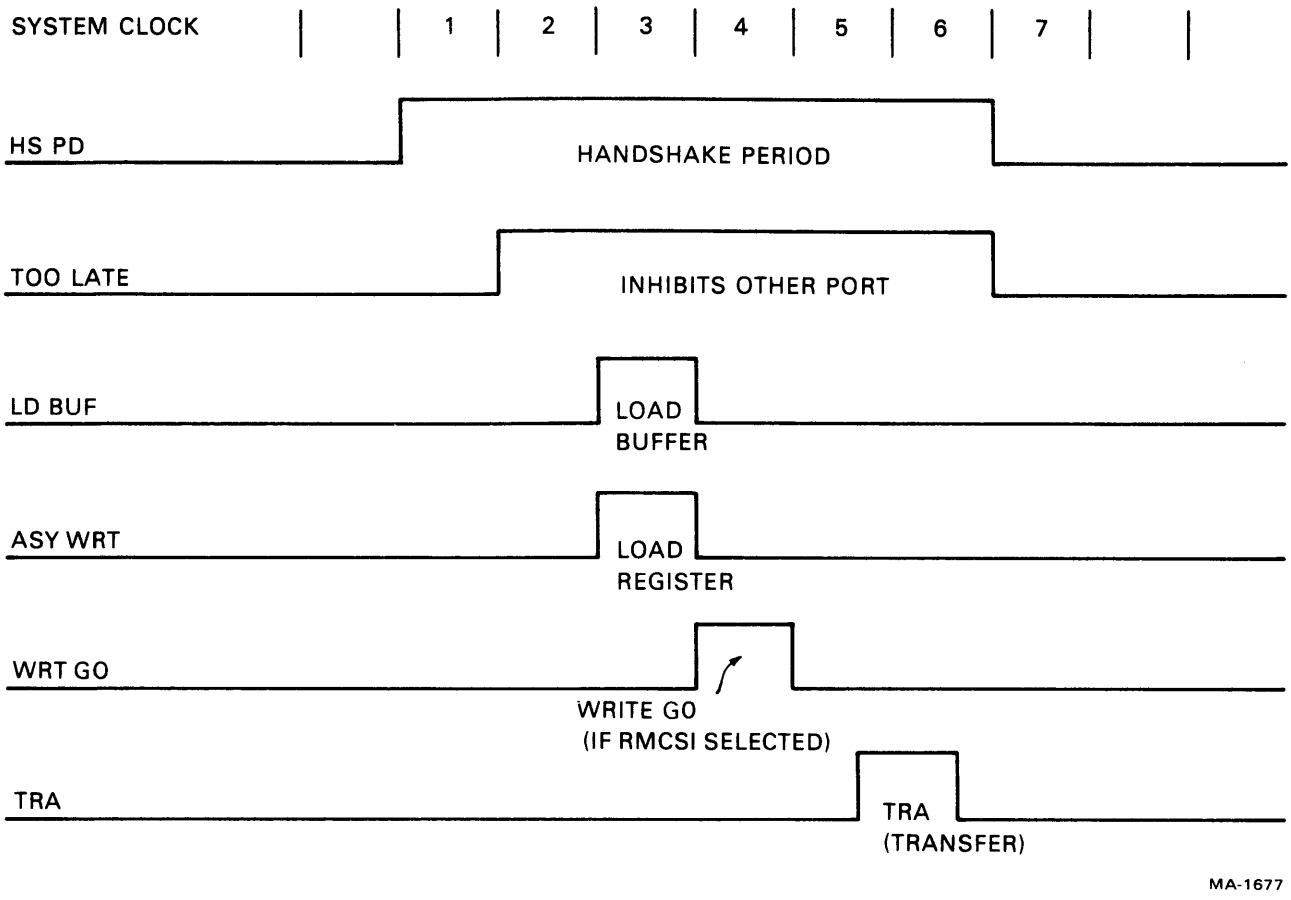


Figure 4-10 Handshake Timing for Register Write

4.7.2 Register Read

When the controller reads information from a drive, the following sequence occurs.

1. The drive is selected (Figure 4-6), the register is selected (Figure 4-7), the CTOD line is negated, and the DEM line is asserted.

2. Again, the handshake control circuits perform the required timing but now a different portion of the PROM is accessed by the counter. The timing for this read sequence is shown in Figure 4-11.

3. The information in the register is placed on the tri-state bus lines that are common to all registers and then loaded into the control bus buffer by the LD BUF signal.

4. This information is then placed on the 16 lines to the controller.

5. The drive asserts the TRA line to indicate that the sequence can be finished.

6. When the controller receives TRA from the drive, it drops the DEM line.

7. When the drive sees that the controller has dropped DEM, the drive drops TRA. The handshake sequence is complete.

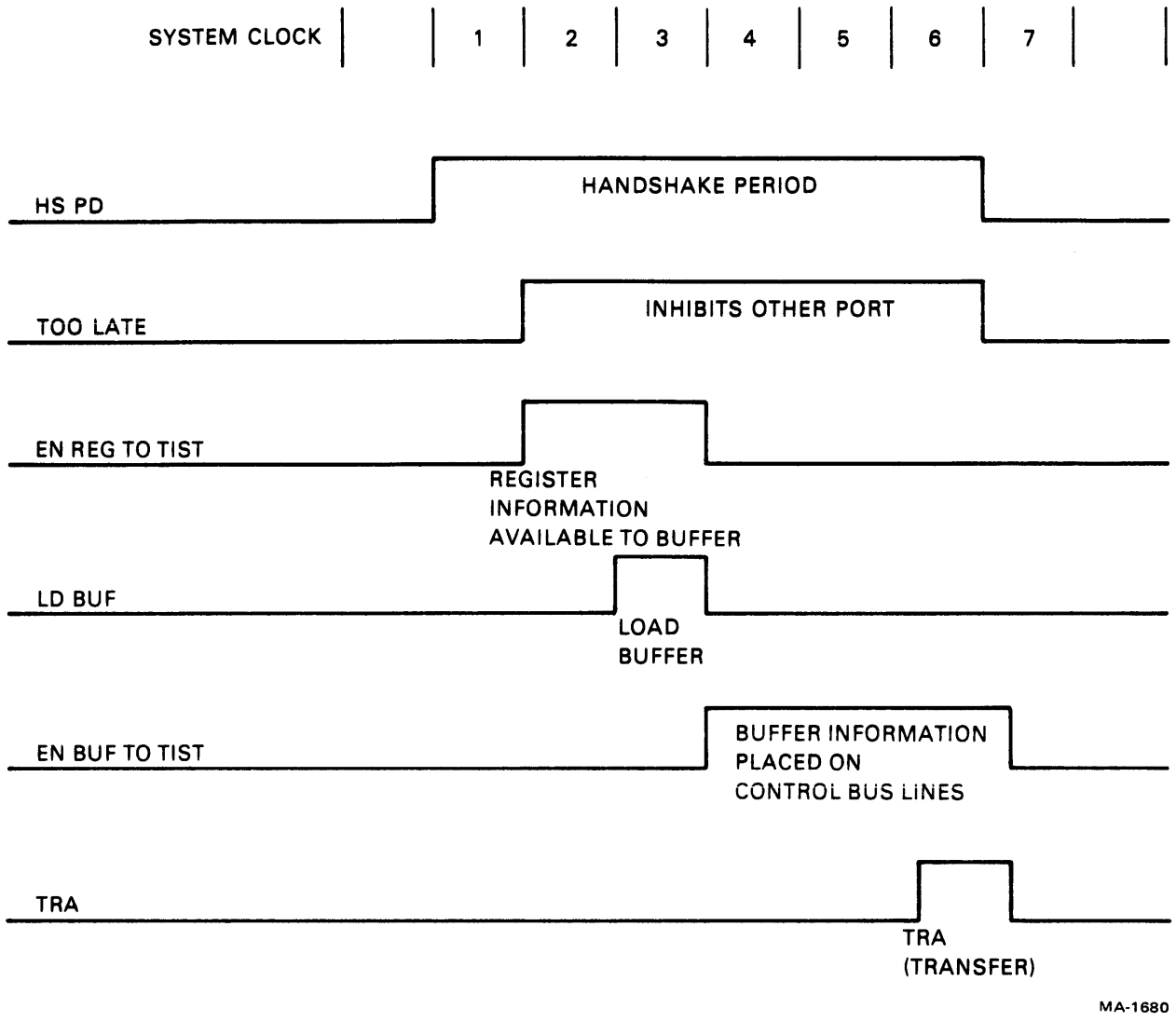


Figure 4-11 Handshake Timing for Register Read

4.8 DETAILED BLOCK DIAGRAM

A detailed block diagram for the RM02/03 adapter is presented in Figure 4-12. This illustration is used throughout this chapter to describe the major functional elements used on each module.

4.8.1 Port Transceivers

Two port A transceivers (M5922) are used for single-port operation. They must be inserted into specific slot locations on the RM02/03 adapter backplane as shown in Figure 4-1. When correctly installed, one port A transceiver receives and transmits all the asynchronous control signals between the Massbus and control interface module via the A control bus shown in Figure 4-12. The second port A transceiver receives and transmits all the synchronous data information between the Massbus and data sequencer module. For dual-port operation, two port B transceivers (M5923) must also be inserted into their specific locations so that all four transceiver positions are occupied.

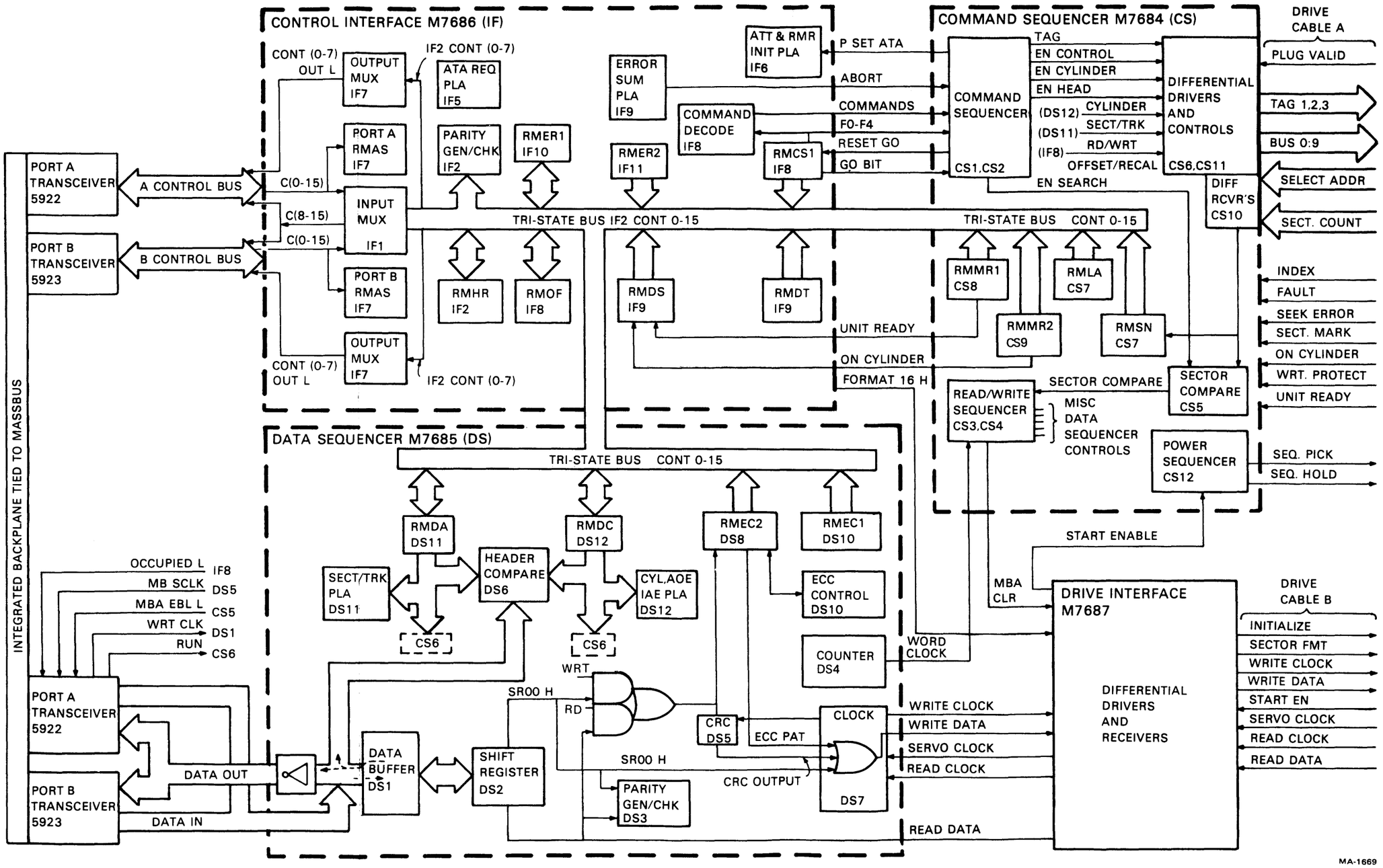


Figure 4-12 RM02/03 Adapter Block Diagram

The control information on the Massbus enters through the port transceivers into the input multiplexer (IF1). This 17-bit-wide multiplexer selects either control bus A or B for its input. If port A is selected, its 16 control bits and parity bit are placed onto the tri-state bus (IF2 CONT 0–15). A parity check is made on this control data by the parity generator and checker circuit (IF2). If the control data on the bus fails the odd prity test, the parity circuit will set the parity error (PAR) in error register 1.

4.8.2 RM02/03 Adapter Registers

From the tri-state control bus, access can be gained to any of the 16 adapter registers spread over all 3 modules.

Attention Summary Register (RMAS) – The RMAS register (IF7) is not like all the other addressable registers. It is actually composed of up to eight flip-flops with each bit physically located in one of eight possible drives that can be connected to a single controller. Each flip-flop corresponds to its drive unit number, and they are arranged in a parallel mode. The attention summary register allows the program to examine the attention status (ATA) of all drives with a single register read operation.

Holding Register (RMHR) – This is an addressable register with no drive function. It is used only by diagnostic software. When writing into this register, all bits remain unchanged and new information is lost. When reading this register (or any illegal register), the complement of the register contents is read. Whenever writing any legal register, this holding register is concurrently written.

Offset Register (RMOF) – The RMOF register (IF8) is used to hold offset information necessary to move the heads 200 microinches off track centerline. This register must be loaded prior to issuing an offset command.

Error Register 1 (RMER1) – The RMER1 register (IF10) contains mostly error status indicators for the RM02/03 adapter operations.

Error Register 2 (RMER2) – The RMER2 register (IF11) contains error information on the status and performance of the drive.

Control Register (RMCS1) – The RMCS1 register (IF8) is used by both the RM02/03 adapter and the controller to store the disk commands and operational status. Setting the GO bit causes the drive to recognize the function code in the register. However, actual command execution only begins after the RUN line is asserted by a data transfer command.

Drive Status Register (RMDS) – The RMDS register (IF9) contains the operational status indicators for the selected drive.

Drive Type Register (RMDT) – The RMDT register (IF9) allows the program to distinguish between different kinds of drives.

Maintenance Register 1 (RMMR1) – The RMMR1 register (CS8) is used to perform maintenance operations. This register has two distinct 16-bit sections: a read-only section and a write-only section. The write-only section provides a method to control the logic functions of the RM02/03 adapter. The read-only section permits monitoring of these operations.

Maintenance Register 2 (RMMR2) – The RMMR2 register (CS9) is used in conjunction with the RMMR1 register to configure the RM02/03 adapter in the maintenance mode.

Serial Number Register (RMSN) – The RMSN register (CS7) contains the lowest four digits of the drive serial number. It provides the program with a means to distinguish between different drives connected to the same controller. This register consists of up to 16 jumper wires on the RM02/03 adapter backplane.

Look Ahead Register (RMLA) - The RMLA register (CS7) contains the count of the sector that is currently positioned under the heads. The count value is reset to 0 by the index pulse and incremented by 1 at each sector pulse.

Disk Address Register (RMDA) - The RMDA register (DS11) is used to address the sector and track on the disk to or from which a transfer is desired. The register content is incremented by 1 each time a data sector block is transferred.

Desired Cylinder Register (RMDC) - The RMDC register (DS12) contains the address of the cylinder to which the drive positioner moves the heads for a seek or search.

ECC Position Register (RMEC1) - The RMEC1 register (DS10) contains the position of the ECC error burst.

ECC Pattern Register (RMEC2) - The RMEC2 register (DS8) contains the correction pattern that the program can use to replace the incorrect data (in memory) with the correct data.

4.8.3 RM02/03 Adapter PLAs

The RM02/03 adapter uses five programmable logic arrays (PLAs) to perform signal testing and error decoding operations. Each PLA has 16 input lines (variables) and 8 output lines (functions). Inside each PLA is a matrix of crosspoints that acts as an input decoder. The particular crosspoint pattern used has been selectively connected by a factory masking procedure. Each device output bit is the product of a match between the PLA input variables with the combinational logic in the input decoder.

In a PLA, some combinations of inputs may have no effect on the output, and some groups of input combinations may generate the same output. These functions are different from a read-only memory (ROM) where all combinations of inputs cause an output to appear.

Appendix A contains more detailed information on programmable logic arrays.

4.8.3.1 ATA Control/Request PLA (IF5) - This PLA is used to control the port A or B attention summary registers, and to set the port request flip-flops. Each port always has access to its RMAS register. The status of the RMAS register is read through an 8-bit-wide output multiplexer (IF7) onto the port control bus via its output lines CONT (0–7) OUT L. If port A is requested, the ATA control/request PLA (IF5) asserts the SET CONT REQ A H line shown in Figure 4-13. To select the port A RMAS register, the PLA asserts RMAS A H. When writing the port A RMAS register, the PLA asserts the WRT ATA DEC A H signal. To read the register, it asserts the TRANS A H signal.

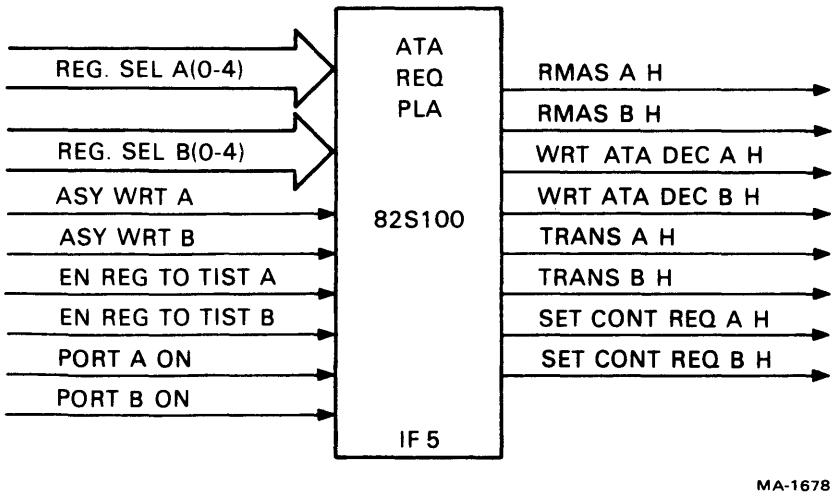


Figure 4-13 Attention Control/Request PLA

4.8.3.2 Error Sum PLA (IF9) - The error sum PLA is used to monitor the error conditions that can occur in the RM02/03 adapter or disk drive.

There are four signals generated by this PLA. A composite error signal is produced whenever one or more error conditions are detected at its input. An exception error signal is produced and sent to the Massbus to notify it that an error condition has occurred during a data command. Any class B error (catastrophic error) causes an abort signal to be asserted. This abort condition terminates any non-data transfer commands immediately and resets the GO bit.

If an abort condition occurs during a data transfer command, the PLA asserts the ABORT L line. This signal causes an end-of-block (EBL) pulse to be generated to end the data sequence.

4.8.3.3 ATA, RMR, INIT PLA (IF6) - This PLA is used to generate the attention conditions, to initialize registers, and to detect when a register write attempt was made illegally during a command operation. The RMR SET signal out of this PLA indicates a register modification refused (RMR) condition. If bit 2 (RMR) of error register 1 is set, it means that an illegal attempt was made to write into a register before the completion of a command operation.

The attention bit in the RMAS register and RMDS register is set when any of several attention conditions are detected by the PLA. For instance, ATA is set for any error condition in the error registers, or if the MOL bit changes state. It is also set at the completion of a seek, search, recalibrate, offset, or return-to-centerline command.

4.8.3.4 Sector/Track PLA (DS11) - This PLA is used in conjunction with the RMDA register to monitor when several disk address milestones or limits are reached. At its input are the five track bits, the five sector bits, and a format bit. From this input information, the PLA indicates when the last sector is reached (sector wraparound), when the last track is reached (track address wraparound), when the last sector and last track are reached, and also whether any invalid sector or track is found in the RMDA register.

4.8.3.5 CYL/AOE/IAE PLA (DS12) - This PLA monitors the cylinder bits in the RMDC register along with several other related conditions. From this input information, the PLA produces the following output conditions. It indicates when the maximum cylinder on the disk is reached, and also when the last address on the pack is reached. It also provides two error conditions. It sets the invalid address error (IAE) and the address overflow error (AOE).

4.8.4 Command Sequencer (CS1, CS2)
The command sequencer controls most of the command operations of the RM02/03 adapter. During data handling commands, the read/write sequencer controls the data transfer portion of these functions.

The command sequencer is illustrated in Figure 4-14. It consists of a program counter and four PROMs having 256 memory locations each. The counter is used to step through the sequence and to address the PROMs. The counter is continuously forced to 0 whenever the GO bit in the control register is cleared.

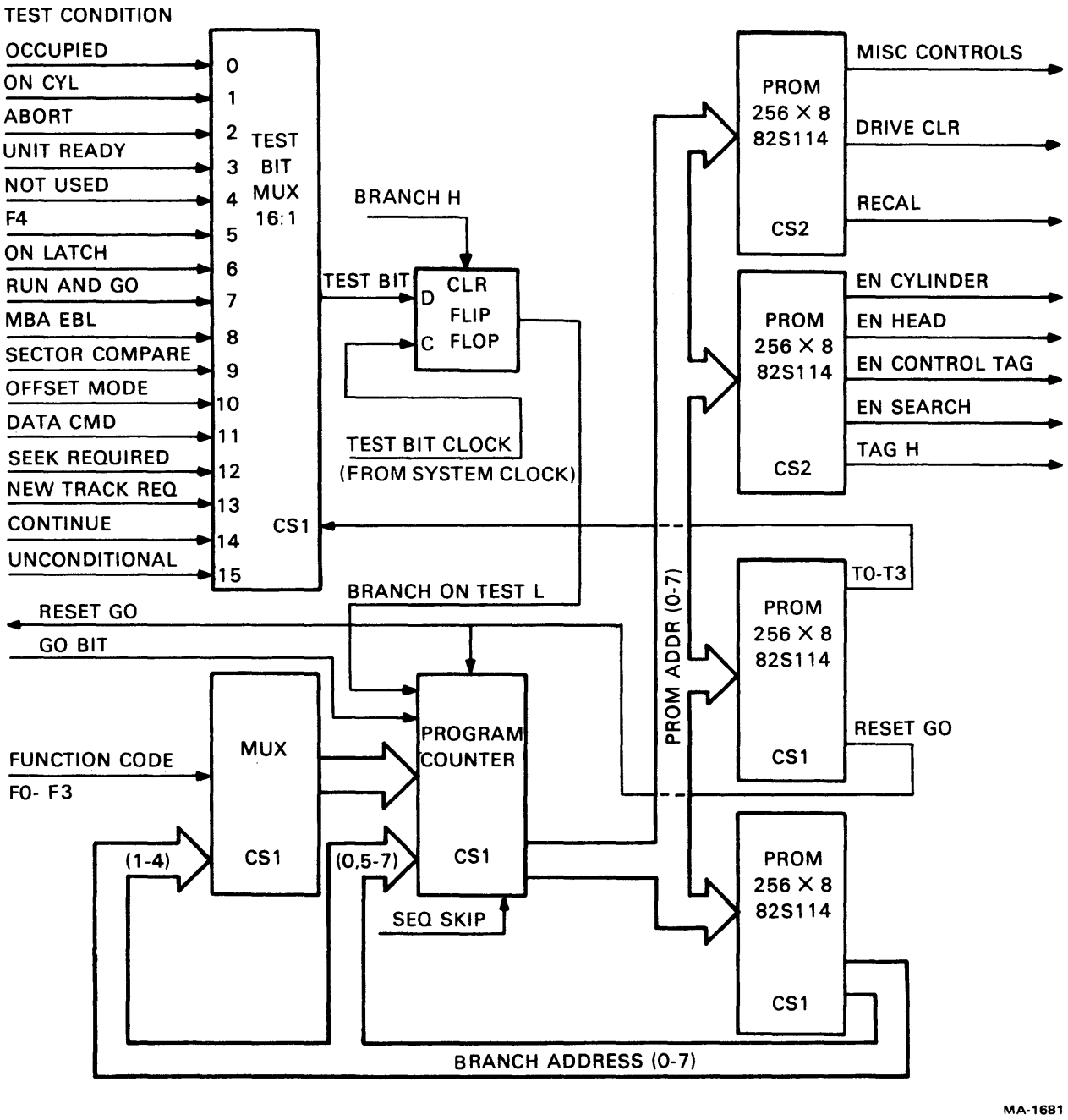


Figure 4-14 Command Sequencer
Block Diagram

Feeding the program counter with address information is a branch multiplexer that can select either the lower 4 bits of the function code or 4 bits of a branch address location. Upon receiving a branch request condition from the PROMs, the program counter loads a new branch address which forces the PROMs to a new memory location. This new branch address is dependent upon various test conditions that are being monitored by the test bit multiplexer. Upon request of the PROM code (T0–T3), any one of 16 different test conditions are selected. If test condition 3 is selected, for example, and the unit ready signal is not asserted, a new branch address is loaded into the CS program counter. When a branch to a new address occurs, the sequencer jumps to the new location and continues its program sequence from there.

The command sequencer PROMs issue the necessary control signals used throughout the RM02/03 adapter during command operations. The most important ones are described below.

EN SEARCH, for example, enables the sector compare circuit (CS5) to begin looking for a sector match with that in the disk address register. Once this match is detected, a sector compare signal is issued to the Read/Write sequencer, allowing it to exercise control over the reading and writing of data.

The EN CYLINDER, EN HEAD, EN CONTROL, EN OFFSET, and RECAL signals out of the sequencer PROMs permit positioning and control information to be transmitted by the differential drivers (CS6) to the disk drive. The tag signal is used in combination with the EN CYLINDER, EN HEAD, and EN CONTROL signals to generate the correct tag number as shown on page CS11 of the print set.

4.8.5 Read/Write Sequencer (CS4)

The read/write sequencer consists of a counter and three PROMs as shown in Figure 4-15. It is used to format a sector during read and write operations. The counter remains reset as long as SECTOR COMPARE H remains inactive. Once the desired sector has been found during a data command, SECTOR COMPARE H is asserted and the counter starts incrementing to provide the addressing for the PROMs. The word clock provides the timing for the counter to step through its addressing sequence.

The PROM maps and timing diagrams are all found in the print set. The PROM microcode routine is divided into seven major areas related to the sector format. They are as follows.

1. Zeros gap and sync byte (Gap is for head scatter, mechanical tolerance, and PLO synchronization.)
2. Header area
3. CRC
4. Gap and sync byte (Gap is for splice area and PLO synchronization.)
5. Data
6. ECC
7. Postamble

The PROM output signals control all of these sector subdivisions and determine when to read or write them. For example, the BR RD TO WRT signal causes the program counter to branch from the read area of memory to the write area. The PLFS signal prepares the data sequencer to look for the sync byte, etc.

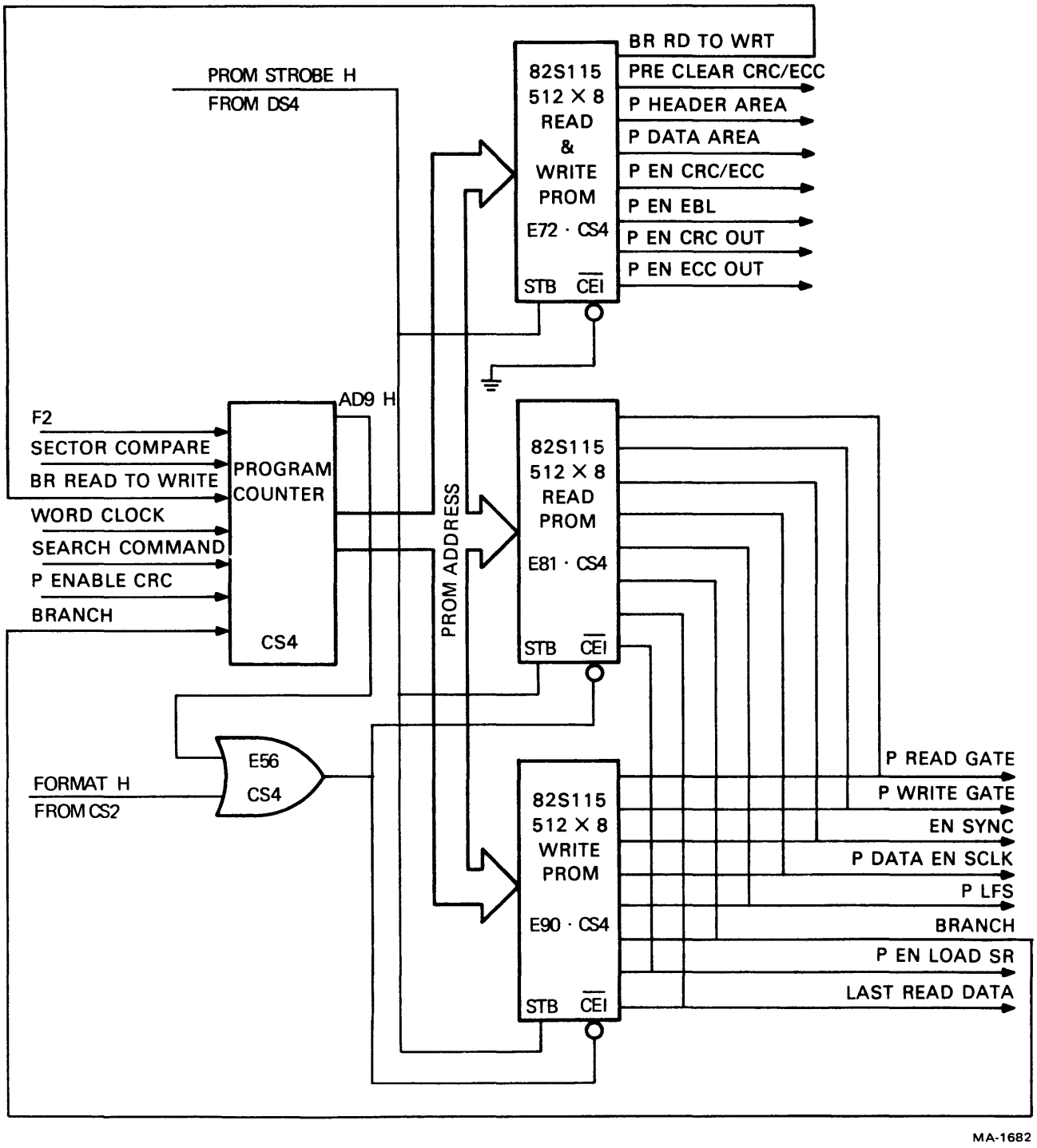


Figure 4-15 Read/Write Sequencer Block Diagram

4.8.6 Data Sequencer Data Paths

Although the read/write sequencer is located on the command sequencer module (M7684), the data paths followed by the data are on the data sequencer module (M7685). Paragraphs 4.8.6.1 and 4.8.6.2 describe the write and read paths, respectively.

4.8.6.1 Write Path - Figure 4-16 shows the path taken by data during a write command. Assuming port A is selected, data words requested from the Massbus are loaded into the data buffer (DS1) one word at a time. From here they are serialized (by shifting the register to the right) as they enter the shift register (DS2). The serial output (SR00 H) from the shift register is sent to three places. One path takes the data to the CRC circuit (DS5) (for CRC generation during the header write) and to the ECC circuit (DS8, DS10) (for ECC generation during the data write), where it can be checked or corrected. The second path presents the serial data to a series of gates on DS7 that act like a multiplexer. This multiplexer can select its output data from one of three sources at its input. It can select the serial shift register data (SR00 H), or a CRC output word, or an ECC pattern out of the ECC pattern register (RMEC2). Which input is selected depends on what portion of a sector format is being written and also which command was issued. Write data, together with its clock, is transmitted via cable B to the disk drive.

The purpose of the third path is to allow a parity check to be made on this serial data as it leaves the shift register. The logic for the parity generator and checker is shown on page DS3 of the print set.

4.8.6.2 Read Path - Figure 4-17 shows the path taken by data during a read command. The data being read off the disk enters the RM02/03 adapter via drive cable B. It enters and leaves the differential receivers on module M7687 on the read data line. It is read in sync with the read clock generated by the disk. The read data passes through the parity generation circuitry on DS3 (for the generation of a parity bit) and then enters the shift register (DS2). A branch of the read data is fed to the CRC (DS5) and ECC (DS8, DS10) circuits where the header words and data words can be checked for CRC and ECC errors, respectively. The read data in the shift register is converted to parallel format as it enters the data buffer (DS1). As the read data leaves the data buffer, a header comparison is done on only the first two header words to be sure they match the desired cylinder and address information stored in the RMDC and RMDA registers. The read data from the data buffer is then inverted and sent over the data out bus to whichever port is selected.

4.9 COMMAND EXECUTION

All command execution is handled by the command sequencer after the GO bit is set. As long as the GO bit in the control register is cleared, the program counter on CS1 remains reset to 0.

On the first clock pulse following the GO bit becoming active, the sequencer jumps to an address specified by the function code excluding bit F4. Function code bit F4 indicates a data command and is monitored as 1 of the 16 test conditions later on in the microcode sequence.

After the sequencer jumps to the address specified by the function code, further sequencing depends on the command type. There are three types of commands.

Type 1: Command Immediate

In this type of command, the sequencer jumps to the function code and then immediately ends by resetting GO. The operation performed by the command occurs immediately on decoding the function. The following commands fall into this category.

- No-Op Command
- Release Command
- Read-In-Preset Command
- Drive Clear Command
- Pack Acknowledge Command

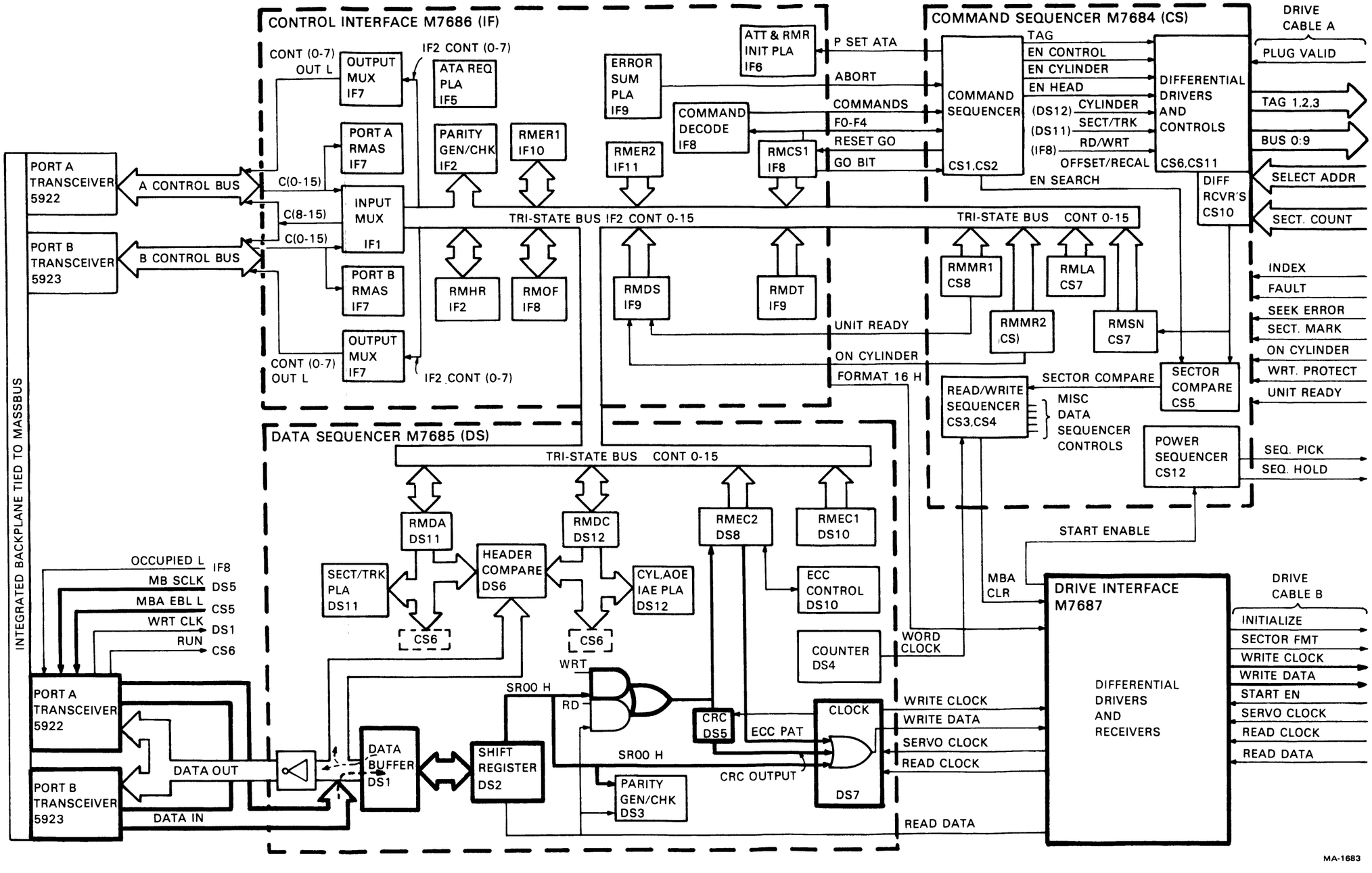


Figure 4-16 Write Data Flow Path Diagram

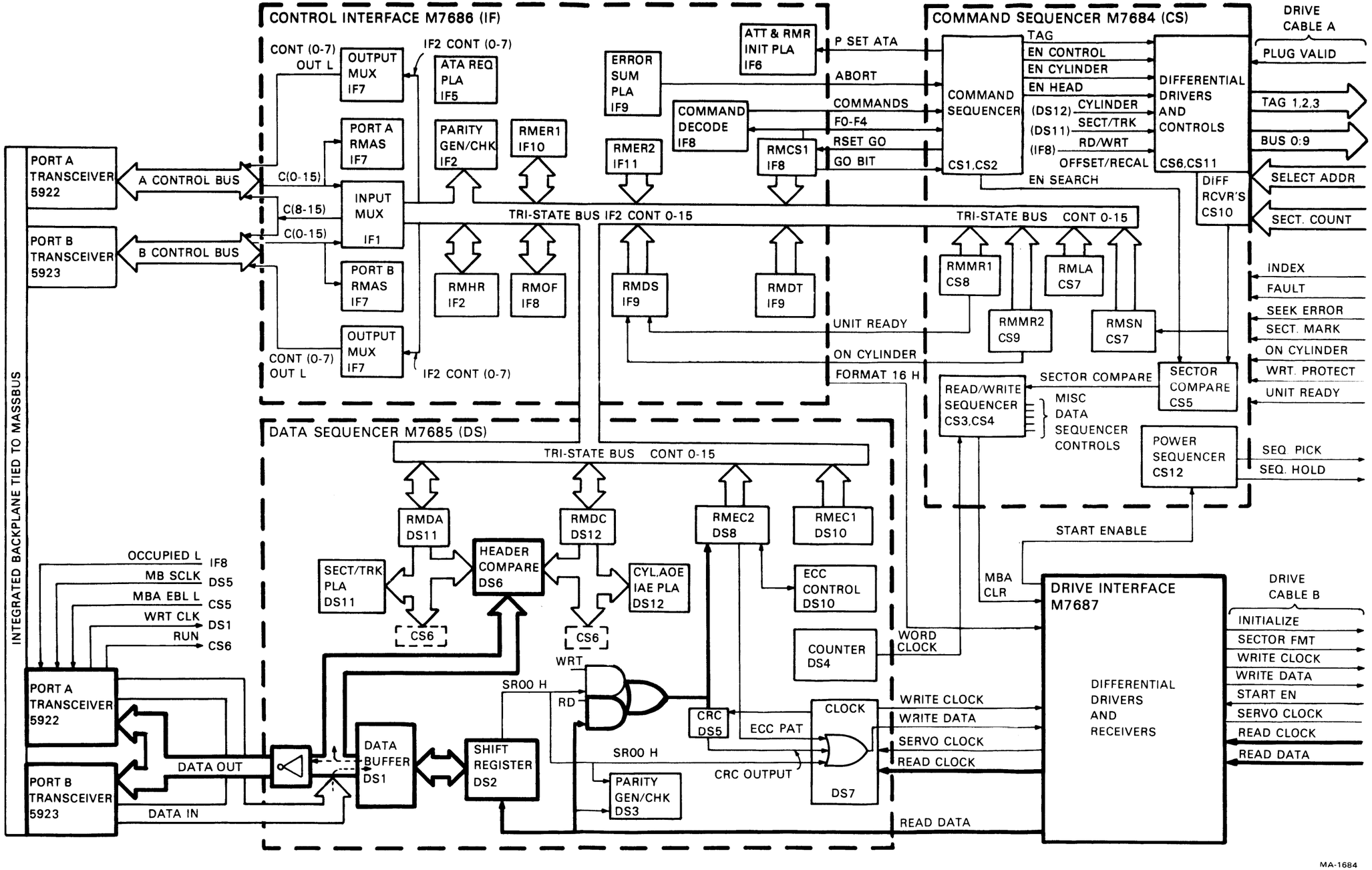


Figure 4-17 Read Data Flow Path Diagram

Type 2: Command Immediate with ATA
These are mechanical motion commands where the sequencer jumps to the function code, executes a sequence (i.e., mechanically positions the heads), sets ATA, and resets GO. The following commands fall into this category.

- Offset Command
- Return-To-Centerline (RTC) Command
- Recalibrate Command
- Seek Command
- Search Command

Two of these, offset and RTC, just set ATA and then reset GO.

NOTE
Offset and RTC do not cause the actual positioning of the heads.

Type 3: Data Transfer Commands
These are the commands that cause data to be transferred to or from the disk. In executing these commands, the command sequencer jumps to the function code, then jumps to address 128, executes a sequence, and then loops during enable search. When the desired sector is found, the read/write sequencer executes its data formatting routine and ends the sector with an end-of-block (EBL) pulse. Upon receiving this pulse, the command sequencer continues through its program and ends by resetting GO. The following are the commands that fit into this category.

- Read Data Command
- Read Header and Data Command
- Write Check Data Command
- Write Check Header and Data Command
- Write Data Command
- Write Header and Data Command

4.9.1 Command Immediate Execution
Command immediate commands a jump directly from the function code location to the end where reset GO L is asserted.

4.9.1.1 No-Op Command – This command simply resets the GO bit.

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start	Branch to Function	BRANCH H
1 = Function	Branch to End	BRANCH H
19 = Function	Branch to End	SET PULSE L
126 = End	Reset GO	END RESET GO L

4.9.1.2 Release Command – This command performs a drive clear function and then releases the drive for use by the other port.

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start	Branch to Function	RELEASE CMD L
11 = Function	Branch to End	RELEASE CMD L
19 = Function	Branch to End	SET PULSE L
126 = End	Reset GO	END RESET GO L

4.9.1.3 Read-In Preset Command – This command sets the volume valid bit (06) in the drive status register for the port that issued the command. It also clears all bits in the RMDC and RMDA registers as well as clearing the following bits in the offset register (bits 7, 10, 11, and 12).

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start	Branch to Function	READ IN CMD L RET TO CNT L
17 = Function	Branch to End	READ IN CMD L RET TO CNT L
19 = Function	Branch to End	SET PULSE L
126 = End	Reset GO	RESET GO L

4.9.1.4 Drive Clear Command – This command clears any drive errors if their cause is no longer present. It also clears the bits indicated in the following registers.

RMDS	Bits 14 and 15
RMER1	All bits
RMER2	All bits
RMAS	All bits
RMMR1	All bits
RMEC2	All bits

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start	Branch to Function	BRANCH H
9 = Function	Branch to DRV CLR	SET PULSE L BRANCH H
125 = DRV CLR	Increment	DRIVE CLR L
126 = End	Reset GO	RESET GO L

4.9.1.5 Pack Acknowledge Command – This command must be issued before any data transfer or positioning command if the disk drive has gone off- and on-line again (i.e., MOL changes state). This command sets volume valid (bit 6 in the drive status register). Note that volume valid is generated from a ROM (E50 on IF6).

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start	Branch to Function	BRANCH H
19 = Function	Branch to End	SET PULSE L BRANCH H
126 = End	Reset GO	RESET GO H

4.9.2 Command Immediate with ATA Execution

These commands are executed exactly like a command immediate, except that the attention bit (ATA) is set while resetting the GO bit to flag the end of the command.

4.9.2.1 Offset Command – An offset command allows the heads to be moved ±200 microinches off the track centerline during a read data command.

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start	Branch to Function	OFFSET CMD L
13 = Function	Branch to ATA	OFFSET CMD L
19 = Function	Branch to End	SET PULSE L
127 = ATA + End	Set ATA Reset GO	P SET ATA L RESET GO L

OFFSET CMD L sets the offset mode flip-flop.

4.9.2.2 Return-to-Centerline Command – This command returns the heads to the track centerline after an offset command.

PROM ADDR (DEC)	PROM Instruction	Active Signals
0 = Start	Branch to Function	RET TO CNT L
15 = Function	Branch to ATA	RET TO CNT L
19 = Function	Branch to End	SET PULSE L
127 = ATA + End	Set ATA Reset GO	P SET ATA L RESET GO L

RET TO CNT L resets the offset mode flip-flop.

4.9.2.3 Recalibrate Command – This command positions the heads over cylinder 0 and sets the current cylinder address register to 0. A flowchart of this command is shown in Figure 4-18. The command begins by testing function code bit 4 and unit ready. F4 is always tested to determine if this could be a data command. Unit ready is tested to ensure that all interlock conditions are met in the disk drive. The sequencer then checks whether any abort conditions are present. The control tag, together with control bus bit 7 is then sent to the disk drive. At this point, the on latch is tested to be sure the drive has accepted the command and has initiated motion of the heads. If it passes this test, the sequencer then waits for on cylinder to become active again, indicating that the heads are over the correct cylinder. It then sets the ATA bit and resets GO.

4.9.2.4 Seek Command – This command causes the heads to move to the cylinder address specified in the RMDC register. The command is complete when the current cylinder equals the desired cylinder. A flowchart of this command is provided in Figure 4-19. All commands begin by testing unit ready and F4 to see if the drive is busy and whether this function is a data command. If the sequencer passes these tests and there are no abort conditions present, it issues tag 1 and cylinder information to the drive. The set pulse has already reset the on latch flip-flop and the sequencer now waits for on cylinder to become active again. When on cylinder is detected, the sequencer then jumps to the end where it sets ATA and resets GO.

4.9.2.5 Search Command – The search command combines a seek command with a search for the desired sector address. A flowchart for this command is shown in Figure 4-20. Like all other commands, it begins by testing drive unit ready, F4, and abort conditions. After testing abort, the sequencer jumps to decimal address 144 and uses the implied seek portion of a data command. It issues tag 1 and cylinder information to the drive and then tests the occupied bit to determine if the sequence should continue the search.

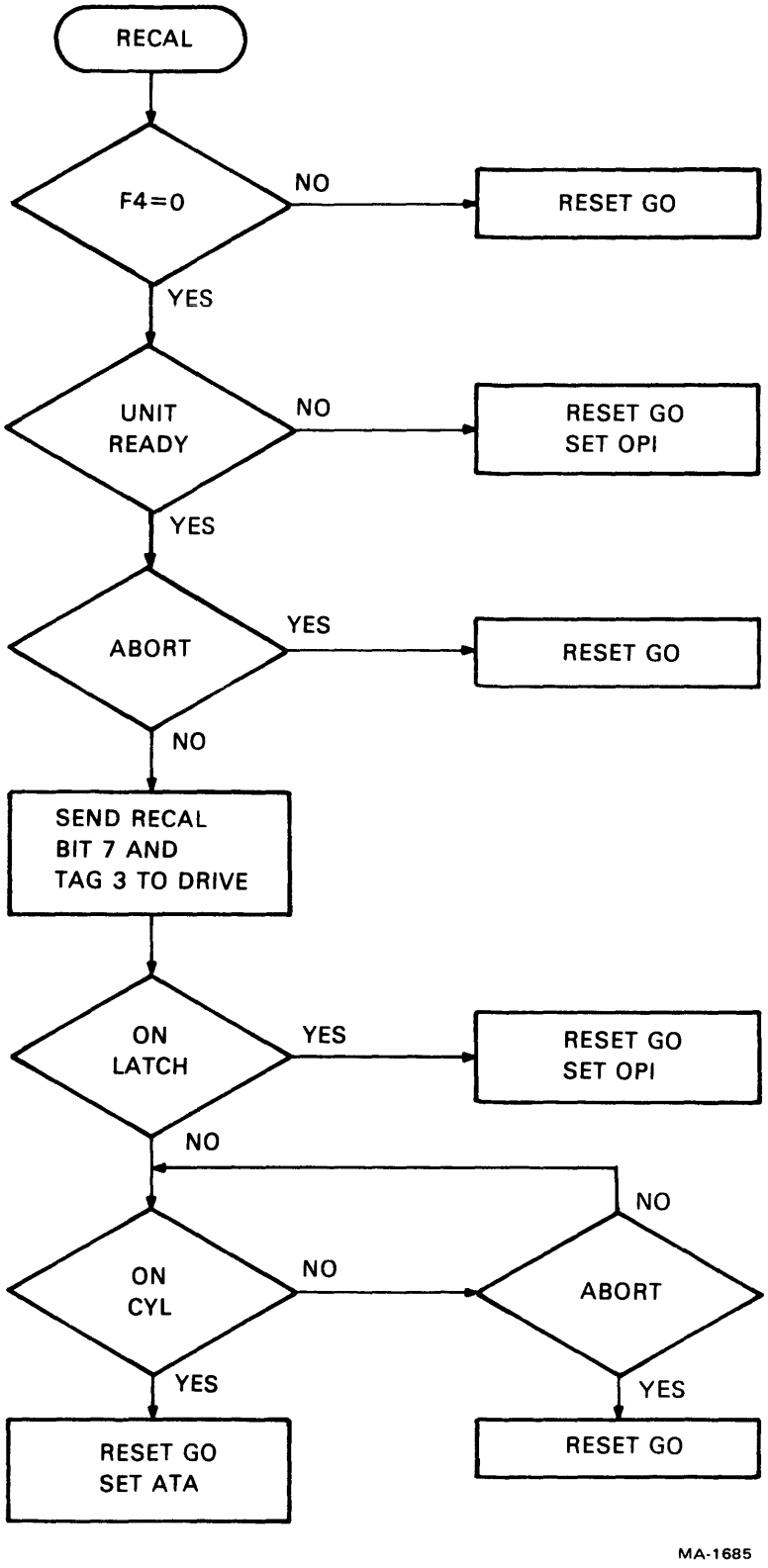


Figure 4-18 Recalibrate Command

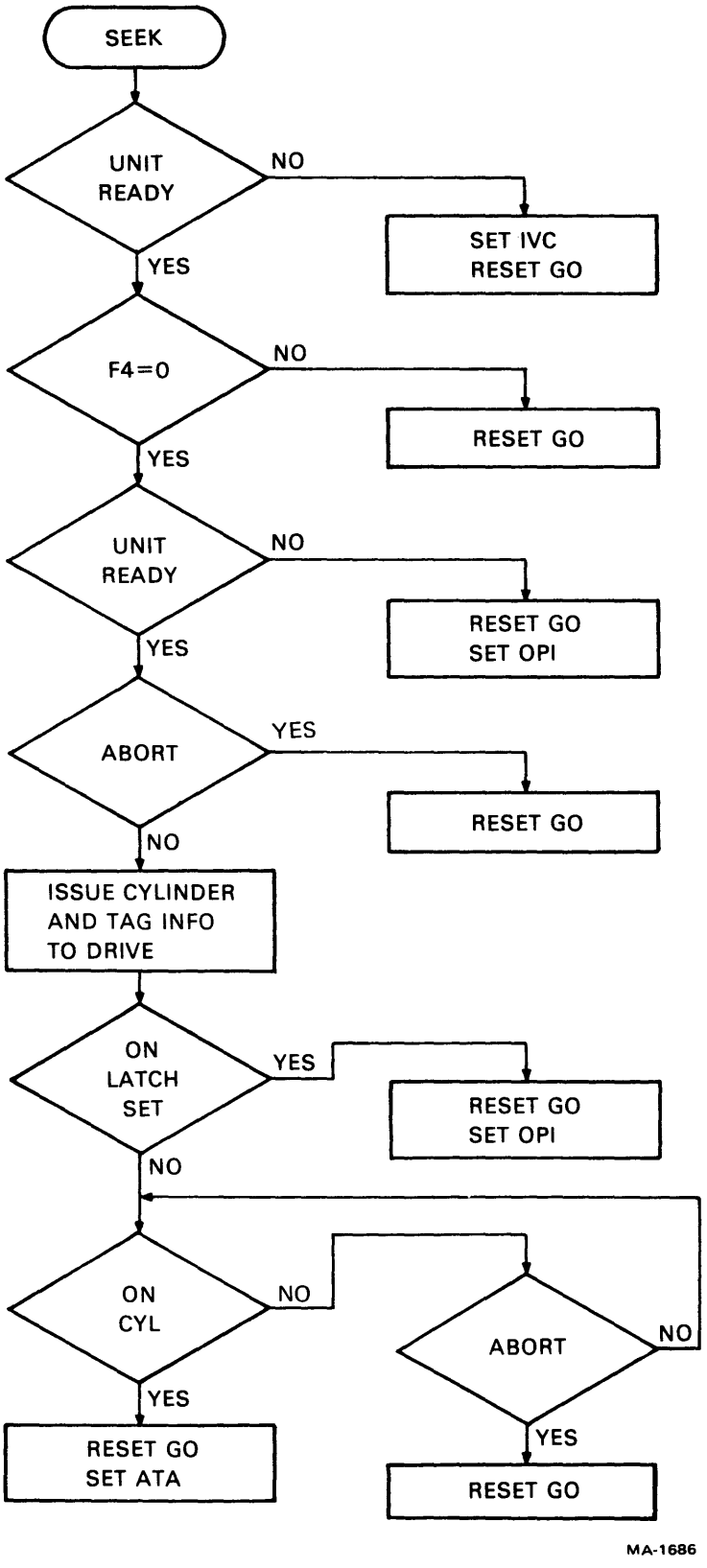


Figure 4-19 Seek Command

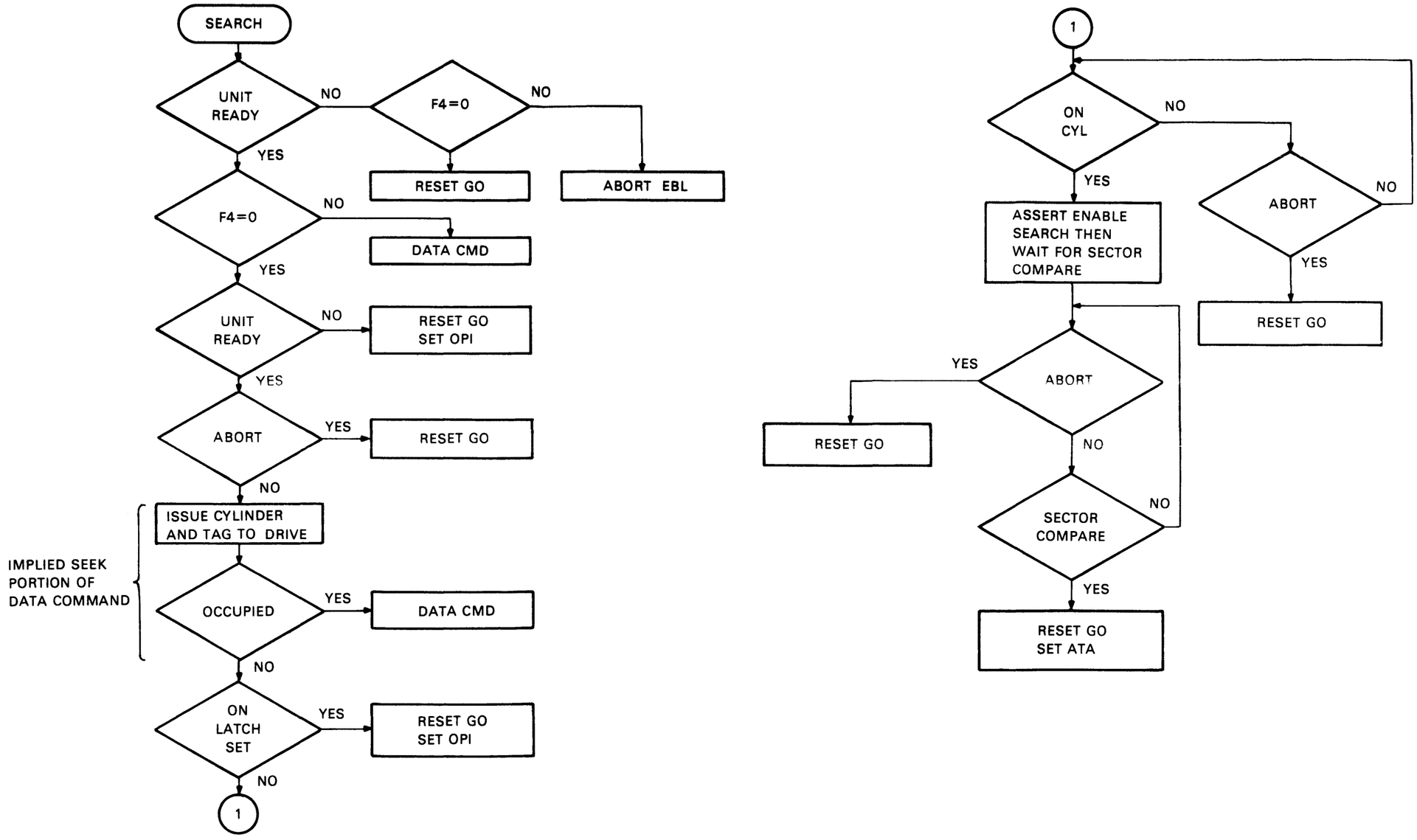


Figure 4-20 Search Command

If occupied = 1, it proceeds to perform a data command. If occupied = 0, it continues the search routine. The SET PULSE has already reset the on latch flip-flop so the sequencer waits for on cylinder to become active. When it does so, indicating that the heads are on cylinder, the sequencer then asserts the enable search signal, starting the search for the correct sector. Each sector is continuously compared with the contents of the disk address register until a match is found. At this point, if no error conditions are present to cause an abort, the sector compare signal causes the sequencer to jump to the end of its routine, setting ATA and resetting the GO bit.

4.9.3 Data Transfer Command Execution

All data commands are executed by the same routine which starts at decimal address 128. Prior to the routine, command execution is similar to other commands. That is, the sequencer starts at 0 and jumps to the function and then to the routine.

The data routine consists of six consecutive segments. They are as follows.

1. Check initial conditions
2. Execute an implied seek
3. Execute a head selection and wait
4. Execute an offset (if required)
5. Execute a search and data transfer
6. Continue or terminate

A data command flowchart is presented in Figure 4-21. Before executing the data command, the microcode checks for a drive ready condition. Next the microcode checks for any abort conditions. If an abort is indicated, the command terminates at this point. The microcode then checks the RUN line on the Massbus interface. The command proceeds if the RUN line is active. If not, the program loops on checking for an abort condition or for an active RUN line. If the RUN line does not become active within 50 ms after the GO bit is set, a timeout causes an abort condition.

The second segment of the program involves the implied seek. Seek execution starts at decimal 144 and increments up to location 156. During this portion of the microcode, all signals required for seek execution become active. EN CYLINDER becomes active first. It is used to enable the outputs of the desired cylinder register onto the bus lines to the drive. The TAG H signal is gated with EN CYLINDER to generate tag 1 to the drive. On the leading edge of tag 1, the drive strobes the bus lines. On the trailing edge of tag 1, the drive initiates the seek. The sequencer then checks the occupied bit to determine whether to perform a search command or a data command. The on latch is checked to ensure that head motion was initiated, and then the program loops until on cylinder becomes active. The program aborts if it must loop for more than 500 ms.

The third segment of the program is the selection of the head. Head execution begins at decimal address 157 and continues to location 165. During this period, the sequencer asserts the EN HEAD signal to enable the outputs of the desired address register onto the bus lines to the drive. The TAG H line is asserted and is gated with EN HEAD to generate tag 2 to the drive. The drive selects the new head on the trailing edge of tag 2. Inserted into the microcode is a 5 μs waiting period after head selection to allow the heads to settle and provide reliable data.

The fourth segment of the program allows for an offset to be executed if an offset command was issued prior to this data command to set the offset mode flip-flop. To see if this was the case, the microcode tests to see if the offset flip-flop is active. If not, then the offset execution is bypassed. If the offset flip-flop is active, the sequencer asserts the EN CONTROL signal to enable the offset direction information in the offset register onto the disk drive bus lines. It then asserts TAG H which is gated with EN CONTROL to generate tag 3 to the disk drive. The heads become offset $\pm$200 microinches, depending on the offset direction bit sent. The on cylinder is tested and allows the sequencer to move onto the next segment when it becomes active. It will abort if on cylinder does not become active within 500 ms.

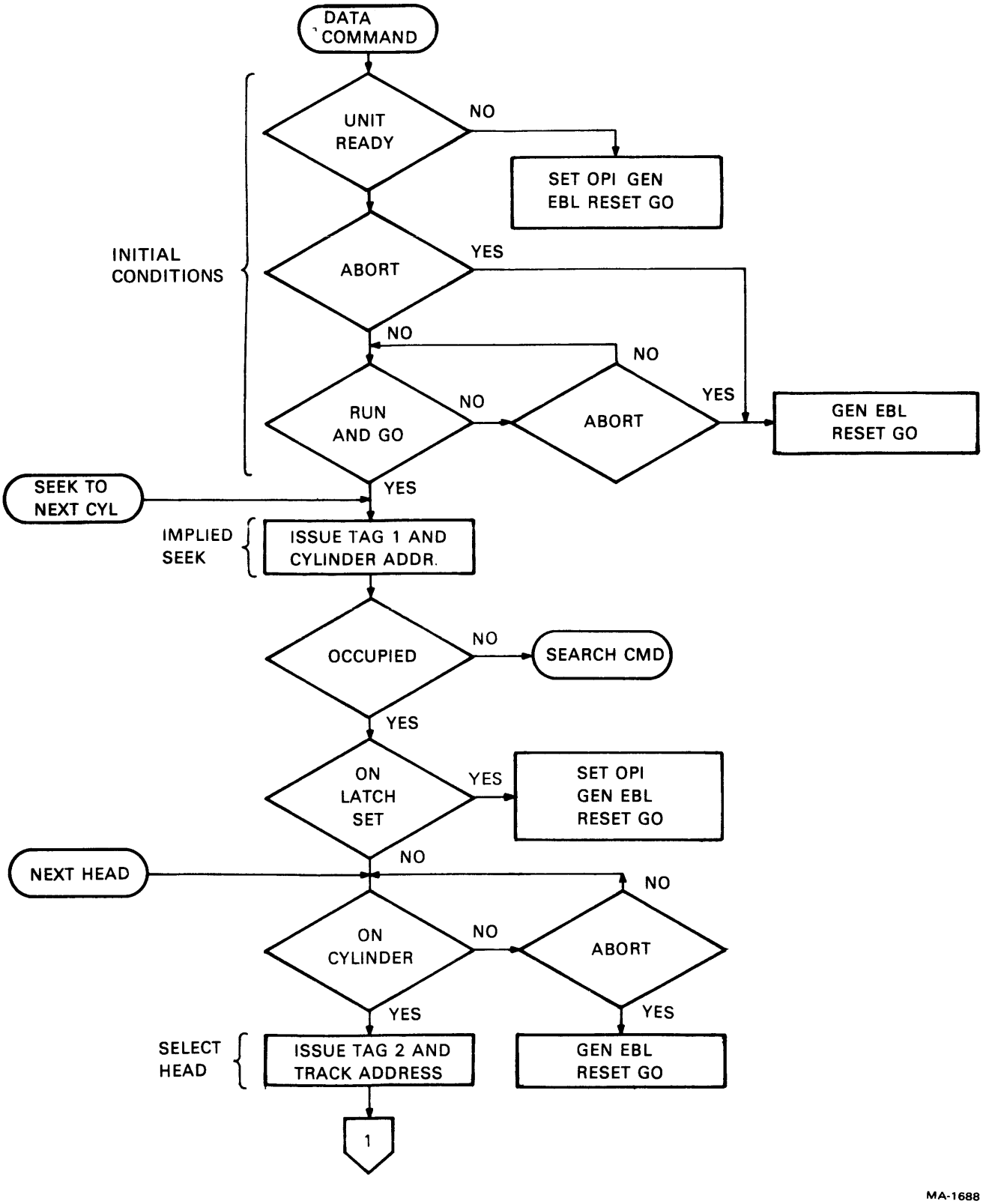


Figure 4-21 Data Transfer Commands (Sheet 1 of 3)

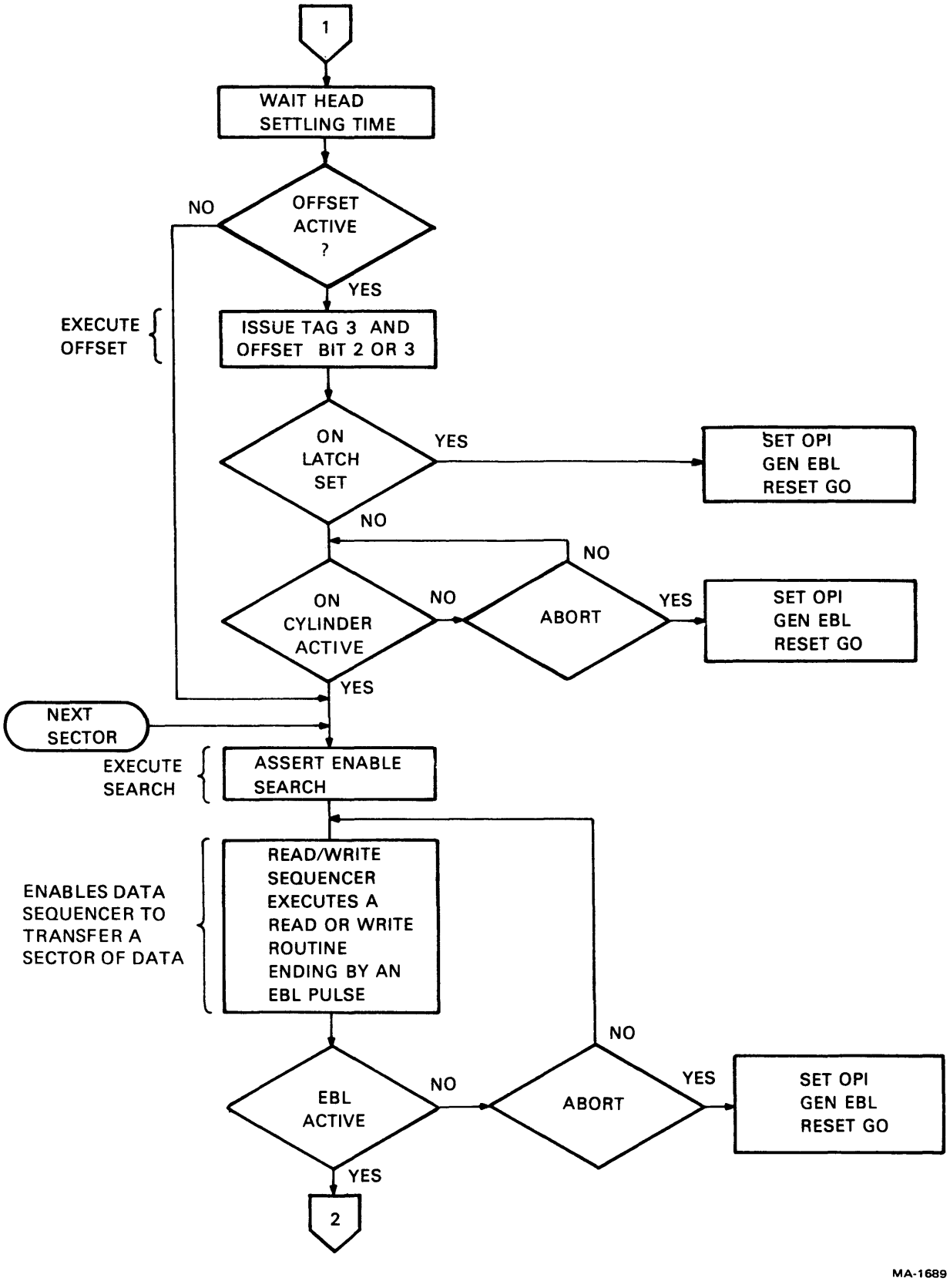


Figure 4-21 Data Transfer Commands (Sheet 2 of 3)

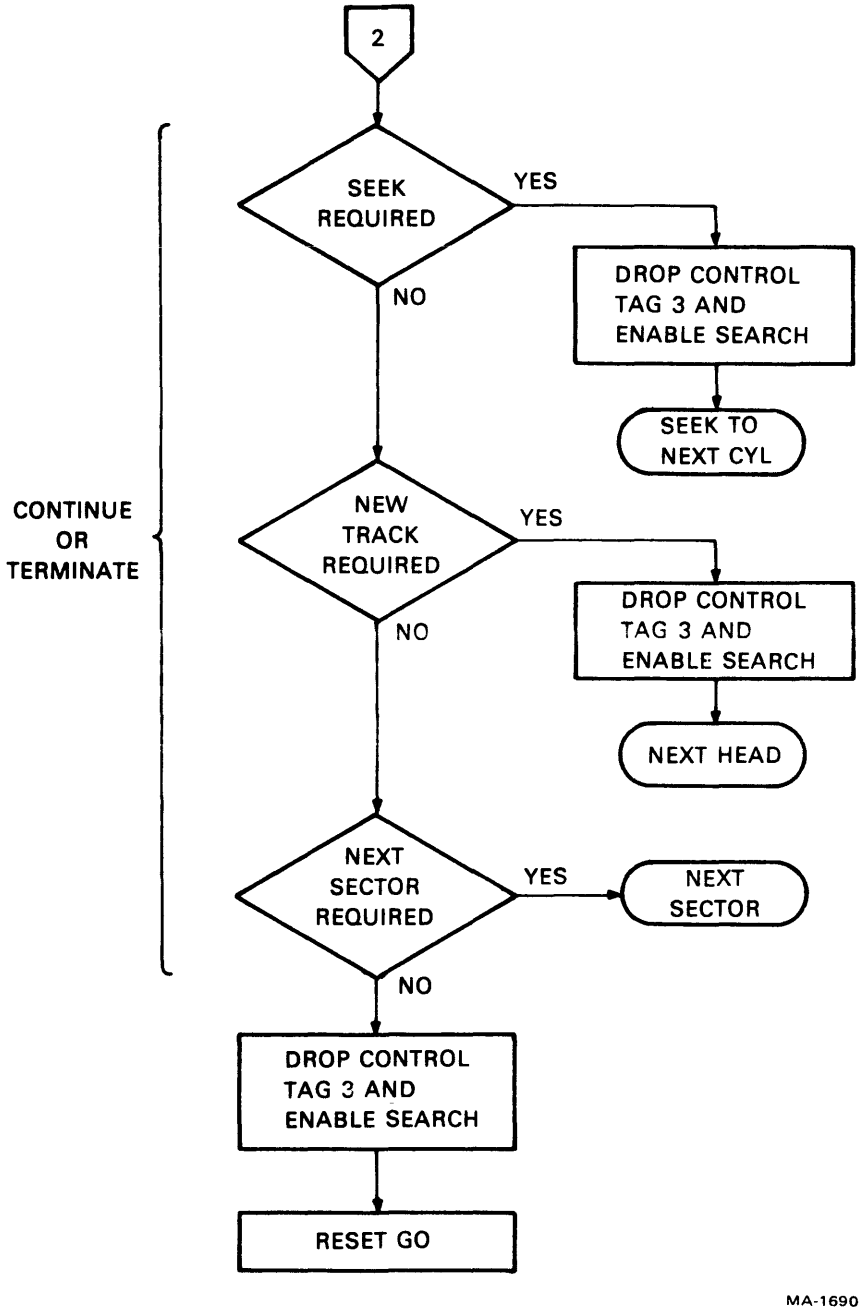


Figure 4-22 Data Transfer Commands (Sheet 3 of 3)

The fifth segment of the program begins the search routine. It is initiated when the command sequencer asserts the EN SEARCH signal. The sequencer now loops until either the correct sector is found and the entire sector has been transferred or until a timeout occurs. If a timeout occurs, the command is aborted. (The timeout occurs if no comparison happens within three revolutions.) When the correct sector is found (sector compare is true), the read/write sequencer takes over control and executes a read or write sequence for one sector. At the end of that sector, it generates an EBL pulse to notify the command sequencer that it may proceed.

In the sixth segment of the program, it is decided whether or not the command should continue. The microcode first checks whether or not to do a mid-transfer seek. Next, it checks whether or not to select a new head. Finally, it checks to see if it should proceed on to the next sector. If none of these decisions are affirmative, the command terminates here and resets the GO bit.

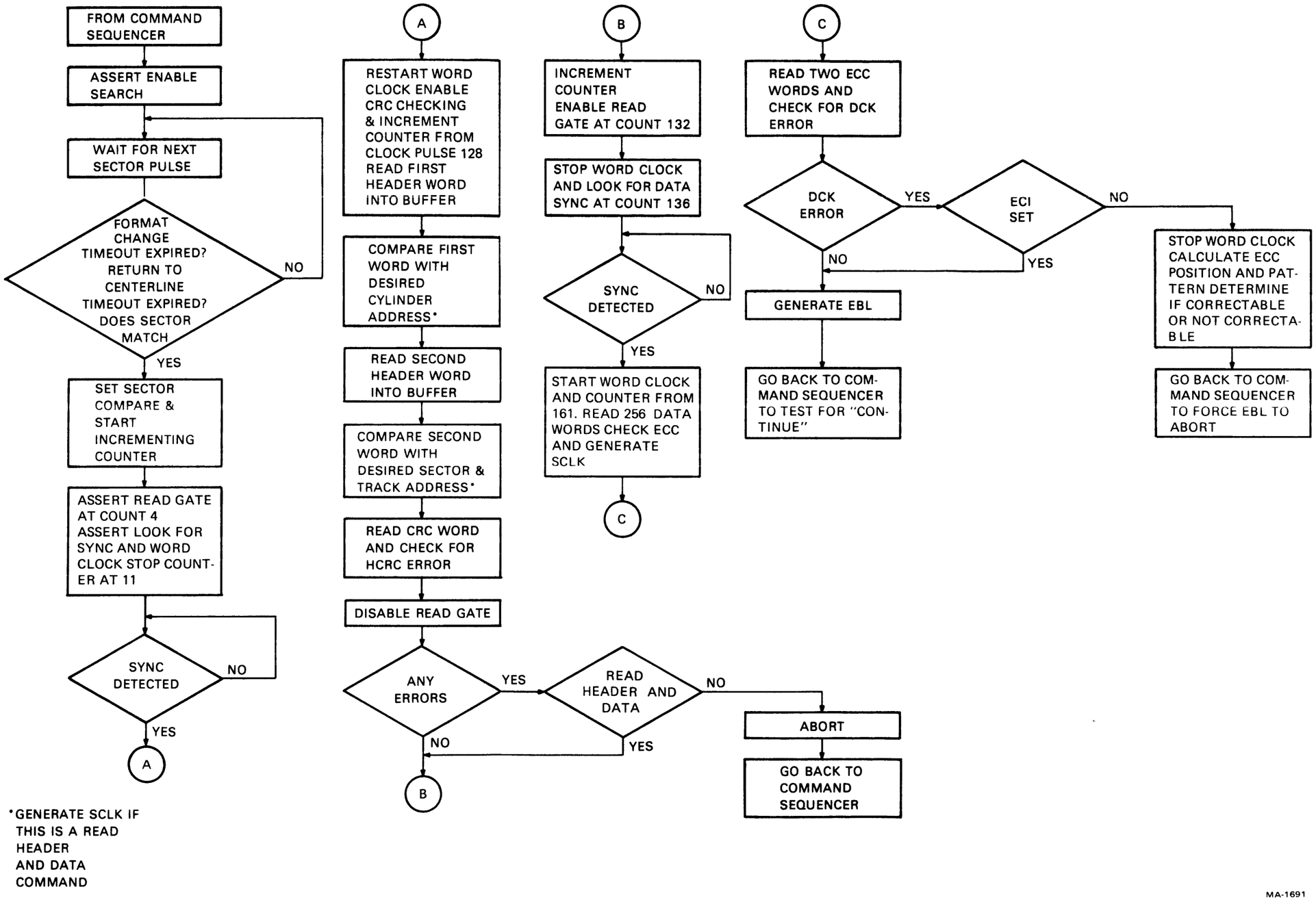
4.9.3.1 Read and Write Check Data Execution – The read data and write check data commands are so similar that a single flowchart is used for both operations. Figure 4-22 illustrates all the functions that they perform. Only a portion of the entire command is covered here because the overall data transfer operation was described in the preceding paragraph. This flowchart deals with the operation of the read/write sequencer from the time it receives a sector compare signal until the end of that sector. Assuming that the command sequencer has already performed a seek and head selection operation, it then asserts the EN SEARCH line which initiates a search for the correct sector. When a sector match is found, it sets sector compare and the read/write sequencer begins incrementing. The read gate is enabled at count 4. At count 11, look for sync is asserted and the counter is stopped. When sync is detected, the word clock is started again. Beginning from clock pulse 128, the first header word is read into the data buffer and compared with the desired cylinder address (Figure 4-22, Sheet 2). The format and bad sector flags are also checked at this time.

At count 129, a second header word is read off the disk and compared with the disk address register. If this is a read header and data command, both of these words are sent on to the Massbus with SCLK pulses. At count 130, the CRC word is read and checked for HCRC errors. The read gate is then disabled while testing for errors. The read gate is then enabled again at count 132 and looking for data sync begins at count 136. After sync is detected, data words are read from count 161 until a total of 256 data words are read. Each data word is shifted into the data buffer and through the ECC logic and parity generation circuitry and then onto the Massbus with a SCLK pulse. At count 417 and 418, two ECC words are read and checked for DCK errors. If no errors are found, an EBL pulse is generated to signal the command sequencer that the current sector has been read.

4.9.3.2 Write Data Execution – During a write data command, the RM02/03 adapter transfers 256 data words onto the disk for each sector specified by the controller. The adapter also generates a sync byte to precede the data field and a 32-bit ECC word after it. If the adapter detects a CRC error in the header, it aborts the command.

Figure 4-23 provides a flowchart of the write data command. As with all data commands, the read/write sequencer takes over control of the sector formatting after a search is executed and a sector match is found. This results in the assertion of sector compare which permits the program counter to begin incrementing. The microcode asserts read gate at the count of 4 and then begins looking for sync byte at count 11. After sync byte is detected, the first header word is read off the disk into the buffer at count 128. It is then compared with the desired cylinder address. At count 129, the second header word is read off the disk and compared with the desired disk address register. At this point, the CRC word is read off the disk and checked for HCRC error. This concludes the read portion of the write command. Read gate is disabled, and write gate is enabled by the BR RD TO WRT L signal.

The write portion of the command begins by writing the preamble and sync byte on the disk. Data is then requested from the Massbus and 256 data words are written.



MA-1691

Figure 4-22 Read and Write Check Data Commands

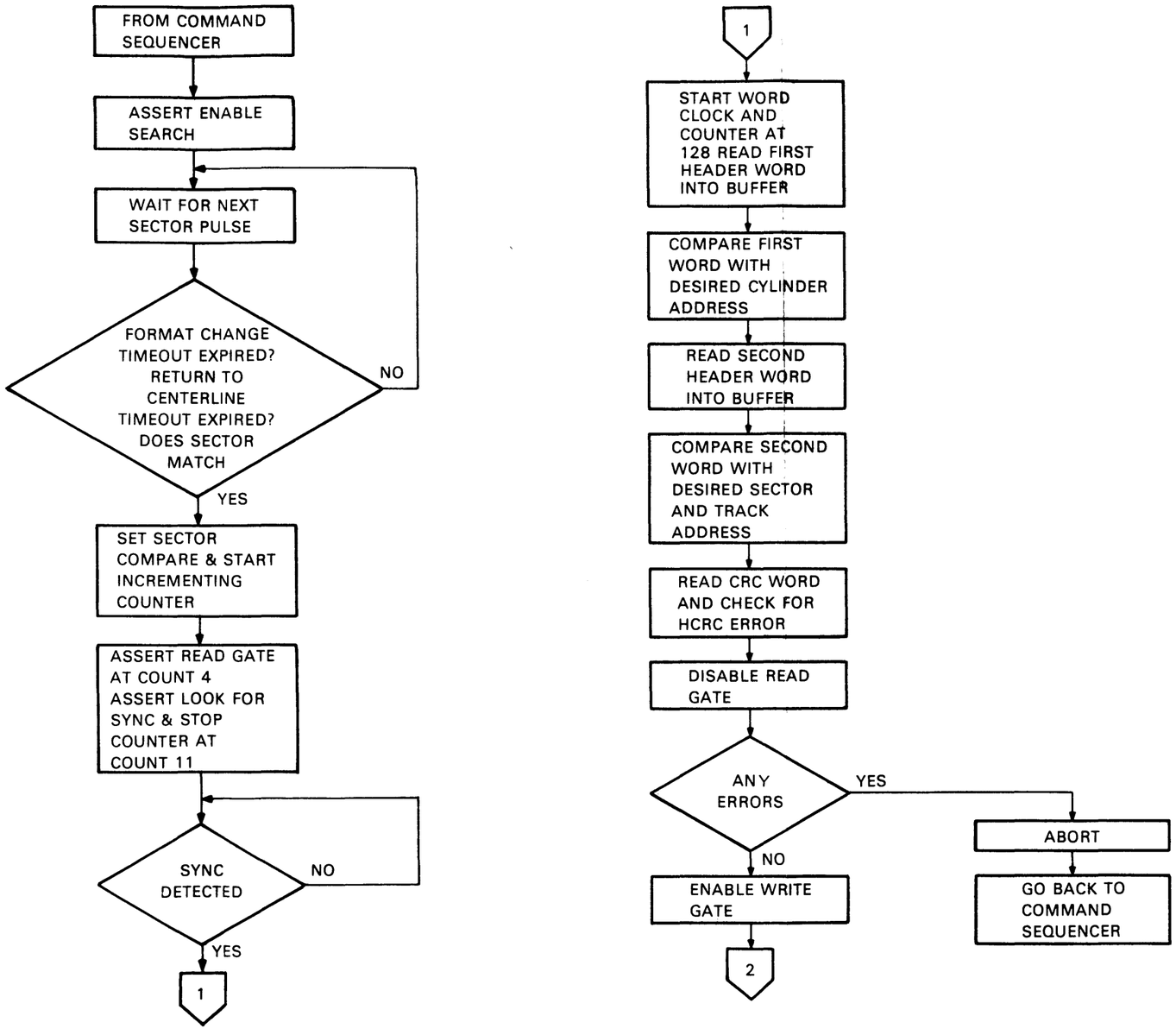


Figure 4-23 Write Data Command

At this point, the adapter generates two ECC words and writes them on the disk followed by a postamble which concludes the sector. The microcode then generates an EBL pulse to notify the command sequencer that it has finished the data portion of the command.

4.9.3.3 Write Header and Data Execution – This command formats the disk with gaps, headers, and data for specified sectors. A controller supplies 2 header words and 256 data words for each sector. The RM02/03 adapter generates the gaps including sync bytes, CRC word, and ECC words.

Figure 4-24 provides a flowchart of the write header and data command. Once the sector compare signal is asserted, the read/write sequencer assumes control over the sector formatting. It enables the word clock and write gate, and begins writing 27 bytes of 0s plus a sync byte on the disk. It then requests two header words from the Massbus and writes them while generating their CRC code. Next, it writes this CRC word and 17 bytes of data preamble on the disk. It ends the preamble by writing a sync byte, indicating the beginning of the data field. At this point, the RM02/03 adapter starts requesting data from the Massbus. It writes a total of 256 data words followed by their 2-word ECC pattern. The postamble is the last to be written before generating an EBL pulse to notify the command sequencer to resume control.

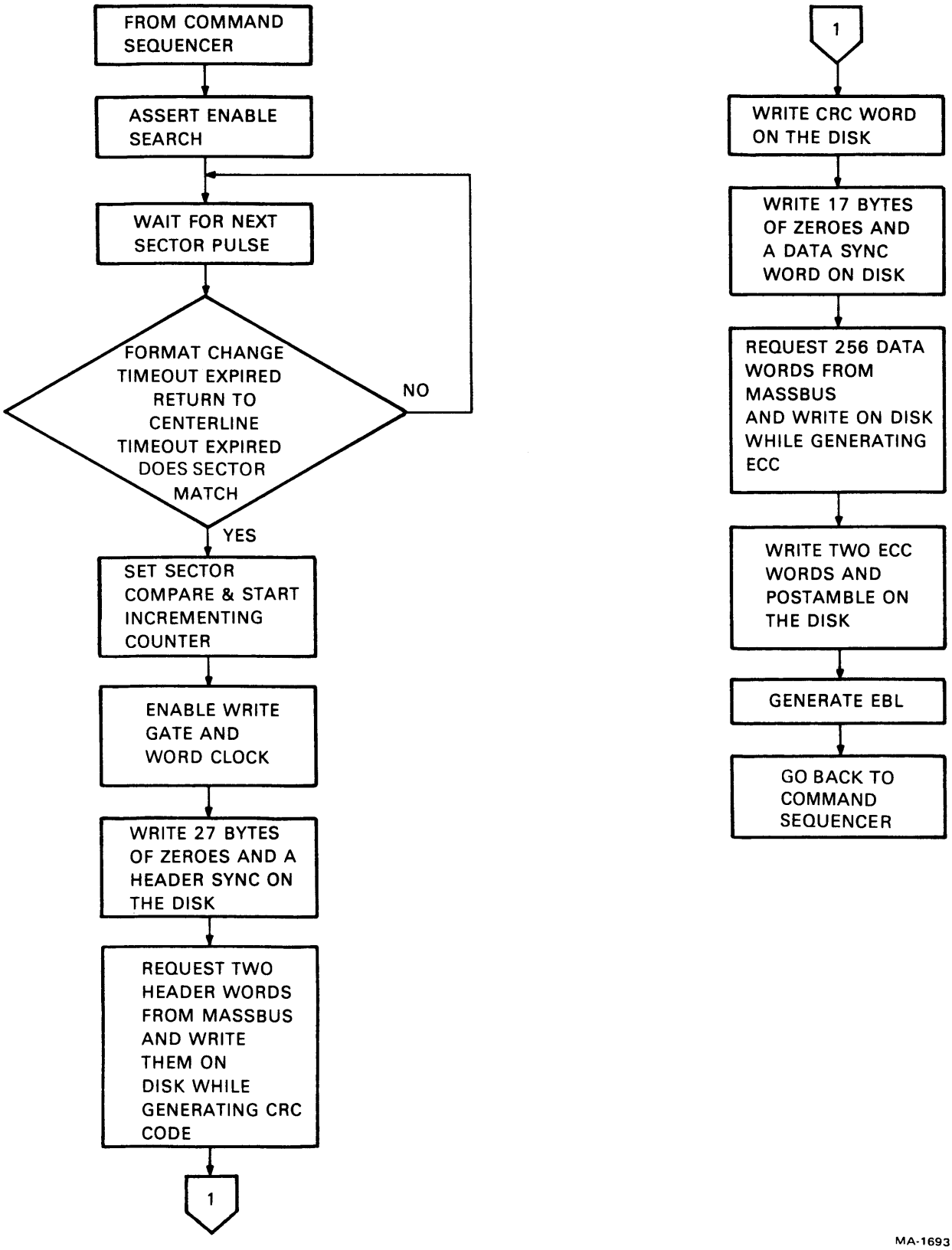


Figure 4-24 Write Header and Data Command

APPENDIX A
PROGRAMMABLE LOGIC ARRAYS

A.1 INTRODUCTION

The RM02/03 adapter uses the 82S100 field-programmable logic arrays (FPLA). This device offers the following characteristics.

- Field programmable (Ni-Cr link)
- 16 input variables
- 8 output functions
- 48 product terms
- 50 ns, maximum access time
- 600 mW power dissipation
- TTL compatible
- 28-pin package
- $\overline{CE}$ input for expansion
- Outputs individually programmable active "high" or "low"
- Single +5 V power supply

In many ways, an FPLA is very similar to a programmable read-only memory (PROM). Both of these devices are programmable and can store microcoded words. Both consist of an input buffer, decoder, storage matrix, and output buffer as shown in Figure A-1.

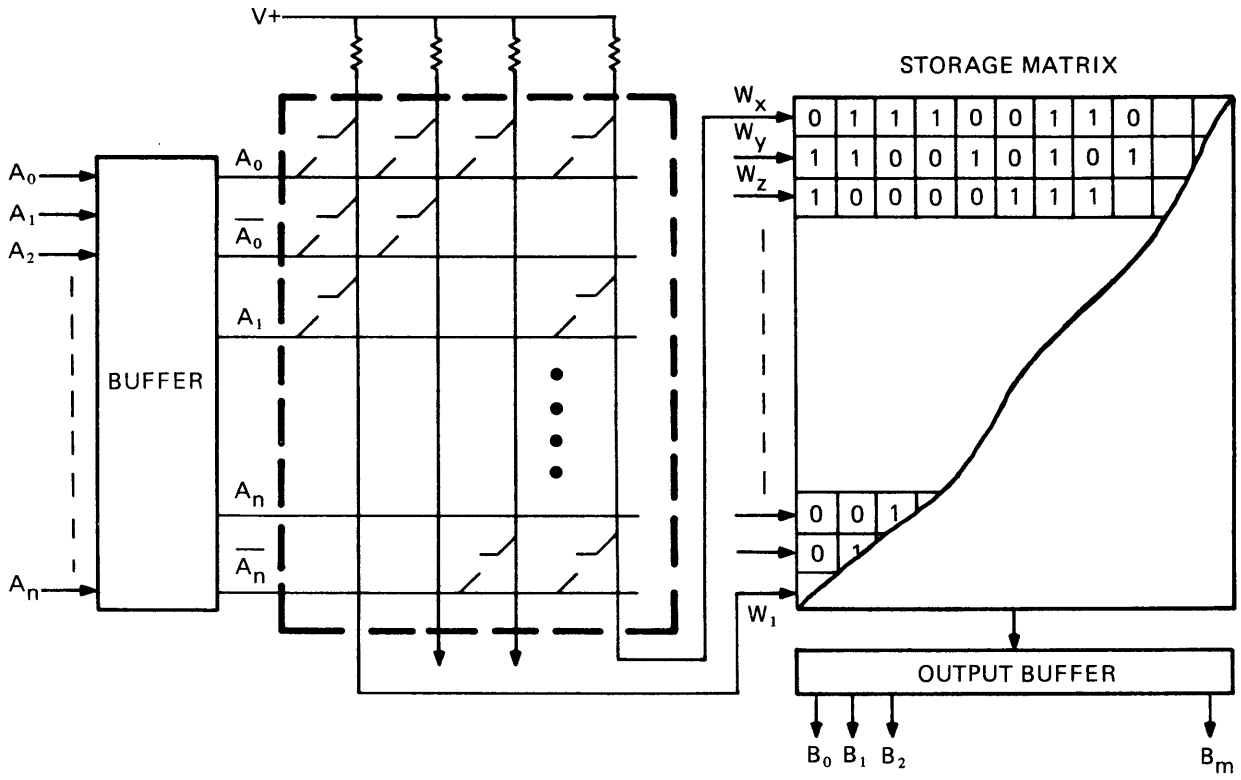
In a PROM, all internal words are reached by a fixed decoder, internal to the device. The size of this decoder and its storage matrix doubles for each additional address input. The presence of this fixed decoder cannot be avoided and forces the PROM to be used in discrete sizes.

The FPLA does away with this fixed decoder in favor of a programmable address matrix. This feature allows tremendous efficiencies to be obtained by truth table compression. Storage for unused min-terms is no longer required.

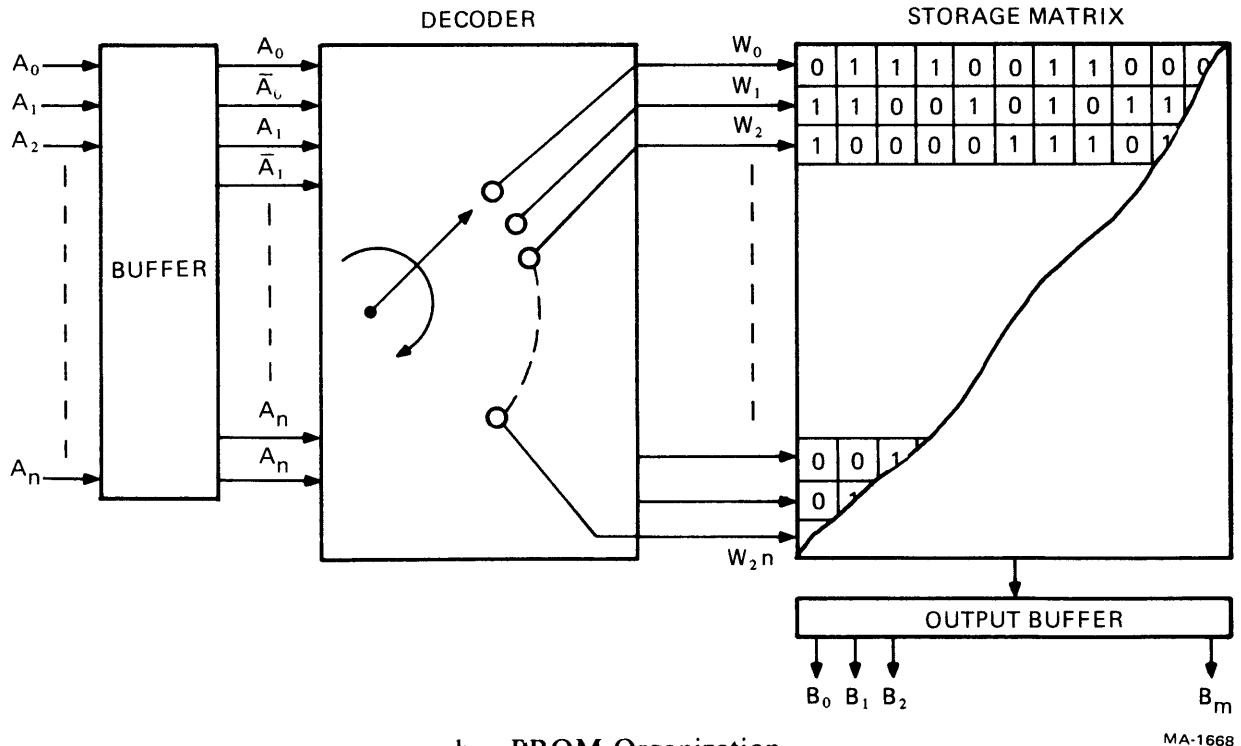
In the case of the 825100 FPLA, its 48 words can be addressed by a minimum of 48 input address combinations, chosen by the user from a total available pool of 2^{16} (65,536). The address matrix (decoder) in the FPLA need only be large enough to address 48 words. Also its storage matrix need only be large enough to store 48 words.

A.2 THE PLA CIRCUIT ORGANIZATION

Figure A-2 shows the logic structure for the FPLA. It consists of an AND matrix containing 48 product term columns (P-terms), and an OR matrix containing 8 sum term rows (S-terms). Each P-term in the AND matrix is coupled to each input variable via two Schottky diodes for programming the desired input state. It is also coupled to each S-term in the OR matrix through an emitter follower with an emitter fuse. This pulls the summing node to a HIGH level when the P-term is activated. Each S-term is coupled to its respective output by an EX-OR gate, which is polarity programmable by means of an input to ground through a fusible link.



a. FPLA Organization



b. PROM Organization

Figure A-1 FPLA and PROM Block Diagrams

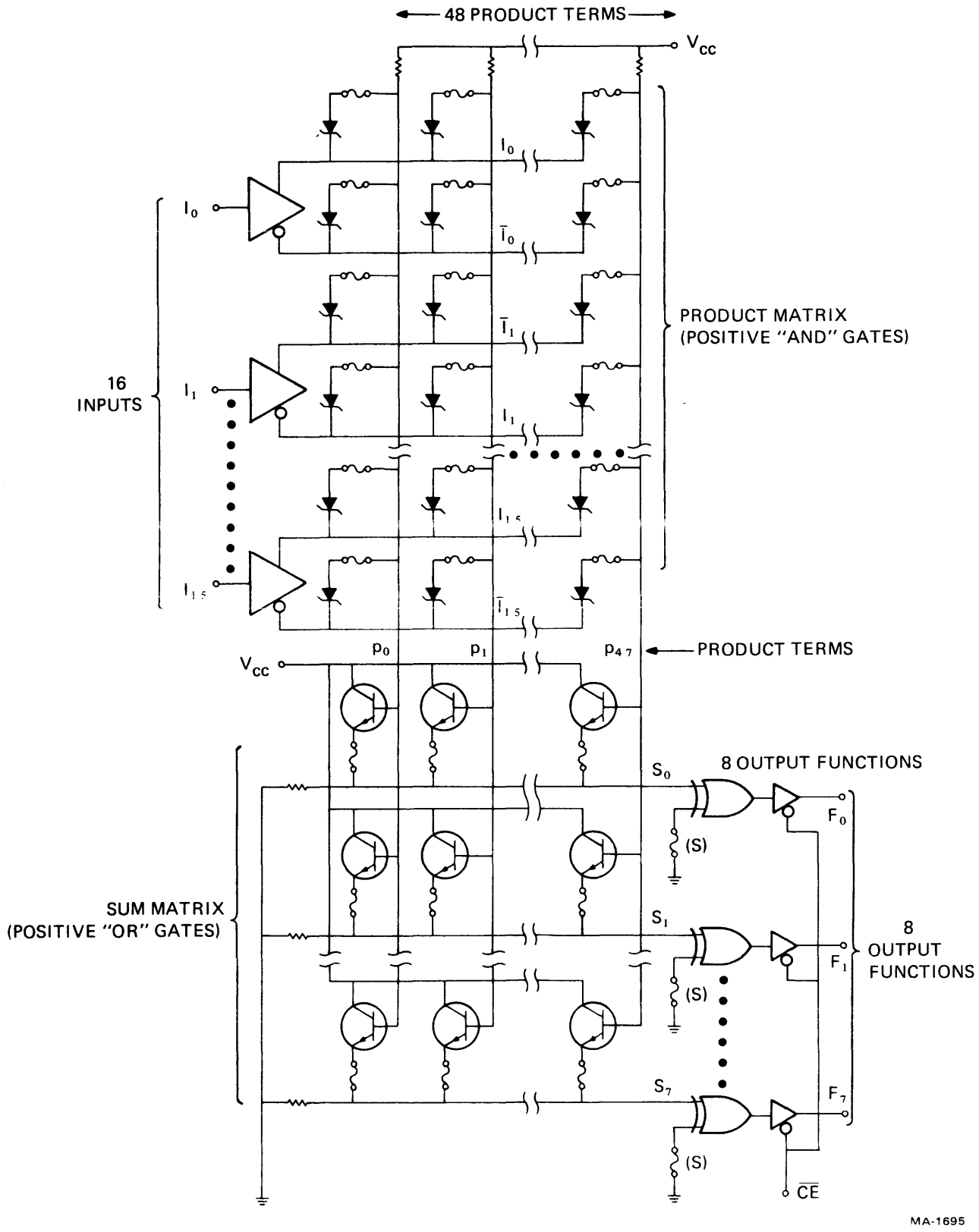


Figure A-2 FPLA Logic Structure

A.3 FPLA Program Maps

The FPLA is programmed by the user to contain the desired program table similar to the one illustrated in Figure A-3.

Each P-term is programmed to contain the desired logic state of each input variable by fusing the appropriate Ni-Cr link. In its initial unprogrammed state, all links are intact. If a product term (P^n) contains I^m, then the I^m link is fused, and vice versa. If I^m is a don't care condition in P^n, both the I^m and I^m must be fused. If any of the 16 input variables are not used, they represent don't care conditions and both of their links should be fused.

The sample program table shown in Figure A-3 can be read in the following manner.

1. The input variable columns use three kinds of symbols to designate how to modify the FPLA input decoder. An (H) symbol indicates that an I^m input state is desired and thus the I^m link should be fused. An (L) symbol indicates that an I^m input state is desired and that the I^m link should be fused. An (–) symbol indicates a don't care condition and requires that both should be fused.

2. The output function columns use two symbols. An (A) symbol indicates an active level and means that the input product term is present in the output function. The (.) symbol indicates that it is not present and thus the output is inactive.

3. The active level may be either high or low and is indicated as such directly above the output function columns.

PROGRAM TABLE ENTRIES						
INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
I_m	$\overline{I_m}$	DON'T CARE	PROD. TERM PRESENT IN F_p	PROD. TERM *NOT* PRESENT IN F_p	ACTIVE HIGH	ACTIVE LOW
H	L	– (DASH)	A	•(PERIOD)	H	L
NOTE: ENTER (-) FOR *UNUSED* INPUTS OF *USED* P-TERMS.			NOTES: 1) ENTRIES INDEPENDENT OF OUTPUT POLARITY. 2) ENTER (A) FOR *UNUSED* OUTPUTS OF *USED* P-TERMS.		NOTES: 1) POLARITY PROGRAMMED ONCE ONLY. 2) ENTER (H) FOR ALL *UNUSED* OUTPUTS.	

PRODUCT TERM *																	ACTIVE LEVEL							
NO.	INPUT VARIABLE																H	H	L	H	L	H	L	H
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OUTPUT FUNCTION *							
																	7	6	5	4	3	2	1	0
0	–	–	–	–	–	–	–	L	L	L	H	H	H	H	H	H	A	A	•	•	•	•	A	A
1	–	–	–	–	–	–	–	L	L	L	H	H	H	L	H	L	A	A	•	•	•	•	A	A
2																								
3																								
4																								
5																								
6																								
7																								
8 ↓ 47																								

MA-1696

Figure A-3 Sample FPLA Table

RM02/03 ADAPTER
TECHNICAL DESCRIPTION MANUAL
EK-RM023-TD-001

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