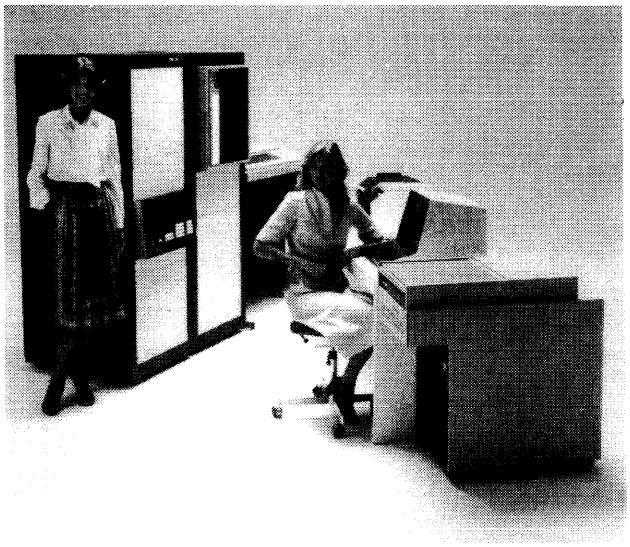
SYSTEMS 32 Series



The packaged SYSTEMS 32/7760 consists of 512K bytes of ECC MOS memory, 10 available SelBUS slots, 80-megabyte master moving-head disk drive, TLC controller, 75-ips 9-track tape unit, 600-lpm line printer, 300-cpm card reader, console CRT, RTM operating system, macro-assembler, and control panel with hex display. Price of the 32/7760 is $109,900.

SYSTEMS, formerly SEL, has expanded its 32-bit line by adding the 32/30A MAXIBOX, the 32/57, and the 32/77 to the previously offered 32/75. The SelBUS, a 32-bit-wide, high-speed bus, provides a system throughput of over 26 megabytes per second. The new computers are upwardly compatible with older SYSTEMS 32-bit models. All of the 32 Series computers use the same CPU, and their basic differences are in the packaging, the expansion capability, and the type of memory used. Prices range from $25,100 for a basic MAXIBOX nucleus to $109,900 for a packaged system based on the top-of-the-line 32/77.

MANAGEMENT SUMMARY

Systems Engineering Laboratories, which now identifies itself as SYSTEMS instead of SEL, continues to expand its product line of 32-bit minicomputers. The previously existing 32/75 has been joined by the 32/30A MAXIBOX, the 32/57, and the 32/77. The 32-bit machines' inherent ability to address large amounts of memory directly has been combined at SYSTEMS with interleaved and overlapped memory techniques and memory management to produce systems with high throughput as well as multiple-user and high-volume capabilities. SYSTEMS' processors are suitable candidates for any applications where large volumes of information must be processed. Applications falling into this category include laboratory and scientific computation, simulation, power plant monitoring and control, and seismic processing.

These features are implemented to the greatest degree in SYSTEMS' highest-performance processor, the 32/77. This processor, along with the MAXIBOX, the 32/57, and the 32/75, constitute the present offerings in the SYSTEMS 32 Series.

The original 32 Series was announced in January 1975 and marked the beginning of a new trend in minicomputers: the 32-bit machine. The 32-bit computer was far from new; the IBM System/360 and System/370 computers were 32-bit systems, and SYSTEMS itself marketed the medium-scale 32-bit 8500 and 8600 in the late 1960's. But by no stretch of the imagination could the 360/370 and the 8500 and 8600 have been looked upon as minicomputers. In the development of minicomputers, ▷

CHARACTERISTICS

MANUFACTURER: Systems Engineering Laboratories, Inc., 6901 West Sunrise Boulevard, Fort Lauderdale, Florida 33313. Telephone (305) 587-2900.

Systems Engineering Laboratories, Inc., formerly known as SEL but now called SYSTEMS, was founded in 1961 as a manufacturer of data measurement products and custom data acquisition systems. The company's first systems generated data tapes to be processed off-line by digital computers. The company today is a minicomputer manufacturer whose primary aim is to provide computer systems for a broad range of engineering, scientific, and industrial real-time applications. SYSTEMS has 1,296 employees, with the largest percentage of its staff located in Fort Lauderdale. SYSTEMS' sales are approximately 75 percent domestic and 25 percent foreign, with a customer ratio of 65 percent industrial and 35 percent governmental.

MODELS: 32/30A, 32/57, 32/75, and 32/77.

DATE ANNOUNCED: 32/30A, June 1978; 32/57, June 1978; 32/75, April 1977; 32/77, June 1978.

DATE OF FIRST DELIVERY: 32/30A, September 1979; 32/57, April 1979; 32/75, January 1978; 32/77, June 1978.

NUMBER INSTALLED TO DATE: 32/30A, 10; 32/57, 10; 32/75, 325; 32/77, 275.

DATA FORMATS

BASIC UNIT: 39-bit word (32 data bits plus seven ECC bits) in the 32/30A, 32/57, and 32/77; 36-bit word (32 data bits plus four parity bits) in the 32/75.

FIXED-POINT OPERANDS: Integers can be 8-bit bytes, 16-bit halfwords, 32-bit words, and 64-bit doublewords. All have the same general format, with the high-order bit used as a sign. Negative numbers are represented in two's-complement form. Any bit in memory can be directly addressed by bit-manipulation instructions. Any bit in any general-purpose register can also be manipulated.

FLOATING-POINT OPERANDS: Two floating-point formats are available: single- and double-precision. In both, the high-order bit is used as a sign and the next seven bits are the exponent. Single-precision fractions are 24 bits ▶

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SYSTEMS 32 Series

16 bits had come to be the widely accepted word length, and 16-bit systems had long accounted for most of the revenues in the minicomputer field. SYSTEMS' commitment to 32-bit machines remained constant, however, even on the firm's entry into the minicomputer market in the face of the overwhelming preponderance of 16-bit machines.

The reason goes back to the company's incorporation in 1961. The commitment then was to custom-built data measuring and acquisition systems employed in industrial process control, simulation, testing of engines and airframes, etc. In the early 1970's, with the maturation of the minicomputer field and the advent of the superminicomputer era, the medium-scale systems market appeared to offer a less attractive future. To meet the challenge of the rapidly changing marketplace, SYSTEMS redirected its research and development capabilities toward an entirely new product line, the 32-bit word machine. These superminicomputers provide high performance at comparatively lower cost while surpassing some of the capabilities of older and larger machines. In addition, the market for 32-bit computers is vastly increased because of the growing demand in more and more fields for an improved performance/cost ratio.

The commitment now is to on-line measurement and acquisition, applications of the type to which the large word size of the SYSTEMS 32 Series lends itself particularly well.

The 32 Series system architecture is based on a 32-bit-wide, high-speed, synchronous, time-multiplexed bus, the SelBUS. Data and commands are passed between the CPU, memory, and I/O subsystems over the SelBUS every 150 nanoseconds. The result is a system throughput greater than 26 megabytes per second. The current 32 Series computers are upwardly compatible with the older 32/35 and 32/55 computers and incorporate all of the features of the 32/55, including 26.67-megabyte per second SelBUS; three-board CPU; floating point instructions; bit, byte, halfword, word, and doubleword operands and memory addressing; instruction lookahead; memory overlapping and interleaving; 600-nanosecond memory; core/MOS memory modules; byte parity (core) or ECC (MOS); intelligent microprogrammed I/O controllers; block-oriented, direct-memory transfers; and upward software compatibility. Additional capabilities of the 32 Series are 16-megabyte memory addressing; hardware memory management; optional high-speed floating-point hardware; support for the new Mapped Program Executive (MPX-32) and Real-Time Monitor (RTM); support for new I/O processors with 16-megabyte addressing, command chaining, and data chaining; support for Writable Control Store (WCS); and support for Regional Processing Units (RPU), the Scientific Accelerator, and the Internal Processing Unit (IPU).

All of the current 32 Series models use the same CPU and deliver comparable levels of performance. The primary

long, while double-precision fractions are 56 bits long. The exponent is biased by 64 (excess 64 notation). Negative numbers are represented in two's-complement form. The fraction is a hexadecimal normalized number with a radix point to the left of the highest-order fraction bit. Single-precision operands are six hexadecimal digits long and double-precision operands are fourteen hexadecimal digits long.

INSTRUCTIONS: The SYSTEMS 32 Series instructions are either 16 bits (one halfword) or 32 bits (one word) long. All operation codes are six bits.

Floating-point instructions have an operation code, a 3-bit general-purpose register designator, a 2-bit index register designator, one indirect bit, a 1-bit operation code modifier, and a 19-bit word-address field.

Memory reference instructions include an op code, a 3-bit general-purpose register designator, a 2-bit index register designator for addressing purposes, one indirect bit, one byte-mode selector bit, a 17-bit word-address field, and a 2-bit byte address field, used in conjunction with the byte-mode selector bit. Bit manipulation instructions substitute a 3-bit bit address for the general-purpose register designator.

Immediate mode instructions are a full word (32 bits) in length but can operate only on halfword operands. This format includes an op code, a 3-bit general-purpose register designator, a 3-bit operation modifier, and a 16-bit immediate operand. Four bits are unassigned in this format.

Register-to-register instructions are one halfword long and include an op code, a 3-bit source register selector, a 3-bit destination register selector, and a 4-bit operation modifier. Bit manipulation instructions substitute a 3-bit bit-address for the destination register selector.

Shift instructions are also one halfword in length. There are two types of shift instructions: single-register and dual-register. Both formats include the op code and a 3-bit general-purpose register selector. Single-register shifts have a one-bit direction selector (left or right) and a 5-bit shift count. Dual-register shifts have a 3-bit destination register selector and a 4-bit operation modifier.

Two types of I/O instructions are included in the 32 Series instruction repertoire: one for use with the PSW mode and the other with the PSD mode.

The I/O instructions used with the PSW mode provide the capability to perform I/O operations between an external device and the lower 512K bytes of memory. These instructions are 32 bits long and include an op code, 7-bit device address, 3-bit operation modifier, and a 16-bit function code.

The I/O instructions used with the PSD mode provide the capability to perform I/O between an external device and up to 16 million bytes of main memory. These instructions also support the command and data chaining features. The word format for these I/O instructions includes an op code, 3-bit register field, 4-bit sub-op code, 3-bit augment code, 8-bit logical channel address, and an 8-bit subaddress.

Interrupt control instructions include an op code, a 7-bit priority level designator, and a 3-bit operation modifier. The remaining 16 bits are unassigned.

MAIN STORAGE

GENERAL: Two types of main memory are used with the 32 Series computers: core memory and MOS memory. The core memory modules used with the 32/75 contain 32K bytes each. The high density MOS memory modules used

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SYSTEMS 32 Series

PERIPHERALS/TERMINALS

DEVICE	DESCRIPTION & SPEED	MANUFACTURER
MAGNETIC TAPE EQUIPMENT		
9377/9577/9571/9572	9-track, 800 bpi NRZI/1600 bpi PE, electronically selectable recording mode and density, 75 ips, vacuum column, IBM-compatible, 10½-inch reels, 60K/120K bytes/sec	Pertec 9640-98
9361/9561	9-track, 800 bpi, 45 ips, NRZI, tension arms, IBM-compatible, 10½-inch reels, 36K bytes/sec	Pertec 8840A-9
9363/9563/9568/9569	9-track, 1600 bpi PE/800 bpi NRZI, electronically selectable recording mode and density, 45 ips, tension arms, IBM-compatible, 10½-inch reels, 36K/72K bytes/sec	Pertec 8640A-98
PRINTERS		
9223/9225	Drum Printer; 64-character set, 6 or 8 lines per inch, 4 to 14.87-inch paper, 20-ips slew rate, 136 positions; 300 lpm	Dataproducts 2230
9226	Drum Printer; 64-character set, 6 or 8 lines per inch, 4.88 to 16.75-inch paper, 20-ips slew rate, 136 positions; 600 lpm	Dataproducts 2260
9237	Drum Printer; 64-character set, 6 or 8 lines per inch, 4- to 14.87-inch paper, 20-ips slew rate, 136 positions, 900 lpm	Dataproducts 2290
9245	Same as 9225 with 96-character set and 260 lpm	Dataproducts 2230
9246	Same as 9226 with 96-character set and 436 lpm	Dataproducts 2260
9247	Same as 9237 with 96-character set and 600 lpm	Dataproducts 2290
PUNCHED CARD EQUIPMENT		
9210	Reader; 80-column, optical read station, 550-card hopper, 12-bit parallel read, uses CR channel in 9004 TLC controller; 300 cpm	Documation M200
9211	Reader; 80-column, optical read station, 1000-card hopper, 12-bit parallel read, uses CR channel in 9004 TLC controller; 1000 cpm	Documation M1000
PUNCHED TAPE EQUIPMENT		
9260	Reader; 8-track, bidirectional, supply card take-up tanks opt.; 300 cps	Remex RR6500
9262	Reader/Spooler; 8-track, bidirectional, asynchronous; 300 cps	Remex RRS 6500
9264	Punch/Spooler; 8-track, bidirectional, asynchronous; 120 cps	Remex RPS 6121
TERMINALS		
9202	Teletypewriter; 72/80/132 characters per line, 64 ASCII character set, 30 cps	Teletype 43
9203	Alphanumeric CRT; 1920 characters, 24 lines by 80 characters, 5 x 7 dot matrix, 95 ASCII character set, Teletype-style keyboard; up to 19,200 bps	Hazeltine 1500

differences are in the packaging, expansion capability, and type of memory installed.

The smallest member of the 32 Series, the 32/30A MAXIBOX, is designed for real-time requirements and offers complete hardware and software compatibility with the larger configurations. The basic MAXIBOX includes a 32-bit CPU with a mapped memory management system and floating-point firmware, 128K-byte 600-nanosecond ECC MOS memory, ten available slots for memory and I/O expansion, an integral power supply, and a battery backup unit. The MAXIBOX's memory can be expanded to 1024K bytes with no additional chassis or power supplies. It can also address up to 16 megabytes of memory in special configurations. The MAXIBOX features two modes of operation: Program Status Word (PSW), which is RTM-compatible, and Program Status Doubleword (PSD), which is MPX-32-compatible. (A table showing the functional differences between the PSD and PSW modes is included in this report.) There are eight 32-bit general-purpose registers, three of which are available for indexing, and up to 112 priority interrupt levels for I/O, external interrupts, and traps. High-speed floating-point arithmetic, Writable Control Store, the

with the 32/30A, 32/57, and 32/77 are available in 128K-byte and 256K-byte capacities.

All memory modules plug into a Memory Bus which is driven by a Memory Bus Controller (MBC). An MBC can support up to 16 memory modules of the same type. Additional MBC's can be added to the system to accommodate larger memories. The MBC includes a four-word-deep buffer that allows overlapping or interleaving. When overlapping is used, up to four memory modules can be started on consecutive SelBUS cycles (i.e., every 150 nanoseconds). In this way, the system does not have to wait for a full memory cycle before starting another memory operation using another memory module. With overlapping, consecutive memory addresses are located in the same memory module. This arrangement allows the CPU and I/O controllers to be operating concurrently using different memory modules.

Interleaving, a user-selectable option, can be set for 0-, 2-, or 4-way interleaving. With interleaving, consecutive memory addresses are located in different memory modules. For example: with 4-way interleaving, four memory modules (or multiples of four modules) are used. Locations 0, 4, 8, 12, etc., would be in the first memory module, and locations 1, 5, 9, 13, etc., would be in the second module. Both overlapping and interleaving are designed to improve system performance by allowing more than one memory module to be operating at any given time.

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Real-Time Option Module, the Scientific Accelerator, and the Internal Processing Unit are available options for the MAXIBOX.

The 32/57 is a medium-size, high-performance computer with 600-nanosecond ECC MOS memory and new packaging techniques which provide maximum performance in minimum space. A universal chassis provides 18 SelBUS slots and houses the CPU, I/O controllers, memory bus controllers, and memory modules. Unused SelBUS slots can be used for additional controllers or memory modules. Basic memory size is 256K bytes, which can be expanded to a maximum of one megabyte. The 32/57 operates in the PSW and PSD modes and has eight 32-bit general-purpose registers and up to 112 priority interrupt levels. Available options include fast floating-point arithmetic, Writable Control Store, Regional Processing Units, Real-Time Option Modules, the Scientific Accelerator, the Internal Processing Unit, and multiprocessor options.

The 32/75 is a core memory computer that uses separate chassis and power supplies for memory and logic modules, providing maximum flexibility for configuring large single-processor systems or multiprocessor systems using shared memory. The 32/75 is available with 32K-byte 600-nanosecond memory modules. Maximum memory capacity is eight megabytes. The architecture is built around multiple high-speed, synchronous, shared, multiplexed buses: the SelBUS and one or more memory buses. The 32/75 has eight 32-bit registers and up to 112 priority interrupt levels. Options include additional external interrupts, additional real-time clocks, interval timers, high-speed floating-point, Writable Control Store, the Scientific Accelerator, the Internal Processing Unit, memory ports, memory modules, and real-time interfaces. The 32/75 operates in the PSW and PSD modes.

The most powerful member of the 32 Series, the 32/77, employs 600-nanosecond ECC MOS memory and has a maximum capacity of 16 megabytes. Four megabytes can be put into a single memory chassis by using 256K-byte modules. In addition to the standard 32 Series features, the 32/77 can be enhanced with options which include fast floating-point arithmetic, Writable Control Store, Regional Processing Units, Real-Time Option Modules, the Scientific Accelerator, the Internal Processing Unit, and multiprocessor options. The 32/77 operates in the PSW and PSD modes and is offered in basic nucleus form as well as in packaged systems.

Even though these are 32-bit systems, the data operands for all memory-reference instructions can be 8-bit bytes, 16-bit halfwords, 32-bit words, or 64-bit doublewords. Special bit-manipulation instructions permit addressing individual bits. Despite the fact that memory is organized into 32-bit words, addressing is effectively to the byte level. Therefore, when entering operands into memory, all halfword operands must be on an even byte boundary, fullword operands must be on a four-byte boundary, and doubleword operands must be on an eight-byte boundary.

The MBC used with all 32 SERIES computers also supports shared memory configurations with up to four CPU's sharing memory. For shared memory systems with up to eight CPU's, a Multiprocessor Shared Memory Option and Memory Access Routes are available.

In situations where memory must be installed in a chassis remotely located from a CPU, Memory Bus Adapters (MBA) are used. The MBA allows memory to be up to 20 feet from the CPU and induces a 300-nanosecond delay for read operations. Therefore, using 600-nanosecond memory modules in a remote chassis, the access time for read operations is 900 nanoseconds. Because of the buffer in the MBA, memory write operations are not affected and memory write operations to a single memory module can occur at 600-nanosecond intervals.

TYPE: 32/75, core; 32/30A, 32/57, and 32/77, ECC MOS.

CYCLE TIME: The full cycle time for 32 Series memories is 600 nanoseconds for a full 32-bit word. Effective cycle time is dependent on the degree to which overlapping and interleaving are implemented. Typical effective cycle time is 300 nanoseconds. Read access time is degraded by 300 nanoseconds for remote memory in the system.

CAPACITY: All current 32 Series computers are capable of addressing up to 16 million bytes of main memory. Physical packaging considerations and memory module densities limit the inherent and maximum memory for each computer as shown in the table below:

CPU Type	Memory Type	Increment	Included Memory	Maximum Inherent Capacity	Maximum Expansion
32/30A	MOS	128KB 256KB	128KB 256KB	512KB 1,024KB	—
32/57	MOS	128KB 256KB	128KB 256KB	512KB 1,024KB	—
32/75	CORE	32KB	128KB	256KB	8MB
32/77	MOS	128KB 256KB	256KB 256KB	2MB 4MB	8MB 16MB

The inherent capacity is defined as the amount of memory that can be added to a basic system without having to provide any additional chassis or power supplies. The maximum memory expansion is achieved through the use of optional memory carriages or memory support packages. These options include a memory chassis, power supply, and MBC.

CHECKING: One parity bit per byte is standard in core memory (32/75). Parity is inserted during writing and checked during reading.

MOS memory is organized in 39-bit words: 32 bits of data and seven Error Checking and Correction (ECC) bits. During write operations, the ECC bits are generated and stored in memory. When a read operation takes place, the ECC bits are checked. All single-bit errors are detected and corrected. All double-bit errors and most multiple-bit errors are detected. If two bits are in error, an error signal is generated.

STORAGE PROTECTION: Write protection is provided for individual memory pages. Up to 256 512-word pages can be protected at a time. The memory protect registers can be changed by executing privileged instructions.

In addition, the memory management feature in Program Status Doubleword mode provides memory protection for each 32K-byte memory block of logical program address space. One protect bit is associated with each 32K-byte memory block.

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One outstanding feature of the 32 Series is the inclusion of floating-point firmware as a standard feature. Coupled with 35-nanosecond internal registers and 65-nanosecond scratchpad memory (not accessible to the user), the firmware enables the CPU to perform floating-point operations nearly as fast as fixed-point. The 32 Series can perform floating-point operations still faster if the high-speed floating-point option is installed. With this option, execution speeds can be improved by as much as a factor of two for single precision and five for double precision.

The Writable Control Store (WCS) option allows for user expansion of the instruction set and thus for enhanced performance on user programs. Up to 4096 64-bit words of random access memory (RAM) can be added in increments of 2048 64-bit words.

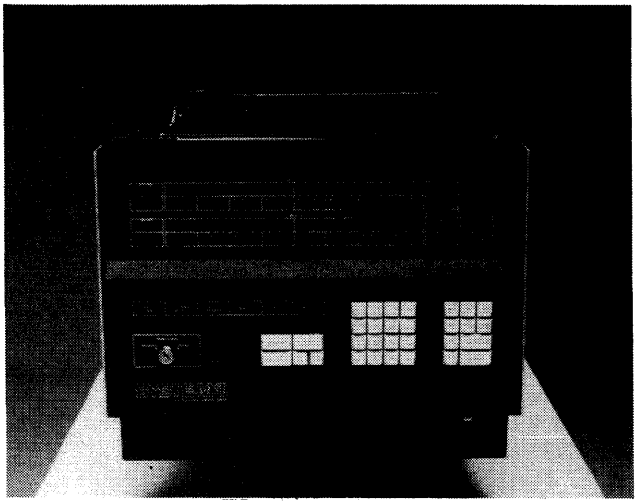
The Scientific Accelerator (SA) option provides FORTRAN system performance improvements of from 10 to 30%. This is accomplished by placing some more frequently used FORTRAN run-time library routines in firmware. Two versions of the SA are available: a low-cost PROM implementation and a more flexible RAM version.

The Internal Processing Unit (IPU) is another option that provides significant performance improvements. It is in reality a second CPU and plugs into the SelBUS to provide almost twice the performance of a single CPU at a fraction of the cost.

The I/O capacity of the 32 Series computers is dependent on the number of available SelBUS slots in the system. These SelBUS slots can be used for I/O controllers as well as CPU options. Two basic types of I/O controllers are available: IOM-based (Input/Output Microprocessor) controllers and RPU-based controllers. IOM-based controllers are generally implemented on wire-wrap boards and require two SelBUS slots. These controllers provide block-oriented transfers between memory and an external device. IOM-based controllers make use of the CD/TD instructions and have an addressing limitation of 512K bytes. RPU-based controllers are implemented on etched copper boards and require only one SelBUS slot. In addition to the capabilities offered by IOM-based controllers, RPU-based controllers offer extended addressing to 16 million bytes, command chaining, and data chaining.

The minimum MAXIBOX nucleus is priced at $25,100. This includes a 15-slot chassis with CPU, 128K bytes of 600-nanosecond MOS memory, turnkey panel, power supply, and battery backup. Ten SelBUS slots are available for options and additional memory.

The large 32/7760 packaged system, priced at $109,900, includes a 32/77 nucleus in a double cabinet with ten available SelBUS slots, 512K bytes of 600-nanosecond ECC MOS memory, an 80-megabyte moving-head disk subsystem, 75-ips magnetic tape, a 600-lpm line printer, a 300-cpm card reader, CRT console device, RTM operating system, Macro Assembler, and control panel with hex display.



The SYSTEMS 32 SERIES 32/30A, the MAXIBOX, includes 10 available SelBUS slots, CPU, 128K bytes of 600-nanosecond MOS memory, turnkey panel, power supply, and battery backup at $25,100. Three optional additional 128K-byte memory modules can be configured.

RESERVED STORAGE: 208 words of low-order memory are reserved for interrupt vectors in all SYSTEMS 32 systems. If more than one real-time option module (RTOM) is added, 320 extra memory locations are reserved for the additional interrupts.

CENTRAL PROCESSOR

GENERAL: All current SYSTEMS 32 Series computers including the 32/30A, 32/57, 32/75, and 32/77, use the same CPU. The CPU is implemented on three etched copper boards and features a hardware memory management system and two modes of operation (PSD and PSW). The functional differences between these modes are shown in the following table.

CPU Modes of Operation

Characteristics	PSW Mode*	PSD Mode**
Program Status	Word	Doubleword
Number of Instructions	162	186
Integrity Features	Interrupts on first RTOM	Traps
Memory Addressing		
Nonmapped		
Nonextended	512 KBytes	512 KBytes†
Extended	1 MByte	1 MByte†
Mapped		
Nonextended	None	512 KBytes per user in 16 MBytes
Extended	None	1 MByte per user in 16 MBytes
CD I/O	Yes	Yes
Addressing	512 KBytes	512 KBytes
Extended I/O	No	Yes
Addressing	None	16 MBytes

* RTM supported
**MPX supported
† No software support

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The available peripheral equipment includes disk processors (16-megabyte addressing, command and data chaining), moving-head disks, cartridge disks, fixed-head disks, tape processors (16-megabyte addressing, command and data chaining), magnetic tape, card equipment, printers, paper tape equipment, terminals, regional processing units, data communications, and interfaces.

All SYSTEMS software is classified by its licensing status and level of support. The definitions of these classes of software are:

A1—Standard Product Software

A2—Application Software products

B1—Software products which are fully-supported and non-licensed

B2—Applications Software Products which are non-licensed and not fully supported

B4—Software which includes user exchange software packages.

Software Communications Service (SCS) is available on an annual subscription basis. Subscribers receive one copy per subscription of the bi-monthly Software Communications Memo (SCM). This document reflects all standard SYSTEMS software products and contains announcements of the introduction of new products, notices of new releases of existing products, other miscellaneous software news, Software Problem Report (SPR) summary by product, and technical notes and helpful hints.

Software Update Services (SUS) are available on a per software product per facility annual subscription basis for Class A1 standard software products which are licensed on a per system basis. The Software Distribution Service (SDS) is a packaged software support plan that is available to all RTM users on an annual subscription basis for each installation.

SYSTEMS provides standard time-and-materials maintenance service through service centers in 19 U.S. cities and one Canadian city. Six U.S. cities also serve as regional parts depots.

USER REACTION

During December 1979, Datapro interviewed five users of SYSTEMS 32 Series computers who had a total of 63 systems. All were using the RTM operating system, and four were programming with FORTRAN and three with the SYSTEMS assembler.

The principal applications mentioned included scientific/engineering computing, real-time control, data base management, flight simulation, software development, data communications, and analysis of naval data. Four users had applications written by in-house personnel; three were using proprietary software packages; and three had used

Earlier models in the 32 Series (32/35 and 32/55) used a similar CPU that was implemented on three wire-wrap boards and supported the PSW mode only. The current CPU occupies three slots on the SelBUS compared to the six slots required by the earlier wire-wrap version. Two of the CPU boards are used for the arithmetic unit while the third is used for the control unit.

The PSW mode of operation is provided to support the Real-Time Monitor (RTM) operating system. This support provides compatibility between the current 32 Series computers and the earlier 32/35 and 32/55.

The PSD mode takes advantage of the newer features such as hardware memory management and extended I/O addressing and is supported by the Mapped Programming Executive (MPX-32) operating system.

The 32 Series computer architecture is centered around a synchronous, time-division multiplexed, 184-line, bidirectional bus. This bus, called the SelBUS, contains 32 data lines and 24 address lines. All functional elements of the system, including the CPU, MBC's, and I/O controllers, plug directly into the SelBUS. Other options such as WCS and Fast Floating-Point also plug into SelBUS slots for power and ground.

A 150-nanosecond system clock is used for timing on the SelBUS. During each SelBUS cycle, a full 32-bit word (4 bytes) can be transferred between the CPU and memory, I/O and memory, or CPU and I/O. This results in an aggregate SelBUS transfer rate of 26.67 million bytes per second.

The 32 data lines and 24 address lines on the SelBUS operate simultaneously. When the CPU wishes to access memory, it places the address of the memory location to be accessed on the address lines and its address on the data lines. This is captured by the MBC, which starts the memory module into its cycle. During the time that the memory module is in its cycle, the SelBUS is free to transfer data or commands between other elements of the system. When the data from memory is available, it is placed on the data lines, the CPU's address is placed on the address lines, and the data is returned to the CPU.

Access by various parts of the system to the SelBUS is handled on a priority basis. Each module that plugs into the SelBUS is assigned one of 23 SelBUS priority lines.

The 32 Series computers employ instruction look-ahead. At any time, the CPU can be executing one instruction, a second instruction can be decoded, and a third instruction can be fetched from memory. With this feature, instruction decoding and fetching do not have to wait for the current instruction to complete execution.

Other performance features include direct addressing of bits, bytes, halfwords, words, or doublewords; pre- and post-indexing; a real-time clock; 32-bit programmable interval timer; and external hardware priority interrupts. For increased reliability and integrity, the 32 SERIES computers feature memory protection, byte parity (core) or ECC (MOS), power fail/auto-restart, and zoned power.

Floating-point arithmetic instructions for add, subtract, multiply, and divide of both single and double precision operands are standard on all 32 SERIES computers. A fast floating-point option, which uses the same instructions, is also available. The following table provides a comparison between the relative performance of the standard and fast floating-point execution speeds:

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contract programming houses. The systems had been in use from nine months to two years, and all had been obtained through purchase from SYSTEMS. Peripherals in use, in addition to the usual disk and tape drives, included plotters, graphic CRT's and color graphics CRT's, an array processor, a display system, and a printer/plotter.

The table below shows how the users rated the SYSTEMS 32 Series computers:

	Excellent	Good	Fair	Poor	WA*
Ease of operation	4	1	0	0	3.8
Reliability of mainframe	4	1	0	0	3.8
Reliability of peripherals	2	2	0	0	3.5
Maintenance service:					
Responsiveness	2	3	0	0	3.4
Effectiveness	3	2	0	0	3.6
Technical support	2	2	0	1	3.0
Manufacturer's software:					
Operating system	2	2	1	0	3.2
Compilers and assemblers	2	3	0	0	3.4
Ease of programming	1	4	0	0	3.2
Ease of conversion	0	1	3	0	2.3
Overall satisfaction	1	4	0	0	3.2

*Weighted Average on a scale of 4.0 for Excellent.

The comments expressed by these users consisted of unstinting praise for the hardware but less enthusiasm for SYSTEMS' support and software. One OEM said that his customers "have had very good service" from SYSTEMS, and another OEM called the equipment "easily reconfigurable to a customer's environment" and "OEM-adaptable and easy to grow." But the most highly praised aspect of the hardware was its speed. This was perhaps best expressed by a government contractor who said the two 32/75's he had were "faster than the 370 in the next room."

However, there was less joy in Mudville regarding what might be called SYSTEMS' paperwork. Documentation was described as poorly organized, with inaccuracies, and costing the customer's time. Another user felt that SYSTEMS was inclined to release "improvements in the operating system (MPX) before the bugs are out." Other complaints were voiced about technical and customer support, getting help with problems, and interfacing to devices and controllers.

The overall impression received from these users, especially the OEM's, who were extremely pleased with SYSTEMS' hardware and equipment but who would like to see improvement in the company's support services.□

Relative Performance = Firmware Floating Point Times / Hardware Floating Point Times

FLOATING INSTRUCTION	SINGLE PRECISION	DOUBLE PRECISION
ADD/SUB	1.62	2.96
MULTIPLY	1.91	4.05
DIVIDE	1.63	4.95

CONTROL STORAGE: 4,096 48-bit words of PROM that operates at 50 to 70 nanoseconds is used in all 32 Series computers.

As an option, the 32 Series computers can also have up to 4096 64-bit words of writable control store (WCS) in increments of 2048 64-bit words. Each increment plugs into the SelBUS for power and clock. WCS is driven by a 13-bit microinstruction address from the CPU and furnishes a 64-bit microinstruction output. The output is divided in such a way that 48 bits are provided for CPU control and 16 bits to drive the high-speed floating-point option. Performance specifications for WCS include arithmetic logic unit operations, shifts, memory access (except read latency), conditional branch, and instruction decode—all executable in 150 nanoseconds. WCS read latency is specified as 450 nanoseconds.

A Scientific Accelerator, based on the standard WCS Option, is also available. This option includes a combination of hardware, firmware, and software. Included with the Scientific Accelerator are frequently used mathematical subroutines, implemented in firmware, from the FORTRAN run-time library. The Scientific Accelerator also provides space for user-implemented subroutines in WCS.

REGISTERS: Eight general-purpose registers are provided. In addition to their use for arithmetic, logical, and data manipulation functions, the first five are assigned special functions including subroutine linking (1), indexing (3), and mask (1). A total of 256 32-bit registers are provided for memory mapping and a 256-bit configuration for program protection. Internally, two groups of 16 by 16-bit 35-nanosecond registers are provided in the IOM. Additionally, there are 256 32-bit, 50-nanosecond scratchpad registers. The arithmetic/logic unit includes a 3-bit status register, which functions to indicate a previous carry, most significant bit, or all-zeroes condition.

ADDRESSING: The address field of all memory reference instructions is 19 bits long, subdivided into a 17-bit word address and a 2-bit byte address. This means that the basic unit of data that can be addressed is one byte, although one 32-bit word is transferred during each memory cycle. Full words are 4 bytes long, halfwords are 2 bytes long, and doublewords are 8 bytes long. Operands can be 1, 2, 4, or 8 bytes long but must be aligned on corresponding boundaries; that is, halfword operands must be on even byte boundaries, words must be on 4-byte boundaries, and doubleword operands must be on 8-byte boundaries.

The 32 Series computer can access memory in four ways: Nonmapped; Nonmapped, Extended; Mapped; and Mapped, Extended.

Nonmapped addressing allows the CPU to access instructions or operands (bit, byte, halfword, word, or doubleword) in the first 512K bytes of memory directly without mapping, indexing, or address modification. A 19-bit address field is provided in memory referencing instructions for that purpose. Bit addressing is accomplished by using the register (R) field in the instruction word to select a bit in the byte specified by the 19-bit address. Therefore, any bit in the first 512K bytes of memory can be directly addressed by the bit-manipulation instructions.

Nonmapped, Extended addressing provides the same capabilities as above, plus it allows operand addressing beyond the first 512K bytes of memory. The effective address (indexed) can reference any bit, byte, halfword, word, or doubleword residing anywhere from 512K bytes to one megabyte of physical memory.

Mapped addressing allows the CPU to access any instruction or operand within a logical primary address space of 512K bytes. This logical address space is mapped into the required number of 32K-byte physical memory blocks, which can be scattered throughout the 16 megabytes of physical memory.

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Mapped, Extended addressing provides all the capabilities of Mapped addressing plus access to a logical extended address space. This space consists of 512K bytes of memory beyond the logical primary address space. It allows users additional memory space to store data (operands). The combination of logical primary address space and logical extended address space is mapped into the required number of 32K-byte physical memory blocks scattered throughout 16 megabytes of physical memory. This mode supports user programs up to one megabyte with all executable code residing within the primary address space.

MEMORY MAPPING: The SYSTEMS 32 Series includes 32 nine-bit registers, the primary map, and the extended operand map. The primary map and the extended operand map are used to map the 512K-byte logical primary address space and the 512K-byte logical extended operand address space, respectively, onto physical memory addresses. Each of the registers associates 32K bytes of the logical primary address space or logical extended operand address space with 32K bytes of physical memory. Logical address spaces are defined by building memory descriptor tables.

Each memory descriptor table is a 24-word array in memory which contains a memory descriptor. The memory descriptor includes an image of the memory protect registers that specifies which 2048-byte pages in the logical primary address space are to be protected, a primary map image that defines a 512K-byte logical primary address space, and an extended operand map image that defines a 512K-byte logical extended operand space. The descriptor pointer table index (DPTI) enables the computer to run either unmapped, where DPTI equals zero, or mapped, where DPTI is not equal to zero.

INSTRUCTION REPERTOIRE: The instruction repertoire in the 32 Series includes 187 standard instructions, only 162 of which can be executed in the PSW mode. The functional classifications and number of instructions in each class are summarized in the following table.

Class	PSW Mode	PSD Mode
Fixed-point arithmetic	30	30
Floating-point arithmetic	8	8
Boolean	17	17
Load/store	30	31
Bit manipulation	8	8
Shift	13	13
Interrupt	5	11
Compare	11	11
Branch	9	10
Register transfer	13	13
Input/output	2	11
Control	11	17
Hardware memory management	2	4
Writable control store	3	3
Total instructions	162	187

The eight bit-manipulation instructions provide the capability to test and set, test and zero, add to, or simply test any selected bit in any memory location within 512K bytes of memory or in any general purpose register.

Instructions are either halfword (16 bits) instructions or word (32 bits) instructions. The word instructions primarily reference memory locations, while the halfword instructions deal primarily with register operands. Because approximately one-third of the instructions are halfword instructions, program memory space is conserved by packing two consecutive halfword instructions into a single memory location. The two instructions are fetched simultaneously, necessitating fewer memory accesses and making programs execute faster.

INSTRUCTION TIMINGS: SYSTEMS feels that the execution times of instructions is so data-dependent and program-dependent that any attempt to quote exact times becomes meaningless.

INTERRUPTS: The basic CPU interrupt facility is provided through the real-time options module (RTOM), which includes 16 interrupt levels, a real-time clock, and a 32-bit interval timer. The maximum number of user interrupt levels is 112, each with a separate priority. There are two RTOM's, the basic unit and the expansion unit. The basic RTOM is included in any SYSTEMS 32 system and includes the fundamental ten system interrupts (power fail, system override, memory parity, arithmetic exception, console interrupts, nonpresent memory, undefined instruction, privilege violation, call monitor, and real-time clock) plus the six highest user I/O interrupts. One of these may be used for the interval timer. RTM also requires three external interrupts for operating system control functions. The expansion RTOM includes I/O interrupts only.

Interrupts force an indirect branch through the vectors stored in a dedicated memory location. The program status word, which includes the program counter contents, is automatically stored at the beginning of the interrupt service routine.

All interrupt levels can be selectively enabled, disabled, activated, deactivated, or requested under software control. Interrupt control instructions are all privileged; attempts at user execution of these instructions will lead to a privilege violation. All I/O interrupts signal that the requested I/O operation has been completed either normally or abnormally.

In the PSD mode, only four of the basic integrity features require interrupts provided by the first RTOM. These are system override, console interrupt, Call Monitor, and the real-time clock. The other six integrity features are implemented using traps.

PHYSICAL SPECIFICATIONS: SYSTEMS 32 systems are packaged in one- or two-cabinet configurations which contain several chassis. Cabinet-mounted systems are 71.1 inches high and 32.5 inches deep. Single-cabinet systems are 25 inches wide, and two-cabinet systems are 48 inches wide. System weights vary between 595 and 1473 pounds, and heat dissipation varies from 6,300 to 18,851 Btu's per hour, depending on configuration.

Power requirements for all SYSTEMS 32 Series computers are 230V ±10 percent at 50 or 60 Hertz ±2 percent except for the 32/30A, which uses 115V. Current requirements vary from a minimum of 8 amps to a maximum of 24 amps, depending on the system.

OPERATING environment for all SYSTEMS 32 Series computers is 50 to 104 degrees F. and 5 to 95 percent relative humidity, noncondensing.

INPUT/OUTPUT CONTROL

I/O CHANNELS: The SYSTEMS 32 Series processors have a common-bus architecture in which the bus (SelBUS) is shared between all processor functional blocks, memories, and I/O controllers. Two basic types of I/O controllers are used with the 32 SERIES computers: IOM-based controllers and RPU-based controllers. Génerally, the IOM-based controllers are implemented on wire-wrap boards that use two SelBUS slots. These IOM-based controllers use the CD and TD I/O instructions and have the capability for performing I/O operations between an external device and the lower 512K bytes of memory.

The IOM is a microprocessor-driven unit that interfaces different peripheral devices to the SelBUS merely by imple-

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menting different firmware in control storage and satisfying specific interface requirements. The input/output microprogrammable processor (IOM) receives 64-bit commands from the CPU and performs all data transfers between itself and memory. In addition to specifying the operation, the I/O doubleword specifies the transfer count, memory buffer address, and format (byte, halfword, or word).

There are two general styles of specific IOM's: multiple-device IOM's, which control several similar devices (e.g., four tape transports), and multiple-controller IOM's for controlling several nonsimilar but low-speed I/O peripherals.

Individual IOM's are capable of block data transfer rates of 1.2 million bytes per second (300K transfers per second). Concurrently operating IOM's, in conjunction with overlapped and/or interleaved memory, permit transfer rates of up to 26.67 million bytes per second (6.67 million 4-byte transfers per second).

The second type of I/O controller used with the 32 Series computers is the newer RPU-based controller. Currently implemented for disks and magnetic tape, these I/O processors provide the capability for performing I/O operations between an external device and 16 megabytes of main memory. The RPU-based Disk Processor and Tape Processors also feature command and data chaining and single-slot copper boards.

SIMULTANEOUS OPERATIONS: All functional units of the SYSTEMS 32 Series computers are asynchronous devices operating on a common bus. As such, the CPU, I/O microprocessors, and memories can be operating concurrently and independently of each other. Up to four memory modules can be simultaneously executing a cycle (four-way overlap). In addition, two- or four-way interleaving is available with the 600-nanosecond core memory. See the I/O Channels section (above) for further details.

CONFIGURATION RULES

The physical packaging for each of the different 32 Series computers is different. The 32/30A and 32/57 computers both use a single universal chassis for housing the CPU, I/O, and memory. The 32/75 and 32/77 computers are larger multi-chassis systems that use separate chassis for logic and memory.

The 32/30A universal chassis includes 15 SelBUS slots which can be used for the CPU, memory, or input/output controllers. A typical 32/30A configuration using one 256K-byte memory module would require eight slot allocations (three for the CPU, and one each for the memory module, a memory bus controller, a real-time option module, a TLC controller, and a disk controller). The remaining seven available slots can be used to accommodate either additional memory (up to a total of four modules) or I/O controllers and interfaces. Processor options such as High-Speed Floating-Point (3 slots), Writable Control Store, and Regional Processing Units (RPU) can be added. The 32/30A can be installed in any standard 19-inch rack and includes its own power supply and battery backup unit.

The 32/57 universal chassis includes 18 SelBUS slots which may be used for CPU, memory, or I/O controllers in any mix between memory and I/O controllers up to a maximum of four memory modules (one megabyte). A typical configuration using two 256K-byte MOS memory modules would require nine slot allocations (three for the CPU, two for the memory modules, and one each for a real-time option module, a memory bus controller, a TLC controller, and a disk controller). The remaining nine slots may be used for nine additional I/O controllers or up to two additional memory modules. Such processor options as High-Speed Floating-Point, Writable Control Store, and Regional Processing Units can be added to the 32/57.

The 32/75 is provided in a double cabinet configuration and includes two logic chassis with 31 available SelBUS slots and one memory chassis with a capacity of eight 32K-byte memory modules. Standard equipment on the 32/75 is a TLC controller which provides an interface for the console device (TTY or CRT), a line printer, and a card reader. Memory Carriages and Memory Carriage Extenders are available for expanding the 32/75 memory beyond 256K bytes. Each Memory Carriage includes a Memory Chassis, power supply, and an MBC. Space is provided for eight memory modules. Similarly, the Memory Carriage Extender is used to support an additional eight memory modules in conjunction with the MBC in the Memory Carriage.

The 32/77 computer includes two chassis in its basic form, a logic chassis with 14 available SelBUS slots for options, and a memory chassis with slots for up to 16 memory modules. Depending on the number of additional Memory Support Packages (chassis), the 32/77 can be housed in either a single or double cabinet. A fully expanded 32/77 with 16 megabytes of main memory can be configured in a double cabinet. One cabinet houses the logic chassis and four memory chassis (4 megabytes each) and the second cabinet houses all required power supplies.

Currently available 32 Series computers, with their specific configurations and available SelBUS slots, are listed in the equipment price list at the end of this report.

A number of devices are available to provide custom interfacing to the 32 Series computer. Of particular significance are the 9131 High-Speed Data (HSD) Interface, which is capable of 32-bit block transfers at 3.2 megabytes per second; the 9145 Regional Processing Unit (RPU), which has a maximum throughput rate of 2.4 megabytes per second aggregate; and the 9134 Serial Data Interface (SDI), which has a maximum throughput of 158K 16-bit transfers per second.

The HSD provides an interface between the SelBUS and customer-designed equipment or other SYSTEMS computers. Bidirectional block transfers of up to 262,144 bytes can occur. Simultaneous CPU/HSD and HSD/memory transactions are possible.

The 9145 RPU provides 2048 32-bit words of PROM and 4096 32-bit words of RAM for firmware and data. Special interfaces can be implemented on the RPU by providing firmware and designing the device interface, which for the most part consists of matching signal levels between the RPU's microprogrammable processor and the device. The RPU is designed to serve individual tasks such as communications interfacing and control, mass storage allocation and control, telemetry interfacing, etc. Software support for the 9145 RPU is provided by the Register Transfer Language (RTL), a high-level language designed for writing microprograms. The 9144 RPU is the same unit without the RAM component.

The 9134 SDI is implemented in the IOM format, in that it consists of a SelBUS interface, a microprogrammed processor with a 32-bit control memory, and a serial link interface. The interface is used principally with the 9137 16-bit data terminal, providing the capability for interfacing special devices to the SYSTEMS 32, such as graphic CRT's.

Options each require a specific number of slots of either the memory or SelBUS type. Options and their slot requirements include: the 2345 additional RTOM, one SelBUS; the 2146 System Control Panel, none; the 32K-byte 2152 memory module, one memory; various memory bus controllers, one dedicated slot each in a memory chassis; the

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2178 Memory Interface Adapter, one SelBUS; the 2341 High-Speed Floating-Point feature, two (three on the 32/30A) SelBUS; the 2344 Writable Control Store, one SelBUS; the 2346 System Control Panel, two SelBUS; and the 2366 Memory (Access Route) Port, one SelBUS slot.

SelBUS slot requirements for peripherals and related devices include: the 9144 Regional Processing Unit, one; the 9005 TLC Controller, one; the 9102 General-Purpose I/O Module, two; the 9103 and 9104 General-Purpose Multiplexer Controllers, two; the 9131 High-Speed Data Interface, one; and the 9134 Serial Data Interface, two slots.

All magnetic tape and disk controllers support multiple devices.

MASS STORAGE

Two different types of moving-head disk controllers are available for the 32 Series computers. One is based on the IOM and can transfer data between disk and the lower 512K bytes of memory. The RPU-based controller, called a Disk Processor, provides extended addressing to 16 megabytes of memory and command and data chaining capabilities. Both types of controllers support up to four disk drives with capacities of 80 megabytes and 300 megabytes each. Intermixing of disk types is permitted on the RPU-based controllers.

MODEL 9337 FIXED-HEAD DISKS: Provide a storage capacity of 4 million bytes per drive. A maximum of two drives can be intermixed on one 9014 controller. Data is stored on 256 tracks per drive, with 23 sectors per track and 768 bytes per sector. Average rotational delay is 8.5 milliseconds, and data transfer rate is 1.1 million bytes per second. The 9337 drive is manufactured by Digital Development Corporation (Model 60-256).

MODEL 9520/9320/9523/9323 MOVING-HEAD DISKS: Provide storage for 80 megabytes (9520/9320) or 300 megabytes (9523/9323). Up to four of the moving-head drives can be connected to a controller.

The 9520 (80-megabyte disk) contains five recording surfaces per drive on a 3330-technology removable pack. Three of the five platters are employed for recording, with five surfaces for data and the sixth for servo use. The remaining two platters, located on the top and bottom of the pack, provide protection. The 9520 contains 823 tracks per surface (808 active data cylinders per spindle).

The 9523 (300-megabyte disk) contains 19 recording surfaces per drive on a 12-platter removable pack. The drives employ a technology similar to that of the IBM 3330 applied to the actuator and disk pack design. The top and bottom platters are designed to protect the pack. The bottom surface of the 11th platter is for servo use, leaving platters 2 through 10 and the top surface of platter 11 for data storage. The 9523 contains 823 tracks per surface (808 active data cylinders per spindle).

Bit density for all drives is 6038 bpi, while track density is 384 tpi. Unformatted track capacity and formatted track capacity for all drives are 20,160 and 17,664 bytes, respectively. All drives have 23 sectors per track and 768 bytes per sector. Actual storage capacities in bytes, including spare tracks, are 72,687,360 for the 9520 and 276,211,968 for the 9523. The drives rotate at 3600 rpm, resulting in an average rotational delay of 8.3 microseconds. Track-to-track, average, and across-all-tracks head positioning times are 7, 30, and 55 milliseconds, respectively. Head positioning is performed by a closed-loop proportional servo system driving a voice-coil actuator. The drives have a data transfer rate of 1.2 megabytes per second.

Data security is provided by a write protect feature with positive manual control, electronically inhibiting write functions upon detection of a seek error, track position error, loss of rotational speed, or loss of voltage. The last two malfunctions also cause head retraction. The drives are manufactured by Control Data as Models 9760, 9762, and 9766.

The 9010 Moving-Head Disk Controller, like other standard SYSTEMS 32 IOM devices, is contained on a single plug-in board for direct connection to the SelBUS. The controller is capable of correcting and detecting errors caused by disk pack imperfections. Each sector read is buffered in memory, and an error correction code (ECC) is generated based on Nth-degree polynomials. Errors consisting of up to seven sequential bits are corrected, while errors consisting of up to nine sequential bits are detected with 100 percent probability. Random errors, along with sequential errors exceeding nine bits, have a high probability of being detected. Since the controller itself is in charge of detecting and correcting errors, CPU intervention is necessary only for checking status flags.

The Model 9024 Disk Processor provides all of the same features and capabilities as the IOM-based controller plus 16-megabyte addressing, command and data chaining, overlapped seeks and angular position targeting, and optional dual port capability for multiprocessors.

MODEL 9508 CARTRIDGE DISKS: These 5440-type units provide storage for up to 10 million bytes per drive on one fixed and one removable disk cartridge. The controller and formatter are included. The drives have a bit density of 2200 bpi and a track density of 200 tpi. Model 9508 stores data on IBM 5440-type disks with 406 cylinders per drive, 4 tracks per cylinder, 16 sectors per track, and 384 bytes per sector. Drive capacities are 9,977,586 bytes.

The 9508 has an average head positioning time of 35 milliseconds, revolves at 2400 rpm, and has an average rotational delay of 12.5 milliseconds. Data transfer rate is 312K bytes per second. The drives feature voice-coil positioners, an optical detent system, and a track offset feature to aid in recapturing data from a disk recorded from another source. Model 9508 is a Pertec D3422 drive and will support three additional slave drives.

INPUT/OUTPUT UNITS

See Peripherals/Terminals table.

COMMUNICATIONS CONTROL

For configurations requiring support of only a few data communications lines, the 9122 Asynchronous Data Set Interface can be used. For larger configurations, the 9104 General-Purpose Multiplexer Controller is used with the 9109 Synchronous, 9110 Asynchronous, or 9116 Binary Synchronous Line Interface modules.

9122 ASYNCHRONOUS DATA SET INTERFACE (ADS): Supports four fully software-programmable full-duplex asynchronous communications lines operating at 15 selectable rates up to 9600 bps. Common RS-232C interfaces are accommodated, and parameters such as the number of bits per character are specified under program control. As high rate select option with rates up to 38.4K bps is available for the ADS.

9103/9104 GENERAL-PURPOSE MULTIPLEXER CONTROLLER (GPMC): This IOM supports up to 16 controllers, which may be either peripheral devices or data communications line controllers. The GPMC consists of four functional parts: a SelBUS interface, a microprogrammable processor, an auxiliary memory to store the channel control

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information for each channel, and a multiplexed input/output (MIO) bus in the form of two 9105 GPDC chassis for the 16 controllers. The 9103 GPMC supports 16-megabyte addressing.

The GPMC features 8- or 16-bit data transfers, up to 64K transfers per block, command chaining, and automatic peak throughput control. A system can be configured with one GPMC and 16 GPDC-based controllers, offering a combined transfer rate of up to 1,920,000 8-bit or 16-bit transfers per second without software assistance.

9109 SYNCHRONOUS LINE INTERFACE MODULE (SLIM): Provides one full-duplex or two half-duplex channels with transmission rates of up to 9600 bps. The module is always used in conjunction with the GPMC.

9110 ASYNCHRONOUS LINE INTERFACE MODULE (ALIM): Provides two full-duplex or four half-duplex channels. The ALIM is programmable and handles transmission rates of up to 9600 bps. Like the 9109, the 9110 is always used in conjunction with the GPMC.

9116 BINARY SYNCHRONOUS LINE INTERFACE MODULE (BLIM): Provides one half-duplex channel with rates of up to 50,000 bps.

SOFTWARE

The 32 SERIES computers are available with a choice of two operating systems, a choice of programming languages, and a variety of related software packages. All SYSTEMS software is classified by its licensing status and level of support. The definitions of these classes of software are as follows:

A1—Standard Product Software is discountable, fully supported by SYSTEMS and is available to customers under SYSTEMS License Agreement.

A2—Application Software products are available under SYSTEMS License Agreement. Support, discounts, and warranty varies for individual products. Source is not available for any class A2 product.

B1—Software Products are fully supported nonlicensed software. Source for these products is available subject to the conditions in SYSTEMS Proprietary Agreement for Source Material.

B2—Applications Software Products are nonlicensed products and are not fully supported by SYSTEMS.

B4—Software includes user exchange software packages. This software is distributed as submitted to the User's Group Library and is not warranted or supported by SYSTEMS. The charge for Class B4 Software only covers the distribution media.

Class A1 and A2 Software Products are available to customers subject to the terms of SYSTEMS License Agreement. A Single System Binary License is available for Class A1 or A2 products. This perpetual license is granted for specific products for use on a designated 32 Series computer system. The Single System Binary License includes one machine-readable copy of the product binary on 9-track magnetic tape, one copy of documentation, 12 month warranty, and a 12 month subscription to the Software Update Service (SUS). The first copy of a Single System Binary License for class A1 or A2 is non-discountable. Additional copies for class A1 are subject to Discount Schedule III. Class A2 products are discounted on a per product basis.

A Facility Source License is available for Class A1 products. This license is granted for a specific product at a designated facility. The facility may include multiple 32 Series computer systems; however, each system must be covered with a Single System Binary License. The Facility Source License includes one machine-readable copy of the product source, distributed on 9-track magnetic tape. The first copy of a Facility Source License is nondiscountable. Additional copies are subject to Discount Schedule III. Both binary and source licenses are transferable subject to the terms and conditions of the SYSTEMS license agreement.

A Source Listing on microfiche is available for Class A1 products. This listing is for use in conjunction with systems covered with single System Binary Licenses. The first Source Listing is nondiscountable. Additional copies are subject to Discount Schedule III. Class B1 and B2 Binary Software Products are available to 32 SERIES computer users for a one time usage charge. Source for Non-Licensed Class B1 and B2 products is available subject to the terms of SYSTEMS Proprietary Agreement for Product Source Material.

OPERATING SYSTEMS: There are two operating systems available for the SYSTEMS 32 computers: Real-Time Monitor (RTM) and Mapped Programming Executive (MPX-32).

SYSTEMS 32 RTM is a Class B1 operating system that supports simultaneous multiple real-time (foreground) tasks, interactive terminal operations, and batch (background) processing. Sequencing of task executions is regulated by priority levels established when programs are catalogued, but which can be modified at run time. Context switching among tasks is initiated by an event, such as initiation or completion of an I/O transfer, which results in a call from a user program to the monitor for servicing, or by an elapsed-time constraint. A time scheduler, operating as a foreground task, uses interrupts from the real-time clock to update parameters maintained in a queue for time-related tasks. Context switching, if initiated, always gives control to the highest priority task outstanding. Control need not be relinquished by any foreground program. In addition to the priority level control, the programmer has options for relinquishing or not relinquishing control after initiating a monitor call.

The Real-Time Monitor provides 64 software priority levels for controlling the user's foreground programs, system programs, and background programs. All system scheduling is performed by priority. Users can assign multiple programs to any priority level. The software priority levels are used by the Resource Allocator for peripheral and core allocation, by the I/O Supervisor for the queuing of I/O requests, and by the RTM Executive whenever CPU control is allocated.

Programs assigned the batch level (64) or foreground levels 55 through 63 are automatically rolled out to disk if a higher-priority task is to be initiated or restarted and insufficient system resources are available. The programs are restored to memory and restarted upon the completion of higher-priority tasks. Programs with priority level assignments of 1 through 54 are not rolled out.

Overall control of the system can be exercised by the operator through the console keyboard printer. Tasks can be activated, made resident or nonresident (priority level permitting), removed from the queue, or aborted. Resident tasks are always in memory whether or not they are currently active. Nonresident tasks are maintained on disk and must be loaded when activated. Batch jobs can be disk-resident or entered through the system input device specified during system generation or reassigned from the console. An alternate device can be specified as the data source for a batch program, or the data can follow the program control

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card images in the job control stream from the system input device. Task activation can also be controlled through specific directives in currently active tasks.

File access methods supported by RTM include sequential and random. File protection mechanisms are available to prevent unauthorized access to and deletion of permanent files. Protection of individual files may be specified when the files are created, and is based on a one- to eight-character password. In addition, read and write access to a file may be restricted. An installation option is also available whereby user files may be protected on a per-user basis. This option requires that a user key be specified before any access to a given user's files is permitted.

Four spooled system files are maintained on disk for object code, input data, output data to be printed, and output data to be punched. Alternatively, the programmer can elect to utilize I/O devices directly. For high-speed, time-critical transfers, the standard operating system input/output control procedures can be bypassed, with the programmer assuming responsibility for handling the input/output controller directly; this, of course, locks out any other access until released.

By exercising the facilities of the Cataloger, users can create permanent foreground and background tasks. During cataloging, relocatable object modules produced by compilers are loaded and linked internally and externally to library subroutines. The linked body of code thus produced is then sent to a selected permanent file in relocatable format. In addition, the Cataloger places a preamble on this file. This preamble contains a summary of the resources required by the task, such as core, permanent files, and peripheral devices. Once created, a task is known to the system by the name of the permanent file on which it resides. The task may then be activated, saved, restored, or otherwise operated on by invoking its name in the appropriate job control statement, monitor service call, or processor directive.

By specifying whether tasks are privileged or unprivileged, users can dynamically control system security. Tasks designated to run in the privileged mode are free to execute any instruction in the instruction repertoire. They also have read/write access to all memory locations.

Support for all standard peripheral devices is included in RTM. However, direct support for the extensive multiprocessing configurational capabilities is supported only in limited fashion. RTM will support multiple processors sharing a common main memory but only with the processors executing independent job streams. Typically, multiple processors are used to distribute the processing load as well as to provide backup in critical applications, in case one processor goes down. It is feasible to consider running real-time applications in one processor and batch operations in a second, with manual initialization and cutover in case of malfunction.

The Real-Time Monitor offers facilities for conducting communications between individual users, between internal system elements, and between the operator and the system. Users communicate with one another through permanent files. Global Common, and job status flags which can be set and interrogated by monitor service routines.

The operator has control of system configuration to the extent of enabling and disabling external interrupts, activating or deactivating individual peripheral devices, and establishing the memory limits for the batch partition.

Language processors supported under RTM include the Macro Assembler, Extended FORTRAN 66+ compiler, ANS COBOL, and BASIC programming language. Specialized capabilities are supported under the Terminal Support Subsystem for interactive program development and HASP for intelligent remote job entry (see Communications Software).

RTM requires a SYSTEMS 32 configuration with 128K bytes of memory (of which at least 48K bytes are used for the resident portion of RTM), the first RTOM, an operator console, a card reader, a printer, a magnetic tape drive, and a disk storage facility of at least two million bytes.

SYSTEMS 32 Series Mapped Programming Executive (MPX-32) is a Class A1 disk-based, multiprogramming system designed to run on all SYSTEMS 32 Series computers which support memory mapping. These include the 32/30A, 32/57, 32/75, and 32/77. MPX-32 provides real-time processing, multi-terminal interactive processing, and multi-stream batch processing. Tasks operating under MPX-32 can be scheduled for execution because of hardware interrupts, system service requests, interactive commands, job control directives, or the expiration of timers. Multiple copies of a task can be executed concurrently in real-time, interactive, and batch environments.

SYSTEMS 32 Series computers operating under MPX-32 use hardware and software priorities for scheduling and executing tasks. Dependent on the user's requirements and the number of peripheral devices in the configuration, there can be up to 128 hardware priority interrupt and trap levels. The traps are used for exceptional conditions such as power fail-safe/autostart, memory parity, nonpresent memory, undefined instruction, privilege violation, arithmetic exception, and supervisor call. Prioritized interrupts are used for console interrupts, I/O service interrupts, clock interrupts, and external interrupts. User tasks can be connected directly or indirectly to the external interrupts. MPX-32 provides 64 software priority levels for controlling the user's application. All system scheduling is performed by priority. Users can assign multiple tasks to any priority level. The software priority levels are used by the Resource Allocator for peripheral and memory allocation, by the I/O Supervisor for the queueing of I/O requests, and by MPX-32 whenever CPU control is allocated.

Within each of the 64 priority levels, there are six sublevels of software priority which support a software interrupt facility. Each task can execute at five software interrupt priority sublevels in addition to the normal execution priority sublevel, which has the lowest priority of the six.

Software interrupts cause the asynchronous higher priority execution of user-specified software routines to be initiated upon the occurrence of conditions such as intertask message reception, I/O completion, or an interactive terminal user's request for service. MPX-32 achieves responsiveness to real-time requests through the use of a task execution scheduler which is primarily event-driven. Of the 64 software priority levels, the 54 highest are reserved for real-time tasks and are scheduled on an absolute priority basis. Thus, an external event which makes a real-time task eligible for execution will immediately trigger a context switch away from an interactive, batch, or lower-priority real-time task. Time slicing and priority migration are in effect on the time-sliced priority levels, which have the ten lowest software priorities. CPU time is allocated among tasks at these levels by a priority migration algorithm, the objective of which is to ensure that the interactive response time experienced by terminal users is not compromised by compute-bound batch or interactive tasks. Tasks decrease in priority as they become compute-bound and increase in priority when they finish waiting for terminal input or I/O completion. Although a task assigned to one of these ten low-priority levels will be interrupted immediately whenever CPU time is required by a real-time tasks, it is guaranteed a minimum

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amount of CPU time before the CPU is allocated to another task assigned to any time-sliced priority level. Two time values, specified at system generation time, control the frequency with which CPU time is reallocated among tasks executing at time-sliced priority levels.

MPX-32 provides support for real-time processing by its response to external events and by offering a wide selection of task-activation methods. User software may be connected directly to external interrupt hardware priority levels, completely bypassing all executive overhead. Additionally, tasks may be activated or resumed in response to timer expiration, time of day, the request of another task, or an external interrupt to which no user interrupt routine is directly connected. Tasks which must respond immediately to external events may be specified as memory-resident tasks when catalogued. Less time-critical tasks may be swapped to disk when idle to increase the utilization of main memory. Swap scheduling is a complementary extension to task execution scheduling and controls the transfer of tasks between main memory and disk storage. In general, tasks are eligible for swapping unless catalogued as resident. MPX-32 maintains a list of the tasks which are considered memory-resident. The swap scheduler attempts to keep the highest priority, ready-to-run tasks in memory by moving lower priority or suspended tasks to their swap areas on disk and moving the highest priority tasks into memory. Any systems event that affects task residency or the release of memory causes the swap scheduler to re-evaluate its memory residency decisions. Time distribution logic enforces a swapping rotation for compute-bound tasks; however, these tasks are guaranteed a minimum amount of execution time prior to being rotated back to disk storage.

MPX-32 permits up to 64 interactive terminal users to concurrently create, debug, and execute programs. Other interactive features include interterminal communications and the ability to perform console operator functions from any terminal. Although some facilities and processors are dedicated to either the interactive or the batch mode, most facilities, including compilers and assemblers, are available in both modes. Programs compiled or assembled in batch mode may be linked with those produced interactively and then run and debugged interactively. Likewise, programs assembled from an interactive terminal may be linked and executed in batch.

MPX-32 supports the processing of multiple batch streams concurrently with real-time and interactive processing. Batch streams, as a group, can be assigned to operate at any time-sliced software priority level, assuring that multiple batch streams assigned to the same software priority level will have equal access to the system. A multibatch scheduler selects batch jobs for execution based on the availability of resources. The number of batch jobs that can be accommodated is defined at system generation time. Batch jobs may be submitted on punched cards or magnetic tape under control of the console operator, or they may be created, edited, and submitted as disk files by interactive terminal users. Output from batch jobs is stored on disk before being directed by an output spooler to a user-specified printer or other destination.

The *SYSTEMS 32 Terminal Support Subsystem (TSS)*, a Class B1 product, provides services for multiple terminal users, including text editing, interactive BASIC, debugging, and batch job submission. The text editing capabilities provide for creating, deleting, and editing disc-based files. TSS requires a minimum RTM configuration, an Asynchronous Line Interface Module, and appropriate CRT or hard-copy terminals.

LANGUAGES: The major programming languages supported are the Macro Assembler, FORTRAN 66+, FORTRAN 77+, COBOL, and BASIC.

The *Macro Assembler*, a Class B1 product, is a two-pass processor that permits unlimited nesting and recursion of macro structures. It supports the full range of SYSTEMS 32 instructions, with bit, byte, halfword, and word addressing and manipulation capabilities. Many data types, including decimal, hexadecimal, character, bit fields, single and doubleword fixed-point and floating-point representations, can be used by the programmer. Independently assembled program segments can be linked together to form an executable program. Two types of common (DATAPOOL and GLOBAL) data storage are provided to facilitate communication of data values between independent assembly-language and FORTRAN-coded programs. Macro assembly can be made conditional on computed data values or the results of tests.

Nested macros are allowed. Macro coding may be defined within the user's source program or called in from a user-generated library on the system disk. Assembler directives allow production of relocatable code, absolute code, or any combination of the two; provide for storage allocation; and provide for data constant definition. The Macro Assembler requires 32K bytes of memory.

The *FORTRAN 66+ Compiler*, a Class A1 product, supports a superset of ANSI X3.9-1966 FORTRAN IV plus extensions oriented toward real-time applications. Extensions include eleven variable and data types, mixed-mode extensions, in-line assembly coding, coding conventions extensions, array extensions, subprogram extensions, data definition extensions, absolute references, Global Common and Datapool, code optimization, and error diagnostics.

Whereas ANSI Standard calls for five variables and data types, FORTRAN 66+ recognizes eleven: bit, logical byte, logical word, integer byte (8-bit), integer halfword (16-bit), integer word, integer doubleword, real, double precision real, complex, and double precision complex. The ability to manipulate halfwords directly, without packing or unpacking, facilitates the handling of 16-bit analog data. The bit manipulation capability, which allows direct access to individual bits without resorting to masking operations, is important in any application where discrete on-off data must be processed. Direct manipulation of bytes makes it convenient to process data associated with alphanumeric displays, communications equipment, and all types of text processing (e.g., translators and crossassemblers). Type declarations may be implicit or explicit. The IMPLICIT declaration allows extensions and changes to the standard implicit typing of all variables whose names start with I through N as integers, the rest being real. Explicit typing allows overriding the implicit typing for specific variable names. In either case, all eleven types may be used.

FORTRAN 66+ permits complete freedom in mixing items of any arithmetic mode or of any logical mode within expressions as well as in replacement statements. Arithmetic and logical types cannot be mixed, however. The compiler automatically calls the necessary conversion routines.

The programmer can insert assembly language code anywhere within a FORTRAN 66+ program without concern for the status of registers used by the compiler. FORTRAN statement numbers and names, used elsewhere in the program, are also valid within the in-line code. Machine language permissible in in-line coding is a subset of assembly language. The compiler does not require the Macro Assembler to complete compilation but

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generates binary code directly in all uses. The binary outputs of both the compiler and the assembler are compatible; they are therefore processed by the same loader.

Variable names may be of unlimited length, although the compiler retains only the first eight characters. This feature improves the readability of programs.

Flexible I/O provisions are included in addition to standard FORTRAN provisions. A Buffered I/O facility is included that permits using non-SYSTEMS standard record formats and establishing data blocks longer than the system standard of 192 words (768 bytes). Nameless I/O (i.e., inputting variable names as well as values) is supported. Extensions include ENCODE, for conversion of binary values to ASCII independently of an I/O operation, and DECODE, for conversion of numeric fields in source text to binary.

System spooled files (RTM) on disk can be used for data input and output. Random access to RTM disk files is supported. Eight-character alphanumeric strings can be output when a STOP or PAUSE statement is executed to specifically identify the occurrence.

Global COMMON for communication between independent programs is supported along with DATAPOOL common. The latter is implemented with variable symbols and corresponding relative addresses maintained on disk rather than in main memory, thus conserving space; address references are completed at program load time. Access to the DATAPOOL area can be made by variable name without knowledge of the common area layout.

The FORTRAN 66+ compiler is a three-pass processor. Either of two operating systems, RTM or MPX-32, is required as a software prerequisite. In addition, the Scientific Run Time Library is required. Hardware prerequisites for FORTRAN 66+ are a SYSTEMS 32 Series computer in a minimum RTM or MPX-32 configuration (as applicable) and 50K bytes of memory allocated to the compiler.

FORTRAN 77+, a Class A1 product, when combined with the Scientific Run Time Library, meets and exceeds the standards of ANSI X3.9-1978, MIL STD 1753, and ISA S61.1 and S61.2. FORTRAN 77+ extensions fall into four broad categories: FORTRAN-based extensions, PASCAL-based extensions, real-time system-based extensions, and industry-based extensions.

FORTRAN-based extensions include more variable types (bit, byte, halfword, double precision integer, and double precision complex), abbreviated argument lists, null arguments, compound assignment statements, and single statement array initialization.

PASCAL-based extensions include BEGIN-END block constructs, multiple statements per line, end-line comments, infinite line continuation, infinite length variable names, and structured loop controls.

Real-time system-based extensions include Global Common, Datapool, in-line assembly, monitor calls, bit/byte data types, and absolute references. Industry-based extensions include ENCODE/DECODE, NAMELIST, type statement data initialization, asterisk comment lines, and conditional compilation.

The compiler operates in three passes, the largest of which requires approximately 60K bytes of memory. Compilation proceeds at about 1,200 lines per minute. Compiler overlays are nonre-entrant. FORTRAN 77+ programs must be catalogued against the Scientific Run Time Library or the Scientific Accelerator. Either RTM or MPX-32 is required to operate the compiler. Assembly subroutines can be linked to FORTRAN 77+ programs.

FORTRAN 66+ programs are not necessarily 100 percent upwardly compatible with FORTRAN 77+ because of ANSI standard incompatibilities. However, FORTRAN 66+ subroutines can be linked to FORTRAN 77+ programs.

The *SYSTEMS COBOL Compiler*, a Class A1 product, is a multi-phase processor designed specifically to meet the ANSI X3.23 1974 and FIPS 21-1 standards for the COBOL language. SYSTEMS COBOL extensions provide the RTM COBOL programmer with performance optimization, pinpoint diagnostics, and additional statement capabilities. SYSTEMS COBOL is implemented at ANSI Level 2 for all modules except the Segmentation and Library modules (Level 1). The Report Writer and Communication modules are not provided. An interactive debug package allows for symbolic control of COBOL programs via TSS. Also included is the SYSTEMS COBOL Support Library, a collection of programs that perform supplemental I/O, arithmetic, and character-oriented execution-time operations via standard linkage sequences.

The *SYSTEMS BASIC* programming language is compatible with ANSI Standard X3J2 and features string handling and disk file input/output extensions. A total of 28 statements and 14 console commands are included in the interpreter. Additionally, the amount of main memory required for execution is reduced by bringing only part of a BASIC program into memory and paging the remainder from disk space as needed. An immediate mode of operation allows program debugging facilities.

BASIC, a Class B1 product, runs under RTM with TSS and requires a configuration with a minimum of 160K bytes of memory and an asynchronous line interface module or asynchronous data set interface. Terminal support capacity is a function of memory allocation and desired response time.

COMMUNICATIONS SOFTWARE: SYSTEMS presently offers one product in this area, *SYSTEMS 32 HASP*, a Class B1 product, which provides the capability for establishing communications, transmitting job streams, and receiving output between computer systems. A SYSTEMS 32 RTM system with HASP functions with any host system supporting the IBM HASP 3.0 multileaving protocol. The minimum hardware needed to run HASP is a SYSTEMS 32 operating under RTM, a 9104 General-Purpose Multiplexer Controller, and a 9166 BSC Line Interface Module.

DIAGNOSTICS: SYSTEMS provides a set of system diagnostics and peripheral exercisors to simplify maintenance procedures. Individual diagnostic programs are available for execution in a stand-alone environment under the Diagnostic Executive Program. On-line diagnostics that execute under control of RTM include mainframe, floating-point, and magnetic tape routines.

GRAPHICS COMPATIBILITY SYSTEM (GCS): A FORTRAN-based computer graphics system designed for interactive use, with printer/plot graphics both in batch mode and from a terminal, pen/plot graphics, static or add-on CRT graphics, or dynamic CRT graphics. GCS is a Class B4 program included with the User Group Program Library and requires 11.5K bytes of batch background area for FORTRAN.

APPLICATION PROGRAMS: Packages from the company that can be considered applications programs include TOTAL, Instrumenter I/II, the IBM 1130 Simulator, and the SEL Sort. The products are covered below.

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TOTAL, developed by Cincom Systems, Inc., is available from SYSTEMS as a Class A2 product. Single-task and multi-task versions of TOTAL are available for use with the 32 Series computer running under MPX-32. The single-task version can also be used with RTM.

Instrumenter I/II are Class A2 software products that provide optimization and testing assistance. These tools produce optimization and test coverage profiles (i.e., reports) of FORTRAN 66+ and FORTRAN 77+ programs. The profiles follow a top-down strategy with Instrumenter I reporting at the routine level and Instrumenter II at the statement level. The Instrumenters operate on the source FORTRAN program, showing how much time each subroutine or source statement spends executing. This enables real-time users to pinpoint the most critical performance bottlenecks. Typically less than 5 percent of the code accounts for well over 75 percent of the execution time. Once discovered, users can optimize the offending code using any of three methods: hand optimized FORTRAN source, Assembly Language Programming, or customized microcoded routines in Writeable Control Store (WCS).

The *IBM 1130 Simulator* permits any SYSTEMS 32 to emulate the IBM 1130. It runs under RTM as a foreground task and will accommodate 1130 RPG programs. The simulator is specifically designed to assist users in converting from IBM 1130 installations. The simulator also supports the DNA Systems 1130 SORT proprietary software package, which enables sort operations to be performed on the contents of one disc file, consisting of up to 5000 records.

The *SYSTEMS Sort* package consists of three programs designed to function as an integrated system. The File Sort Program is a four-phase program capable of sorting either disk (SYC files included) or tape files with a maximum physical record length of 8192 bytes; two files with identical record formats may be merged before sorting. The File Select Program is a two-phase program capable of selecting from either disk or tape ASCII files with a maximum physical record length of 8192 bytes and producing a new disk or tape file with the selected records. The File Print Program is a two-phase program capable of producing formatted printed reports and counting on level breaks of a specified field composed of up to four scattered subfields from either disk or tape ASCII files with a maximum physical record length of 8192 bytes.

PRICING

POLICY: Systems Engineering Laboratories markets the SYSTEMS 32 systems on a purchase or lease basis to both OEM's and end users. Lease prices are dependent on the term and are calculated according to a lease-term factor which is 0.09 (one year), 0.048 (two years), 0.034 (three years), 0.027 (four years), or 0.023 (five years). The monthly charge is calculated by multiplying the purchase price by the lease-term factor and adding the standard monthly maintenance charges.

All purchase prices include factory installation and configuration. Additional installation charges are made for field upgrading.

The Software Communications Service (SCS) is available on an annual subscription basis. Subscribers receive one copy per subscription of the bimonthly Software Communications Memo (SCM). This document reflects all standard SYSTEMS software products and contains announcement of the introduction of new products, notice of new releases of existing products, other miscellaneous software news, Software Problem Report (SPR) summary by product, and technical notes and helpful hints.

Software Update Services (SUS) are available on a per software product per facility annual subscription basis for Class A1 standard software products which are licensed on a per system basis. SUS provides subscribers with the following items in support of the specified software product during the subscription year: automatic distribution (including magnetic tape media) of one copy per subscription of enhanced software product binary as available (appropriately licensed subscribers also receive the corresponding enhanced software product source or microfiche listings); one copy per system of revised reference and technical manuals as applicable; all the benefits of the Software Communications Service (SCS); and acknowledgement of product enhancement suggestions submitted via SPR and a best efforts attempt to incorporate generally applicable enhancements into subsequent versions of the product.

The Software Distribution Service (SDS) is a packaged software support plan that is available to all RTM users on an annual subscription basis for each installation. The products supported are Real-Time Monitor, Macro Assembler, Basic, Statistical Subroutine Library, Terminal Support Subsystem, and HASP.

The SDS provides users with the following services during the subscription year: automatic notification of new and revised software products as they become avaialble; automatic distribution (including magnetic tape media) of revised product object elements which were previously purchased; automatic distribution (including magnetic tape media) of revised product source elements which were previously purchased; one copy per installation of revised reference and/or technical manuals required with product revision, if applicable; one copy per installation of the bimonthly Software Communications Memo (SCM); guaranteed acknowledgement of any software problem or enhancement suggestion submitted via the Software Problem Report (SPR); and one copy per installation of the bimonthly SPR Summary (included in the SCM).

SYSTEMS offers customer training facilities at its Fort Lauderdale, Florida, headquarters. Information concerning contents and scheduling should be directed to the Technical Training Section of Customer Services.

Courses presently available from SYSTEMS include Computer Concepts, FORTRAN Programming, Assembly Language Programming, RTM I, RTM II, RTM III, RTM IV, RTM to MPX Transition, MPXI, MPX II, GPDC Firmware, Introduction to Programming WCS, Introduction to Programming WCS/RPU, 810B Maintenance, 8500/8600 Maintenance, 32/55 System Architecture, 32/55 to 32/75 Transition, 32/75 System Architecture, Diagnostic Software, Card Reader/Line Printer, Magnetic Tape, Moving-Heat Disk, Cartridge Disk, HSD/GPMC/GPDC Interfaces, Card Reader/Matrix Printer, Magnetic Tape, and System Installation. The price per student is $525 to $575 per course week depending on the particular course.

On-site training can be scheduled at a rate of $4,500 per class week plus round-trip air fare from the Fort Lauderdale area for the instructor(s). Class size is limited to 10 trainees. On-site training requests must be made at least 90 days in advance.

On-site programming services are also available, through the Customer Services organizations, on a scheduled basis, portal-to-portal, plus air fare and expenses, for $55 per hour, $2,000 per week, or $8,000 per month.

Comprehensive maintenance is the recommended plan for all computer systems having consistently high uptime requirements. This type of maintenance plan provides scheduled preventive maintenance visits, timely response to emergency service requests, and replacement parts necessary to keep the

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computer equipment in good operating condition. This service is available for fixed monthly rates for easy budgeting. The monthly maintenance charge is determined by the equipment configuration and proximity to a SYSTEMS' Customer Services Center. The basic rate includes coverage during the Principal Period of Maintenance (PPM) which is from 8:00 a.m. through 5:00 p.m., Monday through Friday, excluding holidays. Extended periods of maintenance for customers requiring coverage during off-shift hours can be arranged for additional charges.

Travel surcharges within the contiguous 48 states are as follows:

	Distance From Service Center	Surcharge Based On Monthly Maintenance Rate
	0- 30 miles	0%
Zone A	30 - 60 miles	5%
Zone B	61 - 90 miles	10%
Zone C	91 - 120 miles	15%
Zone D	Over 120 miles	Quote

For customers with critical response time requirements, site-based service may be provided at the customer's request, provided the basic comprehensive monthly charge is $6,200 or more. If the basic monthly comprehensive maintenance charge is less than $6,200, site-based service may be provided at the customer's request if the customer agrees to pay $6,200 per month for a minimum period of one year.

For customers who do not have high uptime requirements or who maintain their own equipment and need only occasional backup support, SYSTEMS provides service on an hourly basis plus parts and expenses. Customers should contact the nearest Service Center. A purchase order number is required before service will be rendered. All parts required to effect repair will be invoiced at SYSTEMS' current Spare Parts List Price. Time and material labor rates are as follows:

Regular hours: 8:00 a.m. to 5:00 p.m., Monday through Friday, except holidays.

$46.00 per hour including travel time with a minimum charge of 2 hours.

After hours (outside regular hours as defined above).

$52.00 per hour including travel time with a minimum charge of 4 hours.

Resident Support provides dedicated, on-site, full time customer engineers for customers with large, complex systems and applications which require on-site coverage. Resident engineers not only provide on-site support but can act as the customer's liaison to SYSTEMS' Home Office Support Group. Rates for Resident Support for periods of one year or more will be quoted upon request. This plan provides for labor only; spares inventories and provision for replacement parts must be furnished by the customer.

SYSTEMS can offer individually structured programs based upon unique requirements of OEM customers who may require either full-time or part-time support on a scheduled basis. This support service can be arranged to include parts replacement and/or repair based upon customer needs. Contact the nearest SYSTEMS Service Center to arrange for a meeting to discuss this service.

A repair depot located in SYSTEMS' Fort Lauderdale facility is equipped and staffed with technicians to accomplish fault isolation and repair to the component level. All the latest engineering changes are incorporated into updatable assemblies. This repair/update service is provided at fixed prices to eliminate lengthy quotation procedures and open or "will advise" purchase orders. The cycle for 32 Series assemblies is four weeks after receipt of part.

Those customers without adequate spares backup to be comfortable with a normal repair cycle can take advantage of the assembly exchange service. Certain assemblies may be exchanged for new or repaired assemblies at the latest revision level. Assemblies which have been modified, damaged, or obsoleted by an Engineering Change Order are not eligible for exchange. Replacement assemblies will be shipped within five working days after receipt and acceptance of returned assemblies.

SYSTEMS currently maintains service centers in 19 U.S. cities, seven of which serve as area parts depots. International service for SYSTEMS equipment is provided through a network of wholly owned subsidiaries, agents, and distributors. The countries served include Australia, Belgium, Canada, England, France, India, Italy, Israel, Japan, Mexico, the Netherlands, Sweden, and West Germany.

EQUIPMENT: The SYSTEMS 32 Series computers are available as complete packaged systems or can be configured from a nucleus and appropriate memory, peripherals, and software.

The following equipment price list represents SYSTEMS' current offerings in the 32 Series product line. Other equipment, including data acquisition systems (analog and digital I/O), is also available.

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.
PROCESSORS			
2124	32/30A MAXIBOX; nucleus includes integrated single universal 15-slot chassis with CPU, MBC, 128K bytes of 600-nanosecond MOS memory, turnkey panel, power supply and battery backup; provides 10 available SelBUS slots for options and memory with a maximum of three additional 128K-byte modules	$ 25,100	$ 200
2125	32/30A MAXIBOX; includes integrated single universal 15-slot chassis with CPU, RTOM, MBC, 256K bytes of 600-nanosecond MOS memory, control panel with hex display, power supply and battery backup; provides 9 available SelBUS slots for options and memory with a maximum of three additional 256K-byte modules	29,700	245
2013	32/57 nucleus; includes basic computer in a universal chassis with 256K bytes of 600-nanosecond ECC MOS memory, a 1-megabyte expansion capability, 12 available SelBUS slots for options, control panel with hex display, real-time option module, memory bus controller, and power supplies	39,500	295

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EQUIPMENT PRICES

	PROCESSORS (Continued)	Purchase Price	Monthly Maint.
2312	32/75 computer; includes double cabinet configuration with CPU boards, real-time option module, memory bus controller, 128K bytes of 600-nanosecond core memory, memory chassis with expansion capability to support 256K bytes of memory, two logic chassis with 31 SelBUS slots for options, power supplies, control panel with hex displays, and TLC controller	72,300	470
2316	32/75 dual processor package; provides two 32/75 computers in a shared memory, double cabinet configuration that includes two CPU's, 320K bytes of 600-nanosecond core memory, chassis for each CPU, shared memory chassis, logic chassis with 13 SelBUS slots per CPU, two real-time option modules, power supplies, two control panels with hex displays, and two TLC controllers	165,700	1,085
2021	32/77 nucleus; includes CPU with 256K bytes of 600-nanosecond ECC MOS memory, real-time option module, memory bus controller, logic chassis with 14 available SelBUS slots, logic power supply, memory chassis with refresh board and inherent expansion to 4,096K bytes in 256K-byte increments, memory power supply, control panel with hex display	38,100	290
	PACKAGED SYSTEMS		
2325	32/7720 Packaged System; includes 32/77 nucleus (Model 2021) in a single cabinet with 12 available SelBUS slots, 256K-bytes of memory, 10-megabyte cartridge disk, 30-cps console printer, TLC controller, TRM operating system, macro assembler, and control panel with hex display	57,400	550
2329	32/7760 Packaged System; includes 32/77 nucleus (Model 2021) in a double cabinet with 10 available SelBUS slots, 512K bytes of memory, 80-megabyte master moving-head disk, TLC controller, 75-ips master magnetic tape, 600-lpm line printer, 300-cpm card reader, CRT, RTM operating system, macro-assembler, and control panel with hex display	109,900	1,085
	PROCESSOR OPTIONS		
2005	Internal Processing Unit; allows user to run two tasks in the processor simultaneously	15,000	100
2146	Control panel; provides full operator controls and indicators with hex displays to augment the functions of the turnkey panel on the 32/30A	4,000	25
2341	High-Speed Floating Point Option	7,000	60
2343	Scientific Accelerator (WCS) includes WCS module, software license, and firmware	8,000	55
2344	Writable Control Store Option; 2,048 x 64 bits of RAM	7,500	50
2345	Real-Time Option Module; provides 16 interrupt levels, a real-time clock, and a 32-bit interval timer	3,000	20
2346	Systems control panel	5,500	30
2347	Scientific Accelerator (PCS); includes PROM module software and firmware	4,500	35
2348	Expansion Logic Chassis; provides logic chassis with 18 additional SelBUS slots for expanding the 32/77 nucleus	5,500	38
2349	Expansion Logic Chassis; provides logic chassis with 18 additional SelBUS slots for expanding the 32/57 nucleus	6,000	42
	MEMORY OPTIONS		
2135	Master Clock; provides master clock for multiprocessor configurations and systems with remote memory; supports 8 slave clocks in remote or multiprocessor shared memory	2,000	10
2137	Slave Clock	1,200	7
2152	32K-byte 600-nanosecond core memory module	6,300	50
2154	128K-byte 600-nanosecond core memory package	17,000	200
2158	128K-byte 600-nanosecond MOS memory module; for 32/30A or 32/57 computers; maximum 3 per 2124, 2 per Model 2013 with Model 2159	9,300	50
2159	Memory Module Exchange; provides exchange of the 256K-byte memory module included in the basic CPU for two 128K-byte memory modules; allows 4-way interleaving of 512K-byte memory; must be ordered with CPU at time of order (32/30A, 32/57)	6,100	25
2160	256K-byte 600-nanosecond ECC MOS memory module; for use in 32/30A or 32/57 universal chassis	12,500	75
2162	Core Memory Bus Controller; 4-port control provides interface between SelBUS and a shared memory bus with up to 16 32K-byte 600-nanosecond core memory modules; allows up to four 32 SERIES CPU's to share a common memory; features 4-way interleaving and overlapping	6,000	50
2178	Memory Bus Adapter (MBA); provides an interface between a SelBUS and an MBC in a remote memory; can be used with either core or MOS memory	6,000	40
2332	Memory Carriage; supports up to eight Model 2152 memory modules; includes memory chassis and power supply	8,500	75
2336	Memory Carriage Extender; supports up to eight additional memory modules (Model 2152 or 2153) in conjunction with a memory carriage; memory modules must be the same as in the memory carriage being extended	3,900	30
2364	Multiprocessor Shared Memory Options; provides space and power for up to eight Model 2152 memory modules and up to eight Model 2366 Memory Access Routes; each Model 2364 may be expanded by the addition of a Model 2336 Memory Carriage Extender, a Model 2332 Memory Carriage and, subsequently, a second Model 2336 Memory Carriage Extender	14,900	95
2366	Memory Access Route (MAR); provides access to shared memory when using the Multiprocessor Shared Memory Option; one per CPU accessing shared memory	9,900	80
2373	Multiprocessor Shared Memory Option; provides space for up to 16 MOS memory modules and up to 8 memory access routes; supports up to 4 megabytes of MOS memory in 256K-byte increments; includes one Memory Bus Controller that supports up to 16 memory modules	18,500	150
2374	Battery Backup Unit; provides emergency battery backup power for MOS memory on 32/57 or 32/77 computers	5,500	55
2378	128K-byte 600-nanosecond MOS memory module; provides 131,072 bytes of 600-nanosecond ECC MOS memory for 32/77 computer	9,300	50
2379	256K-byte 600-nanosecond MOS memory module; provides 262,144 bytes of 600-nanosecond ECC MOS memory for 32/77 computer	13,500	75

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EQUIPMENT PRICES

	MEMORY OPTIONS (Continued)	Purchase Price	Monthly Maint.
2382	MOS Memory Bus Controller; provides support for up to 16 MOS memory modules in a private or shared memory	6,000	40
2394	MOS Memory Upgrade Package; 600-nanosecond memory modules for one 256K-byte module (32/77)	5,100	25
2395	MOS Memory Support Package; provides space and power to support up to 16 MOS memory modules of the same speed and density; includes memory chassis, MOS MBC, refresh board, and memory power supply	12,500	55
	UPGRADES		
2254	10/80 Megabyte Disk Upgrade; substitution of 80 MB Model 9520 Disk Unit for 10 MB Model 9508 Disk Unit; must be ordered at same time as 32/7720 Packaged System	8,900	50
2256	10/300 Megabyte Disk Upgrade; substitution of 300 MB Model 9523 Disk Unit for 10 MB Model 9508 Disk Unit; must be ordered at same time as 32/7720 Packaged System	22,500	100
	CABINET OPTIONS		
2397	Single CPU Cabinet	3,000	5
2397-1	Single CPU Expansion Cabinet	3,000	5
2397-2	Single CPU Cabinet for Dual Processor	3,000	5
2398	Double CPU Cabinet	4,000	5
2398-1	Double CPU Expansion Cabinet	4,000	5
2398-2	Double CPU Cabinet for Dual Processor	4,000	5
2398-3	Tall Double Cabinet	5,000	5
2399	Bay Extender	1,200	—
2399-1	Tall Bay Extender	1,500	—
	MASS STORAGE		
9024	Disk Processor; with 16-megabyte addressing; provides I/O control for up to four disk drive units; can be used to provide second Disk Processor in conjunction with Model 9326-X Dual-Port Option	15,500	85
9326	Dual-Port Option Kit	2,000	30
9542	Single 80-megabyte Disk Processor Subsystem; includes a Disk Processor, 80-megabyte disk drive, disk pack, and associated cables; can be expanded with up to three additional disk drives	27,000	260
9342	80-megabyte Expansion Disk Drive	17,400	175
9543	Double 80-megabyte Disk Processor Subsystem; same as 9542 except two disk drives and two disk packs	44,000	435
9544	Triple 80-megabyte Disk Processor Subsystem; same as 9542 except three disk drives and three disk packs	60,500	610
9545	Quad 80-megabyte Disk Processor Subsystem; same as 9542 except four disk drives and four disk packs		
9546	Single 300-megabyte Disk Processor Subsystem; includes a disk processor, 300 megabyte disk drive, one disk pack, and necessary cables; can be expanded with up to three additional disk drives	40,500	360
9346	300-megabyte Expansion Disk Drive	31,000	275
9547	Double 300-megabyte Disk Processor Subsystem; same as 9546 except two disk drives and two disk packs	71,000	635
9548	Triple 300-megabyte Disk Processor Subsystem; same as 9546 except three disk drives and three disk packs	101,000	910
9549	Quad 300-megabyte Disk Processor Subsystem; same as 9546 except four disk drives and four disk packs	131,000	1,185
9010	Moving-Head Disk Controller; for up to four 80/300-megabyte disk drives	7,500	45
9508	10-megabyte Master Cartridge Disk Drive; includes 10-megabyte cartridge disk drive, disk pack, controller and formatter; supports up to three additional 9308 slave disk drives	14,000	170
9308	10-megabyte Slave Cartridge Disk Drive	7,500	125
9521	40-megabyte Master Moving Head Disk Drive; includes 40-megabyte cartridge disk drive, disk pack, controller and formatter; supports up to three 9321 slave disk drives	21,000	210
9321	40-megabyte Slave Moving-head Cartridge Disk Drives	15,500	165
9520	80-megabyte Master Moving-Head Disk Drive; includes 80-megabyte disk drive, disk pack, and controller; supports up to three 9320 slave disk drives	22,900	220
9320	80-megabyte Slave Moving-Head Disk Drive; includes disk pack	17,400	175
9523	300-megabyte Master Moving-Head Disk Drive; includes 300-megabyte disk drive, disk pack and controller; supports up to three 9323 slave disk drives	36,500	320
9323	300-megabyte Slave Moving-Head Disk Drive; includes disk pack	31,000	275
9331	Write Protect Switches	1,000	5
9332	Helium Resupply	3,000	15
9337	4-megabyte Fixed-Head Disk Drive; 8.5 ms. average access	30,000	180
9337-1	4-megabyte Fixed-Head Disk Drive; 10.2 ms average access	30,000	180
	TAPE PROCESSOR		
9020	Tape Processor; 16-megabyte addressing provides I/O control for up to four 800/1600-bpi, NRZI/PE magnetic tape transport	9,900	35
9568	Single 45-ips Tape Processor Subsystem; includes tape processor, 800/1600-bpi, NRZI/PE 45-ips magnetic tape transport with tape formatter and interconnecting cables; supports three additional tape transports	17,000	145
9569	Double 45-ips Tape Processor Subsystem; same as 9568 except two tape transports	25,000	225
9571	Single 75-ips Tape Processor Subsystem; same as 9568 except NRZI/PE 75-ips Magnetic tape transport	22,000	165
9572	Double 75-ips Tape Processor Subsystem; same as 9571 except two tape transports	34,000	285

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EQUIPMENT PRICES

		Purchase Price	Monthly Maint.
MAGNETIC TAPE EQUIPMENT			
9561	45-ips Master Magnetic Tape Unit; includes 9-track, 800-bpi, NRZI tape transport, formatter, and control unit; supports three additional 9361 Slave Units	12,500	115
9361	45-ips Slave Magnetic Tape Unit; 9-track, 800-bpi, NRZI	7,600	75
9563	45-ips Master Magnetic Tape Unit; same as 9561 except 800/1600 bpi and supports three 9363 or 9377 Slave Units	15,500	135
9363	45-ips Slave Magnetic Tape Unit; 9-track, 800/1600-bpi, NRZI/PE	9,000	80
9577	75-ips Master Magnetic Tape Unit; same as 9563 except 75 ips	19,900	155
9377	75-ips Slave Magnetic Tape Unit; 9-track, 800/1600-bpi, NRZI/PE	13,400	120
CARD EQUIPMENT			
9210	Card Reader (300 cpm); 550-card hopper/stacker	4,500	55
9211	Card Reader (1000 cpm); 1000-card hopper/stacker	9,000	90
PRINTERS			
9223	Matrix Printer (340 cps)	5,900	75
9225	Line Printer (300 lpm); 64-character set and anti-static option	10,700	90
9226	Line Printer (600 lpm); 65-character set and anti-static option	16,800	150
9237	Line Printer (900 lpm); same as 9225 except 900 lpm	23,500	200
9245	Line Printer (260 lpm); 96-character set and anti-static option	13,800	90
9246	Line Printer (436 lpm); same as 9245 except 436 lpm	18,800	150
9247	Line Printer (600 lpm); same as 9245 except 600 lpm	25,100	200
PAPER TAPE EQUIPMENT			
9264	Paper Tape Punch/Spooler (120 cps)	4,200	40
9460	Paper Tape Reader (300 cps); includes paper tape reader/punch controller	3,100	35
9462	Paper Tape Reader/Spooler (300 cps); includes paper tape reader/punch controller	5,400	47
TERMINALS			
The following devices may be used as a console with the 9005 TLC or as a terminal with the 9110 or 9112 Asynchronous Interface.			
9201	KSR-33 Teletypewriter; 10 cps	1,800	30
9202	Teletypewriter; 30 cps	2,800	30
9203	1920-Character Alphanumeric CRT; 95-character set	2,100	25
9503	CRT Package; includes four 9203 CRT's and a 9122 Asynchronous Data Set Interface	11,100	125
I/O CONTROL			
9005	TLC Controller, for one teletypewriter, one card reader, and one hard-copy printer	3,000	20
9102	General-Purpose I/O Module (GPIO); provides IOM with blank firmware and space for adding customer device interface logic; maximum throughput is 1.2 million bytes/second	2,500	—
9103	General-purpose Multiplexer Controller (GPMC); addresses up to 16 megabytes of memory, supports one MIO bus, 16 MIO channels, maximum aggregate rate is 300K bytes per second	3,500	25
9104	General-Purpose Multiplexer Controller (GPMC): 16-channel multiplexer for use as a general-purpose interface; maximum aggregate rate is 150K transfers per second	3,500	25
9305	General-Purpose Device Controller Chassis (GPDC); provides 18 multiplexer bus slots for GPMC; includes power supply	2,700	22
9305-2	Second GPDC Chassis; provides GPDC with an additional 14 multiplexer bus slots	2,700	37
9106	GPDC; throughput rates up to 240K bytes per second	750	—
9115	GPDC Coupler; one MIO channel/CPU	2,500	15
9132	High Speed Data Interface (HSD); provides 32-bit parallel interface with throughput rate above 3.2 million bytes per second; maximum of one per bus	4,000	30
9134	Serial Data Interface (SDI); provides serial link; emulates the I/O operation of the SEL System 85 and 86	4,000	35
9136	High-Speed Inter-Bus Link for 32-bit parallel transfers	8,500	90
9144	Regional Processing Unit; 2048 32-bit words of PROM	4,000	—
9145	Regional Processing Unit; 2048 32-bit words of PROM and 4096 32-bit words of RAM	14,000	—
COMMUNICATIONS CONTROL			
9109	Synchronous Line Interface Module (SLIM); one full-duplex or two half-duplex channels; rates up to 9600 bps	2,000	20
9110	Asynchronous Line Interface Module (ALIM); two full-duplex or four half-duplex channels; rates up to 9600 bps; programmable	2,000	20
9116	Binary Asynchronous Line Interface Module (BLIM); one half-duplex channel; rates up to 50K bps	2,000	20
9122	Asynchronous Data Set Interface (ADS); provides four fully software-programmable full-duplex RS-232C asynchronous channels with 15 selectable rates to 9600 bps	3,500	25
9122-10	Current Loop Option	600	6
9122-11	Diagnostic Kit	250	3
9122-12	PLO/High Rate Select Option	400	4

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SOFTWARE PRICES

CLASS A1 SOFTWARE (licensed)—Class A1 software is discountable, fully supported by SYSTEMS and is available to customers under SYSTEMS License Agreement.

		Price
1401-001	MPX-32 Binary	3,000
1401-021	MPX-32 Source	6,000
1401-040	MPX-32 Source Listing	1,200
1410-001	Scientific Accelerator Binary	2,700
1410-021	Scientific Accelerator Source	5,500
1410-040	Scientific Accelerator source listing	1,800
1411-001	Scientific Run-Time Library (SRTL) Binary	1,700
1411-002	SRTL Binary (10-megabyte disk)	1,900
1411-021	SRTL Source	3,500
1411-040	SRTL Source Listing	1,100
1412-001	Fortran 66+ Binary	1,900
1412-002	Fortran 66+ Binary (10-megabyte disk)	2,100
1412-021	Fortran 66+ Compiler Source	2,000
1412-040	Fortran 66+ Compiler Source Listing	900
1412-101	Fortran 66+ Compiler Binary	200
1413-001	Fortran 77+ Binary	5,700
1413-002	Fortran 77+ Binary (10-megabyte disk)	5,900
1413-021	Fortran 77+ Compiler Source	9,500
1413-040	Fortran 77+ Compiler Source Listing	3,000
1413-101	Fortran 77+ Compiler Binary	4,000
1420-001	Cobol Binary	6,000
1420-002	Cobol Binary (10-megabyte disk)	6,200
1420-021	Cobol Source	12,600
1420-040	Cobol Listing	2,100
1430-001	Micro Binary	1,500
1430-021	Micro Source	3,150
1430-040	Micro Source Listing	1,050

CLASS A2 SOFTWARE (licensed)—Class A2 software is available under SYSTEMS License Agreement; support discounts and warranty varies for individual products; source is not available for any Class A2 product.

TOTAL (DBMS); includes a data definition language (DDL) and data manipulation language (DML).

1510-001	TOTAL—Single Task Operation	13,000
1511-001	TOTAL—Multi-Task Operation	16,000
1521-001	Instrumenter I Binary	2,500*
1522-001	Instrumenter II Binary	2,500*

CLASS B1 SOFTWARE (non-licensed)—Class B1 software is fully supported nonlicensed; source for these products is available subject to the conditions in SYSTEMS Proprietary Agreement for Source Material.

1001-001	Real-Time Monitor (RTM) Binary	750*
1001-002	RTM Binary (10-megabyte disk)	950*
1001-021	RTM Source	1,500*
1011-031	Macro Assembler Source	750*
1013-001	Basic Binary	250*
1013-002	Basic Binary (10-megabyte disk)	450*
1013-021	Basic Source	1,000*
1043-001	Statistical Subroutine Library (SSL) Binary	75*
1043-002	SSL Binary (10-megabyte disk)	275*
1043-021	SSL Source	250*
1080-001	Terminal Support Subsystem (TSS) Binary	500*
1080-002	TSS Binary (10-megabyte disk)	700*
1080-021	TSS Source	1,155*
1081-001	HASP Binary	500*
1081-002	HASP Binary (10-megabyte disk)	500*
1081-021	HASP Source	700*

CLASS B2 SOFTWARE (non-licensed)—Class B2 software is non-licensed and not fully supported by SYSTEMS.

1189-001	Sort Binary	200*
1191-001	Versaplot Binary	1,200*

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SOFTWARE PRICES

		Price
➤	CLASS B4 SOFTWARE (user-exchange)—This software is distributed as submitted to the User's Group Library and is not warranted or supported by SYSTEMS; charge covers only the distribution media.	
1380-021	User's Group Library	60*
	SOFTWARE SERVICES**	
1001-051	RTM Software Distribution Service (SDS)	800*
1401-051	MPX-32 Annual Software Update Service (SUS)	840*
1410-051	Scientific Accelerator SUS	270*
1411-051	Scientific RTL Annual SUS	180*
1412-051	Fortran 66+ Annual SUS	240*
1413-05	Fortran 77+ Annual SUS	480*
1420-051	Cobol Annual SUS	600*
1430-051	Micro Annual SUS	100*
1510-051	TOTAL Annual SUS	1,000*
1521-051	Instrumenter I Annual SUS	500*
1522-051	Instrumenter II Annual SUS	500*
1901	Software Communications Service	75

*Software prices are non-discountable.
**Prices are for yearly rate.

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