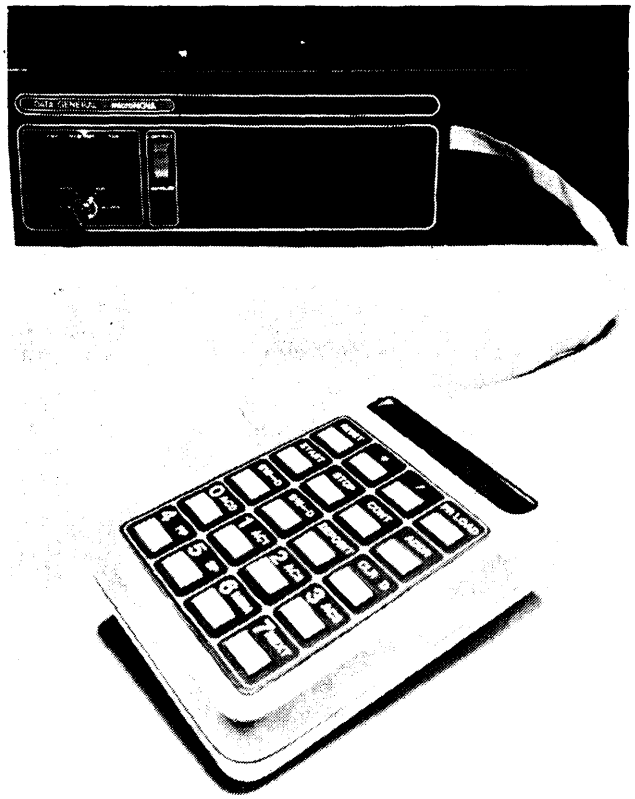
Data General microNova



Among the features of the microNova development system is the hand-held programmer's console in the foreground. The display is in octal; procedures for its use are conveniently imprinted on the rear of the unit. Addressing one memory location allows the user to display the contents of the previous and next locations also. The microNova is the small box in the background. The development system is diskette-based, allowing programs to be written in real-time FORTRAN IV. Control and monitoring are performed by the Disk Operating System, a compatible member of Data General's RDOS family.

MANAGEMENT SUMMARY

Archie Bunker, move over; you don't have an exclusive on the title "All in the Family."

Data General has reinforced and slightly redefined its OEM position with its March 2, 1976 announcement of the 16-bit microNova. In doing so, it has achieved a number of firsts. DG became the first major minicomputer manufacturer to introduce a full microprocessor-based computer line–from chips, through boards, to boxes. Furthermore, the microprocessor is being home-built by DG. Finally the microNova is compatible with the older Nova line, enabling the full range of developed and tested Nova software to be used with the new processor.

It is apparent that integrated-circuit manufacturers are fast becoming a significant factor in the manufacture of minicomputers. In order to take away the strong ▷

By the chip, by the board, or by the box, a Nova by any other name is still a Nova. The microNova is a 16-bit microprocessor in a 40-pin chip package. It is available singly by the chip at $225, by the board at $950, or by the minicomputer at $1,995. OEM quantity prices are available. The microNova is fully compatible with the Nova Series in architecture and utilizes the complete range of Nova software.

CHARACTERISTICS

MANUFACTURER: Data General Corporation, Southboro, Massachusetts 01772. Telephone (617) 485-9100.

Data General is a leading manufacturer of minicomputers, peripherals, and associated equipment. The company maintains sales offices in most major North American cities and in South America, Europe, and Australia. Manufacturing operations are located at the company's Southboro, Massachusetts headquarters; in Westbrook, Maine; and in Sunnyvale, California. Assembly operations are also performed in Hong Kong and in Thailand.

MODELS: microNova Chip Set (model number unspecified); Microcomputer, Models 8562 and 8563; Minicomputer, Models 8560 and 8561; Development Systems, Models 9040, 9041, and 9042.

DATE ANNOUNCED: March 2, 1976.

DATE OF FIRST DELIVERY: Fall 1976.

DATA FORMATS

BASIC UNIT: 16-bit word or 8-bit byte.

FIXED-POINT OPERANDS: 16-bit words can be interpreted as signed or unsigned binary numbers, logical words, memory addresses, or portions of decimal character strings.

Decimal numbers can be either character decimal or packaged decimal. In character decimal format, each digit is an 8-bit ASCII character, and the sign is either carried separately as an extra character at the beginning or end of the decimal string or by modifying either the first or last digit in the string. The packed decimal format places each digit in 4-bit hexadecimal code, with a separate sign character at one end of the string.

FLOATING-POINT OPERANDS: 32-bit single-precision operands with a 7-bit exponent and signed 24-bit fraction; and 64-bit double-precision operands with a 7-bit exponent and signed 56-bit fraction. Single and double-precision floating-point arithmetic is implemented through software subroutines. No hardware floating-point arithmetic is available.

INSTRUCTIONS: One-word instructions. There are four basic instruction types, each with different formats: Jump and Modify Memory, Move Data, I/O, and Arithmetic and Logic. In all instructions, bits 0 through 2 specify the instruction type. ▶

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possibility that these IC manufacturers could ultimately encroach on their territory, companies like Data General had to do something, and fast.

Moreover, effective competition in the low end minicomputer business means cost-cutting procedures—procedures that would eliminate repackaging IC's and placing heavy reliance on original source manufacturers for those IC's. This has led Data General into production of its own chips, and ultimately to the microNova. A strong plus for Data General and similar companies is in the area of software and system support, where the minicomputer makers have a strong advantage over the semiconductor manufacturers.

Data General, however, is not alone in this field. Computer Automation, General Automation, IBM, Microdata, and Texas Instruments have all employed microprocessor chips, in one form or another, as early as 1971. But Data General is the first to manufacture and offer its product as a chip set, on a board as a microcomputer, and in a box as a minicomputer.

For OEM accounts, the microNova offers some interesting possibilities. They can start with a minicomputer development system, and integrate downward to microNovas on boards or to chip sets with a minimum of difficulties. Such a move permits production economies as volume increases, but does not require the heavy front-end investment associated with IC development or software conversion. At this writing, few vendors can make this type of offer.

All the package variations are built around the 40-pin mN601 NMOS microNova processor. The chip has the Nova 16-bit architecture and instruction set, hardware stack and frame pointer with stack overflow protection, 16-bit hardware multiply and divide, real-time clock, all memory control and timing, integral hidden refresh logic for dynamic RAM's, four general-purpose accumulators (two of which can be used for indexing), programmed priority interrupt to 16 levels, CPU and memory control for DMA, and separate memory and input/output buses.

Besides the mN601, the chip set consists of two 20-pin bipolar mN634 Octal Memory Bus Transceivers, sixteen 20-pin NMOS mN606 chips to make a 4K-word RAM (Random Access Memory), two 20-pin bipolar mN633 Octal Memory Address Drivers, four 14-pin bipolar mN506 Quad Sense Amplifiers, a 20-pin mN629 CPU I/O Transceiver, a 20-pin bipolar mN636 I/O transceiver, a PC board, some TTL logic, and passive components. The chip set makes up a 4K-word RAM CPU system, and in a quantity of one, sells for $950.

All components of the chip set are produced by Data General. The mN606 4K-word RAM was introduced with the Nova 3 for first delivery to Megatek Corporation in February 1976. The mN603 I/O Controller (IOC) provides the functions of the 47-line Nova I/O bus by decoding data from a two-line serial I/O bus up to 100 ➤

➤ In Jump and Modify instructions, bits 3 and 4 identify the specific function (op code), and the rest of the word contains information used to calculate the effective address, including an 8-bit displacement, 2-bit index register specification, and 1-bit indicator to specify direct or indirect addressing.

In Move Data instructions, bits 3 and 4 address an accumulator, and the rest of the word is identical in structure to the Jump and Modify type above.

In I/O instructions, bits 5 through 9 specify the function (indication of transfer direction, selection of an I/O device register, and/or specification of an operation). Bits 3 and 4 select an accumulator for transfer, and bits 10 through 15 indicate a specific device.

Arithmetic and Logic instructions use bits 1 and 2 to identify an accumulator containing a second operand (if present), bits 5 through 7 to specify primary function, and the rest of the word to specify secondary functions, if any.

For all memory reference instructions, bits 5 through 15 are used for addressing, using bits 8 through 15 as the displacement or direct address. Each instruction can address 256 words directly, or can use either relative or base register addressing.

INTERNAL CODE: ASCII and binary.

MAIN STORAGE

TYPE: Dynamic MOS RAM, requiring 64 refresh cycles every 2.4 milliseconds. Refresh is overlapped with CPU execution.

CYCLE TIME: 960 nanoseconds.

CAPACITY: 32K words in 4K- and 8K-word increments.

CHECKING: None.

STORAGE PROTECTION: None.

RESERVED STORAGE: The microNova has 16 reserved words which function as auto-increment/auto-decrement registers.

CENTRAL PROCESSOR

The microNova is available as a chip set which includes the mN601 Microprocessor, mN606 4K RAM, and these System Buffer elements: mN634 Octal Memory Bus Transceiver, mN633 Octal Memory Address Driver, mN506 Quad Sense Amplifier, and two I/O Transceivers, mN629 and mN636.

Above this level, the microNova is available as a microcomputer on a 7.5 by 9.5-inch printed circuit board. Model 8562 comes with 2K words of dynamic RAM, while Model 8563 comes with 4K words.

In a minicomputer or development system configuration, the microNova features power fail/auto restart, real-time clock, rack-mountable 9- or 18-slot chassis with CPU and 4K RAM on a single board, operator's control panel, power supply, asynchronous interface boards, general-purpose I/O interface boards, per-device data channel facility, up to 100 feet of external I/O bus, and PROM memory boards.

On the Models 8560 and 8561 microNova Minicomputers, automatic program load, battery backup, and a hand-held programmer's console are optional. These are standard on the Models 9040, 9041, and 9042 microNova Development Systems. Other options for both the minicomputer and ➤

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PERIPHERALS/TERMINALS

DEVICE	DESCRIPTION	MANUFACTURER
TERMINALS		
4010A/E	ASR-33 teletypewriter; 10 cps	Teletype
4010B	KSR-33 teletypewriter; 10 cps	Teletype
6012	CRT display; 1920-character, variable codes, local editing, EIA or 20-ma current loop interface, full or half-duplex; up to 4800 bps	Data General

feet in length. The IOC also performs integral device identification, interrupt logic, and per-device interrupt masking.

The microNova microcomputer on a board combines an mN601 processor with 2K (Model 8562) or 4K (Model 8563) words of RAM, power fail/auto restart, and a real-time clock on a 7.5 by 9.5-inch board. The front edge of the board optionally provides operator panel functions, including lights and switch controls for lock, reset, start program load, and continue. Additional 7.5 by 9.5-inch boards are utilized for 4K or 8K words of RAM; 512, 1K, 2K, or 4K words of PROM; a PROM programmer; and various interfaces. The 2K-word microNova on a board is priced at $800 in a quantity of one.

The microNova as a minicomputer is available in a 9-slot chassis (Model 8561) and in an 18-slot chassis (Model 8560). As a minicomputer development system, the microNova is available in an 18-slot chassis with an ASR-33 teletypewriter (Model 9040), a KSR-35 teletypewriter (Model 9041), or a teletypewriter modification kit for the user's choice of terminal (Model 9042).

Both the minicomputer systems and the minicomputer development systems (MDS) are available with a diskette subsystem. On the minicomputer, the user may elect either 157K words (315K bytes) in a single diskette drive or 315K words (630K bytes) on a dual diskette drive. The MDS is available with a dual diskette drive as standard equipment. The diskette subsystem includes a DMA controller.

The minicomputer prices start at $1,995 for the Model 8561 in a single-unit quantity. MDS prices start at $10,715, not including the 72-inch cabinet. Power fail/auto restart and real-time clocks are standard on both the minicomputer and MDS, whereas automatic program load, battery pack, hand-held programmer's console, and rack cabinet are optional on the minicomputer but standard on the MDS. Other standard features of the minicomputer and MDS are additional RAM and/or PROM memory up to 32K words, asynchronous interface boards, addressability for up to 61 peripherals, and up to 100 feet of external I/O bus. Optional features include the PROM programmer, 9-slot expansion chassis, card frames, extender cards, and device connector cables.

development systems include PROM programmer, expansion chassis, card frames, and extender cards.

CONTROL STORAGE: 0.5K, 1K, 2K, or 4K words of PROM (programmable read-only memory) are available for the microNova. Each size of PROM module is separately mounted on a memory board. A PROM programmer on its own board permits PROM chip burning under program control. The programmer acts directly on the PROM board and is inserted in the chassis only when needed.

REGISTERS: The microNova has four 16-bit accumulators and a 15-bit program counter. Two accumulators can be used for address indexing.

The microNova, like the Nova 3, has a last-in/first-out (LIFO) push-down/pop-up stack implemented in any 256 consecutive memory locations and two additional hardware registers (the stack pointer and the frame pointer). The stack pointer identifies the first memory location designed as the stack, and the frame pointer marks intra-stack boundaries to permit several "register saves" to be accumulated in the stack. The frame pointer can be set randomly to access words stored in stack frames without popping an entire frame.

Also, like the Nova 3, the microNova has 16 reserved memory locations which function as auto-increment or auto-decrement registers when addressed indirectly.

ADDRESSING MODES: The microNova has six addressing modes: direct (256 words), indirect (multi-level), indexed, indexed-indirect (pre-indexing), program-relative, and program relative-indirect.

INSTRUCTION REPERTOIRE: The basic complement includes four Jump and Modify Memory instructions, two Move Data instructions, 16 I/O instructions, and eight Arithmetic and Logic instructions. There are 256 variations on each of the Arithmetic and Logic instructions. Hardware multiply/divide instructions are standard.

INSTRUCTION TIMINGS: The timings shown are for full-word, fixed point operands, in *microseconds.*

Load/Store	2.88
Add/Subtract	2.4
Multiply/Divide	41.28/59.04
Jump	2.88

INTERRUPTS: A 16-level programmed priority interrupt facility is used to recognize interrupts for I/O operations. Each device is wired to one of 16 bus positions, and is either authorized or denied authorization to interrupt particular service routines by an Interrupt Disable Mask Bit that corresponds to the bus positions of the device.

PHYSICAL SPECIFICATIONS: The microNova in a minicomputer configuration is housed in a chassis of either

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Nova 3/4 and 3/12 development systems are available for users who need more power in system development.

Beside the aforementioned support by a wide range of Nova software, the microNova has its own development software. This is a special package consisting of the Disc Operating System, Command Line Interpreter, Text Editor, FORTRAN IV compiler, Macro Assembler, Library File Editor, and Relocatable Loader. The software developed under DOS will run under DOS or RTOS (Real Time Operating System). Both DOS and RTOS are subsets of RDOS. DOS is most logically used for development only. For run-time control, RTOS should be used because of its small memory space requirements. DOS requires 16K words of RAM, versus only 4K words for RTOS.

Data General sees three prime areas of application for the microNova: medical and instrumentation, data communications, and process control. The implementation of serial I/O (with its potential for cabling up to 100 feet and high noise immunity), the IOC chip, and the significant quantity of tested software are indicative of DG's intention to make this portent of future applications a reality. □

9 or 18 slots. The 9-slot chassis is 5.25 inches high, 19 inches wide, and 14.5 or 23 inches deep; the greater depth is with battery backup. The 18-slot chassis has the same height and width; its depth, with or without the battery pack, is 27.5 inches. A microNova development system complete with dual diskette subsystem will fit into a 72-inch cabinet.

Power requirements for all chassis types are 100, 120, 220, or 240 VAC ±10 percent, 47 to 63 Hz. Operating temperatures are 32 to 132 degrees F. A relative humidity of up to 90 percent, noncondensing, can be tolerated. The processor outputs 1023 BTU/hour maximum. Air conditioning requirements are those of a normal office environment.

The 9-slot chassis weighs approximately 37 pounds without battery backup. The 18-slot chassis weighs approximately 52 pounds without battery backup. Add 5 pounds to the chassis weight for battery backup for either chassis.

INPUT/OUTPUT CONTROL

INPUT/OUTPUT CHANNELS: An I/O bus and a Direct Memory Access (DMA) channel are standard.

The I/O bus is serial in structure and can be up to 100 feet long. Bipolar transceivers differentially drive the microNova serial I/O signal on a parallel two-line basis. This technique offers high noise immunity and ease of cabling.

The basic I/O bus is etched in the backplane. It functions to provide communication between mainframe-based I/O boards and the CPU board. The basic I/O bus is offered with a standard extension of 15 feet to connect the dual diskette subsystem. Longer extensions as discussed above are optional. Mainframe-based I/O boards are connected to free-standing peripherals by a 50-line device cable. Speed of the I/O bus is 16.6 megahertz, which translates to a data transfer rate of up to 1 million words per second.

The Input/Output Controller (IOC), a 40-pin chip located at each device interface, decodes the serial I/O signal and routes it into a parallel 16-line bidirectional data bus for I/O operations. This is the logical equivalent of the 47-line Nova I/O system. The IOC has the ability to address up to 61 I/O devices. The program I/O facility has six commands for each device. Also incorporated are controller start, clear, and I/O pulses and the facility for programmed I/O, program interrupt, and DMA functions.

For the DMA channel, rates are quoted as 148,000 words per second for input and 173,000 words per second for output. The DMA channel can be used to increment the contents of storage locations by 1.

CONFIGURATION RULES

The microNova can have up to 61 peripheral devices attached to the I/O bus. The processor chassis is available with either 9 or 18 slots. Expansion chassis are available in the 9-slot size only. The actual number of peripherals that can be attached depends upon the available number of slots and the method of attachment.

Generally speaking, all peripherals require one slot for direct attachment. The processor is mounted on one board along with either 2K or 4K words of memory, and requires one slot. The PROM programmer requires one slot, the Asynchronous Interface Board requires one slot, each General-Purpose I/O Board requires one slot, the Terminal Interface Board requires one slot, and the Programmer's Console Board requires one slot. A maximum of two diskette controllers (up to eight drives) can be attached.

MASS STORAGE

6038 FLOPPY DISC SUBSYSTEM: Consists of a four-drive controller and either a 6038 single drive or a 6039 dual drive. Each floppy disc stores up to 315K bytes on 77 tracks. Maximum storage capacity is 1.26 million bytes on a four-drive subsystem. Average head positioning time is 260 milliseconds, and average rotational delay is 83 milliseconds. Data transfer rate is 31K bytes/second. The 6038 drives feature IBM 3740 compatibility and are supported by Data General's RDOS operating system. The controller occupies one slot. The 6038 drives are manufactured by Data General.

INPUT/OUTPUT UNITS

See Peripherals/Terminals table.

COMMUNICATIONS CONTROL

ASYNCHRONOUS INTERFACE BOARD: Provides single-line connection of teleprinters and 6012 Video Displays to the I/O bus. Device codes are jumper-selectable. Transmission speeds are 110 to 9600 bps. Interface levels for RS-232C and 20-ma dc current loop are provided. Also provided are variable character lengths of 5, 6, 7 or 8 bits; either 1, 1.5, or 2 stop bits; and even, odd, or no parity. A firmware-based (256 words) Console Debug Option allows any ASCII console to supervise program execution, and also allows for modification of RAM locations and CPU registers. Included with this option is a multi-device loader routine.

GENERAL-PURPOSE INTERFACE BOARD: Provides a generalized programmed I/O, program interrupt, and DMA interface. An area on the board is pre-drilled and allocated for user-designed and built circuitry. Up to 35 IC's can be accommodated.

SOFTWARE

For all software specifications except DOS, see Report M11-304-101. Limitations on software use are predicated

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only on the memory size limitations of the microNova. DOS is discussed below.

DISC OPERATING SYSTEM (DOS): A subset of RDOS, DOS is designed for use in development systems only. DOS requires a minimum of 16K words and includes a Command Line Interpreter, Text Editor, FORTRAN IV compiler, Macro Assembler, Library File Editor, and Relocatable Loader. Since DOS is a compatible subset of RDOS, any program developed under DOS can be run under RDOS or RTOS.

PRICING

POLICY: Data General provides the microNova family on a purchase-only basis. Maintenance and service arrangements are currently being developed; details were unavailable at this writing.

Prices shown are for single-unit quantities. Standard OEM three-to-five quantity discounts of 19 percent apply. Discounts of about 40 percent are available for quantities of 200 or more units of Models 8560, 8561, 8562, 8563, 9040, 9041, and 9042.

Data General software is licensed so as to be included without charge on a system with sufficient Data General hardware to operate it. The software is also available for purchase for use on configurations utilizing other than Data General equipment (e.g., peripherals, add-on memory, etc.).

Data General provides training courses for customers at its Southboro, Massachusetts headquarters, at its Western Training Center in El Segundo, California (at a future date), and at its United Kingdom Training Center in Greenford, Middlesex, England. A special five-day course, "Designing with microNova," covering hardware components design and maintenance, memory systems, instruction set, interfacing, configuration, and program development will be offered beginning in June 1976. In addition to the centers listed above, this course can be taught at customer locations by special arrangement. Two training credits are given for each development system purchased by an end user, which entitle the customer to approximately one man-week of training. Schedules for training courses can be obtained at any Data General field office.

Software and Hardware Subscription Services are available. They provide automatic updates, additions, and documentation for a fixed yearly fee.

The Data General Users' Group provides a forum for interchange of programs. The programs are available for a fee to cover reproduction and distribution costs.

TYPICAL MICRONOVA DEVELOPMENT SYSTEM: Includes an 18-slot chassis containing CPU/4K-word RAM board with automatic program load, real-time clock and power fail/auto restart; 8K-word RAM board; 4K-word RAM board; terminal interface board; programmer's console board; and power supply with battery backup. Also included are a dual-diskette subsystem with integral data channel controller, hand-held programmer's console, and ASR-33 teletypewriter. All components except the ASR-33 are packaged in a 72-inch cabinet. Purchase price is $12,265. ■

EQUIPMENT PRICES

		Purchase Price
PROCESSORS		
8562	microNova on a board with 2K words of RAM	$ 800
8563	microNova on a board with 4K words of RAM	950
8560	microNova Minicomputer in 18-slot chassis with 4K words of RAM	2,595
8561	microNova Minicomputer in 9-slot chassis with 4K words of RAM	1,995
PACKAGED SYSTEMS		
9040 & 9040A	microNova Development System with ASR-33 Teletypewriter	12,265
9041 & 9041A	microNova Development System with KSR-35 Teletypewriter	13,965
9042 & 9042A	microNova Development System with Teletypewriter Modification Kit	10,715
PROCESSOR OPTIONS		
8565	Automatic Program Load	150
8575	Edge-Mounted Controls Indicator	200
8564	Hand-Held Programmer's Console	700
8566	Battery Backup	300
MEMORY		
8572	Board with 4K words of RAM	600
8573	Board with 8K words of RAM	950
8567	Board with 0.5K words of PROM	300
8568	Board with 1K words of PROM	375
8569	Board with 2K words of PROM	500
8570	Board with 4K words of PROM	750
8574	PROM Programmer	1,650
MASS STORAGE		
6038	Single Diskette Drive Subsystem with controller	2,900
6039	Dual Diskette Drive Subsystem with controller	3,900
1098A	Carton of Diskettes	120

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EQUIPMENT PRICES

		Purchase Price
TERMINALS		
6012H	Video Display	2,700
4010A	33-ASR Teletypewriter	1,750
4010C	35-ASR Teletypewriter	3,450
HARDWARE		
4207	Asynchronous Interface Board	250
4208	Console Debug option	200
4210	General-Purpose Interface Board	250
4211	GPIO Wirewrap Pins/Sockets	200
1114	Predrilled Circuit Card	200
2303A	Extender Card	200
1115A	Card Puller Tool	50
8571	I/O Expansion Chassis	1,600
4212	Card Frame Assembly	250
4213	Power Supply	750
4214	Power Supply/Battery Backup	1,050

CHIP PRICES (OEM only)

				PRICE RANGE	
		Quantity	Purchase Price	Quantity	Purchase Price
CHIPS					
mN601	CPU	1	$225	500	$95
mN603	IOC	1	100	500	60
mN606	4K words RAM	16	24	8,000	10
mN629	CPU 10X	1	60	500	25
mN636	IUC 10X	1	14	500	8
mN634	OCT MBX	2	20	1,000	8
mN633	OCT MAD	2	20	1,000	8
mN506	QUAD SA BD	4	24	2,000	10
1116A	Twelve 1K PROM chips	1	100	—	—
1117A	Twelve 2K PROM chips	1	250	—	—
CHIP SETS					
8563A	CPU with 4K words of RAM	1	950		
4210	General-Purpose Interface Chip Set	1	250		