Amdahl 470 Systems

MANAGEMENT SUMMARY

Amdahl Corporation was the first company to develop and produce an IBM plug-compatible mainframe computer. The company, formed in 1971 by Dr. Gene Amdahl, delivered its first processor, the 470V/6, in June 1975.

The original Amdahl 470 was intended to be a real-memory system targeted at IBM's System/370 Model 165. The target moved, however, with IBM's announcement of the virtual-memory 370/168 in August 1972, and Amdahl modified its system design to incorporate virtual-memory hardware, enabling the new system to compete with IBM's latest technology. The system that resulted from this shift in direction, the 470V/6, featured about twice the performance level of the IBM 370/168 at a similar price, while occupying only one-third of the space required by the IBM counterpart. Further, it operates in an ordinary air-conditioned environment with no requirements for the liquid cooling facilities that are necessary for very large IBM systems. The two systems have one requirement in common: a motor-generator set for the 400-Hertz system power is needed for both the Amdahl 470V/6 and the IBM 370/168.

The first Amdahl 470V/6 system was installed in the National Aeronautics and Space Administration's Institute for Space Studies, replacing an IBM 370/165. A second system replaced an IBM 370/168 at the University of Michigan in August 1975. A third system was installed at Texas A and M University in October 1975, while the fourth (and Amdahl's first commercial account) was installed at Computer Usage Corporation in November 1975.

Other later 470V/6 users include Massachusetts Mutual Life Insurance Co., Liberty National Life Insurance Co., Scientific Time Sharing Corp., and Canadian Pacific Ltd. By August 1977, the company reported 55 systems installed. Additional facilities have been established that

The large-scale Amdahl 470V/6 computer has been enhanced and expanded into a family of three IBM plug-compatible processors. The new 470V/5 and 470V/7 systems are performance-compatible with IBM's 370/168 and 3033 processors, respectively. The enhanced 470V/6, now designated the 470V/6-II, provides a performance increase of between 5 and 15 percent over the early version. All models can execute any System/360 or System/370 software and utilize any peripheral device that is compatible with the IBM system.

CHARACTERISTICS

MANUFACTURER: Amdahl Corporation, 1250 East Arques Avenue, Sunnyvale, California 94086. Telephone (408) 735-4011.

MODEL: Amdahl 470V/5, 470V/6-II, 470V/7.

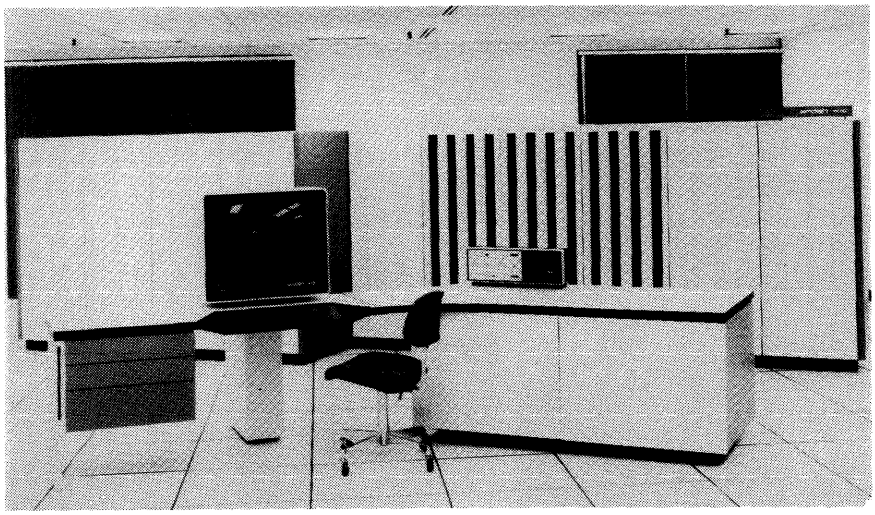
DATA FORMATS

All data formats, instruction formats, and other architectural features completely follow IBM System/370 architecture.

BASIC UNIT: 8-bit bytes. Each byte can represent 1 alphanumeric character, 2 BCD digits, or 8 binary bits. Two consecutive bytes form a "halfword" of 16 bits, while 4 consecutive bytes form a 32-bit "word."

FIXED-POINT OPERANDS: Can range from 1 to 16 bytes (1 to 31 digits plus sign) in decimal mode; 1 halfword (16 bits) or 1 word (32 bits) in binary mode.

FLOATING-POINT OPERANDS: 1 word, consisting of 24-bit fraction and 7-bit hexadecimal exponent, in "short" format; 2 words, consisting of 56-bit fraction and 7-bit hexadecimal exponent, in "long" format; for 4 words in "extended precision" format.



The Amdahl 470V/6-II is the successor to the 470V/6, the industry's first IBM plug-compatible processor. It provides performance levels that are 5 to 15 percent higher than its predecessor system, which, in turn, provided about 50 percent more throughput than an IBM 370/168. The new version was introduced as a countermove to IBM's enhanced 370/168-3 and maintains the same perforamance ratio between the rival systems. The 470/6-II system console incorporates a Data General Nova 1200 minicomputer that acts as both a console processor and a diagnostic processor. The minimum 470V/6-II system contains 4 megabytes of main memory and 16 channels and is priced at $3,280,000.

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increased the production rate from four to six systems per month.

The Amdahl 470 configuration consists of a central processor unit with 8, 12, or 6 integrated input/output channels, a minicomputer-based system console with CRT display, from 2 to 16 million bytes of main memory, and a power distribution unit. Central processor functions are performed by four independent functional units: a Storage Unit that controls accesses to main memory and includes both virtual address translation hardware and a cache memory; an Instruction Unit for controlling instruction interpretation and execution; an Execution Unit that performs the arithmetic, logic, and data manipulation functions of instruction execution; and a Channel Unit that interprets and executes input/output instructions and interfaces with the standard control unit interface that can communicate with any System/360- or System/370-compatible peripheral equipment. Operation of all the functional units can be overlapped, and four-way interleaving can be performed on accesses to main memory.

In February 1977, Amdahl announced an enhanced version of the 470V/6, designated the 470/6-II, that provides about 5 to 15 percent greater performance levels than the early model, but at an increase of $100,000 in purchase price. The differences between the two systems are academic in view of the fact that Amdahl will soon withdraw the 470V/6 from active marketing and offer only the 470V/6-II.

In March 1977, Amdahl announced the 470V/5 and 470V/7 systems. The 470V/5 is a scaled-down version of the 470V/6-II that provides only 60 to 70 percent of the performance of the larger system. It is designed to offer users of IBM's 370/155 and 370/158 systems the same type of growth opportunities that the 470V/6 provided to 370/168 users. This marketplace is also being exploited by Itel Corporation with its Advanced Systems processors that are built by National Semiconductor (see Report 70C-546-01).

The 470V/5 has less memory capacity than the 470V/6-II (2 to 6 megabytes compared to 4 to 8 megabytes), fewer I/O channels (8 compared to 16), and a smaller high-speed buffer (16K bytes compared to 32K bytes). In most other aspects, it is identical to the 470V/6-II. And, the 470V/5 is field-upgradable to a 470V/6-II for $780,000. Deliveries of the 470V/5 began in September 1977.

The 470V/7 was announced at the same time as the 470V/5 as a reaction to IBM's announcement of the high-powered Model 3033 processor. Although Amdahl stated its characteristics quite definitively, a prototype of the 470V/7 is not yet complete and production units are not scheduled for delivery until August 1978. The 470V/7 is reported to be based on a new processor that will be 50 to 70 percent faster than the 470V/6-II and about 20 to 40 percent faster than the anticipated speed of IBM's 3033 processor. It will attain its greater performance levels

INSTRUCTIONS: 2, 4, or 6 bytes in length, which usually specify 0, 1, or 2 memory addresses respectively.

INTERNAL CODE: EBCDIC (Extended Binary-Coded Decimal Interchange Code).

MAIN STORAGE

STORAGE TYPE: Metal oxide semiconductor (MOS) LSI circuitry.

CAPACITY: For the 470V/5, from 2,097,152 to 6,291,456 bytes, and for the 470V/6-II, from 4,194,304 to 8,388,608 bytes, in 1,048,576-byte increments. For the 470V/7, the following memory sizes are offered: 4,194,304, 6,291,456, 8,388,608, 12,582,912, or 16,277,216 bytes.

In 470V/5 and 470V/6-II systems, memory is housed in main storage units that can contain one or two megabytes. 470V/7 memory units contain up to eight megabytes. Each is equipped with an independent power supply. Memory access is 4-way interleaved in 2-million-byte storage units and 2-way interleaved in 1-million-byte units. All 470V/7 memory accesses are 16-way interleaved.

CYCLE TIME: For Models 470V/5 and 470V/6-II, 300 nanoseconds per 32-byte "line." An effective cycle time of 163 nanoseconds is achieved using 4-way interleaving. The 470V/7 uses the same technique, and will be significantly faster, according to Amdahl.

CHECKING: Error checking and correction (ECC) circuitry in main memory performs automatic correction of all single-bit errors and detection of all double-bit and most other multiple-bit memory errors.

A Configuration Control Register, associated with each one- or two-million-byte storage unit, maintains a map of the assignment of main storage address space for that storage unit. In the event of an unrecoverable memory error, the one-million-byte memory module can be removed from operation and the remaining memory reconfigured for continuous system operation.

In addition, a parity check is performed on all data transferred between main memory and the High-Speed Buffer. A separate parity check is also made on storage keys, which are used to implement storage protection and to record references and modifications to main storage.

STORAGE PROTECTION: Storage protection facilities are comparable to those implemented in the IBM System/370.

STORAGE CONTROL UNIT (S-UNIT): The Storage Control Unit, or S-Unit, handles all requests for data from main storage made by the CPU and the channels. An internal priority structure is used to resolve conflicts resulting from multiple concurrent requests for access to main memory. The internal priority structure of the S-Unit has the following five priority levels, in descending order: Internal High (including ECC handling), Channel Unit High, Central Processing Unit, Channel Unit Low, and Internal Unit Low (such as instruction prefetch). Normally, the central processor unit is given higher priority than a channel except when a channel issues a high-priority request. The Storage Control Unit locates the requested data either in the High-Speed Buffer or in main memory and includes a dynamic address translation facility for translating program-specified virtual addresses into real-memory addresses.

All Amdahl 470V processors include a High-Speed Buffer (HSB) that is organized as a set associative memory composed of primary and alternate halves. Each half is organized into 32-byte lines that can be addressed on a single-word or

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CHARACTERISTICS OF THE AMDAHL 470 SYSTEMS

	470V/5	470V/6-II	470V/7
SYSTEM CHARACTERISTICS			
Primary IBM target	370/158	370/168-3	3033
Date of introduction	March 1977	February 1977	March 1977
Number of processors	1	1	1
Multiprocessor configurations	No	No	No
Principal operating systems	OS/VS1; OS/VS2 (SVS and MVS); VM/370	OS/VS2 (SVS and MVS); VM/370	OS/VS2 (SVS and MVS); VM/370
Upgradable to:	470V/6-II	None	None
MAIN STORAGE			
Type	MOS	MOS	MOS
Cycle time, nanoseconds	300 per 32 bytes; 163 with 4-way interleaving	300 per 32 bytes; 163 with 4-way interleaving	NA
Minimum capacity, bytes	2,097,152	4,194,304	4,194,304
Maximum capacity, bytes	6,291,456	8,388,608	16,727,216
Bytes fetched per cycle	4	4	4
Interleaving	4-way	4-way	16-way
PROCESSOR			
Relative performance level	0.6 to 0.7	1.0	1.5 to 1.7
Cycle time, nanoseconds	32.5	32.5	28.5
Translation lookaside buffer	256 entries	256 entries	512 entries
Segment table origin stack	32 entries	32 entries	128 entries
Features:			
Clock Comparator and CPU Timer	Standard	Standard	Standard
Direct Control	Standard	Standard	Standard
Dynamic Address Translation	Standard	Standard	Standard
Floating-Point	Standard	Standard	Standard
Extended-Precision Floating-Point	Standard	Standard	Standard
High-Speed Multiply	Standard	Standard	Standard
Instruction lookahead	4 levels	4 levels	4 levels
High-speed buffer:			
Cycle time, nanoseconds	65	65	57
Capacity, bytes	16,384	32,768	32,768
I/O CHANNELS			
Byte mutliplexer	8 (max. all types)	16 (max. all types)	16 (max. all types)
Block multiplexer	8 (max. all types)	16 (max. all types)	16 (max. all types)
Selector	8 (max. all types)	16 (max. all types)	16 (max. all types)
Aggregate data rate, bytes per second	12,000,000	15,000,000	18,000,000

through a shorter CPU cycle time, improved algorithms for selected instructions, a larger translation lookaside buffer and segment table origin stack, and an increase in memory interleaving from 4-way to 16-way, as well as by improving the performance of certain other processor functions.

The 470V/7 processor will be offered in five memory configurations of 4, 6, 8, 12, and 16 megabytes. Unlike the 470V/5 and 470V/6-II, its complement of I/O channels will be expandable, from 12 in the basic system to 16 by the addition of a 4-channel group. The decision to offer this flexibility in the I/O configuration is considered a reaction to IBM's packaging of its Model 3033 processor.

Amdahl Corporation was founded by computer wizard Gene M. Amdahl, principal designer of the IBM System/360 and subsequently a director of IBM's advanced systems laboratory and an IBM Fellow, the company's highest scientific position. Its original investors included Heizer Corporation, Fujitsu Ltd., and Nixdorf Computer AG. Nixdorf Computer, however, recently divested itself of its shares in Amdahl Corporation.

double-word basis. The HSB is "pipelined," requiring two clock cycles for a full cycle. It can accept data on every clock cycle.

The HSB employed in Models 470V/5 and 470V/6 has a cycle time of 65 nanoseconds (two 32.5-nanosecond clock times), while that of the 470V/7 HSB is 57 nanoseconds (two 28.5-nanosecond clock times). The capacity of the 470V/5 HSB is 16,384 bytes, organized into two 256-line groups of 32-byte lines. The 470V/6-II and 470V/7 HSB's each contain 32,768 bytes, with the 470V/6-II HSB organized into two 512-line groups. The organization of the 470V/7 HSB has not been determined at the time of this writing.

Data is transferred between the buffer and the central processing unit in groups of 4 bytes per cycle and is brought into the buffer from main memory in lines of 32 bytes, each requiring 4 buffer cycles. In contrast to the System/370, Amdahl I/O channels as well as the CPU access the High-Speed Buffer. A tag field associated with each 32-byte line in the buffer includes a block identifier containing the high-order real address bits of the buffer data, plus parity and check fields, modification indicators, and reference bits to specify whether a central processor or channel access brought the data into the buffer and whether the CPU was in the supervisor or problem state of operation. The 470V/6 allows the user to control the location of data in the High-Speed

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Fujitsu, in addition to being the largest investor in Amdahl, holding nearly 29 percent of the corporation's common stock, has manufactured a substantial portion of the subassemblies used in the 470 systems. However, Amdahl has increased its manufacturing facilities and now makes most subassemblies in-house. Fujitsu also manufactures and markets, in Japan, an M-180-II computer system that is capable of about two-thirds the performance of the 470V/5. Under the present agreements with Amdahl, Fujitsu could begin marketing the M-180-II system in the U.S. and become a fourth competitor in the IBM plug-compatible mainframe race.

The Amdahl 470 design is based on the System/370 architecture. It achieves its superior performance through the use of the latest in super-fast integrated circuit technology and, to a lesser extent, from central processor architectural optimization that provides for more efficient operation of the high-speed buffer memory and the virtual-storage address translation hardware, and permits extensive overlapping of input/output operations and instruction execution in the central processor.

Large-scale integrated (LSI) semiconductor circuits are used extensively throughout the system, resulting in increased processing speeds, higher reliability, and reduced space and cooling requirements. The central processor uses an LSI version of bipolar emitter-coupled logic (ECL) with chip speeds in the area of 600 picoseconds (trillionths of a second), and has a CPU cycle time of approximately 32 nanoseconds. The new 470V/7 reportedly will cut this time to 28.5 nanoseconds.

Main memory in the 470V/5 and 470V/6 uses metal oxide semiconductor (MOS) LSI circuits and has a cycle time of 300 nanoseconds, while ultra-high-speed bipolar components are used in the cache-like buffer memory. Buffer loading from main memory is performed in 32-byte blocks. Using the maximum (four-way) main storage interleaving capabilities, a maximum data transfer rate of one 32-byte "line" per 163 nanoseconds can be achieved between the high-speed buffer and main memory.

At the time when development began on the Amdahl system, economically practical LSI technologies were not available to produce circuit chips with the density and speed required to implement the Amdahl concepts. As a result, all of the circuitry, plus the manufacturing techniques, test equipment, and chip interconnection methods, have been specially designed by Amdahl engineers.

The LSI chips developed for the Amdahl 470V's measure 154 thousandths of an inch square, are 10 mils thick, and have a maximum capacity of about 100 circuits. The LSI chips are mounted on a multi-chip carrier, which is the field-replaceable unit of the system. Each carrier has a maximum capacity of about 4200 circuits. Thus, all 150,000 circuits comprising the 470V/6-II system can be housed on 51 multi-chip carriers, resulting in a system requiring an estimated one-third of the floor space occupied by an IBM System/360 Model 168 with its associated channels. Similar space reductions are possible with the 470V/5.

Buffer according to the CPU state and whether it originates from a central processor channel access.

When a request is made for data by the central processor Instruction Unit or by the Channel Unit, the Storage Control Unit forms a printer into the buffer and reads four 32-byte lines of data from the primary and alternate halves of the buffer. The S-Unit then uses the real line address calculated by the address translation hardware to select one of the four lines, and a tag comparison on the real address bits is used to select the data from the primary or alternate half of the buffer. Location of the data in the buffer can be performed in two machine cycles, although overlapped buffer operations allow it to accept a request for data during each cycle. If the data is not in the buffer, a main storage request is generated and the request data is made available to the program and is also placed in the High-Speed Buffer.

Operation of the High-Speed Buffer is based on a non-store-through technique, in which data that is modified in the buffer is not written to main storage until the line is removed from the buffer to make room for new data. As a result, frequently referenced data can be accessed and modified in the buffer without incurring a large number of main memory accesses. An instruction prefetch function can be enabled for accesses to the buffer from input/output channels, the operand stream, or the instruction stream. A combination of three bits in the Storage Unit controls the order of prefetch operations, although that order can be modified through the use of an additional register bit provided for that purpose. Six operating state register bits are used to control the operation of the buffer replacement algorithm. Four additional bits of the S-Unit operating state register can be set through the System Console, can be used to partition the buffer to configure out a portion of the buffer with a hardware failure.

DYNAMIC ADDRESS TRANSLATION: The dynamic address translation facility is located in the S-Unit and controls the translation of program-specified virtual addresses into real-memory addresses. Virtual memory implementation in the 470V's is similar to that of the IBM System/370. Virtual storage is divided logically into segments of 64K bytes or 1024K bytes, which are in turn divided into pages of either 2048 or 4096 bytes. Segment and page tables are maintained in main storage to perform address mapping. A high-speed Translation Lookaside Buffer (TLB) is used to store the most recently referenced addresses, and a Segment Table Origin (STO) stack stores information on the size and main memory location of the segment table associated with TLB entries.

The 470V/5 and 470V/6-II TLB consists of 128 virtual and real address pairs in each of the primary and alternate halves, while the 470V/7 TLB contains two halves, each with 256 address pairs.

Translation of virtual to real addresses for data located in the TLB is overlapped with the High-Speed Buffer search, and data for both real and virtual operation can be accessed in two S-Unit cycles. If the data is not located in the TLB, an address translation is performed and two additional storage references are required to locate the data either in High-Speed Buffer or in main memory. The new translated address is translated in the TLB according to an algorithm similar to that used by the High-Speed Buffer.

The STO stack contains virtual-storage identification fields (32 in the 470V/5 and 470V/6-II and 128 in the 470V/7) associated with the TLB entries. The identification fields correspond with address translation information such as segment table size and location, contained in Control Register 0 and Control Register 1. When the contents of these registers are modified, subsequent TLB entries are assigned a new STO ID by the S-Unit, but earlier TLB entries are

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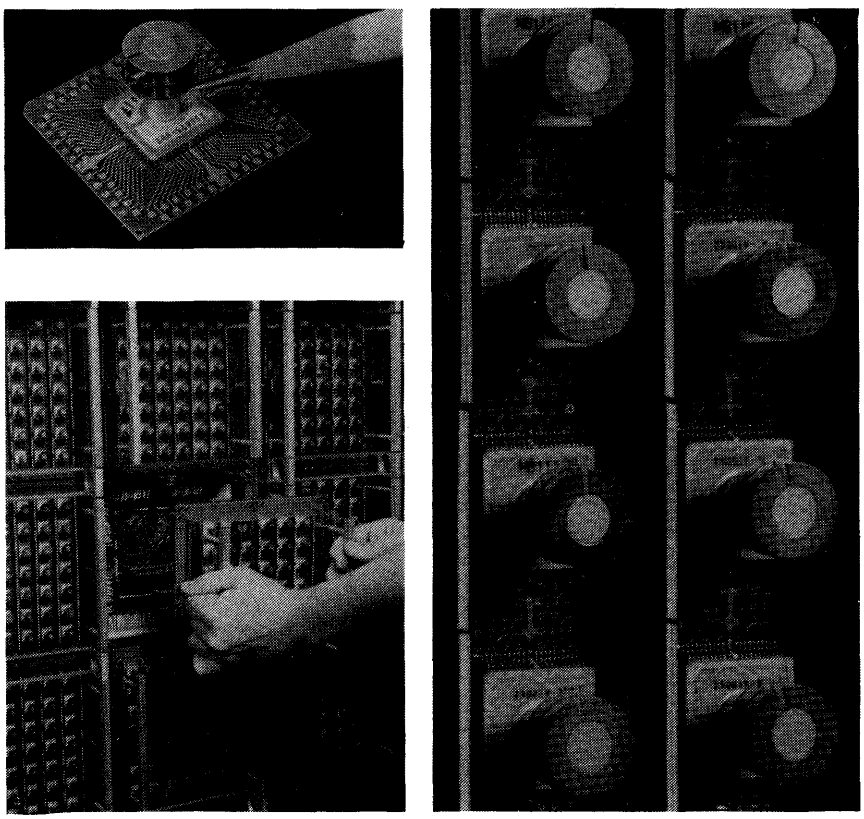

Unique to the Amdahl 470's, this "fourth-generation" LSI packaging technique was developed to reduce both physical system size and power consumption. The basic logic unit of the 470 system is a "chip" (top left) that contains 75 to 100 emitter-coupled logic (ECL) circuits and requires signficantly less power. A typical chip is shown, with its air cooling fins, mounted on a printed circuit board for testing purposes. The chips are then mounted in multiple chip carriers (right) that can contain up to 42 of the LSI circuits. The MCC's are, in turn, connected to a computer backplane (bottom left) with the chip cooling fins protruding into an air stream. The use of air cooling in the 470V systems is a distinct advantage over the liquid cooling required by their IBM counterpart, the 370/168.

The Amdahl circuits also require significantly less power than that consumed by standard ECL circuitry, resulting in significantly reduced cooling requirements for the system. The entire 470V/6 system is air-cooled, and a cooling stub is bonded to the surface of each LSI chip carrier to conduct heat into the air flow.

The miniaturization of the 470 circuitry substantially reduces the number of wiring interconnections required in the system, resulting in potentially fewer system failures. Additional circuitry on each subassembly also allows some 16,000 key logic points in the system to be examined and exercised by diagnostic programs under control of the system console. Remote diagnostic services are also available through a modem supplied with the system console. Other reliability features incorporated in the design include instruction retry, error checking and correction (ECC) circuitry in main memory, and the ability to recover from high-speed buffer and main memory failures by configuring out the malfunctioning portions of the buffer and main memory.

Although the basic concept underlying the 470 system design is to produce an extremely fast but architecturally simple computer system, sophisticated modifications have been made to several key functional components to achieve more efficient operation. The high-speed buffer, for example, uses a "non-store-through" technique, permitting data to be modified in the buffer without updating main storage. Main storage is updated only when the data is written back to main storage to provide space for new data. In addition, Amdahl has

not invalidated provided they do not exceed the capacity of the stack (32 or 128). If Control Registers 0 and 1 are restored to a previous value, any previous TLB entries remaining are thus still available. The S-Unit controls selective purging (when an STO entry is automatically removed from the stack and its associated TLB entries invalidated) of the TLB and STO stack during spare cycles.

CENTRAL PROCESSOR

Central processor functions such as instruction fetching and decoding and instruction execution are performed by two separate units, the Instruction Unit (I-Unit) and the Execution Unit (E-Unit).

The I-Unit controls instruction execution through a pipeline structure and can have up to six instructions concurrently in some phase of execution. The instruction execution process is divided into the fetch phase plus six additional decoding and execution phases. The instruction fetching operation requires three cycles, while Phases A, B, and C, which perform instruction decoding, operand address generation, and operand retrieval, each require a minimum of two central processor cycles. Phases D, E, and F each require a minimum of one cycle, and perform execution plus checking and writing of the results of the instruction execution. The overlapped instruction execution in the pipeline can result in the completion of an instruction execution every two machine cycles, except in the case of long instructions requiring additional cycles for execution.

Extensive parity checking is performed throughout the I-Unit. All incoming instructions are checked for parity, and the results are checked again after completion of execution. All control registers and the program status word are checked each time they are used. In addition, parity is checked for the timer and the address generation function, and parity is also maintained for all program-referable data.

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engineered a number of probe points into the hardware to facilitate the use of hardware monitors.

Instruction execution is performed in a "pipeline" structure which allows the execution of up to six instructions to occur concurrently. In addition, although the Amdahl Dynamic Address Translation (DAT) feature provides virtual-storage operations comparable to those of the System/370, Amdahl has extended its design for more efficient operation. The Amdahl DAT feature maintains a segment table origin (STO) stack that allows up to 31 (127 in the 470V/7) different virtual-storage environments to maintain translation information in the Translation Lookaside Buffer, reducing the amount of updating activity in the buffer. When the capacity of the STO stack is exceeded, the oldest entry in the stack and its associated translation lookaside buffer entries are purged during spare machine cycles. In the 470V/5 and 470V/6, the translation lookaside buffer portion of the address translation hardware has also been expanded to 256 entries, compared to the System/370's 128. In the 470V/7, the number of entries will be 512.

Each I/O channel can be configured as a byte multiplexer, a block multiplexer, or a selector channel. Byte multiplexer channels have a maximum data transfer rate of 110,000 bytes per second. Block multiplexers can transfer data at 2 million bytes per second, or at 4 million bytes per second using the optional two-byte interface. Selector channels are capable of transferring data at 2 million bytes per second.

The aggregate data rate, however, is the limiting factor in each system, and this, in turn, is governed by the channel-to-processor interface circuitry of each four-channel group. The exact aggregate data rate is heavily dependent on the system configuration, but a rule-of-thumb value is available. For the 470V/5, the aggregate data rate is about 12 million bytes per second, for the 470V/6-II, it is 15 million bytes per second, and for the 470V/7, the expected rate is 18 million bytes per second.

A dynamic priority allocation scheme based on the availability of space in each channel buffer is used to allocate cycles between central processor operations and input/output data transfers. Normally, the central processor has the highest priority in the system, but channels performing high-speed data transfers are allowed to take precedence over the central processor by the Amdahl internal priority scheme. This allows high-speed devices to be attached to any channel without performance degradation and provides additional flexibility in the configuration of peripheral subsystems.

COMPETITIVE POSITION

Competitively, the waters were tranquil until IBM announced its Model 3033 processor. The original Amdahl 470V/6 was priced very close to IBM's 370/168 and offered about twice the performance. Itel (Report 70C-456-01) was also in the plug-compatible processor mar-

The Execution Unit (E-Unit) executes arithmetic and logical instructions received from the I-Unit; it consists of a logical unit and checker (LUCK), a group of functional units (multiplier, adder, shifter, and byte mover), a table lookup unit to generate an inverse in the I-register (for divide operations), registers for storage of intermediate results, and a result register for output of the result of instruction execution to the I-Unit. Instruction operation codes plus control information are sent from the I-Unit to the E-Unit, and instruction operands are received either from the I-Unit or directly from main storage. The LUCK checks the validity of incoming operands, performs logical operations and comparisons on incoming operands, validates decimal digit formats, sets conditions codes, and counts leading zeroes for use in shifting and normalization. LUCK operations require one CPU cycle. Additional arithmetic functions are performed by the multiplier, adder, shifter, and byte mover units, each of which also completes its functions in one machine cycle.

When instructions require processing by multiple E-Unit functions, the I-Unit synchronizes the operation of its pipeline by delaying the progress of other instructions in the pipeline until the final cycle of the instruction that is currently in the E-Unit. The E-Unit performs parity checks on all incoming data and on logical and shift operations, and uses a check summation technique to verify the results of addition and multiply functions. The E-Unit also generates parity for final instruction execution results, and the parity is checked by the I-Unit before storing the final results.

Failure to complete the execution of an instruction because of a hardware malfunction results in a machine check condition. Most instructions in the Amdahl 470 repertoire can be automatically retried by the E-Unit. The instruction retry feature attempts to re-execute the failed instruction (in contrast to returning the machine state to a hardware checkpoint). Instructions that cannot be retried or recovered result in a hard machine check, which is handled according to standard System/370 procedures.

INDEX REGISTERS: Sixteen 32-bit general registers are used for indexing, base addressing, and as accumulators.

INSTRUCTION REPERTOIRE: The Amdahl 470 instruction set consists of the complete System/370 Universal Instruction Set, including the five System/370 instructions for Dynamic Address Translation. Two exceptions are the Store CPU ID (STIDI) and Store Channel ID (STIDC) instructions, which differ in their operations because of architectural differences between the System/370 and the Amdahl processors. In the Amdahl units, a machine check extended logout (MCEL) is performed by the Console Processor in its own memory, whereas in the System/370 the address in main memory and size of the machine check extended logout are dependent on the central processor model and control register information. Since the MCEL on the 470 is made to the Console Processor, the MCEL length field stored by the STIDP instruction is all zeroes. The model number is 0470. The STIDC instruction stores zeroes for a channel model number because all Amdahl channel types are implicit in CPU type. According to Amdahl, no system or application program is likely to be affected by these model dependencies.

INSTRUCTION TIMING: The following instruction execution times, in *nanoseconds,* have been estimated by scaling performance information supplied by Amdahl for the Model 470V/6 in the absence of specific timing data for the newer models.

	470V/5	470V/6-II	470V/7
Add (32-bit binary):	110	65	40
Multiply (32-bit binary):	380	228	140
Divide (32-bit binary):	2700	1625	1015

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ket, but the Itel systems were aimed at IBM's 370/158 systems and not really competing with Amdahl's. Further, Itel's philosophy is based on matching IBM's performance at a lower price rather than providing more performance at a similar price.

The March 1977 introduction of the IBM 3033 processor stirred up these tranquil waters. The 3033 features performance levels about 65 to 90 percent above those of the 370/168, and is priced at about $3,380,000 for a 4-megabyte configuration. This new IBM product resulted in Amdahl's quickly reducing the price of a 4-megabyte 470V/6-II from $4,635,000 to the current price of $3,280,000. Amdahl also announced plans for the 470V/7, an enhanced processor with 1.5 to 1.7 times the performance of its 470V/6 and about 3.0 to 3.4 times faster than the 370/168, the original Amdahl market target. The 470V/7 is designed to restore the price/performance ratios that originally existed between the Amdahl and IBM systems.

One aspect of the IBM 3033 that may cause trouble for Amdahl is IBM's increased use of system-level microcoding in the 3033. This technique goes beyond the implementation of the basic instructions in microcode and adds frequently-used operating system functions to the 3033's firmware complement. By implementing portions of the operating system in firmware, IBM has made it impossible for the new MVS/SE enhancement program product for its MVS operating system to be executed in current Amdahl systems. Amdahl must design modifications to its present systems in order to take advantage of IBM's future operating systems and enhancements. This aspect of the new IBM products casts a definite shadow on the Amdahl systems, but Amdahl has demonstrated a high degree of resourcefulness in the past and will almost certainly overcome this challenge.

The 470V/5, Amdahl's low-end system that was announced concurrently with the 470V/7, features performance levels similar to those of the IBM's 370/168 processor that was obsoleted by the more cost-effective Model 3033. Thus, the 470V/5 competes directly with no current IBM models nor those of any other plug-compatible vendors. But if industry speculations about forthcoming lower-performance versions of the IBM Model 3033 are substantially correct, these models will compete with the 470V/5.

Recently, Control Data Corporation joined the plug-compatible processor scramble by announcing the Omega 480 line. The Omega 480-I and 480-II processors are manufactured by IPL Systems Inc. and are targeted at IBM's smaller 370/135 through 148 systems.

USER REACTION

Datapro contacted six Amdahl 470V/6 users to record their impressions of the IBM plug-compatible system. The survey population included two large university computing centers, two insurance companies, a service bureau, and a railroad. Generally, the processors were

	470V/5	470V/6-II	470V/7
Load (32-bit binary):	110	65	40
Store (32-bit binary):	110	65	40
Add (5-digit packed decimal):	705	423	265
Compare (5-digit packed decimal):	815	488	305
Add (short floating-point):	325	195	120
Multiply (short floating-point):	435	260	165
Divide (short floating-point):	1465	878	550
Add (long floating-point):	435	260	165
Multiply (long floating-point):	1085	650	405
Divide (long floating-point):	3465	2080	1300

OPERATIONAL MODES: Like the System/370, the Amdahl CPU's can operate in either the Basic Control (BC) or Extended Control (EC) mode. The BC mode maintains general upward compatibility with the System/360 architecture and programming. In the EC mode, the Program Status Word (PSW) and the layout of the permanently assigned lower main storage area are altered to support Dynamic Address Translation and other new system control functions; therefore, the virtual-storage-oriented operating systems must be used.

PROCESSOR FEATURES: The standard timing features of the System/370 architecture are included in all Amdahl central processors. These include a CPU timer and a Clock Comparator; the latter provides a means for causing an interrupt when the standard Time-of-Day Clock reaches a program-specified value. Additional instructions are provided to set and store the Time-of-Day Clock, Clock Comparator, and CPU Timer.

The optional Direct Control Feature, as on the System/370, provides six external interrupt lines which operate independently of the normal data channels, plus the Read Direct and Write Direct instructions which provide for single-byte data tranfers between an external device and main storage.

The optional Channel-to-Channel Adapter permits direct communication between an Amdahl processor and a System/370 via a standard I/O channel. It can be attached to either a selector channel or a block multiplexer channel and uses one control unit position on either channel. In an interconnection between an Amdahl 470 and a System/360 or System/370, either system can be equipped with the Channel-to-Channel Adapter, and it is required on only one of the interconnected channels.

The Two-Byte Interface, available as an option for all selector and multiplexer channels, doubles the bandwidth of the data path between the channel and the control units which support this option.

CONSOLE INPUT/OUTPUT

The system console includes a Data General Nova 1200 minicomputer that acts as a console processor, an operator control panel, and a CRT display and keyboard. The console processor is also equipped with a magnetic disk cartridge that is used by the console operating system and for logout and other functions, a floppy disk unit for loading diagnostic programs, and a modem to provide for remote diagnostic services.

The console has a direct interface to the central processing unit to allow access to the status of approximately 16,000 system key logic points and setting of control and data registers. The computer-to-console interface allows diagnostic tests to be performed on the central processor modules under control of the Console Processor without regard to the operating condition of the central processor, the I/O

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being used as the host systems for large, widely distributed networks of interactive terminals. In this survey group, the smallest number of terminals was 110 and the largest was between 450 and 500—the exact number was not known. The smaller networks were employed by the universities, and the larger ones were owned by the insurance companies.

The nature of the applications performed on each system held no surprises. The insurance companies were using the 470V/6 for customer and policy records; the universities were employing the systems for scientific/engineering computation and administrative applications; and the service bureau was using the 470V/6 to provide specialized accounting services to automotive-related businesses. The railroad was using its 470V/6 to record car loadings, equipment moving, and general railway operations.

The peripheral complements in use with each system included roughly even mixes of IBM and non-IBM disk drives and magnetic tape units, but the unit record equipment (line printers, card equipment, etc.) was almost entirely IBM's.

The systems surveyed had been installed for between 2 and 22 months, averaging slightly over 14 months for the 6 systems. The average memory size was slightly above 4 megabytes, which was also the most frequently encountered configuration.

The question we deemed most significant in this survey was not one of the standard Datapro questions listed below, but instead involved the degree of *compatibility* between the 470V/6 and its IBM counterpart, the 370/168. The answer to this and subsequent questions was the same in every interview: *no difference!* The IBM operating software ran in the Amdahl 470's exactly as it ran in the IBM system. In fact, one user reported 12 long-standing OS/MVT problems that could not be resolved by IBM service personnel but had since been resolved by Amdahl.

The aspect of the Amdahl 470 that most impressed the users was not its compatibility with the IBM systems, but its exceedingly short installation times—usually only a matter of a few hours. Another aspect that has been well received is Amdahl's built-in diagnostics that locate failed components at the chip level. Most of the users felt that these facilities, coupled with the high quality of Amdahl's field support personnel, have been responsible for system availability in excess of 95 percent, even through the initial start-up period.

The ratings provided by the users are summarized in the following table. Four of the usual twelve categories—Peripheral Reliability, Operating System, Compilers and Assemblers, and Application Programs—have been omitted because they are not part of the Amdahl product. In addition, the Ease of Programming category has been re-interpreted in this survey to reflect on the compatibility of the IBM software executing in the Amdahl processor.

channels, or other components of the main system. The system console is also equipped with a channel interface to a selector or multiplexer channel for operation as a standard console device.

The system console operates in three modes: the maintenance mode, the hardware command mode, and the device support mode. In the device support mode, the console emulates either an IBM 3066 system console or an IBM 3215 console printer-keyboard (using the CRT display for output in place of the 3210 matrix printers), and can be connected to either a selector or block multiplexer channel. Functions that can be performed in the hardware command mode include IPL, reset operations, display and modification of the contents of registers and main storage locations, and setting of operating conditions for the system.

INPUT/OUTPUT CONTROL

Each 470 central processor includes standard input/output channels, each of which can be configured as a byte multiplexer, block multiplexer, or selector channel. A byte multiplexer channel can support a maximum data rate of about 110,000 bytes per second, and a selector channel can support up to 2 million bytes per second. The block multiplexer channel supports data rates of 2 million bytes per second with its standard one-byte interface or up to 4 million bytes through the addition of the optional Two-Byte Interface.

The 470V/5 is supplied with 8 channels, the 470V/6-II has 16 channels, and the basic 470V/7 has 12 channels. The 470V/7 processor can be upgraded to 16 channels through the addition of 4 optional channels.

The aggregate I/O data transfer rate for each system is less than the total of the maximum rates of all the attached channels. Each group of four channels shares certain hardware elements, causing contentions at the interface to the CPU. The resulting aggregate I/O data rates are 12 million bytes per second for the 470V/5, 15 million bytes per second for the 470V/6-II, and 18 million bytes per second for the 470V/7.

Each selector-type channel can address up to 256 input/output devices and contains a single implicit channel for addressing one device at a time at burst-mode speeds. For the 470V/5 and 470V/6-II, an additional 1024 subchannels are available for allocation to byte multiplexer and block multiplexer operations in groups of 64, 128, or 256 subchannels. Channels with either 64 or 128 assigned subchannels can be configured for shared-channel operation. In channels with 64 nanoseconds, 4 can be shared, while those with 128 subchannels can have 8 shared subchannels. For the 470V/7, subchannels are allocated in groups of 32, providing a total of 2048 subchannels.

In the 470V/5 and 470V/6-II, input/output operations are performed under control of the Channel Unit (C-Unit), which operates independently of central processor operations. The C-Unit consists of three major functional units called the Central Interface Control Logic (CICL), the Direct Access Control Logic (DACL), and the Operation Control Logic (OCL), plus buffers and communications areas and the Remote Inteface Logic which interfaces to control units for any System/360 or System/370-compatible peripheral devices.

The CICL controls the transfer and buffering of data between the Channel Buffer Store and the peripheral devices. It polls the channels every eight cycles for data transfer requests, and transfers data from the Channel Buffer Store to the Remote Interface Logic one or two bytes at a time.

The DACL controls the movement of data between the Storage Unit and the Channel Buffer Store and has a data

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	Excellent	Good	Fair	Poor	WA*
Ease of operation	6	0	0	0	4.0
Reliability of mainframe	6	0	0	0	4.0
Responsivenesss of maintenance service	6	0	0	0	4.0
Effectiveness of maintenace service	5	1	0	0	3.8
Technical support	5	1	0	0	3.8
Ease of programming	6	0	0	0	4.0
Ease of conversion	6	0	0	0	4.0
Overall satisfaction	6	0	0	0	4.0

*Weighted Average on a scale of 4.0 for Excellent.

The user ratings awarded the 470V/6 do not provide much of an opportunity for analysis. Clearly, the system performs exactly as expected, it is fully compatible with its IBM counterparts, and Amdahl has gone beyond IBM in providing reliability and maintenance aids. Further, the Amdahl users are convinced that the company has not stopped at providing good, efficient hardware, but has assembled a highly competent field support organization in sufficient numbers to insure the highest possible system availability.□

transfer rate of one word every eight cycles. The DACL is organized as a pipeline to allow overlapping of the functions. It polls each channel every 16 cycles for service requests, concurrently transfers data in both directions between the Storage Unit and the Channel Buffer Store, and reads or stores the results of each transfer operation.

The OCL translates channel commands and coordinates channel program execution for the C-Unit.

A dynamic priority scheme controls the allocation of service to I/O channels. Channels can issue high-priority and low-priority requests for service. Each channel is assigned a 32-byte buffer area in the Channel Buffer Store. Channels with less than half a buffer area remaining are assigned high priority, while those with more than half a buffer space available are assigned low priority. The S-Unit resolves conflicts for access to the High-Speed Buffer according to its own internal priority structure, permitting high-priority channel requests to take precedence over central processor requests for access to the High-Speed Buffer. An I/O operation is always executed at a higher priority than buffer prefetch operations.

The C-Unit performs parity checks on all input and output data transfers and on data transfers to the Storage Unit. Other functions include channel indirect addressing comparable to that implemented on the System/370, and extended channel logout.

According to Amdahl, the 470V/7 I/O operations will be similar to those of the 470V/5 and 470V/6-II, but there will be certain differences within the DACL and CICL units. No details were forthcoming at the time of this writing.

PERIPHERAL EQUIPMENT

The Amdahl 470 systems can utilize all IBM System/360 and System/370 input/output and mass storage devices, as well as their plug-compatible counterparts from independent vendors. Detailed coverage of many of these peripherals can be found in Volume 2 of DATAPRO 70.

SOFTWARE

Amdahl offers complete functional compatibility with IBM System/360 and System/370 software. Amdahl Corporation intends to support users of current IBM system software by providing new releases of the software, including minor modifications to account for differences in the way the 470's handle machine check conditions, and by supplying software support services for its customers.

Operating systems supported include OS/MVT, OS/VS1, OS/VS2 (SVS and MVS), and VM/370. Also included is support for such major IBM subsystems as HASP, ASP, TSO, TCAM, JES2, JES3, VTAM, RSCS, CMS, and IPCS.

Amdahl maintains a Programming Systems Support (PSS) group that supplies its own versions of the supported IBM systems releases. The PSS group also issues Amdahl versions of the IBM Program Temporary Fix (PTF) tapes.

PRICING

The Amdahl 470 systems are offered for purchase or for lease under a four-year operating lease that can be terminated after three years upon payment of a penalty. Amdahl does not offer a short-term rental program.

Prices for all current configurations of the Amdahl 470 systems are shown in the following Equipment Prices section.■

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.
PROCESSORS AND MAIN MEMORY			
470V/5	CPU Complex; includes 16K-byte buffer storage, 8 I/O channels, console including maintenance processor, power distribution unit, and main memory as indicated:		
	With 2,097,152 bytes of main memory	$2,430,000	$7,680
	With 3,145,728 bytes of main memory	2,550,000	8,200
	With 4,194,304 bytes of main memory	2,650,000	8,500
	With 5,242,880 bytes of main memory	2,770,000	9,050
	With 6,291,456 bytes of main memory	2,870,000	9,400
470V/6	CPU Complex; includes 16K-byte buffer storage, 16 I/O channels, console including maintenance processor, power distribution unit, and main memory as indicated:		
	With 4,194,304 bytes of main memory	3,180,000	8,500
	With 5,242,880 bytes of main memory	3,300,000	9,050
	With 6,291,456 bytes of main memory	3,400,000	9,400
	With 7,340,032 bytes of main memory	3,520,000	9,900
	With 8,388,608 bytes of main memory	3,620,000	10,250

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		Purchase Price	Monthly Maint.
PROCESSORS & MAIN MEMORY (Continued)			
470V/6-II	CPU Complex; includes 32K-byte buffer storage, 16 I/O channels, console including maintenance processor, power distribution unit, and main memory as indicated:		
	With 4,194,304 bytes of main memory	3,280,000	8,600
	With 5,242,880 bytes of main memory	3,400,000	9,150
	With 6,291,456 bytes of main memory	3,500,000	9,500
	With 7,340,032 bytes of main memory	3,620,000	10,000
	With 8,388,608 bytes of main memory	3,720,000	10,350
470V/7	CPU complex; includes 32K-byte buffer storage, 12 I/O channels, console including maintenance processor, power distribution unit, and main memory as indicated:		
	With 4,194,304 bytes of main memory	3,480,000	8,600
	With 6,291,456 bytes of main memory	3,700,000	9,500
	With 8,388,608 bytes of main memory	3,920,000	10,350
	With 12,582,912 bytes of main memory	4,360,000	12,100
	With 16,777,216 bytes of main memory	4,800,000	15,850
Four Additional I/O Channels for 470V/7 (16 channels maximum)		150,000	NC
PROCESSOR OPTIONS			
Two-Byte Interface for I/O channels		1,400	NC
Channel-to-Channel Interface, for multiprocessor systems		32,500	NC
Upgrade; 470V/5 to 470V/6-II		780,000	NC
Upgrade; 470V/6 to 470V/6-II		100,000	NC