UNIVERSAL ASSEMBLER VERSION 3.1 FEBRUARY 29, 1980 (IN-HOUSE)


```
COMMAND LINE WAS: SNAP3 PROC14.PROC,,,PROC144;GBQPLX

INCLUSION A: PROCINC/TXT:DR0
INCLUSION B: PROC14/LIB:DR0.PMACMIC
INCLUSION C: PROC14/LIB:DR0.GMACROZ
INCLUSION D: PROC14/LIB:DR0.PROCEQUS
INCLUSION E: PROC14/LIB:DR0.BDEF1800
INCLUSION F: PROC14/LIB:DR0.MDEF1800
INCLUSION G: PROC14/LIB:DR0.PORTEQUS
INCLUSION H: PROC14/LIB:DR0.PORTASGN
INCLUSION I: PROC14/LIB:DR0.PROCP4
D   20.A                        CAPIVS    EQU       0              INVERTED DISPLAY SCREEN VERSION **NEW**

*** ERRORS: D

PROGRAM NAME: PROC

PROGRAM ADDRESS BLOCKS:         010000    /ABSOLUTE/  SIZE=000000  (ABS)
                                167400    /SYSIVR/    SIZE=000400  (ABS)
                                170000    /SYSROM/    SIZE=000047  (ABS)
                                000000    /PROCL/     SIZE=002000  (REL)
                                000000    /PROCP/     SIZE=004000  (REL)

PRIMARY TRANSFER ADDRESS:       000000    /PROCL/

EXTERNAL DEFINITIONS:

POR       000000 /PROCL/    SCLSTW    000271 /PROCL/    MIN       000115 /PROCL/    IVIOLs    000266 /PROCL/
MOUT      000150 /PROCL/    BP        000236 /PROCL/    SC        000240 /PROCL/    SCRAMI    000242 /PROCL/
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SCROMLI	000250	/PROCL/	SCROM	000260	/PROCL/	SCROML	000257	/PROCL/	SCDON	000304	/PROCL/
UDPOP	000263	/PROCL/	UDOP	000270	/PROCL/	SCLST	000274	/PROCL/	SCRAM	000302	/PROCL/
BETA	000400	/PROCL/	ALPHA	000417	/PROCL/	SYSRET1	000512	/PROCL/	REGS	000563	/PROCL/
STL	000650	/PROCL/	RIND	001215	/PROCL/	SYSTAT	000755	/PROCL/	BT	001000	/PROCL/
RIN256	001110	/PROCL/	RINST	001116	/PROCL/	BCP	001126	/PROCL/	RIN16	001207	/PROCL/
BFSB	001222	/PROCL/	BFAC	001226	/PROCL/	BFS	001300	/PROCL/	SLC	001346	/PROCL/
SRC	001355	/PROCL/	SRE	001366	/PROCL/	CCS	001402	/PROCL/	PLR	001407	/PROCL/
PSR	001440	/PROCL/	INCPA	001463	/PROCL/	INCP	001470	/PROCL/	DECPA	001512	/PROCL/
DECP	001517	/PROCL/	DECX	001541	/PROCL/	INCX	001543	/PROCL/	DS	001647	/PROCL/
DLHL	001651	/PROCL/	DL	001655	/PROCL/	BRL	001731	/PROCL/	EI	001745	/PROCL/
DI	001756	/PROCL/									

EXTERNAL REFERENCES (UNDEFINED SYMBOLS):

RCVMRK RETS SRVRPT EXMOUT FETCHW PSHST0 PCMOD SRVDO POPST0 SYSRET0 FETCHRW FETCHI
MEMPF$ FETCH EIROJ

UNUSED LABELS:

MEMPFSC

```
1.  *
2.  . 2.14.I  HJS  82 AUG   7    DO A NEW IMA WITH OUTPUT MODEM CONTROLS
3.  . 2.14.F  HJS  80 JAN  16    START CHANGES FOR IMA VERSION
4.  *
5.  . 2.13    HJS  79 FEB  12    VERSION 13 RELEASE
6.  . 2.13.A  HJS  79 JAN  22    FIX REGS TO WORK WITH ACCESS PROTECTED STACK
7.  *
8.  . 2.12    HJS  78 OCT  16    FINAL RELEASE
9.  . 2.12.D  HJS  78 OCT  15    CHANGE SYSTAT SO CAN TELL THE PRE-RELEASE LEVEL
10. . 2.12.C  HJS  78 OCT  12    CORRECT THE PC FOR MEMORY FAULTS TO MATCH 6600 PC
11. . 2.12.A  HJS  78 SEP  05    REFORMAT, RECOMMENT & FIX STACK FOR ACCESS ENABLE
12. .   12                       THE NUMBER IS OCTAL!! TO MATCH DEBGU ? DISPLAY
13. *
14. . 2.9   HJS   78 JUL  20     FINAL RELEASE OF VERSION 9
15. . 2.9.K HJS   78 APR  23     SPLIT PROC, MAKE RELOCATABLE, CHANGE APF, ADD AML
16. . 2.9.J HJS   78 MAR  20     RESTRUCTURE INTERRUPT SEQUENCE & MINOR MODS
17. . 2.9.I HJS   78 FEB  27     CORRECT 9.H FOR FAULT CLEANUP
18. . 2.9.H HJS   78 FEB  16     EVERYBODY MEMPF'S, KEYBOARD SCAN, & SIR CHANGE
19. . 2.9.G HJS   78 FEB   3     CORRECT TIMING, COMMENTS, & ADD POR TIMEOUT
20. . 2.9.F HJS   78 JAN  11     FIXING MIN/MOUT TIMINGS
21. . 2.9.E HJS   78 JAN   4     TESTING REPEATED KEYIN CONTROLS
22. . 2.9.D HJS   77 DEC  21     CORRECT STL INSTRUCTION
23. . 2.9.C HJS   77 DEC  13     BACK OFF FROM KBD RPT & RE-DO STL FOR TIMING
24. . 2.9.B HJS   77 NOV  20     INCLUDE TIMINGS AS CALCULATED & FIX MINOR BUGS
25. . 2.9.A HJS   77 NOV  14     CHANGE KEYBOARD CODE TO AID REPEATED KEY CONTROL
26. *
27. . 2.8.B HJS   77 SEP  22     MTI CHANGE SO LENGTH IS 2 BYTE NUMBER
28. . 2.8.A HJS   77 SEP  19     MTI CHANGE TO ALLOW MFRPT ON ANY INTERRUPT
29. *
30. . 2.7.  HJS   77 SEP   7     MINOR BUG-FIX AND OPTIMIZATION FOR RELEASE
31. *
32. . 2.H.B HJS   77 AUG  31     MTI SPECIAL VERSION
33. *
34. . 2.5.C HJS   77 AUG  16     UPDATE COMMENTS ON THE CODE
35. . 2.5.B HJS   77 JULY 13     CORRECTED NAMES FOR COM REGISTERS
36. . 2.5.A HJS   77 JULY 12     UP TO NEXT NEW VERSION NUMBER
37. *
38. . 2.4.B HJS   77 JULY 12     FIXED ILLEGAL MAR CHANGE IN REGL RETURN TO FETCH
39. .                            FIXED FILE TO CONFORM TO VRP FORMAT (A LITTLE)
40. . 2.4.A HJS   77 JULY 7      INITIAL PRE-RELEASE OF THE MICRO-CODE
```

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41.                                     *
```

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42.                     +
43.                     . USEFUL INFORMATION TO BE PASSED ON:
44.                     *
45.                     . ************************************************************************
46.                     . IF SECTOR CONTAINING SEKBS1 IS WRITE PROTECTED THEN CAN NOT DO A RESTART!!!!
47.                     . ************************************************************************
48.                     . DL$DO CODE, ACC$DO & SYSRET FORCE! PRIVED MODE TO BE SURE CAN WRITE/ACCESS
49.                     . MEMORY THAT PROTECTED, FXIO, COMM MUST DO THIS ALSO!!
50.                     . ************************************************************************
51.                     . ALL SMR'S AND MDW'S MUST HAVE FOLLOWING   MWAIT ,MEMPFX    EVERYWHERE
52.                     . IN THE CODE EVEN IF  MWAIT ,$+1 IS USED (IGNORING MEMORY FAULT)
53.                     . ************************************************************************
54.                     . FOR TESTING MEMPF, CHANGE MWAIT MACRO TO BE JT,MP  $+1   <<<
55.                     . CODE THERE, TESTABLE AS USED BUT NO EFFECT!!
56.                     . ************************************************************************
57.                     . EACH SERVICE ROUTINE THAT USES THE MAR MUST HAVE A MWAIT ,$+1 BEFORE THE
58.                     . MAR CHANGED, IF NOT USED, RETURN THROUGH SRVNXT!
59.                     . ************************************************************************
60.                     . ALL INPUTS FROM A PORT INSTRUCTION SHOULD BE LOGICAL (OUTPUT CAN ONLY BE
61.                     . LOGICAL OR 'IT').
62.                     . ARITHMETICS MAY BE DONE ON INPUTS WITH CAUTION. ONLY IF THE DATA HAS NO SETU
63.                     . TIME, i.e. MDR IS OK, BUT IMPI OR URI ARE NO-NO'S.
64.                     . ************************************************************************
65.                     . DELAY AROUND SECTOR TABLE WRITES IS NOT NECESSARY.
66.                     . ************************************************************************
67.                     . DELAY DURING FONT LOAD IS ONLY AFTER LDCH.  A 400 nSEC. DELAY IS NECESSARY
68.                     . FROM AFTER LDCH TO ANY OF  RDLM, SDLM, SKCH, MAROL, OR  LDMAP.
69.                     . ALSO, RDLM AND SDLM SHOULD NOT BE TOO CLOSE TOGETHER.
70.                     . ************************************************************************
71.                     .
72.                             INC     PROCINC
```

```
14.A                        SNAPOPT   X
15.A                  * TYPE    EQU       4              DEFINE VERSION OF MACHINE TO BE ASSEMBLED
16.A                        INC       PROC14.PORTASGN     PORT ASSIGNMENT DISPLAY
```

```
. THE PORT ASSIGNMENTS, ORGANIZED BY PORT - SUBPORT NUMBER IN IN/OUT PAIRS

*
.PORT
.    SUB   0       1       2       3       4       5       6       7
.
. 0    0 O LIREG   LIMP            BASW    MODW    STW     LUF     LUCF
.      0 I MODIN                           INBUS   MIFIN   SDLCIN  ACUIN
.
. 0    0 O IIMP    DIMP    COMF    CHUF    IMAR    DMAR
.     10 I
.
. 1    0 O OTBUS   MDW     LSPKR   SDLCOT  ACUOT   SDLCMD  MIFADR  MIFDAT
.      0 I SRVREQ. STATUS          IDCODL  IDCODH  UCFLG   MDR     STEK
.
. 1    0 O MIFSTB  MIFIAK  MIFSTB2 SINS    SIOD    CSRF    CSTF    SOTS
.     10 I
.
. 2    0 O LDCH    LDMAP   SKCH    SDLM    KBSC    RDLM    CMPF    SMR
.      0 I KBDD    SNID
.
. 3    0 O URFO
.        I
.
. 4    0 O URO (MR2XXL)
.        I MARIL
.
. 5    0 O URO (MR2XXH)
.        I MARIH
.
. 6    0 O MAROL (XX2MRL)
.        I URI
.
. 7    0 O MAROH (XX2MRH)
.        I URI
.
.
. USER IO PORTS 4-7
. REGS  0 URA     URB     URC     URD     URE     URH     URL     URX
.      10 PCH     PCL     SPH     SPL     PSW     I35     I02     IMP
*
.SUBITS    0       1       2       3       4       5       6       7
.
.SRVREQ:   SCPMEM  SCMBUS  SCSDLCR SCSDLCT SCDSPNL SCONMS  SCHUMS
.
.STATUS:   STUSCF  STIODR  STPFIN  STPFOU  STKBKC  STKBNS  STKBRDY STBOILN
.
.MODW:     SWINTE  SWBASD  SWUSER          SWSTDT  SWRPT           SWALBT
.
.STEK:     STLA                                                    STLW    STLSP
.
```

```
                        . THE PORT ASSIGNMENTS, ORGANIZED BY PORT - SUBPORT NUMBER IN IN/OUT PAIRS
52.H                    *
53.H                    . JUMP INPUT CONDITION CODES ARE:
54.H                    .
55.H                    .SELECT    0       1       2       3       4       5       6       7
56.H                    .
57.H                    .         CARRY   ZERO    MEMRDY  PARITY  IMPZERO IMPODD  BUSRDY  TRUE
58.H                    .
59.H                    *
60.H                    . DOUBLY NAMED (SUB)PORTS ARE:
61.H                    .
62.H                    .         URO     <>  MR2XXL
63.H                    .         URO     <>  MR2XXH
64.H                    .         MAROL   <>  XX2MRL
65.H                    .         MAROH   <>  XX2MRH
66.H                    .
17.A                              INC       PROC14.PROCP4     INDIRECT TO PARAMETER FILE
 1.I 000002             VER       EQU       2                 1800 - INFO INSTRUCTION PROCESSOR NUMBER
 2.I 000014             REV       EQU       014               INFO INST. MICRO-CODE REVISION NUMBER
 3.I                    .
 4.I 000004             TYPE      EQU       4                 =0 FOR 1800 PROCESSOR (DISK, ICA)
 5.I                    .                                     =1 FOR 1871 PROCESSOR (DISK, ICA, APF/AML)
 6.I                    .                                     =2 FOR 3800 PROCESSOR (ICA)
 7.I                    .                                     =3 FOR 3802 PROCESSOR (RIM)
 8.I                    .                                     =4 FOR 38MP PROCESSOR (IMA)
 9.I                    *
10.I                              SNAPOPT   X
11.I                    *
```

```
14.I                    *
15.I                    . CONDITION CODES
16.I                    .
17.I 020002             MO          EQU     F6+2            MEMORY READY
18.I 020003             MP          EQU     F6+3            MEMORY FAILURE (OF ANY SORT!)
19.I 020004             IZ          EQU     F6+4            IMPLICIT REGISTER ZERO
20.I 020005             IO          EQU     F6+5            IMPLICIT REGISTER ODD
21.I 020006             BR          EQU     F6+6            BUS READY (MICRO-BUS ONLY)
22.I                    *
23.I                    . REGISTER ALLOCATION
24.I                    .
25.I 010002             Q           EQU     F5+02           NOBODY SHOULD DO WRITE'S TO Q
26.I                    .
27.I 010000             PDLNP       EQU     F5+0            DISPLAY LINE POINTER
28.I 010001             KBSCNT      EQU     F5+01           KEYBOARD SCAN COUNTER
29.I 010002             SCANSV      EQU     F5+02           KEYBOARD SAVED SCAN NUMBER, REPEATED AI
30.I                    *
31.I                    . DISKETTE CONTROL REGISTERS
32.I                    .
33.I 010003             MADR        EQU     F5+03           DISKETTE DEVICE ADDRESS
34.I 010004             MBITS       EQU     F5+04           DISKETTE I/O CONTROL, FUNCTION & STATUS
35.I 010005             MBSTAT      EQU     F5+05           DISKETTE STATE CONTROL LINK REGISTER
36.I 010006             MCRCH       EQU     F5+06           DISKETTE CRC GENERATOR STORAGE REG.
37.I 010007             MCRCL       EQU     F5+07           DISKETTE CRC GENERATOR STORAGE REG.
38.I 010010             MDSKS       EQU     F5+010          DISKETTE HEADER READ SECTOR NUMBER
39.I 010011             MDSKT       EQU     F5+011          DISKETTE HEADER READ TRACK NUMBER
40.I 010012             MTRAK       EQU     F5+012          DISKETTE USER DESIRED TRACK NUMBER
41.I 010013             MSECT       EQU     F5+013          DISKETTE USER DESIRED SECTOR NUMBER
42.I                    .                                   * APF VERSION ABOVE 2 BYTES IN MEMORY *
43.I                    *
44.I                    . HONEYWELL-APF DMA CHANNEL CONTROL REGISTERS
45.I                    .
46.I 010013             APFRP       EQU     F5+013          APF RECEIVER POINTER LSB
47.I 010014             APFRK       EQU     F5+014          APF RECEIVER COUNTER LSB
48.I 010015             APFTP       EQU     F5+015          APF TRANSMITTER POINTER LSB
49.I 010016             APFTK       EQU     F5+016          APF TRANSMITTER COUNTER LSB
50.I                    *
51.I                    . AUDIO CHANNEL CONTROL REGISTER
52.I                    .
53.I 010015             ACD         EQU     F5+015          AUDIO CHANNEL ATTEN/VALUE
54.I 010016             ACPL        EQU     F5+016
55.I 010017             ACPH        EQU     F5+017          AUDIO CHANNEL CONTROL & MSB POINTER
56.I 010017             ACCTL       EQU     ACPH            APF - AUDIO CHANNEL 1 BYTE CONTROL
57.I                    .                                   (ACPH & ACCTL SHOULD BE SAME REG.)
```

. EXTENDED CONDITIONS, AND SYSTEM REGISTER DEFINITIONS

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58.I                    *
59.I                    . TEMPORARIES - AVAILABLE IN ANY ROUTINE, LOST BETWEEN ROUTINES
60.I                    .
61.I 030000             LINK      EQU     F5+F6+00          SUBROUTINE CALL AND RETURN LINKAGE REGS
62.I 030001             TEMP1     EQU     F5+F6+01          PROCESSOR EMULATION TEMPORARIES
63.I 030002             TEMP2     EQU     F5+F6+02
64.I 030001             TEMPH     EQU     TEMP1             H & L ONLY FOR DOUBLE H/L MACROS
65.I 030002             TEMPL     EQU     TEMP2
66.I                    *
67.I                    . COMMUNICATIONS CHANNEL CONTROL REGISTERS
68.I                    .
69.I 030003             RSTAT     EQU     F5+F6+03          COM RECEIVER STATUS
70.I 030004             RPNTR     EQU     F5+F6+04          COM RECEIVER MEMORY POINTER
71.I 030005             RDATA     EQU     F5+F6+05          COM RECEIVER DATA
72.I 030006             RCRCH     EQU     F5+F6+06          COM RECEIVER CRC GENERATOR STORAGE AREA
73.I 030007             RCRCL     EQU     F5+F6+07          COM RECEIVER CRC GENERATOR STORAGE AREA
74.I 030010             UXPNTR    EQU     F5+F6+010         USER TRANSMIT BUFFER POINTER
75.I 030011             COMMODE   EQU     F5+F6+011         COMMUNICATION MODE CONTROL REGISTER
76.I 030012             URPNTR    EQU     F5+F6+012         USER RECEIVE BUFFER POINTER
77.I 030013             XSTAT     EQU     F5+F6+013         COM TRANSMITTER STATUS
78.I 030014             XPNTR     EQU     F5+F6+014         COM TRANSMITTER MEMORY POINTER
79.I 030015             XDATA     EQU     F5+F6+015         COM TRANSMITTER DATA
80.I 030016             XCRCH     EQU     F5+F6+016         COM TRANSMITTER CRC GENERATOR STORAGE
81.I 030017             XCRCL     EQU     F5+F6+017         COM TRANSMITTER CRC GENERATOR STORAGE
82.I                    *
83.I                    . INTERNAL MULTI-PORT ADAPTER CONTROL REGISTER
84.I                    .
85.I                    .COMMODE  EQU     F5+F6+011!!!      COMMUNICATIONS MODE
86.I 010013             TRNFCN    EQU     F5+013            TX CONTROL LINE SHADOW
87.I 030003             TRNCHN    EQU     F5+F6+03          TRANSMITTING CHANNEL NUMBER
88.I 030004             TRNDTA    EQU     F5+F6+04          TRANSMITTING CHANNEL DATA
89.I 030005             TRNCTL    EQU     F5+F6+05          TRANSMITTING CHANNEL CONTROL
90.I 030006             TRNSEL    EQU     F5+F6+06          TRANSMITTING CHANNEL SELECTION
91.I 030007             RCVCTL    EQU     F5+F6+07          RECEIVER CONTROL REGISTER
92.I 030010             RCH0C     EQU     F5+F6+010
93.I 010014             RCH0D     EQU     F5+014            SWAP OUT WITH COMMODE
94.I 030012             RCH1C     EQU     F5+F6+012
95.I 030013             RCH1D     EQU     F5+F6+013
96.I 030014             RCH2C     EQU     F5+F6+014         RECEIVER CHANNEL & DATA REGISTERS
97.I 030015             RCH2D     EQU     F5+F6+015
98.I 030016             RCH3C     EQU     F5+F6+016
99.I 030017             RCH3D     EQU     F5+F6+017
```

```
 100.I                          *
 101.I                          . CAPABILITY BITS:
 102.I                          .    THESE BITS DEFINE THE VERSION OF THE 1800/3800 PROCESSOR THAT THIS IS FOR
 103.I                          .
 104.I                          .    XX XXX XXX
 105.I                          .              0 --- MICRO I/O BUS AVAILABLE
 106.I                          .             1 ---- 1500 SINGLE DENSITY DISKETTE DRIVE AVAILABLE
 107.I                          .            2 ----- 1800 SINGLE/DOUBLE DISKETTE DRIVE AVAILABLE
 108.I                          .          3 ------- APF SPECIAL MICRO-BUS INTERFACE AVAILABLE
 109.I                          .         4 -------- INTERNAL MULTIPORT ADAPTER AVAILABLE
 110.I                          .        5 --------- INBOARD RIM AVAILABLE
 111.I                          .      6 ----------- 5500 I/O BUS AVALIABLE
 112.I                          .    7 ------------ COMMUNICATIONS INTERFACE AVAILABLE (ASYNC, BISYNC, & SDLC)
 113.I                          .
 114.I                          . *PROCESSOR*                          1800 1871 3800 3802 38MP
 115.I 000000                   CAPMICR   EQU      0<0                  YES  YES
 116.I 000002                   CAPIMA    EQU      1<1                                      YES
 117.I 000000                   CAPBLUE   EQU      0<2                  YES  YES
 118.I 000000                   CAPAPF    EQU      0<3                       YES
 119.I 000000                   CAPDMPIO  EQU      0<4                                 YES
 120.I 000000                   CAPRIM    EQU      0<5                                 YES
 121.I 000100                   CAP55IO   EQU      1<6                  YES  YES  YES       YES
 122.I 000000                   CAPCOM    EQU      0<7                  YES  YES  YES
 123.I                          . *TYPE*                                0    1    2    3    4
 124.I                          .
 125.I 000102                   CAPABILI  EQU   CAPCOM+CAP55IO+CAPRIM+CAPDMPIO+CAPAPF+CAPBLUE+CAPIMA+CAPMICR
 126.I                          *
 127.I                          . LOCATION OF THE CODE IN ROMS IS A FOLLOWS   (MSB & LSB OF COURSE)
 128.I                          .
 129.I 000000                   PROC      EQU      00<9            EMULATION SUPPORT CODE IN ROMS 0 & 1
 130.I 002000                   PROD      EQU      02<9            EMULATION SUPPORT CODE IN ROMS 2 & 3
 131.I 004000                   FLEX      EQU      04<9            MICRO-BUS CODE IN ROMS 4 & 5
 132.I 006000                   CDOX      EQU      06<9            COMM TRANSMIT CODE IN ROM 6
 133.I 007000                   CDOR      EQU      07<9            COMM RECEIVE CODE IN ROM 7
 134.I                          .
 135.I 000000                   CAPIVS    EQU       0
  18.A 000111                   PRE       EQU       'I'            RELEASE LEVEL (FINAL IS BINARY ZERO)
  19.A                          *
D 20.A 000000                   CAPIVS    EQU       0              INVERTED DISPLAY SCREEN VERSION **NEW**
  21.A                          *                                  0 = NORMAL, 1 = INVERTED (PURE RASTER!)
  73.                           .
  74.  000000                   PROCL     ORG       PROC           LOGICAL SPACE IN ROM'S
  75.  000000                   PROCP     ORG       0              PHYSICAL SPACE DONE AT LINK TIME
  76.  000000                   PROCL     USE       PROCL          ENABLE BOTH ADDRESS SPACES
  77.  000000                             USE       PROCP          BUILD CODE IN PHYSICAL SPACE
  78.  000000L                  PROCP     LOC       PROCL,2        LOC'ING TO LOGICAL ADDRESSES
```

```
                        . POWER ON RESTART, INITIALIZE THE WORLD
 81.                    *
 82.  000000L           POR:
 83.
 84.                    . INITIALIZE ALL CONTROL TABLES THAT CAN NOT BE INIT'D BY POR MACRO CODE
 85.
 86.  000000L 01011001 11111111          BPGX    $
 87.                                .     STB     RDLM            DO NOT CLEAR UP THE DISPLAY
 88.  000001L 11000100 11111110          MWAIT   ,IGNORE         TIMEOUT SAFETY (IGNORE MEMORY FAULT)
 89.  000002L 00110111 01000110          STB     CMPF            (INSTEAD OF FAULT JUMP)
 90.                                .                             T-REG IS ZERO FOR THE FOLLOWING
 91.  000003L 01010001 00000000          LDPI    PSW0,0          SET EMULATION PSW
      000004L 00110111 10001100
 92.  000005L 00110111 00000100          LDPT    MODW            PORT CONTROLS APPROPRIATLY
 93.  000006L 00110111 00000011          LDPT    BASW            BASE REGISTER IS INITIALLY ZERO
 94.  000007L 00000111 11110101          LDRT    MBSTAT          MICRO-BUS STATE INITIALLY OFF!
 95.  000010L 00000111 11110100          LDRT    MBITS           MICRO-BUS INITIALLY CLEARED FOR ACTION
 96.  000011L 00000111 11111111          LDRT    ACPH            NO AUDIO CHANNEL INITIALLY
 97.  000012L 00000111 11110001          LDRT    KBSCNT          SAVE THE SCAN NUMBER AND
 98.  000013L 00110111 01000100          LDPT    KBSC            START THE FIRST KEY SCAN
 99.
100.  000014L 00110111 00100101          LDPT    SDLCMD          COMM OUTPUT IS OFF (MODEM OUTPUT)
101.  000015L 00110111 00100100          LDPT    ACUOT           AUTO CALL UNIT IS OFF (OR IMA IN MARK)
102.  000016L 01101111 11111001          LDRT    COMMODE         FLUSH THE COMMODE! ("MURF")
103.                                    IFS     CAPIMA
104.  000017L 00000111 11111011          LDRT    TRNFCN          INIT TX MODEM CONTROLS (NOT FIRST EXADR)
105.
106.  000020L 01101111 11110111    .     LDRT    RCVCTL          NO RECEIVER HAS DATA BUFFERED (YET)
107.  000021L 01101111 11110101          LDRT    TRNCTL          NO TRANSMITTER HAS DATA FOR OUTPUT
108.  000022L 01101111 11110110          LDRT    TRNSEL          NO TRANSMITTER IS SELECTED FOR OUTPUT
109.  000023L 01101111 11110011          LDRT    TRNCHN          ALL TRANSMITTER CHANNELS ARE MARK
110. >000024L 01010001 11111111          BAL     RCH0C,RCVMRK    RECEIVER CHANNEL ZERO WAITING IN MARK
      000025L 01101111 11111000
111.  000026L 01101111 11111010          BAS     RCH1C           RECEIVER CHANNEL ONE WAITING IN MARK
112.  000027L 01101111 11111100          BAS     RCH2C           RECEIVER CHANNEL TWO WAITING IN MARK
113.  000030L 01101111 11111110          BAS     RCH3C           RECEIVER CHANNEL THREE WAITING IN MARK
114.                                    XIF
115.
116.  000031L 01010001 11111111          LDRI    MADR,-1         NO DEVICE ACCESSED YET ON MICRO-BUS
      000032L 00000111 11110011
117.  000033L 01010001 10011100          LDRI    PDLNP,SEDLBOT,CC POINT TO THE BOTTOM LINE
      000034L 00000111 10110000
118.  000035L 01010001 00100100          LDPI    PCOL,SRTMOUT    ASSUME THAT A TIMEOUT WILL HAPPEN
      000036L 00110111 10001001
119.  000037L 00110001 00110111          TSTIP   ,STLIMOUT,STEK  CHECK IF IT DID
      000040L 01000101 00000010
120.  000041L 11000010 11001000          BRA     POROUT,FZ       YES, DON'T INIT STL OR MEMORY
121.
122.                    . MUST INIT SECTOR TABLE & ZERO SYSESR OR IMMEDIATE RESTART OR MEMPF
123.
124.  000042L 01010001 00001100          LDTI    STAE+STWE       INIT WHOLE SECTOR TABLE
125.  000043L 00110111 11100000  PORLST   LDPT    MAROH,STW
      000044L 00110111 00000101
```

```
                . POWER ON RESTART, INITIALIZE THE WORLD

126.  000045L 01010010 00010000          DOTI    ,AC,16              LOOP TILL ALL ARE ACCESS & WRITE ENABLE
127.  000046L 11000000 11011100          BRA     PORLST,FC
128.
129.  000047L 01010001 11110000          LDPI    STW,SYSROM>8.AND.0360 SECTOR 017 IS SYSTEM ROM, PROTECT IT
      000050L 00110111 00000101
130.  000051L 01010001 11101111          LDPI    MAROH,SYSESR>8      POINT TO THE EMULATION SUPPORT PAGE
      000052L 00110111 11100000
131.  000053L 01010001 00000000          LDPI    MAROL,SYSESR        START OF IT (T-REG IS ZERO)
      000054L 00110111 11000000
132.  000055L 01101111 11110010          LDRT    TEMPL               INITIALIZE THE COUNTER
133.  000056L 00110111 00001101          STB     DMAR                CORRECT MAR SO ALL OF PAGE INITED
134.
135.  000057L 00110111 00001100  PORZRO   STB     IMAR,MDW            ZERO THE NEXT BYTE (T-REG IS ZERO)
      000060L 00110111 00100001
136.  000061L 01110001 11110010          INCR    TEMPL,TEMPL         COUNT ALL OF THE BYTES IN THE PAGE
      000062L 01101110 01110010
137.  000063L 01010001 00000000          LDTI    0                   DATA TO BE WRITTEN IS ZERO
138.  000064L 11000100 11001011          MWAIT   ,IGNORE             !! IGNORE ANY AND ALL FAULTS !!
139.  000065L 11000000 11010000          BRA     PORZRO,FC           CONTINUE TILL ALL PAGE DONE
140.                            *
141.  000066L 00110111 10001001  FETPC    LDPT    PCOL                LOAD THE PC LSB ADDRESS
142.
143.  000067L 01010001 11110000  POROUT   LDPI    PCOH,SYSROM>8
      000070L 00110111 10001000
144.
145.                            . NOTE:  NORMALLY HERE, PCL IS ZERO AND PCH = SYSROM>8
146.                            .        THIS GENERATES A POINTER TO SRPOWER-UP VECTOR ENTRY
147.
148. >000071L 01011001 11111111          BRAX    RETS                OK, MICRO-POR DONE, DO MACRO POR
     >000072L 11001111 11111111
149.                            .                                    (OR TIMEOUT) (OR SC ERROR)
```

```
                                *
                                        IFC     CAPIMA          **ONLY FOR NON-IMA VERSION**
                                        XIF
000073L 01010001 00000110       MINPAR  LDTI    SVINP           USE PARITY INPUT ERROR VECTOR
000074L 11001111 01000110               BRA     SCLSTW          AND CALL SUPERVISOR ERROR ROUTINE
                                .                               PC CORRECT OR BACK UP IF IMP NON-ZERO
                                *
000075L                         MINOWT
                                . COMMON MIN/MOUT FINAL TERMINATION CODE
000075L 00110111 00101100               STB     SIOD            DOUBLE DELAY AT THE END
000076L 00110001 11011100               DOPIP   PSWO,ND,-1-SWRPT,PSWI TURN OFF THE REPEATED FLAG
000077L 01010101 11011111
000100L 00110111 10001100
000101L 00110111 00000100               LDPT    MODW            RESET IT AND EI/DI BITS
                                        IFC     CAPIMA          * MINOWT FALLS THROUGH TO OUTW1 IFS CAPIMA
                                        XIF
000102L 00110001 00110001       OUTW1   TSTIP   ,STIODR,STATUS
000103L 01000101 00000010
000104L 11000011 10111101               BRA     OUTW1,TZ        DELAY 1 WAITING FOR COMMAND TO GET THER
000105L 00110111 00101100               STB     SIOD            EXTEND THE COMMAND DELAY FOR FINAL STEP
000106L 00110001 00110001       OUTW2   TSTIP   ,STIODR,STATUS
000107L 01000101 00000010
000110L 11000011 10111001               BRA     OUTW2,TZ        DELAY 2 WAITING FOR PARITY TO RETURN
000111L 01000101 00001000               TSTIT   ,STPFOU         WAS THERE AN OUTPUT PARITY FAULT?
000112L 11000011 01100011               BRA     FTCHIO,TZ       NO!
000113L 01010001 00001100       MOTPAR  LDTI    SVOUTP          YES, TELL SUPERVISOR THAT THERE WAS
000114L 11001111 01000110               BRA     SCLSTW
```

```
                                +
                                MIN:
                                . NOTE: IF  EI / MIN, THE EI DOESN'T TAKE EFFECT UNTIL THE INSTRUCTION
                                .       AFTER THE MIN. ONE LATER THAN ON 5500
                                .       BUT, IF MIN INTERRUPTED AT MACRO LEVEL FOR ANY REASON,
                                .       WHEN IT IS RETURNED IT WILL BE AS IF THE EI HAD ALREADY TAKEN EFFECT!
                                .
                                .        (111 061)  MIN                 MULTIPLE INPUT
                                . 5.15~5.60 + C * 8.30                  (HL) <- INBUS; HL <- HL + 1
                                .                                       C <- C - 1; RPT UNTIL C=0 (16)
                                .
000115L 00110001 11011100               TSTIP   ,SWUSER,PSWI
000116L 01000101 00000100
000117L 11000010 01001001               BRA     IVIOL$,FZ               ONLY CONTINUE IF PRIVED
                                        IFS     CAPIMA
000120L 01000101 00001000               TSTIT   ,SWIDEV
000121L 11000010 11000100               BRA     MINPAR,FZ               ** MIN'S ILLEGAL ON 9462 **
                                        XIF
000122L 01010101 11111110               DOPI    MODW,ND,-1-SWINTE       DISABLE ONE MS. INTERRUPTS
000123L 00110111 00000100
000124L 00110001 11000110               DLDX    HL2MR                   PRELOAD MAR WITH WHERE TO SAVE DATA
000125L 00110001 11100101
000126L 00110001 01010001               LDTP    SNID                    ADD 0.15 DELAY TO MATCH TIMING OF 6600!!
000127L 00110111 00101100               STB     SIOD                    START ZEROTH DELAY
000130L 00110001 00110001       MINW0   TSTIP   ,STIODR,STATUS          WAIT ON INITIAL DELAY
000131L 01000101 00000010
000132L 11000011 10100111               BRA     MINW0,TZ
000133L 01000101 00000100               TSTIT   ,STPFIN
000134L 11000010 11000100               BRA     MINPAR,FZ               DO NOT CONTINUE IF PARITY FAULT
000135L 00110001 00010100               LDPP    SINS,INBUS,MDW          GET DATA FAST ACKNOWLEDGE AND SAVE IT
000136L 00110111 00101011
000137L 00110111 00100001
000140L 00110001 10010000               DADDP   URO+UR,MARI             UPDATE HL, SADLY CAN'T BE TOO FAST
000141L 00010110 01110010
000142L 00110111 10000110
000143L 00110001 10110000
000144L 00110110 10000101
000145L 01010001 00110001               LDRI    TEMP1,CODMIN,CC         NEEDED ONLY FOR COMMON SPEEDUP CODE
000146L 01101111 10110001
000147L 11001111 01111011               BRA     MINOUT                  GO TO COMMON MIN/MOUT CODE
```

```
                                                +
                                                MOUT:
                                                . NOTE: SEE THE NOTE IN MIN IN RELATION TO EI
                                                .       (111 071)  MOUT              MULTIPLE OUTPUT
                                                . 5.15~5.60 + C * 8.50~9.60          OUTBUS <- (HL); HL <- HL + 1
                                                .                                    C <- C - 1; RPT UNTIL C=0 (16)
000150L 00110001 11000110                               DLDX    HL2MR,,SMR           GET DATA AS SOON AS POSSIBLE
000151L 00110001 11100101
000152L 00110111 01000111
000153L 00110001 11011100                               TSTIP   ,SWUSER,PSWI         ONLY CONTINUE IF PRIVED
000154L 01000101 00000100
000155L 11000010 01001001                               BRA     IVIOL$,FZ
                                                        IFS     CAPIMA
000156L 01000101 00001000                               TSTIT   ,SWIDEV
000157L 11000010 01101011                               BRA     IMAOUT,FZ
                                                        XIF
000160L 01010101 11111110                               DOPI    MODW,ND,-1-SWINTE    DISABLE ONE M.SEC. INTERRUPT
000161L 00110111 00000100
000162L 11000100 10001101                               MWAIT   ,MEMPF0
000163L 11010111 00000101
000164L 00110001 00110110                               LDPP    OTBUS,MDR,SIOD       OUTPUT DATA AND START DELAY
000165L 00110111 00100000
000166L 00110111 00101100
000167L 01010001 01010111                               LDPI    LIREG,CODWRT         FIX IT UP FOR THE SOTS
000170L 00110111 00000000
000171L 00110001 00110001       MOTW0                   TSTIP   ,STIODR,STATUS
000172L 01000101 00000010
000173L 11000011 10000110                               BRA     MOTW0,TZ             DELAY WHILE DATA GETS TO THE DEVICE
000174L 01000101 00001000                               TSTIT   ,STPFOU
000175L 11000010 10110100                               BRA     MOTPAR,FZ            DO THE PARITY CHECK (FASTER THAN EX COM
000176L 00110111 00101111                               STB     SOTS                 OK, SO DO THE COMMAND NOW!
000177L 00110111 00001100                               STB     IMAR
000200L 00110001 10000110                               DLDX    MR2HL                UPDATE HL (THIS IS FASTEST WAY)
000201L 00110001 10100101
000202L 01010001 00111001                               LDRI    TEMP1,CODMOUT,CC     FOR MINOUT CODE
000203L 01101111 10110001
                                                *
000204L                                         MINOUT
000204L 00110001 00110001       MINW1                   TSTIP   ,STIODR,STATUS       WAIT ON ACK. TO GET TO THE DEVICE
000205L 01000101 00000010
000206L 11000011 01111011                               BRA     MINW1,TZ
                                                . * * *  7.00~8.10 - MOUT
                                                .        6.80 - MIN
                                                . * * *  1.50 - RPT
                                                .        6.65~7.1 - END
000207L 00110001 11010010                               DOPIP   URFO+URC,SB,1,URI+URC DECREMENT THE COUNT IN C
000210L 01010100 00000001
000211L 00110111 01100010
```

```
336.  000212L 01000101 00001111          TSTIT   ,017            BASE 16 END?
337.  000213L 11000011 11000010          BRA     MINOWT,TZ       COMPLETE AS A SIMPLE EX COM
338.  000214L 01110001 11110001          LDPR    LIREG,TEMP1     RESTORE TO MIN OR MOUT
      000215L 00110111 00000000
339.                                     *
340.  000216L 11000100 01110001          MWAIT   ,MEMPF0         WAIT ON MIN MDW TO FINISH
      000217L 11010111 00000101
341.  000220L 00110001 00110000          TSTPT   FI,SRVREQ       ANY SERVICE REQUESTS? THEN DO THEM
342.  000221L 10100011 00110011          BRP     IDCODL,TZ       ELSE, CONTINUE MIN'ING OR MOUT'ING
343.                                     .                       (I KNOW ITS ON THIS PAGE)
344. >000222L 01011001 11111111          BRAX    SRVRPT          DO SERVICE
     >000223L 11001111 11111111
345.                                              XIF
346.                                              IFS     CAPIMA
347.  000224L                           IMAOUT
348.  000224L 01010001 00001111          LDPI    LIMP,IMPL       FAKE OUT THE EXWRITE CODE
      000225L 00110111 00000001
349.  000226L 11000100 01101001          MWAIT   ,MEMPF0
      000227L 11010111 00000101
350.  000230L 00110001 00110110          LDPP    IMPO,MDR        BY PUTTING MEMORY DATA IN HIDDEN REGISTER
      000231L 00110111 10001111
351. >000232L 01011001 11111111          BRAX    EXMOUT          AND GO TO COMMON POINT IN CODE
     >000233L 11001111 11111111
352.
353. >000234L 01011001 11111111  FTCHIO  BRAX    FETCHW          NEEDED ON THIS PAGE FOR IMA VERSION
     >000235L 11001111 11111111
354.                                              XIF
```

```
                                *
                                . NOTE:  FOR INSTRUCTION ENTRIES THE WAY THE PC SHOULD BE LEFT IS SPECIFIED
                                *
000236L                         BP:                                 !! PC LEFT AFTER THE INSTRUCTION
                                .       (    052)  BP               BREAKPOINT
                                . 9.45~9.65                         (SP-2 I SP-1) <- PC
                                .                                   SP <- SP - 2; PC <- BRKPNT

000236L 01010001 00110000               LDTI    SVBKPNT             DEBUGGING BREAKPOINT RAM VETCOR
000237L 11001111 01011010               BRA     SCBP
                                *
000240L                         SC:                                 !! PC LEFT AFTER THE INSTRUCTION
                                .       (    067)  SC               SYSTEM CALL (SUPERVISOR CALL)
                                . 9.45~9.65                         (SP-2 I SP-1) <- PC
                                .                                   SP <- SP - 2; PC <- SYSCAL

000240L 01010001 00101010               LDTI    SVSCAL              SUPERVISOR CALL RAM VECTOR
000241L 11001111 01011010               BRA     SCBP
                                *
000242L                         SCRAMI:                             !! PC LEFT AFTER THE INSTRUCTION
000242L 00110001 11001001               DLDX    PC2MR               !! MEMORY ACCESS & WRITE VOILATIONS
000243L 00110001 11101000
000244L 01110001 11110010               LDTR    TEMPL                 CORRECT FOR IT
                                *
000245L                         SCBP                                !! UP THE PC TO NEXT INSTRUCTION
                                . 9.15~9.35                         !! RAM VECTOR FOR INTERRUPT

000245L 01101111 11110010               LDRT    TEMPL               RAM VECTOR SAVED
000246L 00110111 00001100               STB     IMAR                CORRECT THE PC
000247L 11001111 00111111               BRA     SCPC
                                *
000250L                         SCROMLI:                            !! UP THE PC TO NEXT INSTRUCTION
                                .                                   !! MEMORY OR SECTOR TABLE PARITY ERROR
000250L 01101111 11110010               LDRT    TEMPL               ROM VECTOR SAVED
000251L 00110001 11001001               DLDX    PC2MR,,IMAR         TO THE NEXT OP-CODE
000252L 00110001 11101000
000253L 00110111 00001100
000254L 00110001 10001001               DLDX    MR2PC
000255L 00110001 10101000
000256L 11001111 01001111               BRA     SCROM
```

```
393.                                    *
394.  000257L                          SCROML:                         !! ROM VECTOR ENTRY, PC ALREADY OK?
395.                                    .                               !! FAULT INSIDE MEMORY FAULT ROUTINE
396.                                    .                               !! RESTART, DEC PC ALREADY DONE AS NEED
397.
398.  000257L 01101111 11110010                 LDRT    TEMPL
399.  000260L 01010001 11110000        SCROM:  LDRI    TEMPH,SYSROM>8
      000261L 01101111 11110001
400.  000262L 11001111 00111011                 BRA     SCDON
```

```
401.                                    +
402.  000263L                          UDPOP:                          !! PC LEFT AT NEXT INSTRUCTION
403.                                    .       (    000)  HALT         UNDEFINED PRIVILEDGED OP
404.                                    .       (    001)  HALT         (SP-1 ! SP-1) <- PC
405.                                    .       (    377)  HALT         SP <- SP - 2; PC <- IVIOL
406.                                    . 9.45~9.65 (+0.10 IF NOT USER MODE)
407.
408.  000263L 00110001 11011100                  TSTIP   ,SWUSER,PSWI
      000264L 01000101 00000100
409.  000265L 11000011 01000111                  BRA     UDOP,TZ         UNDEFINED IF IN USER MODE
410.                                    *
411.  000266L 01010001 00011110  IVIOL$:  LDTI    SVIVIOL                 !! PC LEFT AT LAST INSTRUCTION
412.  000267L 11001111 01000110          BRA     SCLSTW                  TRIES PRIV'D INSTRUCTION WHILE USER MOD
413.                                    *
414.  000270L                          UDOP:                           !! PC LEFT AT LAST INSTRUCTION
415.                                    .       (    147)               UNDEFINED OP-CODE
416.                                    .       (    171)               (SP-2 ! SP-1) <- PC
417.                                    .       (    173)               SP <- SP - 2; PC <- UAINST
418.                                    .       (    175)
419.                                    .       (    177)               UNDEFINED (EXCEPT APF VERSION)
420.                                    . 9.00~9.20 (+0.65 IF IMP # 0)
421.
422.  000270L 01010001 00110110                  LDTI    SVUAINS         UNDEFINED OP-CODE VECTOR SYSCALL
423.                                    *
424.  000271L                          SCLSTW:                         !! RAM VECTOR INTERRUPT
425.                                    .                               !! 5500 I/O BUS PARITY ERROR
426.                                    .                               !! BACKUP PC TO START OF
427.                                    .                               !! INTERRUPTING INSTRUCTION
428.
429.  000271L 11000100 01000110                  MWAIT   ,MEMPF0
      000272L 11010111 00000101
430.  000273L 01101111 11110010                  LDRT    TEMPL           SAVE RAM VECTOR ADDRESS
431.  000274L 11001001 00111101  SCLST:  BRA     SCRAM,T@,IZ             POINTS TO START OF LAST INSTRUCTION.
432.                                    .                               !! 1 MSEC INTERRUPT WHEN REPEATED
433.  000275L 00110001 11001001          DLDX    PC2MR,,DMAR             BACK UP TO IMP SPEC CODE
      000276L 00110001 11101000
      000277L 00110111 00001101
434.  000300L 00110001 10001001  SCPC    DLDX    MR2PC                   !! SYSTEM CALL PERFORM SECTION
      000301L 00110001 10101000
435.                                    .                               SAVE P.C. AS SHOULD BE
```

```
436.                                    *
437.  000302L 01010001 11101111  SCRAM:  LDRI   TEMPH,SYSIVR>8   !! RAM VECTOR DOESN'T WANT PC BACKUP
      000303L 01101111 11110001
438.                                    .                       !! 1 MSEC INTERRUPT WHEN NOT REPEATED
439.                                    *
440.  000304L                           SCDON:
441.                                    . 8.20~8.40
442.
443.  000304L 01010001 11110000          LDPI   MAROH,SYSROM>8.AND.0360 CORRECT ENTRY 017 TO BE SURE
      000305L 00110111 11100000
444.  000306L 00110111 00000101          LDPT   STW              IN THE SECTOR TABLE
445.  000307L 01010001 11000000          LDTI   0300
446.  000310L 00110101 11001011          DOP    SP2MRL,ND        POINT TO THE PSW SAVE BYTE
447.  000311L 00110001 11101010          LDX    SP2MRH,DMAR
      000312L 00110111 00001101
448.  000313L 00110001 11011100          DOPIP  MODW,ND,-1-SWSCF,PSWI CLEAR NECESSARY SYSCALL FLAGS
      000314L 01010101 11011010
      000315L 00110111 00000100
449.  000316L 00110001 11011100          LDPP   MDW,PSWI         SAVE ORIGINAL PSW IN ITS SAVE AREA
      000317L 00110111 00100001
450.  000320L 01010101 11011010          DOPI   PSWO,ND,-1-SWSCF SET NEW SYSCALL FLAGS
      000321L 00110111 10001100
451.  000322L 01010001 00001001          LDPI   LIMP,PCL         GET SET FOR PUSH OF THE P.C.
      000323L 00110111 00000001
452.  000324L 11000100 00101011          MWAIT  ,IGNORE          WAIT ON WRITE & IF ERROR, TROUBLE
453. >000325L 01011001 11111111          BRCX   PSHSTO,F@,MP,PCMOD IF NO ERROR, GO TO IT (SAVED 1 WORD)
     >000326L 01010001 11111111
     >000327L 11000110 11111111
454.                                    *
455.  000330L                           MEMPFSC
456.                                    . WOW! SYSTEM SAVE AREA HAD SECTOR TABLE OR WRITE PROTECT FAULT
457.                                    .      USE THE ROM VECTOR POINT TO MARK A DOUBLE BAD INTERRUPT
458.
459.  000330L 01010001 00000110          LDTI   SRSYSMF          DO SPECIAL INTERRUPT
460.  000331L 01011001 11111111          BRAX   FETPC            FORGET PUSH, WILL PROBABLY NOT WORK
      000332L 11001111 11001001
461.
462.  000333L 11111111 11111111          TABPAGE PROCL
      000334L 11111111 11111111
      000335L 11111111 11111111
      000336L 11111111 11111111
      000337L 11111111 11111111
      000340L 11111111 11111111
      000341L 11111111 11111111
      000342L 11111111 11111111
      000343L 11111111 11111111
      000344L 11111111 11111111
      000345L 11111111 11111111
      000346L 11111111 11111111
      000347L 11111111 11111111
      000350L 11111111 11111111
      000351L 11111111 11111111
```

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000352L 11111111 11111111
000353L 11111111 11111111
000354L 11111111 11111111
000355L 11111111 11111111
000356L 11111111 11111111
000357L 11111111 11111111
000360L 11111111 11111111
000361L 11111111 11111111
000362L 11111111 11111111
000363L 11111111 11111111
000364L 11111111 11111111
000365L 11111111 11111111
000366L 11111111 11111111
000367L 11111111 11111111
000370L 11111111 11111111
000371L 11111111 11111111
000372L 11111111 11111111
000373L 11111111 11111111
000374L 11111111 11111111
000375L 11111111 11111111
000376L 11111111 11111111
000377L 11111111 11111111
```

```
                                        *
000400L                                 BETA:
                                        .       (    020)  BETA             SAVE ALPHA REGS AND LOAD BETA SET
                                        . 30.60~31.40 (1.35 IN BETA)
                                        .                                   'FXLHEDCBA' <- FXLHEDCBA
                                        .                                   FXLHEDCBA <- "FXLHEDCBA"
                                        .       (111 020)  BETAL            LOAD REGS FROM BETA SAVE AREA
                                        . 16.15~16.75                       FXLHEDCBA <- "FXLHEDCBA"
                                        .       (062 020)  SYSSAV           SAVE SYSTEM REGS
                                        . 14.50~14.70 (-0.10 IF BETAS)      "'FXLHEDCBA"' <- FXLHEDCBA
                                        . NOTE: CAN NOT 1MS. INTERRUPT BETWEEN BETA & FOLLOWING INSTRUCTION.
000400L 00110001 11011100                       TSTIP   ,SWUSER,PSWI        ONLY IF PRIV'D
000401L 01000101 00000100
000402L 11000010 01001001                       BRA     IVIOL$,FZ
000403L 01000101 00100000                       TSTIT   ,SWRPT
000404L 11010010 11000110                       BRA     BETAL,FZ            IF REPEATED DO SECOND HALF
000405L 11011011 11000110                       BRA     BETAL,T@,IO         IF ODD, ONLY LOAD BETA REGS
000406L 01000101 10000000                       TSTIT   ,SWALBT             TEST HERE, SYSSAV NEEDS IT
000407L 11011000 11110010                       BRA     SYSSAV,F@,IZ        SYSTEM SAVE IF NON-ZERO
000410L 11010010 00000111                       BRA     FTCHIAB,FZ          SIMPLE BETA, FORGET IT, ALREADY IN BETA
000411L 01010011 00100000                       DOPI    PSWO,OR,SWRPT       TWO PARTS, SO REPEATED
000412L 00110111 10001100
000413L 01010001 00111110       ALPHAS          LDTI    SESAVAF.AND.0177    POINT TO CORRECT SAVE AREA (7 BITS!)
000414L 11011111 11100100                       BRA     MODSAV
                                        *
000415L                                 SYSSAV
                                        .       (062 020)  SYSSAV           SYSTEM SAVE WHICHEVER REGISTERS & FLAGS
                                        . 14.50~14.70 (-0.10 IF BETAS)      "'FXLHEDCBA"' <- FXLHEDCBA
000415L 11010011 11110100                       BRA     ALPHAS,TZ           SAVE ALL REGISTERS TO THE ALPHA SET
000416L 11011111 11100101                       BRA     BETAS               NO, TO BETA SET
```

```
                        . REGL, ALPHA, BETA MODE SWAPS AND SUB-PARTS

                        +
000417L                 ALPHA:
                        .       (    030)  ALPHA             SAVE BETA REGS AND LOAD ALPHA SET
                        . 30.60~31.20 (14.85~15.05, 16.15~16.55 IF SPLIT)
                        .                                    "FXLHEDCBA" <- FXLHEDCBA
                        .                                    FXLHEDCBA <- 'FXLHEDCBA'
                        .       (111 030)  ALPHAL            LOAD REGS FROM ALPHA SAVE AREA
                        . 16.25~16.65                        FXLHEDCBA <- 'FXLHEDCBA'
                        .       (062 030)  SYSRET            RESTORE REGS AND RETURN
                        . 25.10~25.50 (+0.10~0.30 IF BETAL)  PC <- (SP+1 | SP); SP <- SP + 2
                        .                                    FXLHEDCBA <- "'FXLHEDCBA"'

                        . NOTE: CAN NOT 1MS. INTERRUPT BETWEEN ALPHA & FOLLOWING INSTRUCTION.

000417L 00110001 11011100               TSTIP   ,SWUSER,PSWI      ONLY IF PRIVED
000420L 01000101 00000100
000421L 11000010 01001001               BRA     IVIOL$,FZ
000422L 01000101 00100000               TSTIT   ,SWRPT
000423L 11010010 10011110               BRA     ALPHAL,FZ          IF REPEATED JUST DO SECOND HALF
000424L 11011011 10011110               BRA     ALPHAL,T@,IO       NO SAVE, JUST DO ALPHA LOAD
000425L 11011000 10111010               BRA     SYSRET,F@,IZ       RELOAD REGS & RETURN
000426L 01000101 10000000               TSTIT   ,SWALBT            IS A SIMPLE ALPHA INSTRUCTION
000427L 11010011 00000111               BRA     FTCHIAB,TZ         FORGET IT, ALREADY IN ALPHA MODE
000430L 01010011 00100000               DOPI    PSWO,OR,SWRPT      MARK REPEATED BECAUSE 2 PARTS!
000431L 00110111 10001100
000432L 01010001 00110101       BETAS   LDTI    SESAVBF.AND.0177 (7 BITS) TO POINT TO THE SAVE AREA
                                .       BRA     MODSAV
```

```
525.                                        +
526.  000433L                               MODSAV                                  SAVE FLAGS AND REGS IN SAVE AREA
527.                                        . 13.05~13.25 (IF FECTHW, +0.75 IF ALPHAL, +0.65 IF BETAL, +0.50 IF SERVICE)
528.
529.  000433L 01101111 11110010                    LDRT    TEMP2                   SAVE AWAY FOR THE MOMENT
530.  000434L 00110001 11011011                    DOTIP   ,ND,0200,SPIL           GET 128 BYTE BOUNDARY BIT (1 MSBIT)
      000435L 01010101 10000000
531.  000436L 01110011 11110010                    DOPR    MAROL,OR,TEMP2          COMBINE WITH THE FLAG ADDRESS
      000437L 00110111 11000000
532.  000440L 00110001 11101010                    LDX     SP2MRH                  MSB STACK POINTER IS SAVE AREA ALSO
533.  000441L 00110001 00110101                    DOPIP   MDW,ND,0303,UCFLG       SAVE THE FLAGS, ONLY 4 BITS OF INTEREST
      000442L 01010101 11000011
      000443L 00110111 00100001
534.  000444L 01010001 00010000  REGSVLP  LDPI    LIMP,IMP8               INIT COUNT
      000445L 00110111 00000001
535.
536.  000446L 00110111 00001001  MODSVLP  STB     DIMP
537.  000447L 00110001 11011111            LDTP    IMPI                    SPEEDUP, GET DATA NOW
538.  000450L 11010100 11010111            MWAIT   ,MEMPF0
      000451L 11010111 00000101
539.  000452L 00110111 00001101            STB     DMAR                    SAVE THE REGISTER
540.  000453L 00110111 00100001            LDPT    MDW
541.  000454L 11011000 11011001            BRA     MODSVLP,F@,IZ           LOOP TILL ALL 8 REGS. ARE SAVED
542.
543.  000455L 00110001 11011100            TSTIP   ,SWRPT,PSWI             WELL, ONE OR TWO PARTS?
      000456L 01000101 00100000
544.  000457L 11010011 01101000            BRA     FTCHABW,TZ              ONLY SYSSAV, NO-LOAD NEW REGS.
545.  000460L 01010101 11111110            DOPI    MODW,ND,-1-SWINTE       TEMPORARILY DISABLE INTERRUPTS FOR IT
      000461L 00110111 00000100
546.
547.  000462L 00110001 00110000            TSTPT   FI,SRVREQ               ANY REQUESTS PENDING?
548.  000463L 11010010 10111100            BRA     MODSRV,FZ               YES, DO THEM AND I HOPE NO TROUBLE
549.  000464L 00110001 11011100            TSTIP   ,SWALBT,PSWI            WHAT WAS IT?
      000465L 01000101 10000000
550.  000466L 11010100 11001001            MWAIT   ,MEMPF0                 NEEDED AFTER MDW AT END OF LOOP ABOVE
      000467L 11010111 00000101
551.  000470L 11010010 10011110            BRA     ALPHAL,FZ               WAS BETA, DO ALPHAL NOW
552.                                        BRA     BETAL                   WAS ALPHA DO BETAL NOW
```

```
                                                +
000471L                                         BETAL
                                                .       (111 020)  BETAL            LOAD REGS FROM BETA SAVE AREA
                                                . 15.40~16.00 (HERE ON)             FXLHEDCBA <- "FXLHEDCBA"
000471L 00110001 11011011                               DOTIP    ,ND,0200,SPIL
000472L 01010101 10000000
000473L 01010011 00110101                               DOPI     MAROL,OR,SESAVBF.AND.0177 POINT TO BETA FLAGS IN SAVE AREA
000474L 00110111 11000000
000475L 00110001 11101010                               LDX      SP2MRH,SMR
000476L 00110111 01000111
000477L 00110001 11011100                               DOTIP    ,OR,SWALBT,PSWI   SET BETA MODE
000500L 01010011 10000000
000501L 01010101 11011111                               DOTI     ,ND,-1-SWRPT      RESET REPEAT FLAG (IF SET)
000502L 11011111 10010110                               BRA      MODLOD
                                                .
>000503L 01011001 11111111  MODSRV    BRAX     SRVDO             GO TO SERVICE AS NEEDED (MODSAV USES IT)
>000504L 11001111 11111111
                                                *
000505L                                         SYSRET
                                                .*      NOTE: THIS INSTRUCTION IS VERY LONG IN EXECUTION
                                                .*            IF DMA SLOWS IT EVEN FARTHER WE MAY HAVE PROBLEMS

                                                .* WARNING:   IF AS SOLUTION TO LENGTH IT IS DONE AS REPEATED INSTRUCTON
                                                .*    THEN:   IF INTERUPTED (I.E. BY RESTART-DEBUG INTERRUPT)
                                                .*            THE PC WILL REFLECT THE ADDRESS OF THE INSTRUCTION TO RETURN
                                                .*            TO, WITH REPEATED FLAG ON AND THE INCORRECT REGISTER SET IN THE
                                                .*            SUPPORT REGISTERS (THE ALPHAL OR BETAL NOT COMPLETED!)
                                                .*            THIS IS VERY BAD!  BUT POSSIBILITY IS LOW AND NO SOLUTION SEEN

                                                .* WARNING:   IF INSIDE SYSRET (REGISTER LOAD PART) THERE IS A MEMORY FAULT,
                                                .*            THE PC WILL BE INCORRECT BECAUSE OF A SPECIAL PRE-DECREMENT.
                                                .*            IF THE IMP WAS NON-ZERO, IT WILL BE EVEN FARTHER OFF

                                                .       (062 030)  SYSRET           SYSTEM RETURN (FROM SC, BP, ETC)
                                                . 24.70~25.10 (+0.10~0.30 IF BETAL) PC <- (SP+1 | SP); SP <- SP + 2
                                                .                                   FXLHEDCBA <- "'FXLHEDCBA"'
000505L 01010001 00001001                               LDPI     LIMP,PCL          GET THE RETURN ADDRESS INTO THE P.C.
000506L 00110111 00000001
>000507L 01011001 11111111                              BRCX     POPST0,,SYSRET0   OFF PAGE WITH SPECIAL RETURN
>000510L 01010001 11111111
>000511L 11001111 11111111

000512L                                 SYSRET1:
000512L 00110001 11001001                               DLDX     PC2MR,,DMAR       CORRECT FOR IMAR IN FETCH CODE
000513L 00110001 11101000
000514L 00110111 00001101
000515L 00110001 10001001                               DLDX     MR2PC
000516L 00110001 10101000
000517L 00110001 11101010                               LDX      SP2MRH            GET THE PSW
000520L 01010001 11000000                               LDTI     0300              TO BE LOADED
```

```
                                                DOP     SP2MRL,ND           FROM THE SYSTEM SAVE AREA
                                                DOPIP   MODW,ND,-1-SWUSER,PSWI  ASSUME ENTERED INST LEGALLY, (PRIVD)
000521L 00110101 11001011
000522L 00110001 11011100
000523L 01010101 11111011
000524L 00110111 00000100
                                        .                                   SO, COMPLETE IT LEGALLY IN PRIV'D MODE
                                                STB     DMAR,SMR
000525L 00110111 00001101
000526L 00110111 01000111
                                                IFC     CAPIMA              NON-IMA VERSION
                                                XIF
                                                IFS     CAPIMA              IMA-VERSION
                                                DORI    TEMP1,ND,SWIDEV+SWSTDT   SAVE OLD ADDRESSED/MODE BITS
000527L 01010101 00011000
000530L 01101111 11110001
                                                LDTI    -1-SWIDEV-SWSTDT
000531L 01010001 11100111
                                                MWAIT   ,MEMPF0
000532L 11010100 10100101
000533L 11010111 00000101
                                                DOTP    ,ND,MDR             SELECT ONLY THOSE BITS THAT CAN CHANGE
000534L 00110101 00110110
                                                DOPR    PSW0,OR,TEMP1       SET OLD VALUES OF SAVED BITS
000535L 01110011 11110001
000536L 00110111 10001100
                                                XIF
                                        .                                   MAY HAPPEN IF STACK IN PROTECTED MEMORY
                                                TSTIT   ,SWALBT             WHICH WAY TO GO?
000537L 01000101 10000000
                                                BRA     BETAL,FZ            TO BETA
000540L 11010010 11000110
                                        .       BRA     ALPHAL              TO ALPHA
                                        *
000541L                                 ALPHAL
                                        .       (111 030)  ALPHAL           LOAD REGISTERS FROM ALPHA SAVE AREA
                                        . 15.50~15.90 (HERE ON)             FXLHEDCBA <- 'FXLHEDCBA'
                                                DOTIP   ,ND,0200,SPIL       GET IT ON 128 BYTE BOUNDARY
000541L 00110001 11011011
000542L 01010101 10000000
                                                DOPI    MAROL,OR,SESAVAF.AND.0177 ONLY 7 BITS OF INTEREST
000543L 01010011 00111110
000544L 00110111 11000000
                                                LDX     SP2MRH,SMR
000545L 00110001 11101010
000546L 00110111 01000111
                                                DOTIP   ,ND,-1-SWRPT-SWALBT,PSWI RESET REPEAT FLAG AND SET ALPHA
000547L 00110001 11011100
000550L 01010101 01011111
                                        .       BRA     MODLOD
                                        *
000551L                                 MODLOD
                                        .                                   LOAD USERS FLAGS AND REGISTERS
                                        . NOTE: IF MACRO LEVEL PLAYS WITH FLAG BYTE, IT BETTER DO IT CORRECTLY

                                                LDPT    PSW0                LOAD STATUS WORD
000551L 00110111 10001100
000552L 00010111 10110010               CCLR
                                                MWAIT   ,MEMPF0
000553L 11010100 10010100
000554L 11010111 00000101
                                                DOTPP   ,AC,MDR,MDR         SET USER FLAGS
000555L 00110001 00110110
000556L 00110010 00110110
                                                STB     DMAR,SMR            POSITION CORRECTLY
000557L 00110111 00001101
000560L 00110111 01000111
                                                STB     LUF
000561L 00110111 00000110
                                                BRA     MODLOP              AND DO THE REGISTER LOAD
000562L 11011111 01100011
```

. REGISTER SAVE AND RESTORE

```
637.
638.  000563L                          *
                                       REGS:
639.                                   . ??.??       055)  REGS            REGISTER SAVE
640.                                   .                                   (SP-7 | SP) <- XLHEDCBA; SP <- SP - 8
641.
642.                                   .       (111 055)  REGL            REGISTER LOAD
643.                                   . 13.70~14.10                       XLHEDCBA <- (HL-7 | HL)
644.
645.  000563L 11011000 01100110              BRA     REGL,F@,IZ        DO REGISTER LOAD NOT SAVE!
646.  000564L 00110001 11011100              DOPIP   MODW,ND,-1-SWUSER,PSWI  ALLOW STACK ACCESS TO PROTECTED MEM.
      000565L 01010101 11111011
      000566L 00110111 00000100
647.  000567L 00110001 11001011              DLDX    SP2MR,,SMR        GET TOP ENTRY ON THE STACK
      000570L 00110001 11101010
      000571L 00110111 01000111
648.  000572L 11001110 11111111              MWAIT   NOOP,MEMPF0
      000573L 11010100 10000100
      000574L 11010111 00000101
649.  000575L 00110001 00110110              LDRP    TEMPL,MDR,CC      SAVE LSB OF POINTER
      000576L 01101111 10110010
650.  000577L 01010100 00001000              DOPI    MDW,SB,8          UPDATE TOS (ASSUMING REGS WORKS)
      000600L 00110111 00100001
651.  000601L 11001110 11111111              MWAIT   NOOP,MEMPF0
      000602L 11010100 01111101
      000603L 11010111 00000101
652.  000604L 00110111 00001100              STB     IMAR,SMR          GET MSB OF TOS
      000605L 00110111 01000111
653.  000606L 11001110 11111111              MWAIT   NOOP,MEMPF0
      000607L 11010100 01111000
      000610L 11010111 00000101
654.  000611L 00110001 00110110              LDRP    TEMPH,MDR         SAVE MSB OF POINTER
      000612L 01101111 11110001
655.  000613L 01010100 00000000              DOPI    MDW,SB,0          UPDATE TOS (ASSUMING REGS WORKS)
      000614L 00110111 00100001
656.  000615L 01110001 11110010              LDTR    TEMPL             GET ORIGINAL (SAVED) LSB
657.  000616L 11010100 01110001              MWAIT   ,MEMPF0
      000617L 11010111 00000101
658.  000620L 00110111 11000000              LDPT    MAROL             LOAD THE MAR WITH THE INITIAL TOS
659.  000621L 01110001 11110001              LDPR    MAROH,TEMPH,IMAR  AND CORRECT FOR THE FIRST DMAR
      000622L 00110111 11100000
      000623L 00110111 00001100
660.  000624L 00110001 11011100              LDPP    MODW,PSWI         RESTORE THE CORRECT MODE
      000625L 00110111 00000100
661.  000626L 11011111 11011011              BRA     REGSVLP           AND GO SAVE ALL THE REGS
662. >000627L 01011001 11111111  FTCHABW     BRAX    FETCHW            (SO AS LITTLE CHANGES AS POSSIBLE)
     >000630L 11001111 11111111
```

. REGISTER SAVE AND RESTORE

```
663.                                    +
664.  000631L                          REGL
665.                                    .       (111 055)  REGL          REGISTER LOAD
666.                                    . 13.70~14.10                    XLHEDCBA <- (HL-7 | HL)
667.
668.  000631L 00110001 11000110               DLDX     HL2MR,,SMR       INIT HL TO MAR AND GET FIRST REG (X)
      000632L 00110001 11100101
      000633L 00110111 01000111
669.  000634L 01010001 00010000   MODLOP      LDPI     LIMP,IMP8        INIT COUNTER
      000635L 00110111 00000001
670.  000636L 00110111 00001001   REGLLP      STB      DIMP             COUNT DOWN
671.  000637L 11010100 01100000               MWAIT    ,MEMPF0
      000640L 11010111 00000101
672.  000641L 00110001 00110110               LDTP     MDR              GET DATA AND START NEXT READ FAST!
673.  000642L 00110111 00001101               STB      DMAR,SMR
      000643L 00110111 01000111
674.  000644L 00110111 10001111               LDPT     IMP0             SAVE THE DATA IN ITS REGISTER
675.  000645L 11011000 01100001               BRA      REGLLP,F@,IZ     LOOP FOR THE FULL COUNT
676. >000646L 01011001 11111111               BRAX     FETCHRW          RESTORE CORRECT MODE (FOR SYSRET)
     >000647L 11001111 11111111
```

```
                        . SECTOR TABLE LOAD
679.                    *
680.  000650L             STL:
681.                    .       (    077)  STL              LOAD THE SECTOR TABLE
682.                    . 5.45~5.25 + C * 2.50~2.70 (+0.55~0.35 IF C>8, OR 1.50 IF C=0)
683.                    .                                   STL (0..C) <- (HL+C ! HL); STL (15) <- SYS
684.
685.                    .       (022 077)  STLOA            LOAD WITH OFFSET
686.                    .       (111 077)  STLOB            STL (R..R+C) <- (HL+C ! HL)
687.                    .       (062 077)  STLOC            STL(15) <- SYSROM
688.                    .       (113 077)  STLOD
689.                    .       (174 077)  STLOE
690.                    . 5.80~5.60 + C * 2.5~2.70 (+0.55~0.35 IF C>8, OR 1.50 IF C=0)
691.
692.                    .       NOTE: DOES NOT CHANGE HL OR C-REGISTERS
693.                    .       NOTE: IN STLO'C', LOW 4 BITS COUNTER & HIGH 4 BITS OFFSET!
694.
695.  000650L 00110001 11011100          TSTIP   ,SWUSER,PSWI      ONLY IF PRIVED
       000651L 01000101 00000100
696.  000652L 11000010 01001001          BRA     IVIOL$,FZ
697.  000653L 01010101 00100000          TSTIT   ND,SWRPT,,,IW     ASSUME WILL BE ZERO, NOT REPEATED
698.  000654L 11010011 01001001          BRA     STLNRPT,TZ        WAS NOT REPEATED
699.
700.  000655L 00110001 11010010          DORIP   TEMP2,ND,07,URI+URC REPEATED, GET THE HL (MAR) BIAS AND
       000656L 01010101 00000111
       000657L 01101111 11110010
701.                                    RPT     4
702.  000660L 00010111 10100010          SHIFT   SL                THE POINTER BIAS AND COUNT FOR THE
702.  000661L 00010111 10100010          SHIFT   SL                THE POINTER BIAS AND COUNT FOR THE
702.  000662L 00010111 10100010          SHIFT   SL                THE POINTER BIAS AND COUNT FOR THE
702.  000663L 00010111 10100010          SHIFT   SL                THE POINTER BIAS AND COUNT FOR THE
703.  000664L 01010011 00001000          DOTI    ,OR,010           FINAL EIGHT STL LOADS
704.  000665L 11011111 01000101          BRA     STLRPTD
705.
706.  000666L 01101111 11110010  STLNRPT LDRT    TEMP2             REGULAR HL (MAR) NEEDS NO BIAS
707.  000667L 00110001 11010010          TSTIP   ,017,URI+URC,TW   GET THE COUNT OF THE STEPS TO DO
       000670L 01010101 00001111
708.  000671L 11010011 00000111          BRA     FTCHIAB,TZ        IF ZERO, WAS NOTHING TO DO. SO, THE END
709.
710.  000672L 11011001 01000000  STLRPTD BRA     STLZRO,T@,IZ      DO STANDARD STL
711.  000673L 01101111 11110001          LDRT    TEMP1             SAVE AWAY
712.  000674L 00110001 11011111          DOTIP   ,ND,0360,IMP1     IMP STL STARTS STL WITH OFFSET
       000675L 01010101 11110000
713.  000676L 01110010 00110001          DOTR    ,AC,TEMP1,,C0     COMBINE GIVEN OFFSET WITH BIAS
714.
715.  000677L 01101111 11110001  STLZRO  LDRT    TEMP1             SAVE THE POINTER/COUNTER AS GENERATED
716.  000700L 00110001 11010110          DOPRP   MAROL,AC,TEMP2,URI+URL,C0 BIAS TABLE ADDRESS (IF NEEDED)
       000701L 01110010 00110010
       000702L 00110111 11000000
717.  000703L 00110001 11010101          LDRP    TEMP2,URI+URH     SAVE AWAY URH SO CAN BE RESTORED
       000704L 01101111 11110010
718.  000705L 00110110 11100000          DOP     MAROH,IT
719.  000706L 00110111 01000111          STB     SMR               GET NEXT (FIRST) TABLE ENTRY
```

```
                        . SECTOR TABLE LOAD

720.  000707L 00110111 10000101          LDPT    URO+URH          IN CASE TABLE CROSSES PAGE BOUNDARY
721.
722.  000710L 01110001 11110001  STLAGN   LDTR    TEMP1            GET THE INITIAL VIRTUAL ADDRESS
723.
724.  000711L 11010100 00110110  STLOOP   MWAIT   ,STLDONE         RESTORE REGS & SET VECTOR FIRST
      000712L 11010111 00011111
725.  000713L 00110111 11100000          LDPT    MAR0H            LOAD VIRTUAL ADDRESS FROM TEMP
726.  000714L 01010001 00000010          LDPI    MODW,SWBASD      DISABLE BASING (AND 1 MS INTERRUPTS)
      000715L 00110111 00000100
727.  000716L 00110001 00110110          DOPIP   STW,ND,0375,MDR  SET PHYSICAL SECTOR # IN VIRTUAL LOCN.
      000717L 01010101 11111101
      000720L 00110111 00000101
728.  000721L 00110001 11011100          LDPP    MODW,PSWI        RESTORE BASING (1 MS INT. 1 INST. DELAY
      000722L 00110111 00000100
729.  000723L 00110001 11100101          LDX     HL2MRH           RESTORE MARH FROM H SAVE AREA
730.  000724L 00110111 00001100          STB     IMAR,SMR         GET NEXT TABLE ENTRY
      000725L 00110111 01000111
731.  000726L 00110001 10100101          LDX     MR2HLH           SAVE MARH IN H
732.  000727L 01110001 10110001          DORIR   TEMP1,AC,017,TEMP1,CC INC VIRTUAL SECTOR # & DECR COUNT
      000730L 01010010 00001111
      000731L 01101111 11110001
733.  000732L 01000101 00000111          TSTIT   ,07              AT SPLIT POINT?
734.  000733L 11010010 00110110          BRA     STLOOP,FZ        NO, CONTINUE
735.                                     .                        LOOPING JUMP IS DURING MEMORY READ
736.                                     .                        THIS MAKES EXEC FASTER.
737.  000734L 01000101 00001111          TSTIT   ,017             REALLY FINISHED?
738.  000735L 11010011 00011111          BRA     STLDONE,TZ       YES, CLEANUP AND END
739.  000736L 00110001 00110000          TSTPT   FI,SRVREQ        NO, ANY SERVICE TO DO?
740.  000737L 11010011 00110111          BRA     STLAGN,TZ        NO, THEN DO SECOND HALF NOW
741.                                     .                        REPEATED! WILL DO SERVICE BEFORE SECOND
742.                                     .                        PART BUT DO CLEANUP FIRST
743.  000740L 11010100 00011111  STLDONE  MWAIT   ,$+1             RESTORE BEFORE MEMPF
      000741L 11010111 00011101
744.                                     .                        BUT NOTE: MAR MSB WILL BECOME INCORRECT
745.  000742L 01110001 11110010          LDPR    URO+URH,TEMP2    RESTORE H-REG
      000743L 00110111 10000101
746.  000744L 01010001 11110000          LDPI    MAR0H,SYSROM>8.AND.0360 !! FORCE LAST ENTRY TO
      000745L 00110111 11100000
747.  000746L 00110111 00000101          LDPT    STW              ACCESS PROTECT AND WRITE PROTECT
748.  000747L 01011001 11111101          BPGX    RIND
749.  000750L 01110001 11110001          TSTIR   ,017,TEMP1       REALLY FINISHED?
      000751L 01000101 00001111
750.  000752L 11000011 01110010          BRA     RIND,TZ          YES, RESET REPEAT FLAG
751. >000753L 01011001 11111111          BRAX    SRVRPT           NO, DO IT AS REPEATED INST.
     >000754L 11001111 11111111
752.                                     .                        (BOTH RIND & SRVRPT INDIRECT TO MEMPF)
```

. SYSTAT INSTRUCTION (157 OP-CODE)

```
755.
756.  000755L                          *
757.                                   SYSTAT:
758.                                   .        (    157)  UDOP            UNDEFINED OP-CODE
759.                                   . 9.20~9.40
760.                                   . 1.30   (111 157)  SYSTAT1          PROCESSOR STATUS WORD
761.                                   .                                    C<- 0; B <- PSW
762.                                   . 1.70   (062 157)  SYSTAT2          SELECTABLE NODE I.D.
763.                                   .                                    C<- 0; B <- SNID
764.                                   . 1.70   (113 157)  SYSTAT3          SYSTEM STATUS (UNUSED - 0)
765.                                   . 1.70   (174 157)  SYSTAT4          C <- 0; B <- 0
766.                                   . 1.70   (115 157)  SYSTAT5
767.                                   . 1.70   (176 157)  SYSTAT6          (IF PRE-RELEASE, C <- PRE-RELEASE CODE)
768.                                   . 1.70   (117 157)  SYSTAT7          (SO CAN TELL PRE-RELEASE LEVEL)
769.                                   . 1.70   (022 157)  SYSTAT8
770.  000755L 11001001 01000111                BRA     UDOP,T@,IZ        157 ALONE IS UNDEFINED
771.  000756L 00110111 00001001                STB     DIMP              CHECK 111
772.  000757L 01010001 01001001                LDPI    URO+URC,PRE       WHATEVER ELSE, C=PRE-RELEASE LEVEL
      000760L 00110111 10000010
773.  000761L 00110001 11011100                LDTP    PSWI              (ASSUME 1)
774.  000762L 11011001 00001000                BRA     SYSTND,T@,IZ
775.  000763L 00110111 00001001                STB     DIMP              CHECK 062
776.  000764L 00110001 01010001                LDTP    SNID
777.  000765L 11011001 00001000                BRA     SYSTND,T@,IZ
778.  000766L 01010001 00000000                TCLR                      WILL BE 113 - 022
779.  000767L 00110111 10000001  SYSTND  LDPT  URO+URB
780. >000770L 01011001 11111111  FTCHIAB BRAX  FETCHI                    (FINISHED ALPHA/BETA THAT DID NOTHING)
     >000771L 11001111 11111111
781.                                   *
782. >000772L 01011001 11111111  MEMPF0 BRAX  MEMPFS
     >000773L 11001111 11111111
783.  000774L 11111111 11111111          TABPAGE PROCL
      000775L 11111111 11111111
      000776L 11111111 11111111
      000777L 11111111 11111111
```

```
                                . BLOCK TRANSFER AND CONVERT
786.                            *
787.  001000L                   BT:
788.                            .       (    021)  BT                BLOCK TRANSFER
789.                            . -0.30 + N * 5.55 - N * 0.15 / ODDSTEP + 0.10 WHEN TCFZ / STEP - 0.50 IF MATCH
790.                            .                                    (DE) <- T <- A + (HL)
791.                            .                                    DE <- DE + 1; HL <- HL + 1
792.                            .                                    STOP IF T = -B; C <- C - 1; UNTIL = 0
793.
794.                            .       (111 021)  BTR               BLOCK TRANSFER REVERSE
795.                            . -0.30 + N * 5.75 - N * 0.15 / ODDSTEP + 0.10 WHEN TCFZ / STEP - 0.50 IF MATCH
796.                            .                                    (DE) <- T <- A + (HL)
797.                            .                                    DE <- DE - 1; HL <- HL - 1
798.                            .                                    STOP IF T = -B; C <- C - 1; UNTIL = 0
799.
800.                            .       (062 021)  BCV               BLOCK CONVERT
801.                            . -0.30 + N * 7.35 - N * 0.15 / ODDSTEP + 0.10 WHEN TCFZ / STEP - 0.50 IF MATCH
802.                            .                                    (DE) <- T <- A <- (HL + (DE))
803.                            .                                    DE <- DE + 1
804.                            .                                    STOP IF T = -B; C <- C - 1; UNTIL = 0
805.
806.                            .       NOTE:  NONE OF THESE CHANGE THE CONDITION FLAGS
807.
808.  001000L 11001001 11101110          BRA     BTX,T@,IZ           BT (021)
809.  001001L 11001011 11010110          BRA     BTR,T@,IO           BTR (111 021)
810.  001002L 00110001 11000100          DLDX    DE2MR,,SMR          BCV (062 021)
      001003L 00110001 11100011
      001004L 00110111 01000111
811.  001005L 00010111 10110010          CCLR
812.  001006L 00110001 11010110          LDTP    URI+URL             ADD DATA AT DE TO TABLE POINTER IN HL
813.  001007L 11000100 11111000          MWAIT   ,MEMPF1
      001010L 11010111 00001001
814.  001011L 00110010 00110110          DOPP    MAROL,AC,MDR        A <- MAR <- L + (DE)
      001012L 00110111 11000000
815.  001013L 00110111 10000000          LDPT    URO+URA             STORE IN A SO CAN FIND STOP POINT
816.  001014L 00110001 11010101          LDTP    URI+URH             ADD IN CARRY ALSO
817.  001015L 00110110 11100000          DOP     MAROH,IT
818.  001016L 00110111 01000111          STB     SMR                 INDIRECT THROUGH THIS FOR TABLE ENTRY
819.  001017L 01010001 00000000          TCLR                        NO A-REG OFFSETS
820.  001020L 11001111 11100101          BRA     BTCVT
821.                            *
822.  001021L 00110001 11000110  BTX     DLDX    HL2MR,,SMR          GET DATA AT HL TO BE MOVED
      001022L 00110001 11100101
      001023L 00110111 01000111
823.  001024L 00110001 10010000          DADDP   URO+UR,MARI         INCREMENT HL FOR BT
      001025L 00010110 01110010
      001026L 00110111 10000110
      001027L 00110001 10110000
      001030L 00110110 10000101
824.  001031L 00110001 11010000          LDTP    URI+URA
825.  001032L 01101111 11110001  BTCVT   LDRT    TEMP1               SAVE THE A-REG OFFSET (ZERO FOR BCV)
826.  001033L 11000100 11100100          MWAIT   ,MEMPF1
      001034L 11010111 00001001
```

```
827.  001035L 00110001 11000100          DLDX    DE2MR              POINT TO WHERE TO STORE RESULT
      001036L 00110001 11100011
828.  001037L 00110001 00110110          DOPRP   MDW,AC,TEMP1,MDR,C0 STORE DATA IN (DE) AND IN TEMP1
      001040L 01110010 00110001
      001041L 00110111 00100001
829.  001042L 01101111 11110001          LDRT    TEMP1
830.  001043L 00110001 10010000          DADDP   UR0+UDE,MARI       INCREMENT DE FOR BT & BCV
      001044L 00010110 01110010
      001045L 00110111 10000100
      001046L 00110001 10110000
      001047L 00110110 10000011
831.  001050L 11001111 10111100          BRA     BTEND
832.                                     *
833.  001051L 00110001 11000110  BTR     DLDX    HL2MR,,SMR         GET DATA AT HL TO BE MOVED
      001052L 00110001 11100101
      001053L 00110111 01000111
834.  001054L 00010111 10110010          CCLR
835.  001055L 00110001 10010000          DDECP   UR0+UR,MARI        DECREMENT HL FOR BTR
      001056L 01010100 00000001
      001057L 00110111 10000110
      001060L 00110001 10110000
      001061L 01010100 00000000
      001062L 00110111 10000101
836.  001063L 00110001 11010000          LDRP    TEMP1,URI+URA      LOAD UP THE A-REG OFFSET
      001064L 01101111 11110001
837.  001065L 11000100 11001010          MWAIT   ,MEMPF1
      001066L 11010111 00001001
838.  001067L 00110001 11000100          DLDX    DE2MR
      001070L 00110001 11100011
839.  001071L 00110001 00110110          DOPRP   MDW,AC,TEMP1,MDR,C0 GET RESULTANT DATA
      001072L 01110010 00110001
      001073L 00110111 00100001
840.  001074L 01101111 10110001          LDRT    TEMP1,,CC          STORE DATA IN (DE)
841.  001075L 00110001 10010000          DDECP   UR0+UDE,MARI       BACKUP DE FOR BTR
      001076L 01010100 00000001
      001077L 00110111 10000100
      001100L 00110001 10110000
      001101L 01010100 00000000
      001102L 00110111 10000011
842.                                     *
843.                                     . BT - 3.50, BTR - 3.70, BCV - 5.30~5.50
844.
845.  001103L 00110001 11010001  BTEND    TSTRP   AC,TEMP1,URI+URB,C0 AT THE ENDPOINT?
      001104L 01110010 00000001
846.  001105L 11000000 10110111          BRA     RIN256,FC          NO, WANT CARRY TRUE & ZERO TRUE
847.  001106L 11000011 01110010          BRA     RIND,TZ            YES, END NOW!
848.                                     .       BRA     RIN256     NO!
849.                                     .                          NO, REPEAT 256 TIMES (OR LESS)
850.  001107L 00010111 10110010          CCLR                       ONLY CARRY SET RIN256 CASE
```

```
                                        *
001110L                                 RIN256:
                                        . ODD - 1.45, RPT - 1.60, SRV - 1.35, END - 1.30
                                        .       WARNING, CARRY MUST BE CLEAR ON ENTRY
                                        .       BLOCK REPEATED INSTRUCTIONS (THOSE THAT COUNT C THROUGH 256 MAX STEPS
                                        .       DOES NOT CHANGE FLAGS
001110L 00110001 11010010                       DOPIP   URO+URC,SB,1,URI+URC IF ZERO, FINISHED
001111L 01010100 00000001
001112L 00110111 10000010
001113L 11000011 01110010                       BRA     RIND,TZ
001114L 01000101 00000001                       TSTIT   ,1                  DO THEM IN PAIRS SO CAN'T INTERRUPT
001115L 11000010 10101111                       BRA     RINDO,FZ            DURING DOUBLE BYTE MOVE
                                        .                                   !CAN USE BT IN DISPLAY POINTER MOVES!
                                        *
001116L                                 RINST:
                                        . SRV - 0.65, RPT - 0.90
                                        .       LOOP THROUGH REPEATED INSTRUCTIONS, SET THE REPEAT MODE AND DO
                                        .       SERVICE REQUEST IF NEEDED ELSE RE-EXECUTE THE INSTRUCTION.
001116L 00110001 00110000                       TSTPT   FI,SRVREQ           DO SERVICE IF NEEDED
001117L 11000010 10101011                       BRA     RINRPT,FZ
001120L 11000100 10101111       RINDO   MWAIT   ,MEMPF1
001121L 11010111 00001001
001122L 00111001 00110100                       BRPX    IDCOD               GO DO OPCODE AGAIN
001123L 10101111 00110011
                                        *
>001124L 01011001 11111111      RINRPT  BRAX    SRVRPT              YES, DO IT!
>001125L 11001111 11111111
```

```
                                . BLOCK COMPARE
881.                            *
882.  001126L                   BCP:
883.                            .       (    041)  BCP              BLOCK COMPARE
884.                            . -0.30 + N * 5.45 - 0.15 * N / ODDSTEP - 0.5 IF MATCH
885.                            .                                   (HL) - (DE); HL <- HL + 1; DE <- DE + 1
886.                            .                                   STOP IF TZ; C <- C - 1; CONTINUE UNTIL = 0
887.
888.                            .       (111 041)  DFAC             DECIMAL FIELD ADD
889.                            . -0.30 + C * 7.45                  (DE) <- B .OR. (DE) .DAD. (HL) + CRY
890.                            .                                   DE <- DE - 1; HL <- HL - 1
891.                            .                                   C <- C - 1; UNTIL = 0 (16)
892.
893.                            .       (062 041)  DFSB             DECIMAL FIELD SUBTRACT
894.                            . -0.30 + C * 7.65                  (DE) <- B .OR. (DE) .DSB. (HL) - CRY
895.                            .                                   DE <- DE - 1; HL <- HL - 1
896.                            .                                   C <- C - 1; UNTIL = 0 (16)
897.
898.  001126L 1100.1000 1000.1101          BRA     DFOP,F@,IZ      GO TO DECIMAL STUFF
899.  001127L 00110001 11000100           DLDX    DE2MR,,SMR
      001130L 00110001 1.1.00011
      001131L 00110111 01000111
900.  001132L 00110001 10010000           DADDP   URO+UDE,MARI    GET DATA AND UPDATE DE
      001133L 00010110 0.1110010
      001134L 00110111 10000100
      001135L 00110001 10110000
      001136L 00110110 100.00011
901.  001137L 11000100 10100000           MWAIT   ,MEMPF1
      001140L 11010111 00001001
902.  001141L 00110001 00110110           LDRP    TEMP1,MDR
      001142L 01101111 11110001
903.  001143L 00110001 11000110           DLDX    HL2MR,,SMR      GET DATA AND UPDATE HL
      001144L 00110001 1110010.1
      001145L 00110111 01000111
904.  001146L 00110001 10010000           DADDP   URO+UR,MARI
      001147L 00010110 01110010
      001150L 00110.111 .10000110
      001151L 00110001 10110000
      001152L 00110.110 10000101
905.  001153L 01110001 10110001           LDTR    TEMP1,CC        GET DE DATA
906.  001154L 11000100 10010011           MWAIT   ,MEMPF1
      001155L 11010111 .00001001
907.  001156L 00110100 00110110           DOPP    LUF,SB,MDR      SUBTRACT HL DATA AND SET COMPARE FLAGS
      001157L 00110111 .00000110
908.  001160L 11000011 10110.111          BRA     RIN256,TZ       CONTINUE IF A MATCH (CARRY ZERO TOO!)
909.  001161L 11001111 0.1110010          BRA     RIND            END IF DATA DIFFERS
```

```
912.                                    *
913.  001162L                          DFOP
914.                                    .        (111 041)  DFAC          DECIMAL FIELD ADD
915.                                    . -0.30 + C * 7.45                (DE) <- B .OR. (DE) .DAD. (HL) + CRY
916.                                    .                                 DE <- DE - 1; HL <- HL - 1
917.                                    .                                 C <- C - 1; UNTIL = 0 (16)
918.
919.                                    .        (062 041)  DFSB          DECIMAL FIELD SUBTRACT
920.                                    . -0.30 + C * 7.65                (DE) <- B .OR. (DE) .DSB. (HL) - CRY
921.                                    .                                 DE <- DE - 1; HL <- HL - 1
922.                                    .                                 C <- C - 1; UNTIL = 0 (16)
923.
924.  001162L 01010001 00001111                LDRI    TEMP2,017         SELECT 4 BITS, NOT ALL OF THEM
      001163L 01101111 11110010
925.  001164L 01010001 10000000                BAL     ,DFADD            (ASSUME THIS)
926.  001165L 11001011 01100110                BRA     BFOP,T@,IO        WAS ODD THEREFORE WAS DECIMAL ADD
927.  001166L 01010001 10000111                BAL     ,DFSUB
928.  001167L 11001111 01100110                BRA     BFOP              WAS EVEN SO IT WAS DECIMAL SUBTRACT
929.
930.  001170L                          DFSUB
931.  001170L 01110100 11110001                DOPR    LUF,SB,TEMP1      SET FLAGS ON SUBTRACT
      001171L 00110111 00000110
932.  001172L 11000000 10000011                BRA     DFSEND,FC         NO CARRY, NO PROBLEMS
933.  001173L 01010010 00001001                DOTI    ,AC,10-1          CARRY, CORRECT THE VALUE (ADDS 10!)
934.  001174L 00110011 11010001       DFSEND   DOPP    MDW,OR,URI+URB    SET THE ZONE BITS
      001175L 00110111 00100001
935.  001176L 11001111 01111000                BRA     RIN16
936.
937.  001177L                          DFADD
938.  001177L 01110010 11110001                DORR    TEMP1,AC,TEMP1    ADD TOGETHER (CARRY FALSE ON RESULT)
      001200L 01101111 11110001
939.  001201L 01010010 11110110                DOPI    LUF,AC,-10        SET FLAGS & CORRECT IF OVERFLOW
      001202L 00110111 00000110
940.  001203L 11000001 01111010                BRA     DFAEND,TC         IF OVERFLOWED, CORRECTED NOW
941.  001204L 01110001 11110001                LDTR    TEMP1             NO CARRY, GET CORRECT VALUE
942.  001205L 00110011 11010001       DFAEND   DOPP    MDW,OR,URI+URB    SET THE ZONE BITS
      001206L 00110111 00100001
943.                                    .        BRA     RIN16
```

```
946.                                    *
947.  001207L                          RIN16:
948.                                    . RPT - 1.70, SRV - 1.45, END - 1.40
949.
950.                                    .       FIELD REPEATED INSTRUCTIONS ARE THOSE THAT COUNT C THROUGH 16 MAX STEP
951.
952.  001207L 00010111 10110010                CCLR
953.  001210L 00110001 11010010                DOPIP   URO+URC,SB,1,URI+URC COUNT DOWN
      001211L 01010100 00000001
      001212L 00110111 10000010
954.  001213L 01000101 00001111                TSTIT   ,017                AT THE END (BASE 16)?
955.  001214L 11000010 10110001                BRA     RINST,FZ            NOT YET
956.                                    *
957.  001215L                          RIND:
958.                                    . 0.70                              REPEATED INSTRUCTION END
959.
960.  001215L 00110001 11011100                DOPIP   PSWO,ND,-1-SWRPT,PSWI
      001216L 01010101 11011111
      001217L 00110111 10001100
961. >001220L 01011001 11111111                BRAX    FETCHW
     >001221L 11001111 11111111
```

```
964.                                    *
965.  001222L                           BFSB:
966.                                    .         (    031)  BFSB          BINARY FIELD SUBTRACT
967.                                    . -0.30 + C * 6.90                  (DE) <- (DE) - (HL) - CRY
968.                                    .                                   DE <- DE - 1; HL <- HL - 1
969.                                    .                                   C <- C - 1; UNTIL = 0 (16)
970.
971.  001222L 01010001 11111111                LDRI    TEMP2,0377          SELECT ALL THE BITS
      001223L 01101111 11110010
972.  001224L 01010001 01000011                BRC     BFOP,,BFSUB
      001225L 11001111 01100110
973.                                    *
974.  001226L                           BFAC:
975.                                    .         (    011)  BFAC          BINARY FIELD ADD
976.                                    . -0.30 + C * 6.70                  (DE) <- (DE) + (HL) + CRY
977.                                    .                                   DE <- DE - 1; HL <- HL - 1
978.                                    .                                   C <- C - 1; UNTIL = 0 (16)
979.
980.  001226L 01010001 11111111                LDRI    TEMP2,0377          SELECT ALL THE BITS
      001227L 01101111 11110010
981.  001230L 01010001 01000111                BAL     ,BFADD
982.                                    *
983.  001231L                           BFOP
984.                                    . 4.1                               BINARY FIELD OPERATIONS (ARG GETTER)
985.
986.  001231L 01101111 10110000                BAS     LINK,CC
987.  001232L 00110001 11000110                DLDX    HL2MR,,SMR
      001233L 00110001 11100101
      001234L 00110111 01000111
988.  001235L 00110001 10010000                DDECP   URO+UR,MARI         GET (HL) DATA AND UPDATE HL
      001236L 01010100 00000001
      001237L 00110111 10000110
      001240L 00110001 10110000
      001241L 01010100 00000000
      001242L 00110111 10000101
989.  001243L 01110001 11110010                LDTR    TEMP2
990.  001244L 11000100 01011011                MWAIT   ,MEMPF1
      001245L 11010111 00001001
991.  001246L 00110101 00110110                DORP    TEMP1,ND,MDR,,CC    PUT IT IN TEMP1
      001247L 01101111 10110001
992.  001250L 00110001 11000100                DLDX    DE2MR,,SMR
      001251L 00110001 11100011
      001252L 00110111 01000111
993.  001253L 00110001 10010000                DDECP   URO+UDE,MARI        GET (DE) DATA AND UPDATE DE
      001254L 01010100 00000001
      001255L 00110111 10000100
      001256L 00110001 10110000
      001257L 01010100 00000000
      001260L 00110111 10000011
994.                                                                        CARRY IGNORED, BITS 2&6 NOT BOTH HIGH
995.  001261L 00110001 00110101                DOTPP   ,AC,UCFLG,UCFLG     SET THE CARRY
      001262L 00110010 00110101
```

```
  996.  001263L 01110001 11110010          LDTR    TEMP2
  997.  001264L 11000100 01001011          MWAIT   .MEMPF1
        001265L 11010111 00001001
  998.  001266L 00110101 00110110          DOTP    .ND,MDR
  999.  001267L 11101111 00000000          BRR     LINK            SELECT ADD & SUBTRACT, BINARY & DECIMAL
 1000.                                    *
 1001.  001270L 01110010 11110001  BFADD   DOPR    MDW,AC,TEMP1    (DE) <- (DE) + (HL)
        001271L 00110111 00100001
 1002.  001272L 00110111 00000110          LDPT    LUF
 1003.  001273L 11001111 01111000          BRA     RIN16
 1004.
 1005.  001274L 01110100 11110001  BFSUB   DOPR    MDW,SB,TEMP1    (DE) <- (DE) - (HL)
        001275L 00110111 00100001
 1006.  001276L 00110111 00000110          LDPT    LUF
 1007.  001277L 11001111 01111000          BRA     RIN16
```

```
                                . BINARY FIELD SHIFTS LEFT AND RIGHT

 1010.                          *
 1011.  001300L                 BFS:
 1012.                          .       (    075)  BFSL          BINARY FIELD SHIFT LEFT
 1013.                          . -0.30 + C * 4.55                (HL) <- (HL) + (HL) + CRY; HL <- HL - 1
 1014.                          .                                 C <- C - 1; UNTIL = 0 (16)
 1015.
 1016.                          .       (111 075)  BFSR          BINARY FIELD SHIFT RIGHT
 1017.                          . -0.30 + C * 4.55                (HL) <- SHFTRGHT (HL); HL <- HL + 1
 1018.                          .                                 C <- C - 1; UNTIL = 0 (16)
 1019.
 1020.                          .       NOTE: ONLY CHANGES THE CARRY FLAG
 1021.
 1022.  001300L 00110001 11000110          DLDX    HL2MR,,SMR    GET DATA TO SHIFT & SELECT R/L ROUTINE
        001301L 00110001 11100101
        001302L 00110111 01000111
 1023.  001303L 11001001 00101001          BRA     BFSL,T@,IZ
 1024.                          . BFSR
 1025.  001304L 00110001 10010000          DADDP   URO+UR,MARI   UPDATE HL
        001305L 00010110 01110010
        001306L 00110111 10000110
        001307L 00110001 10110000
        001310L 00110110 10000101
 1026.  001311L 00110001 00110101          LDTP    UCFLG
 1027.  001312L 00010111 10100010          SHIFT   SL            PUT THE CARRY IN THE LSB (BIT 0)
 1028.  001313L 00010111 10110010          CCLR                  AND INTO THE LINK
 1029.  001314L 11000100 00110011          MWAIT   ,MEMPF1
        001315L 11010111 00001001
 1030.  001316L 00110001 00110110          LDTP    MDR           GET THE DATA
 1031.  001317L 00010111 10010010          SHIFT   SR            DO EXTENDED SHIFT
 1032.  001320L 00110111 00100001          LDPT    MDW           OUTPUT SHIFTED DATA
 1033.  001321L 00010111 10010010          SHIFT   SR            PUT LINK IN THE MSB
 1034.  001322L 01101111 11110001          LDRT    TEMP1
 1035.  001323L 01110010 00110001          DOPR    LUCF,AC,TEMP1,,CO SET THE CARRY FROM THE MSB (LINK)
        001324L 00110111 00000111
 1036.  001325L 11001111 01111000          BRA     RIN16
 1037.
 1038.  001326L 00010111 10110010  BFSL    CCLR                  UPDATE HL
 1039.  001327L 00110001 10010000          DDECP   URO+UR,MARI   CARRY IN STOPPED IN BIT 2 OR 6 OF UCFLG
        001330L 01010100 00000001
        001331L 00110111 10000110
        001332L 00110001 10110000
        001333L 01010100 00000000
        001334L 00110111 10000101
 1040.  001335L 00110001 00110101          DOTPP   ,AC,UCFLG,UCFLG SET CARRY FROM USER CARRY
        001336L 00110010 00110101
 1041.  001337L 11000100 00100000          MWAIT   ,MEMPF1
        001340L 11010111 00001001
 1042.  001341L 00110001 00110110          DOPPP   MDW,AC,MDR,MDR SHIFT LEFT!
        001342L 00110010 00110110
        001343L 00110111 00100001
 1043.  001344L 00110111 00000111          LDPT    LUCF          SET CARRY ON RESULT
 1044.  001345L 11001111 01111000          BRA     RIN16
```

. SHIFT OPERATIONS

```
1047.                                   *
1048.  001346L                          SLC:
1049.                                   . 0.95   (    002)  SLC              SHIFT LEFT CIRCULAR
1050.                                   . 0.95   (IMP 002)  SLCR             RN <- R(N-1); CRY <- R0 <- R7
1051.
1052.  001346L 00110001 11011111                  LDRP     TEMP1,IMP1
       001347L 01101111 11110001
1053.  001350L 01110010 00110001                  DOPR     LUCF,AC,TEMP1,,C0 ADD TOGETHER AND SET USER CARRY
       001351L 00110111 00000111
1054.  001352L 00110110 10001111                  DOP      IMP0,IT           PUT CARRY IN THE LSB
1055. >001353L 01011001 11111111                  BRAX     FETCHI            DON'T USE IMPF0, WILL GET BAD CARRY
      >001354L 11001111 11111111
1056.                                   *
1057.  001355L                          SRC:
1058.                                   . 1.15   (    012)  SRC              SHIFT RIGHT CIRCULAR
1059.                                   . 1.15   (IMP 012)  SRCR             CRY <- R7 <- R0; R(N-1) <- RN
1060.
1061.  001355L 00110001 11011111                  LDTP     IMP1
1062.  001356L 00010111 10110010                  CCLR                       SET THE LINK BIT ON LSB
1063.  001357L 00010111 10010010                  SHIFT    SR                RIGHT CIRCULAR
1064.  001360L 00110111 10001111                  LDPT     IMP0              STORE RESULT
1065.  001361L 01101111 11110001                  LDRT     TEMP1
1066.  001362L 01110010 00110001                  DOPR     LUCF,AC,TEMP1,,C0 SET CARRY ON THE MSBIT
       001363L 00110111 00000111
1067. >001364L 01011001 11111111                  BRAX     FETCHI
      >001365L 11001111 11111111
1068.                                   *
1069.  001366L                          SRE:
1070.                                   . 1.50   (    032)  SRE              SHIFT RIGHT EXTENDED
1071.                                   . 1.50   (IMP 032)  SRER             R7 <- CRY; R(N-1) <- RN; CRY <- R0
1072.
1073.  001366L 00110001 00110101                  LDTP     UCFLG             GET CARRY
1074.  001367L 00010111 10100010                  SHIFT    SL                IN LSBIT
1075.  001370L 00010111 10110010                  CCLR                       AND INTO LINK
1076.  001371L 00110001 11011111                  LDTP     IMP1
1077.  001372L 00010111 10010010                  SHIFT    SR                DO RIGHT EXTEND
1078.  001373L 00110111 10001111                  LDPT     IMP0
1079.  001374L 00010111 10010010                  SHIFT    SR                PUT LINK IN MSBIT
1080.  001375L 01101111 11110001                  LDRT     TEMP1
1081.  001376L 01110010 00110001                  DOPR     LUCF,AC,TEMP1,,C0 SET CARRY ON LINK
       001377L 00110111 00000111
1082. >001400L 01011001 11111111                  BRAX     FETCHI
      >001401L 11001111 11111111
```

```
1083.                                   *
1084.                                   .       TABPAGE PRODL
1085.                                   *
1086.  001402L                          CCS:
1087.                                   . 0.70  (    042)  CCS            CONDITION CODE SAVE
1088.                                   . 0.70  (IMP 042)  CCSr           R <- (CRY)(SGN)0000(~ZRO.SGN)(~ZRN.PTY)
1089.
1090.  001402L 00110001 00110101                DOPIP   IMP0,ND,0303,UCFLG
       001403L 01010101 11000011
       001404L 00110111 10001111
1091. >001405L 01011001 11111111                BRAX    FETCHI
      >001406L 11001111 11111111
```

. SINGLE AND DOUBLE PAGED LOAD AND STORE

```
1094.                                   *
1095.  001407L                         PLR:
1096.                                  . 3.90   (    1R4)  PLR.IDX        LOAD REGISTER FROM PAGED LOCATION
1097.                                  .        (    105)  PLR.IDX        A-REG LOAD (104 IS NOT A PLR)
1098.                                  .        (    114)  PLR.IDX        R <- (X,IDX)
1099.                                  .        (    124)  PLR.IDX
1100.                                  .        (    134)  PLR.IDX
1101.                                  .        (    144)  PLR.IDX
1102.                                  .        (    154)  PLR.IDX
1103.                                  .        (    164)  PLR.IDX
1104.
1105.                                  . 5.50   (111 124)  DPL.IDX        C <- (X,IDX); B <- (X,IDX+1)
1106.                                  .        (062 114)  DPLR.IDX       B <- (X,IDX); C <- (X,IDX+1)
1107.                                  .        (113 144)  DPL.IDX        E <- (X,IDX); D <- (X,IDX+1)
1108.                                  .        (174 134)  DPLR.IDX       D <- (X,IDX); E <- (X,IDX+1)
1109.                                  .        (115 164)  DPL.IDX        L <- (X,IDX); H <- (X,IDX+1)
1110.                                  .        (176 154)  DPLR.IDX       H <- (X,IDX); L <- (X,IDX+1)
1111.
1112.  001407L 00110111 00001100                STB      IMAR,SMR         GET THE INDEX
       001410L 00110111 01000111
1113.  001411L 00110001 10001001                DLDX     MR2PC            AND SAVE AWAY NEW PC
       001412L 00110001 10101000
1114.  001413L 11010100 11110100                MWAIT    ,MEMPF1
       001414L 11010111 00001001
1115.  001415L 00110001 00110110                LDPP     MAROL,MDR        LSB ADDRESS
       001416L 00110111 11000000
1116.  001417L 00110001 11100111                LDX      XX2MRH+URX,SMR   MSB ADDRESS AND GET DATA
       001420L 00110111 01000111
1117.  001421L 11001110 11111111                MWAIT    NOOP,MEMPF1
       001422L 11010100 11101101
       001423L 11010111 00001001
1118.  001424L 00110001 00110110                LDPP     I350,MDR         GOT THE DATA
       001425L 00110111 10001101
1119.  001426L 11011001 11100001                BRA      FETPL,T@,IZ      IF IMP NOT ZERO GET ANOTHER BYTE
1120.  001427L 00110111 00001100                STB      IMAR,SMR
       001430L 00110111 01000111
1121.  001431L 11001110 11111111                MWAIT    NOOP,MEMPF1
       001432L 11010100 11100101
       001433L 11010111 00001001
1122.  001434L 00110001 00110110                LDPP     IMPO,MDR         GET THE SECOND DATA BYTE
       001435L 00110111 10001111
1123. >001436L 01011001 11111111      FETPL    BRAX     FETCH
      >001437L 11001111 11111111
```

. SINGLE AND DOUBLE PAGED LOAD AND STORE

```
1124.                                   *
1125.  001440L                         PSR:
1126.                                  . 3.05   (     1R6)  PSR.IDX        STORE REG INTO PAGED LOCATION
1127.                                  .        (     107)  PSR.IDX        A REG SAVE (106 IS NOT A PSR)
1128.                                  .        (     116)  PSR.IDX        (X,IDX) <- R
1129.                                  .        (     126)  PSR.IDX
1130.                                  .        (     136)  PSR.IDX
1131.                                  .        (     146)  PSR.IDX
1132.                                  .        (     156)  PSR.IDX
1133.                                  .        (     166)  PSR.IDX
1134.
1135.                                  . 4.40   (111 126)  DPSR.IDX        (X,IDX) <- C; (X,IDX+1) <- B
1136.                                  .        (062 116)  DPSR.IDX        (X,IDX) <- B; (X,IDX+1) <- C
1137.                                  .        (113 146)  DPS.IDX         (X,IDX) <- E; (X,IDX+1) <- D
1138.                                  .        (174 136)  DPSR.IDX        (X,IDX) <- D; (X,IDX+1) <- E
1139.                                  .        (115 166)  DPS.IDX         (X,IDX) <- L; (X,IDX+1) <- H
1140.                                  .        (176 156)  DPSR.IDX        (X,IDX) <- H; (X,IDX+1) <- L
1141.
1142.  001440L 00110111 00001100              STB      IMAR,SMR          GET THE INDEX
      001441L 00110111 01000111
1143.  001442L 00110001 10001001              DLDX     MR2PC             UPDATE THE PC SO IT CORRECT
      001443L 00110001 10101000
1144.  001444L 11010100 11011011              MWAIT    ,MEMPF1
      001445L 11010111 00001001
1145.  001446L 00110001 00110110              LDPP     MAROL,MDR         LSB ADDRESS
      001447L 00110111 11000000
1146.  001450L 00110001 11100111              LDX      XX2MRH+URX        AND MSB ADDRESS FROM X-REG
1147.  001451L 00110001 11011101              LDPP     MDW,I35I          SAVE THE REGISTER IN MEMORY
      001452L 00110111 00100001
1148.  001453L 11011001 11001110              BRA      FETPS,T@,IZ       DONE IF IMP ZERO
1149.  001454L 00110001 11011111              LDTP     IMPI              GET OTHER REG TO SAVE
1150.  001455L 11010100 11010010              MWAIT    ,MEMPF1
      001456L 11010111 00001001
1151.  001457L 00110111 00001100              STB      IMAR              POINT TO ITS SAVE AREA
1152.  001460L 00110111 00100001              LDPT     MDW               SAVE IT
1153. >001461L 01011001 11111111     FETPS    BRAX     FETCHW
      >001462L 11001111 11111111
```

```
1156.                                   *
1157.  001463L                         INCPA:
1158.                                  . 1.50   (    017)  INCP          HL <- HL + A
1159.                                  . 1.35   (062 017)  INCP          BC <- BC + A
1160.                                  . 1.35   (174 017)  INCP          DE <- DE + A
1161.                                  . 1.35   (022 017)  INCP          XA <- XA + A
1162.                                  . +0.65 IF CRY FROM LSB
1163.
1164.  001463L 11011000 11001001              BRA     INCPAS,F@,IZ
1165.  001464L 01010001 00000110              LDPI    LIMP,URL          USE HL IF NO IMP SPECIFICATION
       001465L 00110111 00000001
1166.  001466L 00110001 11010000  INCPAS      LDTP    URI+URA
1167.  001467L 11011111 11000000              BRA     INCPIT            T LOADED WITH VALUE TO ADD, GO DO IT
1168.                                   *
1169.  001470L                         INCP:
1170.                                  . 1.45   (    015)  INCP          HL <- HL + 1
1171.                                  . 1.45   (111 015)  INCP          XA <- XA + 2
1172.                                  . 1.30   (062 015)  INCP          BC <- BC + 1
1173.                                  . 1.45   (113 015)  INCP          BC <- BC + 2
1174.                                  . 1.30   (174 015)  INCP          DE <- DE + 1
1175.                                  . 1.45   (115 015)  INCP          DE <- DE + 2
1176.                                  . 1.45   (117 015)  INCP          HL <- HL + 2
1177.                                  . 1.30   (022 015)  INCP          XA <- XA + 1
1178.                                  . +0.65 IF CRY FROM LSB
1179.
1180.  001470L 11011000 11000100              BRA     INCPS,F@,IZ
1181.  001471L 01010001 00000110              LDPI    LIMP,URL          DEFAULT TO HL PAIR
       001472L 00110111 00000001
1182.  001473L 01010001 00000001  INCPS      LDTI    1                 ASSUME ITS BY 1 (ODD)
1183.  001474L 11011010 11000000              BRA     INCPIT,F@,IO
1184.  001475L 01010001 00000010              LDTI    2                 NO, BY 2 CAUSE WAS EVEN
1185.  001476L 00110111 00001001              STB     DIMP              CORRECT IT TO BE ODD
1186.  001477L 01101111 11110001  INCPIT     LDRT    TEMP1
1187.  001500L 00110001 11011111              DOPRP   IMPFO,AC,TEMP1,IMPI,C0 INC THE LSB (T-SAVE NECESSARY)
       001501L 01110010 00110001
       001502L 00110111 01101111
1188. >001503L 01011001 11111111              BRAX    FETCHI,FC         IF NO CARRY FORGET THE MSB
      >001504L 11000000 11111111
1189.  001505L 00110111 00001001              STB     DIMP
1190.  001506L 00110001 11011111              DOPIP   IMPFO,AC,0,IMPI   INC THE MSB (COULD USE IT)
       001507L 01010010 00000000
       001510L 00110111 01101111
1191.                                  .                                 CAN'T USE 'IT IMPFO' BECAUSE DELAYED
1192.                                  .                                 ALU CARRY THROUGH PROCESSOR CARRY
1193. >001511L 11001111 11111111              BRA     FETCHI
```

```
                                . REGISTER PAIR INCREMENT AND DECREMENT
1194.                           +
1195.  001512L                  DECPA:
1196.                           . 1.50   (     037)  DECP          HL <- HL - A
1197.                           . 1.35   (062 037)  DECP          BC <- BC - A
1198.                           . 1.35   (174 037)  DECP          DE <- DE - A
1199.                           . 1.35   (022 037)  DECP          XA <- XA - A
1200.                           . +0.65 IF BRW FROM LSB
1201.
1202.  001512L 11011000 10110010          BRA     DECPAS,F@,IZ
1203.  001513L 01010001 00000110          LDPI    LIMP,URL        SELECT HL AS DEFAULT REG PAIR
       001514L 00110111 00000001
1204.  001515L 00110001 11010000  DECPAS  LDTP    URI+URA
1205.  001516L 11011111 10101001          BRA     DECPIT          GO DECR. USING A-REG AS DISP.
1206.                           *
1207.  001517L                  DECP:
1208.                           . 1.45   (     035)  DECP          HL <- HL - 1
1209.                           . 1.45   (111 035)  DECP          XA <- XA - 2
1210.                           . 1.30   (062 035)  DECP          BC <- BC - 1
1211.                           . 1.45   (113 035)  DECP          BC <- BC - 2
1212.                           . 1.30   (174 035)  DECP          DE <- DE - 1
1213.                           . 1.45   (115 035)  DECP          DE <- DE - 2
1214.                           . 1.45   (117 035)  DECP          HL <- HL - 2
1215.                           . 1.30   (022 035)  DECP          XA <- XA - 1
1216.                           . +0.65 IF BRW FROM LSB
1217.
1218.  001517L 11011000 10101101          BRA     DECPS,F@,IZ
1219.  001520L 01010001 00000110          LDPI    LIMP,URL
       001521L 00110111 00000001
1220.  001522L 01010001 00000001  DECPS   LDTI    1               EXACTLY LIKE ABOVE BUT USING SB'S NOT A
1221.  001523L 11011010 10101001          BRA     DECPIT,F@,IO
1222.  001524L 01010001 00000010          LDTI    2
1223.  001525L 00110111 00001001          STB     DIMP
1224.  001526L 01101111 11110001  DECPIT  LDRT    TEMP1
1225.  001527L 00110001 11011111          DOPRP   IMPFO,SB,TEMP1,IMPI,C0
       001530L 01110100 00110001
       001531L 00110111 01101111
1226. >001532L 01011001 11111111          BRAX    FETCHI,FC       IF NO CARRY FORGET THE MSB
      >001533L 11000000 11111111
1227.  001534L 00110111 00001001          STB     DIMP
1228.  001535L 00110001 11011111          DOPIP   IMPFO,SB,0,IMPI
       001536L 01010100 00000000
       001537L 00110111 01101111
1229. >001540L 11001111 11111111          BRA     FETCHI
```

```
1232.                                   *
1233.  001541L                         DECX:
1234.                                  .       (    025)  DECI.LSP.IDX      (X,IDX+1 | X,IDX) <-
1235.                                  . 9.05~9.65                          (X,IDX+1 | X,IDX) - DSP
1236.                                  .       (111 025)  DECI.LSP.MSB.IDX (X,IDX+1 | X,IDX) <-
1237.                                  . 10.55~11.15                        (X,IDX+1 | X,IDX) - DSP
1238.                                  .       (062 025)  LFID.LSP.IDX     RP <- (X,IDX+1 | X,IDX) - DSP
1239.                                  .       (174 025)  LFID.LSP.IDX
1240.                                  .       (176 025)  LFID.LSP.IDX
1241.                                  . 7.55~8.15
1242.                                  .       (113 025)  LFID.LSP.MSP.IDX RP <- (X,IDX+1 | X,IDX) - DSP
1243.                                  .       (115 025)  LFID.LSP.MSP.IDX
1244.                                  .       (117 025)  LFID.LSP.MSP.IDX
1245.                                  . 9.05~9.65
1246.
1247.  001541L 01010001 01101011                BRC      INDX,,DECIT       GO TO INDEX SPECIFYING DECIT SET
       001542L 11011111 10011011
1248.                                   *
1249.  001543L                         INCX:
1250.                                  .       (    005)  INCI.LSP.IDX      (X,IDX+1 | X,IDX) <-
1251.                                  . 8.75~9.35                          (X,IDX+1 | X,IDX) + DSP
1252.                                  .       (111 005)  INCI.LSP.MSP.IDX (X,IDX+1 | X,IDX) <-
1253.                                  . 10.25~10.85                        (X,IDX+1 | X,IDX) + DSP
1254.                                  .       (062 005)  LFII.LSP.IDX     RP <- (X,IDX+1 | X,IDX) + DSP
1255.                                  .       (174 005)  LFII.LSP.IDX
1256.                                  .       (176 005)  LFII.LSP.IDX
1257.                                  . 7.45~8.05
1258.                                  .       (113 005)  LFII.LSP.MSP.IDX RP <- (X,IDX+1 | X,IDX) + DSP
1259.                                  .       (115 005)  LFII.LSP.MSP.IDX
1260.                                  .       (117 005)  LFII.LSP.MSP.IDX
1261.                                  . 8.95~9.55
1262.
1263.  001543L 01010001 10000000                BAL      .INCIT
```

. INDEXED LOCATIONS, INCREMENT AND DECREMENT IN PLACE OR TO REG PAIR

```
1264.                                   +
1265.  001544L                         INDX
1266.
1267.                                   . INDEXED OPERATIONS TAKES 2 BYTES ON PAGE X-REG ADDS DISPLACEMENT TO IT
1268.                                   .     AND STORES THE RESULT IN A REG. PAIR OR BACK ON TOP OF ITSELF
1269.
1270.  001544L 00110111 00001100                STB     IMAR,SMR          GET DISPLACEMENT LSP
       001545L 00110111 01000111
1271.  001546L 01101111 11110000                BAS     LINK              FREE REGISTER FOR INC, DEC SELECT
1272.  001547L 11010100 10011000                MWAIT   ,MEMPF1
       001550L 11010111 00001001
1273.  001551L 00110001 00110110                LDTP    MDR
1274.  001552L 00110111 00001100                STB     IMAR,SMR          GET MSP OR INDEX
       001553L 00110111 01000111
1275.  001554L 01101111 11110010                LDRT    TEMPL             SAVE LSP (LSP DISPLACEMENT)
1276.  001555L 01010001 00000000                TCLR                      ASSUME MSP IS ZERO
1277.  001556L 11011010 10001010                BRA     INDGET,F@,IO
1278.  001557L 11010100 10010000                MWAIT   ,MEMPF1           NO, GET MSP OF DISPLACEMENT
       001560L 11010111 00001001
1279.  001561L 00110001 00110110                LDTP    MDR               GOT MSB
1280.  001562L 00110111 00001100                STB     IMAR,SMR          POINT AND GET INDEX
       001563L 00110111 01000111
1281.  001564L 00110111 00001001                STB     DIMP              CORRECT IMP REG
1282.  001565L 01101111 11110001  INDGET       LDRT    TEMPH             SAVE MSP
1283.  001566L 00110001 10001001                DLDX    MR2PC             PC SAVED AS CORRECT VALUE NOW
       001567L 00110001 10101000
1284.  001570L 11010100 10000111                MWAIT   ,MEMPF1           GOTTINDEX
       001571L 11010111 00001001
1285.  001572L 00110001 00110110                LDPP    MAROL,MDR         INDEX TO THE MAR LSB
       001573L 00110111 11000000
1286.  001574L 00110001 11100111                LDX     XX2MRH+URX,SMR    AND MAR MSB FROM THE X-REG
       001575L 00110111 01000111
1287.  001576L 11101111 00000000                BRR     LINK              SELECT DECIT OR INCIT
1288.                                   *
1289.  001577L 11010100 10000000  INCIT       MWAIT   ,MEMPF1
       001600L 11010111 00001001
1290.  001601L 00110001 00110110                LDTP    MDR
1291.  001602L 00110111 00001100                STB     IMAR,SMR          START TO READ FOR MSB FAST
       001603L 00110111 01000111
1292.  001604L 01110010 00110010                DORR    TEMPL,AC,TEMPL,,C0 ADD DATA AND DISPLACEMENT LSB
       001605L 01101111 11110010
1293.  001606L 11010100 01111001                MWAIT   ,MEMPF1
       001607L 11010111 00001001
1294.  001610L 00110001 00110110                DOTRP   ,AC,TEMPH,MDR     ADD MSB PART, LEAVE RESULT IN T
       001611L 01110010 11110001
1295.  001612L 11011000 01011111                BRA     INDXL,F@,IZ       SELECT LOAD REG PAIR OR RELOAD MEMORY
1296.
1297.  001613L 00110111 00100001  INDXS       LDPT    MDW               PUT MSB RESULT BACK IN MEMORY
1298.  001614L 00110111 00000110                LDPT    LUF               SET CONDITION CODES
1299.  001615L 01110001 11110010                LDTR    TEMPL
1300.  001616L 11010100 01110001                MWAIT   ,MEMPF1           PUT LSB DATA BACK ALSO
       001617L 11010111 00001001
```

```
1301.  001620L 00110111 00001101          STB     DMAR                IN CORRECT SPOT
1302.  001621L 00110111 00100001          LDPT    MDW
1303. >001622L 01011001 11111111          BRAX    FETCHW
      >001623L 11001111 11111111
1304.
1305.  001624L 11010100 01101011  DECIT    MWAIT   ,MEMPF1
       001625L 11010111 00001001
1306.  001626L 00110001 00110110          LDTP    MDR                 GET LSB DATA
1307.  001627L 00110111 00001100          STB     IMAR,SMR            START TO READ FOR MSB FAST
       001630L 00110111 01000111
1308.  001631L 01110100 00110010          DORR    TEMPL,SB,TEMPL,,C0 SUBTRACT DISPLACEMENT FROM THE DATA
       001632L 01101111 11110010
1309.  001633L 11010100 01100100          MWAIT   ,MEMPF1
       001634L 11010111 00001001
1310.  001635L 00110001 00110110          DOTRP   ,SB,TEMPH,MDR       SIMILARLY FOR THE MSB PART
       001636L 01110100 11110001
1311.  001637L 11011001 01110100          BRA     INDXS,T@,IZ         SELECT LOAD REG PAIR OR RELOAD MEMORY
1312.
1313.  001640L 00110111 00001001  INDXL    STB     DIMP                CORRECT POINTER TO MSB
1314.  001641L 00110111 01101111          LDPT    IMPFO,IIMP          LOAD THE INDEX INTO A REGISTER PAIR
       001642L 00110111 00001000
1315.  001643L 01110001 11110010          LDPR    IMPO,TEMPL          THE LSB ALSO
       001644L 00110111 10001111
1316. >001645L 01011001 11111111          BRAX    FETCH
      >001646L 11001111 11111111
```

```
1319.                                   *
1320.  001647L                         DS:
1321.                                   . 3.95   (     027)  DS          (HL) <- E; (HL+1) <- D
1322.                                   . 4.65   (111 027)  DS          (HL) <- C; (HL+1) <- B
1323.                                   . 3.95   (113 027)  DS          (DE) <- C; (DE+1) <- B
1324.                                   . 3.80   (174 027)  DS          (BC) <- E; (BC+1) <- D
1325.                                   . 3.80   (176 027)  DS          (BC) <- L; (BC+1) <- H
1326.                                   . 3.95   (117 027)  DS          (DE) <- L; (DE+1) <- H
1327.
1328.  001647L 01010001 00110000                BRC      DLS,,DSTORE   SELECT REG PAIRS & DO SAVE
       001650L 11011111 01010001
1329.                                   *
1330.  001651L                         DLHL:
1331.                                   . 4.55   (     057)  DL          L <- (HL); H <- (HL+1)
1332.
1333.  001651L 01010001 00111111                BAL      LINK,DLOAD    LOAD REG PAIR
       001652L 01101111 11110000
1334.  001653L 01010001 00000110                LDTI     URL           HL
1335.  001654L 11011111 01000011                BRA      DLSLMP        FROM (HL)
1336.                                   *
1337.  001655L                         DL:
1338.                                   . 4.55   (     047)  DL          E <- (HL); D <- (HL+1)
1339.                                   . 5.25   (111 047)  DL          C <- (HL); B <- (HL+1)
1340.                                   . 4.40   (062 047)  DL          C <- (BC); B <- (BC+1)
1341.                                   . 4.55   (113 047)  DL          C <- (DE); B <- (DE+1)
1342.                                   . 4.40   (174 047)  DL          E <- (BC); D <- (BC+1)
1343.                                   . 4.55   (115 047)  DL          E <- (DE); D <- (DE+1)
1344.                                   . 4.40   (176 047)  DL          L <- (BC); H <- (BC+1)
1345.                                   . 4.55   (117 047)  DL          L <- (DE); H <- (DE+1)
1346.
1347.  001655L 01010001 00111111                BAL      ,DLOAD        LOAD SELECT
1348.                                   *
1349.  001656L                         DLS                            DECODE ADDRESS & REG SPEC. OPERATORS
1350.
1351.  001656L 01101111 11110000                BAS      LINK
1352.  001657L 11011001 01000100                BRA      DLSZRO,T@,IZ  DE,HL - 000
1353.  001660L 11011010 01001001                BRA      DLSBC,F@,IO   XX,BC - 062, 114...
1354.  001661L 00110111 00001001                STB      DIMP
1355.  001662L 00110001 11000100                LDX      DE2MRL        DELAY ONE FROM THE DIMP BEFORE BRA
1356.  001663L 11011001 01000110                BRA      DLSONE,T@,IZ  BC,HL - 111
1357.  001664L 00110001 11100011                LDX      DE2MRH
1358.  001665L 11101111 00000000                BRR      LINK          XX,DE - 113, 115...
1359.  001666L 00110001 11000010         DLSBC  LDX      XX2MRL+URC
1360.  001667L 00110001 11100001                LDX      XX2MRH+URB    XX,BC - 062, 114...
1361.  001670L 11101111 00000000                BRR      LINK
1362.  001671L 01010001 00000010         DLSONE LDTI     URC           BC,HL - 111
1363.  001672L 11011111 01000011                BRA      DLSLMP
1364.  001673L 01010001 00000100         DLSZRO LDTI     URE           DE,HL - 000
1365.  001674L 00110111 00000001         DLSLMP LDPT     LIMP
1366.  001675L 00110001 11000110                DLDX     HL2MR         XX,HL - 000, 111, HL,HL
       001676L 00110001 11100101
1367.  001677L 11101111 00000000                BRR      LINK
```

```
1368.                                   *
1369.  001700L                         DLOAD                           LOAD REGISTER PAIR FROM MEMORY
1370.
1371.  001700L 00110111 01000111                 STB     SMR
1372.  001701L 11001110 11111111                 MWAIT   NOOP,MEMPF1
       001702L 11010100 00111101
       001703L 11010111 00001001
1373.  001704L 00110001 00110110                 LDTP    MDR             GET THE LSB DATA
1374.  001705L 00110111 00001100                 STB     IMAR,SMR
       001706L 00110111 01000111
1375.  001707L 00110111 10001111                 LDPT    IMPO,DIMP       AND MORE OF THE SAME
       001710L 00110111 00001001
1376.  001711L 11010100 00110110                 MWAIT   ,MEMPF1
       001712L 11010111 00001001
1377.  001713L 00110001 00110110                 LDPP    IMPO,MDR        GET THE MSB
       001714L 00110111 10001111
1378. >001715L 01011001 11111111                 BRAX    FETCH
      >001716L 11001111 11111111
1379.                                   *
1380.  001717L                         DSTORE                          SAVE REGISTER PAIR IN MEMORY
1381.
1382.  001717L 00110001 11011111                 LDPP    MDW,IMPI,DIMP   OUTPUT LSB AND POINT TO MSB
       001720L 00110111 00100001
       001721L 00110111 00001001
1383.  001722L 00110001 11011111                 LDTP    IMPI
1384.  001723L 11010100 00101100                 MWAIT   ,MEMPF1
       001724L 11010111 00001001
1385.  001725L 00110111 00001100                 STB     IMAR
1386.  001726L 00110111 00100001                 LDPT    MDW             OUTPUT MSB
1387. >001727L 01011001 11111111                 BRAX    FETCHW
      >001730L 11001111 11111111
```

```
1390.                                   *
1391.  001731L                         BRL:
1392.                                  . 2.20   (    072)  BRL             BASE REGISTER LOAD
1393.                                  .        (IMP 072)  BRL             BASE <- (SEBRLS) <- R
1394.
1395.  001731L 00110001 11011100              TSTIP    ,SWUSER,PSWI
       001732L 01000101 00000100
1396.  001733L 11010010 00000111              BRA      IVIOL1,FZ
1397.  001734L 01010001 10101011              DLDPI    MARO,SEBRLS       SAVE BASE REG VALUE AWAY
       001735L 00110111 11000000
       001736L 01010001 11101111
       001737L 00110111 11100000
1398.  001740L 00110001 11011111              LDPP     BASW,IMPI         LOAD BASE REG BEFORE WRITE!
       001741L 00110111 00000011
1399.  001742L 00110111 00100001              LDPT     MDW
1400. >001743L 01011001 11111111              BRAX     FETCHW
      >001744L 11001111 11111111
1401.                                   *
1402.  001745L                         EI:
1403.                                  . 1.05   (    050)  EI              ENABLE INTERRUPTS
1404.                                  . 5.20   (111 050)  EJMP.LSB.MSB   ENABLE INTERRUPTS & PC <- NN
1405.                                  . 7.20   (062 050)  EUR             ENABLE INTERRUPTS & USER &
1406.                                  .                                  PC <- (SP+1 | SP); SP <- SP + 2
1407.
1408.  001745L 00110001 11011100              TSTIP    ,SWUSER,PSWI      NOT ALLOWED IN USER MODE
       001746L 01000101 00000100
1409.  001747L 11010010 00000111              BRA      IVIOL1,FZ
1410.  001750L 01010011 00000001              DOPI     PSWO,OR,SWINTE    SET THE INTERRUPTS ON BIT
       001751L 00110111 10001100
1411.  001752L 00110111 00000100              LDPT     MODW              IN EMULATION SUPPORT ALSO
1412. >001753L 01011001 11111111              BRAX     FETCHI,T@,IZ      WAS SIMPLE EI
      >001754L 11001001 11111111
1413. >001755L 11001111 11111111              BRA      EIROJ             WAS EJMP OR EUR
1414.                                   *
1415.  001756L                         DI:
1416.                                  . 1.05   (    040)  DI              DISABLE INTERRUPTS
1417.
1418.  001756L 00110001 11011100              TSTIP    ,SWUSER,PSWI      NOT ALLOWED IN USER MODE
       001757L 01000101 00000100
1419.  001760L 11010010 00000111              BRA      IVIOL1,FZ
1420.  001761L 01010101 11111110              DOPI     PSWO,ND,-1-SWINTE RESET THE BIT, DISABLING INTERRUPTS
       001762L 00110111 10001100
1421.  001763L 00110111 00000100              LDPT     MODW              IN EMULATION SUPPORT ALSO
1422. >001764L 01011001 11111111              BRAX     FETCHI
      >001765L 11001111 11111111
```

```
 1423.                                  *
 1424. >001766L 01011001 11111111      MEMPF1   BRAX     MEMPF$
       >001767L 11001111 11111111
 1425.                                  .
 1426.  001770L 01011001 11111111      IVIOL1   BRAX     IVIOL$
        001771L 11001111 01001001
 1427.                                  .
 1428.  001772L 11111111 11111111               TABPAGE  PROCL
        001773L 11111111 11111111
        001774L 11111111 11111111
        001775L 11111111 11111111
        001776L 11111111 11111111
        001777L 11111111 11111111
 1429.  002000                          PROCLEN  EQU      $-PROCP
 1430.  000000                                   USE      PROCL
 1431.  000000                                   SKIP     PROCLEN
 1432.  000000                                   END      POR
```

*** ERRORS: D

```
        AC              126     631     713     716     732     814     828     839     845     933     938     939
                        995    1001    1035    1040    1042    1053    1066    1081    1187    1190    1292    1294
010017  ACCTL           *56:I
010015  ACD             *53:I
010017  ACPH            *55:I    56:I    96
010016  ACPL            *54:I
        ACUOT           101
000417  ALPHA           *499
000541  ALPHAL          *614    517     518     551
000413  ALPHAS          *489    496
010014  APFRK           *47:I
010013  APFRP           *46:I
010016  APFTK           *49:I
010015  APFTP           *48:I
        BASW             93    1398
001126  BCP             *882
000400  BETA            *466
000471  BETAL           *554    483     484     611
000432  BETAS           *523    497
001226  BFAC            *974
001270  BFADD           *1001   981
001231  BFOP            *983    926     928     972
001300  BFS             *1011
001222  BFSB            *965
001326  BFSL            *1038   1023
001274  BFSUB           *1005   972
000236  BP              *360
020006  BR              *21:I
001731  BRL             *1391
001000  BT              *787
001032  BTCVT           *825    820
001103  BTEND           *845    831
001051  BTR             *833    809
001021  BTX             *822    808
        C0               713    716     828     839     845    1035    1053    1066    1081    1187    1225    1292
                        1308
        C1               136    295     823     830     900     904    1025
000100  CAP55IO         *121:I  125:I
000102  CAPABILI        *125:I
000000  CAPAPF          *118:I  125:I
000000  CAPBLUE         *117:I  125:I
000000  CAPCOM          *122:I  125:I
000000  CAPDMPIO        *119:I  125:I
000002  CAPIMA          *116:I  125:I   103     153     193     282     309     346     598     602
000000  CAPIVS          *135:I  *20:A
000000  CAPMICR         *115:I  125:I
000000  CAPRIM          *120:I  125:I
        CC               117    296     324     629     649     702     732     811     834     840     850     905
                         952    986     991    1027    1028    1031    1033    1038    1062    1063    1074    1075
                        1077    1079
001402  CCS             *1086
007000  CDOR            *133:I
```

```
006000  CDOX        *132:I
        CF           94    95    96    97   102   104   106   107   108   109   110   111
                    112   113   116   132   136   338   378   383   389   398   399   430
                    437   529   531   603   607   654   656   659   700   706   711   715
                    717   722   732   745   749   825   829   836   902   924   931   938
                    941   971   980   989   996  1001  1005  1034  1052  1065  1080  1186
                   1224  1271  1275  1282  1292  1294  1299  1308  1310  1315  1333  1351
        CMPF         89
        CODMIN      296
        CODMOUT     324
        CODWRT      316
030011  COMMODE     *75:I  102
        DE2MRH       810   827   838   899   992  1357
        DE2MRL       810   827   838   899   992  1355
001624  DECIT      *1305  1247
001517  DECP       *1207
001512  DECPA      *1195
001515  DECPAS     *1204  1202
001526  DECPIT     *1224  1205  1221
001522  DECPS      *1220  1218
001541  DECX       *1233
001177  DFADD       *937   925
001205  DFAEND      *942   940
001162  DFOP        *913   898
001174  DFSEND      *934   932
001170  DFSUB       *930   927
001756  DI         *1415
        DIMP         536   670   771   775  1185  1189  1223  1227  1281  1313  1354  1375
                    1382
001655  DL         *1337
001651  DLHL       *1330
001700  DLOAD      *1369  1333  1347
001656  DLS        *1349  1328
001666  DLSBC      *1359  1353
001674  DLSLMP     *1365  1335  1363
001671  DLSONE     *1362  1356
001673  DLSZRO     *1364  1352
        DMAR         133   433   447   539   590   597   632   673  1301
001647  DS         *1320
001717  DSTORE     *1380  1328
001745  EI         *1402
        EIROJ       1413
        EXMOUT       351
        FETCH       1123  1316  1378
        FETCHI       780  1055  1067  1082  1091  1188  1193  1226  1229  1412  1422
        FETCHRW      676
        FETCHW       353   662   961  1153  1303  1387  1400
000066  FETPC       *141   460
001436  FETPL      *1123  1119
001461  FETPS      *1153  1148
004000  FLEX       *131:I
000627  FTCHABW     *662   544
```

000770	FTCHIAB	*780	487	521	708								
000234	FTCHIO	*353	266										
	HL2MRH	287	306	668	729	822	833	903	987	1022	1366		
	HL2MRL	287	306	668	822	833	903	987	1022	1366			
	I35I	1147											
	I350	1118											
	IDCODH	876											
	IDCODL	342	876										
	IIMP	1314											
000224	IMAOUT	*347	311										
	IMAR	135	322	384	390	652	659	730	1112	1120	1142	1151	1270
		1274	1280	1291	1307	1374	1385						
	IMP8	534	669										
	IMPFO	1187	1190	1225	1228	1314							
	IMPI	537	712	1052	1061	1076	1149	1187	1190	1225	1228	1382	1383
		1398											
	IMPL	348											
	IMPO	350	674	1054	1064	1078	1090	1122	1315	1375	1377		
	INBUS	294											
001577	INCIT	*1289	1263										
001470	INCP	*1169											
001463	INCPA	*1157											
001466	INCPAS	*1166	1164										
001477	INCPIT	*1186	1167	1183									
001473	INCPS	*1182	1180										
001543	INCX	*1249											
001565	INDGET	*1282	1277										
001544	INDX	*1265	1247										
001640	INDXL	*1313	1295										
001613	INDXS	*1297	1311										
020005	IO	*20:I	484	518	809	926	1183	1221	1277	1353			
	IT	136	295	718	817	823	830	900	904	1025	1054		
	ITW	845											
000266	IVIOL$	*411	281	308	481	515	696	1426					
001770	IVIOLI	*1426	1396	1409	1419								
020004	IZ	*19:I	431	486	519	541	645	675	710	770	774	777	808
		898	1023	1119	1148	1164	1180	1202	1218	1295	1311	1352	1356
		1412											
	KBSC	98											
010001	KBSCNT	*28:I	97										
	LIMP	348	451	534	586	669	1165	1181	1203	1219	1365		
030000	LINK	*61:I	986	999	1271	1287	1333	1351	1358	1361	1367		
	LIREG	316	338										
	LUCF	1035	1043	1053	1066	1081							
	LUF	633	907	931	939	1002	1006	1298					
010003	MADR	*33:I	116										
	MARIH	295	823	830	835	841	900	904	988	993	1025	1039	
	MARIL	295	823	830	835	841	900	904	988	993	1025	1039	
	MAROH	125	130	443	659	718	725	746	817	1397			
	MAROL	131	531	559	619	658	716	814	1115	1145	1285	1397	
010004	MBITS	*34:I	95										
010005	MBSTAT	*35:I	94										

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010006  MCRCH       *36:I
010007  MCRCL       *37:I
        MDR          315    350    606    631    649    654    672    727    814    828    839    902
                     907    991    998   1030   1042   1115   1118   1122   1145   1273   1279   1285
                    1290   1294   1306   1310   1373   1377
010010  MDSKS       *38:I
010011  MDSKT       *39:I
        MDW          135    294    449    533    540    650    655    828    839    934    942   1001
                    1005   1032   1042   1147   1152   1297   1302   1382   1386   1399
        MEMPFS       782   1424
000772  MEMPF0      *782    314    340    349    429    538    550    605    630    648    651    653
                     657    671
001766  MEMPF1     *1424    813    826    837    875    901    906    990    997   1029   1041   1114
                    1117   1121   1144   1150   1272   1278   1284   1289   1293   1300   1305   1309
                    1372   1376   1384
000330  MEMPFSC     *455
000115  MIN         *270
000204  MINOUT      *326    297
000075  MINOWT      *187    337
000073  MINPAR      *183    284    293
000130  MINW0       *290    291
000204  MINW1       *327    328
020002  MO          *17:I    88    138    314    340    349    429    452    538    550    605    630
                     648    651    653    657    671    724    743    813    826    837    875    901
                     906    990    997   1029   1041   1114   1117   1121   1144   1150   1272   1278
                    1284   1289   1293   1300   1305   1309   1372   1376   1384
000551  MODLOD      *624    563
000634  MODLOP      *669    634
000433  MODSAV      *526    490
000503  MODSRV      *565    548
000446  MODSVLP     *536    541
        MODW          92    192    286    313    448    545    595    646    660    726    728   1411
                    1421
000113  MOIPAR      *267    320
000171  MOIW0       *317    318
000150  MOUT        *299
020003  MP          *18:I    314    340    349    429    453    538    550    605    630    648    651
                     653    657    671    724    743    813    826    837    875    901    906    990
                     997   1029   1041   1114   1117   1121   1144   1150   1272   1278   1284   1289
                    1293   1300   1305   1309   1372   1376   1384
        MR2HLH       323    731
        MR2HLL       323
        MR2PCH       391    434    591   1113   1143   1283
        MR2PCL       391    434    591   1113   1143   1283
010013  MSECT       *41:I
010012  MTRAK       *40:I
        OTBUS        315
000102  OUTW1       *260    261
000106  OUTW2       *263    264
        PC2MRH       377    390    433    590
        PC2MRL       377    390    433    590
        PCL          451    586
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        PCMOD          453
        PCOH           143
        PCOL           118     141
010000  PDLNP          *27:I   117
001407  PLR            *1095
        POPSTO         587
000000  POR            *82     1432
000043  PORLST         *125    127
000067  POROUT         *143    120
000057  PORZRO         *135    139
000111  PRE            *18:A   772
000000  PROC           *129:I   74
000000  PROCL          *76      78     462     783     1428
002000  PROCLEN        *1429   1431
000000  PROCP          *78     1429
002000  PROD           *130:I
        PSHSTO         453
001440  PSR            *1125
        PSWI           191     280     307     408     448     449     480     514     543     549     561     595
                       621     646     660     695     728     773     960     1395    1408    1418
        PSWO            91     191     450     488     522     607     628     960     1410    1420
010002  Q              *25:I   295     629     702     811     823     830     834     850     900     904     952
                       1025    1027    1028    1031    1033    1038    1062    1063    1074    1075    1077    1079
030010  RCH0C          *92:I   110
010014  RCH0D          *93:I
030012  RCH1C          *94:I   111
030013  RCH1D          *95:I
030014  RCH2C          *96:I   112
030015  RCH2D          *97:I
030016  RCH3C          *98:I   113
030017  RCH3D          *99:I
030006  RCRCH          *72:I
030007  RCRCL          *73:I
030007  RCVCTL         *91:I   106
        RCVMRK         110
030005  RDATA          *71:I
000631  REGL           *664    645
000636  REGLLP         *670    675
000563  REGS           *638
000444  REGSVLP        *534    661
        RETS           148
000014  REV             *2:I
001207  RIN16          *947    935     1003    1007    1036    1044
001110  RIN256         *854    846     908
001215  RIND           *957    748     750     847     862     909
001120  RINDO          *875    864
001124  RINRPT         *878    874
001116  RINST          *867    955
030004  RPNTR          *70:I
030003  RSTAT          *69:I
        SB             335     650     655     835     841     861     907     931     953     988     993     1005
                       1039    1225    1228    1308    1310
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000240	SC	*368										
010002	SCANSV	*29:I										
000245	SCBP	*380	366	374								
000304	SCDON	*440	400									
000274	SCLST	*431										
000271	SCLSTW	*424	184	268	412							
000300	SCPC	*434	385									
000302	SCRAM	*437	431									
000242	SCRAMI	*376										
000260	SCROM	*399	392									
000257	SCROML	*394										
000250	SCROMLI	*387										
	SDLCMD	100										
	SEBRLS	1397										
	SEDLBOT	117										
	SESAVAF	489	619									
	SESAVBF	523	559									
	SINS	294										
	SIOD	190	262	289	315							
	SL	702	1027	1074								
001346	SLC	*1048										
	SMR	306	560	597	620	632	647	652	668	673	719	730	810
		818	822	833	899	903	987	992	1022	1112	1116	1120	1142
		1270	1274	1280	1286	1291	1307	1371	1374				
	SNID	288	776									
	SOTS	321										
	SP2MRH	447	532	560	592	620	647					
	SP2MRL	446	594	647								
	SPIL	530	558	618								
	SR	1031	1033	1063	1077	1079						
001355	SRC	*1057										
001366	SRE	*1069										
	SRSYSMF	459										
	SRTMOUT	118										
	SRVDO	565										
	SRVREQ	341	547	739	873							
	SRVRPT	344	751	878								
	STAE	124										
	STATUS	260	263	290	317	327						
	STEK	119										
	STIODR	260	263	290	317	327						
000650	STL	*680										
000710	STLAGN	*722	740									
000740	STLDONE	*743	724	738								
	STLIMOUT	119										
000666	STLNRPT	*706	698									
000711	STLOOP	*724	734									
000672	STLRPTD	*710	704									
000677	STLZRO	*715	710									
	STPFIN	292										
	STPFOU	265	319									
	STW	125	129	444	727	747						

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                STWE            124
                SVBKPNT         365
                SVINP           183
                SVIVIOL         411
                SVOUTP          267
                SVSCAL          373
                SVUAINS         422
                SWALBT          485     520     549     561     610     621
                SWBASD          726
                SWIDEV          283     310     603     604
                SWINTE          286     313     545    1410    1420
                SWRPT           191     482     488     516     522     543     562     621     697     960
                SWSCF           448     450
                SWSTDT          603     604
                SWUSER          280     307     408     480     514     595     646     695    1395    1408    1418
                SYSESR          130     131
                SYSIVR          437
000505          SYSRET         *567     519
                SYSRET0         587
000512          SYSRET1        *589
                SYSROM          129     143     399     443     746
000415          SYSSAV         *492     486
000755          SYSTAT         *756
000767          SYSTND         *779     774     777
030001          TEMP1          *62:I     64:I    296     324     338     603     607     711     713     715     722     732
                                749      825     828     829     836     839     840     845     902     905     931     938
                                941      991    1001    1005    1034    1035    1052    1053    1065    1066    1080    1081
                               1186     1187    1224    1225
030002          TEMP2          *63:I     65:I    529     531     700     706     716     717     745     924     971     980
                                989      996
030001          TEMPH          *64:I     399     437     654     659    1282    1294    1310
030002          TEMPL          *65:I     132     136     378     383     389     398     430     649     656    1275    1292
                               1299     1308    1315
030003          TRNCHN         *87:I     109
030005          TRNCTL         *89:I     107
030004          TRNDTA         *88:I
010013          TRNFCN         *86:I     104
030006          TRNSEL         *90:I     108
000004          TYPE            *4:I
                UCFLG           533     995    1026    1040    1073    1090
                UDEH            830     841     900     993
                UDEL            830     841     900     993
000270          UDOP           *414     409     770
000263          UDPOP          *402
                URA             815     824     836    1166    1204
                URB             779     845     934     942    1360
                URC             335     700     707     772     861     953    1359    1362
                URE            1364
                URFO            335
                URH             295     717     720     745     816     823     835     904     988    1025    1039
                URI             335     700     707     716     717     812     816     824     836     845     861     934
                                942     953    1166    1204
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        URL             295     716     812     823     835     904     988    1025    1039    1165    1181    1203
                       1219    1334
        URO             295     720     745     772     779     815     823     830     835     841     861     900
                        904     953     988     993    1025    1039
030012  URPNTR         *76:I
        URX            1116    1146    1286
030010  UXPNTR         *74:I
000002  VER             *1:I
030016  XCRCH          *80:I
030017  XCRCL          *81:I
030015  XDATA          *79:I
030014  XPNTR          *78:I
030013  XSTAT          *77:I
        XX2MRH         1116    1146    1286    1360
        XX2MRL         1359
```