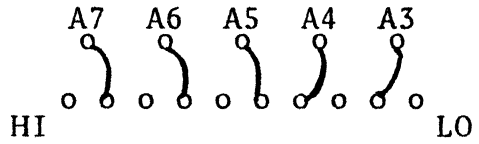
# D+7AI/O™ REV E

Cromemco
Specialists in computer peripherals
2432 Charleston Rd., Mountain View, CA 94043 • (415) 964-7400

# OPERATING INSTRUCTIONS

## Introduction

The Cromemco D+7A module allows you to input and output analog signals with your computer as easily as digital signals. Five port address jumpers on the D+7A board are used to select the port addresses of the eight (one digital and seven analog) I/O ports. The suggested selection is to use port 030 (octal) as the digital I/O port and ports 031 through 037 (octal) as the seven analog I/O ports. The pc traces located just above IC32 on the D+7A board are connected in the following way for this address selection:




If other port addresses are desired, these traces must be cut and the other corresponding addresses jumped appropriately.

## Connector Pin Assignments

The analog I/O channels, the parallel digital I/O channel, and several power supply voltages are brought to the edge connector on the top of the D+7A module. These contacts are gold-plated for high reliability. The following chart shows the detailed pin assignment for this connector:

CONNECTOR PIN ASSIGNMENTS

| COMPONENT SIDE | PIN No. | PIN No. | SOLDER SIDE |
|---|---|---|---|
| ANALOG GROUND | A | 1 | ANALOG GROUND |
| ANALOG INPUT 7 | B | 2 | ANALOG OUTPUT 7 |
| 6 | C | 3 | 6 |
| 5 | D | 4 | 5 |
| 4 | E | 5 | 4 |
| 3 | F | 6 | 3 |
| 2 | H | 7 | 2 |
| ANALOG INPUT 1 | J | 8 | ANALOG OUTPUT 1 |
| -12V REGULATED | K | 9 | +12V REGULATED |
| ANALOG GROUND | L | 10 | ANALOG GROUND |
| -17V UNREGULATED | M | 11 | +17V UNREGULATED |
| - 5V REGULATED | N | 12 | + 5V REGULATED |
| INPUT $\overline{STB}$ | P | 13 | OUTPUT $\overline{STB}$ |
| PARALLEL INPUT BIT 7 | R | 14 | PARALLEL OUTPUT BIT 7 |
| 6 | S | 15 | 6 |
| 5 | T | 16 | 5 |
| 4 | U | 17 | 4 |
| 3 | V | 18 | 3 |
| 2 | W | 19 | 2 |
| 1 | X | 20 | 1 |
| PARALLEL INPUT BIT 0 | Y | 21 | PARALLEL OUTPUT BIT 0 |
| DIGITAL GROUND | Z | 22 | DIGITAL GROUND |

PC BOARD

## Twos Complement Representation

The analog I/O channels use twos complement notation for ease of representing both positive and negative voltages. The least significant bit represents a 20 millivolt increment. The analog voltage range on both input and output is from -2.56 volts to +2.54 volts. For example, the following 8-bit codes are used to represent these analog voltages:

| | |
|---|---|
| 01111111 | +2.54 volts |
| 00000001 | +0.02 volts |
| 00000000 | 0 volts |
| 11111111 | -0.02 volts |
| 10000000 | -2.56 volts |

## Calibration Procedure

Two potentiometers are used for calibration of the A/D converter (R12 and R10) and two potentiometers are used for calibration of the D/A converter (R2 and R5 ). Calibration of the A/D converter must be done before calibration of the D/A converter.

To calibrate the A/D converter, known voltages must be applied to any one of the seven analog input channels (for example analog channel 7, port 037, on contact "B" of the top edge connector). Now enter and execute the following program with your computer to input from analog port 7 (port 037 octal) and output to digital port 030 (octal):

```
000 000 333 (input)    Note: output port 030 is
000 001 037 (port 037)       used here since it
000 002 323 (output)         is available on D+7A.
000 003 030 (port 030)       IMSAI 8080* users may
000 004 303 (jump)           find output port 377
000 005 000 (000)            on the front panel more
000 006 000 (000)            convenient to use.
```

*Note: if using front panel lights of an IMSAI computer for output port 377, note that light on is a logic low, off is high.

Apply a -2.56 volt signal to pin B and adjust R12 for an output of 1000000 on pins 14 to 21. Now apply a +2.54 volt signal to pin B of the top edge connector and adjust R10 for an output of 0111111 on pins 14 to 21 of the digital output port. Since R10 and R12 interact, you may need to repeat the above procedure once or twice.

To calibrate the D/A converter, a voltmeter must be used to measure the output voltage at any one of the seven analog output ports (say analog port 7, port 037, on contact "2" of the top edge connector). Now enter and execute the following program:

```
000 000 076
000 001 177
000 002 323 (output)
000 003 037 (to port 037)
000 004 303 (jump)
000 005 000 (000)
000 006 000 (000)
```

While the above program is executing adjust R5 for an output voltage on pin 2 of +2.54 volts. Now modify the above program so that the second byte, 177, is replaced by "000". Execute this modified program and adjust R2 so that the output voltage on pin 2 is zero. Calibration is now complete.

# D+7A I/O THEORY OF OPERATION

## Analog Output

When the CPU sends PSYNC and SOUT at the start of an analog output cycle in coincidence with a port address in the range 31 to 37, IC30 P6 goes high to indicate this event. Gating logic then causes PRDY to be pulled to a logic 0, causing the CPU to enter a wait state. One $\overline{CLK}$ cycle later, IC31 P8 goes low instructing the successive approximation register (SAR) to begin operation on the following $\overline{CLK}$ rising edge. The SAR then begins operation and holds down its $\overline{CC}$ output for an additional 8 $\overline{CLK}$ cycles. During analog output, the SAR is used only as a timing device to generate a sufficient number of wait states to cause proper circuit operation. Its other outputs are ignored. The logic gating holds down PRDY until the SAR has completed operation and released its $\overline{CC}$ output, causing IC31 P5 to go low. IC30 P6 goes low on the next Ø2 positive edge. A total of 5.5 $\mu$s of wait states are produced at 2MHz, and 5.0 $\mu$s at 4MHz.

As a result of SOUT going to a logic 1, IC34 P12 goes to a logic 0. This signal switches most of the circuitry between input and output modes. In particular, pin 1 of IC26 and IC35 go low, selecting the A inputs, and Q1 produces +5V at the control inputs of IC22, turning its sections ON.

With IC26 and IC35 switched to their A inputs, the 8 data bits flow from the DO bus to the inputs of the D/A converter IC12. This causes a current to be pulled by the IO output, pin 4, towards the −12V supply, with its magnitude proportional to the binary number at its inputs A1-A8. Resistors R10 and R11 provide the full scale reference current for the D/A converter, while R12 and R14 produce a half scale offset so that the code 10000000 at the D/A converter input produces 0 volts output.

Inverter IC34 complements DO7 so that 0 volts output occurs for the code 00000000 on the DO bus, thereby giving 2's complement operation. This allows bipolar operation of the D/A converter with binary numbers the CPU can generate.

Since the CMOS transmission gate IC22 is ON, a resistance of about 30 ohms connects the D/A converter output to pin 2 of IC10. This amplifier then produces whatever voltage is needed at its pin 6 (in the range ±2.56) so that the current through R5 and R7 exactly balances the D/A converter output current. The output voltage at IC10 P6 then goes to the output S/H multiplexer IC20 P3. The output port address bits AØ-A2 direct the multiplexer IC20 to connect IC10 P6 to one of the .0022 voltage hold capacitors with a CMOS transmission gate. Current then flows to charge the selected holding capacitor to the desired output voltage. Charging is enabled only during the wait states of an analog output function. Voltage follower amplifiers with MOS inputs copy the holding capacitor voltages to the analog output pins, thereby preventing drift due to loading. Residual voltage drift primarily results from CMOS multiplexer leakage currents. Because of the drift, the analog outputs in use must be refreshed at a 1Hz or faster rate by OUTPUT instructions.

Analog Input

At the start of an analog input cycle, the CPU sends PSYNC and SINP in coincidence with an analog port address. IC 30 detects this event and initiates a cycle in a manner similar to the analog output sequence. In this case, however, the SAR output is connected by the multiplexers IC26 and IC35 to the D/A converter's data inputs.

The input port command for channels 1 to 7 is taken from AØ through A2 by the analog multiplexer IC9 and used to connect an analog input to the voltage follower IC21. In this case, IC22 is an open circuit. Voltage follower IC21 has a very low input current requirement in combination with a fast slewing capability. This prevents loading of the signal sources and

allows full accuracy for source impedances of up to 10K ohms. Output from the voltage follower goes through R20 to inject current into the summing node at IC12 P4 and IC11 P2. After the time delay generated by IC31 to allow for settling of the input circuit, the SAR begins the conversion process.

When the conversion cycle starts, the SAR first sets its Q7 output to a logic Ø and outputs QØ through Q6 to a logic 1. This causes the D/A to sink a current equal to 127/256 of the full scale value of approximately 2mA. At the end of the first clock period, the SAR checks the output of the comparator IC11. If the analog input voltage is negative, the SAR leaves bit Q7 clear. Otherwise, it is set. At the same time, the SAR also sets Q6 to a logic Ø. It then waits one clock cycle before using the comparator output to set the state of Q6, and clears Q5. In a similar manner, the successive approximation procedure continues until all bits QØ-Q7 have been set and subsequently tested. This procedure corresponds to the use of a set of 2 pan balance scales with binary weight values to weigh an object, and is the fastest procedure operating on only one bit at a time.

At the end of the conversion cycle, the SAR outputs contain the desired data word. The $\overline{CC}$ output goes to a logic Ø, signalling the end of the conversion process and allowing the CPU to proceed. The CPU then inputs QØ-Q6 and $\overline{Q7}$ as its data. Q7 is complemented to produce a two's complement binary code and allow straightforward bipolar operation.

Digital Output

When digital output from the CPU to port Ø occurs, data flows from the DO bus through IC26 and IC35, serving as bus buffers, to the port latches IC1 and IC2. Decoder IC13 then uses $\overline{PWR}$ to generate an output strobe and latch the data into IC1 and IC2.

## Digital Input

When digital input from port Ø to the CPU occurs, IC13 generates an input strobe to tristate bus drivers IC16, IC27, and IC36. The digital input data is then passed directly to the DI bus.

## D+7A I/O APPLICATION INFORMATION

### 1. Source Impedance Effects

The analog inputs have a DC input impedance and bias current that are a function of the sampling rate for the port under consideration. At a 10KHZ sampling rate, $R_{IN}$=2MΩ and $I_B$=-.2μA. These values vary inversely with the sampling rate. To prevent loss of gain accuracy and zero offset, a maximum source impedance of 10KΩ is recommended for most applications. If the signal port will be digitized at the maximum rate of 100KHZ or so, the signal source should have $R_S$<100Ω. This requirement also stems in part from frequency response limitations imposed by the 1KΩ resistor and .001μf capacitor on each analog input. These components are to give some protection to the multiplexer in general purpose applications and may be omitted if the user is especially careful about static voltage dicharges and overvoltage inputs. Usually only the capacitor must be removed. This is recommended for best accuracy on high frequency inputs. If sampling rates of 100HZ or less are used, the analog inputs may be treated as an essentially infinite input impedance and used accordingly.

### 2. Input Accuracy

Since the analog input has a very high input impedance, and is commutated among the input ports with a low impedance multiplexer, all input channels track very closely when attached to a common voltage source. They normally differ by an unmeasurable quantity. The only factor disturbing tracking is the source impedance effect as described in (1) above.

3. Output Accuracy

As with inputs, the analog outputs use a common set of hardware down to the point where the demultiplex, sample and hold, and voltage follower activity occurs. Accordingly, the primary causes of inaccuracy are pedestal error in charging the output capacitor and offset in the voltage follower. The pedestal error has a dynamic dependence on the magnitude of voltage change for the output in question. Under worst case conditions, the pedestal error may be as much as $\pm$3 LSB's (60mv) for a full scale voltage change of 5.12V.

For smaller step changes the pedestal error diminishes rapidly in size, since it is a 2nd order phenomenon. Pedestal error can be practically eliminated by doing two outputs of the same value in succession when large changes occur.

Also, during steady state operation as with test program D or E, there is a static error caused by the demultiplexer switching transients. This causes a nonlinearity evidenced by the + full scale output being slightly high ($\sim$20mv) when the zero and - full scale outputs are correct. This error term is a function of the internal demultiplexer construction and occurs on ports 33, 35, and 36 for the IC's presently in use.

Offset voltage in the voltage follower for each analog output adds directly to the output for that channel. Typically, this is less than 8mv ($<$1/2 LSB) for the CA3140 devices, so no offset adjustment is provided on a per channel basis. In applications requiring careful channel matching, the CA3140's may have to be rearranged or selected to give the desired performance. Alternately, offset adjustment pots can be added according to the manufacturer's data sheet.

4. Output Drift

Since the analog outputs use a sample and hold to retain the output voltage after each output action, periodic refreshing of the capacitor voltage is necessary. The typical drift rate is $< 10$mv/sec at $25^{o}$C, requiring refresh at a rate of 1HZ or faster. In continuous control situations this usually doesn't cause a problem since the feedback iteration rate is faster. Incidentally, 10mv/sec drift corresponds to a total leakage of $20 \times 10^{-12}$ amperes from the capacitor. Therefore, cleanliness of the PCB is essential for good operation. The drift rate exhibits a strong dependence on temperature, increasing rapidly at high temperatures.

If problems with excessive drift occur, first try interchanging the associated CA 3140 with one from a good port location. If the drift is not reduced, then exchange the input and output CD4051 multiplexer IC's. The input multiplexer location is much more tolerant of leakage currents. Persistent problems with drift indicate either a defective holding capacitor or contamination on the capacitor or associated PCB area.

5. Bipolar/Unipolar Operation

The D+7A is normally used for analog voltages in the range of -2.56 to +2.54 volts. Since both positive and negative voltages are included in this range this is referred to as "bipolar operation". Bipolar operation is selected by a trace on the D+7A pc board connecting the "polarity" pad to the "bipolar" pad.

If you desire unipolar operation (0 to 2.54v or 0 to -2.56) this is also possible. Simply sever the trace connecting "polarity" to "bipolar" and in its place install a jumper from "polarity" to "unipolar". See Table 1 on the schematic diagram for proper resistor values with this mode of operation.

## 6. Rescaling Inputs

The nominal input voltage range is -2.56V to +2.54V. This can be altered for unipolar operation or larger bipolar voltage ranges. The component values of Table 1 tell what resistor valves to alter for unipolar operation. Note that the input voltage range must lie between ±2.56V to prevent saturation problems in the multiplexers and buffer amplifiers. However, resistor dividers may be added at the appropriate points to permit input ranges to ±100V and output ranges to ±10V. The only restriction is that all inputs and outputs must be of the same type, i.e., unipolar or bipolar, as this is determined by the D/A converter configuration.

Table 1

| MODE | R22 | R5 | R7 & R20 | R12 | R14 | VOLTAGE |
|---|---|---|---|---|---|---|
| BIPOLAR | OMIT | 500 | 2.7 K | 500 | 5.1 K | -2.56 to 2.54 |
| + UNIPOLAR | 100K | 200 | 1.3 K | 20K | 39 K | 0 to 2.54 |
| - UNIPOLAR | OMIT | 200 | 1.3 K | 200 | 2.4 K | -2.56 to 0 |

Fig 1

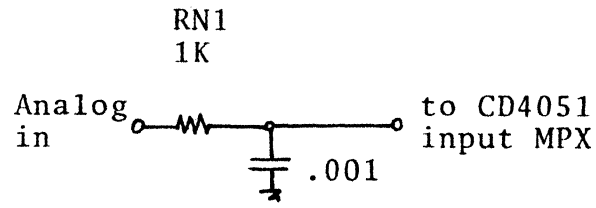
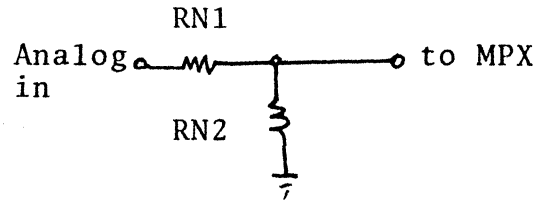



Fig 2




$$\frac{RN1}{RN2} = \frac{Vm-2.56}{2.56}$$

Given that the nominal maximum converter input is 2.56 volts, the input bypass capacitor may be replaced by a resistor RN2. The resistors RN1 and RN2 then form a voltage divider to reduce the maximum input Vm to 2.56 volts according to the equation in Fig 2. The PCB layout allows substitution of a resistor DIP network for the capacitors if all inputs are to be similarly scaled. When all inputs are scaled to the same sensitivity, the A/D gain and offset adjustments may be used to alter the basic ADC range. This permits use of standard resistor values for RN1 and RN2.

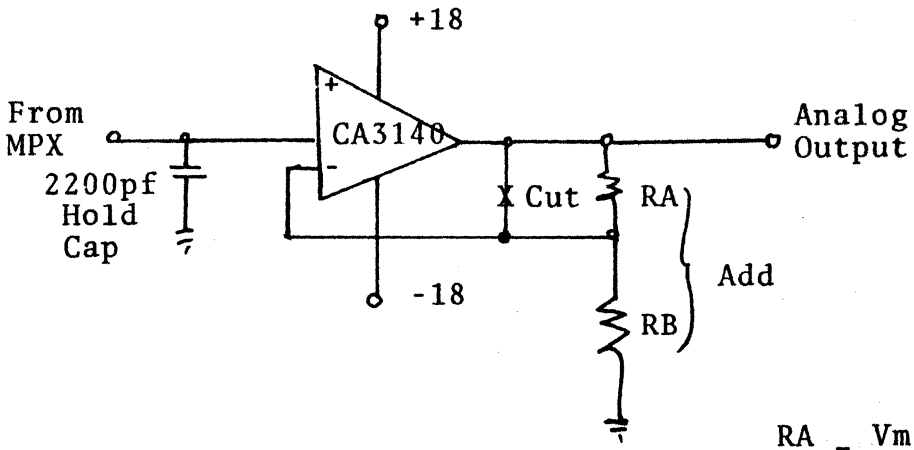
In order to preserve the ADC accuracy in critical gain matched applications, the input divider RN1 and RN2 must be metal film devices with a ±0.1% tolerance. Most engineering applications will allow use of 1% resistors. Type RN55C metal film resistors are preferred. This gives an absolute channel input accuracy of ±2% worst case. Hobby and error feedback applications may permit use of 5% tolerance resistors.

It is recommended that the parallel combination of RN1 and RN2 be kept below 10K ohms. This may be easily done by always using RN2=10K ohms. Then for Vm=10 volts, use RN1=28.7K ohms as the nearest common 1 value. When using this divider, be careful that its equivalent 40K ohm input impedance does not seriously load the signal source.

## 7. Rescaling Outputs

The sample and hold output amplifiers are presently configured as unity gain voltage followers for ±2.56V maximum output. If greater output is desired, such as ±10V, two changes must be made. First, the amplifiers are connected to the +18 and -18 voltage busses for power to allow larger output savings. Second, a feedback voltage divider as shown in Fig 3 permits gain in the voltage follower.

Fig 3




$$\frac{RA}{RB} = \frac{Vm-2.56}{2.56}$$

Changing the amplifiers to ±18V power requires cutting the power traces on the PCB and installing appropriate jumpers. Pads are provided for installation of the resistors RA and RB. A trace on the PCB solder side must be cut to permit RA to function.

The equations for RA and RB are identical to the input divider equations, and similar resistor values are required. Again, 10K ohms is a good nominal value for RB, making RA= 28.7 ohms for Vm=±10V maximum output.

8. D+7A Timing

Conversion time for the D+7A A-to-D converter is 5 microseconds. To assure complete conversion before allowing the processor to proceed, the READY line is held down for 5.5 microseconds, i.e. 11 wait states, whenever data is input fron one of the seven analog input ports. The ready line is also held down for 5.5 microseconds when data is output to one of the seven analog output ports to assure adequate time for settling of the analog sample and hold amplifier. When operating with the ZPU at 4 MHZ, a total of 21 wait states (5.25μs) is invoked.

9. Using the D+7A with the Cromemco Dazzler

If the Cromemco Dazzler is being used to display a picture when the D+7A is used to input or output analog data, a small modification must be made to REV B and REV B-1 series of the Dazzler to avoid flashes in the picture. The modification is simply to remove pin 10 of Dazzler IC 29 (a 7400 IC). No modification is required to REV C Dazzlers.

10. New Joystick Console

Cromemco is pleased to announce a new joystick console (model JS-1) designed specifically to interface to your computer using the D+7A interface. In fact two such consoles can be completely interfaced using just one D+7A board. Each console consists of a two-axis joystick, four push-button control switches, and a speaker with amplifier. The JS-1 kit is available for $65. Assembled for $95.

11. Service

Should your D+7A require repair, servicing or calibration, you may return it to Cromemco, 2400 Charleston, Mountain View, California, 94043 along with payment of our

fixed service fee of $35. We will service and calibrate your D+7A module and return it postpaid.

Units returned without the $35 service fee will be returned freight collect and will not be serviced.

We reserve the right to decline servicing any unit that has been subject to abnormal electrical or mechanical abuse or that has been modified from the original design. All our kits are supplied with IC sockets and we will not repair boards unless these IC sockets are used.

# D+7A I/O TECHNICAL SPECIFICATIONS

Interface:

Computer - S-100 Bus

Known compatibility with ALTAIR, IMSAI, and CROMEMCO machines using 8080 and Z80 CPU's at 2 or 4 MHZ.

Digital Ports

Standard TTL signal levels
Input 8 bits - one TTL equivalent load
Output 8 bits - can drive up to 10 TTL loads
Logic levels
$>$+2.0V - logic 1
$<$+0.8V - logic 0
Strobes - output is normally a logic 1 state
Trailing edge of a pulse to logic 0 state indicates occurrence of data transfer.
Separate input and output strobes.
Output 8 data bits are latched.

Analog Ports (after calibration; typical values)

Signal levels for standard configuration:

| | |
|---|---|
| +2.54V - 01111111 | - .02V - 11111111 |
| + .02V - 00000001 | -2.54V - 10000001 |
| 0.0V - 00000000 | -2.56V - 10000000 |

Two's complement code
Data Input:
Absolute maximum allowed - $\pm$5.0V
Input impedance
$Z_{in}$ = 20M$\Omega \| .001\mu f$ , 1KHZ sample rate
$Z_{in}$ = 2M$\Omega \| .001\mu f$ ,10KHZ sample rate
Recommended source impedance $R_S < 10K\Omega$
Input bias current $|I_B| < 2\ \mu A$ and flows into inputs
Accuracy $\pm \frac{1}{2}$ LSB
No missing codes
Data Output:
Maximum load current $|I_L| \leq 1.5mA$
$R_L min \geq 2K\Omega$
Output impedance $Z_{out} < .25\Omega$, F$\leq$10KHZ
Accuracy $\pm \frac{1}{2}$ LSB when refreshed
Drift rate $\left|\frac{dv}{dt}\right| < 10mV/sec$ at 25°C

# D+7A KIT ASSEMBLY INSTRUCTIONS

If you purchased your D+7A as a kit you will find the assembly to be straightforward. The location and value of every component is printed directly on the pc card to facilitate assembly. The components are simply inserted as shown and soldered into position. Be sure to use a low-wattage soldering iron and high-quality rosin-core solder.

1. Install all IC sockets. Note that IC sockets must be used for all ICs except the voltage regulators (IC3, IC6, and IC28).

2. Install all resistors. The resistor color codes are shown below:

| | |
|---|---|
| 10 | brown-black-black |
| 100 | brown-black-brown |
| 150 | brown-green-brown |
| 180 | brown-gray-brown |
| 220 | red-red-brown |
| 470 | yellow-violet-brown |
| 560 | green-blue-brown |
| 1K | brown-black-red |
| 1.2K | brown-red-red |
| 1.5K | brown-green-red |
| 2.2K | red-red-red |
| 2.4K | red-yellow-red |
| 2.7K | red-violet-red |
| 4.7K | yellow-violet-red |
| 5.1K | green-brown-red |
| 10K | brown-black-orange |
| 18K | brown-gray-orange |
| 100K | brown-black-yellow |

3) Install calibration potentiometers R2, R5, R10, R12. NOTE: R2 is 25K, the others are 500 ohms.

4) Install resistor network RN2. Note that pin 1 is leftmost, as indicated by the arrow.

5) Install all six diodes in place taking care that the banded (cathode) end of each diode is properly oriented.

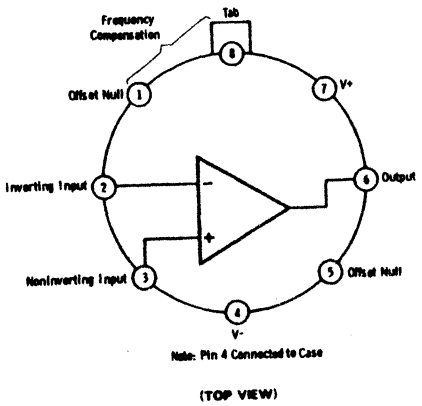
6) Install transistor Q1 (2N3906) and install IC6 (78L05). Note that the flat surface of each of these parts faces the top of the pc board.

7) Install voltage regulator ICs 3 and 28. A heatsink should be placed between the regulator and the pc board and the assembly secured with 6-32 hardware. Note that IC3 is a LM340T-5 or 7805 part. IC28 is a LM320T-5 or 7905 part. BE CAREFUL NOT TO INTERCHANGE THESE TWO ICs.

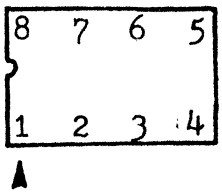
8) Install the two inductors L1 and L2.

9) Install all capacitors as marked on the pc board. Note that the "+" end of each of the tantalum capacitors must be oriented properly. Capacitors C31, C32, C33, and C34 are mounted side-by-side but should NOT be in physical contact with one another.

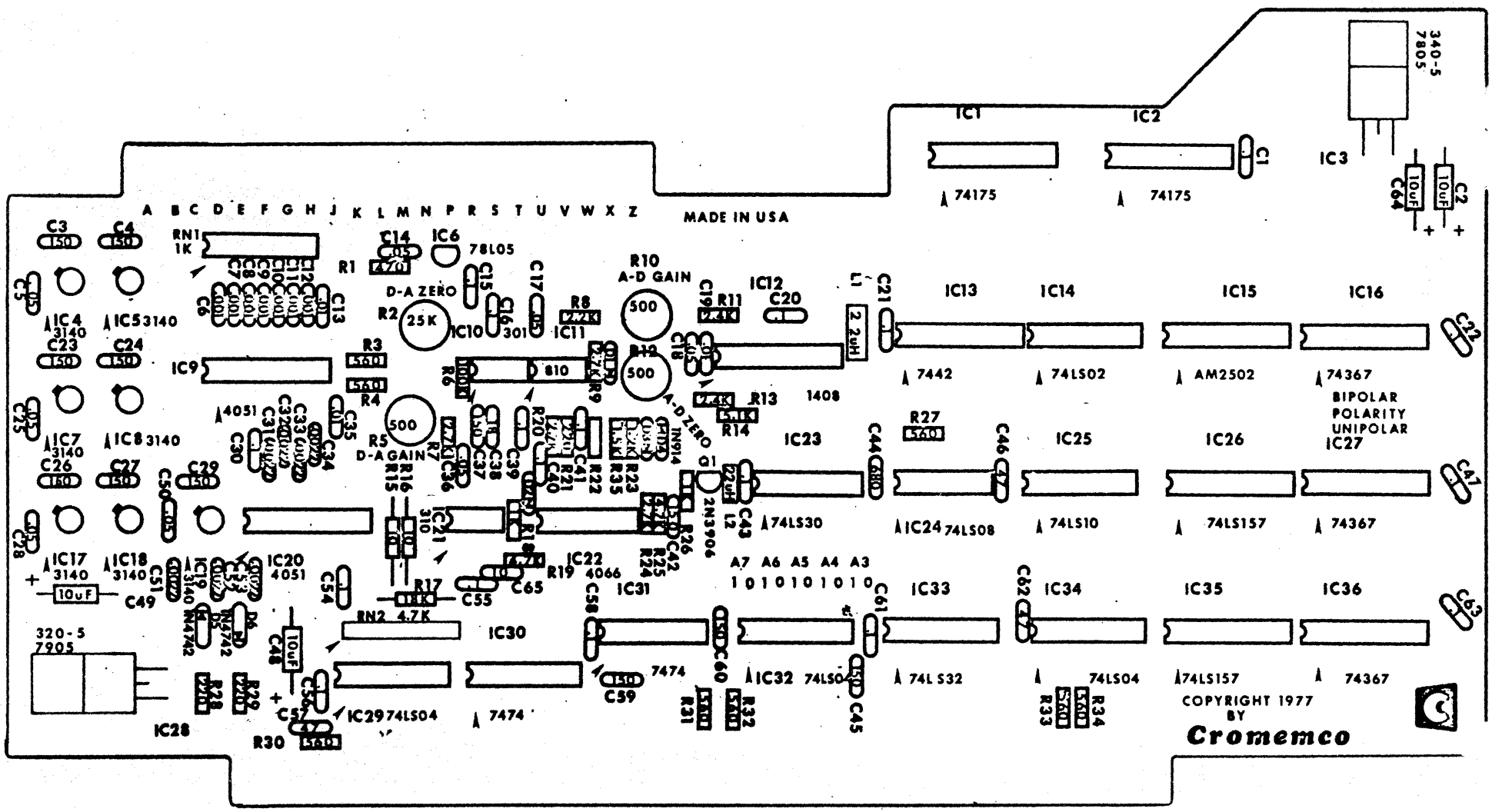
10) Install all ICs and RN1 in their sockets taking care to see that pin one of each part is oriented as indicated by the arrow on the pc board. When installing ICs in the metal TO-5 style case note that the metal tab denotes pin 8 of the IC as shown below:




The leads of the TO-5 style ICs should be shaped into two rows of four and inserted into the IC socket in this order:




11) Carefully inspect your work. Make certain that the ICs are all properly oriented and that every pin of every IC is properly engaged in its socket. Carefully inspect your soldering for cold solder joints or accidental solder bridges.


A B C D E F G H J K L M N P R S T U V W X Z
MADE IN USA
IC1
IC2
IC3
74175
74175
340-5
7805
C64
10uF
C2
10uF
RN1
1K
C14
.05
IC6
78L05
R1
470
C15
C16
.01
C17
.01
R10
A-D GAIN
500
D-A ZERO
R2
25K
IC10
301
IC11
R8
7.2K
C19
.01
R11
7.4K
IC12
C20
L1
2.2uH
C21
IC13
IC14
IC15
IC16
C22
C3
150
C4
150
C5
.05
C6
.01
C13
.01
IC4
3140
IC5
3140
C23
150
C24
150
IC9
R3
560
R4
560
R6
100
810
R9
2.7K
R19
500
A-D ZERO
R13
7.4K
R14
1.1K
1408
7442
74LS02
AM2502
74367
BIPOLAR
POLARITY
UNIPOLAR
IC27
4051
C31
.01
C32
.01
C33
.01
C34
.01
C35
.01
R5
D-A GAIN
500
R7
2.7K
C36
.05
C37
.05
C38
.01
C39
.01
R20
2.7K
C40
.01
C41
.01
R21
2.7K
R22
2.7K
R35
1.5K
R23
2.7K
IN914
Q1
2N3906
R26
2.7K
C42
.01
R24
2.7K
R25
2.7K
R27
560
C44
.01
C46
.01
IC23
IC25
IC26
C41
.01
C43
.22uF
L2
74LS30
IC24
74LS08
74LS10
74LS157
74367
C25
.05
C26
150
C27
150
C29
150
C50
.05
C30
.01
R15
100
R16
100
IC21
310
R18
2.7K
C28
.05
IC17
3140
IC18
3140
IC19
3140
IC20
4051
C51
.01
10uF
C49
C53
.01
C54
.01
R17
4.7K
C55
.01
C65
.01
IC22
4066
R19
A7 A6 A5 A4 A3
1 0 1 0 1 0 1 0 1 0
IC31
C58
.01
C60
.01
C61
.01
IC33
IC34
IC35
IC36
C62
C63
320-5
7905
D4
1N4742
D5
1N4742
R21
220
R28
220
C48
10uF
RN2 4.7K
IC30
7474
IC32
74LS04
74LS32
74LS04
74LS157
74367
C59
.05
R31
560
R32
560
C45
.01
R33
560
R34
560
IC28
C57
10uF
IC29
74LS04
7474
R30
560
COPYRIGHT 1977
BY
Cromemco

# D+7A PARTS LIST

1) Voltage regulators and hardware.

IC 3 - LM340T-5.0 (7805)
IC 6 - 78L05
IC28 - LM320T-5.0 (7905)
2 - 6-32 x 3/8 screws
2 - 6-32 nuts
2 - #6 lock washers
2 - Heatsinks

2) IC sockets

12 - 14 pin
16 - 16 pin
2 - 8 pin

3) Integrated Circuits

IC 1 - 74175
IC 2 - 74175
IC 4 - 3130 or 3140
IC 5 - 3130 or 3140
IC 7 - 3130 or 3140
IC 8 - 3130 or 3140
IC 9 - 4051
IC 10 - LM301
IC 11 - 72710 or 72810
IC 12 - MC1408L8
IC 13 - 7442
IC 14 - 74LS02
IC 15 - AM2502PC
IC 16 - 74367
IC 17 - 3130 or 3140
IC 18 - 3130 or 3140
IC 19 - 3130 or 3140
IC 20 - 4051
IC 21 - 310
IC 22 - 4066
IC 23 - 74LS30
IC 24 - 74LS08
IC 25 - 74LS10
IC 26 - 74LS157
IC 27 - 74367
IC 29 - 74LS04
IC 30 - 7474
IC 31 - 7474
IC 32 - 74LS04
IC 33 - 74LS32
IC 34 - 74LS04
IC 35 - 74LS157
IC 36 - 74367

4) Resistors and discrete semiconductors.

R 1 - 470
R 2 - 25k pot
R 3 - 560
R 4 - 560
R 5 - 500 pot
R 6 - 100k
R 7 - 2.7k
R 8 - 2.2k
R 9 - 2.7k
R 10 - 500 pot
R 11 - 2.4k
R 12 - 500 pot
R 13 - 2.4k
R 14 - 5.1k
R 15 - 10
R 16 - 10
R 17 - 18k
R 18 - 1k
R 19 - 4.7k
R 20 - 2.7k
R 21 - 220
R 22 - omit for bipolar operation
R 23 - 1.2k
R 24 - 2.7k
R 25 - 4.7k
R 26 - 1k
R 27 - 560
R 28 - 220
R 29 - 220
R 30 - 560
R 31 - 560
R 32 - 560
R 33 - 560
R 34 - 560
R 35 - 1.5k
RN 1 - 14 pin dip 7 resistors 1k
RN 2 - 8 pin sip, 7 resistors, 4.7k

D 1 - 1N914
D 2 - 1N914
D 3 - 1N914
D 4 - 1N914
D 5 - 1N4742
D 6 - 1N4742

Q 1 - 2N3906

5) Capacitors

C 1 - 0.1
C 2 - 10 uF tantalum
C 3 - 150
C 4 - 150
C 5 - .05
C 6 - .001
C 7 - .001
C 8 - .001
C 9 - .001
C 10 - .001
C 11 - .001
C 12 - .001
C 13 - .01
C 14 - .05
C 15 - 0.1
C 16 - 0.1
C 17 - .05
C 18 - .05
C 19 - .01
C 20 - 0.1
C 21 - 0.1
C 22 - 0.1
C 23 - 150
C 24 - 150
C 25 - .05
C 26 - 150
C 27 - 150
C 28 - .05
C 29 - 150
C 30 - 0.1
C 31 - .0022
C 32 - .0022
C 33 - .0022
C 34 - .0022
C 35 - .01
C 36 - .05
C 37 - 150
C 38 - 18
C 39 - 0.1
C 40 - 0.1
C 41 - 0.1
C 42 - 150
C 43 - 0.1
C 44 - 680
C 45 - 150
C 46 - 47
C 47 - 0.1
C 48 - 10 uF tantalum
C 49 - 10 uF tantalum
C 50 - .05
C 51 - .0022
C 52 - .0022
C 53 - .0022
C 54 - 0.1
C 55 - 0.1
C 56 - 0.1
C 57 - 47
C 58 - 0.1
C 59 - 150
C 60 - 150
C 61 - 0.1
C 62 - 47
C 63 - 0.1
C 64 - 10uF
C 65 - 10 Pf

6) Inductors

L1 - 22uH
L2 - 22uH

7) Connector Assembly

Dual 22 contact connector, hood, assembly hardware.

8) Miscellaneous

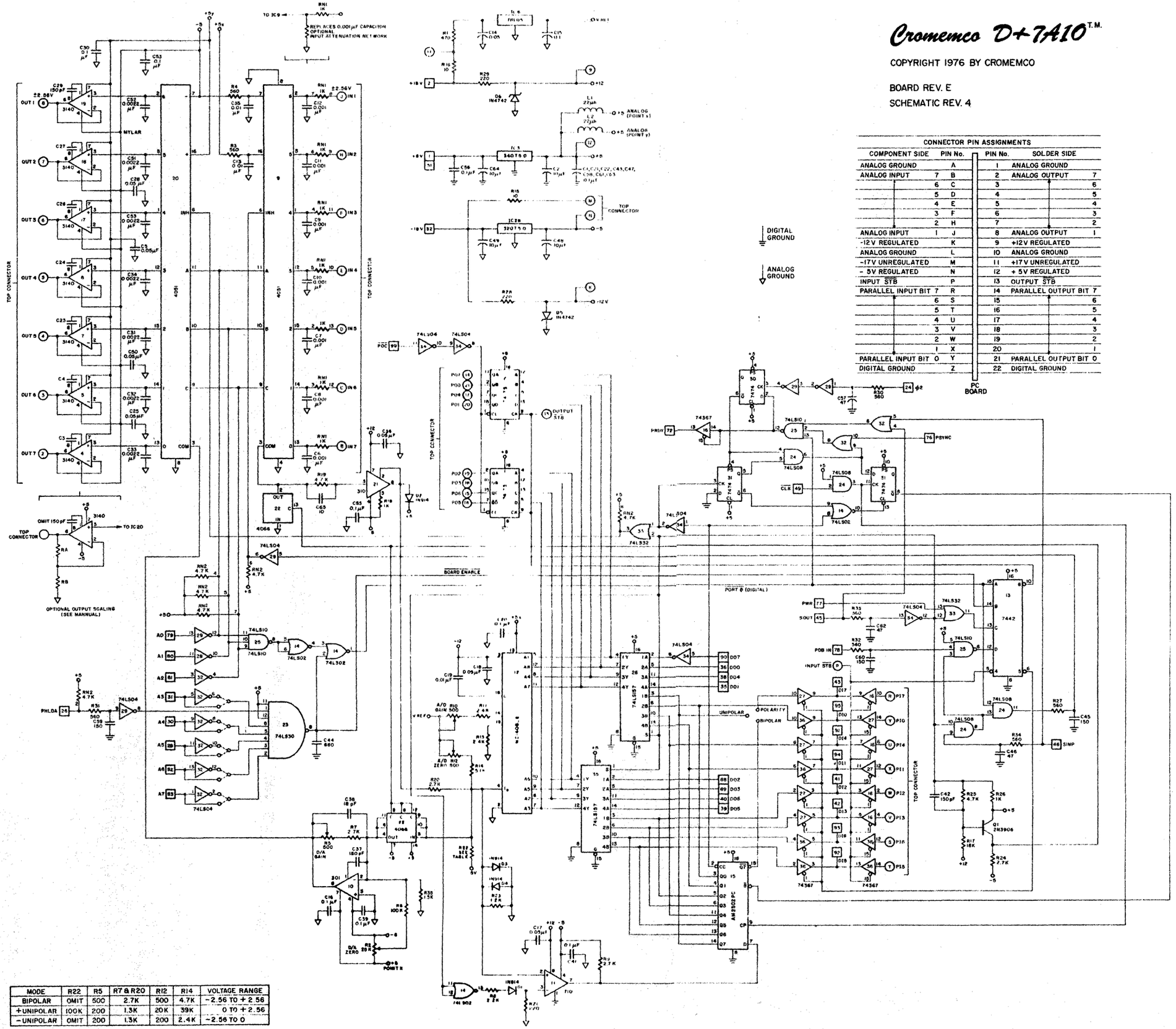
Printed circuit board.
Assembly and operating instructions.
Schematic diagram.

# Cromemco D+7A10™



BOARD REV. E

SCHEMATIC REV. 4



CONNECTOR PIN ASSIGNMENTS

| COMPONENT SIDE | PIN No. | | PIN No. | SOLDER SIDE |
|---|---|---|---|---|
| ANALOG GROUND | | A | 1 | ANALOG GROUND |
| ANALOG INPUT 7 | | B | 2 | ANALOG OUTPUT 7 |
| 6 | | C | 3 | 6 |
| 5 | | D | 4 | 5 |
| 4 | | E | 5 | 4 |
| 3 | | F | 6 | 3 |
| 2 | | H | 7 | 2 |
| ANALOG INPUT 1 | | J | 8 | ANALOG OUTPUT 1 |
| -12 V REGULATED | | K | 9 | +12 V REGULATED |
| ANALOG GROUND | | L | 10 | ANALOG GROUND |
| -17 V UNREGULATED | | M | 11 | +17 V UNREGULATED |
| - 5V REGULATED | | N | 12 | + 5V REGULATED |
| INPUT STB | | P | 13 | OUTPUT STB |
| PARALLEL INPUT BIT 7 | | R | 14 | PARALLEL OUTPUT BIT 7 |
| 6 | | S | 15 | 6 |
| 5 | | T | 16 | 5 |
| 4 | | U | 17 | 4 |
| 3 | | V | 18 | 3 |
| 2 | | W | 19 | 2 |
| 1 | | X | 20 | 1 |
| PARALLEL INPUT BIT 0 | | Y | 21 | PARALLEL OUTPUT BIT 0 |
| DIGITAL GROUND | | Z | 22 | DIGITAL GROUND |

PC BOARD

| MODE | R22 | R5 | R7 & R20 | R12 | R14 | VOLTAGE RANGE |
|---|---|---|---|---|---|---|
| BIPOLAR | OMIT | 500 | 2.7K | 500 | 4.7K | -2.56 TO +2.56 |
| +UNIPOLAR | 100K | 200 | 1.3K | 20K | 39K | 0 TO +2.56 |
| -UNIPOLAR | OMIT | 200 | 1.3K | 200 | 2.4K | -2.56 TO 0 |

# Cromemco D+7A10 T.M.



BOARD REV. C

SCHEMATIC REV. 3

CONNECTOR PIN ASSIGNMENTS

| COMPONENT SIDE | PIN No. | | PIN No. | SOLDER SIDE |
|---|---|---|---|---|
| ANALOG GROUND | | A | 1 | ANALOG GROUND |
| ANALOG INPUT | 7 | B | 2 | ANALOG OUTPUT 7 |
| | 6 | C | 3 | 6 |
| | 5 | D | 4 | 5 |
| | 4 | E | 5 | 4 |
| | 3 | F | 6 | 3 |
| | 2 | H | 7 | 2 |
| ANALOG INPUT | 1 | J | 8 | ANALOG OUTPUT 1 |
| -12 V REGULATED | | K | 9 | +12V REGULATED |
| ANALOG GROUND | | L | 10 | ANALOG GROUND |
| -17V UNREGULATED | | M | 11 | +17V UNREGULATED |
| - 5V REGULATED | | N | 12 | + 5V REGULATED |
| INPUT STB | | P | 13 | OUTPUT STB |
| PARALLEL INPUT BIT 7 | | R | 14 | PARALLEL OUTPUT BIT 7 |
| | 6 | S | 15 | 6 |
| | 5 | T | 16 | 5 |
| | 4 | U | 17 | 4 |
| | 3 | V | 18 | 3 |
| | 2 | W | 19 | 2 |
| | 1 | X | 20 | 1 |
| PARALLEL INPUT BIT 0 | | Y | 21 | PARALLEL OUTPUT BIT 0 |
| DIGITAL GROUND | | Z | 22 | DIGITAL GROUND |

PC BOARD

DIGITAL GROUND

ANALOG GROUND