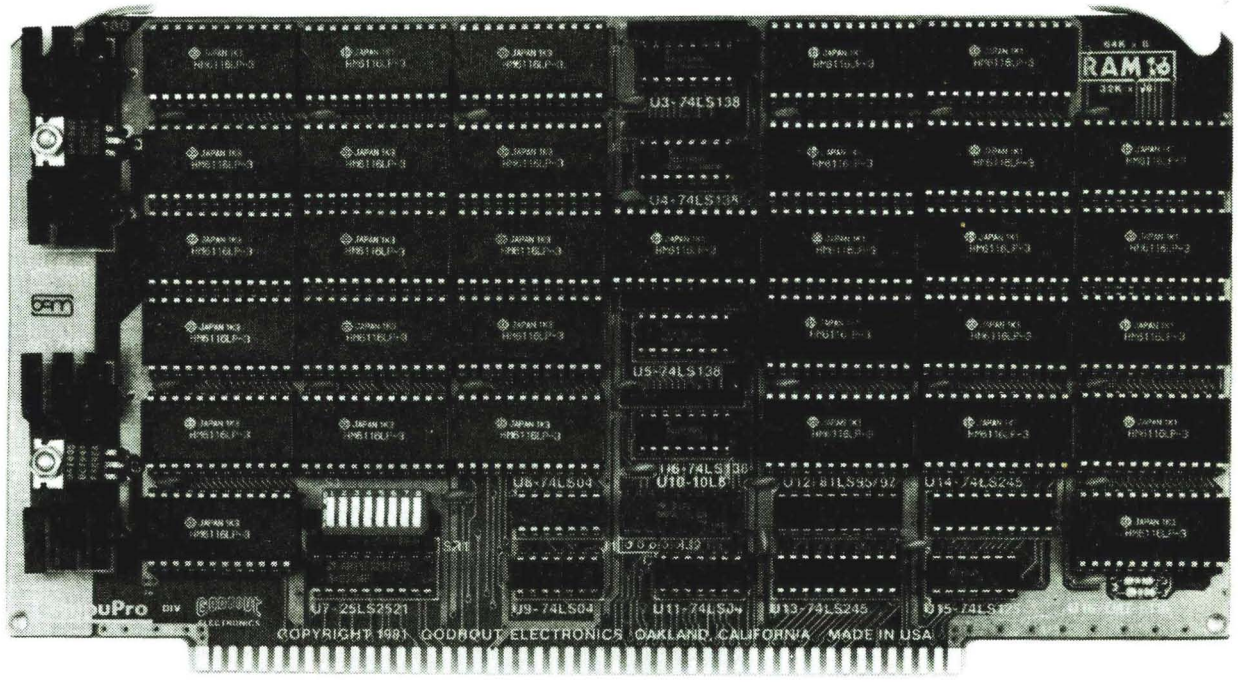
RAM 16™
TECHNICAL MANUAL



IEEE 696 / S-100

STATIC MEMORY
64K x 8 or 32K x16

180A

mac

CompuPro™ SYSTEMS

COMPUPRO division, GODBOUT ELECTRONICS

4/82

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RAM 16 USER MANUAL

ABOUT RAM 16

The RAM 16 from **CompuPro** represents one of the most advanced RAM boards ever produced for the IEEE 696/S-100 Bus. Combining state-of-the-art static CMOS RAM technology with **CompuPro's** design excellence makes the RAM 16 the most versatile, efficient and reliable RAM available today. The RAM 16 works as a "byte-wide" memory in 8 bit systems and automatically switches to "word-wide" mode for today's newer 16 bit systems. The RAM 16 is the choice of professionals for scientific, industrial and commercial applications where the emphasis is on full speed operation with the advanced CPUs of today and tomorrow while maintaining downward compatibility with 8 bit CPUs.

TECHNICAL OVERVIEW

The RAM 16 uses thirty-two of the 6116 CMOS RAM chips to provide a total of 64K bytes or 32K words of storage. The RAM 16 is addressable on any 64K byte boundary in the 16 megabyte address space as specified by the IEEE 696 standard.

The RAM 16 also dynamically switches between "byte-wide" or "word-wide" modes per the state of the sXTRQ* signal on the S-100 Bus (see the Theory of Operation section for a complete discussion of how this protocol works).

The RAM 16 was designed to work with 8086/88 type processors at speeds exceeding 10 MHz. It also handles DMA flawlessly, a feature few 64K boards can boast.

To reduce the number of support ICs required to pack all this function and capacity onto a standard height S-100 board, a PAL (programmable-array-logic) element was used. The PAL selects the proper memory chip or chips and controls the complicated data bus switching scheme required to mix 8 and 16 bit operations.

All of this goes onto a high-quality double-sided circuit board that has a full solder-mask and silk-screened component legend. Sockets are provided for all ICs for ease of maintenance.

IMPORTANT NOTE: Due to the critical timing requirements of the 6 MHz CPU-Z and the internal architecture of the RAM 16 being optimized for 16 bit CPU's, a memory request wait state (S1-3) may be required when running this board at 6 MHz with the CPU-Z. This board will run fine with 8 MHz 8085 and 10 MHz 8088 or 8086 type CPU's without wait states.

HOW TO CONFIGURE THE RAM 16 FOR YOUR SYSTEM

The RAM 16 has only one user selectable option, and that is the address of the board in memory. This board responds to the upper eight address lines (A16-23) as provided for by the IEEE 696/S-100 standard.

The starting address of the board is selected by the setting of the eight paddles of dip-switch S1. S1 is located near the bottom left-hand corner of the board. The address is set in a binary fashion with each paddle of S1 representing an address bit. An "ON" paddle represents a binary "zero" and an "OFF" paddle represents a binary "one". The paddle to address bit relationship is shown in the following table:

SWITCH SETTINGS FOR S1 - ADDRESS SELECTION

ADDRESS BIT	PADDLE NUMBER	
A23	1	
A22	2	
A23	3	ON = 0
A20	4	
A19	5	OFF - 1
A18	6	
A17	7	
A16	8	

EXAMPLE: If this is the first RAM board in your system and you want 64K starting at address 000000H, set all the paddles of S1 ON.

EXAMPLE: If this is the second 64K board in the above system and you want it addressed at 010000H set paddles 1 through 7 ON and paddle 8 OFF.

EXAMPLE: If you want this board to reside at the top of the first megabyte of address space (i.e., starting address 0F0000H), set paddles 1 through 4 ON and paddles 5 through 8 OFF. Incidentally, this would put the board at the hightest 64K address which an 8086 or an 8088 can directly address.

LOCATING RAM IC'S FROM THEIR ADDRESS

The COMPONENT LAYOUT at the back of this manual may be used as a map to locate 6116 RAM IC's by address. The 32 RAM IC's marked 16 to 47 each have a unique label ranging from 0 through F EVEN and 0 through F ODD. The first character of this label indicates the most significant hex digit of the address controlled by that IC, while EVEN and ODD indicate that the last bit of the address is low or high respectively.

EXAMPLE: IC 19 controls even addresses XX2000 through XX2FFE.
EXAMPLE: IC 36 controls odd addresses XXD001 through XXDFFF.
EXAMPLE: Address XXE800 is controlled by IC 44.
EXAMPLE: Address XX024B is controlled by IC 28.

THEORY OF OPERATION

The RAM 16 is designed to work in 8 and 16 bit systems per the protocol established by the IEEE 696/S-100 standard. This works by using the DATA IN and DATA OUT buses as a bidirectional 16 bit data path when a word access is requested. The two buses remain uni-directional during byte operations.

Here's how the protocol works: If the master desires a 16 bit transfer, it requests one by pulling the sXTRQ* (line 58) low. If the slave (in this case the RAM 16) is capable of accepting or providing 16 bit data, it acknowledges this fact to the master by asserting SIXTN* (line 60) low. The master then transfers the data 16 bits at a time. If the slave is incapable of transferring 16 bit data, it does not assert SIXTN* and the master conducts the transfer "byte-serial", which means two consecutive 8 bit transfers.

Sometimes, even a 16 bit master may only want to transfer one byte rather than a whole word. In this case, the master does not assert sXTRQ* but instead uses the data buses as an 8 bit master would, that is: data from the master would be transferred on the DO bus and data to the master would be transferred on the DI bus.

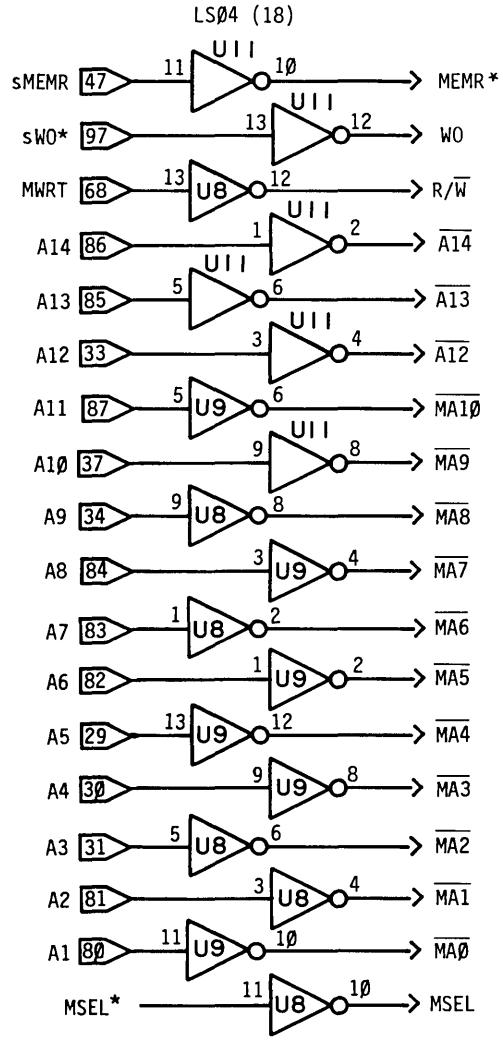
The RAM 16 handles this multiplexing of the data buses with two bi-directional bus buffers (U13 and U14) and a third intermediate buffer (U12). If a 16 bit transfer is occurring, both U13 and U14 are enabled. If a byte write transfer is occurring with A0=0, U13 is enabled and U12 and U14 are disabled. If a byte write transfer is occurring with A0=1, then U13 and U12 are enabled and U14 is disabled. If a byte read transfer is occurring with A0=0, then U14 and U12 are enabled while U13 is disabled. If a byte read transfer is occurring with A0=1, then U14 is enabled with both U12 and U13 disabled.

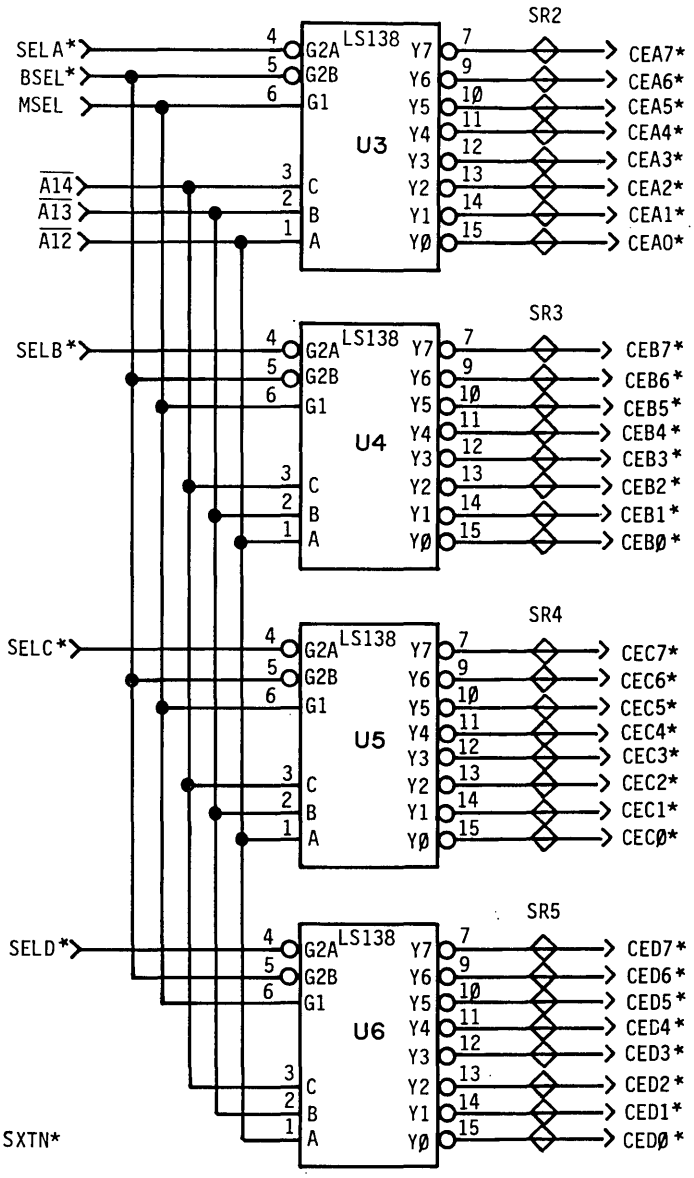
This complicated algorithm is executed by the 10L8 PAL (programmable array logic) element (U10). The PAL also selects the proper RAM chip or chips depending on whether 8 or 16 bits of data are required. The RAM array is configured as four blocks of 16K by 8 bits. They are blocks A, B, C, and D. The A and C blocks are the "even" data bits (those corresponding to A0=0) and the B and D blocks are the "odd" data bits (corresponding to A0=1). For a 16 bit transfer either A and B blocks or C and D blocks are enabled (which set depends on whether A15 is high or low). Only one block is enabled at a time for 8 bit transfers depending on A0 and A15. The PAL also controls the block enables on the SELA-SELD outputs. These outputs go to one of four 74LS138 decoder ICs (U3-6) that select one 2K chip in each 16K block.

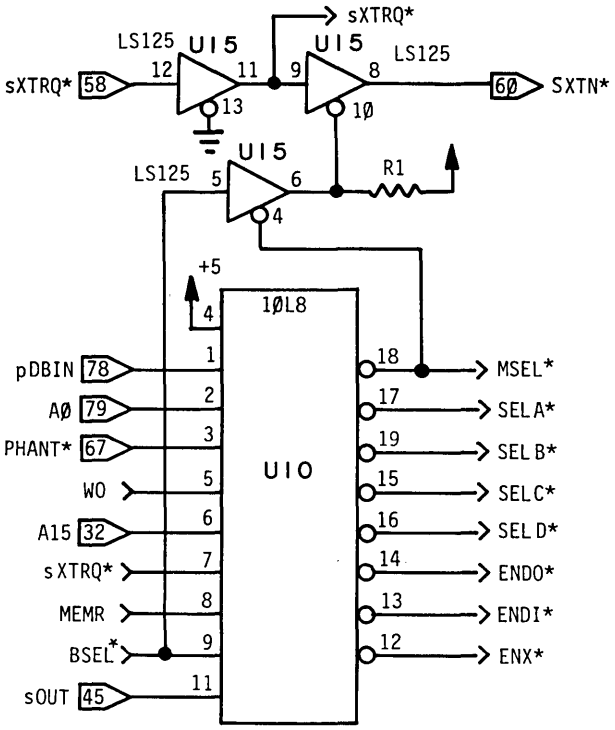
The base address of the board is set with dip-switch S1 and a 25LS2521 octal comparator (U7) and forms the BSEL* signal.

MSEL is a signal from the PAL that signifies a memory cycle is occurring. When both MSEL* and BSEL* are active (low) U15 pin 6 will go low allowing the sXTRQ* signal to assert SIXTN*, telling the master that a 16 bit transfer is possible.

USER NOTES







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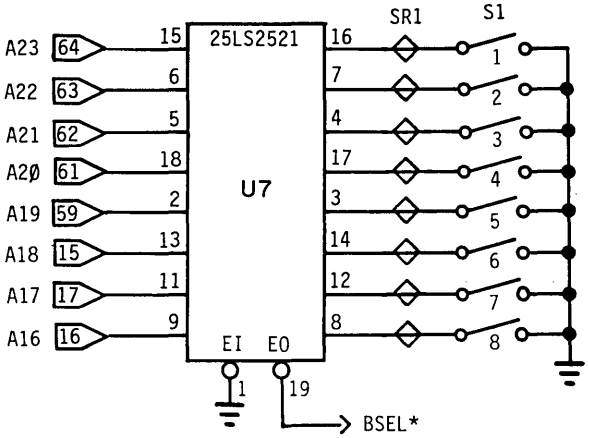

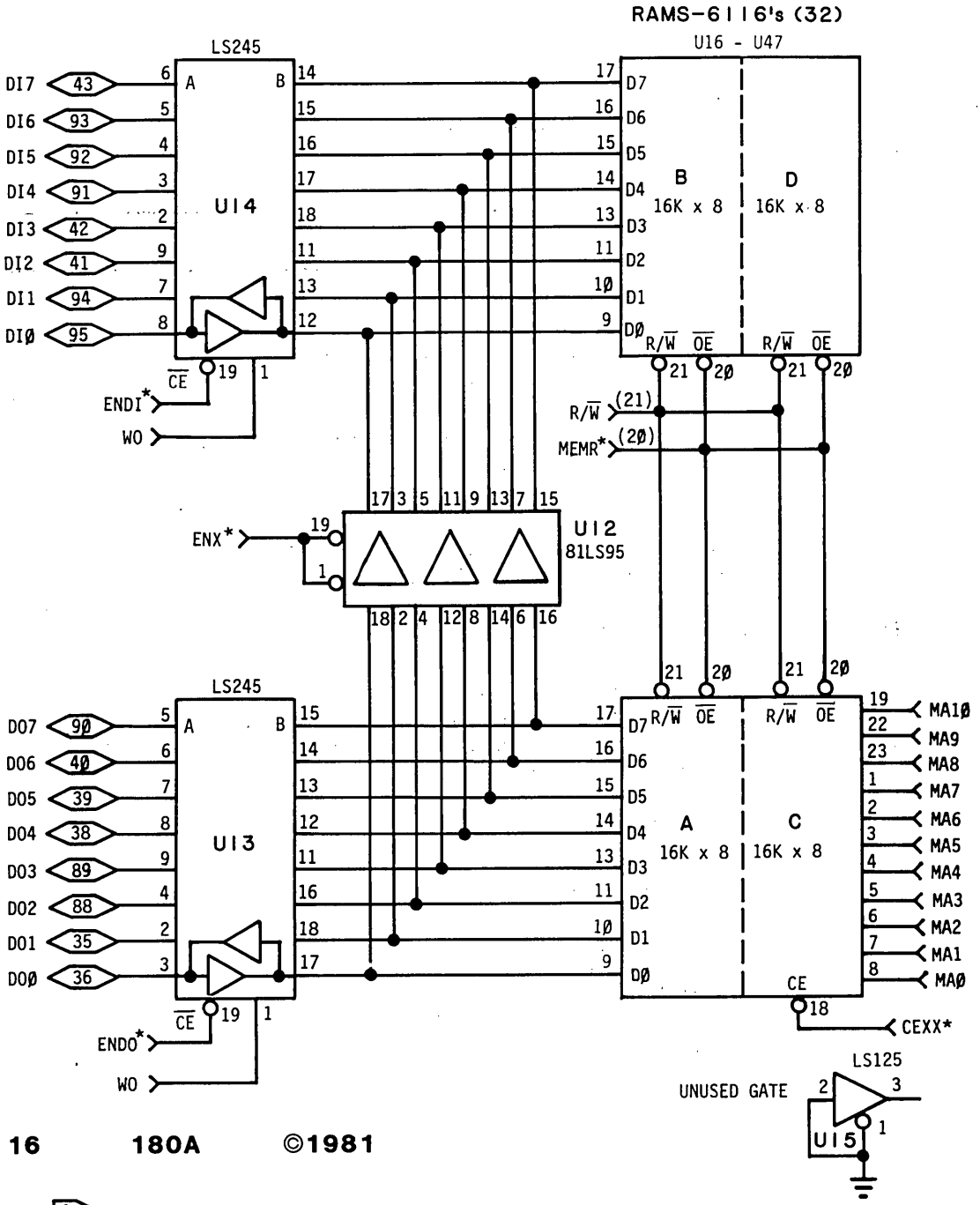

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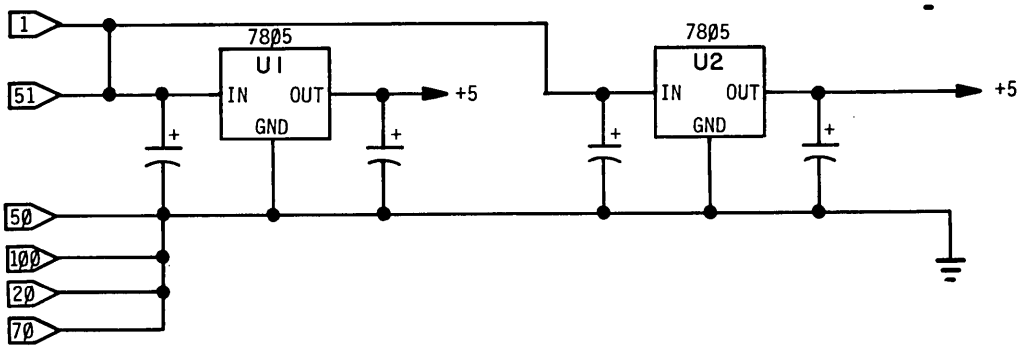
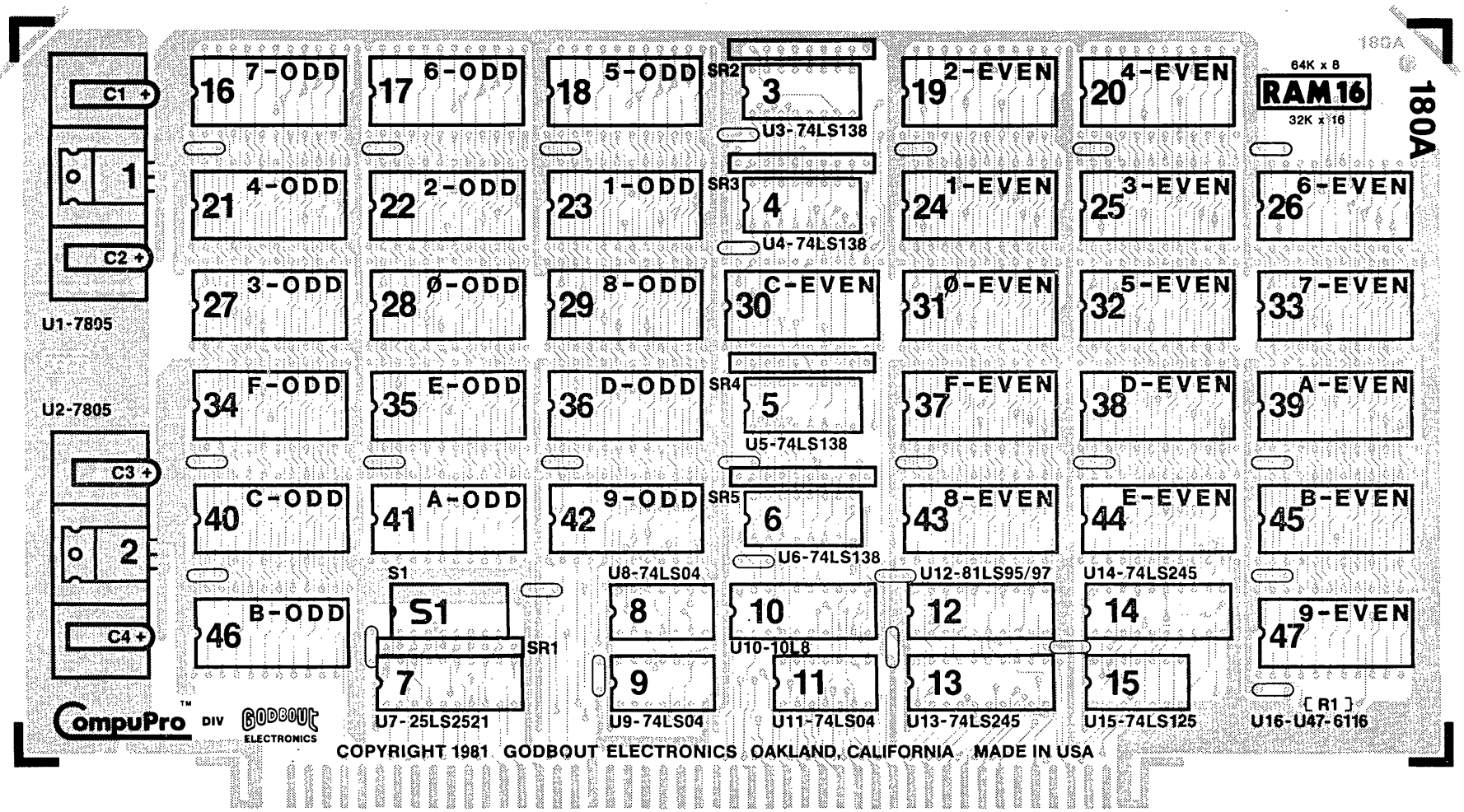


PARTS LIST

QTY	DESCRIPTION
SEMICONDUCTORS	
3	74LS04 Hex Inverter (U8,9,11)
1	74LS125A Quad Bus Driver (U15)
4	74LS138 One-of-eight Decoder (U3-6)
2	74LS245 Octal Bus Transceiver (U13,14)
1	81LS95/97 Octal Bus Buffer (U12)
1	25LS2521 Octal Comparator (U7)
1	10L8 PAL - G182 (U10)
32	HM6116 CMOS RAM or equivalent (U16-47)
2	7805 +5V Regulators (U1,2)
OTHER ELECTRICAL COMPONENTS	
1	4.7K Ohm Resistor (R1)
5	4.7K or 5.1K Ohm Resistor Pack - 10 pin (SR1-5)
4	Tantalum Axial Capacitors - 10V or higher (C1-4)
25	Bypass Capacitors
MECHANICAL COMPONENTS	
1	8 Position DIP Switch
2	Heatsinks
2	6-32x3/8" Screws
2	6-32 Hex Head Nuts
2	Lockwashers
2	Card Ejectors
1	PC Board #180



COMPONENT LAYOUT

IF YOU NEED ASSISTANCE ALWAYS CONTACT
YOUR **COMPUPRO DEALER FIRST**

CUSTOMER SERVICE INFORMATION

Our paramount concern is that you be satisfied with any Godbout CompuPro product. If this product fails to operate properly, it may be returned to us for service; see warranty information below.

If you need further information feel free to write us at:

Box 2355, Oakland Airport, CA 94614-0355

LIMITED WARRANTY INFORMATION

Godbout Electronics will repair or replace, at our option, any parts found to be defective in either materials or workmanship for a period of 1 year from date of invoice. Defective parts *MUST* be returned for replacement.

If a defective part causes a Godbout Electronics product to operate improperly during the 1 year warranty period, we will service it free (original owner only) if delivered and shipped at owner's expense to and from Godbout Electronics. If improper operation is due to an error or errors on the part of the purchaser, there may be a repair charge. Purchaser will be notified if this charge exceeds $50.00.

We are not responsible for damage caused by the use of solder intended for purposes other than electronic equipment construction, failure to follow printed instructions, misuse or abuse, unauthorized modifications, use of our products in applications other than those intended by Godbout Electronics, theft, fire, or accidents.

Return to purchaser of a fully functioning unit meeting all advertised specifications in effect as of date of purchase is considered to be complete fulfillment of all warranty obligations assumed by Godbout Electronics. This warranty covers only products marketed by Godbout Electronics and does not cover other equipment used in conjunction with said products. We are not responsible for incidental or consequential damages.

Prices and specifications are subject to change without notice, owing to the volatile nature and pricing structure of the electronics industry.

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