QED-1

User's Information Manual

Revision 2.0

NOTE: ALL OF CLEARPOINT'S PRODUCTS ARE TESTED PRIOR TO SHIPMENT; FAILURES IN THE FIELD ARE LARGELY ATTRIBUTED TO COMPONENT FAILURE CAUSED BY HANDLING. PLEASE VERIFY THAT ALL NECESSARY PRECAUTIONS ARE TAKEN DURING INSTALLATION, SPECIFICALLY PROTECTION FROM ELECTRO-STATIC DISCHARGE (ESD).

CONTENTS

CHAPTER 1

GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

This manual supplies user information for the QED-1 family of memory modules. The QED-1 provides high density, low cost-per-bit storage for systems based upon the Digital Equipment Corporation Q-Bus and PMI-Bus. Using 256K DRAM technology, the board has a capacity of 4 MB, and is available in 2 and 4 MB configurations. Using 64K DRAM technology the board is available in 1 MB. The single quad-height module has the following features:

1.2 GENERAL DESCRIPTION

The QED-1 is a single quad-height memory module which interfaces to the LSI -11 Q-Bus and also the augmented Q-Bus (PMI-Bus) for the PDP 11/83 and 11/ 84. All timing and control logic for the memory, refresh circuitry, Error Detection and Correction (EDC), and Control Status Register (CSR) are contained on board.

The QED-1 is the first implementation of the Clearpoint EDC chip set, a CMOS VLSI semi-custom design that allows EDC with a cost and performance typical of parity memory. The chip set uses a 64 bit word with a 10 bit Error Correction Code. The major benefit of the 64 bit word is that there is effectively a four word cache in the chip set. Even though EDC takes longer than parity checking on the first word of a read or write, the subsequent three words can be read directly from the cache with a very fast access time. In most applications, this allows EDC to occur with little or no performance degradation.

The MOS memory array consists of 2 rows of 256K X 1 DRAM devices with 74 devices per row. Circuitry for refresh of the MOS memory devices is provided on board and operates transparently to the user. The QED-1 module's starting address is selectable using program plugs P6 to P9 (see figure 1). The QED-1 is designed for use with 22-bit addressing.

1.3 FEATURES

1. Completely hardware and software compatible with the MSV11-XX line of DEC memories.

2. Error Detection and Correction -- Single bit error correction and double bit error detection. Performs true EDC on writes as well as error scrubbing.

3. Four word cache memory for very fast average access time.

4. Runs all DEC memory diagnostics, including parity memory diagnostics (VMSAA0 and ZMSP0).

5. Bank select option allows addressability on the Q-Bus to expand to over 60 MB.

6. Selectable ending address or address gap (Windowing up to 1 MB) for reserved address space, to allow for memory-mapped peripherals.

7. Addressable at any modulo 256K starting address.

8. Access Times:

   - 60 ns match read time
   - 130 ns match write time
   - 310 ns non-match read time
   - 80 ns non-match write time

9. Cycle times:

   - 580 ns match read time
   - 650 ns match write time
   - 750 ns non-match read time
   - 1050 ns non-match write time

10. Full PMI-Bus compatibility -- for the PDP 11/84 and 11/83

11. Full Q-Bus compatibility -- for the PDP 11/73, 11/23, VAXstation I and MicroVAX I.

12. Battery back-up support.

1.4 SPECIFICATIONS

Characteristics	Specifications
memory device types	MOS dynamic RAM 256K X 1, 150 ns 64K X 1, 150 ns
read access time--cache hit	85 ns
--cache miss	255 ns
--average (2:1)	142 ns
write access time--cache hit	65 ns
--cache miss	145 ns
--average (2:1)	92 ns
operating temperature	0 to +65 C
storage temperature	-40 to +85 C
relative humidity	0 to 90% (non-condensing)
voltages required	+5V +/- 5%
battery backup voltage	+5V +/- 5%
+5V operating current	3.2 Amps typical 4.25 Amps maximum
+5V stand-by current	2.8 Amps typical 3.75 Amps maximum
+5V battery backup current	.75 Amps typical 1.0 Amps maximum

BOARD SIZING:

1MB--64K DRAMS P00 P01

2MB-256K DRAMS P00 P01

4MB-256K DRAMS P00 P01

STARTING ADDRESSES:

000KB P06 P07 P08 P09

256KB P06 P07 P08 P09

512KB P06 P07 P08 P09

1MB P06 P07 P08 P09

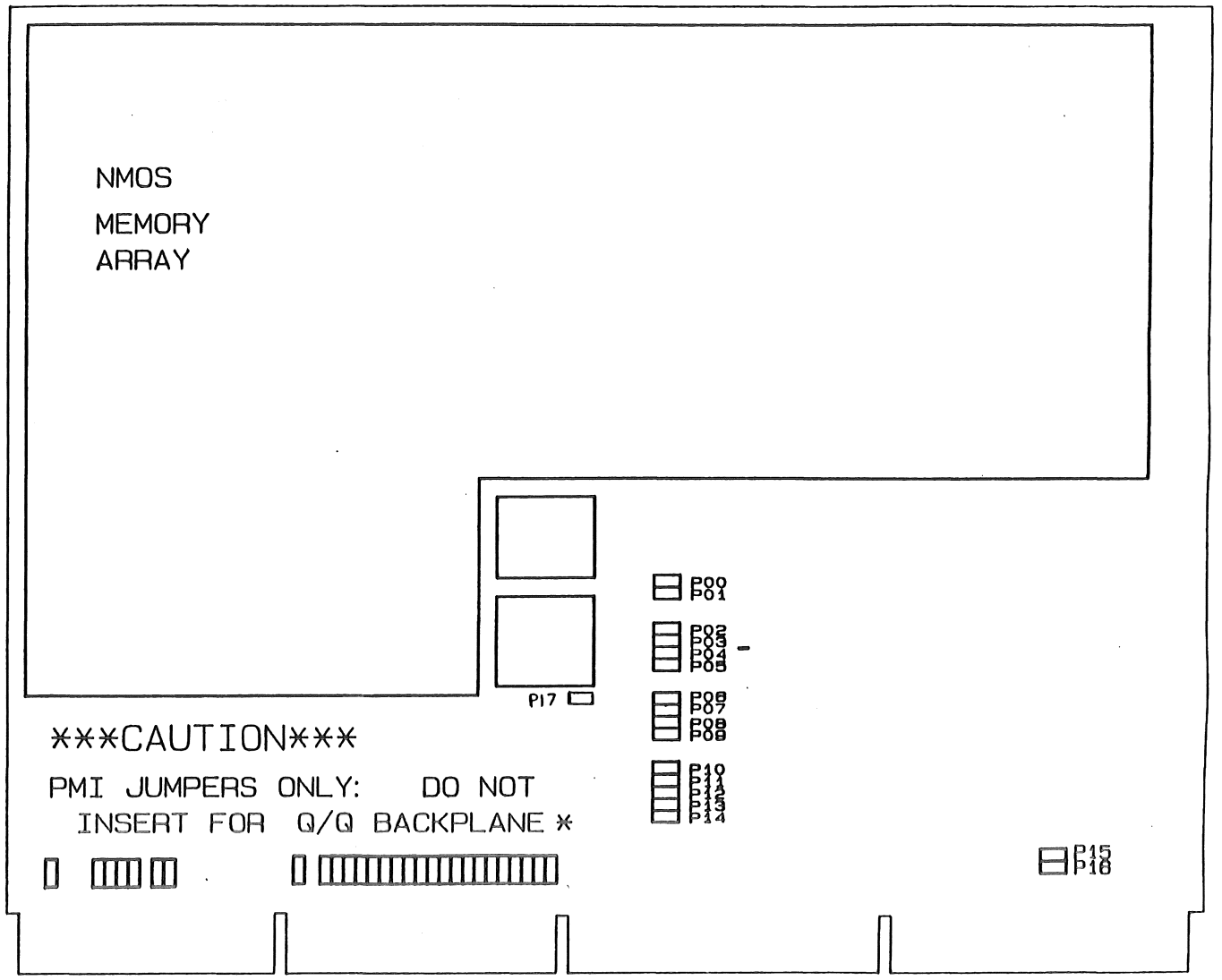
2MB P06 P07 P08 P09

CSR ADDRESSES:

7772100 P02 P03 P04 P05

7772102 P02 P03 P04 P05

7772136 P02 P03 P04 P05



1.4.1 FIGURE 1 - QED-1 Jumper Plug Identification

1.5 BACKPLANE PIN UTILIZATION

Table 1 contains backplane power pins required for the QED-1. Table 2 designates pins used for other signals. Board finger designations shown in Table 1 and 2 are equivalent to backplane pin designations.

1.5.1 TABLE 1 - Backplane Power Pins Required

VOLTAGE	PIN
+5 normal	BV1
	AA2
	BA2
ground	AT1
	BT1
	AC2
	BC2
+5 battery (if used)	AV1

1.5.2 TABLE 2 - Backplane I/O Signal Pins

Signal	Pin
AC1	BDAL 16 L
AD1	BDAL 17 L
BA1	BDCOK H
BC1	BDAL 18 L
BD1	BDAL 19 L
BE1	BDAL 20 L
BF1	BDAL 21 L
AE2	BDOUT L
AF2	BRPLY L
AH2	BDIN L
AJ2	BSYNC L
AK2	BWTBT L
AM2	BIAKI L
AN2	BIAKO L
AP2	BBS7 L
AR2	BDMGI L
AS2	BSMGO L
AU2	BDAL 00 L
AV2	BDAL 01 L
BE2	BDAL 02 L
BF2	BDAL 03 L
BH2	BDAL 04 L
BJ2	BDAL 05 L
BK2	BDAL 06 L
BL2	BDAL 07 L
BM2	BDAL 08 L
BN2	BDAL 09 L
BP2	BDAL 10 L
BR2	BDAL 11 L
BS2	BDAL 12 L
BT2	BDAL 13 L
BU2	BDAL 14 L
BV2	BDAL 15 L

TABLE 2 Continued

PMI-Bus Signal Pins	
Signal	Pin
CB1	PSSEL L
CD1	PUBMEM L
CE1	PBCYC L
CF1	PUBSYS L
CH1	PHBPAR L
CJ1	PSBFUL L
CK1	PLBPAR L
CM1	PRDSTB L
CP1	PBLKM L
CR1	PBSY L
CV1	PUBTMO L
DB1	PWTSTB L
DC1	PBYT L

CHAPTER 2

HARDWARE INSPECTION, INSTALLATION, AND CHECKOUT

2.1 INTRODUCTION

This chapter provides information for configuring the QED-1 programmable plug options prior to system installation followed by installation and checkout procedures.

VERY IMPORTANT - READ THIS FIRST

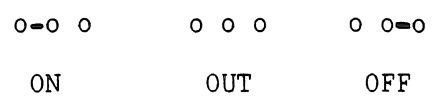
Before installation, it is very important to determine the type of backplane into which this board is to be inserted. Many backplanes currently in use are of the Q/Q variety. Q/Q backplanes repeat the A/B connectors on both sides of the quad slots. If the QED-1 is to be used in a Q/Q backplane the PMI Option Jumpers MUST BE REMOVED or damage to the system may occur. The PMI Option Jumpers are the 28 jumpers directly above the gold fingers on the left side of the board. When the QED-1 is used in a PMI-Bus system (with the necessary QCD slots) these jumpers should remain in place.

Note: the MicroVAX I is not a PMI-Bus system, even though the backplane has 3 QCD slots. The PMI-Bus Option Jumpers MUST BE REMOVED for the MicroVAX I.

2.2 CONFIGURING THE QED-1 PROGRAM PLUGS

Figure 2 provides the program plug settings of the various QED-1 option jumpers. Left and Right refer to the position of the jumpers when the board is faced, gold fingers pointing down. The module should be inspected prior to installation to assure that it has been properly configured. The sections below describe the various QED-1 program plug options.

2.2.1 FIGURE 2 - QED-1 Program Plug Settings



2.3 ADDRESSING AND BOARD SIZING OPTIONS

The memory starting address may be programmed to any 256K boundary using jumpers P0 through P3. Depending on the size of the board, the memory will utilize up to 4 megabyte (MB) addresses in the address space beginning at the selected starting address. The QED-1 can be sized to 512KB, 1 MB, 2 MB, 3 MB or 4 MB. The basic size options handled by the P0 and P1 plugs are 1, 2 and 4 MB. Other configurations use the Memory Window jumpers P10 through P14.

2.3.1 TABLE 3 - Board Size Options

Board Memory Capacity	P0	P1
1 MB (64K DRAMs)	Right	Right
2 MB (256K DRAMs)	Right	Left
4 MB (256K DRAMs)	Left	Left

2.3.2 TABLE 4 - Setting The Starting Address

Use the following table to configure the starting address over resident memory:

STARTING ADDRESS: BYTES	OCTAL ADDRESS	P09	P08	P07	P06
0	0000000	Left	Left	Left	Left
256K	1000000	Right	Left	Left	Left
512K	2000000	Left	Right	Left	Left
768K	3000000	Right	Right	Left	Left
1M	4000000	Left	Left	Right	Left
1.25M	5000000	Right	Left	Right	Left
1.5M	6000000	Left	Right	Right	Left
1.75M	7000000	Right	Right	Right	Left
2M	10000000	Left	Left	Left	Right
2.25M	11000000	Right	Left	Left	Right
2.5M	12000000	Left	Right	Left	Right
2.75M	13000000	Right	Right	Left	Right
3M	14000000	Left	Left	Right	Right
3.25M	15000000	Right	Left	Right	Right
3.5M	16000000	Left	Right	Right	Right
3.75M	17000000	Right	Right	Right	Right

2.4 RESERVED I/O PAGE SPACE

The BBS7 signal is used during the address portion of a data transfer cycle on the Q-Bus. It indicates that the bus master is requesting a data transfer with one of the I/O devices in the 4K I/O page space. This space is reserved at the top of the 4MB address range (Octal Address 17774000). BBS7 is asserted whenever an I/O page transfer is requested. The memory board will ignore all transfers requested within the I/O space.

2.5 MEMORY WINDOW OPTIONS

The QED-1 provides a "memory window" option to allow for the use of memory-mapped peripherals with a reserved address space. The windowing option also enables unusual board sizing, such as 3.5 MB or 3 MB. The same jumpers are also used by the bank select feature,

which allows direct addressing beyond the 22-bit limitation of 4 MB. The bank select feature is detailed in Appendix 2.

Program plugs P10-P14 are used for these features. P10 determines which of the various options is being used. If P10 is removed, windowing and bank select are not in use. If P10 is in and to the Right, windowing is enabled. (P10 to the Right also enables bank select, implying that this is the base board of a bank of boards. P10 to the Left implies that this is a paged board among a bank of boards. For more detail on the bank select feature, see Appendix 2.)

If P10 is in and to the Right, then P11-P14 are used to specify both the size and the location of the memory window.

2.5.1 TABLE 5 - Window Option Starting Address

Program Plug	Address Line	Example
P11	A21	Left
P12	A20	Right
P13	A19	Left
P14	A18	Right

2.5.2 Specifying A 256 KB Window

Simply using all of plugs P11-P14 implies a 256 KB window. The position of these plugs is then used to specify the starting address of the window. The address correspondence is as follows:

All jumpers to the Right would imply a 256 KB window starting at address 0. P14 to the Left and P11-P13 to the Right would imply a 256 KB window starting at address 256 KB, and so forth. In the above example, there would be a 256 KB window starting at address 2.5 MB.

2.5.3 Specifying A 512 KB Window

A 512 KB window is implied by the removal of plug P14. In this case, plugs P11-P13 are used to specify the starting address. The correspondence is the same as above (with a 256 KB window). For example, P11 to the Right, P12 to the Left, P13 to the Right and P14 out would imply a 512 KB window starting at address 1 MB.

2.5.4 Specifying A 1 MB Window

A 1 MB window is specified by removing plugs P13 and P14. P11 and P12 are then used to specify the starting address of the 1 MB window. For example, P11 and P12 to the Left, and P13 and P14 removed would imply a 1 MB window starting at address 3 MB; this is equivalent to a 3 MB board with no window.

2.6 CSR AND EDC OPERATION

The QED-1 offers Error Detection and Correction (EDC) completely transparently to the user. To all software, the QED-1 appears to be a parity memory with a Control and Status Register (CSR) assigned for parity support. For more information on the CSR and EDC operation, see chapter 3.

2.7 CSR OPTION PLUG CONFIGURATION

The Control and Status Register has an I/O page address in the top 4K of memory. This address may be any one of 16 specified locations reserved by DEC for this purpose. Program plugs P2, P3, P4, and P5 are used to select one of the reserved addresses. Table 6 illustrates the use of these plugs. Note that each memory board used in a system must be configured to a different address.

2.7.1 TABLE 6 - CSR Configurations

CSR Address	P2	P3	P4	P5
772100	Left	Left	Left	Left
772102	Left	Left	Left	Right
772104	Left	Left	Right	Left
772106	Left	Left	Right	Right
772110	Left	Right	Left	Left
772112	Left	Right	Left	Right
772114	Left	Right	Right	Left
772116	Left	Right	Right	Right
772120	Right	Left	Left	Left
772122	Right	Left	Left	Right
772124	Right	Left	Right	Left
772126	Right	Left	Right	Right
772130	Right	Right	Left	Left
772132	Right	Right	Left	Right
772134	Right	Right	Right	Left
772136	Right	Right	Right	Right

2.8 BATTERY BACKUP OPTION PLUGS

MOS memory requires the 5 volt supply to retain data. If for any reason power is interrupted, system memory data will be lost. In order to maintain data during power failures, the QED-1 has a battery backup option to sustain power on pin AV1. P15 and P16 should be configured as follows:

2.8.1 TABLE 7 - Battery Backup Mode Options

Battery Backup Mode	P15	P16
No Battery Backup	Left	Left
Battery Backup +5V AV1	Right	Right

2.9 INSTALLATION PROCEDURE

Prior to installation, determine whether the backplane the QED-1 is to be inserted into is a Q/Q or QCD type backplane. Q/Q backplanes only use the AB connectors and repeat the AB bus signals on both sides of a quad-height backplane. QCD backplanes typically have the first 2 or 3 slots with PMI-Bus compatibility; the PMI-Bus uses the CD connectors for additional signals. The remaining slots in these systems are usually Q/Q to allow the use of standard Q-Bus devices.

The PDP 11/73+ is the PMI-Bus compatible processor; the PDP 11/84 and 11/83 are PMI-Bus compatible systems. Installation of these types of systems is slot dependent, unlike the standard Q-Bus. These instructions must be followed exactly or the system will not function with the PMI-Bus, and damage to the system may result. If the system to be used is standard Q-Bus (PDP 11/23, 11/73 or MicroVAX I), skip to section 2.10.

2.10 PMI-BUS COMPATIBLE SYSTEM INSTALLATION

There are two types of PMI-Bus system. The PDP 11/84 has a 5 slot QCD backplane and an 8 slot UNIBUS backplane. The QCD slots should be utilized as follows:

Slot 1 -- Console Board; Part Number M7677
Slot 2 -- CPU; Part Number KDJ11-BF
Slot 3 -- Memory
Slot 4 -- Memory or other PMI device
Slot 5 -- UBA (UNIBUS to Q-Bus Adapter)
Part Number M8191

PDP 11/83 and 11/73+ processors can be used in systems with 2 or more QCD slots. In a 2 slot system the positions should be:

Slot 1 -- Memory
Slot 2 -- CPU; KDJ11 BC or BF

In a three slot QCD backplane the positions should be:

Slot 1 -- Memory
Slot 2 -- CPU
Slot 3 -- Any Q/Q device with no CD connections

or:

Slot 1 -- Memory or other PMI device
Slot 2 -- Memory
Slot 3 -- CPU

2.11 Q-BUS INSTALLATION PROCEDURE

The following procedure should be followed when a QED-1 board is received:

1. Visually inspect the module to make sure that it has arrived in good condition.

2. Set up program plug options for required operation.

3. Verify that the required power connections are available on the backplane (see Table 2).

4. Power down the system. Make sure that the system is powered off before plugging in the module.

5. Plug the module into the Q-BUS. Some DEC literature suggests that memories be installed in sequential slots following the CPU. However anyplace in the backplane is sufficient. Do make sure that the module is not being inserted backwards; the component side must face in the same direction as other modules in the system.

6. Power up the system and run any DEC memory diagnostic as an initial test. If available, use the following diagnostics:

   1. MAINDEC-11 CVMSA (22 bit system diagnostic)

2. MAINDEC-11 CZKMA (18 bit system diagnostic)

2.12 LED INTERPRETATION

The QED-1 has three Light Emitting Diodes (LEDs) for quick interpretation of the status of the board. The Red LED indicates that a double bit or multiple bit error has occurred. The Yellow LED indicates that a single bit error has occurred since the last BUS INIT. The Green LED indicates that initialization of the memory is complete and that operation is normal. During normal operation, the green light should always remain on.

2.13 VERIFICATION OF PROPER SYSTEM INSTALLATION

Depending on the type of system this QED-1 is installed in, the normal screen display will vary. Refer to the appropriate system installation guide for the system in use. Proper installation of the QED-1 can always be recognized by the green LED turning on approximately 20 seconds after power on.

CHAPTER 3

CSR AND HYPER-CSR DESCRIPTION

3.1 INTRODUCTION

The QED-1 offers Error Detection and Correction transparently to the software. What this implies is that the QED-1 appears to be a parity memory card to the rest of the system. Parity interrupts are only generated on multiple-bit errors, since single bit errors are corrected on- board. In order for software to utilize the EDC information generated by the QED-1, a CSR and a hyper-CSR are provided. Essentially, the CSR latches the address on an interrupt caused by a multiple-bit error. The hyper-CSR latches the address on any error, single or multiple-bit. For the purpose of error logging single-bit errors without interrupting the system, the hyper-CSR can be read. The hyper-CSR can also be decoded to locate a failing memory chip.

The CSR is assigned an address in the I/O page which may be accessed by software. When a parity error is detected, the upper address bits of the bad memory location (A11 to A21) are latched in the CSR. Control bits are provided in the CSR to enable interrupt on double-bit error and write of bad parity for diagnostic purposes.

3.1.1 TABLE 7 - CSR Bit Assignment

The CSR is a 16 bit register located in the I/O page. The function of the 16 bits in the CSR are as follows:

Bit 0	Parity error interrupt enable If set to 1, the memory board will interrupt the processor on error, by setting bits BDAL 17 and BDAL 16 along with the data bits BDAL 0 to BDAL 15. This will result in an LSI-11 processor trap to location 114. BUS INIT clears this bit. Note that with the QED-1 an interrupt will only occur with an uncorrectable error.
Bit 1	UNUSED
Bit 2	Write wrong parity If this bit is set to 1, any word or byte written to the array will be stored if there is an uncorrectable error. This is for maintenance purposes. It enables diagnostics to check the boards ability to detect errors and interrupt when enabled. This bit is cleared by BUS INIT.
Bit 3	UNUSED
Bit 4	UNUSED
Bit 5 - 11	Latch address bits When an uncorrectable error is detected, the upper address bits of the failing location are latched. These bits are not cleared by BUS INIT, but are writeable, as well as readable. When an error is detected, address bits 11 to 21 are displayed in these bits. Since there are only 7 bits and there are 11 latched address bits, they are multiplexed. Bit 14 in the CSR controls which of the latched address bits are on display. (see Table 8).
Bit 12	UNUSED
Bit 13	UNUSED

Bit 14 Extended CSR read enable

(See Table 8.) This bit is used to multiplex the extended latched address bits A18 to A21 into the CSR bits 5 to 11. This bit is cleared by BUS INIT.

Bit 15 Parity error flag

This bit is set if an uncorrectable error is detected and remains set until cleared by being written or by BUS INIT.

Table 8 - CSR Bit Assignment Summary

CSR BIT	DESCRIPTION
00	Parity error interrupt enable; 1 = interrupt
01	Unused
02	Write wrong parity; 1 = w.w.p.
03	Unused
04	Unused
05 --	
06 -	
07 -	
08 --	Bits 5-11 are Latch Address Bits
09 -	
10 -	
11 --	
12	Unused
13	Unused
14	Extended CSR read enable; see table 8
15	Parity error flag; 1 = error

3.1.2 TABLE 9 - CSR Bits 5 To 11

CSR Bit	CSR BIT 14 = 0	CSR BIT 14 = 1
05	Latched A11	Latched A18
06	Latched A12	Latched A19
07	Latched A13	Latched A20
08	Latched A14	Latched A21
09	Latched A15	0
10	Latched A16	0
11	Latched A17	0

3.2 THE HYPER-CSR

The QED-1 utilizes an additional CSR for control of the Error Detection and Correction features. This additional CSR is called the "hyper-CSR". The hyper-CSR is accessed by writing 777721XX to the CSR, then again writing 777721XX to the CSR a second time, where XX is the CSR register for the board in question. If only one memory board is in the system, this becomes 77772100. (Writing a third time will return to the normal CSR.) This access must be made on two consecutive writes; intervening writes will result in starting over with an access to the normal CSR. The hyper-CSR bits can be decoded as follows:

3.2.1 TABLE 10 - Hyper-CSR Bit Assignment

Hyper-CSR Bit	Description
00 ---	
01 --	
02 --	
03 --	These are the syndrome bits for any
04 --	error, single or multiple bit. If
05 --	there is a multiple bit error the syndrome
06 --	bits correspond to the last error.
07 --	See Table 10 for decoding.
08 --	
09 ---	
10	Row in error; 1 = row 1; 0 = row 2
11	Error type; 1 = double bit, 0 = single bit
12	Interrupt enable; 1 = enable, double bit error*
13	Write bad EDC; 1 = enable
14	Correction enable; 1 = enable
15	Error; 1 = error since last BUS INIT

*EXCEPT if correction enable = 0, then single OR double bit error.

3.2.2 Notes On Use Of The Hyper-CSR

The information in table 10 is only valid if an error has occurred (i.e. if bit 15 = 1). This register will always show the last error that occurred; if previous error has occurred but goes unnoticed and then another error is logged, then the first error will no longer be visible.

Bit 10 (Row latch) is used with the data bits to determine the location of a hard failure. Bit 11 denotes the occurrence of a single or double bit error. If a double bit error or multiple bit error has occurred then the syndrome bits are not likely to contain useful decoding information. Bit 12 is used to enable interrupt on single or double bit errors. To interrupt on single bit errors prior to correction, Bit 14 should be set to 0 (disabled) and Bit 12 should be set to 1 (enabled). Bit 13 is used primarily for diagnostic purposes. Setting Bit 13 to 1 disables the update of the check-bits, which allows insertion of single or multiple bit errors. This is useful for testing the functionality of the EDC logic.

3.3 DECODING THE SYNDROME BITS

The syndrome bits are used to determine the location of a failing data bit. Combined with the Row, these two pieces of information uniquely identify the location of a failure. Syndrome bits 0 to 9 are used in the following table to locate the appropriate data bit. To use the table, begin with the least significant digit to enter the table in the correct column. Then continue iteratively until the correct combination of syndrome bits is found.

Note: if only one syndrome bit is asserted, then the error is in the corresponding check-bit (i.e. a 1 only in syndrome bit 3 implies that check-bit 3 is in error, not a data bit). The syndrome bits only imply a data bit error if 3 syndrome bits are asserted (i.e. = 1).

3.3.1 TABLE 11 - Syndrome Bit Decoding - 1 Bit Asserted

Syndrome Bits (X = asserted)										
1 Bit Asserted										
0	1	2	3	4	5	6	7	8	9	CHECK BIT
X	-	-	-	-	-	-	-	-	-	00
-	X	-	-	-	-	-	-	-	-	01
-	-	X	-	-	-	-	-	-	-	02
-	-	-	X	-	-	-	-	-	-	03
-	-	-	-	X	-	-	-	-	-	04
-	-	-	-	-	X	-	-	-	-	05
-	-	-	-	-	-	X	-	-	-	06
-	-	-	-	-	-	-	X	-	-	07
-	-	-	-	-	-	-	-	X	-	08
-	-	-	-	-	-	-	-	-	X	09

3.3.2 TABLE 12 - Syndrome Bit Decoding - 3 Bits Asserted

3 Bits Asserted										
0	1	2	3	4	5	6	7	8	9	DATA BIT
X	X	X	-	-	-	-	-	-	-	08
X	X	-	X	-	-	-	-	-	-	09
X	X	-	-	X	-	-	-	-	-	00
X	X	-	-	-	X	-	-	-	-	01
X	X	-	-	-	-	X	-	-	-	13
X	X	-	-	-	-	-	X	-	-	14
X	X	-	-	-	-	-	-	X	-	07
X	-	X	X	-	-	-	-	-	-	16
X	-	X	-	X	-	-	-	-	-	17
X	-	X	-	-	X	-	-	-	-	02
X	-	X	-	-	-	X	-	-	-	48
X	-	X	-	-	-	-	X	-	-	03
X	-	-	X	X	-	-	-	-	-	24
X	-	-	X	-	X	-	-	-	-	25
X	-	-	X	-	-	X	-	-	-	04
X	-	-	X	-	-	-	X	-	-	05
X	-	-	-	X	X	-	-	-	-	32
X	-	-	-	X	-	X	-	-	-	06
X	-	-	-	X	-	-	X	-	-	33
X	-	-	-	-	X	X	-	-	-	40
X	-	-	-	-	X	-	X	-	-	41
X	-	-	-	-	-	X	X	-	-	56
X	-	-	-	-	-	X	-	X	-	55
-	X	X	X	-	-	-	-	-	-	10
-	X	X	-	X	-	-	-	-	-	34
-	X	X	-	-	X	-	-	-	-	18
-	X	X	-	-	-	X	-	-	-	19
-	X	X	-	-	-	-	X	-	-	57
-	X	X	-	-	-	-	-	X	-	15
-	X	-	X	X	-	-	-	-	-	35
-	X	-	X	-	X	-	-	-	-	42
-	X	-	X	-	-	X	-	-	-	26
-	X	-	X	-	-	-	X	-	-	27
-	X	-	-	X	X	-	-	-	-	43
-	X	-	-	X	-	X	-	-	-	49
-	X	-	-	X	-	-	X	-	-	58
-	X	-	-	-	X	X	-	-	-	50
-	X	-	-	-	X	-	X	-	-	11
-	X	-	-	-	-	X	X	-	-	12

3.3.3 TABLE 13 - Syndrome Bit Decoding

Syndrome Bits (X = asserted)										
0	1	2	3	4	5	6	7	8	9	DATA BIT
-	-	X	X	X	-	-	-	-	-	36
-	-	X	X	-	X	-	-	-	-	28
-	-	X	X	-	-	X	-	-	-	20
-	-	X	X	-	-	-	X	-	-	21
-	-	X	-	X	X	-	-	-	-	22
-	-	X	-	X	-	X	-	-	-	51
-	-	X	-	X	-	-	X	-	-	60
-	-	X	-	-	X	X	-	-	-	44
-	-	X	-	-	X	-	X	-	-	45
-	-	X	-	-	X	-	-	X	-	23
-	-	X	-	-	-	X	X	-	-	59
-	-	-	X	X	X	-	-	-	-	29
-	-	-	X	X	-	X	-	-	-	30
-	-	-	X	X	-	-	X	-	-	37
-	-	-	X	X	-	-	-	X	-	31
-	-	-	X	-	X	X	-	-	-	53
-	-	-	X	-	X	-	X	-	-	61
-	-	-	X	-	-	X	X	-	-	52
-	-	-	X	-	-	-	X	X	-	63
-	-	-	-	X	X	X	-	-	-	38
-	-	-	-	X	X	-	X	-	-	46
-	-	-	-	X	-	X	X	-	-	54
-	-	-	-	X	-	-	X	X	-	39
-	-	-	-	-	X	X	X	-	-	62
-	-	-	-	-	X	X	-	X	-	47

CHAPTER 4

BLOCK MODE DMA

The QED-1 is designed to implement the block mode DMA protocols on the Q-BUS. Block mode DMA reduces the "handshaking" necessary to transfer data and thereby increases the transfer rate by a factor of nearly 2 over non-block mode data transfer. From the user's perspective there is no difference in the operation or configuration of the QED-1 since the board will operate transparently using whatever form of DMA is invoked by other devices on the bus.

4.1 WHAT IS BLOCK MODE DMA?

Under conventional direct memory access (DMA), direct data transfers between I/O devices and memory occur one (16 bit) word at a time or one byte at a time using DATI, DATO or DATO (B) bus cycles. Under block mode DMA, the starting address is followed not only by data for that address, but by data for up to 16 consecutive addresses. By eliminating the assertion of the address for each data word, the transfer rate is nearly doubled.

The QED-1 can also be used in system configurations with non-block mode DMA memory boards (either above or below). Most new Q-BUS peripheral controllers support block mode protocols and take advantage of the improved bus bandwidth using DATBI and DATBO type bus cycles. For devices already designed that do not use these block mode bus cycles, bus operation is unaffected.

For a complete technical description of these protocols, refer to the 1985 PDP-11 Micro/PDP-11 Handbook published by Digital Equipment Corporation.

CHAPTER 5

BANK SELECTION DESCRIPTION

5.1 GENERAL

The bank select feature of the QED-1 allows multiple 4MB boards to be configured into a standard Q-BUS backplane with no hardware modifications.

One of the boards is referred to as the base memory and is always resident and visible to the system in its portion of the 4MB address space. All other boards are referred to as paged memory and are visible in 256K portions through a window in the 4MB address space.

5.2 ADDRESSING THE CSR

To set up a bank selectable system the user must first select the amount of base memory required and the location of the window in the address space available. The window must start on a modulo 256K boundary.

All boards are jumper configured to be 4MB boards with a starting address of "0" each with a different control and status register address. Up to 16 control and status register addresses are available in a standard QED-1. Each board MUST have a different address as this address defines the board select bits which each board will respond to when the paging software is implemented. (Table 14 indicates the board select bits associated with each CSR Address.)

5.2.1 TABLE 14 - Addressing The CSR

CSR ADDRESS	SELECT BITS
7772100	0000
7772102	0001
7772104	0010
7772106	0011
7772110	0100
7772112	0101
7772114	0110
7772116	0111
7772120	1000
7772122	1001
7772124	1010
7772126	1011
7772130	1100
7772132	1101
7772134	1110
7772136	1111

5.3 THE PAGE OPTION JUMPERS

Then the 5 page option jumpers must be configured. These jumpers consist of one (1) Bank Enable jumper and four (4) Bank Select address jumpers. They are the first 5 jumpers closest to the board fingers--numbered P10 - P14 in Figure 1.

With the handle held upwards, the top jumper -- P10 -- is the bank enable jumper. This jumper should be removed except when bank select features are desired. The next 4 are the bank select address jumpers. Note that these are the same jumpers used for setting a memory window, described in section 2.6.

5.4 DESCRIPTION OF PAGE OPTION JUMPERS

BANK SELECTION DESCRIPTION

1. Bank Enable Jumper

   - o out - No paging features enabled.
   - o right - Board is base board; answers to all addresses except those specified by the 256K modulo address programmed into the Bank Select address jumpers. The state of the board select bits written into the Page Select Register is irrelevant.
   - o left - Board is paged board; answers to no addresses after initialize but if its board select bits are written into the Page Select Register the specified 256K page will become resident in the 256K window specified by the Bank Select Address Jumpers.

2. Bank Select Address Jumpers

These four jumpers specify the 256K window. The bottom jumper (P14) defines A18, the second (P13) A19, the third (P12) A20, and the fourth (P11), A21.

   - o right = 0
   - o left = 1
   - o Example: All jumpers to the right puts the page window at address 0.

5.5 PAGE REGISTER CONTROL

To access the Page Register of any QED-1 in the system, the QED-1's must first be placed in Hyper-CSR mode.

The Hyper CSR occupies the same address as the DEC-compatible parity CSR. It must be made accessible by the following sequence.

1. Select any resident parity CSR.

2. Write 12100 to that register.

3. With no other writes to memory allowed in between, write 12100 to that register again.

All QED-1's in the system will then be in Hyper CSR mode.

The Hyper CSR consists of 2 registers:

1. The ECC Control and Status Register

2. The Page Register

The ECC Control and Status Register is read/write and any read of the Hyper CSR reads this register. A write to the Hyper CSR with bit 15 = 0 is directed to the ECC CSR. (See Chapter 3 for description of this register.)

The Page Register is write-only; it cannot be read and is written to when Bit 15 = 1.

5.5.1 TABLE 15 - The Page CSR Bit Description:

Bit 0 -	Must be 0.	
Bit 1 -	LSB	Board Select Bits Choose 1 of 16 Boards
Bit 2 -	SB	Board Select Bits Choose 1 of 16 Boards
Bit 3 -	SB	Board Select Bits Choose 1 of 16 Boards
Bit 4 -	MSB	Board Select Bits Choose 1 of 16 Boards
Bit 5-7 -	Unused	
Bit 8 -	LSB	Selects which of the 16-256K pages will
Bit 9 -	SB	be visible in the Paging window if
Bit 10 -	SB	this board is selected.
Bit 11 -	MSB	this board is selected.
Bit 12-14	Unused	
Bit 15	Must be 1.	

NOTE: MSB is most significant bit LSB is least significant bit

CHAPTER 6

HELP AND REPAIR

6.1 CUSTOMER SERVICE

800 332 2578 PRODUCT SUPPORT NUMBER

Clearpoint offers a 24-hour before/repair replacement on all its products and a **LIFETIME WARRANTY** on parts and workmanship. Clearpoint is not responsible for product that has been mishandled or used in an inappropriate manner.

Return of all product must be accompanied by a **RETURN AUTHORIZATION NUMBER.** To receive this authorization number, call Clearpoint's Customer Service Department.

Call toll free in the United States (outside Mass.) **1-800-CLEARPT** (1-800 -253-2778). Outside of the United States or within Massachusetts, call 617- 435-5395, or 617-478-7794.

The following information will be needed in order to properly process your request:

1. Clearpoint Part Number :_____
2. Configuration (memory size) :_____
3. Serial Number : 2508 _____
4. Revision Number :_____
5. Reason for Return :_____
6. Return ship to address :_____
7. Bill to Address :_____
8. Purchase/Sales Order Number :_____
9. CPU :_____
10. Operating System :_____
11. Other Peripherials :_____

:_____

:_____

:_____

:_____

:_____

CHAPTER 7

ABOUT CLEARPOINT

Clearpoint was founded on the premise that memory is a unique component of a computer system requiring a different set of capabilities for production. Since its inception, Clearpoint has focused first and foremost on engineering. The result has been the development of a first rate staff and facility for CAD and engineering Research and Development. In order to achieve the most effective customer support, Clearpoint has an extensive network of systems, both for the DEC-compatible and non-DEC-compatible markets. There are 8 DEC systems spanning the entire line on DECNET in the house system alone.

Manufacturing became the next focus of attention: Clearpoint burn-in and test systems are now the standard to compare all others. Complete ESD protection and comprehensive board tracking for quality assurance are clearly evident throughout the manufacturing process.

Clearpoint growth has been marked by stability and profitability. Compounded growth has exceed 100 percent per year with consistent quarterly growth and profit. Sales per employee have been high throughout, because of Clearpoint's lean organization and clear delineation of responsibilities. The Clearpoint standard of excellence is expected at all levels in the company. Good people and a good environment combine to achieve the best product possible.