MEMORY SYSTEM

CI - 1173 - EDC

TECHNICAL MANUAL

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CONTENTS

SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the elements of operation, installation, and design of the CI-1173-EDC dynamic read/write memory.

1.2 THE MEMORY MODULE

The CI-1173-EDC various options are summarized below. All options come standard with Error Detection and Correction (EDC) circuitry.

OPTION	MEMORY CAPACTIY	MEMORY CHIP UTLIZED
128K	128Kx8 bits with EDC	64Kx1 (4164)
256K	256Kx8 bits with EDC	64Kx1 (4164)
512K	512Kx8 bits with EDC	64Kx1 or 256Kx1 (4164) or (41256)
1 MEG	1024Kx8 bits with EDC	256Kx1 (41256)
2 MEG	2048Kx8 bits with EDC	256Kx1 (41256)

1.2.1 CI-1173-EDC MEMORY DESCRIPTION

The CI-1173EDC is a ultra high density, high speed state-of-the-art memory with built in Error Detection and Correction circuitry which is plug compatible with any Q-bus computer system.

1.2.2 OPERATIONAL FEATURES

The CI-1173-EDC performs all memory functions according to Q-BUS protocol including BLOCK MODE DMA. START and STOP addresses for memory selection are user selectable on any 16K BYTE boundary in the 0 to 4 megabyte address range. The EDC logic requires no special installation or initialization procedures and operates at the speed of most comparable memory systems without such capability.

The module contains it's own CONTROL STATUS REGISTER (CSR) which is upward hardware and software compatible with standard DEC parity CSR's. Standard error trapping is performed requiring no software or hardware modification to the system. Trap on single (correctable) or double (noncorrectable) error is user selectable by placement of shunts on the memory. The CSR is addressable at any of the 16 reserved parity CSR locations in the I/O page. When an error occurs the CSR latches address information according to standard parity memory protocol. Also by controlling an originally unused bit in the CSR additional information can be read describing the exact failing RAM location on single bit errors for maintenance purposes. The user has the option of latching

information on the first or last occurring error. A LED indicator also quickly identifies which module is experiencing problems in the system.

User selectable advance reply tap allows generation of BRPLYL 60 nanoseconds prior to actual placement of data on the bus during read cycles. The advance reply tap which is totally allowable according to Q-BUS protocol results in an actual access time of 160 nanoseconds for the memory module.

Memory protect logic and battery backup bussing allow the user to operate in a battery backup mode. Power is less than 650MA from a battery +5 volt source for up to 2 megabytes of memory.

1.2.3 POWER REQUIREMENTS

The CI-1173-EDC requires only the +5 volt supply from the Q-BUS backplane.

TABLE 1-1

GENERAL SPECIFICATIONS REQUIREMENTS

CHARACTERISTICS SPECIFICATIONS	
Capacity	128K, 256K, 512K, 1 and 2 Megabytes
Cycle Time	395 Nanoseconds
Access Time* typ.	Wirte-160 Nanoseconds Read 220 Nanoseconds (160 Nanoseconds)**
Word Size	16 Bits
CSR	Read/Write Via I/O Port in I/O Page (DEC Hardware and software compatible with Extended EDC Logging)
Data-In/Data-Out	16 Bits Bidirectional with Open Collector TTL Voltage Compatible
Modes of Operation	DATO(B), DATI, DATIO(B), BLOCK MODE DMA
Selection	16K Byte Increments Anywhere within a 4 megabyte Address Field
Refresh	Internal, Distributed
Interrupt	On Single or Double Bit Error (Using DEC Parity Interrupt and Compatible CSR)
Interface Signals Inputs Outputs	TTL Compatible Open Collector
Operating Temperatures	0 to +70 C Non Condensing***
Storage Requirements	-40 to +80 C Non Condensing

Power Requirements****	NORMAL		BACKUP	
at 5 volts +5% and 25 C	Operate	Standby	Operate	Standby
+5 volts	2.6 A	2.4A	1.8 A	1.75 A
+5 VB	—	—	800 MA	650 MA

Dimensions	8.44 x 10.46

* SYNCH to REPLYL inside memory drivers. Add 30ns typ. 50ns max. for actual bus measurements. Assumes max. delay SYNCH to DINH or DOUTH =150ns. For delays greater than 150ns reply will be delayed by the amount over 150ns for writes and the amount over 200ns for reads.

** With advance Reply Implemented.

*** With Adequate Air Flow.

**** Power requirements for 512K and 2 Meg. options.
Other options power requirements will be less.

SECTION II

HANDLING AND INSTALLATION

2.1 INTRODUCTION

This section details handling precautions and the procedure to interface the CI-1173-EDC with a Q-BUS compatible system.

2.2 HANDLING PRECAUTIONS

The memory ICs used on the CI-1173-EDC are MOS devices. They can be damaged by static electricity discharge. ALWAYS HANDLE MOS ICs in a manner such that no discharge will flow through the ICs. Also avoid unnecessary handling and wear cotton rather than synthetic clothing when you handle these ICs.

2.3 INTERFACE SIGNALS

The input signals to the memory are TTL compatible and the output signals are open collector. The Q-BUS pin assignments are shown in TABLE 2-1.

2.4 MEMORY INTERFACE

The CI-1173-EDC has both a memory address selection and, for the CSR an I/O port selection. Also various user options must be considered before installing the module in a Q-BUS backplane. Please read the following three sections carefully before selecting the desired options and address configurations required by your system application. After configuration, the CI-1173-EDC may be installed in any available slot in the Q-BUS backplane. Insure that the priority chain for interrupts and DMA have not been broken by leaving an empty slot between the CPU and modules requiring such service. DC power must be removed from the backplane during module removal or insertion.

CAUTION: The memory module and backplane can be damaged if the module is installed backwards. Care should be taken to insure that the module is installed with the component side of the module facing the same way as other LSI modules. Do not install the memory module in any backplane that has power connected to any of the extended address lines, BDAL 18-21 (connector pins BC1, BD1, BE1, and BF1 respectively.)

2.4.1 USER OPTIONS

The following user options may be selected for specific system applications. The CI-1173-EDC is shipped with the option disabled or where applicable in the most commonly used configuration. Refer to Appendix A for detailed information on the implementation of the following options.

OPTION	SELECTION
Advance Reply	Disabled*; Enabled
Block Mode DMA	Disabled*; Enabled
I/O Page Select	4K*; 2K
Interrupt on Memory Error	Disabled; on single bit error; on double error*; on single or double bit error
Extended CSR	Disabled*; Enabled
Latched Error	Latch on First Error; Latch on Last Error*
Battery Backup	Implemented; Not Implemented*

2.4.2 MEMORY ADDRESS SELECTION (REFER TO LAYOUT DRAWING 71354 FOR SHUNT LOCATIONS)

The CI-1173-EDC has an individually selectable START address and END address with 16K byte granularity in the 4 megabyte (22 bit address) field.

To make the address selection, START and STOP addresses are individually determined at shunt AREA F for START address and shunt AREA G for STOP address. Shunt AREAS F and G each contain 8 shunt positions labled 21, 20, 19, 18, 17, 16, 15, and 14. Each shunt position corresponds directly to its respective address bit in decimal. An installed shunt represents a decode of "O" to its respective address bit and a removed shunt represents a "1". To enable the memory simply select the start address at AREA F by installing shunts at each respective address bit decoded as "0". Remove the shunt at each respective address bit decoded as "1". Do likewise at AREA G for the STOP address. Address selection is inclusive. As little as 16K bytes of memory can be selected up to as much as is contained on your CI-1173-EDC option size. Unused shunts can be stored at AREA L.

* Factory shipped configuration

For example: To place a CI-1173-EDC 512K option size in a system with a START address of 00200000 (octal) and STOP address of 02177777 (octal) perform the following:

SHUNTS AREA F START ADDRESS	SHUNTS AREA G STOP ADDRESS
21 INSTALLED	21 INSTALLED
20 INSTALLED	20 INSTALLED
19 INSTALLED	19 NOT INSTALLED
18 INSTALLED	18 INSTALLED
17 INSTALLED	17 INSTALLED
16 NOT INSTALLED	16 INSTALLED
15 INSTALLED	15 NOT INSTALLED
14 INSTALLED	14 NOT INSTALLED

The CI-1173-EDC is shipped with a START address of 00000000 (octal) and a STOP address corresponding to it's option size.

2.4.3 CSR ADDRESS SELECTION

The CI-1173-EDC CSR is a 16 bit read/write register that can be placed at any of 16 reserved parity CSR locations or disabled. A full description of it's function and application is given in SECTION III.

The CSR address is selected according to the placement of shunts at AREA B and E on the module. By convention, the CSR addresses are assigned as follows: The CI-1173-EDC with the lowest starting address should be jumpered for the lowest CSR address (refer to table 2-1). The remaining CI-1173-EDC memory modules should be jumpered in sequence.

NOTE: When running DEC parity memory diagnostics the CSR register must be disabled. This is because the CI-1173-EDC automatically corrects errors on subsequent memory cycles and the diagnostics do not expect such an occurrence from a memory module.

TABLE 2-1

CSR ADDRESS SELECTION

ADDRESS SELECTED	SHUNT AREA B	SHUNTS INSTALLED AREA E	ADDRESS SELECTED	SHUNT AREA B	SHUNTS INSTALLED AREA E
17772100*	0-1	1,2,3	17772120	0-2	1,2,3
17772102	0-1	2,3	17772122	0-2	2,3
17772104	0-1	1,3	17772124	0-2	1,3
17772106	0-1	3	17772126	0-2	3
17772110	0-1	1,2	17772130	0-2	1,2
17772112	0-1	2	17772132	0-2	2
17772114	0-1	1	17772134	0-2	1
17776116	0-1	NONE	17772136	0-2	NONE
DISABLED	NONE	DON'T CARE			

NOTE: An installed shunt at AREAS E, F and G is a shunt installed horizontally across the two gold posts at its specific designation. Remove shunts at all shunt areas may be stored at AREA L.

* Factory shipped configuration

TABLE 2-2

CI-1173-EDC PIN ASSIGNMENTS

COMPONENT SIDE			CIRCUIT SIDE		
PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
AA1			AA2	+5	+5 VDC
AB1			AB2		
AC1	BDAL16L	ADDRESS	AC2	GND	GROUND
AD1	BDAL17L	ADDRESS	AD2		
AE1			AE2	BDOUTL	DATA OUT CONT
AF1			AF2	BRPLYL	REPLY
AH1			AH2	BDINL	DATA IN CONT
AJ1	GND	GROUND	AJ2	BSYNCL	SYNCHRONIZE
AK1			AK2	BWTBTL	WRITE/BYTE
AL1			AL2		
AM1	GND	GROUND	AM2	BIAKIL	INT ACK IN*
AN1			AN2	BIAKOL	INT ACK OUT*
AP1			AP2	BBS7L	BANK 7 SEL
AR1	BREFL	BLOCK MODE ACK	AR2	BDMGIL	DMA IN*
AS1			AS2	BDMGOL	DMA OUT*
AT1	GND	GROUND	AT2	BINITL	INITIALIZE
AU1			AU2	BDAL0L	DATA/ADDRESS
AV1	+5B	+5V BATTERY	AV2	BDAL1L	DATA/ADDRESS
BA1	BDCOKH	DC POWER OK	BA2	+5	+5 VDC
BB1			BB2		
BC1	BDAL18L	ADDRESS	BC2	GND	GROUND
BD1	BDAL19L	ADDRESS	BD2		
BE1	BDAL20L	ADDRESS	BE2	BDAL2L	DATA/ADDRESS
BF1	BDAL21L	ADDRESS	BF2	BDAL3L	DATA/ADDRESS
BH1			BH2	BDAL4L	DATA/ADDRESS
BJ1	GND	GROUND	BJ2	BDAL5L	DATA/ADDRESS
BK1			BK2	BDAL6L	DATA/ADDRESS
BL1			BL2	BDAL7L	DATA/ADDRESS
BM1	GND	GROUND	BM2	BDAL8L	DATA/ADDRESS
BN1			BN2	BDAL9L	DATA/ADDRESS
BP1			BP2	BDAL10L	DATA/ADDRESS
BR1			BR2	BDAL11L	DATA/ADDRESS
BS1			BS2	BDAL12L	DATA/ADDRESS
BT1	GND	GROUND	BT2	BDAL13L	DATA/ADDRESS
BU1			BU2	BDAL14L	DATA/ADDRESS
BV1	+5	+5 VDC	BV2	BDAL15L	DATA/ADDRESS

* BIAKIL and BIAKOL are bussed together as well as BDMGIL and BDMGOL on the A and C slots to maintain interrupt and DMA chain on the bus. The CI-1173-EDC only used +5 vdc and Gnd from the C and D slots, therefore it may be used in both standard and special C and D slot backplanes.

SECTION III

GENERAL OPERATIONAL INFORMATION

3.1 MEMORY CYCLES

All memory cycles, byte or word, result in a Word Read-Modify-Write (RMW) cycle within the CI-1173-EDC. Timing for a typical DATI and DATO cycle are shown in figures 3-1 and 3-2 respectively.

During a memory read, data from the memory array is fed to the two Error Detection Correction (EDC) chips on the module (U15 and U16). Here it is corrected if a single bit error is detected or outputed unaffected if no error has occurred. The corrected output data is placed on the bus and is written back to the memory array along with six check bits on the subsequent write portion of the RMW cycle.

During a memory write, data from the bus is latched following the occurrence of BDOUTL. It then enters the two EDC chips. Here six check bits are generated. The check bits, along with the data, are then passed to the memory array where they are stored on the subsequent write portion of the RMW cycle.

On byte write operation the RMW cycle first performs a read on the corresponding word location, correcting any single bit errors if any occurred without placing data on the bus. The latched byte to be stored then enters its corresponding EDC chip (each EDC chip operates on one byte, U15 for the low byte, U16 for the high byte) where in correlation with the remaining unchanged or corrected byte a new set of six check bits are generated for the entire word. The new check bits, along with the new byte from the bus and the unchanged or corrected byte are stored on the subsequent write portion of the RMW cycle.

With this memory access technique all single bit errors are immediately corrected and rewritten to the memory array. This eliminates the possibility of additional soft errors occurring at a later time resulting in a double uncorrectable error. Also any read or write to a word or byte location results in correct check bits being generated for the corresponding word address. This eliminates the need for any special initialization sequence for the EDC to function correctly. The EDC functions correcting single bit errors and detecting double bit errors from turn-on. The user must insure however that all used locations are written to or read from prior to enabling the error interrupts to avoid the occurrence of unnecessary incorrect error trapping. The CI-1173-EDC has an access time of 220 nanoseconds and cycle time of 395 nanoseconds. The access and cycle times correspond to a cycle where correction is made as well as one where none is made. The access and cycle times would be still 220 and 395 nanoseconds even if each row of the memory array had an IC missing.

3.2 CONTROL STATUS REGISTER (CSR) USE

The control status register in the CI-1173-EDC allows program control of certain EDC functions and contains diagnostic information if a single or double bit error should occur. The CSR has been structured to maintain compatiblity with standard DEC parity CSR's with added enhancements allowing extensive error logging for single bit errors for maintainability while causing no degradation to system performance. The CSR is assigned an address and can be accessed via the Q-BUS. The CSR bit assignments are described as follows:

BITS 1,3 12 Under standard operation these bits are not used and are read as logical "0"s. Writing into these bits has no effect on the CSR. They are used under extended EDC operation.

BIT 4 This bit is not used and is always read as a logical "0". Writing into this bit has no effect on the CSR.

BIT 0 ERROR ENABLE
If bit 0 is set on DATI or DATIO(B) BDAL 17 is be asserted on the bus simultaneously with data. This is a read/write bit reset to zero on power-up or BUS INIT. Also this bit is used for extended EDC information. See bit 13 description.

BIT2 WRITE WRONG CHECK BIT
If this bit is set and a DATO or DATOB cycle to memory occurs, check bit 3 will be written incorrectly to memory. This bit may be used to check the EDC logic as well as failed address and EDC information in the CSR. Also this bit is used for extended EDC information. See bit 13 description.

BIT 5-11 ERROR ADDRESS BITS
If an error occurs on a DATI or DATIO(B) cycle, then A11-A17 are stored in CSR bits 5-11 and bits A18-A21 are latched. The first read CSR bit 14=0 sends A11-A17 to the bus (CSR bits 5-11). Then the program must set CSR bit 14=1. This enables A18-A21 to be read from CSR bits 5-8.

BIT 13 EXTENDED CSR ENABLE
If enabled (See Appendix A) and if set this bit allows syndrome and memory bank information to be read from CSR bits 0-3 and 12-15. The information will determine the exact location of the failing RAM on single bit errors or decoded a double bit error according to TABLE 3-1 and TABLE 3-2. When set to zero the CSR acts as a standard parity CSR. This is a read/write bit if enabled and reset to zero on power up or BUS INIT.

BIT 14 EXTENDED CSR ADDRESS READ ENABLE
Bit 14 is a read/write bit and is reset by a power up or BUS INIT. When set it allows retrieval of failed address bits A18-A21. Also this bit used for extended EDC information.

BIT 15 ERROR
If a single or double bit error occurs on a DATI or DATIO(B) cycle this bit will be set to a 1. This is a read/write bit and is reset to zero by power-up or BUS INIT. Bit 15 will remain set unless rewritten or initialize. Also this bit is used for extended EDC information.

TABLE 3-1

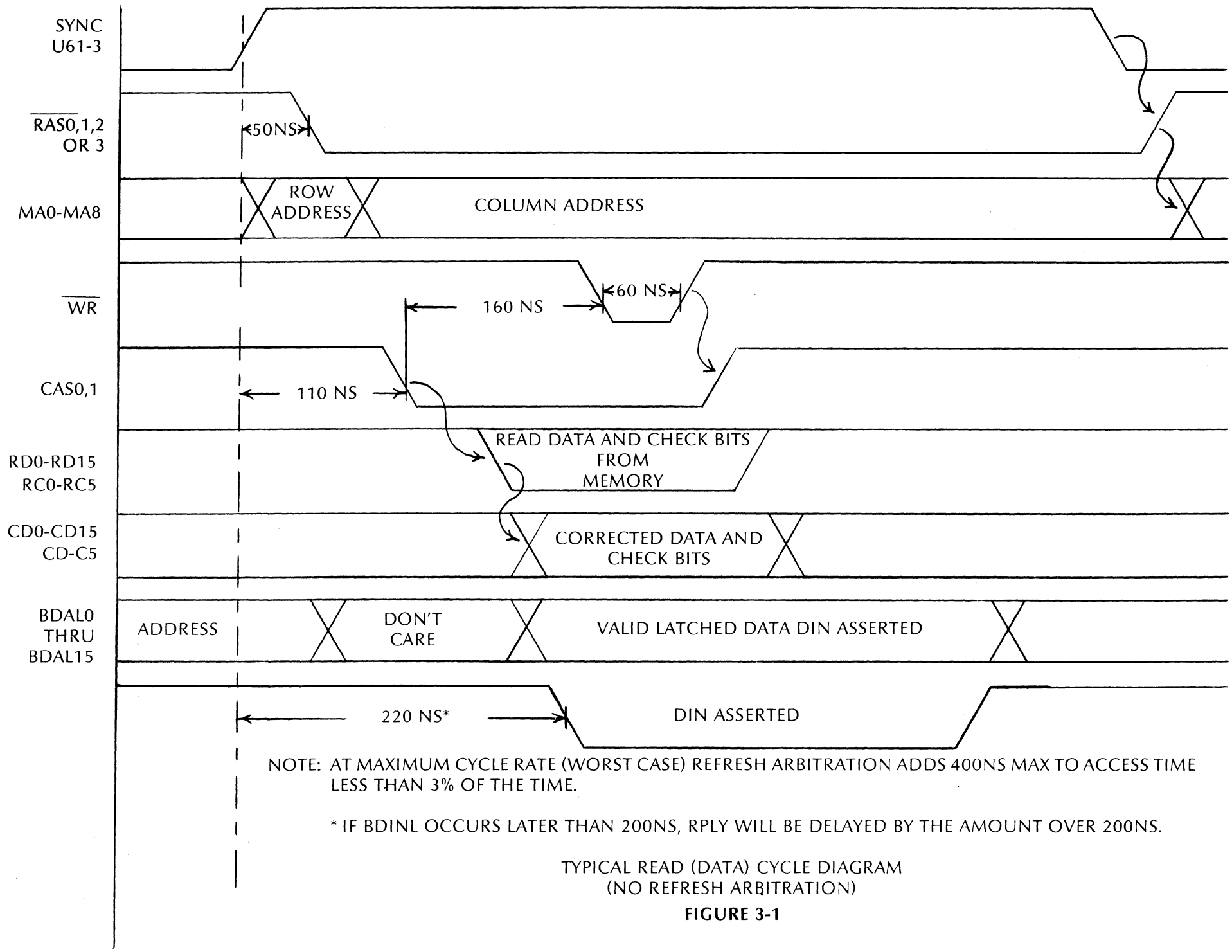
CSR BIT POSITIONS						FAILED RAM
15	14	13	12	3	2	BIT
1	1	1	1	1	1	NONE
1	0	1	1	1	1	C0
1	1	1	1	1	0	C1
1	1	1	1	0	1	C2
1	1	0	1	1	1	C3
0	1	1	1	1	1	C4
1	1	1	0	1	1	C5
1	1	0	0	0	1	D0
1	0	1	0	0	1	D1
1	1	1	0	0	0	D2
1	0	1	0	1	0	D3
0	1	1	0	0	1	C4
0	0	1	0	1	1	D5
0	1	1	0	1	0	D6
0	0	1	0	0	0	D7
0	1	0	0	1	1	D8
0	0	0	1	1	1	D9
0	1	0	1	1	0	D10
1	0	0	1	1	0	D11
0	1	0	1	0	1	D12
1	0	0	1	0	1	D13
1	1	0	1	0	0	D14
0	0	0	1	0	0	D15

All remaining bit combinations are multiple error

TABLE 3-2

CSR BIT LOCATIONS		FAILED MEMORY BANK
1	0	
0	0	B0
1	0	B1
0	1	B3
1	1	B4

The actual physical location of the failing RAM is determined by the intersection of the failing bit location in TABLE 3-1 with the failing bank indicated in TABLE 3-2. The CI-1173-EDC PCB has bit designation labeling across the top of the 88 bit memory array and bank designation along the left side of the memory array. EDC information can be read only if bit 13 is set and is valid only if an error has occured (bit 15 set).

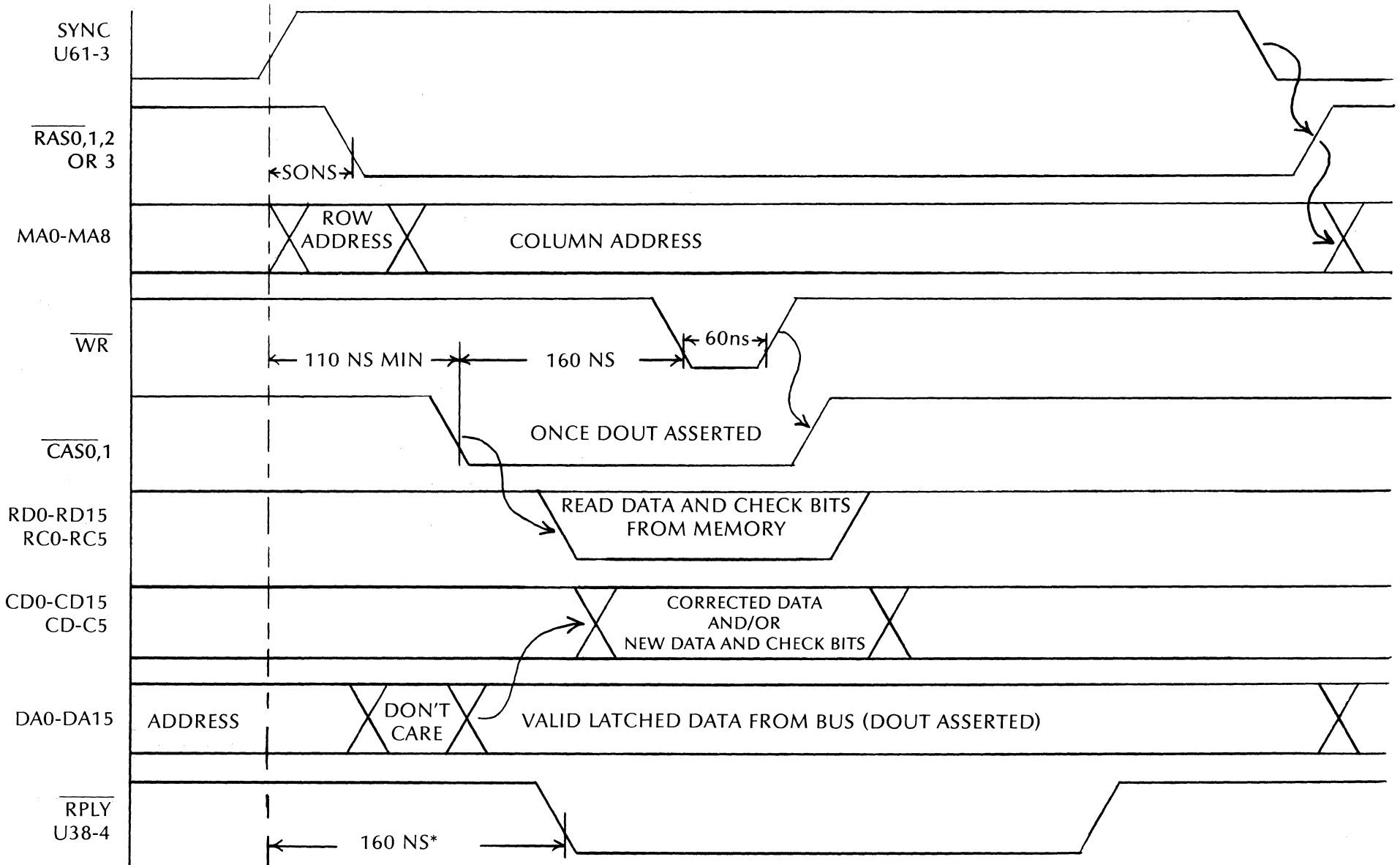


NOTE: AT MAXIMUM CYCLE RATE (WORST CASE) REFRESH ARBITRATION ADDS 400NS MAX TO ACCESS TIME LESS THAN 3% OF THE TIME.

* IF BDINL OCCURS LATER THAN 200NS, RPLY WILL BE DELAYED BY THE AMOUNT OVER 200NS.

TYPICAL READ (DATA) CYCLE DIAGRAM
(NO REFRESH ARBITRATION)

FIGURE 3-1

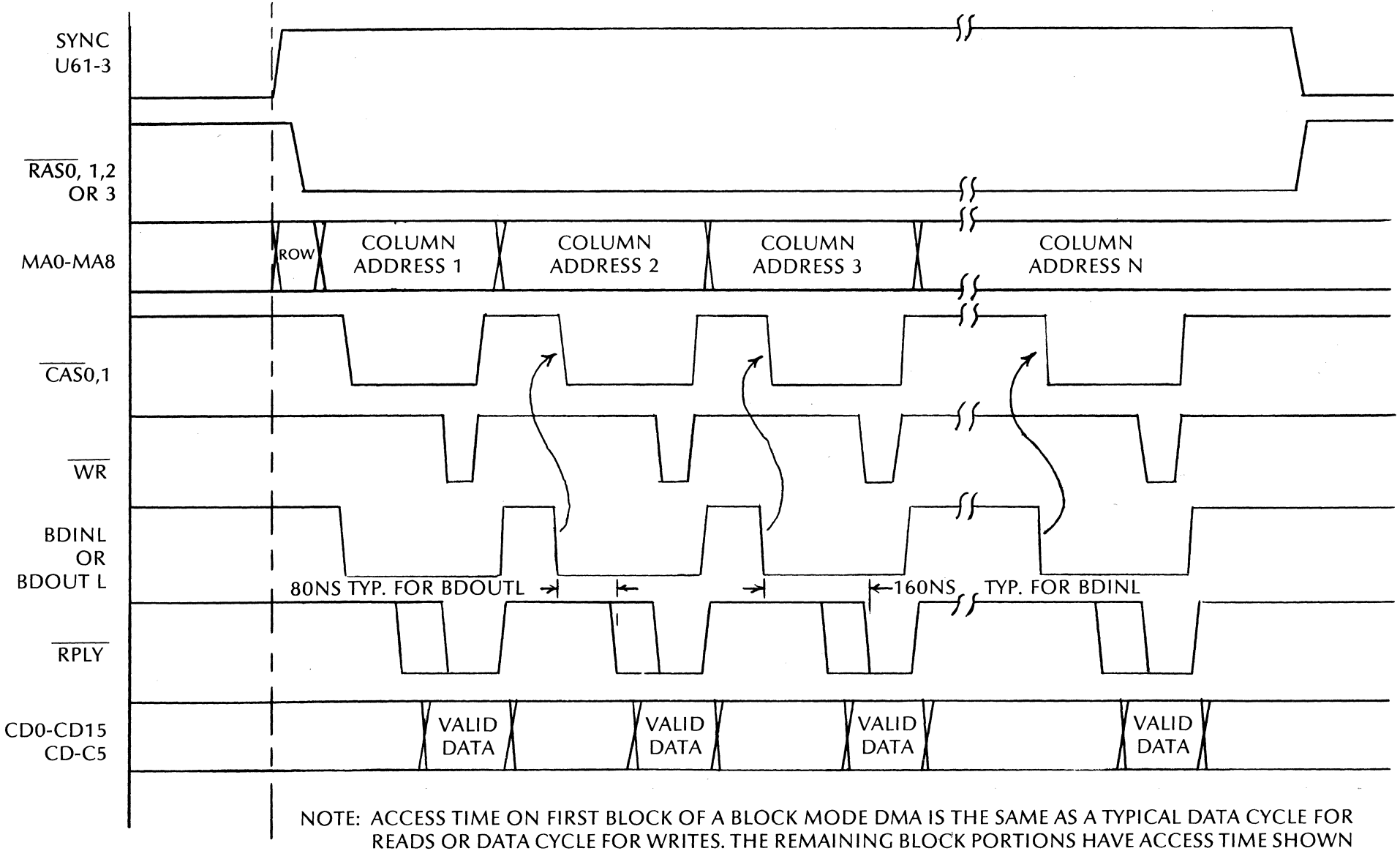


NOTE: AT MAXIMUM CYCLE RATE (WORST CASE) REFRESH ARBITRATION ADDS 400NS MAX TO ACCESS TIME LESS THAN 3% OF THE TIME.

* IF BDOUTL OCCURS LATER THAN 100NS AFTER BSYNCL, RPLY WILL BE DELAYED BY THE AMOUNT OVER125NS.

TYPICAL WRITE (DAT0(B)) CYCLE DIAGRAM
(NO REFRESH ARBITRATION)

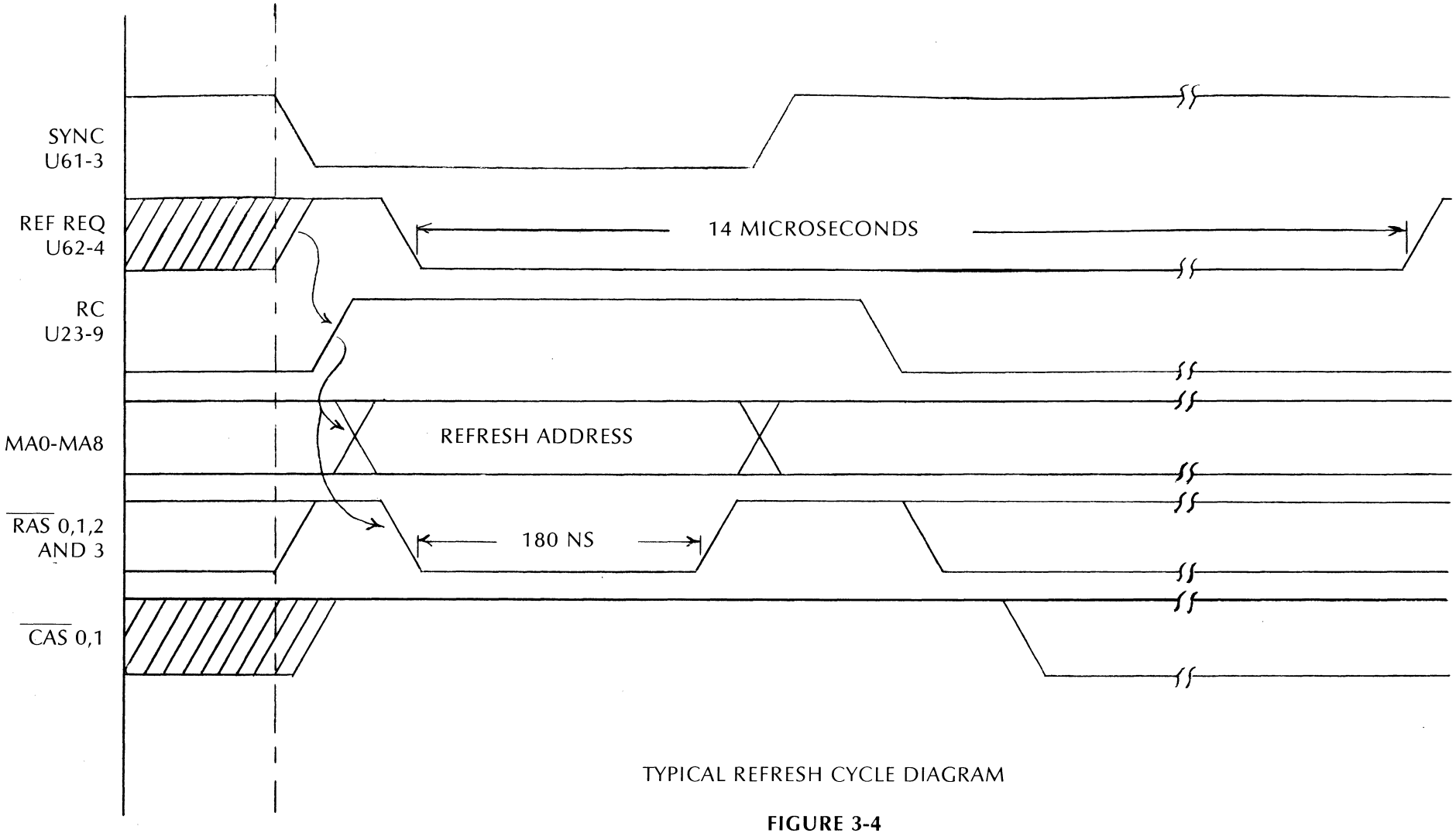
FIGURE 3-2



NOTE: ACCESS TIME ON FIRST BLOCK OF A BLOCK MODE DMA IS THE SAME AS A TYPICAL DATA CYCLE FOR READS OR DATA CYCLE FOR WRITES. THE REMAINING BLOCK PORTIONS HAVE ACCESS TIME SHOWN FOR WRITE CYCLES (BDOUTL ASSERTED) AND READ CYCLES (BDINL ASSERTED)

TYPICAL BLOCK MODE DMA CYCLE TIMING
(NO REFRESH ARBITRATION0

FIGURE 3-3



TYPICAL REFRESH CYCLE DIAGRAM

FIGURE 3-4

APPENDIX A

USER OPTIONS
(refer to layout drawing 71354 for shunt locations)

1) ADVANCE REPLY

The CI-1173-EDC has the option of generating BRPLYL 60 nanoseconds prior to actual data being placed on the bus during read cycles. If your system conforms in all respects to the Q-BUS specification the implementation of this option will insure a worst case access time of 160 nanoseconds. The implementation may not be possible if there are nonstandard modules in your system.

ADVANCE REPLY is determined by the placement of the shunt at AREA H.

SHUNT INSTALLED AT AREA H	OPTION SELECTED
0-1	ADVANCE REPLY ENABLED
0-2*	ADVANCE REPLY DISABLED

2) BLOCK MODE DMA

The CI-1173-EDC supports BLOCK MODE DMA (please consult MICRO/PDP-11 handbook for detailed description). This function should be enabled only in systems that have DMA devices that support this feature. Also because the function utilizes the BREFL (AR1) signal, it cannot be implemented in systems utilizing this signal for another function such as refresh.

BLOCK MODE DMA is determined by the placement of the shunt at AREA J.

SHUNT AT AREA J	OPTION SELECTED
installed	BLOCK MODE DMA enabled
not installed*	BLOCK MODE DMA disabled

3) I/O PAGE SELECT

The CI-1173-EDC has the option of allowing the lower 2K of the Q-BUS I/O page to be utilized as memory. This option can only be enabled in systems that do not use the lower 2K for I/O operations.

* factory shipped configuration

The I/O PAGE SELECT is determined by the placement of the shunt at AREA I.

SHUNT INSTALLED AT AREA I	OPTION SELECTED
0-1	2K I/O PAGE selected
0-2*	4K I/O PAGE selected

4) INTERRUPT ON MEMORY ERROR

The CI-1173-EDC has the option of generating a Q-BUS parity trap on single bit errors only, double bit errors only, both single bit and double bit errors, or it can be disabled.

The type of error interrupt is determined by the placement of the shunt at AREA C.

SHUNT INSTALLED AT AREA C	ERROR INTERRUPT SELECTED
0-1*	Only double bit errors
0-2 Only single bit errors	
0-3 Both double and single	
Not installed	Interrupt disabled

5) EXTENDED CSR

To read the CI-1173-EDC syndrome information when errors occur, it is necessary to set bit 13 of the CSR to a "1". Bit 13 of the originally defined parity CSR register is an unused bit that must be read as a "0". To make the CI-1173-EDC CSR register like a standard CSR the user has the option of disabling the EXTENDED CSR function.

Whether the EXTENDED CSR function is enabled or disabled is determined by the placement of the shunt at AREA D.

SHUNT INSTALLED AT AREA D	OPTION SELECTED
0-1	EXTENDED CSR enabled
0-2*	EXTENDED CSR disabled

6) LATCHED ERROR

When an error occurs syndrome and memory bank information is latched into bits 0-3 and 12-15 of the extended CSR. The CI-1173-EDC has the option of allowing the first error to disable any succeeding errors from latching new information into the CSR (latch on first error) or the first error and each succeeding error to latch new information into the CSR (latch on last error).

The LATCHED ERROR option selected is determined by the placement of the shunt at AREA A.

SHUNT INSTALLED AT AREA A	OPTION SELECTED
0-1*	Latch on last error
0-2	Latch on first error

7) BATTERY BACKUP

The CI-1173-EDC has an optional battery backup mode of operation. For operation in this mode the user must supply an uninterruptable 5 volt power source (SPEC given in TABLE 1-1 at Q-BUS pin AV1. The user must insure that his system contains a DEC power supply with power fail control logic, or the existing system must meet Q-BUS specifications for power up and down sequencing.

To implement battery backup remove the two 5 volt bus etches at AREA M (0 to 1) and install two bus jumpers at AREA M (0 to 2).