Century Data Systems
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Trident

Model T2000B
Exerciser Technical Manual

Part No. 76203-101

MODEL T2000B

DISK DRIVE EXERCISER

TECHNICAL MANUAL

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SECTION 1

GENERAL INFORMATION

The Model T2000B Exerciser is a portable testing device specially designed to operate CalComp Trident disk drives offline to or disconnected from their controllers.

Controls on the exerciser allow manual simulation of all controller bus and tag line control functions as well as providing several automatic modes of operation; its indicators monitor most major control, sequence, and error signals from the drive.

In its automatic mode the exerciser will:

- Write on the disks (in either of two fixed data patterns)
- Set up a read operation (data read may be monitored with an external scope or the T2001 Head Alignment Meter.)
- Forward Seek (sequential single step)
- Random Seek (to cylinder addresses selected at random).

Special switches on the exerciser will cause the drive to:

- Reset its head address to zero (RSTHD).
- Advance its head address by one (ADVHD).
- Recalibrate to cylinder 000 and head 0 (REZERO).
- Disable seek incomplete (SKINC).
- Reset device check errors (RST).

The exerciser is 8 inches high by 10-1/4 inches wide by 2-1/2 inches deep and weighs approximately 6 pounds. The overall length of its interconnecting cable is 48 inches. All power required by the exerciser is supplied by the dc power supply in the disk drive via the interconnecting cable.

SECTION 2

INSTALLATION AND OPERATION

Offline operation of a Trident Disk Drive for maintenance checkout or head alignment requires the installation of the T2000B Exerciser and the INTERFACE/DEGATE switch on the disk drive to be set to DEGATE. The exerciser may be installed with the drive powered up.

Note

The DEGATE switch on the disk drive must be active to enable exerciser control inputs, even when the disk drive is not connected to a controller.

INSTALLATION

To install the T2000B Exerciser, perform the following steps.

1. Remove the rear cover from the disk drive for maintenance access.

2. Place the exerciser adjacent to the disk drive, and install the interconnecting cable between the exerciser and connector J01 on the card cage assembly of the disk drive. See Figure 2-1.

3. Turn off all toggle switches on the exerciser (CONT, SKINC, and all BIT switches down).

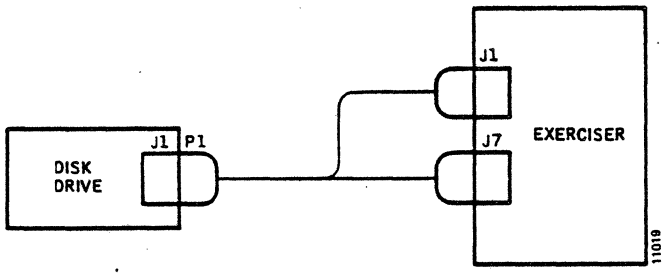


Figure 2-1. Exerciser Interconnection Diagram

4. Set the disk drive INTERFACE/DEGATE switch to DEGATE.

The disk drive is now ready for offline operation by means of exerciser control switches. Usually a pack change is performed prior to maintenance operation by replacing the system pack with a scratch pack (or the Head Alignment pack, if applicable) to protect the system record.

CAUTION

During maintenance, make sure to turn the disk drive PWR ON/OFF switch to OFF before disconnecting or installing any disk drive components, including circuit boards.

To operate the disk drive with the exerciser, refer to the Operating Procedures (Automatic) and the Operating Procedures (Manual) given further on in this section.

Note

When the disk drive is connected to an operating system, operate the PWR ON/OFF switch only when the drive is offline (DEGATE active). This prevents power transients from reaching the system.

REMOVAL

To return the disk drive online to the system and/or disconnected the exerciser, perform the following steps.

1. Check that the PWR ON/OFF switch is turned ON.

2. If a pack change is necessary before returning the disk drive online, power down the disk drive and change the pack.

3. Set the INTERFACE/DEGATE switch to INTERFACE. The drive is now online and exerciser inputs are inoperable.

4. Disconnect the exerciser interconnecting cable from the drive and remove the exerciser.

5. Reinstall the rear cover on the disk drive.

CONTROLS AND INDICATORS

All exerciser controls and indicators are mounted on its front panel. See Figure 2-2. The controls perform the following functions.

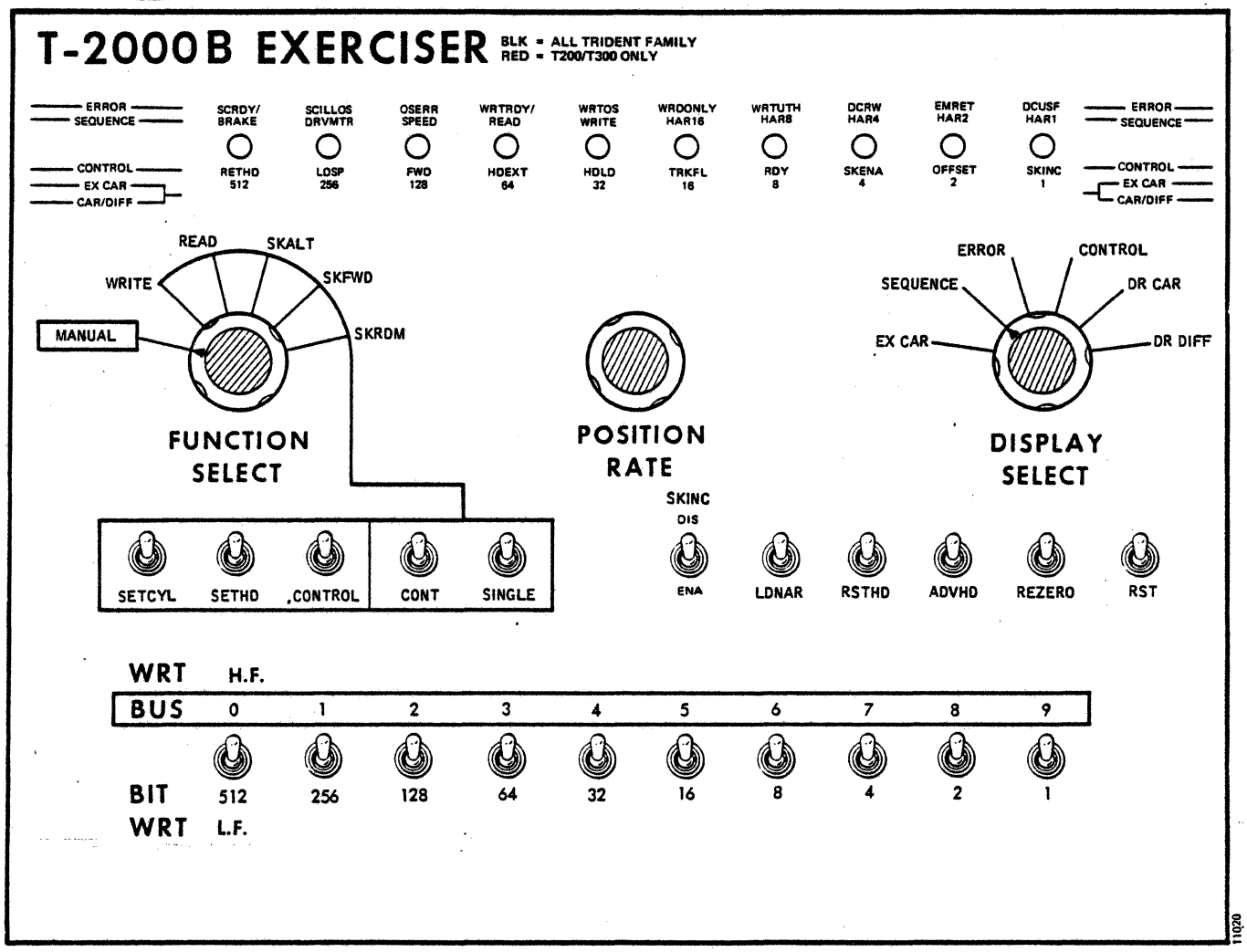


Figure 2-2. Exerciser Controls and Indicators

Control	Description and Function
FUNCTION SELECT Switch	Six-position rotary switch used to select primary operating mode of exerciser. The MANUAL position of this switch enables the SETCYL, SETHD, and CONTROL tag line switches. Other (automatic) positions of this switch are under control of the SINGLE or CONT switches.
POSITION RATE Control	Potentiometer used to adjust the repetition rate of continuous alternate, forward, and random seek operations performed under exerciser control.
DISPLAY SELECT Switch	Six-position rotary switch that selects the set of inputs applied to the exerciser indicators for display.
SETCYL Switch	Momentary-action switch used to simulate Set Cylinder Tag line active when operating the exerciser in the MANUAL mode.
SETHD Switch	Momentary-action switch used to simulate Set Head Tag line active when operating the exerciser in the MANUAL mode.

Control	Description and Function
CONTROL Switch	Momentary-action switch used to simulate Control Tag line active when operating the exerciser in the MANUAL mode.
CONT Switch	Toggle switch that starts (up) or stops (down) continuous execution of the FUNCTION SELECT switch operating mode.
SINGLE Switch	Momentary-action switch used to enable single execution of any seek mode selected by the FUNCTION SELECT switch. This switch is also used to start a single track record write operation.
SKINC Switch	Toggle switch that disables seek incomplete errors from being detected (up).
LDNAR Switch	Momentary-action switch used to load exerciser Next Address Register with bit pattern set into ten BIT switches.
RSTHD Switch	Momentary-action switch used to reset disk drive Head Address Register count back to head 0 address. (READ or WRITE only).
ADVHD Switch	Momentary-action switch used to advance disk drive Head Address Register count by one, selecting the next read/write head. (READ or WRITE only).
REZERO Switch	Momentary-action switch used to initiate a recalibrate seek operation back to cylinder 000. Also resets the drive Head Address Register to 0 and clears SCILLOS Device Check errors.
RST Switch	Momentary-action switch used to reset most disk drive Device Check errors.
BIT Switches	Ten toggle switches used to simulate Bus line control bits in MANUAL mode and to enter cylinder addresses for seek operations.
WRT Switch (Same as BIT Switch 512)	In Write mode, this switch is used to select the write pattern: At H. F. (up), the exerciser writes a pattern of all ones or all zeros (which of the two is determined by how the exerciser write signal syncs up with the disk drive logic and cannot be selected by the operator). At L. F., the exerciser writes a pattern of alternate ones and zeros.

The ten LED indicators are multifunction, displaying one of six sets of status signals according to the position of the DISPLAY SELECT switch. When the DISPLAY SELECT switch is set to CAR, the indicators will display the binary content of the internal exerciser Cylinder Address Register, i.e., the cylinder address that is sent to the drive when a seek operation is commanded. In the DR CAR position the cylinder number standing in the drive cylinder address register is displayed. In the DR DIFF position the contents of the drive difference counter are displayed. In other positions of the switch, error, sequence, or control signals from the drive are displayed. Each of these latter functions is listed below with a description of its significance.

Error Status	Significance
SCRDY/	Set Cylinder Tag when not ready (Device Check)
SCILLOS	Seek while offset or to illegal cylinder (Device Check)
OSERR	Set Head Tag when not ready (Device Check)
WRTRDY/	Write command when not ready (Device Check)
WRTOS	Write command while offset is active (Device Check)
WRDONLY	Write command with READ ONLY switch on (Device Check)
WRTUTH	Write command while off track (Device Check)

Error Status (Continued)	Significance
DCRW	Write command without data transitions or with write current unsafe, or read or write command with more than one head selected (Device Check)
EMRET	Emergency Retract condition (Attention)
DCUSF	Dc voltages unsafe (an Emergency Retract condition)

Sequence Status	Significance
BRAKE	Brake voltage applied during power down
DRVMTR	Spindle motor power on
SPEED	Spindle is up to speed (85 percent of full speed or greater)
READ	Read command is active
WRITE	Write command is active
HAR16, HAR8, HAR4, HAR2, HAR1	Binary Head Address Register count

Control Status	Significance
RETHD	Retract heads control signal
LDSP	Load Speed control signal
FWD	Forward seek direction control signal
HDEXT	Heads-Extended microswitch closed
HDLD	Heads are Loaded (servo signal present)
TRKFL	Track-Following mode control signal
RDY	Device is Ready (seek completed)
SKENA	Seek Enable control signal
OFFSET	Heads offset control signal
SKINC	Seek incomplete condition (Attention)

OPERATING PROCEDURES (AUTOMATIC)

Most operations performed using the exerciser will be executed with the FUNCTION SELECT switch set to some position other than MANUAL. These operations are called automatic in that they automatically sequence bus and tag line commands to simulate the controller. Automatic disk drive operations that can be executed are covered in the following paragraphs.

Seek to Cylinder

With the disk drive powered up and the heads loaded, the heads can be positioned to any legal cylinder by performing the following steps.

1. Press RST and then REZERO to initialize the drive. The drive should do a rezero, detenting at cylinder 0. (Rezero also resets the head address to 0.)

2. Then, if seek to some other cylinder is desired, enter the binary address of the cylinder into the exerciser BIT switches (up for one, down for zero in each bit position) and press LDNAR.

3. Set the DISPLAY SELECT switch to DR DIFF, in order to monitor the drive difference counter.

4. Leave the BIT switches set to the same cylinder address as in step 2, set the FUNCTION SELECT switch to SKALT, and press SINGLE to start the seek. Observe the activity in the CAR/DIFF display, indicating that the drive has set and is counting down its difference counter in the course of the seek, and that the CAR/DIFF display culminates in a zero indication as the drive reaches the new cylinder.

5. Set the DISPLAY SELECT switch to DR CAR. The ten indicators should light in the same bit pattern as the BIT switches turned on in step 2, indicating that the drive has reached the correct cylinder.

Note

The only way to further verify that a seek has actually reached the desired cylinder is to read the recorded address from the disk track, as is done by the controller online. This the exerciser is not equipped to do.

Alternate Seeks

To execute an alternate seek operation with the disk drive powered up and the heads loaded, proceed as follows:

1. Press REZERO and RST to initialize the drive.

2. Set BIT switches to one of the two seek limit cylinder addresses and press and release the LDNAR switch.

3. Set BIT switches to the other seek limit cylinder address, and set the FUNCTION SELECT switch to SKALT.

4. To start continuous alternate seeks between the two cylinders addressed in steps 1 and 2, turn on the CONT switch (up). The disk drive should begin doing forward and reverse seeks between the two cylinder address positions.

Note

All continuous seek operations can be slowed down or speeded up by turning the POSITION RATE control counterclockwise or clockwise.

5. To execute alternate seek operations step by step, leave the CONT switch turned off (down) and press the SINGLE switch. The disk drive should perform one forward or reverse seek operation each time the SINGLE switch is pressed.

6. To terminate continuous alternate seeks, turn off the CONT switch (down).

Stepped Forward Seeks

To perform single cylinder seek operations between cylinder 000 and the highest-numbered cylinder, perform the following steps:

1. Press REZERO and RST to initialize the drive. Set all BIT switches down (all zeros) and press LDNAR.

2. Set FUNCTION SELECT to SKFWD and turn on the CONT switch. The drive should seek continuously through all cylinders one at a time, then return to zero and repeat.

3. To execute forward seek operations one cylinder at a time, set the FUNCTION SELECT switch to SKFWD, leave the CONT switch turned off (down), and press the SINGLE switch. The disk drive should advance one cylinder position each time the SINGLE switch is pressed.

4. To terminate continuous forward seeks, turn off the CONT switch (down).

Random Seeks

Continuous random seeks are used as a general head-positioning exercise, particularly after head alignment, to make sure that the heads have been tightened enough to stay in tolerance. Proceed as follows:

1. With the disk drive powered up and the heads loaded, press RST, then REZERO. The disk drive should seek to cylinder 000 if the heads are not already in this position.

2. Set the FUNCTION SELECT switch to SKRDM.

3. To begin the random-seek operation, turn on the CONT switch (up). The disk drive should begin performing forward and reverse seeks to randomly selected cylinders.

4. To terminate random seeks, turn off the CONT switch (down).

Head Selection

Before an automatic read or write operation is started, the read/write head to be used must be selected. This is normally done after the heads have been positioned to the desired cylinder. (Refer to the Seek to Cylinder procedure.) To select a head for reading or writing, proceed as follows:

1. Set the DISPLAY SELECT switch to SEQUENCE. This causes the five right-hand indicators (HAR16 thru HAR1) to display the contents of the drive Head Address Register. Set FUNCTION SELECT to READ or WRITE.

2. If head 0 is to be selected, press and release the RSTHD switch. The HAR indicators should go out, indicating that the Head Address Register has been reset to head address 0.

3. If head 1 thru 18 is to be selected, press and release the RSTHD switch, and then press the ADVHD switch as required until the binary address of the desired head appears in the HAR indicators.

Write on Pack

Write data transitions are simulated by a write-clock generator in the exerciser that can be used to write a single track (from index to index) on a pack or can be used continuously to check disk drive write circuits. To use the exerciser write function, perform the following steps:

1. With a scratch pack loaded and the disk drive powered up, set the READ-WRITE/READ ONLY switch on the disk drive to READ-WRITE.

2. Press RST and then REZERO.

3. Select the cylinder on which the record is to be written. Refer to the Seek to Cylinder procedure.

4. Set the FUNCTION SELECT switch to WRITE.

5. Select the head with which the record is to be written. Refer to the Head Selection procedure.

6. Select the desired write pattern with BIT switch 512 (H. F. = all ones or all zeros; L. F. = alternate ones and zeros).

7. To write a one track record, press and release the SINGLE switch.

8. To write continuously in order to troubleshoot the write circuits, turn on the CONT switch (up).

Read from Pack

The exerciser permits continuous reading of any record (or the dibit pattern written on certain cylinders of the CE Alignment pack) to check disk drive read circuits (or head alignment). To use the exerciser read function, perform the following steps:

1. With a recorded scratch pack (or the CE Alignment pack) loaded and the disk drive powered up, set the READ-WRITE/READ ONLY switch on the disk drive to READ ONLY.

Note

The READ-WRITE/READ ONLY switch on the disk drive must be set to READ ONLY whenever the CE Alignment pack is used. This protects the pack from being written on (optional when a scratch pack is used).

2. Press RST and then REZERO.

3. Select the cylinder containing the record to be read. Refer to the Seek to Cylinder procedure.

4. Set the FUNCTION SELECT switch to READ.

5. Select the head with which the record is to be read. Refer to the Head Selection procedure.

6. To start reading, turn on the CONT switch (up).

7. To terminate reading, turn off the CONT switch (down).

Device Check Reset

If the disk drive locks up due to a Device Check error, the error condition can be determined by setting the exerciser DISPLAY SELECT switch to ERROR and looking at the indicators. If the Device Check is due to a machine malfunction (DCRW, EMRET, or DCUSF indicator lit), the malfunction must be located and corrected before the Device Check can be reset. However, if the Device Check was due to an operating error, the Device Check can be reset immediately and normal operation restored by proceeding as follows:

1. If the SCILLOS indicator is lit, press and release the REZERO switch. This action should cause the drive to seek to cylinder 000 and extinguish the SCILLOS indicator.

2. If an indicator other than SCILLOS is lit, press and release the RST switch. The indicator should be extinguished.

3. If performing step 1 or 2 fails to clear the Device Check condition, power down the disk drive, wait for the spindle to stop, and power the disk drive back up.

4. If the Device Check error continues after performing step 3, an equipment malfunction exists.

OPERATING PROCEDURES (MANUAL)

These procedures allow the disk drive interface bus and tag line signals to be simulated by the exerciser to check all disk drive command decode logic.

Note

Disk drive bus and tag line receivers are not checked by these exerciser-simulated control signals.

Manual bus and tag line controlled disk drive operations that can be executed include:

- Set Cylinder and Seek Start
- Set Head Address
- Head Offset Forward and Reverse
- Read Command

Set Cylinder and Seek Start

1. With a scratch pack installed and the disk drive powered up, set the exerciser FUNCTION SELECT switch to MANUAL.

2. Set BIT 0 thru 9 switches to the binary value of the cylinder address to which the disk drive is to seek (switch up is a one; switch down is a zero). Observe bit weights indicated below each switch.

3. Press and release the SETCYL switch. The disk drive should perform a seek operation to the cylinder selected in step 2 when the switch is released.

Set Head Address

After seeking to a cylinder and before issuing a read or write command, the head to be used for the read or write operation must be addressed. To enter the head address manually via the Bus lines, proceed as follows:

1. Turn off all BIT switches (down) and make sure that the FUNCTION SELECT switch is set to MANUAL.

2. Set BIT 5, 6, 7, 8, 9 switches to the binary address of the head to be selected (switch up is a one; switch down is a zero). Observe the bit weights of the switches indicated.

3. Press and release the SETHD switch.

4. To verify the correct loading of the head address, set the DISPLAY SELECT switch to SEQUENCE. The HAR indicators should light in the same bit pattern as the BIT 5, 6, 7, 8, 9 switch settings.

Head Offset Forward and Reverse

Proper operation of head offset commands can be checked by performing this procedure while monitoring the disk drive POSITION signal or while scoping the dibit signal read by the disk drive servo head. To command head forward or reverse offset, proceed as follows:

1. With a scratch pack installed and the disk drive powered up, set the exerciser FUNCTION SELECT switch to MANUAL.

2. Turn off all BIT switches (down) and turn on BIT switches 2 and 3 (up). Set the DISPLAY SELECT switch to CONTROL.

3. Press and release the SETHD switch. Heads should offset 300 microinches toward the spindle (POSITION +450 mv) and the OFFSET indicator should be lit.

4. Turn off BIT switch 3, and press and release the SETHD switch. Heads should offset 300 microinches in the reverse direction (POSITION -450 mv).

5. Turn off BIT switch 2, and press and release the SETHD switch. The heads should return to track center. The OFFSET indicator should go out.

Read Command

A controller read command, with or without early or late date strobing, can be simulated in the manual mode by performing the following steps:

1. With a scratch pack installed and the disk drive powered up, perform a seek to the cylinder to be read by using the Seek to Cylinder or the Set Cylinder and Seek Start procedure.

2. Select the head to be used by performing the Head Selection or Set Head Address procedure.

3. Turn off all BIT switches (down), and set the FUNCTION SELECT switch to MANUAL. Set the DISPLAY SELECT switch to SEQUENCE.

4. Press and hold the CONTROL switch down. Turn on the BIT 7 switch (Head Select) and then turn on the BIT 3 switch (Read). The READ indicator should light, and the disk drive should be reading data.

5. To check early or late data strobe, turn on the BIT 0 switch (Strobe Late) or the BIT 1 switch (Strobe Early).

6. To terminate the read command, release the CONTROL switch.

SECTION 3

THEORY OF OPERATION

Highlights of the T2000B Exerciser circuit are diagrammed in Figure 3-1; essentially, the exerciser is a dynamic testing device which simulates bus and tag signals to the logic of the disk drive, commanding the drive to perform its various functions, as if it were online, and then monitoring the resulting operations via a set of front panel indicators which are fed a wide variety of status signals from the internal drive logic.

The exerciser contains its own sequential control logic which, after simple setups are made at its front panel, will automatically develop the required tag and bus signal configurations and put them on the lines to the drive with the correct timing to cause the drive to go through seek sequences and write and read operations. Seeks may be made to one selected cylinder, through all cylinders successively, alternately back and forth between two selected cylinders, or continuously to randomly selected cylinders chosen by the exerciser logic. For write operations, the exerciser generates tag and bus commands and also produces a write signal consisting of clock-generated pulses which simulate data transitions to the drive. When operated in its read mode, the exerciser puts the drive into a read operation but does not monitor the output data; this can be observed with a scope connected to the drive data read line, or, for head alignment, the Model T2001 Head Alignment Meter can be used to read the prerecorded dibit signal from a C.E. pack.

Supplementing these automatic operations, the exerciser can also be operated in manual mode; with the FUNCTION SELECT switch at MANUAL, the operator can set up his own tag and bus configuration, then gate them out to the drive separately by operating the applicable enabling switches.

Manual-mode operations are slower but provide a greater degree of flexibility in testing and allow closer observation of the status changes which occur in the indicators. Some operations, like offsetting, can be done only in manual mode.

CIRCUIT DESCRIPTIONS

The following paragraphs describe the basic circuits of the exerciser. How these are used to perform seeks, writes, and reads is explained later under Sequential Operations.

Control and Bit Switches

The functions of these switches are described in Section 2. As they are operated, each of them sets or resets a latch (Figure 3-2) which makes the corresponding signal true or false to the logic. As a typical sequential operation progresses, the pattern set into the BIT switches (BITSW001 thru BITSW512) is looked at by the logic to obtain the bit configuration to be strobed out to the drive on the bus lines. Each of the control switches institutes a particular operation; operating SETCYL, for example, causes the pattern previously set into the BIT switches to be strobed to the drive as the cylinder address.

Function Select Circuit

The FUNCTION SELECT switch and the simple logic combinations in its outputs (Figure 3-3) serve to select the overall mode of operation of the exerciser.

Ready-Delay Circuit (Position Rate Adjust)

The rate at which successive seeks are performed (in any of the continuous seek modes of the exerciser) is adjustable by means of the POSITION RATE control. This potentiometer controls the reaction time of the exerciser seek circuits to the raising of RDY (drive ready) through a time-delay circuit, employing a unijunction transistor; this is the ready-delay circuit, shown at the top of Figure 3-3. When RDY comes up from the drive, there is a controllable time interval between this and the raising of RDYDLY, the signal which indicates the "ready" condition to the exerciser seek circuits. Thus, the longer this time interval, the longer the exerciser will wait after the completion of one seek before starting another, and the number of seeks occurring over a given period will vary accordingly.

Referring to Figure 3-3, the ready-delay circuit operates as follows: With RDY low, the latch whose reset side generates RDYDLY/ will be reset, keeping RDYDLY false. When RDY does come up, the unijunction transistor (Q1) will not trigger immediatley, but only after a time delay established by the R/C ratio between R_T (essentially the POSITION RATE pot) and C_T, the timing capacitor. When the charge on C_T reaches the Q1 triggering level, the resulting positive output of the unijunction transistor turns on the switching transistor (Q2), presenting a low to the set side of

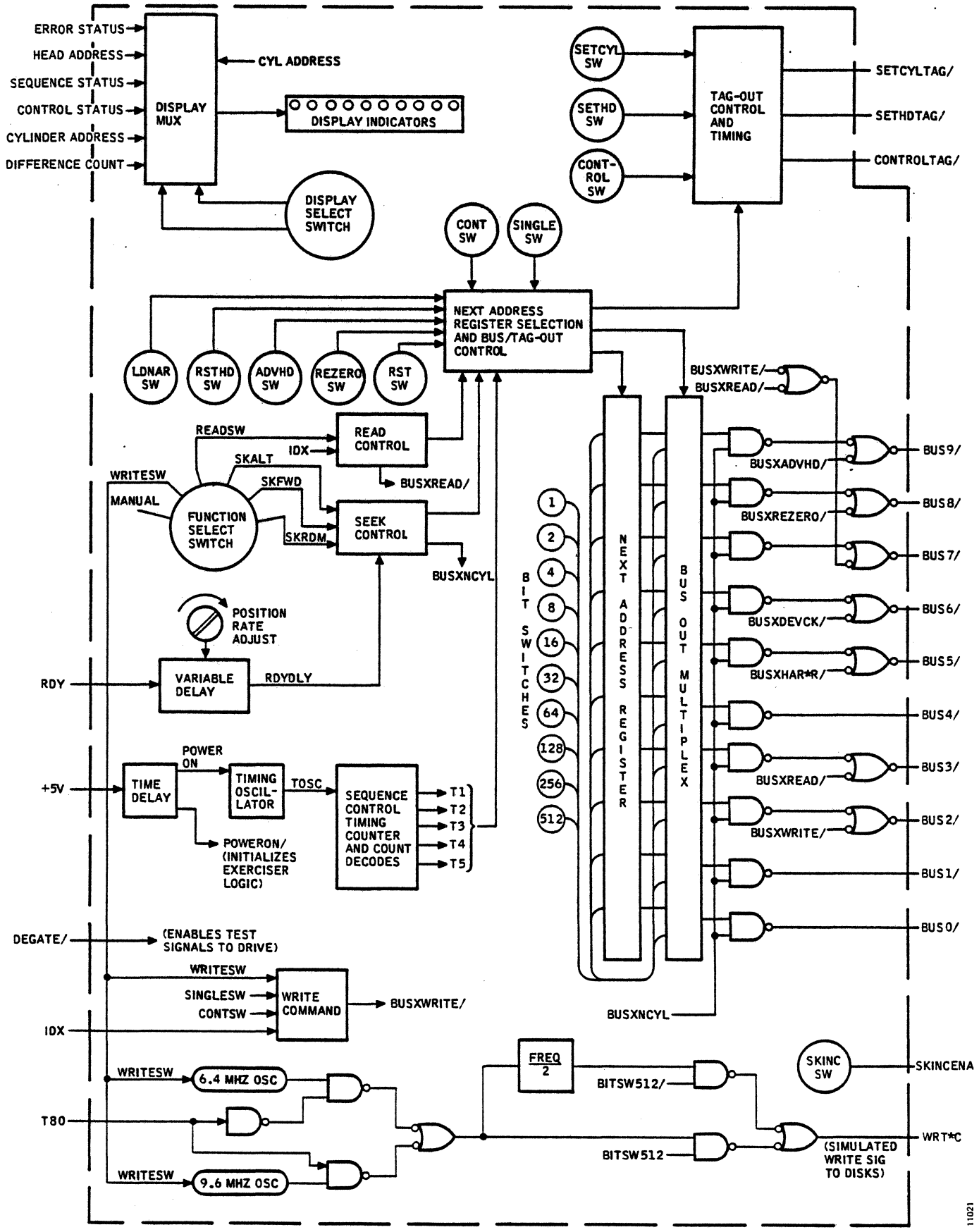


Figure 3-1. Exerciser Functional Block Diagram

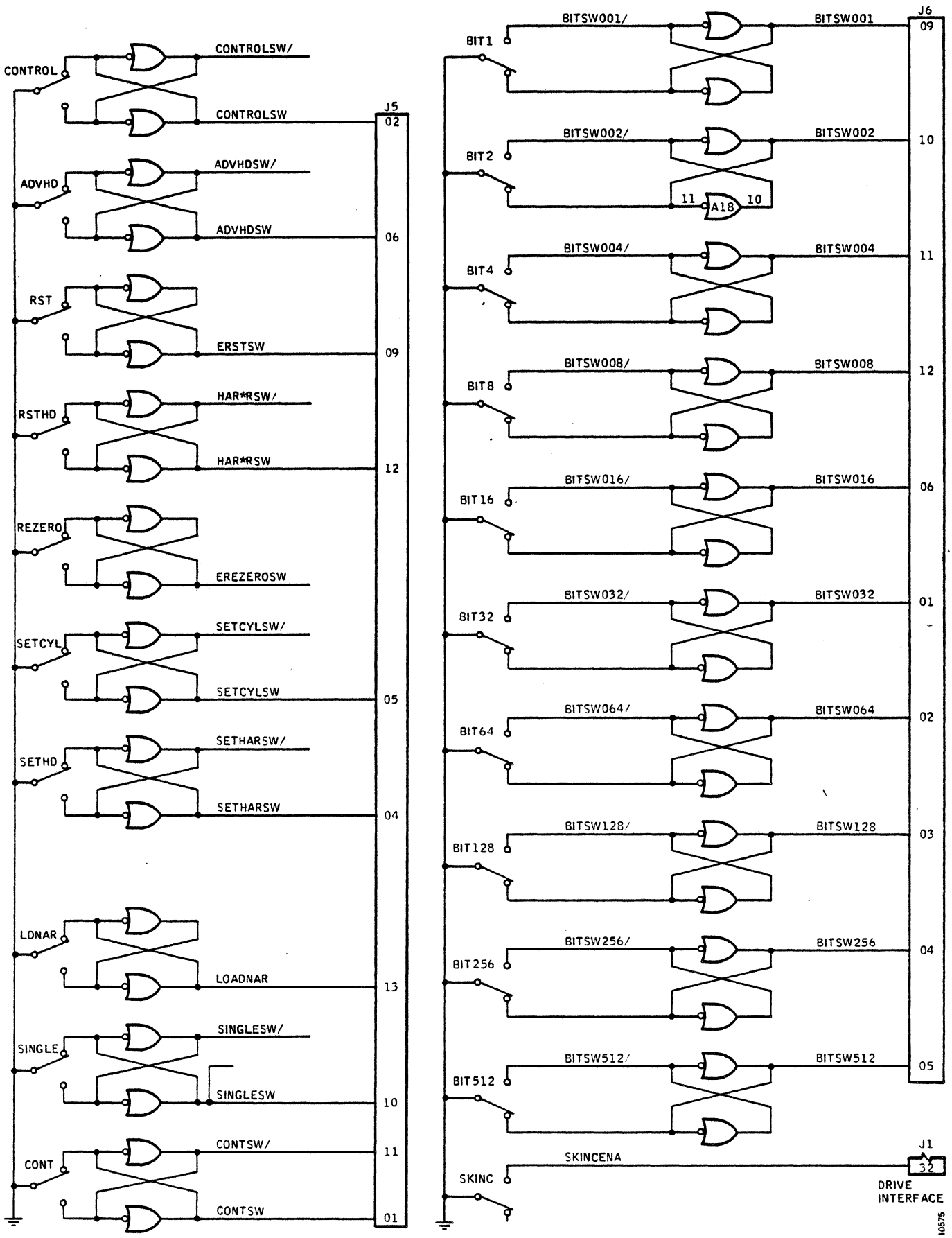


Figure 3-2. Control and Bit Switches, Logic Diagram

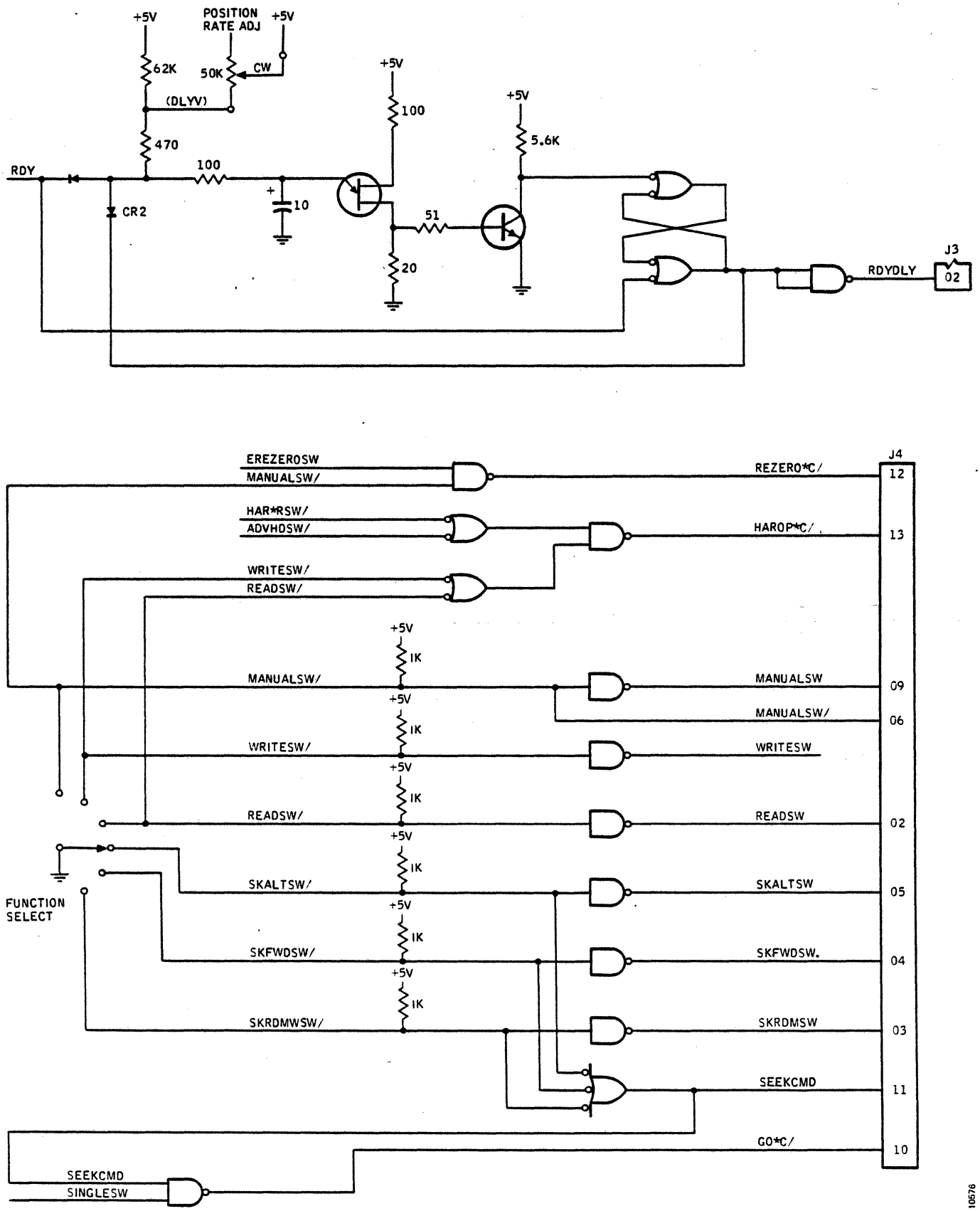


Figure 3-3. Function Select and Ready-Delay Circuit

the latch; the latch sets, raising RDYDLY to the exerciser seek control circuits, and a seek command sequence is sent to the drive.

To complete the cycle, RDYDLY/ is fed back through CR2 to the trigger input of the unijunction transistor. When RDYDLY/ goes low with the setting of the latch, this shuts off the unijunction transistor, and, in its turn, Q2, removing the low at the set input to the latch. When RDY drops, as the drive starts its seek, the low at its reset input resets the latch and returns the circuit to the initial condition, awaiting another RDY at the completion of the seek.

Sequence Control

Five of the functions performed by the exerciser – seek, rezero, reset head, advance head, and reset device check – are controlled by the four flip-flops at the top of Figure 3-4, in conjunction with the timing circuit of Figure 3-5.

Once the function is set into its flip-flop by the switch term, it is clocked out by the timing circuit to raise, in the correct order, the required bus and tag signals to the drive. This process is described in more detail in later paragraphs covering the operational sequences.

Power-On Initialization and Timing Oscillator

These two circuits are shown in Figure 3-4. They are associated only to the extent that the power-on sequence starts the timing oscillator after the other logic has been initialized. When +5-volt power is first applied to the exerciser (by plugging it in and powering up the drive), Q1 is turned on by the positive voltage at its base and Q2 is off because of the delay interposed by the charging time of C35. Thus, initially, POWERON/ is false and, in this state, initializes the logic by resetting key flip-flops and counters. Then when C35 becomes charged, the resulting positive voltage at the base of Q2 turns on Q2, turning off Q1. POWERON/ goes true and is NANDed with TOSC/, which will also be true as its one-shot has assumed its stable state, to produce a negative transition at the input of the first one-shot of the timing oscillator; the one-shot fires and this starts the oscillator.

The timing oscillator consists of two one-shots in series, each with a 1-microsecond on-time. After the first is fired by POWERON/, it remains on for a microsecond, then times out and fires the second, sending TOSC true for a microsecond. As TOSC times out, its complement, TOSC/, goes true and this produces another negative excusion at the input of the first one-shot; it fires, times out, fires TOSC, and the process is self-perpetuating, developing a system clock with a 2-microsecond cycle time.

Sequence Control Timing

The clock signal from the timing oscillator, TOSC, is applied to the clock input of a binary counter (Figure 3-5) to develop six sequential timing signals which are used to control automatic operations sent to the drive. The counter is initially set to zero at POWERON, then, when the timing oscillator starts to run, it advances in count once at each TOSC/. The outputs of the counter are fed to a decoder which generates the separate timing signals in sequence as the count increases. CNT0 is fed back to the sequence control circuit (Figure 3-4) where its effect is to allow initiation of a function only when the counter is starting a sequence; then, as T1 thru T5 are generated, the next address register (NAR) is operated and bus and tag configurations are put on the lines to the drive in the correct order to cause seek, rezero, advance head, reset head, and device check operations as shown in the small table included in Figure 3-5. Also see later paragraphs in this section describing the operational sequences.

Tag Signal Generation

The logic which generates tag signals to the drive is shown in Figure 3-6. When the desired function has been set up by the control switches, the tag is raised to strobe the bus lines. Note that all three tags are enabled by the degate signal from the drive, ensuring that the drive is offline to its controller before testing with the exerciser can be accomplished.

Write Circuit

The exerciser performs a write operation by sending to the disks a write data signal in one of two fixed patterns, selectable from its front panel. With BIT switch 512 in the H.F. position, the signal is a square wave of the correct frequency to generate one data transition for each data-cell bit time. The resulting recording will be a string of all ones or all zeros, depending on whether the drive logic happens to sync up to receive these data transitions as data bits or as clocks. This is because the exerciser write signal is not a meaningful data pattern as would be received from the controller online; there are no data gaps or sync characters and therefore the drive logic has no information from which it can determine whether the string of bits consists of ones or clocks.

With BIT switch 512 in the L.F. position, the exerciser write signal is at half the data cell frequency. This will always be received as alternate ones and zeros; the lack of sync information will only cause the choice of which of each pair of data cells is the one or the zero to be random.

The T2000B also has two basic write signal frequencies which are divided by two, or not, depending on the position

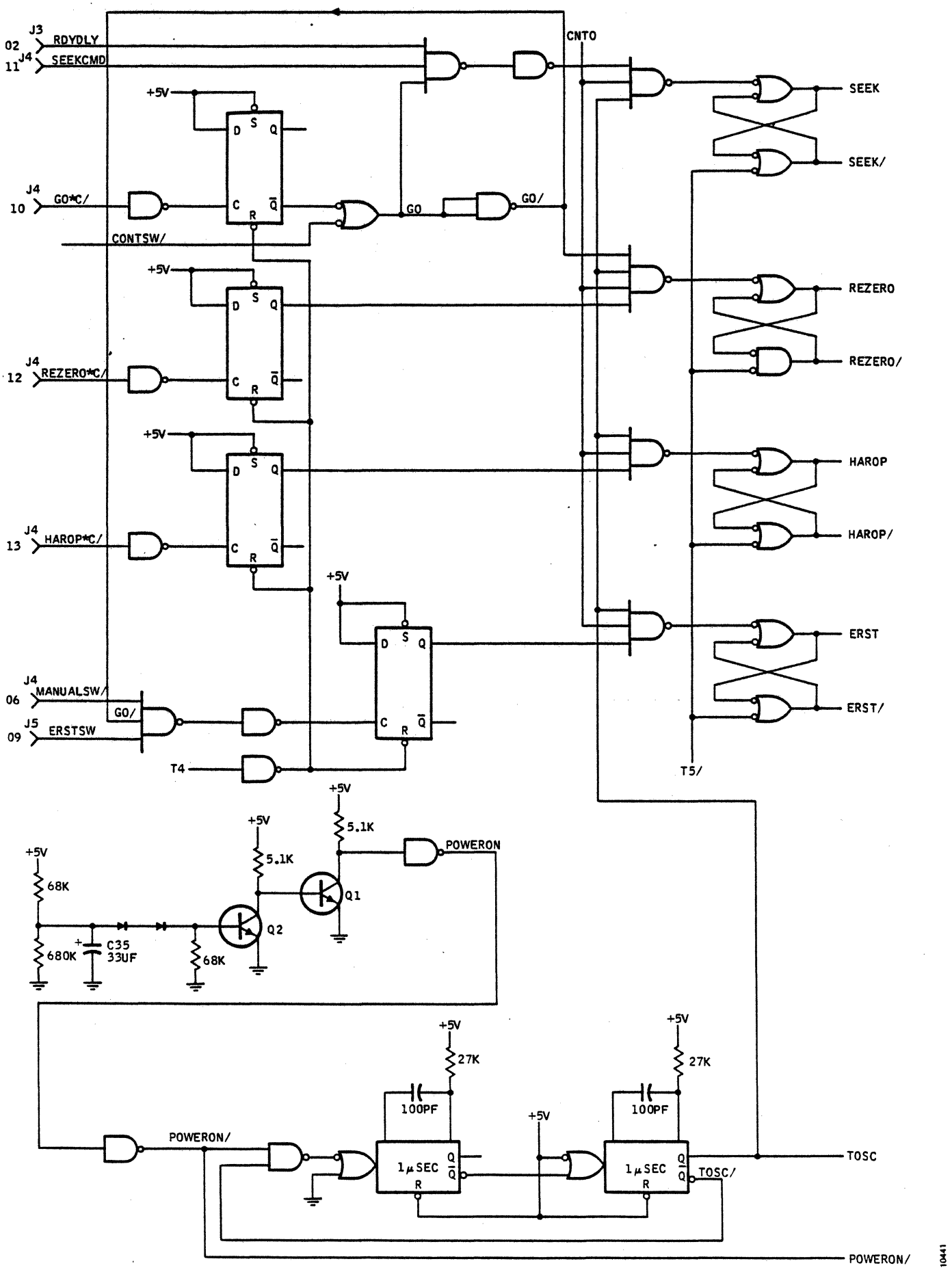
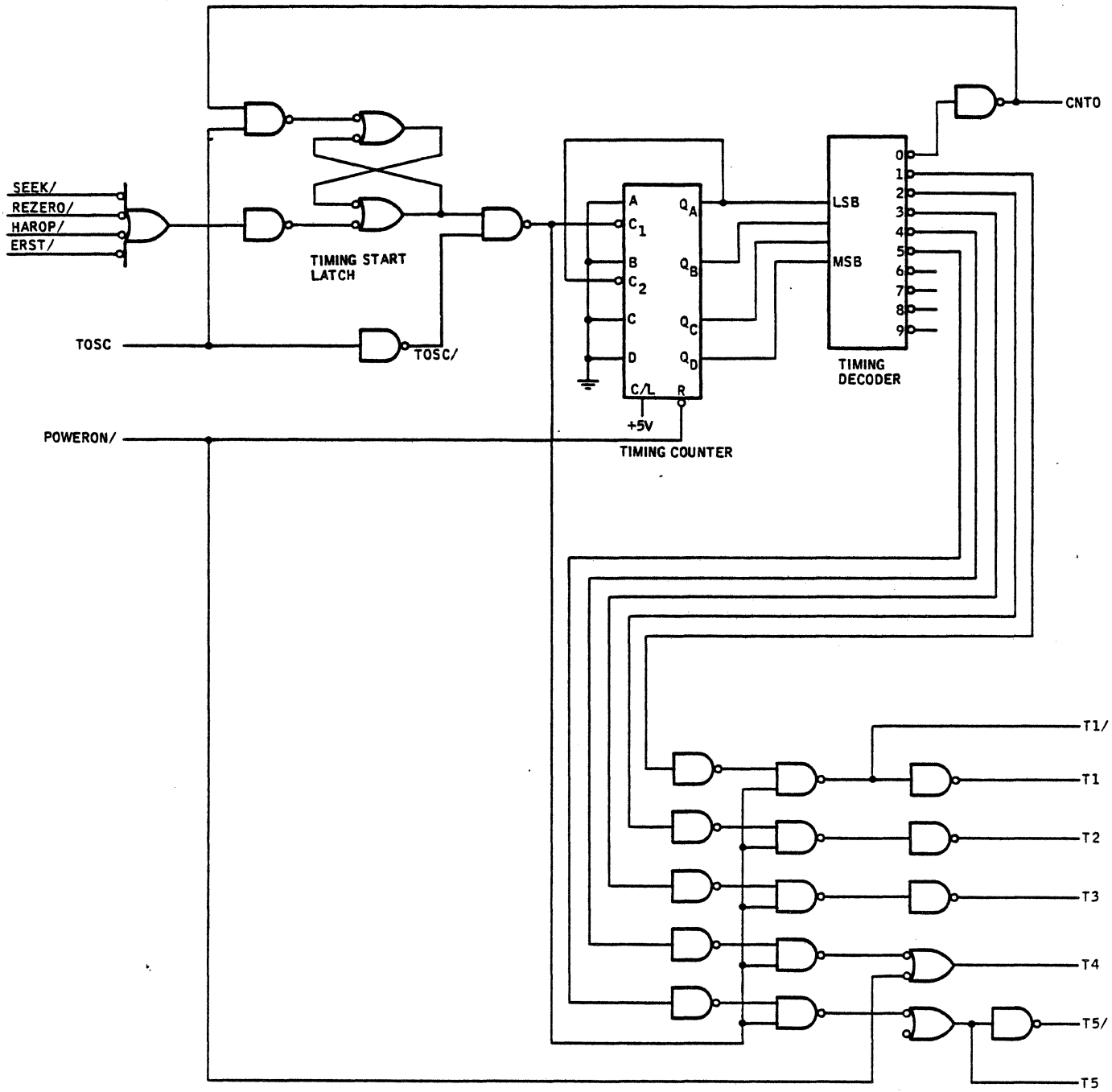


Figure 3-4. Sequence Control, Power-On Initialization, and Timing Oscillator



CONTROL TIMING SEQUENCES					
TIME	SEEK	REZERO	ADHAR	RSTHAR	DEVCK*R
T1	NARSTOP				
T2	BUSXNCYL	BUSXREZERO	BUSXADVH	BUSXHAR*R	BUSXDEYCK*R
T3	SETCYLTAG	CONTROLTAG	CONTROLTAG	CONTROLTAG	CONTROLTAG
T4	DROPBUS	DROPBUS	DROPBUS	DROPBUS	DROPBUS
T5	STARTNAR/ADV				

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Figure 3-5. Sequence Control Timing Logic

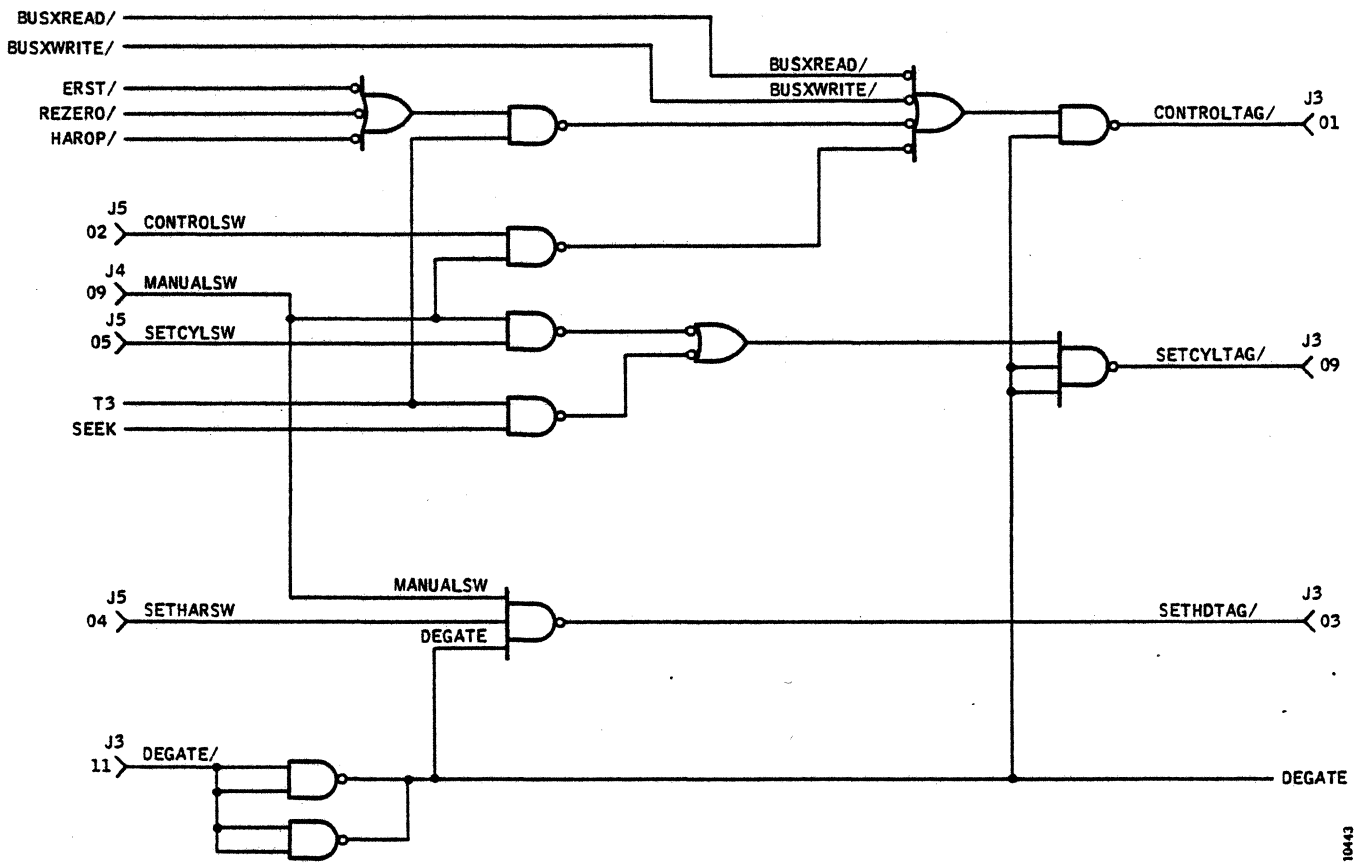

Figure 3-6. Tag Signal Generation

of BIT switch 512. The higher of these, 9.6 MHz, is used for Model T80 and T300 drives, while the lower, 6.4 MHz, is for other Trident models. The exerciser logic selects one of these automatically when it is plugged into the drive. If the drive is a T80 or T300, a logic signal, (T80) wired true in the drive, causes the 9.6 MHz oscillator in the exerciser to be enabled; if this signal is false, the 6.4 MHz oscillator runs to supply the basic write frequency.

Write operations are implemented by the circuit shown in Figure 3-7; it consists of a pair of control flip-flops that generate the write command and the two oscillators that supply the basic write signals. Once the exerciser has been connected to the drive and the T80 term (or T80/) has enabled the correct oscillator, a write operation is instituted by placing the FUNCTION switch in WRITE. From this, the WRITESW term starts the enabled oscillator running and also enables SINGLESW or CONTSW to the first control flip-flop. If CONT is then turned on or SINGLE pressed, the first flip-flop sets. With this flip-flop set, the circuit waits for the disk rotation to reach the index mark; when this occurs, the IDX term sets the second control flip-flop, generating BUSXWRITE. BUSXWRITE sets Bus 2 and Bus 7 (Figure 3-10) and raises the control tag (Figure 3-6). Thus the disk receives a write command, goes into write mode, and begins to record the data pattern already coming over the WRT*C line.

If the SINGLE switch was used to start the write, the operation will continue only until index is again reached at the end of the track because BUSXWRITE/, being enabled to the reset input of the first flip-flop by CONTSW/, will reset the first flip-flop. With this flip-flop reset, the next IDX resets BUSXWRITE and removes the write command from the bus lines. If the CONT switch is on, this will not occur and the write will continue.

Bus Signal Generation

The logic which generates the bus signals to the drive is shown in Figure 3-8. Except for BUSXREAD/, each of these latches is set when its activating control switches are on and T2 arrives from the timing oscillator; they are reset at T4. The latch outputs go to the bus-out selection circuit to enable the bus configurations that command the drive to perform the functions. (See Bus-Out Selection, below.)

Next Address Register

The next address register (Figure 3-9) is used during seek alternate operations to hold one of the two cylinder

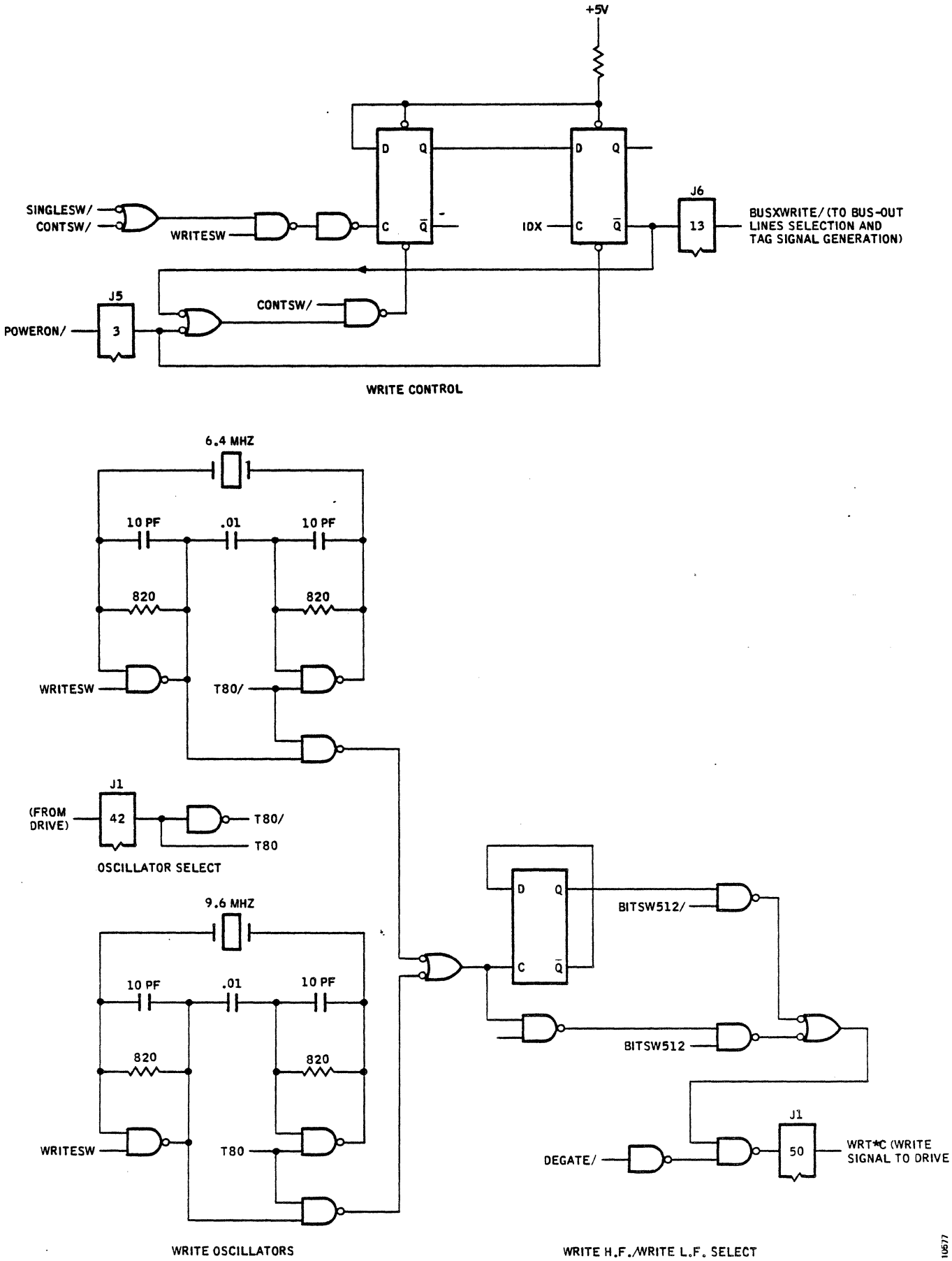

Figure 3-7. Write Circuit

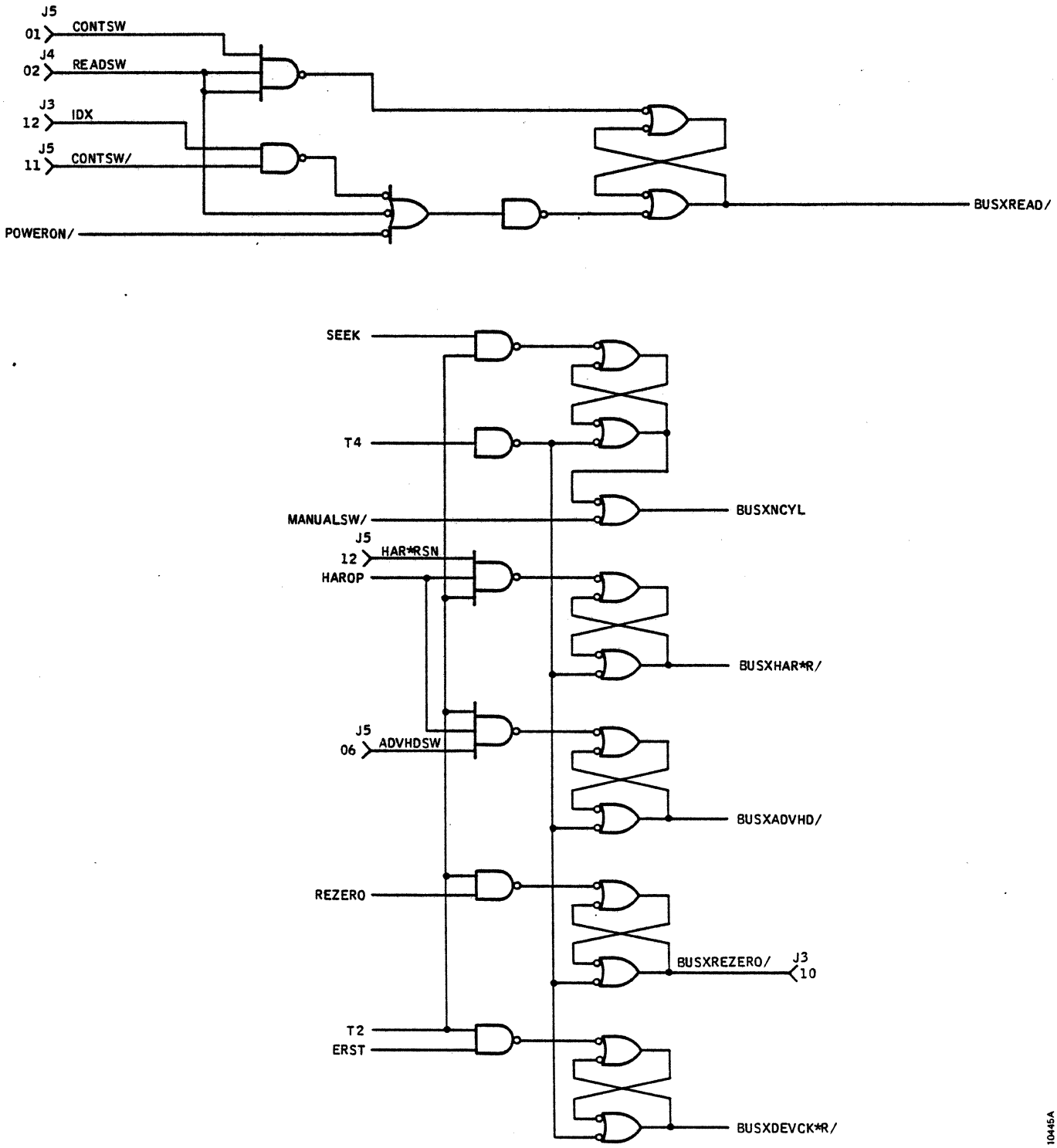

Figure 3-8. Bus Signal Generation

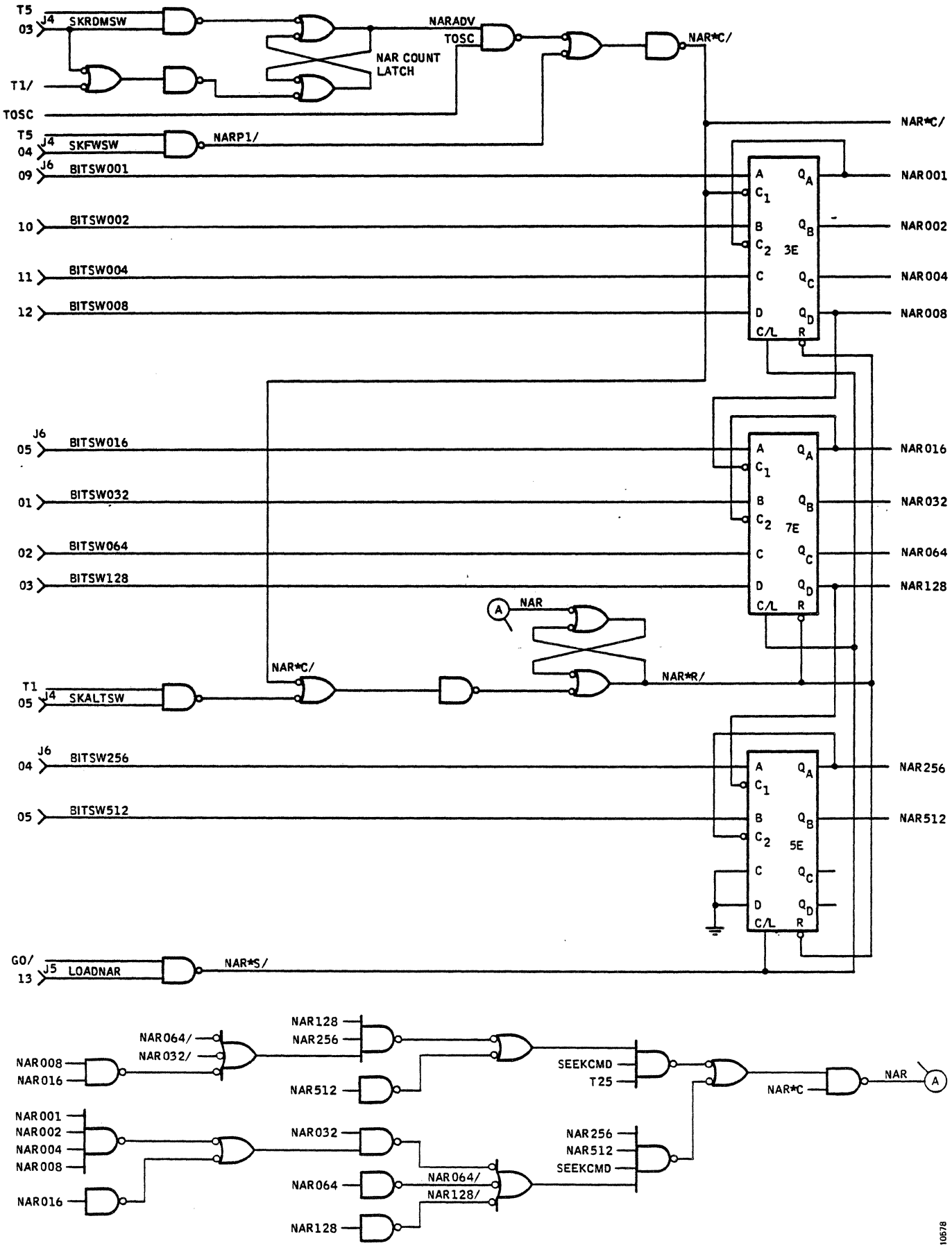

Figure 3-9. Next Address Register

addresses between which the drive is made to seek (the other is in the bit switches) and in seek forward and seek random operations to generate the successive cylinder addresses required by these functions.

To accomplish this, the next address register is equipped with control logic which loads it with the address set into the bit switches at the start of a seek operation, counts it up during forward and random seeks, and resets it when an illegal cylinder address (greater than the highest cylinder number for the drive) is reached or set in initially. The details of this control logic are as follows:

- Load

NAR*S = GO/ LOADNAR	(Load with LDNAR switch)

- Count

NAR*C = NARADV TOSC	(Count up as TOSC runs) (Random seeks)
+ SKFWSW T5	(Advance once at T5) (Forward seeks)
NARADV = SKRDMSW T5	(Set latch to start count at T5)
NARADV/ = T1	(Reset latch to stop count at T1 or switch off)
+ SKRDMSW/	

- Reset

NAR*R = NAR	(Set latch to reset next address register at count greater than highest cylinder number, 407 for T25 drives, 814 for others)
NAR*R/ = NAR*C	(Reset latch at count start)
+ SKALTSW T1	(Reset latch at alternate seek)

Bus-Out Selection

Signals placed on the bus lines to the drive are selected by the logic shown in Figure 3-10. The cylinder number, NCYL001 thru NCYL512, is sent out during seek operations; it is derived from the output of the multiplexer whose inputs are the BIT switches and the next address register (Figure 3-9) and is enabled to the bus lines by BUSXNCYL (from Figure 3-8). The multiplexer is operated (by the NARSEL flip-flop) to select alternately the BIT switches and the next address register during automatic alternate seek operations; this control sequence is described later.

When the FUNCTION SELECT switch is in SKFWD or SKRDM (not in SKALT), then SKALTSW/ at the set input of the NARSEL flip-flop holds the flip-flop true and the multiplexer is held selecting only the next address register as the source of cylinder numbers put on the bus lines during seek random and seek forward operations.

When the FUNCTION SELECT switch is in MANUAL, then the multiplexer is held selecting only the BIT switches and the next address register is not used. Also, in MANUAL, enabling term BUSXNCYL (from Figure 3-8) is always true, making the multiplexer output, and, therefore, the BIT switch signals, the *only* source for the bus lines. This is because in manual operations all bus configurations are set in with the BIT switches and then strobed to the drive with the appropriate switch-generated tag signal.

When the operation is an automatic head advance, rezero, device check reset, head address register reset, write, or read, the appropriate bus lines are enabled (set to zero) by the gating shown to the right of the multiplexer. The control signals which do this are generated in the logic of Figure 3-8.

No bus signals go to the drive unless the DEGATE signal is up. This signal originates in the disk drive itself, when the DEGATE switch is activated, ensuring that the drive is off-line to its controller before it can be operated from the exerciser.

Display Indicator Circuit

The exerciser display indicators are driven by signals from the drive, except when the DISPLAY SELECT switch is in EX CAR. In this case the bottom row of indicators contain the number standing in the exerciser's own cylinder address register, ready for transmission to the drive in a seek operation. The functions of all indicators are listed in Section 2.

As shown in Figures 3-11 and 3-12, signals are applied to the LED indicators via a set of four-to-one multiplexers which are, in turn, under control of the DISPLAY SELECT switch operating through display select MUX A31. The display select MUX is a quad two-to-one chip (or eight-to-four as sometimes described) whose input array selection is determined by the state of the term T200/ from the drive. When T200/ is false the drive is either a T200 or T300 (not a T25, T50, or T80) and the exerciser display select circuit is switched to accomodate the different signal arrays received from T200/300 drives. (See Figure 3-13.) Also, when operating with T200/300 drives, the exerciser display select circuit develops and sends to the drive, the signal ECNT+DIFF. This signal tells the drive that the exerciser is calling for either a control or difference count signal-set (not drive CAR) and the drive logic puts the desired

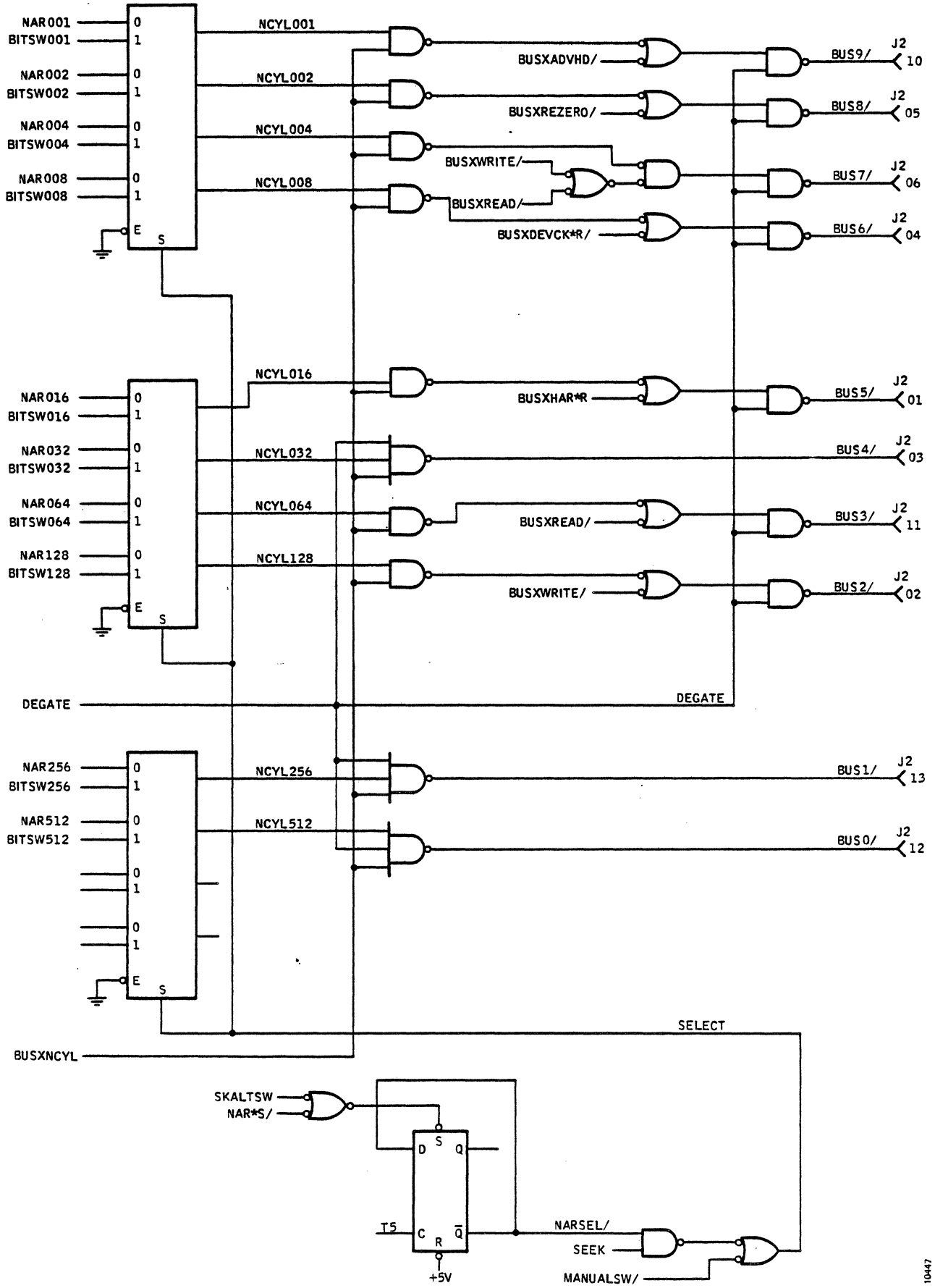

Figure 3-10. Bus-Out Lines Selection

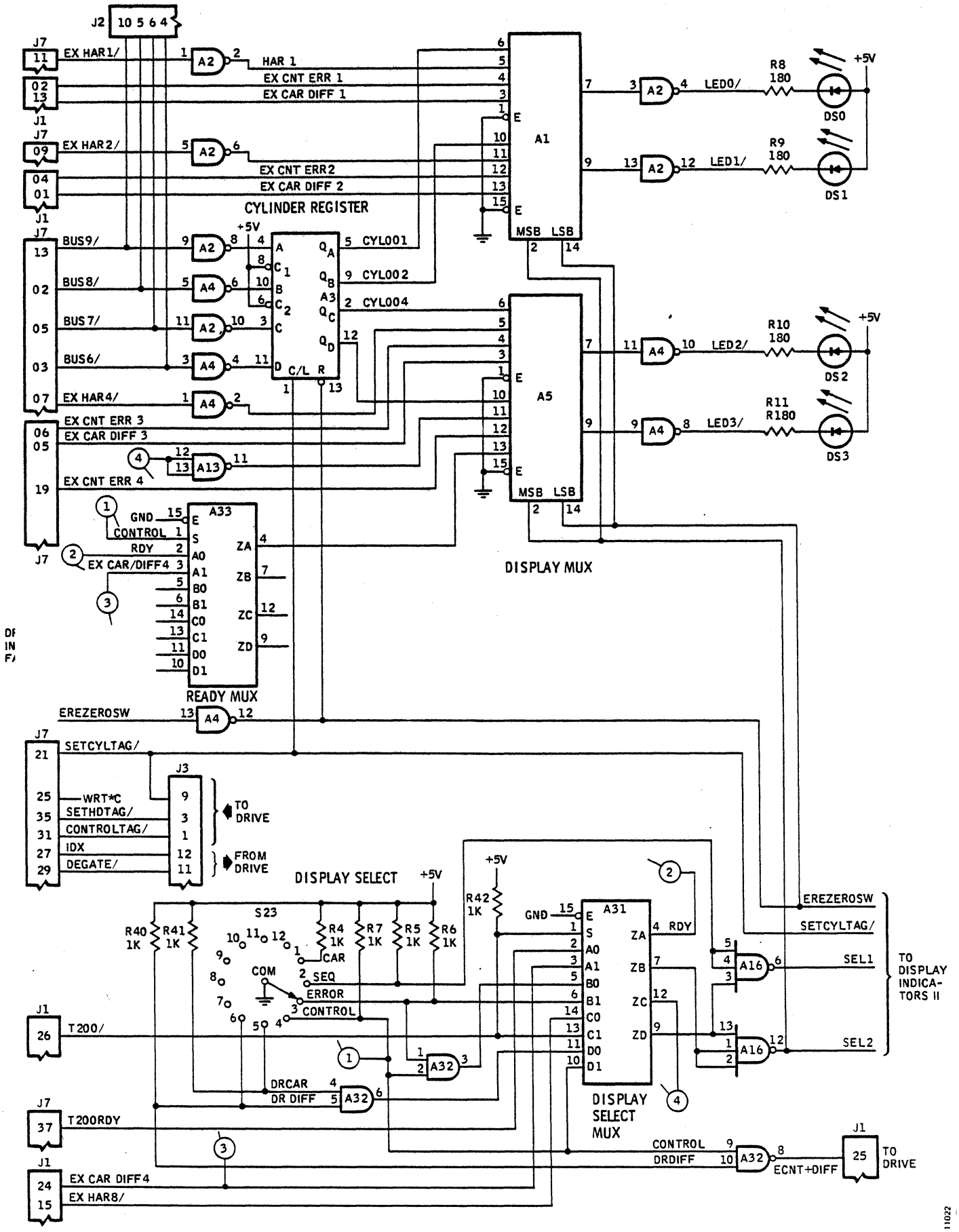

Figure 3-11. Display Indicators I

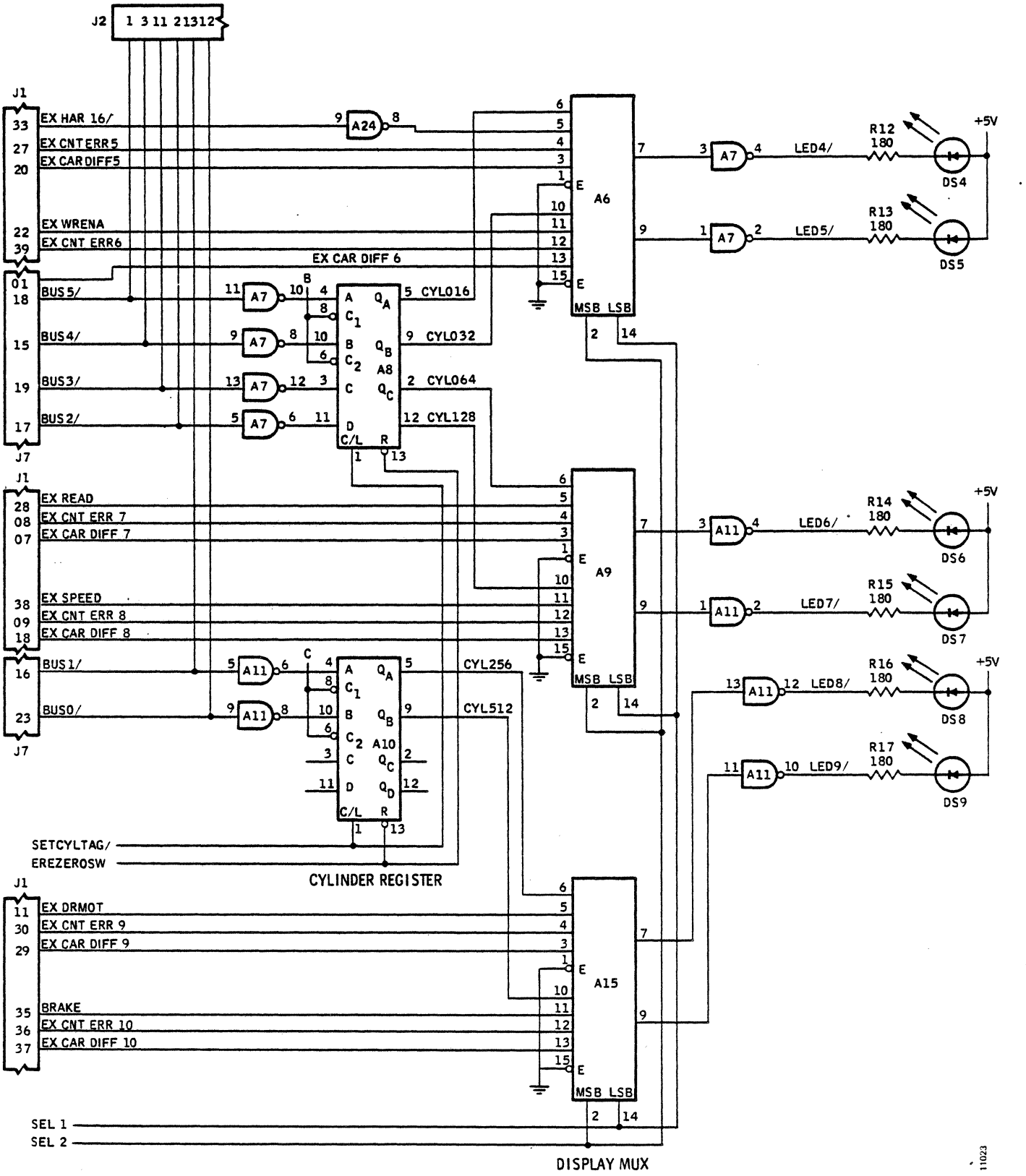

Figure 3-12. Display Indicators II

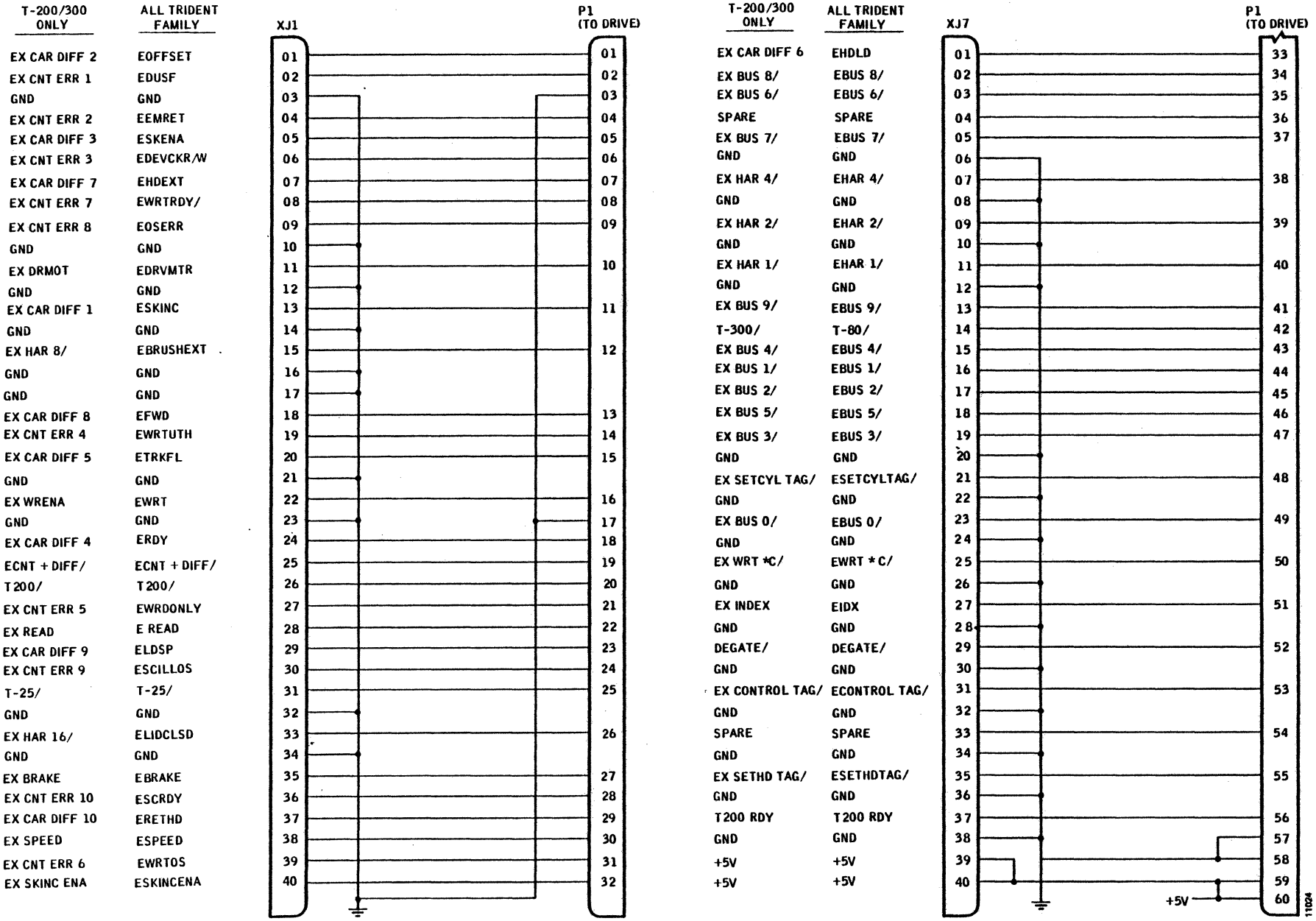

Figure 3-13. Drive Interface Signal Schematic

signals on the lines. This function, in conjunction with the selected state of the display select MUX, modifies the operation of the indicator multiplexers to select the correct display at each of the six positions of the DISPLAY SELECT switch.

The display select MUX provides one other function. Note, from Figure 3-13, that the drive-ready signals from the two types of drives (T200RDY or RDY) do not come into the exerciser on the same line. As the display select MUX is switched by the signal T200/ true or false, the exerciser internal RDY signal (which goes to the ready-delay circuit) is connected to and driven by the correct one of these drive-ready lines.

SEQUENTIAL OPERATIONS

When the exerciser is operated in automatic mode, signals sent to the drive and, therefore, the operation commanded, are generated by sequential control logic within the exerciser. Seeks, rezeros, head advances, head address resets, and device check resets are under control of the sequence control timing logic of Figure 3-5. Necessary control settings are made, of course, and the operation is started by turning on the CONT switch or pressing SINGLE, but then the sequence of events proceeds in sync with the timing oscillator which drives the timing counter to generate the six sequential signals, CNT0, T1, T2, T3, T4, and T5. Each time the counter cycles, the required bus-out configuration is placed on the bus lines, the tag is raised to strobe it out, and then the buses are dropped. To the drive, the operation appears the same as when it is functioning from its controller, online.

Write and read operations are also automatic, but the timing oscillator is not used in their implementation; they have separate control circuits.

Sequential operations are described in the following paragraphs.

Seek Alternate

Alternate seek operations (back and forth between two selected cylinders) are accomplished by using both the next address register and the BIT switches as sources of cylinder addresses. The first of the two cylinder numbers is initially loaded into the NAR from the BIT switches, then the BIT switch pattern is changed to the second cylinder number and left there. Then, with the FUNCTION SELECT switch in SKALT, turning on the CONT (or SINGLE) switch activates the sequence control timing logic to command a seek, first to the address in the NAR, then to the address in the BIT switches, back to the NAR address, and so on.

Details of this operation are as follow: (Refer to the logic in Figures 3-4, 3-5, 3-6, 3-8, 3-9, and 3-10).

SEEK ALTERNATE OPERATION	LOGIC FUNCTIONS
1. Set BIT switches to first cylinder number	(No op)
2. Press LDNAR	Loads the next address register from the BIT switches: NAR*S = LOADNAR GO/ (CONT switch not on) Sets NARSEL to enable next address register out to the bus lines on the first seek: NARSEL = NAR*S
3. Set BIT switches to second cylinder	(No op)
4. Set FUNCTION SELECT to SKALT	SKALTSW enables toggling of NARSEL at each timing cycle
5. Turn on CONT switch or press SINGLE	Raises GO to set the SEEK latch and start the timing cycle. (CNT0, counter at zero, is true after a previous timing cycle or at power-on.) GO = CONTSW (Continuous seeks) + SEEKCMD (Single seek) SEEK = RDYDLY SEEKCMD GO CNT0 TOSC Enable NAR to bus-out multiplexer if NARSEL, or Enable BIT switches to bus-out multiplexer if NARSEL/: SELECT/ = NARSEL (1st and odd seeks) SELECT = SEEK NARSEL/ (2nd and even seeks)

SEEK ALTERNATE OPERATION	LOGIC FUNCTIONS
6. TIMING CYCLE RUNS	The timing counter, which has been holding at CNT0, starts to run at the first TOSC after SEEK resets the timing start latch.
T1	(No op)
T2	Set BUSXNCYL latch to enable bus-out multiplexer (cylinder number) to bus lines: BUSXNCYL = SEEK T2
T3	Enable SETCYL tag: SETCYLTAG = SEEK T3
T4	Reset BUSXNCYL latch: BUSXNCYL/ = T4
T5	Reset SEEK: SEEK/ = T5 Toggle NARSEL to reverse selection of NAR to BIT switches at CNT0 of next cycle:

7. The timing counter continues to run through count = 9 and returns to CNT0 where it will hold if the CONT switch is off because CNT0 sets the timing start latch, disabling the counter.

8. If the CONT switch is on, the next seek (to the second cylinder) will occur as soon as RDYDLY comes up after the delay set in with the POSITION RATE control.

9. If SINGLE was pressed in step 5 to start the operation, then it must be pressed again to start another timing cycle and the seek to the second cylinder.

10. At each seek, the state of NARSEL is reversed (at T5), selecting, at the set state, the next address register or, at the reset state, the BIT switches, to be strobed on to the bus lines. Thus seeks will alternate between the cylinder addresses selected in steps 1 and 3.

11. The seek alternate operation is also used to seek to a single cylinder by loading the desired cylinder number into the next address register and pressing SINGLE once. This is simply the first half of a seek alternate operation.

Seek Forward

In forward seek operations, cylinder addresses are taken from the next address register which is automatically advanced once at each sequence control timing cycle, causing the disks to seek forward one cylinder at a time. When the highest-numbered cylinder is reached, the NAR resets to zero and the seeks proceed from cylinder zero through maximum again; this will continue as long as the CONT switch is left on (or the SINGLE switch is pressed). Forward seeks will start at the cylinder address standing in the next address register; that is, the first seek will be to this cylinder from wherever the heads are positioned, and subsequent seeks will go forward from this point in increments of one. Therefore, to start with cylinder zero and go throughout the pack, it is necessary to load the NAR with all zeros at the beginning. (One may start at any desired cylinder, of course).

Note that in forward seek operations the NARSEL flip-flop (Figure 3-10) is held in the set state by SKALTSW/ (FUNCTION SELECT not at SKALT) and this keeps the bus-out multiplexer always reading the NAR output, not the BIT switches.

A seek forward is processed through the logic as follows. Refer to Figures 3-4, 3-5, 3-6, 3-8, 3-9, and 3-10.

SEEK FORWARD OPERATION		LOGIC FUNCTIONS
1	Set BIT switches to desired starting cylinder	(No op)
2.	Press LDNAR	Loads the next address register from the BIT switches: NAR*S = LOADNAR GO/
3.	Set FUNCTION SELECT to SKFWD	Puts the sequence control timing logic in seek mode and enables T5 to the count input of the NAR: NARPI = SKFWDSW T5
4.	Turn on CONT switch or press SINGLE	Raises GO to set the SEEK latch and start the timing cycle. (CNT0, counter at zero, is true after a previous timing cycle or at power-on.) GO = CONTSW (Continuous seeks) = SEEKCMD GO*C (Single seek) SEEK = RDYDLY SEEKCMD GO CNT0 TOSC
5.	Timing cycle runs	The timing counter, which has been holding at CNT0, starts to run at the first TOSC after SEEK resets the timing start latch.
	T1	(No op)
	T2	Set BUSXNCYL latch to enable bus-out multiplexer (cylinder number) to bus lines: BUSXNCYL = SEEK T2
	T3	Enable SETCYL tag: SETCYLTAG = SEEK T3
	T4	Reset BUSXNCYL latch: BUSXNCYL/ = T4
	T5	Reset SEEK: SEEK/ = T5 Advance (count up once) NAR: NAR*C = SKFWSW T5

6. The timing counter counts up to maximum, overflows to CNT0 (count zero), then repeats the cycle if the CONT switch is on, seeking this time to the cylinder number now in the next address register. If the SINGLE switch is being used, it must be pressed again to do the next seek.

7. When the highest-numbered cylinder is reached (407 for T25 drives, 814 for others), decoding of outputs of the next address register (Figure 3-9) sets NAR true at the next NAR*C/ and this sets the NAR*R latch which, in turn, resets the next address register to zero; the next seek will be to cylinder zero.

Seek Random

A seek random operation is similar to a seek forward; the next address register is used as the sole source of cylinder addresses and its contents are changed at each sequence control timing cycle to automatically produce a new address. The address change is made at T5 but, instead of a single increment, the register is allowed to count up under control of the timing oscillator, TOSC, until the next seek is started.

A seek random is implemented as follows. Refer to Figures 3-4, 3-5, 3-6, 3-8, 3-9, and 3-10 for the logic functions referred to.

SEEK RANDOM OPERATION	LOGIC FUNCTIONS
1. Set BIT switches to all zeros	(No op)
2. Press LDNAR	Loads the next address register from the BIT switches: NAR*S = LOADNAR GO/
3. Set FUNCTION SELECT to SKRDM	Puts the sequence control timing logic in seek mode and enables T1 and T2 to the NAR count latch.
4. Turn on CONT switch	Raises GO to set the SEEK latch and start the timing cycle. (CNT0, counter at zero, is true after a previous timing cycle or at power-on.) GO = CONTSW SEEK = RDYDLY SEEKCMD GO CNT0 TOSC
5. TIMING CYCLE RUNS	The timing counter, which has been holding at CNT0, starts to run at the first TOSC after SEEK resets the timing start latch.
T1	Reset NAR count latch to stop up-count. NAR*C = NARADV/ NARADV/ = T1 (This operation becomes effective only after the first timing cycle has been completed and the NAR count latch has been set at T5. Note also that SKRDMSW/ holds the NAR count latch reset for all operations other than a seek random).
T2	Set BUSXNCYL latch to enable bus-out multiplexer (cylinder number) to bus lines: BUSXNCYL = SEEK T2
T3	Enable SETCYL tag: SETCYLTAG = SEEK T3
T4	Reset BUSXNCYL latch: BUSXNCYL/ = T4

SEEK RANDOM OPERATION	LOGIC FUNCTIONS
5. TIMING CYCLE RUNS (Continued) T5	Reset SEEK; SEEK/ = T5 Set NAR count latch to start the next address register up-count: NARADV = SKRDMSW T5
6. Next address register up-count runs	With NARADV enabling TOSC to the next address register count input, each pulse from the timing oscillator will count the register up by one. The count will continue as long as CNT0 holds true (step 4, above) or, in other words, until another sequence control timing cycle is initiated with T1. This interval is, in turn, dependent on the length of the RDYDLY time delay as set in by the POSITION RATE Control. Therefore, in seek random operations, the intervals between selected cylinders can be varied with POSITION RATE.

7. As long as the CONT switch is on, the operation will cycle through steps 4 thru 6, counting up the next address register at T5, stopping the count at T1, and doing a seek to the cylinder address then left in the register during timing counts T2 thru T4.

Rezero, Advance Head, Reset Head, and Device Check Reset

These four operations all follow the same pattern. Operating the panel switch sets the applicable control flip-flop (Figure 3-4) to establish the function which will be performed; then the latch for that function sets, starting the sequence control timing cycle (Figure 3-5) which has been holding at CNT0 as described above for the seek sequences. At T2 of the timing cycle, the bus lines are enabled; at T3 the tag goes out; at T4 the buses are dropped and the control flip-flop is reset; it resets the latch. The drive has received its command and should perform the function. Note that the term GO/ is NANDed with the other terms at the set input of the rezero latch. This is to prevent a rezero command (which causes head positioning) from going to the drive while a seek is in porgress.

Write

Write operations are implemented by the special circuit of Figure 3-7. This circuit and its operation during a write are fully described in an earlier paragraph entitled Write Circuit.

Read

A read operation is controlled by the BUSXREAD latch (top of Figure 3-8) and its set/reset logic. With FUNCTION SELECT in the READ position, turning on the CONT switch sets the latch, and BUSXREAD enables bus-out lines 3 and 7 (Figure 3-10), the read command configuration. At the same time, BUSXREAD enables the control tag (Figure 3-6) and this starts the drive on a read operation. When the CONT switch is turned off, the read stops at the next IDX (index) received from the drive.

MANUAL OPERATIONS

With the FUNCTION SELECT switch in MANUAL, all automatic functions of the exerciser logic are disabled, and only the BIT switches are connected to the bus-out lines (by the MANUALSW/ term, Figures 3-9 and 3-10). Also, the CONTROL, SETCYL, and SETHD switches are enabled to the control tag and set head tag logic of Figure 3-6. Thus any command sequence can be sent to the drive by raising BIT switches in the correct bus-out configuration and then pressing the appropriate tag switch.

SECTION 4

ILLUSTRATED PARTS BREAKDOWN

This section contains an illustrated parts breakdown that describes and illustrates all replaceable parts for the Model T2000B Disk Drive Exerciser. The illustrated parts breakdown consists of a Group Assembly Parts List, and Figures 4-1 through 4-3 which illustrate the component parts of the disk drive exerciser and their physical relationships. The component parts are listed in disassembly order with each having an assigned item number. The item number is shown on the accompanying illustration, which portrays its physical location within the assembly.

The purpose of this section is to provide a listing of all items necessary to support the maintenance and overhaul effort for the Model T2000B Disk Drive Exerciser. This illustrated parts breakdown is intended for use in requisitioning, storing, issuing, and identifying replacement parts. This section also serves to illustrate assembly and disassembly relationships.

GROUP ASSEMBLY PARTS LIST

The Group Assembly Parts List consists of a complete breakdown of the Model T2000B Disk Drive Exerciser into subassemblies and detailed parts. Each assembly is listed in its order of disassembly and is followed immediately by its component parts properly indented to show their relationship to the assembly. The Group Assembly Parts List is divided into five columns of information as follows:

- Figure and Item Number
- Part Number
- Description
- Quantity Per Assembly
- Usage Code

Figure and Item Number

The figure number relates the parts list to its associated illustration. The item number assigned to each part is shown on the illustration to show physical location.

Part Number

The Part Number column lists part numbers of all parts replaceable in the unit. Items without a part number are listed as No Number.

Description

Description includes designated and descriptive information necessary to define the items adequately. Entries are indented to indicate their relationship to the next higher assembly. The subheading Attaching Parts within this column lists those parts used for attaching the immediately preceding item, unless otherwise indicated.

The symbol - - - * - - - signifies the end of the attaching parts for the preceding item(s). The symbol NHA refers to the Next Higher Assembly, U/O indicates Used On, NFS indicates Not Furnished Separately, and N/I indicates that the item is not illustrated.

Quantity Per Assembly

The Quantity Per Assembly column contains the number of parts required for each assembly or subassembly. The letters A/R denote that the selection of a part or parts should be made As Required. REF refers to an assembly or item that is shown completely assembled in a preceding illustration or the item is listed for reference only.

Usage Code

The Usage Code column lists part variations within different models, assemblies, or subassemblies of the same equipment. In cases where the column is blank, the listed part will apply to all models, assemblies, or subassemblies listed in this publication.

PURCHASED PARTS

Many parts used in the Model T2000B Disk Drive Exerciser may be obtained directly from a vendor.

Purchased parts will also be supplied by CalComp on receipt of an order specifying the part number as shown in this section. The inclusion of the model designation (such as Model T2000B) and the figure, item number, and description for each part ordered will ensure positive identification of parts.

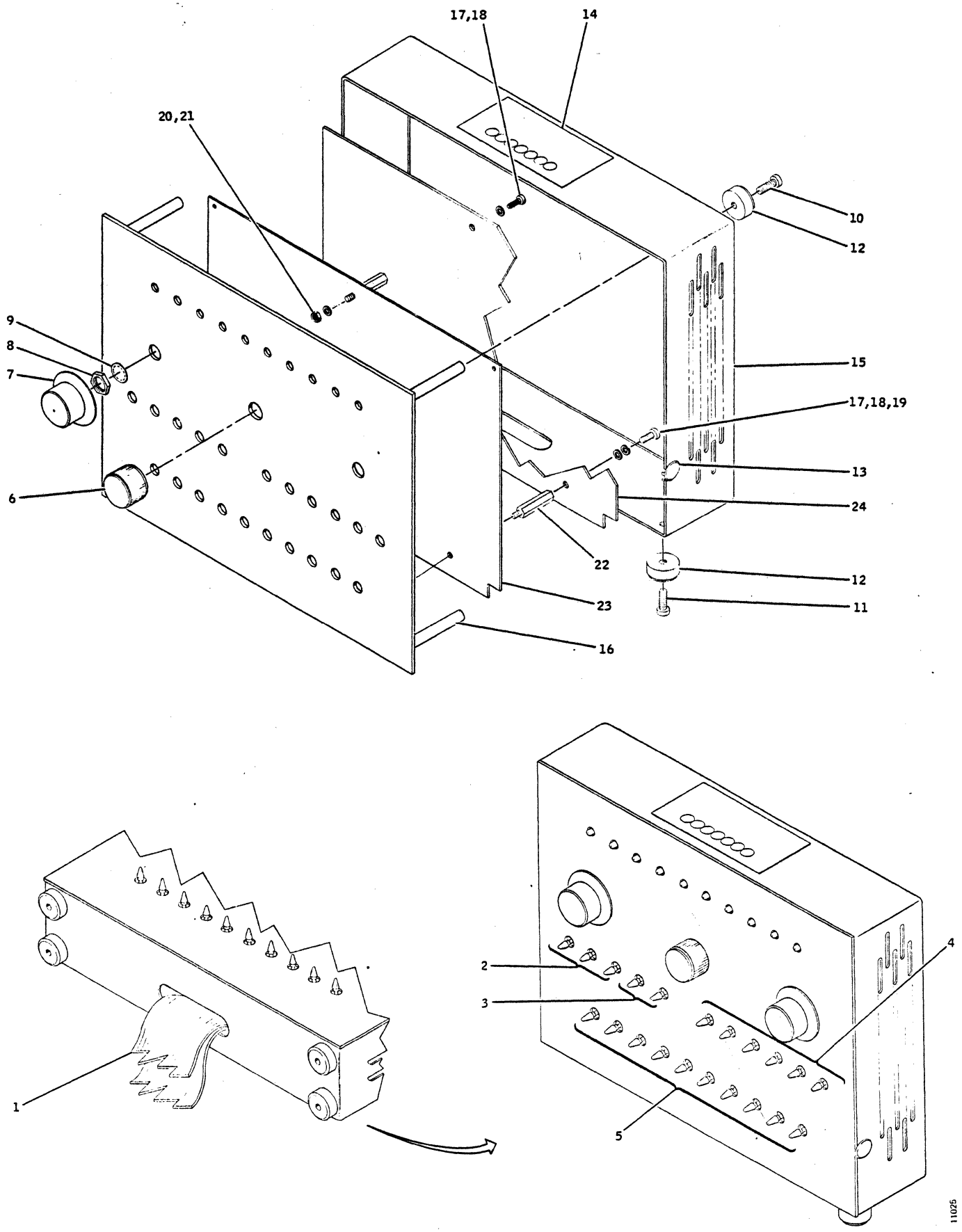

Figure 4-1. Model T2000B Exerciser Assembly

FIGURE ITEM NO.	PART NUMBER	DESCRIPTION	QTY PER ASSY	USAGE CODE
1-	18327-001	Exerciser Assy, Model T2000B	REF	
-1	16639-001	. Cable Assy, Interface	1	
-2	90879-002	. Cap, Plastic, Black	3	
-3	90879-005	. Cap, Plastic, Yellow	2	
-4	90879-002	. Cap, Plastic, Black	6	
-5	90879-009	. Cap. Plastic, White	10	
-6	90512-013	. Knob, Round, .25 Dia Shaft	1	
-7	90513-013	. Knob, Round, Skirted	2	
-8	98874-001	. Nut, Hexagon, Thin	2	
-9	90490-008	. Lockwasher, Internal Tooth	2	
-10	90448-020	. Screw, Pan Hd, 6-32 x .50 Lg	4	
-11	90448-018	. Screw, Pan Hd, 6-32 x .38 Lg	4	
-12	90529-008	. Bumper, Rubber	8	
-13	93182-005	. Plug, Hole	1	
-14	91598-001	. Plate, Indeitication	1	
-15	17232-xxx	. Chassis, Exerciser	1	
-16	17233-121	. Panel, Exerciser	1	
-17	90448-009	. Screw, Pan Hd, 4-40 x .38 Lg	3	
-18	90489-002	. Lockwasher, Split	3	
-19	90488-003	. Washer, Flat	2	
-20	90487-003	. Nut, Hexagon	1	
-21	90693-002	. Washer, Flat, Fiber	1	
-22	96946-020	. Spacer, Hexagon	3	
-23	17070-001	. Board Assy, Operator Control, VL22 (refer to Figure 4-2 for components)	1	
-24	15527-001	. Board Assy, Logic Control, GL22 (refer to Figure 4-3 for components)	1	

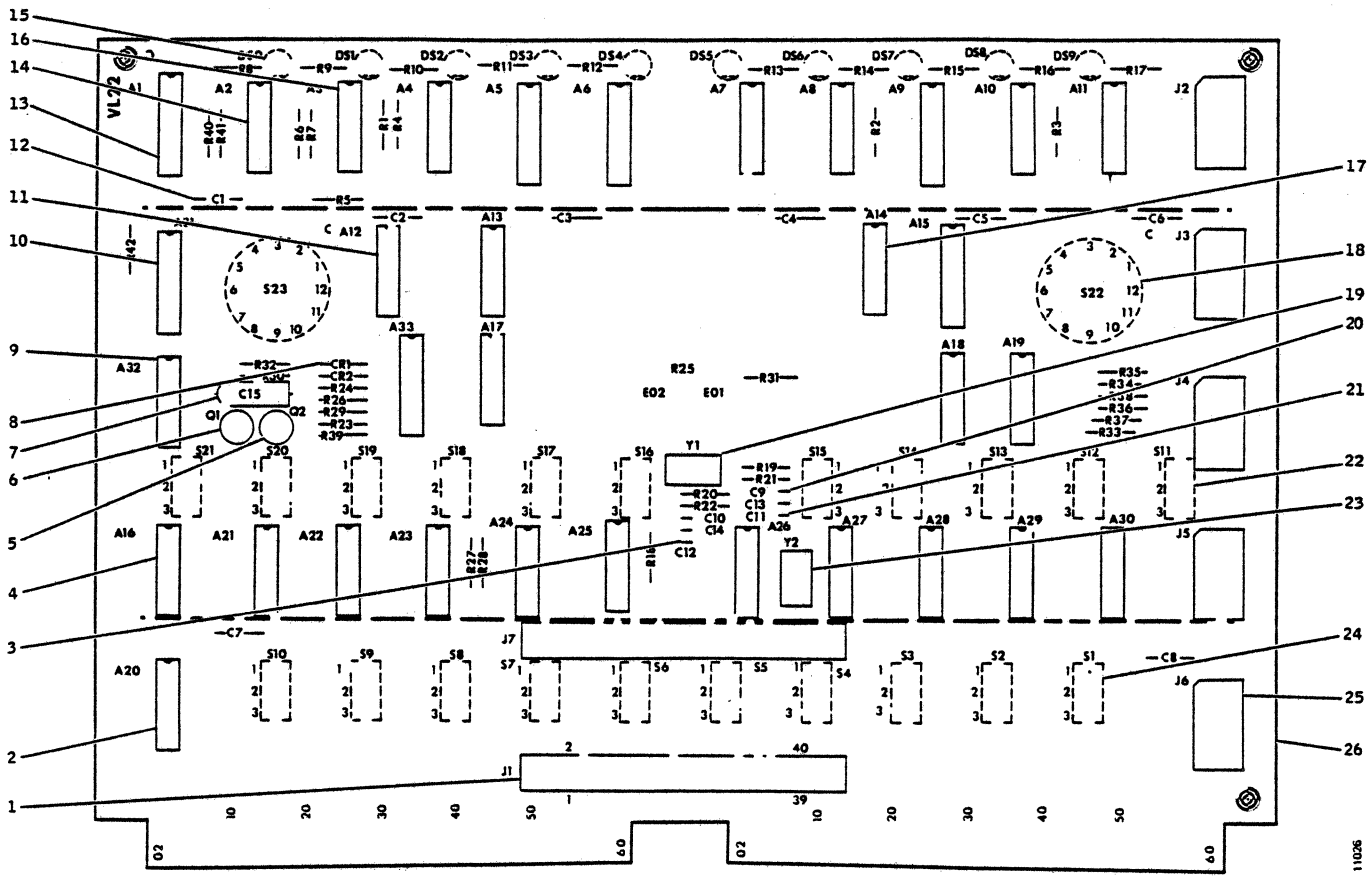

Figure 4-2. Operator Control Board Assembly, VL22

FIGURE ITEM NO.	PART NUMBER	DESCRIPTION	QTY PER ASSY	USAGE CODE
2-	17070-001	Board Assy, Operator Control, VL22 (see Figure 4-1 for NHA)	REF	
-1	95361-040	. Connector, 40 Pin, J1, J7	2	
-2	90314-001	. Gate, NAND, Hex, 1-Input, DTL, A20-23, A28-30	7	
-3	98175-122	. Capacitor, Ceramic, 220PF, C12	1	
-4	92129-001	. Gate, NAND, Triple, 3-Input, TTL, A16	1	
-5	90338-001	. Transistor, General Purpose, NPN, Q2	1	
-6	90334-001	. Transistor, Unijunction, Q1	1	
-7	90356-206	. Capacitor, Tantalum, 10 MF, 10%, 20v, C15	1	
-8	90342-001	. Diode, General Purpose, CR1, 2	2	
-9	19149-001	. Gate, And, Quad, 2-Input, TTL, A32	1	
-10	95544-001	. Multiplexer, Quad, 2-Input, TTL, A31, 33	2	
-11	92128-001	. Gate, NAND, Quad, 2-Input, TTL, A12, 13, 17, 18, 26, 27	6	
-12	95379-347	. Capacitor, Ceramic, .047 MF, 50V, C1-8	8	
-13	95019-001	. Multiplexer, Dual, TTL, A1, 5, 6, 9, 15	5	
-14	92127-001	. Gate, NAND, Hex, 1-Input, TTL, A2, 4, 7, 11, 19, 24	6	
-15	96408-001	. Lamp, Solid State, DS0 – DS9	10	
-16	95549-001	. Counter, Binary, Preset, TTL, A3, 8, 10	3	
-17	92136-001	. Flip-Flop, Dual D, TTL, A14, 25	2	
-18	92164-001	. Switch, Rotary, 12-Position, S22, 23	2	
-19	91436-017	. Crystal, Series, 9.6 MHz, Y1	1	
-20	98175-010	. Capacitor, Ceramic, 10PF, 10%, 200v, C9, 10, 13, 14	4	

FIGURE ITEM NO.	PART NUMBER	DESCRIPTION	QTY PER ASSY	USAGE CODE
2-21	98175-310	. Capacitor, Ceramic, .01 MF, 10%, 100v, C11	1	
	90364-102	. Resistor, 1K, 5%, 1/4w, R1-7, 18, 27, 28, 31, 33-38, 40-42, N/I	20	
	90364-101	. Resistor, 100 ohms, 5%, 1/4w, R26, 29, N/I	2	
	90364-181	. Resistor, 180 ohms, 5%, 1/4w, R8-17, N/I	10	
	90364-200	. Resistor, 20 ohms, 5%, 1/4w, R30, N/I	1	
	90364-471	. Resistor, 470 ohms, 5%, 1/4w, R24, N/I	1	
	90364-562	. Resistor, 5.6K, 5%, 1/4w, R39, N/I	1	
	90364-510	. Resistor, 51 ohms, 5%, 1/4w, R32, N/I	1	
	90364-623	. Resistor, 62K, 5%, 1/4w, R23, N/I	1	
	90364-821	. Resistor, 820 ohm, 5%, 1/4w, R19-22, N/I	4	
	90369-503	. Resistor, 50K, Panel Mtg, R25, N/I	1	
	13472-001	. Bracket, Resistor, N/I	1	
-22	99445-002	. Switch, Toggle, SPDT, S11-13, 15, 17-21	9	
-23	91436-004	. Crystal, Series Resistor, 6.4 MHz, Y2	1	
	18542-001	. Socket, Crystal, Vert Mtg, XY1, XY2, N/I	2	
-24	99445-001	. Switch, Toggle, SPDT, S1-10, 14, 16	12	
-25	99482-004	. Plug, IC, 14-Pin, Cable, J2-6	5	
-26	17071-001	. Board, Operator Control	1	

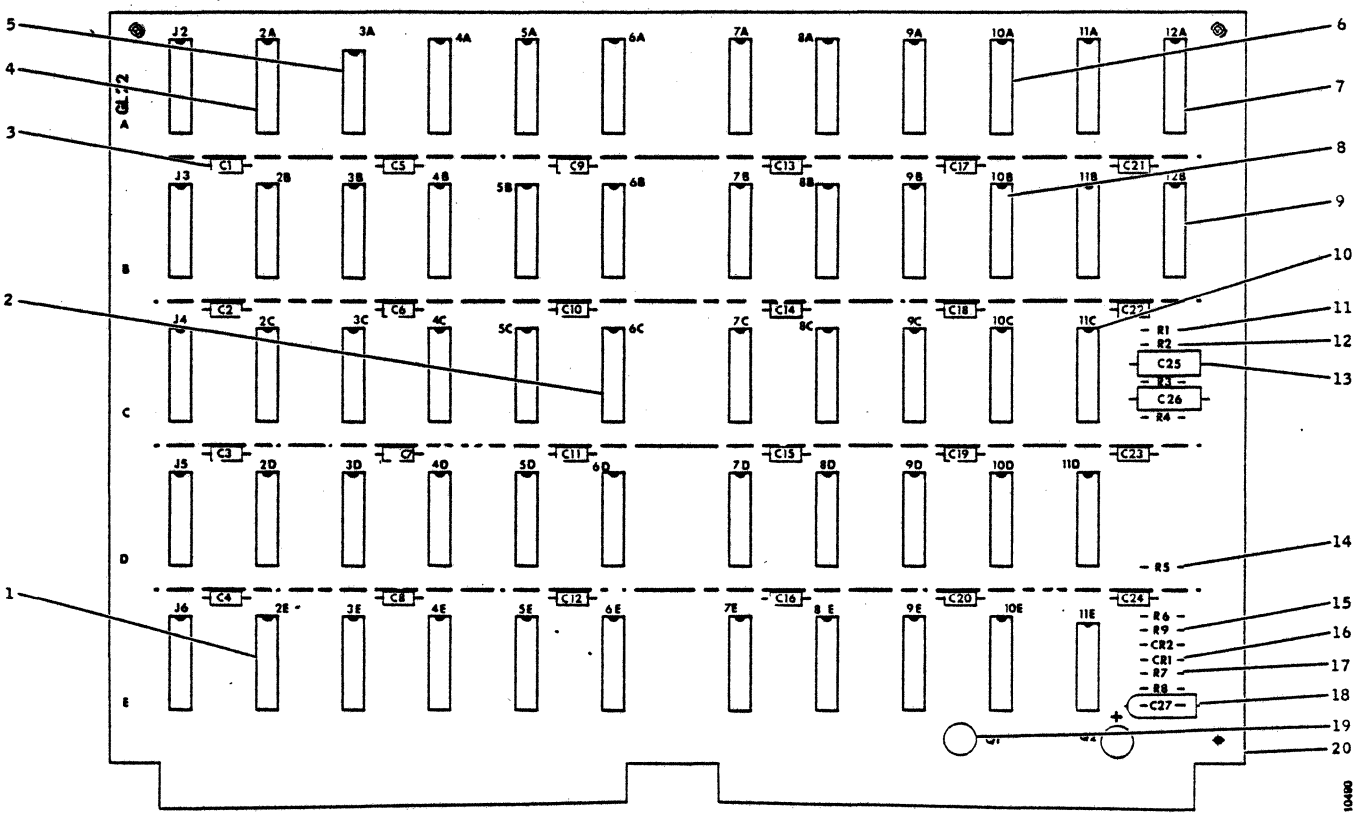

Figure 4-3. Logic Control Board Assembly, GL22

FIGURE ITEM NO.	PART NUMBER	DESCRIPTION	QTY PER ASSY	USAGE CODE
3-	15527-001	Board Assy, Logic Control, GL22 (see Figure 4-1 for NHA)	REF	
-1	95544-001	. Multivibrator, Quad, 2-Input, TTL, 2E, 4E, 6E	3	
-2	92136-001	. Flip-Flop, Dual D, TTL, 6C, 7C, 7D	3	
-3	95379-347	. Capacitor, Ceramic, .047 MF, C1-24	24	
-4	92129-001	. Gate, NAND, Quad, 3-Input, TTL, 2A, 3B, 2C, 8C, 3D, 11D, 8E	7	
-5	92128-001	. Gate, NAND, Quad, 2-Input, TTL, 3A-9A, 11A, 2B, 4B-8B, 10B, 2D, 4C, 5C, 9C, 10C, 4D, 5D, 8D, 10D	24	
-6	92127-001	. Gate, NAND, Hex, 1-Input, TTL, 10A, 11B, 3C, 6D, 9D, 10E	6	
-7	95549-001	. Counter, Binary, TTL, 12A, 3E, 5E, 7E	4	
-8	92130-001	. Gate, NAND, Dual, 4-Input, TTL, 9B, 9E, 11E	3	
-9	92135-001	. Decoder, 4-10 Line, TTL, 12B	1	
-10	94526-001	. Multivibrator, Dual, TTL, 11C	1	
-11	90364-102	. Resistor, 1K, 5%, 1/4w, R1, 4	2	
-12	90364-273	. Resistor, 27K, 5%, 1/4w, R2, 3	2	
-13	90354-101	. Capacitor, Mica, 100PF, C25, 26	2	
-14	90364-512	. Resistor, 5.1K, 5%, 1/4w, R5, 6	2	
-15	90364-684	. Resistor, 680K, 5%, 1/4w, R9	1	
-16	90342-001	. Diode, General Purpose, CR1, 2	2	
-17	90364-683	. Resistor, 68K, 5%, 1/4w, R7, 8	2	
-18	90356-104	. Capacitor, Tantalum, 33 MF, C27	1	
-19	90338-001	. Transistor, General Purpose, Q1, 2	2	
-20	15528-001	. Board, Logic Control	1	

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