



**Hardware Reference Manual
128K-2M Dynamic RAM Board
EDC Version**

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1. General Information

The Central Data 128K-2M EDC Dynamic Ram Board allows the user to add 128K, 256K, 384K, or 512K of RAM (512K, 1M, 1.5M, or 2M for 256K RAMs) to any Multibus¹ system. Error detection and correction (EDC) is a standard feature which will correct any single bit error and detect all double bit errors. Correction of single bit errors is normally accomplished without processor intervention while double bit errors cause an interrupt to be generated. For testing purposes, the board may be strapped to interrupt on any error. When an error is detected, two input ports may be read to determine the type of error (single or double bit) and to identify the RAM chip that failed. Reading the second input port clears the error condition and removes the interrupt output.

Completely Multibus compatible, the board runs at a maximum read data access time of 215ns, and a maximum XACK return time of 275ns. The data out lines can take the form of 8- or 16-bits, depending on the BHEN line of the Multibus. This feature allows the board to work without changes in any 8- or 16-bit system.

The board decodes the full 24-bit address bus, allowing a system-wide memory address capacity of 16 megabytes. The board is divided into two sections, each of which can be addressed on a 256K memory boundary (1M boundary for 256K RAMs). Additionally, each row of memory devices may be disabled by removing one of four row enable jumpers.

The on-board refresh arbitration circuitry is designed to minimize wait states caused by refresh cycles, which are normally initiated every 15 microseconds. If the processor accesses another board in the system at any time between refresh cycles, a new refresh cycle is initiated to overlap that memory cycle (giving hidden refresh). Also, refresh cycles are hidden between access cycles to the board.

Noise immunity of the board is greatly enhanced by the use of sockets with built in bypass capacitors. The printed circuit board is constructed in 5 layers with two of the internal layers being power and ground to further minimize noise.

¹Multibus is a trademark of Intel Corporation.

As with all EDC RAM boards, the memory must be initialized when power is first applied if the ERROR LED and interrupt output are to be meaningful. The error correction circuitry will function properly either way, however byte-write operations will cause reads to uninitialized bytes of data producing erroneous error indications.

2. Functional Description

The 128K-512K EDC Dynamic RAM Board is divided into several major sections. A brief description of each section is provided in this chapter, with more detailed information given in the Principles of Operation chapter.

The I/O addressing circuit consists of a 7-position dip-switch for address lines A1-A7, an 8-position dip-switch for lines A8-A15, and an option block to select between 8- or 16-bit I/O addressing. The address block is labeled 8-BIT I/O and EXT I/O, and selects 8- or 16-bit I/O addressing, respectively. The two ports provide error status information, and reading the second port clears the error condition and removes the interrupt output.

The memory addressing circuit divides the board into two sections. Each section consists of two rows of RAM chips, with each row containing 22 devices. The first 16 devices contain data bits D15-D0. The last 6 devices contain syndrome/check bits used by the EDC circuitry.

The board is designed to accommodate both 8- and 16-bit transfers, depending on the states of the BHEN and A0 lines. When BHEN is active, 16-bit (word) mode is selected, and address line A0 is ignored. When BHEN is inactive, the 8-bit (byte) mode is selected and address line A0 determines if the operation is to affect the even byte (bits D0-D7) or the odd bytes (bits D8-D15).

The error detection and correction (EDC) circuitry generates check bits (SC0-SC5) and stores them in memory during write cycles. During read cycles, new check bits are generated from the stored read data and compared to the check bits stored in memory to determine if an error has occurred. If an error is detected, the resulting syndrome bits are stored in the first I/O port along with the ERROR and MULT ERR flags. Single bit errors are normally corrected without processor intervention while multiple bit errors cause an interrupt to be generated and an error LED to be lit. For testing purposes, the correction circuitry may be disabled, an error may be forced, and the board may be strapped to interrupt on any error (even single bit).

The EDC circuitry generates one set of check bits for each 16-bit word of data and therefore must always operate in the 16-bit mode. When a byte read is to be performed, all 16 data bits are enabled, and the byte swapping circuitry determines which byte of data is to be output to the D0-D7 lines.

During byte-writes, only 8-bits of the 16-bit word are updated. Since the EDC circuitry must generate new check bits to reflect both bytes of data, a read operation must first be performed to detect/correct the existing 16-bit data field and latch the byte of data not affected by the byte-write operation. After this is accomplished, a 16-bit write is performed using the old and new bytes of data for the check bit generation. The read cycle during byte-write operations is transparent to the user except that the XACK time is stretched to 665ns (max).

The timing section of the board controls the generation of all timing signals needed by the dynamic RAM chips. It also makes sure that the refresh cycle is performed when needed and places these cycles after access cycles are completed so that a minimum of interference is generated. In most systems, refresh cycles will never hold up an access, and the board will operate at its maximum speed.

3. Principles of Operation

This chapter details the operation of the entire memory board. Any signal names in this text followed by a slash (/) indicates that the signal is active-low.

As in all Central Data schematics, a grid system is provided to help locate sources and destinations of signals. The source of any named signal will have references to all locations in the schematics where the signal is used. Each location where a signal is used, a reference is given to where it was generated.

If the location is on the same sheet as it is being referenced, it will show only a grid location (i.e. D2). If, however, the referenced signal appears on a separate page, it will have the grid location preceded by the sheet number (i.e. 2-B5).

Furthermore, if a group of signals is commonly routed together, that group may be cross-referenced together. It is not necessary that all members of the group go to each destination listed, since the purpose of the cross reference system is only to guide a user through the schematics.

Addressing and Buffering

This board allows two independent dip-switch addressable 256K memory sections. Also, the EDC I/O ports require address decoding on the lower 16 address lines.

Sheet 1 of the schematics contains the memory address comparators, the cycle/refresh arbiter, the memory/refresh timing and control circuitry, the XACK circuitry, and the interrupt circuitry.

Memory Address Comparators

The memory address comparator circuit consists of four configuration jumpers (labeled 64 or 256), two 6-bit comparators (IC140 and IC142), two 6-position dip-switches (IC128 and IC160), a 3-8 line decoder (IC114), four row enable jumpers (EN1-EN4), and two 4-input NAND gates (IC125).

The three configuration jumpers labeled 64 should be shorted for boards using 64K devices, while the jumper labeled 256 should be shorted for boards using 256K devices. The sets of jumpers should never both be inserted in the board at once.

Each comparator performs a bit-for-bit comparison between its 6-position dip-switch and bus address lines A18/-A23/, indicating a matched condition by setting its Q=P/ output (pin 19) low. Address lines A18/-A23/ are active low, therefore the dip-switches must be closed to indicate the active state and open to indicate the inactive state. Comparator IC140 serves to select or deselect the top two rows of RAM chips while IC142 controls the bottom two rows of RAM chips. Note that boards with 256K RAMs use only four of the comparator's inputs. The switches for the unused two inputs should be left open.

Pin 6 of IC125 is normally high, enabling the 3-8 line decoder (IC114) which selects one of the four possible rows of RAM chips with an active low output based on the two comparator outputs and A17 (A19 for 256K devices).

The MSEL signal (pin 8 of IC125) determines if the board is to be selected. Therefore, in order for a row of RAM chips to be enabled, the correct address must be applied and the row enable jumper (EN1-EN4) must be installed.

Cycle/Refresh Arbiter

The Cycle/Refresh Arbiter initiates both memory and refresh cycles, and in the case of a conflict determines which will be performed first.

When either MRDC/ or MWRC/ are asserted, the COMD line switches from low to high, indicating that a system memory cycle is in progress. This low to high transition latches the state of the MSEL line into pin 6 of IC133 to determine if the memory cycle is to affect this board (if pin 6 is low).

When a refresh cycle is required, the state of the COMD line is latched into pin 9 of IC133 by the low to high transition of the START REFRESH signal which selects either pin 6 or pin 8 of IC118 to start the refresh cycle.

If COMD was low, (indicating no memory cycle is in progress), pin 8 of IC133 will be high, and the refresh cycle will be initiated by the low to high transition of the delayed START REFRESH signal.

If COMD was high (indicating a system memory cycle is in progress), pin 9 of IC133 will be high. If pin 6 of IC133 is low (indicating a memory cycle to this board), the refresh cycle will be held off until the memory cycle is complete and pin 6 of IC133 has been reset.

The two delay lines at IC123 prevent glitches on the START/ line (pin 8 of IC138) when simultaneous memory and refresh requests occur.

When START REFRESH and COMD both switch high at approximately the same time, the data set up and/or hold times at pin 12 of IC133 will be violated, and IC133 may enter an unstable condition. The START REFRESH signal is delayed by the 12ns delay and is used to hold off the refresh starting gates providing a minimum of 10ns settling time for the flip-flop.

When simultaneous memory and refresh requests occur, it is uncertain which requests will be processed first. Therefore, the start of the memory cycle must be delayed until the arbiter has made its choice. The COMD line is delayed by the 19ns delay to produce the CYCLE signal, which is used to start memory cycles. The minimum delay from COMD to CYCLE is 20ns, while the maximum delay from the rising edge of START REFRESH to the falling edge of pin 6 of IC118 is 19.3ns. Since when either pin 6 or 8 of IC118 are low memory cycles will be inhibited, these delays will prevent false triggering of the START/ line.

Memory Cycle Timing and Control Circuitry

Memory cycles are initiated by the falling edge of START/, and the memory cycle timing is controlled by the delay line at IC134, and its associated circuitry.

At the start of a memory cycle, the 24 address lines are applied to the board. The buffered row address lines (BA1-BA8 and BA17 for 256K devices) are applied to the DRAM address inputs, while address lines A17/-A23/ are decoded by the memory address comparator circuit to produce the MSEL and row enable outputs. The row enable outputs pass through a 74F158 quad 2-input multiplexer (IC139) to the four pairs of NAND gates (IC112, IC113, IC126 and IC127) used to drive the RAS/ inputs of the DRAMS. Each output of IC139 controls one row of RAM chips, and each of the four-input NAND gates drives 11 devices (half a row). Before the start of a cycle, the COMD, DLY COMD, CYCLE, and RESTART/ lines will all be low, preventing the start of a memory cycle and providing the following preset conditions:

1. BDSEL is low indicating board is deselected.
2. HOLD is low allowing memory cycles to be initiated.
3. MEMERR is low to indicate the no-error condition.
4. BW RD is high selecting read mode (WR is low).

Next, the MRDC/ or MWRC/ signals are applied at least 50ns after the address lines are valid, causing COMD to switch high. DLY COMD switches from low to high 19ns later, latching the state of the BYTE WRITE line into pin 9 of IC148 (BW RD).

The WR signal determines whether a read or write operation will take place and pin 9 of IC148 serves to force a read operation when a byte write cycle is requested. When BW RD is high WR will be low, selecting the read mode. When BW RD is low, the state of the WR line will be controlled by the buffered MRDC line.

Shortly after DLY COMD switches high, CYCLE will switch high and assuming that a refresh cycle is not in progress, the two RAS drivers selected by IC139 will be enabled, and START/ will switch from high to low initiating the memory cycle. START/ is inverted and used to set pin 5 of IC120 (BDSEL).

IC134 is a five tap active delay line, which generates the required memory timing signals. Each output provides a fixed amount of delay from the input. The high to low transition of the fourth tap (LATCH DATA/) sets IC105 (HOLD), which causes the input of the delay line (START/) to switch high again, producing a negative pulse of 164-192ns at the input to the delay line. Each tap of the delay line is simply a shifted version of this pulse. The active delays for DL3 are as follows:

<u>Signal Name</u>	<u>Output Tap No.</u>	<u>Delay (ns)</u>
R/C	T1	30 <u>+2.1</u>
CASEN/	T2	54.5 <u>+2.5</u>
EXT CYCLE/	T3	145 <u>+7</u>
LATCH DATA/	T4	168 <u>+8</u>
NORM XACK/	T5	200 <u>+9</u>

The falling edge of R/C causes the column addresses (BA8-BA16 and BA18 for 256K devices) to be applied to the RAMs.

When CASEN/ switches low, CAS (pin 10 of IC116) switches high, enabling the column address strobe to the DRAMS.

The falling edge of EXT CYC/ is used to generate the XACK signal during word write cycles, and start the write portion (second half) of byte-write cycles.

The high to low transition of LATCH DATA/ sets HOLD causing pin 6 of the row decoder (IC114) to switch low, and START to switch

high. This removes the RAS/ inputs to the RAMs and the START/ input to the delay line. On read cycles, or the read portion of a byte-write cycle, this signal is used to latch the RAM output data into the 2960 EDC chip and the 74S373 output latches.

The falling edge of NORM XACK/ latches the state of WR/ into pin 5 of IC105, which on read cycles will be high. That output then latches the state of the 2960 EDC ERROR/ output into pin 5 of IC130. The falling edge of NORM XACK/ is also used to generate the XACK/ signal during read cycles if no errors are detected.

The rising edge of R/C causes CAS to switch low, removing the CAS/ inputs to the DRAMs.

With WR low (a read operation), the rising edge of CASEN/ will cause pin 6 of IC145 to switch high, latching the error status into the interrupt flip-flop (IC146) and causing LATCH STATUS (pin 8 of IC145) to switch high. This signal latches the status information from the 2960 EDC chip into IC137 (I/O port 0).

With the DBL/ANY option block set to DBL, INT (pin 9 of IC146) will only be set on multiple bit errors. With the ANY position selected, INT will be set on the occurrence of either a single or multiple bit error. If neither position is strapped an interrupt will never be generated and the error LED will never be lit. Once INT is set, pin 8 of IC146 will be low, holding IC146 in the set condition. With INT high, pin 10 of IC144 will light the error LED, pin 4 of IC144 will generate an interrupt (if strapped) and further LATCH STATUS pulses will be inhibited (to save the error status). INT may be reset by pressing the reset interrupt switch, by reading I/O port 1, or by applying the INIT/ signal to the board.

The rising edge of pin 6 of IC145 also clocks the state of the BYTE WRITE line into pin 9 of IC130. If the cycle in progress is a byte-write operation, (BYTE WRITE is high), pin 9 of IC130 will switch high. The rising edge of EXT CYC/ will cause RESET/ (pin 8 of IC117) to switch low, and the rising edge of NORM XACK/ will cause RESTART/ (pin 6 of IC106) to switch low. RESET/ clears pin 9 of IC148, selecting the write mode (WR=1), and causes pin 6 of the row decoder to switch high, which in turn causes the RAS/ outputs to be asserted. RESTART/ clears HOLD, initiating the second (WRITE) cycle associated with the byte-write operation by allowing START/ to switch low. As mentioned earlier, pin 6 of IC145 is normally high and will only follow the CASEN/ input when WR=0. Therefore, the RESET/ and RESTART/ outputs will only be generated at the end of the read operation during a byte-write cycle.

XACK Circuitry

The XACK/ circuit generates the acknowledge signal for port reads and memory cycles for the board.

For I/O port read cycles, the RD PORT/ signal is inverted and applied to an open collector inverter, pulling the XACK/ line low.

For memory cycles, the XACK/ circuit must generate four different acknowledge times depending on whether the cycle is a word write, a read without error, a read with error, or a byte-write.

When a system memory cycle is not in progress, COMD is low, holding the two XACK/ flip-flops (IC96 and IC146) in the reset state. When a memory cycle is started, COMD will be high, removing the reset input to pin 1 of IC146. With COMD high, pin 8 of IC106 will switch from low to high if either WR or BYTE WRITE/ are high, removing the reset from pin 14 of IC96.

The EN signal (which will be high if BDSEL is true and INH1/ is false), indicates that a memory cycle to this board is in progress. The EN signal is inverted by IC131 and enables the memory cycle XACK/ driver (with pin 19 of IC153).

At the start of a word write cycle, COMD, WR, BYTE WRITE/, EXT CYC/, and NORM XACK/ are all high. Pin 3 of IC117 will be low, so that when EXT CYC/ switches from high to low, pin 11 of IC145 will switch low setting the following flip-flop. Pin 6 of that flip-flop sets the XACK flip-flop, whose output is inverted by IC153 to produce the XACK/ signal. Pin 7 of IC96 is inverted and NOR'ed with INIT to reset the command request flip-flop (IC133). When NORM XACK/ switches low, pin 3 IC117 switches high causing the output of the following gate to switch high, removing the set input from the 74F74. When the host removes the MRDC/ or MWRC/ signal, the COMD line switches from high to low, resetting the circuitry to the starting state.

On memory read cycles, the high to low transition of NORM XACK/ latches the state of the ERROR/ line to pin 9 of IC96. If ERROR/ is high (no error) the flip-flop will be set, generating the XACK/ signal.

When an error is detected, the MEMERR signal enables the error correction logic and 2960 EDC data output drivers, and the output data latches are selected to follow the 2960 EDC outputs. When MEMERR/ switches low, EXT CYC/ will already be low and pin 3 of IC145 will switch low. The low to high transition of EXT CYC/

will cause pin 3 of IC145 to switch high, latching the state of the BYTE WRITE/ line into IC146. If the board is not in a byte-write operation, pin 6 of IC146 will be cleared, eventually generating the XACK/ output.

Byte-write operations consist of a memory read cycle followed by a memory write cycle. The XACK circuit must be held off during the read portion and allowed to generate the XACK/ signal during the write portion. During the read portion both WR and BYTE WRITE will be low, and pin 3 of IC117 will be forced high, preventing IC146 from being set. Further, pin 8 of IC106 will be low, holding IC96 reset. During the write portion of the cycle, WR will be high removing the reset input from IC96 and allowing the falling edge of EXT CYC/ to set IC146 as in word write cycles.

Refresh Timing and Control Circuitry

Sheet 2 of the schematics contains the refresh timer (IC103), which generates the REF REQ and FORCED RFSH/ signals used to initiate refresh cycles.

IC103 is a dual 4-bit binary counter, configured as an 8-bit binary counter. The counter is incremented by each high to low transition of the CCLK input. After 64 transitions of the CCLK input, the Q6 output of IC103 will switch from low to high, and REF REQ (pin 5 of IC104) will switch high allowing hidden refresh cycles to be initiated. After 128 CCLK inputs, Q7 will switch from low to high and FORCED RFSH/ will switch low, initiating a forced refresh cycle. When a refresh cycle is performed, IC103 will be reset by the low to high transition of the REFRESH signal and IC104 will be reset when RFSH/NORM/ switches low.

Sheet 1 of the schematics contains the refresh timing circuitry and the circuit used to initiate hidden refresh cycles. When COMD switches from low to high, the state of the REF REQ line is latched into pin 5 of IC119 and the clock input of the second flip-flop pin 11 of IC119 switches low. REF REQ is totally asynchronous to COMD so pin 5 of IC119 may be unstable for a short period of time after the clock transition. Pin 11 of IC119 is clocked when COMD switches low, providing the required settling time for pin 5 of IC119. If REF REQ is high when COMD switched high, pin 5 of IC119 will be set and pin 8 of IC119 will be dropped when COMD switches low, generating the HIDDEN RFSH/ signal.

When either HIDDEN RFSH/ or FORCED RFSH/ switch low, START REFRESH (pin 11 of IC117) switches high and the cycle/refresh

arbiter takes over as previously described. After some delay the arbiter will cause either pin 6 or 8 of IC118 to switch low, preventing the start of a memory cycle and setting IC120 which produces the REFRESH signal. The falling edge of REFRESH/ starts the timing sequence for refresh cycles, which is controlled by delay line at IC107.

This delay line is a five tap active delay line which generates the required timing signals for refresh cycles. Each output provides a fixed amount of delay from the input. The high to low transition of the fifth tap resets IC120 causing the input to the delay line (REFRESH/) to switch high again, producing a negative pulse of 393-441ns at the input to the delay line. Each tap of the delay line is simply a shifted version of this pulse. The active delays for IC107 are as follows:

<u>Signal Name</u>	<u>Output Tap No.</u>	<u>Delay (ns)</u>
RFSH/NORM/	T1	45 <u>+2.5</u>
HOLD START/	T2	65 <u>+3</u>
-----	T3	105 <u>+5</u>
-----	T4	300 <u>+15</u>
-----	T5	410 <u>+20</u>

When IC120 is set, the rising edge of REFRESH causes CYCLE to switch high, and the falling edge of REFRESH/ starts the refresh timing sequence. The REFRESH line also controls the select input of three 74S157 quad 2-input Multiplexers (shown on sheet 3 of the schematics), which select between the row address lines (for memory cycles) and the refresh counter lines (for refresh cycles).

When RFSH/NORM/ switches low, START/ will be further disabled, and IC104 (sheet 2) will be reset, clearing the REF REQ and FORCED RFSH/ signals. RFSH/NORM/ is also connected to the select line of IC139. When it is high, the outputs of IC139 follow the B inputs (the row select lines), and when it is low the outputs follow the A inputs controlled by RSTROBE/. The RSTROBE/ line will initially be high, causing the four outputs of IC139 to be low, disabling the RAS drivers.

When HOLD START/ switches low, the hidden refresh flip-flops are reset, and the start refresh flip-flop (IC133) is reset.

After taps 1 and 2 of DL2 have switched low, pins 6 and 8 of IC118 and CYCLE will all be high, allowing the RAS drivers to be

enabled entirely under the control of IC139. Taps 1 and 2 prevent memory cycles from being initiated by forcing START/ high.

When tap 3 of the delay line switches low, RSTROBE/ (pin 3 of IC121) will go low causing all four outputs of IC139 to switch high, enabling all eight RAS drivers. When the RAS/ outputs switch low, the refresh address will be strobed into all four rows of RAM chips.

When tap 4 switches low, RSTROBE/ will switch high, removing the RAS/ inputs from the RAM chips.

When tap 5 switches low, IC120 is reset and REFRESH switches low. This causes CYCLE to switch low and address multiplexer to again select the row address lines. REFRESH/ switching high removes the active-low input to the delay line. When RFSH/NORM/ switches high, the outputs of IC139 will follow the B inputs (row select inputs).

The refresh cycle is completed with the low to high transition of the HOLD START/ line. When HOLD START/ switches high, START/ will switch low if an impending memory cycle is to be performed.

In conclusion, the refresh address set up time and RAS precharge time for the refresh cycle is guaranteed by the delay from the falling edge of REFRESH/ to the falling edge of RSTROBE/. The RAS/ signal is initiated by tap 3 of the delay line and removed by tap 4, while the row address set up time and the RAS precharge time for the impending memory cycle is guaranteed by the delay from the rising edge of REFRESH/ to the rising edge of HOLD START/.

Multibus Interface Logic

Sheet 2 of the schematics contains the bus interface logic. Bus address lines A0/-A18/ in addition to the BHEN/, CCLK/, IORC/, and INIT/ lines are all buffered by 74S240 octal inverting buffers (IC152-IC155). The Schmitt trigger PNP inputs of the 74S240 provide excellent noise immunity, and low input current requirements.

The 16 internal data bus lines (BD0/-BD15/) interconnect the 2960 EDC chip, the RAM array, and the Multibus data buffers. Three 8-bit I/O paths are required to interface the internal data bus with the Multibus data lines. For word operations, two buffers are used, while for byte operations, a third 8-bit data path is

required between the internal data bus lines BD8/-BD15/, and the Multibus lines D0/-D7/.

Three 74LS244 Tri-State noninverting octal buffers are used to enable data transfers into the board (write cycles), while three 74S373 Tri-State octal latches, enable data transfers out of the board (read cycles). Each of the six devices used for data I/O are enabled independently with enable lines EN1/-EN6/.

IC156 will be enabled by EN1/ during word write cycles, while IC149 will be enabled by EN2/ during word read cycles. IC158 will be enabled by EN5/ during either a word write cycle, or a byte write cycle to an even address boundary (BA0=0). IC151 is enabled by EN6/ during either a word read cycle, or a byte read cycle to an even address boundary (BA0=0). IC157 and IC150 are used for the byte swap operation. IC157 is enabled by EN3/ during a byte write cycle to an odd address boundary (BA0=1), and IC150 is enabled by EN4/ during read cycles from an odd address boundary (BA0=1).

I/O Circuitry

An I/O address comparator circuit allows the user to set the base address for the two I/O ports on a two byte boundary in a 64K address field. Address line BA0 is used to select either port 0 or port 1, while address lines BA1-BA15 are used to set the base address for the I/O ports, with BA8-BA15 optionally disconnected for 8-bit I/O addressing.

IC115 compares address lines BA1-BA7 with a 7-position dip-switch (IC102) while IC129 compares address lines BA8-BA15, with an 8-position dip-switch (IC143). Address lines BA1-BA15 are active high signals, therefore each dip-switch must be left open to indicate an active address line and must be closed to indicate an inactive address line. The P=Q/ output (pin 19) of each comparator will be low if the address lines to the comparator match the state of the dip-switch lines. With the I/O option block set to 8-BIT I/O, pin 3 of IC116 will follow the output of IC115. With EXT I/O selected, the outputs of IC115 and IC129 must both be low for pin 3 of IC116 to switch high.

When IORC is high, and pin 3 of IC116 is high, RD PORT/ switches low, indicating that an I/O read to this board is in progress. With RD PORT/ low, BA0 selects either port 0 (BA0=0) or port 1 (BA0/=0). When an I/O read to port 1 is initiated, pin 10 of IC147 switches low causing RES INT to switch high, which will remove the error condition, and clear the interrupt output. A reset interrupt switch is also provided for this purpose.

I/O Port Definitions

Even Address (BA0=0):

<u>Bit</u>	<u>Definition</u>
0	Syndrome Bit 0/
1	Syndrome Bit 1/
2	Syndrome Bit 2/
3	Syndrome Bit 3/
4	Syndrome Bit 4/
5	Syndrome Bit 5/
6	Error=1
7	Multiple Error=1

Odd Address (BA0=1):

<u>Bit</u>	<u>Definition</u>
0	Row 1
1	Row 2
2	Row 3
3	Row 4
4-7	Not used

Syndrome Bit Definitions:

<u>Failed Device</u>	<u>SB5/</u>	<u>SB4/</u>	<u>SB3/</u>	<u>SB2/</u>	<u>SB1/</u>	<u>SB0/</u>	<u>HEX BYTE</u>
No Errors	1	1	1	1	1	1	3F
0	1	1	0	0	0	1	71
1	1	1	0	1	0	0	74
2	1	0	1	1	0	0	6C
3	1	0	1	0	1	0	6A
4	1	0	1	0	0	1	69
5	1	0	0	1	1	0	66
6	1	0	0	1	0	1	65
7	1	0	0	0	1	1	63
8	0	1	1	1	0	0	5C
9	0	1	1	0	1	0	5A
10	0	1	1	0	0	1	59
11	0	1	0	1	1	0	56
12	0	1	0	1	0	1	55
13	0	1	0	0	1	1	53
14	0	0	1	1	1	0	4E
15	0	0	1	0	1	1	4B
CB0	1	1	1	1	1	0	7E
CB1	1	1	1	1	0	1	7D
CB2	1	1	1	0	1	1	7B
CB3	1	1	0	1	1	1	77
CB4	1	0	1	1	1	1	6F
CB5	0	1	1	1	1	1	5F

Error Detection/Correction Circuitry

Error detection and correction is accomplished by an AMD 2960 EDC device. This device will correct single bit errors in either the 16-bit data field or the 6-bit check byte field, and will detect all double bit errors.

The 2960 EDC device contains the following:

1. 16-bit data input latch
2. Check bit latch
3. Check bit generation logic
4. Syndrome bit generation logic
5. Error detection logic
6. Error correction logic
7. Two 8-bit data output latches
8. Control logic

During write cycles, 16-bits of data are loaded by the 2960, from the bi-directional data lines under control of the latch enable

input (LE IN). At the start of a cycle HOLD will be low and LE IN will be high, causing the outputs of the data input latch to follow the data bus. The data input latch outputs feed the check bit generation logic. The GEN/ input (pin 42) will be low at the start of a memory write cycle causing six check bits to be generated from the 16-bit data bus inputs, based on a modified hamming code. The check bits generated will appear on the syndrome-check bit outputs (SC0-SC5) and will be written into the six RAMs used for check bit storage, while the 16 data bits will be written into the data RAMs.

At the start of a memory read cycle, both GEN/ and LE IN will be high putting the 2960 in the read mode. At the end of the read cycle HOLD will switch high causing LE IN to switch low, latching the data bits and the check bits into their respective latches. The syndrome generation logic compares the check bits read in from memory against a newly generated set of check bits produced from the data input latch outputs (memory data). If both sets of check bits match, then there are no errors. If there is a mismatch, then one or more of the data or check bits is in error.

The syndrome bits are produced by an exclusive-or of the two sets of check bits. If the two sets of check bits are identical (meaning there are no errors) the syndrome bits will be all 0's. If there are errors, the syndrome bits can be decoded to determine the number of errors and the bit in error position. The ERROR/ output will be low if any error is detected, while the MULT ERR/ line will be low during multiple bit errors only. The six syndrome bits along with the ERROR/ and MULT ERR/ signals are latched into IC137 (port 0) at the end of each read operation.

As described earlier, when an error is detected on a read cycle, the XACK/ signal will be held off, MEM ERR will be high, and MEM ERR/ will be low. When MEM ERR switches high, pin 3 of IC106 will switch high enabling the correction logic in the 2960. Error correction may be disabled by installing the CORR DIS jumper at pin 1 of IC106.

The OE0/ and OE1/ inputs to the 2960 serve to enable the low order and high order data output latches respectively. During word read cycles, the BYTE WRITE input to pins 2 and 13 of IC141 will be low causing the outputs to be high. If an error is detected and MEM ERR/ switches low, pin 6 of IC147 will switch high causing both OE0/ and OE1/ to switch low, enabling both tri-state data output latches.

During byte-write cycles, a 16-bit data read must be performed first to detect/correct errors in the 16-bit data field. The

corrected data is latched by the data output latches in the 2960. Once this has been accomplished, the Multibus data input buffer associated with the even or odd byte to be written is enabled, with the other byte being provided by the 2960 data output latch, and a 16-bit word write to memory is initiated (the write portion of the byte write cycle). During byte write cycles the BYTE WRITE input to pins 2 and 13 of IC141 will be high and, depending upon the state of the BA0 and BA0/ lines, either pin 3 or pin 11 of IC141 will be high. At the end of the read portion of the byte-write cycle pin 6 of IC148 will switch low causing pin 6 of IC147 to switch high enabling either OE0/ or OE1/.

Dynamic RAM Array

Sheet 3 of the schematics contains the Dynamic RAM array.

The 88 Dynamic RAM chips are divided into four rows of 22 devices each. The first 16 dynamic RAMs (from left to right) of all four rows are used to store data bits DB15/-DB0/, while the last six dynamic RAMs (from left to right) are used to store check bits CB5-CB0.

Each of the 22 columns of RAM chips contains four devices, and the data I/O pins for each column are bussed together. For the RAMs used to store bus data, the data input and output pins are tied together. For the check bit memory, the data input and output lines are bussed separately. The TST ERR jumper is provided to allow errors to be forced, for testing purposes. When the TST ERR jumper is removed, data I/O line BD5 is disconnected from the dynamic RAMs.

Six 74S240 Octal inverting buffers are used to drive the dynamic RAM address inputs, CAS/ inputs and WE/ inputs. IC97, IC98, IC99 and IC101 provide the address inputs A0-A7, IC110 provides the WE/ inputs and address line A8, and IC100 provides the CAS/ inputs. Each address and WE/ output device drives 22 inputs, while the CAS/ output drivers each drive 11 inputs. The RAS/ drivers are shown on sheet 1 of the schematics, and each RAS/ output drives 11 devices. All address, WE/, CAS/, and RAS/ inputs to the RAM array are driven through a 15-ohm sip resistor.

The refresh address counter consists of a 74LS393 dual 4-bit counter (IC92) and a 74S112 J/K flip-flop (IC96). These two devices provide a 9-bit binary counter whose address is incremented each time REFRESH switches from high to low (at the end of each refresh cycle). Three 74S157 quad 2-input multiplexers select between either the refresh address counter outputs, or the row address inputs (BA1-BA8 and BA17), depending on the state of

the REFRESH line. When REFRESH is high the outputs of IC89-IC91 will contain the 9-bit refresh address. When low, the outputs will contain the row addresses. Three 74F158 quad 2-input inverting multiplexers (IC93-IC95) drive the address buffers and select between the column address lines (BA9-BA16 and BA18) and the outputs of IC89-IC91, depending on the state of the R/C line. When the R/C line is high, the outputs of the multiplexer are selected; when R/C is low, the column address lines (BA9-BA16 and BA18) are selected.

88 high reliability IC sockets with built in bypass capacitors are provided to both increase reliability and reduce system noise.

4. Installation/User Selectable Options

The 128K-512K Dynamic RAM board is designed to operate in any standard Multibus system. The board can occupy any card position of the system, since it does not operate as a bus master.

Configuration Jumpers

There are four configuration jumpers used to configure the board to accept 64K or 256K Dynamic RAM chips. The 3 configuration jumpers labeled 64 should be strapped for boards using 64K RAMs, while the jumper labeled 256 should be strapped for boards using 256K chips.

Row Enable Jumpers

Each row of RAM chips has a row enabled jumper which should be strapped if that row of devices is to be enabled. The four row enable jumpers are labeled EN1-EN4.

Memory Address

Each half (top and bottom) of the board is addressed independently by dip-switches. The half can be set up to start on any 256K boundary (1M boundary for 256K RAMs) in a 16-megabyte system address space.

The memory is addressed by setting switches for the top or bottom rows of memory. The top two rows are addressed with dip-switch IC128, while the bottom two rows of RAMs are addressed with dip-switch IC160. Also marked on the board are indications of the address line corresponding to each switch position, as well as the polarity of the switches. Address 23 is selected by the left most switch, while address 18 is selected by the right most. When a switch is up (on), the corresponding address line is compared for 1. When the switch is down (off), the line is compared for 0. If only one row of either half is being used, then you must make sure that the memory chips are in the proper sockets for selection, and the row enable jumpers are enabled or disabled according. If the lower 128K (or 512K) half is desired, then the chips should reside in the top row for the section. If the upper 128K (or 512K) half is desired, the chips should be moved to the bottom row of the section.

I/O Address

The board provides two error detection I/O ports. The base address for these I/O ports may be set on any two port boundary within a 64K address space. A 7-position dip-switch (IC102) is provided to select address lines 1-7, while an 8-position dip-switch (IC143) is provided to select address lines 8-15. An option block labeled EXT I/O or 8-BIT I/O is provided to select between 16-bit and 8-bit I/O addressing, respectively. One of these two positions must be strapped with a shorting plug.

Interrupt Selection

An option block labeled DBL/ANY can be strapped to cause an interrupt on multiple bit errors or on any errors, respectively. In normal operation, the position labeled DBL should be strapped to allow single bit errors to be corrected without host intervention. This mode interrupts the host only on the occurrence of a multiple bit error. The use of the ANY strap will cause any error (even corrected single-bit errors) to interrupt the processor.

The error detection interrupt can be gated to any of the vectored interrupt lines. The selection of which interrupt line is used is made with a shorting plug placed over the corresponding set of wire-wrap pins. These pins are marked 0-7 and are located near the P1 connector in the center of the board.

If the user does not desire errors to generate interrupts, he must leave the shorting plug off the interrupt pins.

Test Options

Under normal conditions, the TST ERR jumper must be strapped providing the data I/O line BD5 to the RAM array. For testing purposes, errors may be forced by removing the TST ERR jumper.

The correction circuitry may be disabled by installing the jumper labeled CORR DIS. This should be done for testing purposes only and under normal operating conditions the jumper should be removed.

5. Specifications

Word Size

8- or 16-bits determined by the Multibus BHEN Line.

Memory Size

131,072 Bytes (128K board)
262,144 Bytes (256K board)
393,216 Bytes (384K board)
524,288 Bytes (512K board)

Access Time (ns)

	<u>Typ</u>	<u>Max</u>
All Reads--Data Available	180	215
All Reads--XACK Valid	245	275
Word Writes--XACK Valid	205	235
Byte Writes--XACK Valid	600	665

Cycle Time (ns)

335ns Maximum (word writes)
375ns Maximum (all reads)
765ns Maximum (byte writes)

Address Selection

Dip-switch addressing for each half of the board to reside on any 256K (1M for 256K RAMs) memory boundary in the 16 megabyte address space. Four row enable jumpers for row deselection are also provided.

15-bit dip-switch address selection for the two I/O ports is used, with A8-A15 optionally disconnected.

Interface

All signals meet the IEEE Multibus proposed specification. IEEE 796 bus compliance: Slave D16 M24 I16

Electrical Characteristics

Vcc: +5V $\pm 5\%$
Icc: 4.4A typ, 6.4A max

Dynamic RAM Parameters

TRAC=150ns Maximum
TCAC=80ns Maximum
TRCD (min)=35ns Maximum
TRAH (min)=20ns Maximum

Qualified 64K DRAMs

INMOS: 2600-S12
Motorola: MCM6665AL15
Mitsubishi: M5K4164NS-15

Environmental Characteristics

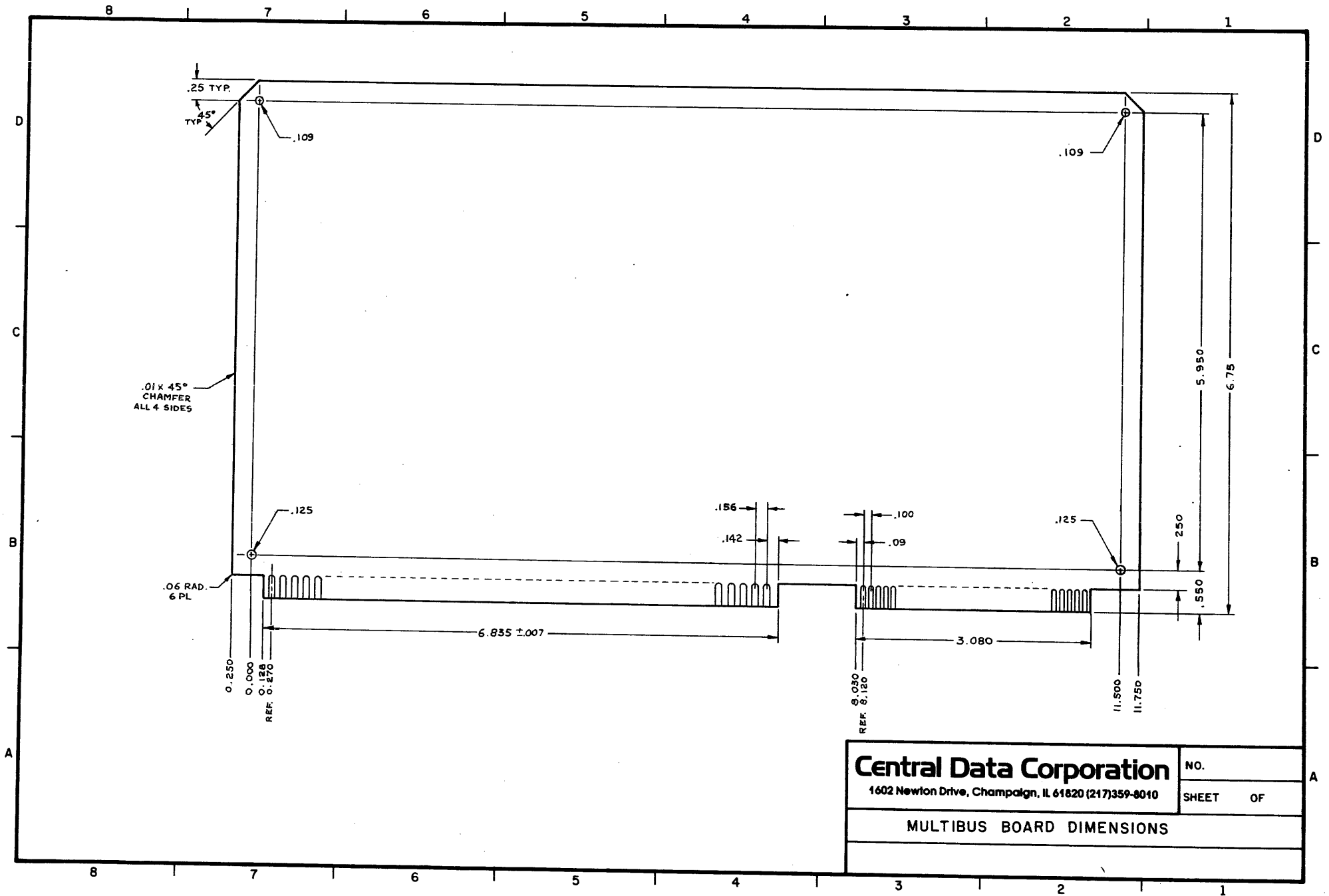
Operating Temperature: 0°C to +55°C
Relative Humidity: 0 to 90% (non-condensing)

Physical Characteristics

Dimensions: see the drawing on the following page
Weight: 16oz (458gm)

Ordering Information

Part Number: B1027
Description: Multibus Dynamic RAM Board
Sizes: /128 128K size
 /256 256K size
 /384 384K size
 /512 512K size
 /012 512K size, using 256K RAMs
 /024 1024K size, using 256K RAMs
 /036 1536K size, using 256K RAMs
 /048 2048K size, using 256K RAMs



Central Data Corporation		NO.
1602 Newton Drive, Champaign, IL 61820 (217)359-8010		SHEET OF
MULTIBUS BOARD DIMENSIONS		

6. Schematics

The following pages contain the schematics for the 128K-2M Dynamic RAM board. A full description of the circuitry is given in the Principles of Operation section of this manual.

8

7

6

5

4

3

2

1

D

C

B

A

3-INPUT 'AND' GATE



2-INPUT 'OR' GATE



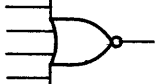
INVERTER



2-INPUT 'NAND' GATE



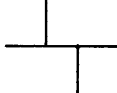
4-INPUT 'NOR' GATE



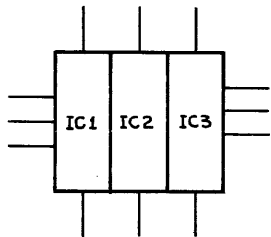
TWO LINES - NO CONNECTION



3 LINES - ALL CONNECTED



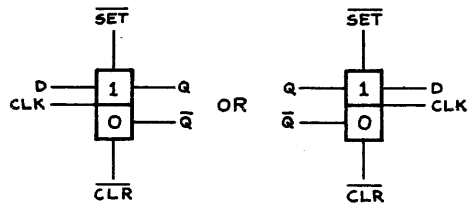
GROUP OF SIMILAR PARTS



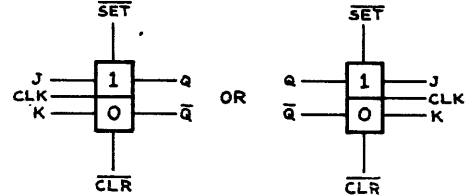
ALL LINES ENTERING ON THE SIDES ARE BUSSED TO ALL CHIPS

ALL LINES ENTERING ON THE TOP OR BOTTOM ARE SEPARATE FOR EACH CHIP

D-TYPE FLIP-FLOP



J/K FLIP-FLOP



UNMARKED ARROWS GO TO +5V

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NO.

SHEET OF

DRAWING CONVENTIONS

8

7

6

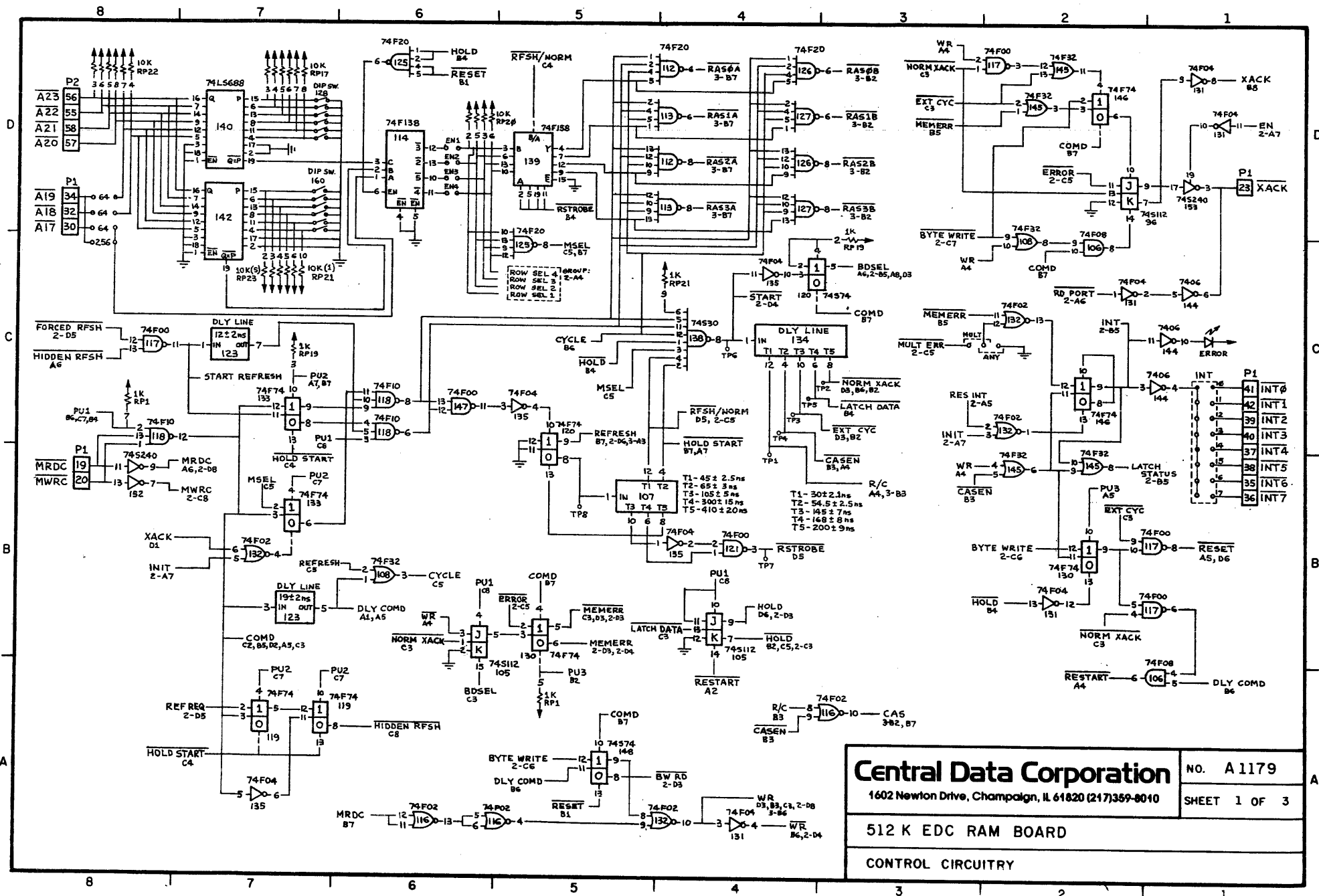
5

4

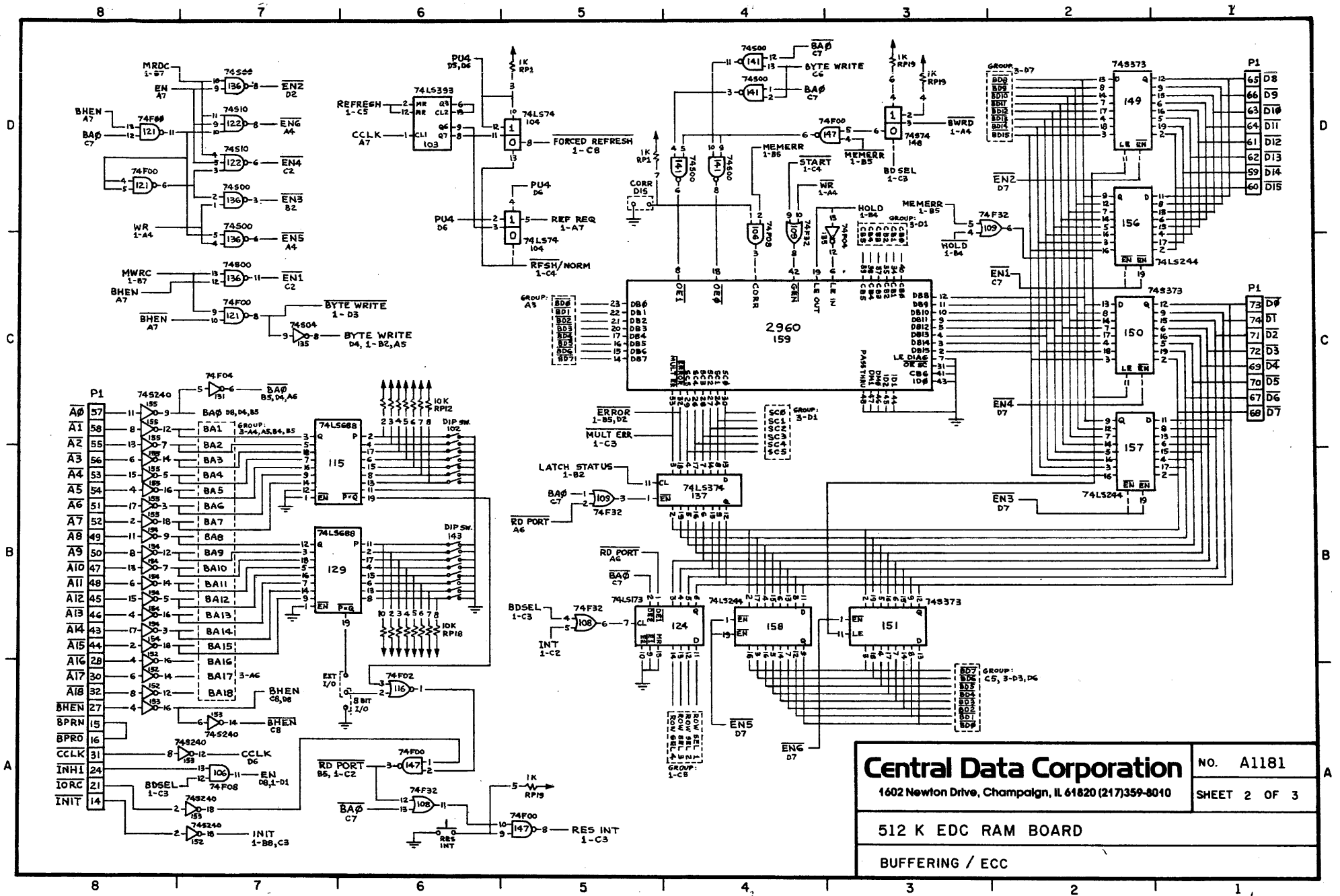
3

2

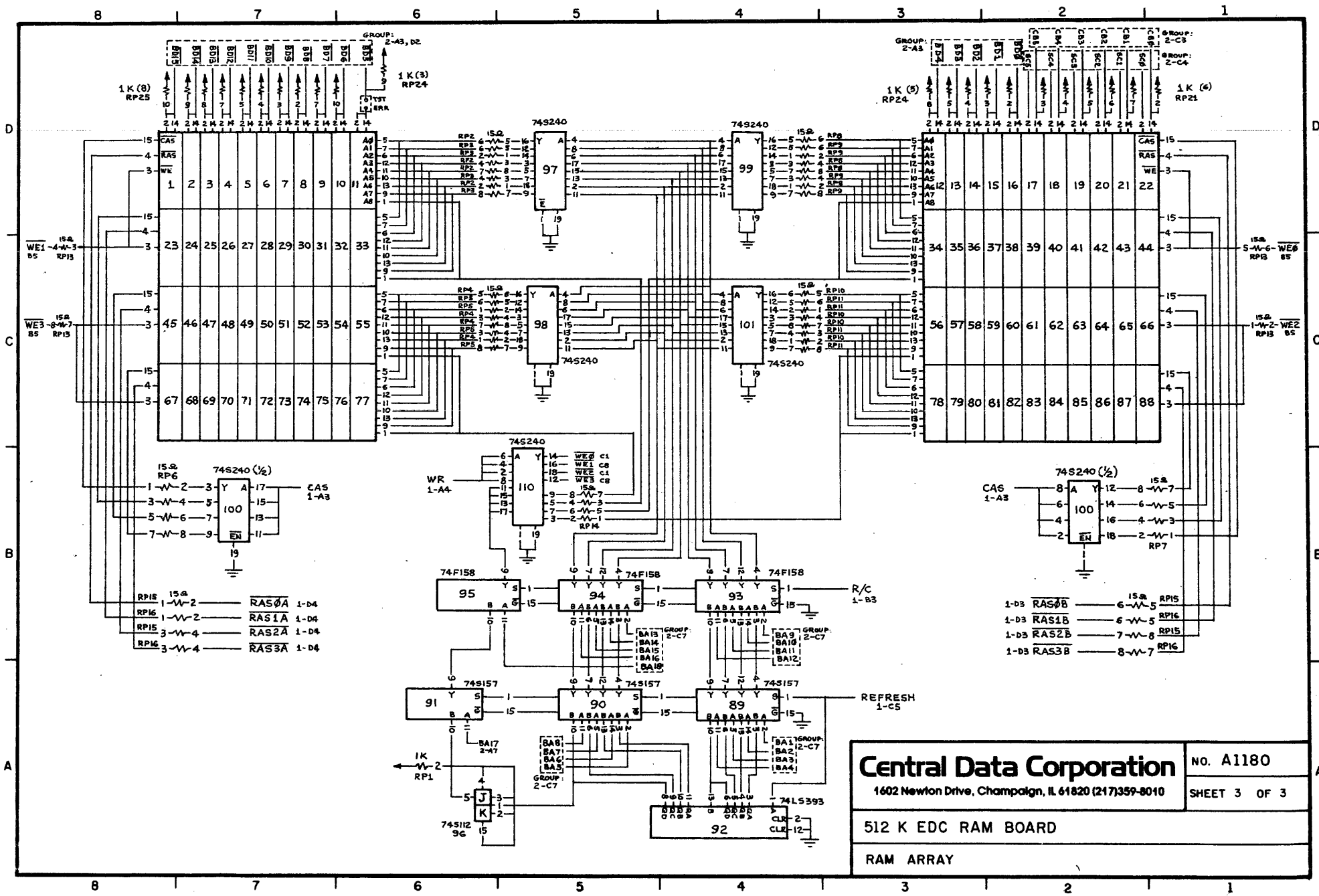
1



Central Data Corporation NO. A1179
 1602 Newton Drive, Champaign, IL 61820 (217)359-8010 SHEET 1 OF 3
 512 K EDC RAM BOARD
 CONTROL CIRCUITRY



Central Data Corporation 1602 Newton Drive, Champaign, IL 61820 (217)359-8010	NO. A1181
	SHEET 2 OF 3
512 K EDC RAM BOARD	
BUFFERING / ECC	



Central Data Corporation 1602 Newton Drive, Champaign, IL 61820 (217)359-8010	NO. A1180
	SHEET 3 OF 3
512 K EDC RAM BOARD	
RAM ARRAY	