Printed Circuit Manual

VOLUME 3

CONTROL DATA

CORPORATION

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

REVISION RECORD

REVISION	DESCRIPTION
A	Corrections.
B	1604 Inverter Ground Rules and Hammer Storage Card 91 pages added.
C	Long Line Driver and Receiver Cards CA98 and HA26 pages added.
D	Corrections to card type C64 and C65.
E	Add index tabs, chapter headings, new Table of Contents addition to Appendix, type "E" and 1604 cards; and Delay Card P13A.
F	Replace the following pages 3-HA18-1 and 2; 4-C62 and C-61-5 and 6; Appendix pages 5 through 10. Add pages 4-60, 60A, 62 and 67-1 through 3; 4-79A-1, 5-97-1 and 2, 5-E10-1. Replace page 4-E12-1.
G	6600 information and circuit module schematics added as volume 3.
H	Volume 1, addition of revised record of revisions volume 2, addition of record of revisions. Replace the following revised pages; chapter 4 contents page, 4-C62 and C61-1, 4-C62 and C61-2, 4-C62 and C61-3, 4-C62 and C61-5, 4-C62 and C61-6, 4-C62 and C61-7, 4-P14A and P16A-3, 5-C94-3.
J	Volume 1, page 2-3600 inv-3 revised. Volume 2, chapter 5, second page of contents revised, removes pages 5-PED-1 through 5-PED-22. Chapter 6 added and Appendix 1, pages 16, 17, and 18 removed and new pages added.
K	Publication Change Order 11170. Record of Revisions for volumes 1 and 2 revised. Removed pages 15 through 31 of volume 2, Appendix 1 and replaced with revised pages.
L (10-5-65)	Change Orders 10344 and 10708. Pages v, vi, vii, viii of volume 1 revised. Chapter 4 contents page, 4-HA19-3, 4-HA37 and HA43-10, 4-P14C and P16A-1, 4-P14C and P16-2, 4-P14C and P16-A-3, chapter 5 contents pages, 5-C84-1, 5-C84-2, 5-C84-3 (new pages), 3, 4, 7, and 8 (appendix) revised. Pages 5-C60-1, 5-C60-2, 5-C60-3, 5-C97-1, 5-C97-2, and 5-C97-3 added. Pages 5-HA27 and 5-HA28-1 and 5-HA27 and 5-HA28-2 revised.
M (12-13-65)	Change Order 12131. Appendix 1; pages 16 through 31 revised and pages 32 through 47 added.
N (5-13-66)	Publication Change Order 12940. New peripheral equipment cards added to chapter 6; ADH, ITA/ITB/ITC, ITD, TYA, OJB, OYA, and UJB. Revised text for page; 6-OHA-1. Revised schematic for page 6-IAA, IAB-2. Appendix 1 revised. This revision obsoletes all editions of pin assignments- 1604 and 3600. Printed circuit cards, publication number 60106200, which is now included in this revision.
P (5-13-66)	Publication Change Order 13632. Pages 6-ISC-1 of chapter 6 is revised. The following new cards are added to chapter 6; ALA, AMF, AMG, AMH, AMI, ANB, ANC, AND, AUA, EUA, EUC, EVB, FCA, FCB, FDA, FGA, FHA, FIA, FJA, FKA, FLA, FLB, FMA, FNA, FPA, FRA, FSA, FTA, FUA, FVA, FWA, FYA, JBA, JCA, JDA, and OTA.
R (2-13-67)	Publications Change Order 15800. The following new cards added to chapter 6; AIB, AKA, AOA, ATA, ATB, AVA, AYA, BAA, BAB, BBA, BCA, EEG, EEH, EWA, EWB, EZA, FAB, FOA, FOB,

Publication No. 60042900

REVISION LETTERS I, O, Q AND X ARE NOT USED

Address comments concerning this manual to:

Control Data Corporation
Publications and Graphics Division
4201 North Lexington Avenue
St. Paul, Minnesota 55112

or use Comment Sheet in the back of this manual.

Printed in the United States of America

REVISION RECORD (CONT'D)

REVISION	DESCRIPTION
R	FRB, FEC, FRD, FSB, FUB, FWB, FXB, GAA, GBA, GCA, GCB, GCC, GCD, IOB, IOC, IOD,
(Cont'd)	JEB, JEC, ONA, OUA, OVA, UEA, UHB, UIA, UJC, UKA, and UKB.
S	Publications Change Order 16541. The following new cards are added; AHC, AMJ, AMK, AMI, AVB,
(6-23-67)	AVC, AVD, AYB, BCB, BDA, BFA, BGA, BHA, BHB, BIA, BJA, EEK, EEL, EEM, EEO, EUD,
	EWC, FCC, FCD, FCE, FGB, FGC, FOC, FOD, FOE, FOF, FOG, FOH, FVB, FXC, GAB, GAC,
	GDA, GEA, GFA, GFB, GFC, GGA, HAA, IOE, IOF, ISH, JAD, JAE, JAF, JAG, OSC, OVB, TAA,
	ULA.
T	Engineering Change Order 20995, publications change only. The following new cards are added;
(11-22-68)	Card type 144, CC10, ADG, AMM, AMN, AMO, AMP, AMQ, AUB, AUC, AZA, BEA/B, BMA,
	BOA, BRA, BTA, BUA, EJA, FMB, FYB, GHA, GIA, GIB, GOA, GSB, HAB, IOG, IVA, IVB, IVC,
	JAH, JAI, JED, JEE, JFA, JHB, JJA, JLA, JOA, JPA, OGD, OWB, PJA, PJB, UPA, URA, USA.
	The documentation for the following cards is affected by either revisions or page number changes;
	Card type 54, 74; HA18; C07C; HA20; HA27; HA28; HA35; AMF through AML; AUA, AVA, through
	AVD; FCA through FCE; FGA through FGC; FMA; FOA through FOH; FXB, FXC, FYA, HAA, IOB
	through IOF; JAD through JAG; UAA, UAB, UHB, ULA, pages 5, 20, and 21 under appendix 1.
	The following miscellaneous changes are being made: expansion from two to three volumes, re-
	labeling of chapter 6 tabs, and appendix 1 tab repositioned.
U	Engineering Change Order 28728, publications change only. Incorporates publications change
(8-9-71)	from the following ECO's: 24045A, 23441, 20211, 21766, and FCO PR1168. The following pages
	are revised: 3-HA14-3, V5-E08-2, 5-97-1, 5-97-2, 5-HA20-1, appendix 1 page 15.
V	Engineering Change Order 36403, publications change only. No effect on this publication.
(6-10-75)	
W	Manual revised; includes Engineering Change Order 37817, publications change only. Page
(2-23-77)	3-HA14-3 is revised.

Publication No.
60042900

CHAPTER 6. PERIPHERAL EQUIPMENT CARDS*

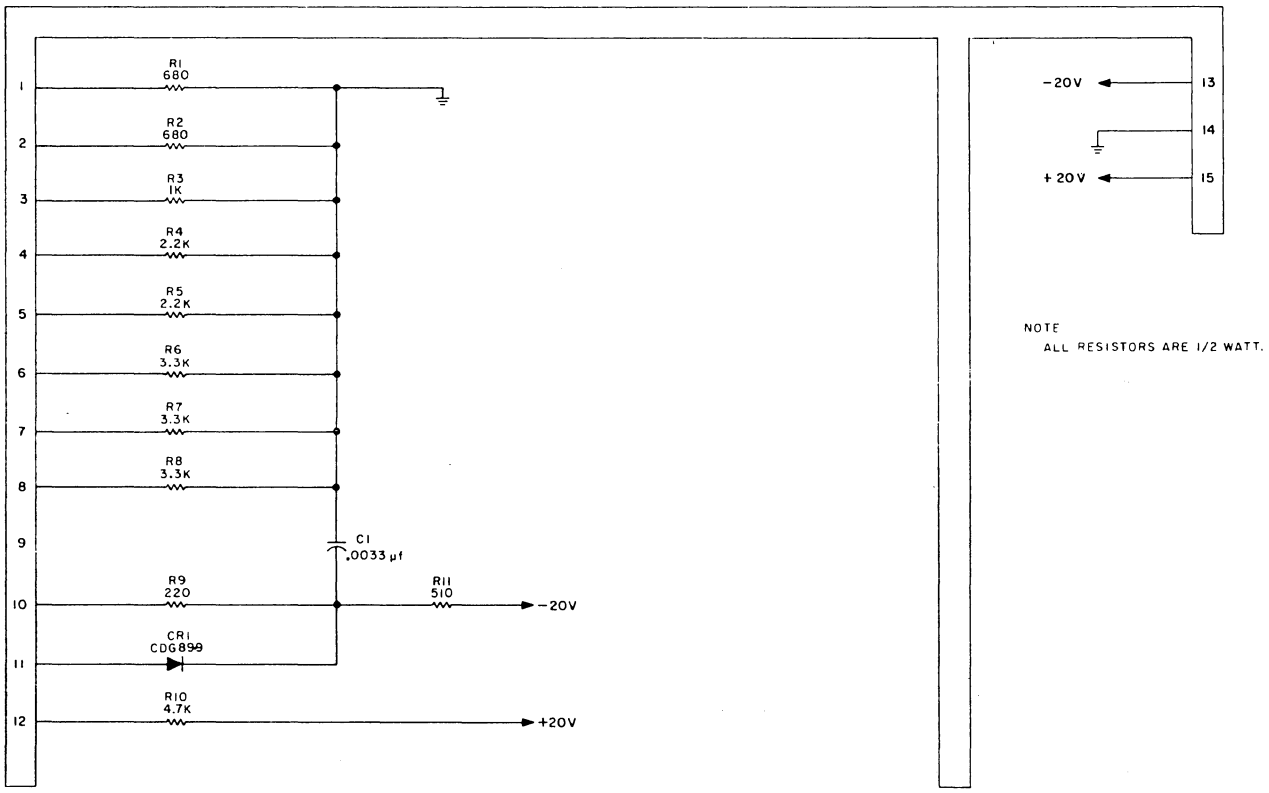
(Types H-- Thru Z--)

Resistor Termination	HAA, HAB
Relay Puller	IAA, IAB
Power Emitter Follower	IBA
Dual Driver	ICA
Write Driver	IIA
Flip-Flop Write Driver	IJA
Output Amplifier	IKA
Voice Coil Driver	ILA
Output Amplifier	INA
Head Selector	IOB, IOC, IOD, IOE, IOF, IOG
Output Amplifier	IPA
Output Amplifier	IQA
Output Amplifier	ISC
Output Amplifier	ISH
Pulse Delay and Output Amplifier	ITA, ITB, ITC, ITD
Gated Oscillator	IVA, IVB, IVC
Output Amplifier	IYA
Speed Detector	JAD, JAE, JAF, JAG, JAH, JAI
Positive Voltage Reference Switch	JBA
Negative Voltage Reference Switch	JCA
Long Stroke and Short Stroke Switch	JDA
Tuned Amplifier	JEB, JEC
Tuned Amplifier	JED, JEE
Ramp Generator	JFA
Write Driver	JHB
Transmitters	JJA, JLA
Current Controlled Lamp Drivers	JOA, JPA
Photocell Amplifier	OAA
Dual Photocell Amplifier	OCA
Read Peak Detector	ODA
Input Amplifier	OFA
Peak Detector	OGA, OGB, OGC

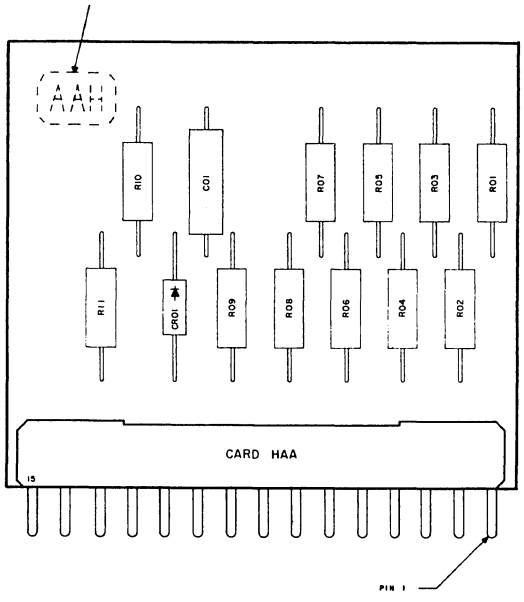
*Refer to Volume 2 for Card Types A-- thru G--.

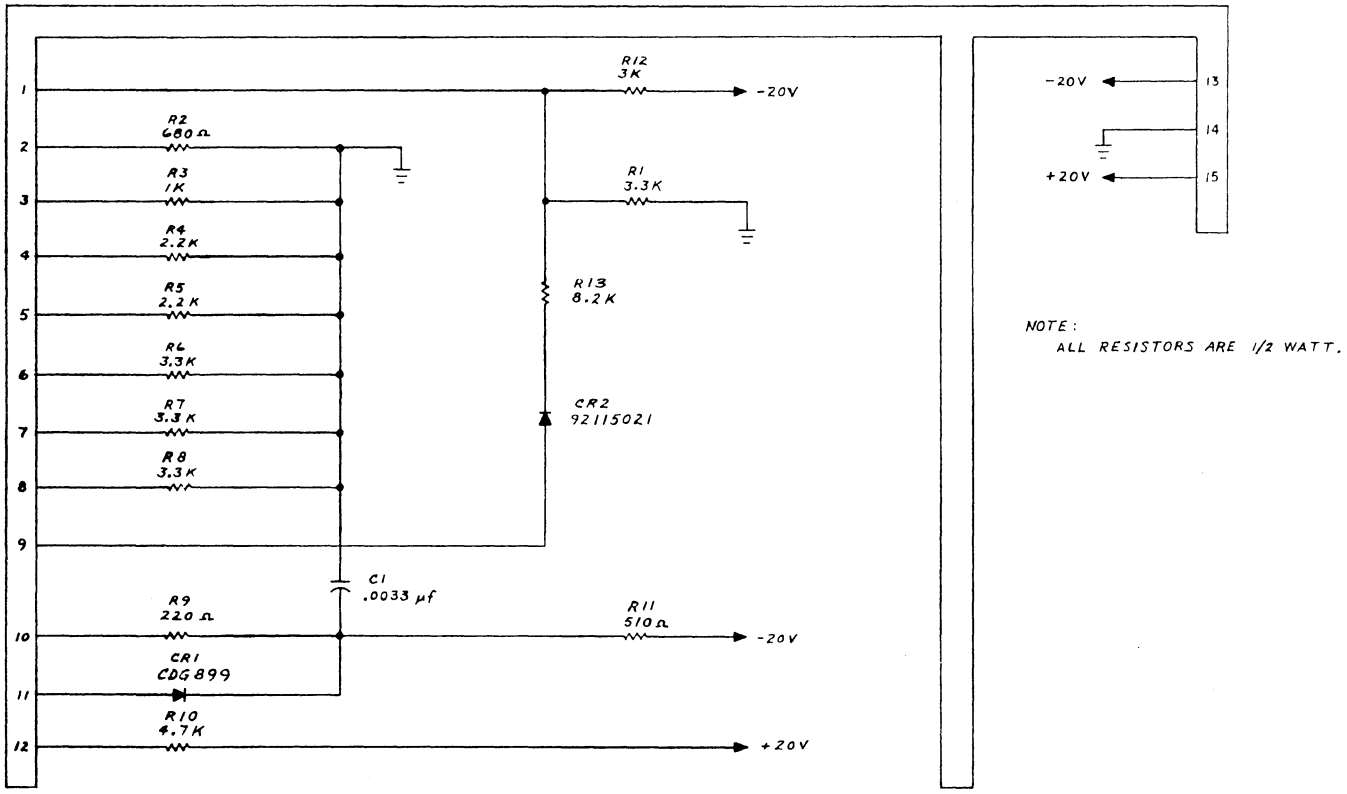
Peak Detector	OGD
Peak Detector	OHA
Input Amplifier	OIA
Long Term Delay	OJB
Input Amplifier	OKA
Flyback Verify Flip-Flop	OLA
Input Amplifier, High Fan-Out	OMA
Photocell Amplifier	ONA
Input Amplifier	OPA
Input Amplifier	OQA
Comparator and Readout	ORA
Input Amplifier	OSA, OSB, OSC
Output Amplifier	OSC
Level Switch	OTA
Schmitt Trigger	OUA
Gated Pulse Shaper	OVA, OVB
Voltage Sensor	OWB
Input Amplifier	OYA
Dual Line Receivers	PJA, PJB
Dual Photodiode Amplifier	TAA
Adjustable Delay	UAA, UAB
Double Inverter	UBA
Adjustable Pulse Delay	UCB
Oscillator Calibrator	UEA
Voltage Controlled Delay	UFA, UFB
Voltage Controlled Pulse Delay	UGA
Adjustable Short Term Delay	UHB
Pulse Shaper	UIA
Adjustable Long Term Delay	UJB, UJC
Gated Toggle Flip-Flop	UKA
Gated Toggle Flip-Flop	UKB

AC Write Current Sensor and Delay	ULA
One-Shot Multivibrator	UPA
One-Shot Delay Card	URA
One-shot Delay Card	USA
Pulse Shaper	XKA, XKC

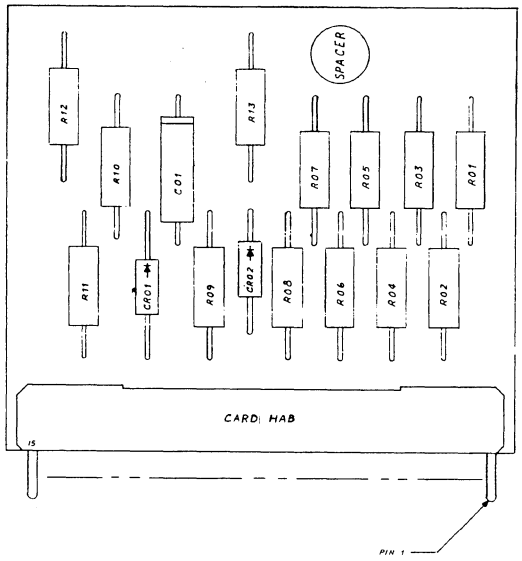

R1
680
R2
680
R3
1K
R4
2.2K
R5
2.2K
R6
3.3K
R7
3.3K
R8
3.3K
C1
.0033 µf
R9
220
R11
510
-20V
CR1
CDG899
R10
4.7K
+20V
1
2
3
4
5
6
7
8
9
10
11
12
-20V
+20V
13
14
15
NOTE
ALL RESISTORS ARE 1/2 WATT.

HAA


R10
C01
R07
R05
R03
R01
R11
CR01
R09
R08
R06
R04
R02
CARD HAA
15
PIN 1


R12
3K
-20V
R2
680Ω
R3
1K
R4
2.2K
R5
2.2K
R6
3.3K
R7
3.3K
R8
3.3K
R1
3.3K
R13
8.2K
CR2
92115021
C1
.0033 μf
R9
220Ω
R11
510Ω
-20V
CR1
CDG899
R10
4.7K
+20V
-20V
13
14
+20V
15
NOTE:
ALL RESISTORS ARE 1/2 WATT.

HAB

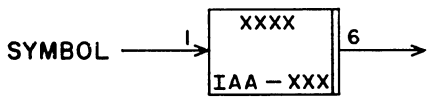

SPACER
R12
R10
C01
R13
R07
R05
R03
R01
R11
CR01
R09
CR02
R08
R06
R04
R02
CARD: HAB
15
PIN 1

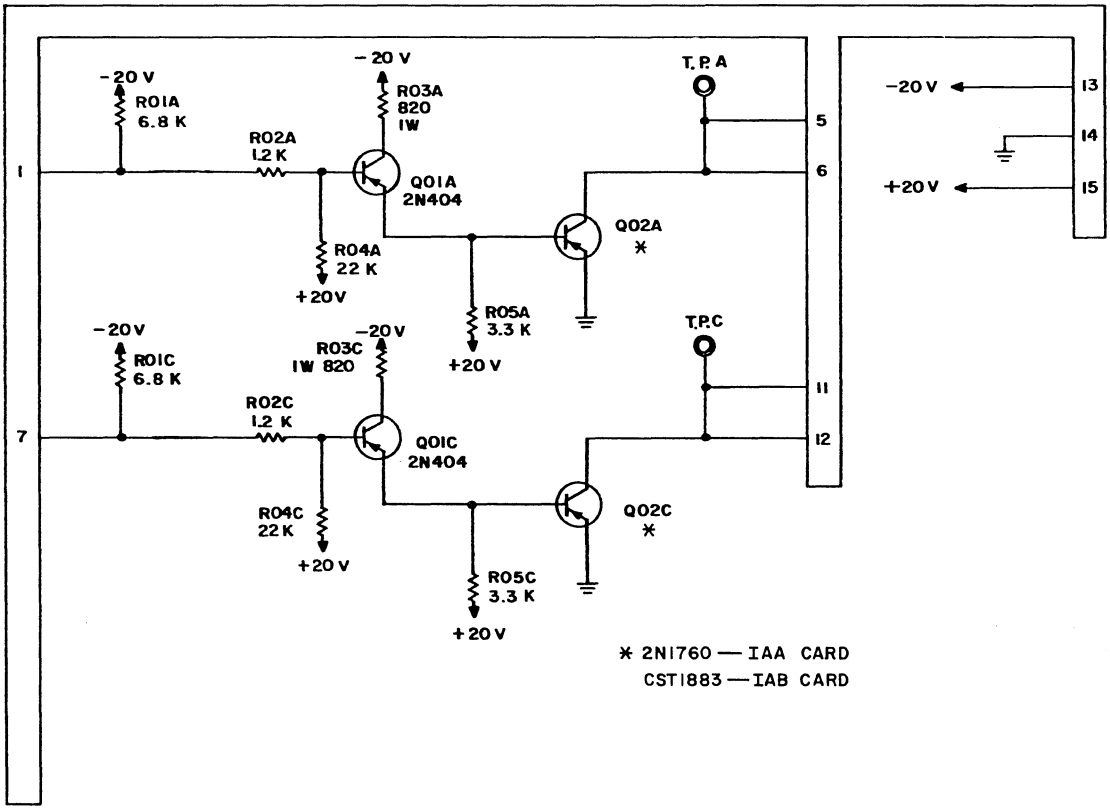
RELAY PULLER
IAA, IAB

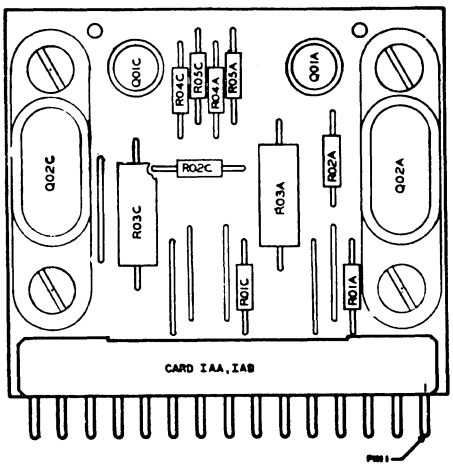
This circuit is used to drive inductive loads such as relays and solenoids and loads with high current surges such as incandescent lamps and the discharge of capacitors. It is particularly useful in driving loads up to 0.6 amp which are terminated at negative voltages from -5v to -36v. IAB cards drive loads to 0.4 amp.

The relay puller circuit can also be used as a slow L---card. The input-output voltage levels are the same for both cards.

The input stage of the relay puller circuit has its transistor connected as an emitter follower with the collector returned to -20v through a limiting resistor R03. The first stage emitter follower current does not flow through the load as it does in circuits such as the 55 card. The only current flowing to the load in the turnoff condition is the leakage current of the output transistor. The circuit limits collector voltage on Q01 to -20v; Q02 may have excursions to -36v. Turnon time is 5 usec maximum and turnoff switching is 25 usec maximum.




-20 V
R01A
6.8 K
R02A
1.2 K
-20 V
R03A
820
1W
Q01A
2N404
R04A
22 K
+20V
R05A
3.3 K
+20 V
Q02A
*
T.P.A
1
5
6
-20 V
13
14
+20 V
15
-20V
R01C
6.8 K
R03C
1W 820
-20V
R02C
1.2 K
Q01C
2N404
R04C
22 K
+20 V
R05C
3.3 K
+20 V
Q02C
*
T.P.C
7
11
12
* 2N1760 — IAA CARD
CST1883 — IAB CARD


Q01C
R04C
R05C
R04A
R03A
Q01A
Q02C
R02C
R03C
R03A
R02A
Q02A
R01C
R01A
CARD IAA, IAB

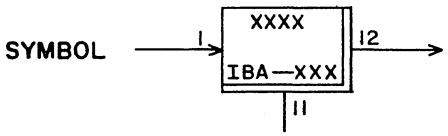
POWER EMITTER FOLLOWER

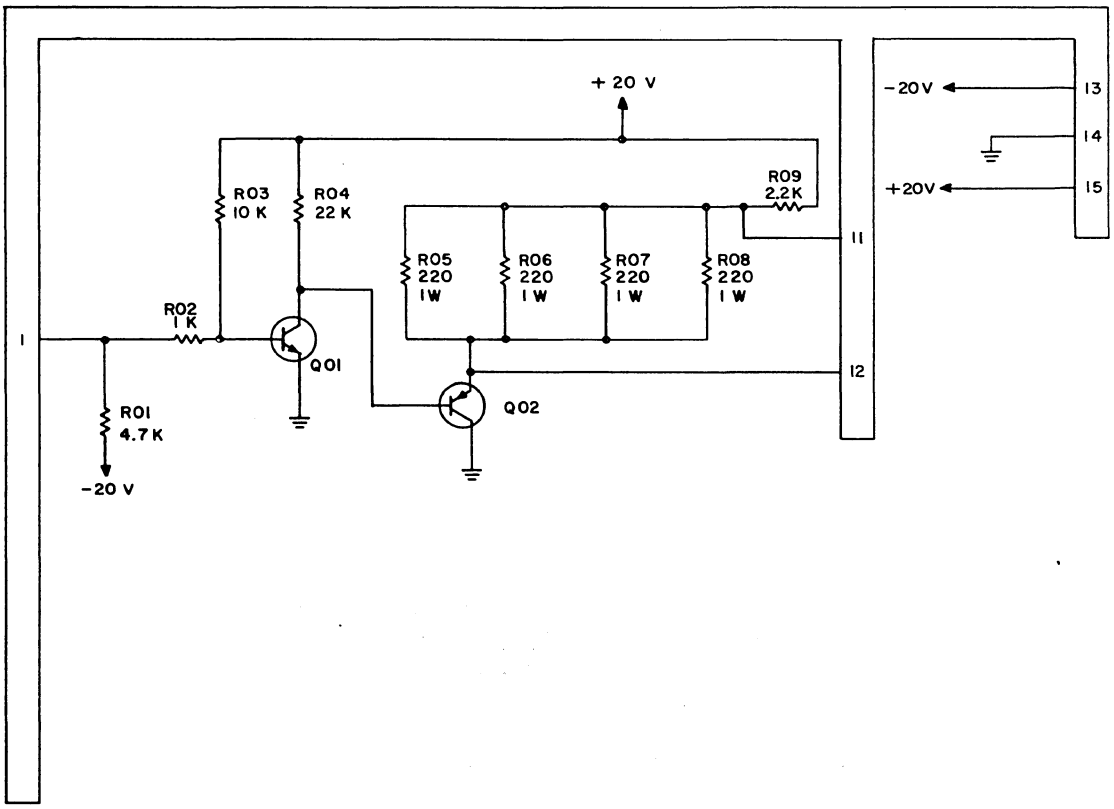
IBA

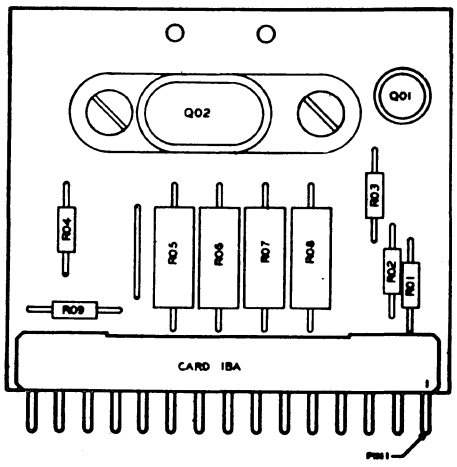
This circuit, used with a solid-state H switch (capstan drive circuit), drives diagonally opposite legs of the switch. A separate card of this type drives a switching transistor which provides a 2-msec double-magnitude current pulse to reduce actuation time.

The circuit differs from the regular inverter circuit in that the output load is returned to +20v instead of -20v.

Turnon time varies from 1 to 20 usec with the current limiting resistor output connected to +20v. Turnoff switching ranges from 5 to 50 usec. Loads on pins 11 and 12 should require a total of 0.6 amp or less and be terminated to -12v or less.




+ 20 V
-20V
+20V
13
14
15
11
12
1
R01
4.7 K
-20 V
R02
1 K
R03
10 K
R04
22 K
R05
220
1W
R06
220
1 W
R07
220
1 W
R08
220
1 W
R09
2.2K
Q01
Q02


Q02
Q01
R04
R05
R06
R07
R08
R03
R02
R01
R09
CARD IBA

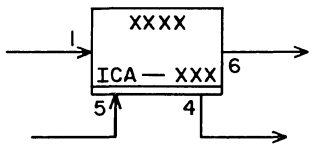
DUAL DRIVER

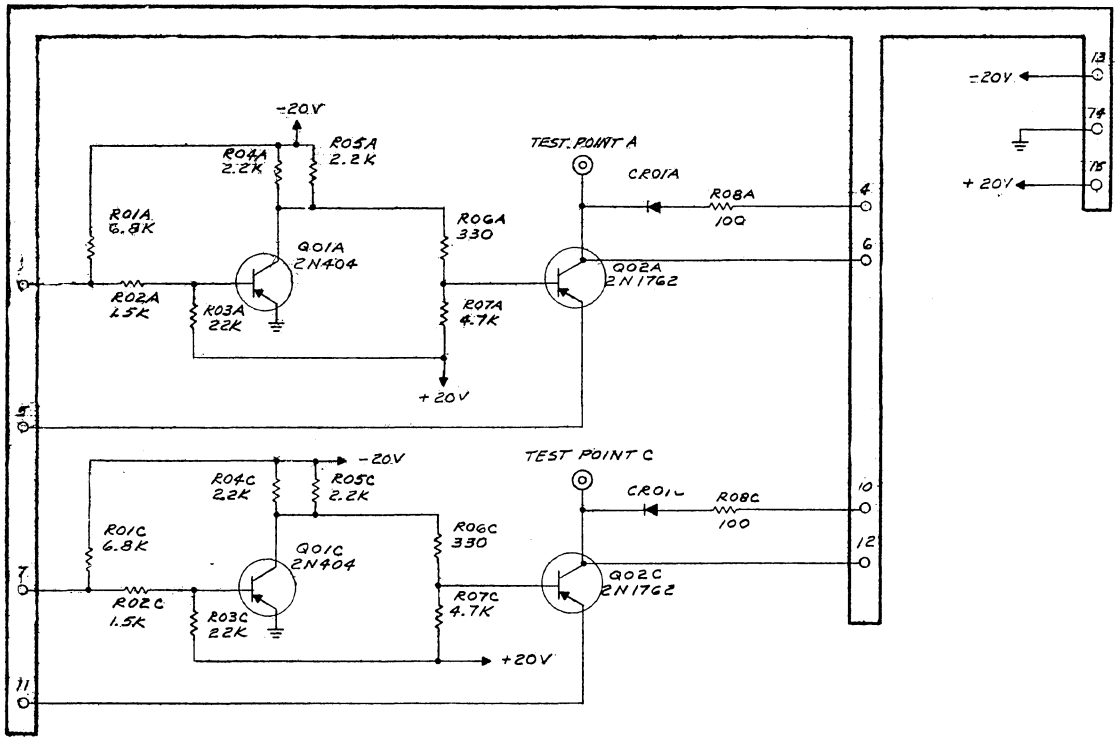
ICA

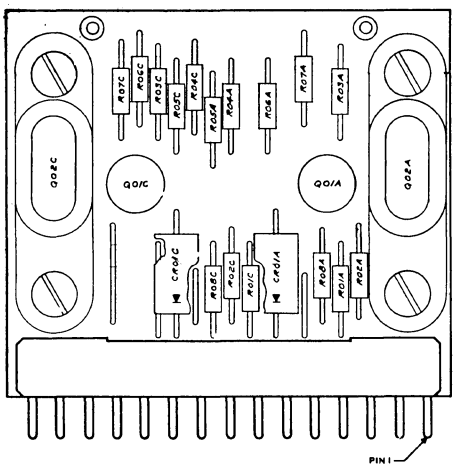
This circuit was designed to drive stepping switches and other inductive loads in the 180 Data Collector. It is particularly useful in driving loads up to 0.4 amp which are terminated at negative voltages from -5v to -60v. A small power transistor in its output circuit allows it to be used for driving incandescent lamps or discharging capacitors where the surge current reduces to 0.4 ampere within 50 milliseconds.

The circuit contains several differences when compared to more conventional output drivers. Each of the two circuits has an output that is double inverting from the first input (pin 1, 7) and noninverting from the second input (pin 5, 11). Both inputs must be driven toward ground (+ AND) to cause the output to be driven toward ground. The first input operates from normal logic "0" (-1/2v) and logic "1" (-3v) levels. The second input may be grounded directly or switched to ground by a circuit such as the IAA or ICA, which has a switching capability equal to the output of the ICA card. To switch off completely, the second input should be allowed to go to -15v. CR01 and R08 are available at pins 4, 10 and protect output transistors from inductive kicks when clamped to the load termination voltage (-60v or less).

SYMBOL




-20V
R04A 2.2K
R05A 2.2K
R01A 6.8K
R02A 1.5K
R03A 22K
Q01A 2N404
R06A 330
R07A 4.7K
+20V
TEST POINT A
CR01A
R08A 100
Q02A 2N1762
-20V
R04C 2.2K
R05C 2.2K
R01C 6.8K
R02C 1.5K
R03C 22K
Q01C 2N404
R06C 330
R07C 4.7K
+20V
TEST POINT C
CR01C
R08C 100
Q02C 2N1762
-20V
+20V
+20V
1
5
7
11
4
6
10
12
13
14
15


R07C
R05C
R03C
R04C
R02C
R01C
R04A
R07A
R03A
Q02C
Q01C
Q01A
Q02A
CR01C
CR01A
R08C
R01C
R08A
R01A
R02A
PIN 1

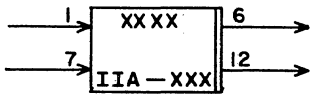
WRITE DRIVER
IIA

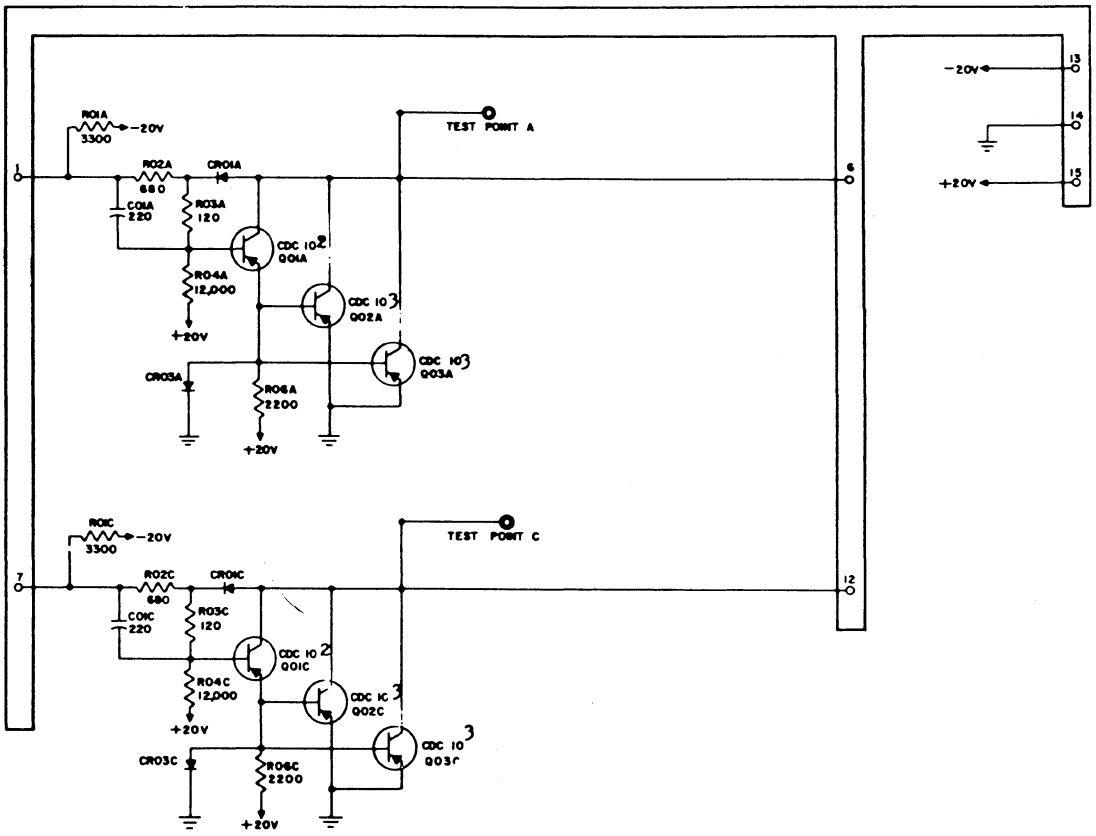
The write driver circuit switches the current through the write heads during a write operation. Each card contains two independent drive circuits whose outputs are connected to opposite ends of the windings of the write head.

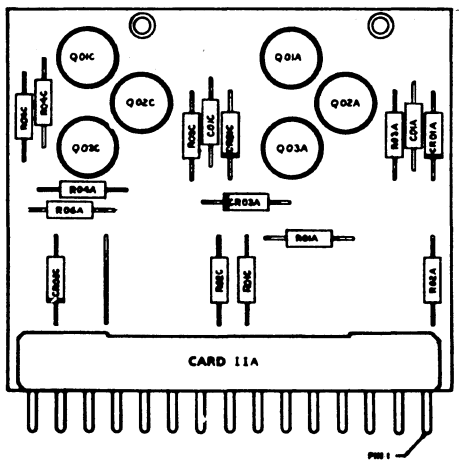
The circuit consists of transistor Q01, connected as an emitter follower, and transistors Q02 and Q03 connected in parallel as amplifiers. A "0" input results in 0v at the base of Q01. The emitter of Q01 is clamped to ground by CR03; neither Q02 nor Q03 conduct. Consequently, no current flows to the output pin.

A "1" input signal causes Q01 to conduct; conduction is held below saturation by feedback diode CR01. The negative voltage applied to the bases of Q02 and Q03 causes these transistors to conduct. Current, therefore, flows through the emitter of Q02 and Q03 to the collector and then to the output pin. Maximum output current is 160 ma to a load terminated to -20v or less.

SYMBOL




R01A
3300
-20V
TEST POINT A
R02A
680
CR01A
C01A
220
R03A
120
CDC 102
Q01A
R04A
12,000
CDC 103
Q02A
+20V
CR03A
CDC 103
Q03A
R06A
2200
+20V
R01C
3300
-20V
TEST POINT C
R02C
680
CR01C
C01C
220
R03C
120
CDC 102
Q01C
R04C
12,000
CDC 103
Q02C
+20V
CR03C
CDC 103
Q03C
R06C
2200
+20V
-20V
+20V
1
6
7
12
13
14
15


Q01C
Q02C
Q03C
Q01A
Q02A
Q03A
R04A
R06A
CR03A
CARD IIA

FLIP-FLOP WRITE DRIVER

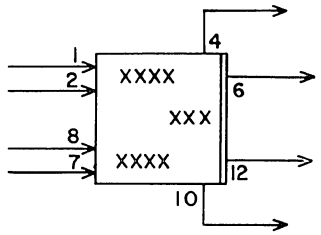
IJA

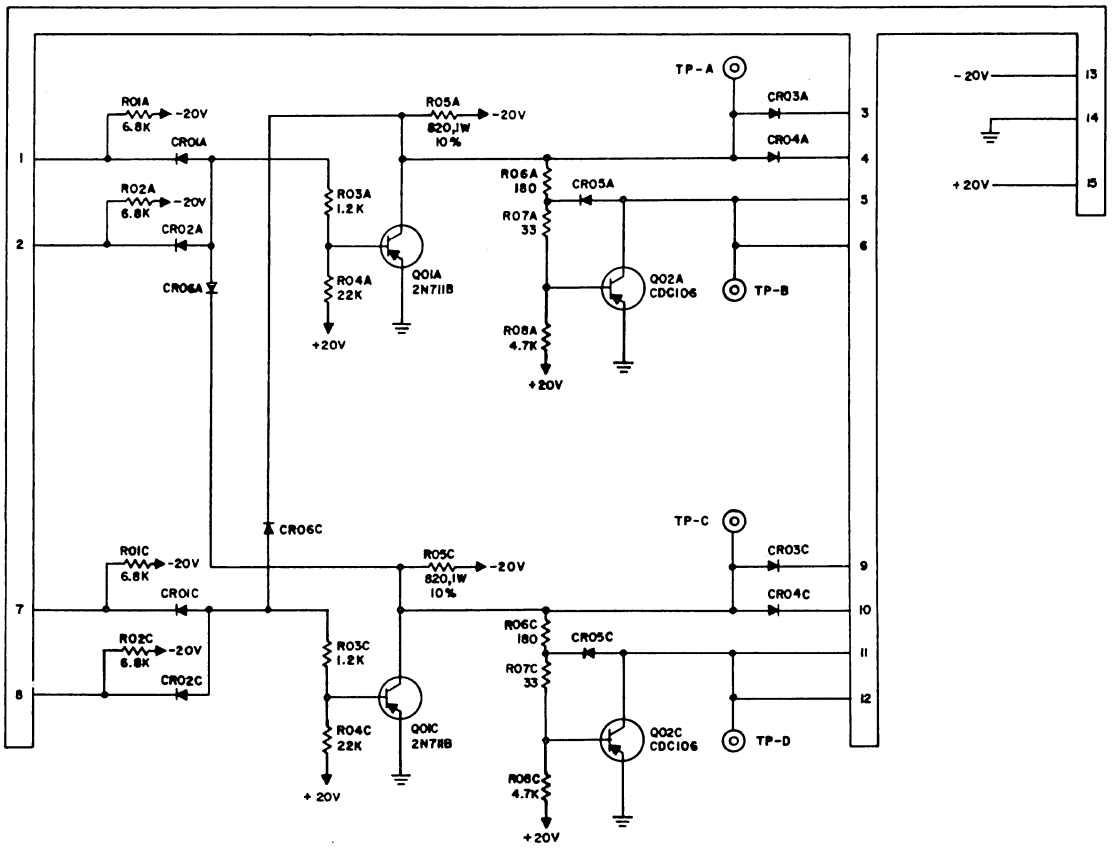
A flip-flop and write driver circuit are combined on one card (refer to IIA write driver discussion).

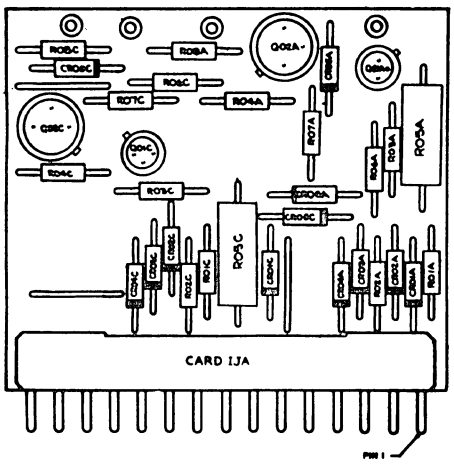
The circuit consists of two transistors (Q01A and Q01C) connected as a flip-flop, each with two OR inputs (diodes CR01 and CR02). Each side of the flip-flop is provided with two AND outputs (diodes CR03 and CR04). The remainder of the flip-flop output is used to drive transistors Q02A and Q02C, which supply up to 160 ma output load.

Because of the double inversion in this circuit, continuous "1" inputs to both sides of the flip-flop turn off both Q02A and Q02C to shut off write current.

SYMBOL




TP-A
TP-B
TP-C
TP-D
R01A
6.8K
-20V
CR01A
R02A
6.8K
-20V
CR02A
CR06A
R03A
1.2K
R04A
22K
+20V
Q01A
2N718B
R05A
820,1W
10%
-20V
R06A
180
CR05A
R07A
33
R08A
4.7K
+20V
Q02A
CDC106
CR03A
CR04A
CR06C
R01C
6.8K
-20V
CR01C
R02C
6.8K
-20V
CR02C
R03C
1.2K
R04C
22K
+20V
Q01C
2N718B
R05C
820,1W
10%
-20V
R06C
180
CR05C
R07C
33
R08C
4.7K
+20V
Q02C
CDC106
CR03C
CR04C
-20V
+20V
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15


CARD IJA

OUTPUT AMPLIFIER
IKA

The output amplifier card is used to interface from standard logic signals (0 to -3v) to equipment operating from excursions of +12v to -2v. One or two receivers may be connected to each amplifier circuit. Each receiver may be on a separate line and has a series 220-ohm input resistor. The other end of this resistor is clamped at +6.5v in the positive direction and at ground in the negative direction. It is also connected to the emitters of two gating transistors in each receiver.

Two identical circuits are provided on each card. Each circuit includes four transistors. Q01 inverts standard logic input signals. Q02 supplies current amplification of the inverted signal to provide drive in the positive direction. The output of Q02 is shifted 4 volts negative by CR01 to obtain an excursion above and below ground.

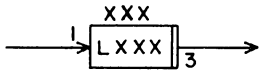
Q03 and Q04 are emitter followers which provide the output drive current. The positive drive current is limited by R06 in the collector of Q03 and the negative drive is limited by R08 in the collector of Q04. R09 limits collector voltage on Q04 during the positive output excursion.

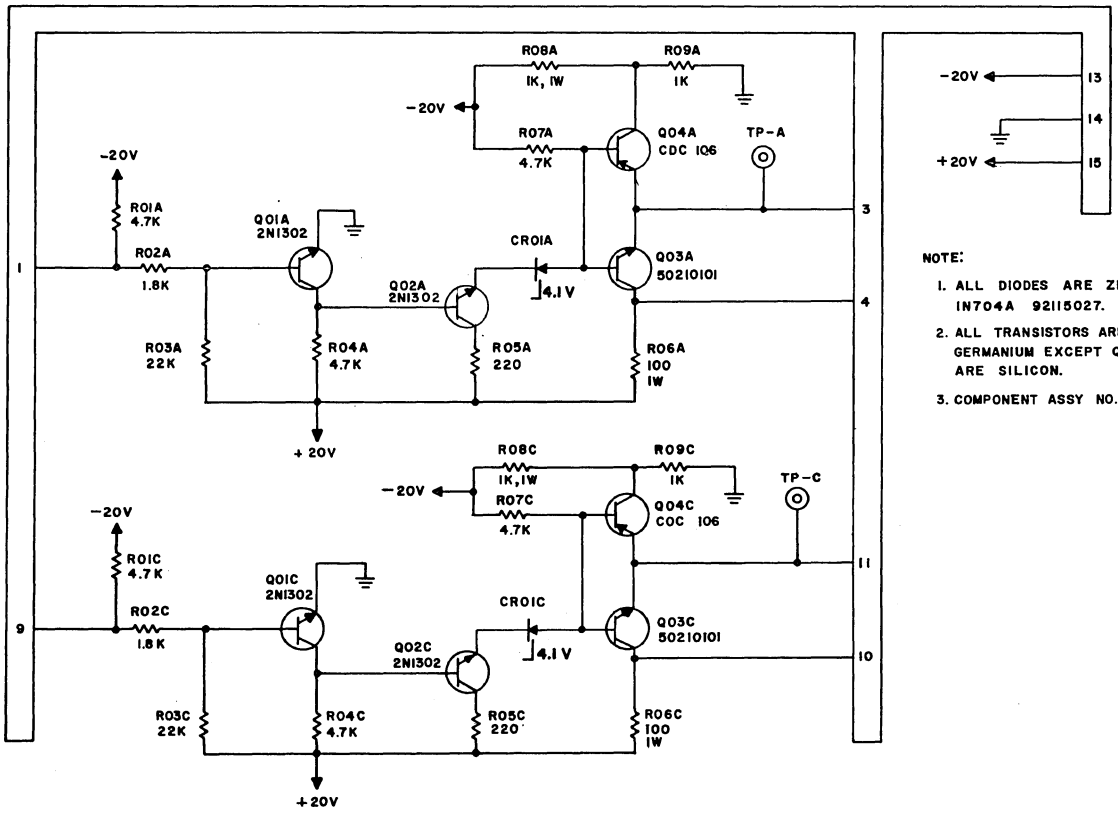
The positive output excursion of +12v will be reduced as the external load increases to about 70 ma. The negative output excursion of -2v has a current capability of about 15 ma.

Rise time to the +10v point is 1 microsecond maximum with a cable capacity of 4400 pf and two equivalent receiver loads in parallel. Fall time to the 0v point is 1 to 2 microseconds with this same load.

The circuit is subject to overloading the current limiting resistors R05 and R06 if an output is left shorted to ground while the input is a "1".

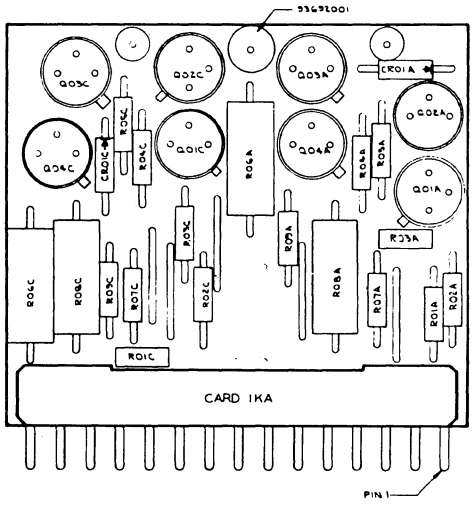
SYMBOL





NOTE:

1. ALL DIODES ARE ZENER IN704A 92115027.
2. ALL TRANSISTORS ARE GERMANIUM EXCEPT Q03 A,C ARE SILICON.
3. COMPONENT ASSY NO.50002000.



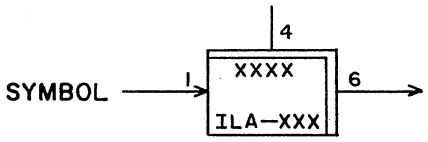
VOICE COIL DRIVER

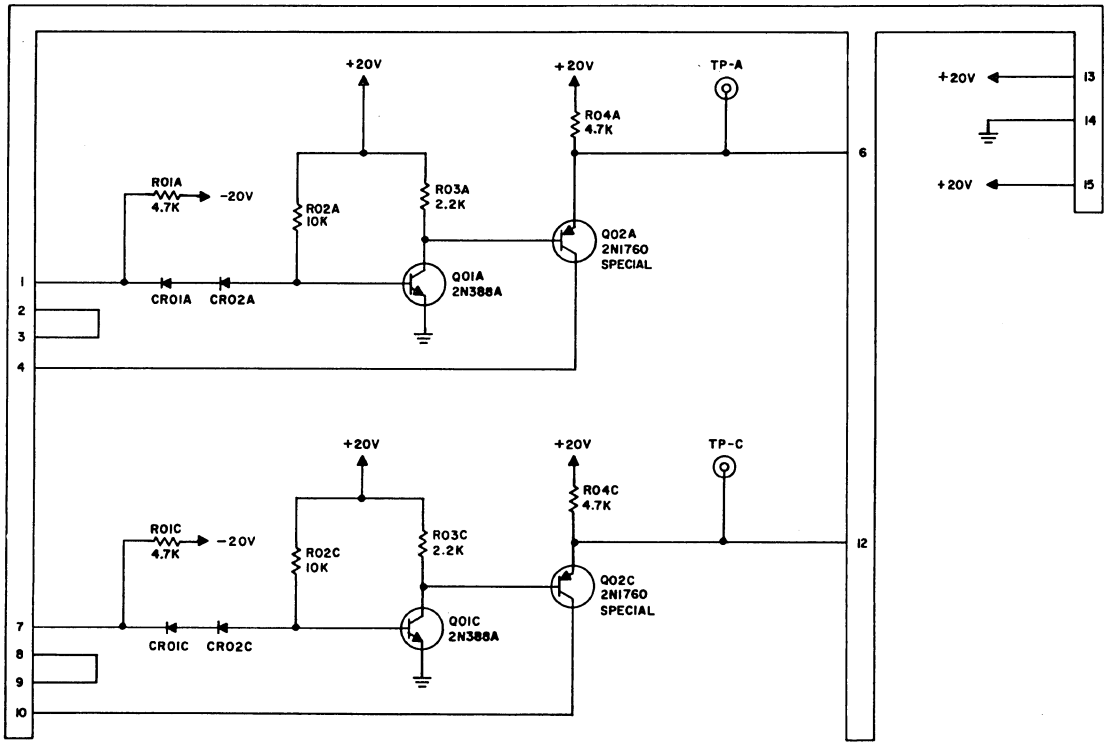
ILA

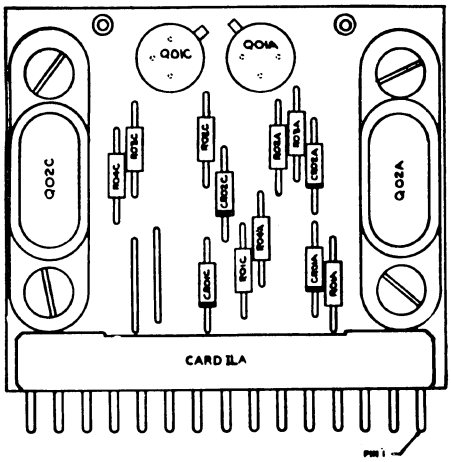
This circuit is used as a relay puller which drives inductive loads terminated at positive voltages of +12v or less.

Two circuits on this card are used as a push-pull capstan coil driver operating directly from a standard flip-flop.

The input stage is an inverting circuit using two forward drop silicon diodes CR01 and CR02 and high gain transistor Q01. The output stage, transistor Q02, is used as an emitter follower to drive a maximum load of 1¼ amperes. Separate grounds to pins 4 and 10 must be provided. Pins 2-3 and 8-9 are provided for interlocking purposes where circuits are paraleled on different ILA cards.




+20V
+20V
TP-A
R04A
4.7K
R01A
4.7K
-20V
R02A
10K
R03A
2.2K
Q02A
2N1760
SPECIAL
Q01A
2N388A
CR01A
CR02A
+20V
+20V
TP-C
R04C
4.7K
R01C
4.7K
-20V
R02C
10K
R03C
2.2K
Q02C
2N1760
SPECIAL
Q01C
2N388A
CR01C
CR02C
+20V
+20V
+20V
1
2
3
4
6
7
8
9
10
12
13
14
15


Q01C
Q01A
Q02C
Q02A
CARD ILA

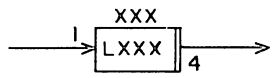
OUTPUT AMPLIFIER
INA

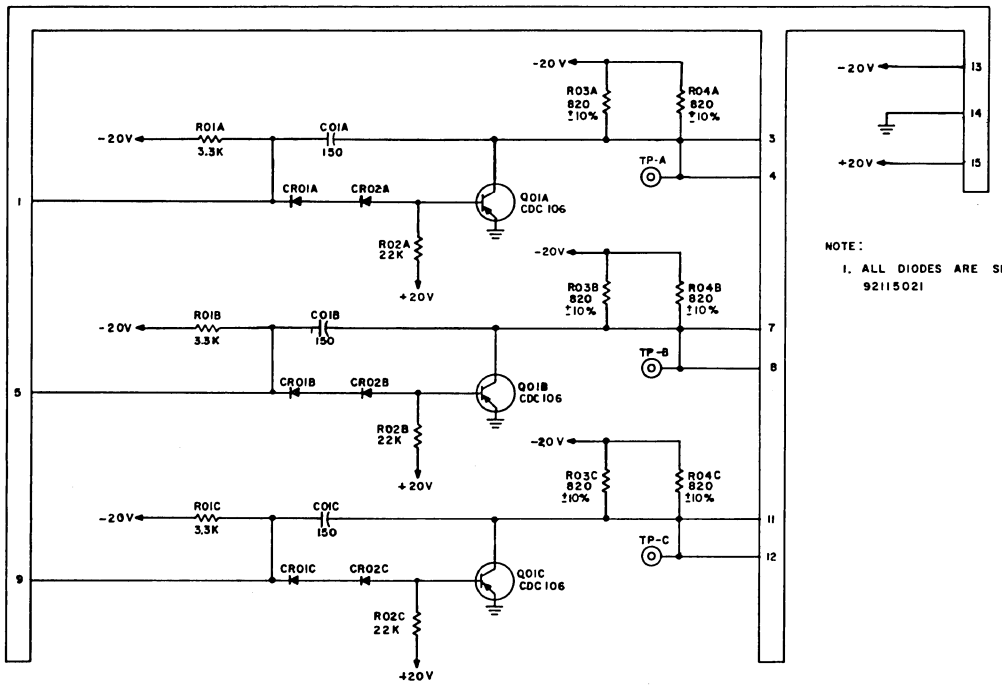
The output amplifier card is used to interface from standard logic signals (0 to -3v) to external equipment operating from excursions of 0 to -6v. The external load impedance is significant in determining the negative excursion and should closely approximate 200 ohms to ground for the standard excursion. This impedance will also approximately match twisted pair lines used in the cables between equipment.

Three identical circuits are used. Each is a switching type inverter with certain variations from a typical output circuit such as the type 62 card. A single stage of gain is used to provide the output current. This requires additional base current drive and is obtained by decreasing the input resistance and using two silicon diodes (CR01, CR02) in the base voltage divider.

With a 200-ohm load to ground, the positive excursion is 0 to -1/2v and the negative excursion is -5 1/2 to -7 1/2v. Rise and fall times are less than 3/4 usec if external cable capacity is 1000 pf or less.

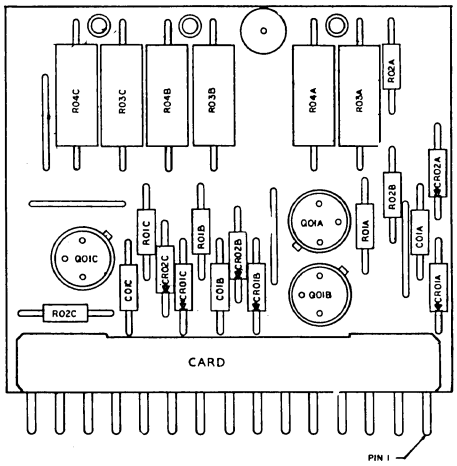
SYMBOL





NOTE:

1. ALL DIODES ARE SILICON 92115021



HEAD SELECTOR
IOB, IOC, IOD, IOE, IOF, IOG

These cards have two circuits, each of which will absorb up to 1.5A from a positive voltage (with the proper external resistor tied in to provide drive).

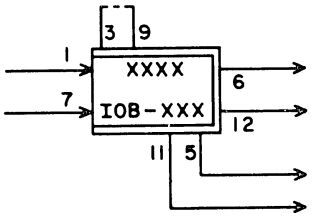
When Q01 is on, Q02 is held off. When Q02 is on, it furnishes base drive for Q03, which will accept up to 1.5A. The collector current for Q02 is determined by R04. For disc pak use, since only one out of 10 IOB circuits are on at any time, R04's on various circuits can be shared. To get the proper collector current for Q02 for disc paks, two R04's on various IOB's are tied in parallel by tying pins 3 or 9 together. For the disc file, 16 R04's are paralleled in this way.

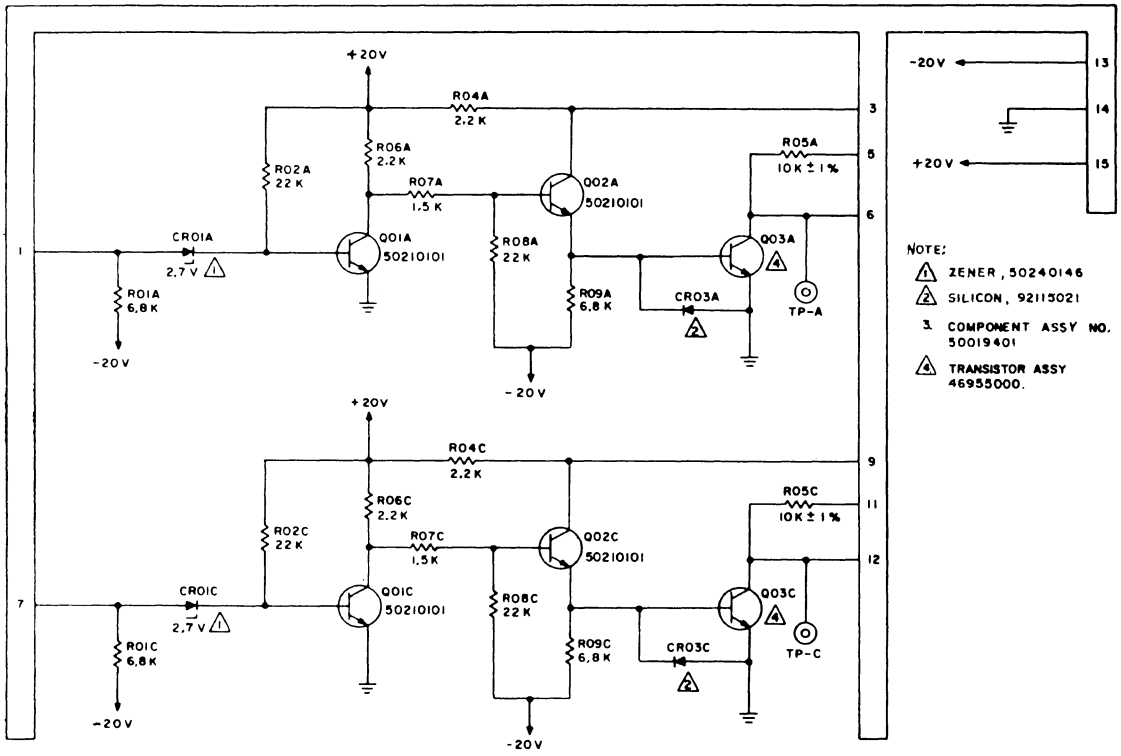
CR01 is a zener diode, used for level translation. The outputs at pins 5 and 11 are used for error detection (see cards ANB, ANC, AND, and AOA).

The IOC, IOE, and IOG cards are the same as the IOB, except that R03A, C replaces CR03A, C to give a faster turn-off.

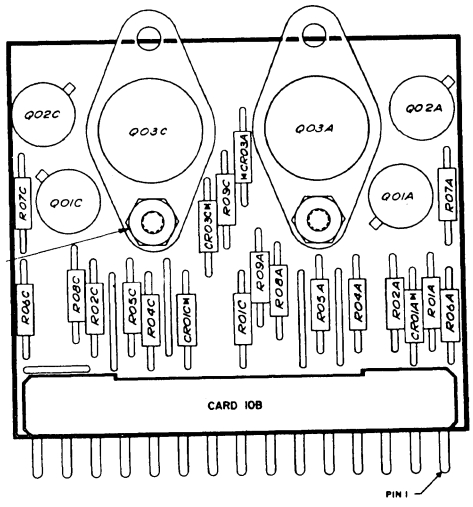
The IOD and IOF cards are the same as the IOB, except that CR02A, C are added to cut down input noise sensitivity; R09A, C values are changed to make turn off faster; and the network of C01, CR04, and R10 is added to control turn-on time. In this card, I_c = 0.6A.

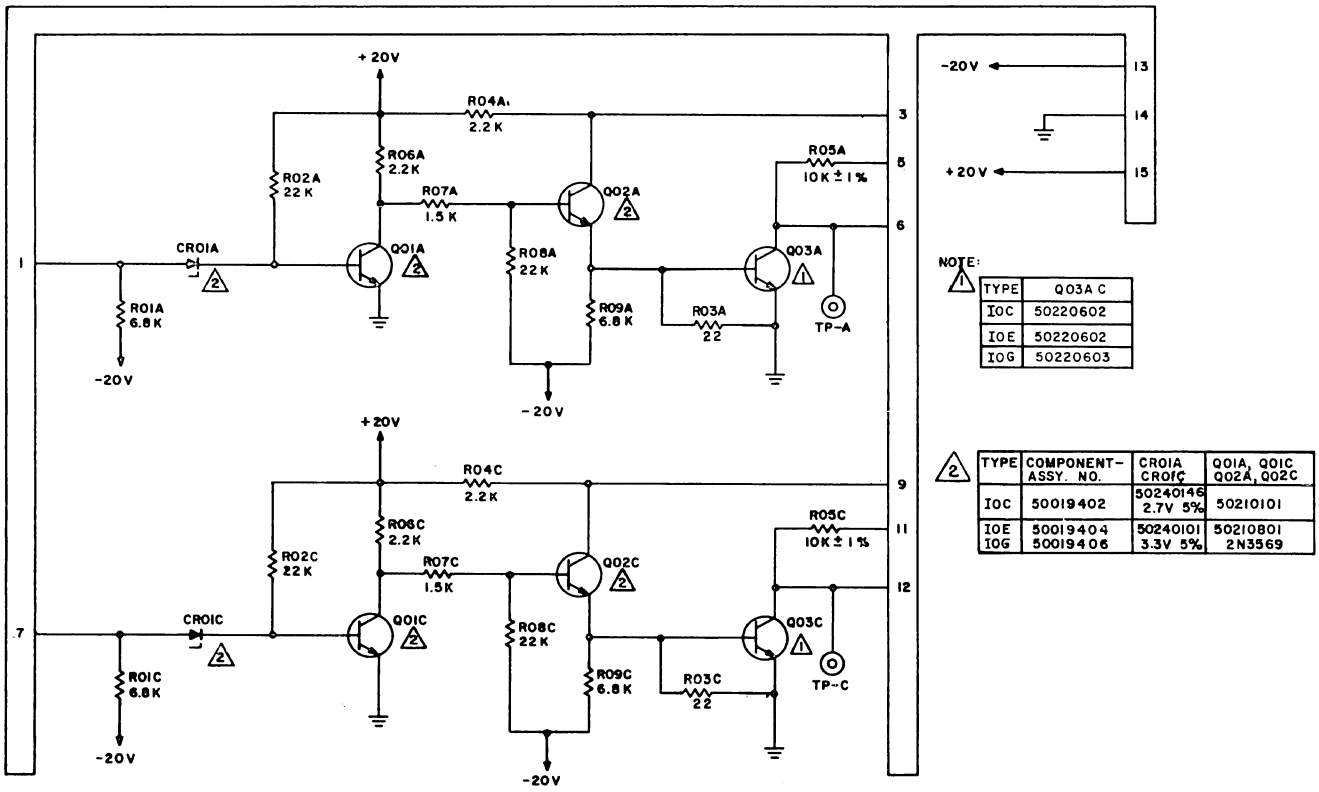
TYPICAL SYMBOL




+20V
R04A
2.2 K
R06A
2.2K
R02A
22 K
R07A
1.5 K
Q02A
50210101
R05A
10K ± 1%
CR01A
2.7V
Q01A
50210101
R08A
22K
Q03A
R01A
6.8K
R09A
6.8 K
CR03A
TP-A
-20V
-20V
+20V
R04C
2.2 K
R06C
2.2K
R02C
22 K
R07C
1.5K
Q02C
50210101
R05C
10K ± 1%
CR01C
2.7V
Q01C
50210101
R08C
22K
Q03C
R01C
6.8K
R09C
6.8 K
CR03C
TP-C
-20V
-20V
-20V
+20V
1
3
5
6
7
9
11
12
13
14
15
NOTE:
1 ZENER, 50240146
2 SILICON, 92115021
3 COMPONENT ASSY NO. 50019401
4 TRANSISTOR ASSY 46955000.

IOB


Q02C
Q03C
Q03A
Q02A
Q01C
Q01A
R07C
R07A
R06C
R02C
R05C
R04C
R02A
R04A
R05A
R08A
R03A
R01C
R01A
R06A
CR01C
CR03C
CR03A
CR01A
CARD 10B
PIN 1

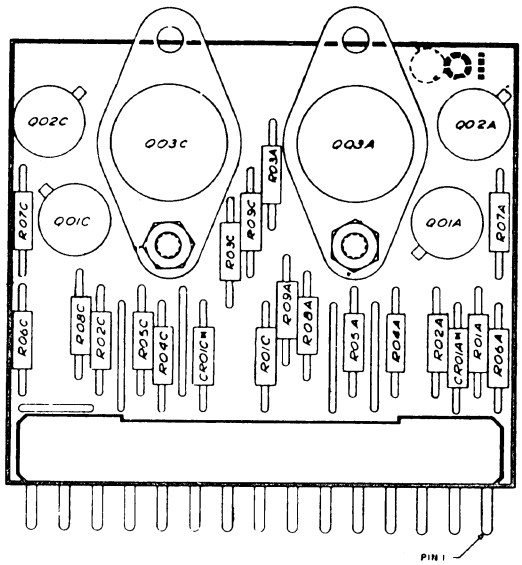


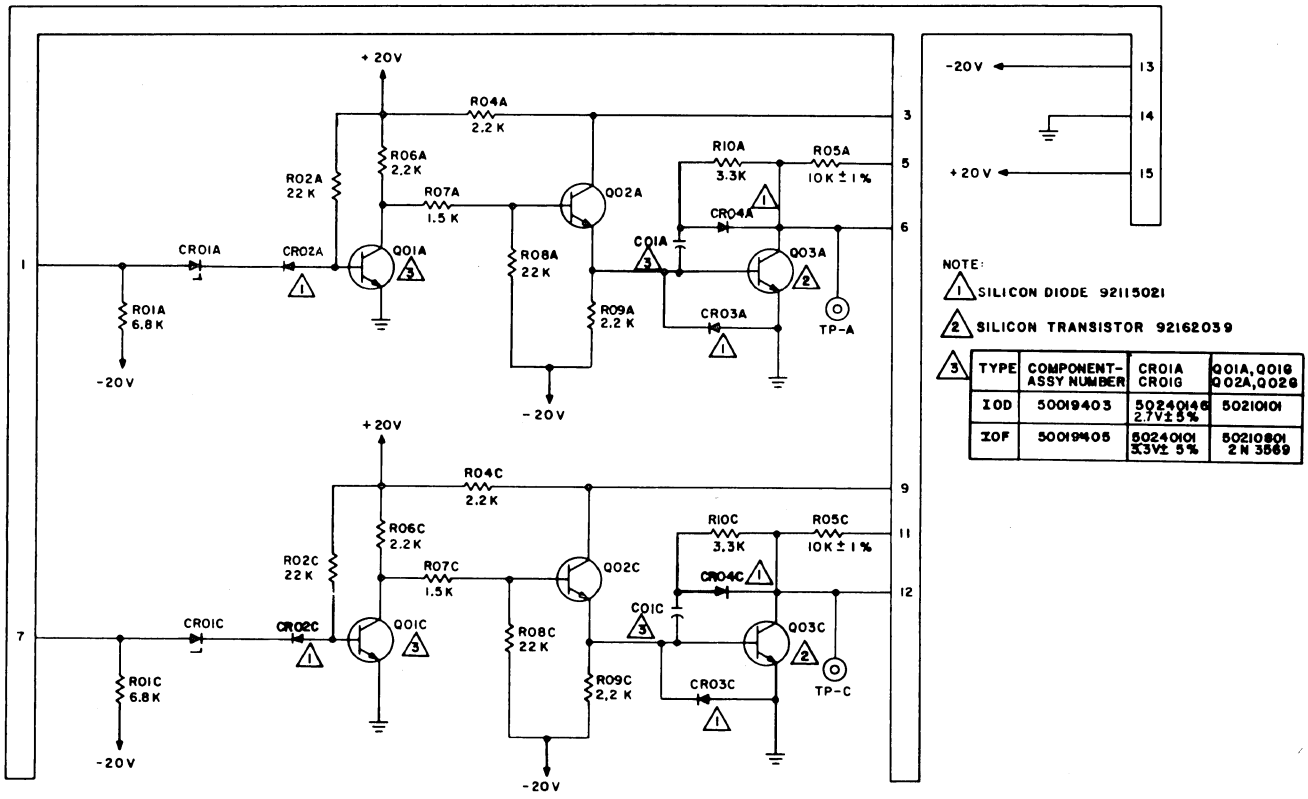
NOTE:

TYPE	Q03A C
IOC	50220602
IOE	50220602
IOG	50220603

TYPE	COMPONENT-ASSY. NO.	CR01A CR01C	Q01A, Q01C Q02A, Q02C
IOC	50019402	50240146 2.7V 5%	50210101
IOE IOG	50019404 50019406	50240101 3.3V 5%	50210801 2N3569

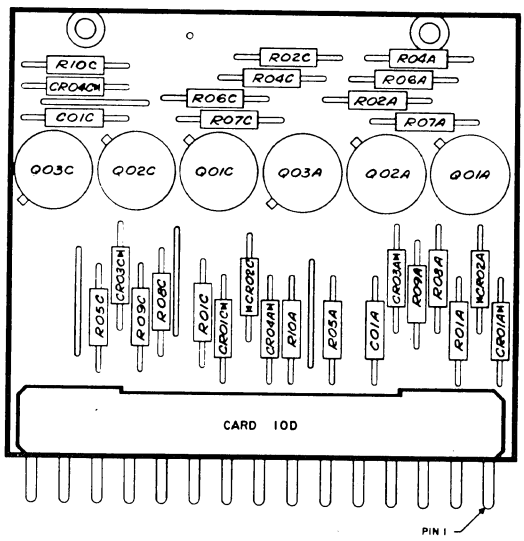
IOC, IOE, IOG





3 TYPE	COMPONENT-ASSY NUMBER	CR01A CR01G	Q01A, Q01G Q02A, Q02G
IOD	50019403	50240146 2.7V ± 5%	50210101
IOF	50019405	50240101 3.3V ± 5%	50210801 2N 3569

IOD, IOF

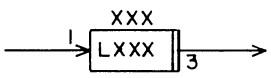


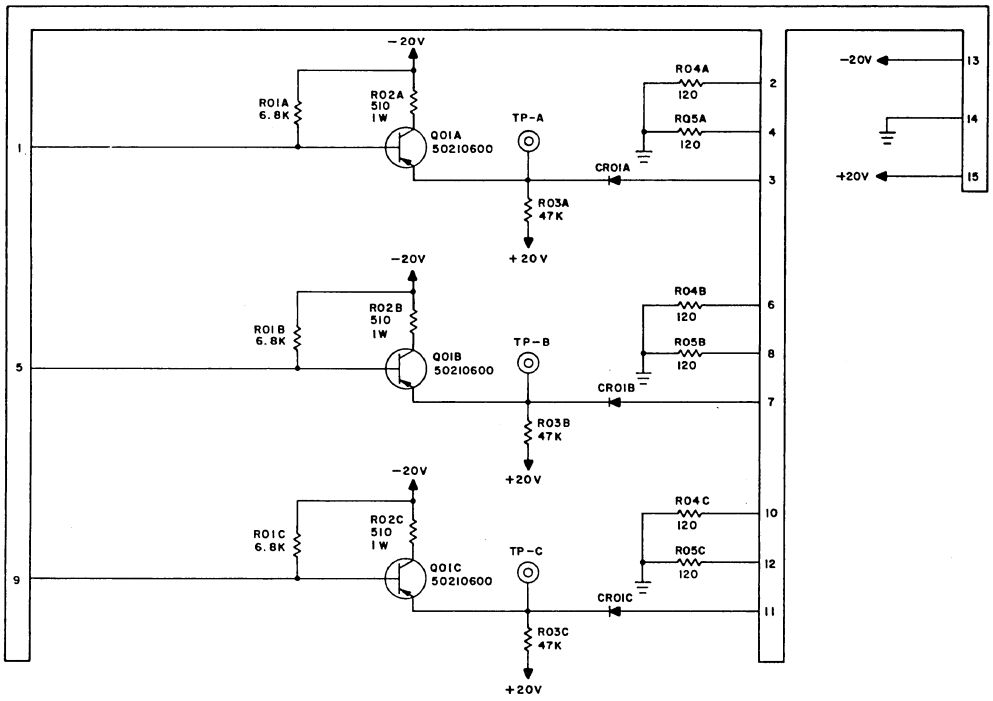
OUTPUT AMPLIFIER
IPA

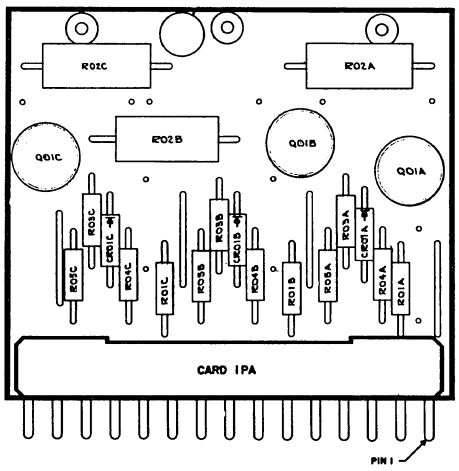
The IPA was initially designed to be used in a 699 tester adapter in conjunction with 9131 Tape Transports which have OPA receiver cards. The input is designed for standard logic signals (0 to -3v). Its output switches from 0v to -1.8v. The output should be terminated at the end of the line to match the impedance characteristic of the line. The IPA has resistors available by jumpering to its output pins for matching line impedance at the input to the line. In this application, one IPA was called on to drive six receivers (OPA) in parallel over a 25-ft. max. coax line. The IPA can be used to drive a twisted pair line if the line noise level is kept sufficiently low.

A logical "0" input (0v) provides a 0v output, and a logical "1" input (-3v) provides a -1.8v output. With a termination of 120 ohms to ground at both ends of the line, the IPA puts out 30 ma @ -1.8v. Switching times are as fast as 100 nsec, but being an emitter follower, it will vary with the switching speed of the input signal. Since the IPA circuit is an emitter follower, the output voltage will equal the input voltage, $-V_{BE}$ of Q01 - V_f of CR01. There are three identical circuits per card.

SYMBOL




-20V
R01A
6.8K
R02A
510
1W
Q01A
50210600
TP-A
R04A
120
R05A
120
CR01A
R03A
47K
+20V
1
2
3
4
-20V
13
14
+20V
15
-20V
R01B
6.8K
R02B
510
1W
Q01B
50210600
TP-B
R04B
120
R05B
120
CR01B
R03B
47K
+20V
5
6
7
8
-20V
R01C
6.8K
R02C
510
1W
Q01C
50210600
TP-C
R04C
120
R05C
120
CR01C
R03C
47K
+20V
9
10
11
12


R01C
R02A
R02B
Q01C
Q01B
Q01A
R05C
R03C
CR01C
R04C
R01C
R03B
CR01B
R04B
R01B
R05A
R03A
CR01A
R04A
R01A
CARD IPA
PIN 1

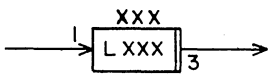
OUTPUT AMPLIFIER

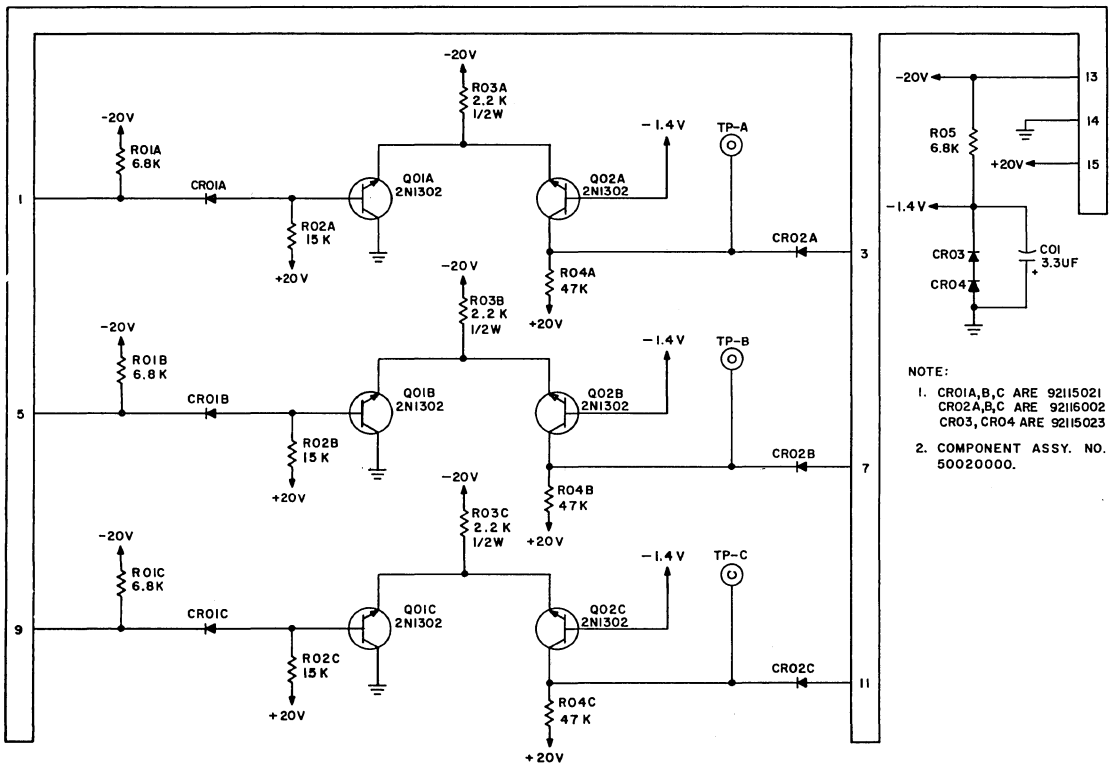
IQA

The output amplifier card, IQA, is used to interface from standard logic signals (0 to -3v) to a "n" type line driving a current mode receiver. Up to 8 outputs may be paralleled for daisy-chaining between tape handlers and an adaptor. Daisy-chaining is a term used to describe a series connection of an IQA output in one transport to a corresponding IQA output in another transport and so on to the end transport in the chain where the IQA output is connected to the line going to a receiver in the adaptor.

There are three identical circuits on each card and each circuit includes two transistors. Q01 and Q02 form a differential amplifier. CR03 and CR04 provide a nominal -1.4v at the base of Q02 for the switching threshold. Emitter resistor R03 provides 8 ma of output drive at -1v. Output diode CR02 is for isolation of "OFF" drivers from an "ON" driver in a daisy-chain connection. The IQA has a switching time of 0.5 usec maximum in either direction. A logical "1" input turns the driver on with the output at -1v. A logical "0" input turns the driver off with the receiver input circuitry determining the "0" line voltage. To avoid ringing from line reflections, the end of the line should be terminated approximately in its characteristic impedance.

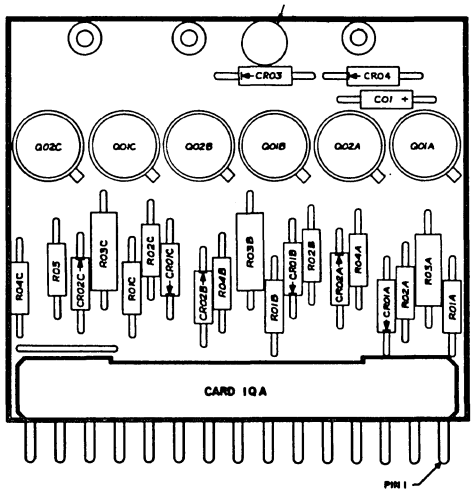
SYMBOL





NOTE:

1. CR01A,B,C ARE 92115021
   CR02A,B,C ARE 92116002
   CR03, CR04 ARE 92115023
2. COMPONENT ASSY. NO. 50020000.



OUTPUT AMPLIFIER
ISC

The ISC output amplifier card, initially designed for 601 tape transports and controllers operating on a time-shared line, is used to interface from standard logic signals (-½ to -3v) to line signals of 0 to +2v. The external load impedance determines the positive output excursion (for example 60 ohm = +2v, 100 ohm = +3v). It is designed as part of an overall line transmission system in which considerations of cable type, cable length, terminations, crosstalk, paralleling of output and input amplifiers, simplicity of biasing voltages, and speed were considered versus overall cost. As such, it has controlled rise and fall time of 0.50 ± 0.15 microseconds.

Circuit operation of each of the three circuits is as follows: With a logical "0" input (-½v), Q01 is turned on and the base of Q02 is almost two volts negative thereby turning off Q02. When the input goes to a "1" (-3v), Q01 turns off and the current through its emitter resistor (R04) is now routed through diodes CR03, CR04, and CR05 to ground. The collector voltage of Q01 starts to go positive. However, as soon as Q02 starts to conduct current to the external load (typically equivalent to 60 ohms to ground), the voltage drop across R06 in the collector circuit of Q02 is coupled back to its base via C01 causing it to act as a Miller integrator in which the output current rises quite linearly over about 0.5 microsecond. The time constant is basically determined by C01 and R03. The end of the current rise ramp is reached as Q02 nears saturation, and output current equals about 34 ma (2 volts across a 60-ohm external load to ground).

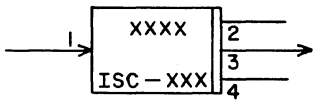
When the input returns to a logical "0", the Miller integrator circuit causes the output current to reduce quite linearly to zero. In this case, the time constant is basically determined by C01 and the divider composed of R03 and R04 which connects between +20v and -20v. Saturation-limiting diodes CR01 and CR02 reduce turnoff time of Q01 and Q02, respectively. Base current in Q01 is limited by the drop across R02. With a logical "0" input, R01 and R02 load the previous logic

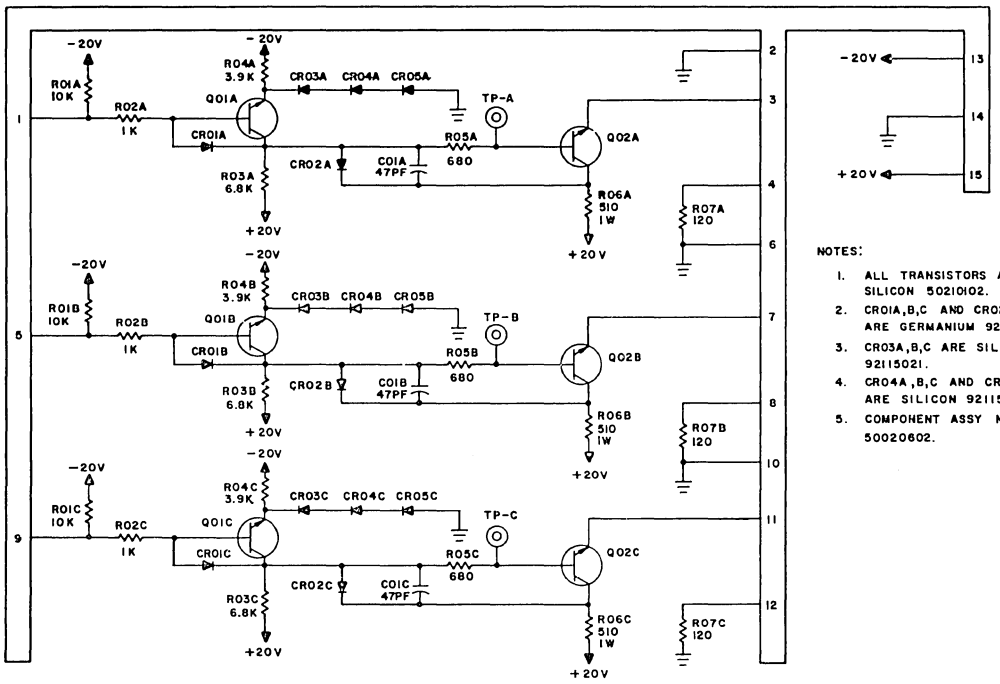
stage about 3 ma. With a logical "1" input, loading of the previous stage is limited to R01 and does not exceed 2 ma.

Line-terminating resistors are available as a jumper option for each circuit. A pin is also available for each circuit as a convenience for grounding one side of a twisted pair of the outer conductor of a coax line.

The following cautions should be observed in application and use. Capacitive loading of test probes on the test point affects the output waveform and should be minimized by using low capacitance probes or eliminated by monitoring the output pin with a card extender in critical timing situations. The current supplied to the load through the internal collector supply resistor (R06) increases power from 0.2w per circuit to nearly 0.8w per circuit when the input switches from a logical "0" to a logical "1". While the silicon transistors used in the circuit are designed to operate at above normal logic card temperature, it is generally advisable to avoid logic card assignments which cause all three circuits of the ISC card to remain continuously in a "1" state.

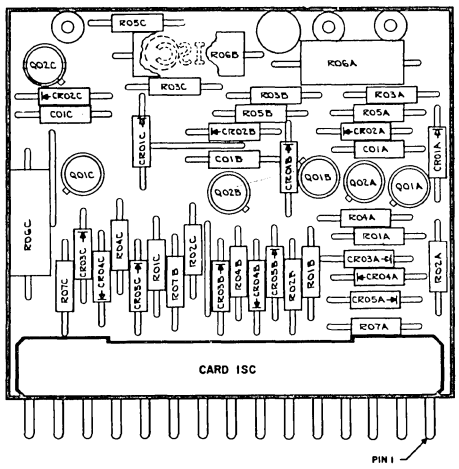
SYMBOL





NOTES:

1. ALL TRANSISTORS ARE SILICON 50210102.
2. CR01A,B,C AND CR02A,B,C ARE GERMANIUM 92116002.
3. CR03A,B,C ARE SILICON 92115021.
4. CR04A,B,C AND CR05A,B,C ARE SILICON 92115019.
5. COMPONENT ASSY NO. 50020602.



OUTPUT AMPLIFIER

ISH

The ISH output amplifier card is specifically designed to interface standard logic signals (-1/2 to -3V) to line line signals of 0 to +3V on a 100 ohm coax cable between a controller and a single peripheral device such as a tape transport, disk file, or display unit. It is not designed for party line operation at this impedance and voltage level since output current capability is only sufficient to drive one line termination and this must be at the receiver end of the line; the transmitter must be at the opposite end. The circuit is designed for minimum rise and fall times, and thus is not generally applicable from crosstalk considerations to non-coax cables where several signals are present in a cable without individual shields. Output drive current is closely equivalent to that of the ISC circuit at two volts or less.

Operation of each of the three circuits on a card is as follows: with a logical "0" input (-1/2V), Q01 turns on and the base of Q02 turns off by about 2/3 volt at which point any excess turn off current drives the output load slightly negative through CR02. The exact value of negative drive is determined by tolerances of R03 and R04 together with the power supplies and will not be less than 1 ma nor more than 4 ma into a 100 ohm load terminated to ground for the power supply conditions described in the following paragraph.

With a logic "1" input (-3V), Q01 turns off and the current through its emitter resistor (R04) is routed through diodes CR03, CR04, and CR05 to ground. This causes the collector of Q01 to go positive, turning on Q02 and back-biasing CR02. Sufficient base drive is available to partially saturate Q02. Zener diode CR01 limits the positive drive at the output emitter of Q02. CR03 also limits the collector voltage swing of Q02 to a very small amount in the off direction decreasing the switching time to a minimum. Output "1" current is not less than 23 ma nor more than 35 ma to termination ranging from 105-116 ohms based on the following power supply conditions:

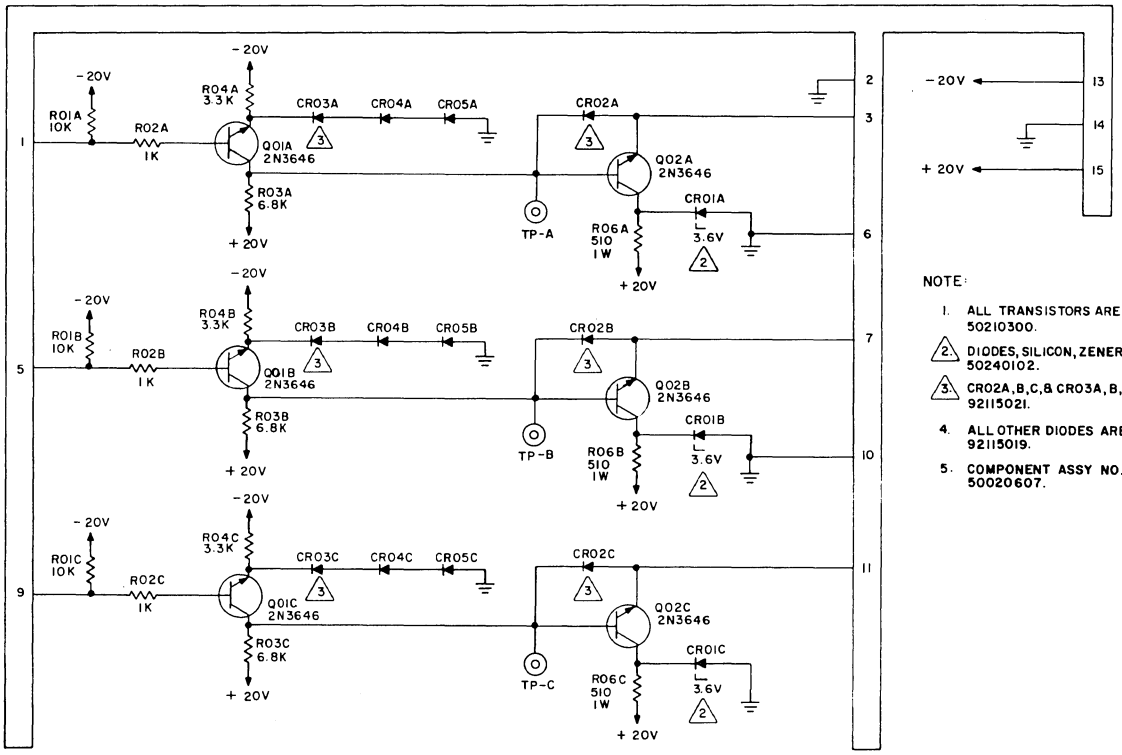
$$+23V > V_{+20v} > +17v$$
$$-23V > V_{-20v} > -17v$$

$$|V_{+20v}| - |V_{-20v}| < 2V$$
$$|V_{-20v}| - |V_{+20v}| < 2V$$

Output rise and fall times (10-90%) into a pure resistive termination of 100 to 120 ohms is 30 nanoseconds or less. Non resistive loads affect the rise-time characteristic or cause ringing of the signal. Test point loading affects the rise and fall times more seriously and should be avoided when speed is a factor. Scopes are requires to monitor accurately the typical 15 nanosecond rise and fall time of this circuit.

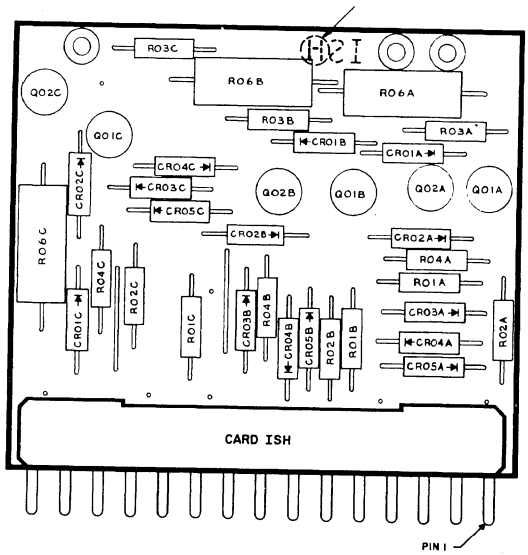
CAUTION

Care should be exercised in using this circuit since it exceeds the maximum dissipation of 2 watts by 1/2 watt under normal conditions (regardless of whether the circuit is conducting or off). Silicon semiconductors are employed to minimize the effect of higher temperature on the circuit, but cooling considerations should be exercised to compensate for the added dissipation.



NOTE:

1. ALL TRANSISTORS ARE SILICON, 50210300.
2. DIODES, SILICON, ZENER 50240102.
3. CR02A,B,C,& CR03A,B,C, ARE SILICON 92115021.
4. ALL OTHER DIODES ARE SILICON 92115019.
5. COMPONENT ASSY NO. 50020607.



PULSE DELAY AND OUTPUT AMPLIFIER
ITA/ITB/ITC

The ITA, ITB, and ITC circuits are functionally interchangeable with the improved ITD circuit. Existing ITA and ITB circuits are retrofittable to ITC and ITD circuits respectively to eliminate tendency toward runt output pulses (by increasing the value of R02) and from delay failure at low temperatures (by changing CR03 from germanium to silicon). The ITA and ITC incorporate a different output circuit associated with Q06 and Q07 than used in the ITB and ITD. While the ITA and ITC test points are less susceptible to capacitive loading of test prods than the ITB and ITD, a greater production yield problem is experienced with uniformity in generating the rising ramp on the ITA and ITC output circuit. The ITB and ITD circuit improve uniformity of the output pulse shape by using a lower storage transistor for Q06 and by adding a resistor in the base of Q07.

The delay portion of the circuit is covered in the UGA description. Additional output circuit and application information are included in the following ITD circuit.

PULSE DELAY AND OUTPUT AMPLIFIER
ITD

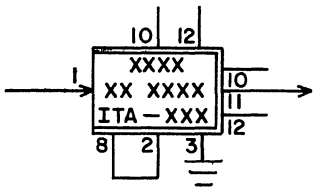
The ITD pulse delay and output amplifier circuit is used for read deskew adjustment in magnetic tape units which interface to a controller with 1 usec digital pulse signals ahead of an accumulation register used to group the bits of each frame of data. Except for the value of R and the line transmitter output, the circuit is the same as the UGA voltage controlled pulse delay. The output circuit is designed to provide an output signal similar to the IS.. series output amplifiers. The output signal is designed to be transmitted on a twisted pair 120-ohm line for receipt by an OS.. series input amplifier. Up to eight ITD outputs may be paralleled for time sharing of a common signal line. Except for the small capacitance of the output emitters, parallel transmitters cause no perceptible loading of the signal on the line. This applies whether parallel circuits have power on or off.

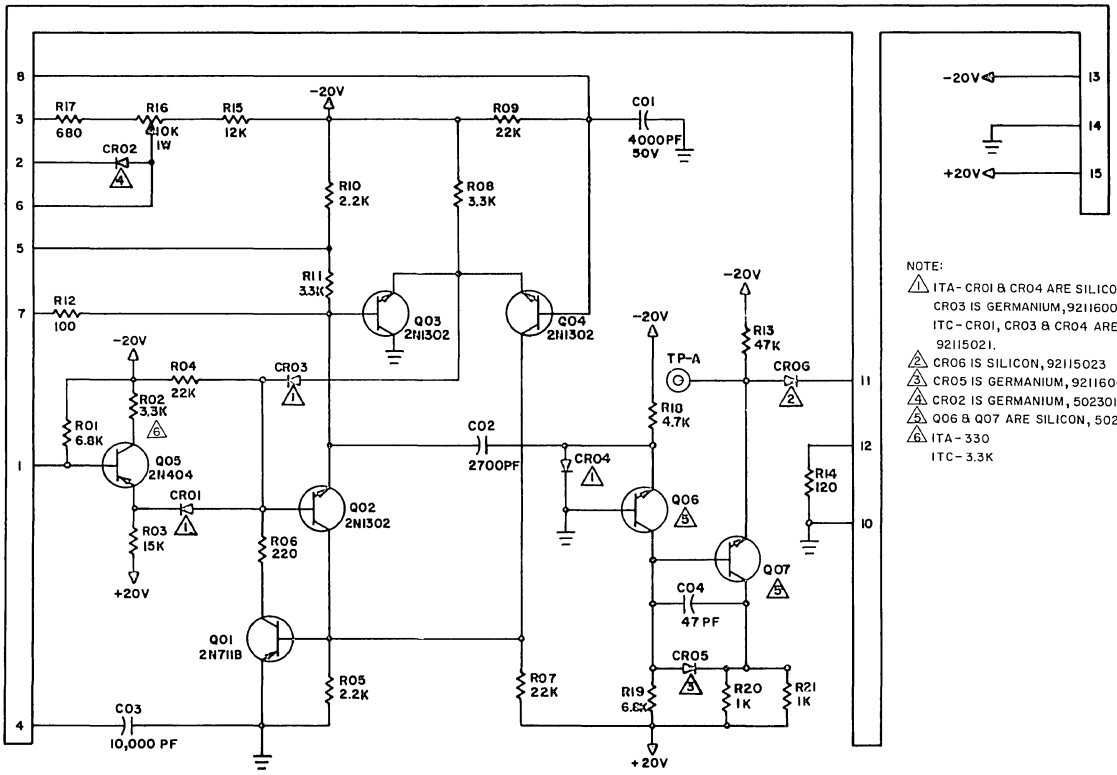
For a description of the delay portion of the circuit, refer to the

description of the UGA circuit. This applies to Q01 through Q05 and their associated components for which reference symbol designations are identical. Thus wiring for pins 1 through 8 does not change between the ITA and UGA when used on the same delay ranges.

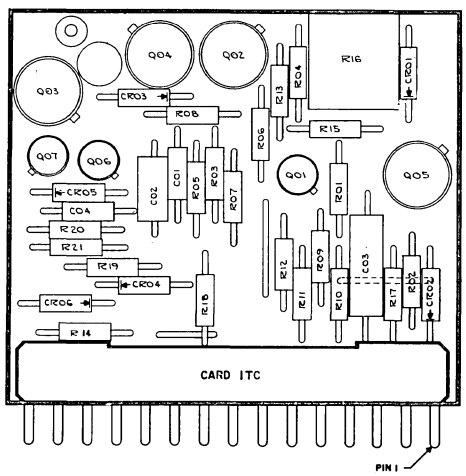
The output circuit consists of Q06 and Q07. The width of the output pulse at the end of the delay period is a function of the time constant of C02 and R18 over a voltage excursion determined by the sum of the forward voltage drops of CR04 and V_{EB} of Q06. This shuts Q06 off for about 1 usec at the end of the delay period. Q07 acts as an output driver with controlled rise (0.5 $\pm$ .15 usec) and fall (0.5 $\pm$ .15 usec) times. It is designed to drive a +2.0v min signal into a 60-ohm load terminated to ground. This is equivalent to a line with 120-ohm characteristic impedance terminated at each end with a 120-ohm load. Rise and fall time of the output drive current are determined by a Miller integrating circuit composed of C04, R19, and R18. The output circuit is compatible with the ISC card, and capacitive loading of test probes on the test point affects the output waveform. This loading should be minimized by using low capacitance probes or eliminated by monitoring the output pin with a card extender in critical timing situations. R14 may be connected as an option to the output when an ITD is used at one end of a line and it is undesirable to use a separate 120-ohm terminating resistor external to the card. The 120-ohm terminating impedance to ground provides the off voltage of 0v. Output pulse width over the recommended delay ranges is 1.0 $\pm$ .3 usec at 16 2/3 ma (60 ohm @ 1v).

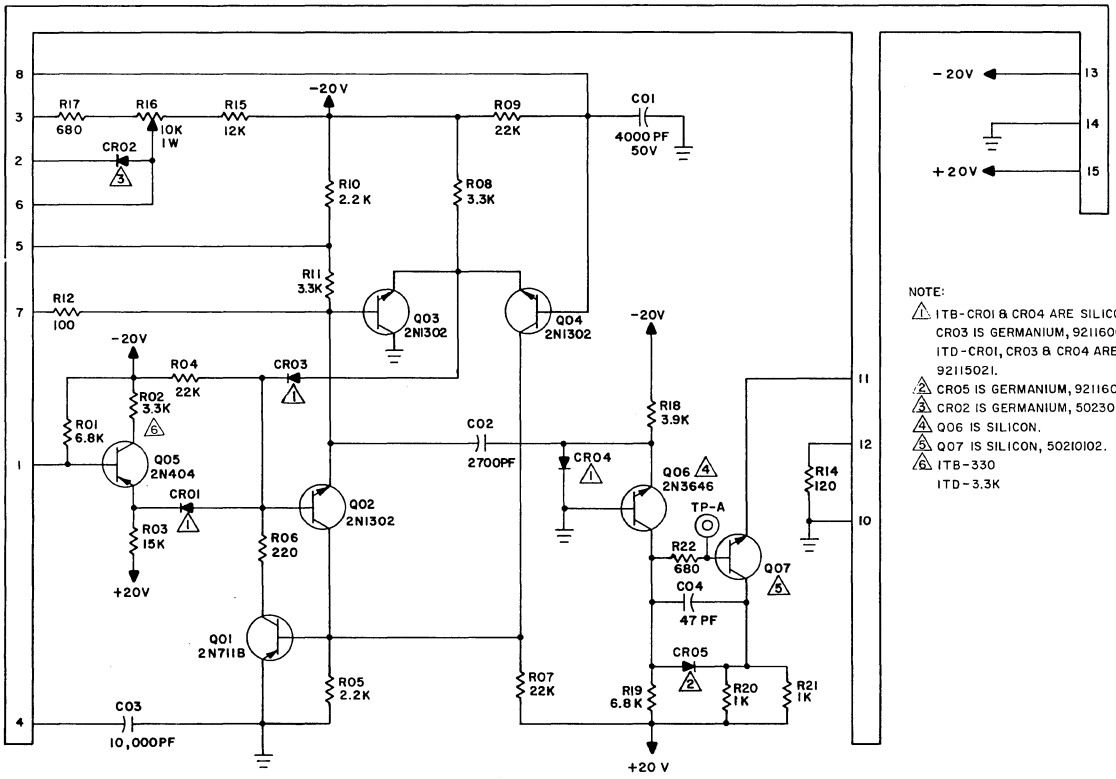
SYMBOL




-20V
+20V
R17 680
R16 10K 1W
R15 12K
R09 22K
C01 4000PF 50V
CR02
R10 2.2K
R08 3.3K
R11 3.3K
R12 100
Q03 2N1302
Q04 2N1302
R04 22K
CR03
R02 3.3K
R01 6.8K
Q05 2N404
CR01
R03 15K
R06 220
Q02 2N1302
Q01 2N711B
R05 2.2K
C03 10,000 PF
C02 2700PF
CR04
TP-A
R13 47K
CR06
R10 4.7K
R14 120
Q06
Q07
C04 47 PF
CR05
R19 6.8K
R20 1K
R21 1K
NOTE:
1 ITA-CR01 & CR04 ARE SILICON, 92115021. CR03 IS GERMANIUM, 92116002. ITC-CR01, CR03 & CR04 ARE SILICON, 92115021.
2 CR06 IS SILICON, 92115023
3 CR05 IS GERMANIUM, 92116002.
4 CR02 IS GERMANIUM, 50230100.
5 Q06 & Q07 ARE SILICON, 50210102.
6 ITA-330 ITC-3.3K

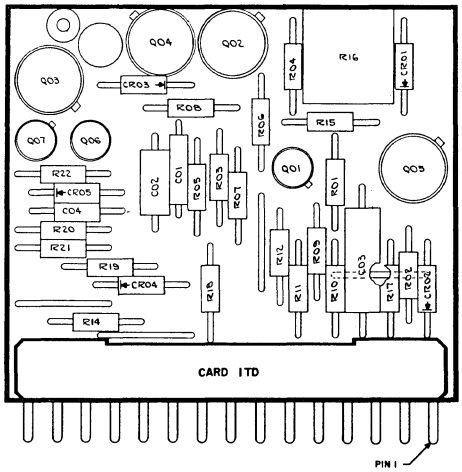
ITA, ITC


CARD ITC
PIN 1



NOTE:

1. ITB-CR01 & CR04 ARE SILICON, 92115021. CR03 IS GERMANIUM, 92116002. ITD-CR01, CR03 & CR04 ARE SILICON, 92115021.
2. CR05 IS GERMANIUM, 92116002.
3. CR02 IS GERMANIUM, 50230100.
4. Q06 IS SILICON.
5. Q07 IS SILICON, 50210102.
6. ITB-330 ITD-3.3K



GATED OSCILLATOR

IVA, IVB, IVC

IVA

This card is a gated oscillator, with adjustable frequency. The oscillator always starts out at the same part of the cycle when the circuit is enabled.

-6V and -12V are generated internally by CR03, CR04, R13, R14 and by CR01, CR02, R10, R11 respectively in order to make the circuit insensitive to machine power supply variations.

When pin 1 is at -3V, Q01 and Q02 are on. This causes Q04 to inject a fixed amount of current into the tank circuit, made up of L01, C03, R21, and R22, and also holds Q03 off, breaking the oscillator feedback loop. Oscillation is thus suppressed.

When pin 1 goes to ground, Q01 and Q02 go off. Energy has been stored in the tank circuit, in the form of current flowing through L01. As Q02 turns off, the voltage at the base of Q04 goes positive, reducing the current flowing from Q04 into the tank. This drives the voltage at the base of Q03 negative, which also tends to make the voltage at the base of Q04 positive. Thus positive feedback is established. As the voltage at the base of Q04 goes positive, the voltage at the emitter of Q03 goes negative. When this voltage swings below -6V, which is applied to one side of the tank and to the base of Q05, Q05 turns on, coupling a negative pulse to the Q06 circuit through C02. The Q06 circuit is an adaptation of a standard 1604 type inverter.

When Q05 comes on, Q03 goes off. This breaks the feedback path, and the current from Q04 into the tank circuit tends toward zero. The voltage at the base of Q03 returns toward -6V. Q05 goes off, and Q03 comes on. This increases the current again from Q04 into the tank circuit, driving the voltage at the base of Q03 more positive, so that positive feedback again exists for the other half of the cycle. Voltage gain of Q03 is less than one, so the positive half-cycle is limited, and the tank circuit subsequently swings back to the negative half-cycle. When Q05 goes off, a positive pulse is coupled through C02 to Q06. The signal at the test point is not quite at a standard logic level; however, passing it through CR07 to a logic circuit makes it into standard logic.

R22 allows frequency tuning over a limited range around 699.527 kHz, the design frequency for 852 Disc Pack use.

IVB

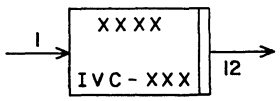
This card is the same as the IVA, except that -6V and -12V are generated by only two zener diodes (CR01 and CR02). Q04 is also changed to a different type of transistor.

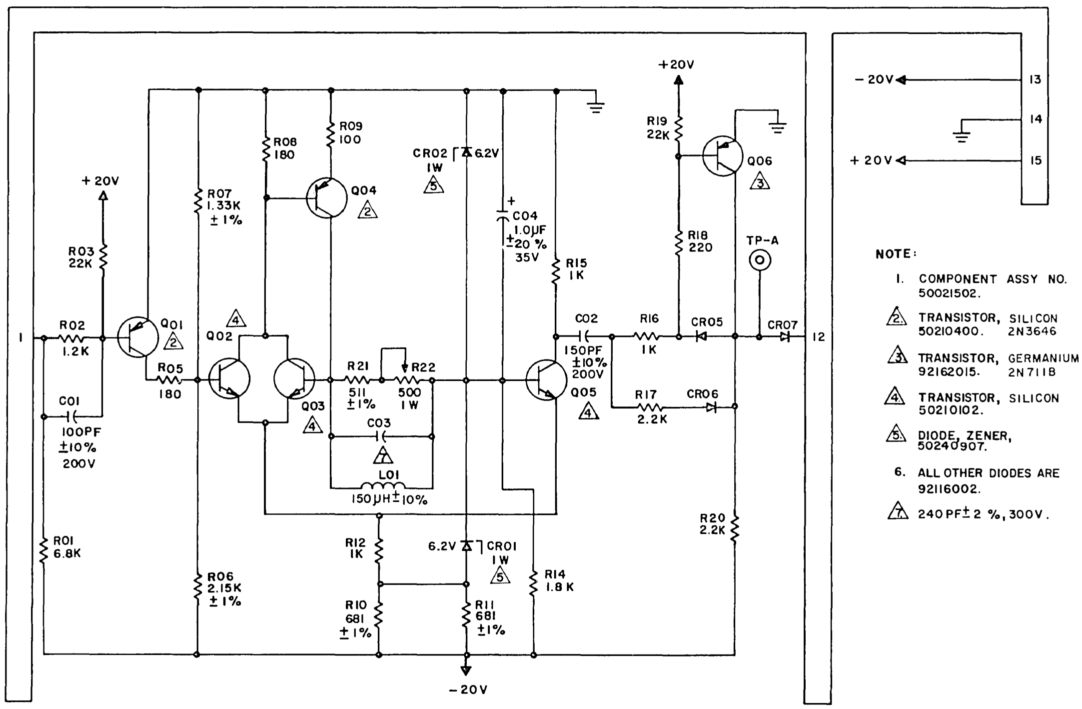
IVC

This card is the same as the IVB, with minor component value changes (Q01 is also changed to a different type of transistor) and R04 is deleted.

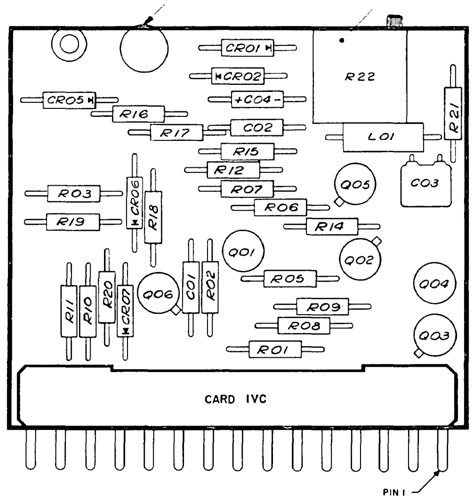
NOTE

The IVA and IVB cards are obsoleted - only the IVC is presently in use.




+20V
R19
22K
Q06
R18
220
TP-A
R03
22K
R02
1.2K
Q01
R05
180
C01
100PF
±10%
200V
R01
6.8K
R07
1.33K
±1%
R06
2.15K
±1%
R08
180
R09
100
Q04
Q02
Q03
R21
511
±1%
R22
500
1W
C03
L01
150μH±10%
R12
1K
R10
681
±1%
R11
681
±1%
CR02
6.2V
1W
CR01
6.2V
1W
C04
1.0μF
±20 %
35V
R15
1K
R14
1.8 K
C02
150PF
±10%
200V
Q05
R16
1K
CR05
R17
2.2K
CR06
CR07
R20
2.2K
-20V
1
12
13
14
15
NOTE:
1. COMPONENT ASSY NO. 50021502.
2 TRANSISTOR, SILICON 50210400. 2N3646
3 TRANSISTOR, GERMANIUM 92162015. 2N711B
4 TRANSISTOR, SILICON 50210102.
5 DIODE, ZENER, 50240907.
6. ALL OTHER DIODES ARE 92116002.
7 240PF±2 %, 300V.

IVC


CR01
CR02
C04
C02
R22
L01
R21
CR05
R16
R17
R15
R12
R07
R06
R14
C03
Q05
R03
R19
CR06
R18
Q01
Q02
Q04
Q03
R05
R09
R08
R01
R11
R10
R20
CR07
Q06
C01
R02
CARD IVC
PIN 1

OUTPUT AMPLIFIER
IYA

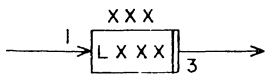
The output amplifier card, IYA, is used to interface between standard logic signals (0v to -3v) and equipment operating from excursions of -12v to -1v. Only one receiver circuit is to be connected to the output amplifier circuit.

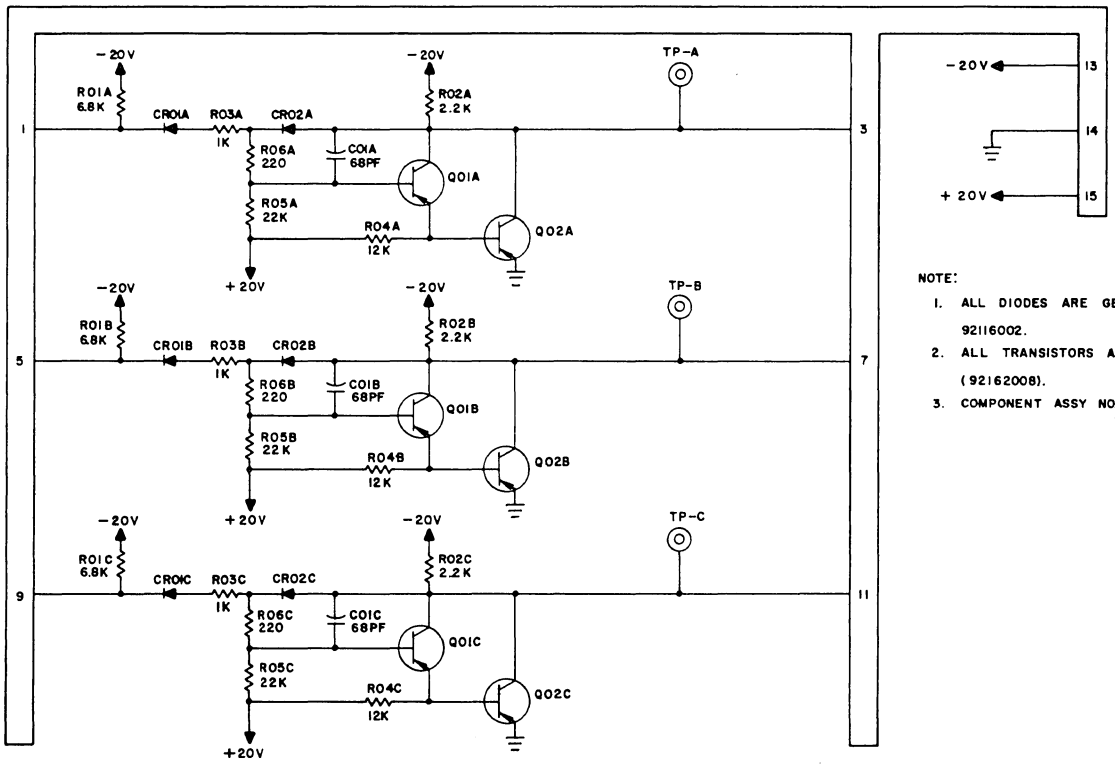
Each IYA card has three identical circuits. The circuit converts a logical "1" (-3v) input to a -0.5v output, and a logical "0" (-0.5v) input to a -14v output when connected to a Beckman receiver and external load resistor.

The IYA circuit is basically a 60 series output amplifier with a different feedback capacitor to modify the output voltage rise and fall times. With a -3v input, forward emitter to base bias for Q02 is provided by voltage divider R01, R03, R06 and R05, and emitter follower Q01. Q02 turns on with a rise time that is controlled by a Miller integrating circuit composed of C01 and the voltage divider. Diode CR02 is used as feedback to the base to prevent Q01 from going into saturation thus minimizing storage time problems. With a "0" input (-0.5v), the divider and Q01 provide a back bias on Q02 emitter-base and Q02 turns off with a fall time controlled by the integrating circuit.

This application called for 60 feet max. twisted-pair output lines to be terminated in a Beckman receiver circuit. An external load resistor of 680 ohms to -20v was added to the circuit to provide the necessary line charging current when Q02 switches off to bring the fall time into the required range. With this arrangement, the IYA switches between the levels of -14v and -0.5v with a rise time of 1.2 usec $\pm$0.6 usec and a fall time (switching from -1v to -10v) of 1.2 usec $\pm$0.6 usec. When turned on, the circuit is required to deliver 10 ma to the receiver.

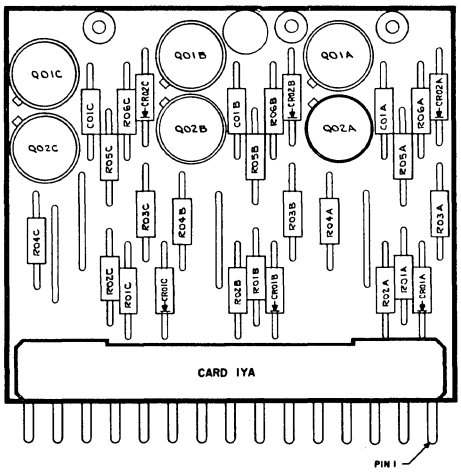
SYMBOL





NOTE:

1. ALL DIODES ARE GERMANIUM 92116002.
2. ALL TRANSISTORS ARE 2N404 (92162008).
3. COMPONENT ASSY NO. 50022400.



SPEED DETECTOR

JAD, JAE, JAF, JAG, JAH, JAI

The JA.. series speed detector circuits are intended as interlocks on disk files and disk storage drives using flying heads. They prevent head loading below a predetermined speed thereby avoiding damaging contact between the recording medium and head. The output of a JA.. series circuit is 0V (ON) or +20V (OFF) signifying that the disk speed is respectively above or below the predetermined speed. This predetermined speed varies with the different card types in the JA.. series and is optimized individually for each product.

The circuit is divided into two parts, each using a similar timing circuit. Input of the first part of the circuit matches 1604 logic levels, output of the first part matches the input of the second part, and the output of the second part of the circuit is intended to drive a relay terminated to +20V.

The first half of the circuit monitors the time, T_i, between input logic "1" pulses by comparing this time to a time standard T_S. The time standard, composed of base circuits associated with differential amplifier Q03 and Q04, generates a positive pulse of width $T_i - T_S$. When T_i is equal or less than T_S, the positive pulse completely disappears. T_S is fixed within limits (±4%) during manufacture by trimming a fixed resistor divider (R10) with a selected value of resistor.

The second half of the circuit uses a timing circuit, Q06 & Q07, similar to the first half of the circuit described above. This circuit is used to sense the presence or absence of positive pulses from the first circuit. The timing period, T_2, of this circuit is not critical to the performance, provided it is always somewhat longer than T_S. T_2 determines the time required for the output to switch ON after receipt of the last positive pulse from the first half of the circuit. If the output is ON, and the first half of the circuit generates a positive pulse, the output returns to OFF in less than 2% of T_2.

The circuit operates as follows:

Initially a logical "1" at pin 1 holds Q01 off and Q02 on, the base of Q03 being clamped to ground through Q02. A logical "0" at Pin 1 initiates the circuit into action by turning on Q01. The base of Q02 is pulled sufficiently negative to turn it off allowing C01 to charge, via R06, toward +20 volts.

In the time standard differential amplifier Q03 is conducting and Q04 is off whenever the voltage at the base of Q03 is less than the voltage at the base of Q04; diodes CR04 and CR05 protect the base emitter junction of Q03 and Q04 and hold base voltages to within one volt of each other. As C01 charges to a voltage equal to the reference divider voltage at the base of Q04, the polarity of the bases of Q03 and Q04 is reversed thus switching the time standard differential amplifier to the state where Q03 is off and Q04 is on. Thus TP-A is driven positive from ground and turns on CR08 in the second part of the circuit.

Reinitiation of a logical "1" at pin 1 again turns Q01 off and Q02 on. This discharges C01 toward ground switching the time standard differential amplifier to the state where Q03 is on and Q04 is off and thus ending the positive pulse at TPA.

If the input frequency is increased slightly (T_i decreased), the time standard differential amplifier is returned to its initial state sooner, thus decreasing the positive pulse width from the time standard. A further increase in input frequency results in C01 being recycled before it attains the voltage necessary to switch the time standard differential amplifier, causing the positive pulse width at TP-A to go to zero.

C01 must be recycled completely to keep the time standard from varying. This is accomplished by Q10 detecting the discharge current through R05. Turning Q02 on starts the discharge of C01. Q10 conducts and pulls the emitter of Q01 from the three diode drop below ground to ground thus holding Q01 off and allowing it to continue discharging through Q02. The circuit returns to the original state when the discharge current of C01 drops below the minimum current which Q10 can detect. In this manner the circuit is made independent of input pulse width and thus the time standard is held constant.

R10 is selected during manufacture to reduce accumulated tolerances of components C01, R06, R08 and R09 in the timing circuit. The differential amplifier Q06 and Q07 in the second part of the circuit operates similar to Q03 and Q04. If positive pulses appears at TP-A, C02 is recycled before it reaches a voltage adequate to switch Q06 and Q07 (Q06 being on and Q07 being off). If the pulses at TP-A disappear, C02 will not be recycled, and will charge to a voltage adequate to switch Q06 off and turn Q07 on. This switches Q08 from a conducting state to an off condition and thus turns Q09 on.

C02 must recycle completely to eliminate output state chatter when T_i approximates T_s. The Silicon controlled rectifier (SCR), CR08, is gated by the time standard output pulse and serves to discharge C02. For gating pulse widths less than the recycle time of C02, the SCR operates as a pulse stretcher which turns off only when the discharge current decays to less than the SCR holding current.

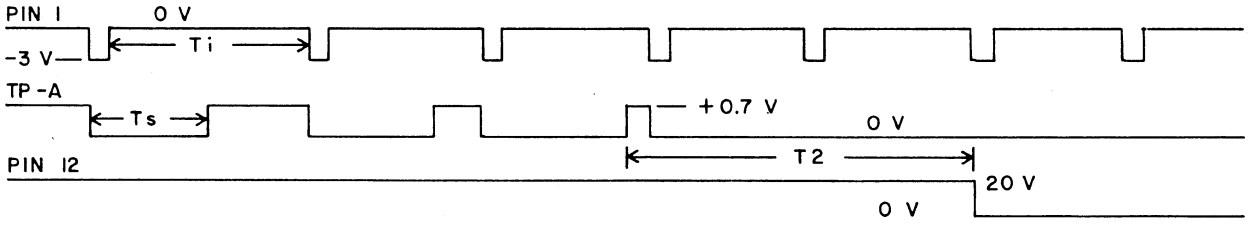
R18 provides a feedback path to help define the minimum pulse width which the SCR detects. This also helps to eliminate output state chatter.

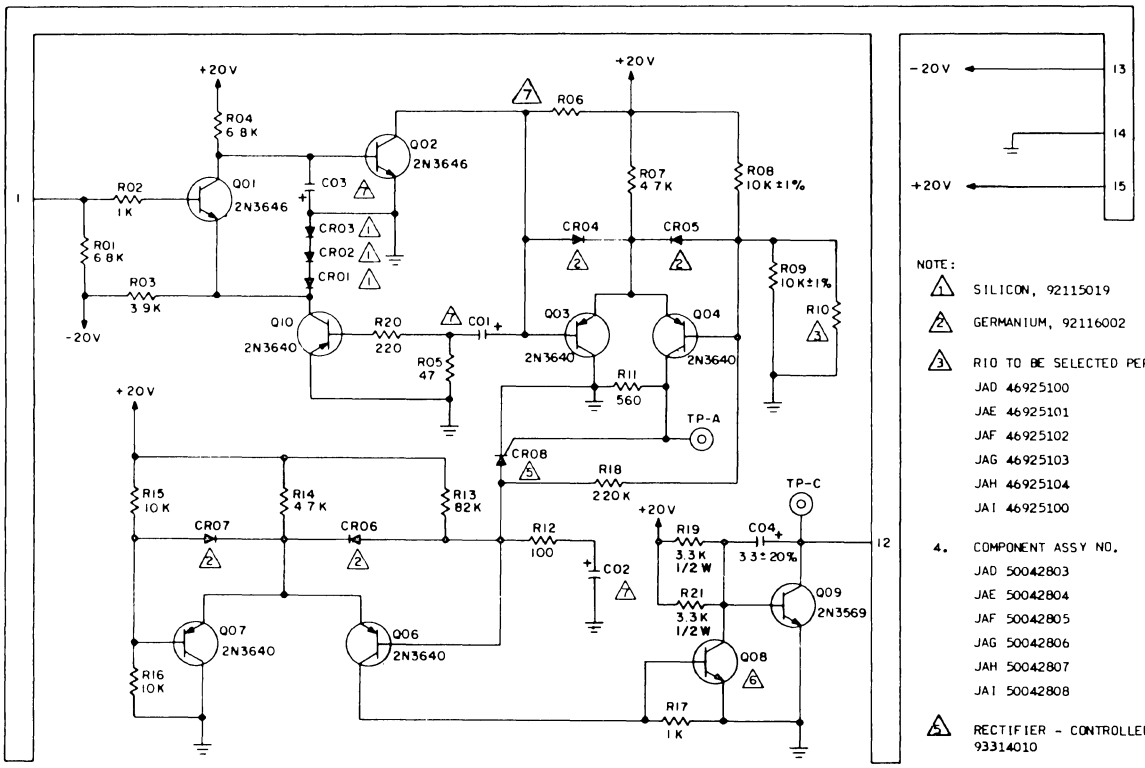
C03 defines the minimum input pulse width which initiates circuit operation.

C04 is provided to eliminate inductive kick back and the need for a suppression diode.

Maximum output current should be no greater than 0.3 amperes.

	JAD	JAE	JAF	JAG	JAH	JAI
Speed in RPM	1000	1200	1900	1900	1200	1500
Input Pulses Per revolution	1	20	20	32	1	1
Input Pulse width-usec	25-150	25-50	25-50	25-50	25-150	25-150
Threshold Period - ms	60	2.5	1.58	0.98	50	40

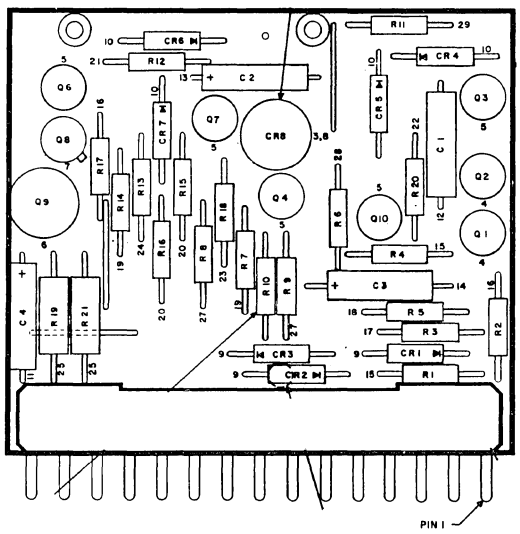




NOTE:

1. SILICON, 92115019
2. GERMANIUM, 92116002
3. R10 TO BE SELECTED PER
   - JAD 46925100
   - JAE 46925101
   - JAF 46925102
   - JAG 46925103
   - JAH 46925104
   - JAI 46925100
4. COMPONENT ASSY NO.
   - JAD 50042803
   - JAE 50042804
   - JAF 50042805
   - JAG 50042806
   - JAH 50042807
   - JAI 50042808
5. RECTIFIER - CONTROLLED SILICON, 93314010
6. NPN SILICON, 50210102
7.

	JAD	JAE	JAF	JAG	JAH	JAI
R06	6.81K	4.64K	2.87K	1.78K	6.19K	5.11K
C01	15.0	1.0	1.0	1.0	15.0	15.0
C02	4.7	0.22	0.1	0.1	4.7	4.7
C03	0.022	0.01	0.01	0.01	0.022	0.022



POSITIVE VOLTAGE REFERENCE SWITCH
JBA

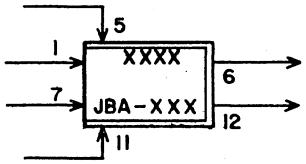
The JBA card is used in the disk file servo actuator coarse control loop. There are two identical circuits per card. Seven circuits are needed to position to each of seven tracks, and an eighth circuit is needed for positioning ±0.020 inches either side of each track. A total of four JBA cards are used per servo.

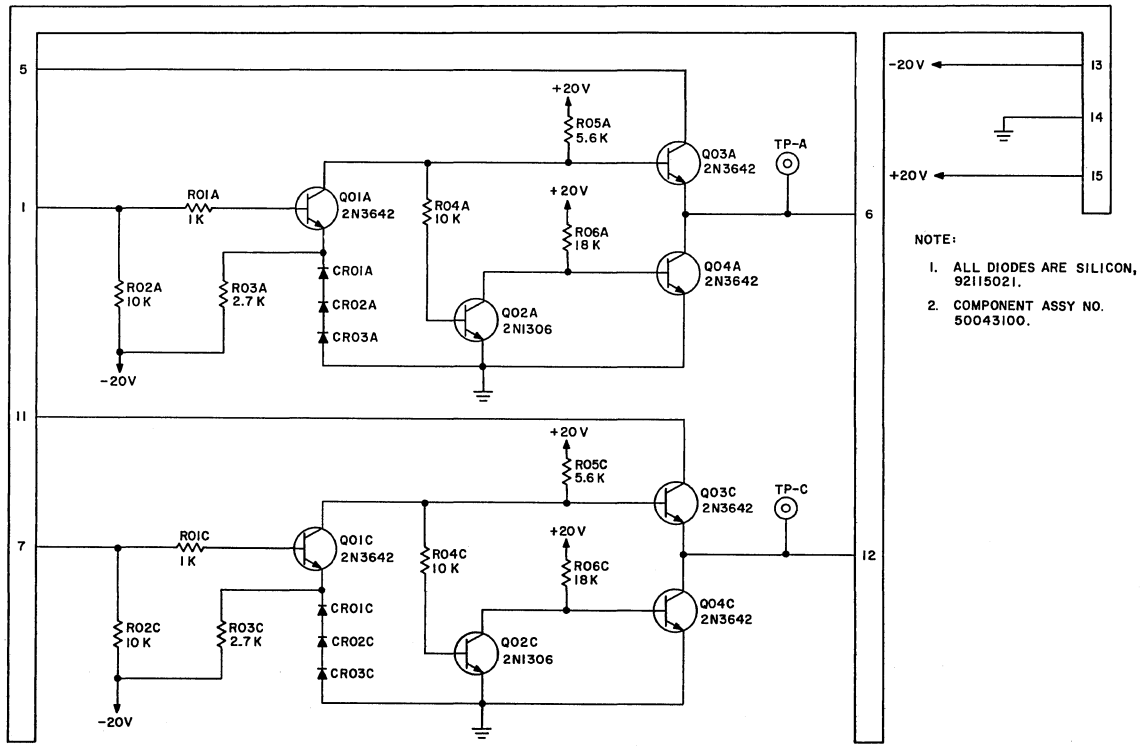
By means of logic signals in, the circuit performs the function of applying a positive 8v reference to an output line, or shorting that line to ground. The 8v is applied to pins 5 and 11, with the output taken from pins 6 and 12.

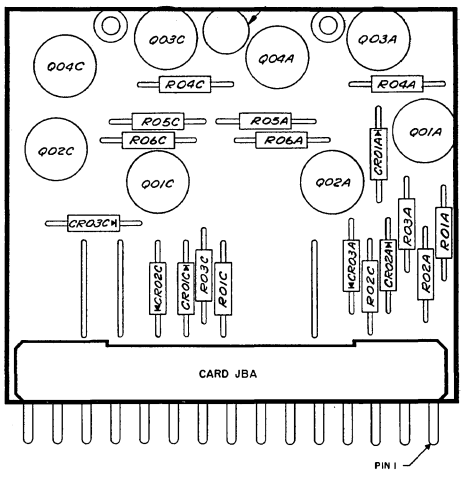
With a logical "1" input at pin 1 (or pin 7), transistor Q01A turns off. Transistor Q02A turns on, causing Q04A to turn off. At the same time, transistor Q03A turns on.

A logical "0" input at pin 1 (or pin 7) will turn Q01A on, holding both Q02A and Q03A off. Since Q02A is off, Q04A will be turned on, shorting the output line to within approximately 15mv of ground. The load current has a maximum value of approximately 1.1 ma.

SYMBOL




5
1
11
7
6
12
-20V
13
14
+20V
15
+20V
R05A
5.6K
Q03A
2N3642
TP-A
R01A
1K
Q01A
2N3642
R04A
10K
+20V
R06A
18K
Q04A
2N3642
R02A
10K
R03A
2.7K
CR01A
CR02A
CR03A
Q02A
2NI306
-20V
+20V
R05C
5.6K
Q03C
2N3642
TP-C
R01C
1K
Q01C
2N3642
R04C
10K
+20V
R06C
18K
Q04C
2N3642
R02C
10K
R03C
2.7K
CR01C
CR02C
CR03C
Q02C
2NI306
-20V
NOTE:
1. ALL DIODES ARE SILICON, 92115021.
2. COMPONENT ASSY NO. 50043100.


Q03C
Q04A
Q03A
Q04C
R04C
R04A
R05C
R06C
R05A
R06A
Q01A
Q02C
Q01C
Q02A
CR01AW
CR03CW
MCR03A
R03A
R01A
MCR02C
CR01CW
R03C
R01C
R02C
CR02AW
R02A
CARD JBA
PIN 1

NEGATIVE VOLTAGE REFERENCE SWITCH
JCA

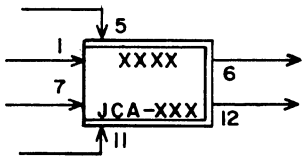
This card is used in the coarse control loop of the disk file servo actuator. There are two identical circuits on each card. Seven circuits are needed to position to each of seven tracks, and an eighth circuit is used for positioning ±0.020 inches either side of each track. A total of four JCA cards are used per servo.

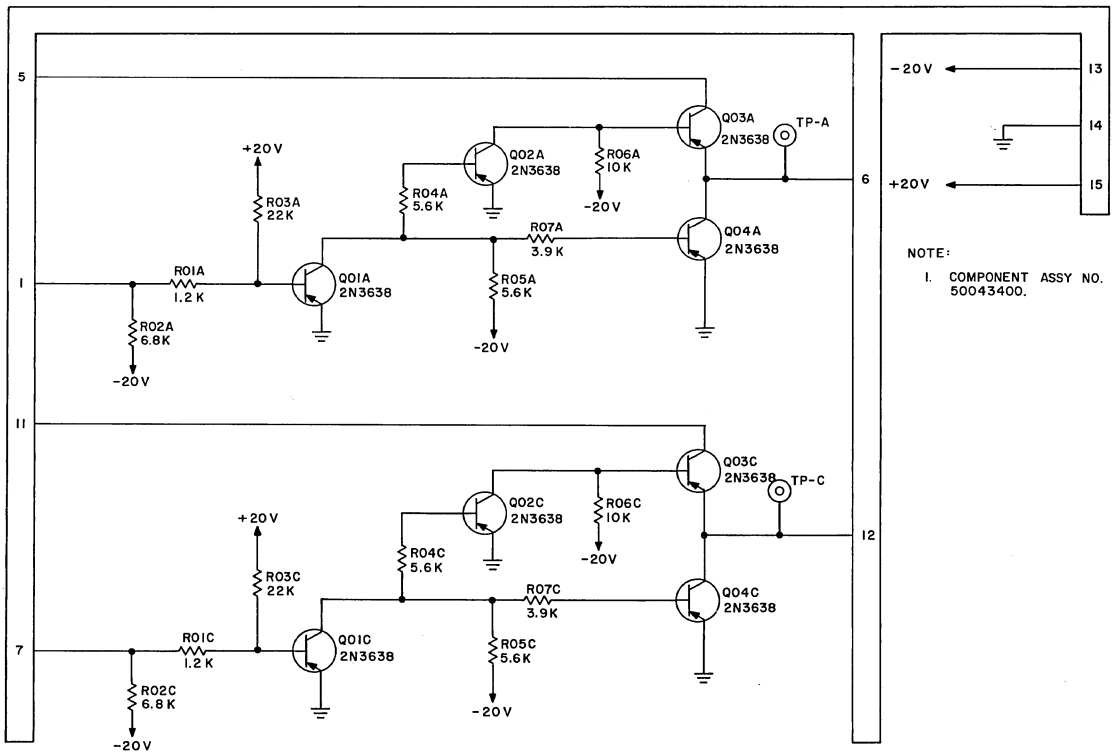
By means of logic signals in at pins 1 and 7, the circuit performs the function of applying a negative 8v reference to an output line, or shorting that line to ground. The -8v is applied to pins 5 and 11, with the output taken from pins 6 and 12.

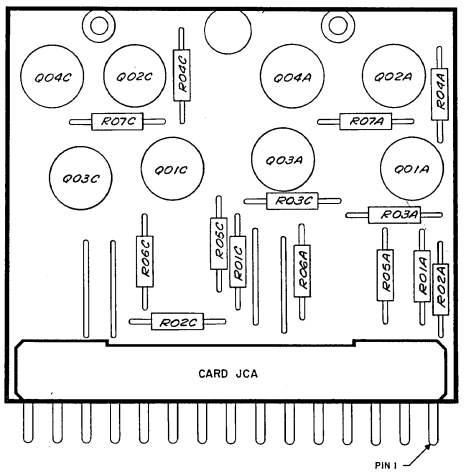
When the input at pin 1 (or pin 7) is at logical "0", Q01A is off, allowing both Q02A and Q04A to be on. Since Q02A is on, Q03A must be off. Therefore, the output line is shorted to within approximately 15mv of ground. With a logical "1" input, Q01A goes on, turning Q02A and Q04A off. This allows Q03A to turn on, thereby connecting the reference voltage to the output line.

The load current supplied by this card is approximately 1.1 ma maximum.

SYMBOL




5
1
11
7
6
12
13
14
15
-20V
+20V
TP-A
TP-C
Q01A 2N3638
Q02A 2N3638
Q03A 2N3638
Q04A 2N3638
Q01C 2N3638
Q02C 2N3638
Q03C 2N3638
Q04C 2N3638
R01A 1.2 K
R02A 6.8K
R03A 22K
R04A 5.6K
R05A 5.6K
R06A 10K
R07A 3.9K
R01C 1.2 K
R02C 6.8 K
R03C 22K
R04C 5.6K
R05C 5.6K
R06C 10K
R07C 3.9K
NOTE:
1. COMPONENT ASSY NO. 50043400.


Q04C
Q02C
R04C
Q04A
Q02A
R04A
R07C
R07A
Q03C
Q01C
Q03A
Q01A
R03C
R03A
R06C
R05C
R01C
R06A
R05A
R01A
R02A
R02C
CARD JCA
PIN 1

LONG STROKE AND SHORT STROKE SWITCH
JDA

The JDA card is used in the disk file servo actuator. The circuit performs the function of removing the short stroke (fine control) signal from the short stroke valve amplifier when the system is in the long stroke (coarse control) mode. It is also used for removing the long stroke signal from the long stroke valve amplifier when the system is in the short stroke mode.

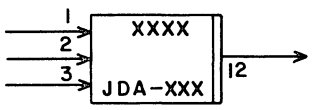
The circuit has three input lines and one output line tied to the collectors of a NPN and PNP transistor. This is done so either polarity of the input signal can be shorted to ground.

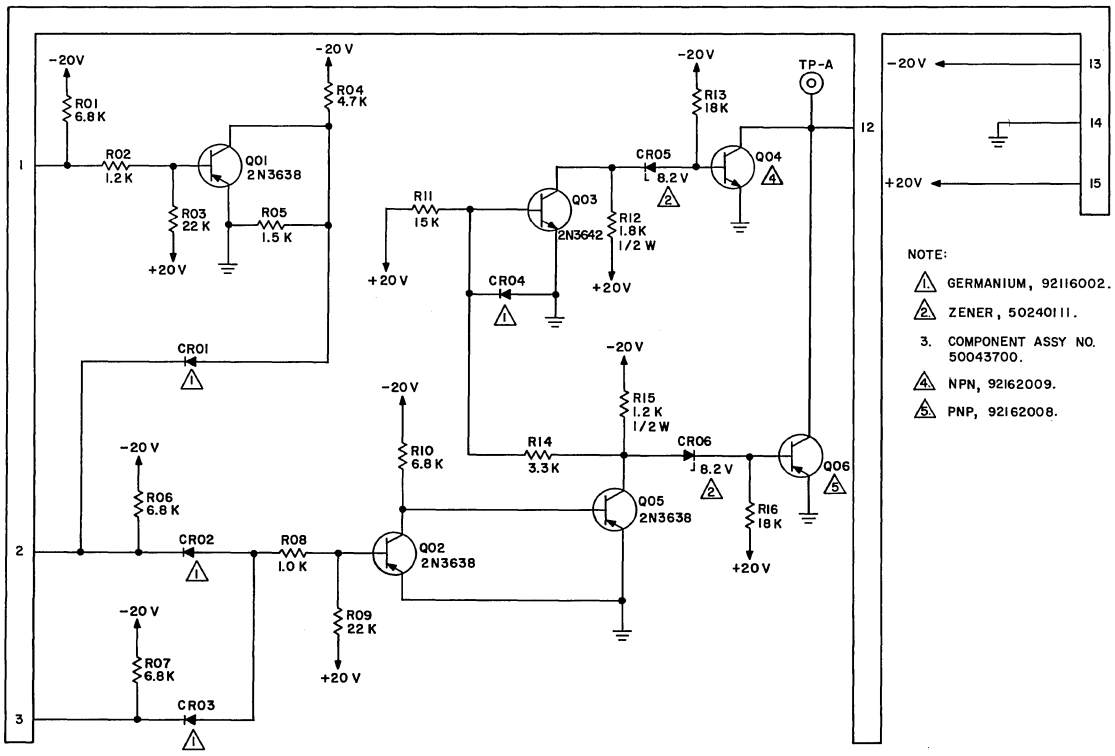
The normal input signals on pins 1, 2, and 3 are -0.5v and -3v (logical "0" and "1" respectively). The output on pin 12 is open or grounded and is defined as logical "0" and "1" respectively. The logic performed by the circuit satisfies the equation: $V_{12} = \overline{V}_1 \cdot V_2 + V_3$, where the subscripts refer to the input and output pins. Thus if pin 3 is a logical "1", the output is also a logical "1" (i.e. grounded). Pin 3 at -3v, regardless of the voltage on pin 2, causes Q02 to turn on. This turns off Q05, allowing Q06 to turn on. Also, Q03 turns off and Q04 turns on. The positive and negative voltages on pin 12 are now grounded (output at logical "1").

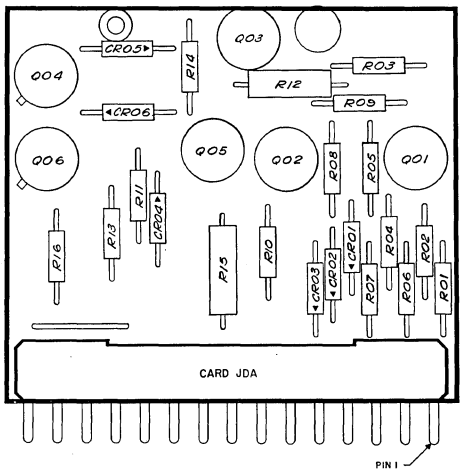
The circuit involving Q01 is an inverter, which is diode coupled to input pin 2. This can be recognized as an AND circuit, since both the collector of Q01 and the voltage at pin 2 must be -3v (logical "1"), before transistor Q02 can turn on. This requires pin 1 to be at "0". The first term of the logic equation is then realized.

This circuit can pass approximately ± 3 ma peak when in the logical "1" state.

SYMBOL




-20V
R01 6.8K
R02 1.2K
Q01 2N3638
R03 22K
+20V
R05 1.5K
-20V
R04 4.7K
R11 15K
+20V
Q03 2N3642
R12 1.8K 1/2W
+20V
CR04
CR05 8.2V
-20V
R13 18K
Q04
TP-A
12
CR01
-20V
R15 1.2K 1/2W
-20V
R10 6.8K
R14 3.3K
CR06 8.2V
Q06
-20V
R06 6.8K
Q05 2N3638
R16 18K
+20V
CR02
R08 1.0K
Q02 2N3638
2
-20V
R09 22K
+20V
R07 6.8K
CR03
3
-20V
13
14
+20V
15
NOTE:
1. GERMANIUM, 92116002.
2. ZENER, 50240111.
3. COMPONENT ASSY NO. 50043700.
4. NPN, 92162009.
5. PNP, 92162008.


CR05
R14
Q03
R03
Q04
R12
R09
CR06
Q06
Q05
Q02
R08
R05
Q01
R11
CR04
R13
R16
R15
R10
CR03
CR02
CR01
R07
R04
R06
R02
R01
CARD JDA
PIN 1

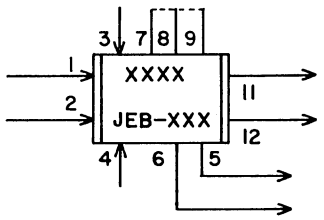
TUNED AMPLIFIER
JEB, JEC

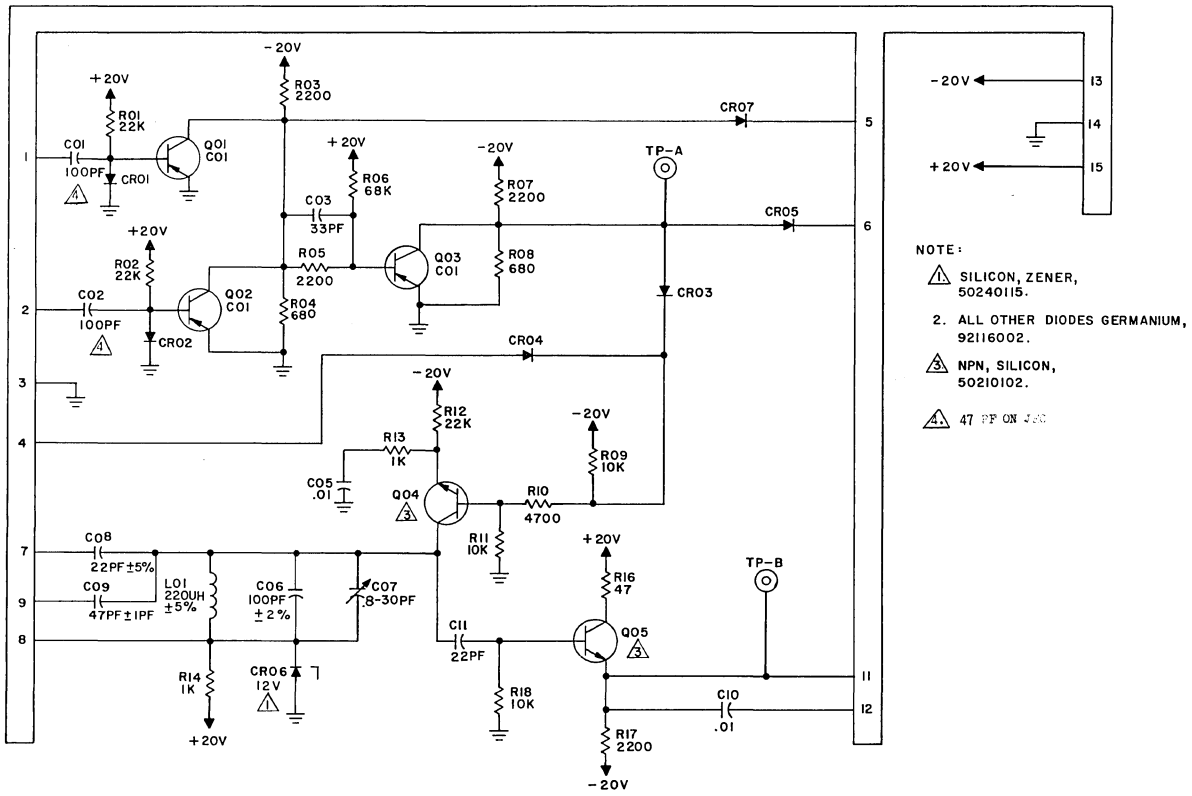
This card is intended for use in the read/write chain in the disk file. Its function is to provide a sine wave output at a basic frequency, which is insensitive to slight variations of input frequency, caused by the effects of peak shifting in the data.

The inputs applied at pins 1 and 2 are complimentary negative square waves derived from the recorded information. These are differentiated by C01, Q01 and C02, Q02. The outputs of Q01 and Q02 are summed across R04 and applied to the base of Q03. The voltage across R04 is therefore a series of positive pulses occurring for each negative going transition on pins 1 and 2.

Amplifier Q03 passes the negative going pulses through the "AND" circuit CR03, CR04, and R09 (assuming pin 4 is negative providing the enable) and then to the under damped tuned collector amplifier Q04. This stage is normally on and is turned off by the incoming negative pulses. This allows the stored energy in the tank inductor to oscillate between L01, C06, C07 and possibly C08 and/or C09 if they are externally connected. The sine wave of voltage across the tank is coupled to the output by the emitter follower Q05.

SYMBOL

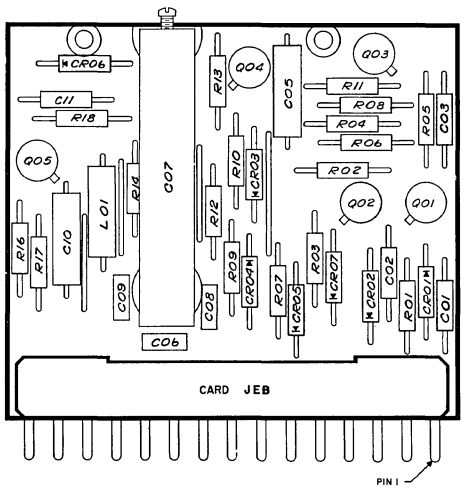




NOTE:

1. SILICON, ZENER, 50240115.
2. ALL OTHER DIODES GERMANIUM, 92116002.
3. NPN, SILICON, 50210102.
4. 47 PF ON J&C

JEB



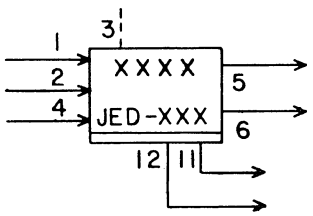
TUNED AMPLIFIER
JED, JEE

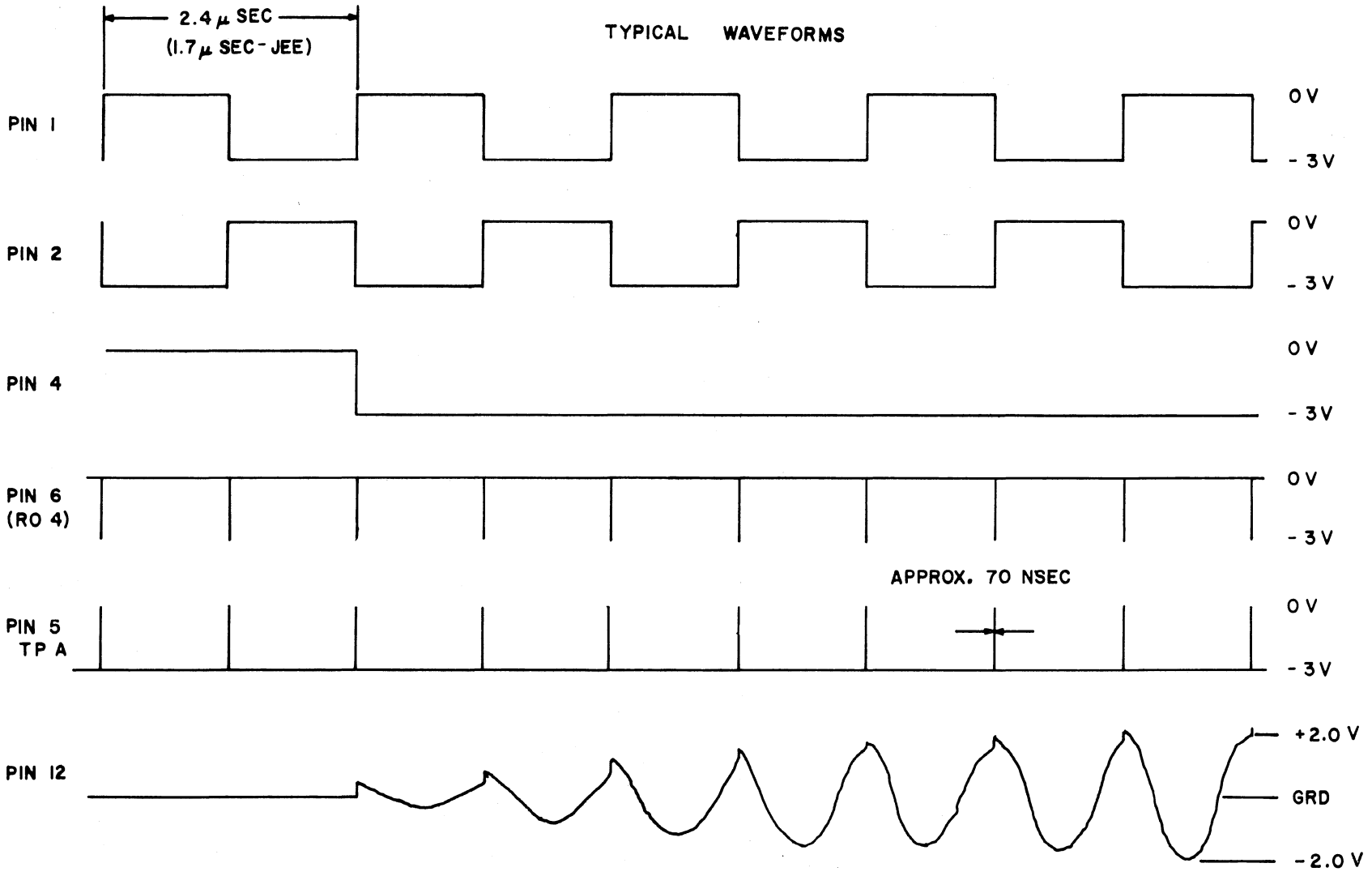
The principal function of the tuned amplifier is to provide an output frequency (sine wave) which is insensitive to slight variations of input frequency caused by peak shifting in the data. It can also be used as a free-running oscillator. The circuitry of each card consists of a differentiating network and a tuned amplifier.

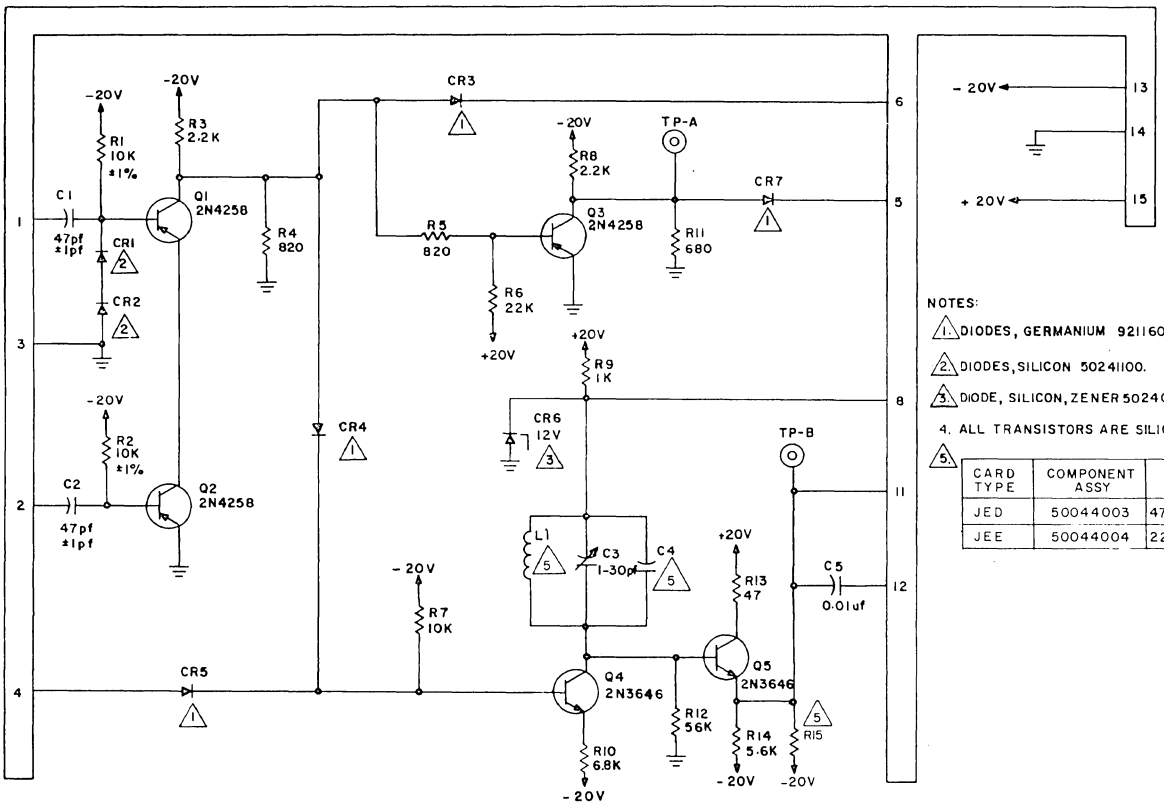
The differentiating network generates a 70-nsec pulse for each transition of the square wave input. These pulses appear at output pins 5 and 6 and are of opposite polarity. The inputs applied at pins 1 and 2 are complementary, negative square waves supplied by a FAB-type card. Each positive transition of these waveforms is differentiated at its respective input by either C1 and R1 or C2 and R2. The differentiated pulses (positive-going) alternately turn off transistors Q1 and Q2 (OR circuits), which generate a negative pulse across R4. This pulse has a duration of 60 nsec (±20) and appears at output pin 6. Diodes CR1 and CR2 prevent C1 from charging when Q2 turns off. Transistor Q3 is an inverting stage which supplies positive-going 70 nsec (±20) pulses at pin 5. Diodes CR4 and CR5 form a gate which is enabled by a "1" on pin 4. The enabling permits a differentiated pulse to reach the tuned amplifier.

The tuned amplifier (ringing circuit) oscillates at a frequency of 847 kHz for the JED, and 1.175 MHz for the JEE. Pulses from the differentiator are fed to the amplifier to maintain oscillation while the gate on pin 4 is enabled. The sinusoidal output to the amplifier is supplied by an emitter follower on pins 11 and 12. Transistor Q4 and the tank circuit of L1, C3, and C4 constitute the tuned amplifier. Capacitor C3 permits tuning of the tank according to the rate of incoming data. Capacitor C4 furnishes additional capacitance for resonating near 847 kHz/1.175 MHz. The negative temperature coefficient of C4 compensates for the positive coefficient of inductor L1.

To operate as a free-running oscillator, the tuned amplifier card is combined with the EWC.



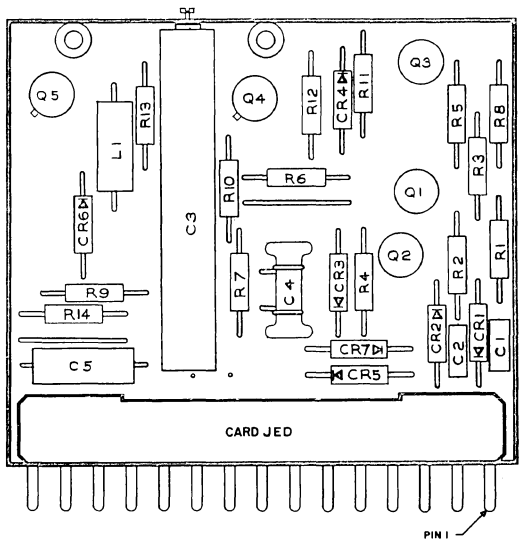

2.4 μ SEC
(1.7 μ SEC - JEE)
TYPICAL WAVEFORMS
PIN 1
0 V
- 3 V
PIN 2
0 V
- 3 V
PIN 4
0 V
- 3 V
PIN 6
(RO 4)
0 V
- 3 V
APPROX. 70 NSEC
PIN 5
TP A
0 V
- 3 V
PIN 12
+2.0 V
GRD
-2.0 V

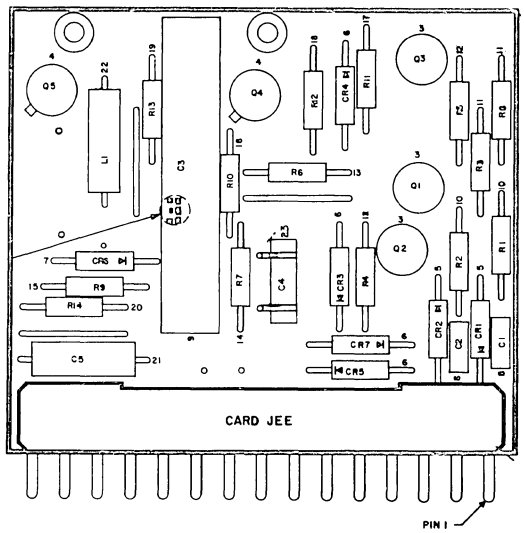


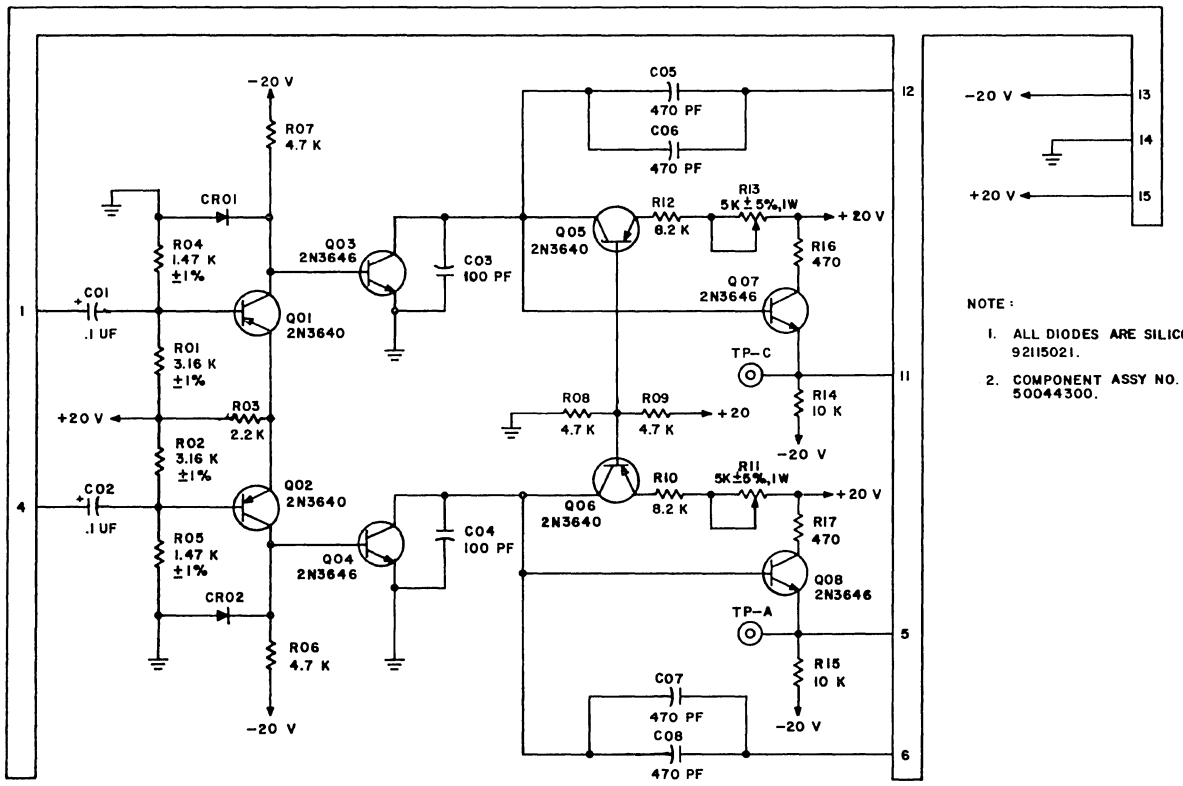
NOTES:

1. DIODES, GERMANIUM 92116002.
2. DIODES, SILICON 50241100.
3. DIODE, SILICON, ZENER 50240115.
4. ALL TRANSISTORS ARE SILICON.
5.

CARD TYPE	COMPONENT ASSY	L1 uh	C4 uuf	R15
JED	50044003	470,10%	47, 5%	OMIT
JEE	50044004	220,10%	60,5%	OMIT

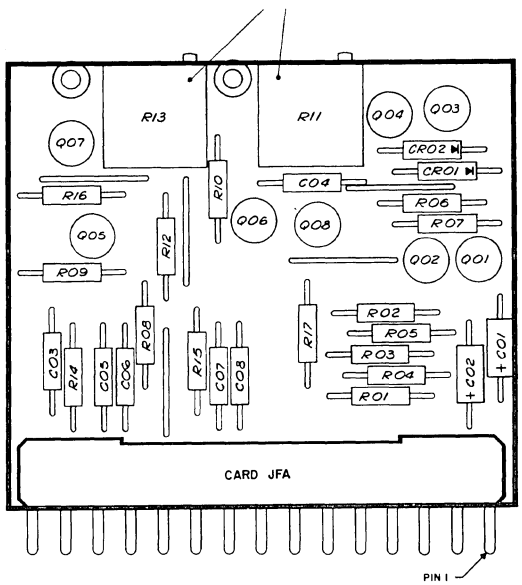






NOTE :

1. ALL DIODES ARE SILICON, 92115021.
2. COMPONENT ASSY NO. 50044300.

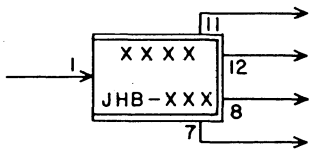


WRITE DRIVER
JHB

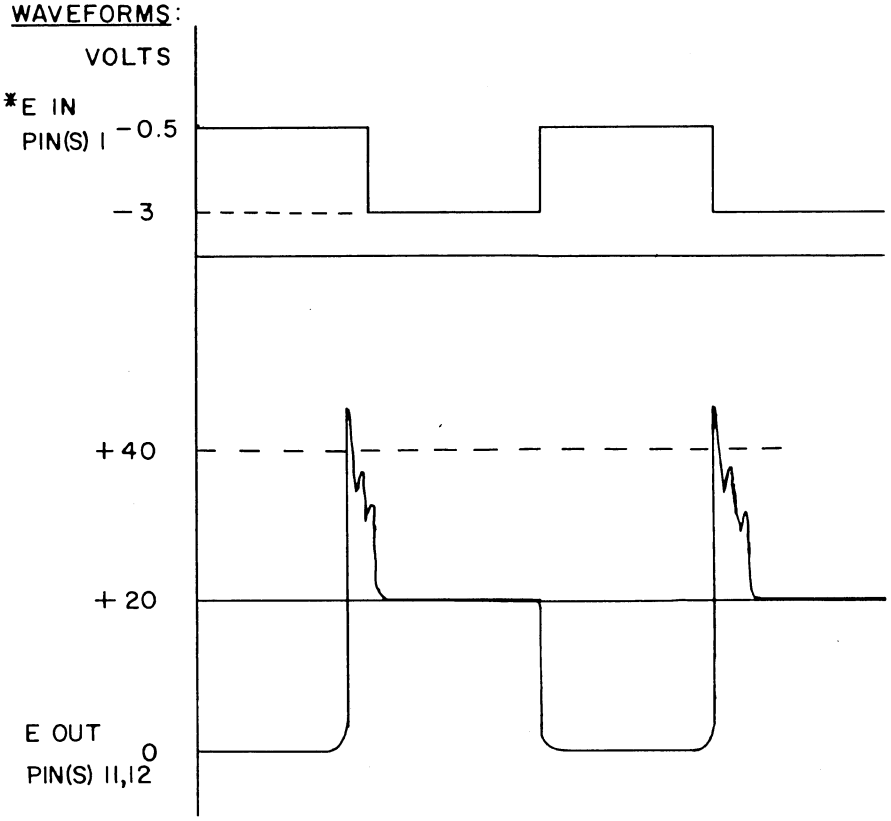
The JHB provides current switching for write and erase heads. It is operated (when driven at pin 1) by a 1604 logic "0" (-0.5v) and logic "1" (-3v) at a repetition rate capability of 240 KHz. The output current capability is 1.8 amperes. A procedure which helps to prevent large current pulses from flowing through the ground wire connections in logic circuits is to connect a load resistor to pins 11 or 12 and to return it to a +20v supply source; in addition, pins 7 or 8 must be connected to the +20v source return and also jumpered to pin 14. Typical values for turn-on and turn-off time are 95 nsec and 171 nsec respectively.

When Q1 is turned on by a logic "0" at pin 1, Q2 turns off and Q3 turns on. The exact opposite occurs when a logic "1" is applied at pin 1, namely, Q2 turns on and Q3 turns off. The parallel arrangement of capacitors and diodes connected to the collectors of Q1 and Q2 serves as a switching speed-up device for transistors Q2 and Q3 by improving the switch-on and storage time performance. Resistors R5 and R9 and diodes CR1 and CR2 form a reverse bias voltage network for Q2 and Q3, allowing only the collector reverse saturation current to flow when these transistors are switched off.

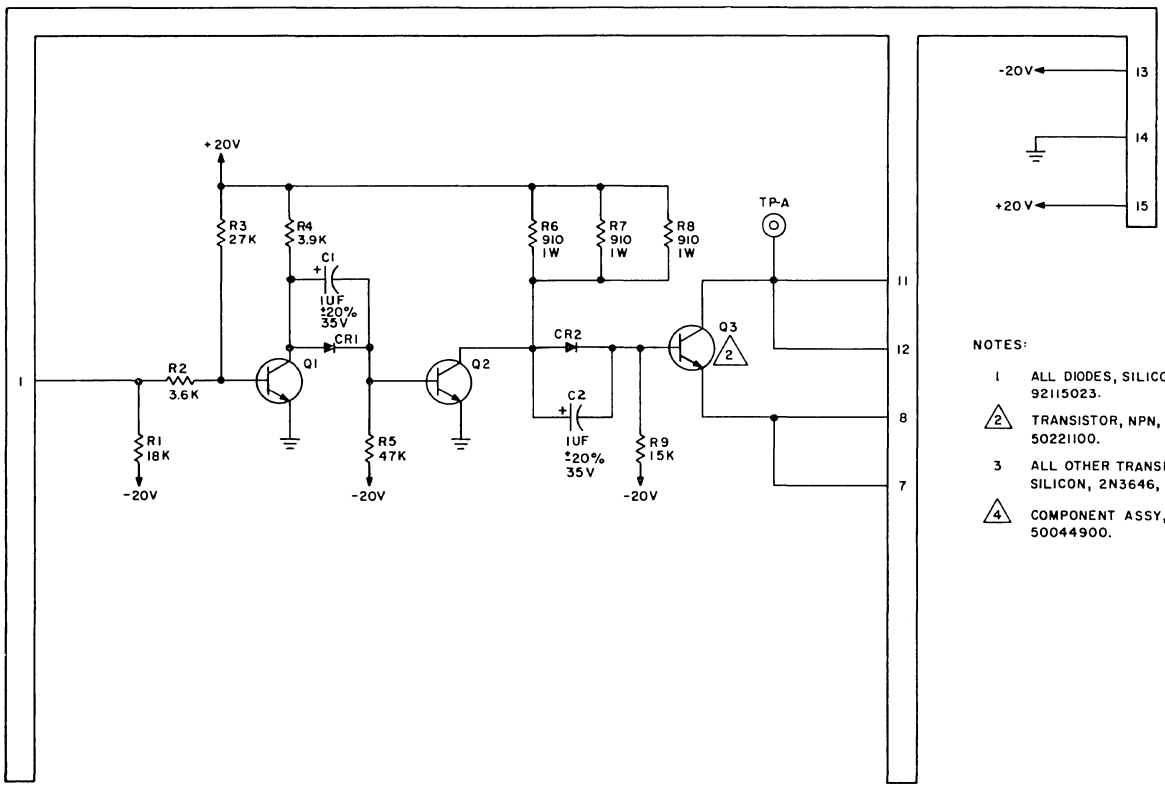
When the JHB is loaded with a fixed composition resistor (7.5 ohms) and is driven with the indicated input signal, the collector voltage swings from a few tenths of a volt and overshoots the supply voltage value considerably as shown in the waveform picture.



TYPICAL
WAVEFORMS:

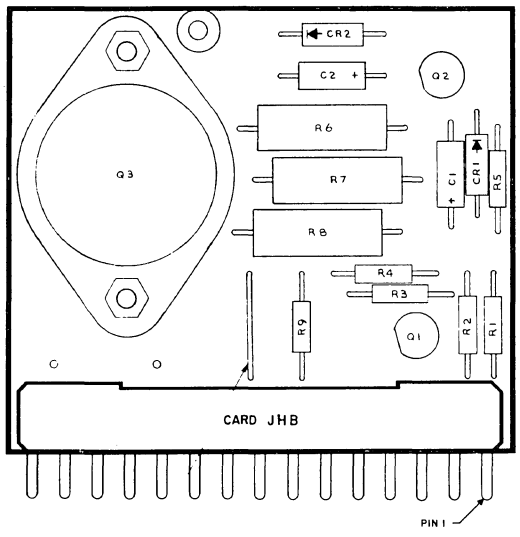


* The load resistor (fixed composition), 7.5 ohms, is connected to pin 11 or 12 and the +20v supply source for the load resistor is turned of when E_{in} is measured.



NOTES:

1. ALL DIODES, SILICON, 92115023.
2. TRANSISTOR, NPN, SILICON, 50221100.
3. ALL OTHER TRANSISTORS, SILICON, 2N3646, 50210300.
4. COMPONENT ASSY, 50044900.



TRANSMITTERS
JJA, JLA

JJA

The JJA card is a single-input, pin-interchangeable, improved-performance replacement for the 121 and P14 transmitter series. The output is compatible with the balanced-line, twisted-pair, transmission lines used extensively in 3000 Series computers, controllers, and peripheral equipment.

The intended application is to interface 1604 Series logic levels (-3v = TRUE, -0.5v = FALSE) with twisted-pair lines suitable for transmission of signals between cabinets up to 100 ft apart. The typical transmission system assumes a party line operation with multiple transmitters/receivers and 112-ohm center-tap terminations to ground at each end to match the characteristic impedance of the twisted-pair line. This represents a nominal load of 28 ohms to ground at each output pin of the transmitter. Back bias (usually incorporated with the terminator at each end) is approximately 10 ma, providing a differential signal of -0.56v at pin 6 (or pin 12) relative to pin 5 (or pin 11). This voltage amplitude on the line represents a FALSE signal. A TRUE signal is represented by a transmitter being ON (-3v input). A worst case minimum transmitter output of 20 ma provides a net differential signal of +0.56v at pin 6 relative to pin 5. Correspondingly, the nominal transmitter drive of 25 ma will provide a differential signal of +0.84v.

GROUND RULES

1. A card with an unused section should have the input/output pins grounded to prevent interaction between the two sections through the common voltage divider. Failure to do so should not cause permanent damage, but it can impair the ability of the circuit to switch properly, thereby greatly reducing its reserve margins.
2. A "1" input (-3v) turns the transmitter ON. A "0" input (-0.5v) turns the transmitter OFF.

3. The JJA circuit allows power bus voltages to be off on paralleled transmitters; however, extreme measures may be required to avoid unwanted signals during the up- or down-cycling of power bus voltages.

4. Transmitter ON drive is 25 ma (±4) over a worst case range of 15 to 25v on both plus and minus power supplies and in any combination. However, an allowance must be made for changes in power dissipation and in the amount of common mode capability as the power voltages vary from a 20-volt nominal level.

5. Propagation time in logic designs must allow for a turn-on time of 28 (±10) nsec and a turn-off time of 34 (±11) nsec measured from the point at which the input crosses -2v to the time that the output current equals 10 ma (the nominal point for 0v differential on an output line). Rise and fall times at the input should be equivalent to those obtained from regular inverters when not driving capacitor loads.

At the input, the circuit employs inverting stage (Q1) followed by a complementary stage (Q2 and Q3) which sinks the current from the plus and minus constant current sources (Q4 and Q5) whenever the input is FALSE (-0.5v). When the input is TRUE (-3v), Q2 and Q3 are OFF and the current from the constant current sources is fed to the output pins through the emitters of the complementary output stage (Q6 and Q7). The voltage divider shared by the two identical circuits provides bias voltages to the constant current sources (VA and VD) and to the output transistors (VB and VC). The complementary current sink (Q2 and Q3) maintains a close phase relationship during turn-on and turn-off by having the emitter of Q2, a NPN transistor, drive the emitter of Q3, a PNP transistor. Resistor R5 is sized to provide base overdrive to Q2 in case the current source (Q5) exceeds the current source (Q4) by up to 3 or 4 ma. As both current sources approach equality, or when Q4 is greater, Q3 receives increasing amounts of base overdrive.

The current source is obtained by negative feedback from a 1% resistor (R7 or R9) in the emitter circuit of each constant current source transistor (Q4 and Q5). Zener diodes (CR5 and CR6) furnish an essentially constant voltage between the emitter resistor return and the bases of Q4 and Q5 over a wide range of power supply variation. Variation in the value of the constant current source is a function of the following four component tolerances:

Zener voltage		(CR5 or CR6)	±5%
Emitter resistors		(R7 or R9)	±1%
VBE @ Ic	25 ma	(Q4 or Q5)	±3-1/4% (±0. 2v)
HFE @ Ic	25 ma	(Q4 or Q5)	±1-3/4%

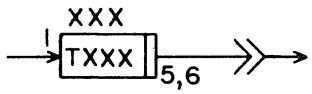
Temperature coefficients of the zener diodes and VBE also have a bearing on the variation.

The output stages are emitter-driven by shutting off the current sink. The bases of Q6 and Q7 are nominally maintained at -5v (V_B) and +5v (V_C), respectively. As a result, output stages are able to maintain the characteristics of a constant current source with a common mode voltage range of ±5v at the output pins. For each 2 1/4v increase or decrease in either the +20v or -20v supply, there is a corresponding 1v increase or decrease in the common mode voltage range. Diodes CR3 and CR4 minimize line loading of transmitters that are logically OFF, with or without power-on.

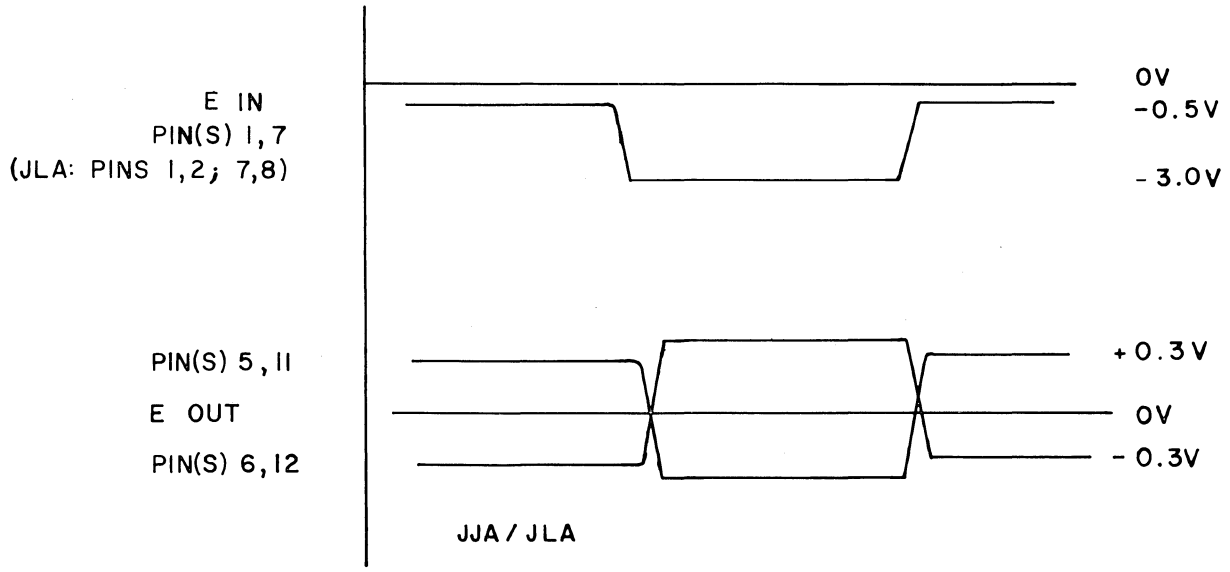
JLA

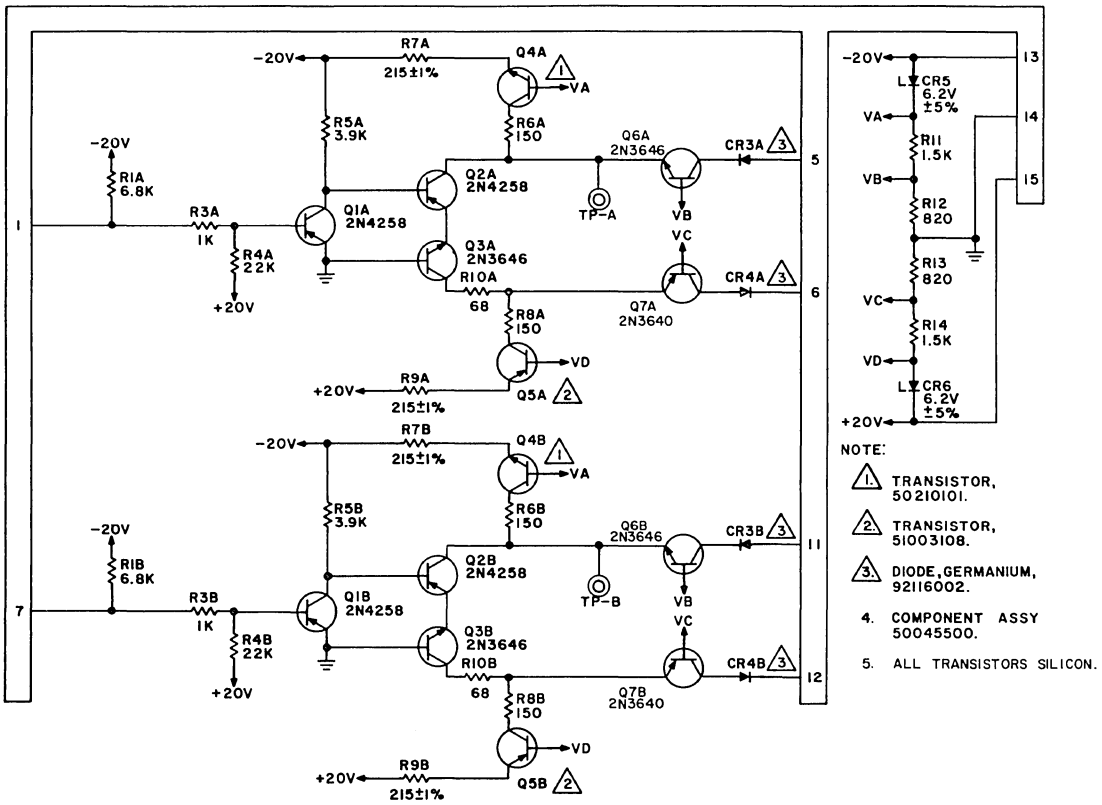
The JLA transmitter is identical in operation to the JJA, but differs functionally in that it has two input OR diodes, CR1 and CR2, plus the presence of R2 as a second input resistor in each of the circuits. The value of R3 is also reduced in the JLA to compensate for the diode drop of either CR1 or CR2.

Typical waveforms are shown below.

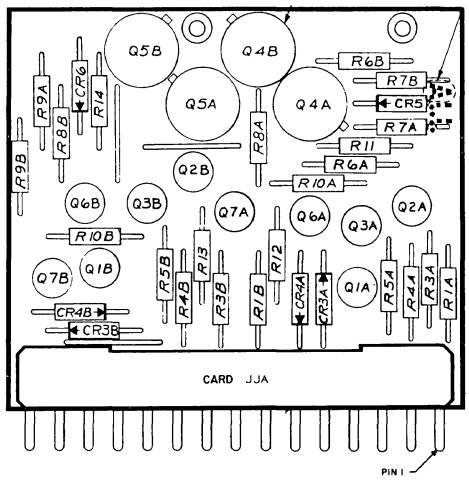


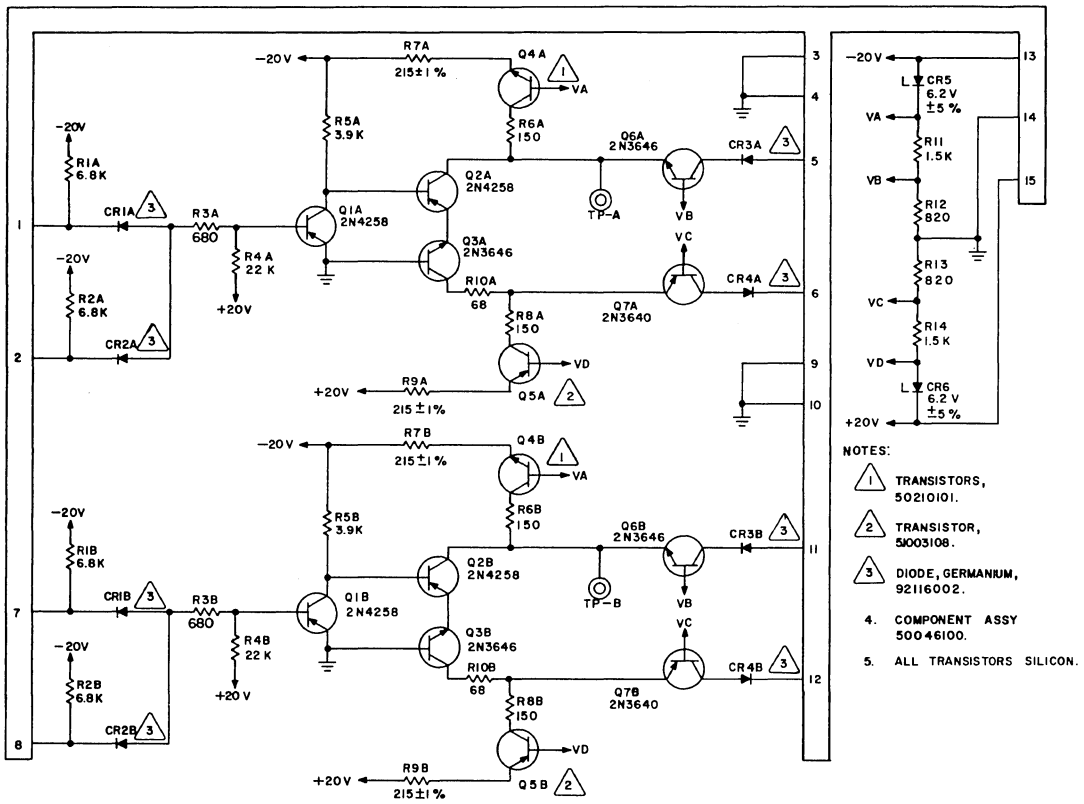
WAVEFORMS:


E IN
PIN(S) 1, 7
(JLA: PINS 1,2; 7,8)
0V
-0.5V
-3.0V
PIN(S) 5, 11
E OUT
PIN(S) 6, 12
+0.3V
0V
-0.3V
JJA / JLA

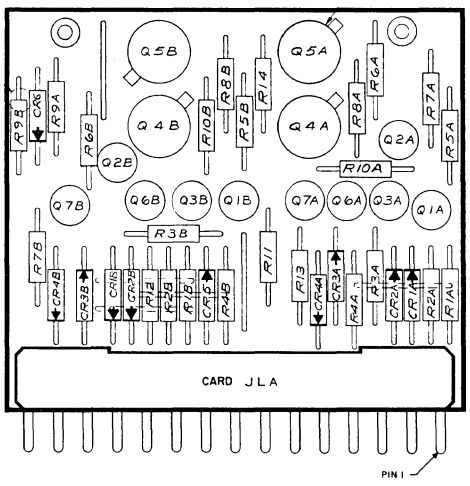

-20V
R7A
215±1%
Q4A
1
VA
R5A
3.9K
R6A
150
Q6A
2N3646
CR3A
3
5
R1A
6.8K
R3A
1K
Q1A
2N4258
Q2A
2N4258
TP-A
VB
VC
Q3A
2N3646
R4A
22K
+20V
R10A
68
CR4A
3
6
R8A
150
Q7A
2N3640
VD
R9A
215±1%
Q5A
2
R7B
Q4B
R5B
3.9K
R6B
150
Q6B
2N3646
CR3B
11
R1B
6.8K
R3B
1K
Q1B
2N4258
Q2B
2N4258
TP-B
Q3B
2N3646
R4B
22K
R10B
68
CR4B
12
R8B
150
Q7B
2N3640
R9B
215±1%
Q5B
7
CR5
6.2V
±5%
R11
1.5K
R12
820
R13
820
R14
1.5K
CR6
6.2V
±5%
13
14
15
NOTE:
1. TRANSISTOR, 50210101.
2. TRANSISTOR, 51003108.
3. DIODE, GERMANIUM, 92116002.
4. COMPONENT ASSY 50045500.
5. ALL TRANSISTORS SILICON.

JJA


Q5B
Q4B
R6B
R7B
CR5
R7A
R11
R6A
R10A
Q5A
Q4A
R8A
R9A
R8B
CR6
R14
R9B
Q2B
Q6B
Q3B
Q7A
Q6A
Q3A
Q2A
R10B
Q7B
Q1B
R5B
R4B
R3B
R13
R12
R1B
CR4A
CR3A
Q1A
R5A
R4A
R3A
R1A
CR4B
CR3B
CARD JJA
PIN 1


-20V
R7A
215±1%
Q4A
VA
R5A
3.9K
R6A
150
Q6A
2N3646
CR3A
R1A
6.8K
Q2A
2N4258
TP-A
VB
VC
CR1A
R3A
680
Q1A
2N4258
Q3A
2N3646
R4A
22 K
+20V
R2A
6.8K
R10A
68
CR4A
Q7A
2N3640
CR2A
R8A
150
VD
R9A
215±1%
Q5A
R7B
Q4B
R5B
3.9K
R6B
150
Q6B
2N3646
CR3B
RIB
6.8K
Q2B
2N4258
TP-B
CRIB
R3B
680
Q1B
2N4258
Q3B
2N3646
R4B
22 K
R2B
6.8K
R10B
68
CR4B
Q7B
2N3640
CR2B
R8B
150
R9B
215±1%
Q5B
CR5
6.2 V
±5 %
R11
1.5K
R12
820
R13
820
R14
1.5K
CR6
6.2 V
±5 %
NOTES:
1. TRANSISTORS, 50210101.
2. TRANSISTOR, 51003108.
3. DIODE, GERMANIUM, 92116002.
4. COMPONENT ASSY 50046100.
5. ALL TRANSISTORS SILICON.

JLA


Q5B
Q5A
Q4B
Q4A
Q2B
Q2A
Q7B
Q6B
Q3B
Q1B
Q7A
Q6A
Q3A
Q1A
R10A
R3B
CARD JLA
PIN 1

CURRENT CONTROLLED LAMP DRIVERS
JOA, JPA

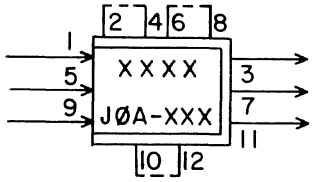
The JOA and JPA provide ground to one or two lamps which are connected to either +20v (JOA) or -20v (JPA) power supplies. With either card driving the intended lamp (P/N 92629003; rated at 24v, 73 ma), a logic "1" (-3.0v) turns the lamp on and a logic "0" (-0.5v) turns the lamp off. Both cards include in their circuitry a constant current source which eliminates turn-on current surges, as well as inverting stages at the inputs for matching the 1604 logic levels. The ordinary maximum load current (60 ma) for these cards can be doubled by paralleling emitter resistors R6 and R7 (jumpering pins 2 & 4, 6 & 8, or 10 & 12).

JOA

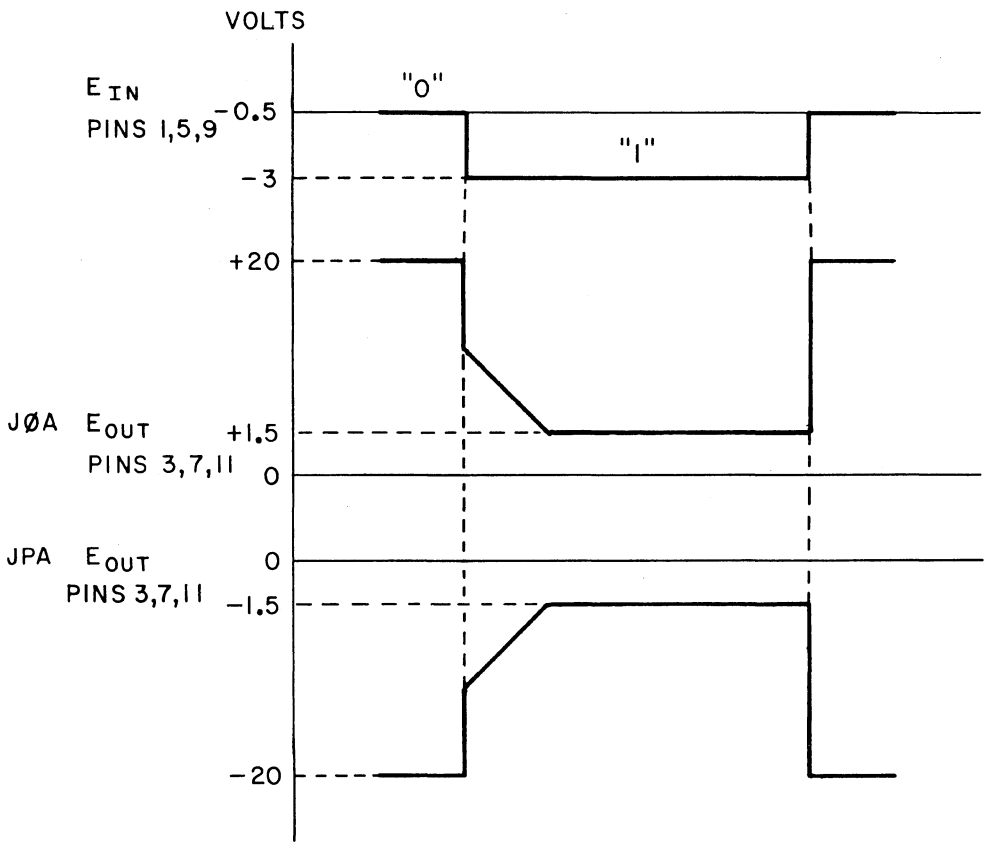
With a "0" at the input (pin 1, 5, or 9), transistor Q1 is off, allowing the Q1 collector to go to a -4v. This back biases the base of Q2 which prevents current from going to the load. When a "1" is at the input, the collector of Q1 goes to ground, putting the 3.3v zener diode in parallel with the 2.7v zener diode. The lower voltage zener determines the voltage at the base of Q2 and with Q2 on, current flows to the load. The lamps are pulled to about +1.5v. Zener diode CR1 couples the input and output stages.

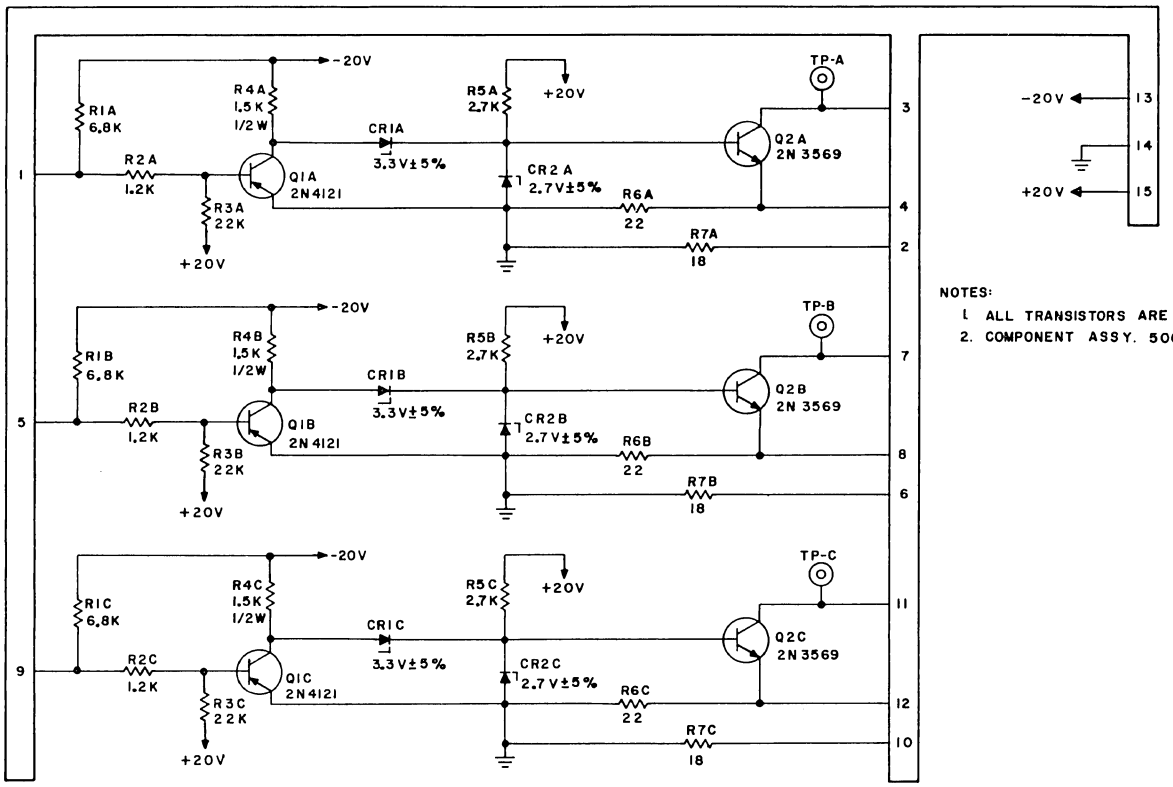
JPA

A "0" at the input (pin 1, 5, or 9) keeps Q1 off and Q2 on, which grounds the base of Q2, preventing the flow of load current. With a "1" at the input, Q1 turns on and Q2 turns off. The zener (CR1) voltage now establishes itself at approximately 2.3v with the current levels being used. Transistor Q3 turns on and about 1.5v appear across the emitter resistor R6 (or R6 and R7). The lamps are pulled to about -1.5v. The coupling circuit between the input inverter and the current source is transistor Q2 with its base to the Q1 collector and its collector to the base of Q3 (output stage).

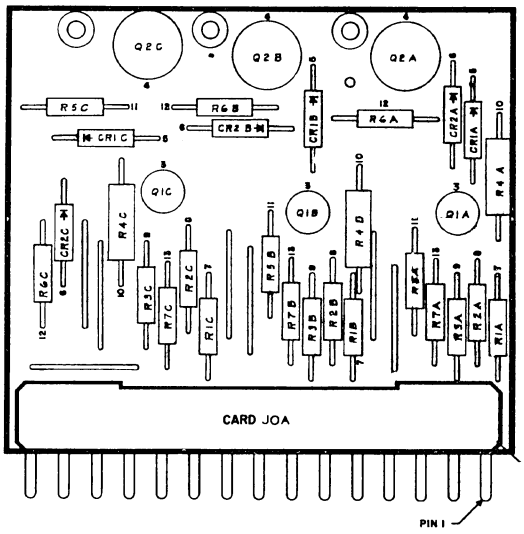

2
4
6
8
1
5
9
XXXX
JØA-XXX
3
7
11
10
12

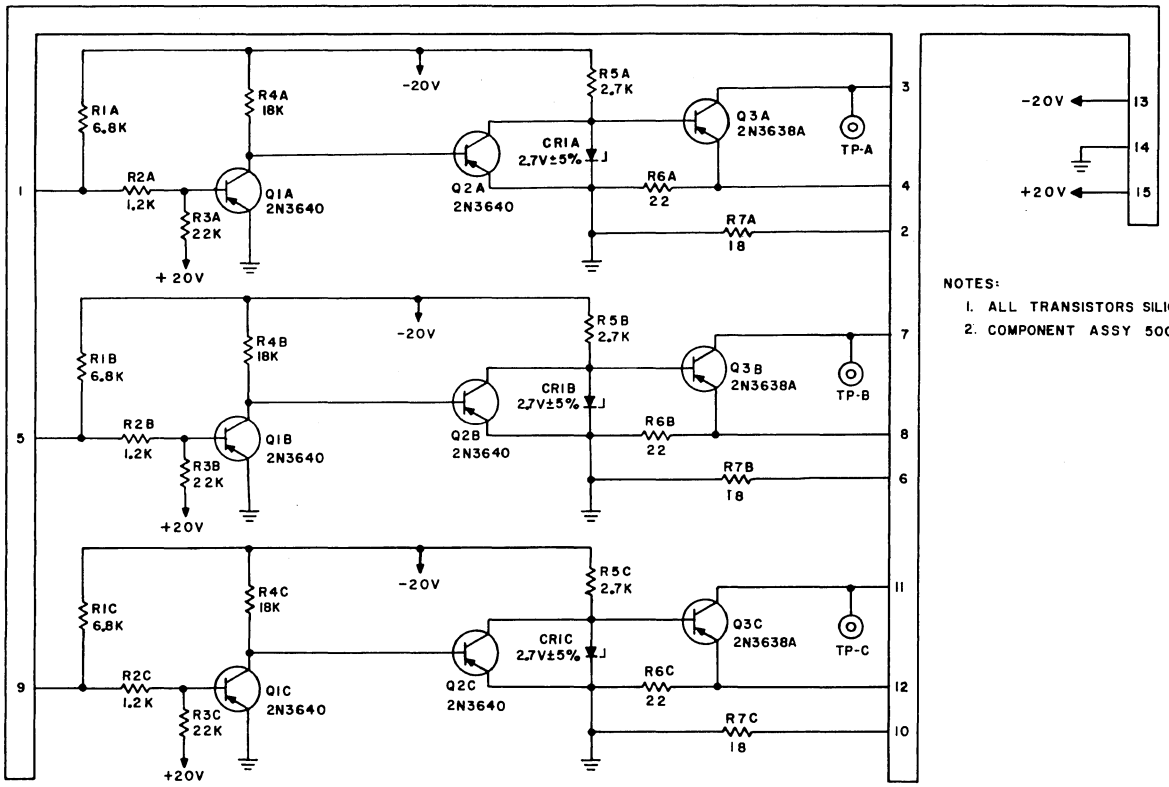
WAVEFORMS:


VOLTS
E IN
PINS 1,5,9
"0"
"1"
-0.5
-3
+20
JØA E OUT
PINS 3,7,11
+1.5
0
JPA E OUT
PINS 3,7,11
0
-1.5
-20


-20V
R1A 6.8K
R4A 1.5K 1/2W
CR1A 3.3V±5%
R5A 2.7K
+20V
TP-A
Q2A 2N 3569
Q1A 2N4121
R2A 1.2K
R3A 22K
CR2A 2.7V±5%
R6A 22
R7A 18
+20V
1
2
3
4
-20V
13
14
+20V
15
NOTES:
1. ALL TRANSISTORS ARE SILICON.
2. COMPONENT ASSY. 50047000.
-20V
R1B 6.8K
R4B 1.5K 1/2W
CR1B 3.3V±5%
R5B 2.7K
+20V
TP-B
Q2B 2N 3569
Q1B 2N4121
R2B 1.2K
R3B 22K
CR2B 2.7V±5%
R6B 22
R7B 18
+20V
5
6
7
8
-20V
R1C 6.8K
R4C 1.5K 1/2W
CR1C 3.3V±5%
R5C 2.7K
+20V
TP-C
Q2C 2N 3569
Q1C 2N4121
R2C 1.2K
R3C 22K
CR2C 2.7V±5%
R6C 22
R7C 18
+20V
9
10
11
12

JOA

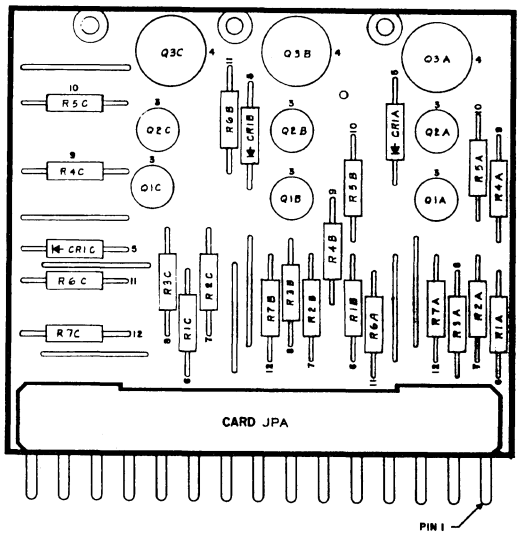

Q2C
Q2B
Q2A
R5C
R6B
R6A
CR1C
CR2B
CR1B
CR2A
CR1A
R4A
Q1C
Q1B
Q1A
R4C
R4B
CR2C
R6C
R3C
R7C
R2C
R1C
R5B
R7B
R3B
R2B
R1B
R6A
R7A
R3A
R2A
R1A
CARD JOA
PIN 1



NOTES:

1. ALL TRANSISTORS SILICON.
2. COMPONENT ASSY 50047300.

JPA



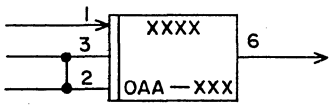
PHOTOCELL AMPLIFIER
OAA

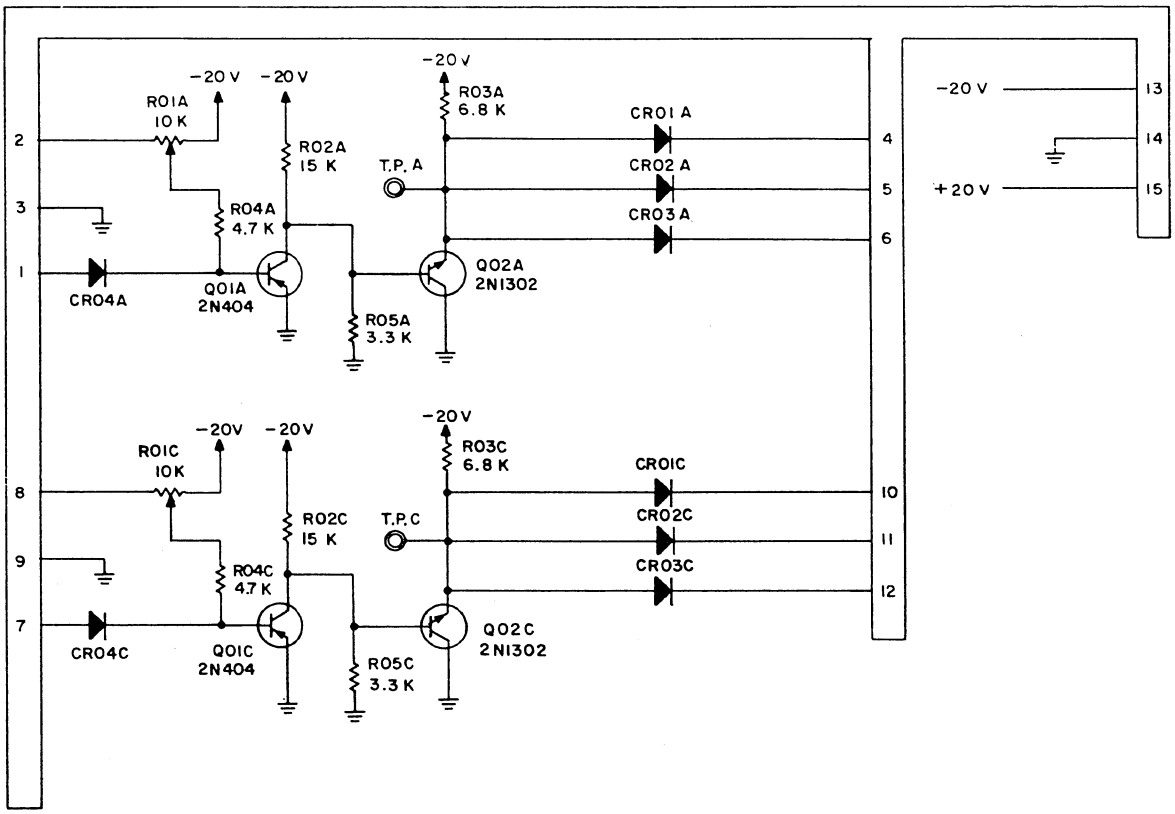
The photocell amplifier receives inputs from silicon solar cells. The output from the amplifier is a "1" when the solar cell is illuminated and a "0" when unlighted. An adjustable potentiometer is provided because of low level signals normally available from the solar cells. This allows optimum centering of the switching point of the amplifier to compensate for the overall photocell excitation, sensitivity, and amplifier tolerances.

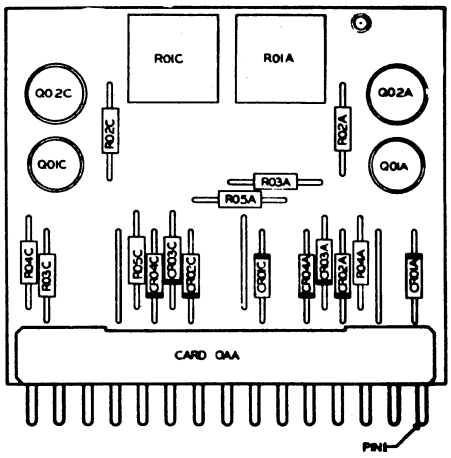
The first stage of the amplifier consists of an inverting amplifier Q01. This transistor is turned on by drive current flowing through R04 from potentiometer R01. Normally pin 2 is jumpered externally to pin 3 to provide R01 with the maximum range of adjustment. The positive terminal of the photocell counteracts the turnon current of R04. Sufficient output from the photocell turns off Q01. CR04 compensates for the change in base to emitter potential of Q01 with changing temperature.

The output of Q01 is directly coupled to Q02 which acts as an emitter follower. The logical "1" excursion at the output is determined primarily by the divider composed of R02 and R05 since the gain of Q02 is sufficient to provide only minor loading of this resistance regardless of the number of outputs actually used. Three diodes (CR01, 02, 03) are provided for ANDing with other logical circuits.

SYMBOL




-20 V
-20 V
-20 V
R01A
10 K
R02A
15 K
R03A
6.8 K
T.P. A
CR01 A
CR02 A
CR03 A
R04A
4.7 K
CR04A
Q01A
2N404
Q02A
2N1302
R05A
3.3 K
-20 V
-20 V
-20 V
R01C
10K
R02C
15 K
R03C
6.8 K
T.P.C
CR01C
CR02C
CR03C
R04C
4.7 K
CR04C
Q01C
2N404
Q02C
2N1302
R05C
3.3 K
-20 V
+20 V
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

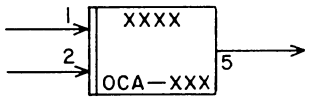

R01C
R01A
Q02C
Q02A
R02C
R02A
Q01C
Q01A
R03A
R05A
R04C
R03C
R05C
CR04C
CR03C
CR02C
CR01C
CR01A
CR02A
CR03A
R04A
CR04A
CARD OAA
PIN1

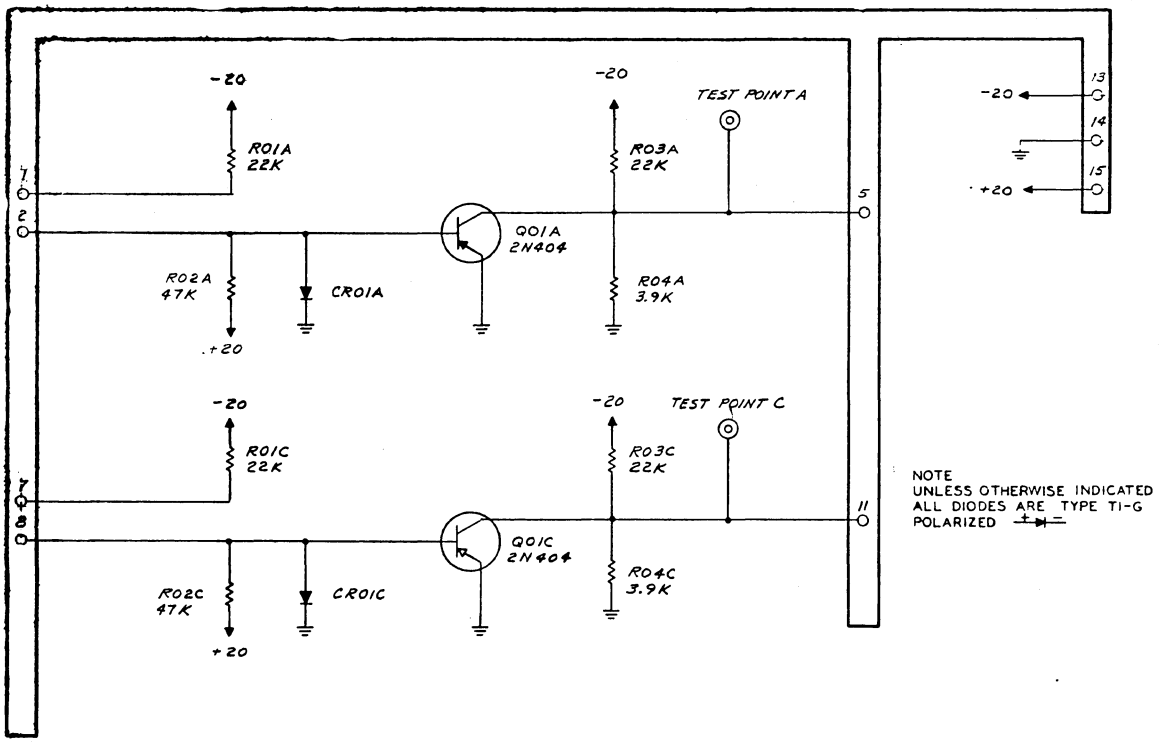
DUAL PHOTOCELL AMPLIFIER

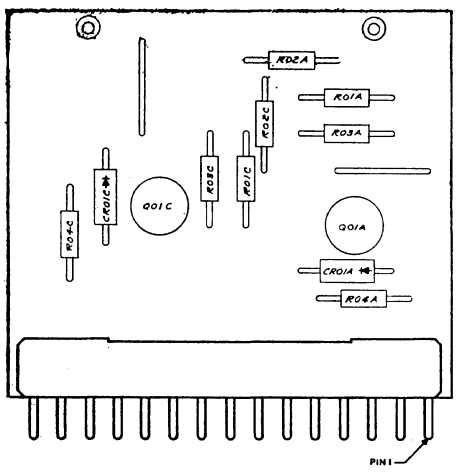
OCA

This photocell amplifier card was designed to work with the photo electric timer circuit of the 180 Data Collector. The input photocell is connected between pins 1 and 2 (or 7 and 8). When its resistance becomes low, Q01 turns on and its output becomes a logic "0" (-1/2v). When the photocell resistance becomes greater than 25K, Q01 turns off and its output becomes a logic "1" (-3v).

SYMBOL




-20
R01A
22K
-20
TEST POINT A
R03A
22K
13
-20
14
15
+20
1
2
Q01A
2N404
5
R02A
47K
CR01A
R04A
3.9K
+20
-20
-20
TEST POINT C
R01C
22K
R03C
22K
7
8
Q01C
2N404
11
R02C
47K
CR01C
R04C
3.9K
+20
NOTE
UNLESS OTHERWISE INDICATED
ALL DIODES ARE TYPE TI-G
POLARIZED


R02A
R01A
R03A
R02C
R01C
R02C
CR01C
R04C
Q01C
Q01A
CR01A
R04A
PIN 1

READ PEAK DETECTOR

ODA

The read peak detector is used with the output of the level detector. The level detector full-wave rectifies a class A signal into positive pulses and passes the portion of the signal which exceeds a predetermined level to the peak detector.

Peak detection is accomplished by first differentiating the rectified class A signal and then detecting the zero crossover point of this differentiated signal.

The first portion of the peak detector circuit consists of the differentiating amplifier (C01, R01, and R02). Because R02 is connected to the output of the high-gain amplifier, the resistance presented to the differentiating capacitor is essentially R02/G where G equals the gain of the amplifier (approximately 1000).

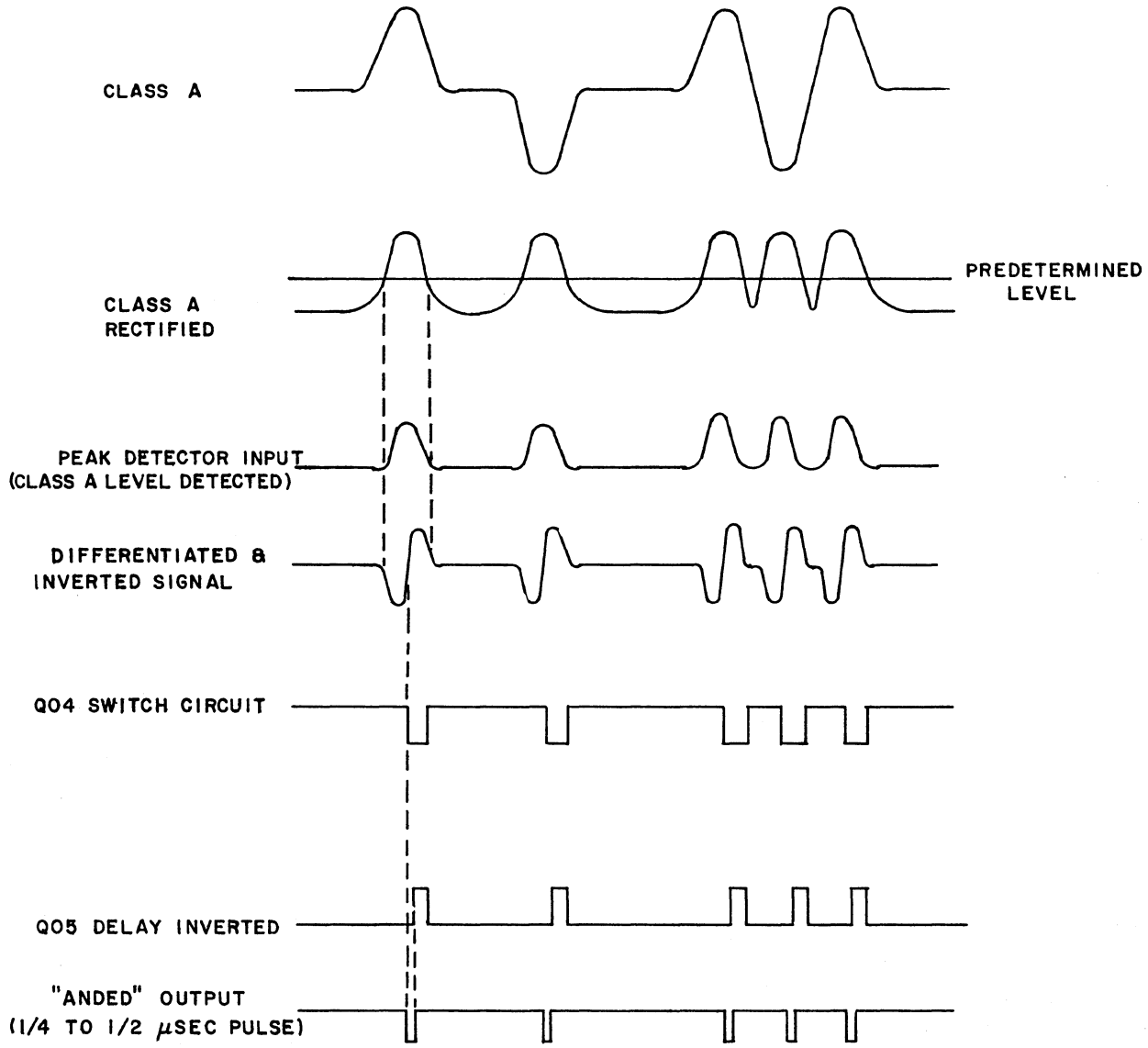
The high-gain amplifier uses three transistors in a single inverting circuit. Q01 is the voltage amplifier; Q02 and Q03 are emitter follower-connected and provide current gain. A positive feedback loop (C04 and R04) returns a signal to the junction of R03 and R04. This signal approaches, but never exceeds, the signal at the collector of Q01. Resistor R03 presents a very high impedance in the collector load of Q01, and increases the a-c voltage gain of Q01 from 100 to 1000. Because the voltage returned to the junction of R03 and R04 is always slightly less than that at the output of Q01, the circuit is free of the usual oscillatory problems associated with positive feedback. The coupling capacitor C04 eliminates d-c positive feedback and thermal drift problems associated with high impedance loads. The d-c (8v) operating point at the output of the amplifier is made stable by the negative feedback divider (R01 and R02).

The differentiated output is coupled by C05 to the zero crossover switching circuit of Q04. R10 normally biases Q04 in the on state. When a signal appears, CR01 prevents Q04 from being overdriven by the differentiated signal which initially swings in the negative direction. When the differentiated signal swings positive and exceeds 0v, CR01 conducts and removes the drive from Q04 causing it to turn off. R09 acts as a load on C05, reducing the effect of nonlinear loading by the switching circuit.

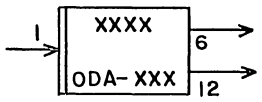
Q05 is used in a simplified version of the normal inverter logic cir-

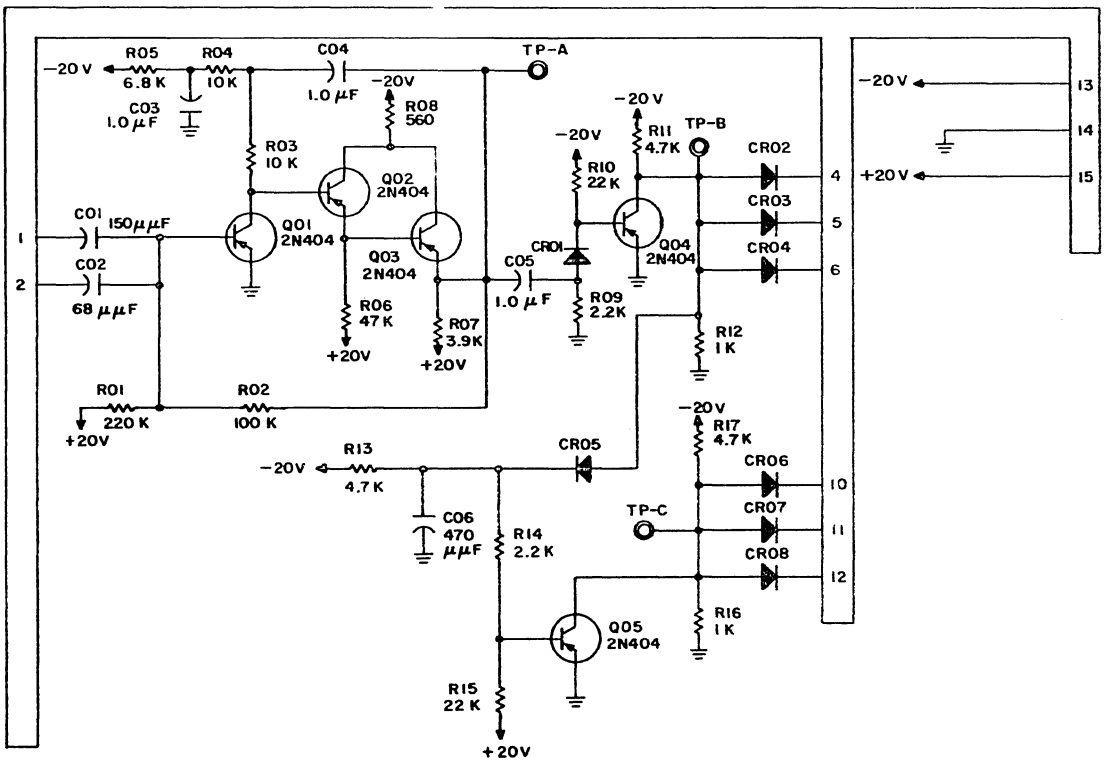
cuit. A delay capacitor, C06, delays the "1" (negative) excursion at the input, and the "0" (positive) excursion at the output.

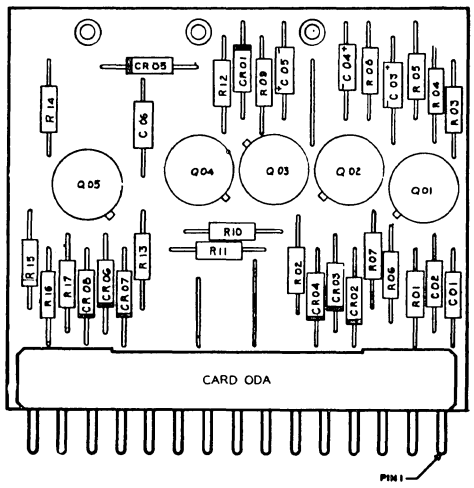
A narrow negative output pulse (1/4 to 1/2 usec) is produced when the output diodes of Q04 and Q05 are ANDed. The "1" (negative) output pulse corresponds to a point just following the positive peak on the input, or the zero crossover point in the positive direction of the differentiator output.



SYMBOL


XXXX
ODA-XXX
1
6
12


-20 V
R05 6.8 K
R04 10 K
C04 1.0 μF
TP-A
C03 1.0 μF
R08 560
R03 10 K
Q02 2N404
C01 150μμF
Q01 2N404
Q03 2N404
C02 68 μμF
R06 47 K
R07 3.9K
+20V
C05 1.0 μF
R10 22 K
R11 4.7K
TP-B
CR01
Q04 2N404
CR02
CR03
CR04
R09 2.2K
R12 1K
R01 220 K
R02 100 K
R13 4.7 K
CR05
R17 4.7K
CR06
CR07
CR08
TP-C
C06 470 μμF
R14 2.2 K
Q05 2N404
R16 1K
R15 22 K
1
2
4
5
6
10
11
12
13
14
15


CR05
R14
C06
R12
CR01
R09
C05
C04
R06
C03
R05
R04
R03
Q05
Q04
Q03
Q02
Q01
R10
R11
R15
R16
R17
CR08
CR07
CR06
R13
R02
CR04
CR03
CR02
R07
R06
R01
C02
C01
CARD ODA
PIN 1

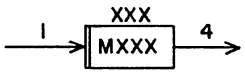
INPUT AMPLIFIER
OFA

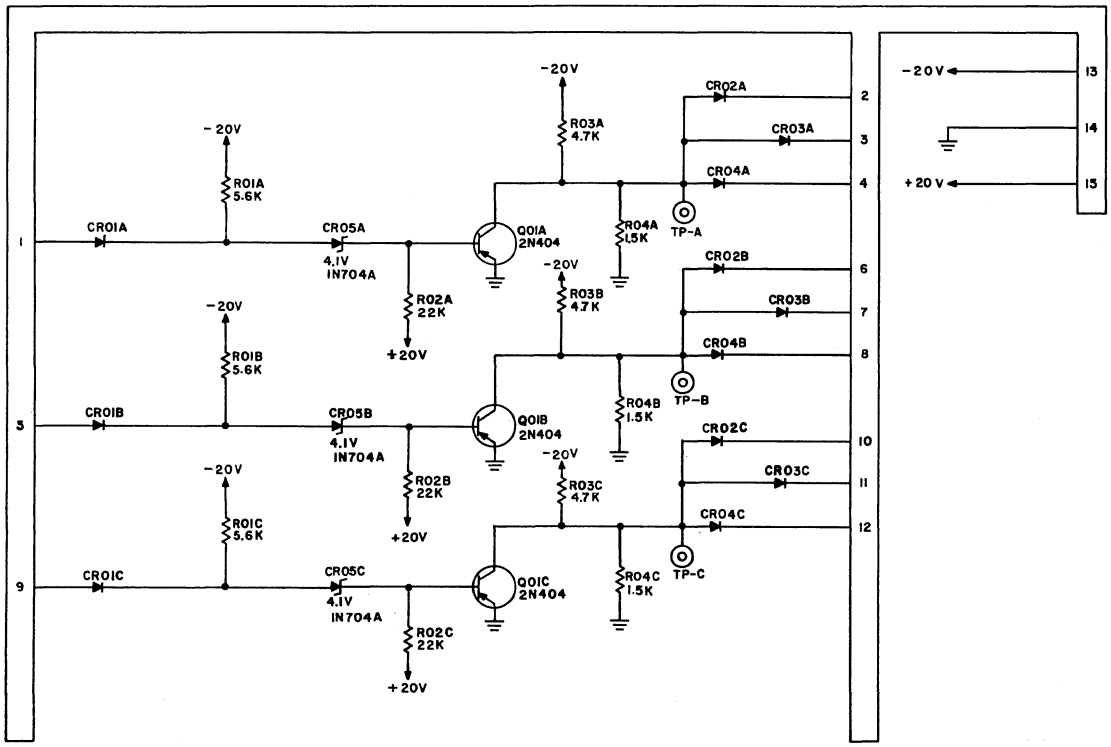
This input amplifier is used to operate from a common line in parallel with other like input amplifiers in other units, part or all of which may have internal power on or off.

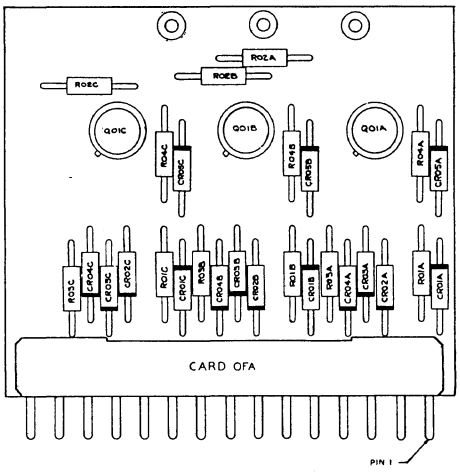
The circuit is a switching type inverter with certain small variations. Diode CR01 minimizes loading of the line in a positive direction when power is removed from this unit. Zener diode CR05 increases the efficiency of the base divider providing the proper switching point (about 4.4 volts negative) for the 0 to -8v input line.

Three standard logic output signals with their isolating diodes are available for each of the three circuits.

SYMBOL




-20V
R01A 5.6K
R01B 5.6K
R01C 5.6K
CR01A
CR01B
CR01C
CR05A
CR05B
CR05C
4.1V IN704A
R02A 22K
R02B 22K
R02C 22K
+20V
R03A 4.7K
R03B 4.7K
R03C 4.7K
Q01A 2N404
Q01B 2N404
Q01C 2N404
R04A 1.5K
R04B 1.5K
R04C 1.5K
TP-A
TP-B
TP-C
CR02A
CR03A
CR04A
CR02B
CR03B
CR04B
CR02C
CR03C
CR04C
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
-20V
+20V


R02A
R02B
R02C
Q01C
Q01B
Q01A
CARD OFA
PIN 1

PEAK DETECTOR

OGA, OGB, OGC

The peak detector operates from either positive or negative rectified signals from the output of level detectors. The peak detector can also be used with class A signals to locate either positive or negative peaks as selected by the input wiring. Provision is included for threshold enablin prior to the output when used with level detector (EI-Series) or "diode ANDing" at the output of level detector (EDA, EGA). The output of the peak detector is shaped to a nominal 3/4-usec pulse independent of the exact shape of the peak.

Peak detection is accomplished by first differentiating the input signal (C01, R01 and C04, R02) and then detecting the zero crossover point of this differentiated signal in the two-stage differential amplifier (Q01 Q02, and Q03, Q04). The detected zero crossover point is re-referenced to ground by Q05 and then shaped by the multivibrator (Q06, Q07) into a nominal 3/4-usec "1" pulse. Pin 8 receives the threshold enable signal, when used with the level detector to disable the output shaper. Other threshold enables (level detector EDA, EGA) are ANDed with pins 11 and 12. Mixing resistors are provided at pins 9 and 10 for use in forming composit signals with peak detectors on other tracks for deskewing purposes.

Pin 1* is used to receive positive rectified signals (pin 5** grounded); and pin 5** is used to receive negative rectified signals (pin 1* grounded). Therefore, the peak detector looks for a negative peak on pin 5** or a positive peak on pin 1*. Balanced or single-ended class A signal may be used also, and the input wiring determines which polarity peak is detected.

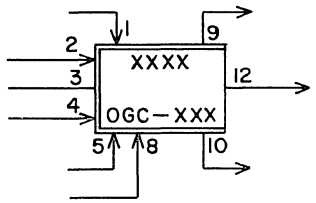
The multivibrator is triggered by the negative input signal at the base of Q06. Conduction of Q06 couples a positive pulse to the base of Q07 and causes it to switch off. Multivibrator regeneration is completed by the common emitter resistor R13. The period of the mutivibrator is determined by C07 and R14. Recycle time is determined by R15, R16, and C07. Diode CR03 supplies the additional emitter current necessary for the collector load of Q07 and references the emitter current to near ground for this stable state of the multivibrator. During the multivibrator period

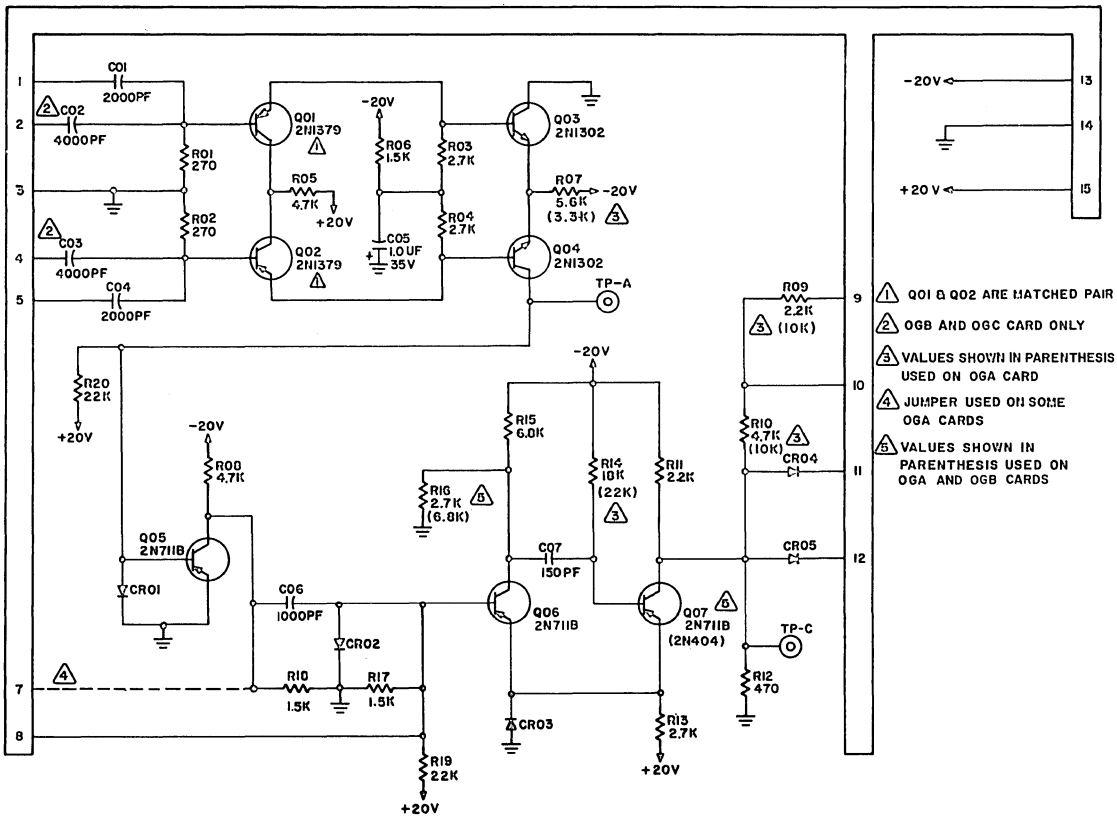
* Pin 2 for 75 ips, OGB, OGC only

** Pin 4 for 75 ips, OGB, OGC only

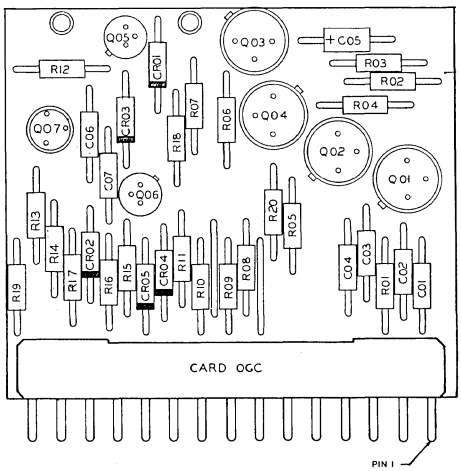
CR03 is reverse-biased, permitting the gain of Q06 and Q07 to be utilized through a common emitter resistance R13, providing fast fall and rise times.

SYMBOL





1. Q01 & Q02 ARE MATCHED PAIR
2. OGB AND OGC CARD ONLY
3. VALUES SHOWN IN PARENTHESIS USED ON OGA CARD
4. JUMPER USED ON SOME OGA CARDS
5. VALUES SHOWN IN PARENTHESIS USED ON OGA AND OGB CARDS



PEAK DETECTOR

OGD

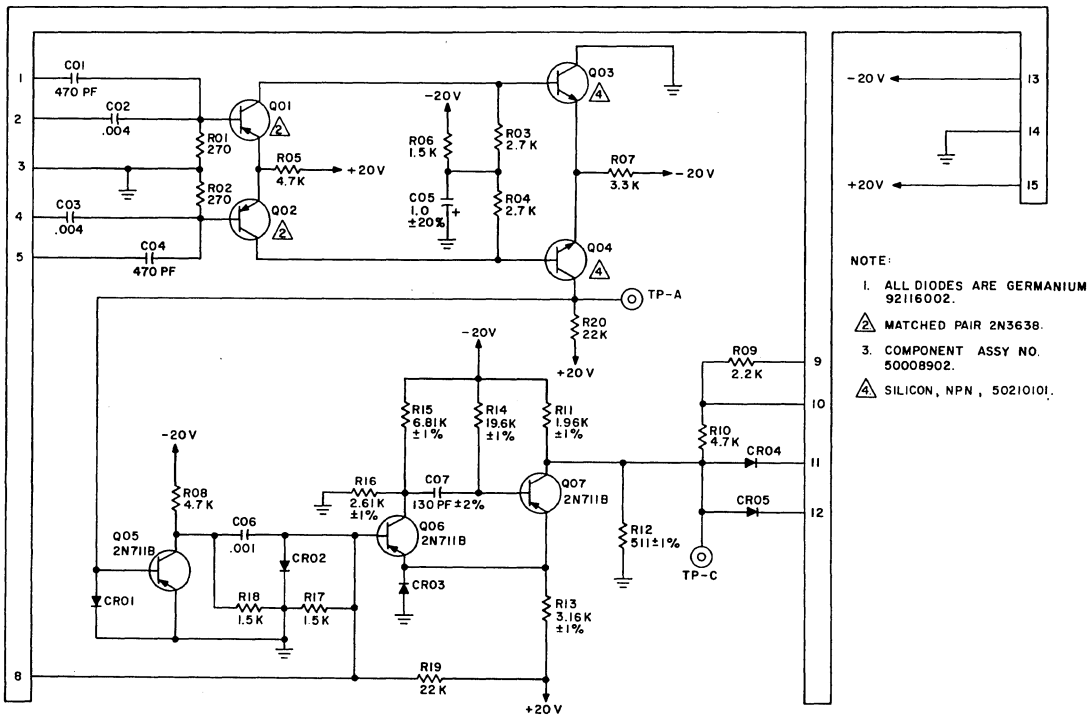
The OGD peak detector operates from either positive or negative rectified signals from the output of level detectors. It can also be used with Class "A" signals to locate either positive or negative peaks as selected by the input wiring. Provision is included for threshold enabling prior to the output when used with level detector (EI-Series) or "diode ANDing" at the output of level detector (EDA, EGA cards). The output of the detector is shaped to a nominal 3/4-μsec pulse independent of the exact shape of the peak.

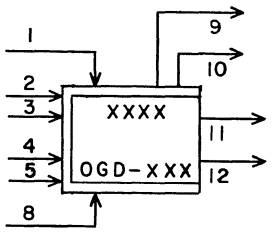
Peak detection is accomplished by differentiating the input signal (C01, R01, and C04, R02) and then detecting the zero crossover point of this differentiated signal in the two-stage differential amplifier (Q01, Q02, and Q03, Q04). The detected zero crossover point is re-referenced to ground by Q05 and then shaped by the multivibrator (Q06, Q07) into a nominal 3/4-μsec "1" pulse. When used with the level detector Pin 8 receives the threshold enable signal to disable the output shaper. Other threshold enables (level detector EDA, EGA) are ANDed with pins 11 and 12. Mixing resistors are provided at pins 9 and 10 for use in forming composite signals with peak detectors on other tracks for deskewing purposes.

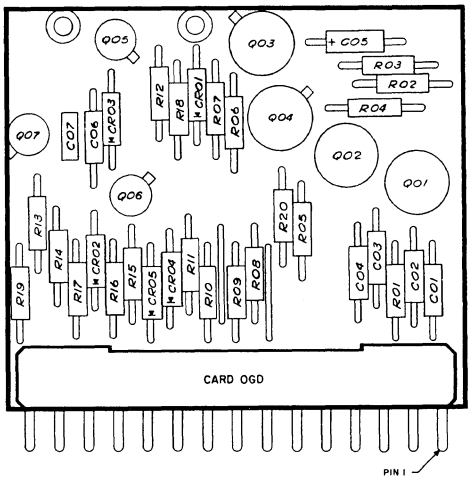
Pin 1 is used to receive positive rectified signals (pin 5 grounded); and pin 5 is used to receive negative rectified signals (pin 1 grounded). Therefore, the peak detector looks for a negative peak on pin 5 or a positive peak on pin 1. Balanced or single-ended class "A" signals may be used also, and the input wiring determines which polarity peak is detected.

The multivibrator is triggered by the negative input signal at the base of Q06. Conduction of Q06 couples a positive pulse to the base of Q07 and causes it to switch off. Multivibrator regeneration is completed by the common emitter resistor R13. The period of the multivibrator is determined by C07 and R14. Recycle time is determined by R15, R16, and C07. Diode CR03 supplies the additional emitter current necessary for the collector load of Q07 and references the emitter current to near ground for

this stable state of the multivibrator. During the multivibrator period CR03 is reverse-biased, permitting the gain of Q06 and Q07 to be utilized through a common emitter resistance R13, providing fast fall and rise times.







PEAK DETECTOR
OHA

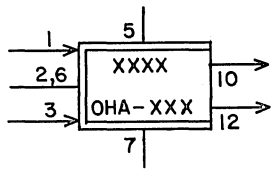
The peak detector operates from a Class A amplified head signal. It is designed for use with balanced input signals but may also be operated single ended by grounding the other input pin. The circuit has two output sections. TP-C provides an output logic "1" pulse for a negative peak (pin 1 relative to pin 3), and TP-D provides an output logic "1" pulse for a positive peak. Both pulses are 0.5 to 1.1 usec width at the -2v level. Provision is included (pins 5 and 7) for threshold enabling prior to the output when used with the ELA or a similar circuit. The circuit is designed for 120 kc data rates (60 and 120 kc sine-wave components) in phase modulation recovery where the amplitude of the nominal signal is 8v peak-to-peak.

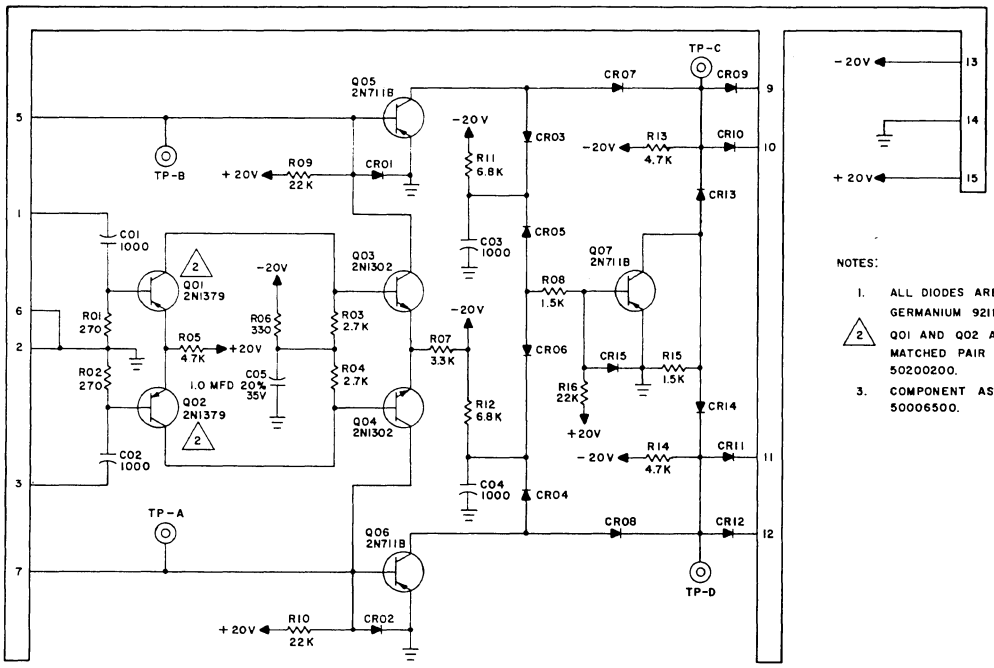
Peak detection is accomplished by first differentiating the input signal (C01, R01 and C02, R02) and then detecting the zero crossover point of this differentiated signal in the two-stage differential amplifier (Q01, Q02 and Q03, Q04). The detected zero crossover point is re-referenced to ground by Q05 and Q06. Threshold disabling may also be connected to the base leads of Q05 and Q06 by supplying current from a negative source. A minimum of 2 ma is required for either transistor and pins 5 and 7 must be from isolated circuits to prevent interaction between Q05 and Q06.

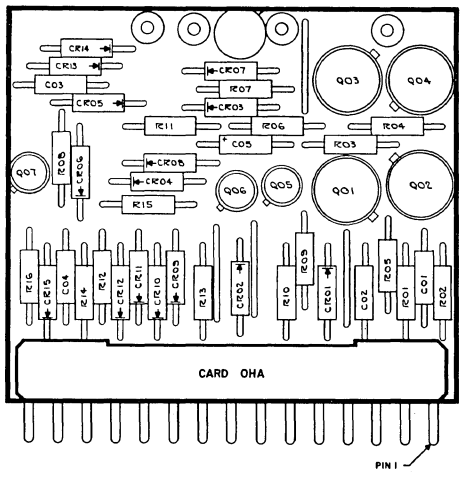
An output pulse appears when Q05 (TP-C) or Q06 (TP-D) turns off. The width of either output pulse is determined by the time Q07 remains off following the switching off of either Q05 or Q06. When Q05 turns off, C03 and R11 in the base circuit of Q07 determine the output pulse width. When Q06 turns off, C04 and R12 determine the width.

Caution should be exercised in using this circuit to drive standard inverters since logic "0" outputs may range from -0.6v to -1.2v. This is caused by the additional series output diode used in the pulse shaping circuit.

SYMBOL



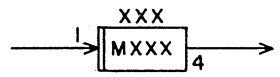

TP-C
TP-B
TP-A
TP-D
Q05 2N718
Q03 2N1302
Q01 2N1379
Q02 2N1379
Q04 2N1302
Q06 2N718
Q07 2N718
CR07
CR09
CR03
CR10
CR13
CR05
CR06
CR14
CR11
CR04
CR08
CR12
CR01
CR02
R09 22K
R13 4.7K
R11 6.8K
R08 1.5K
R15 1.5K
R16 22K
R14 4.7K
R10 22K
R01 270
R02 270
R05 4.7K
R06 330
R03 2.7K
R04 2.7K
R07 3.3K
R12 6.8K
C01 1000
C02 1000
C03 1000
C04 1000
C05 1.0 MFD 20% 35V
-20V
+20V
NOTES:
1. ALL DIODES ARE GERMANIUM 92116002.
2. Q01 AND Q02 ARE MATCHED PAIR PER 50200200.
3. COMPONENT ASSY NO. 50006500.

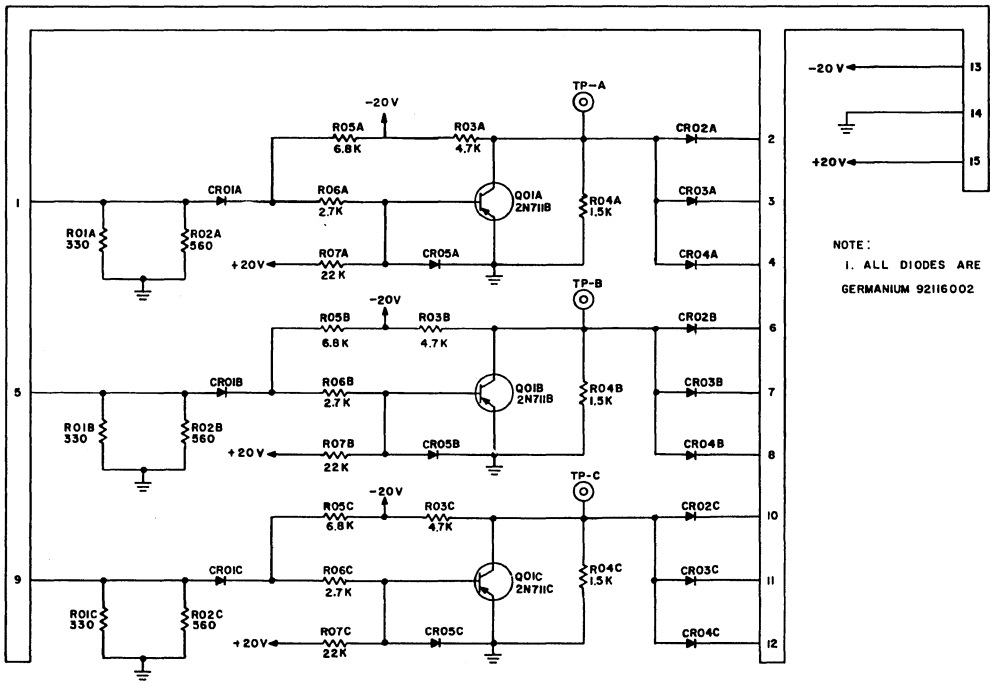

CARD OHA
PIN 1

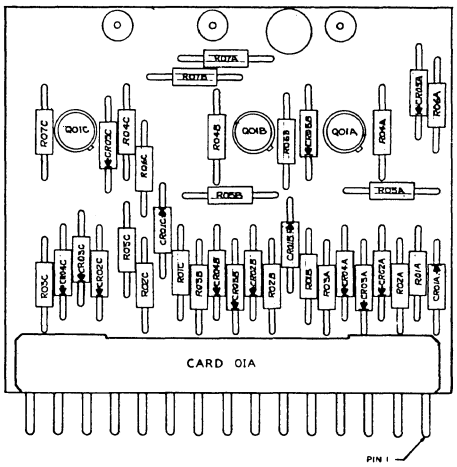
INPUT AMPLIFIER
OIA

The input amplifier card is used to interface from external equipment operating with signal excursions of 0 to -6v. Its output matches standard logic signals (0 to -3v). The input terminates a line at approximately 200 ohms to ground and switches on minimum excursions of -1 1/2 to -4 1/2v.

Three identical circuits are used. Each circuit has three output diodes for AND terms.

SYMBOL 


TP-A
TP-B
TP-C
-20V
+20V
R05A 6.8K
R03A 4.7K
R06A 2.7K
R07A 22K
R01A 330
R02A 560
Q01A 2N711B
R04A 1.5K
CR01A
CR02A
CR03A
CR04A
CR05A
R05B 6.8K
R03B 4.7K
R06B 2.7K
R07B 22K
R01B 330
R02B 560
Q01B 2N711B
R04B 1.5K
CR01B
CR02B
CR03B
CR04B
CR05B
R05C 6.8K
R03C 4.7K
R06C 2.7K
R07C 22K
R01C 330
R02C 560
Q01C 2N711C
R04C 1.5K
CR01C
CR02C
CR03C
CR04C
CR05C
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
NOTE:
1. ALL DIODES ARE GERMANIUM 92116002


CARD 01A
PIN 1

LONG TERM DELAY
OJB

The OJB card is intended for applications requiring a long delay which does not have to be accurately adjusted. By means of jumper options, a total of twenty discrete delays of a logic "0" input can be selected in the range of 2 msec to 50 sec. Table 1 lists the delays for a given set of jumpers. An alternate presentation of the delays is shown in figure 1 and is used when some intermediate value of delay is needed. This can be accomplished with external capacitors between pins 1 and 4.

The input and output waveforms are shown in figure 2. The input is derived from an output card or opening of a set of contacts.

Referring to the schematic, the circuit contains a unijunction transistor (Q02), the basic timer, a silicon controlled rectifier as a bistable device (Q03), and the output transistor (Q01).

The input is applied at pin 1. If this is at ground, no voltage exists on the Q02 - Q03 combination. Therefore, since Q01 has no base voltage, it will be off and the output is -3 volts.

Assuming the input is allowed to go negative, approaching -20v or opened, voltage is applied to the unijunction transistor timer via R01. The timing capacitor C01 (or C01 in parallel with C02) will begin to charge through R01, R02, and R03 (or R03 in parallel with R04, R05, and/or R06). Although the timing capacitor is shunted by the emitter to base 1 circuit of the unijunction transistor, this is not a problem since it represents an impedance of over 3 meg ohms.

When the capacitor reaches 6 to 8 volts with polarity as indicated on the schematic, the unijunction transistor becomes regenerative so the emitter to base 1 impedance becomes very small (approximately 20 ohms). This discharges the capacitor around the emitter-base 1 and R08 loop and generates a positive pulse on R08. This pulse is applied to the gate-emitter junction of Q03. Q03 turns on applying a negative voltage to Q01 so it also turns on. Since the junction of C01 and R01 is only two diode drops from ground when Q01 and Q03 turn on, the voltage on the timing circuit is reduced to approximately -1.6 volts. This prevents the unijunction transistor from becoming a free running oscil-

lator. The output of Q01 remains within a fraction of a volt of ground after the delay period.

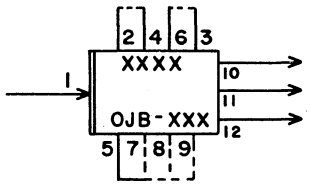
Normally the time delay is changed by changing either the timing capacitor (C01, C02) or the timing resistor (R02, R03). However, by jumpering between pins 3 and 6, a resistor divider reduces the voltage across the unijunction transistor base 1 to base 2. This indicates the capacitor charges to a lower level before regeneration occurs in the unijunction transistor, thereby reducing the delay.

If the input is again brought to ground, the bottom end of R01 is pulled to approximately -0.6v of ground. Since this is less than the voltage drop across Q03 plus the base-emitter junction of Q01, Q03 and Q01 will both turn off. Note that if pin 1 does not come within -1.0v of ground, Q03 and Q01 may not turn off.

The current through Q03 must delay to the holding current level before it will turn off; this takes approximately 40 usec. Therefore, the input logic "1" pulse wodth W in figure 2 should be at least 50 usec wide.

If the input in figure 2 is returned to 0 volts or logic "1" before the time delay has expired, the output will remain at logic "1". Since the timing capacitor may have charged close to the unijunction firing level, it will have to discharge to almost 0 before a new delay period can be initiated. The length of the waiting period should be 10% or more of the minimum delay given in figure 1 for either the 1 uf or 68 uf capacitor (200 usec for the 1 uf capacitor and approximately 14 msec for the 68 uf capacitor). Under these conditions a 10% change in the time delay can be expected due to residual voltage on the capacitor.

SYMBOL



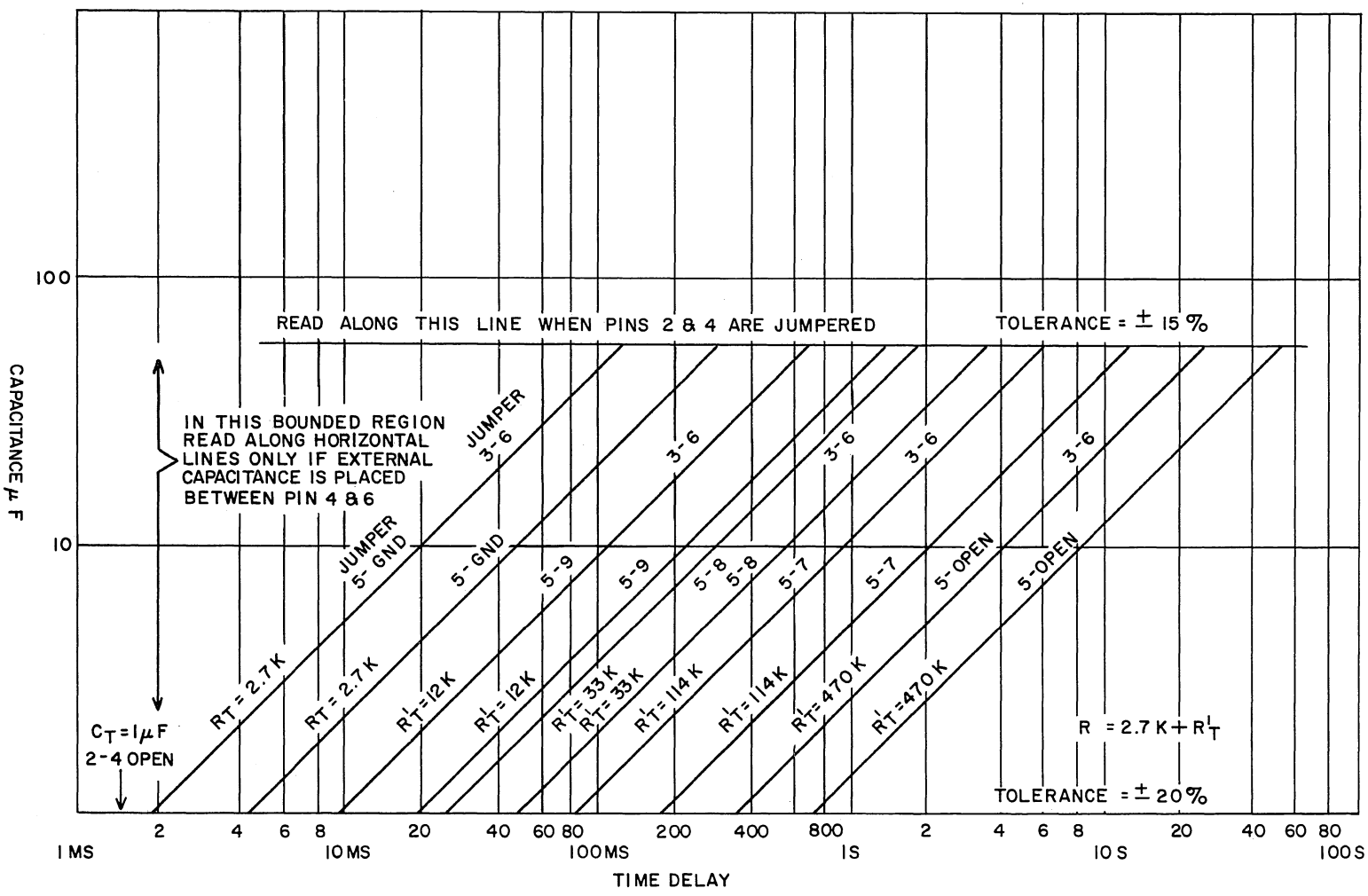
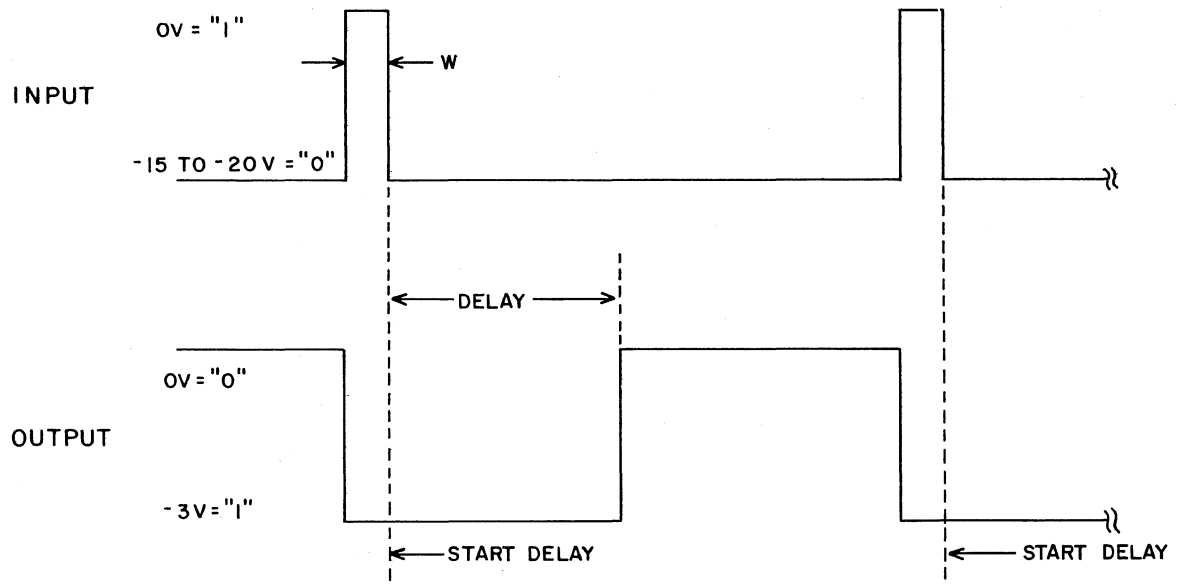
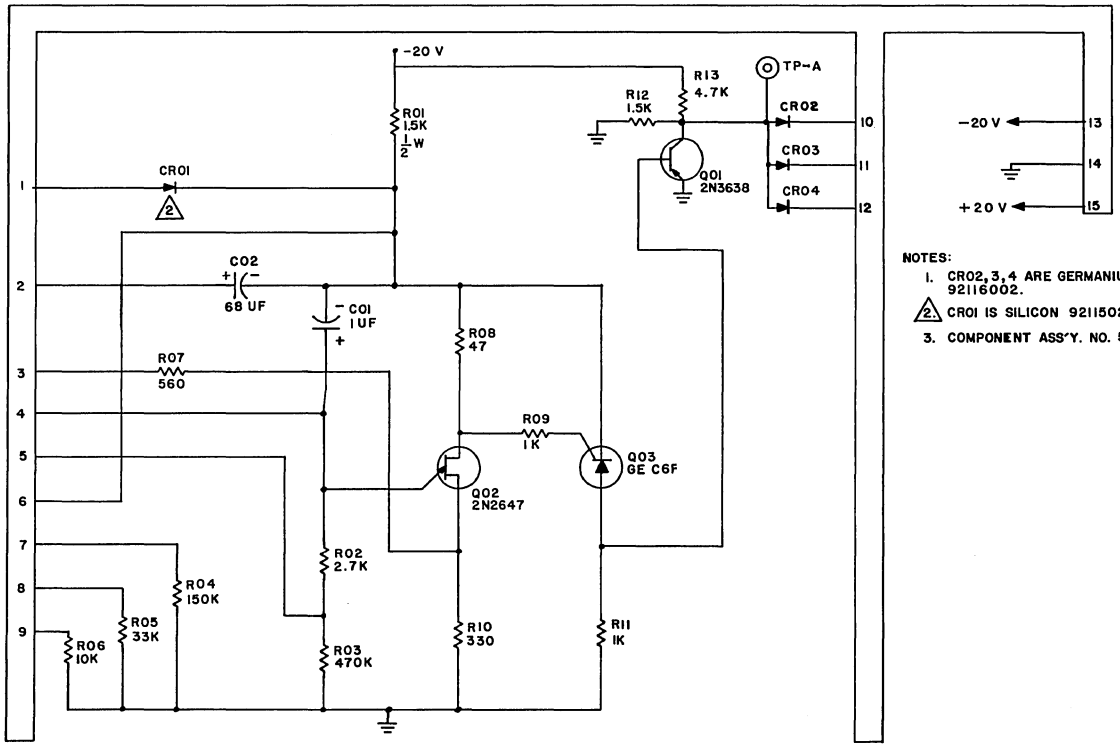


FIGURE 1. TIME DELAY VS EXTERNAL CONNECTIONS

Table 1. Delays

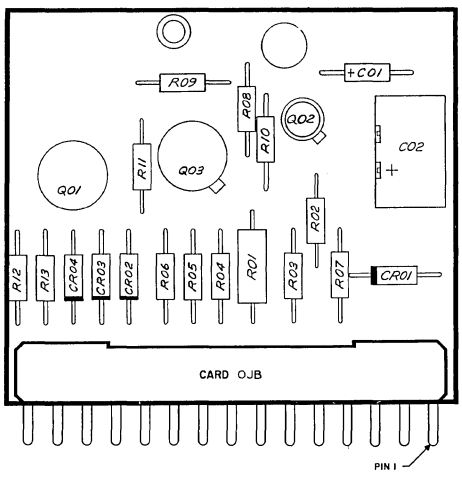
Delay ±20%	Jumper Pins	Delay ±20%	Jumper Pins
1.9 msec	3-6, 5-gnd	340 msec	3-6
4.4 msec	5-gnd	650 msec	2-4, 3-6, 5-9
8.8 msec	3-6, 5-9	760 msec	none
19 msec	5-9	1.3 sec	2-4, 5-9
23 msec	3-6, 5-8	1.7 sec	2-4, 3-6, 5-8
50 msec	5-8	3.6 sec	2-4, 5-8
84 msec	3-6, 5-7	6.0 sec	2-4, 3-6, 5-7
145 msec	2-4, 3-6, 5-gnd	11.5 sec	2-4, 5-7
183 msec	5-7	24 sec	2-4, 3-6
315 msec	2-4, 5-gnd	52 sec	2-4





NOTES:

1. CR02,3,4 ARE GERMANIUM 92116002.
2. CR01 IS SILICON 92115021.
3. COMPONENT ASS'Y. NO. 5002300I.



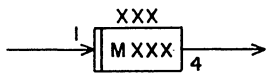
INPUT AMPLIFIER

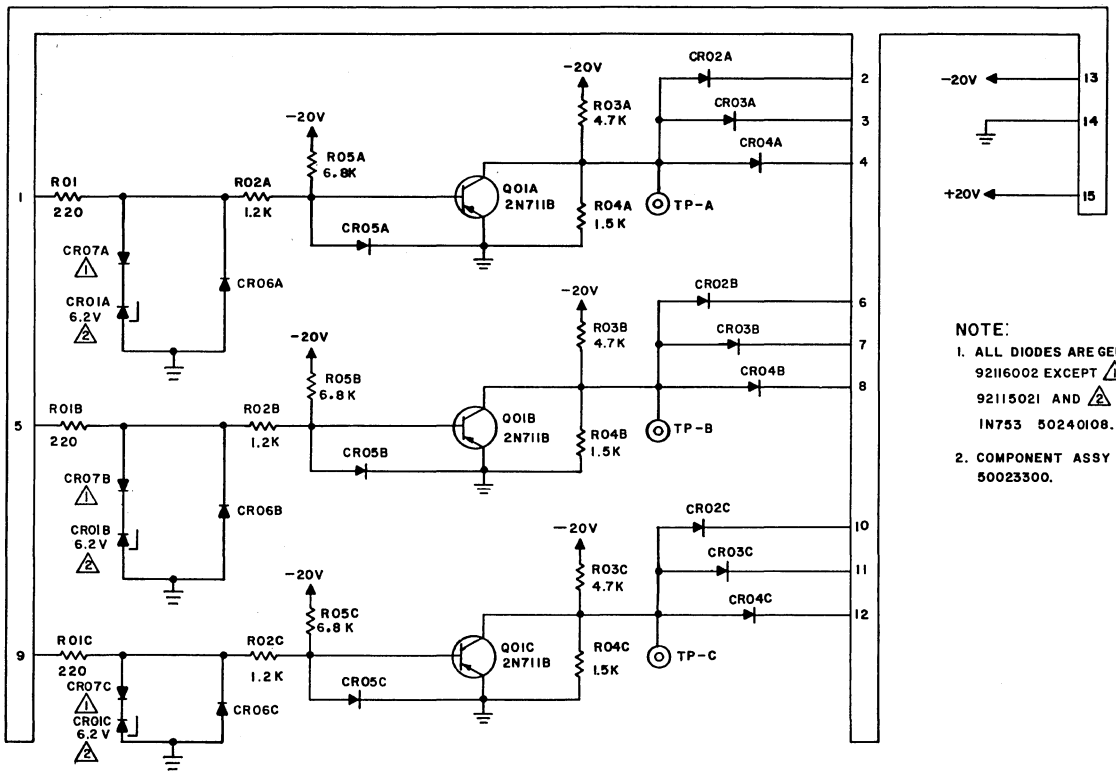
OKA

The input amplifier card is used to interface from external equipment operating with signal excursions from 0 to +9v. Its output matches standard logic signals (0 to -3v). Input to the amplifier is via a 220-ohm series resistor. The other end of the resistor is clamped at +6.5v in the positive direction and at ground in the negative direction. A minimum excursion of +2v to +6v is required at the input pins. Line noise and ringing shall be outside this +2v to +6v region to prevent unwanted switching of the circuit.

Three identical circuits are provided on each card. Each circuit has three output diodes for AND terms.

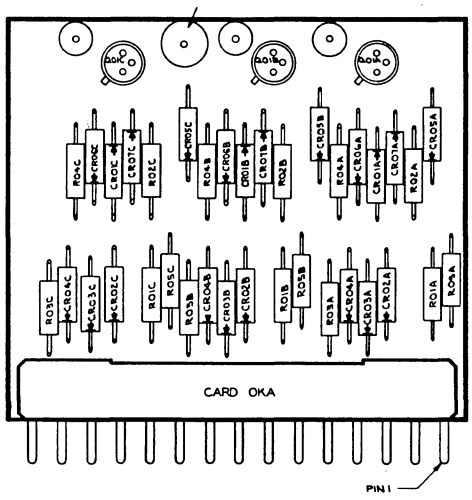
SYMBOL





NOTE:

1. ALL DIODES ARE GERMANIUM 92116002 EXCEPT ⚠1 SILICON 92115021 AND ⚠2 ZENER IN753 50240108.
2. COMPONENT ASSY NO. 50023300.



FLYBACK VERIFY FLIP-FLOP
OLA

This flip-flop was originally designed for use in the 501 Printer error-checking system known as echo checking. The device is a toggle flip-flop with a 2-term AND on the set input, a clear line, and a toggle input. The circuit is normally set when a given character is to be printed. After the hammer for that particular character fires, an inductive-kick pulse, during current delay, toggles the flip-flop back to a cleared state. A lamp is provided on the card so that one can see what state the circuit is in. The output from 12 such cards are capable of being Anded together for forming of an error signal. Output voltage at the test points is nominally -10v instead of the usual -3v.

The circuit is set when standard -3v levels exist on both terms of the AND input or both inputs are open. The flip-flop is cleared by 0 volts on the clear line. Negative pulses on the toggle input of at least 4v will change the state of the flip-flop. The toggle pulse is typically developed from the inductive kick initiated at turnoff of the current to the inductive load (a hammer in the 501 Printer).

Cirucit operation is best understood by referring to the circuit schematic. Assume the following sequence on the inputs: a) the circuit is cleared, b) set pulses are put in, and c) the toggle pulse is applied.

When pin 9, the clear line, is pulsed to within -1.0v of ground, and at least one set input is near 0v, the collector of Q03 is grounded. By the divider action of R08, R09, and R10, a plus voltage of about 1.0v results at the base of Q02. This turns Q02 off and its collector voltage becomes -10v. Since Q02 collector is tied to Q03 base by resistor R12, the -10v collector voltage holds the base of Q03 on. The circuit is now in the cleared state and will remain there until either the set pulses or toggle pulse are applied.

To set the flip-flop, assume that a negative 3 volts appears on both pins 2 and 3 or that both are open, i.e., the AND term is complete and that pin 9 is either open or more negative than -10 volts. Pin 9 voltage should not be less than -10v, otherwise the collector of Q03 will be clamped to whatever the clear line voltage is (assuming a low impedance clear source). Under these conditions, the junction of R07 and R08 is un-

clamped. The voltage divider composed of R07, R08, R09, and R10 lets the base of Q02 go negative thus turning Q02 on. Q02 collector voltage is now near zero and is coupled to the base of Q03 via R12. By the divider action of R12 and R14, the base of Q03 is driven +1 volt so that Q03 is off. The collector of Q03 goes to -10v which now supplies about 1 ma of base current to Q02, holding it on although the input on pins 2 and/or 3 goes back to ground. The flip-flop is now in the set state where it remains until cleared or a toggle pulse occurs.

When the hammer in the printer fires, an inductive kick pulse is formed at the end of the current pulse. This pulse is negative and about 10 volts. The toggle input to the flip-flop is applied to pin 1. Transistor Q01 has its base biased 3.5 volts positive so that the input pulse must rise to -3.7 volts before Q01 turns on. This is done to discriminate against noise pulses on the toggle line. Resistors R04 and R06 form a divider which hold Q01 collector at -10 volts. When Q01 goes on, its collector goes to ground as long as the input pulse is above -3.7 volts. The positive transition from -10v to ground on Q01 is passed through capacitors C03 and C04 as a positive 10-volt pulse.

At this point, consider the voltage across diodes CR05 and CR06. With Q02 on its collector is at about -0.2v. This is passed through forward biased diode CR04 so that the junction of R05 and CR05 is at nearly-0.4 volt. Since Q02 is on, its base voltage is also at about -0.2 volt. Thus it is seen that CR05 is reversed biased only about 0.2 volt.

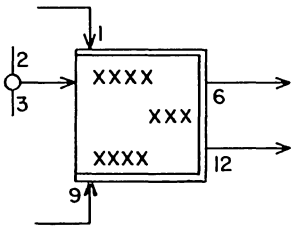
During this time Q03 is off, so its collector voltage of -10 volts is passed through forward-biased diode CR07. The junction of CR06 and R17 is therefore at about -10 volts. The base of Q03 is reversed biased by 1 volt so that diode CR06 is seen to be reverse biased by 11 volts.

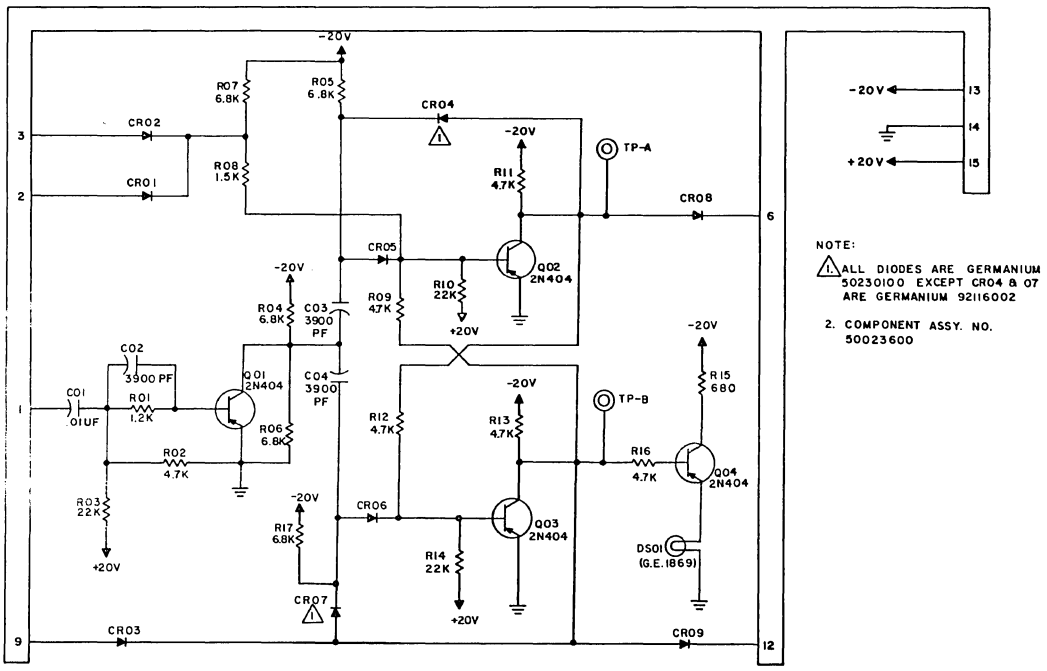
When the 10-volt pulse from Q01 passes through C03 and C04, it sees diodes CR05 and CR06 but can only pass through CR05 because the reverse bias on CR06 exceeds the pulse amplitude. Thus, the toggle pulse turns off the "on" transistor. If Q03 had been on, diode CR05 would be reverse biased and the toggle pulse steered to Q03 instead.

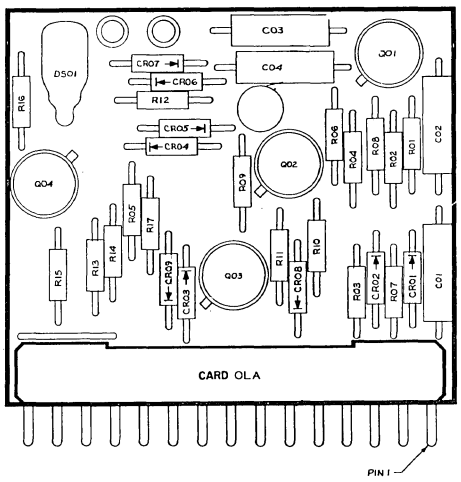
The indicator lamp is lighted when the flip-flop is set. Trans-

istor Q04 is basically an emitter follower circuit. When Q03 is off, the -10 volts on the collector allows base current to flow in Q04 and apply 10 volts to the lamp and the remaining 10v acorss R15.

SYMBOL







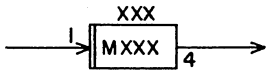
INPUT AMPLIFIER, HIGH FAN-OUT
OMA

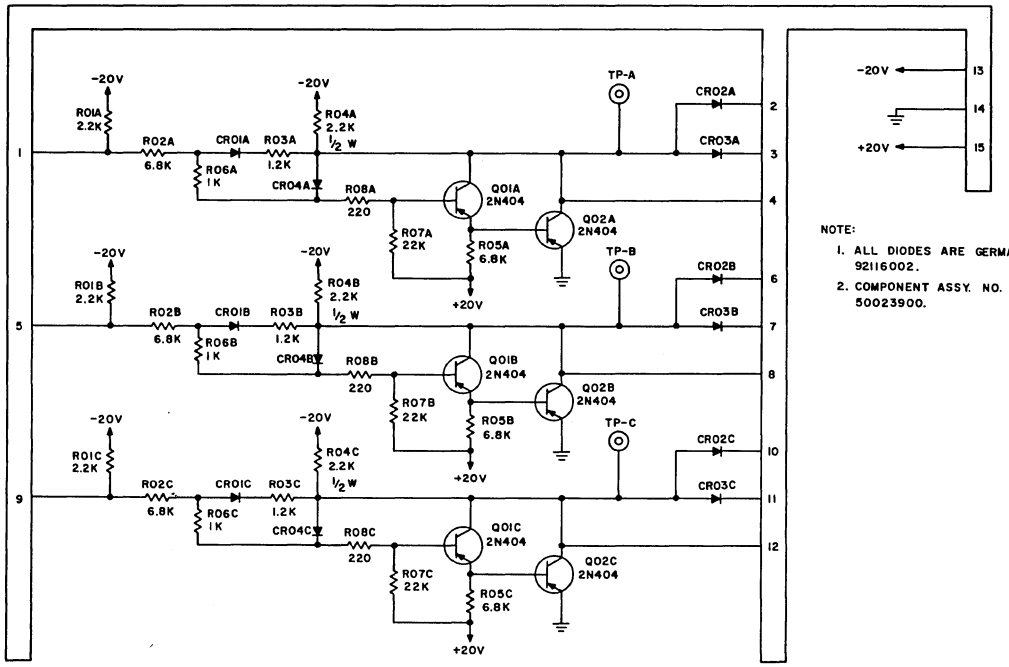
The OMA is a circuit designed to provide high fan-out logic signals for use in printer echo check circuitry. The OMA is essentially an "M" card, i.e., an input amplifier which matches the output of an "L" card. The difference between this card and an "M" card is that one output diode per circuit is omitted on the OMA. There are three identical circuits per card. Output pins 4, 8, and 12 are connected directly to the collector of the output transistor and are the only output pins to be used for the high fan-out. The other two outputs per circuit have the logic diode in series to provide signals for ordinary logic circuits if desired.

When the input signal is at ground, the output switches to -3v. Thus an open input causes the output to switch toward ground. Each output (4, 8, or 12) may be fanned out to as many as 17 input logic circuits requiring 3 ma each, i.e., a 50-ma output at -.5v.

Circuit operation is as follows: an open input provides more negative drive to the base of Q02 through divider R02, R06, R08, R07, and emitter follower Q01. Q02 nears saturation but is held in the active region by CR04 and R08 feeding back negatively to the base of Q01. The output is held at -.5v. A ground at the input provides less drive to the base of Q02 through the divider and Q01. Q02 nears cut-off but is held in the active region by divider R04, R03, CR01, R06, R08, and R07. The output is maintained at -3v.

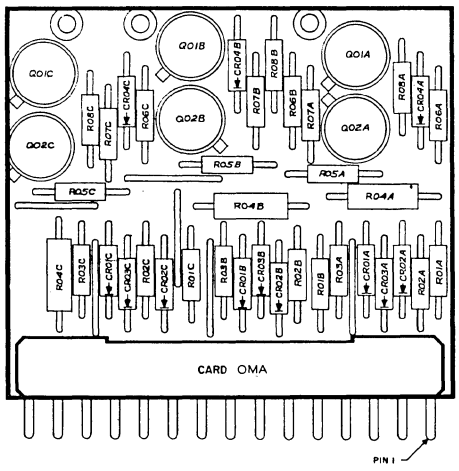
SYMBOL





NOTE:

1. ALL DIODES ARE GERMANIUM 92116002.
2. COMPONENT ASSY. NO. 50023900.



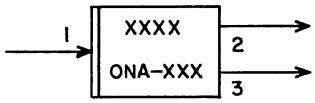
PHOTOCELL AMPLIFIER

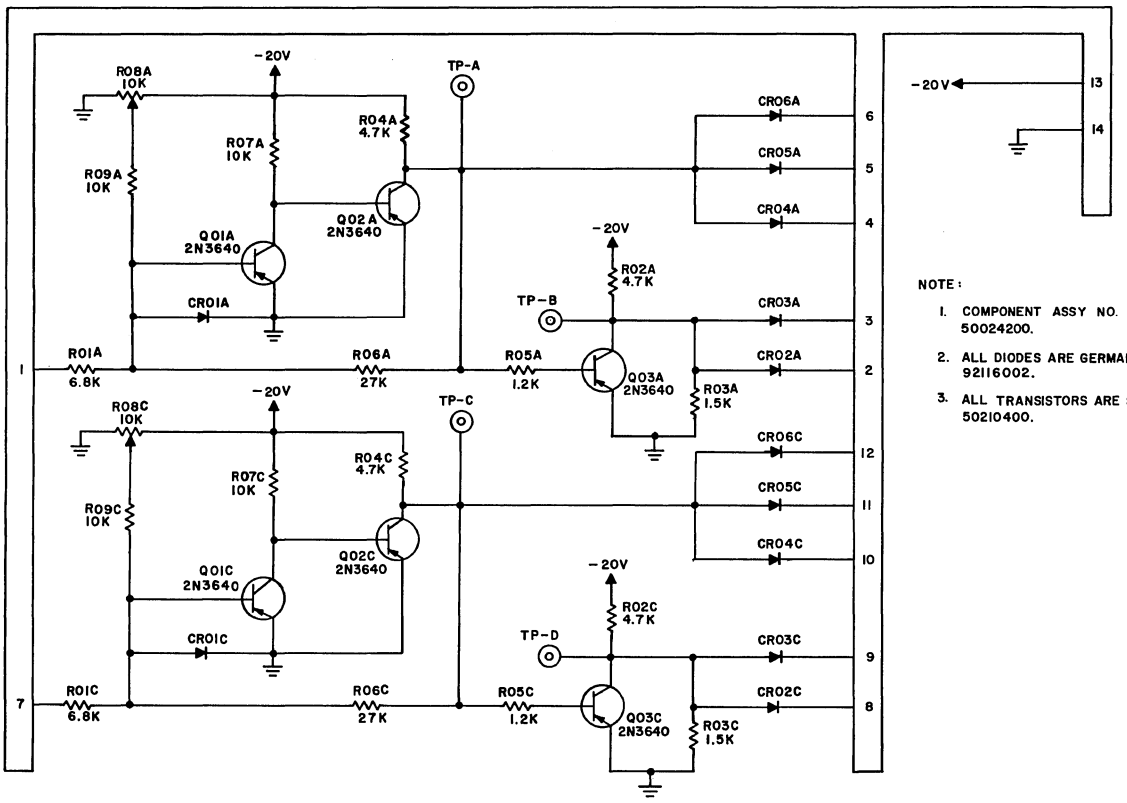
ONA

The photocell amplifier is designed to receive its input from a silicon photo transistor returned to +20V. When the photo transistor is illuminated, output of transistor Q03 is a "1" and Q02 is a "0". Outputs reverse when the photo transistor is unlighted. An adjustable potentiometer is provided to allow optimum centering of the amplifier switching point for tolerances in the light source, the photo transistor, and the input stage of the amplifier. Positive feedback around the first two stages of the amplifier provides a small amount of hysteresis to the input switching point to minimize the possibility of remaining in an intermediate state or switching on hum components of light sources.

Q01 is an input inverting amplifier that is normally turned on by drive current through R09 from potentiometer R08. Q01 is turned off by supplying sufficient current to pin 1 via a photo transistor. Q02 acts as a second inverter that drives three output diodes for "AND" terms. The output of Q02 is coupled back to the input via R06 to provide a controlled amount of hysteresis in the input switching current. The output of Q02 is also used as an input to Q03. This input loading also limits the negative excursion at the collector output of Q02. Q03 compliments the output of Q02 by inversion, and has two output diodes for "AND" terms. Two identical circuits are provided on each card.

SYMBOL

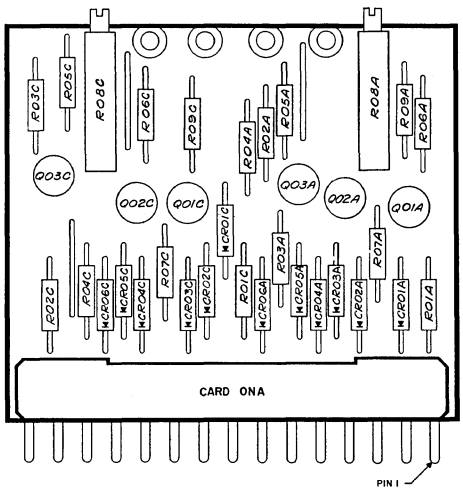




NOTE:

1. COMPONENT ASSY NO. 50024200.
2. ALL DIODES ARE GERMANIUM, 92116002.
3. ALL TRANSISTORS ARE SILICON, 50210400.

ONA



INPUT AMPLIFIER
OPA

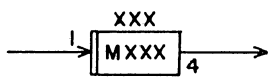
The OPA input amplifier card was initially designed for use on time shared lines between PED 9131 tape units and a controller used by Mitsubishi Co. of Toyko, Japan. The input is designed for signal excursions from +1.5v to -3.5v. Its output matches standard logic signals (0 to -3v). Original application utilizes 8 or less OPA circuits in parallel on twisted pair I/O lines of 100 ft. maximum length.

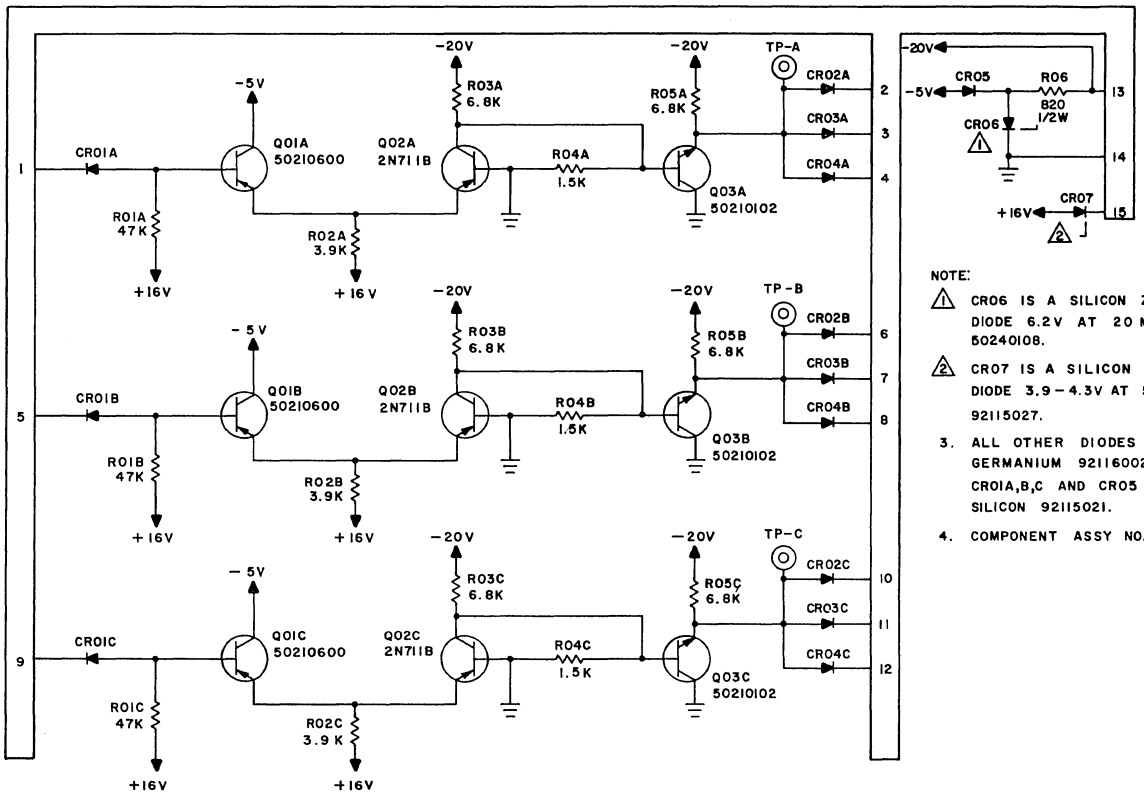
Loading of the line signal is minimized to permit OPA input amplifiers to be paralleled whether their power supply voltages are present or not. The OPA circuit includes power supply disconnect features to minimize loading to ground when voltages are not present. CR07 prevents loading when +20v supply is off. With -20v supply off, CR05 prevents loading to ground. Q01 is one-half of a differential amplifier (Q01, Q02) and represents very little loading to the line. Input switching threshold is -1v $\pm$ .2v. Q03 acts as an emitter follower to drive three output diodes available for AND terms.

A -3.5v input provides a logic "1" output (-4v min). A +1.5v input provides a logic "0" output (-3/4v). Switching time after the input signal is outside the threshold region (-.8v to -1.2v) is 200 nanoseconds or less in both directions.

The line driver used in conjunction with the OPA will provide a "1" signal of -3.5v. When the driver is turned off, a termination at the end piece of equipment determines the "0" voltage on the line. The termination should match the line characteristics and provide a positive "0" voltage (when the line driver is off) sufficient to overcome line attenuation, crosstalk and other related factors.

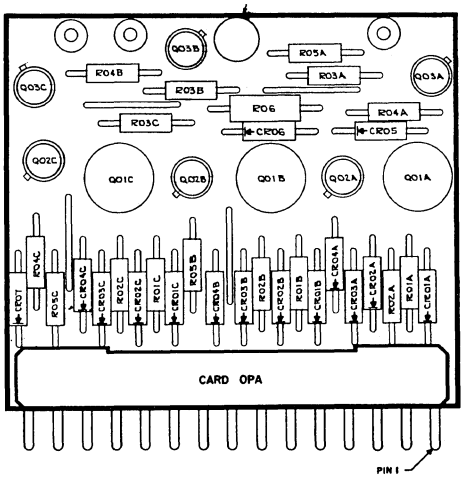
SYMBOL





NOTE:

1. CR06 IS A SILICON ZENER DIODE 6.2V AT 20 MA, 50240108.
2. CR07 IS A SILICON ZENER DIODE 3.9 – 4.3V AT 5 MA, 92115027.
3. ALL OTHER DIODES ARE GERMANIUM 92116002, EXCEPT CR01A,B,C AND CR05 ARE SILICON 92115021.
4. COMPONENT ASSY NO.50024800.



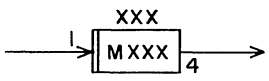
INPUT AMPLIFIER
OQA

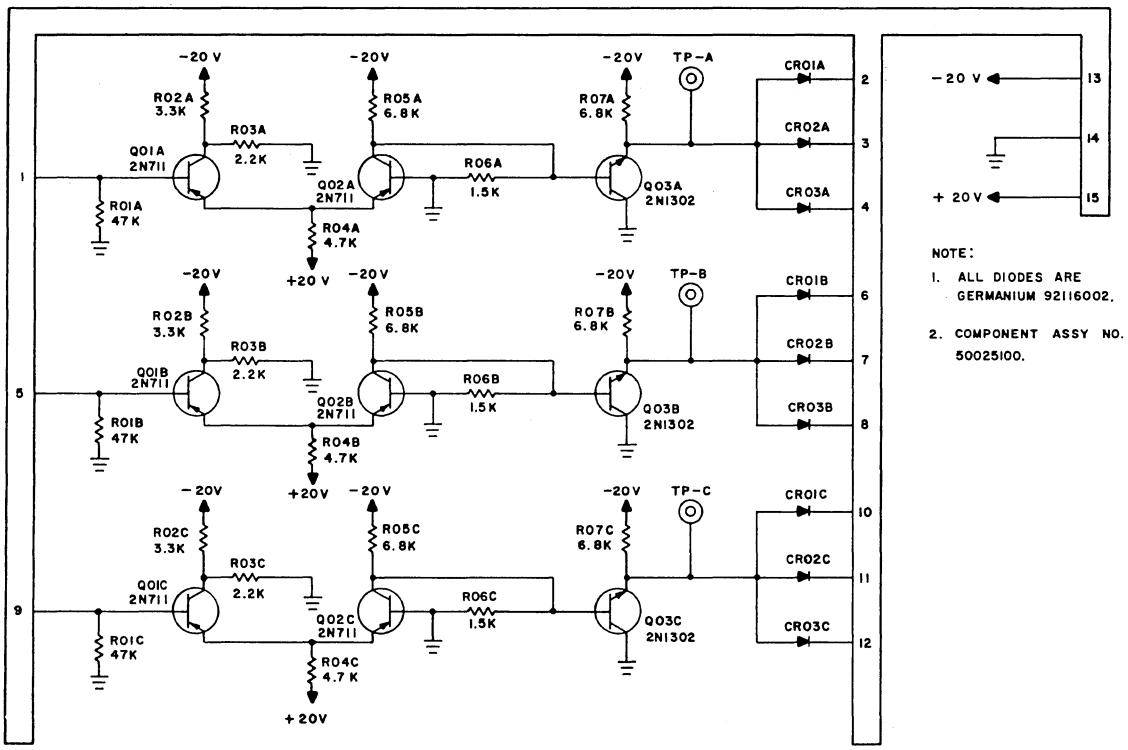
The input amplifier card is used to interface from a signal similar to IBM "n" levels to standard logic signals (0 to -3v). Up to eight OQA receiver circuits may be paralleled (daisy-chained) on one line and located in various equipment such as magnetic tape units. To prevent excessive line loading, power is required on all receivers connected to a given line.

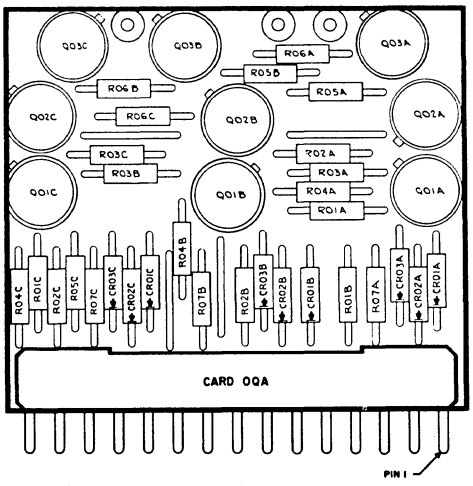
There are three identical circuits on each card and each circuit includes three transistors. Q01 and Q02 form a differential amplifier. The base of Q02 is tied to ground and provides the switching threshold of the circuit. Q03 is an emitter follower output. Each circuit has three output diodes for AND terms.

A minimum excursion of +0.4v to -0.4v free of noise is required at the input. The driver used in conjunction with the OQA will provide a "1" signal of -3.5v. When the driver is turned off, a termination at the end piece of equipment determines the "0" voltage on the line. The recommended termination at the end of the line is 1200 ohms to +20v and 100 ohms to ground, making the "0" voltage +1.5v. The OQA will switch to a "1" (-4v) with a "1" input in 0.25 usec and will switch to a "0" (0v) with a "0" input in 0.35 usec. Both switching times are maximum.

SYMBOL




-20 V
R02A 3.3K
R03A 2.2K
Q01A 2N711
R01A 47K
Q02A 2N711
R04A 4.7K
+20 V
R05A 6.8K
R06A 1.5K
R07A 6.8K
TP-A
Q03A 2N1302
CR01A
CR02A
CR03A
R02B 3.3K
R03B 2.2K
Q01B 2N711
R01B 47K
Q02B 2N711
R04B 4.7K
R05B 6.8K
R06B 1.5K
R07B 6.8K
TP-B
Q03B 2N1302
CR01B
CR02B
CR03B
R02C 3.3K
R03C 2.2K
Q01C 2N711
R01C 47K
Q02C 2N711
R04C 4.7 K
R05C 6.8K
R06C 1.5K
R07C 6.8K
TP-C
Q03C 2N1302
CR01C
CR02C
CR03C
1
5
9
2
3
4
6
7
8
10
11
12
13
14
15
- 20 V
+ 20 V
NOTE:
1. ALL DIODES ARE GERMANIUM 92116002.
2. COMPONENT ASSY NO. 50025100.


Q03C
Q03B
Q03A
R06A
R05B
R06B
R05A
Q02C
R06C
Q02B
Q02A
R02A
R03C
R03A
R03B
R04A
Q01C
Q01B
Q01A
R01A
R04B
R04C
R01C
R02C
R05C
R07C
CR03C
CR02C
CR01C
R01B
R02B
CR03B
CR02B
CR01B
R07B
R01B
R07A
CR03A
CR02A
CR01A
CARD OQA
PIN 1

COMPARATOR AND READOUT

ORA

The ORA is specifically designed for large usage in optical reading machines using the map-matching principle to determine closest comparison to a set of ideal characters prewired in the form of a resistor matrix to a large flip-flop register. The flip-flop register represents the dark and light squares of the character area being optically scanned. The input to each ORA card is a varying analog signal from one output of a large resistor matrix. The ORA card charges its internal storage capacitor with the peak negative excursion of the analog input during an externally controlled time period. At the end of the period, the peak voltages stored in many ORA cards are probed and compared with each other. The ORA card with the most negative voltage stored causes a simplified flip-flop to be set in its output circuit. Flip-flops in other ORA cards normally remain unset, but if two ORA cards have closely equal voltages stored, both may be set. If two are set, a "doubles" circuit connected externally to the negative-going side of the ORA flip-flop monitors this undesired condition to denote a reject. The output flip-flop of each ORA card has five outputs on the side that approaches ground when set. Typically the flip-flop output diodes are used to encode a binary character which thus identifies the ORA card that has the largest negative voltage.

As soon as the probe and readout of the capacitors is completed and the flip-flop set, the internal storage capacitor may be cleared to look for a peak in the next time period. The flip-flop in the output circuit need not be cleared until just prior to the next time the capacitor voltages of the ORA cards are to be probed and compared.

Circuit operation is as follows. An analog signal swinging on both sides of -6v over a maximum range from 0 to -12v is applied to pin 1 and connected to emitter follower Q01. The peak negative excursions are used to charge C01 in a negative direction through CR03. The negative charge on C01 is retained by back-biasing CR02 during this period with a voltage at least 12 volts negative applied to pin 2. Pin 3 is also logically connected to a voltage near ground during this period to prevent R14 from charging the capacitor to more than about

-6v. R01 limits the steady state dissipation of Q01, and C02 stores energy to supply peak current during fast charging of C01. During this time, Q02 is also disconnected logically from the circuit by holding pin 4 at least 12 volts negative.

When the time period allowing C01 to charge on all ORA cards is completed, the comparison of the charge on C01 for all ORA's may then begin. This is accomplished by allowing pin 3 to go negative. This causes C01 to charge toward -20v at a slow rate determined by the time constant of R14, R15, and C01. Thus the voltage at the base of Q02 will be determined by the previous charge on C01 and the drop across CR03 and R15. R15 is selected to compensate for differences in the sum of base to emitter drops of Q01 and Q02 to provide better uniformity between ORA cards. Since CR03 is forward biased during charge of the capacitor as well as during readout, use of a high conductance diode eliminates most of the problem of variations of CR03 on different cards.

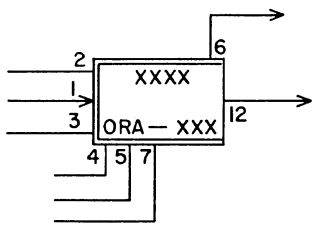
Pin 4 of all ORA cards is connected to a bus which is driven in the positive direction by an external current source. Thus, whichever ORA card has the most negative voltage at the emitter of Q02 when biased forward will hog all the current available from the bus with the constant current source. This will cause collector current to flow in the collector of Q02 of this ORA causing a voltage drop across R04, which will normally cause the base of Q04 to be more positive than the level reference on pin 5. This causes Q03 to turn off and Q04 to turn on. Normally pin 5 has a reference voltage that requires only 30-45 percent of the current available from the constant current source to turn Q04 on.

Q05 and Q06 are connected as a flip-flop. Assuming a clear pulse (pin 7 momentarily driven to near ground) had been applied, Q06 would be conducting and Q05 nonconducting. When Q04 turnon current equals 1-2 ma, this will cause Q05 to also turn on to put the flip-flop in its "set" state (TP-C near ground). Output pins 8-12 have normal logic levels for standard inverter signals. Output pin 6 is used in an external "doubles" circuit where pin 6 of all ORA cards are connected to a load terminated at ground. R11 limits the drive current in the negative direction. Thus if two or more ORA cards have their flip-flops set, the pin 6 bus will become sufficiently more negative so that an

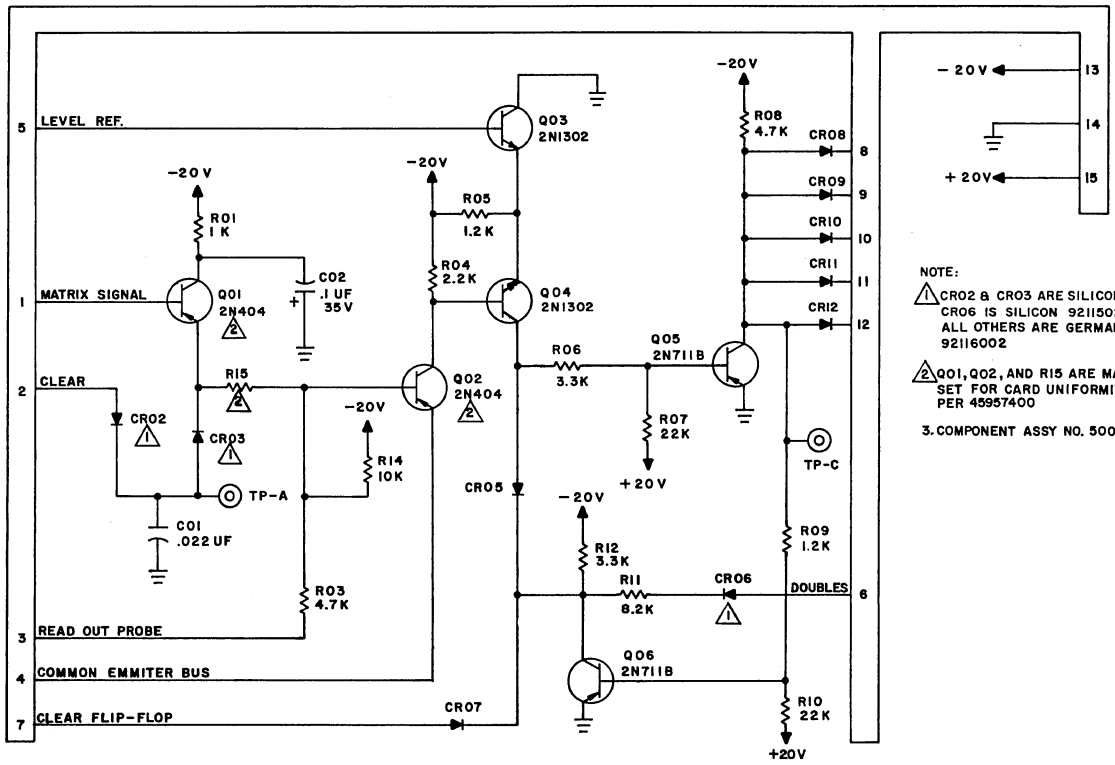
external quantizing circuit can easily detect the undesired condition which indicates two closely equal peak analog voltages.

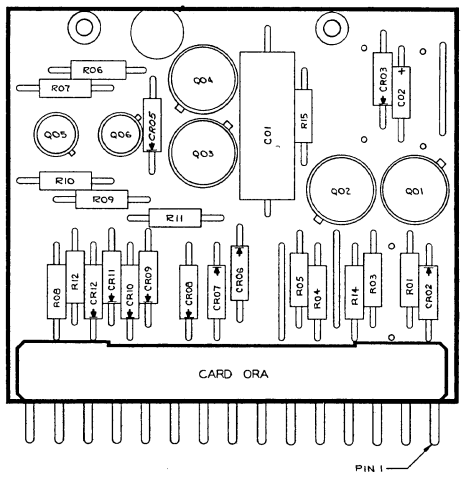
Certain considerations should be observed in use of the ORA circuit. The peak storage circuit ability to follow the input signal without excessive loading depends on both impedance and rate of change of the input. As an example, a 3v step function with 1K impedance requires 2.5 usec to charge to peak value. The rate at which the constant current source is applied during comparator readout can create a problem when the common emitter bus becomes long, so it should be slowly increased over at least 1 microsecond. The bias between the peak input signal and the common emitter readout changes with operating temperature. If all cards are at nearly the same temperature, as they should be, this will cause the temperature offset to be nearly equal on all ORA cards and not affect accuracy to a significant extent.

SYMBOL



COMPARATOR READOUT ORA





INPUT AMPLIFIER
OSA, OSB

The OSA input amplifier card was initially designed for use on time shared lines between 601 tape units and a 601 synchronizer. The input is designed for signal excursions from 0 to +2v. It's output matches standard logic signals (0 to -3v). Original application utilizes 4 or less OSA circuits on standard 24 pin I/O lines of 100 ft. maximum length (23 twisted pairs on a common ground reference). The input circuit is designed for use in conjunction with circuits such as the IS.. series output amplifiers or the ITA pulse delay and output amplifier. Loading of the line signal is minimized to permit several OSA input amplifiers to be paralleled whether their power supply voltages are present or absent.

Each of the three circuits function as follows. Q01 acts as an emitter follower to reduce line loading. Input switching threshold is 1.0 $\pm$ .2v and is determined by combining silicon and germanium semiconductor drops as follows.

$$(V_{BE} \text{ of } Q01) + (V_{fwd} \text{ of } CR01) - (V_{BE} \text{ of } Q02).$$

Q02 acts as an inverting circuit to drive three output diodes available for AND terms.

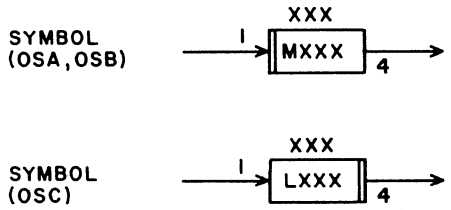
The OSA circuit includes power supply disconnect features to minimize loading to ground when voltages are not present. With +20v voltage off, the base to collector diode in Q01 cannot load to ground because of CR07 in the +3v network. With -20v voltage off, diode CR05 prevents R02 from loading to ground.

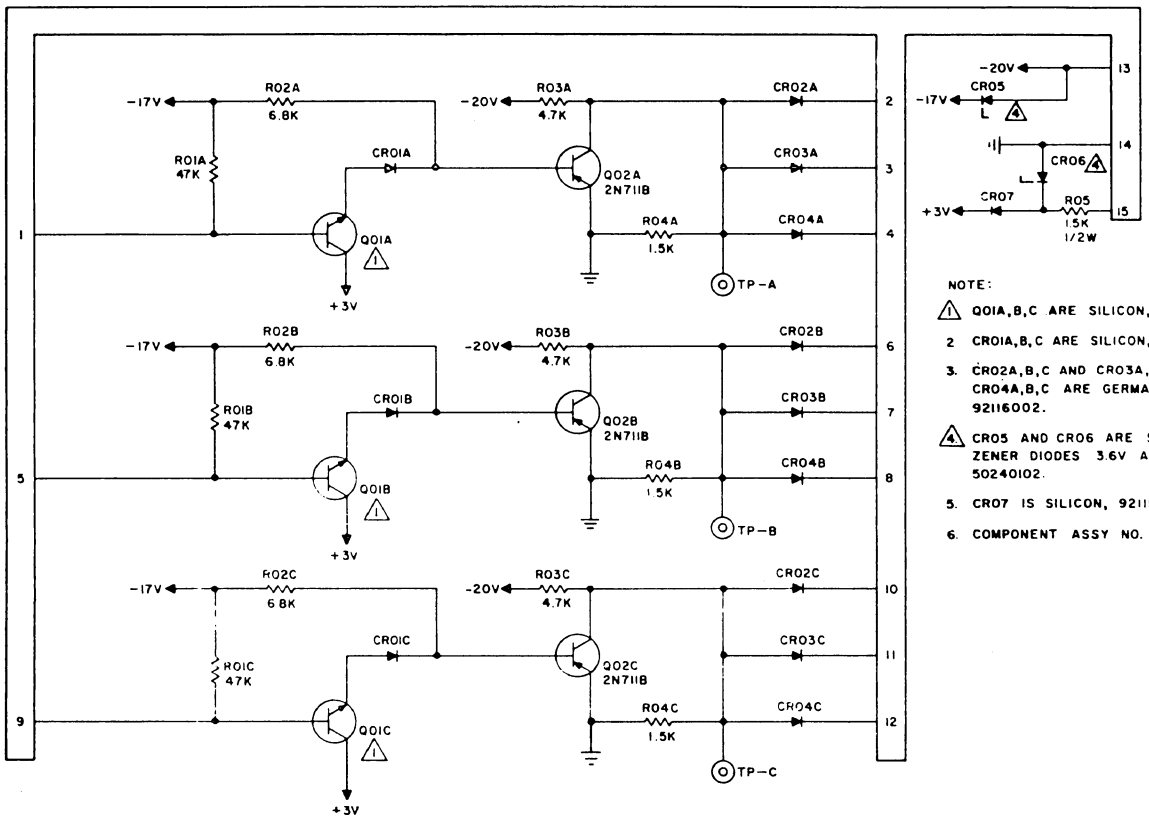
Signal polarity is as follows: A +2v input provides a logic "1" output (-4v min). A 0v input provides a logic "0" output (-3/4v). Switching time after the input signal is outside the threshold region (+0.8 to +1.2v) is 150 nanoseconds or less in both directions. The number of OSA input amplifiers paralleled depends on the margin of input signal provided as regards driving source, line attenuation, crosstalk and other related factors. Each OSA circuit can be expected to bias the line about 30 mv negative with 120 ohm terminations at both ends of a line.

The OSB circuit is the same as the OSA as regards signal level conversion but is designed for use where a receiver is at one end of a line and it is undesirable to use a separate 120 ohm terminating resistor external to the card. The OSB does not incorporate the power supply disconnect features of the OSA circuit. It should therefore have its power supply on if OSA or similar circuits are to be active in receiving signals on the same line.

OUTPUT AMPLIFIER
OSC

The OSC circuit is specifically designed to interface from Bell Telephone Lab line signals (approximately 0 to +3v) to standard logic signals (-0.5 to -3v) on a non party line configuration using a 100 ohm coax cable. When -3v is applied as an input to the card a +3v output is produced. The only difference schematically from the OSB is the use of a 100 ohm terminating resistor (R01) instead of 120 ohms at the input of each of the three circuits. The switching point and propagation times are equivalent to that of the OSA circuits

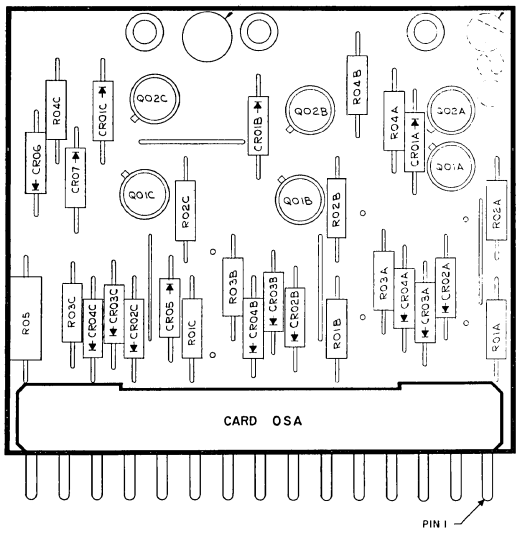


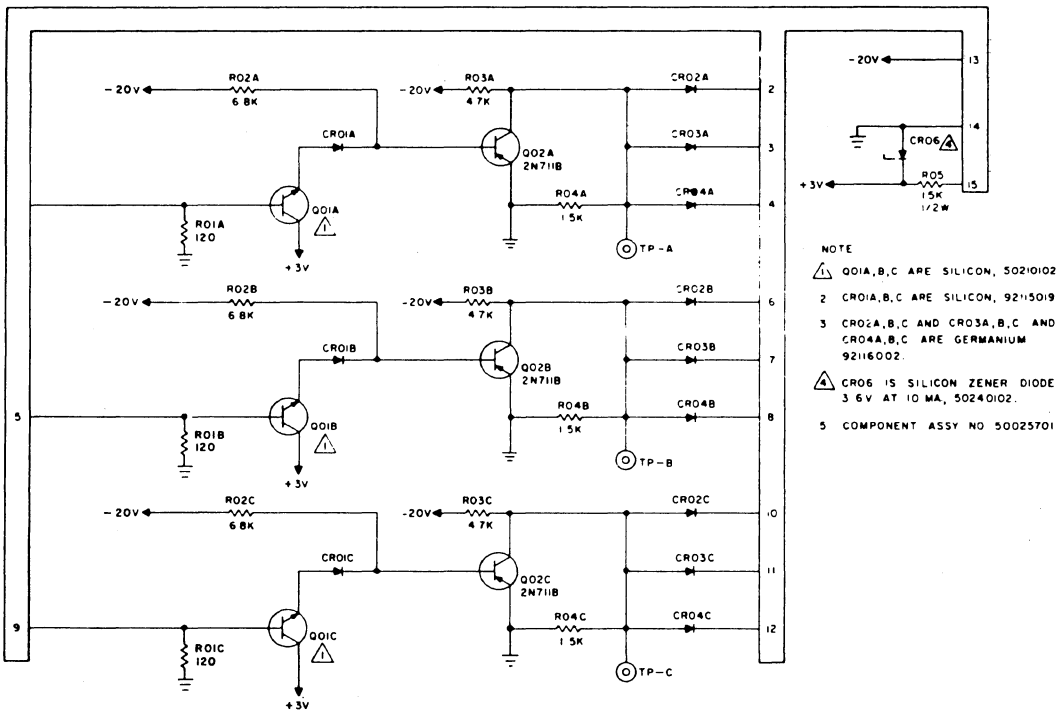


NOTE:

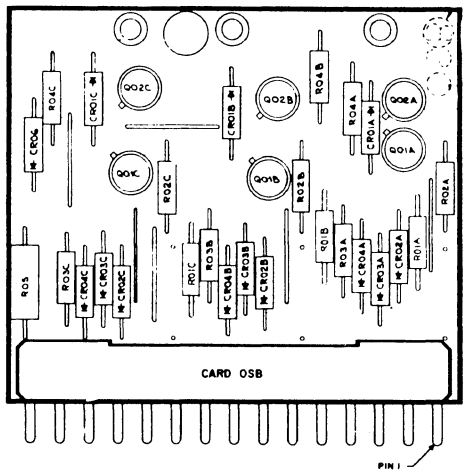
1. QOIA,B,C ARE SILICON, 50210102.
2. CROIA,B,C ARE SILICON, 92115019
3. CR02A,B,C AND CR03A,B,C AND CR04A,B,C ARE GERMANIUM 92116002.
4. CR05 AND CR06 ARE SILICON ZENER DIODES 3.6V AT 10 MA, 50240102.
5. CR07 IS SILICON, 92115021.
6. COMPONENT ASSY NO. 50025700.

OSA




-20V
R02A
6.8K
R03A
4.7K
CR02A
CR01A
Q02A
2N711B
CR03A
R04A
1.5K
CR04A
Q01A
R01A
120
+3V
TP-A
R02B
6.8K
R03B
4.7K
CR02B
CR01B
Q02B
2N711B
CR03B
R04B
1.5K
CR04B
Q01B
R01B
120
TP-B
R02C
6.8K
R03C
4.7K
CR02C
CR01C
Q02C
2N711B
CR03C
R04C
1.5K
CR04C
Q01C
R01C
120
TP-C
CR06
R05
1.5K
1/2W
NOTE
1 Q01A,B,C ARE SILICON, 50210102
2 CR01A,B,C ARE SILICON, 92115019
3 CR02A,B,C AND CR03A,B,C AND CR04A,B,C ARE GERMANIUM 92116002.
4 CR06 IS SILICON ZENER DIODE 3.6V AT 10 MA, 50240102.
5 COMPONENT ASSY NO 50025701

OSB, OSC


CARD OSB
PIN 1

LEVEL SWITCH

OTA

The OTA card is used in the disk file servo actuator. The circuit performs the function of switching the system between coarse and fine (long stroke and short stroke) control modes, when the long stroke signal gets near the trigger level.

The input at pin 1 can be driven between plus and minus 10 volts. The output line at pin 12 has standard logic levels. The plus or minus trigger levels can be set between approximately 50 and 400mv by potentiometers R03 and R05.

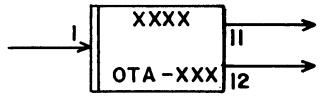
The circuit consists of two similar channels. The one for positive inputs consists of transistors Q02, Q04, and Q06. The one for negative inputs consists of transistors Q01, Q03, and Q05.

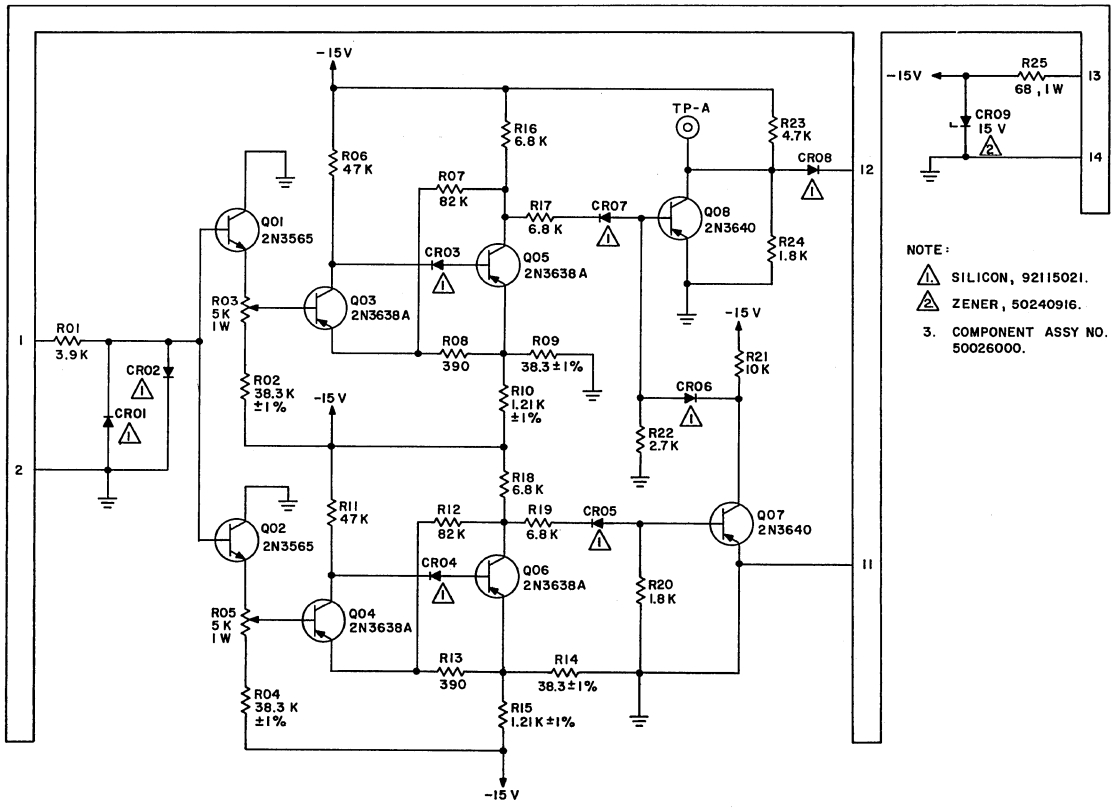
Assuming the trigger levels are set at approximately $\pm$50mv, if the input is within this range transistor Q03 is adjusted by R03 turning it off, and Q04 is adjusted by R05 turning it on. Transistor Q06 is then off, and Q05 and Q07 are on. There is no base drive for Q08, so it is off and the output is at logical "1".

If the input exceeds the trigger level, the output will be at logical "0". Assuming a positive input, Q02 is driven so its emitter goes positive. This turns off Q04 and allows Q06 to turn on. Transistors Q04 and Q06 form a Schmitt trigger circuit. With Q06 turned on, its collector is near ground, so transistor Q07 goes off allowing its collector to go negative. During this time no change occurs in the states of transistors Q03 and Q05. Although Q05 tends to hold the base of Q08 at ground, diode CR07 opens, so the base of Q08 is driven on by Q07's being off. Therefore, transistor Q08 turns on and grounds the output to give a logical "0".

If the input goes negative above the trigger level, the emitters of Q01 and Q02 go more negative tending to turn on Q03 and Q04. Stages with Q05 and Q06 will both be off at this time. Transistor Q07 will now be on since the collector of Q06 is negative (approximately -7.5v). However, since Q05 is also off and its collector is also approximately -7.5v, Q08 will be driven on and the output is again at ground (logical "0"). Diode CR06 becomes back biased, so the on state of Q07 does not take base drive away from Q08.

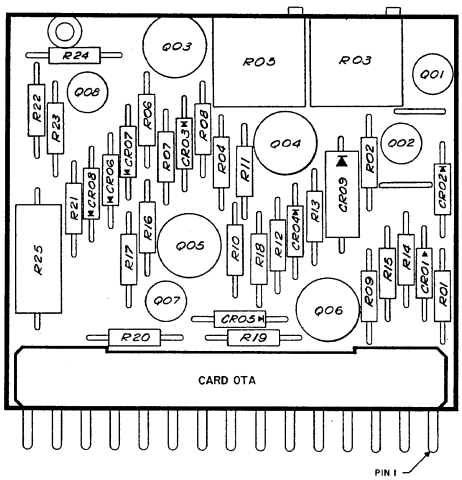
SYMBOL





NOTE:

1. SILICON, 92115021.
2. ZENER, 50240916.
3. COMPONENT ASSY NO. 50026000.



SCHMITT TRIGGER

OUA

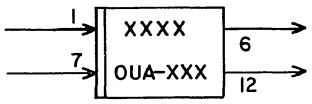
This circuit is used in the temperature servo for the disc file. It is used to indicate when the temperature in the file exceeds certain limits from the control temperature. There are two identical circuits per card.

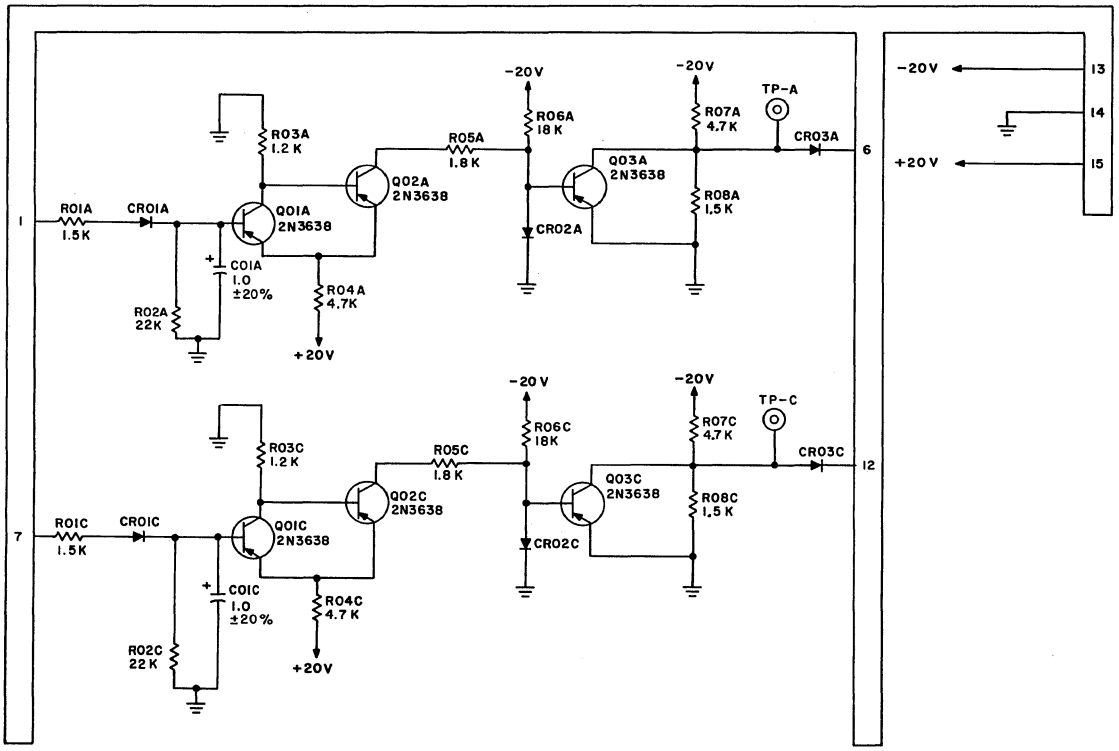
With the input voltage less than approximately +2.5v, transistor Q01 is on and Q02 is off, allowing Q03 to be on. The output is then at a logic "0" (-0.5v).

If the input voltage rises to about +3.5 volts, Q01 will turn off and Q02 goes on. This action removes the base drive to Q03, so it goes off and the output becomes a logic "1" (-3v).

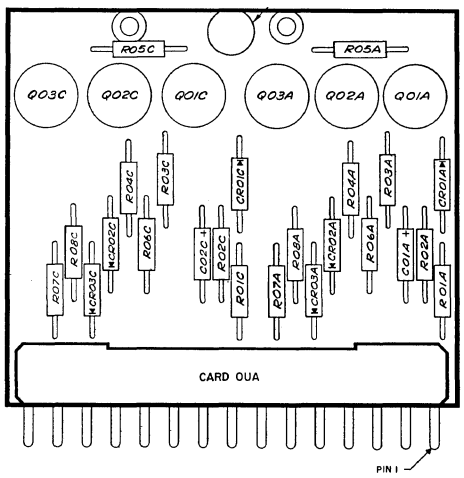
This card (at logic "0") will handle a load of 20 ma, but in this application is only approximately 3 ma.

SYMBOL




-20V
13
14
+20V
15
TP-A
TP-C
R03A
1.2 K
R05A
1.8 K
R06A
18K
R07A
4.7K
CR03A
6
Q02A
2N3638
Q03A
2N3638
R08A
1.5K
CR02A
1
R01A
1.5K
CR01A
Q01A
2N3638
C01A
1.0
±20%
R02A
22K
R04A
4.7K
+20V
R03C
1.2K
R05C
1.8 K
R06C
18K
R07C
4.7K
CR03C
12
Q02C
2N3638
Q03C
2N3638
R08C
1.5 K
CR02C
7
R01C
1.5K
CR01C
Q01C
2N3638
C01C
1.0
±20%
R04C
4.7 K
R02C
22 K

OUA


R05C
R05A
Q03C
Q02C
Q01C
Q03A
Q02A
Q01A
CARD OUA
PIN 1

GATED PULSE SHAPER
OVA, OVB

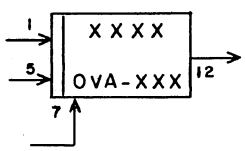
These circuits are designed to produce a nominal 210-nsec in the OVA (150 nsec in the OVB) 1604 logic level pulse for each switchover of differential input level. The input is a differential 0.7-volt signal switching about a bias level of +8 volts provided by an EW- circuit. The circuits are designed for a maximum nominal input signal repetition rate of 1.25 MHz. The output can be gated on or off with a logic level signal.

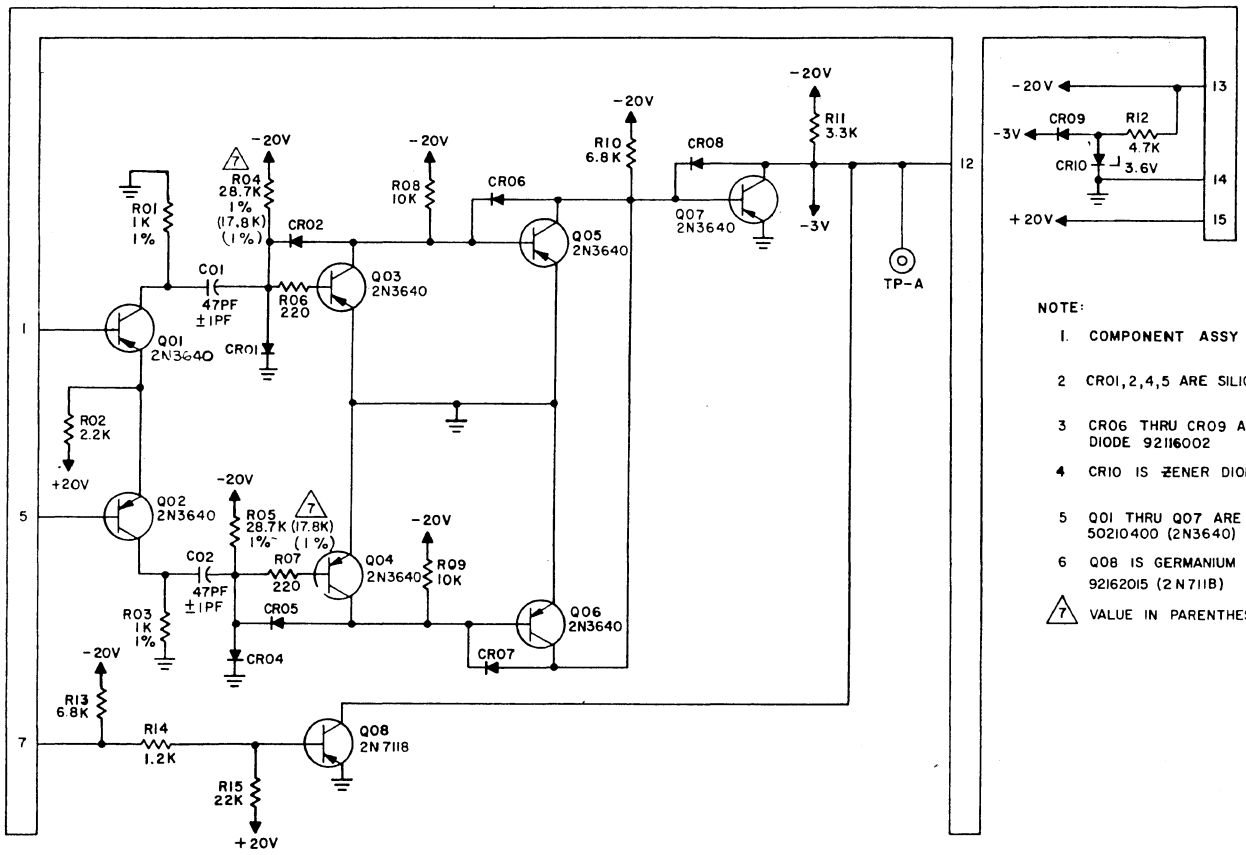
Pins 1 and 5 are the differential input pins with the output at pin 12. Pin 7 is the gate input.

With an EW- Series card providing the signal and the bias for Q01 and Q02, the common emitters are held at approximately +9 volts. The transistor whose base is swinging negative (assume Q01) will be turning on while the other turns off. The collector of Q01 then goes positive to +5 volts (determined by emitter resistor value). This positive going transition is coupled by C01 into the base circuitry of Q03, turning it off. CR01 clamps the pulse height and C01, R01, and R04 determine the off time of Q03, and hence the pulse width appearing at the collector of Q03. The other side of the circuit (i.e., Q02, Q04, etc.), functions in an identical manner to that described above. Q05 and Q06 then are simply inversions which are necessary to properly OR these pulses to a common output via Q07. The pulse widths should be 210 nsec $\pm$ 10% (150 nsec in the OVB). When the output goes negative, it is clamped to a -3.6-volt zener, which produces a better negative going transition than hold-down resistors.

CR06, CR07, and CR08 are germanium anti-saturation diodes. CR02 and CR05 are silicon anti-saturation diodes used in conjunction with R06 and R07 to keep Q03 and Q04 out of saturation.

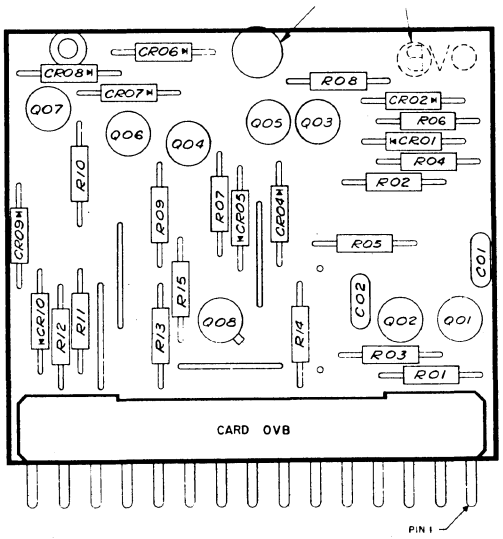
The output can be gated on or off by means of a logic signal into pin 7. A "1" (-3v) will turn Q08 on, which holds the output (pin 12) at a constant "0". A "0" (0v) input will turn Q08 off, permitting a pulse output at pin 12.





NOTE:

1. COMPONENT ASSY NO. 0VA50026600
   0VB50026601
2. CR01,2,4,5 ARE SILICON DIODE 92115021.
3. CR06 THRU CR09 ARE GERMANIUM DIODE 92116002
4. CR10 IS ZENER DIODE 50240102
5. Q01 THRU Q07 ARE SILICON TRANSISTOR 50210400 (2N3640)
6. Q08 IS GERMANIUM TRANSISTOR 92162015 (2N711B)
7. VALUE IN PARENTHESIS ARE FOR 0VB



VOLTAGE SENSOR

OWB

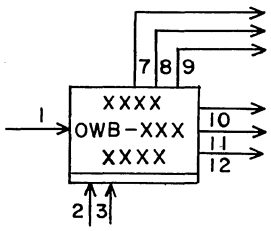
The OWB card senses the disk storage drive units + and - 20v terminator voltages and is used to prevent the carriage from hitting the stops due to a loss of either of the terminator voltages. The circuit is also capable of providing an output pulse if the primary AC voltage source (to the drive unit) fails.

A logical input enters pin 1, +20v is applied to pin 2, and -20v to pin 3. Transistors Q01, 03 and 04 form a positive AND or a negative OR function such that if these transistors are OFF due to normal inputs on pins 1, 2, and 3, the voltage at TPB is a logical "1" and at TPC a logical "0". If any input fault* occurs, the state of TPB and TPC change.

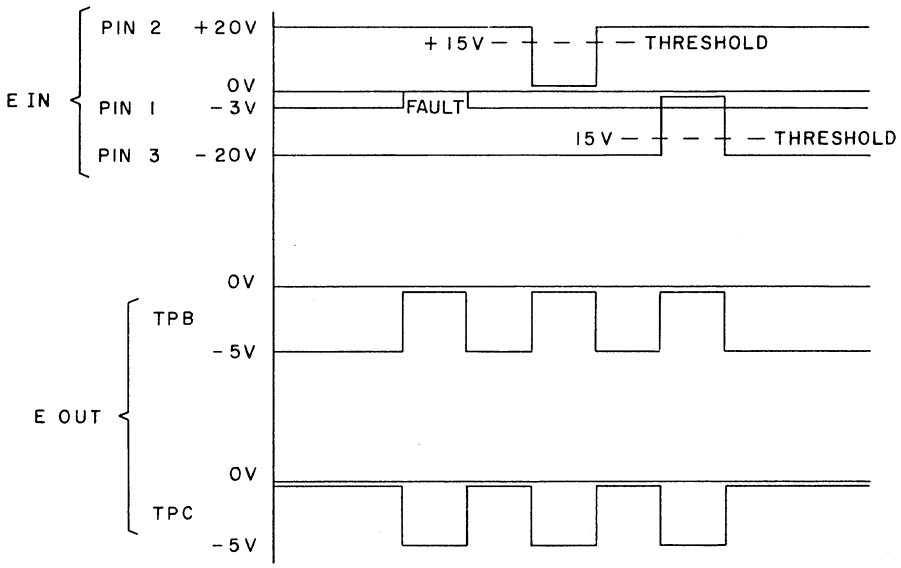
With normal inputs on pins 1, 2, and 3, transistor Q01 is OFF due to the divider action of R01, R02, and CR01, 2, and 3. This causes the junction of R03, 4, and 5 to be at +5v nominally, which drives Q02 ON and Q03 OFF; the junction of R07, R15 is -5v nominally and Q04 is held OFF.

With Q01, 3, and 4 OFF, the divider action of R08, 9, 14 and CR06 cause TPA to be at +2.4v and Q05 to be turned OFF. This causes TPB to go to -4.9v and Q06 to turn ON; TPC goes to ground. Any fault causes TPA to go to ground; CR06 becomes back biased as current is pulled through Q05 causing TPB to go to 0v and TPC to become -4.9v.

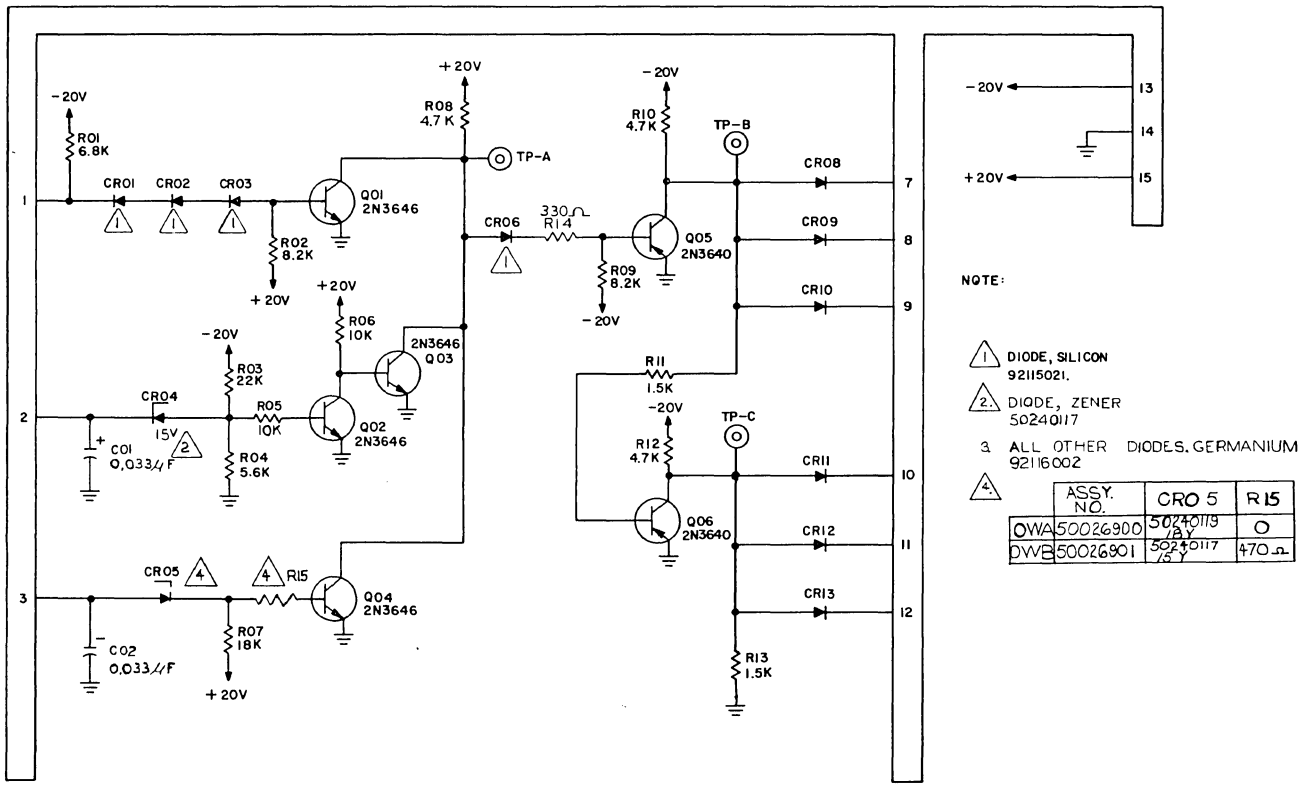
The accompanying figure indicates typical waveforms and is furnished for reference purposes only.



* A Fault is a logical "0" on pin 1, approximately +15v on pin 2, or approximately -15v on pin 3.



TYPICAL WAVEFORMS

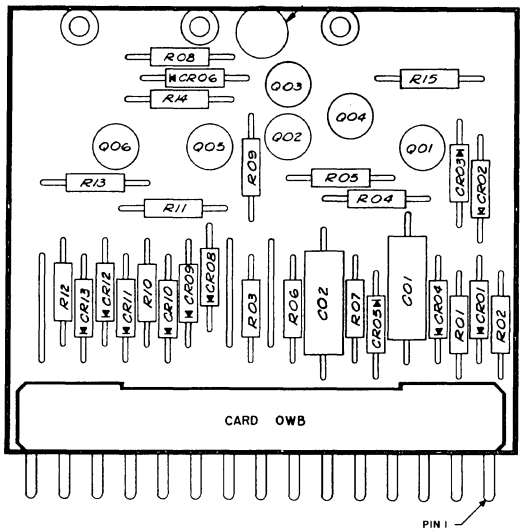


NOTE:

1. DIODE, SILICON 92115021.
2. DIODE, ZENER 50240117
3. ALL OTHER DIODES. GERMANIUM 92116002
4.

ASSY. NO.	CR05	R15
OWA 50026900	50240119 /BY	0
OWB 50026901	50240117 /5Y	470Ω

OWB



INPUT AMPLIFIER
OYA

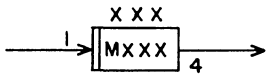
The input amplifier card OYA is used to interface between equipment operating with excursions of -12v to -1v and standard logic signals (0v to -3v).

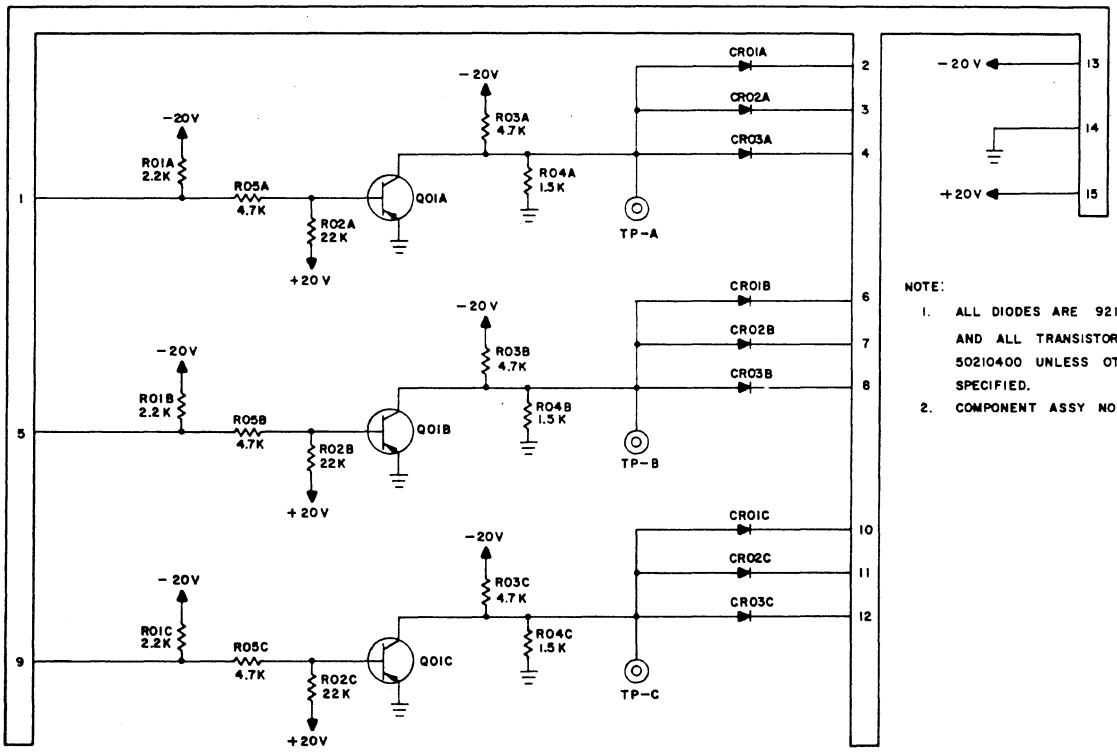
Each OYA card has three identical circuits. The circuit converts a -12v signal input to a "0" (-0.5v) logic signal output and a -1v signal input to a "1" (-3v) logic signal output.

With a -12v input, the emitter-base of Q01 will forward biased and Q01 will turn on. R05 is chosen so that Q01 will switch when the input signal is at a nominal -6v. Q01 is then in a saturated state capable of providing 12 ma at about -0.5v. With a -1v input, the emitter-base of Q01 will be back biased and Q01 will turn off. Voltage divider R03 and R04 then determine the "1" output voltage.

Each circuit represents a load of about 10 ma when the input is held to ground. The threshold point of the circuit is at -6v $\pm$ 1.5v. Output diodes CR01, CR02 and CR03 provide for AND terms if required.

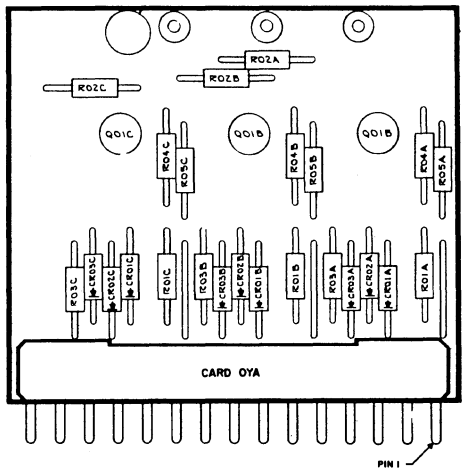
SYMBOL





NOTE:

1. ALL DIODES ARE 92116002 AND ALL TRANSISTORS ARE 50210400 UNLESS OTHERWISE SPECIFIED.
2. COMPONENT ASSY NO. 50027500.



DUAL LINE RECEIVERS
PJA, PJB

The PJA card is a balanced-line receiver designed as a pin-interchangeable, interim replacement for the P16A receiver. It is basically a minimal revision to the P16A that increases the common-mode input capability from -2.5v to -4.5v and from +4.5v to +7v.

The PJB card is a pin-interchangeable, performance-improved replacement for the P16 series and the PJA receiver. Its principal improvement is an increase in the tolerable amount of common mode signal (headroom) to $\pm$8v. The PJB card is also less susceptible to power supply variations.

PJA

The differential signal is applied to the bases of Q1 and Q2, which function as a PNP differential amplifier over a range of input signals between -5v and +8v. One collector is normally OFF and the other is normally ON. The collector signal of Q1 is fed through a voltage divider to the base of Q3. Transistor Q3 (without a saturation-limiting diode) functions as a logic-state output stage.

Resistors R1 and R2 terminate the input stages to ground when no input signals are present. The collector of Q2 is returned to a network which is equivalent to about 510 ohms at -8v (statically). Capacitor C1 reduces the ac impedance encountered by the collector during switching operations.

In the output stage, the input divider (R8 and R9) serves two purposes: 1) it shifts the dc level of the previous stage; 2) in combination with the feedback diode (CR1) at the collector of Q3, it clamps the negative excursion of the output at approximately -5v. Four output diodes (in each of the two circuits) are provided for signal fan-out to AND terms.

Propagation delay through the circuit (measured from 0v input to -2v output) is from 20 nsec to 40 nsec in the direction of a "1" output and 22 nsec to 42 nsec in the direction of a "0". Input rise and fall times for these propagations do not exceed 40 nsec within the range of 10% to 90%.

PJB

The differential input signal is applied to the bases of Q1 and Q2, which function as a PNP differential amplifier over a range of input singals from -8v to +8v. One collector output of either Q1 or Q2 is normally OFF and the other is ON. A second NPN differential amplifier stage (Q3 and Q4) amplifies and changes the outputs to a switching signal at either above or below ground. Silicon transistor Q5 functions as a logic-state output stage, with no saturation-limiting diode included.

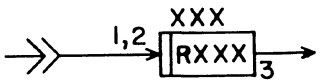
Resistors R1 and R2 terminate the input stages to ground when input signals are absent, but they still represent a relatively minor loading of the input provided the common mode component of the signal is also near 0v. Base resistors R12 and R13 minimize the ac loading of the input stage, particularly at the threshold switching point (0v differential) of the input stage. Resistor R3 is the current source for the input differential stage.

A divider (R4 and R7), together with the voltage drop across resistors R5 and R6, determines the base voltage at Q3 and Q4. This base voltage, along with the value of R8, determines the current flow through either Q3 or Q4. There must be enough current flow to turn on Q5 should there be a common mode input signal of +8v. Resistor R10 provides negative feedback and, together with V_{BE} of Q5 and the value of R9, determines the negative output excursion. Propagation delay through the circuit (measured from 0v input to -2v output) is normally from 22 to 42 nsec in the direction of a "1" output and from 10 to 25 nsec in the direction of a "0" output.

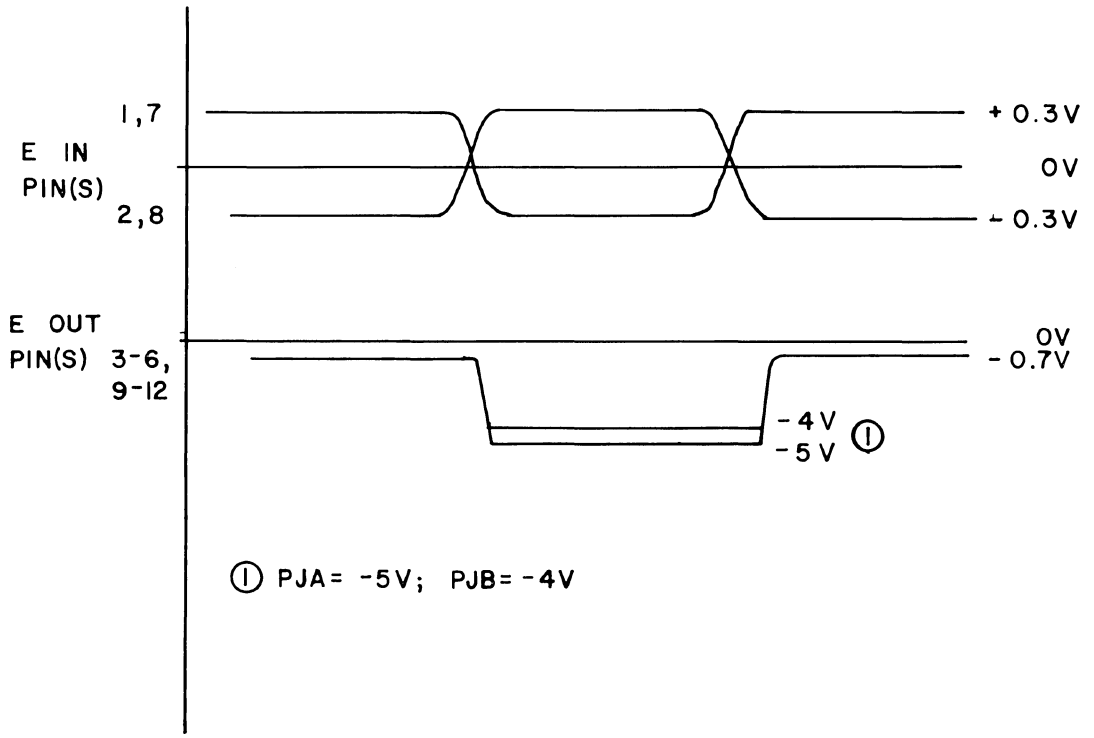
The switching threshold of the amplifier is within $\pm$0.1v of the differential input. If the input level is near $\pm$0.1v and some of the output signal is coupled back to the input, enough gain may exist at the switching threshold to cause oscillation. It is important, therefore, that caution be exercised to prevent the output of this circuit, or other circuits, from being ac coupled back to the input.

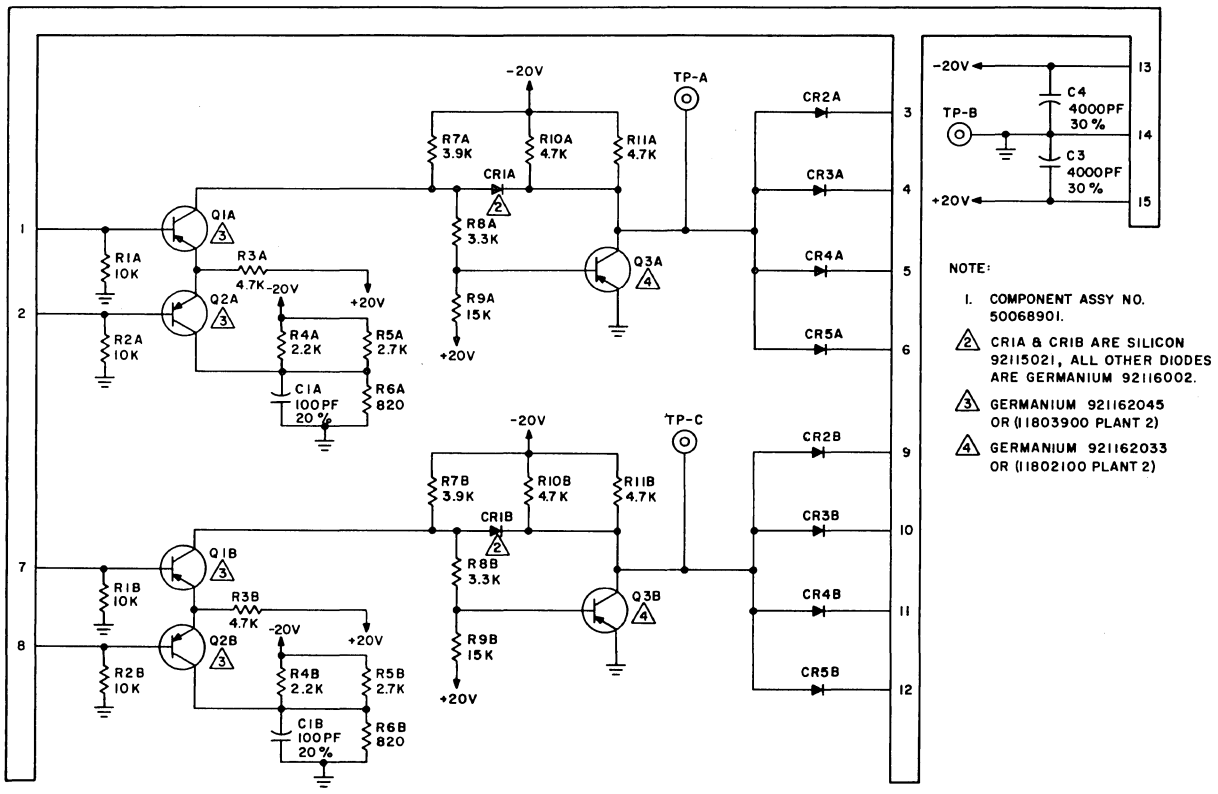
Four output diodes (in each of the two circuits) are provided for signal fanout to AND terms.

Typical waveforms for the cards are shown below.

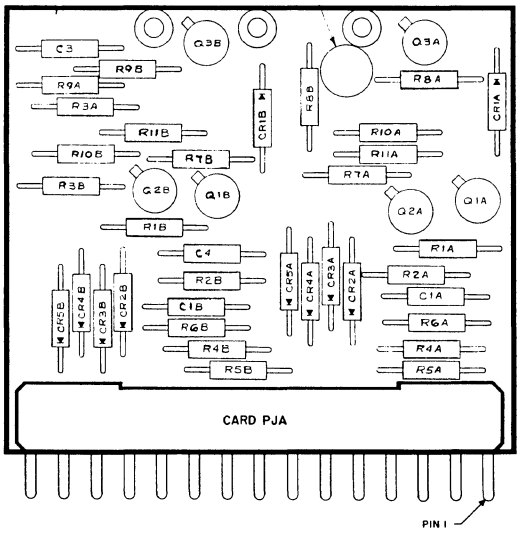


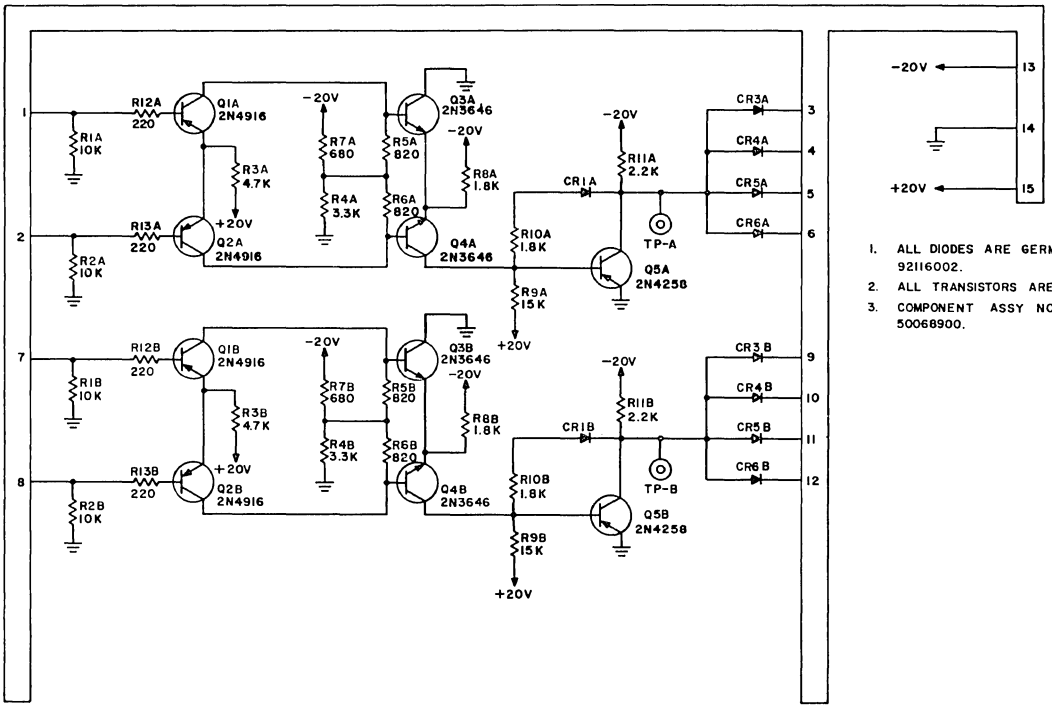
WAVEFORMS:




-20V
TP-A
CR2A
R7A 3.9K
R10A 4.7K
R11A 4.7K
CR1A
CR3A
Q1A
R8A 3.3K
R3A 4.7K
Q3A
CR4A
R1A 10K
Q2A
R9A 15K
+20V
R4A 2.2K
R5A 2.7K
CR5A
R2A 10K
C1A 100PF 20%
R6A 820
-20V
TP-C
CR2B
R7B 3.9K
R10B 4.7K
R11B 4.7K
CR1B
CR3B
Q1B
R8B 3.3K
R3B 4.7K
Q3B
CR4B
R1B 10K
Q2B
R9B 15K
+20V
R4B 2.2K
R5B 2.7K
CR5B
R2B 10K
C1B 100PF 20%
R6B 820
-20V
C4 4000PF 30%
TP-B
C3 4000PF 30%
+20V
NOTE:
1. COMPONENT ASSY NO. 50068901.
2 CR1A & CR1B ARE SILICON 92115021, ALL OTHER DIODES ARE GERMANIUM 92116002.
3 GERMANIUM 921162045 OR (11803900 PLANT 2)
4 GERMANIUM 921162033 OR (11802100 PLANT 2)

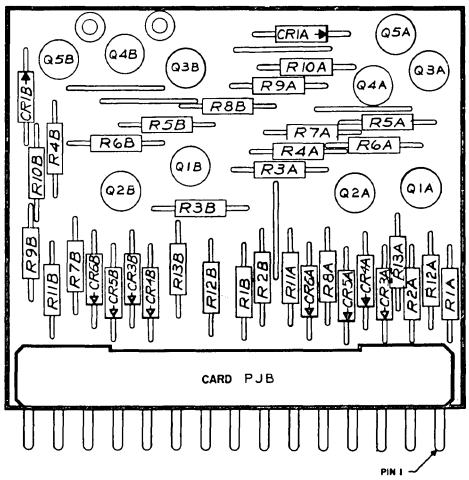
PJA


C3
R9B
R9A
R3A
R11B
R10B
R7B
R3B
R1B
C4
R2B
C1B
R6B
R4B
R5B
CR5B
CR4B
CR3B
CR2B
Q3B
Q2B
Q1B
CR1B
R8B
CR5A
CR4A
CR3A
CR2A
Q3A
R8A
CR1A
R10A
R11A
R7A
Q2A
Q1A
R1A
R2A
C1A
R6A
R4A
R5A
CARD PJA
PIN 1



1. ALL DIODES ARE GERMANIUM 92116002.
2. ALL TRANSISTORS ARE SILICON.
3. COMPONENT ASSY NO. 50068900.

PJB



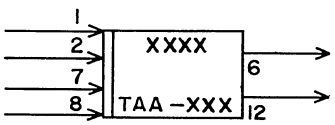
PHOTODIODE AMPLIFIER
TAA

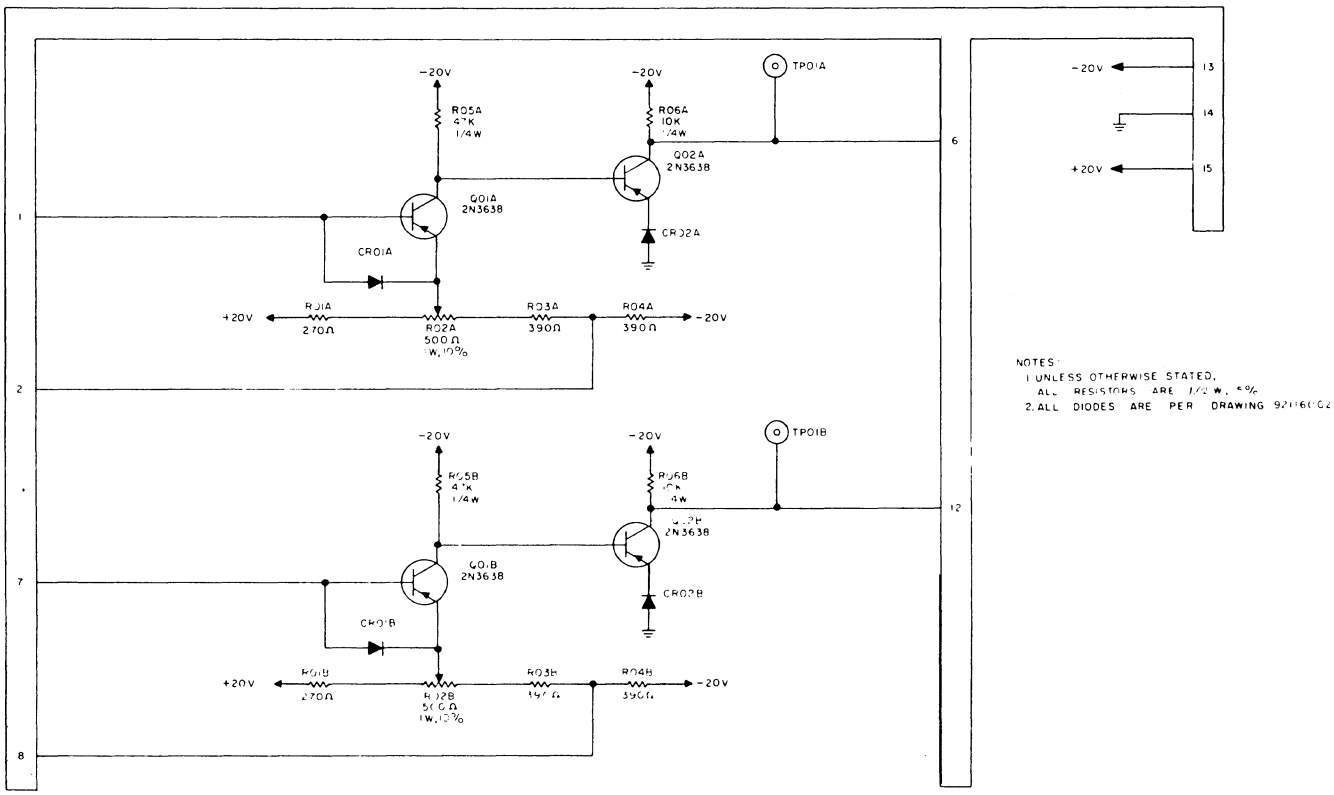
This circuit is designed to compare the light level reaching two photocells. The output is a logical "1" if one cell has more light and a logical "0" if the other cell has more light. The difference in light levels required to cause the output change state can be varied by means of the potentiometer in the circuit.

The photocells are connected in series with the common lead tied to pins 1 and 7. The other leads from the two cells are connected to +20volts and pins 2 and 8 respectively.

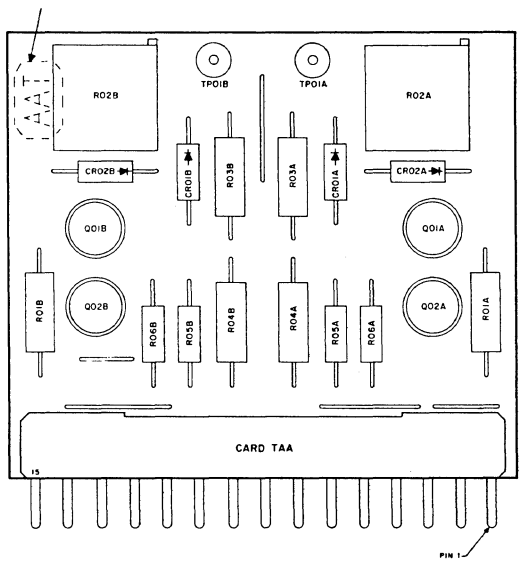
With identical light levels on both cells the potentiometer is adjusted until the output just switches to a logical "1". As the light is reduced on the cell connected between pins 1 and 2 (or 7 and 8), the output will switch to a logical "0". This is the point of most sensitive adjustment.

To reduce the sensitivity return the cells to a balanced light condition, find the point on the potentiometer that causes the output to change state, note the direction that causes a change from "0" to "1" and continue for several turns in this direction.




-20V
R05A
4.7K
1/4W
Q01A
2N3638
CR01A
R01A
270Ω
R02A
500Ω
W, 10%
R03A
390Ω
R04A
390Ω
+20V
-20V
R06A
10K
1/4W
Q02A
2N3638
CR02A
TP01A
R05B
4.7K
1/4W
Q01B
2N3638
CR01B
R01B
270Ω
R02B
500Ω
W, 10%
R03B
R04B
Q02B
CR02B
TP01B
1
2
7
8
6
12
-20V
13
14
+20V
15
NOTES:
1. UNLESS OTHERWISE STATED,
ALL RESISTORS ARE 1/2 W, 5%
2. ALL DIODES ARE PER DRAWING

TAA


R02B
TP01B
TP01A
R02A
CR02B
CR01B
R03B
R03A
CR01A
CR02A
Q01B
Q01A
R01B
Q02B
R06B
R05B
R04B
R04A
R05A
R06A
Q02A
R01A
CARD TAA
15
PIN 1

ADJUSTABLE DELAY

UAA, UAB

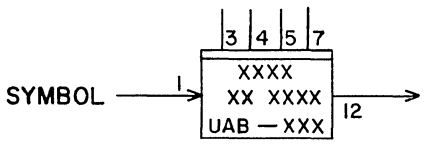
The adjustable delay circuit is noninverting in relation to the input but changes from "1" to "0" are delayed at the output.

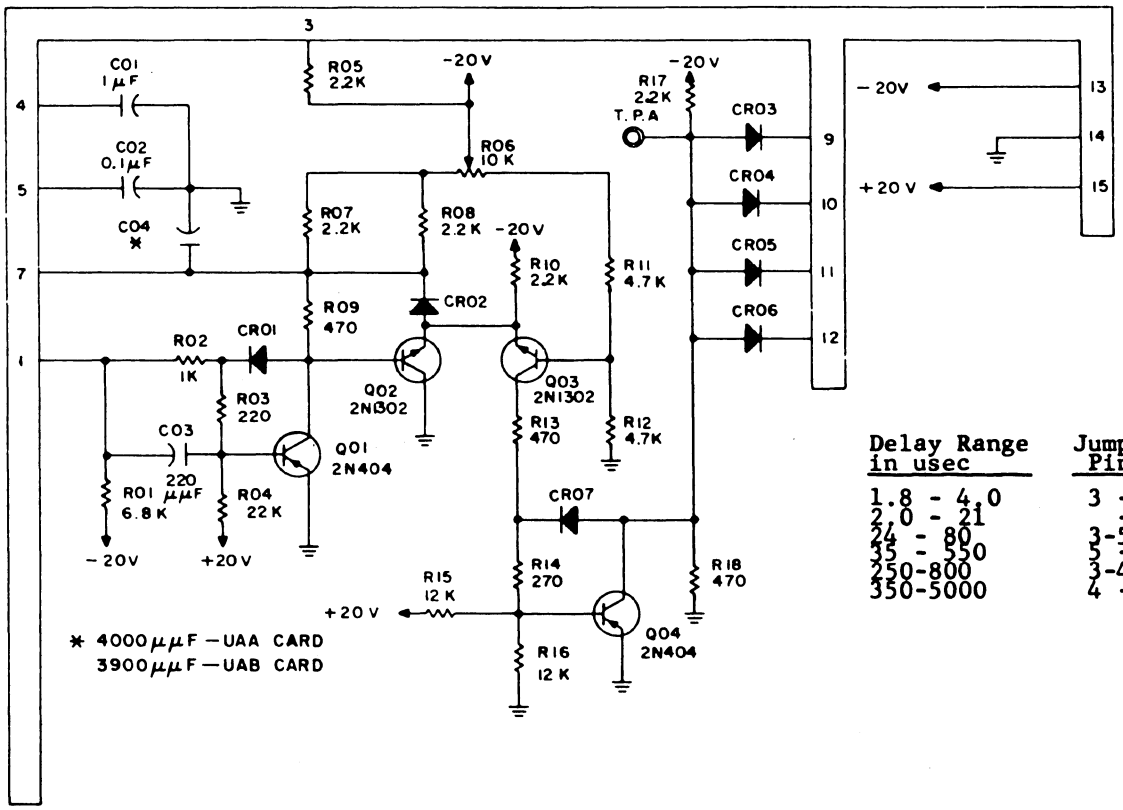
The input stage of the circuit is an inverting circuit with a speed-up diode (CR01) to reduce turnoff time in Q01. The timing circuit is composed of C04, R07, R08, and potentiometer R06. Longer range delays are obtained by paralleling C04 with C01 and/or C02 with external jumpers. A limited delay adjustment may be obtained by paralleling R05 with the charge network (R07, R08, and R06). Some external adjustment may also be obtained by connecting a potentiometer between pins 3 and 7. The UAB card has a temperature stable capacitor, C04, for delays below 25 usec.

Discharge of C04, which recycles the delay, is accomplished by the emitter follower (Q02) in the second stage through diode CR02. Drive to Q02 is determined by the drop across R09 which also provides a small percentage of the current to discharge C04. To provide 98% of the full delay period, a recycle time of 1 usec is required when using C04 alone, 2 usec when C02 is added, and 10 usec when C01 is added.

The third stage is emitter driven to obtain voltage gain and proper bias reference to switch the output stage. The base circuit reference is changed by connecting R06 as a voltage divider. As R06 inserts resistance to increase the RC time constant, it also removes resistance in the base divider of Q03. A greater portion of the RC time constant can be used for long delays. The normal adjustment range of 9 to 1 is extended to approximately 20 to 1.

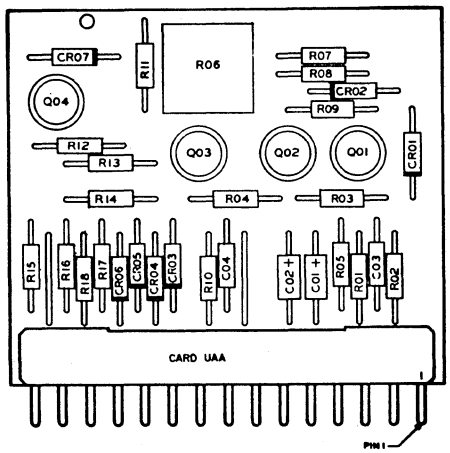
The fourth and final stage, Q04, is an inverter circuit with a saturation limiting diode (CR07) which limits base drive. A divider circuit in the base allows considerable voltage swing to improve turnon time. The output excursions are limited in the negative direction by a resistance divider.

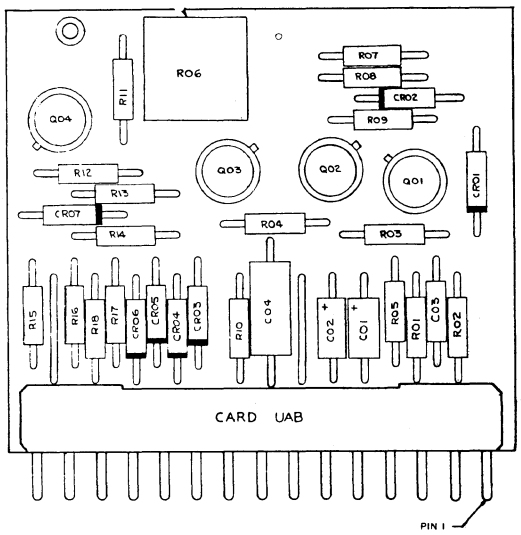




Delay Range in usec	Jumper Pin
1.8 - 4.0	3 - 7
2.0 - 21	-
24 - 80	3-5-7
35 - 350	5 - 7
250-800	3-4-7
350-5000	4 - 7

UAA, UAB





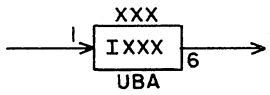
DOUBLE INVERTER

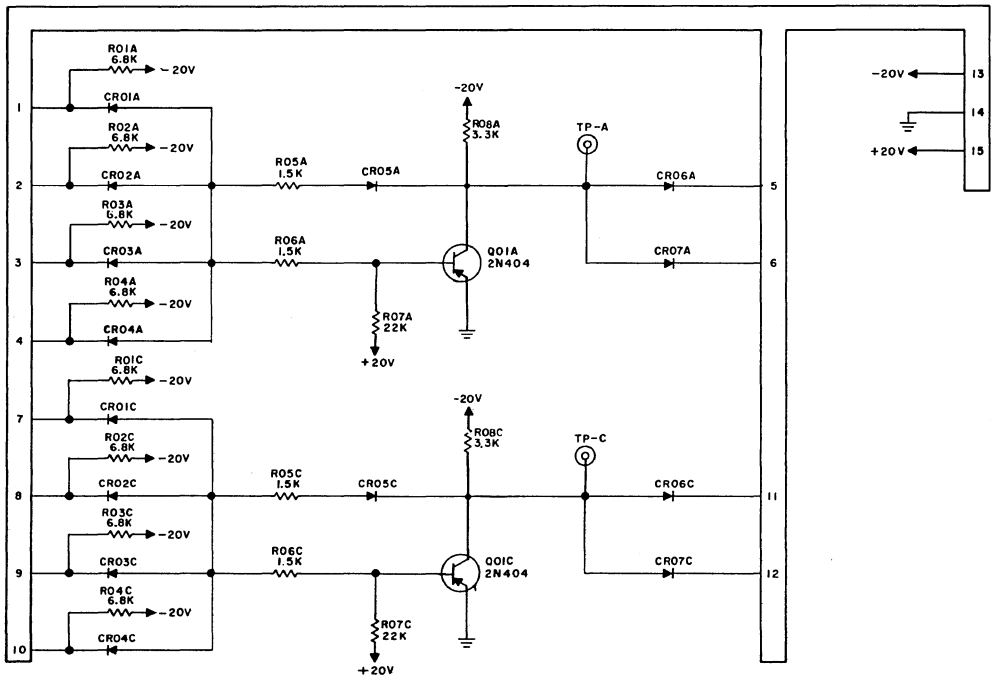
UBA

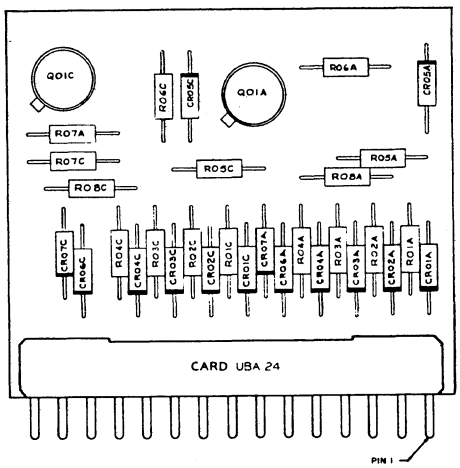
This inverter card was designed for use in the 180 Data Collector where speed requirements could be relaxed to favor low cost. Except for the number of input OR terms and output AND terms, it is the same basic circuit as Control Corporation cards CC-21, CC-22, and CC-23.

Since the newer Computer Division 24A card now closely approaches the cost of the UBA card, the UBA is no longer recommended for new designs in the interest of reducing the number of card types to be handled from a logistics standpoint in production and in the field.

SYMBOL




R01A 6.8K
-20V
CR01A
R02A 6.8K
CR02A
R03A 6.8K
CR03A
R04A 6.8K
CR04A
R01C 6.8K
CR01C
R02C 6.8K
CR02C
R03C 6.8K
CR03C
R04C 6.8K
CR04C
R05A 1.5K
CR05A
R06A 1.5K
R07A 22K
+20V
R08A 3.3K
TP-A
CR06A
CR07A
Q01A 2N404
R05C 1.5K
CR05C
R06C 1.5K
R07C 22K
R08C 3.3K
TP-C
CR06C
CR07C
Q01C 2N404
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15


Q01C
Q01A
R07A
R07C
R08C
R06C
CR05C
R05C
R06A
CR05A
R05A
R08A
CR07C
CR04C
R04C
R01C
CR03C
R03C
CR02C
R02C
R01C
CR07A
CR04A
R04A
R03A
CR03A
R02A
CR02A
R01A
CR01A
CARD UBA 24
PIN 1

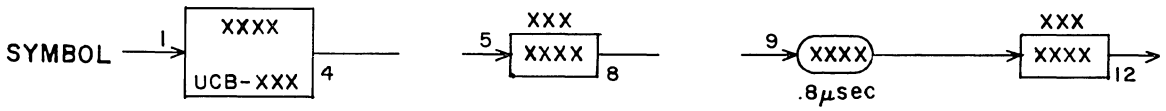
ADJUSTABLE PULSE DELAY
UCB

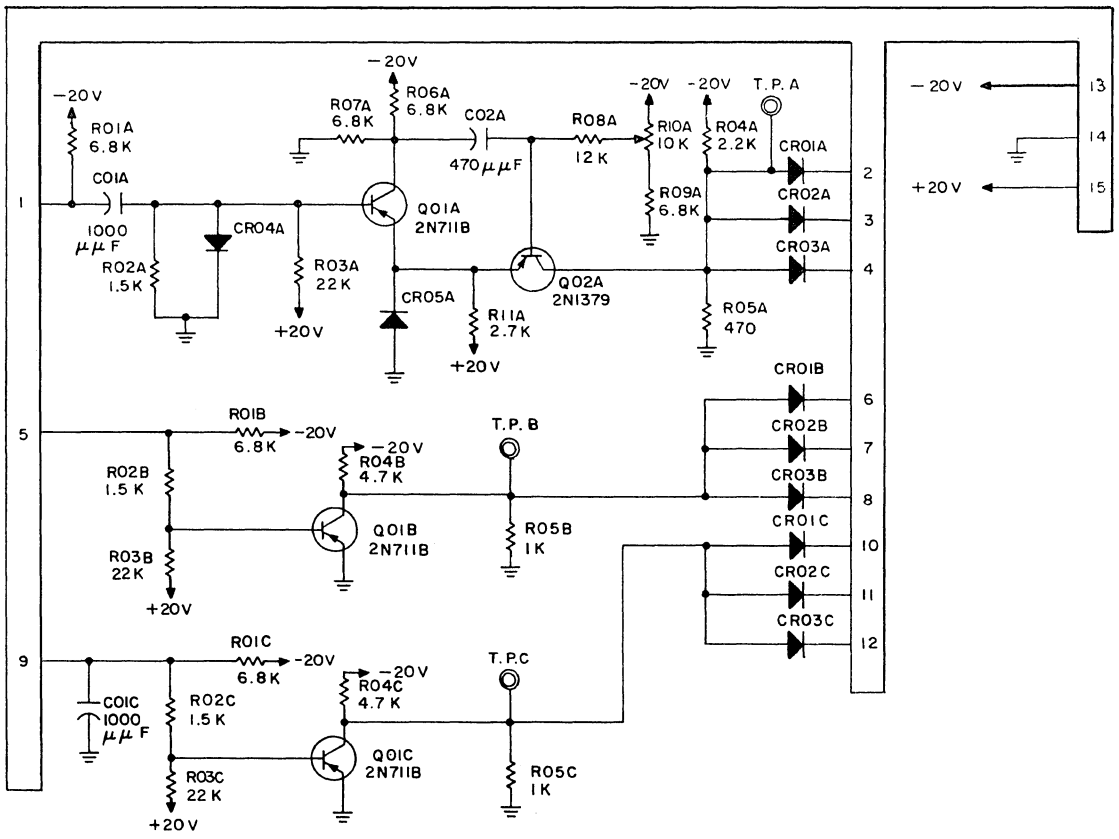
The pulse delay card is used as a read and write skew adjustment which compensates for mechanical misalignment of head gaps and small switching delays or phase lags in the electronic amplifiers. The card produces a narrow output pulse after a short adjustable delay (1 3/4 - 5 usec). A recycle time of 5 usec is necessary for delays to equal 95% of the specified delay period.

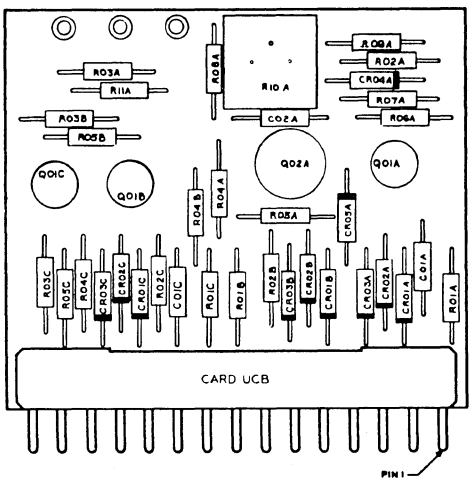
The circuit is divided into three sections. Circuit A is a one-shot multivibrator circuit composed of transistors Q01A and Q02A. The multivibrator is triggered by a negative input signal passing through a differentiating network to the base of Q01A. Conduction of Q01A couples a positive pulse to the base of Q02A and causes it to switch off. Multivibrator regeneration is completed by the common emitter resistor R11A. The period of the multivibrator is determined by R08A, C02A, and the resistance of potentiometer R10A. Recycle time is determined by resistors R06A and R07A and capacitor C02A. Transistor Q02A is a high-gain transistor which provides reserve output current for the limited base drive available in the circuit. Diode CR05A supplies the additional emitter current necessary for the collector load of Q02A, and references the emitter to near ground for this stable state of the multivibrator. During the multivibrator period, CR05A is reverse biased, permitting the gain of the two transistors to be utilized through a common emitter resistance (R11A) providing fast fall and rise times.

Circuits B and C are simplified inverter circuits which use a high-frequency transistor to decrease switching time. Circuit C also uses a delay capacitor C01C which allows the positive output to be delayed permitting ANDing with the output of circuit B for a 3/4-usec pulse output.

The three circuits are not connected internally and may be used as separate and complete elements. The circuits may also be connected through external jumpers to provide a delay output pulse from a negative input.




-20V
R01A 6.8K
C01A 1000 μμF
R02A 1.5K
CR04A
R03A 22K
+20V
R07A 6.8K
R06A 6.8K
C02A 470μμF
Q01A 2N711B
CR05A
R11A 2.7K
+20V
R08A 12K
Q02A 2N1379
R10A 10K
R09A 6.8K
R04A 2.2K
R05A 470
T.P. A
CR01A
CR02A
CR03A
CR01B
CR02B
CR03B
CR01C
CR02C
CR03C
R01B 6.8K
R02B 1.5K
R03B 22K
R04B 4.7K
Q01B 2N711B
R05B 1K
T.P. B
R01C 6.8K
C01C 1000 μμF
R02C 1.5K
R03C 22K
R04C 4.7K
Q01C 2N711B
R05C 1K
T.P.C
1
5
9
2
3
4
6
7
8
10
11
12
13
14
15

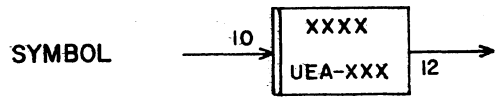

CARD UCB
PIN 1

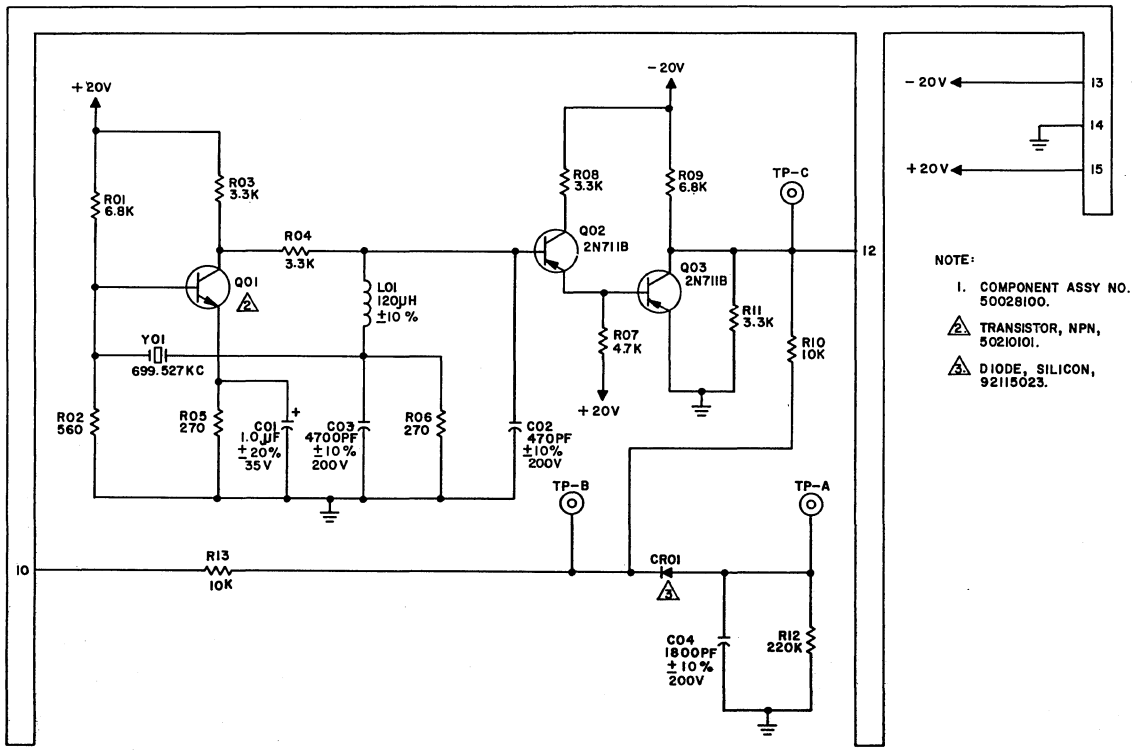
OSCILLATOR CALIBRATOR
UEA

The UEA card was designed to be used for routine maintenance on the 852 Disk Pack, to check the frequency of the IVA oscillator cards. Q01, Y01, L01, C02, C03 etc., comprise a crystal-controlled oscillator set to 699.527 Kc. Q02 and Q03 comprise a buffer amplifier to isolate the load from the oscillator, and to shape the oscillations into standard logic pulses. The output from Q03 is logic pulses at 699.527 kc repetition rate. This output appears at pin 12. It is also fed through R10 to the mixing network made up of R12, C04 and CR01. The IVA output enters pin 10 and goes through R13 to the mixing network. The sum of the two signals is seen at TP-B, and the difference (beat frequency) can be observed at TP-A.

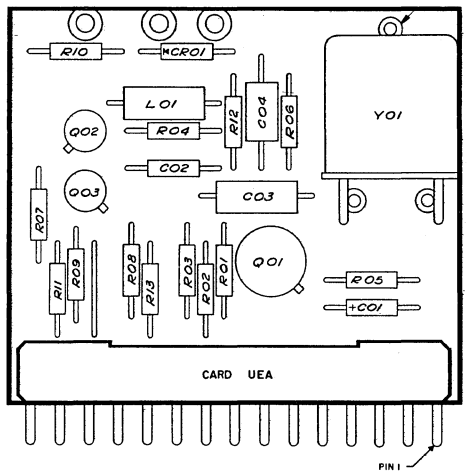
If the signal seen at TP-A is a 1Kc frequency, this indicates that the IVA signal fed in on pin 10 is either 1KC above, or 1KC below the frequency of the Q01 crystal-controlled oscillator. To tune in the IVA, it should be adjusted so the frequency seen at TP-A decreases to as near zero cycles per second as possible.

The main output is the difference in frequency between the internal oscillator and the oscillator signal fed in on pin 10.




+20V
-20V
R01 6.8K
R03 3.3K
R04 3.3K
Q01
L01 120μH ±10%
Y01 699.527KC
R02 560
R05 270
C01 1.0μF ±20% 35V
C03 4700PF ±10% 200V
R06 270
C02 470PF ±10% 200V
R08 3.3K
R09 6.8K
Q02 2N711B
Q03 2N711B
R07 4.7K
R11 3.3K
R10 10K
TP-C
TP-B
TP-A
R13 10K
CR01
C04 1800PF ±10% 200V
R12 220K
10
12
13
14
15
NOTE:
1. COMPONENT ASSY NO. 50028100.
2. TRANSISTOR, NPN, 50210101.
3. DIODE, SILICON, 92115023.

UEA


R10
MCR01
L01
R04
R12
C04
R06
Y01
Q02
C02
C03
Q03
R07
R11
R09
R08
R13
R03
R02
R01
Q01
R05
+C01
CARD UEA
PIN 1

VOLTAGE CONTROLLED DELAY

UFA, UFB

The voltage controlled delay circuit provides several options in delay duration and in the type of output signal desired at the end of the delay timeout by the use of external jumpers. It may have its delay controlled remotely by an analog d-c voltage in applications such as remote read and write deskew. It is also possible to use the circuit as a voltage comparator over a limited range.

The delay period is armed by having a "1" input on pin 1 for 0.5 usec or more for delay capacitors up to 5000 pf total. While armed and during the delay period, the output of circuit A (pins 5 and 6) is a "0" and the output of circuit C (pins11 and 12) is a "1". The delay period is initiated by an input on pin 1 going from a "1" to a "0". The input must remain a "0" during the delay period, or the delay rearms and does not time out. When the delay period times out, the output of circuit A goes to a "1" and the output of circuit C goes to a "0". Grounding pin 10 delays the output of circuit C going to a "0" for 1 to 3 usec. Thus a "1" coincidence at the end of the delay may be obtained by ANDing one diode from each of the two outputs. For delays below 10 usec, where the optional capacitor on pin 4 is not used in the delay circuit, pin 10 may be connected to pin 4 and reduce the "1" coincidence by 30% or more. Other external capacitors can be used instead; but care should be exercised with external capacitors or the "1" coincidence may go to zero, particularly when the voltage on pin 9 is less than -8v. Long delays cannot reliably utilize the "1" coincidence feature of this circuit.

Q01 and Q02 form an inverter-emitter follower combination for discharging C02 (and any other capacitors connected to pin 7). Q03 and Q04 act as a differential comparison amplifier and switch close to the point at which pins 7 and 9 have equal voltage. This determines the timeout period which switches output circuits A and C. The RC timeout period is controlled by several factors, nearly all of which are accessible to output pins for optional timing periods. Pin 7 allows external capacitors to be added for a coarse step adjustment. Pin 2 may be used to clamp the voltage (usually about -10v) used in the RC charge circuit. Pin 3 permits some of the charge resistance to be shorted out; however, care should be taken to make sure the maximum current in potentiometer R15

does not exceed 7 ma under any possible condition. Internal potentiometer R15 provides a fine vernier adjustment of the RC charge curve. The voltage on pin 9 determines the comparison point of the delay timeout and can be from -1 1/2 to -10v. This may be a fine vernier adjustment remote to the card, or may be preset at about -5v without external connections, or preset to about -10v by jumpering pin 8 to 9. Very low voltages on pin 9 permit delays down to about 0.2 usec to be obtained. Gating diodes (or transistors) on analog voltage circuit cards permit the voltage on pin 9 to be "ORed" from any of several analog voltage sources. Similar techniques can be used internally or remotely to program different delay times to one delay circuit.

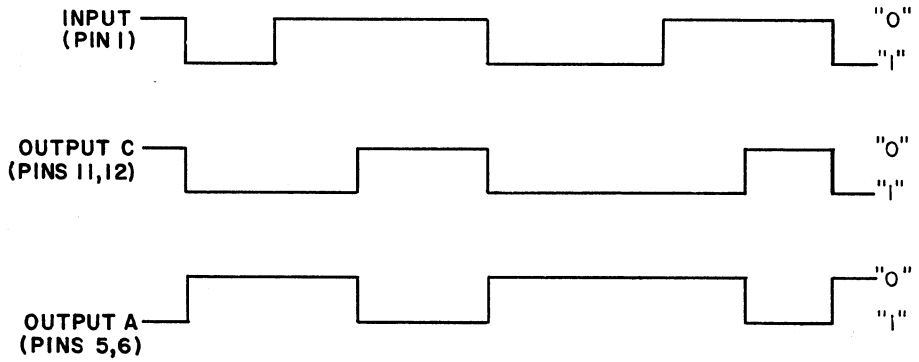
Q05 and Q06 are the output switching transistors which provide standard logic excursions. C04 delays the turn on of Q05 if connected directly to ground or via another capacitor to ground.

For best independence from power supply variations, the voltage on pin 9 and the voltage used to charge C02 should track with each other and not have significant variations within the timeout period.

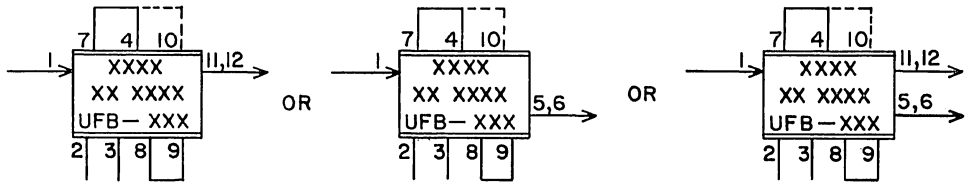
If the circuit is used as a voltage comparator in the usable -1 1/2 to -10v range, Q01 and Q02 should be disabled by a "0" on pin 1. The most rapidly changing voltage should be generally connected to pin 9 and the less dynamic voltage connected to pin 7 to minimize the need to drive charge current in C02.

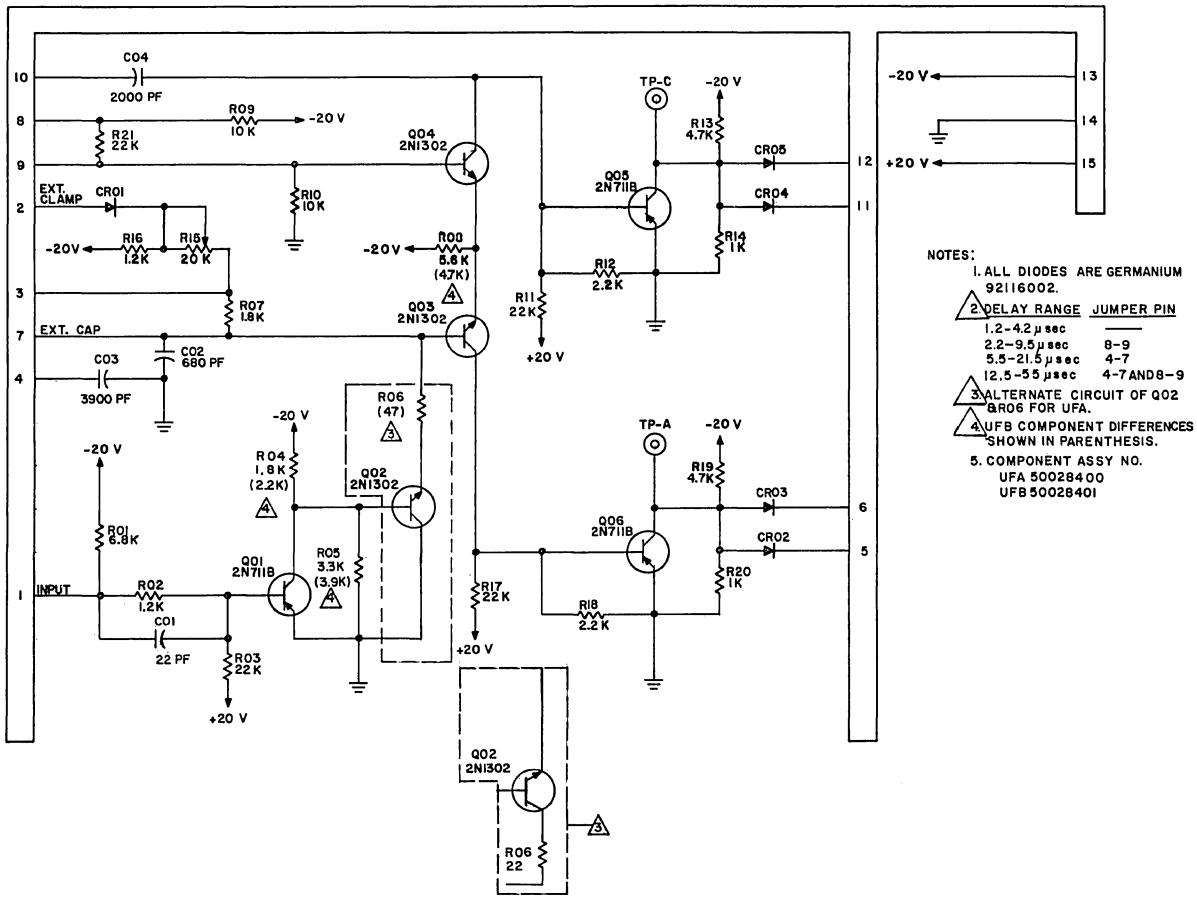
The logic symbol for the voltage controlled delay circuit shows the C output circuit (pins 11, 12) directly opposite the input. The A output circuit (pins 5, 6) is the other output and is never directly opposite the input even if the C output is not used.

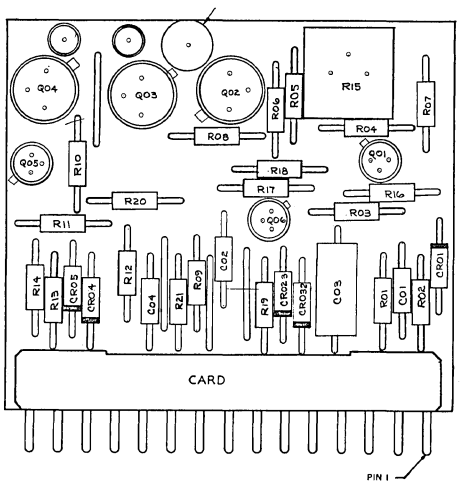
Waveforms for the input and outputs are shown below.

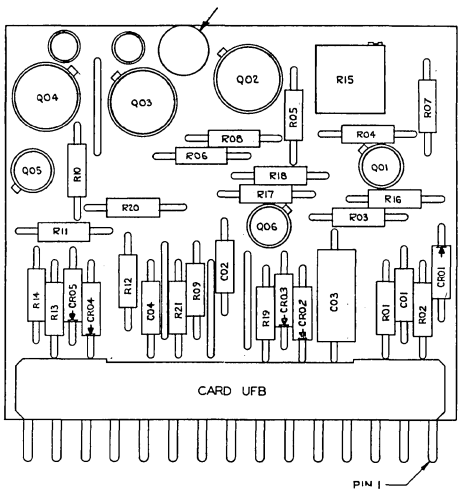


SYMBOL


7 4 10
1
XXXX
XX XXXX
UFB— XXX
11,12
2 3 8 9
OR
7 4 10
1
XXXX
XX XXXX
UFB— XXX
5,6
2 3 8 9
OR
7 4 10
1
XXXX
XX XXXX
UFB—XXX
11,12
5,6
2 3 8 9


C04
2000 PF
R09
10 K
-20 V
R21
22 K
Q04
2N1302
EXT. CLAMP
CR01
R10
10K
-20V
R16
1.2K
R15
20 K
R08
5.6K
(4.7K)
R07
1.8K
EXT. CAP
C03
3900 PF
C02
680 PF
R06
(47)
R04
1.8K
(2.2K)
Q02
2N1302
R01
6.8K
INPUT
R02
1.2K
C01
22 PF
R03
22K
+20 V
Q01
2N1118
R05
3.3K
(3.9K)
R17
22K
R11
22K
TP-C
R13
4.7K
CR05
CR04
Q05
2N7118
R14
1K
R12
2.2K
TP-A
R19
4.7K
CR03
CR02
Q06
2N7118
R20
1K
R18
2.2K
Q02
2N1302
R06
22
-20 V
+20 V
NOTES:
1. ALL DIODES ARE GERMANIUM 92116002.
2. DELAY RANGE / JUMPER PIN
1.2-4.2 μsec —
2.2-9.5 μsec 8-9
5.5-21.5 μsec 4-7
12.5-55 μsec 4-7 AND 8-9
3. ALTERNATE CIRCUIT OF Q02 & R06 FOR UFA.
4. UFB COMPONENT DIFFERENCES SHOWN IN PARENTHESIS.
5. COMPONENT ASSY NO.
UFA 50028400
UFB 50028401


CARD
PIN 1


CARD UFB
PIN 1

VOLTAGE CONTROLLED PULSE DELAY

UGA

The voltage controlled pulse delay circuit is used for read and write deskew adjustment in magnetic tape units or in similar functions where a narrow pulse (0.25 - 0.75 usec) is desired at the end of the delay period. It is also useful where optional delays are to be gated into a circuit without requiring the hardware of a complete delay circuit. The UGA card performs a function similar to the UCB pulse delay card with the following differences:

1) Shorter recycle time.

2) Increased range of delay with optional ranges available.

3) Provisions for logically selecting different delays in a given range by gating in different d-c voltages.

4) Output pulse shaping is internally wired.

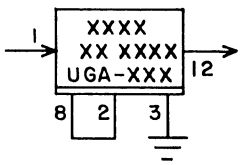
5) Input pulse width must be less than the duration of the delay.

Transistors Q01 and Q02 are connected in a bistable circuit which is equivalent to that of a SCR with turnoff provisions. Q03 and Q04 act as a differential amplifier for comparing voltages on their input bases. Q06 converts the end of the delay time period to standard logic element levels. Q05 provides turnoff of the Q01, Q02 bistable circuit.

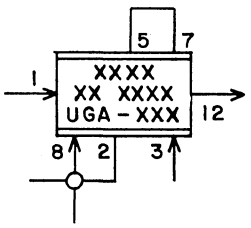
The delay period is initiated by a logical "1" pulse on Q05 (pin 1). If the previous delay period has been completed, both Q01 and Q02 would have been in a stable-on condition and pin 7 would be a fraction of a volt negative. Q05 drives the base of Q02 more negative than its emitter (pin 7) which turns Q02 off. The turnoff of Q02 results in Q01 also losing its base drive and turning off, thereby causing Q01 and Q02 to assume a stable-off condition. C02 and any additional external capacitor connected to pin 7 then charge negative through R10 and R11 with the voltage at emitter of Q03 following this charge curve. When the emitter voltage at Q03 and Q04 becomes slightly negative relative to the voltage on the base of Q04 (obtained from external connections to pin 8), then Q03 begins to turn off and Q04 starts to turn on. The collector current of Q04 then causes Q01 to be turned on. The turnon of Q01 also drives Q02 on

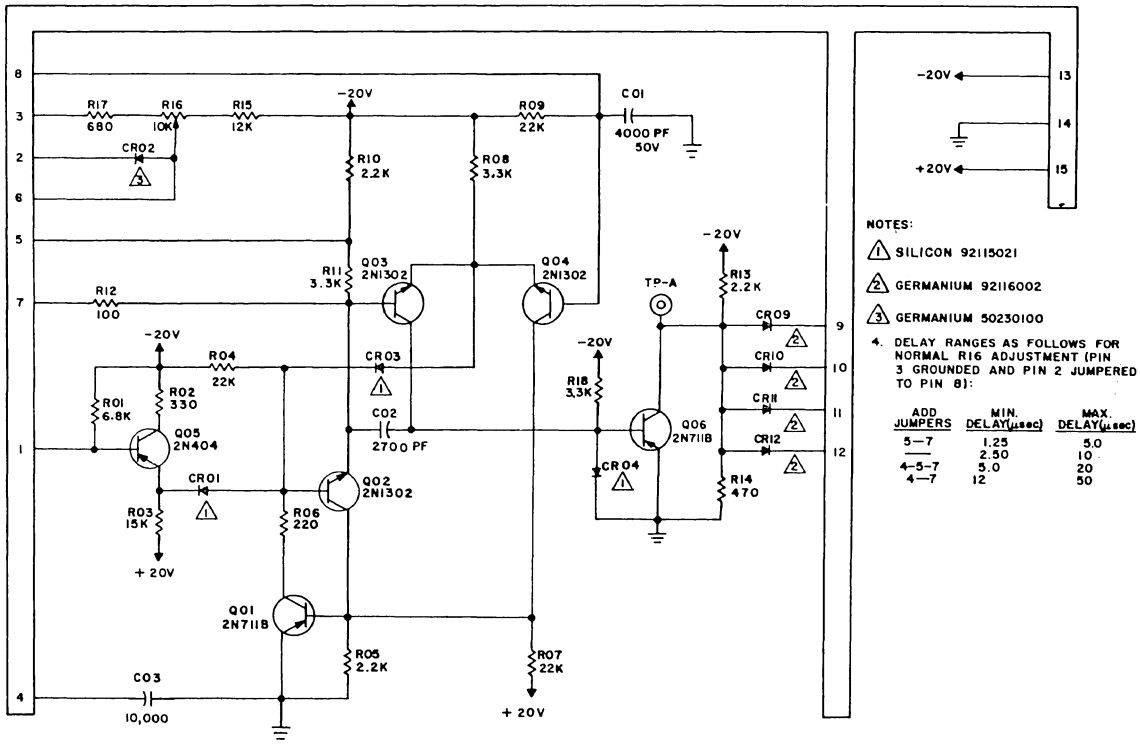
and Q02 continues to maintain base drive for Q01. Capacitor C02, and any external capacitors, are discharged to ground by the stable-on condition of Q01 and Q02. The discharge return current of C02 is supplied primarily by CR04 as long as the voltage at the base of Q06 is sufficiently positive for CR04 to conduct. As voltage drops below the forward conducting threshold of CR04, current from R18 and from R08 through Q03 drives the return point of C02 in a negative direction until clamped by the turn-on base to emitter voltage of Q06. Thus the time it requires for the return of C02 to re-establis its normal voltage determines the time Q06 is off and hence the "1" output pulse width. Because of the large turnon gain of the Q01, Q02 combination, the pulse width is determined almost wholly by the values of R08, R18, and C02. The use of R12 with externally added capacitors reduces the peak discharge current of the external capacitor sufficiently to maintain the output pulse width over delay ranges up to 10 sec. R12 also protects Q01 and Q02 from overload failure. As soon as C02 and any externally connected capacitors are discharged by Q01, Q02, the circuit is ready for the next delay. If an input pulse to initiate a delay comes during the previous delay period, it is ignored since Q01, Q02 are already turned off.

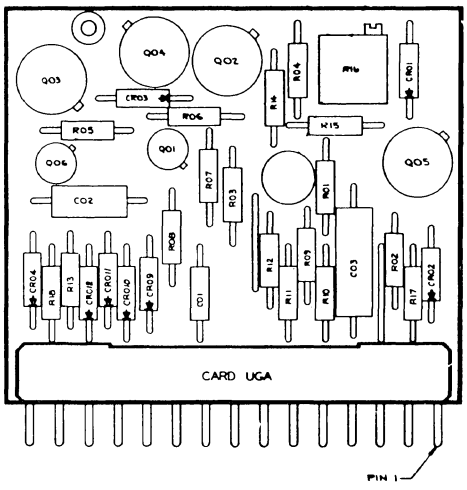
SYMBOL



OR




-20V
13
14
+20V
15
NOTES:
1. SILICON 92115021
2. GERMANIUM 92116002
3. GERMANIUM 50230100
4. DELAY RANGES AS FOLLOWS FOR NORMAL R16 ADJUSTMENT (PIN 3 GROUNDED AND PIN 2 JUMPERED TO PIN 8):
ADD JUMPERS | MIN. DELAY(μsec) | MAX. DELAY(μsec)
5—7 | 1.25 | 5.0
— | 2.50 | 10
4-5-7 | 5.0 | 20
4—7 | 12 | 50
R17 680
R16 10K
R15 12K
CR02
R10 2.2K
R08 3.3K
C01 4000 PF 50V
R11 3.3K
Q03 2N1302
Q04 2N1302
R12 100
TP-A
R13 2.2K
CR09
CR10
CR11
CR12
R14 470
R18 3.3K
Q06 2N711B
CR04
R04 22K
CR03
C02 2700 PF
R01 6.8K
R02 330
Q05 2N404
CR01
R03 15K
R06 220
Q02 2N1302
Q01 2N711B
R05 2.2K
R07 22K
C03 10,000
+ 20V
8
3
2
6
5
7
1
4
9
10
11
12


Q04
Q02
Q03
CR03
R06
R05
Q01
Q06
C02
Q05
R07
R03
R08
C01
CR04
R10
CR08
CR07
CR10
CR09
R12
R11
R09
C03
R02
R17
CR02
CARD UGA
PIN 1

ADJUSTABLE SHORT TERM DELAY

UHB

The UHB is a one shot multivibrator which produces a logical "1" output for a logical "1" input. The output pulse width is variable between 0.1usec and 1.1usec and is independent of input pulse width.

This card is used in conjunction with the UIA pulse shaper card, to produce a highly accurate, narrow strobe pulse which gates information into a storage flip-flop (FAA).

In the stable state Q03 is conducting, Q01 is off, and C02 is charged to the voltage at the collector of Q01. A negative "1" pulse appearing at the input initiates the one shot. Q01 turns on. The base of Q03 goes positive by an amount equal to the initial voltage charge on the capacitor, thus turning Q03 off. The capacitor then discharges through the series resistance R14 and R09 to the -15v zener voltage on the center tap of R09. As the capacitor discharges through zero volts, Q03 turns on and the pulse is completed.

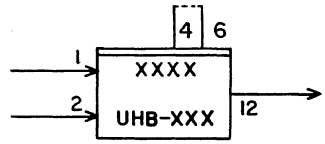
R09 not only adjusts the RC time constant, but also adjust the initial capacitor voltage which is determined by the divider R05 and R06 in series with R09. This tends to decrease the range of current that turns on Q03 and thus, minimize the change in fall time over the delay range.

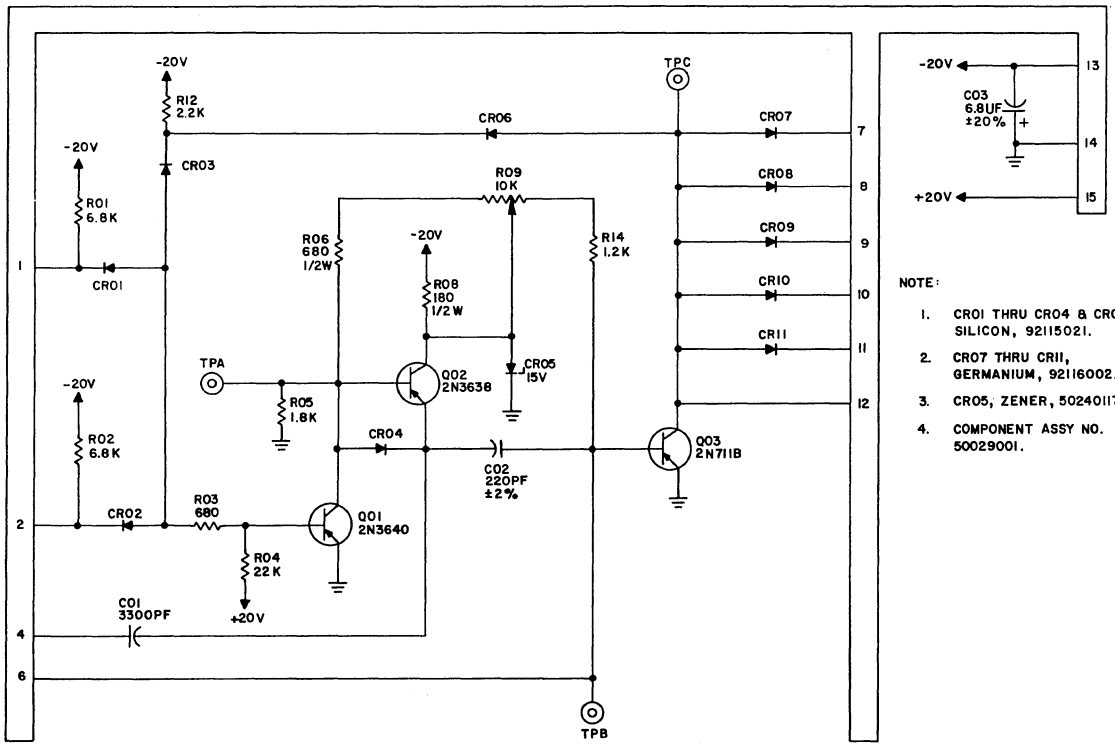
CR03 is coupled back to the input to form an "or" circuit and stabilize the output for changes in input pulse width. CR06 serves to isolate the input from the output circuit.

Test Specifications

	C02	C01 (Pin 4 Jumpered to Pin 6)
Typical Min Width	100 NSec	220 NSec
Typical Max Width	1.1 usec	17 usec
Typical Max Delay @ 50% PT	30 NSec	30 NSec
Typical Max Rise Time	30 NSec	30 NSec
Typical Max Fall Time	30 NSec	425 NSec
Typical Max Recycle Time	350 NSec	655 NSec
Typical Max Delay Change for $\Delta T = 30°C$	0.1% @1.2 usec	2.2% @ 18 usec

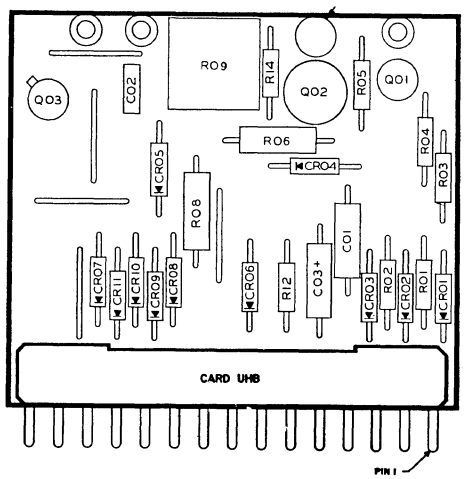
SYMBOL





NOTE:

1. CR01 THRU CR04 & CR06, SILICON, 92115021.
2. CR07 THRU CR11, GERMANIUM, 92116002.
3. CR05, ZENER, 50240117.
4. COMPONENT ASSY NO. 50029001.



PULSE SHAPER

UIA

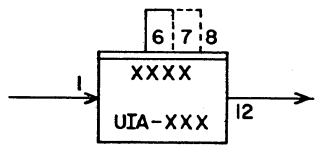
The UIA is used in conjunction with the UHB to produce a highly accurate, very narrow strobe pulse for gating information into the FAA card in the disc file.

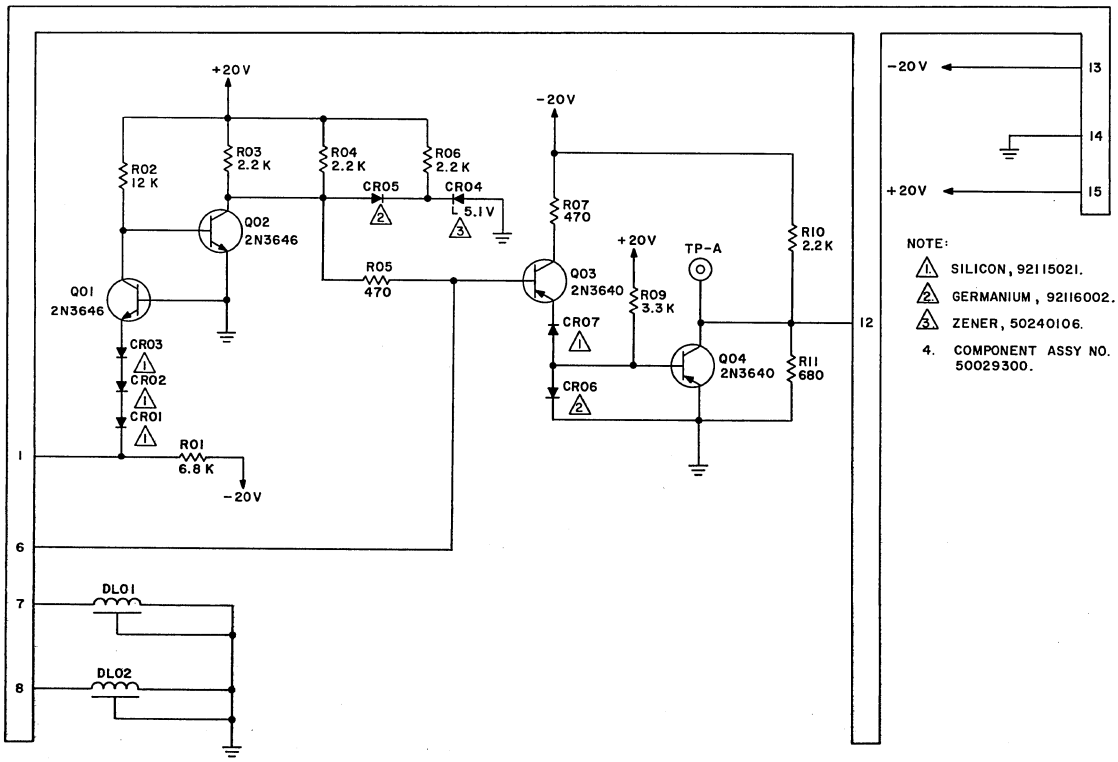
The UIA shapes a logical "0" pulse on the positive going edge of a logical "1" input pulse. The positive going edge at Pin 1 is transmitted through Q01 and turns on Q02. The negative going step voltage at the collector of Q02 propagates down the delay line and is inverted at the short circuit termination. This inversion propagates up the delay line and returns the collector of Q01 to 0 volts, producing a negative pulse equal to twice the value of the delay line at the base of emitter follower Q03. This negative "1" pulse is inverted by Q04 into positive going logical "0" pulse.

In like manner a negative going edge at Pin 1 produces a positive step at the collector of Q02. This is converted by the delay line into a positive pulse which keeps Q03 and thus Q04 in the off state. This positive pulse must time out before the negative pulse occurs or the pulse width will be affected. Therefore, to insure satisfactory operation the input pulse width and the recycle time must be greater than the output pulse width.

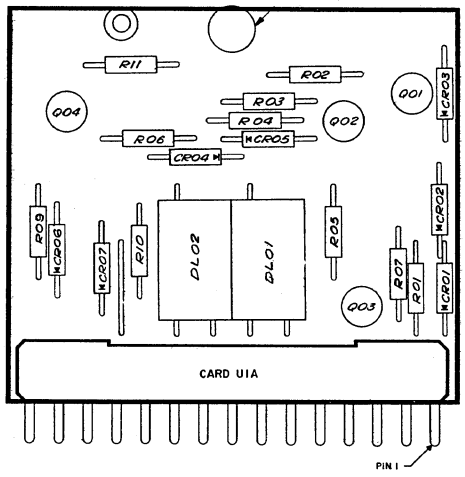
		DL_1 (30us)	DL_2 (100us)
Typical	Pulse Amplitude	4.8v	4.8v
Typical	Rise Time	20 nsec	20 nsec
Typical	Fall Time	40 nsec	70 nsec
Typical	Delay from Input @ 50% pt	60 nsec	60 nsec
Typical	Pulse Width @ - 1.5 v Pt.	80 nsec	230 nsec

SYMBOL




+20V
-20V
R02 12 K
R03 2.2 K
R04 2.2 K
R06 2.2 K
CR05
CR04
5.1V
Q02 2N3646
Q01 2N3646
R05 470
R07 470
Q03 2N3640
R09 3.3 K
TP-A
R10 2.2 K
CR07
Q04 2N3640
R11 680
CR06
CR03
CR02
CR01
R01 6.8 K
DL01
DL02
1
6
7
8
12
13
14
15
NOTE:
1. SILICON, 92115021.
2. GERMANIUM, 92116002.
3. ZENER, 50240106.
4. COMPONENT ASSY NO. 50029300.

UIA


R11
R02
R03
R04
R06
CR05
CR04
Q04
Q02
Q01
CR03
R09
CR08
CR07
R10
DL02
DL01
R05
R07
R01
CR02
CR01
Q03
CARD UIA
PIN 1

ADJUSTABLE LONG TERM DELAY
UJB, UJC

The long delay card is used for applications requiring a long delay that can be adjusted to a given value more accurately than the OJB circuit. This card differs from the OJB card in that the input on pin 1 is standard logic levels (-0.5v and -3v). Also, an input can be applied to pin 3 from either an output card, or a set of contacts. For details refer to the description of the OJB circuit.

There are two outputs on the UJB card; one inverting and one non-inverting (refer to figure 1). These are standard logic levels of -0.5 and -3 volts. The delay is initiated on the logical "0" edge of the input signal.

Delays from 400 usec to 60 sec (100 sec for UJC) are possible by means of jumper options and a potentiometer adjustment. Tables 1 and 2 show the ranges that can be covered by adjusting R07 for a given set of jumper conditions.

An alternate presentation of the delays available is shown in figure 2. Line #1 represents a timing circuit capacitance of 0.22 uf and is read horizontally. The distance between the diagonal lines labeled for a given set of jumper conditions at the intersection with line #1 is the minimum potentiometer range. Line #2 is for a circuit capacitance of 22.22 uf.

Note in figure 2 that in the 400 usec to 60 sec (100 sec for UJC) range of the circuit there exist two gaps; one of 4 msec between 4 and 8 msec, and one of 1 sec between 8 and 9 sec. These gaps can be filled by using an external capacitor between pins 4 and 8.

Referring to the schematic, note that the circuit contains three inverter stages (Q01, Q02, and Q07). There is also the timer composed of Q03, Q04, C01 (or C01 in parallel with C02), R07, R09 (or parallel combinations with R08 and R15), and the unijunction transistor Q05. SCR Q06 is used to provide a bistable device to latch-up the output. Diode CR05 is used to regulate the voltage to the timing and latching circuit, so the time delay is not effected by $\pm$20% power supply changes.

With a -3v input at pin 1 (see figure 1) Q01 will be on, so no voltage is supplied to the timer. Transistor Q02 will then be off, so its

collector voltage is -3v. Since this is also applied to the base of the output inverter Q07 it will be on, grounding the A output.

If the input at pin 1 goes to -0.5v, Q01 goes off allowing the voltage to the timer to rise to the zener voltage. A constant current generator (Q04) supplies a charging current to the timing capacitor (C01). The amount of current is determined by potentiometer R07 and the combinations of R08, R09, and R15. When the timing capacitor reaches approximately 6v with polarity as shown on the schematic, Q05 becomes regenerative and conducts from emitter (E) to base 1 (B1) discharging the capacitor. This develops a positive pulse on B1 which is applied to the gate-cathode junction of the SCR, causing it to turn on. Transistor Q02 turns on and Q07 goes off at this time. The supply voltage to the timer is within 2 diode drops (SCR anode to cathode and Q02 base-emitter) of ground. Therefore, it is pulled to approximately -1.6v at the end of the delay period. This removes the voltage from the timer and prevents free running oscillations of Q05. Transistor Q03 in the timing circuit is used as a compensating diode for temperature effects in the base-emitter junction of the constant current generator.

Any given time delay can be interrupted by returning the input to a "1", which causes Q01 to turn on and removes the voltage from the timer. However, because the timing capacitor may have charged to the full 6 volts, it will have to discharge via the unijunction emitter-base 1 junction and R10. Therefore, if C01 (0.22 uf) is used, a waiting period of approximately 50 usec must be allowed before a new delay is started. This could introduce a -5% change in the next delay period. If C02 (22 uf) is used, the waiting period would have to be approximately 5 msec for a -5% change in the next delay period. Note that the "1" input pulse width on either pin 1 or 3 should not be less than 50 usec to insure sufficient time for SCR to turn off.

To use the card with relay or switch contacts (or an output card) pin 3 is used as the input, but pin 1 must be grounded to keep Q01 off.

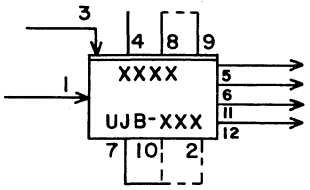
Table 1. Delay Range (UJB)

Min.	Max.	Jumper Pins	Min.	Max.	Jumper Pins
0.4 msec	4 msec	7-10	40 msec	400 msec	7-10, 8-9
8 msec	80 msec	7-2	800 msec	8 sec	7-2, 8-9
90 msec	600 msec	7 open	9 sec	60 sec	7 open, 8-9

Table 2. Delay Range (UJC)

Min.	Max.	Jumper Pins	Min.	Max.	Jumper Pins
0.4 msec	10 msec	7-10	40 msec	1000 msec	7-10, 8-9
10 msec	100 msec	7-2	1000 msec	10 sec	7-2, 8-9
100 msec	1000 msec	7 open	10 sec	100 sec	7 open, 8-9

SYMBOL



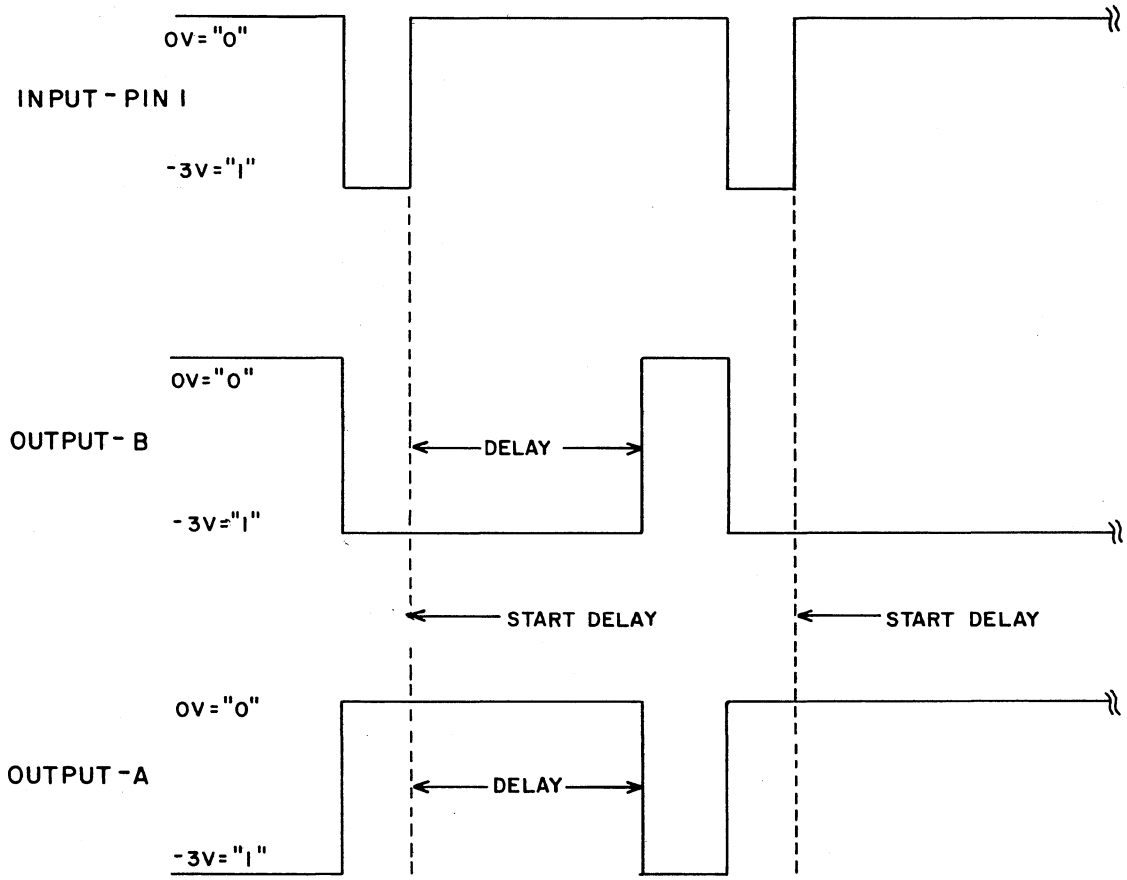


FIGURE 1. INPUT-OUTPUT WAVEFORMS

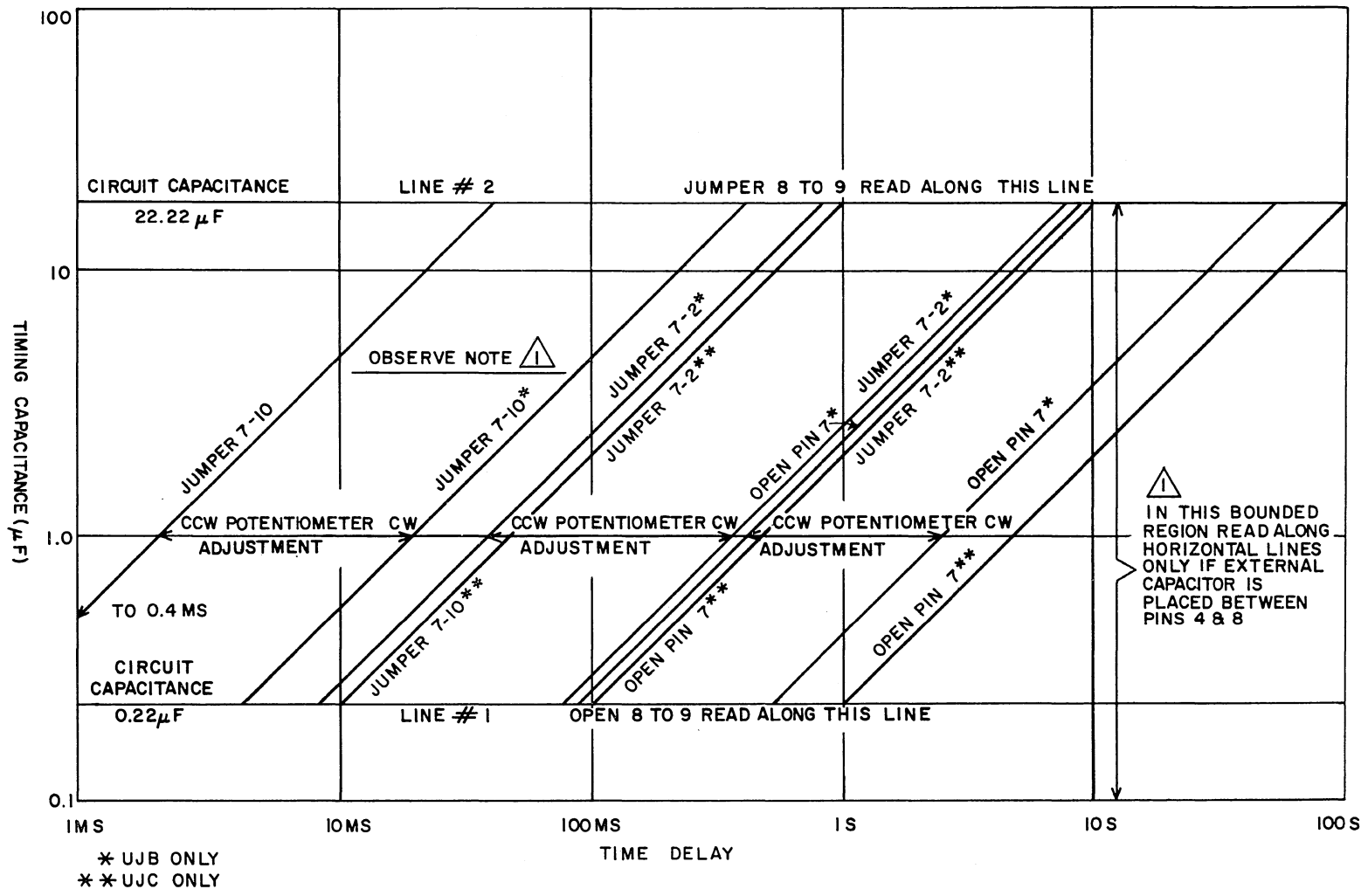
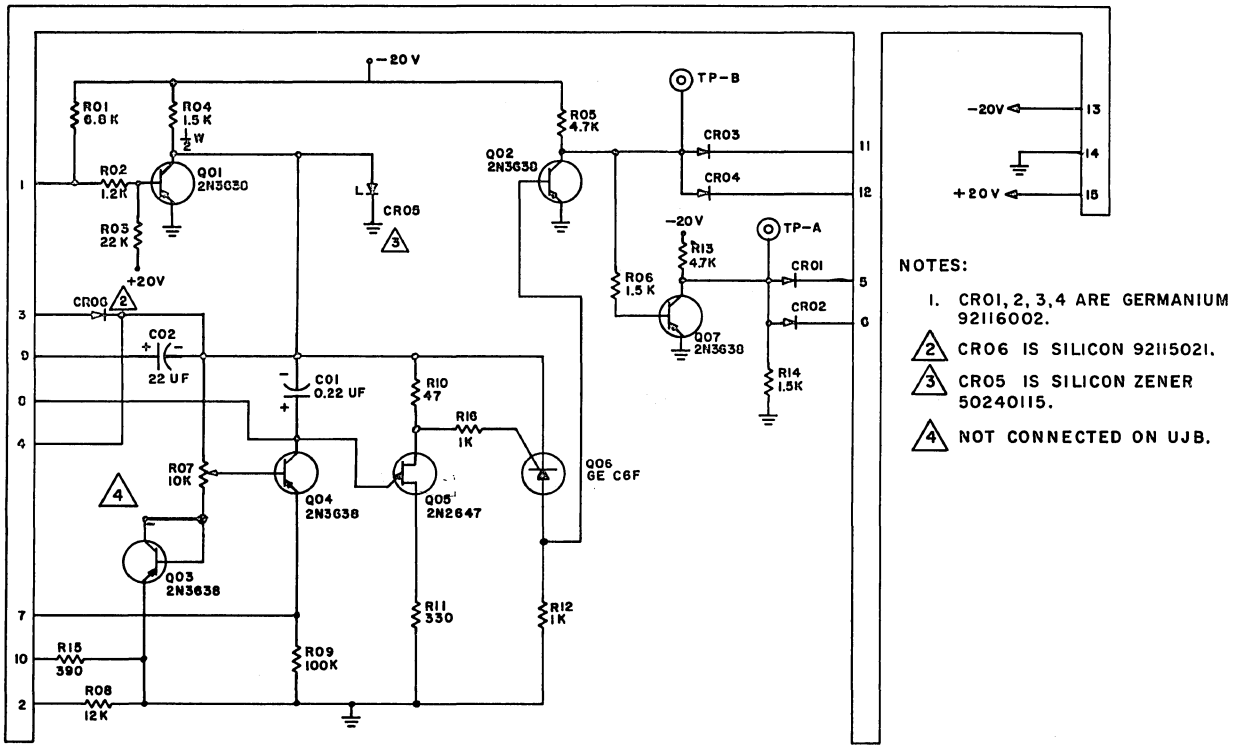
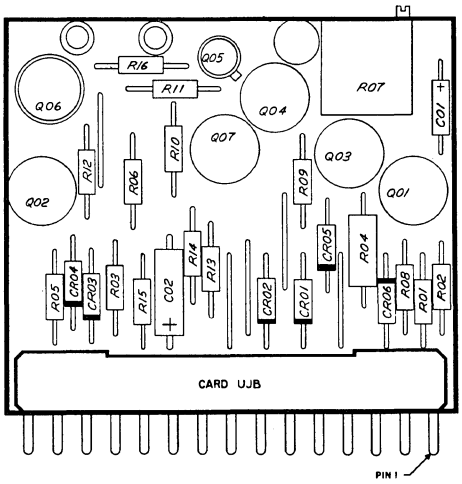


FIGURE 2. TIME DELAY VS JUMPER OPTIONS


-20 V
TP-B
TP-A
R01 6.8 K
R04 1.5 K 1/2 W
R02 1.2K
Q01 2N3638
R03 22 K
+20V
CR06
C02 22 UF
C01 0.22 UF
R10 47
R16 1K
R07 10K
Q04 2N3638
Q05 2N2647
Q06 GE C6F
Q03 2N3638
R11 330
R12 1K
R15 390
R09 100K
R08 12K
R05 4.7K
Q02 2N3638
CR03
CR04
CR05
R13 4.7K
R06 1.5 K
Q07 2N3638
CR01
CR02
R14 1.5K
-20V 13
14
+20V 15
NOTES:
1. CR01, 2, 3, 4 ARE GERMANIUM 92116002.
2 CR06 IS SILICON 92115021.
3 CR05 IS SILICON ZENER 50240115.
4 NOT CONNECTED ON UJB.

UJB


R16
Q05
R11
Q06
Q04
R07
C01
Q07
R10
Q03
R12
R06
R09
Q02
Q01
R05
CR04
CR03
R03
R15
C02
R14
R13
CR02
CR01
CR05
R04
R08
R01
R02
CARD UJB
PIN 1

GATED TOGGLE FLIP-FLOP
UKA

The UKA card is used in the 853 Disk Storage drive. When pin 3 is at logic zero (ground), a change of state from logic zero to logic one (-3V) at pin 1 causes the internal flip-flop to change state. When pin 3 is at logic one, both outputs are forced to logic zero.

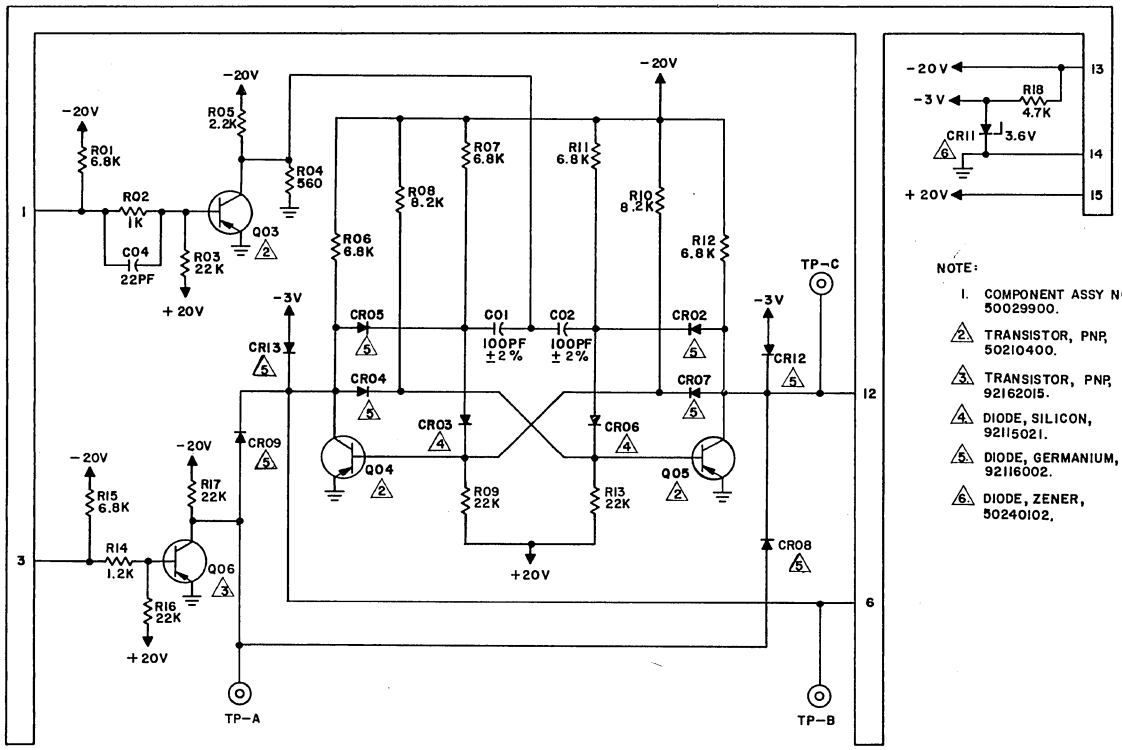
A negative going transition at pin 1 generates a positive going transition at Q03 collector. This is coupled through either C01 and CR03 to Q04 base, or through C02 and CR06 to Q05 base, depending on the state of the flip-flop. If Q04 is on, then the intersection of CR05, CR03, and C01 is at approximately -0.5V and Q04 base is at -0.8V, so that CR03 is reverse biased by 0.2V. On the other side of the flip-flop, the intersection of CR02, CR06, and C02 is at -3.6V while Q05 base is at -0.5V, so that CR06 is reverse biased by 3.1V. When Q03 turns on, current is pushed through C01 and C02 to R07 and R11, making the voltage at the anodes of CR03 and CR06 go more positive. Since CR03 is reverse biased much less than CR06, CR03 will be forward biased first, and the positive going waveform will be coupled to the base of Q04. This will turn Q04 off. As Q04 collector drops, Q05 base follows via CR04, turning Q05 on. As Q05 collector goes positive, this is coupled via CR07 to Q04 base, and the regeneration of the flip-flop is established.

The above description also applies if Q05 is on initially, with the appropriate substitution of components from one side to the other side of the flip-flop. Thus, it can be seen that every time the input at pin 1 passes the threshold going "negative", the flip-flop changes state. CR12 and CR13 clamp the off collector to the -3V internal supply made up of CR11 and R18.

When pin 3 is at ground, operation proceeds as above. When pin 3 goes to -3V, Q06 turns on, pulling both output pins 6 and 12 to -0.5V. Since this circuit drives the write/erase drivers AMC, the -0.5V output at pins 6 and 12 turns off all writing and erasing, regardless of what pin 1 does. When Q06 goes off again, the flip-flop may settle out in either state; however, since the 853 uses double-frequency recording, this is permissible.

There are no AND diodes at the outputs of this card.

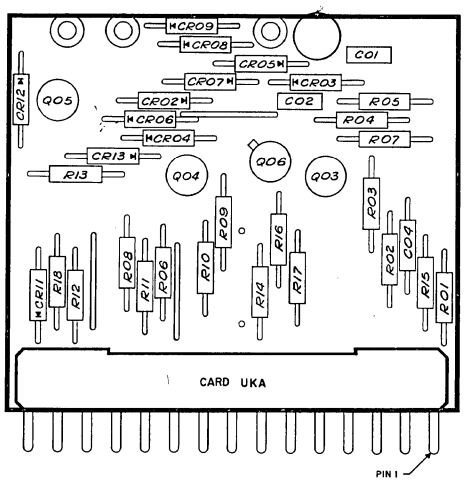
SYMBOL



NOTE:

1. COMPONENT ASSY NO. 50029900.
2. TRANSISTOR, PNP, 50210400.
3. TRANSISTOR, PNP, 92162015.
4. DIODE, SILICON, 92115021.
5. DIODE, GERMANIUM, 92116002.
6. DIODE, ZENER, 50240102.

UKA



GATED TOGGLE FLIP-FLOP
UKB

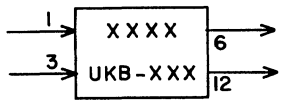
The UKB card contains a toggle flip-flop circuit and a gating circuit which, when turned on, hold the flip-flop outputs at ground. When the gate is turned off, it guarantees that the same output will reset to a "1". The flip-flop changes state with each negative going transition of a logic signal (0v to -3v) input. The gate circuit operates from a logic level input, with a "1" causing the gate to disable the flip-flop outputs. When the gate input goes to a "0", the output at pin 12 will remain at a "0" level while the output at pin 6 will come up as a "1".

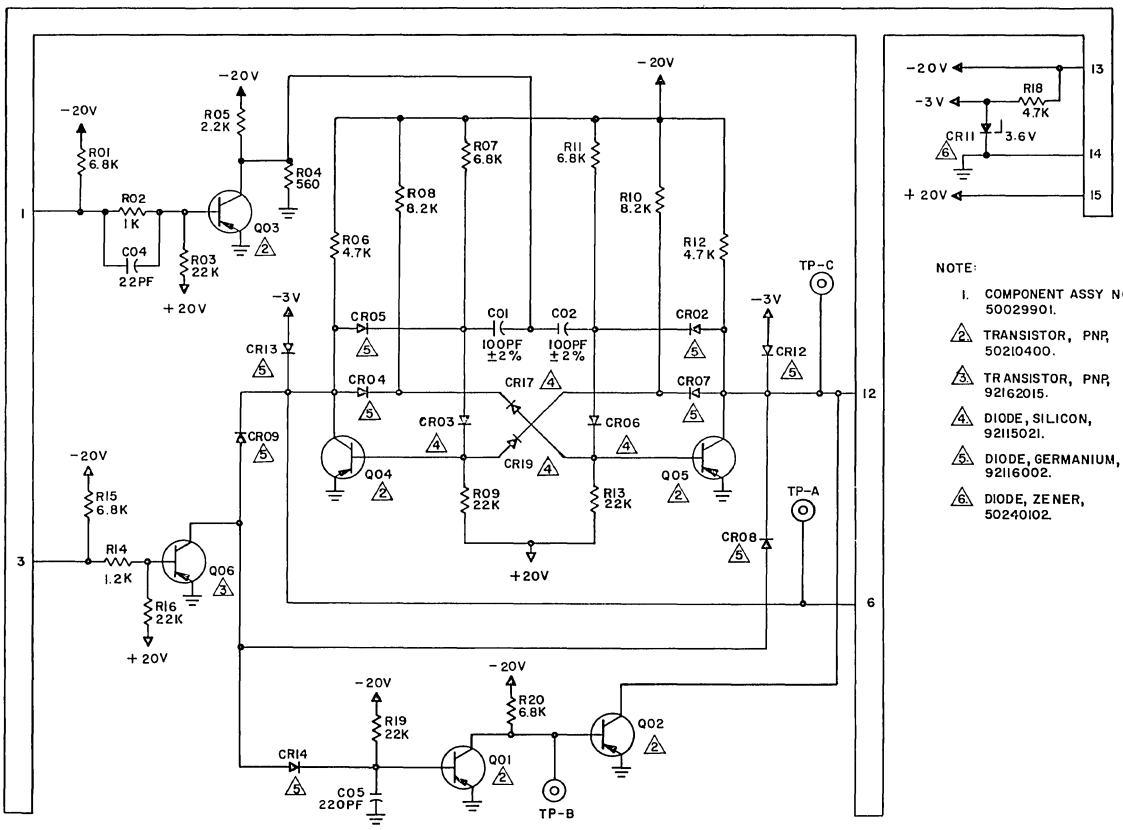
The input to the toggle flip-flop is pin 1. A negative transistion (0v to -3v) on the input causes Q03 to turn on. The collector of Q03 goes from a negative divider voltage (determined by R04 and R05) to near ground. This positive going transition is coupled through C01 and C02 to the anodes of CR03 and CR06. If Q04 is conducting and Q05 is turned off, then CR06 is back biased and CR03 conducts the positive pulse into the base of Q04 and turns it off. The collector of Q04 (pin 6) then goes toward -3.6V with CR04 conducting this change to Q05 base divider circuitry which consists of R13, CR17, and R08. The threshold of Q05 referred back to Q04 collector is at -1.2V. Q05 then turns on and the collector goes toward ground into saturation. CR07 conducts this change into Q04 base divider circuitry (R09, CR19, and R10) and holds Q04 off completing the flip-flop action. The next negative transition which appears at the input gets inverted to a positive transition by Q03 and couples through C02 and CR06 to turn off Q05. CR07 feeds back to the base circuitry of Q04 turning it on. CR04 then feeds back to the base circuitry of Q05 completing the lock up action by providing a back bias. Since the flip-flop is actuated by a short pulse, it is somewhat sensitive to any delay of its feedback mechanism. Consequently, this flip-flop will not reliably operate with more than an equivalent of approximately 100 pf to ground (and 3.3K load resistors to -20V) per output. The excursions are from -0.2V to -4V and nominal switching time is 20 nanoseconds, measured from the -2 volt levels of input to output signal (again with 3.3K loads to -20V).

The gate circuit is operated by a logic level input at pin 3. With

a "1" input (-3V) Q06 turns on and pulls both outputs (Pin 6 and 12) of the flip-flop through diodes to ground. Q06 quickly discharges C05 and Q01 turns off. This allows Q02 to turn on and its output is "anded" with the output of Q06 at pin 12. When the gate input goes to a "0", Q06 turns off, releasing the outputs at 6 and 12. However, pin 12 is still held at ground because of the delaying action of C05 on the reset circuit of Q01 and Q02. This delayed holding of pin 12 is nominally 0.12 microseconds, and allows pin 6 to go to a "1" (-4V) as a conditioned reset. Gate turn on time is 0.08 usec Max.

SYMBOL

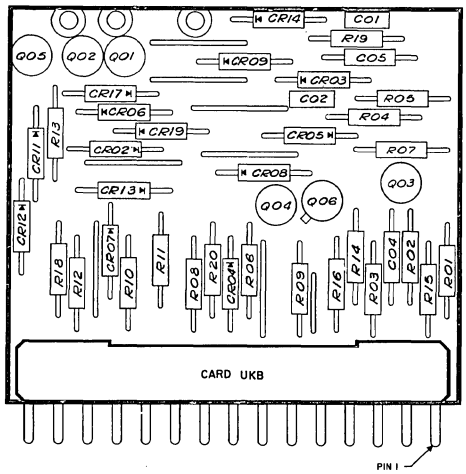




NOTE:

1. COMPONENT ASSY NO. 50029901.
2. TRANSISTOR, PNP, 50210400.
3. TRANSISTOR, PNP, 92162015.
4. DIODE, SILICON, 92115021.
5. DIODE, GERMANIUM, 92116002.
6. DIODE, ZENER, 50240102.

UKB



AC WRITE CURRENT SENSOR AND DELAY

ULA

This card contains two similar circuits (A upper and B lower) and is designed for use in the OEM disk storage drives. The function of the A circuit is to sense whether ac is flowing through the write head during the writing period. If a few write bits are missed, the output changes to a "1" indicating an error. This output is ANDed with the delayed write gate formed by the B half of the circuit.

When used with the disk storage drive, pin 2 is connected to the write head and the voltage waveform should appear as in Figure 1 (a) for satisfactory operation of the A circuit. With pin 2 more positive than the threshold as for WRITE, the collector of Q02 is approximately -11.2v. Both Q03 and Q05 are off and TP-A, Figure 1 (c) is at "1". (All references (a), (b), etc., refer to Figure 1.) If the input goes to write, the first pulse to go more negative than the threshold turns Q02 on, causing the A output to become a "0". During this time the B circuit input (d) is normally at a "1" so the output B (e) is a "0". Since the A and B outputs are normally ANDed together, the output signal will remain "0" during the transition of the A output. Assuming that the write enable B input on pin 7 goes to a "0", transistors Q06 and 7 turn off allowing the timing capacitor C02 to charge to -11.2v at which point Q08 and Q10 turn off and the output B goes to a "1" (e). The delay in the B circuit is approximately 6.4 usec. This delay is used to ensure that the A circuit has assumed a "0" output state before bringing the B output to a "1" state.

At this point the ULA card is "armed" such that if several write cycles are missed (a) the timing circuit R06, R07 and C01 times out (b) causing the A output to become a "1" (c). Since the B output has the AND enabled, a "1" output occurs indicating a faulty Write condition.

In order to keep from indicating a fault at the end of writing, the Write Enable signal (d) should return to a "1" within 6.4 usec of the last Write pulse which exceeds the threshold voltage.

The ULA card can be used with standard 1604-logic levels on pin 1 if pins 2 and 3 are jumpered. Additional delay time can be obtained by using external capacitors from pins 8 and 9 to ground.

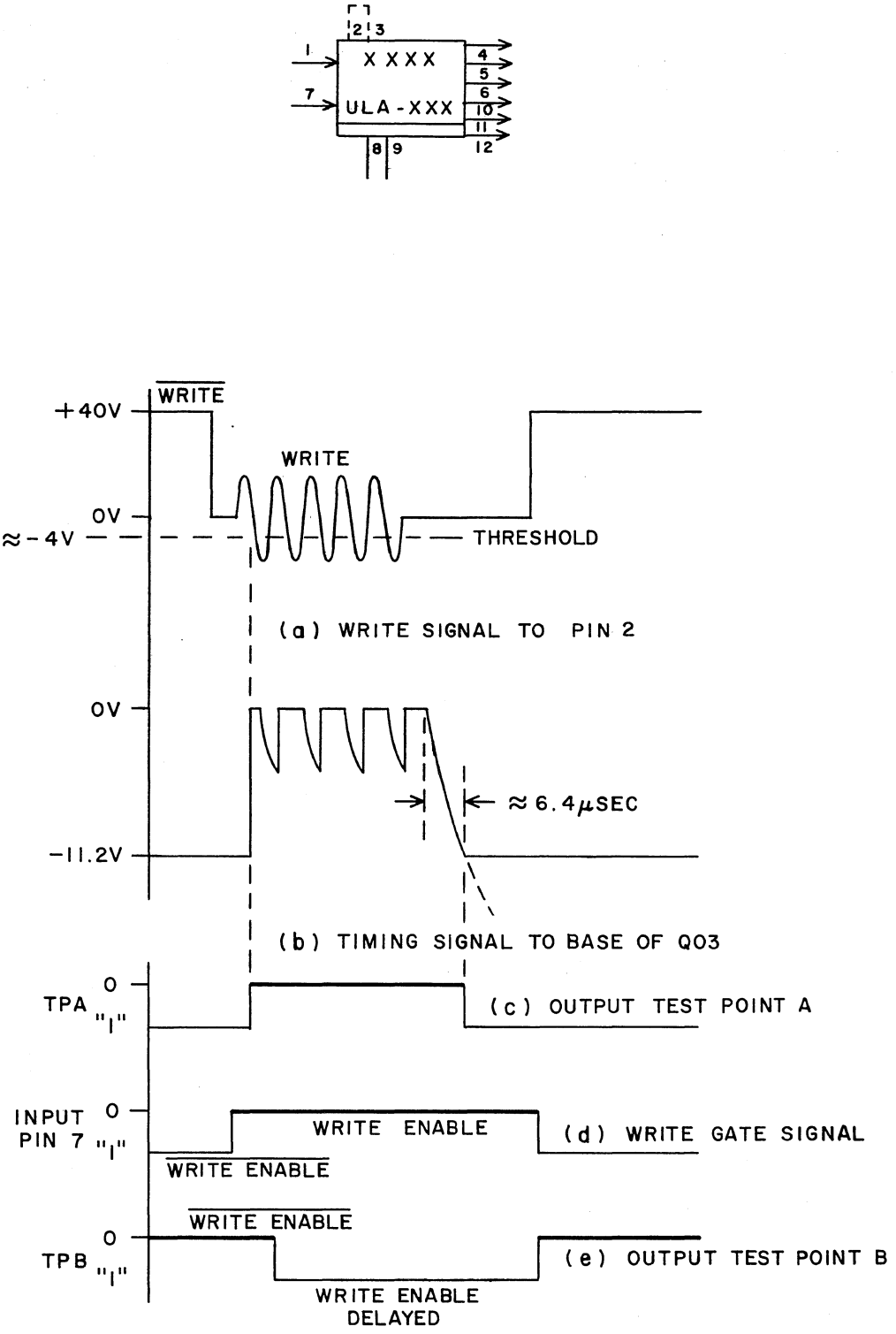
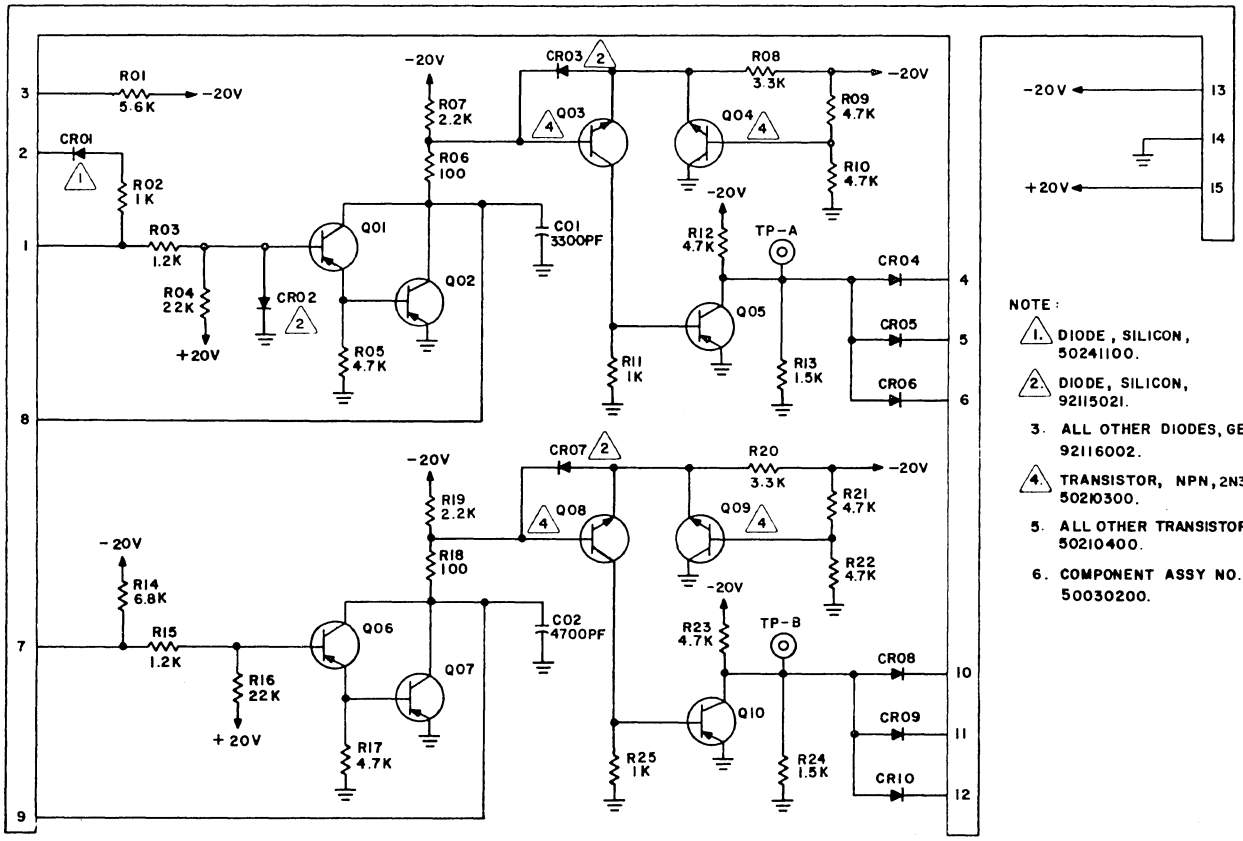
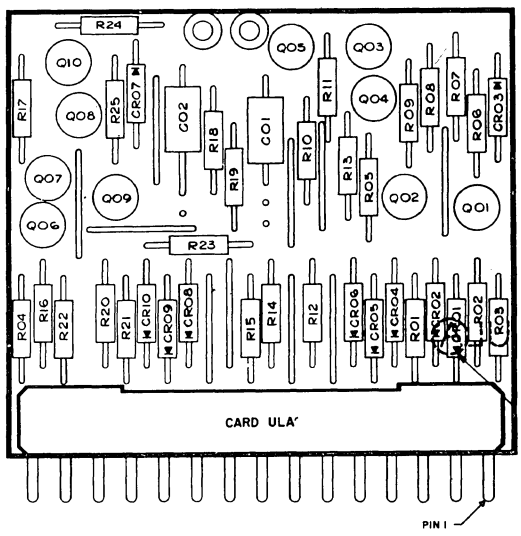


Figure 1. Wave Forms


R01
5.6K
-20V
CR01
R02
1K
R03
1.2K
R04
22K
+20V
CR02
R05
4.7K
Q01
Q02
R06
100
R07
2.2K
CR03
Q03
R08
3.3K
Q04
R09
4.7K
R10
4.7K
C01
3300PF
R11
1K
R12
4.7K
TP-A
Q05
R13
1.5K
CR04
CR05
CR06
R14
6.8K
R15
1.2K
R16
22K
+20V
R17
4.7K
Q06
Q07
R18
100
R19
2.2K
CR07
Q08
R20
3.3K
Q09
R21
4.7K
R22
4.7K
C02
4700PF
R23
4.7K
TP-B
Q10
R24
1.5K
R25
1K
CR08
CR09
CR10
NOTE:
1. DIODE, SILICON, 50241100.
2. DIODE, SILICON, 92115021.
3. ALL OTHER DIODES, GERMANIUM, 92116002.
4. TRANSISTOR, NPN, 2N3646, 50210300.
5. ALL OTHER TRANSISTORS, PNP, 2N3640, 50210400.
6. COMPONENT ASSY NO. 50030200.


CARD ULA
PIN 1

ONE-SHOT MULTIVIBRATOR

UPA

The UPA card is a one-shot multivibrator having two inputs and six outputs (three of the outputs are at a normal logical "0" level; the other three outputs are at a normal logical "1" level.) There is a single circiut per card.

Triggering the card from either of the inputs causes a pulsed output (normally 100 usec in durations; however, this may be altered by shorting various combinations of pins 3, 4, 5, & 6.) Table 1 indicates the pulse durations available via the various combinations of open and/or jumpering of pins 3, 4, 5, & 6.

The card is primarily designed to temporarily disable the AND error checking card. The inputs to pins 1 and 2 are taken from the write and erase gates (or their NOT conditions). When either input pin changes state, the multivibrator is triggered causing a 100 usec (or other selected duration) pulse out of pins 7, 8, & 9 (or 10, 11, & 12 if an inverse pulse is desired).

In order to maintain maximum pulse width, a minimum of 20 usec should elapse between triggering of the card (80 usec when a 320 usec pulse width is used). If the card is triggered before the minimum recycle time is up, a pulse will still occur; however the width of the pulse will be reduced. Figure 1 shows typical waveforms of the card.

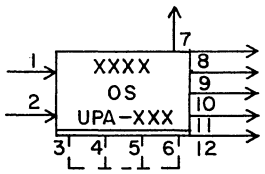


TABLE 1. PULSE DURATION-VARIATIONS

DURATION IN USEC	PINS SHORTED
45±8	3, 4, & 5
55±8	3, & 5
75±10	4, & 5
100±15	NONE
145±20	3, 4, 5, & 6
175±20	3, 5, & 6
240±35	4, 5, & 6
320±50	5, & 6

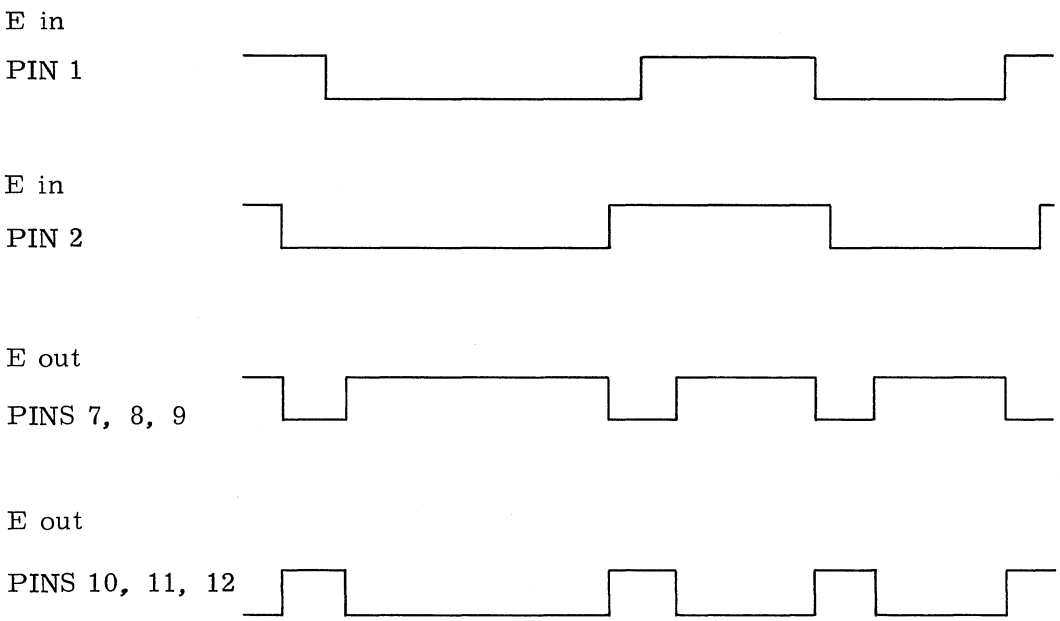
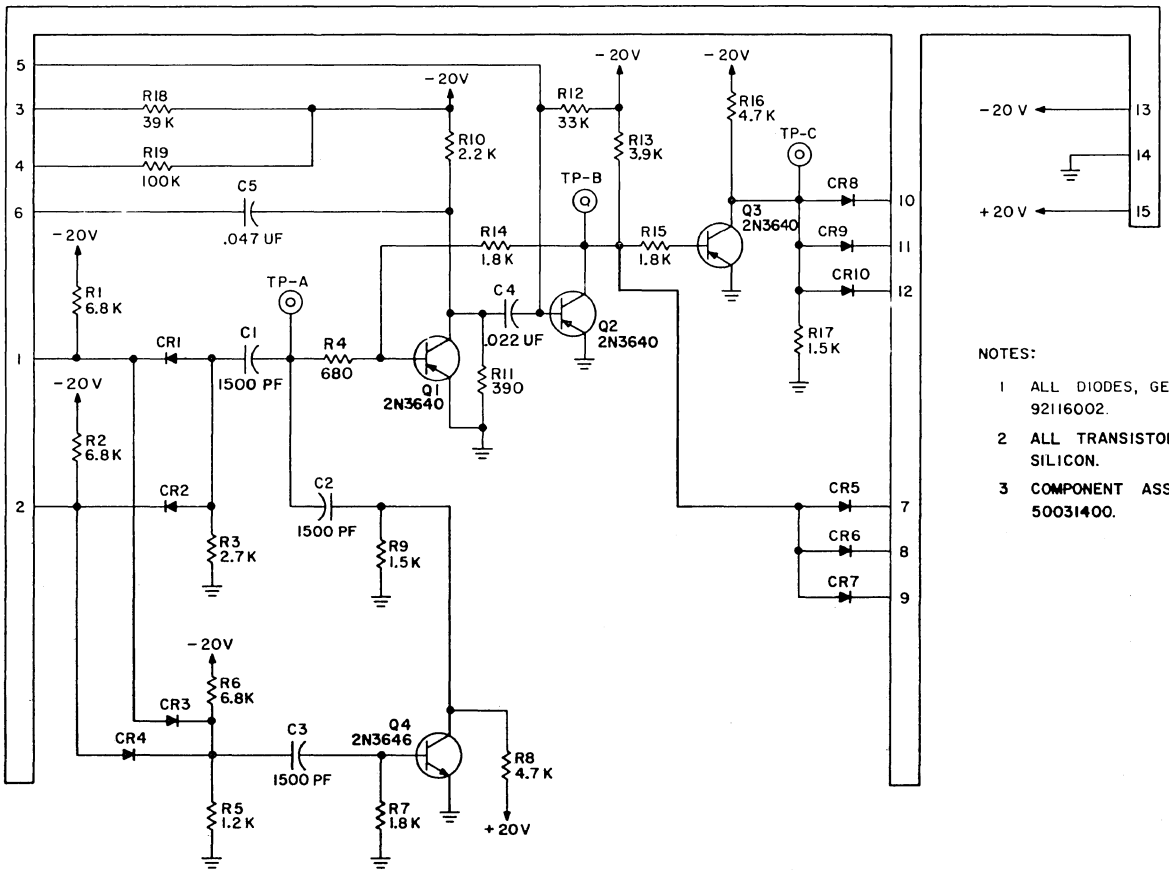


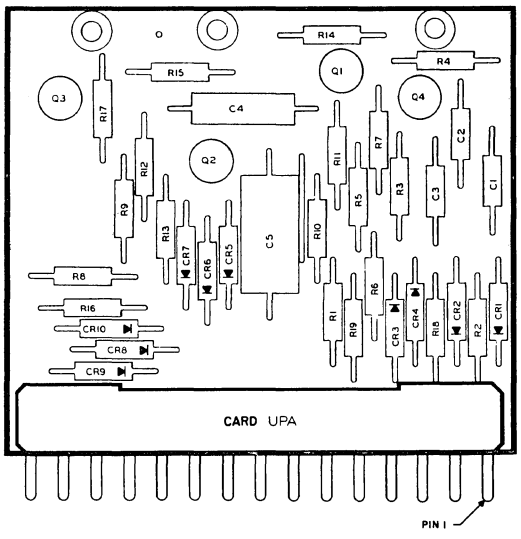
Figure 1. Typical Waveforms



NOTES:

1. ALL DIODES, GERMANIUM, 92116002.
2. ALL TRANSISTORS ARE SILICON.
3. COMPONENT ASSY, 50031400.

UPA



ONE-SHOT DELAY CARD
URA

The URA is an adjustable one-shot multivibrator which separates clock and "1" data bits in the recovery of double frequency encoded format recordings. In this application the trailing edge of logic "1" (-3.0v) pulses from a card such as the OZB is used to initiate the multivibrator delay period (provided it is not already in progress). The delay is normally set to time out at about 3/4 of the period of the low frequency pulse rate input. As a result, every other pulse at the high frequency rate would occur during the delay period. The complementary outputs are then "ANDED" separately with pulse signals from the same logic term as used on the URA input. This separates "1" data pulses from clock pulses in the double frequency encoded format.

Recycle time must equal or exceed the minimum in the table below or the next delay may be drastically reduced. The recycle times shown will provide 99% full delay compared with a recycle of 100 times as long. Delay adjustment ranges are also shown.

EXTERNAL JUMPERS	T_d, DELAY RANGE	MINIMUM RECYCLE TIME
None	190 - 450 ns	80 ns
2-8	450 - 1200 ns	100 ns
2-7	1000 - 3500 ns	130 ns
2-7-8 jumper	1300 - 4000 ns	310 ns

Output at pins 3 through 6 and 9 through 12 incorporate "AND" diodes for subsequent standard inputs. During the multivibrator period, pins 3 through 6 are at logic "0" and lag the logic "1" pulse on pins 9 through 12 by from 5 ns to 100 ns at the -1.5v level as measured on the test points. Exact lag is not predictable but it will increase as the delay setting on a given card is increased.

An input "1" pulse must be at least 50 ns wide before its trailing edge can initiate the multivibrator period. Care must be exercised to ensure that excessive wire length does not degrade the pulse width (measured at -1.5v) as it actually appears at pin 1.

To avoid current "hogging" problems, the input must never be paralleled with another input without using the customary isolation of "AND" diodes in the output of the pre-

ceding stage. The input to this stage is internally clamped and will not go more negative than -1.75v, or the normal turn-on/turn-off point of standard logic.

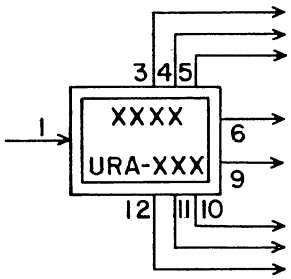
The circuit includes an input "OR" term (Q1); a pulse shaper (Q2); a multivibrator (Q3 and Q5) which also serves as an output stage; a complementary output stage (Q4); and Q6 (reduces recycle time of the multivibrator).

The input "OR" transistor has its emitter returned to approximately -1v as determined by the forward drop of CR1 and CR2. This places the turn-on/turn-off point of the base of Q1 at about -1.75v which is near the center of a normal logic input excursion. High speed is achieved by eliminating the normal input divider network and its speed-up capacitors with accompanying noise coupling problems. As a result, instead of swinging to -3v when in the logic "1" state, the input signal is clamped at about -1.75v.

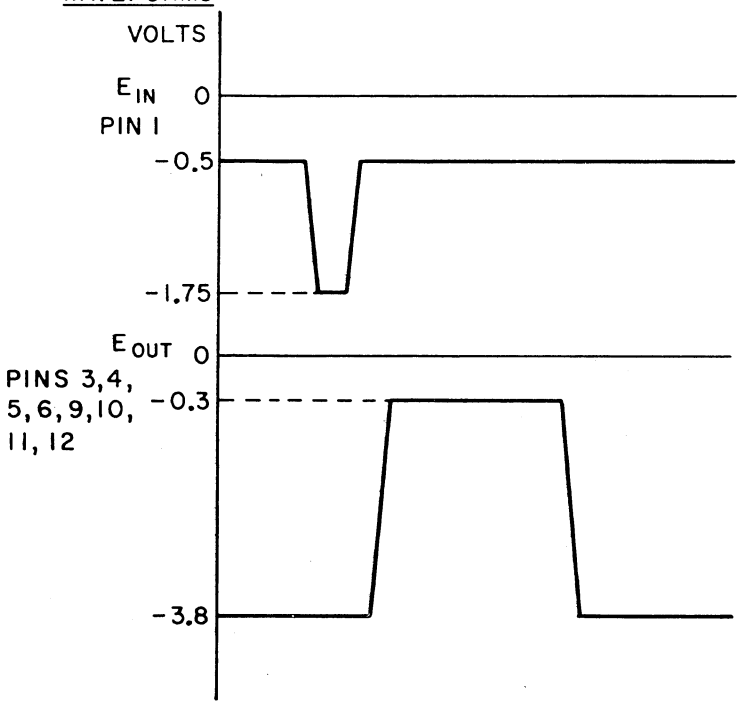
The pulse shaper (Q2) has a differentiator consisting of C1 and R4 that turns on Q2 for about 60 ns whenever Q1 turns off (corresponding to logic "0" input). CR7 allows C1 to recover quickly when the input signal goes to a logic "1".

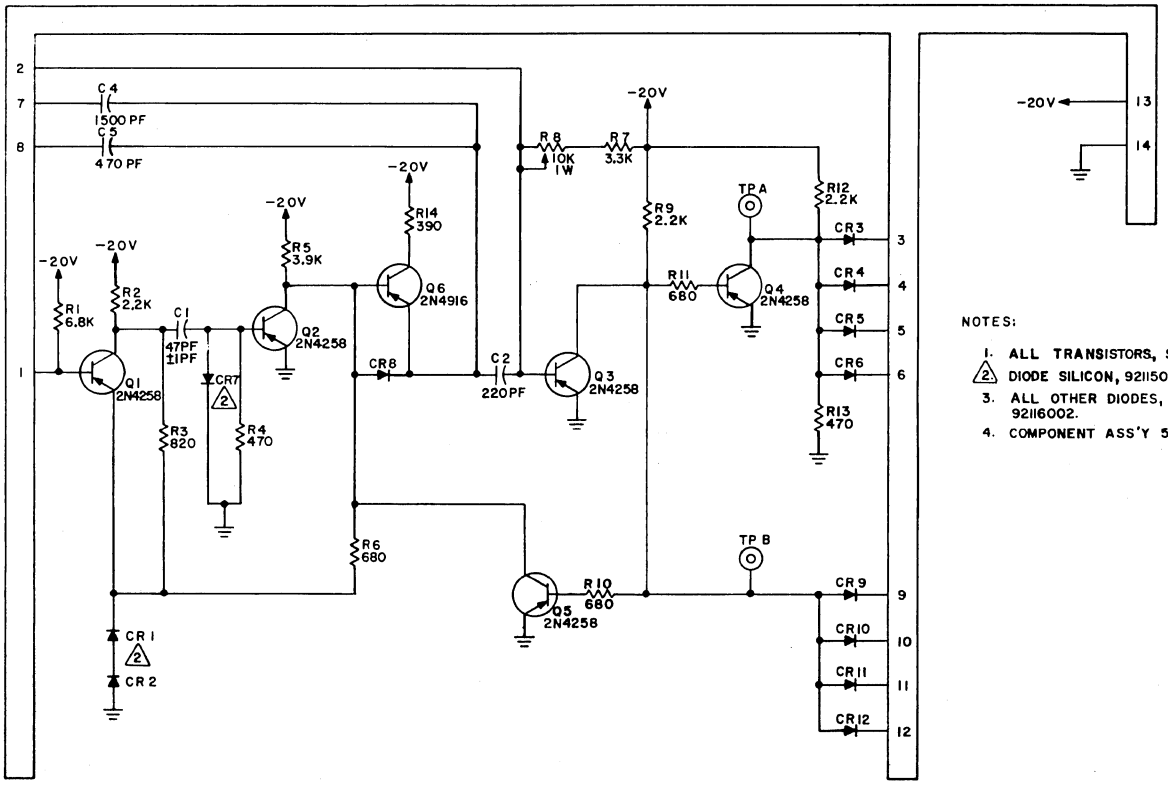
The multivibrator is triggered by a positive-going excursion (Q2 on) at the junction of CR8 and C2. This begins to turn off Q3 which then starts to turn on Q5, causing the circuit to regenerate such that Q3 is fully off and Q5 is fully on. The circuit remains in this state until C2 discharges to the point where Q3 again begins to turn on. At this time, Q5 begins to turn off, allowing the junction of CR8 and C2 to go negative which in turn causes Q3 to turn on harder. Transistor Q6 enhances the negative-going excursion at the junction of CR8 and C2 by providing a low impedance in the negative drive direction. The time period of the multivibrator is determined by R7, potentiometer R8, and C2 (together with C4 and/or C5 according to the use or omission of external jumpers 2-7 and 2-8) along with the magnitude of the positive-going excursion at the junction of CR8 and C2. This excursion is primarily determined by the ratio of R6 to the sum of (R5 + R6). Voltage compensation is obtained by returning R7 to the same source as R6. The positive power supply is not used in the circuit. A temperature increase from 25°C to 50°C will not increase the delay by more than 5%.

The multivibrator also serves as the drive for the logic "0" output during the off-time of the multivibrator. During on-time, Q4 acts as an inverter for driving the logic "0".


3
4
5
XXXX
URA-XXX
1
6
9
12
11
10

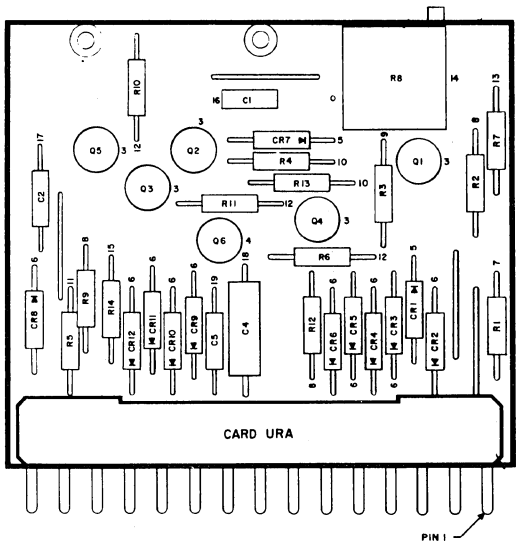
WAVEFORMS:


VOLTS
E IN
0
PIN 1
-0.5
-1.75
E OUT
0
PINS 3,4,
5,6,9,10,
11,12
-0.3
-3.8



NOTES:

1. ALL TRANSISTORS, SILICON.
2. DIODE SILICON, 92115021.
3. ALL OTHER DIODES, GERMANIUM, 92116002.
4. COMPONENT ASS'Y 50032000.



ONE-SHOT DELAY CARD
USA

The USA generates an output "1" pulse of 195 ns (±20 ns) provided the narrower trigger "1" pulses are at least 350 ns apart. An optional "1" pulse of 390 ns (± 40 ns) is available provided that the input trigger pulses are at least 725 ns apart and that either pins 2 and 3 (section A) or pins 8 and 9 (section B) are jumpered. Continuous adjustment of pulse width is not available for either circuit. Output pulse width is defined at the -1.5v level of the test points which is equivalent to about -1.8v at an output pin. The leading edge of the output "1" pulse will be delayed no more than 25 ns from the leading edge of the input "1" pulse crossing -1.5v.

The USA employs faster circuits than the normal 1604 Series inverters. To avoid current "hogging" problems at the input, the two inputs should never be put in parallel with each other without first having the customary isolation of "AND" diodes in the previous stage. Under normal operating conditions, the input to this stage is clamped and will not swing more negative than -1.75v, or the normal turn-on/turn-off point of standard logic.

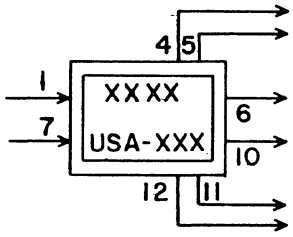
Interconnecting wiring between circuits must be kept short to prevent degradation of both incoming and outgoing pulses.

Each of the two circuits consists of an input "OR" term (Q1) which matches standard logic excursions and a one-shot multivibrator (Q2 and Q3) which also functions as the output stage.

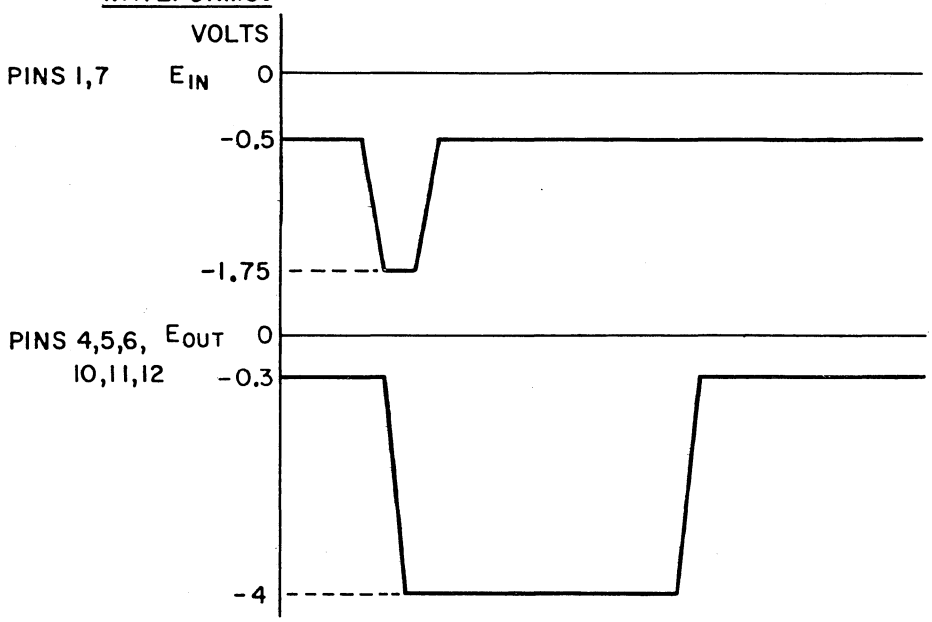
The input "OR" transistor has its emitter returned to approximately -1v as determined by the forward drop of CR1 and CR2. This places the turn-on/turn-off point of the base of Q1 at about -1.75v which is near the center of a normal logic input excursion. High speed is achieved by eliminating the normal input divider network and its speed-up capacitors with accompanying noise coupling problems. As a result, instead of swinging to -3v when in the logic "1" state, the input signal is clamped at about -1.75v. The one-shot multivibrator is triggered by a positive-going excursion at the junction of R2 and C1. This starts to turn off Q2, which begins to turn on Q3, causing regeneration of the circuit until Q2 is fully on and Q3 is fully off. The circuit remains in this state until C1 has discharged to the point where Q2 begins to turn on. At this time, Q3 starts

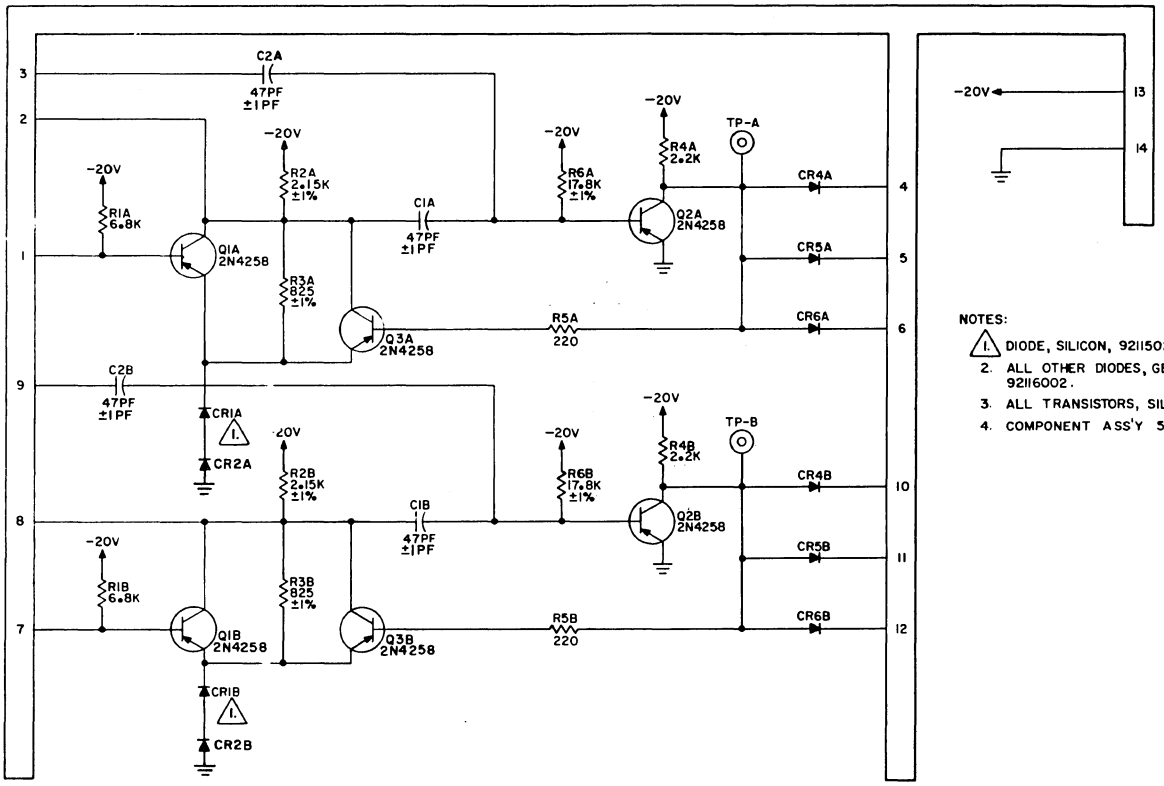
to turn off, allowing the junction of R2 and C1 to go negative which turns on Q2 even harder. Input transistor Q1 must be off before this latter regeneration can take place in the intended manner. The time period of the multivibrator is determined by R6 and C1 (also C2 if pins 2 and 3 or 8 and 9 are jumpered) together with the magnitude of the positive-going excursion at the junction of R2 and C1. This excursion is determined by the ratio of R3 to the sum of (R2 + R3). Voltage compensation is achieved by returning R6 to the same source. A temperature increase from 25°C to 50°C will not increase the delay by more than 6%.

Since the input to Q2 is capacitor-coupled, Q2 is readily operated in the grounded configuration and conveniently serves as an output stage with three diode outputs available for "AND" terms.


4
5
1
XXXX
6
7
USA-XXX
10
12
11

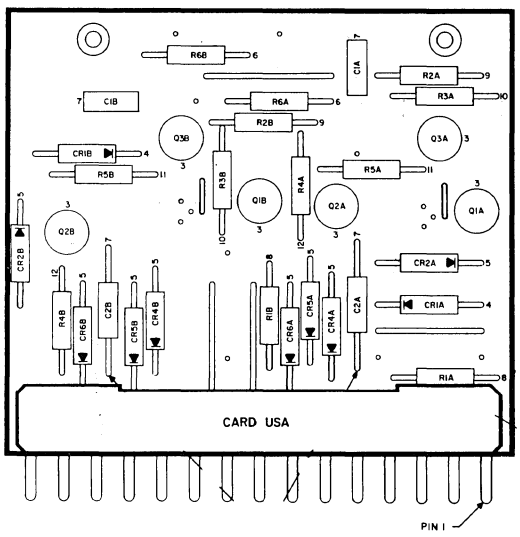
WAVEFORMS:


VOLTS
PINS 1,7
E_{IN}
0
-0.5
-1.75
PINS 4,5,6,
10,11,12
E_{OUT}
0
-0.3
-4



NOTES:

1. DIODE, SILICON, 92115021.
2. ALL OTHER DIODES, GERMANIUM 92116002.
3. ALL TRANSISTORS, SILICON.
4. COMPONENT ASS'Y 50032300.



PULSE SHAPER
XKA

The XKA card operates as a single pulse generator with a circuit normally switched to a "0" on the output. When the last of the two inputs changes from "1" to "0" within 10 usec, the card provides a "1" output for 2 to 4 usec. If either input returns to a "1" while the output is a "1", the output switches to a "0" within 0.5 usec.

The circuit consists of an inverter stage followed by a RC differentiating circuit and an emitter follower output. The input stage is similar to a two-input inverter. The negative excursion on the output of the first stage equals -6v, which compensates for attenuation in the RC differentiator.

The variations in the emitter follower (Q02) or the number of loads connected to the output have only a second order effect on the RC time constant. The time constant depends almost entirely on the values of R07 and C01. Resistor R07 also limits the base drive and saturation.

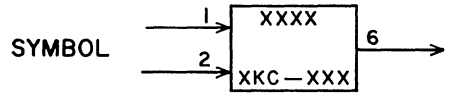
PULSE SHAPER
XKC

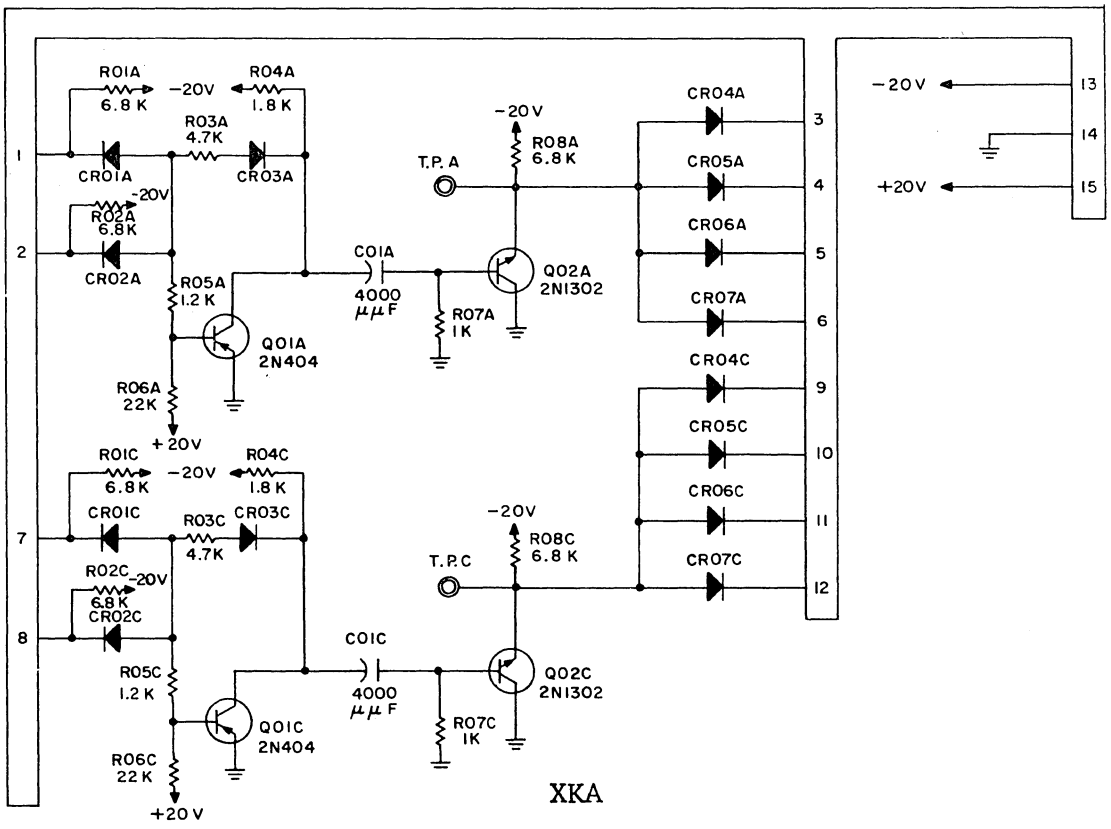
The XKC circuit operates in a similar manner to the XKA but provides much less internal delay and shorter duration output "1" pulses.

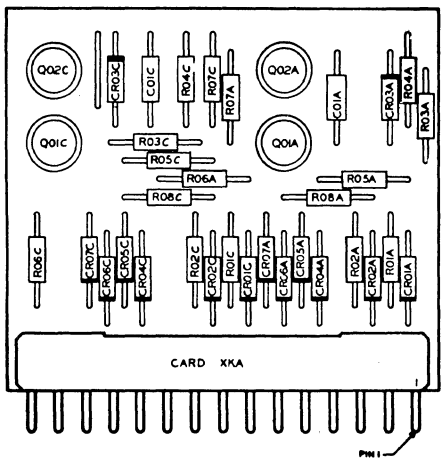
Logic "1" OR inputs feed directly to the Q01 base divider circuit and through diode CR08 to the base divider circuit of Q02. The parallel impedance of both these dividers is approximately the same as the base divider of a standard inverter. Q02 also has an "OR" input from the collector circuit of Q01. C01 in the collector circuit holds Q02 off for about 0.4 usec following a positive input signal. This determines the width of the "1" pulse output from Q02. On the return of the input to a "1", R08 delays recycling of C01 sufficiently to prevent the occurrence of runt output pulses at the time the input goes through the threshold of switching.

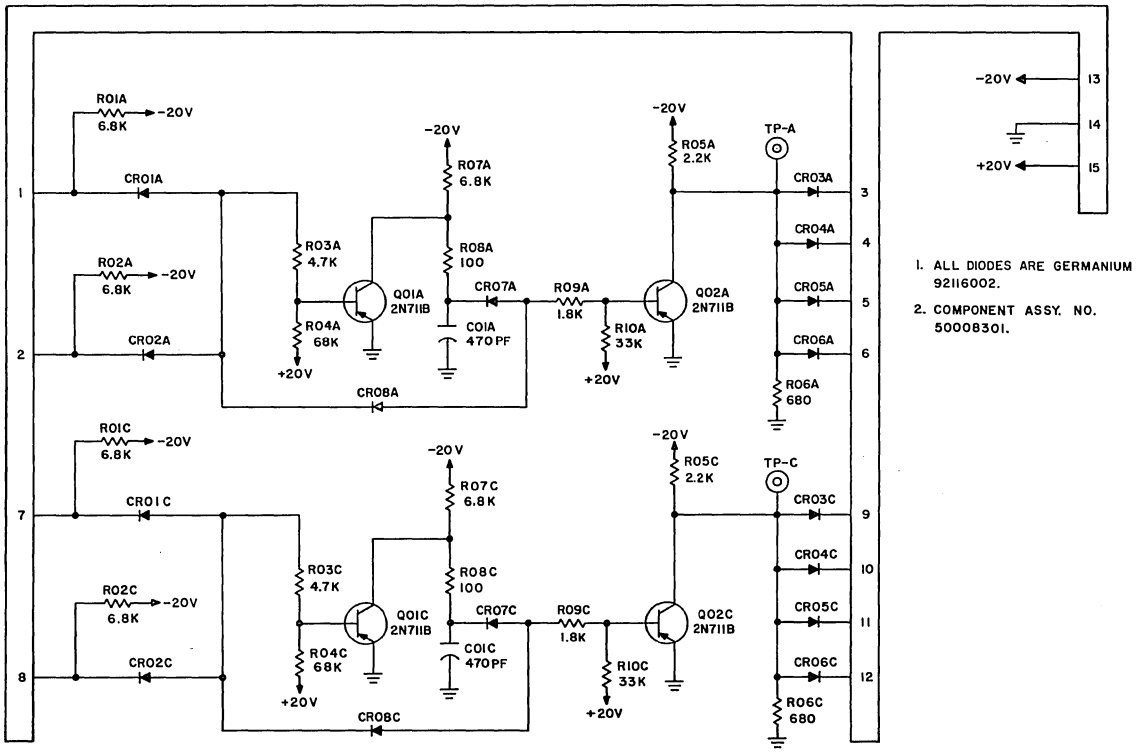
For power supplies in which the + and - voltages are equal within 1 volt and within the range of 16 to 24 volts, the output pulse width at the -2v level is 0.25 to 0.50 usec. Delay between input and output at the -2v level is 30 to 120 nsec under the same power supply conditions. The circuit is critical to rise time at the input and this should not exceed 250 nsec. In timing chain applications using a series string of XKC cards, delay from the first to last card is subject to pulse width variations of individual cards, but remains typically stable within 5% for a given set

of cards over an ambient temperature range of 75° F to 150° F.



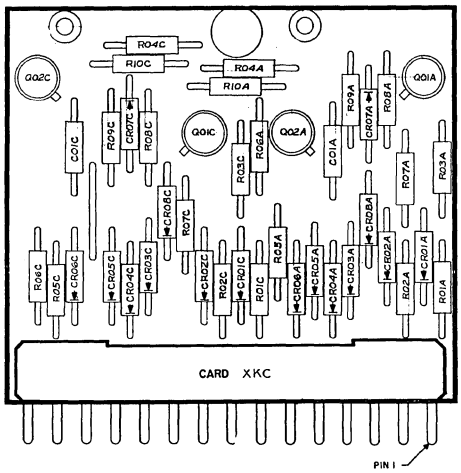






1. ALL DIODES ARE GERMANIUM 92116002.
2. COMPONENT ASSY. NO. 50008301.

XKC



APPENDIX 1

Tabulated Listing,
Control Data Corporation
Printed Circuit Cards

NOTE:
Further up-to-date listings may be obtained at any time by ordering the Standard Printed Circuit Card Index, available from Engineering Services, Computer Division.

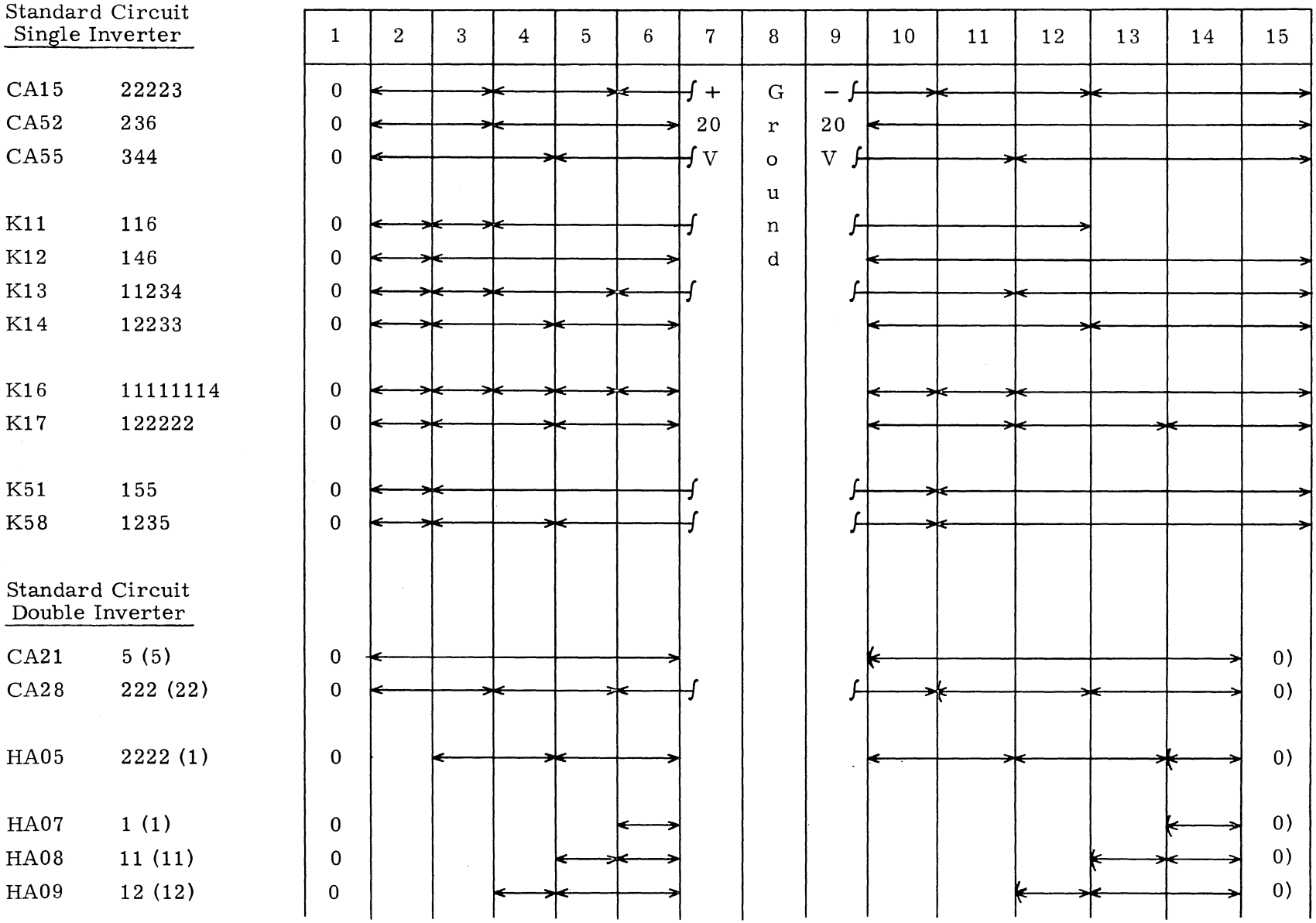
PIN ASSIGNMENTS

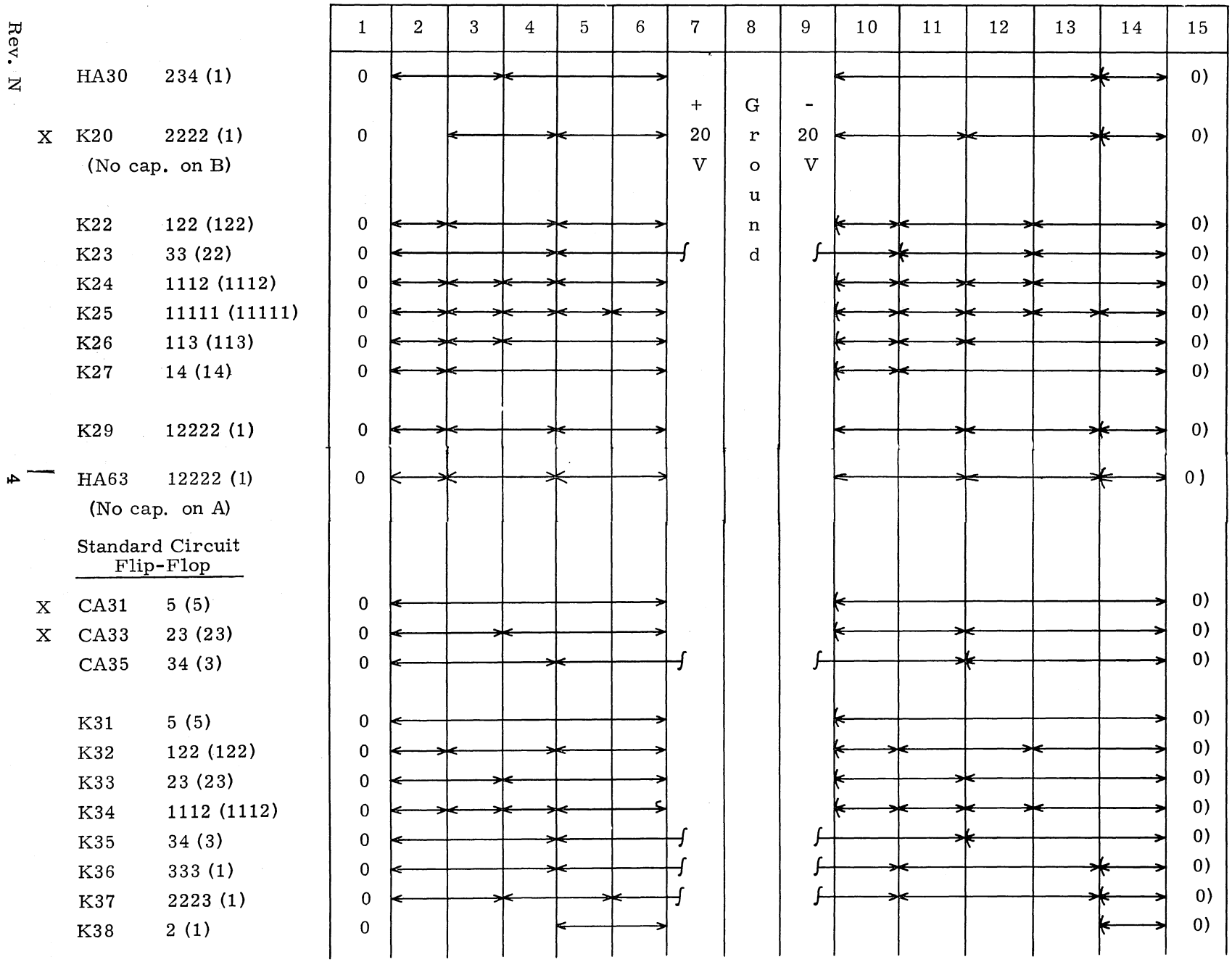
1604 & 3600

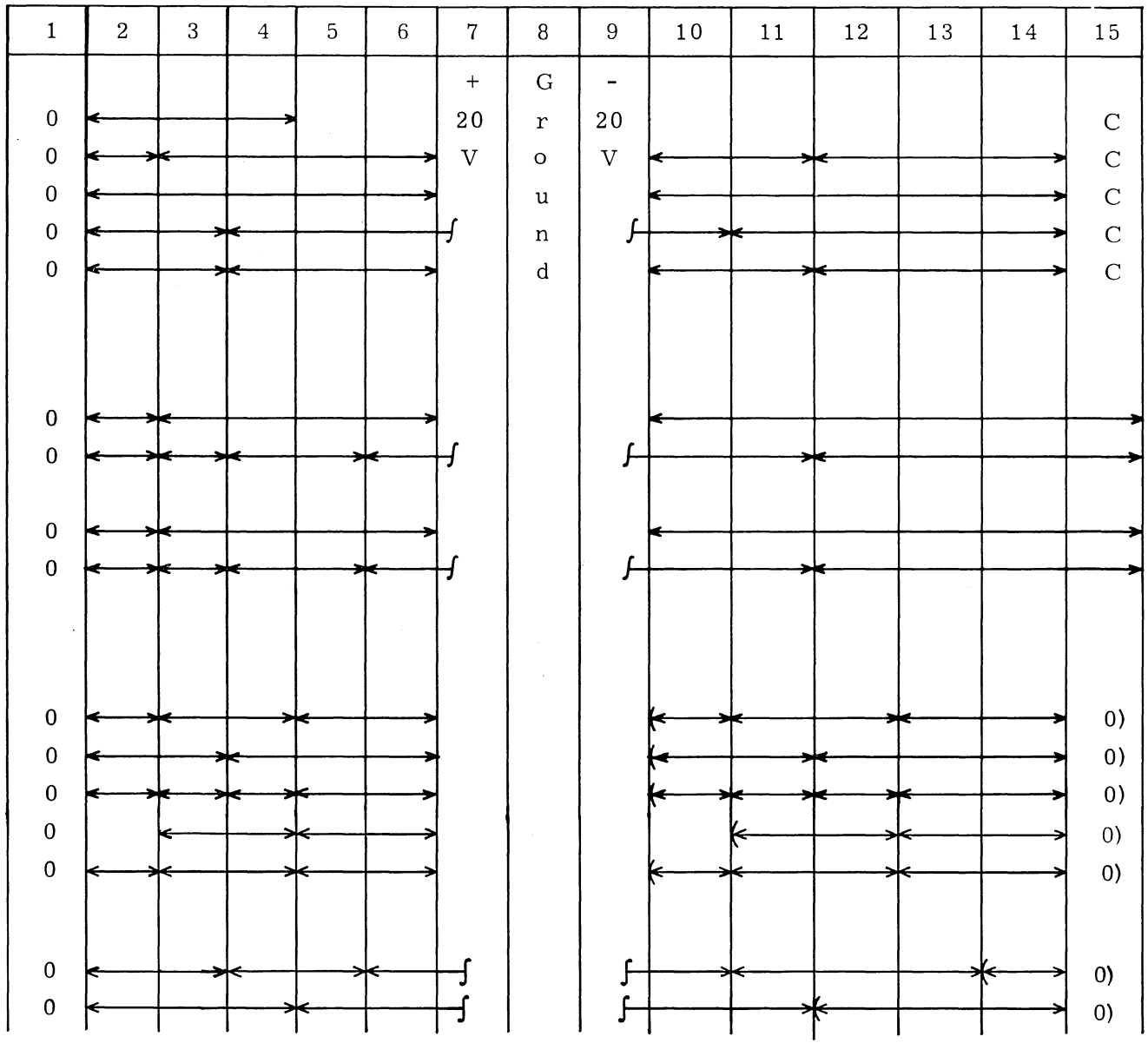
PRINTED CIRCUIT CARDS

X = Production discontinued.

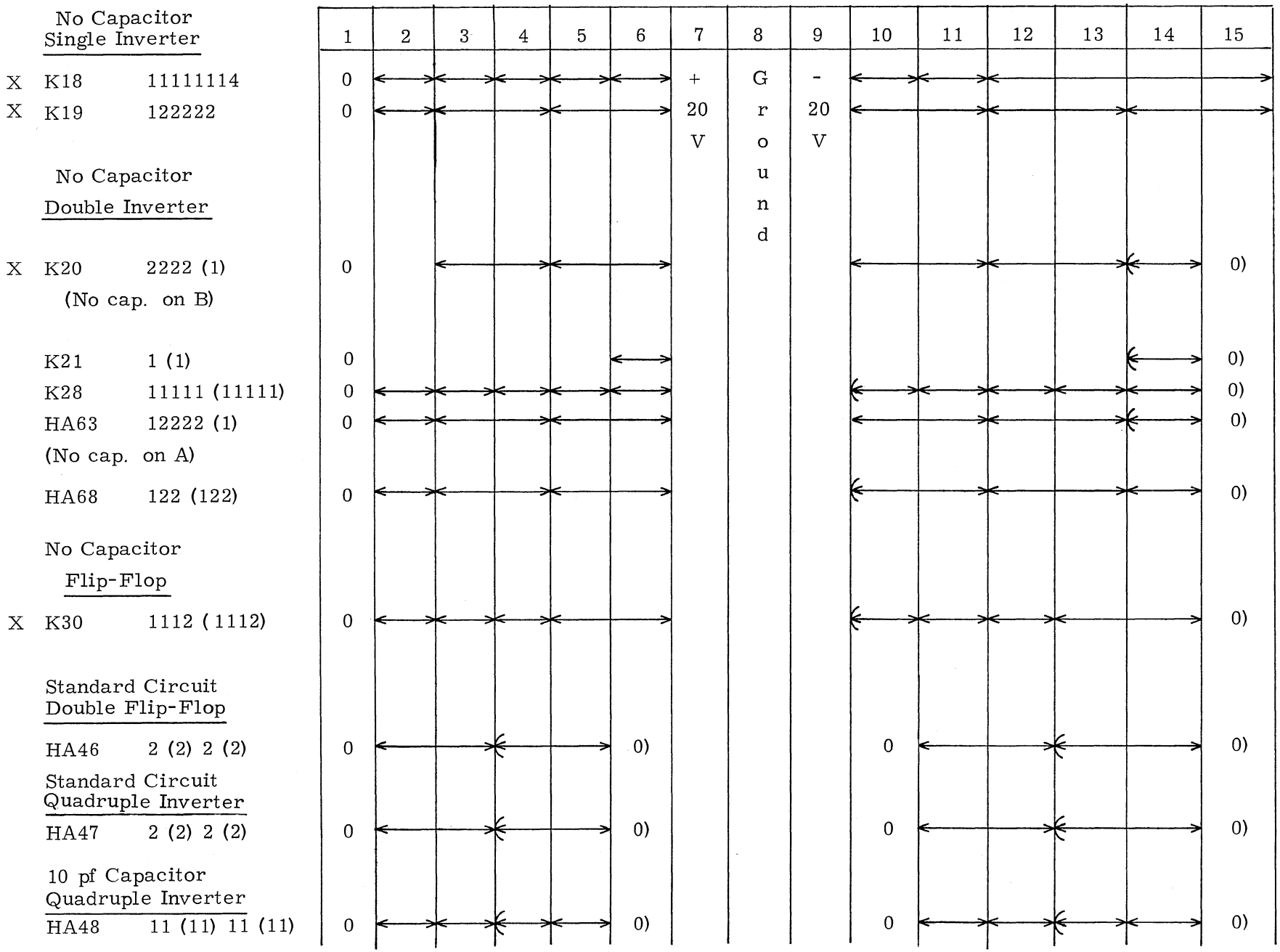
Do not use for new design.

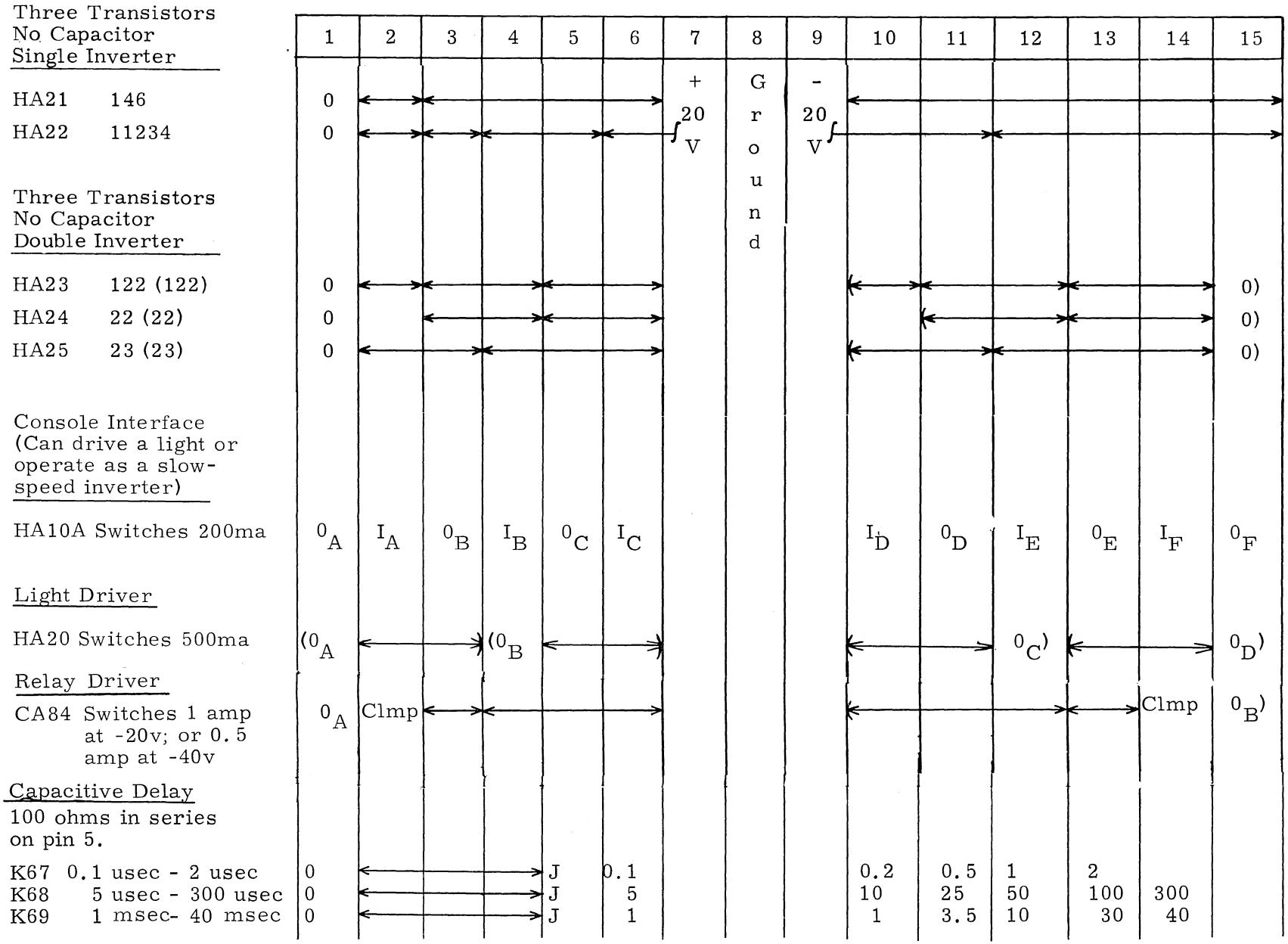

Standard Circuit Single Inverter
CA15 22223
CA52 236
CA55 344
K11 116
K12 146
K13 11234
K14 12233
K16 11111114
K17 122222
K51 155
K58 1235
Standard Circuit Double Inverter
CA21 5 (5)
CA28 222 (22)
HA05 2222 (1)
HA07 1 (1)
HA08 11 (11)
HA09 12 (12)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
0
+ 20 V
Ground
− 20 V
0)

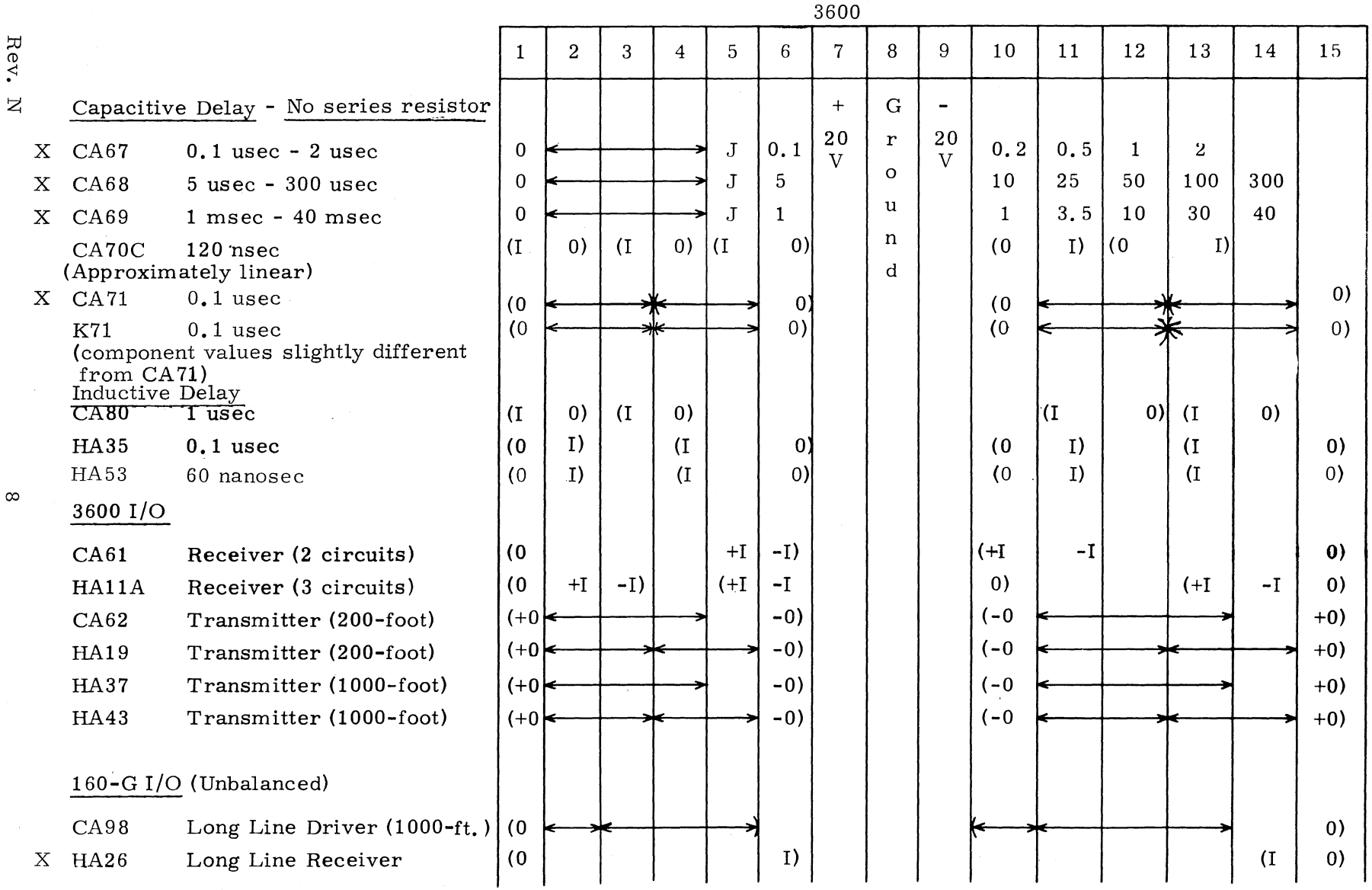

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
HA30 234 (1) 0 0)
+ G -
X K20 2222 (1) 0 20 r 20 0)
(No cap. on B) V o V
u
K22 122 (122) 0 n 0)
K23 33 (22) 0 d 0)
K24 1112 (1112) 0 0)
K25 11111 (11111) 0 0)
K26 113 (113) 0 0)
K27 14 (14) 0 0)
K29 12222 (1) 0 0)
HA63 12222 (1) 0 0)
(No cap. on A)
Standard Circuit Flip-Flop
X CA31 5 (5) 0 0)
X CA33 23 (23) 0 0)
CA35 34 (3) 0 0)
K31 5 (5) 0 0)
K32 122 (122) 0 0)
K33 23 (23) 0 0)
K34 1112 (1112) 0 0)
K35 34 (3) 0 0)
K36 333 (1) 0 0)
K37 2223 (1) 0 0)
K38 2 (1) 0 0)

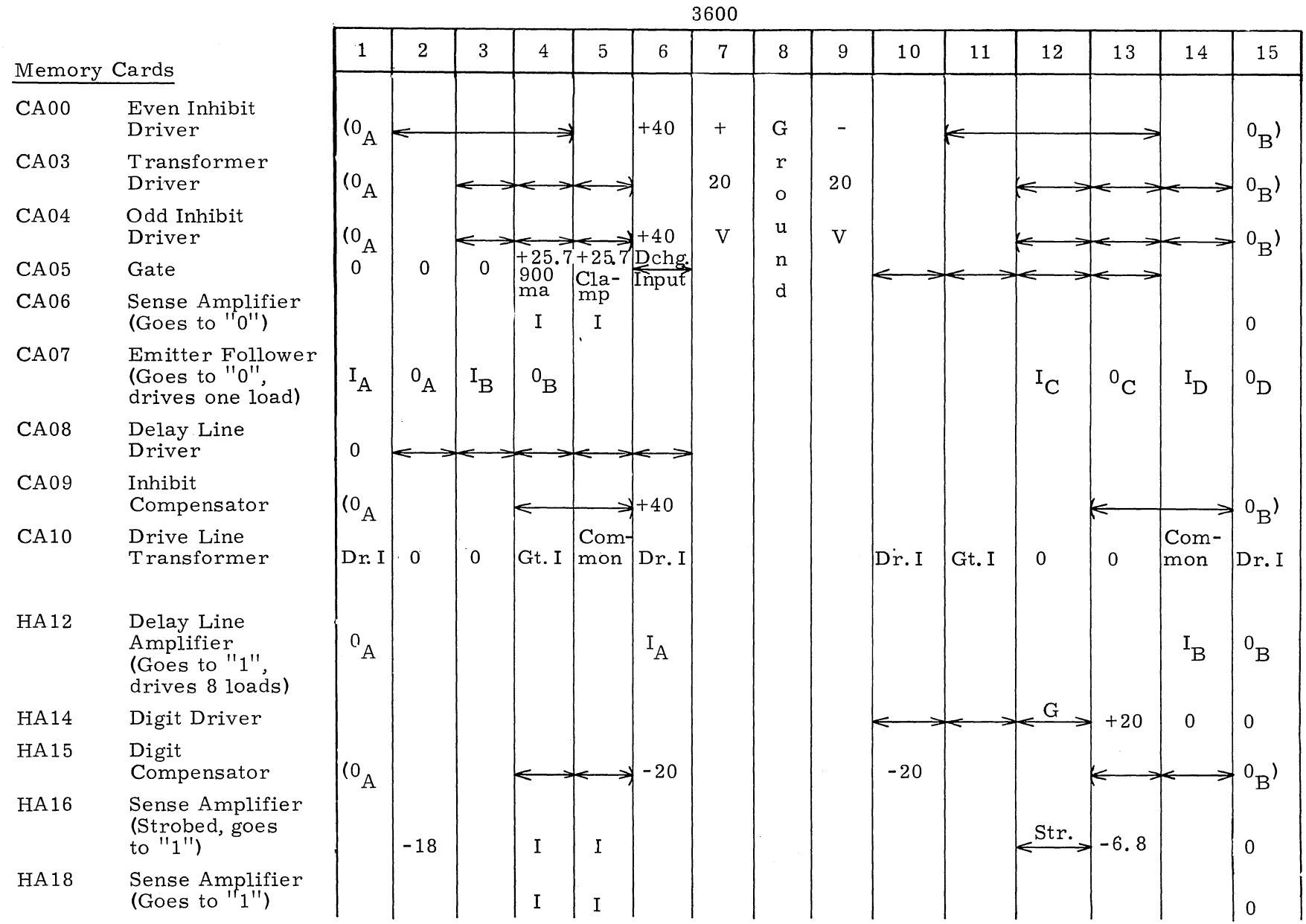

Standard Circuit Control Delay
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
+
G
-
CA40 3
0
20
r
20
C
CA44 1423
0
V
o
V
C
CA46 55
0
u
C
CA47 244
0
n
C
CA48 2323
0
d
C
10 pf Capacitor Single Inverter
X CA92 146
0
X CA93 11234
0
K92 146
0
K93 11234
0
10 pf Capacitor Double Inverter
X CA72 122, (122)
0
0)
CA73 23 (23)
0
0)
CA74 1112 (1112)
0
0)
HA06 22 (22)
0
0)
K72 122 (122)
0
0)
10 pf Capacitor Flip-Flop
HA66
0
0)
HA67 34 (3)
0
0)

3600


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
No Capacitor Single Inverter
X K18 11111114
X K19 122222
No Capacitor Double Inverter
X K20 2222 (1)
(No cap. on B)
K21 1 (1)
K28 11111 (11111)
HA63 12222 (1)
(No cap. on A)
HA68 122 (122)
No Capacitor Flip-Flop
X K30 1112 (1112)
Standard Circuit Double Flip-Flop
HA46 2 (2) 2 (2)
Standard Circuit Quadruple Inverter
HA47 2 (2) 2 (2)
10 pf Capacitor Quadruple Inverter
HA48 11 (11) 11 (11)
0
+ 20 V
Ground
- 20 V
0)


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Three Transistors No Capacitor Single Inverter
HA21 146
HA22 11234
+20 V
Ground
-20 V
Three Transistors No Capacitor Double Inverter
HA23 122 (122)
HA24 22 (22)
HA25 23 (23)
Console Interface (Can drive a light or operate as a slow-speed inverter)
HA10A Switches 200ma
0A IA 0B IB 0C IC ID 0D IE 0E IF 0F
Light Driver
HA20 Switches 500ma
(0A (0B 0C) 0D)
Relay Driver
CA84 Switches 1 amp at -20v; or 0.5 amp at -40v
0A Clmp Clmp 0B)
Capacitive Delay
100 ohms in series on pin 5.
K67 0.1 usec - 2 usec 0 J 0.1 0.2 0.5 1 2
K68 5 usec - 300 usec 0 J 5 10 25 50 100 300
K69 1 msec- 40 msec 0 J 1 1 3.5 10 30 40


3600
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Capacitive Delay - No series resistor
+ 20 V
Ground
- 20 V
X CA67 0.1 usec - 2 usec
0 J 0.1
0.2 0.5 1 2
X CA68 5 usec - 300 usec
0 J 5
10 25 50 100 300
X CA69 1 msec - 40 msec
0 J 1
1 3.5 10 30 40
CA70C 120 nsec (Approximately linear)
(I 0) (I 0) (I 0) (0 I) (0 I)
X CA71 0.1 usec
(0 0) (0 0)
K71 0.1 usec (component values slightly different from CA71)
(0 0) (0 0)
Inductive Delay
CA80 1 usec
(I 0) (I 0) (I 0) (I 0)
HA35 0.1 usec
(0 I) (I 0) (0 I) (I 0)
HA53 60 nanosec
(0 I) (I 0) (0 I) (I 0)
3600 I/O
CA61 Receiver (2 circuits)
(0 +I -I) (+I -I) 0)
HA11A Receiver (3 circuits)
(0 +I -I) (+I -I) 0) (+I -I)
CA62 Transmitter (200-foot)
(+0 -0) (-0 +0)
HA19 Transmitter (200-foot)
(+0 -0) (-0 +0)
HA37 Transmitter (1000-foot)
(+0 -0) (-0 +0)
HA43 Transmitter (1000-foot)
(+0 -0) (-0 +0)
160-G I/O (Unbalanced)
CA98 Long Line Driver (1000-ft.)
(0 0)
X HA26 Long Line Receiver
(0 I) (I 0)


3600
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Memory Cards
CA00 Even Inhibit Driver
CA03 Transformer Driver
CA04 Odd Inhibit Driver
CA05 Gate
CA06 Sense Amplifier (Goes to "0")
CA07 Emitter Follower (Goes to "0", drives one load)
CA08 Delay Line Driver
CA09 Inhibit Compensator
CA10 Drive Line Transformer
HA12 Delay Line Amplifier (Goes to "1", drives 8 loads)
HA14 Digit Driver
HA15 Digit Compensator
HA16 Sense Amplifier (Strobed, goes to "1")
HA18 Sense Amplifier (Goes to "1")
(0A
0B)
+40
+
20
-
20
Ground
V
V
0
+25.7 900 ma
+25.7 Clamp
Dchg. Input
I
0
IA
0A
IB
0B
IC
0C
ID
0D
Dr. I
Gt. I
Common
G
+20
-20
Str.
-6.8
-18

Clock	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Oscillator - Amplifier															
CA01 8 Megacycle HA50 6 Megacycle	LOGIC 0	TRAN. ←	SEC → 0	TANK 0		I	+ 20 V	Ground	- 20 V	I		TANK 0	TRANS. ←	SEC. → 0	LOGIC 0
Clock Regulator															
CA96 8mc Crystal HA49 6mc Crystal					O_A						O_B				
Crystal Oscillator															
CA81 30 Kilocycle CA82 83.3 Kilocycle CA83 120 Kilocycle	O_{LO}	O_{HI}													
HA00 3 Kilocycle		O													
Amplifier - Shaper															
CA89 0.2 usec "1" output on positive-going input	I														O
Tuning Fork Oscillator															
HA42 1 Kilocycle	O_A														O_B
Low Speed Oscillator															
HA33 (Negative Voltage on input varies repetition rate from 3 to 50 cps on 3200 Auto-Step)	O				I										O inv

Cards to Establish Signal Levels		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CA02	Clamp (All Pins held between -0.9v and -6.5v)	I	I	I	I	I	I	+ 20 v	Ground	- 20 v	I	I	I	I	I	I
CA63	Terminator (6 twisted-pair)	(+	-)	(+	-)	(+	-)				(+	-)	(+	-)	(+	-)
HA17	Filter (Series 680Ω, 4.7 uf shunt)	O_A	I_A	O_B	I_B	O_C	I_C				I_E	O_E	I_F	O_F	I_G	O_G
HA39	Line Terminator (Negative-going spikes clamped at -6.2V)	I	I	I	I	I	I				I	I	I	I	I	I
HA44	Ground (Outputs same as "clear" FF)	-6.2v "1"														Grd. "0"
HA45	Bias (All pins held at -5.8v)	"1"	"1"	"1"	"1"	"1"	"1"				"1"	"1"	"1"	"1"	"1"	"1"
HA69	Jumper (Connects pin 1 to pin 10, and pin 15 to pin 2)	•	•								•					•

1604

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
00	Clock Disconnect	I_A	I_A	I_A	I_A	I_A	I_A	I_B	I_B	I_B	I_B	I_B	I_B	20 V	Ground	+20 V
01	Oscillator	T_E	O_E	O_E	O_E	O_E	O_E	T_O	O_O	O_O	O_O	O_O	O_O			
02	Oscillator	T_E	O_E	O_E	O_E	O_E	O_E	T_O	O_O	O_O	O_O	O_O	O_O			
03	Crystal Oscillator, 30KC	O_{LO}	O_{HI}													
04	Amplifier Shaper	I				O	O	O	O	O	O	O	O			
05	Crystal Oscillator, 83.4KC	O_{LO}	O_{HI}													
06	Oscillator Amplifier	I_A	O_A	O_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	O_B	O_B			
07	Crystal Oscillator, 120KC	O_{LO}	O_{HI}													
11	Inverter	I				O	O	O	O	O	O	O	O			
12	Inverter	I	I			O	O	O	O	O	O	O	O			
13	Inverter	I	I	I		O	O	O	O	O	O	O	O			
14	Inverter	I	I	I	I	O	O	O	O	O	O	O	O			
15	Inverter	I	I	I	I	I	O	O	O	O	O	O	O			
16	Inverter	I	I	I	I	I	I	O	O	O	O	O	O			
20	Quadruple Inverter	I_A	O_A	O_A	I_B	O_B	O_B	I_C	O_C	O_C	I_D	O_D	O_D			
21	Double Inverter	I_A	O_A	O_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	O_B	O_B			
22	Double Inverter	I_A	I_A	O_A	O_A	O_A	O_A	I_B	I_B	O_B	O_B	O_B	O_B			
23	Double Inverter	I_A	I_A	I_A	O_A	O_A	O_A	I_B	I_B	I_B	O_B	O_B	O_B			
24	Double Inverter	I_A	I_A	I_A	I_A	O_A	O_A	I_B	I_B	I_B	I_B	O_B	O_B			
28	Triple Inverter	I_A	I_A	O_A	O_A	I_B	I_B	O_B	O_B	I_C	I_C	O_C	O_C			
29	Triple Inverter	I_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	I_C	O_C	O_C	O_C			
30	Double FF	I_A	O_A	O_A	I_B	O_B	O_B	I_C	O_C	O_C	I_D	O_D	O_D			
31	FF	I_A	O_A	O_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	O_B	O_B			
32	FF	I_A	I_A	O_A	O_A	O_A	O_A	I_B	I_B	O_B	O_B	O_B	O_B			
33	FF	I_A	I_A	I_A	O_A	O_A	O_A	I_B	I_B	I_B	O_B	O_B	O_B			
41	Control Delay	I					I_C	O	O	O	O	O	O			
42	Control Delay	I	I				I_C	O	O	O	O	O	O			
43	Control Delay	I	I	I			I_C	O	O	O	O	O	O			
44	Control Delay	I	I	I	I		I_C	O	O	O	O	O	O			

1604

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
45	Control Delay	I	I	I	I	I	I_C	O	O	O	O	O	O	- 20 V	Ground	+ 20 V
50	Capacitor	I	I	I	I	I	I	I	I	I	I	I	I			
51	Drive Generator	I			I			I			O	O	O			
52	Diverter	O	O	O	O	O	O	O	O		I	I	I			
53	Selector	I_A	I_A	O_A	O_A	O_A	O_A	I_B	I_B	O_B	O_B	O_B	O_B			
54	Current Source	I		I		I		I		I						
55	Inhibit Generator	I_A					O_A	I_B					O_B			
56	Sense Amplifier	M	I		I								O			
57	Sense Amplifier	M	I		I		B						O			
58	Inhibit Generator	I_A					O_A	I_B					O_B			
59	Inhibit Generator	I_A					O_A	I_B					O_B			
60	Output	I_A	I_A	I_A	O_A	I_B	I_B	I_B	O_B	I_C	I_C	I_C	O_C			
61	Input	I_A		O_A	O_A	I_B		O_B	O_B	I_C		O_C	O_C			
62	Output	I_A		O_A		I_B		O_B		I_C		O_C				
63	Line Driver	I				O										
64	Modified Input	I									O					
65	Speaker Driver	I											O			
66	Punch Puller	I											O			
67	Output	I_A	I_A	O_A		I_B	I_B	O_B		I_C	I_C	O_C				
68	Input	I_A		O_A	O_A	I_B		O_B	O_B	I_C		O_C	O_C			
69	Output	I_A		O_A		I_B		O_B		I_C		O_C				
70	Read Amplifier	I		B						O	O	O	O			
71	Tape Preamplifier	I_A	I_B									O_A	O_B			
72	Tape Amplifier	M	I		I								O			
73A	Variable Delay	I	O	O	O	O	O	O	O	O	O	O	O			
74	Tape Current Source	I		I		I		I		I						
75	Reader Level Amplifier	I_A	B_A	O_A	I_B	B_B	O_B	I_C	B_C	O_C	I_D	B_D	O_D			
75A	Reader Level Amplifier Brake	I_A	I_B	I_C	I_D	O_A	O_B	O_C	O_D							
76 A	Reader Brake Clutch Driver	I				O		O			O		O			

1604

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
77	Variable Delay	I					O	O	O	O	O	O	O	- 20 V	G r o u n d	+ 20 V
78	Input	I_A	O_A	O_A			I_B	O_B	O_B							
79	Output	I_A		O_A	O_A	B	B	I_B		O_B	O_B	B	B			
80	Long line Receiver, 160	I_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	I_C	O_C	O_C	O_C			
81	Voltage Divider	I	I					O	O	O						
82	Variable Delay	I	O	I	O	I	O	I	O	I	O	I	O			
83	Memory Test	I	I	I	I	O		O	O		I	O	O			
84	Load Simulator	I	I		I	I	O	I	O	I	O	I	I			
85	Magnet Puller	I_A	I_A	O_A		I_B	I_B	O_B		I_C	I_C	O_C	C			
86	Punch Puller	I_A		O_A		I_B		O_B		I_C		O_C				
87	Input	I_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	I_C	O_C	O_C	O_C			
88	Steered FF	I_A	I_A	O_A		O_A	I_A	I_A		I_B	I_B	I_B	O_B			
89	Sheffer Stroke Gate	I_A	I_A	I_A	O_A	I_B	I_B	I_B	O_B	I_C	I_C	I_C	O_C			
90	OR	O	I	I	O	I	I	O	I	I	O	I	I	O	I	I
91	Hammer Storage	I_A	I_A	I_A	I_A		I_B	I_B			G	C	O			
92	Reader Level Amplifier	I_A	I_B	I_C	I_D	O_A	O_B	O_C	O_D							
93	Long Line Transmitter, 160	I_A		O_A		I_B		O_B		I_C		O_C				
94	Long Line Transmitter, 160	I_A	I_A	O_A		I_B	I_B	O_B		I_C	I_C	O_C				
95	Long Line Transmitter, 160	I_A	I_A	I_A	O_A	I_B	I_B	I_B	O_B	I_C	I_C	I_C	O_C			
96	Clock Driver	I_A	O_A	O_A	I_B	O_B	O_B	I_C	O_C	O_C	I_D	O_D	O_D			
97A	Delay	I_A	I_A	I_A	O_A	O_A	O_A	I_B	I_B	I_B	O_B	O_B	O_B			
98	Drive Generator	I_A			I			I_B			O	O	O			
99	Long Line Receiver 160G	I_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	I_C	O_C	O_C	O_C			
101	Amplifier Shaper	I				O	O	O	O	O	O	O	O			
102	Crystal Oscillator, 480KC		O													
103	Crystal Oscillator, 1334.4KC		O													
104	Crystal Oscillator, 1920KC		O													
105	Crystal Oscillator, 240KC		O													
106	Crystal Oscillator, 667.2KC		O													
107	Crystal Oscillator, 960KC		O													

	1604												ALL CARDS		
													-20V	GND	+20V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
108 Long Line Driver, 160G	I_A		O_A		I_B		O_B		I_C		O_C				
109 Long Line Driver, 160G	I_A	I_A	O_A		I_B	I_B	O_B		I_C	I_C	O_C				
110 Long Line Driver, 160G	I_A	I_A	I_A	O_A	I_B	I_B	I_B	O_B	I_C	I_C	I_C	O_C			
111 Current Source	I		I		I		I		I						
112 Capacitor (All 0.001 uf)	I	I	I	I	I	I	I	I	I	I	I	I			
114 Sense Amplifier	M	I		I		B						O			
Transistors CDC 118021															
116 Single Inverter	I				O	O	O	O	O	O	O	O			
117 Single Inverter	I	I			O	O	O	O	O	O	O	O			
118 Double Inverter	I_A	O_A	O_A	O_A	O_A	O_A	I_C	O_C	O_C	O_C	O_C	O_C			
119 Triple Inverter	I_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	I_C	O_C	O_C	O_C			
120 Flip Flop	I_A	I_A	I_A	O_A	O_A	O_A	I_C	I_C	I_C	O_C	O_C	O_C			
121 Transmitter	(I				-O	+O)	(I				-O	+O)			
139 Triple Inverter	I_A	I_A	O_A	O_A	I_B	I_B	O_B	O_B	I_C	I_C	O_C	O_C			
140 Double Inverter	I_A	O_A	O_A	O_A	O_A	O_A	I_B	O_B	O_B	O_B	O_B	O_B			

Type	Title	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Schematic Number
							DISC FILE										
P01	Read Switch	I_A				O_A	O_A	I_A			O_C	O_C					YC2231201
P02	Sense Amplifier-Preamplifier	I	GND	I									O				YC2231202
P03	Sense Ampl. Pk. Dct. and Pulseformer	I															YC2231203
P04	Threshold Detector	I					O										YC2231204
P05	Head Equalization Network	I	I			O	O										YC2231205
P06	Current Source																YC2231206
P07	Head Switching Diodes																YC2231207
P08	Driver	I						I									YC2231208
P09	Current Source Dummy																YC2231209
P10	Head Switch	I	I	I	I	I											YC2231210
P11	Gated Pulse Amplifier																YC2231211
P12	Transformer																YC2231212
P13	Delay	I_A	O_A	I_B	O_B	I_C	O_C	I_D	O_D	I_E	O_E	I_F	O_F				YC2231213
P14	Transmitter	I_A				O_A	O_A	I_C				O_C	O_C				YC2231214
P15	Transmission Line Terminal																YC2231215
P16	Receiver	I_A	I_A	O_A	O_A	O_A	O_A	I_C	I_C	O_C	O_C	O_C	O_C		GND		YC2231216
P17	Solenoid Termination														GND		YC2231217
P18	Voltage Protection												$+40_L$	N.C.	GND	N.C.	YC2231218
P19	Single Inverter	I	I	I	I	I	I	O	O	O	O	O	O				YC2231219
P20	Osc. and Ampl. Buffer																YC2231220
P21	Terminator																YC2231221
							LINE PRINTER										
P51	Memory Driver	I	I	I	I		O						Cap. GND				YC2231251
P52	Memory Diverter	I	I	I	I	O	O	O	O	O	O	O	O				YC2231252
P54	Power Supply Filter and Jump.										I	I	I	I	I	I	YC2231254
P55	Power Supply Filter and Jump.												I				YC2231255
P56	Sense Amplifier	I_A	I_A	O_A	I_B	I_B	O_B	I_C	I_C	O_C	I_D	I_D	O_D				YC2231256

Type	Title	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Schematic Number
						LINE PRINTER											
P91	Hammer Driver	J				J		J									YC2231291
P92	Hammer Driver			O	O	J		J	J		I	O	O				YC2231292
P93	Pulse Shaper		I_A	O_A	O_A		I_B	O_B	O_B		I_C	O_C	O_C				YC2231293
P94	Ribbon Advance	O	O							I							YC2231294
P95	Brake-Clutch One-Shot	O	T	T							I						YC2231295
P96	Ribbon Drive and Hold	O	O	I	I		O	O									YC2231296
P97	Hammer Driver One-Shot	I	I										O				YC2231297
P98	Hammer Driver One-Shot																YC2231298
P99	Brake-Clutch One-Shot	I	T	T		OPCONCTR		O	O	O	O	O	O				
E00	Jumper	See Schematic															
E01	Crosspoint Control	See Schematic															YC2071201
E02	Crosspoint Control	See Schematic															YC2071201
E03	Crosspoint Control	See Schematic															
E04	Crosspoint Control	See Schematic															YC2071204
E05	Decoder	See Schematic															
E06	Resistor Assembly	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	YC2071206
E07	Resistor Assembly	I	I	I	I	I	I	I	I	I	I	I	I	I			YC2071207
E08	Single Pulser	I						O	O	O	O	O	O				YC2071208
E10	Integrator	I	I	I	I	I	I	I	I	I	I	I	I	-6v	GND		YC2071210
E11	Delay	I	I	I	I	I	I	I	I	I	I	I	I				YC2071211
E12	Line Driver	I_A	I_A				O_A	I_B	I_B				O_B				YC2071212
E13	Line Receiver	I_A				O_A	O_A	I_B				O_B	O_B				YC2071213
E14	Variable Clock	O_A		J_A		J_A		O_C		J_C		J_C					YC2071214
E15	Line Driver	I_A			O_A			I_B			O_B						YC2071215
E16	Line Receiver																YC2071216
E19	Terminator	I			T_A		T_B		T_C		T_D		T_E				2071219
E20	Resistor Assembly	I	I	I	I	I	I	I	I	I	I	I	I				2071220
E61	Receiver	I_A		O_A	O_A					I_B		O_B	O_B				YC2071261
E62	Driver	I_A		O_A						I_B		O_B					YC2071262
E67	Driver	I_A	I_A	O_A						I_B	I_B	O_B					YC2071267

Type	Title	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Schematic Number
CM00	Universal Matrix																
CM01	Clock Oscillator Amplifier																YC234805
CM02	Bipolar Amplifier																YC234808
CM03	Transmitter Amplifier																YC234811
CM04	Receiver Amplifier																YC234814
CM05	Low Frequency Oscillator																YC234817
CM06	Phase Splitter																YC234820
CM07	Speaker Driver																YC234823
CM08	Frequencey Switch																YC234826
CM09	Volt Phase Splitter																YC234829
CM10	Low Differential Amplifier																YC234832
CM11	Data Line Driver																YC234835
CM12	One Shot Delay																YC234838
CM13	High Differential Amplifier 1																YC234841
CM14	High Differential Amplifier 2																YC234844
CM15	Low Differential Amplifier																YC234853
CM16	High Differential Amplifier																YC234856

MICROWAVE

Type	Title	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Schematic Number
M01	Bipolar Threshold Amplifier																YC234402
M02	Wideband Amplifier																YC234406
M03	Transmitter																YC234410
M04	Receiver																YC234414
M05	Call Circuit																YC234418
M06	Filter																YC234422
M07	Filter																YC234426
M08	Equalizer																YC234429
M09	Delay Card																YC234433
M10	Clock Oscillator																YC234437
M12	Single Inverter																YC234445
M62	Output																YC234449
M63	Line Driver																YC234453
M64	Line Receiver																YC234456
M73	Delay																YC234459

Type	Title	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Schematic Number
CC10	Relay	I	O	O	O			I	O	O	O			*	*	*	
CC21	Inverter	I	O	O	O	O	O	I	O	O	O	O	O				
CC21A	Inverter	I	O	O	O	O	O	I	O	O	O	O	O				
CC22	Inverter	I	I	O	O	O	O	I	I	O	O	O	O				
CC22A	Inverter	I	I	O	O	O	O	I	I	O	O	O	O				
CC23	Inverter	I	I	I	O	O	O	I	I	I	O	O	O				
CC23A	Inverter	I	I	I	O	O	O	I	I	I	O	O	O				
CC25	Inverter	I	O	O	I	O	O	I	O	O	I	O	O				
CC25A	Inverter	I	O	O	I	O	O	I	O	O	I	O	O				
CC31	Flip Flop	I	O	O	O	O	O	I	O	O	O	O	O				
CC31A	Flip Flop	I	O	O	O	O	O	I	O	O	O	O	O				
CC32	Flip Flop	I	I	O	O	O	O	I	I	O	O	O	O				
CC32A	Flip Flop	I	I	O	O	O	O	I	I	O	O	O	O				
CC33	Flip Flop	I	I	I	O	O	O	I	I	I	O	O	O				
CC33A	Flip Flop	I	I	I	O	O	O	I	I	I	O	O	O				
CC35	Dual FF	I	O	O	I	O	O	I	O	O	I	O	O				
CC35A	Dual FF	I	O	O	I	O	O	I	O	O	I	O	O				
CC61	Input	I		O	O	I		O	O	I		O	O				
CC62	Output	I		O		I		O		I		O					
M62	Output	I		O		I		O		I		O					
CC64	Input	I		O	O					I		O	O				
CC82-1	Delay 6 usec	O	O	O	O	O	O	O	O	O	O	O	O				
CC82-2	Delay 25 usec	O	O	O	O	O	O	O	O	O	O	O	O				
CC82-3	Delay 120 & 545 usec	O		O		O		O		O		O					
CC82-4	Delay 3, 5 & 11 MS	O	O	O	O	O	O	O	O	O	O	O	O				
CC82-5	Delay 27 & 54 usec	O		O		O		O		O		O					

* Unless otherwise noted: pin 13 equals -20v; pin 14 equals ground; pin 15 equals +20v.

Type	Title	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Schematic Number
CC82-6	Delay 0.15 & 0.35 usec	O	O	O	O	O	O	O	O	O	O	O	O	*	*	*	
CC82-7	Delay 1 and 2 usec	O	O	O	O	O	O	O	O	O	O	O	O				
CC82-8	Diode Limiter and Delay	I	O			O	O	O	O		O		O				
CC82-9	Diode	O	O	O	O	O	O	O	O			I					
CC82-10	Jumper	←		→		→		→		→		→					
CC82-11	Delay	G	I				O										
CC83	Adjustable Delay	I	O	O		C		I	O	O		C					
CC83A	Adjustable Delay	I	O			C		I	O			C					
CC84-1	Delay 27 MS	O		O		O	O	O		O	O	O	O				
CC100A	Push-Pull Amplifier	I		I								O	O				
CC100B	Rectifier	I							O								
CC100C	Phase Shifter	I				O	O	O	I	O	O	O	O				
CC100D	Modulator	I			I					I	O	O					
CC101	Class "A"		I	I	O	O				I	I	O	O				
CCLR	Relay/Lamp Driver	I		O		I		O		I		O					
P01	Read Switch	I		Sig. I	Sig. I	Sig. O	Sig. O	I	Sig. I	Sig. I	Sig. O	Sig. O	+40				
P02	Sense Amplifier	I	Gnd	I									O				
P03	Sense Amp., Pk. Det. and Pulse Former	Sig. I					Gate O					Sig. O	Sig. O				
P04	Threshold & Coin. Det.	Gate I	Sig. I	Sig. I		O	O	O	O	O	O	O	O				
P05	Head Equalization	O	O			I	I						+40				
P06	Current Source	O	O	O							O	O	O				
P07	Head Switching Diodes	O	Gnd	O	I	I	I	I	I	I	I	I	Gnd				
P08	Driver	Gate I					Write Curr. O	Write Curr. Source				Write Curr. O	Write Curr. Source				
P09	Current Source Network	Gate I					Curr. O	Gate I					Curr. O				
P10	Head Switch	I	I	I	I	I			O	O	O	I	+40				
P11	Gated Pulse	Sig. I	Gate I	O	O	O	O	Sig. I		O	O	O	O				
P18	Voltage Protection	O	O	O	O	O	O	O	O				+40				

* Unless otherwise noted: pin 13 equals -20v; pin 14 equals ground; pin 15 equals +20v.

PERIPHERAL EQUIPMENT GROUP LOGIC CARD INDEX

	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
ABA	46278200 46278300 46278400	Relay Puller (special for opcon)	Logic "0" Logic "1"	-36V OFF 0.5V at .6A	2 circuits For terminations to -36V or less.
ACA	46514601 46514701 46514801	Photocell Amp. (Card Reader)	Photocell (-) Photocell (+)	OFF -1/4V at 10 MA	3 circuits/card
ADA	50000400 50000500 50000600	Hammer Driver (Printer)	Logic "0" Logic "1"	-1V at 10A -36V OFF	5% max. duty cycle For terminations to -36V or less.
ADB	50000400 50000501 50000601	Hammer Driver (Printer)	Logic "0" Logic "1"	-1V at 6A -36V OFF	ADA Version 2 2% max. duty cycle
ADC	50000402 50000502 50000602	Hammer Driver (501 Printer)	Logic "0" Logic "1"	-2V at 5A -36V OFF	4% max. duty cycle For terminations to -36V or less. Being replaced by ADF
ADD	50000402 50000503 50000603	Hammer Driver (Printer)	Logic "0" Logic "1"	-1.5 V at 7A -36V OFF	ADC with Zener Suppression Emergency fix for Anelex head. Fuse drop is additional. Use ADG for future design.
ADE	50000404 50000504 50000604	Hammer Driver (Printer)	Logic "0" Logic "1"	-1.5V At 7A -36V OFF	ADD with fwd. drop spec and echo check resistor Being replaced by ADG
ADF	Design Underway	Hammer Driver (501 Printer)	Logic "0" Logic "1"	-2V @5A -36V OFF	ADC with 2.2K instead of 6.8K input termination to -20V
ADG	Design Underway	Hammer Driver (501 Printer)	Logic "0" Logic "1"	-1.5V @7A -36V OFF	ADE with 2.2K instead of 6.8K input termination to -20V
ADH	50000407 50000507 50000607	Clutch Driver (501 Printer)	Logic "0" Logic "1"	-1.6V @15A -40 V OFF	Requires space of 2 standard cards due to heat sink

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
AEA	50003400 50003500 50003600	Output Driver (OEM Tag Tape for NCR)	Logic "0" Logic "1"	-8V Clamp -1V at 85MA	3 circuits Not for production use AEB below
AEB	50005800 50005900 50006000	Output Driver (OEM Mag. Tape for NCR)	Logic "0" Logic "1"	-8V Clamp -1V at 85MA	3 Circuits Requires external line termination
AFA	50007900 50008000 50008100	Delay Card (Mag. Tape)	Logic "0" Logic "1" Enable -15V	Logic "0" delayed Logic "1" Selects potentiometer	1 - 50 μsecs delay. Enable input Matches AGA output
AFB	50007900 50008001 50008100	Delay Card (Mag. Tape)	Logic "0" Logic "1" Enable -15V	Logic "0" delayed Logic "1" Selects potentiometer	1 - 50 μsecs delay on "0" Improved AFA
AGA	50004900 50005000 50005100	Selector (Mag. Tape)	Logic "0" Logic "1"	-15V @ 25MA 0V OFF -15V Ref @25MA	3 circuits Delay group selector for AFA/AFB
AHA	50010000 50010100 50010200	Driver Flip-Flop (Optical Reading Machine)	Shift =+12V pulse Enable = -1V Disable = -12V	Set= -12V @20MA Clear= -1V @ 20MA	Flip-Flop for single rank shift register and matrix driver Use AIA driver. Drawings at Rabinow.
AHB	Obsolete	Use AIA circuit			
AHC	50010001 50010101 50010200	Driver Flip-Flop (Optical Reading Machine)	Shift = +12V pulse Enable= -1V Disable= -12V	Set= -12V @ 20MA Clear = -1V @ 20 MA	Low Cost version of AHA Design at Rabinow Drawings at Rabinow

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
AIA	50010300 50010400 50010500	Shift Driver (Optical reading machines)	"0" -1/2V "1" -3V "1" = -5.5 to -16V	-12V @ 45MA -3/4V @25MA -1V @70MA	3 circuits with 3.3K input resistor. Requires -12V Zener clamp.
AIB	50010301 50010401 50010500	Shift Driver (Optical reading machines)	"0" -1/2V "1" -3V "1" = -5.5 to -16V	-12V@ 45MA -3/4V @25MA -1V @ 70 MA	Low cost version of AIA Design at Rabinow
AJA		Photocell AMP			
AKA	50010900 50011000 50011100	Photocell Amp (350 PTR)	Photocell (+) Photocell (-)	-1/4V @10MA OFF	3 circuits
ALA	50011200 50011300 50011400	Power Supply (807/808 File, Function Generator)	60 cps 40V rms Center-tapped	+9.1V @-0-18 MA -9.1V @0-18 MA	Operates from 60 cps transformer
AMA	Obsolete				USE AMB, AMC, AMD, or AME
AMB	50011501 50011601 50011701	Erase/Write Driver (852 disk Drive)	Logic "0" Logic "1"	0V OFF 100 ma @+30V each ckt	2 circuits, only one on at a time. +40V on pin 15. Drives toward + only
AMC	50011502 50011602 50011702	Erase/Write Driver (853 Disk Drive)	Logic "0" Logic "1"	0V OFF 150 ma @ +35V Each Ckt	Similar to AMB
AMD	50011501 50011603 50011703	Write Driver (807/8 Disk File)	Logic "0" Logic "1"	0V OFF 125 ma @+35V Each ckt	Similar to AMB and AMC
AME	50011501 50011604 50011704	Erase Driver (807/8 Disk File)	Logic "0" Logic "1"	0V OFF 300 ma @ +16V each ckt	2 circuits. Both should be on at the same time. Drives toward + only.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
ANA	50011800 50011900 50012000	Head Select & write error check (852 & 853 disk drive)	1) 4 ma toward gnd @+40V for each head select on; 2) +30V to +35V from Erase/Write Drivers	Logic "0" Logic "1"	+40V on pin 15
ANB	50011800 50011901 50012001	Head Select & Write Error Check (807/8 Disk File)	1) +35V from write driver; 2) 0.4 ma toward gnd for each Head Select on	1) Logic "0" Logic "1" 2) +22V for AOA card	+40 on pin 15. Used with AOA
ANC	50011800 50011902 50012002	Erase Error Check (807/8 Disk File)	+16V from Erase Driver	Logic "0" Logic "1"	Used to check AME
AND					
AOA	50012100 50012200 50012300	Head Select Check (807/8 Disk File)	1) +16V from each Head Select turned on 2) +22V from AOA	0.4 ma toward gnd for each Head Select on	+40V on pin 15. Used with ANB.
APA					
AQA		Input Amplifier	+0.5V -0.5V	Logic "0" Logic "1"	1 circuit - matches IQA
		Output Amplifier	Logic "0" Logic "1"	+1½V OFF -3½V at 50 MA	1 circuit - matches OPA Drives toward - only Requires -4V on Pin 7
ARA	Design Underway	Driver Flip-Flop (Optical Reading)	Shift= +12V pulse Enable= -1V Disable= -12V	Set= -12V at 100 MA Clear=-1V at 100 MA	Higher drive than AHA Requires -12V power
ASA	50013301 50013400 50013500	Quantizer - Output amplifier (Optical Reading)	|Analog| >|Ref|** |Analog| < |Ref| |Analog| > |Ref|	0V OFF * +2V at 17MA +3V at 15MA	3 circuits, Matches OSB *Includes internal 120 termination to ground. Reference range -1 to -10V. Analog range -½ to -15V

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
ATA	50013600 50013700 50013800	Gated Read Amplifier (852 Disk Drive)	1) 5mv p-p 1 mc analog 2) +8V gate input	Analog	Requires +12V on pin 15 -12V on pin 13 Adjustable gain
ATB	50013600 50013701 50013801	Gated Read Amplifier (853 Disk Drive)	1) 5mv p-p 1 mc analog 2) +8V gate input	Analog	Requires +12V on pin 15 -12V on pin 13 Adjustable gain
AUA	50013900 50014000 50014100	Power Supply Regulator (807/808 File, Operational Amplifier)	+20VDC -20 VDC	+15 VDC @ 0-30 MA -15 VDC @ 0-30 MA	Two +15V Circuits Two -15V circuits
AVA	50014200 50014300 50014400	Write Resistor Diode Card (807/8 Disk File)	0 to +35V	Input via 275Ω & Series diodes to drive mag. head	Two complete circuits each with four isolating diodes Input matches AMD etc.
AWA	Not to be released	Voltage sensor- Relay Puller (807/8 Disk File)	No external inputs (Monitors Power Supply Voltages)	OV out if voltages are not too close to OV. Open if voltages are too close to OV.	Three outputs, +40V on Pin 12
AXA					
AXB					
AYA	50015100 50015200 50015300	Voltage Check (852/3 Disk Drive)	1) Logic (Pin 1) 2) +20V supply via 17.6V Zener (Pin 2)	1) Logic 2) 0.8A at +1.0V	+40V on pin 15. Used with GAA Card. Pin 2 Input matches GAA circuit
AZA					

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comment
BAA	50058300 50058400 50058500	Voltage Sensor (807/8 Disk File)	1) +20V supply via 17.6V Zener (Pin 1) 2) Logic, Pin 2	1) Logic 2) On = +0.2V OFF = open	+20V or +40V on pin 15. Pin 1 Input Matches GAA pin 11 Pin 2 Input Matches BAB pin 11 or 12 Pin 7 Output Matches BBA, Pin 1
BAB	50058300 50058401 50058501	Voltage Sensor (807/8 Disk File)	+20V Supply Via 17.6 Zener	1) Logic	Input Matches GAA pin 11 Output matches BAA Pin 2.
BBA	50058600 50058700 50058800	Voltage Sensor Amplifier (807/8 Disk File)	ON = +0.2V OFF = Open	ON -200 MA to Gnd OFF Gnd	+20V or +40V on Pin 15 Input matches BAA Pin 7 Output to six BCA's, Pin 1. Pin 10 via external 120Ω to +20V or +40V
BCA	50058900 5005900 0 50060000	Erase/Write Current Sink (807/8 Disk File)	ON = +16V OFF = Ground	OFF ON = 0.8A @ +1.0V	+20V or +40 V on Pin 15 Input matches BBA Pin 12.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
EDA	46278500 46278600 46278700	Read Level Detector (Mag.Tape)	40MV p-p 40 KC	1. Class A 2. Rect. (positive) 3. Logic "1" (level detection)	Preamp, etc. #1 for Mag.Tape
EEA	46281200 46281301 46281101	Resistor Termination (Mag.Tape)	Res.Term.	Res.Term	6.8K to -20V Pins 1-12
EEB	46281200 46281302 46281102	Capacitor Termination (Mag.Tape)	Cap.Term.	Cap. Term.	1000 pf Pins 1-2 2000 pf Pins 3-8 10,000 pf Pins 9-12
EEC	46281200 46281303 46281103	Cap. Termination (Mag.Tape)	Cap.Term.	Cap. Term.	3.3 mfd Pins 1-2 6.8 mfd Pins 3-8 15 mfd Pins 9-12
EED	46281200 46281304 46281104	Resistor Term. (Mag.Tape)	Res. Term.	Res. Term.	680 ohms to -20V pins 1-12
EEE	46281200 46281305 46281105	Capacitor Termination (Mag.Tape)	Cap.Term	Cap. Term	220 pf Pins 1-12
EEF	46281200 46281306 46281106	Resistor Term (Mag. Tape Exerciser)	Res. Term	Res. Term	120 ohms to gnd. Pins 1-12
EEG	46281200 46281307 46281107	Resistor Term (Disk Drive)	Res. Term.	Res. Term.	510 ohms to +20V Pins 1-12

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
EEJ					
EEK	46281200 48304100 48304000	Resistor Term (915 Page Reader)	Res. Term.	Res.Term.	560 ohms to +20V Pins 1-12 Drawings @ Rabinow
EEL	46281200 48302900 48302800	Capacitor Term (915 Page Reader)	Cap.Term.	Cap. Term.	1 mfd Pins 1-3 1.5mfd Pins 4-6 2.2 mfd Pins 7-8 3.3 mfd Pins 10-12 Drawings @ Rabinow
EEM	46281200 48302600 48302700	Resistor Term (915 Page Reader)	Res. Term.	Res. Term.	10K to -20V Pins 1-12 Drawings @ Rabinow
EEN					
EEO	46281200 48303100 48303000	Capacitor Term (915 Page Reader)	Cap.Term.	Cap.Term.	2.2 mfd Pins 1-3 4.7 mfd Pins 4-6 22 mfd Pins 7-9 180 mfd Pins 10-12 Requires two card spaces Drawings @ Rabinow

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
EFA	46529001 46529101 46529201	Clock Amplifier (Card Reader)	400-1200 MV P-P, 40KC	Std. Logic	Signal from Magnetic Pick-up
EGA	50001000 50001100 50001200	Read Level Detector (Mag.Tape)	20 -40MV p-p 40KC	1. Class A 2. Rect (positive) 3. Level Detect Std. logic "1" (level detection)	Preamp etc. #2 for Mag.Tape Not for future use. Use EH.. and E.. in combination.
EHA	50002801 50002901 50003001	Read Pre-amp (Mag.Tape)	10 -50MV p-p 60 KC	Balanced Class A 8V p-p Each side	Preproduction EHB Not for design use.
EHB	50008500 50008600 50008700	Read Pre-amp (Mag.Tape)	8-40MV p-p 60KC	Balanced Class A 8V p-p each side	Preamp for Mag.Tape
EHC	50008501 50008601 50008701	Read Pre-amp (Mag.Tape)	10 -50MV p-p -30KC	Balanced Class A 8V p-p Each side	EHB with high freq. roll off.
EHD					
EIA	50003101 50003201 50003301	Read Level detector (Mag.Tape)	8V Diff. Class A	1. Rect (-8V neg) 2. Enable (non-std)	Preproduction EIB
EIB	50009100 50009200 50009300	Read Level Detector (Mag. Tape)	8V Diff. Class A	1. Rect (-8V neg) 2. Enable (non-std)	Rectifier & level Detector for Mag.Tape
EIC	Design Hold	Read Level Detector (Mag.Tape)			

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
EID	50009102 50009202 50009302	Read Level Detector (Mag.Tape)	8V Diff. Class A	1. Rect (-8V neg) 2. Enable (non-std)	Lower Frequency EIB for 36-75 ips.
EIE	50009103 50009203 50009302	Read Level Detector (Mag.Tape)	8V Diff. Class A	1. Rect (-8V neg) 2. Enable (non-std)	EID with high freq. roll-off
EIF					
EJA	50003700 50003800 50003900	Read Level Detector (852 Disk Drive)	1) 3V p-p 1 mc Class A 2) Reference Voltage	1. Rect (-7V neg) 2. Enable (non-std)	Rectifier & level detector for disk storage drive Reference volts determines threshold
EKA	Not released	Dual Pre-amp (626 Experimental tape unit)	10-50MV p-p 120KC	Balanced Class A	2 circuits, 1 stage of gain
ELA	Not released	Pre-amp (626 experimental tape unit)	200-1000 MV p-p 120 KC	1. Balanced Class A 2. Level Enables (non-std)	Amp & level Detector for Phase modulation (pre-production)
EMA	50004600 50004700 50004800	Pre-amp (601 Mag Tape - Obsolete Analog interface)	10-25MV 15 KC	1. Gated, Balanced Class A 0.3V p-p 2. DC Deskew voltage	Single Stage gain plus Provision for remote control of read-write deskew. Obsolete
EMB	Not released				Similar to EMA with high freq. roll off. Obsolete
ENA	50009400 50009500 50009600	Photocell amp (350 PTR)	Photocell - Photocell +	OFF -1/4 V @ 10MA Compensated bias source	Photocell amp for feedhole 1 circuit Obsolete
ENB	50042500 50042600 50042400	Photocell amp (350 PTR)	Photocell - Photocell +	OFF -1/4 V @ 10MA Compensated bias source	Photocell amp #2 for feed-hole 1 circuit Obsolete

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
EOA	50015700 50015800 50015900	Class A amp & D-C Separator			Obsolete version EOB
EOB	Design Hold	Class A amp & D-C separator (601 Mag. Tape Analog interface)	15 KC 0.3V p-p	1. Balanced Class A 2. D-C voltage for read deskew	Separates 15 KC signals & DC Deskew voltage
EOC	Design Hold	ditto	ditto	ditto	EOB with high freq. roll off.
EPA	50016000 50016101 50016201	Potentiometer card (Mag.Tape)	Class A	Gain Controls	(7) 500 ohms potentiometers for use with EGA
EQA					
ERA	50016600 50016700 50016800	Solenoid Driver (601 Mag.Tape (power supply)	-1V -16V	-0.8V @ 2 1/4A -20V OFF	Pinch Roller Driver Requires 3 card slots
ESA	50016900 50017000 50017100	Delay control potentiometers 60X tapes	0-½V -16V	-2 to -10V Adjustable -13V OFF	7 potentiometers for delay group selection of voltage controlled delay (UGA, etc)
ETA	Not Released	Differential Amplifier	5MV 2MC	Balanced Class A	Adj gain preamp for phase modulation
ETB	Not Released	Differential Amplifier	1MV 2 MC	Balanced Class A	Like ETA except higher gain.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
EUA	50017200 50017600 50017700	Differential Amplifier (852 Disk Drive)	100 mv p-p 1 mc Analog	Balanced Class A	Amp. for magnetic head signals
EUB	Not Released	Differential Amplifier	100 mv p-p 2 mc Analog	Balanced Class A	Use EUC
EUC	50017502 50017602 50017702	Differential Amplifier (853 Disk Drive 807/8 Disk File)	100 mv p-p 1 mc Analog	Balanced Class A	Used with EWA/B Higher gain and lower output impedance than EUA
EVA	50017800 50017900 50018000	Gated, Strobed Receiver-Flip-Flop (807/8 Disk File)	1) Complementary rectangular waves 0.5V at 0V & Gate =0V & strobe = Logic"0" 2) Gate = -7V 3) Strobe = Logic "1"	1) Standard logic Flip-flop follows complementary inputs 2) Jammed to logic "0" 3) Flip-flop stays in last state	No AND diodes on output
EWA	50018100 50018200 50018300	Shaper (853 Disk Drive)	3V p-p 1 mc Analog	Differential 0.6V rectangular waveform referenced @ +8V.	Output changes state when input polarity reverses.
EWB	50018100 50018201 50018301	Peak Detector (807/8 Disk File)	3V p-p 1 mc analog	0.6V Square wave Referenced to +8V	Output changes state when input polarity reverses
EXP	46267000 No Assy No Schematic				Experimental Blank for Breadboard use
EYA	Design Hold				
EZA	50019000 50019100 50019200	AGC Attenuator (852 Disk Drive)	1) 100 mv p-p 1 mc Analog 2) Attenuation Control Signal (+1V to -1V)	Output is input attenuated up to 20 db	Used with FYA Requires +12V on pin 15 - 12V on pin 13

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
FAA	Not Released				Obsolete. Use FAB circuit
FAB	50034601 50034701 50034801	Shaper Flip-Flop (807/8 Disk File)			Logic Outputs have no AND diodes. Used with EWB
FBA	Not to be released	Voltage Limiter for Servo Valve Amp Input (807/8 Disk File)	Analog Signal with 0-1 ma drive capability	Same analog signal limited at +6.8V and -6.8V	1 Circuit
FCA	50035200 50035300 50035400	Outer Track Select & Summing Network (807/8 Disk File)	3 of 4 inputs at 0V, other input +8, 0, or -8V	0 to 1.1 ma dependent on input combination	Resistor Network for summing current into an operational amp.
FCB	50035200 50035301 50035401	Inner Track Select & summing network (807/8 Disk File)	2 of 3 Inputs @ 0v, 3rd input at +8V or -8V 4th input +8V,0,or-8V	0 to 0.6 ma dependent on Input combination	Resistor Network for summing current into an operational amp
FDA	50035500 50035600 50035700	10 KC Oscillator	None	7V P-P @ 10 KC Regulated	Minimum load resistance =2K

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
FGA	50036400 50036500 50036600	Clamp & Summing + 0.020 inch (807/8 Disk file)	Input pin 1, 2 Logic "0", "1" Logic "1", "0" Logic "0", "0"	-1/8 ma +1/8 ma -1/0 ma	Requires +8V & -8VDC Reference on pins 3 & 9. Both polorities of output current separately adjustable. Used to sum into op. amp.
FHA	50036700 50036800 50036900	Valve Amplifier (807/8 Disk File)	Analog voltage of ± 6.8V max. @ ±1 MA max. & Feedback term	Class AB current regulated at about 5 MA	Output used with FMA to drive 30 MA into inductive load.
FIA	50037000 50037100 50037200	10 KC Power Amplifier (807/8 Disk File)	7V P-P from FDA Card & Feedback term	Class AB current regulated at about 5 MA	Output used with FMA to drive 150Ω resistive load to 30V P-P.
FJA	50037300 50037400 50037500	Servo Cycling Generator	Pin 1 - 0V Pin 1 - Open	+10V @ 2.35 K String of pulses 50-100 us wide switched to around @3 MA spaced 100 ms apart.	Used to toggle OLA circuit. Jumper option to space pulses 600 ms apart.
FKA	50037600 50037700 50037800	Demodulator (808/8 Disk File)	Two separate amplitude modulated 10KC signals	D-C difference of demodulated input max output ±1.4 ma.	Output used in summing network at input of op. amp.
FLA	50037900 50038000 50038100	Bridge Rectifier (807/8 Disk File)	10V RMS @ 10 KC	+8V Nom @ 5K -8V Nom @5K (Proportional to Input)	FMA provides suitable input, Output includes compensating diodes for negative feedback loop of op. amp.
'LB	50037900 50038001 50038101	Bridge Rectifier (807/8 Disk File)	10V RMS 10 KC	+8V (No load) -8V (No load) (Proportional to Input)	FMA provides suitable input

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
FMA	50038200 50038300 50038400	Power Amp. Output Stage (807/8 Disk File)	Class AB	Class AB - between +15 and -15VDC 150 Min. Resistive Load 30 MA peak into inductive load.	Current gain only Input matches output of FHA or FIA circuit.
FNA	50038500 50038600 50038700	Retract Inverter & Current Source (807/8 Disk File)	OV, GND Open, -3V	-20V @ 43K, pin 6 Logic "1", pin 12 OV @ 33K, pin 6 Logic "0" pin 12.	Pin 6 intended to drive current summing network for operational amp.
FOA	50038800 50038900 50039000	Feedback Function Generator (807/8 Disk File)	Position Op. Amp (+10V to -10 VDC) & + VDC Floating Power Supply.	Non-linear current feedback	Special network for FSA circuits Floating power supply on input satisfied by ALA.
FOB	50038800 50038901 50039001	Feedback Function Generator (807/8 Disk File)	Position Op. Amp (+10V to -10 VDC) & -VDC Floating Power Supply	Non-linear current feedback	Special Network for FSA circuit. Floating power. Supply on input satisfied by ALA
FPA	50039100 50039200 50039300	Reference Amplifier (807/8 Disk File)	+9.1V Ref or -9.1V Ref.	-8V @ 0-10 MA or +8V @ 0-10 MA	Input reference available from ALA circuit. Output polarity selected by input connections.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
FRA	50039700 50039800 50039900	Velocity, Acceleration Summing Networks (807/8 Disk File)	1. Velocity sensors 2. Velocity Op. Amp. 3. Acceleration Op. Amp.	Summation of Input 1 & 2. Summation of input #2 after differentiation and Input #3.	Special Network for FSA circuit
FSA	50040000 50040100 50040200	Operational Amp. & Booster Amp. (807/8 Disk File)	Low-level signals (Summation of Input & Feedback Signals)	High gain Class AB reproduction of input over +10V to -10V range into 150 Ω min load.	One side of differential input may be grounded for single-ended signals.
FTA	50040300 50040400 50040500	Velocity Summing Networks (807/8 Disk File)	1. Velocity Signal 2. Velocity Op. Amp.	Summation of Input 1 & 2	Special Network for FSA circuit with 2:1 range of gain adjustment.
FUA	50040600 50040700 50040800	Position, Velocity Acceleration Summing Networks (807/8 Disk File)	1. Velocity signal 2. Acceleration signal 3. Summing Op. Amp 4. Short Stroke Op.Amp 5. On point Op. Amp.	Summations of Inputs as follows: a. Inputs 1,2,3,4 b. Input 4 c. Input 4,8,5	Special Network for FSA circuit with gain adjustment on Input 2
FVA	50040900 50041000 50041100	Position & Acceleration Network (807/8 Disk File)	1. Long Stroke Displacement. 2. Long Stroke Displacement Op. Amp. 3. Acceleration 4. Function Gen Op. Amp. 5. Sum of 2 & 3	Summation of inputs: a. Inputs 2,3 & 4 b. Inputs 2 & 3 c. Inputs 2 & 4 d. Inputs 2,3,4	Special network for FSA circuit. Gain adjustment on inputs 3 & 4
FWA	50041200 50041300 50041400	Temperature Servo. Amp. (807/8 Disk File)	Thermistor 1.5K @ 92°F.	Half wave 60 cycle sine wave current 150 ma peak. Open circuit voltage of 40V peak supplied by motor shading coils.	Output connects to shading coils on shaded pole motor. Class "B" operation of output Transistors causes CW or CCW variable speed operation.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comment
FXA	50041500 50041600 50041700	Gated Read Amplifier (807/8 Disk File)	1) 5 mv p-p 1 mc Analog 2) +8V gate	Analog	Can be gated on and off with electronic gate signal, or jumpered on.
FYA	50041800 50041900 50042000	AGC Rectifier (852 Disk Drive)	1) Rectified Analog (-7V) 2) AGC Disable - Std Logic	Attenuation Control Signal (+1V to -1V)	Used with EZA
FZA	50042100 50042200 50042300	Gated Line Driver (853 Disk Drive)	Complementary 0.6V Rectangular waves @ +8V & Gate = Logic "1" Gate = Logic "0"	+2V, 200 ns pulse for each change of rectangular wave input OFF - 0V	120 Ω output terminating resistor. Input 1) matches EWA.

Type	Card Blanks Comp. Schematic	Applications	Input	Output	Comments
GAA	50050500 50050600 50050700	Isolated Diode Cards (852/3 Disk Drive 807/8 Disk File)	Cath. of Diodes	Anode of Diodes +20V Via 17.6V Zener	4 isolated 0.3A Silicon Diodes on pins 1-8. Zener output on pin 11 matches input to AYA, BAA, or BAB.
GBA	50050800 50050900 50051000	Clutch Pre-Driver (350 Paper Tape Reader)	-6.0V 0V	Pin 7 = OFF, -7V Pin 5 =-V@125 MA Pin 7 =-0.5V@125MA Pin 5 = OFF, -7V	Pin 10 & 12 biased to switch external output drivers when pin 5 & 7 are each returned to -25V via 200Ω. Similar to 76A
GCA	50051100 50051200 50051300	500 Cycle Twin "T" Notch Network (807/8 Disk File)	0 to ±10 VAC max. (servo acceleration signal)	No load output voltage equals input except near null	3 db down at 450 & 550 cps. 40 db down @ 500 cps when used with Op. Amp.
GCB	5005100 50051201 50051301	Variable Freq. Twin "T" Notch Network (807/8 Disk File)	0 to ± 10 VAC max. (Servo acceleration signal)	No load output voltage equals input except near null	40 db down point adjustable from 350-800 cps, 3 db points about 100 cps apart when used with op. amp.

Card Blanks
Comp. Layout

Type	Schematic	Application	Input	Output	Comments
HAA	48303600 48303700 48303800	Resistor Term (915 Page Reader)	Res. Term.	Res. Term.	680Ω to gnd. Pin 1,2 1K to gnd. Pin 3 2.2K to gnd. Pin 4,5 3.3K to gnd. Pin 6-8 Network Pin 10-11 4.7K to +20V Pin 12 Drawings at Rabinow

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
IAA	46245300 46241600 46244500	Relay Puller (Mag.Tape)	Logic "0" Logic "1"	-36V OFF - 0.6 V @ .6A	Slow Speed Driver for -3 to -36V terminated loads
IAB	50009700 50009800 50009900	Relay Puller (Mag.Tape)	Logic "0" Logic "1"	-36V OFF - 0.6V @ .5A	Derated IAA Use IAA in new designs
IBA	46245200 46241400 46244200	Power EF(+20V) (Mag.Tape)	Logic "0" Logic "1"	- 0.6V @ 0.6A +14V OFF	Special capstan Driver for +14V or less terminated loads
ICA	41060300 41060400 41060500	Driver Double Inv. (180 D C)	Logic "0" Logic "1"	0.6V @ 0.4A -60V OFF	Stepper Motor Driver 2 circuits Not currently in production.
IDA	46500000 46500100 46500200	D/A Converter (Display)	Std.Logic	Analog	Pre-Production only
IEA	46500300 46500400 46500500	D/A Converter (Display)	Std. Logic	Analog	Pre-Production only
IFA	46500600 46500700 46500800	D/A Converter (Display)	Std.Logic	Analog	Pre-Production only
IGA	46500900 46501000 46501100	Character Size (Display)	Std.Logic	Analog	Pre-Production only
IHA	46501200 46501300 46501400	Character Size (Display)	Std.Logic	Analog	Pre-Production only
IIA	46281400 46281500 46281600	Head Driver (Mag.Tape)	Logic "0" Logic "1"	-20V OFF -1V @ 160 MA	Similar to 55 card

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
IJA	50001600 50001700 50001800	Power Flip-Flop (Mag.Tape)	Logic "0" Logic "1" Logic "0" Logic "1"	Logic "0" Logic "1" -20V OFF -0.6V at 160MA	1 circuit 2 "OR" inputs Input/output pertains to 1 side - set or clear.
IKA	50001900 50002000 50002100	Output amp. (OEM Mag Tape for WU/RCA)	Logic "0" Logic "1"	+13V at 70MA -3V at 15MA	2 circuits for coax line (Matches OKA Receiver)
ILA	50002200 50002300 50002400	Voice Coil Driver (Mag.Tape)	Logic "0" Logic "1"	+0.6V at 1¼A +14V OFF	2 circuits for terminations to +14V or less
IMA	Design Hold	Quadruple Driver			
INA	50005200 50005300 50005400	Line Driver (OEM Mag. Tape for West. Elect.)	Logic "0" Logic "1"	-6V at 30 MA -0.6V at 25 MA	3 circuits Coax Line Driver (Matches OIA)
IOA	Design Hold	Head Selection (mass Memory)	Logic "0" Logic "1"	OFF +0.4V at .1A or +.6V at 1.5A*	Obsolete, Use IOB
IOB	50019301 50019401 50019501	Head Selection (807/8 Disk File 852, 853 Disk Drive)	Logic "0" Logic "1"	OFF +0.4V at 0.2A +0.6V at 1.5A*	2 circuits, Only 1 circuit should be on at a time. For terminations to +40V or less *Requires external 180Ω to +20V
IOC	50019301 50019402 50019501	Head Selection (852/3 Disk Drive) (807/8 Disk File)	Logic "0" Logic "1"	OFF +0.4V @ 0.2A +0.6V @ 1.5A* +0.5V @ 0.5A**	IOB with less leakage current. *Requires ext. 180Ω to +20V **Requires ext 550Ω to +20V

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
IPA	50019600 50019700 50019800	Line Driver (Mag.Tape Exerciser for Mitsubishi)	Logic "0" Logic "1"	0V OFF -1.8V at 30MA	3 circuits (Matches OPA) 120 OHM termination jumper option.
IQA	50019900 50020000 50020100	Line Driver (OEM Mag.Tape for Mitsubishi)	Logic "0" Logic "1"	+E OFF -1.5V to + E at 8MA	3 circuits, Matches OQA Output is 8MA constant current to external termination.
IQB	Design Hold				
IRA					
ISA	Not Released	Line Driver (601 Daisy Chain)	Logic "0" Logic "1"	0V OFF +2.0V at 34MA or +3.0V at 30MA	3 circuits Matches OSA, OSB 120 ohm termination jumper option.
ISC	50020502 50020602 50020702	Line Driver (601 Daisy Chain)	Logic "0" Logic "1"	0V OFF +2.0V at 34MA or +3.0V at 30MA	Improved ISA, Matches OSA, OSB 120 ohm termination jumper option.
ISD					

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
ITA	50020800 50020900 50021000	Pulse Delay & Line Driver (601 Daisy Chain)	Logic "1" pulse	+2.0V at 34MA Pulse delayed	Pins 1-8 same function as UGA Pins 10-12 same as ISA, ISC Matches OSA, OSB. Obsolete. Use ITB in new designs.
ITB	50020801 50020901 50021001	Pulse Delay & Line Driver (601 Daisy Chain)	Logic "1" pulse	+2.0V at 34 MA Pulse delayed	Obsolete. Use ITD
ITC	50020800 50020902 50021002	Pulse Delay & Line Driver (601 Daisy Chain)	Logic "1" pulse	+2.0V @ 34 MA Pulse delayed	Supersedes ITA with improved temp characteristics. Use ITD in new designs.
ITD	50020803 50020903 50021003	Pulse Delay & Line Driver (601 Daisy Chain)	Logic "1" pulse	+2.0V @ 34MA Pulse Delayed	Improved production yield over ITA & ITC. Improved temp. char. over ITA & ITB
IUA					
IVA	50021400 50021500 50021600	Gated Oscillator (852 Disk Drive)	Logic "0" & Logic "1"	Logic "0" pulse at 699.5 KC ±0.1% rate	First transition from "1" to "0" occurs within 150 nsec after input goes to ground.
IWA	Design Underway	Controlled Rise Time amp. & FF (Pluto tapes)	Logic "0" Logic "1" Logic "0" Logic "1"	Logic "0" Logic "1" 0V OFF +3V at 20 ms	1 circuit 2 "or" inputs. Input/Output pertains to 1 side set or clear. Designed for +15V but may use +20V.
IYA	50022300 50022400 50022500	Line Driver (OEM Beckman)	Logic "0" Logic "1"	-12V -½V	3 Circuits, Matches OYA
IZA					

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
JAA JAB JAC	Not to be Released	Speed Detector			JAA, JAB & JAC are being replaced by JAD, JAE & JAF respectively.
JAD	50042702 50042803 50042903	Speed Detector (807/808 Disk File)	80 us Logic "1" Pulses Rep rate 16.7 cps Rep rate 16.7 cps	 -20V OFF -0.6V @ 0.3A	Rep rate of switching point fixed by selected components in manufacture.
JAE	50042702 50042804 50042903	Speed Detector (852 Disk Drive)	50 us Logic "1" Pulses Rep rate 400 cps Rep rate 400 cps	 -20 V OFF -0.5V @ 0.3A	Similar to JAD except for higher rep. rate
JAF	50042702 50042805 50042903	Speed Detector (853 Disk Drive)	.50 us Logic "1" Pulses Rep rate 633 Rep rate 633	 -20V OFF -0.6V @ .3A	Similar to JAD & JAE except for higher rep. rate.
JBA	50043000 50043100 50043200	Positive voltage ref. switch (807/808 Disk File)	+8V Ref Logic "0" Logic "1"	 +0.015V@ 1.1 ma +8.0V @ 1.1 ma	2 Circuits The +8V Ref Input required on pins 5 & 11 matches output of FPA circuit Output matches FCA & FCB circuits
JCA	50043300 50043400 50043500	Negative voltage ref. switch (807/808 Disk File)	+8V ref Logic "0" Logic "1"	 -0.015V @ 1.1 ma -8.0V @ 1.1 ma	2 Circuits. The -8V Ref input required on pins 5 & 11 matches output of FPA circuit. Output matches FCA & FCB circuits.
JDA	50043600 50043700 50043800	Long Stroke - Short Stroke Switch (807/808 Disk File)	Logic "0" & "1" Three inputs	Bidirectional switch to 0V when $V_3+V_2\ \overline{V}_1$ equation satisfied Otherwise output off	Subscripts in equation refer to input pins: Output in off condition should be limited to $\pm$ 10V.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
JEA	Not to be Released				Obsolete, Use JEB
JEB	50043901 50044001 50044101	Tuned Amplifier (807/8 Disk File)	1) Logic 2) Two Complementary Inputs with excursion of 6V	800 KC sine wave, 10 V	

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
OAA	46264200 46264300 46264100	Photocell amp (Mag.Tape)	Solar Cell lighted + Solar Cell dark -	Logic "1" Logic "0"	2 circuits
OAB					
OBA	Obsolete	Peak detector (Mag.Tape)	+ Peak No Peak	Logic "1" Logic "0"	Obsolete Peak Detector Use OGC
OCA	41059700 41059800 41059900	Photocell Pre-amp (180 DC)	Photocell + Photocell -	-3V OFF -½V @ 10MA	2 circuits
ODA	46278800 46278900 46279000	Read Peak Detector (Mag.Tape)	+ Peak No Peak	Logic "1" pulse Logic "0"	40 KC Peak Detector Obsolete after retrofit completed. Use OGC in new design.
OEA	Design Hold	One Second Delay (Card Reader)			
OFA	50002500 50002600 50002700	Input "M" Card (Mag.Tape NCR)	-8V -1V	Logic "0" Logic "1"	3 circuits, external termination to - Matches AEB
OGA	50001300 50001400 50001500	Read Peak Detector (Mag.Tape)	+ Peak Pin 1 - Peak Pin 5 No Peak	Logic "1" pulse Logic "1" pulse Logic "0"	Preproduction OGB Obsolete & not released.
OGB	50008800 50008900 50009000	Read Peak Detector (Mag.Tape)	+ Peak Pin 1 - Peak Pin 5 No Peak	Logic "1" pulse Logic "1" pulse Logic "0"	Peak Detector & Shaper Optional jumpers for lower freq. Use OGC below
OGC	50008801 50008901 50009000	Read Peak Detector (Mag.Tape)	+ Peak Pin 1 - Peak Pin 5 No Peak	Logic "1" pulse Logic "1" pulse Logic "0"	Improved version of OGB
OGD	50008802 50008902 50009002	Read Peak Detector (852 Disk Drive)	+ Peak Pin 1 - peak Pin 5 No peak	Logic "1" pulse Logic "1" pulse Logic "0"	Pulse width 700 ± 100 ns

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
OHA	50006400 50006500 50006600	Peak Detector (OCR and Mag Tape Phase Mod)	No Peak or no enable - Peak Pin 1 or + Peak, Pin 3 + Peak Pin 1 or - Peak, Pin 3	Logic "0" Logic "1" pulse Pin 9, 10 Logic "1" pulse Pin 11, 12	Positive & Negative Peak detector for 120 KC Class A signals
OIA	50006700 50006800 50006900	Line Receiver (OEM Mag.Tape For West. Elect.)	-6V -½V	Logic "0" Logic "1"	Matches INA 3 circuits
OJB	50022901 50023001 50023101	Long term delay (general purpose)	Open -16V 0V	Logic "0" delayed Logic "1"	Delay derived from fixed components. Jumper options from 2 ms to 50 sec.
OKA	50023200 50023300 50023400	Input Amplifier (OEM Mag.Tape for WU/RCA)	-0V +9V	Logic "0" Logic "1"	3 circuits Matches IKA
OLA	50023500 50023600 50023700	Fly back verify Flip-Flop (Printers)	Set = "1" Toggle = -Pulse Clear = "0"	Logic "0" Changes State Logic "1"	1 circuit Operates from ADC or ADE suppression circuit
OMA	50023800 50023900 50024000	High Fanout "M" Card (Printer Echo check)	-16V 0V	Logic "0" Logic "1"	3 circuits Matches "L" Cards Output for setting OLA card
ONA	50024100 50024200 50024300	Photocell Amp (852,853 Disk Drive)	Photodiode lighted+ Photodiode dark -	Logic "0" & "1" Logic "1" & "0"	2 circuits. Each has complementary outputs
OOA	50024400 50024500 50024600	Gated Line Receiver (853 Disk Drive)	Toggle= +2V pulse referenced to 0V & Gate = Logic "0" Gate = Logic "1"	Standard logic Flip-Flop toggles on each 200 ns pulse Jammed to logic "0"	Input pulse from line has 0 to +2V excursion from ISC circuit No "AND" diodes at output
OPA	50024700 50024800 50024900	Line Receiver (OEM Mag.Tape, for Mitsubishi)	0V to +1.5V -1.8V to -3.5V	Logic "0" Logic "1"	3 circuits Matches IPA & AQA

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
OQA	50025000 50025100 50025200	Line Receiver (OEM Mag.Tape for Mitsubishi)	+1V -1V	Logic "0" Logic "1"	3 circuits IBM "N" level Superseded by OPA
ORA	50025300 50025400 50025500	Read Out Comparator (Rabinow OCR)	Analog DC Probe Storage Clear	Store - Peak Logic "0" if Max Logic "1"	Many ORA cards probed simultaneously to determine best Max.
OSA	50025600 50025700 50025800	Line Receiver (601 Daisy Chain)	0V +2.0V	Logic "0" Logic "1"	3 circuits Matches IS.., series ITA & ASA
OSB	50025600 50025701 50025801	Line Receiver (Optical reading Machine)	0V +2.0V	Logic "0" Logic "1"	OSA with 120 ohms input termination
OTA	50025900 50026000 50026100	Level Switch (807/808 Disk File)	D-C Analog from +10V to -10V	Logic "1" when |Input| $\leq$ Threshold Logic "0" when |Input| $>$ Threshold	Threshold adjustable from $\pm$ 50 mv to $\pm$ 400 mv
OUA	50026200 50026300 50026400	Schmitt Trigger (807/808 Disk File)	E in $>$ +3.5V E in $<$ +2.5V	Logic "0" Logic "1"	2 Circuits per card
OVA	50026500 50026600 50026700	Gated Pulse Shaper (853 Disk Drive)	Complementary 0.6V Rectangular waves @+8V & Gate=Logic"1" Gate = Logic "0"	200 ns logic "1" Pulse when rectangular wave polarity reverses Logic "0"	
OWA	Design Under way				
OYA	50027400 50027500 50027600	Line Receiver (OEM Beckman)	-12V -1V	Logic "0" Logic "1"	3 Circuits, Matches IYA

Type	Card Blanks Comp. Layout Schematic	Application	Input	Output	Comments
TAA	48303200 48303300 48303400	Dual Photodiode Amplifier (915 Page Reader)	Photodiode - Photodiode +	Off, -20V -3/4V @ 5 MA	2 Circuits, Bias separately adjustable for each circuit Drawings at Rabinow

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
UAA	46245500 46241800 46244300	Adjustable Delay (Mag. Tape)	Logic "0" Logic "1"	Logic "0" delayed Logic "1"	2-5000 Micro sec delay on "0" Obsolete Use UAB for future design
UAB	50007300 50007400 50007500	Adjustable Delay (Mag. Tape)	Same as UAA		Supersedes UAA with 0-25 μs temp. stabilized delay
UBA	41060000 41060100 41060200	Dual Inverter (180 DC)	Logic "0" Logic "1"	Logic "1" Logic "0"	Similar to Control Corp. 24 Obsolete. Use 24B for future design.
UCB	50000100 50000200 50000300	Multivibrator Delay (Mag. Tape)	Logic "0" Logic "1" leading edge	Std. Logic Logic "1" pulse after delay	1.9 - 4.5 Micro sec delay Do not use in future design
UDA	46501500 46501600 46501700	Display	Std. Logic	Std. Logic8	Inverter Pre-Production only
UEA	50028000 50028100 50028200	699.527 Oscillator Calib. (852 Disk Drive)	Logic "0" Logic "1" (from IVA card)	1)-Std. logic pulses @699.5KC 2)-Beat frequency of1) with Input	Requires 2 card spaces Oscillator crystal controlled
UFA	50028300 50028400 50028500	Voltage Control Assy (Mag. Tape)	Logic "0" Logic "1"	Logic "0" & "1" delayed Logic "1" & "0"	1.2-4.2 μs delay on "0" input. Longer delays with jumpers & external capacitor. Obsolete Retrofitted by UFB.
UFB	50028301 50028401 50028500	Voltage Control delay (Mag. Tape)	Logic "0" Logic "1"	Logic "0" & "1" delayed Logic "1" & "0"	Supersedes UFA Longer delays with jumpers & external capacitor
UGA	50028600 50028700 50028800	Voltage Controlled Pulse Delay (Mag. Tape)	Logic "1" pulse	Logic "1" pulse delayed	1/4 μs input pulse delayed 1 1/4 - 5 us. Optional longer delay with jumpers & external capacitors.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
UHA	50028900 50029000 50029100	Adjustable Short Term Delay (807/808 Disk File)	Logic "1" Pulse	Logic "1" Pulse Adjustable from 0.1 to 1.2μs independent of Logic "1" input pulse width.	Requires 400 ns logic "0" input for full recycle at min delay, 100 ns at max delay. Delay initiated by negative going excursion.
UIA	50029200 50029300 50029400	Pulse Shaper (807,808 Disk File)	Logic "0" Logic "1"	Logic "0" pulse Logic "1"	Output "0" pulse of 75ns when input goes positive. with pin 6,7 jumpered. (180 ns with pin 6,8 jumpered).
UJA	Not to be released				
UJB	50029501 50029601 50029701	Adjustable Long Term Delay (General Purpose)	Logic "0" Logic "1"	Logic "0" & "1" delayed Logic "1" & "0"	Delays on "0" input. Complementary outputs. Delays from 300 μs to 100 sec by jumper options. Range of adjustment = 10:1
UKA	50029800 50029900 50030000	Gated Toggle Flip-Flop (853 Disk Drive)	Toggle = Logic Pulse & Gate = Logic "0" Gate=Logic "1"	Standard Logic, Flip-Flop Toggles on each 200 ns pulse Jammed to Logic "0"	Outputs do not include "AND" diodes.

Type	Card Blank Comp. Layout Schematic	Application	Input	Output	Comments
XKA	46245400 46241700 46244400	Counter Differentiator (Mag.Tape)	Logic "0" Logic "1"	Logic "1" pulse Logic "0"	Output pulse when input goes positive 2 circuits
XKB	50008200 50008300 50008400	Inv. and Diff. (General)	Logic "0" Logic "1"	Logic "1" pulse Logic "0"	Faster than XKA Obsolete Use XKC 2 circuits
XKC	50008201 50008301 50008401	Inv. and Diff. (General)	Logic "0" Logic "1"	Logic "1" pulse Logic "0"	Output "1" pulse for 0.4 microsecond 2 circuits

COMMENT SHEET

MANUAL TITLE CDC Printed Circuit Manual Volume 3

PUBLICATION NO. 60042900 REVISION W

FROM: NAME:

BUSINESS ADDRESS:

CUT ALONG LINE

AA3419 REV. 7/75 PRINTED IN U.S.A

NO POSTAGE STAMP NECESSARY IF MAILED IN U. S. A.

FOLD ON DOTTED LINES AND STAPLE

STAPLE

STAPLE

FOLD

FOLD

FIRST CLASS
PERMIT NO. 8241

MINNEAPOLIS, MINN.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN U.S.A.

POSTAGE WILL BE PAID BY

CONTROL DATA CORPORATION
Publications and Graphics Division
ARH219
4201 North Lexington Avenue
Saint Paul, Minnesota 55112

CUT ALONG LINE

FOLD

FOLD