*Printed Circuit Manual*

VOLUME 2

CONTROL DATA

CORPORATION

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

## REVISION RECORD

| REVISION | DESCRIPTION |
|---|---|
| A | Corrections. |
| B | 1604 Inverter Ground Rules and Hammer Storage Card 91 pages added. |
| C | Long Line Driver and Receiver Cards CA98 and HA26 pages added. |
| D | Corrections to card type C64 and C65. |
| E | Add index tabs, chapter headings, new Table of Contents addition to Appendix, type "E" and 1604 cards; and Delay Card P13A. |
| F | Replace the following pages 3-HA18-1 and 2; 4-C62 and C-61-5 and 6; Appendix pages 5 through 10. Add pages 4-60, 60A, 62 and 67-1 through 3; 4-79A-1, 5-97-1 and 2, 5-E10-1. Replace page 4-E12-1. |
| G | 6600 information and circuit module schematics added as volume 3. |
| H | Volume 1, addition of revised record of revisions volume 2, addition of record of revisions. Replace the following revised pages; chapter 4 contents page, 4-C62 and C61-1, 4-C62 and C61-2, 4-C62 and C61-3, 4-C62 and C61-5, 4-C62 and C61-6, 4-C62 and C61-7, 4-P14A and P16A-3, 5-C94-3. |
| J | Volume 1, page 2-3600 inv-3 revised. Volume 2, chapter 5, second page of contents revised, removes pages 5-PED-1 through 5-PED-22. Chapter 6 added and Appendix 1, pages 16, 17, and 18 removed and new pages added. |
| K | Publication Change Order 11170. Record of Revisions for volumes 1 and 2 revised. Removed pages 15 through 31 of volume 2, Appendix 1 and replaced with revised pages. |
| L (10-5-65) | Change Orders 10344 and 10708. Pages v, vi, vii, viii of volume 1 revised. Chapter 4 contents page, 4-HA19-3, 4-HA37 and HA43-10, 4-P14C and P16A-1, 4-P14C and P16-2, 4-P14C and P16-A-3, chapter 5 contents pages, 5-C84-1, 5-C84-2, 5-C84-3 (new pages), 3, 4, 7, and 8 (appendix) revised. Pages 5-C60-1, 5-C60-2, 5-C60-3, 5-C97-1, 5-C97-2, and 5-C97-3 added. Pages 5-HA27 and 5-HA28-1 and 5-HA27 and 5-HA28-2 revised. |
| M (12-13-65) | Change Order 12131. Appendix 1; pages 16 through 31 revised and pages 32 through 47 added. |
| N (5-13-66) | Publication Change Order 12940. New peripheral equipment cards added to chapter 6; ADH, ITA/ITB/ITC, ITD, TYA, OJB, OYA, and UJB. Revised text for page; 6-OHA-1. Revised schematic for page 6-IAA, IAB-2. Appendix 1 revised. This revision obsoletes all editions of pin assignments- 1604 and 3600. Printed circuit cards, publication number 60106200, which is now included in this revision. |
| P (5-13-66) | Publication Change Order 13632. Pages 6-ISC-1 of chapter 6 is revised. The following new cards are added to chapter 6; ALA, AMF, AMG, AMH, AMI, ANB, ANC, AND, AUA, EUA, EUC, EVB, FCA, FCB, FDA, FGA, FHA, FIA, FJA, FKA, FLA, FLB, FMA, FNA, FPA, FRA, FSA, FTA, FUA, FVA, FWA, FYA, JBA, JCA, JDA, and OTA. |
| R (2-13-67) | Publications Change Order 15800. The following new cards added to chapter 6; AIB, AKA, AOA, ATA, ATB, AVA, AYA, BAA, BAB, BBA, BCA, EEG, EEH, EWA, EWB, EZA, FAB, FOA, FOB, |

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**REVISION LETTERS I, O, Q AND X ARE NOT USED**

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or use Comment Sheet in the back of this manual.



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# REVISION RECORD (CONT'D)

| REVISION | DESCRIPTION |
|---|---|
| R | FRB, FEC, FRD, FSB, FUB, FWB, FXB, GAA, GBA, GCA, GCB, GCC, GCD, IOB, IOC, IOD, |
| (Cont'd) | JEB, JEC, ONA, OUA, OVA, UEA, UHB, UIA, UJC, UKA, and UKB. |
| S | Publications Change Order 16541. The following new cards are added; AHC, AMJ, AMK, AMI, AVB, |
| (6-23-67) | AVC, AVD, AYB, BCB, BDA, BFA, BGA, BHA, BHB, BIA, BJA, EEK, EEL, EEM, EEO, EUD, |
| | EWC, FCC, FCD, FCE, FGB, FGC, FOC, FOD, FOE, FOF, FOG, FOH, FVB, FXC, GAB, GAC, |
| | GDA, GEA, GFA, GFB, GFC, GGA, HAA, IOE, IOF, ISH, JAD, JAE, JAF, JAG, OSC, OVB, TAA, |
| | ULA. |
| T | Engineering Change Order 20995, publications change only. The following new cards are added; |
| (11-22-68) | Card type 144, CC10, ADG, AMM, AMN, AMO, AMP, AMQ, AUB, AUC, AZA, BEA/B, BMA, |
| | BOA, BRA, BTA, BUA, EJA, FMB, FYB, GHA, GIA, GIB, GOA, GSB, HAB, IOG, IVA, IVB, IVC, |
| | JAH, JAI, JED, JEE, JFA, JHB, JJA, JLA, JOA, JPA, OGD, OWB, PJA, PJB, UPA, URA, USA. |
| | The documentation for the following cards is affected by either revisions or page number changes; |
| | Card type 54, 74; HA18; C07C; HA20; HA27; HA28; HA35; AMF through AML; AUA, AVA, through |
| | AVD; FCA through FCE; FGA through FGC; FMA; FOA through FOH; FXB, FXC, FYA, HAA, IOB |
| | through IOF; JAD through JAG; UAA, UAB, UHB, ULA, pages 5, 20, and 21 under appendix 1. |
| | The following miscellaneous changes are being made: expansion from two to three volumes, re- |
| | labeling of chapter 6 tabs, and appendix 1 tab repositioned. |
| U | Engineering Change Order 28728, publications change only. Incorporates publications change |
| (8-9-71) | from the following ECO's: 24045A, 23441, 20211, 21766, and FCO PR1168. The following pages |
| | are revised: 3-HA14-3, V5-E08-2, 5-97-1, 5-97-2, 5-HA20-1, appendix 1 page 15. |
| V | Engineering Change Order 36403, publications change only. No effect on this publication. |
| (6-10-75) | |
| W | Manual revised; includes Engineering Change Order 37817, publications change only. Page |
| (2-23-77) | 3-HA14-3 is revised. |
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# CHAPTER 6. PERIPHERAL EQUIPMENT CARDS*

(Types A-- Thru G--)

| | |
|---|---|
| Relay Puller | ABA |
| Photo-Diode Bias and Preamplifier | ACA |
| Hammer Driver | ADA, ADB |
| Hammer Driver | ADC, ADD, ADE |
| Hammer Driver | ADG |
| Clutch-Brake Driver | ADH |
| Output Driver | AEB |
| Multiple Time Delay | AFA, AFB |
| Enable Amplifier | AGA |
| Flip-Flop Driver | AHA, AHC |
| Shift Driver | AIA, AIB |
| Photocell Amplifier | AKA |
| Power Supply | ALA |
| Write/Erase Driver | AMF, AMG, AMH, AMI, AMJ, AMK, AML, AMM, AMN, AMO, AMQ |
| Head Select and Write Error Checker | ANB, ANC, AND |
| Exclusive OR Circuit | AOA |
| Gated Amplifier | ATA, ATB |
| Power Supply Regulator | AUA, AUC |
| Power and Clamp Voltage Supply | AUB |
| Write Resistor Diode | AVA, AVB, AVC, AVD |
| Voltage Checker | AYA, AYB |
| Write Resistor | AZA |
| Voltage Checker | BAA, BAB, BBA, BCA, BCB |
| Head Switch | BDA |
| Line Terminators | BEA, BEB |
| L Type Data Receiver | BFA |
| L Type Data Transmitter | BGA |
| Q Type Control Receiver | BHA, BHB |
| Q Type Control Transmitter | BIA |
| Supply Sensor and Current Sink | BJA |
| Write Driver | BMA |

*Refer to Volume 3 for Card Types H-- thru Z--.

| | |
|---|---|
| Voltage Checker | BOA |
| Erase Driver | BRA |
| Current Controlled Lamp Driver | BTA, BUA |
| Read Level Detector | EDA |
| Resistor Termination | EEA |
| Capacitor Termination | EEB |
| Capacitor Termination | EEC |
| Resistor Termination | EED |
| Capacitor Termination | EEE |
| Resistor Termination | EEF |
| Resistor Termination | EEG |
| Resistor Termination | EEH |
| Resistor Termination | EEK |
| Capacitor Termination | EEL |
| Resistor Termination | EEM |
| Capacitor Termination | EEO |
| Clock Amplifier | EFA |
| Read Level Detector | EGA |
| Read Preamplifier | EHA, EHB, EHC |
| Read Level Detector | EIA, EIB, EID, EIE |
| Rectifier and Threshold Detector | EJA |
| Potentiometer | EPA |
| Solenoid Driver | ERA |
| Delay Control Potentiometers | ESA |
| Differential Amplifier | EUA, EUC, EUD |
| Receiver Flip-Flop | EVB |
| Zero-Crossing Detector | EWA, EWC |
| Peak Detector | EWB |
| AGC Attenuator | EZA |
| Shaper Flip-Flop | FAB |
| Inner and Outer Track Select and Summing Networks | FCA, FCB, FCC, FCD, FCE |

| | |
|---|---|
| Oscillator | FDA |
| Clamp and Summing | FGA, FGB, FGC |
| Valve Amplifier | FHA |
| Power Amplifier | FIA |
| Servo Cycling Generator | FJA |
| Demodulator | FKA |
| Bridge Rectifier | FLA, FLB |
| Power Amplifier Output Stage | FMA, FMB |
| Retract Inverter and Current Source | FNA |
| Function Generator | FOA, FOB, FOC, FOD, FOE, FOF, FOG, FOH |
| Reference Amplifier | FPA |
| Velocity, Acceleration Summing Network | FRA, FRB, FRC, FRD |
| Operational Amplifier | FSA, FSB |
| Velocity Summing Network | FTA |
| Position, Velocity, and Acceleration Summing Network | FUA, FUB |
| Position and Acceleration Network | FVA, FVB |
| Temperature Servo Amplifier | FWA |
| Temperature Sensing Amplifier | FWB |
| Gated Amplifier | FXB, FXC |
| AGC Rectifier | FYA, FYB |
| Diode Card | GAA, GAB, GAC |
| Brake/Clutch Driver | GBA |
| 500 Cycle Twin "T" Notch Network | GCA, GCB |
| Notch Networks | GCC, GCD |
| Pressure Transducer | GDA |
| Differential Pressure Gain and Balance | GEA |
| Long Stroke Acceleration | GFA, GFB |
| Differential Pressure and Acceleration Crossover Trim | GFC |

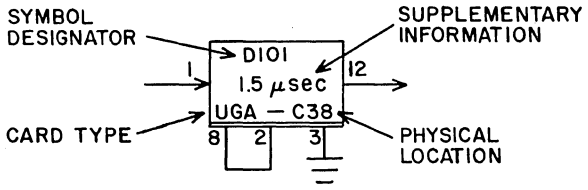
| | |
|---|---|
| Capacitor Card | GGA |
| Preamplifier | GHA |
| Read Level Detector | GIA, GIB |
| 800 & 1050 Hz Filter | GOA |
| Level Monitor | GSB |

## SPECIAL MODULES

LOGIC SYMBOLS

All special modules (including delays*) are represented by rectangles. Inputs are shown with arrows normally from the left, and outputs normally extend out to the right. Other connections to the card such as jumpers and grounds, except disabled OR inputs, are shown without arrowheads. The double bar on one or more sides of the symbol is used to indicate a non-logic voltage level.

EXAMPLE




* Passive delays such as capacitors mounted on a card are represented by an oval symbol (see section 2).

MODULE DESIGNATION

Five general categories are used for classifying special purpose circuits for peripheral equipment:

1. A-D (AA-, AB-, ····· DY-, DZ-)
2. E-H (EA-, EB-, ····· HY-, HZ-)
3. I-N (IA-, IB-, ····· NY-, NZ-)
4. O-T (OA-, OB-, ····· TY-, TZ-)
5. U-Z (UA-, UB-, ····· ZY-, ZZ-)

The two most significant letters (IA-, for example) define the basic circuit. The least signficant letter defines slight variations with the possibility of interchange in some but not all applications. Standard power supply connections are -20v on pin 13, ground on pin 14, +20v on pin 15, and no low impedance voltage sources on other pins. Standard voltage levels on input and output are -0.5v and -3v and match internal logic of standard cards such as flip-flops and inverters (including the 10, 20, and 30 series). Nonstandard input (or output) signals indicate one or more inputs (or outputs) that may be analog or digital, but cannot generally interface with standard cards such as flip-flops and inverters.

| Category | Designation | Power Supply | Input | Output |
|---|---|---|---|---|
| A | AAA to DZZ | Nonstandard | Standard or Nonstandard | Standard or Nonstandard |
| E | EAA to HZZ | Standard | Nonstandard | Nonstandard |
| I | IAA to NZZ | Standard | Standard | Nonstandard |
| O | OAA to TZZ | Standard | Nonstandard | Standard |
| U | UAA to ZZZ | Standard | Standard | Standard |

## 601 DAISY CHAIN LINE TRANSMISSION SYSTEM

The term "601 Daisy Chain Line Transmission System" is derived from its initial application as a digital-signal connection on a time-shared line between several (8 max.) 601 Tape Transports and a 3127 Controller. The following description contains background and ground rules for this system and presents information for other possible applications.

Design criteria included the following:

1. Three output amplifier circuits and three input amplifier circuits, 1604-type cards with pin assignments compatible with existing 69-and 87-type cards.
2. Provision for paralleling multiple output amplifiers (transmitters) and input amplifiers (receivers) at any point on the same line, with or without power supply voltage available.
3. Ability to transmit 1-usec logical "1" pulses from any output amplifier through any input amplifier to set a 1604-series flip-flop (500 kc maximum transmission rate).
4. Ability to operate with standard 24-pin I/0 cables (23 twisted pairs with one side of each pair grounded) over a length of 100 feet or more.
5. Simplification of terminators and bias voltages for terminators and output amplifiers.
6. Circuits capable of operating in 25°C to 50°C ambient air.

With the above basic design objectives, the approach was taken to simplify special output amplifier and terminator biasing requirements by employing line signals that drive away from ground. Thus both shorts and opens on a line result in a logical "0" at a receiver. Output amplifiers cannot drive a "1" on a line without power supply voltages, and both input and output amplifiers have disconnect features built in to prevent unwanted loading of the time-shared line when power supply voltages are off in some units.

The twisted-pair cable is satisfactory from an attenuation standpoint over 100-foot lengths but does present crosstalk problems unless rise and fall times are limited in volts per microsecond. A controlled rise and fall time of ½ usec for the 2-volt swing is used as a compromise

with speed. Crosstalk can be further reduced by using coax. However, unless bulky coax cables are used, attenuation increases and the characteristic impedance decreases; this requires greater line current (higher power levels) or lower voltage excursions, or results in reflections and ringing from improper terminations. The connector used with the 24-pin I/O cables permits the mounting of 23 terminating resistors directly to 23 pins (with one end of the resistors grounded to the remaining pin). Power in each termination is low (1/30 w for 120 ohms) for a logical "1" and essentially zero for a logical "0" on the line. This provides a terminator that can fit in the same space as a 24-pin I/O cable and still be reasonable in cost. Where module flexibility of extending cables is not required, input amplifiers with built-in terminating resistors are available; and the jumper option on the output amplifier may be employed without requiring external terminator resistors.

The voltage excursion of the output amplifier was selected to have a basic excursion that would be about five times the tolerance of the expected input amplifier switching threshold and twice the nominal switching threshold value of the input amplifier. A 2-volt excursion allows realistic tolerances in parts employed in the output and input amplifiers and a margin of safety for ringing, crosstalk, attenuation, and external interference for both logical "0" and logical "1" signals on the line. The positive excursion of the line connecting the output and input amplifiers was selected from a standpoint of circuit simplicity and cost. It is also more compatible with the newer positive logic computer circuits employing silicon components. In each circuit, two transistors are required. One transistor is used for inversion to standardize the voltage excursion over a small input threshold, and the other transistor provides current amplification.

The output amplifier, which receives its input from standard logic, was also designed to have a switching threshold tolerance that permits some noise on its input whether in the "0" or "1" state. Both stages of the output amplifier and one stage of the input amplifier use high-frequency npn silicon transistors. These provide a good compromise in voltage breakdown, power capability, and switching uniformity at moderate cost.

This system may not be ideal in <u>each</u> of the performance criteria,

but it does provide a useful application region within the following ground rules:

1. OS..series input amplifiers are designed to switch at +1.0±0.2v. System application should provide a minimum "1" line signal of +1.6v and a maximum "0" line signal of +0.3v. This allows a reserve for seldom-encountered signal interference and variable factors not usually predictable or easily measured, such as:
   a. Crosstalk from outside interference.
   b. Partial drive leakage from parallel output amplifiers not remaining completely off because of power supply coupling, for example. (This could produce an erroneous "1".)
   c. Slight changes in input amplifier switching because of aging, ambient temperature changes, or small errors in initial card testing measurements.
   d. Imperfections in ground reference points.

   The minimum "1" line signal of +1.6v and the maximum "0" line signal of +0.3v shall be attainable under <u>any</u> combination of the following worst-case conditions:
   a.* +20v power supply of IS..series or equivalent output amplifier at lowest expected value (minimum IS..series output voltage into a 60-ohm load is +2.0v with a +20v power supply and proportionably less as +20v is decreased).
   b.* Maximum line attenuation calculated on the basis of cable type and maximum distance between any output amplifier and input amplifier.
   c.* Maximum number of OS..or equivalent input amplifiers to be connected to a signal line. (With power on, each OS..causes a 0.03v maximum negative bias to a line terminated in 120 ohms at both ends.
   d. Maximum crosstalk from other signals in the cable. (Worst case is usually when other signals are closely in phase; position of worst-case crosstalk varies much over a cable length with cables.)

e. Maximum ringing because of reflections of non-ideal cable and termination conditions.

* These conditions (a, b, and c) tend to reduce the "1" line signal margins. It may be the best compromise to increase cable termination to 150 ohms where "1" signal margins are used up before the "0" signal margins. The following 24-pin terminators are documented for production. (Pin b is the ground reference in all units.)

| Part No. | Ohms ±5% |
|---|---|
| 45948500 | 56 |
| 45948501 | 68 |
| 45948502 | 82 |
| 45948503 | 100 |
| 45948504 | 120 |
| 45948505 | 150 |
| 45948506 | 180 |
| 45948507 | 220 |

2. If the rules of paragraph 1 are satisfied, up to 8 output and 8 input amplifiers may be paralleled on any signal line. They may be grouped or located at different locations. Lines should not "Y" out to several ends, although short stubs may be used to wire to input or output amplifiers. Terminators shall be placed within 3 feet of the end of each cable.

3. Time-shared lines are subject to a "1" coming from any output amplifier on the line. While the system is designed to work with either power on or off on inactive output amplifiers (no external bias required), power sequencing of equipment should provide one of the following during the turning on or turning off of power of any unit with an output amplifier:

   a. Disconnecting +20v from pin 15 of IS.. series cards during time any input can approach a logical "1" threshold.

   b. Clamping the input of the amplifier at ground and

assuring that the +20v supply does not exceed the -20v supply by more than 20 percent.

c. Disabling the AND gates at the output of all input amplifiers (receivers).

d. Providing a program that can repeat an operation when errors are received because of erroneous "1" signals coming from power sequencing operations.

4. The following card types are the present family of cards using this transmission system:

a. ISA Output Amplifier (3 circuits) -- preproduction version of the ISC, but with less predictable turnoff time from "1" to "0".

b. ISC Output Amplifier (3 circuits) -- 0.5 $\pm$0.15 usec rise and fall times. Optional 120-ohm termination to ground for each of the three circuits by using external jumpers. For best results, use caution on loading test point.

c. ITA Pulse Delay and Output Amplifier (1 circuit) -- pins 1 - 8 perform delay function of UGA. Pins 11 and 12 are output and optional 120-ohm termination respectively.

d. ASA Quantizer and Output Amplifier (3 circuits) -- Quantizing point is designed for about -6v but usable above and below this value with variations in fall time. Circuit is generally less uniform in output waveform than ISC. A 120-ohm terminating resistor is permanently wired to the output. Therefore, the circuit is designed to be located only at one of two ends of a line.

e. OSA Input Amplifier (3 circuits) -- No input termination resistor available. Input is single-ended to ground and output of each circuit has 3 AND diodes to match standard logic.

f. OSB Input Amplifier (3 circuits) -- Like the OSA except with 120-ohm input termination to ground. Therefore, the circuit is designed to be located only at one of the

two ends of a line. The OSB does not include all the line-loading disconnect features of the OSA when power is turned off.

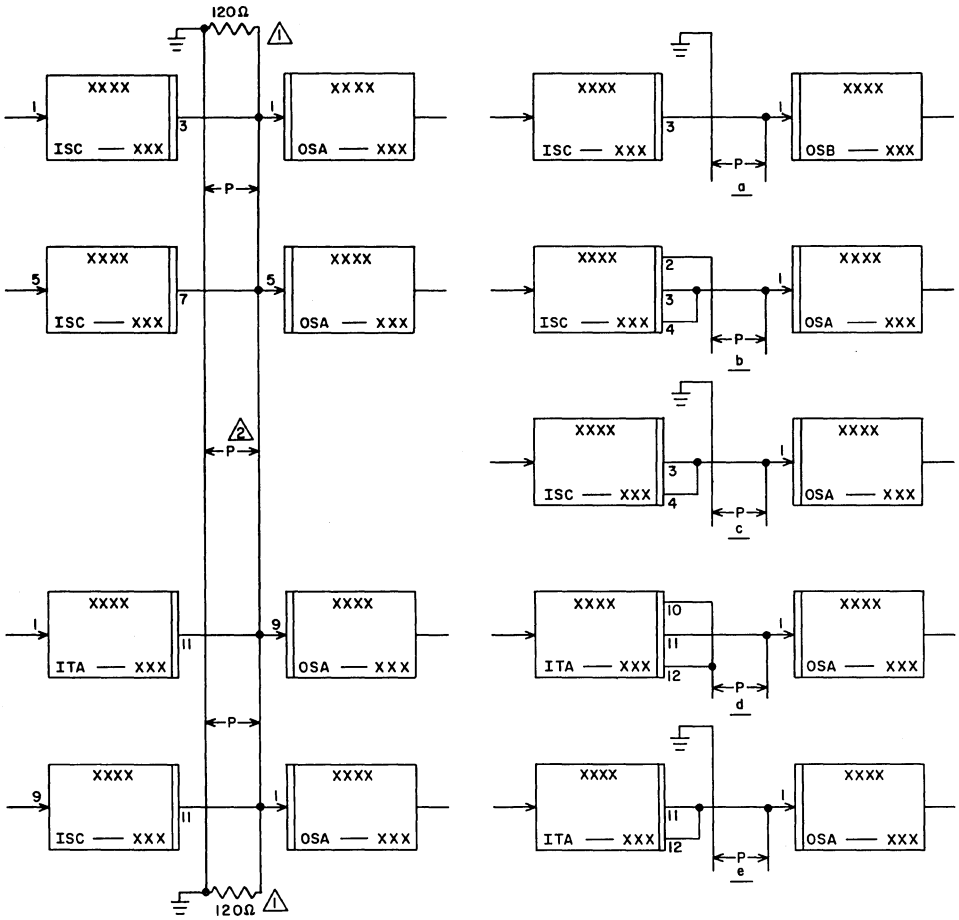
As required in future systems, the family of cards may be expanded to include the following:

a. Output amplifier with fast rise and fall times.

b. Output amplifier with 2 or 3 OR inputs but with only 2 circuits.

c. Input amplifier with differential input stage for common-mode interference rejection on twisted-pair lines.

d. Input amplifier with 0.7v nominal switching point for longer impedance terminations.




601 DAISY CHAIN WIRING SHOWING 4 OUTPUT AND 4 INPUT AMPLIFIERS ON A TIME — SHARED LINE

NOTE:
⚠1 ALTERNATE WAYS OF TERMINATING A LINE ARE SHOWN IN a, b, c, d, and e.
⚠2 TWISTED PAIR

# RELAY PULLER
## ABA

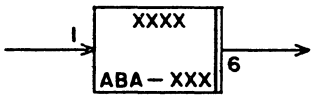
This circuit is used to drive high surge current loads such as lamps or the discharge of capacitors, or inductive loads such as relays and solenoids. It is particularly useful in driving loads up to 0.6 amp which are terminated at negative voltages between -5v and -36v.

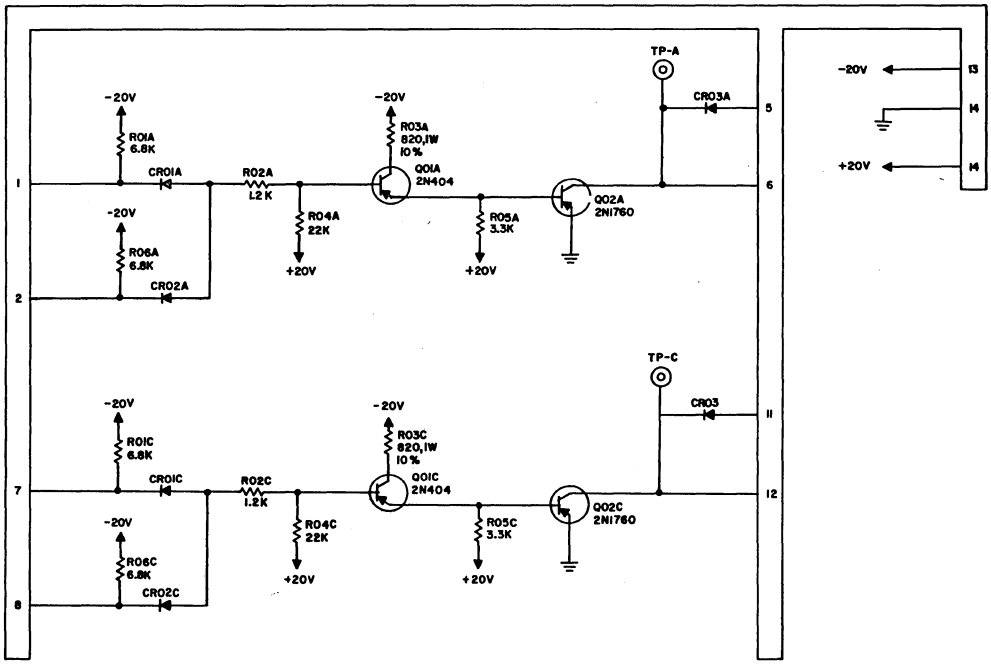
The relay puller circuit can also be used as a slow speed L--- card. The input-output voltage levels are the same for both cards.

This circuit is similar to the IAA relay puller, but has an added "OR" input on each of the two circuits as well as a clamping diode available on pins 5 and 11 to limit the negative excursion when inductive loads are switched off.

The input stage of the relay puller circuit has its transistor connected as an emitter follower with the collector returned to -20v through a limiting resistor, R03. The first stage emitter follower current does not flow through the load as it does in circuits such as the 55 card, thereby limiting collector voltage on Q01 to -20v; Q02 may have excursions to -50v. The only current flowing to the load in the turnoff condition is the leakage current of the output transistor. Turnon time is 5 usec maximum and turnoff switching is 25 usec maximum.

SYMBOL




TP-A
TP-C
-20V
+20V
R01A 6.8K
R02A 1.2K
R03A 820,1W 10%
R04A 22K
R05A 3.3K
R06A 6.8K
CR01A
CR02A
CR03A
Q01A 2N404
Q02A 2N1760
R01C 6.8K
R02C 1.2K
R03C 820,1W 10%
R04C 22K
R05C 3.3K
R06C 6.8K
CR01C
CR02C
CR03
Q01C 2N404
Q02C 2N1760
1
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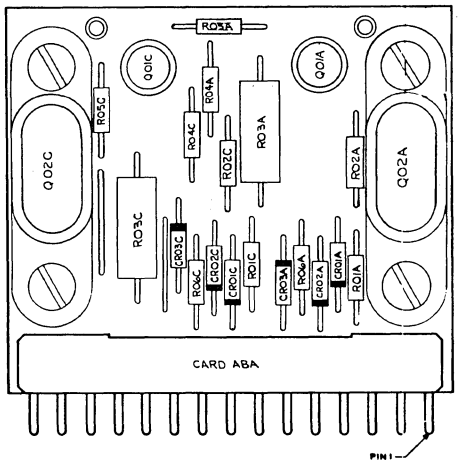
14
16

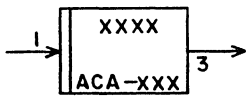

R03A
Q01C
Q01A
R05C
R04A
R04C
R02C
R03A
R02A
Q02C
Q02A
R03C
CR03C
R04C
CR02C
CR01C
R01C
CR03A
R04A
CR02A
CR01A
R01A
CARD ABA
PIN 1

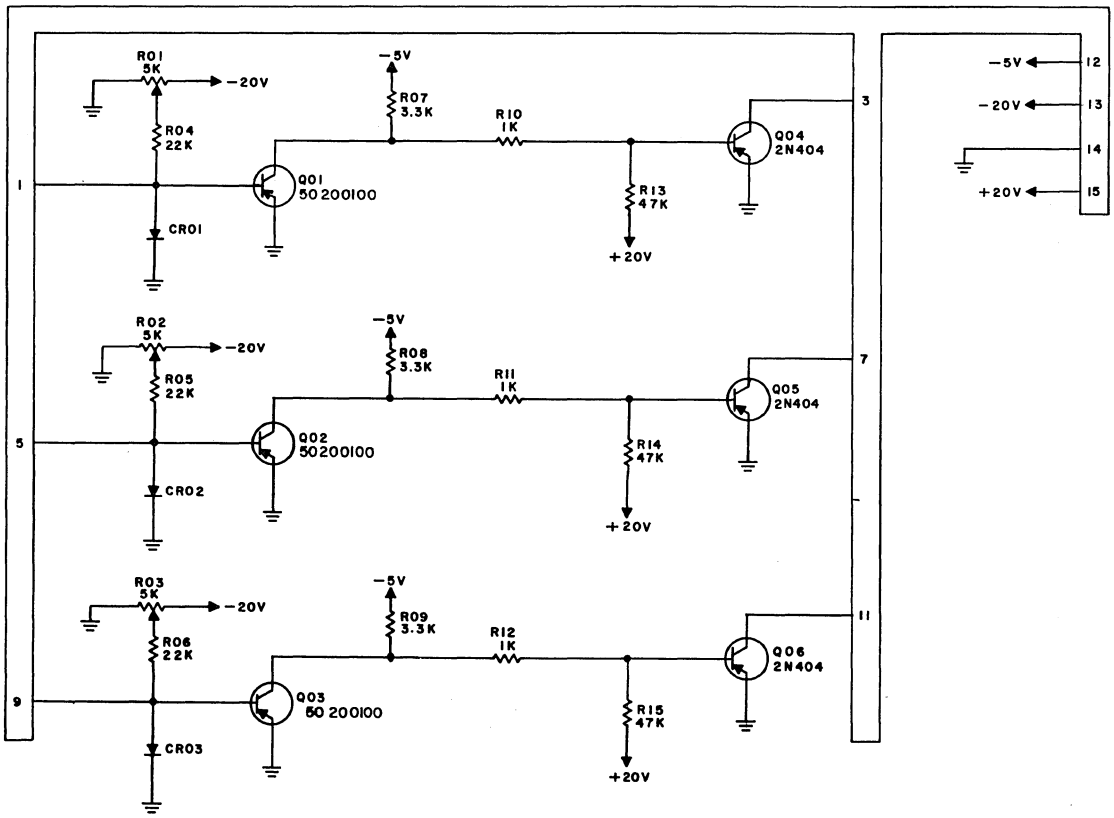
# PHOTODIODE BIAS AND PREAMPLIFIER
## ACA

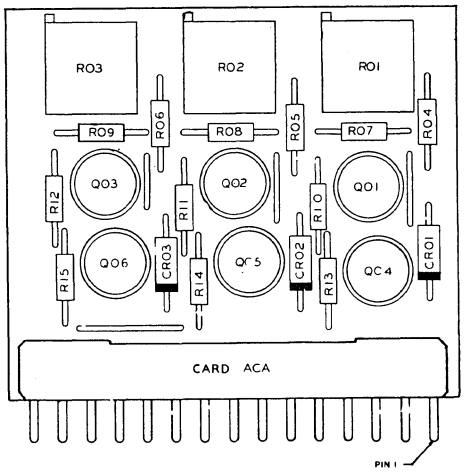
The photocell amplifier is designed to receive inputs from photodiodes or silicon solar cells. The output of the amplifier may be terminated by the input of a standard inverter or an "M" card. The output from the standard inverter or "M" card is a "1" when the photocell is illuminated and a "0" when unlighted. A potentiometer is provided because of the low level signals normally available from the solar cells and the wide range of sensitivity of photodiodes. This allows optimum centering of the switching point of the amplifier to compensate for the overall photocell excitation, sensitivity, and amplifier tolerance.

The first stage of amplifier A consists of an inverting amplifier, Q01. This transistor is turned on by drive current flowing through R04 from potentiometer R01. One lead of the photodiode is connected to pin 1 and the other lead is connected to a positive voltage source. Light on the photodiode causes its conductivity to increase and the photodiode current counteracts the turnon current of R01. CR01 limits the base to emitter voltage of Q01. When using solar cells, the positive terminal is normally connected to pin 1, and the output current of the solar cell counteracts the turnon current of R01.

**SYMBOL**




R01
5K
-20V
R04
22K
-5V
R07
3.3K
R10
1K
Q04
2N404
Q01
50200100
R13
47K
+20V
CR01
R02
5K
-20V
R05
22K
-5V
R08
3.3K
R11
1K
Q05
2N404
Q02
50200100
R14
47K
+20V
CR02
R03
5K
-20V
R06
22K
-5V
R09
3.3K
R12
1K
Q06
2N404
Q03
50200100
R15
47K
+20V
CR03
1
5
9
3
7
11
-5V
-20V
+20V
12
13
14
15


R03
R02
R01
R09
R06
R08
R05
R07
R04
Q03
Q02
Q01
R12
R11
R10
CR03
CR02
CR01
Q06
QC5
QC4
R15
R14
R13
CARD ACA
PIN 1

# HAMMER DRIVER CARD
## ADA, ADB

These cards are intended for low-speed switching of high current pulses of 1.5 to 4.5 msec duration into an inductive load such as the hammers, clutch, or brake in a 501 Printer. An open circuit on pin 1 or -3 volts will keep the circuit off. Driving pin 1 to within -0.5 volt of ground allows a current pulse to flow up to 10 amp for the ADA and 7 amp for the ADB. The duty cycle should be no greater than 12 percent, to avoid excessive heating. The minimum input pulse width needed to reach 2 percent of the maximum current level with an inductive load should be about 4 times the L/R time constant of the load. The total collector circuit resistance should be sufficient to limit the load current to 10 amp maximum for the ADA. The ADB has a 4-ohm resistor mounted on the card in the collector circuit of Q03. With a purely resistive load, the current rises to the 10 amp level in 20 usec typically.

For normal operation of the circuit, the following connections are made (see circuit schematic). One side of the load plus the limiting resistor (for the ADA) is connected to pin 10 or 11. The other side is connected to the high current negative supply which can have a maximum value of -38 volts but is nominally -36 volts. Pin 8 is also connected to the -36v supply. This returns a suppression circuit consisting of CR05 and R07 to the emitter of Q03 via the power supply (-36v) common at pins 5 and 6. For good inductive spike supression, it is evident that the -36 volt lines and power supply impedance must be low. The suppressed pulse is about 10v greater than the power supply voltage. The usual + and -20 volt supplies must also be furnished to the circuit. Normally, the logic ground and high current ground are tied together at the card connector. This is done to minimize the tendency for the circuit to oscillate.

Referring to the schematic, the circuit operates as follows. Transistors Q02 and Q03 comprise a Darlington pair in a collector-loaded switch circuit. This pair is normally off with pin 1 at -3 volts. Transistor Q01 conducts when pin 1 is -3v; its collector is

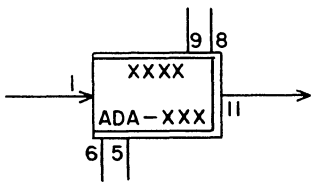
then at ground. This establishes +1.2 volts on the base of Q02 due to current flow from the +20 supply through R05 and silicon diodes CR02 and CR03 to ground. The emitter of Q02 and hence the base of Q03 is at +0.5 volt due to current from +20 volt through R06 and CR04 to ground. Both Q02 and Q03 are therefore off because of the reverse base voltages.

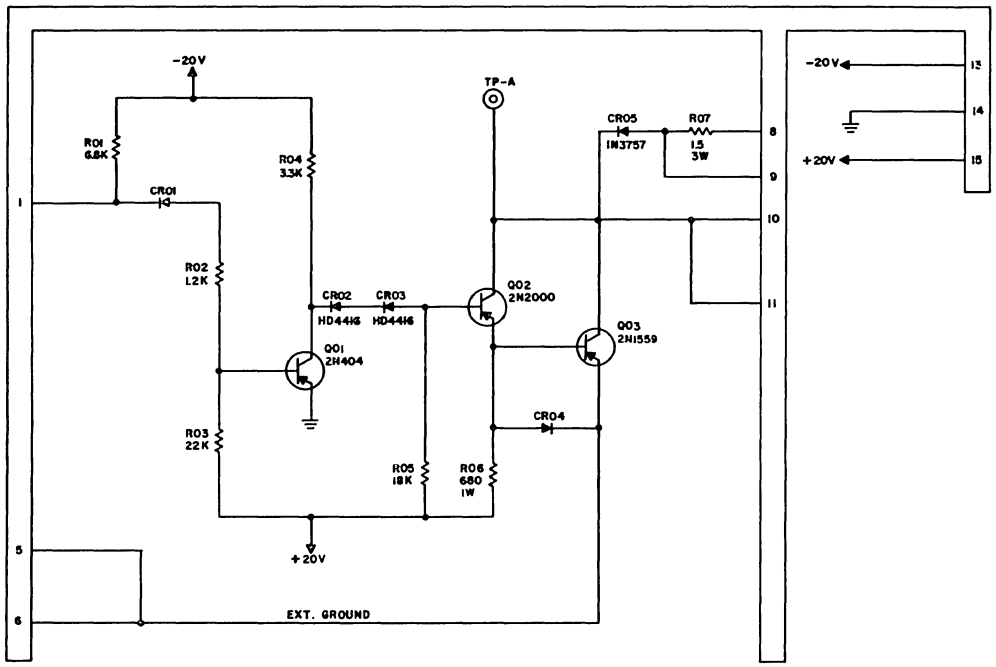
When the input goes to within -0.5 volt of ground, transistor Q01 goes off due to the divider action of R02, R03, and CR01, i.e., the base becomes positive. With Q01 collector unclamped, base current begins to flow in Q02 and Q03 from ground to the -20v supply by way of the collector load resistor R04. This turns on the Darlington circuit and lets load current flow.

In the on state and with a 10 amp load on the ADA card, the collector to emitter voltage of Q03 is about 0.5 volt. With a 12 percent duty cycle the power dissipated in Q03 is about 0.75 watt. In free air (i.e., natural convection) this dissipation causes Q03 to attain 135°F case temperature in 80°F ambient.

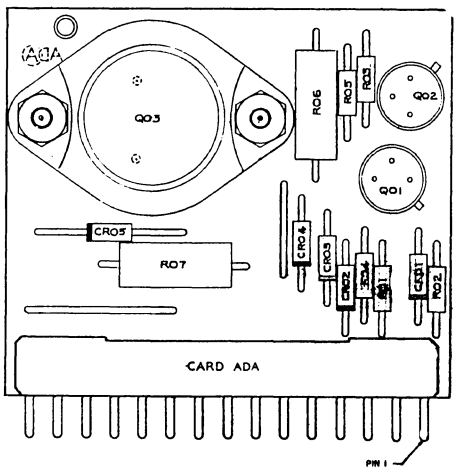
It is recommended that these cards be placed in moving air and away from any temperature sensitive circuits.

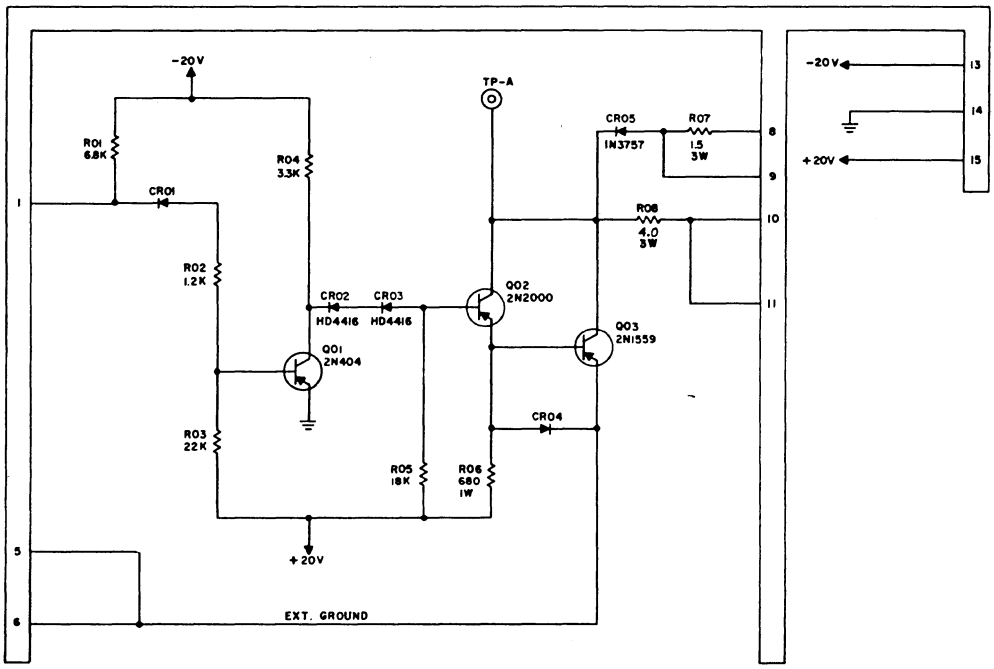
SYMBOL



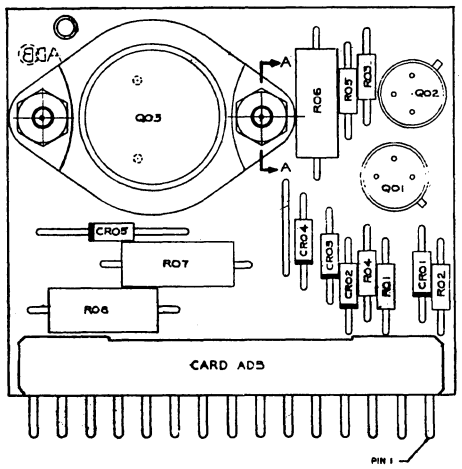

-20V
TP-A
R01
6.8K
R04
3.3K
CR01
CR05
IN3757
R07
1.5
3W
-20V
+20V
R02
1.2K
CR02
HD4416
CR03
HD4416
Q02
2N2000
Q03
2N1559
Q01
2N404
CR04
R03
22K
R05
18K
R06
680
1W
+20V
EXT. GROUND
1
5
6
8
9
10
11
13
14
15

ADA


ADA
Q03
R06
R05
R03
Q02
Q01
CR05
R07
CR04
CR03
CR02
CR01
R02
CARD ADA
PIN 1


-20V
TP-A
R01
6.8K
R04
3.3K
CR01
R02
1.2K
CR02
HD4416
CR03
HD4416
Q01
2N404
Q02
2N2000
Q03
2N1559
CR04
R03
22K
R05
18K
R06
680
1W
+20V
EXT. GROUND
CR05
IN3757
R07
1.5
3W
R08
4.0
3W
-20V
+20V
1
5
6
8
9
10
11
13
14
15

ADB


Q03
R06
R05
R03
Q02
Q01
CR05
R07
R08
CR04
CR03
CR02
R04
R01
CR01
R02
CARD ADB
PIN 1

# HAMMER DRIVER
## ADC, ADD, ADE

The ADC, ADD, and ADE cards are used in the 501 Printer to supply 5 amp (ADC) and 7 amp (ADD, ADE) current pulses of 1.3 msec duration to the basically inductive hammer coils. An open circuit on pin 1 or -3 volts will keep the circuit off. Driving pin 1 to within -0.5 volt of ground lets the load current rise to its 5 or 7 amp levels. The maximum duty cycle of 3 percent must not be exceeded in order to keep the average transistor dissipation to a safe level.

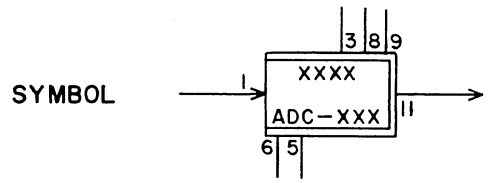
For normal operation of the circuit, the following connections are made (see circuit schematic). One side of the hammer coil is connected at pin 10 or 11 and the other side is connected to the high-current negative power supply. The negative supply voltage is nominally -29 volts for the ADC and -36 volts for the ADD and ADE. Pin 7 or 8 is also connected to this negative supply for suppression of the inductive kick pulse. Since the suppression circuit is returned to the circuit common via the line and supply impedances, these must be kept low to insure reduction of the voltage spike across Q03. The suppressed pulse across Q03 on the hammer driver cards is limited to about 10 volts. The inductive kick pulse is brought out to pin 9. This may be used in conjunction with the OLA card in error checking systems. The pulse is about 100 usec wide with the ADC and 1 msec with the ADD and ADE cards.

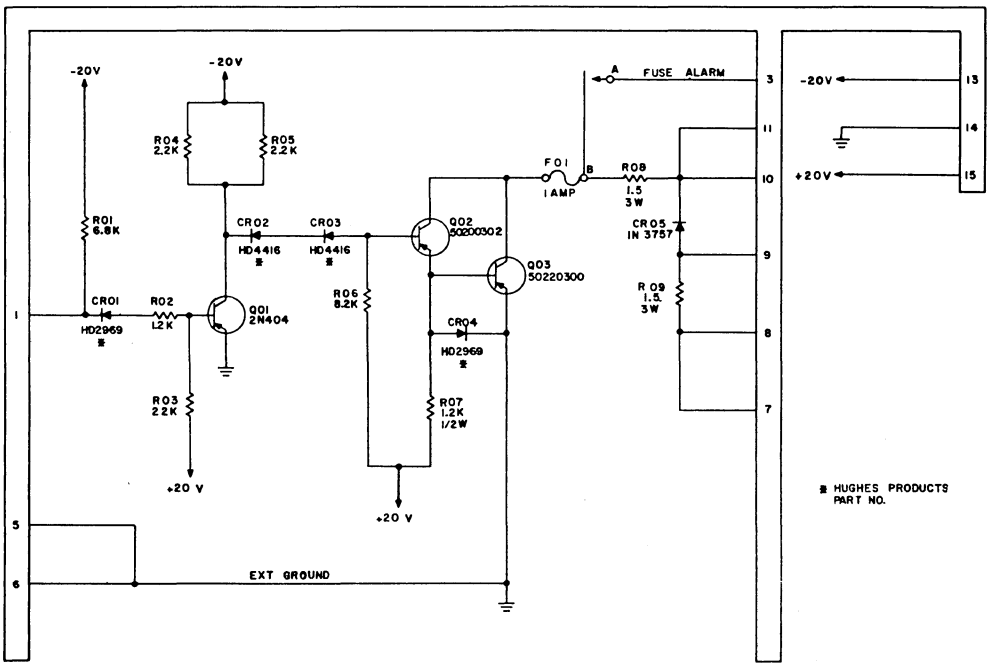
Referring to the schematic, the circuit operates as follows. Transistor pair Q02 and Q03 make up a Darlington switching circuit. The pair is normally off when pin 1 is at -3 volts on the base of Q02 due to current flow from the +20 supply through R06 and silicon diodes CR02 and CR03 to ground. The emitter of Q02 and hence base of Q03 is at +0.5 volt due to current flow from +20 volts through R07 and CR04 to ground. Both Q02 and Q03 are therefore off because of the reverse base voltage.

When the input goes to within -0.5 volt of ground, transistor Q01 goes off due to the divider action of R02, R03, and CR01, i.e., the base becomes positive. With Q01 collector unclamped, base current begins to flow in Q02 and Q03, from ground to the -20v supply by way of collector load resistors R04 and R05 in parallel. This turns on the

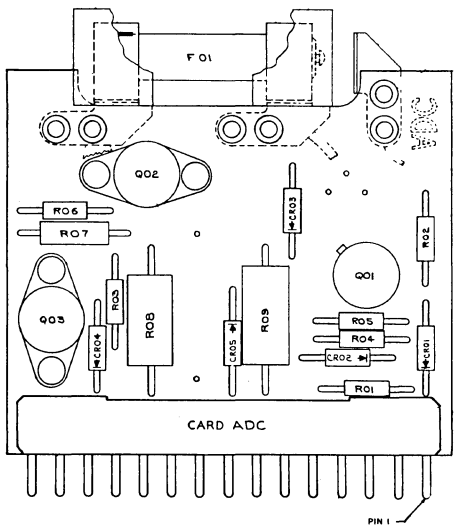
Darlington pair and allows the load current to flow.

In the on state and with a 3 percent duty cycle, the average dissipation in the collector load resistor with 7 amp and 3 percent duty cycle is about 2 watts. This gives a temperature on the resistor of about 180° F. This necessitates placing the card in moving air to eliminate damage to the card.

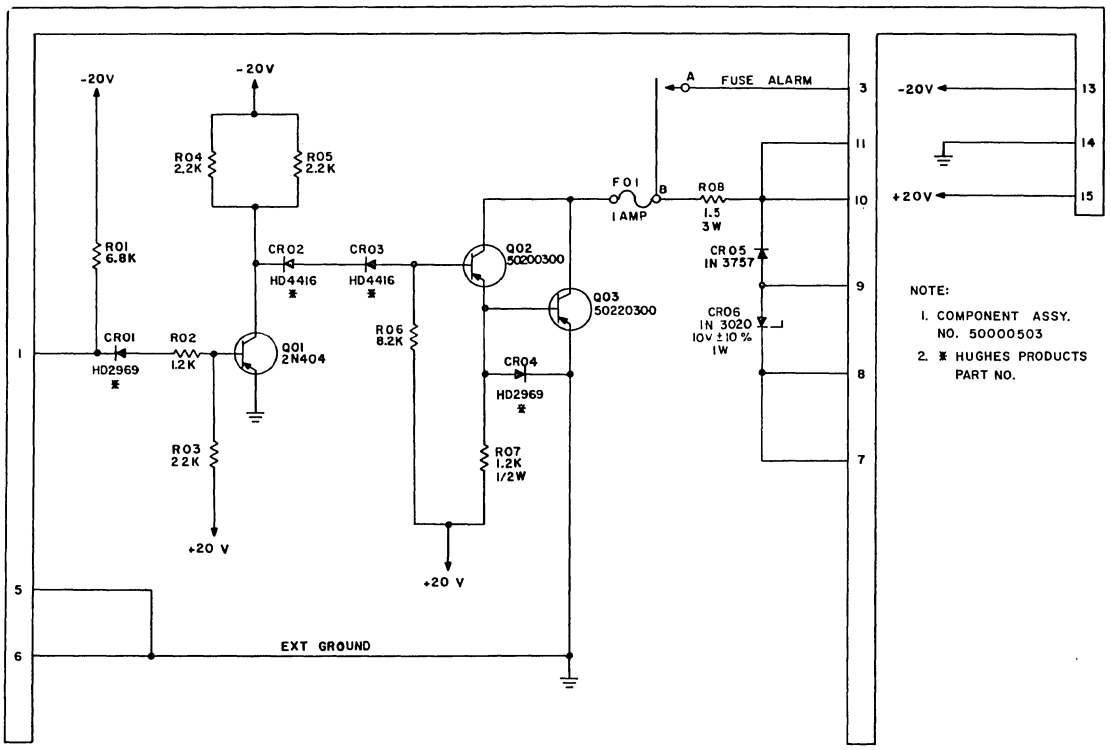


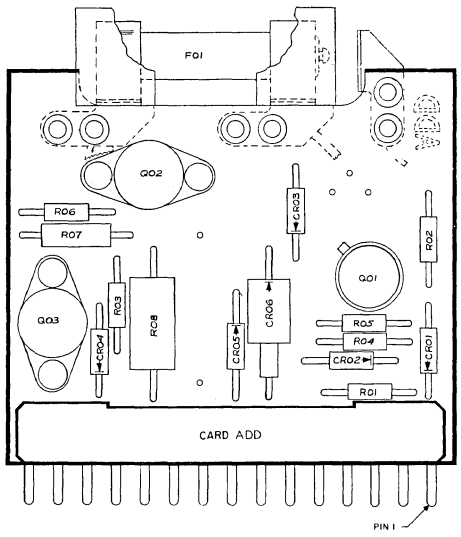

ADC

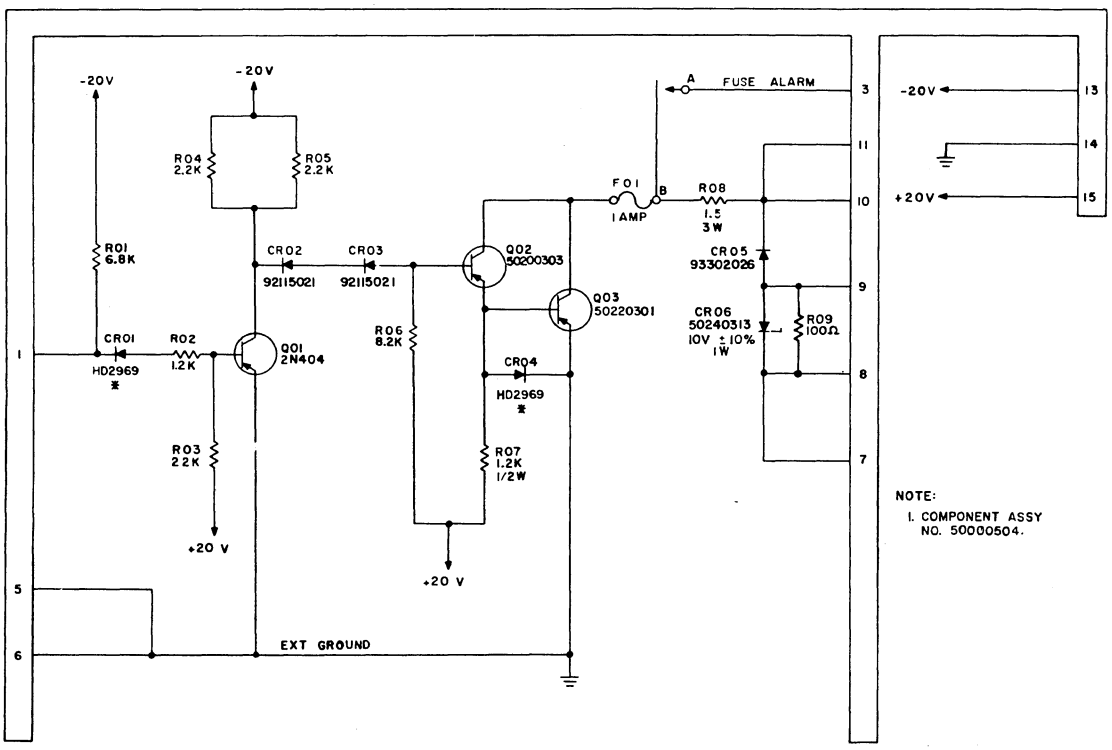



6-ADC, ADD, ADE-2

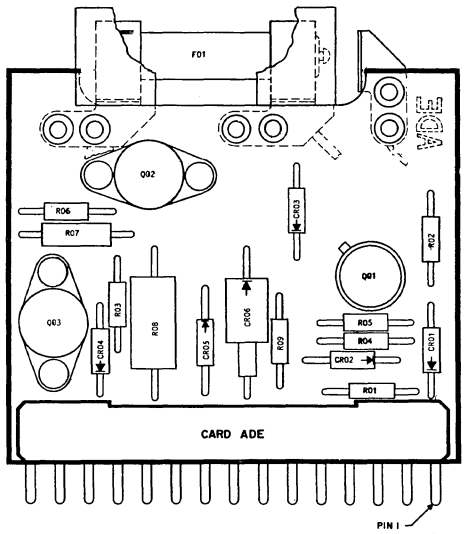

-20V
-20V
R04 2.2K
R05 2.2K
R01 6.8K
CR02
HD4416
CR03
HD4416
Q02 50200300
Q03 50220300
F01 1 AMP
A
FUSE ALARM
R08 1.5 3W
CR05 IN 3757
CR06 IN 3020 10V ±10% 1W
CR01 HD2969
R02 1.2K
Q01 2N404
R06 8.2K
CR04 HD2969
R03 2.2K
R07 1.2K 1/2W
+20 V
+20 V
EXT GROUND
-20V
+20V
NOTE:
1. COMPONENT ASSY. NO. 50000503
2. ✱ HUGHES PRODUCTS PART NO.

ADD


F01
Q02
R06
R07
CR03
R02
Q01
Q03
R03
R08
CR06
CR05
CR04
R05
R04
CR02
CR01
R01
CARD ADD
PIN 1


-20V
-20V
R04 2.2K
R05 2.2K
R01 6.8K
CR01 HD2969 *
R02 1.2K
Q01 2N404
R03 22K
+20 V
CR02 92115021
CR03 92115021
Q02 50200303
Q03 50220301
R06 8.2K
CR04 HD2969 *
R07 1.2K 1/2W
+20 V
EXT GROUND
A
FUSE ALARM
F01 1 AMP
B
R08 1.5 3W
CR05 93302026
CR06 50240313 10V ± 10% 1W
R09 100Ω
-20V
+20V
1
3
5
6
7
8
9
10
11
13
14
15
NOTE:
1. COMPONENT ASSY NO. 50000504.

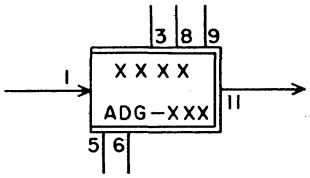
ADE

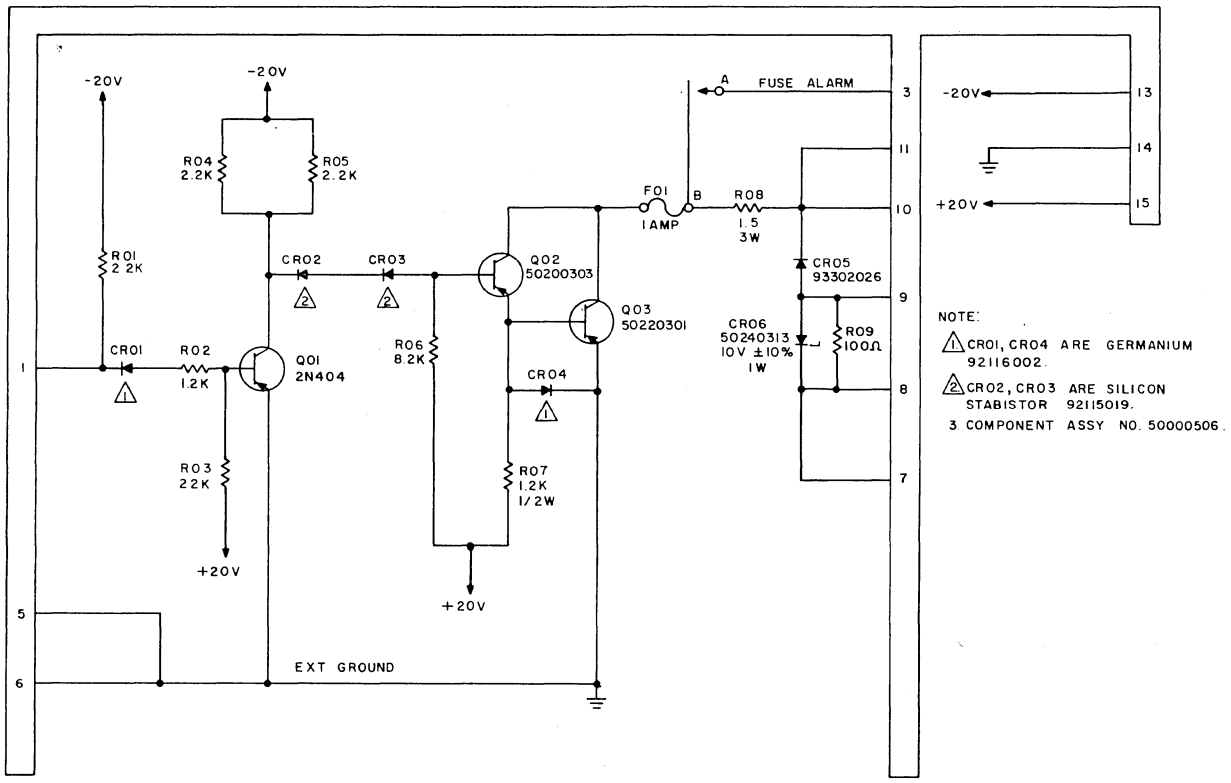

F01
Q02
R06
R07
CR03
R02
Q01
Q03
R03
R08
CR04
CR05
CR06
R09
R05
R04
CR02
CR01
R01
CARD ADE
PIN 1

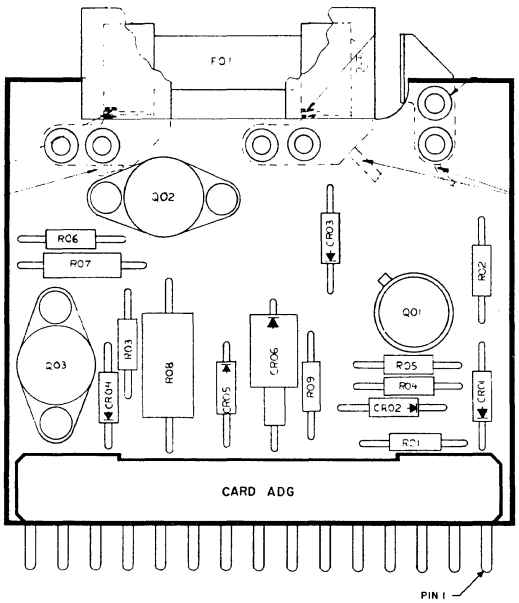
HAMMER DRIVER

ADG

The ADG is designed to minimize the possibility of turn on during controller power down. Except for a value of 2.2K ohms for R01 and the use of a different diode for CR02 and CR03, the ADG is similar to the ADE in circuit operation, application information, and output current.




-20V
-20V
R04
2.2K
R05
2.2K
R01
2.2K
CR01
R02
1.2K
Q01
2N404
R03
22K
+20V
CR02
CR03
Q02
50200303
Q03
5022030I
R06
8.2K
CR04
R07
1.2K
1/2W
+20V
EXT GROUND
A
FUSE ALARM
F01
1 AMP
B
R08
1.5
3W
CR05
93302026
CR06
50240313
10V ±10%
1W
R09
100Ω
-20V
+20V
1
3
5
6
7
8
9
10
11
13
14
15
NOTE:
1 CR01, CR04 ARE GERMANIUM 92116002.
2 CR02, CR03 ARE SILICON STABISTOR 92115019.
3 COMPONENT ASSY NO. 50000506.


F01
Q02
R06
R07
CR03
R02
Q01
Q03
R03
R08
CR06
R09
R05
R04
CR02
R01
CR04
CR05
CR01
CARD ADG
PIN 1

# CLUTCH-BRAKE DRIVER
## ADH

This card is used for low-speed switching of high current pulses of 4.5 msec duration into an inductive load such as the clutch or brake in a 501 printer. An open circuit on pin 1 or -3 volts will keep the circuit off. Driving pin 1 to within -0.5 volts of ground allows a current pulse up to 15 amperes to flow. The duty cycle should be no greater than 12 percent. The minimum input pulse width needed to get 15 amperes into an inductive load should be about 4 times the L/R time constant of the load. An external resistor has to be added to limit the current to 15 amperes maximum. With a resistive load, the minimum input pulse width should be as great as the rise time of the circuit - in this case, 50 usec.

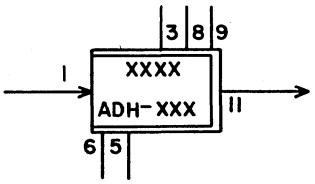
For normal operation of the circuit the following connections are made (see circuit schematic). One side of the load plus the limiting resistor is connected to pin 10 or 11. The other side is connected to the high current negative supply, which can have a maximum value of -38 volts but is nominally -36 volts. Pin 8 is also connected to the -36v supply. This returns a suppression circuit consisting of CR05 and R07 to the emitter of Q03 via the power supply (-36v) common at pins 5 and 6. For good inductive spike suppression, it is evident that the -36 volt lines and power supply impedances must be low. The suppressed pulse is about 10v greater than the power supply voltage. The usual + and -20 volt supplies must also be furnished to the circuit. Normally the logic ground and high current ground are tied together at the card connector, (i.e., jumper pins 5 and 14).

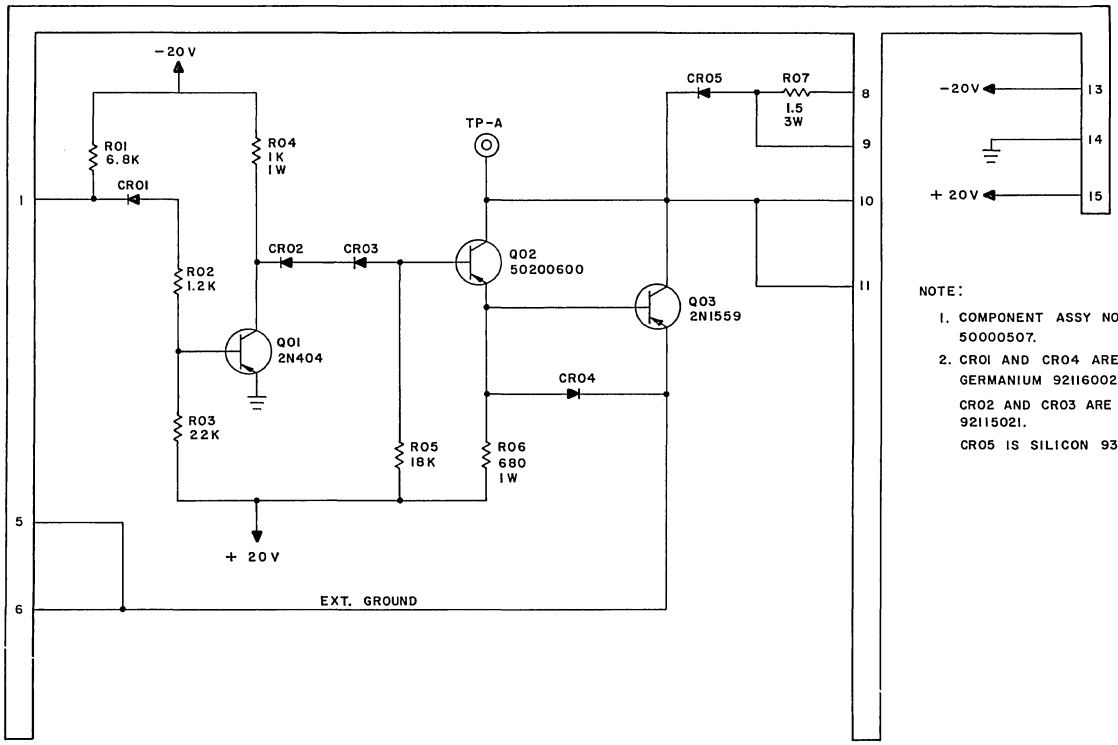
Referring to the schematic, the circuit operates as follows. Transistors Q02 and Q03 comprise a Darlington pair in a collector-loaded switch circuit. This pair is normally off with pin 1 at -3 volts. Transistor Q01 conducts when pin 1 is -3v; its collector is then at ground. This establishes +1.2 volts on the base of Q02 due to current flow from the +20 supply through R05 and silicon diodes CR02 and CR03 to ground. The emitter of Q02 and hence the base of Q03 is at +0.5 volts due to current from +20v through R06 and CR04 to ground. Both Q02 and Q03 are therefore off because of the reverse base voltages.

When the input goes to within -0.5 volts of ground, transistor Q01 goes off due to the divider action of R02, R03, and CR01, i.e., the base becomes positive. With Q01 collector unclamped, base current begins to flow in Q02 and Q03 from ground to the -20v supply by way of the collector load resistor R04. This turns on the Darlington circuit and lets load current flow.

In the on state and with a 15-ampere load, the collector to emitter voltage of Q03 is about 1.2 volts. With a 12 percent duty cycle, the average power dissipated in Q03 is about 2 watts. In free air (i.e., natural convection) at room temperature of 80°F, this dissipation causes Q03 to attain 175°F case temperature. With this high temperature on the card, it is suggested that the card be located in moving air and away from any temperature sensitive circuits.

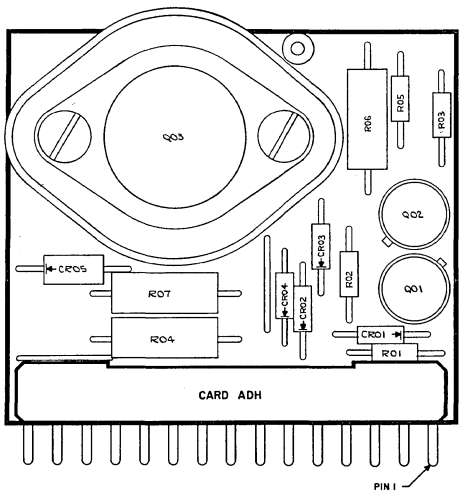
SYMBOL






NOTE:

1. COMPONENT ASSY NO. 50000507.
2. CR01 AND CR04 ARE GERMANIUM 92116002.
   CR02 AND CR03 ARE SILICON 92115021.
   CR05 IS SILICON 93302026.



OUTPUT DRIVER
AEB

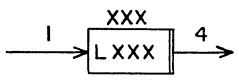
This output driver is used to operate on a common line with other equipment having similar output drivers attached to the same common line. The driver meets the common line requirement that it disconnect itself from signals on the common line whether power is on or off. This power off requirement is satisfied only if a positive voltage of 5 volts or more remains on pin 15. For these particular circuits the internal machine plus 20v is "ORed" with a plus 15v bus from the controller.

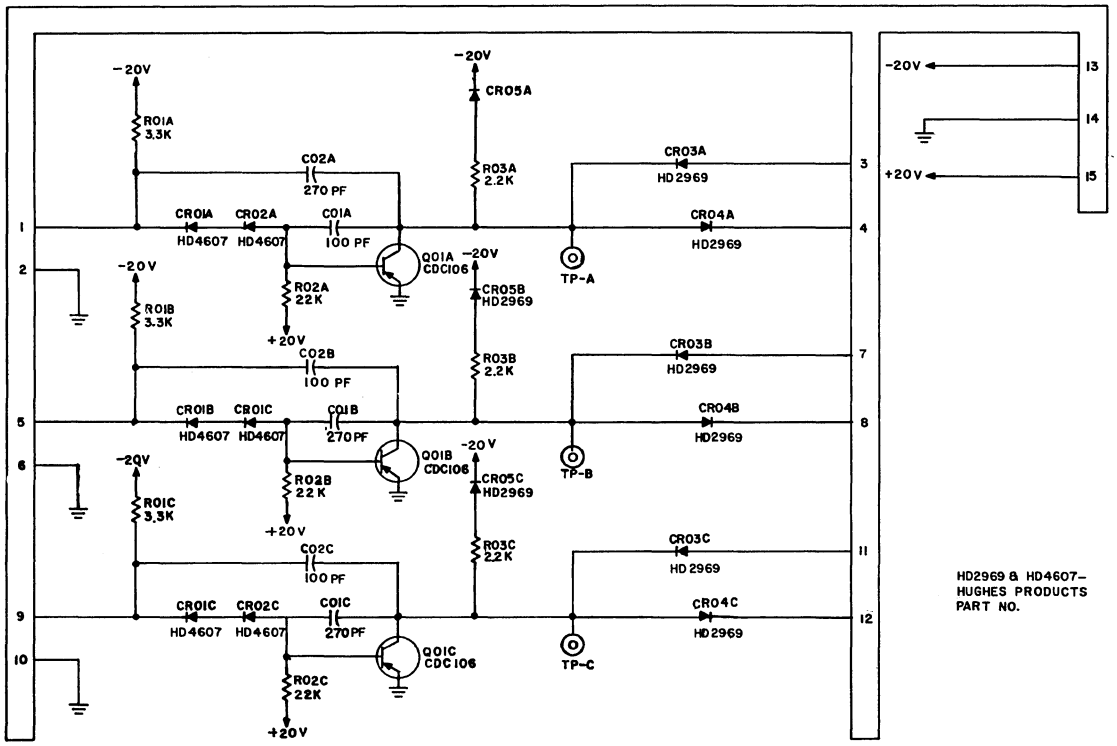
The circuit is designed around the type and length of interconnecting cable (100 ft. max) to provide optimum rise (0.35 to 1.0 use) and fall time (0.30 to 0.65 usec).

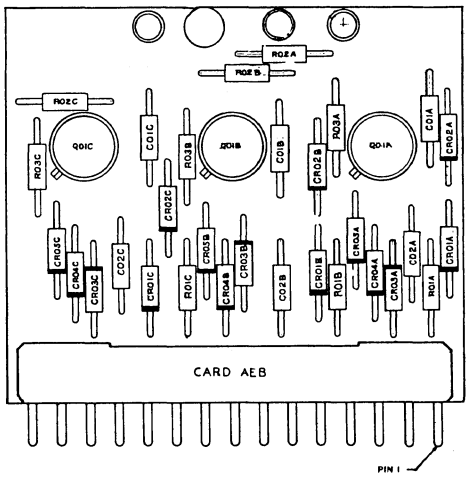
The circuit is a switching type inverter with certain variations. R01 reflects twice the usual load to the previous circuit. CR01 and CR02 are forward biased silicon diodes to improve the efficiency of the base divider of Q01. Capacitors C01 and C02 provide the proper combination of feedback to achieve the desired rise and fall times. Diode CR03 is connected to a minus 8-volt clamp to obtain the desired negative excursion of 8 volts. Diode CR04 prevents loading of this circuit in a negative direction when another signal is on the common line. Diode CR05 prevents loading of this circuit in a positive direction when another signal is on the common line.

A total of 85 ma output current is available for the receiver load, for charging the line capacity, and for driving small shunt leakages in parallel drivers on the same common line.

SYMBOL




-20V
R01A 3.3K
C02A 270 PF
CR01A HD4607
CR02A HD4607
C01A 100 PF
Q01A CDC106
R02A 22K
+20V
CR05A
R03A 2.2K
CR03A HD2969
CR04A HD2969
TP-A
R01B 3.3K
C02B 100 PF
CR01B HD4607
CR01C HD4607
C01B 270 PF
Q01B CDC106
R02B 22K
CR05B HD2969
R03B 2.2K
CR03B HD2969
CR04B HD2969
TP-B
R01C 3.3K
C02C 100 PF
CR01C HD4607
CR02C HD4607
C01C 270PF
Q01C CDC106
R02C 22K
CR05C HD2969
R03C 2.2K
CR03C HD2969
CR04C HD2969
TP-C
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
HD2969 & HD4607- HUGHES PRODUCTS PART NO.


CARD AEB
PIN 1

# MULTIPLE TIME DELAY
## AFA, AFB

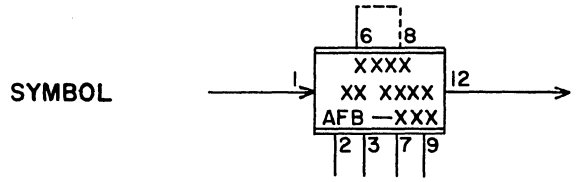
The multiple time delay card is used to delay the positive transition of an input (logic level) signal an amount of time determined by the RC time constant in the circuit. The resistance portion of the time constant includes a linear variable resistor which can be preset to give a particular delay time. More than one preset variable may be used to control the delay time of the circuit, but only one should be connected at a time. An electronic switch can be used to switch the proper resistor into the circuit (enable amplifier, type AG-series).

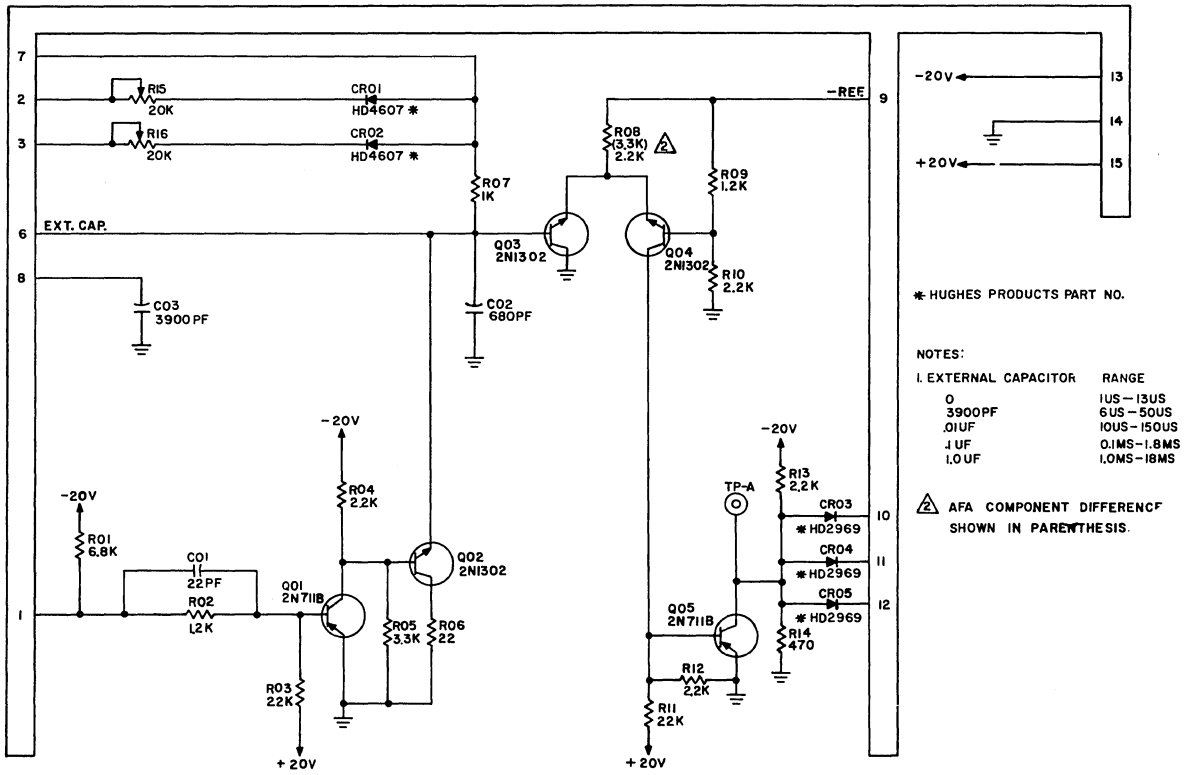
The delay circuit is armed by having a "1" input on pin 1 for 0.5 usec or more for a total delay capacitance of 5000 pf. The delay time accuracy is within $\pm 2$ percent over a temperature range of 0° to 50°C. For 5000 pf delay capacitance, the delay from an input "1" to an output "1" does not exceed 0.1 usec.

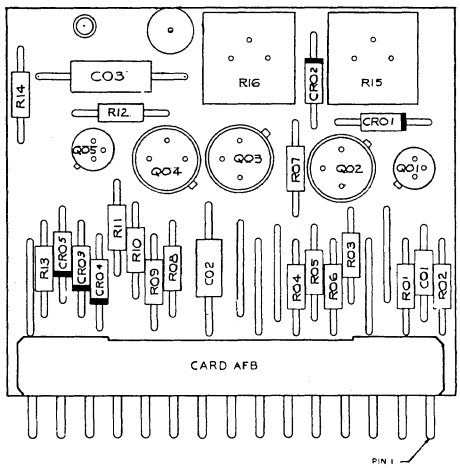
A signal on the input (pin 1) switching from a logical "1" to a "0" causes Q01 to turn off. Its collector goes to about -12v allowing emitter follower Q02 to cease conducting. Capacitor C02 (and the external capacitor if connected) starts charging through resistor R07, diode CR01, and variable resistor R15 to a negative reference voltage (pin 2). A small amount of charging current flows through transistor Q03. At the predetermined delay time, the voltage at capacitor C02 reaches the same voltage (-10v) that appears at the junction of resistors R09 and R10. The voltage supplied to resistor R09 is from the same negative reference as that supplied to R15. The differential amplifier, Q03 and Q04, switches state so that Q03 is now nonconducting and Q04 is conducting. This causes the base of transistor Q05 to go negative and start conducting, thus switching the output from "1" to "0". Similar operation is achieved using variable resistor R16 (pin 3) in the charging circuit and grounding R15 (pin 2). The diode connected to the grounded resistor serves to isolate the resistance from the timing circuit being used during the delay period.

Recovery of the circuit is accomplished by returning the input to a "1". Transistor Q01 turns on, thus grounding (-0.2v) the base of Q02. The emitter of Q02 follows, discharging capacitor C02 (and ex-

ternal capacitor) through Q02 and resistor R06. Resistor R06 limits the current thus protecting transistor Q02 from burnout. Differential amplifier, Q03 and Q04, returns to its original state with Q03 on and Q04 off. Resistor R11 reverses the base current to transistor Q05 allowing the output to return to a "1".



ENABLE AMPLIFIER

AGA

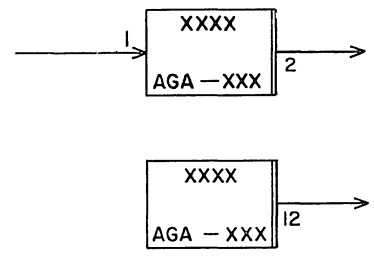
The enable amplifier card is used to select the proper variable resistor and provide a reference voltage for the time delay circuit (AF-series). There are three switching circuits per card.

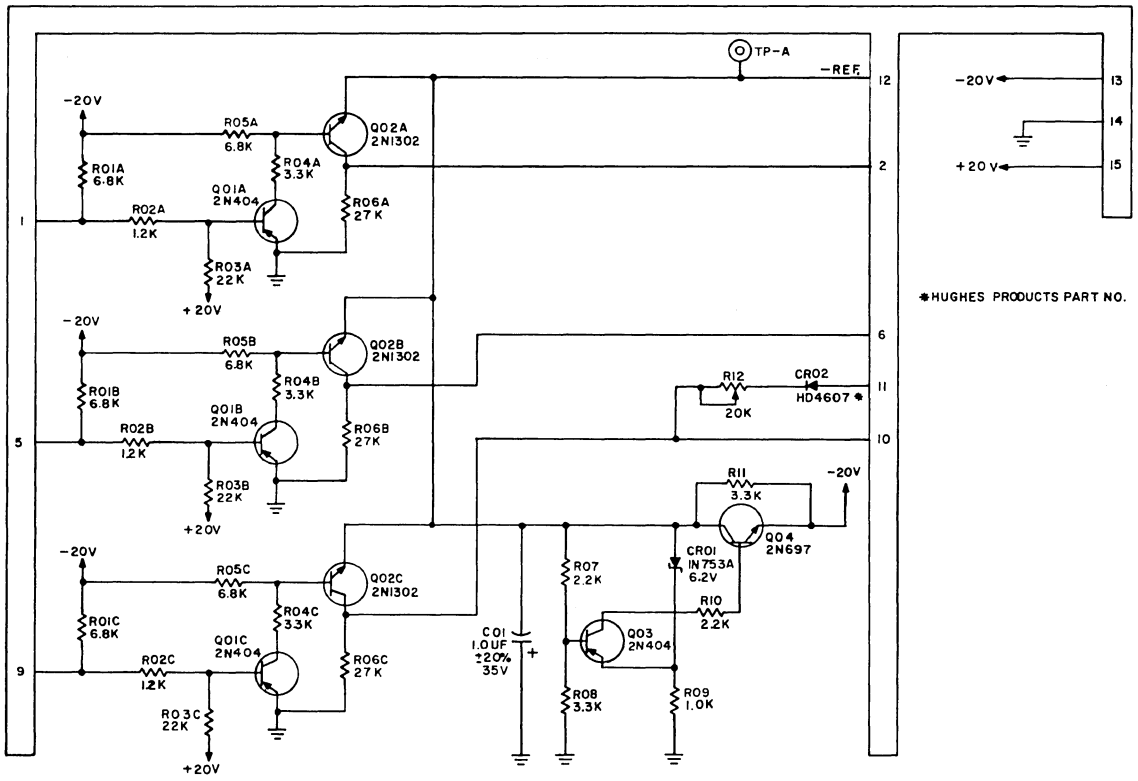
A logical "0" applied to the input pin (three identical circuits) causes transistor Q01 to turn off, allowing its collector voltage (through R04 and R05) to go more negative than the reference voltage at the emitter of Q02. Thus, Q02 is turned off allowing its collector voltage (output) to be at ground potential.

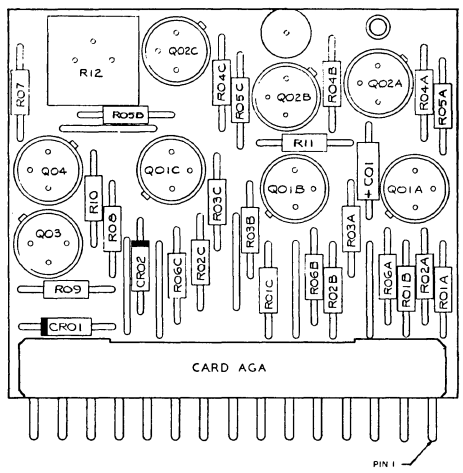
A logical "1" applied to the input pin causes transistor Q01 to turn on, grounding its collector (-0.2v) and turning on Q02 by providing base current through R04. The collector (output) of Q02 then goes to the reference voltage (about -15v). Thus, an external circuit element may be switched to the reference voltage when a "1" is applied to the enable amplifier and returned to ground when a "0" is applied.

The reference voltage section supplies a regulated and filtered current at -15v. This voltage is supplied to both the variable resistor and the differential amplifier on the time delay card (AF-series). The voltage is regulated in the following manner. Resistor R11 supplies starting current to the bridge composed of R07, R08, R09, and CR01. Transistor Q03 senses any voltage difference between the two legs of the bridge and changes the current to the base of transistor Q04 in proportion to the error in voltage. This allows Q04 to supply more or less current to the bridge and load such that the voltage returns to the normal value. Voltage regulation is in the order of $\pm$ 2% for load current up to 100 ma (instantaneous).

SYMBOL




TP-A
-REF
-20V
+20V
R01A 6.8K
R02A 1.2K
R03A 22K
R04A 3.3K
R05A 6.8K
R06A 27K
Q01A 2N404
Q02A 2N1302
R01B 6.8K
R02B 1.2K
R03B 22K
R04B 3.3K
R05B 6.8K
R06B 27K
Q01B 2N404
Q02B 2N1302
R01C 6.8K
R02C 1.2K
R03C 22K
R04C 3.3K
R05C 6.8K
R06C 27K
Q01C 2N404
Q02C 2N1302
R12
CR02
HD4607 *
20K
R11 3.3K
Q04 2N697
CR01 IN753A 6.2V
R10 2.2K
R07 2.2K
C01 1.0UF ±20% 35V
Q03 2N404
R08 3.3K
R09 1.0K
1
5
9
12
2
6
11
10
13
14
15
*HUGHES PRODUCTS PART NO.


R12
Q02C
Q02B
Q02A
Q04
Q01C
Q01B
Q01A
Q03
R09
CR01
CR02
C01
CARD AGA
PIN 1

# FLIP-FLOP DRIVER
# AHA, AHC

These flip-flop drivers are a special circuit designed for economical shift registers used in large quantities in optical character reading equipment. Capacitor coupled inputs allow a single rank of flip-flops to be used in a shift register with shifting possible in both directions. An output excursion of -3/4v to -12v with 20 ma drive provided in both directions eliminates the need for an external buffer driver to operate a resistor matrix load. A 10v, 15 ma lamp in an external display may also be operated from a lamp driver output. The circuit also lends itself to operation as a toggle flip-flop.

Flip-flop operation is as follows. The bistable circuit is composed of transistors Q01A, C and Q02A, C. Q01A, C provide drive in the positive direction. Q02A, C provide drive in the negative direction. R04A, C provide direct coupling between the two basic inverters to maintain either of two stable states. Q03 acts as an emitter follower to operate a low wattage lamp such as the #344 (10v, 15 ma). The positive excursion of the output is determined by the saturation resistance of Q01A, C and CR06A, C. The negative excursion is determined by the voltage on pin 4 which limits the negative-going excursions at the base of Q02A, C. When the output is negative, the output current is limited by R07A, C in the collector of Q02A, C. CR06A, C provide turnoff voltage bias for Q02A, C respectively when Q01A, C are turned on.

Triggering of the flip-flop is as follows. Assume Q01C is conducting (Q02A conducting and Q02C and Q01A nonconducting). If pin 7 is driven within -1/4 to -1v of ground, then a positive-going excursion of about 10v on pin 3 would cause a positive pulse to be coupled through C01C and CR07C to the base of Q01C. This positive signal would overcome the negative voltage supplied by R04C and cause Q01C to turn off. In about 0.1 usec after Q01C turns off, Q01A will be turned on and have changed the flip-flop to its other stable state. Q01C could also have been turned off in a similar manner by having pin 8 near ground and applying a positive-going excursion to pin 5 through C02C and CR08C. When Q01A is on, it may be turned off to change the flip-flop state by a similar combination of signals on pins 1 and 3 or pins 2 and 5. Input signals on pins 1, 2, 7, and 8 should be equivalent in excursion to the output of pins 6 and 12 of the card.

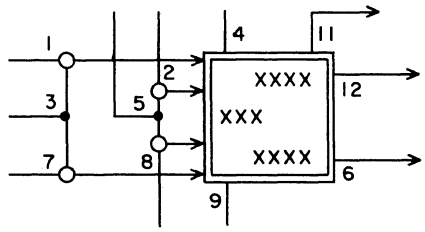
Thus, a positive-going pulse on pin 3 makes the flip-flop assume a state dependent on the levels present on pins 1 and 7 (assuming they are complimentary). Similiarly, a positive-going pulse on pin 5 makes the flip-flop assume a state dependent on the levels present on pins 2 and 8. By interconnecting the cards logically, they can be wired to shift up or down in a shift register by using one of two shift pulse lines from circuits such as the AIA which can interface with standard logic.

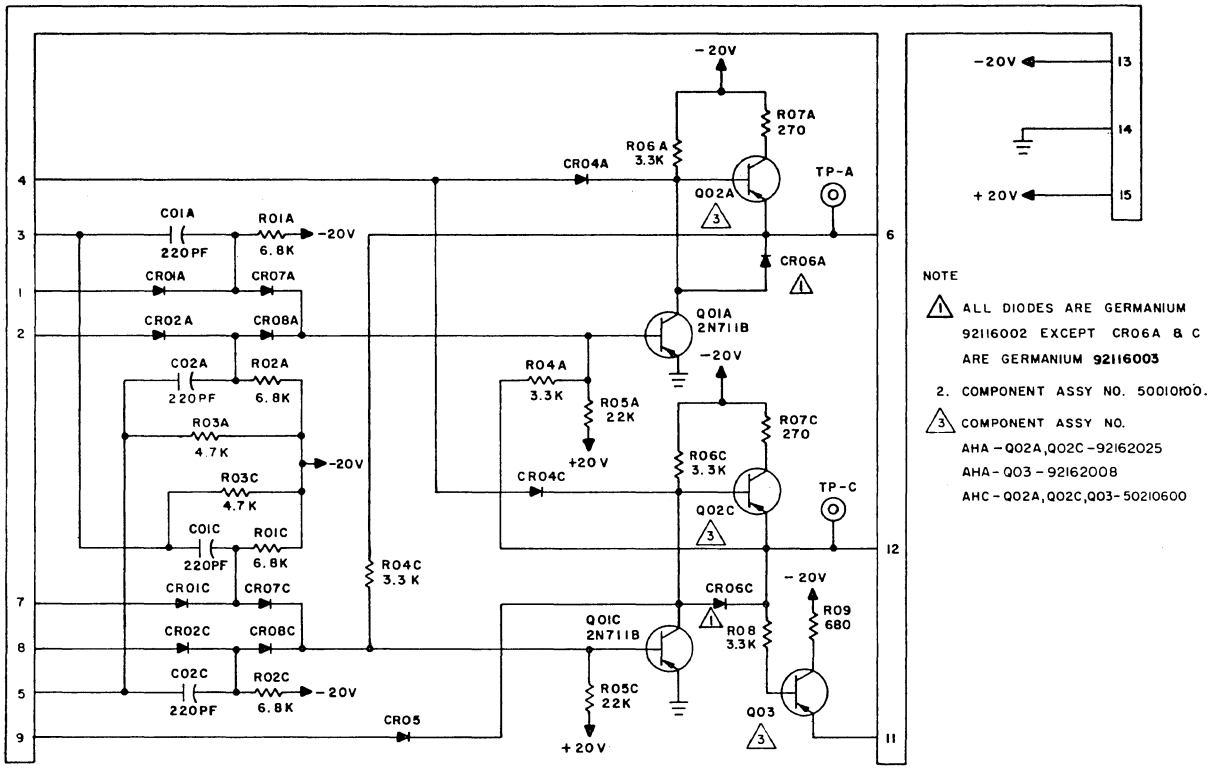
For clearing a counter or shift register, a clear line on pin 9 may be used. This operates from a signal from 0 to -1v and large numbers of AHA's may be cleared by one high current driver. Each card may require 7-25 ma (depends on load) to clear when in the set condition (lamp driver on) or 3 ma when in the clear position. The clear line should be biased between -12v and -20v when a clear is not desired.

While the circuit is specifically designed for an excursion of -1/2v to -12v, clamping pin 4 to a different voltage will change the negative excursion proportionally. Lower voltages significantly reduce output drive in the positive direction and more negative voltages reduce it in the negative direction. The lamp driver circuit of Q03 is also significantly affected by such a change.

Shift pulses should have positive-going rise times of 0.150 usec or less with an excursion of 10 to 12 volts. Larger excursions with rise times this fast can cause faulty operation as can low amplitude slow rise time pulses.

SYMBOL

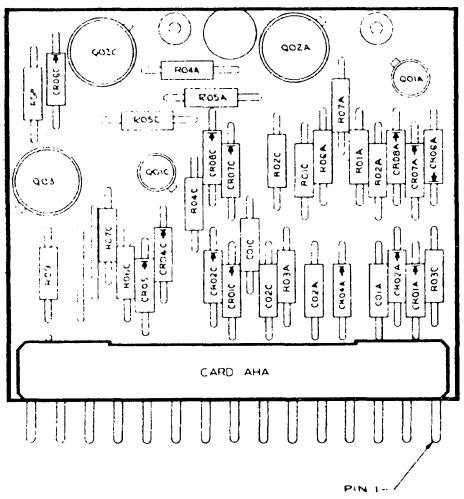





NOTE

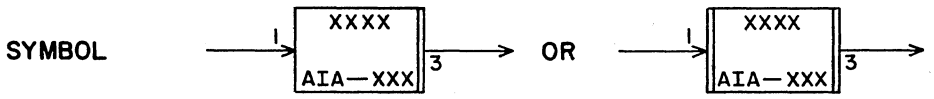
1. ALL DIODES ARE GERMANIUM 92116002 EXCEPT CR06A & C ARE GERMANIUM **92116003**
2. COMPONENT ASSY NO. 50010100.
3. COMPONENT ASSY NO.
   AHA - Q02A, Q02C - 92162025
   AHA - Q03 - 92162008
   AHC - Q02A, Q02C, Q03 - 50210600

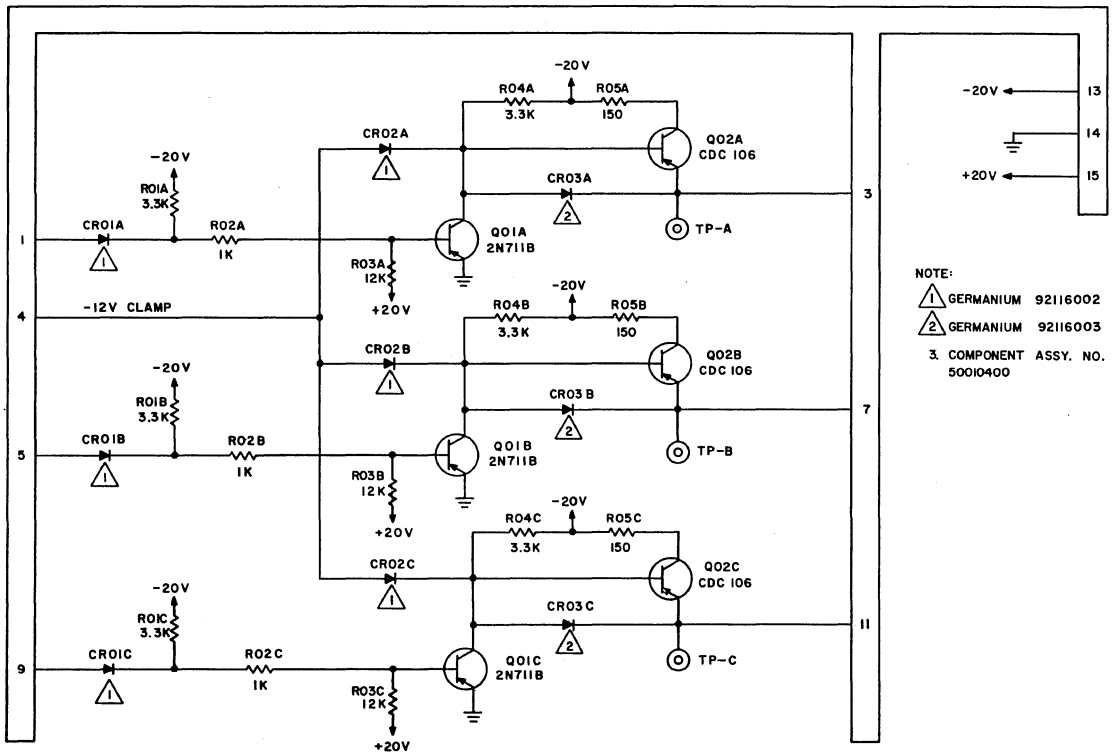
AHA, AHC

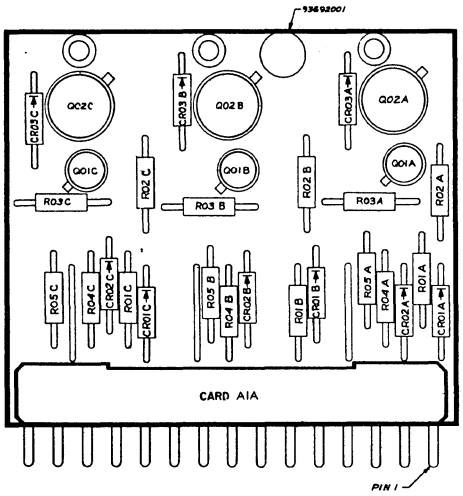


SHIFT DRIVER
AIA, AIB

The shift driver is designed to supply shift pulses and input signals for the AHA and similar circuit requirements. It provides output drive in both the positive and negative direction similar to a 3600 inverter. The output excursion is determined by the clamp voltage on pin 4 which is designed for -12v. Its input may operate from either standard 1604 logic levels or from logic levels that have greater negative excursions. However, if the negative excursion of the input is less than -5.0v, the output drive in the positive direction is reduced from a normal 70 ma to 25 ma at normal 1604 logic inputs. For positive input excursions ranging from 0 to -3/4v, the output drive in the negative direction is 45 ma maximum using a -12v clamp on pin 4. Output drive in the negative direction also reduces proportionably as the difference between -20v and the clamp voltage is reduced. Conversely, it increases if a lower clamp voltage is used. The negative voltage excursion for various loads is within 0.5v of the negative clamp voltage on pin 4. The positive excursion ranges from -0.5v at light load to a maximum of -1.0v at full load.




-20V
R04A
3.3K
R05A
150
CR02A
Q02A
CDC 106
CR03A
TP-A
R01A
3.3K
CR01A
R02A
1K
Q01A
2N711B
R03A
12K
+20V
-12V CLAMP
R04B
3.3K
R05B
150
CR02B
Q02B
CDC 106
CR03B
TP-B
R01B
3.3K
CR01B
R02B
1K
Q01B
2N711B
R03B
12K
+20V
R04C
3.3K
R05C
150
CR02C
Q02C
CDC 106
CR03C
TP-C
R01C
3.3K
CR01C
R02C
1K
Q01C
2N711B
R03C
12K
+20V
-20V
13
14
15
3
7
11
1
4
5
9
NOTE:
1 GERMANIUM 92116002
2 GERMANIUM 92116003
3. COMPONENT ASSY. NO. 50010400


93692001
Q02C
Q02B
Q02A
Q01C
Q01B
Q01A
CR03C
CR03B
CR03A
R03C
R02C
R03B
R02B
R03A
R02A
R05C
R04C
CR02C
R01C
CR01C
R05B
R04B
CR02B
R01B
CR01B
R05A
R04A
CR02A
R01A
CR01A
CARD A1A
PIN 1

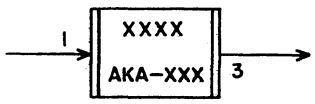
# PHOTOCELL AMPLIFIER
## AKA

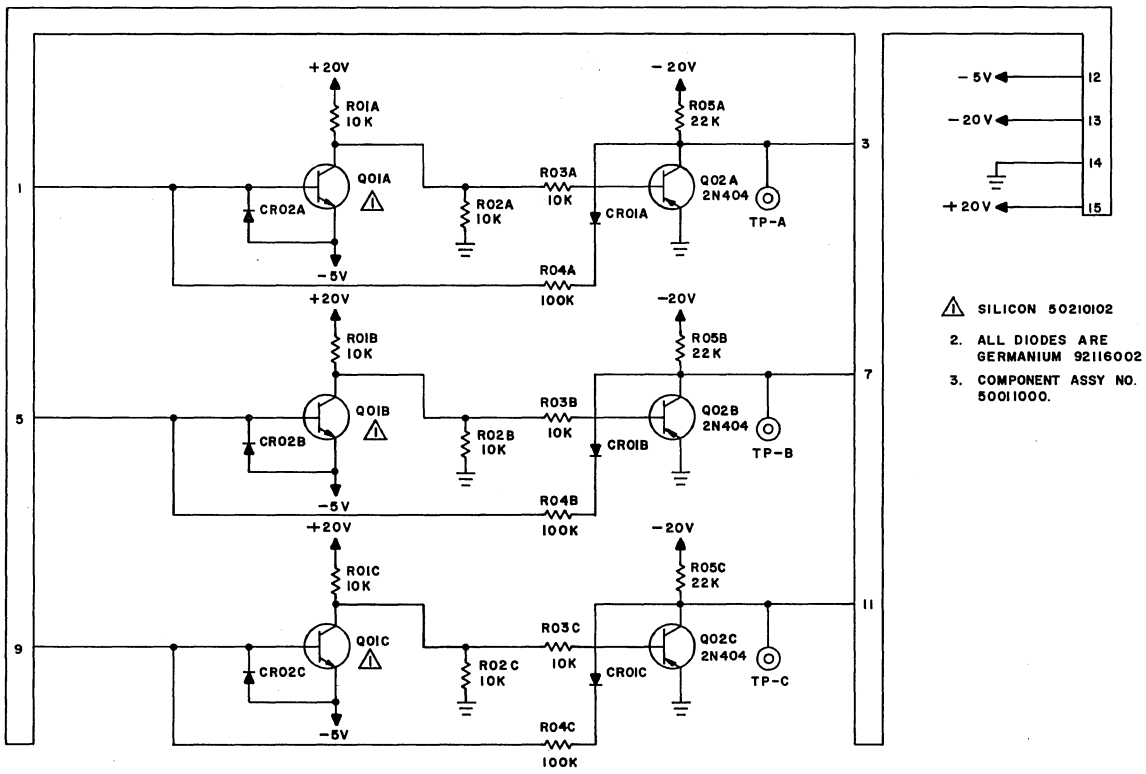
The AKA Photocell Amplifier is designed for use on the 350 and 370 Paper Tape Readers to digitize photo diode or photo transistor signals.

The output of the amplifier is normally terminated by the input of a standard "M" card, such as the 87. In the dark condition, external bias potentiometers supply current from a negative source to the input diode keeping both stages turned off, resulting in an output of -16v dc. In the illuminated state, the photocell provides positive current to the input base over-riding the bias current to turn on both stages. This results in an output of 0 to -1v dc.

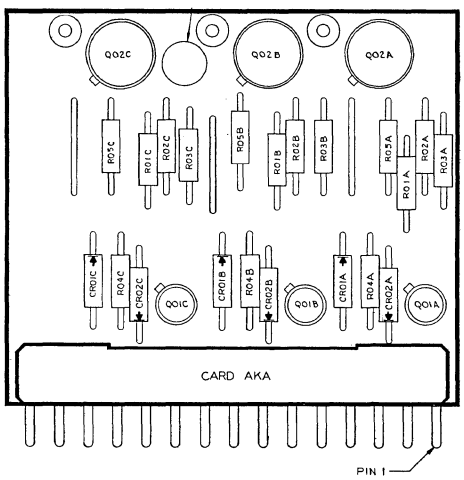
The circuit consists of two direct coupled inverting stages and a feedback circuit. The positive feedback through CR01 and R07 from output to input provides hysteresis or "snap action" to the turn-on and turn-off process. This insures the absence of Class A signals on the output during those times when the photocell is left in a partially illuminated state. Diode CR07 is intended to prevent a reverse feedback current from flowing when the photo diode is dark. Internal leakage in CR07 does allow a slight amount of positive feedback when connected to a "M" card, but this would be reduced even further if terminated by a standard inverter.

SYMBOL




+20V
R01A
10K
Q01A
CR02A
R02A
10K
R03A
10K
CR01A
-20V
R05A
22K
Q02A
2N404
TP-A
-5V
R04A
100K
+20V
R01B
10K
Q01B
CR02B
R02B
10K
R03B
10K
CR01B
-20V
R05B
22K
Q02B
2N404
TP-B
-5V
R04B
100K
+20V
R01C
10K
Q01C
CR02C
R02C
10K
R03C
10K
CR01C
-20V
R05C
22K
Q02C
2N404
TP-C
-5V
R04C
100K
1
3
5
7
9
11
-5V
12
-20V
13
14
+20V
15
SILICON 50210102
2. ALL DIODES ARE GERMANIUM 92116002
3. COMPONENT ASSY NO. 50011000.

AKA


Q02C
Q02B
Q02A
R05C
R01C
R02C
R03C
R05B
R01B
R02B
R03B
R05A
R01A
R02A
R03A
CR01C
R04C
CR02C
Q01C
CR01B
R04B
CR02B
Q01B
CR01A
R04A
CR02A
Q01A
CARD AKA
PIN 1

# POWER SUPPLY
## ALA

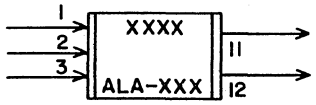
The ALA card contains a floating power supply. It is used with the FOA and FOB function generator cards in the disk file servo actuator.

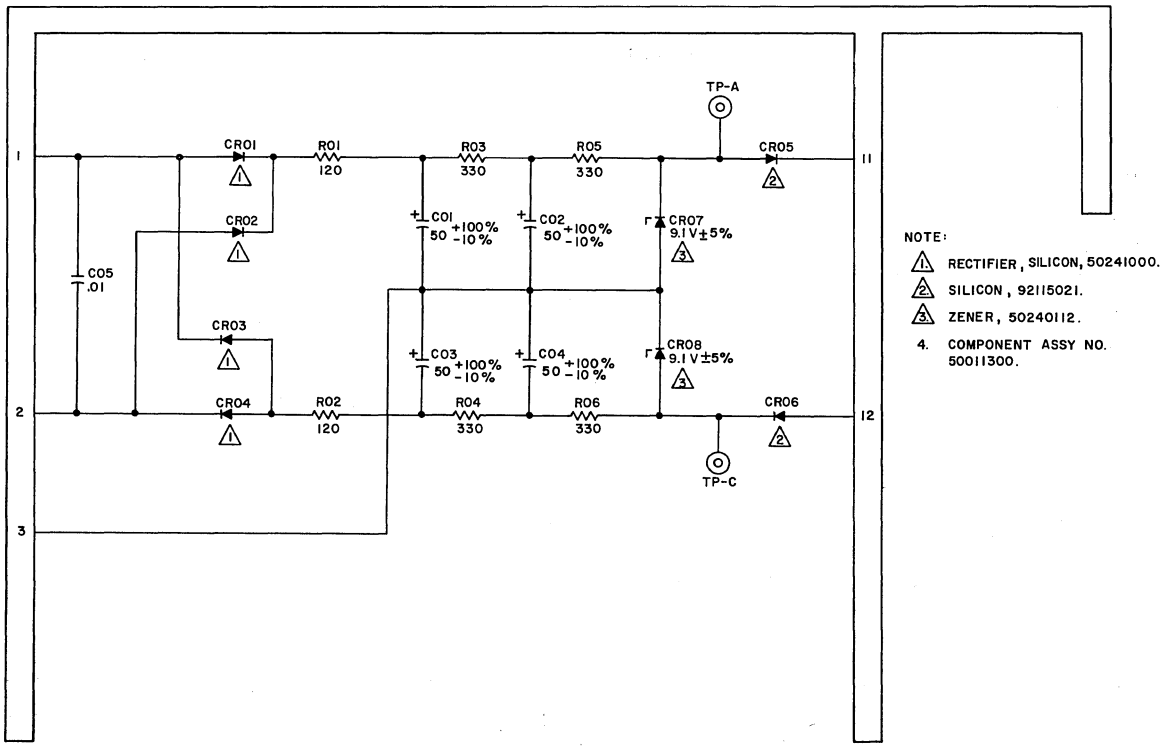
The circuit is supplied by an externally mounted 40v rms 60 cycle center tapped transformer. The transformer is connected to pins 1, 2, and 3. Pin 3 is the center tap and circuit common.

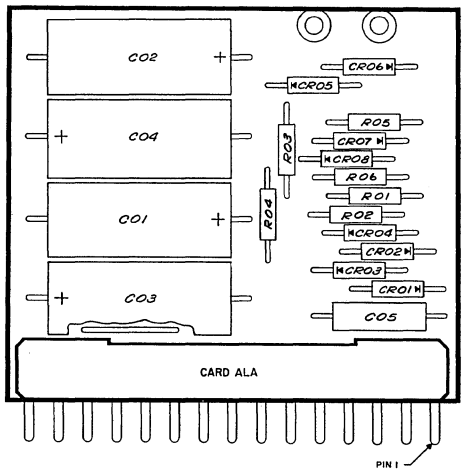
The circuit consists of two full wave rectifier circuits connected for plus and minus voltage, and the filter networks as shown on the schematic. Zener diodes CR07 and CR08 regulate the output voltages to 9.1v nominally. The maximum load is approximately 18 ma.

NOTE: This card requires two card slots.

SYMBOL




TP-A
CR01
R01
120
R03
330
R05
330
CR05
1
11
CR02
C01
50 +100% -10%
C02
50 +100% -10%
CR07
9.1V±5%
C05
.01
CR03
C03
50 +100% -10%
C04
50 +100% -10%
CR08
9.1V±5%
2
12
CR04
R02
120
R04
330
R06
330
CR06
TP-C
3
NOTE:
1. RECTIFIER, SILICON, 50241000.
2. SILICON, 92115021.
3. ZENER, 50240112.
4. COMPONENT ASSY NO. 50011300.


C02
C04
C01
C03
CR06 M
MCR05
R05
CR07 M
MCR08
R06
R01
R02
MCR04
CR02 M
MCR03
CR01 M
C05
R03
R04
CARD ALA
PIN 1

# WRITE/ERASE DRIVERS

## AMF THRU AMQ

The AM-- series cards are used as high speed current switches to control the current to the write or erase heads. The magnitude of the current is determined by the collector resistors of Q03A and Q03C and the emitter resistors external to the card. Except for the variation in collector- and emitter-resistor values according to the current requirements of a particular head, all AM-- series cards are similar. These cards are intended to be driven by toggle flip-flops such as the EVB or the UKB.

| CARD | TYPICAL CURRENT AT EACH OUTPUT |
|---|---|
| AMF | 100 ma |
| AMG, AMM | 125 ma |
| AMH, AMN | 125 ma |
| AMI | 300 ma |
| AMJ, AMO | 85 ma |
| AMK, AMP | 100 ma |
| AML, AMQ | 60 ma |

When transistor Q01 is on, it holds transistors Q02 and Q03 off. Zener diode CR01 is used for level translation. Diode CR03 keeps noise at the input from coupling through the capacitance of CR01 to the base of Q01. Diode CR04 is an anti-saturation diode. Resistor R06 develops a voltage drop proportional to the drive current which is used to check for proper operation (see cards ANB, ANC, AND, and AOA). Diodes CR05 and CR07 are part of the checking circuitry. Diode CR02 allows Q01 to provide turn-off current directly to Q03.

Except for the AMG, AMJ (15 uf), the AML (10 uf), and the AMM thru AMQ (.01 uf), the value of capacitor C02 is 4.7 uf. This provides a longer time constant to ensure correct operation of the error checking circuits in the Disk Storage Drives.

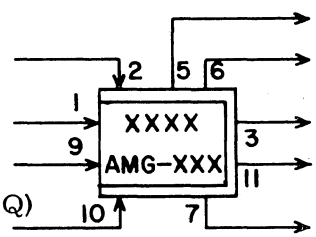
The AMI card is designed to operate at +20v rather than +40v in order to reduce power dissipation. This was necessary because both circuits on the card are on at the same time.

With "1" (-3v) at the input, transistors Q02 and Q03 permit the current to flow from +40v (+20v, AMI card) toward ground. With "0" (ground) in, the output is open. The magnitude of the current is determined by an external resistor in series with the load.

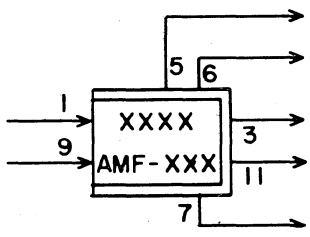
CAUTION

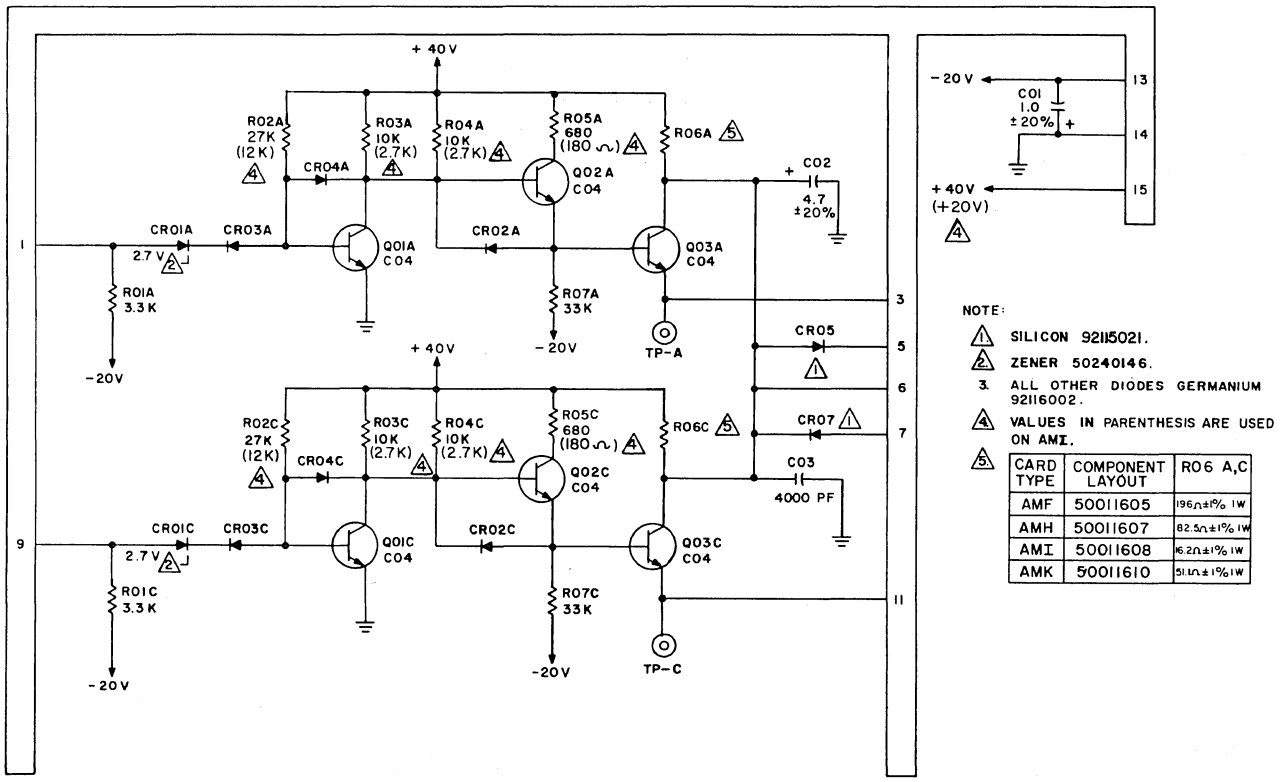
These cards should not be removed from the chassis while +40v is applied.

SYMBOL (AMG, J, L, M, N, O, P, Q)




SYMBOL (AMF, H, I, K)



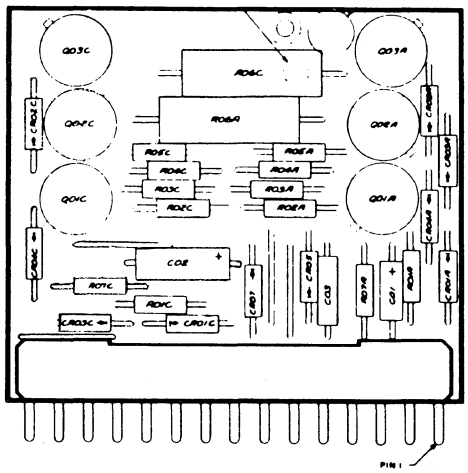


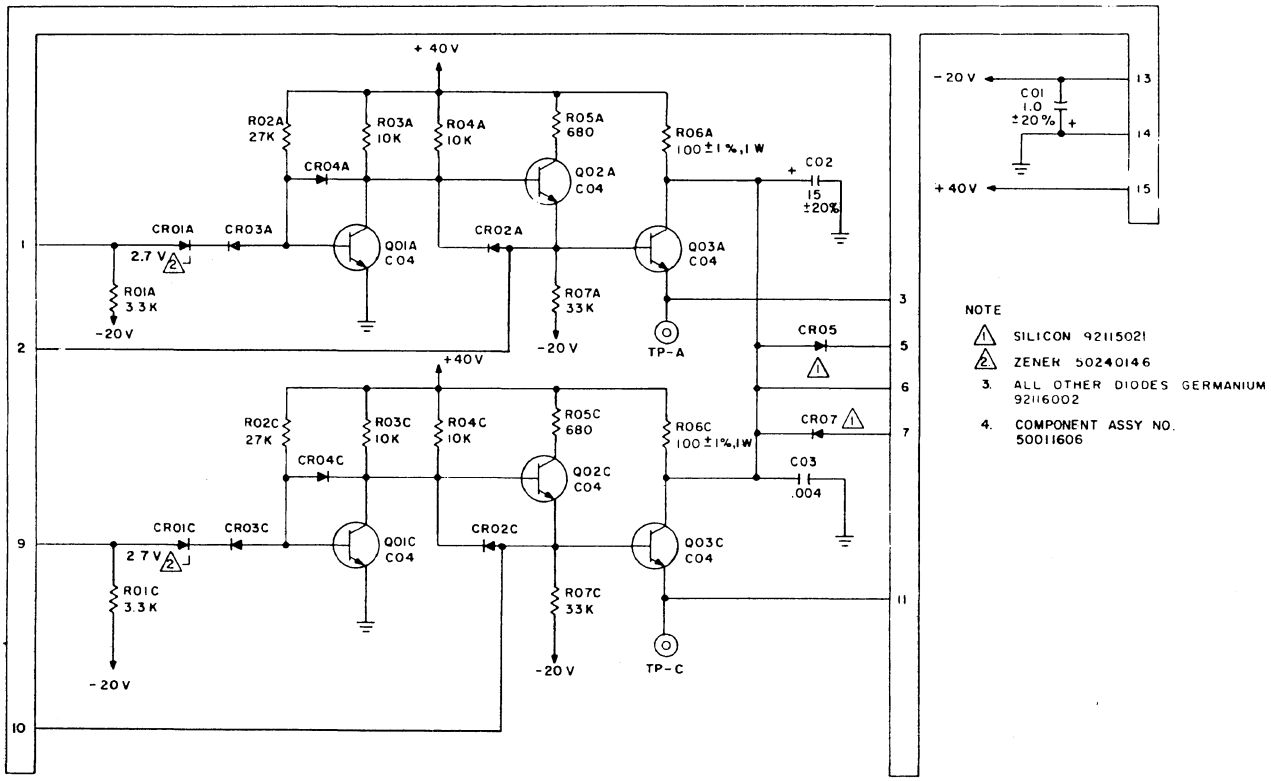

NOTE:

1. SILICON 92115021.
2. ZENER 50240146.
3. ALL OTHER DIODES GERMANIUM 92116002.
4. VALUES IN PARENTHESIS ARE USED ON AMI.
5. 

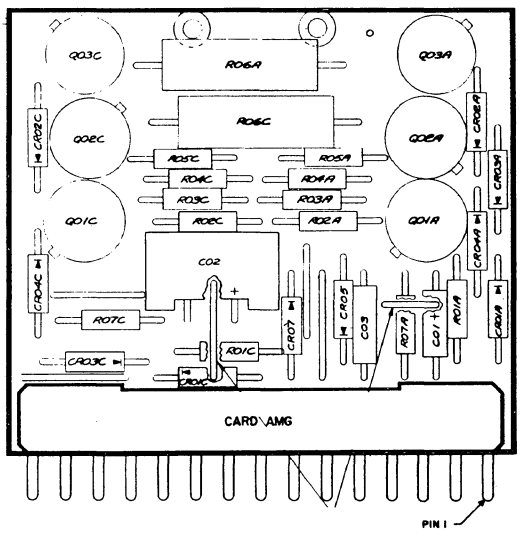
| CARD TYPE | COMPONENT LAYOUT | R06 A,C |
|---|---|---|
| AMF | 50011605 | 196Ω±1% 1W |
| AMH | 50011607 | 82.5Ω±1% 1W |
| AMI | 50011608 | 16.2Ω±1% 1W |
| AMK | 50011610 | 51.1Ω±1% 1W |

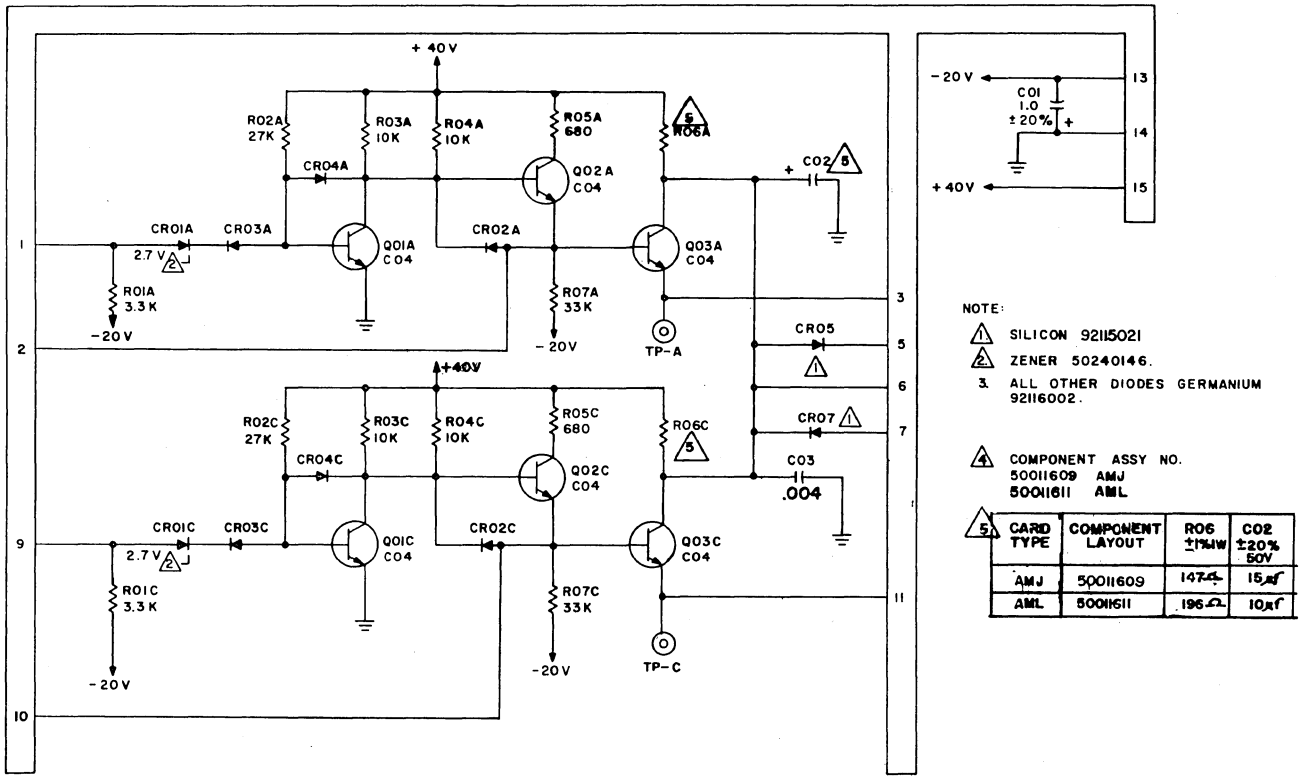
AMF, AMH, AMI, AMK




+40V
R02A 27K
R03A 10K
R04A 10K
R05A 680
R06A 100±1%,1W
CR04A
Q02A C04
C02 15 ±20%
CR01A
CR03A
CR02A
Q01A C04
Q03A C04
2.7V
R01A 3.3K
-20V
R07A 33K
TP-A
CR05
CR07
R02C 27K
R03C 10K
R04C 10K
R05C 680
R06C 100±1%,1W
CR04C
Q02C C04
C03 .004
CR01C
CR03C
CR02C
Q01C C04
Q03C C04
R01C 3.3K
R07C 33K
TP-C
-20V
+40V
C01 1.0 ±20%
1
2
3
5
6
7
9
10
11
13
14
15
NOTE
1. SILICON 92115021
2. ZENER 50240146
3. ALL OTHER DIODES GERMANIUM 92116002
4. COMPONENT ASSY NO. 50011606

AMG


Q03C
R06A
Q03A
CR02C
Q02C
R05C
R05A
Q02A
CR02A
CR05A
R04C
R04A
R03C
R03A
Q01C
R02C
R02A
Q01A
CR01A
C02
CR04C
CR05
C03
R07A
R01A
CR07
CR03C
R07C
R01C
CR01C
CARD\AMG
PIN 1

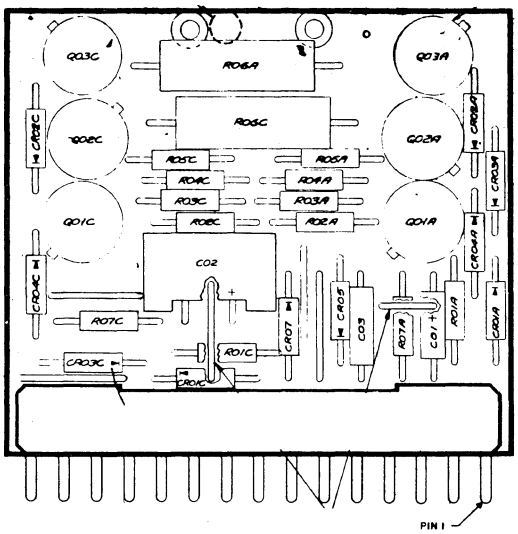


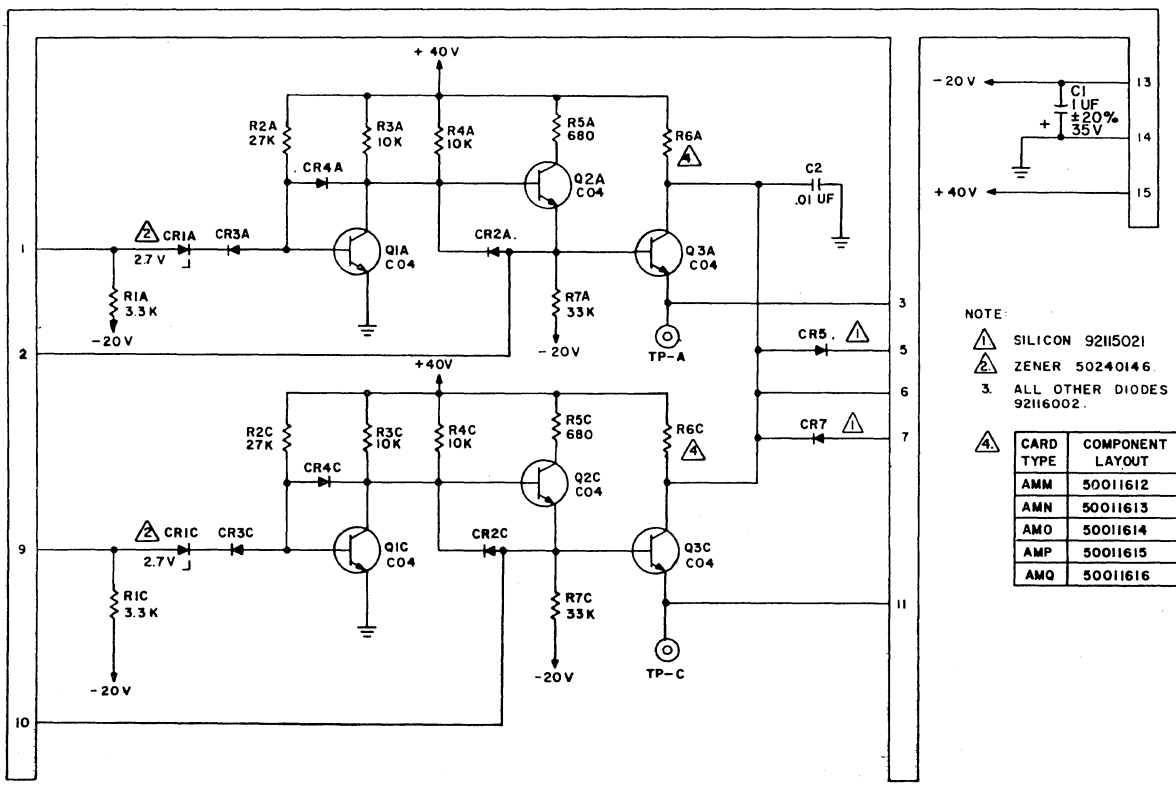

NOTE:

1. SILICON 92115021
2. ZENER 50240146.
3. ALL OTHER DIODES GERMANIUM 92116002.
4. COMPONENT ASSY NO.
   50011609 AMJ
   50011611 AML
5.

| CARD TYPE | COMPONENT LAYOUT | R06 ±1%1W | C02 ±20% 50V |
|---|---|---|---|
| AMJ | 50011609 | 147Ω | 15µf |
| AML | 50011611 | 196Ω | 10µf |

AMJ, AML



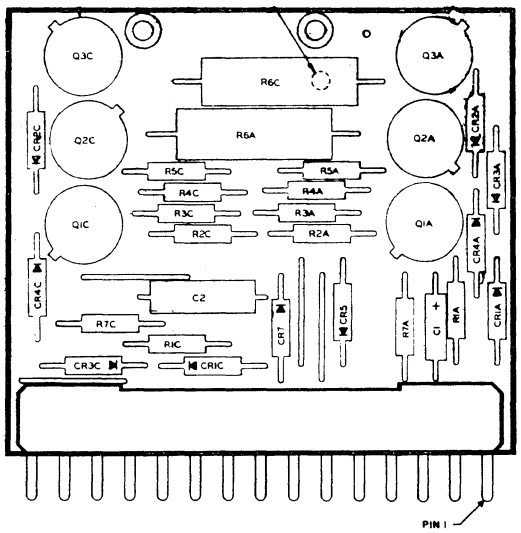



NOTE:

1. SILICON 92115021
2. ZENER 50240146
3. ALL OTHER DIODES GERMANIUM 92116002.
4. 

| CARD TYPE | COMPONENT LAYOUT | R6 ±1% 1W |
|---|---|---|
| AMM | 50011612 | 100 |
| AMN | 50011613 | 82.5 |
| AMO | 50011614 | 147 |
| AMP | 50011615 | 51.1 |
| AMQ | 50011616 | 196 |

AMM, AMN, AMO, AMP, AMQ



HEAD SELECT AND WRITE ERROR CHECKER
AND

This card is used in conjunction with write driver cards AMF and AMG, and head selector card IOB to check for proper operation.

(A) R05, CR07, CR09, and Q02 are used to determine if more than one head select circuit is on. Pins 5 and 11 of all the IOB cards are tied to pin 7. Each transistor Q03 on the IOB cards which is turned on (in saturation), draws approximately 4 ma through R05. When the voltage drop across R05 is greater than 1.6v ($\pm$0.15v), which is the sum of the voltage drops across CR07 and CR09 in series plus $V_{be}$ of Q02, transistor Q02 will turn on. This will turn off transistor Q04. When Q04 goes off, an error has been detected. Resistor R05 is used so if one IOB card is on, Q02 will stay off. However, if two IOB cards are on, Q02 will turn on.

(B) R13, R14, CR08, and Q05 are used to determine if the current flowing out of each of a group of drivers is approximately the same. This will assure that none of them have shorts or opens. Pin 7 on both AMF or AMG cards are tied to pin 8. Pin 5 on both AMF or AMG cards are tied to pin 9. Since R06A and R06C are in parallel on the AMF or AMG card, the voltage across them is a function of the total current flowing through Q03A and Q03C. Capacitor C02 integrates this voltage. Therefore, it doesn't fluctuate with individual write cycles.

Assume that Q03A on driver number 1 becomes shorted. The current will then flow through Q03A all of the time, as well as part of the time through Q03C as dictated by input logic. The voltage at pin 6 of driver number 1 will then be more negative than the voltage at pin 6 of driver number 2. This will pull the voltage at pin 8 of the AND card more negative through CR07 on driver number 1. The voltage at the base of Q05 on card AND will stay one diode drop more negative than at pin 8. If the base of Q05 gets approximately 1.5v negative, with respect to pin 6 of driver number 2, Q05 will be turned on via CR05 on driver number 2. When Q05 turns on, Q04 turns off and an error is indicated. However, if the voltage at the collector of Q03 on driver number 1 is close enough to the voltage at collector Q03 on driver number 2, Q05 will not turn on. If these voltages are called $V_1$ and $V_2$, Q05 will turn on if the absolute

value of $V_1$ minus $V_2$ is greater than 1.77 volts. Transistor Q05 will not turn on if the absolute value of $V_1$ minus $V_2$ is less than 1.27 volts.

## HEAD SELECT AND WRITE ERROR CHECKER
## ANB

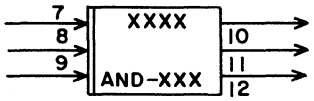
The (B) portion of the AND card description applies to card ANB. The circuits containing Q01 and CR14 are used in conjunction with card AOA to test head selects. If more than approximately 0.8 ma flows from a combination of AOA cards into pin 1, Q01 will turn off indicating an error. R15 and CR14 act as a reference voltage supply for the AOA cards.

## ERASE ERROR CHECKER
## ANC

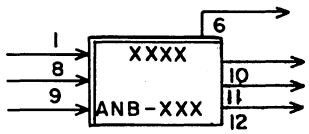
The ANC card is essentially the same as the (B) portion of the AND card description. The ANC card has been modified to test drivers that operate on +20v (AMI card) rather than +40v.

The outputs of cards ANB, ANC, and AND go to logical "1" (-3v) if an error has been detected. If the outputs are at logical "0" (ground), no error has been detected.

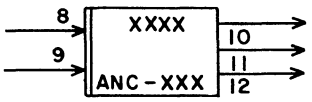
SYMBOL

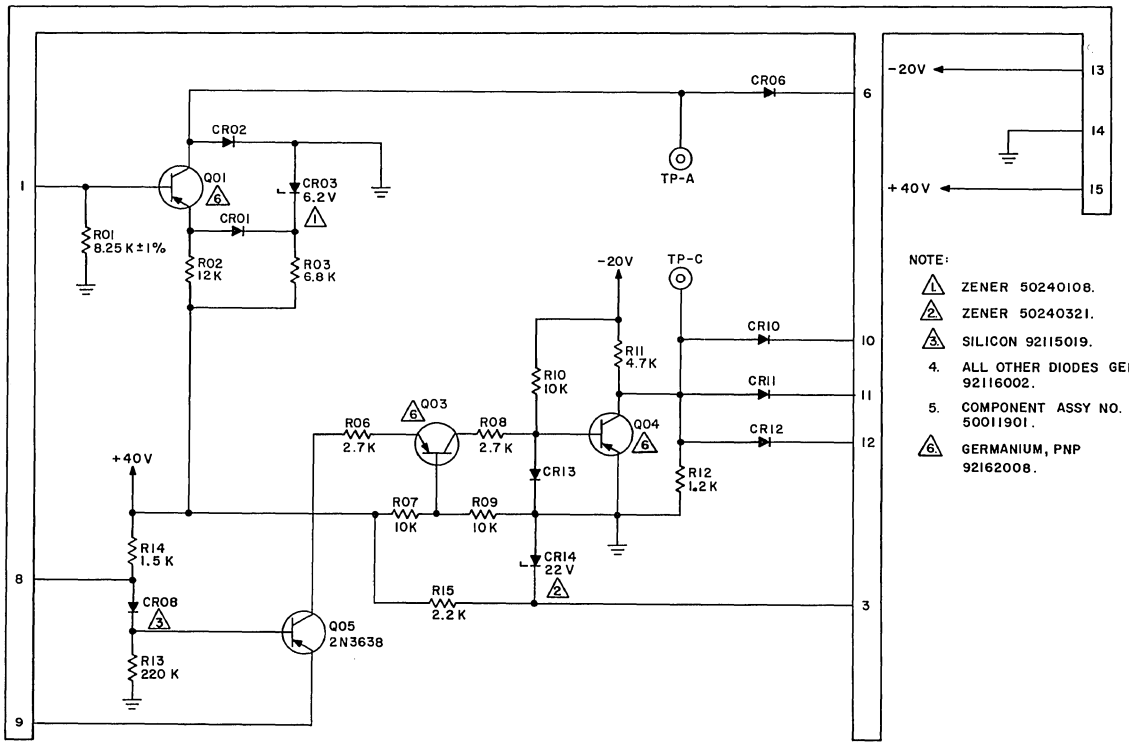



SYMBOL




SYMBOL

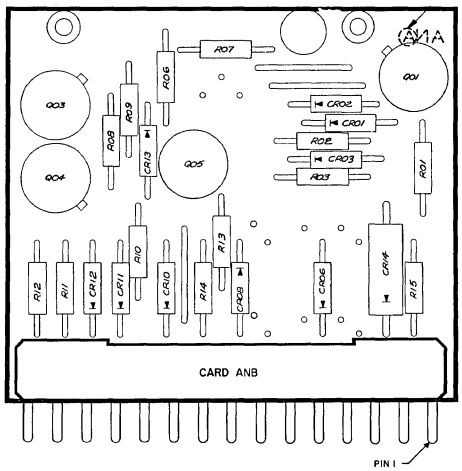


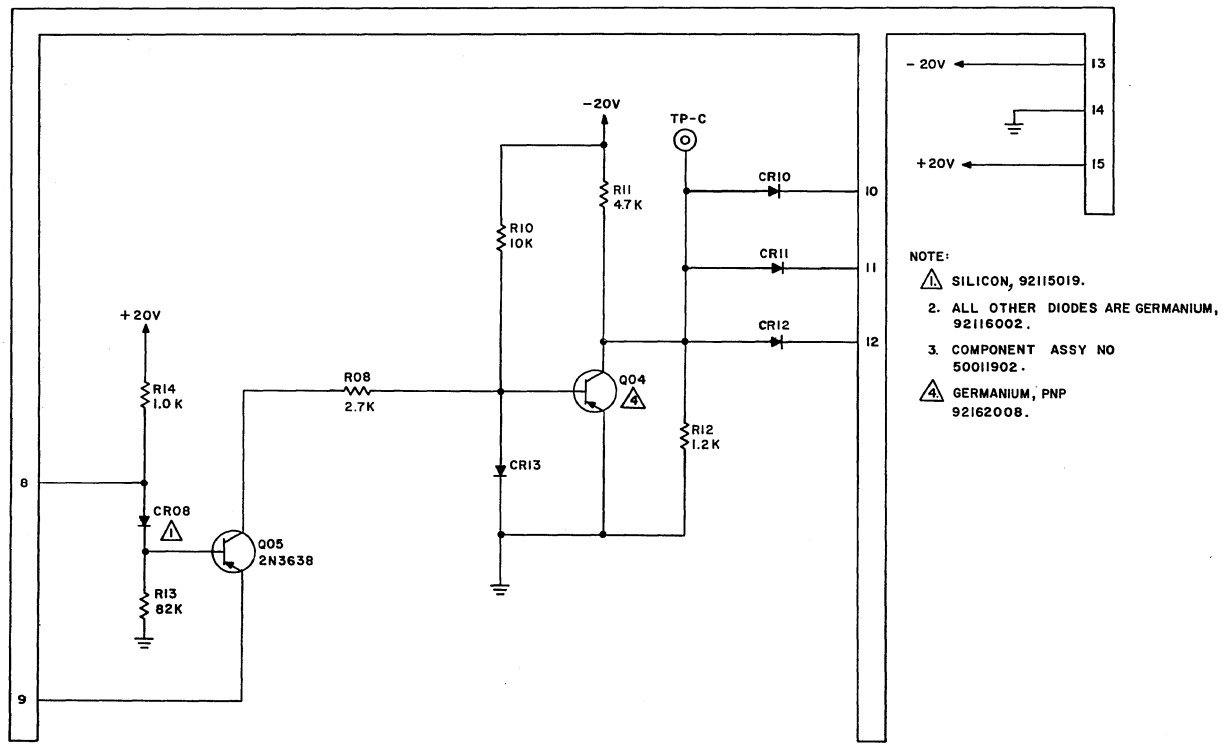



NOTE:

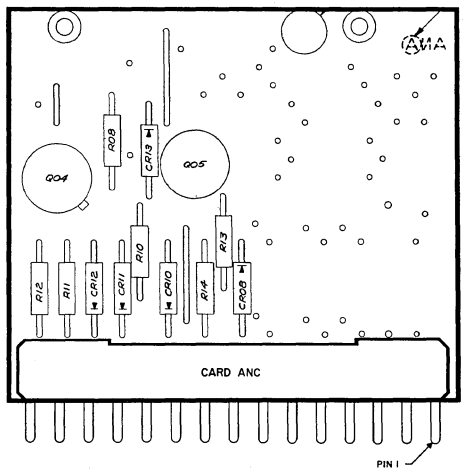
1. ZENER 50240108.
2. ZENER 50240321.
3. SILICON 92115019.
4. ALL OTHER DIODES GERMANIUM 92116002.
5. COMPONENT ASSY NO. 50011901.
6. GERMANIUM, PNP 92162008.

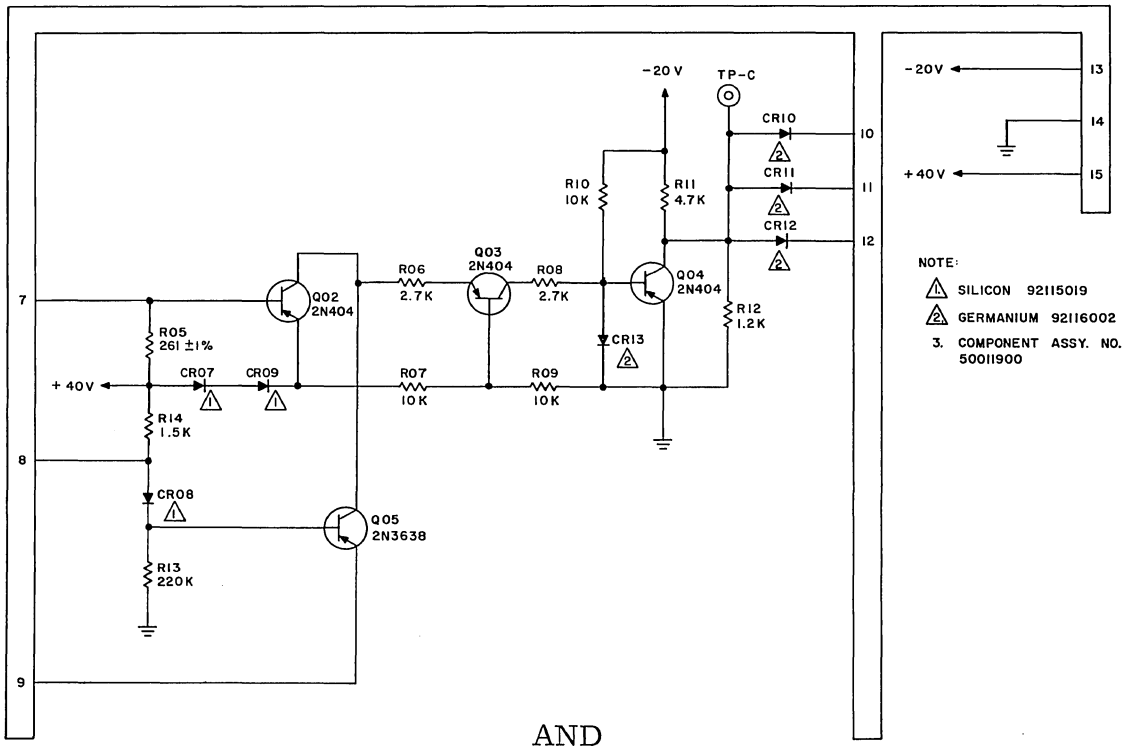
ANB



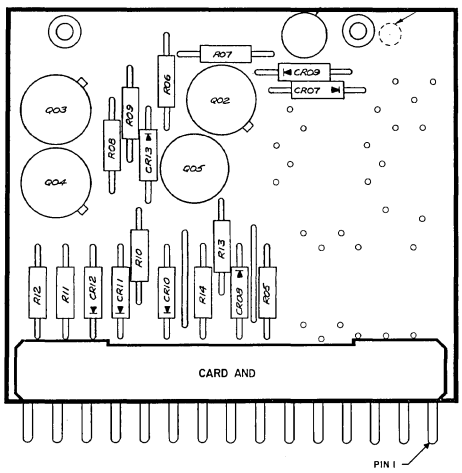

-20V
TP-C
+20V
R14
1.0K
R08
2.7K
R10
10K
R11
4.7K
R12
1.2K
R13
82K
CR08
CR10
CR11
CR12
CR13
Q04
Q05
2N3638
8
9
10
11
12
13
14
15
-20V
+20V
NOTE:
1. SILICON, 92115019.
2. ALL OTHER DIODES ARE GERMANIUM, 92116002.
3. COMPONENT ASSY NO 50011902.
4. GERMANIUM, PNP 92162008.

ANC


AMA
Q04
Q05
R08
CR13
R10
R13
R12
R11
CR12
CR11
CR10
R14
CR08
CARD ANC
PIN 1


-20V
TP-C
CR10
CR11
CR12
R10
10K
R11
4.7K
Q03
2N404
R06
2.7K
R08
2.7K
Q04
2N404
R12
1.2K
CR13
Q02
2N404
R05
261 ±1%
CR07
CR09
R07
10K
R09
10K
+40V
R14
1.5K
CR08
Q05
2N3638
R13
220K
7
8
9
10
11
12
13
14
15
-20V
+40V
NOTE:
1. SILICON 92115019
2. GERMANIUM 92116002
3. COMPONENT ASSY. NO. 50011900

AND


R07
CR09
CR07
R06
R09
Q03
Q02
R08
CR13
Q05
Q04
R12
R11
CR12
CR11
R10
CR10
R14
CR08
R13
R05
CARD AND
PIN 1

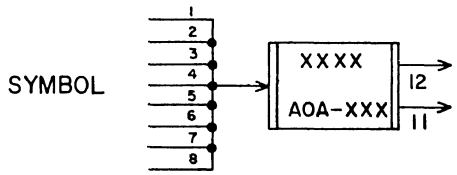
EXCLUSIVE OR CIRCUIT

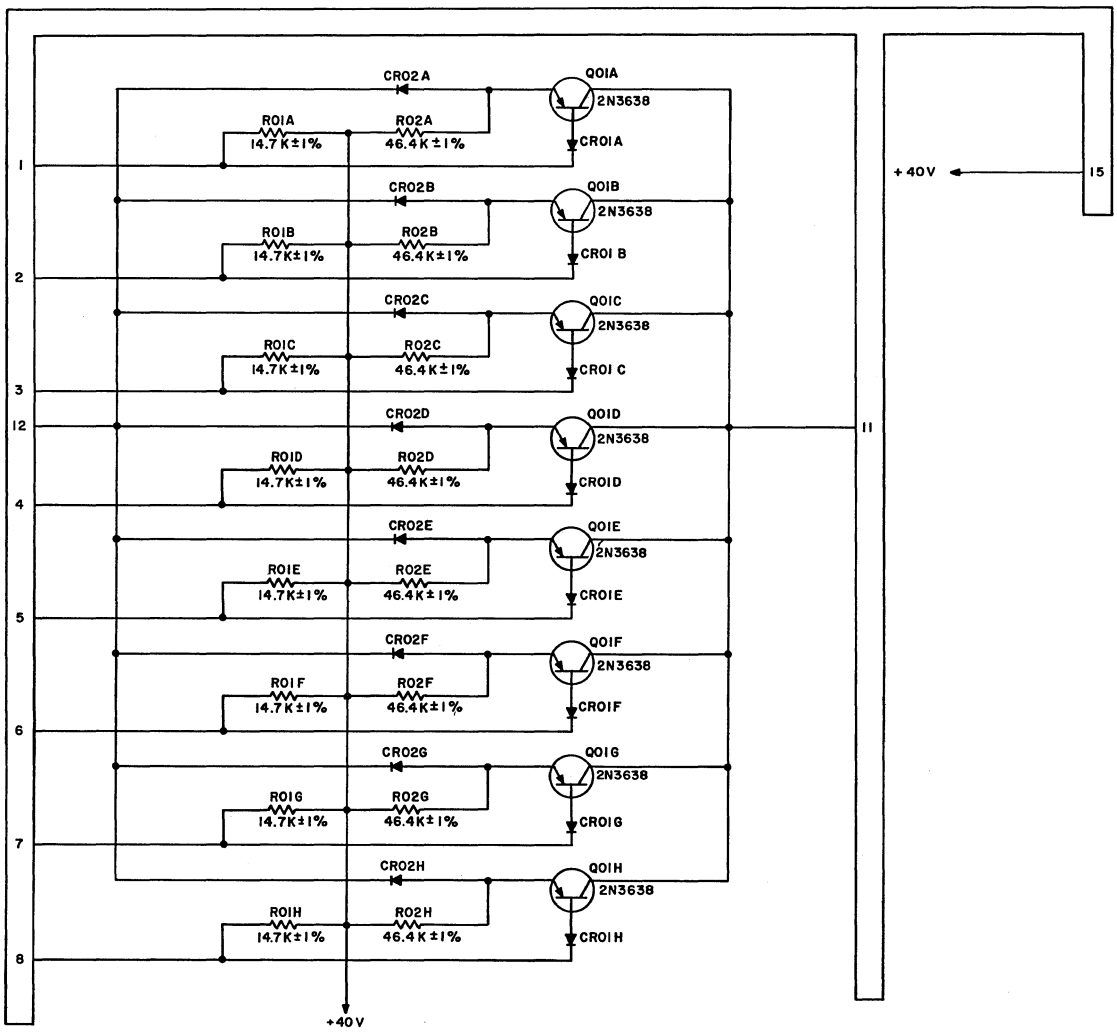
AOA

The AOA card delivers +0.4 ma to an ANB card for each head select circuit (turned on) it is monitoring.

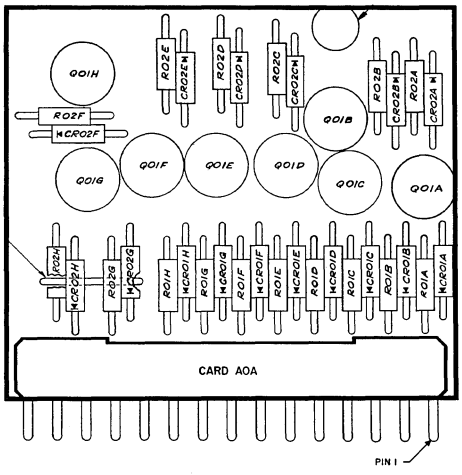
Pins 5 and 11 on the IOB cards are tied to pins 1 through 8, with only one Head Select circuit at each input pin. A total of eight Head Select circuits are tested by each AOA card, in conjunction with an ANB card. If the Head Select circuit tied to pin 1 is turned on, Q01A will be turned on, and it will allow approximately 0.4 ma to flow out pin 11 to the ANB card. The voltage at pin 1 is compared to the voltage at pin 12. If the Head Select circuit tied to any other pin of pins 1 through 8 is on, the associated transistor on the AOA card will also turn on, in the same manner at Q01A. This transistor will also allow approximately 0.4 ma to flow out pin 11 to the ANB card.

Four AOA cards are used in conjunction with one ANB card. Pin 11 on the AOA card goes to pin 1 on the ANB card; pin 12 on the AOA card goes to pin 3 on the ANB card. Thus, 32 Head Select circuits are being checked by one ANB circuit. If more than one Q01 on the four AOA cards is on, there will be 0.8 ma (or more) entering the ANB card at pin 1.




CR02A
Q01A
2N3638
R01A
14.7K±1%
R02A
46.4K±1%
CR01A
CR02B
Q01B
2N3638
R01B
14.7K±1%
R02B
46.4K±1%
CR01B
CR02C
Q01C
2N3638
R01C
14.7K±1%
R02C
46.4K±1%
CR01C
CR02D
Q01D
2N3638
R01D
14.7K±1%
R02D
46.4K±1%
CR01D
CR02E
Q01E
2N3638
R01E
14.7K±1%
R02E
46.4K±1%
CR01E
CR02F
Q01F
2N3638
R01F
14.7K±1%
R02F
46.4K±1%
CR01F
CR02G
Q01G
2N3638
R01G
14.7K±1%
R02G
46.4K±1%
CR01G
CR02H
Q01H
2N3638
R01H
14.7K±1%
R02H
46.4K±1%
CR01H
+40V
+40V
15
11
1
2
3
12
4
5
6
7
8

AOA


Q01H
R02E
CR02EM
R02D
CR02DM
R02C
CR02CM
R02B
CR02BM
R02A
CR02AM
R02F
MCR02F
Q01B
Q01G
Q01F
Q01E
Q01D
Q01C
Q01A
R02H
MCR02H
R02G
MCR02G
R01H
MCR01H
R01G
MCR01G
R01F
MCR01F
R01E
MCR01E
R01D
MCR01D
R01C
MCR01C
R01B
MCR01B
R01A
MCR01A
CARD AOA
PIN 1

# GATED AMPLIFIER
## ATA, ATB

This circuit has a read gate and a linear preamplifier. The read gate is comprised of diodes CR01-CR10, and resistors R01-R04 and R20. Pins 1 and 4 go through an external diode on each side, pointing the same way as CR01-02 and then to the outer terminals of the read head. CR05 and CR06 are replaced by jumpers for use with disc paks.

If pins 5 and 6 are at +5V or more positive, the circuit amplifies a signal put in on pins 1 and 4 from a center-tapped, grounded read head. If pins 5 and 6 are near ground, signals at pins 1 and 4 are ignored.

Pins 5 and 6 are connected through a balancing potentiometer to an ISC card, which is used as the gate control. When the ISC input is at ground, the emitter follower output of the ISC is off, which is equivalent to having pins 5 and 6 floating. Under these conditions, whether the center-tap of the head is at +40v (unselected) or at ground (selected), diodes CR01-CR08 are not conducting, and thus represent a large impedance between the read head and the amplifier. Also, CR09 and CR10 are conducting through R03, R04, and R20, and represent a short circuit across the input to the amplifier for any signal that might leak through the other diodes. While writing is in progress, the outside terminals of the head will experience $\pm$ 20v excursions due to $L \frac{di}{dt}$. The gate portion of the circuit attenuates these voltages, so that resulting disturbances in the read chain are minimized.

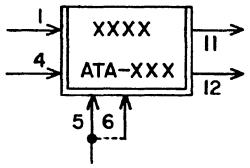
When the ISC turns on, current flows through CR01, CR02, and the two external diodes through the read head to ground via the Head Select. Current also flows through CR03-08 to R03, R04, and R20. Thus CR01-CR08 are foward biased and present a low dynamic impedance to the signal. When CR03-08 are on, CR09 and CR10 are turned off, and thus do not put a short circuit across the input to the amplifier.

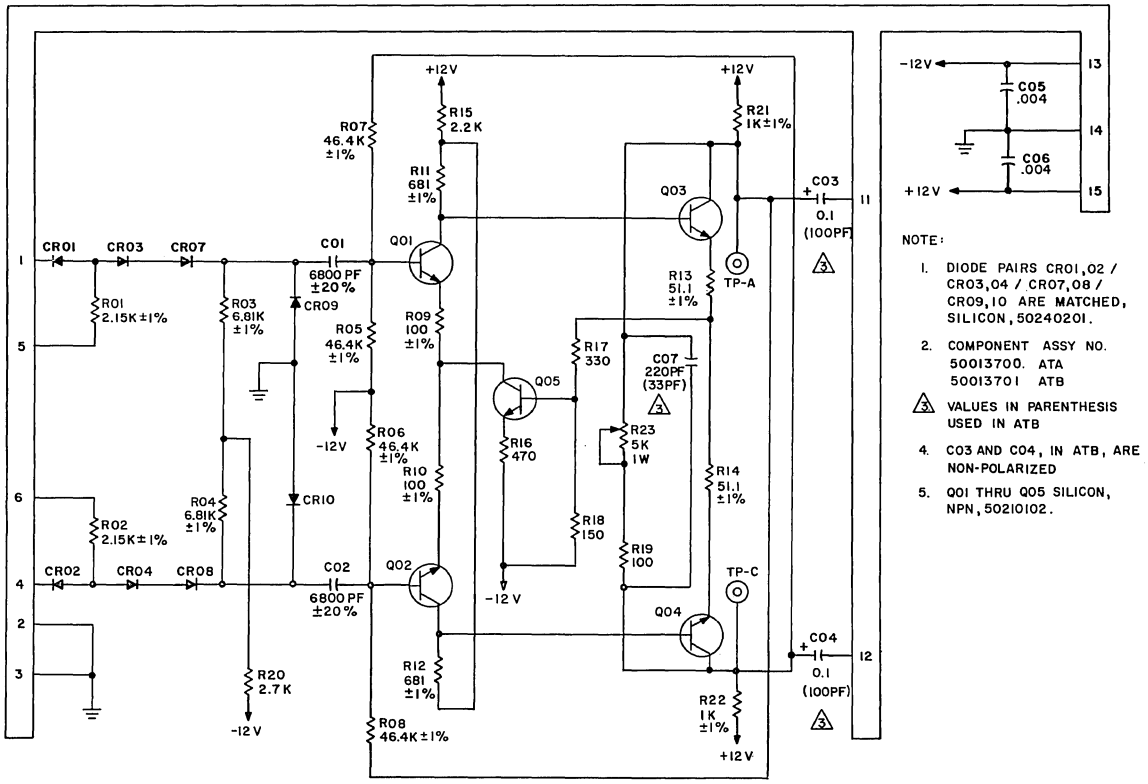
The amplifier is a two stage differential amplifier, with some dc feedback from output to input for stabilization through R07 and R08. C07 controls the high-frequency gain, and R23 controls the overall gain. +12v must be supplied at pin 15, and -12v must be supplied at pin 13. Bandpass is from 10Kc to 5Mc. This card is designed to drive EUA, EUC,

or a similar load of about 1K.

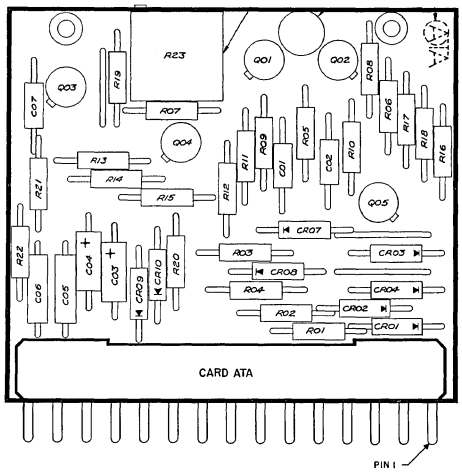
The ATB card is the same as the ATA, except that some component values are changed since the desired gain vs. frequency characteristics are different. Band pass is from 50 Kc to 5Mc.

SYMBOL




+12V
-12V
R01 2.15K ±1%
R02 2.15K ±1%
R03 6.81K ±1%
R04 6.81K ±1%
R05 46.4K ±1%
R06 46.4K ±1%
R07 46.4K ±1%
R08 46.4K ±1%
R09 100 ±1%
R10 100 ±1%
R11 681 ±1%
R12 681 ±1%
R13 51.1 ±1%
R14 51.1 ±1%
R15 2.2K
R16 470
R17 330
R18 150
R19 100
R20 2.7K
R21 1K ±1%
R22 1K ±1%
R23 5K 1W
C01 6800 PF ±20%
C02 6800 PF ±20%
C03 0.1 (100PF)
C04 0.1 (100PF)
C05 .004
C06 .004
C07 220PF (33PF)
CR01
CR02
CR03
CR04
CR07
CR08
CR09
CR10
Q01
Q02
Q03
Q04
Q05
TP-A
TP-C
NOTE:
1. DIODE PAIRS CR01,02 / CR03,04 / CR07,08 / CR09,10 ARE MATCHED, SILICON, 5024020I.
2. COMPONENT ASSY NO. 50013700. ATA 50013701 ATB
3 VALUES IN PARENTHESIS USED IN ATB
4. C03 AND C04, IN ATB, ARE NON-POLARIZED
5. Q01 THRU Q05 SILICON, NPN, 502I0102.

ATA


CARD ATA
PIN 1

# POWER SUPPLY REGULATORS

## AUA

This card provides a regulated ±15v to an operational amplifier (such as the FSA used in the servo actuator for the disk file). There are two identical +15v stages and two identical -15v stages on the card.

Each circuit is an emitter follower with a 15v zener diode from base to ground. The maximum load current possible before the zener comes out of conduction, assuming a 10% low power supply voltage, is 33 ma. This corresponds to an equivalent load resistance of 455 ohms.

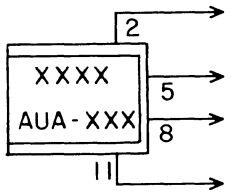
The output impedance is approximately the $r_e$ of the transistor in the Tee parameters. This is also equal to $26/I_e$. For these circuits, $I_e$ is approximately 10 ma, resulting in an output impedance of 2.6 ohms.

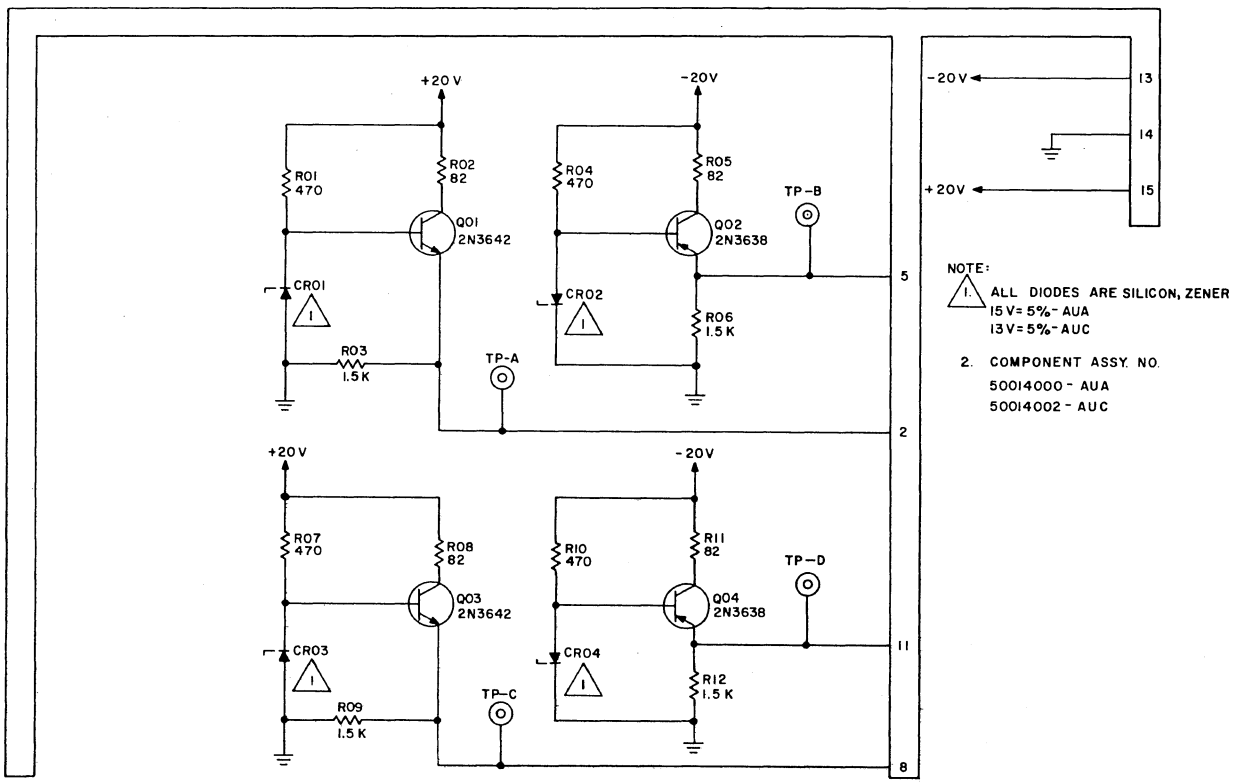
## AUC

The AUC provides a regulated ±12v to the timing arm read preamplifiers. There are two identical +12v stages and two identical -12v stages on the card.

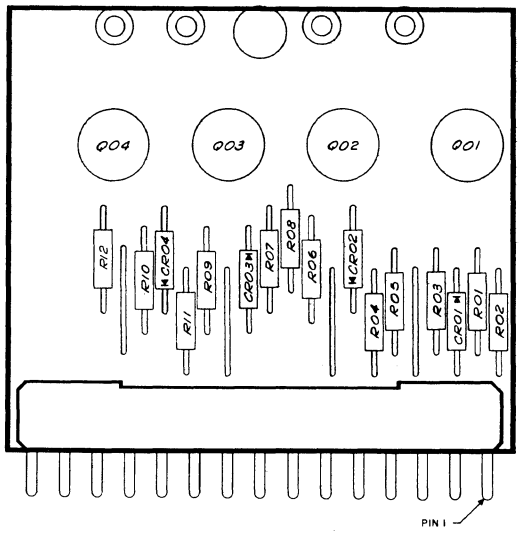
Each circuit is an emitter follower with a 13v zener diode from base to ground. The base-emitter diode drop produces an output voltage of approximately 12.3 volts. The maximum load current that is available before the zener comes out of conduction, assuming a 10% low power supply voltage, is 35 ma. This corresponds to an equivalent load resistance of 345 ohms.

TYPICAL SYMBOL (AUA, C)



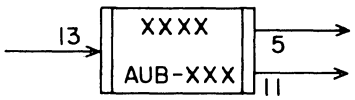

+20 V
-20V
R01
470
R02
82
Q01
2N3642
CR01
R03
1.5K
TP-A
R04
470
R05
82
Q02
2N3638
TP-B
CR02
R06
1.5K
-20V
13
14
+20V
15
5
2
NOTE:
1. ALL DIODES ARE SILICON, ZENER
15 V = 5% - AUA
13 V = 5% - AUC
2. COMPONENT ASSY. NO.
50014000 - AUA
50014002 - AUC
+20 V
R07
470
R08
82
Q03
2N3642
CR03
R09
1.5 K
TP-C
-20V
R10
470
R11
82
Q04
2N3638
TP-D
CR04
R12
1.5 K
11
8

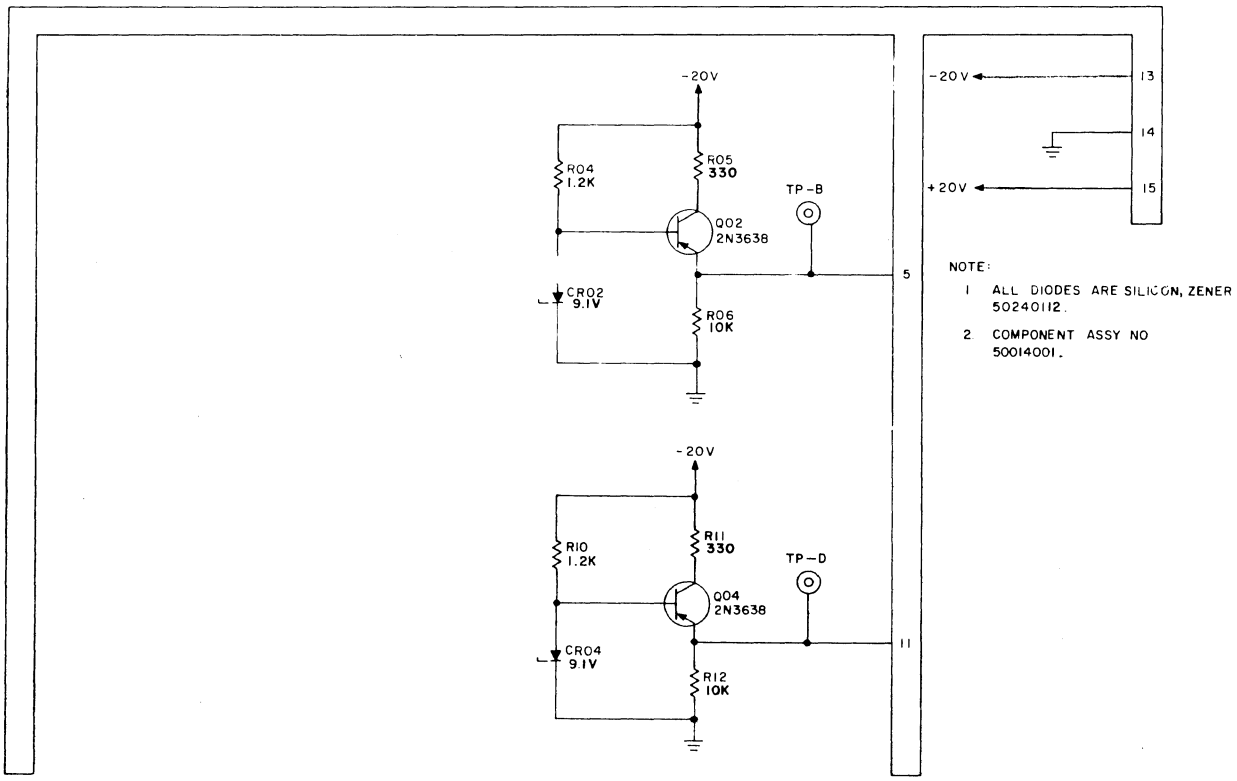
AUA, AUC

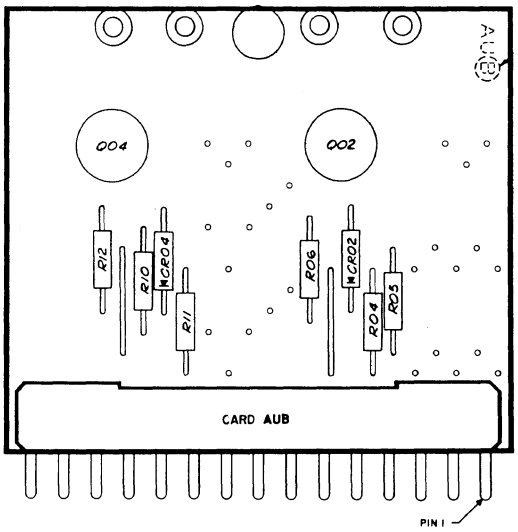

Q04
Q03
Q02
Q01
R12
R10
CR04
R11
R09
CR03
R07
R08
R06
CR02
R04
R05
R03
CR01
R01
R02
PIN 1

# POWER AND CLAMP VOLTAGE SUPPLY
# AUB

The AUB has two identical regulating circuits providing clamp voltages of -8.4v to the AIB. The circuit basically consists of an emitter follower with a PNP transistor and a 9.1v zener diode. The anode of the zener diode is connected to the base of the transistor and the cathode is tied to ground. The zener diode is held in conduction by current flow through resistor R4 (R10) to the -20v supply. Assuming 10% low power supply voltage, a maximum load current of 25 ma is possible without causing the zener diode to stop conducting. This corresponds to an equivalent load resistance of approximately 330 ohms. Collector resistors are used to provide the transistor with some protection against short circuits on the output.




-20V
R04
1.2K
R05
330
TP-B
Q02
2N3638
CR02
9.1V
R06
10K
5
-20V
R10
1.2K
R11
330
TP-D
Q04
2N3638
CR04
9.1V
R12
10K
11
-20V
13
14
+20V
15
NOTE:
1 ALL DIODES ARE SILICON, ZENER 50240112.
2 COMPONENT ASSY NO 50014001.


A1A8
Q04
Q02
R12
R10
MCR04
R11
R06
MCR02
R04
R05
CARD AUB
PIN 1

## WRITE RESISTOR/DIODE CARDS
## AVA, AVB, AVC, AVD

These cards connect between the erase/write drivers and the read/write heads. The read amplifier connects to the head via this card. There are two identical sections per card.

### AVA, AVD

On these, each section of the card contains one input connected to a single resistor or a resistor/diode combination.

The resistor determines the magnitude of the erase/write connect; the diode(s) provide isolation.

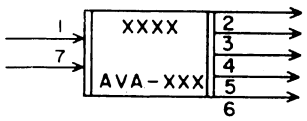
### AVB

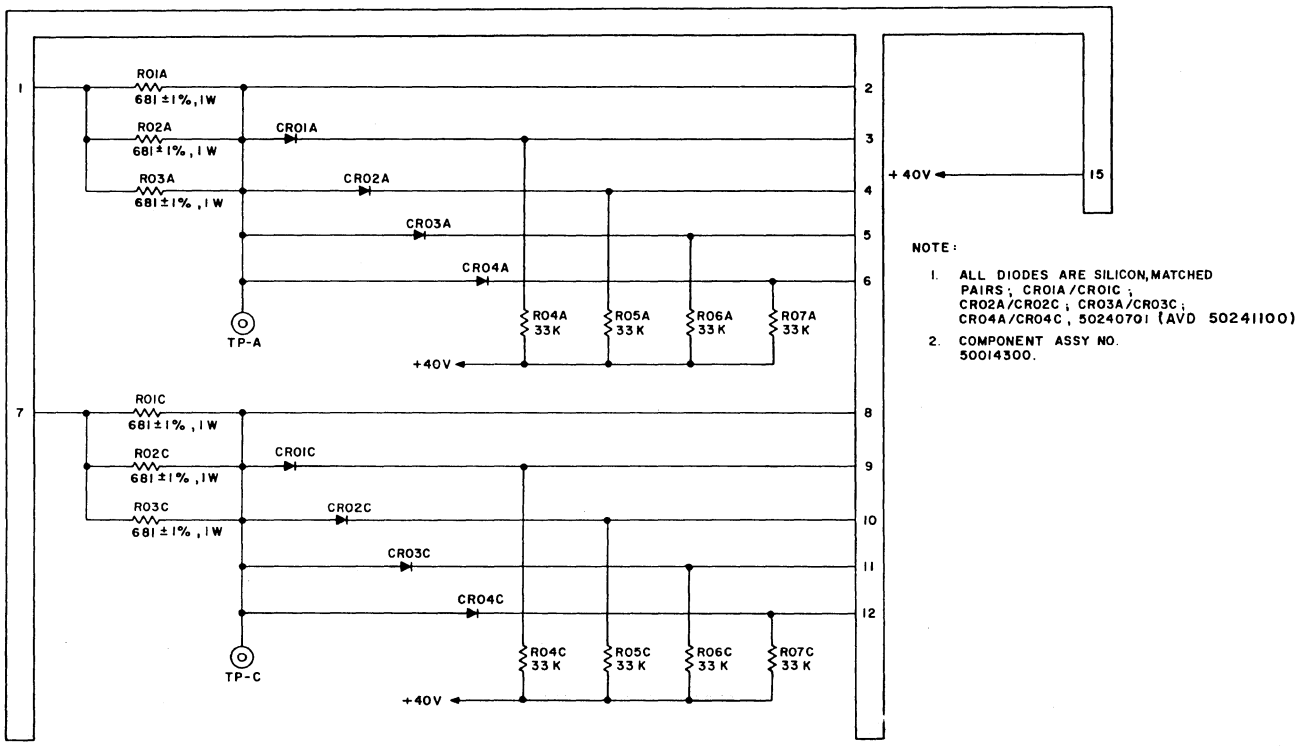
This card is similar to the AVA; however, only the R01, R02, and R03 resistors are present. The isolation diodes and resistors R04 - R07 are not used on the AVB card.

### AVC

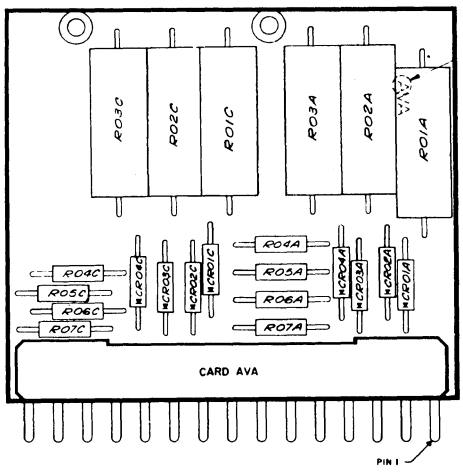
This card is similar to the AVA; however, only the resistors are present on this card. There are no diodes on the AVC card.

SYMBOL




R01A
681 ±1%, 1W
R02A
681 ±1%, 1W
R03A
681 ±1%, 1W
CR01A
CR02A
CR03A
CR04A
R04A 33K
R05A 33K
R06A 33K
R07A 33K
TP-A
+40V
R01C
681 ±1%, 1W
R02C
681 ±1%, 1W
R03C
681 ±1%, 1W
CR01C
CR02C
CR03C
CR04C
R04C 33K
R05C 33K
R06C 33K
R07C 33K
TP-C
+40V
+40V
1
2
3
4
5
6
7
8
9
10
11
12
15
NOTE:
1. ALL DIODES ARE SILICON, MATCHED PAIRS; CR01A/CR01C; CR02A/CR02C; CR03A/CR03C; CR04A/CR04C, 5024070I (AVD 5024II00)
2. COMPONENT ASSY NO. 50014300.

AVA, AVD


R03C
R02C
R01C
R03A
R02A
R01A
R04C
R05C
R06C
R07C
CR04C
CR03C
CR02C
CR01C
R04A
R05A
R06A
R07A
CR04A
CR03A
CR02A
CR01A
CARD AVA
PIN 1

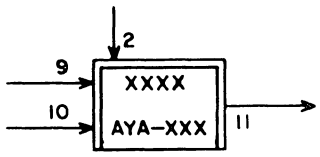
## VOLTAGE CHECKER
## AYA, AYB

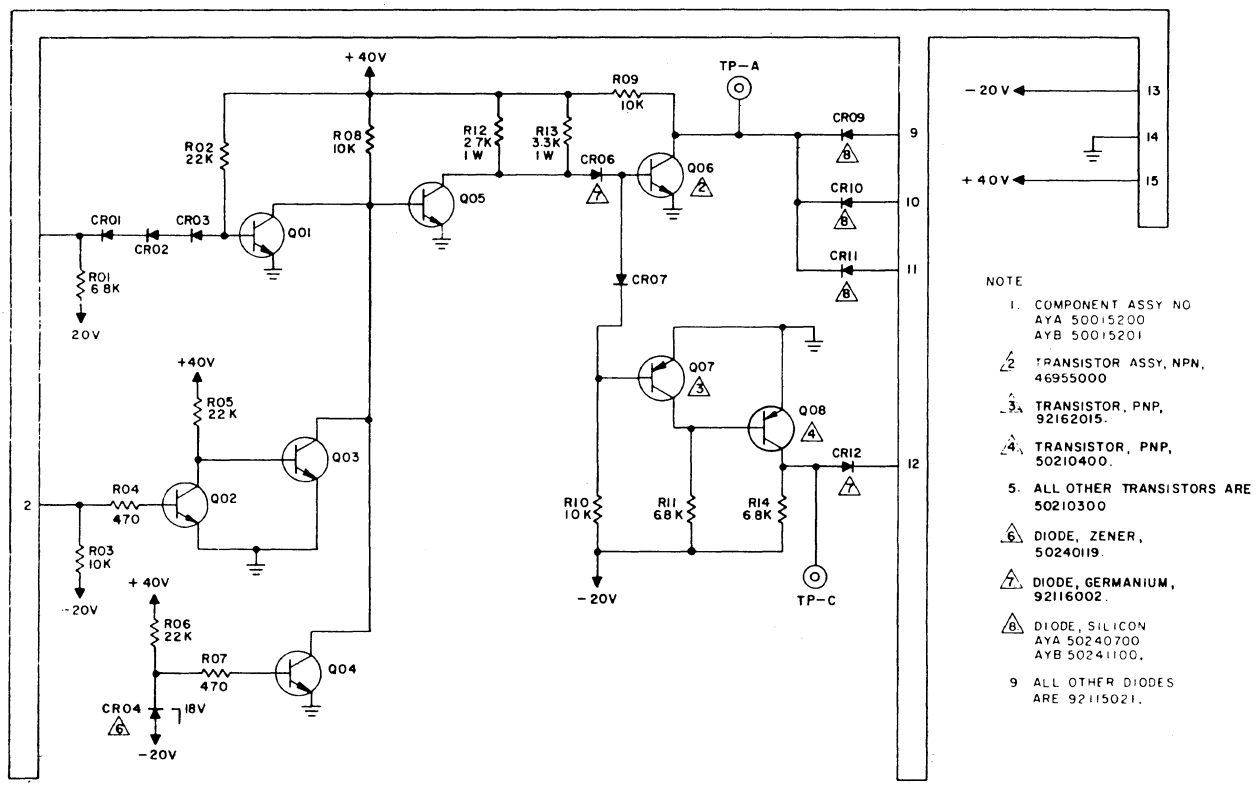
These cards keep and erase current from reaching write and erase heads if one or more of the following conditions is true: 1) If +20V drops below +17.6V nominal. 2) If -20V gets closer to ground than -17.2V nominal. 3) If an external logic signal goes to logic zero (-0.5V). A logic output goes to logic zero.

If pin 1 goes to logic zero, Q01 turns on. This turns off Q05, which turns Q06 on, and forces TP C toward -20V. Q06 absorbs up to 500 ma. CR09, 10, 11 are to isolate the AYA card and the write and erase heads from each other when the AYA card is off.

Pin 2 senses the state of the +20V supply. If it gets to +17.6 $\pm$ 0.9V, Q02 turns off and Q03 turns on. This has the same effect as Q01 turning on. Q04 turns on if -20V supply gets to -17.2V $\pm$ 0.9V. This has the same effect as Q01 turning on. If more than one of these three sensing circuits respond at one time, the effect is the same as if only one was on.

SYMBOL

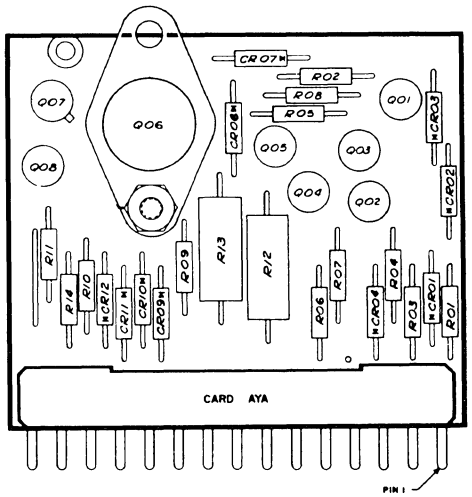





NOTE

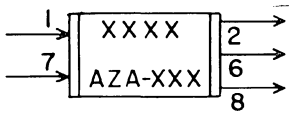
1. COMPONENT ASSY NO
   AYA 50015200
   AYB 50015201
2. TRANSISTOR ASSY, NPN, 46955000
3. TRANSISTOR, PNP, 92162015.
4. TRANSISTOR, PNP, 50210400.
5. ALL OTHER TRANSISTORS ARE 50210300
6. DIODE, ZENER, 50240119.
7. DIODE, GERMANIUM, 92116002.
8. DIODE, SILICON
   AYA 50240700
   AYB 50241100.
9. ALL OTHER DIODES ARE 92115021.

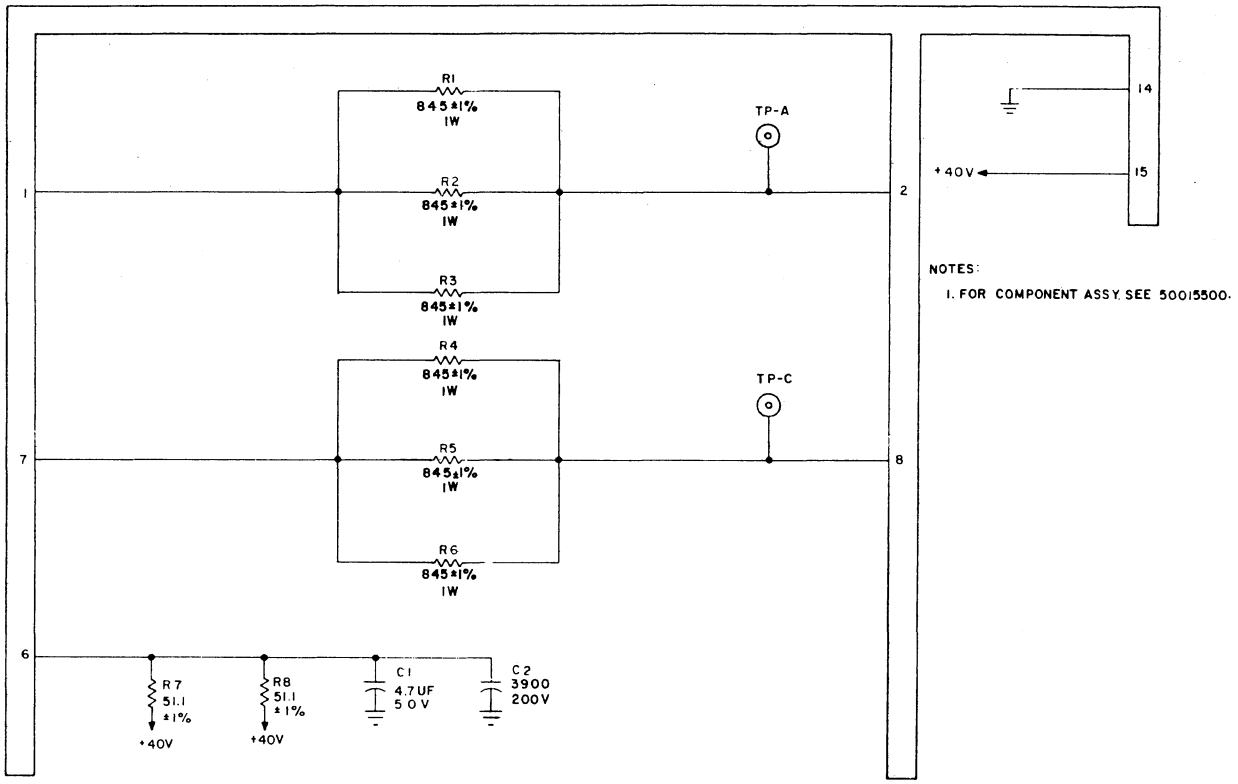
AYA, AYB

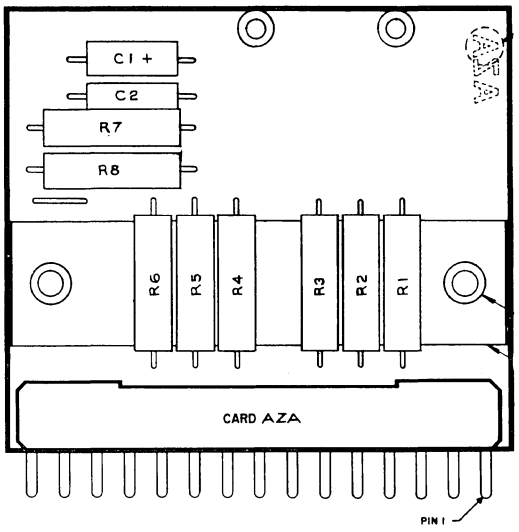


# WRITE RESISTOR
## AZA

This card (follows the BMA write driver in the write chain) controls the amplitude of the write current in the disk file R/W head. It also supplies +40v power to the output stage of the write driver. This current is supplied through two parallel resistors to produce a voltage drop proportional to the write current which is used in error checking. The power output from AZA to the write driver is filtered by two capacitors in parallel, C1 and C2.




R1
845±1%
1W
R2
845±1%
1W
R3
845±1%
1W
R4
845±1%
1W
R5
845±1%
1W
R6
845±1%
1W
TP-A
TP-C
1
2
7
8
6
14
15
+40V
R7
51.1
±1%
+40V
R8
51.1
±1%
+40V
C1
4.7UF
50V
C2
3900
200V
NOTES:
1. FOR COMPONENT ASSY. SEE 50015500.


C1 +
C2
R7
R8
R6
R5
R4
R3
R2
R1
CARD AZA
PIN 1

VOLTAGE CHECKER

## BAA, BAB, BBA, BCA, BCB

These cards keep write current and erase current from reaching write heads and erase heads, if one or more of the following conditions are true: 1) +40v drops below +35.0v nominal. 2) +20v drops below +17.6V nominal. 3) -20v gets closer to ground than -17.2v nominal. 4) An external logic signal goes to zero (-0.5v). Logic outputs go to logic zero.

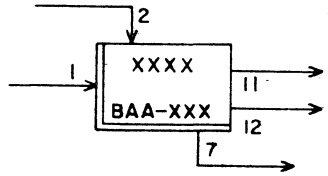
The BAA card has an input on pin 1 from the GAA card, indicating the state of +20v supply. If the +20v supply is at +17.6v ($\pm$ 0.9v), Q01 will turn off and Q02 will turn on. This will turn Q07 off, giving a logic zero out at pins 11 and 12. The Q03 circuit tests the -20V supply. If the -20v is at -17.2v ($\pm$ 0.9v), Q03 will turn on, which has the same effect as Q02 turning on. The Q04-Q05 circuit tests the +40v supply. If the +40v supply is at +35.0v ($\pm$ 1.8v), Q04 will turn off and Q05 will turn on. This has the same effect as Q02 turning on. If the input at pin 2 goes to logic zero (-0.5v), Q06 will turn on. This also has the same effect as Q02 turning on. If more than one of these four sensing circuits respond at one time, the effect is the same as if only one was on.

The BAB card is the same as the BAA card, except that the Q04, 5, and 6 circuits are left off, and R04, 12, and 16 are changed to allow operation from +20v on pin 15.

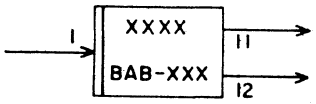
The BBA card has Q01 turned on if Q07 on the BAA card is turned off. An external resistor to $+V_s$ is required from pin 10. The BCA card has Q01 turned on if Q01 on the BBA card is turned on. Diodes CR07-12 are to isolate the BCA cards and the write and erase heads from each other when the BCA cards are off.

As used in the 807 Disc File, one BAA and BBA drive six BCA cards. Each BCA card then absorbs up to 0.8 amperes of write or erase current. These cards operate from a special $+V_s$ on pin 15, to allow operation if either +20v or +40v fails.

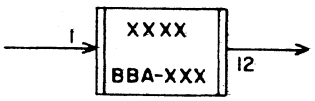
SYMBOL



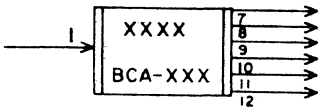

SYMBOL



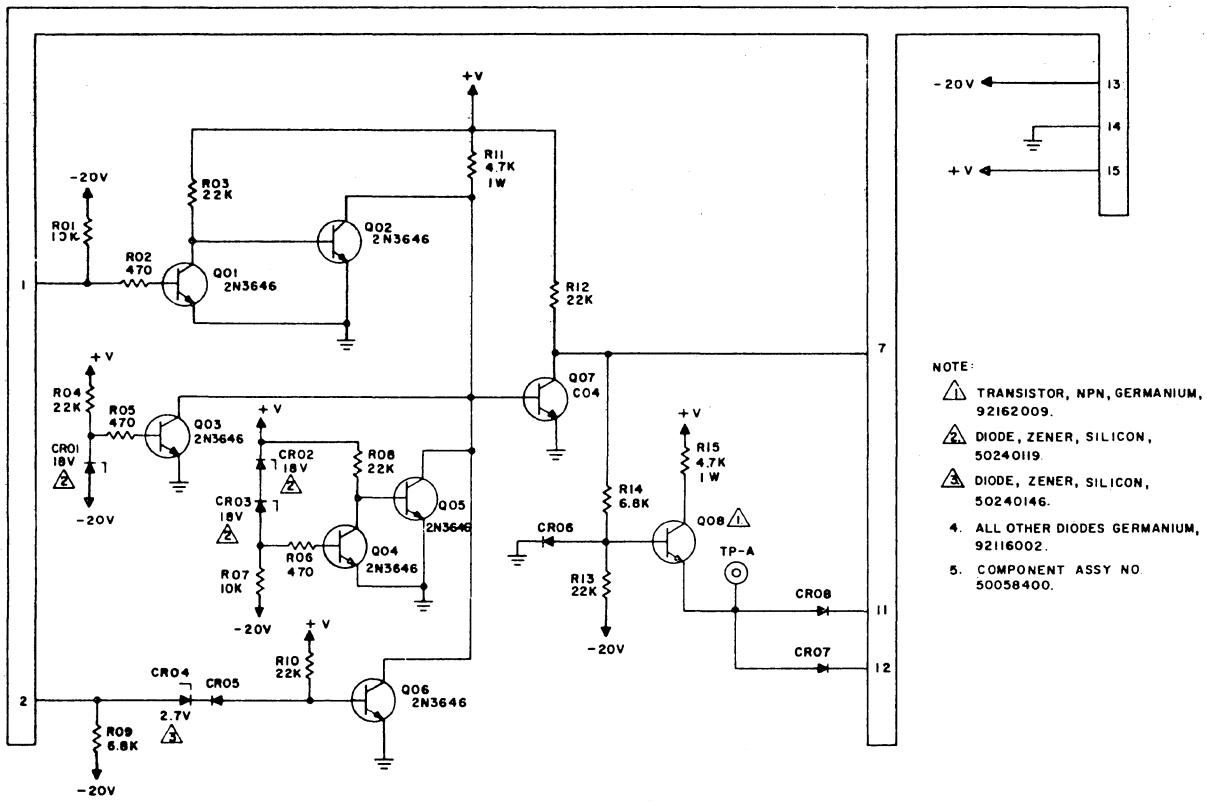

SYMBOL




SYMBOL
(BCA, BCB)

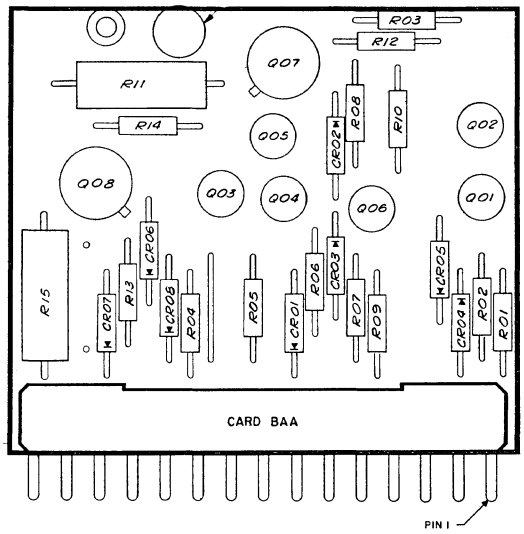


# BAA

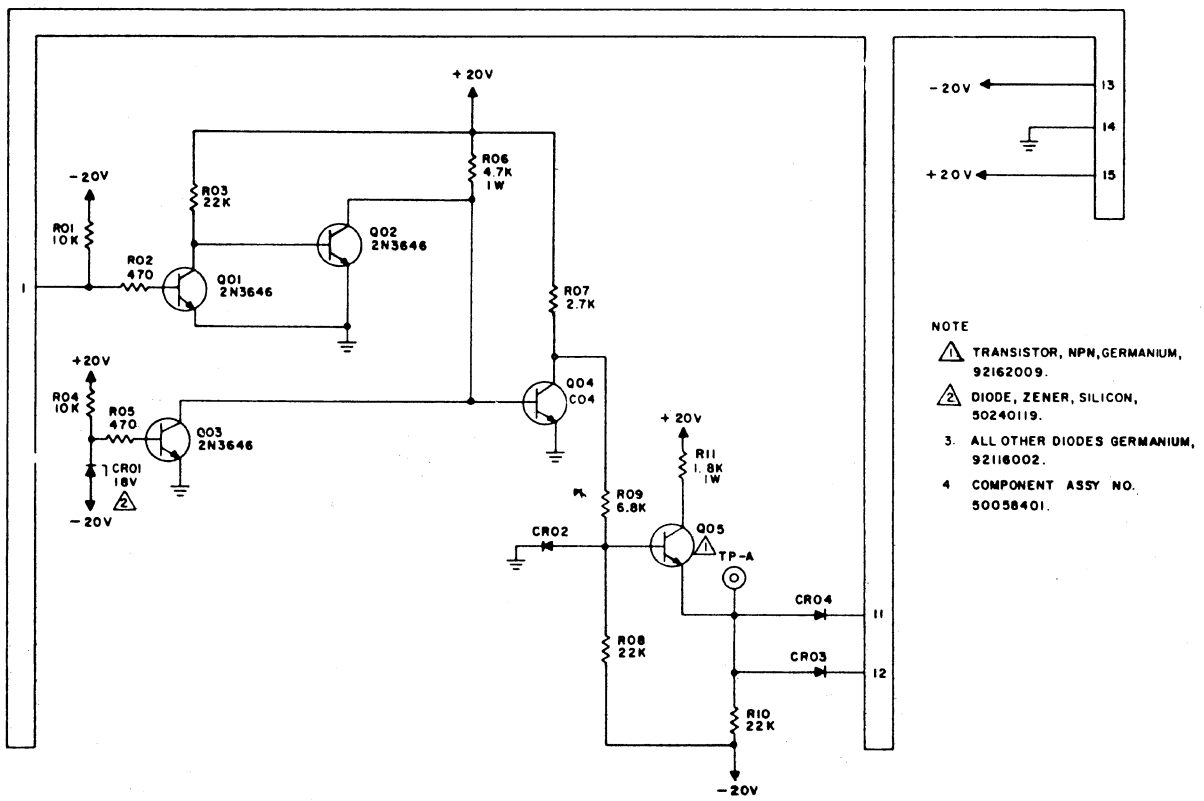



NOTE:

1. TRANSISTOR, NPN, GERMANIUM, 92162009.
2. DIODE, ZENER, SILICON, 50240119.
3. DIODE, ZENER, SILICON, 50240146.
4. ALL OTHER DIODES GERMANIUM, 92116002.
5. COMPONENT ASSY NO 50058400.

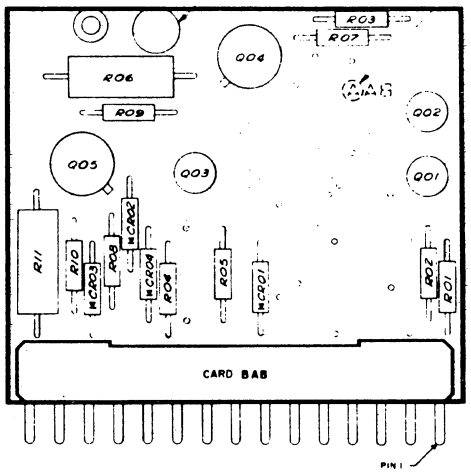


# BAB

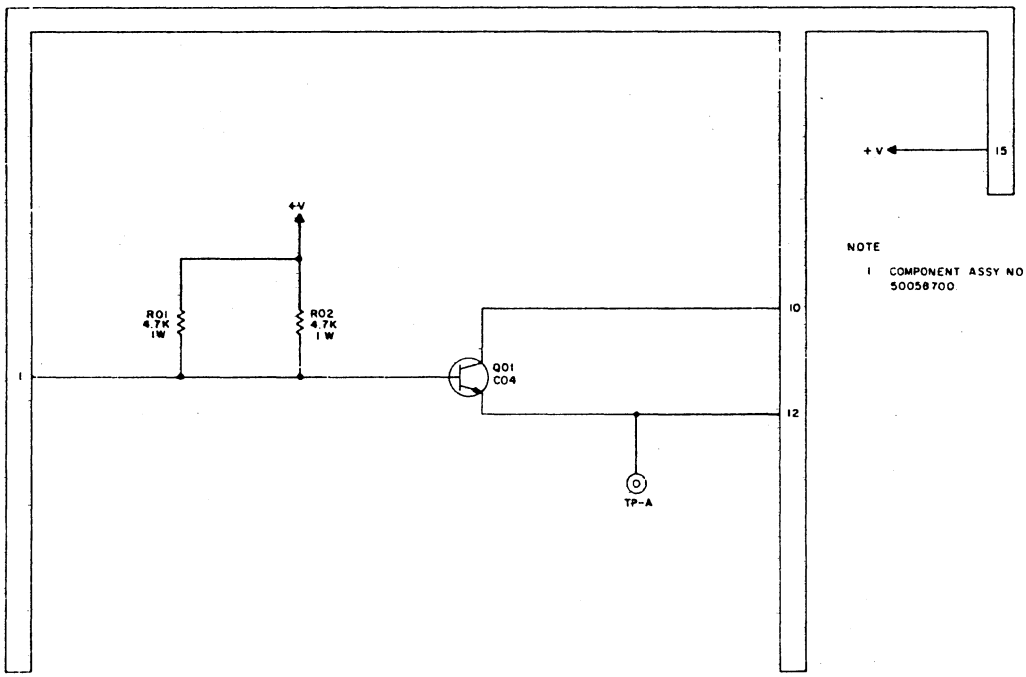


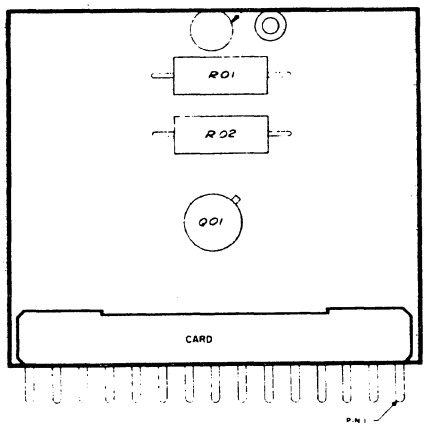

NOTE

1. TRANSISTOR, NPN, GERMANIUM, 92162009.
2. DIODE, ZENER, SILICON, 50240119.
3. ALL OTHER DIODES GERMANIUM, 92116002.
4. COMPONENT ASSY NO. 50058401.

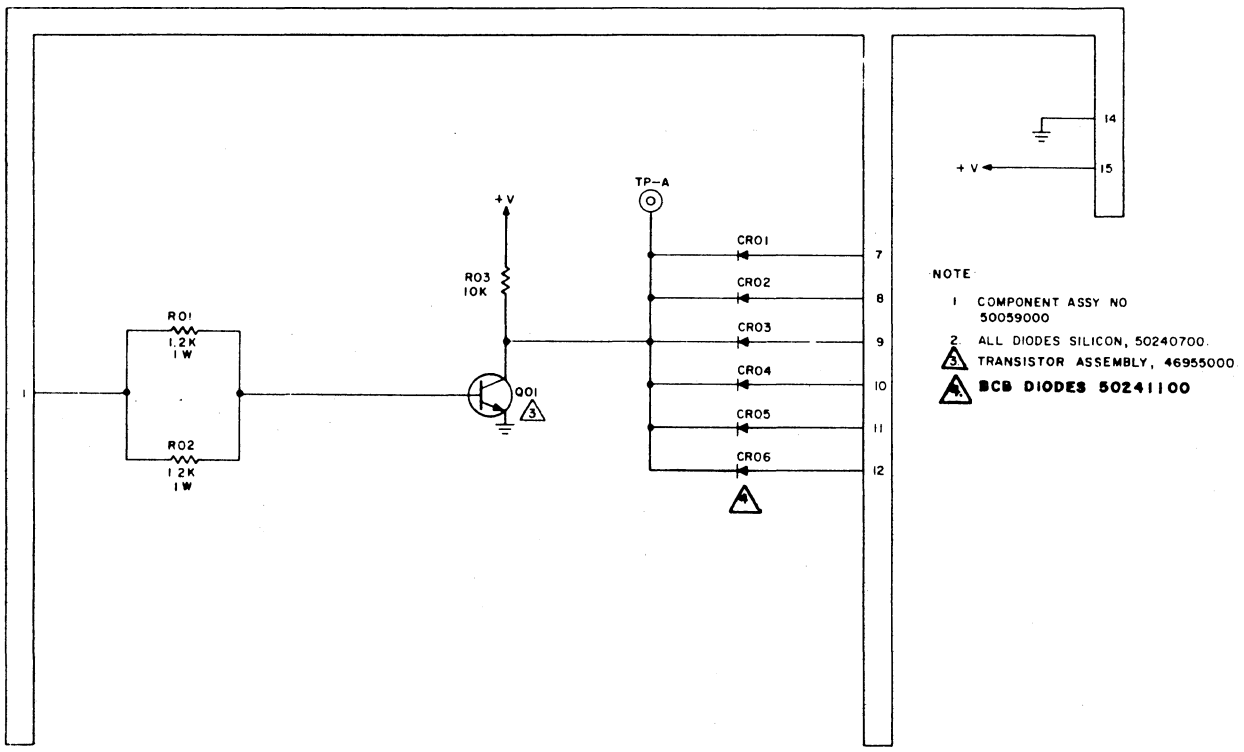


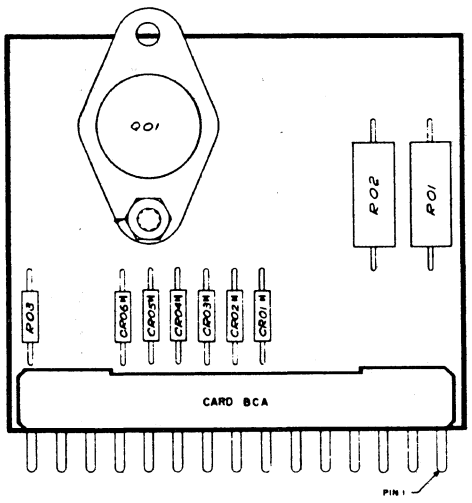
BBA


+V
15
NOTE
1 COMPONENT ASSY NO 50058700.
+V
R01 4.7K 1W
R02 4.7K 1W
Q01 C04
1
10
12
TP-A


R01
R02
Q01
CARD
P.N.1

# BCA, BCB


+V
R03
10K
TP-A
CR01
CR02
CR03
CR04
CR05
CR06
R01
1.2K
1W
R02
1.2K
1W
Q01
3
1
7
8
9
10
11
12
14
15
+V
NOTE
1 COMPONENT ASSY NO 50059000
2 ALL DIODES SILICON, 50240700
3 TRANSISTOR ASSEMBLY, 46955000
4 BCB DIODES 50241100


Q01
R02
R01
R03
CR06
CR05
CR04
CR03
CR02
CR01
CARD BCA
PIN 1

## HEAD SWITCH

## BDA

This card operates as a switch that allows a single writer "AMD" and reader "FXA" to be switched into any head in the head matrix. Center taps of the R/W heads are selected by IOB circuits. The BDA, in conjunction with the IOB, provides head switching for the coordinates of the head matrix. A logic "1" applied to pin 2 causes read/write and erase currents to be applied to the heads and provide an error checking signal. A logic "0" applied to pin 2 causes the circuit to turn off and no read/write or erase current is supplied.

A logic "0" at pin 2 turns Q01 on causing the emitter follower Q02 to go to slightly below ground at the emitter which turns off Q03, Q04, Q05, and Q06.

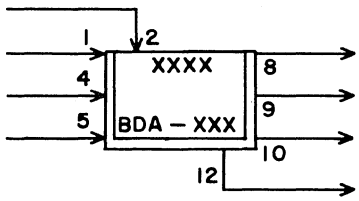
A "1" input on pin 2 turns Q01 to off causing the emitter of Q02 to go to approximately +31 volts which turns on Q03, Q04, Q05, and Q06. Q03 provides erase current (300 ma maximum) to the erase head via pin 8. Q04 and Q05 conduct the write or read current to the heads via pins 10 and 12 respectively. R10 and R11 provide biasing for up to 150 ma of write current per side.

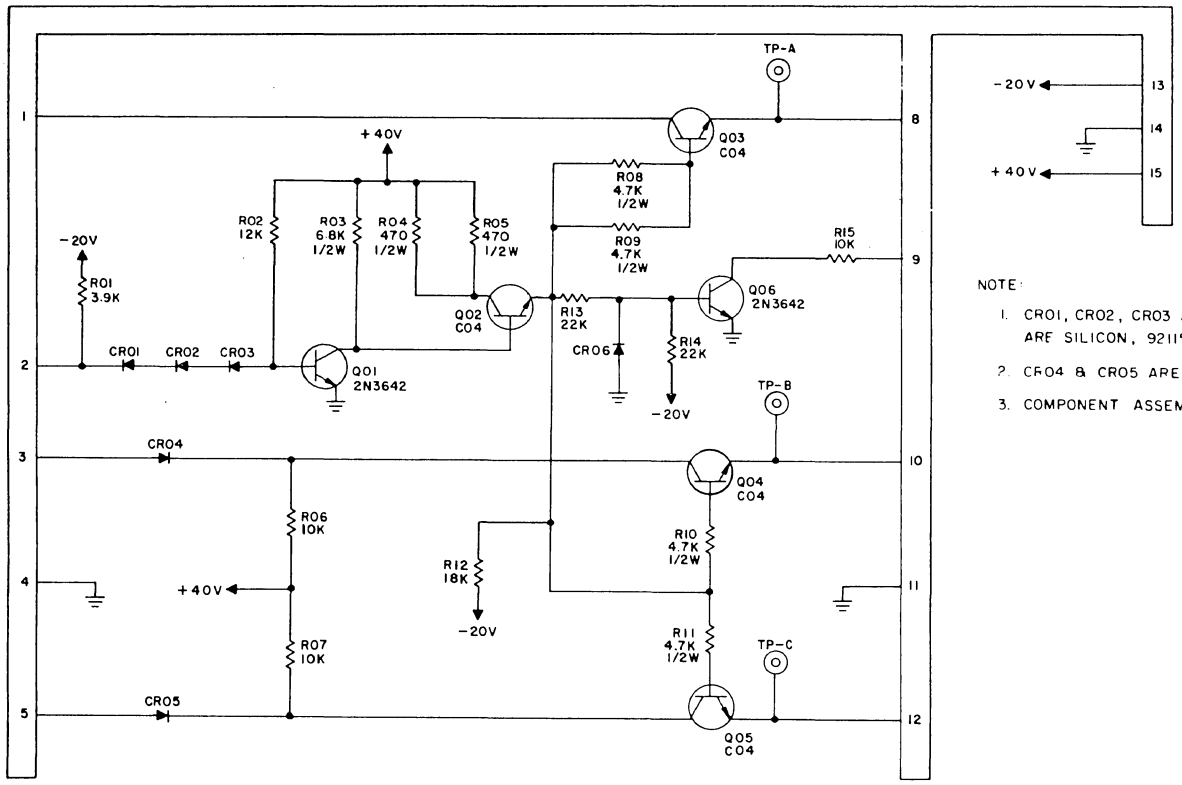
Q06 provides a signal to drive the error detector AOA. The output of pin 9 is identical to the error detector output of pins 5 and 11 of the IOB. R13, CR06, and R14 provide off/on biasing for Q06.

Input 1 is driven via an AME through a resistor card (AVA) to derive the proper erase current from an initial +40 volt source. The AME provides turn-off of the erase current during read operations.

Input 2 is derived from logic levels and requires a maximum of 5.1 ma input at ground.

Inputs 3 and 5 are connected in parallel to other BDA circuits and are connected to both the AMD (through an AVA resistor card) and to the FXA reader.

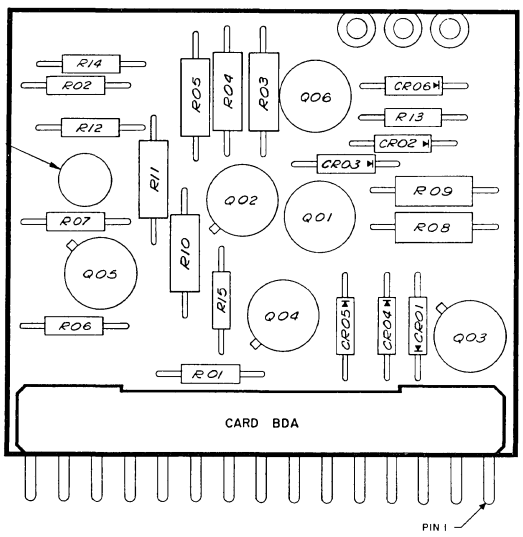




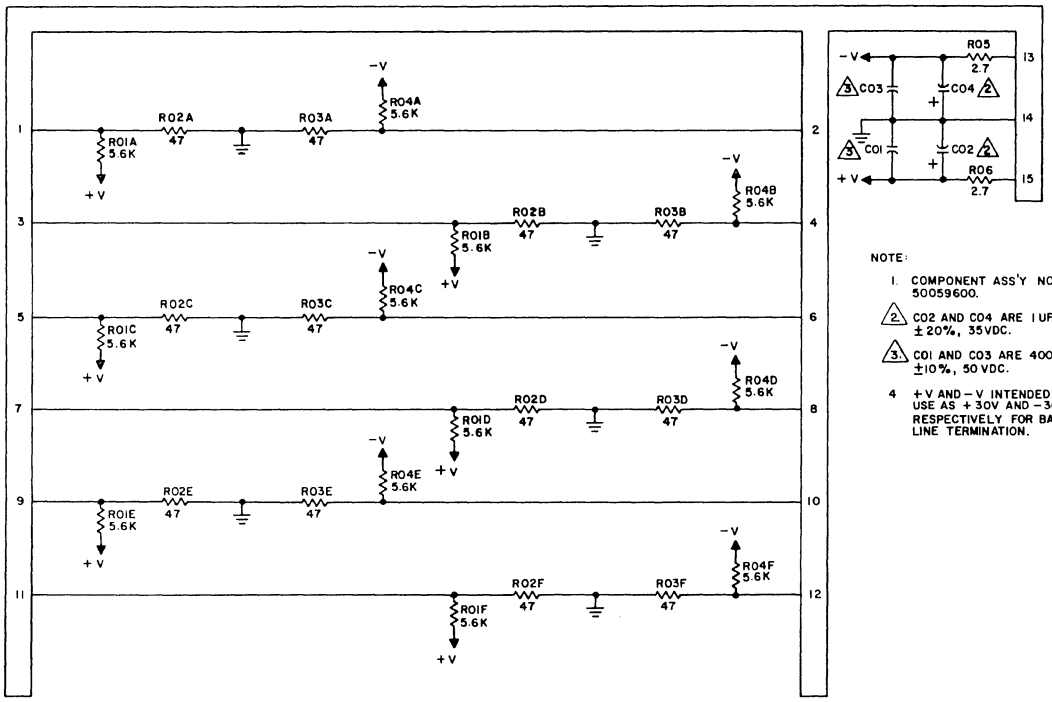

NOTE:

1. CR01, CR02, CR03 AND CR06 ARE SILICON, 92115021.
2. CR04 & CR05 ARE SILICON, 50241100.
3. COMPONENT ASSEMBLY NO. 50059300.

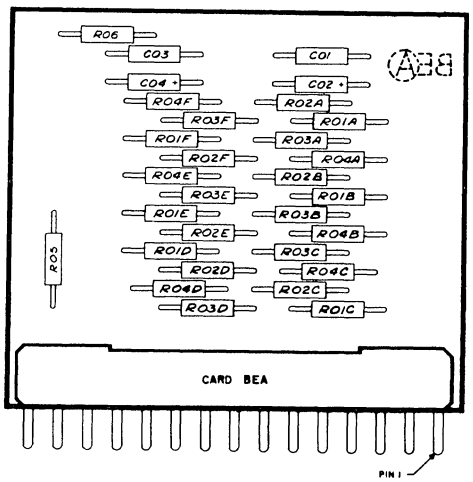
BDA

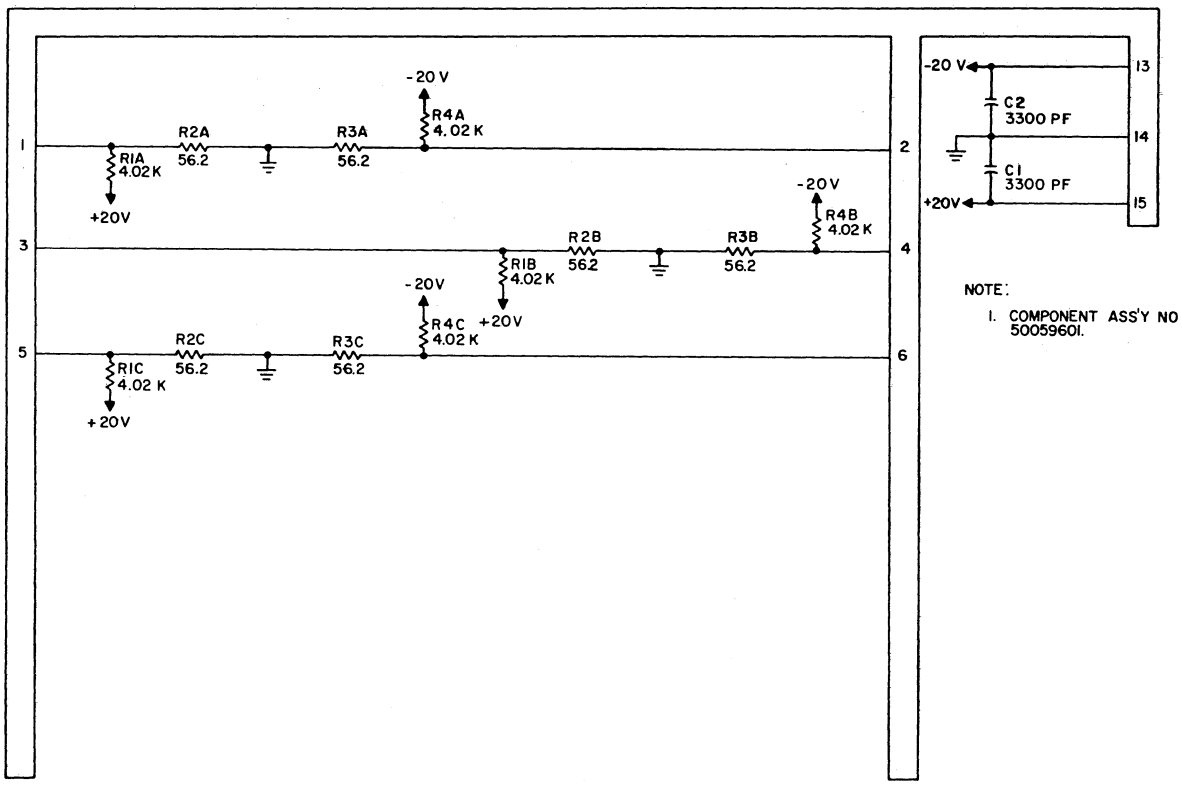


# LINE TERMINATORS
## BEA, BEB

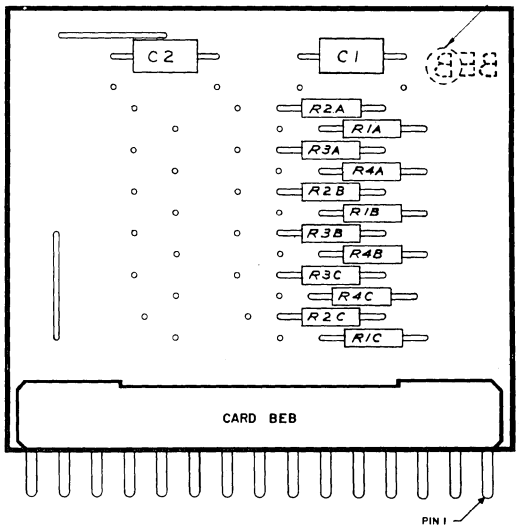



BEA




-20 V
R4A
4.02 K
R2A
56.2
R3A
56.2
1
2
R1A
4.02K
+20V
-20 V
R4B
4.02 K
3
4
R2B
56.2
R3B
56.2
R1B
4.02 K
-20V
R4C
4.02 K
+20V
R2C
56.2
R3C
56.2
5
6
R1C
4.02 K
+20V
-20 V
13
C2
3300 PF
14
C1
3300 PF
+20V
15
NOTE:
1. COMPONENT ASS'Y NO 5005960I.

BEB


C2
C1
R2A
R1A
R3A
R4A
R2B
R1B
R3B
R4B
R3C
R4C
R2C
R1C
CARD BEB
PIN 1

# L TYPE DATA RECEIVER
## BFA

The BFA card was originally designed for use in the OEM disk storage drives as a data receiver. The data is supplied to the circuit via a 95-ohm coaxial cable from the controller at a maximum rate of 3 MHz.

Each BFA card contains a single circuit consisting of two inverters with the input swinging from +.2v to +3v (nominal). The output provides standard Control Data 1604-type logic levels. With the input at +0.2v, the output is at -3v ("1") and with the input at +3v, the output is at 0v ("0").

With the input at +0.2v, diode CR01 conducts such that the anode of CR02 is at about +0.8v. The divider action of CR02, 3, 4 and R06 network causes the base of Q01 to be approximately -1.2v. This represents a low impedance turn-off source for Q01 to provide rapid turn-off. With Q01 off, its collector is at +3v. The divider action of CR05, 6 with R09 causes the base of Q02 to be approximately +1.8v. The equivalent turn-off circuit has a resistance of about 280 ohms. This helps to effect rapid turn-off of Q02. At this time the collector of Q02 is at -3v.

When the input is +3v, diode CR01 opens up as the anode becomes clamped at about +2.4v due to the conduction of CR02, 3, 4, and the base-emitter diode of Q01 via R05 to the +6v supply. The collector of Q01 is now at ground so CR05, 6 open since the base of Q02 clamps to -0.6v due to conduction through R09 to the -3v supply. Q02 is on and the output is near ground.

The switching threshold is approximately +1.8v. Typical switching waveforms are shown in Figure 1.

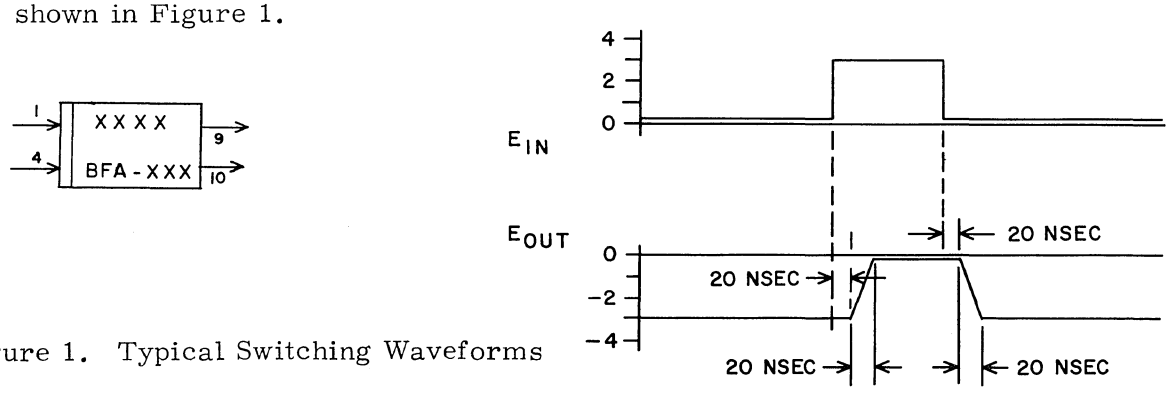
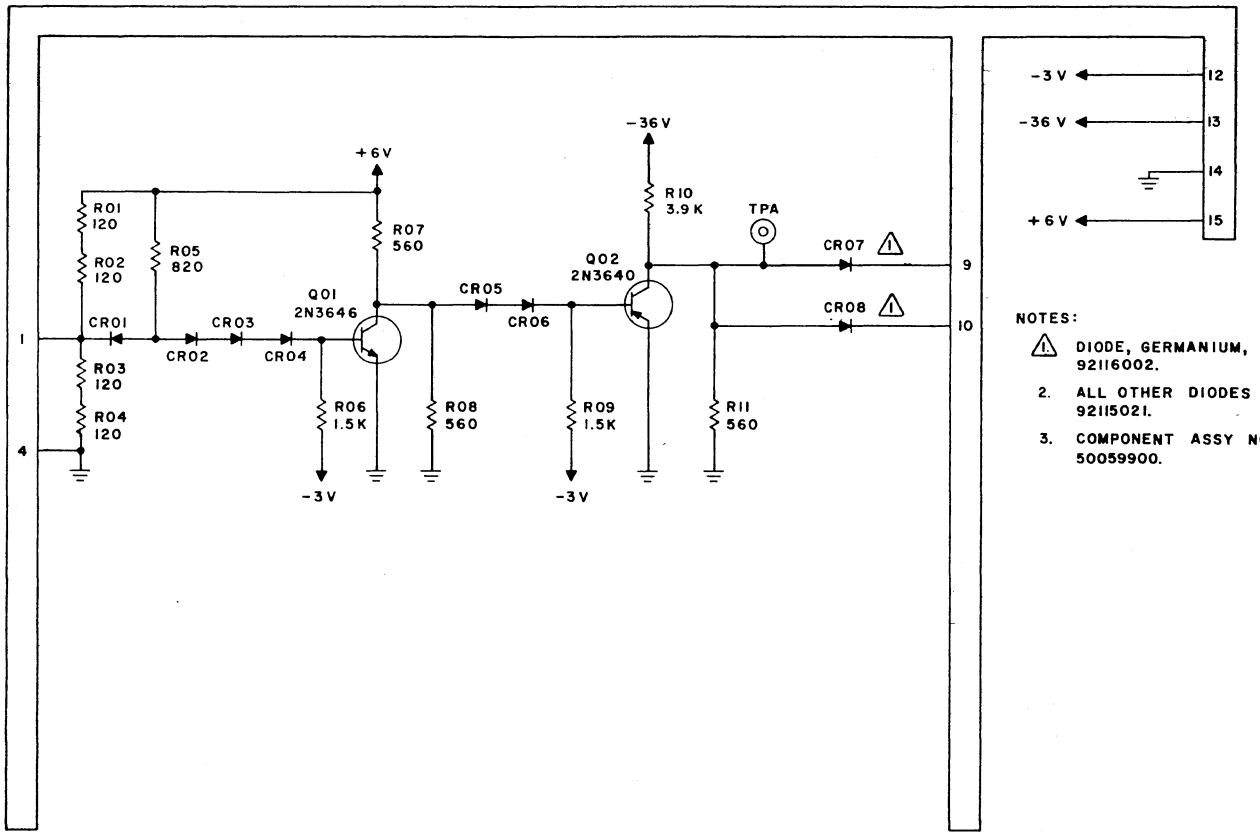
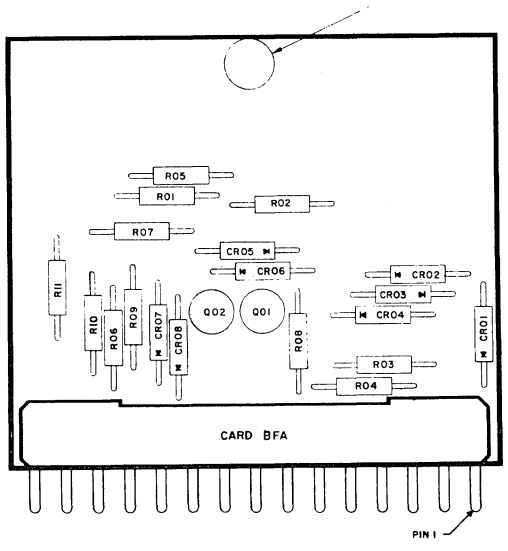



Figure 1. Typical Switching Waveforms


-3 V
-36 V
+6 V
12
13
14
15
-36V
+6V
R10
3.9K
TPA
R01
120
R02
120
R05
820
R07
560
Q02
2N3640
CR07
CR08
9
10
Q01
2N3646
CR05
CR06
1
CR01
CR03
CR02
CR04
R03
120
R04
120
R06
1.5K
R08
560
R09
1.5K
R11
560
4
-3V
-3V
NOTES:
1. DIODE, GERMANIUM, 92116002.
2. ALL OTHER DIODES ARE 92115021.
3. COMPONENT ASSY NO. 50059900.


R05
R01
R02
R07
CR05
CR06
CR02
CR03
CR04
R11
R10
R06
R09
CR07
CR08
Q02
Q01
R08
CR01
R03
R04
CARD BFA
PIN 1

# L TYPE DATA TRANSMITTER

## BGA

The BGA card is designed for use in the OEM disk storage drives as data transmitters for rates up to 3 MHz. A 95-ohm coaxial cable couples to the output and carries the data to the controller. There is a single circuit per card consisting of an emitter follower and an inverter. When the input to the card is 0v, the output is at 0v; when the input is -3v, the output is at +3v.

With a "1" input, pin 1 becomes -2.8v (or more negative). If the diode drops and $V_{BE}$ of Q01 are taken as 0.6v, the base of Q02 becomes -1v and Q02 is turned off so the output is at +3v. The output begins to switch when the input is at about -1.2v.

When the input goes to a -0.5 to 0v range, the emitter of Q01 is essentially at ground and diodes CR01, 2 will not conduct since the base of Q02 clamps to about +0.6v. With Q02 on, the output is at 0v.

The voltage divider composed of R05, 6, 7, and 8 serves to terminate the coaxial cable at the transmitting end and provides for the correct level on the line.

Typical (theoretical) switching waveforms are shown in Figure 1 (these are for guidance and not intended to be used as specifications). It will be noticed that no storage or delay is indicated.

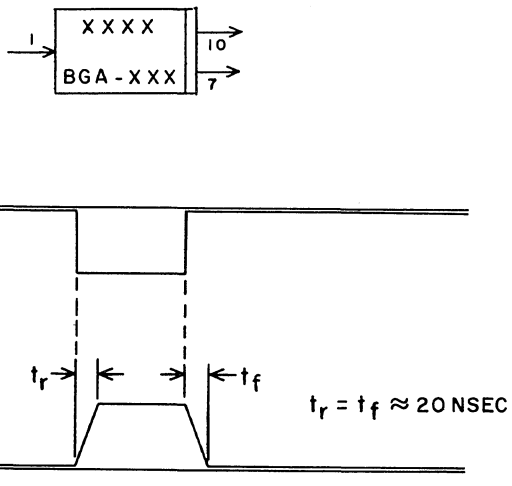
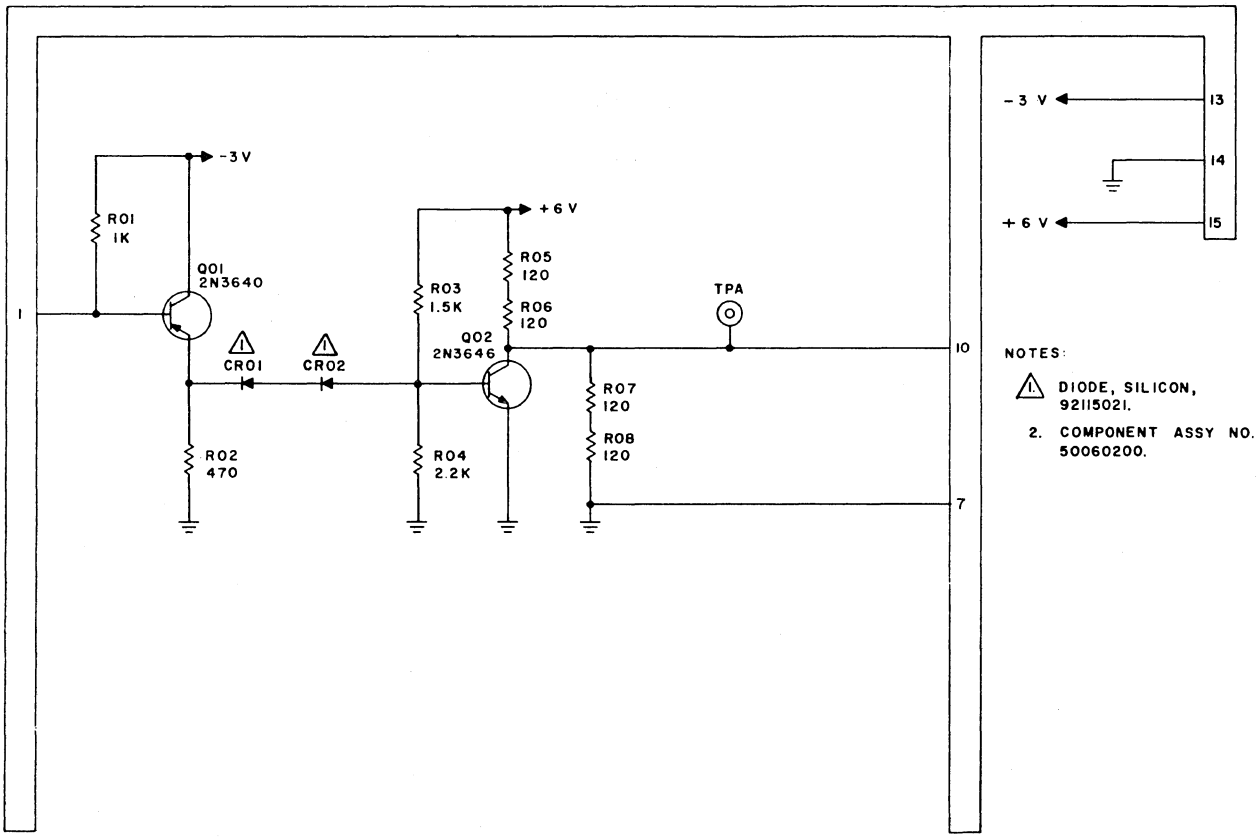
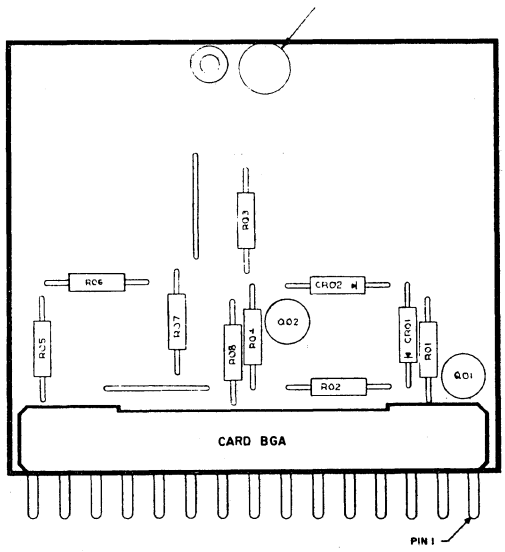



Figure 1. Typical Switching Waveforms


-3 V
13
14
+6 V
15
-3V
R01
1K
Q01
2N3640
+6V
R05
120
R03
1.5K
R06
120
TPA
1
Q02
2N3646
10
CR01
CR02
R07
120
R08
120
R02
470
R04
2.2K
7
NOTES:
1. DIODE, SILICON, 92115021.
2. COMPONENT ASSY NO. 50060200.


R03
R06
CR02
R05
R04
Q02
CR01
R01
Q01
R02
CARD BGA
PIN 1

## Q TYPE CONTROL RECEIVER

## BHA, BHB

The BHA/B receivers are designed for use in the OEM disk storage drives. The cards have two identical circuits per board and are similar except that the BHA has no termination on the card for the twisted-pair input.

The BHA is intended for multiplex (party line) use and the termination is on the last disk storage drive unit in a plug-in assembly. The BHB has the termination on the card and is used for simplex operation. Both cards are used with control (rather than data) lines between the disk storage drive and the controller.

Each circuit consists of a pair of inverters. The high level input, whether terminated on the card or externally, is equivalent to 93.5 ohms in series with +1.27v from the input pin to ground. The low level input is -3v with a series impedance determined by the -3v power supply. Thus if the input is + the output is at ground and when the input is at -3v the output is also at -3v. Typical switching waveforms are shown in Figure 1. (These waveforms are not to be construed as specifications but rather as a guide to proper usage of the card.)

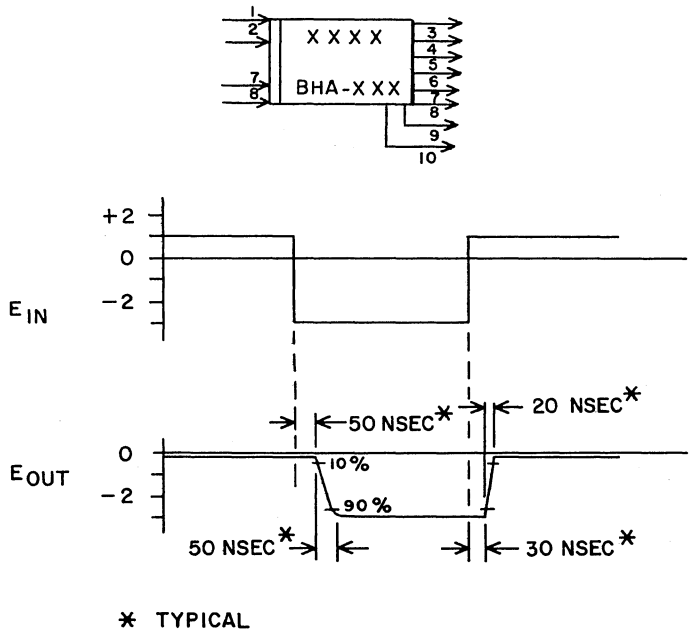
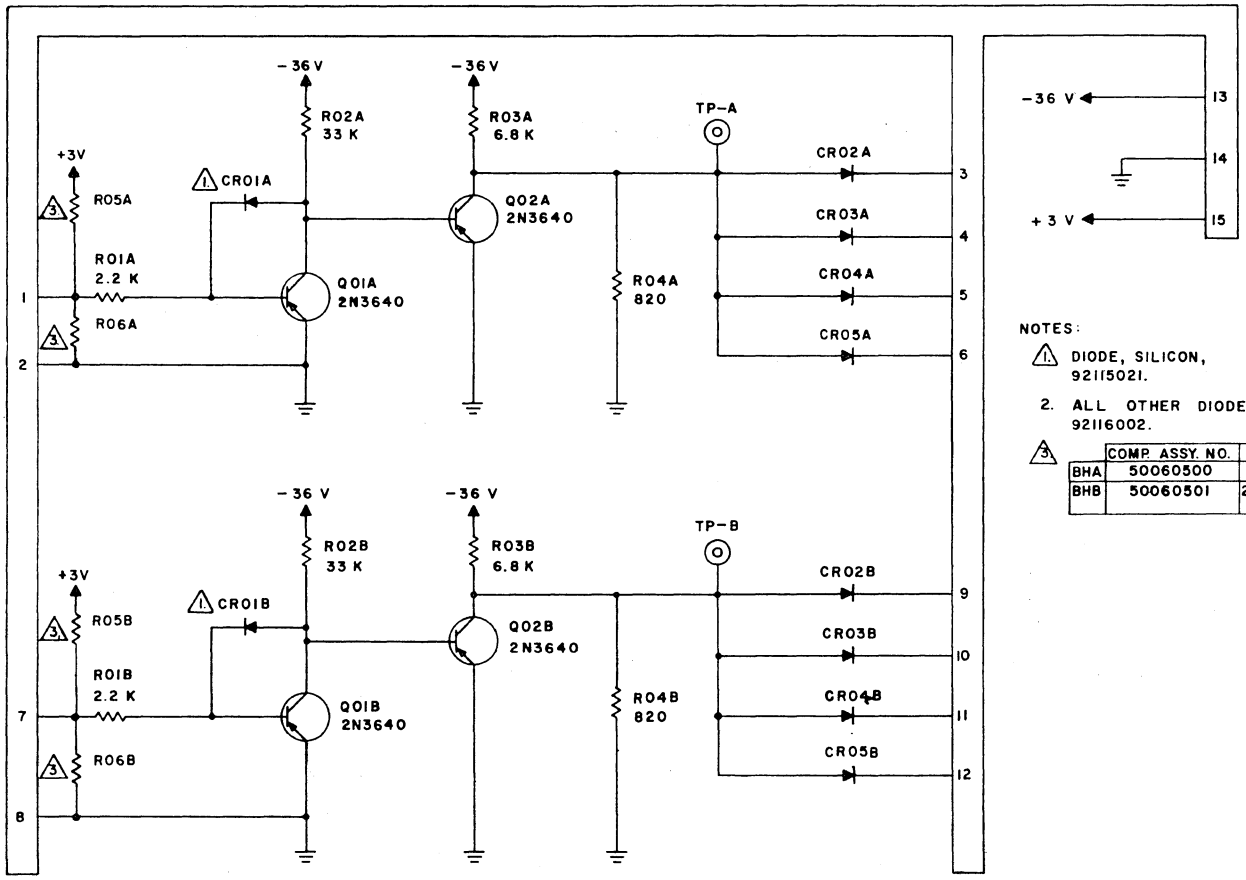


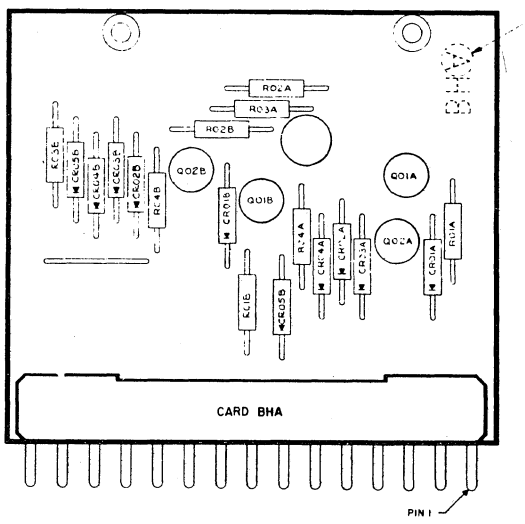

Figure 1. Input/Output Waveforms




NOTES:

1. DIODE, SILICON, 92115021.
2. ALL OTHER DIODES ARE 92116002.
3. 

| | COMP. ASSY. NO. | R05A,B | R06A,B |
|---|---|---|---|
| BHA | 50060500 | NONE | NONE |
| BHB | 50060501 | 221Ω1%, 1/2W | 162Ω1%, 1/2W |



# Q TYPE CONTROL TRANSMITTER

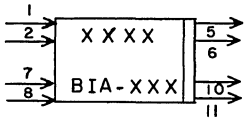
## BIA

The BIA card is designed for use with the OEM disk storage drives. Each card contains two identical transmitter circuits. The transmitters are used on the control or access lines between the disk storage drive and the controller.

The input to the card is the standard 1604-type logic levels to pins 1 and 7. A gating input is also provided on pins 2 and 8. Outputs are taken from pins 5 and 10 and normally go to a twisted-pair terminated in the equivalent of 90 ohms to +1.25v.

With a "0" input and no signals present on pins 2 and 8, Q01 is off as a result of the divider on the +6v (R02 and diodes CR02, 3 bring the base to about +1.2v). With Q01 off, its collector is a negative 4.5v. This is sufficient to keep Q02 off and the output voltage is then determined by the termination on the twisted pair line and should be +1.27v nominally.

With the input a "1", pin 1 is approximately -1.8v determined by the base-emitter junction plus the drop across CR02, 3. Transistor Q01 is thus on. The collector of Q01 is near ground so Q02 turns on because of the -3v on its emitter and R04 to ground. The base of Q02 is approximately -2.4v causing the anode of CR05 to be negative (hence this diode is off). Typical switching waveforms are shown in Figure 1. (These are to be used only as a guide and not as specifications.)



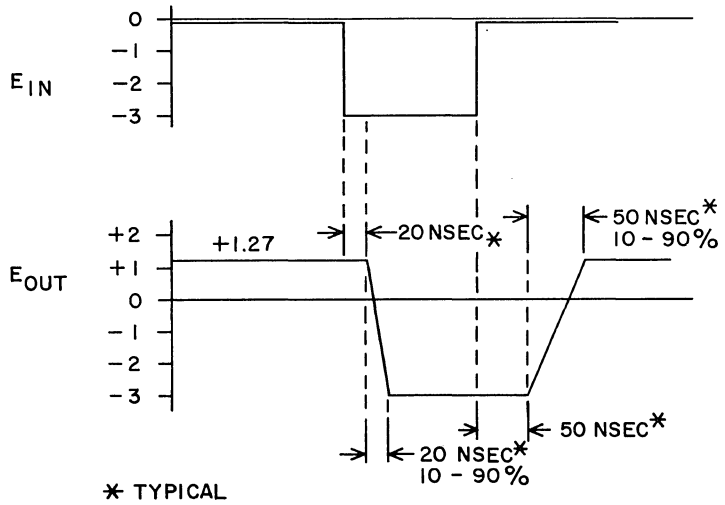
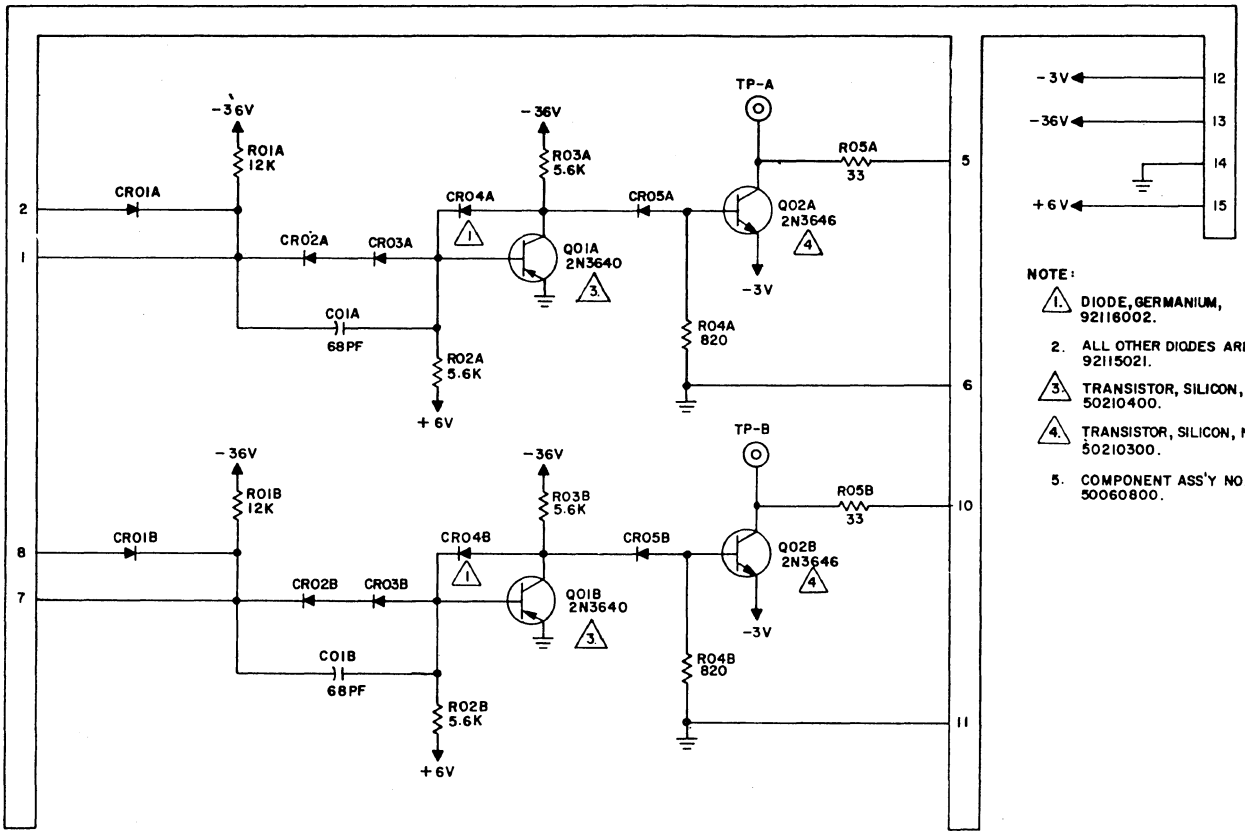
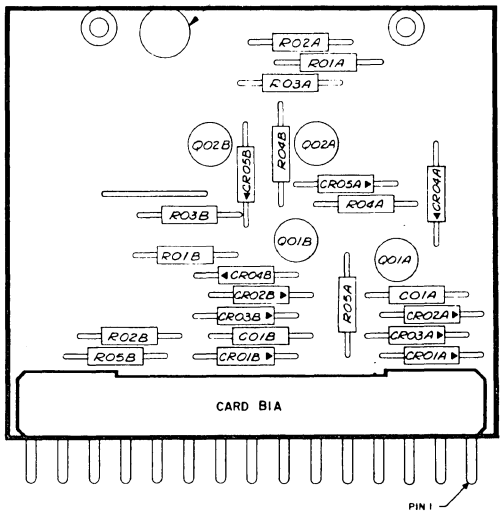




Figure 1. Typical Switching Waveforms




NOTE:

1. DIODE, GERMANIUM, 92116002.
2. ALL OTHER DIODES ARE SILICON, 92115021.
3. TRANSISTOR, SILICON, PNP, 50210400.
4. TRANSISTOR, SILICON, NPN, 50210300.
5. COMPONENT ASS'Y NO. 50060800.



## SUPPLY SENSOR AND CURRENT SINK

## BJA

The BJA card is designed for use in the OEM disk storage drive . It is used as a failure detection circuit to protect the disk storage drive from writing "garbage" by the falling write current when any of the normal power sources drop below specified limits. This card is used with the GAA or GAB cards to check the +20v supply.

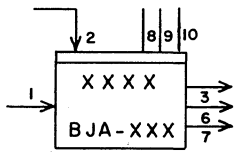
Voltage to the circuit is derived from the controller (+6v and -36v are supplied across the interface).

Normal inputs to the card are a standard 1604-type logic level on pin 1, +20v via a 12v and 5.6v zener in series to pin 2 from the GAA/B card, and -20v and +40v supplies on pins 13 and 15 respectively.

There are essentially three outputs from the card. One output is the write current sink using pins 8, 9, and 10 and will normally be at +40v on TP-C. The other outputs are standard logic levels with pin 3 at -3v and pins 6 and 7 at 0v when all inputs are normal.

Transistors Q01 and Q03 form a + AND circuit such that if Q01 and Q03 are off, Q04 is on and the normal output conditions previously mentioned exist. The input on pin 1 along with the -20v source thru CR04 to the base of Q01 forms an OR circuit such that if either pin 1 or the -20v source become abnormal, Q01 turns on. This disables the Q01, Q03 AND term and causes Q04 to turn off. This action turns on Q05 dropping any write current and changes the states of inverters Q06 and Q07 (which may be used to drive a Fault flip-flop or other detection circuits).

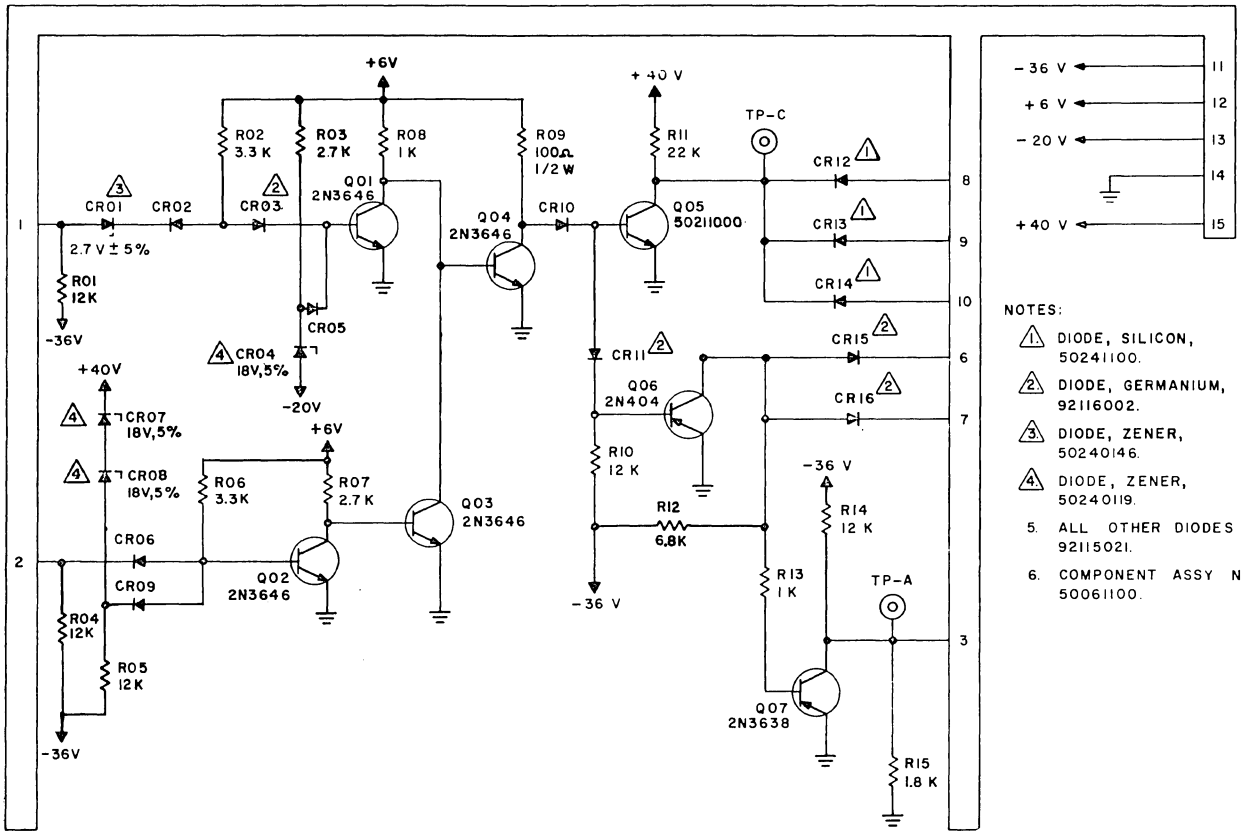
Similarily, the +20v source via zener diodes to pin 2 and the +40v circuit form an OR circuit such that if either is abnormal, Q02 turns off, turning Q03 on. This again disables the Q01, Q03 AND term and causes Q04 to turn off. As before, the outputs change state indicating a Fault condition.



Specifically, the operation of Q01 is: if the pin 1 input is a "1" (-3v) and the -20v supply is normal, the base of Q01 is negative. Since zener CR04 is at 18v, the anode of CR05 is at -2v and with pin 1 at about -3v, the anode of CR03 is approximately -0.6v due to the drops across CR01 and CR02. At the current levels in use, the zener voltage (CR01) is about 1.8v. Because the back to back diodes CR03, 5 have anode voltages of -0.6 and -2.0 respectively and the base of Q01 is approximately in the middle, the base should be about -0.8v. (This arrangement is indeterminate since it depends on leakage currents in the diodes.) If however, pin 1 goes to ground, CR01, 2 open because the junction of CR02, 3 cannot rise above approximately +0.8v due to CR03 and the base-emitter diode of Q01 which turns on. If pin 1 is at -3v again and the -20v drops to -18v or lower, CR04 stops conduction. The anode of CR05 then rises to approximately +1.2v causing Q01 to turn on.

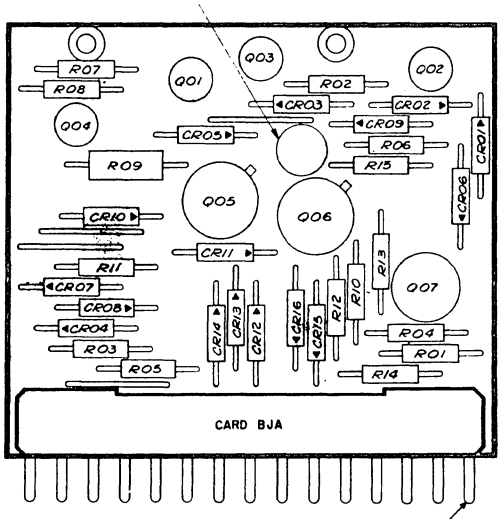
Under normal voltage conditions pin 2 of Q02 is at +2.4v and the cathode of CR09 is at +4v. Since all voltages are positive, the base will clamp to +0.6v so CR06 and 9 are back biased. With Q02 on, Q03 is off. If the +20v supply drops to +17.6v, Q02 starts to turn off because pin 2 goes to 0v and CR06 begins to rob base current from Q02. If the +20v supply drops another 0.6v, Q02 turns off completely and Q03 comes on.

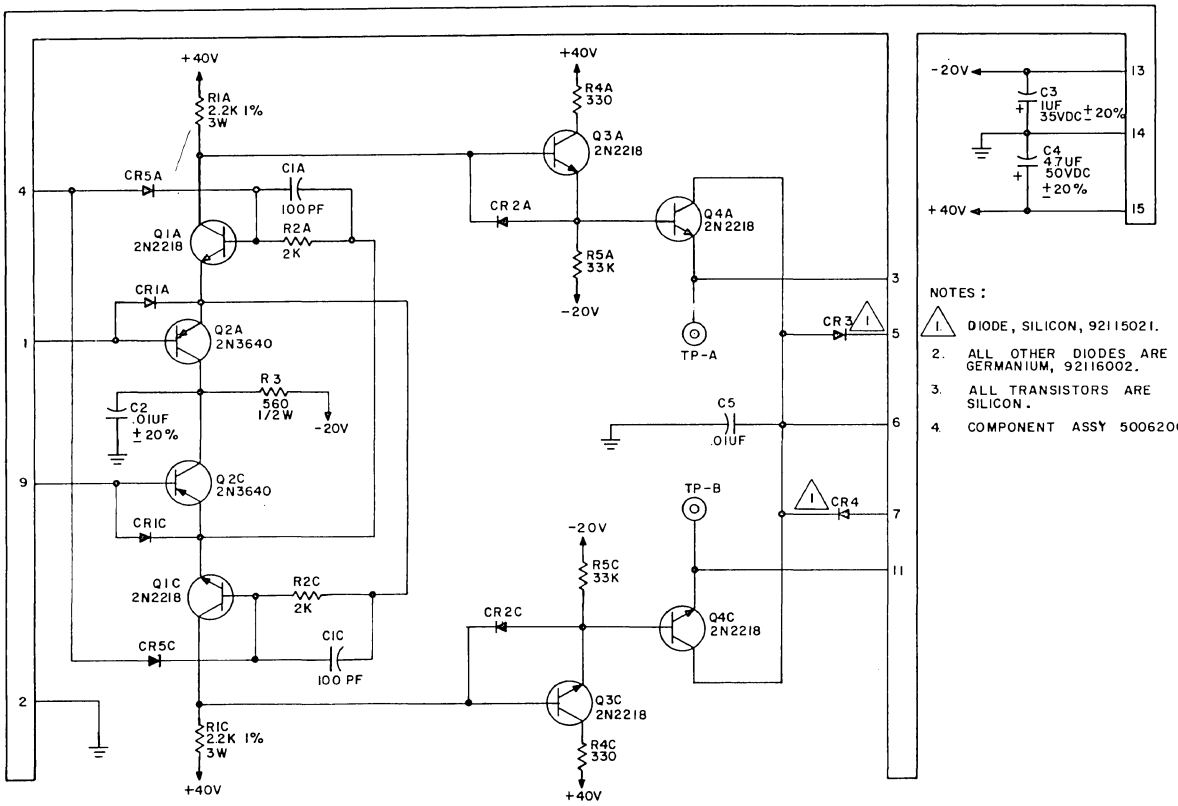
If pin 2 is at normal voltage and the +40v drops to +36v, the cathode of CR09 will be at 0v so CR09 begins to rob Q02 of base current. An additional few tenths of a volt drop in the +40v supply causes Q02 to turn off and Q03 to turn on.




NOTES:

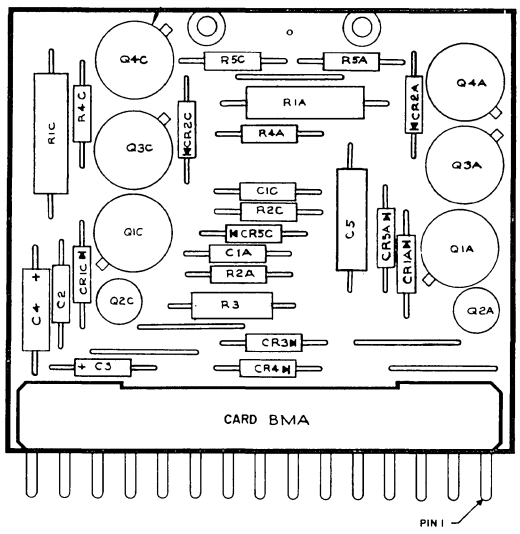
1. DIODE, SILICON, 50241100.
2. DIODE, GERMANIUM, 92116002.
3. DIODE, ZENER, 50240146.
4. DIODE, ZENER, 50240119.
5. ALL OTHER DIODES ARE 92115021.
6. COMPONENT ASSY NO. 50061100.






NOTES :

1. DIODE, SILICON, 92115021.
2. ALL OTHER DIODES ARE GERMANIUM, 92116002.
3. ALL TRANSISTORS ARE SILICON.
4. COMPONENT ASSY 50062000.

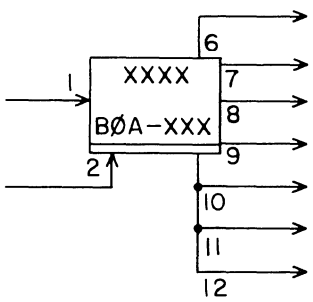


# VOLTAGE CHECKER

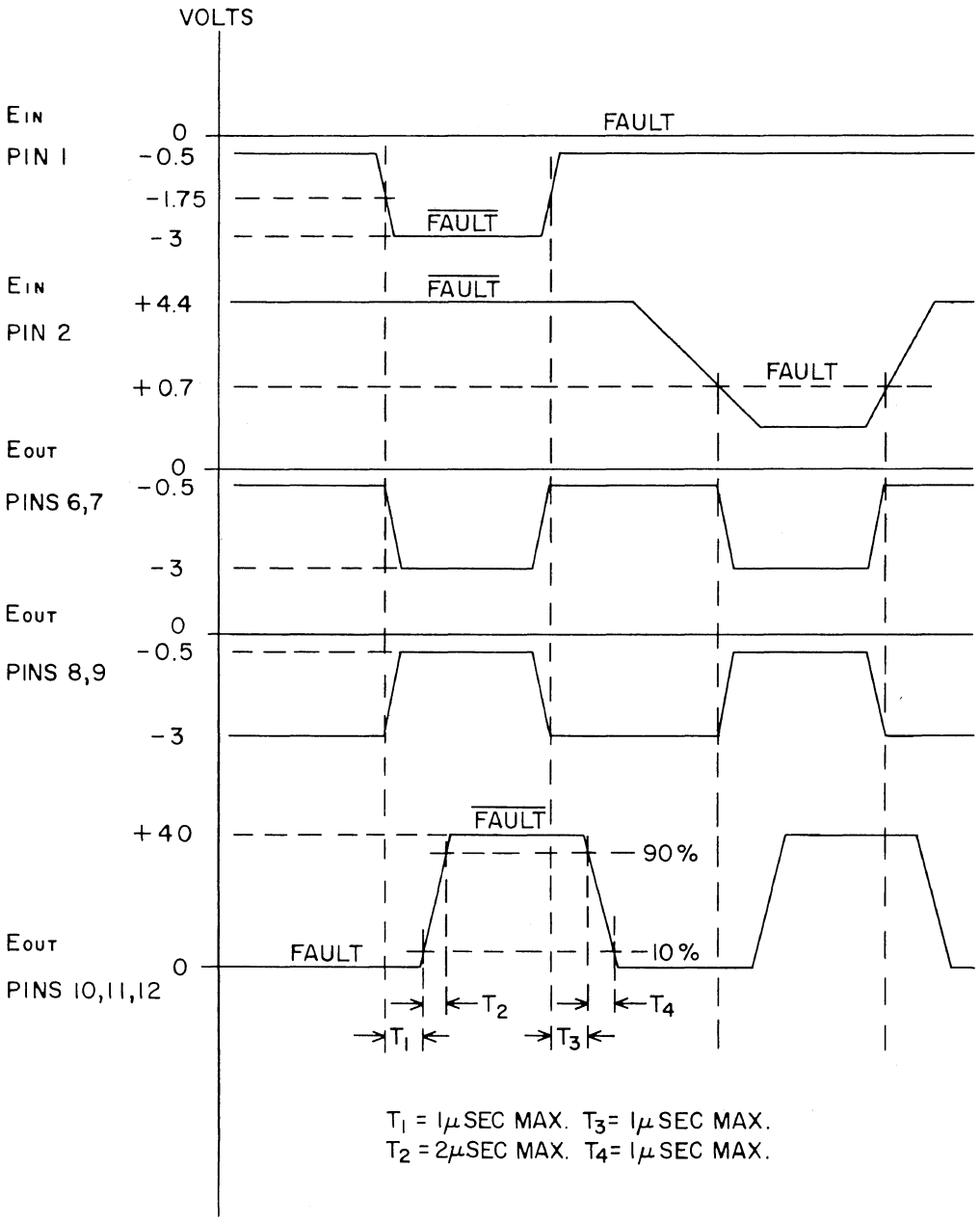
## BOA

This card prevents write and erase currents from reaching write and erase heads when one of the following fault conditions occurs: 1) the +20v power supply (provided by either the GAD or GAE card) drops below +16.3v; 2) the -20v power supply is closer to ground than -16.1v; or 3) an external logic signal on pin 1 goes to a logic "0" (-0.5v). If one of these faults exists, the output at pins 10, 11, and 12 will be at ground level and no current will flow through the write and erase heads. Output pins 6 and 7 will then provide a logic "0", and output pins 8 and 9 a logic "1" (-3.0v).

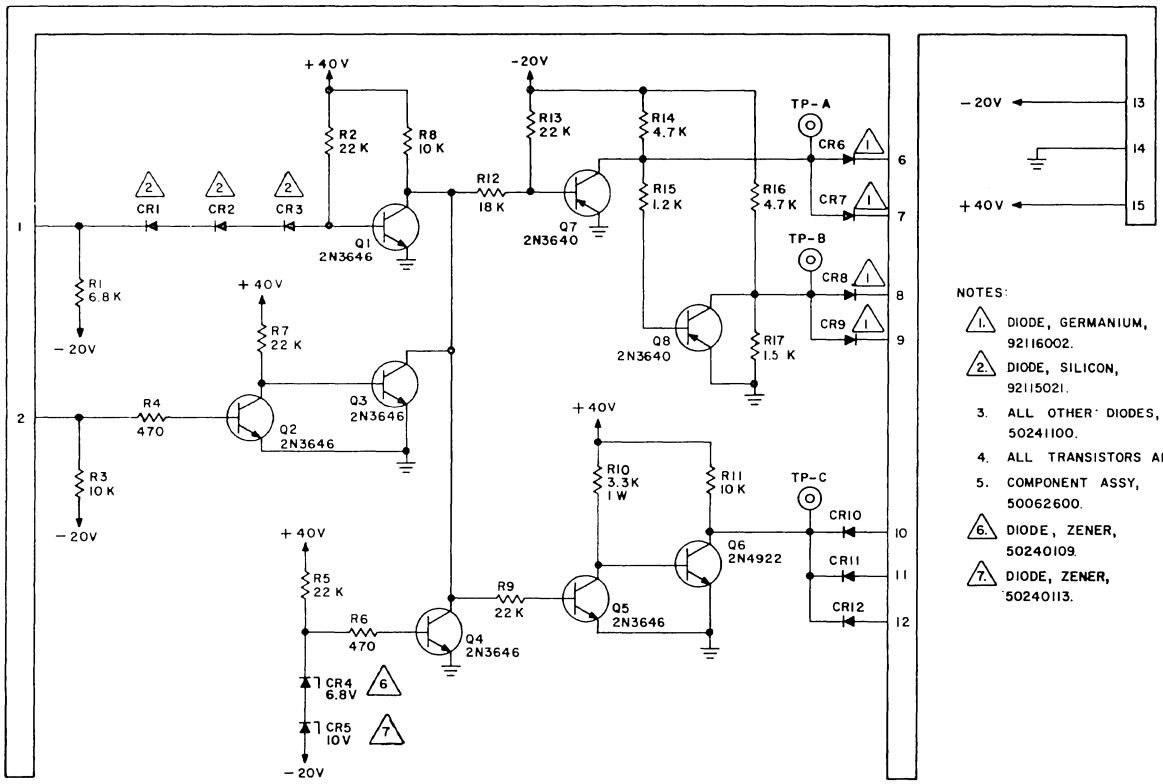
Each of the three fault conditions is sensed by a particular circuit on the BOA card. If the voltage at pin 1 goes to a logic "0", Q1 turns on. This turns off Q5, which turns on Q6 and forces TP-C toward ground level. Transistor Q6 absorbs up to 300 ma. Diodes CR10, CR11, and CR12 isolate the write and erase heads when the BOA card is off (logic "1" at pin 1). Pin 2 senses the state of the +20v power supply through a 10v and a 5.6v zener diode on either the GAD or the GAE card. If the voltage drops to +16.3v ($\pm$0.9), Q2 turns off and Q3 turns on. This will have the same effect as turning on Q1. When the state of the -20v power supply is -16.1v ($\pm$0.9), Q4 turns on, which will have the same effect as turning on Q1. When more than one of these three sensing circuits responds at the same time, the result is as though only one circuit were active.



WAVEFORMS:

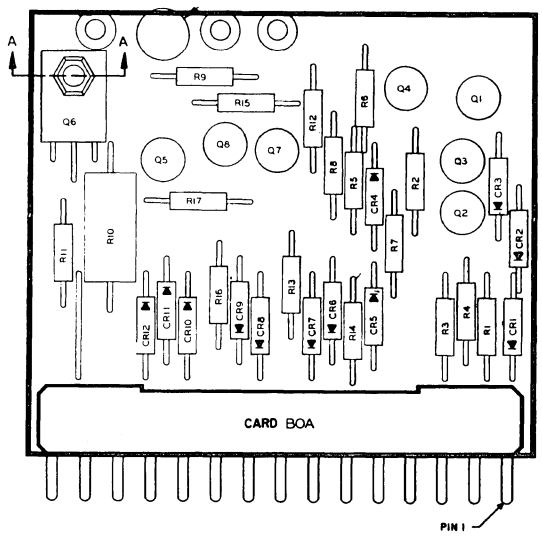



$T_1$ = 1μSEC MAX. $T_3$= 1μSEC MAX.
$T_2$ = 2μSEC MAX. $T_4$= 1μSEC MAX.




NOTES:

1. DIODE, GERMANIUM, 92116002.
2. DIODE, SILICON, 92115021.
3. ALL OTHER DIODES, SILICON, 50241100.
4. ALL TRANSISTORS ARE SILICON.
5. COMPONENT ASSY, 50062600.
6. DIODE, ZENER, 50240109.
7. DIODE, ZENER, 50240113.

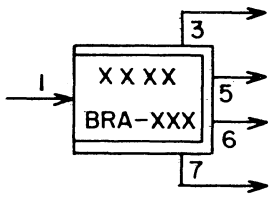


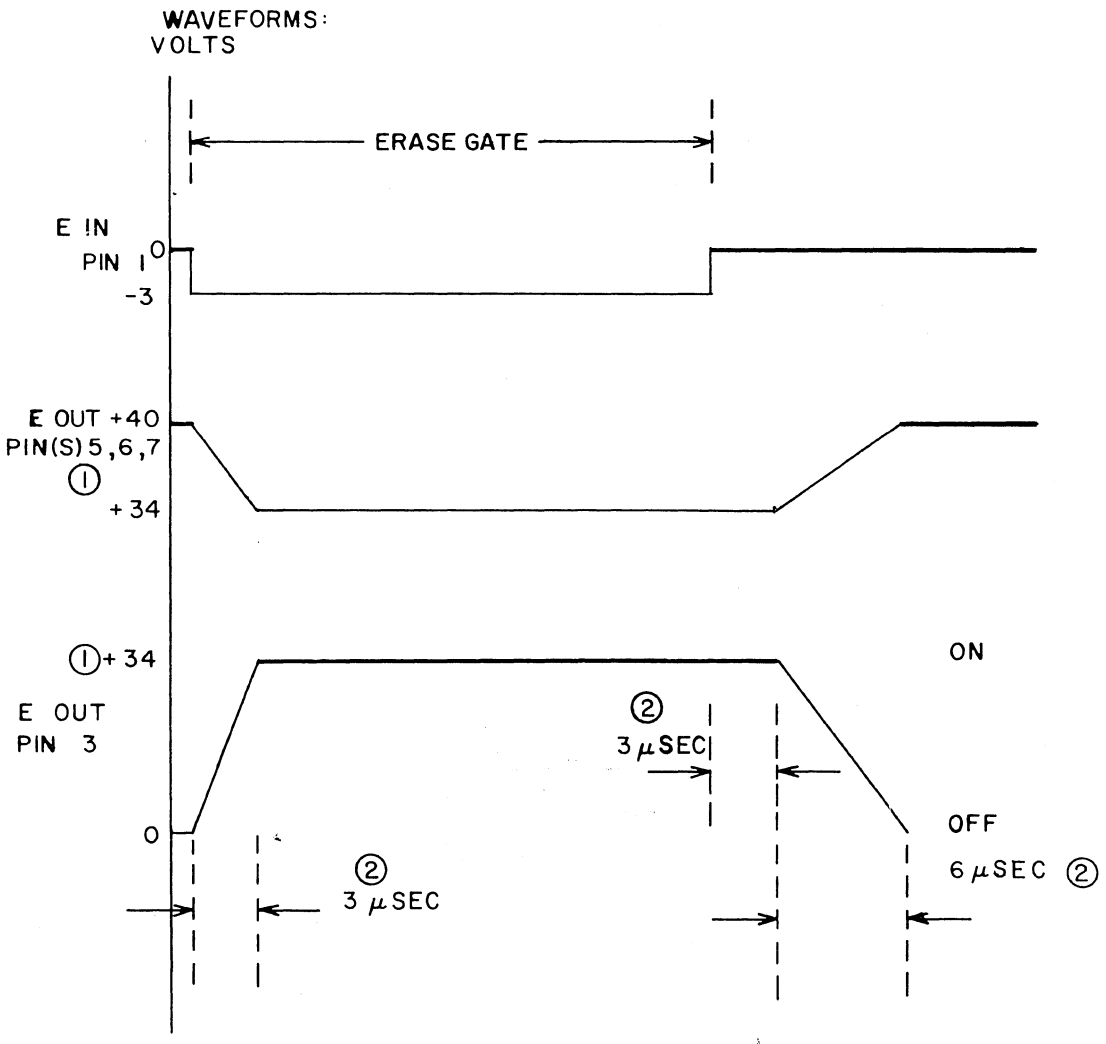
ERASE DRIVER

BRA

This card controls the rise and fall time of the erase current. It is similar to the AMK write/erase driver. Both cards have the same limiting resistors in the output stage for use with the AND-type error checking system; however, the BRA does not include the large capacitance across the resistor for delay during switching. (See the AND circuit description.) The maximum erase current available is 250 ma. The current rise time is approximately 3 usec and fall time is approximately 6 usec.

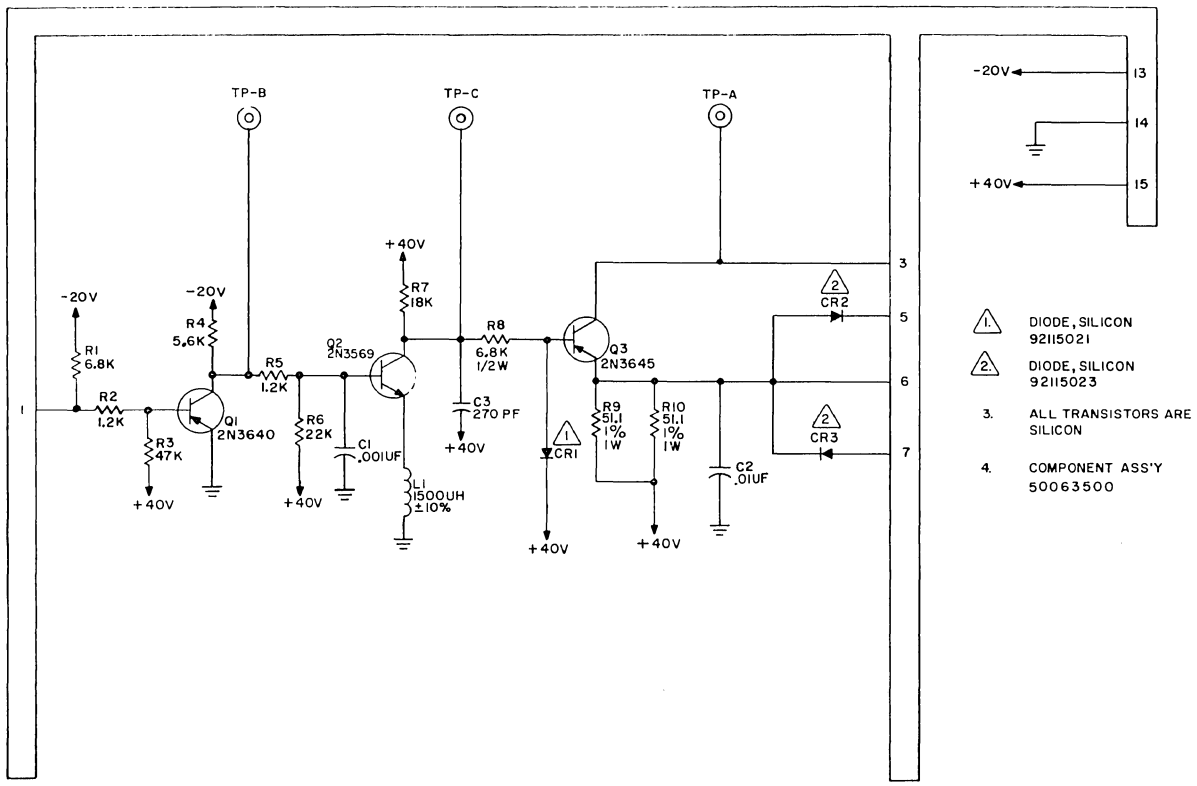
The BRA card is turned on with a logic "1" (-3v) at the input. The combination of L1 and C1 provides a slow, controlled turn-on of Q2. This results in a rise at the output from 0v to 34v in 3 usec, approximating a linear ramp. The capacitor (C3) at the collector of Q2 restricts the fall time at the output by causing a delay of 3 usec and a fall time of 6 usec. Diodes at pins 5 and 7 are for use with the AND error checking scheme.

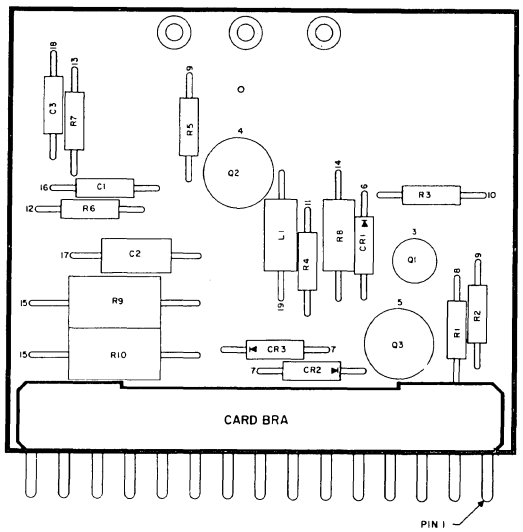





① ACTUAL VOLTAGE DEPENDS ON MAGNITUDE OF ERASE CURRENT.

② APPROXIMATE.


TP-B
TP-C
TP-A
-20V
13
14
+40V
15
-20V
R1
6.8K
R2
1.2K
R3
47K
+40V
-20V
R4
5.6K
Q1
2N3640
R5
1.2K
R6
22K
C1
.001UF
+40V
Q2
2N3569
+40V
R7
18K
L1
1500UH
±10%
R8
6.8K
1/2W
C3
270 PF
+40V
CR1
+40V
Q3
2N3645
R9
51.1
1%
1W
R10
51.1
1%
1W
+40V
C2
.01UF
2
CR2
2
CR3
3
5
6
7
1
2
3
4.
DIODE, SILICON
92115021
DIODE, SILICON
92115023
ALL TRANSISTORS ARE
SILICON
COMPONENT ASS'Y
50063500


C3
R7
R5
Q2
C1
R6
L1
R4
R8
CR1
R3
Q1
C2
R9
R10
CR3
CR2
Q3
R1
R2
CARD BRA
PIN 1

# CURRENT CONTROLLED LAMP DRIVERS
## BTA, BUA

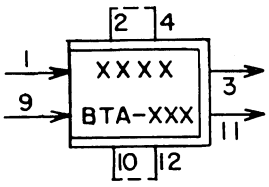
The BTA and BUA cards furnish one or two grounded lamps with +20v and -20v respectively. Both cards include in their circuitry a constant current source which eliminates turn-on current surges. With either card driving the intended lamp (P/N 92629003; rated at 24v, 73ma), a logic "1" (-3.0v) turns it on and a logic "0" (-0.5v) turns it off. All input circuits on both cards have inverting stages for matching the 1604 logic levels.

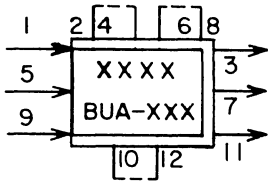
### BTA

There are two identical circuits on this card. With a logic "0" at the input (pin 1 or 9), transistor Q1 turns off. At the same time, transistors Q2 and Q3 will be on, shorting the current source base (Q4) to +20v. As a result, Q4 will turn off, preventing current from flowing through the load. A logic "1" input pulls the Q1 collector to ground, turning off both Q2 and Q3. The zener (CR1) voltage now rests at approximately +2.3v with the current levels being used. Transistor Q4 turns on and 1.5v registers across emitter resistor R8, (or R8 and R9). The output voltage (pin 3 or 11) to the lamps is +18.5v. The maximum current (60ma) from any one output can be doubled by paralleling the emitter resistors R8 and R9 (jumpering pins 2 & 4 or 10 & 12).

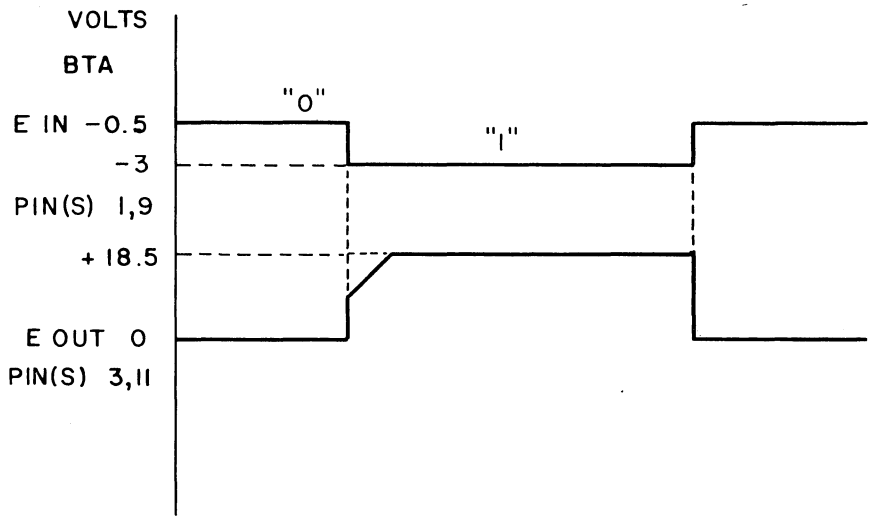
### BUA

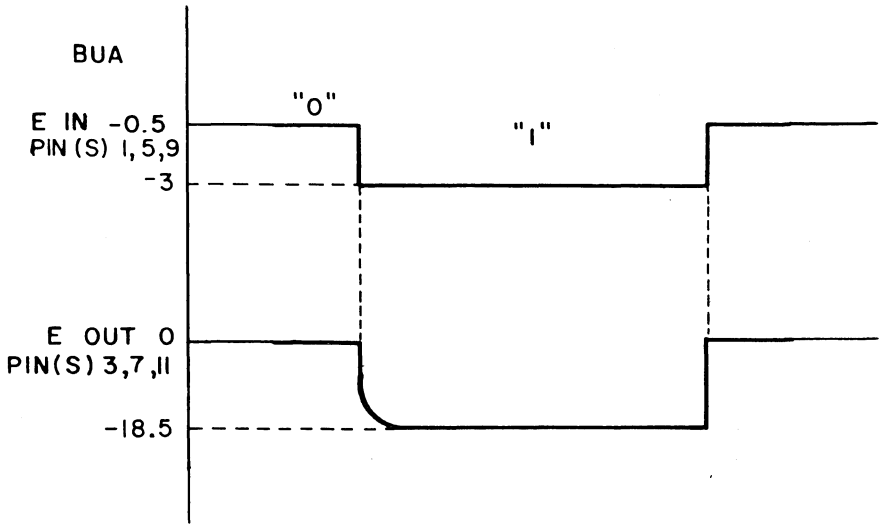
This card has three identical circuits. A logic "0" at the input (pin 1, 5, or 9) turns off transistor Q1. This prevents base current from reaching Q2, and in turn, from flowing through the load. In contrast, a logic "1" input pulls the Q1 collector to ground. The zener (CR1) voltage now rests at approximately -2.3v with the current levels being used. Transistor Q2 turns on and 1.5v appears across the emitter resistor R6, (or R6 and R7). The output voltage (pin 3, 7, or 11) to the lamps is -18.5v. The maximum current (60ma) from any one output can be doubled by paralleling the emitter resistors R6 and R7 (jumpering pins 2 and 4, 6 and 8, or 10 and 12).

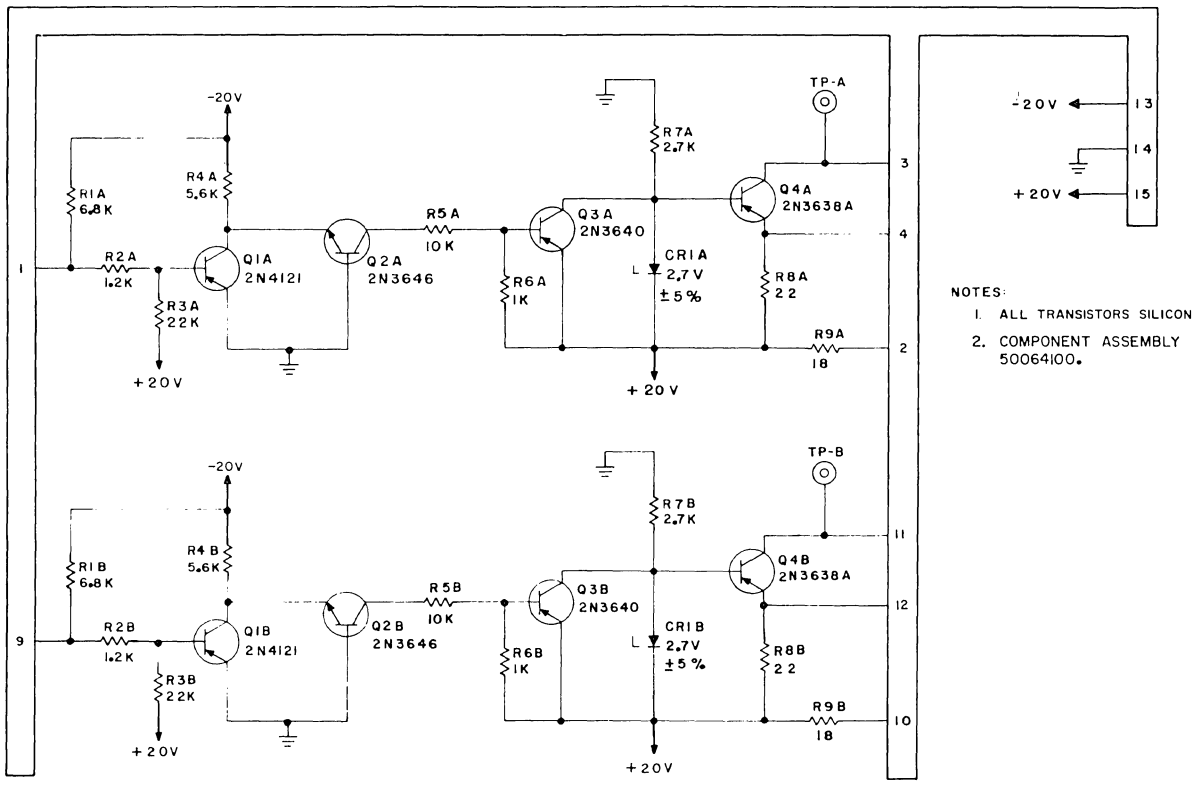

2
4
1
XXXX
9
BTA-XXX
3
11
10
12


1
2
4
6
8
5
XXXX
3
9
BUA-XXX
7
10
12
11

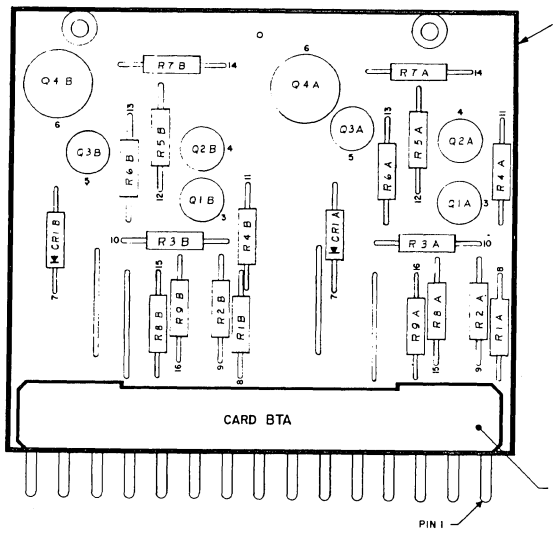
WAVEFORMS:

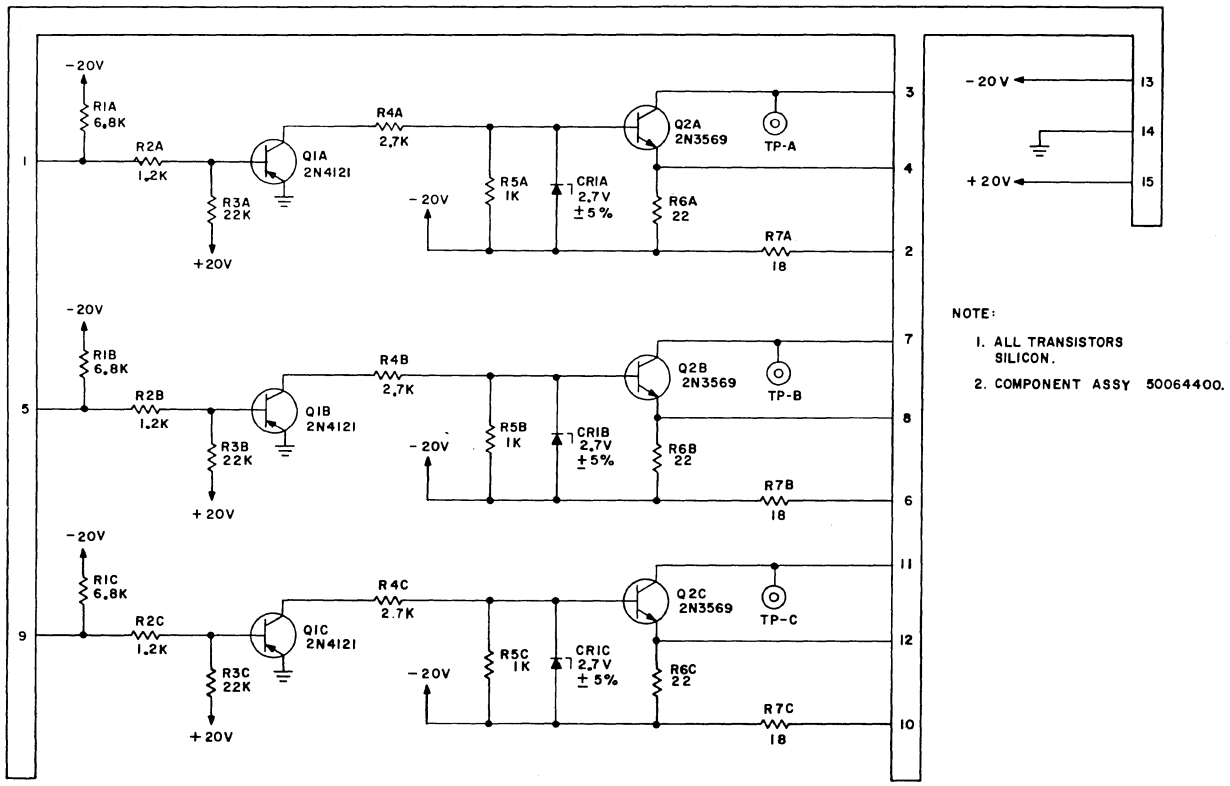

VOLTS
BTA
"0"
E IN -0.5
"1"
-3
PIN(S) 1,9
+18.5
E OUT 0
PIN(S) 3,11


BUA
"0"
E IN -0.5
PIN (S) 1,5,9
"1"
-3
E OUT 0
PIN(S) 3,7,11
-18.5


-20V
R1A 6.8K
R4A 5.6K
R2A 1.2K
R3A 22K
Q1A 2N4121
Q2A 2N3646
R5A 10K
Q3A 2N3640
R6A 1K
R7A 2.7K
CR1A 2.7V ±5%
Q4A 2N3638A
R8A 22
R9A 18
TP-A
+20V
R1B 6.8K
R4B 5.6K
R2B 1.2K
R3B 22K
Q1B 2N4121
Q2B 2N3646
R5B 10K
Q3B 2N3640
R6B 1K
R7B 2.7K
CR1B 2.7V ±5%
Q4B 2N3638A
R8B 22
R9B 18
TP-B
1
2
3
4
9
10
11
12
13
14
15
NOTES:
1. ALL TRANSISTORS SILICON
2. COMPONENT ASSEMBLY 50064100.

BTA

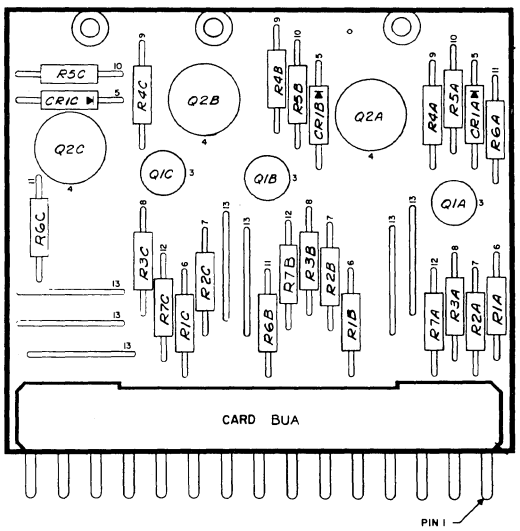

Q4B
Q3B
Q1B
Q2B
Q4A
Q3A
Q2A
Q1A
R7B
R7A
R5B
R5A
R6B
R6A
R4B
R4A
R3B
R3A
CR1B
CR1A
R8B
R9B
R2B
R1B
R9A
R8A
R2A
R1A
CARD BTA
PIN 1




NOTE:

1. ALL TRANSISTORS SILICON.
2. COMPONENT ASSY 50064400.

BUA



# READ LEVEL DETECTOR
## EDA

The read level detector is used in the read data circuit to amplify, rectify, and detect NRZ1 information on magnetic tape. Three outputs are provided:

1) A class A low impedance output which provides a gain of 125. Gai may be increased to 190 by means of an external jumper from groun to pin 3.
2) A rectified signal derived from the class A signal which exceeds threshold of 2 volts peak-to-peak. The rectified signal is increased by a factor of 2 from the class A signal for portions in excess of the threshold point. (The threshold may be reduced to 1.1v by means of an external jumper from ground to pin 7.)
3) A "1" output provided by a switching circuit operating from the threshold point when the peak-to-peak threshold is exceeded.

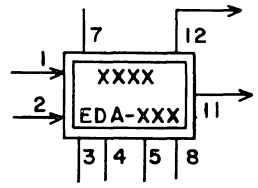
The class A amplifier incorporates a transformer input to minimize common mode signal interference. The amplifier contains one stage of volt age gain (Q01) and two stages of current gain (Q02 and Q03). A positive feedback loop is provided within the amplifier by C02 and R07. This loop returns a signal to the junction of R06 and R07 which approaches, but never exceeds, the signal at the collector of Q01. Thus, R06 presents a very high impedance in the collector load of Q01 and increases the a-c voltage gain of Q01 from a value of less than 100 to over 1000. Gain is stabilize by the negative feedback network composed of R04 and R03 which is used as a reference point for the input transformer secondary. Note that R02 may be connected externally in parallel with R03.

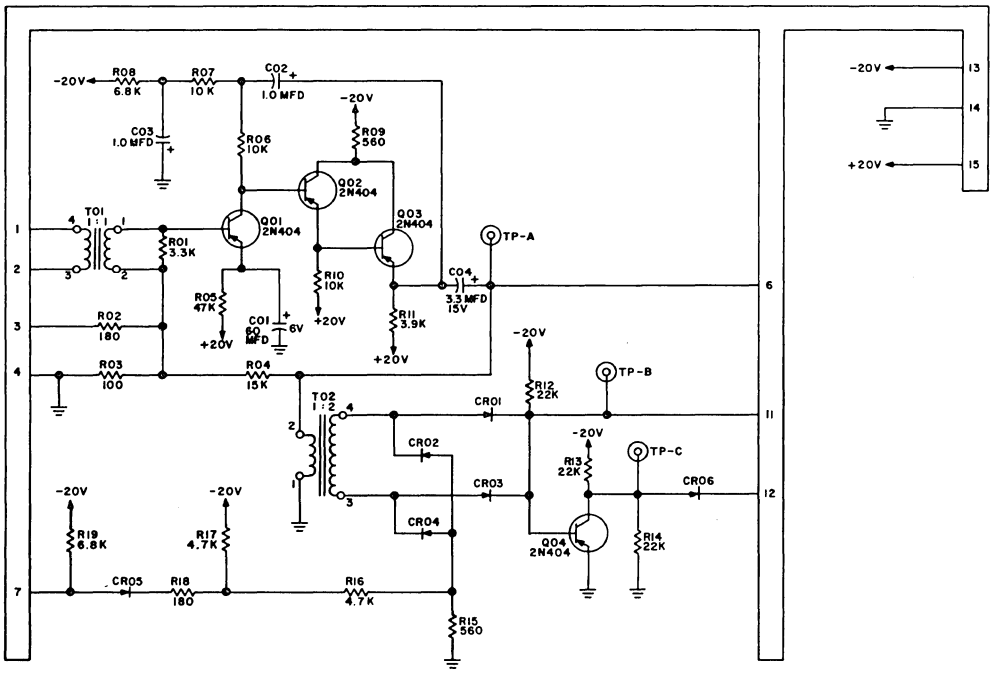
The rectifying circuit is composed of transformer T02 and diodes CR01 through CR04. The threshold at which detection takes place is determined by R15, R16, and R17 when the input to pin 7 is -12v. If pin 7 is jumpere to ground, R18 essentially parallels R15 and R16. Resistor R19 acts as a normal input load and diode CR05 provides isolation from other circuits operating in parallel.

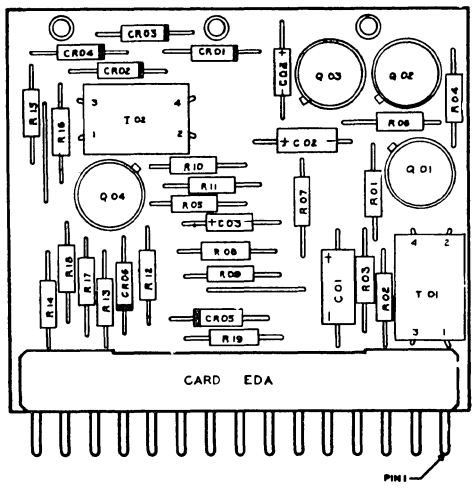
The switching circuit is composed of Q04 which turns off when the rectifier circuit reaches the threshold point. This "1" output may be use directly as a level detection point or as part of an AND term with the pea

detector output.

SYMBOL

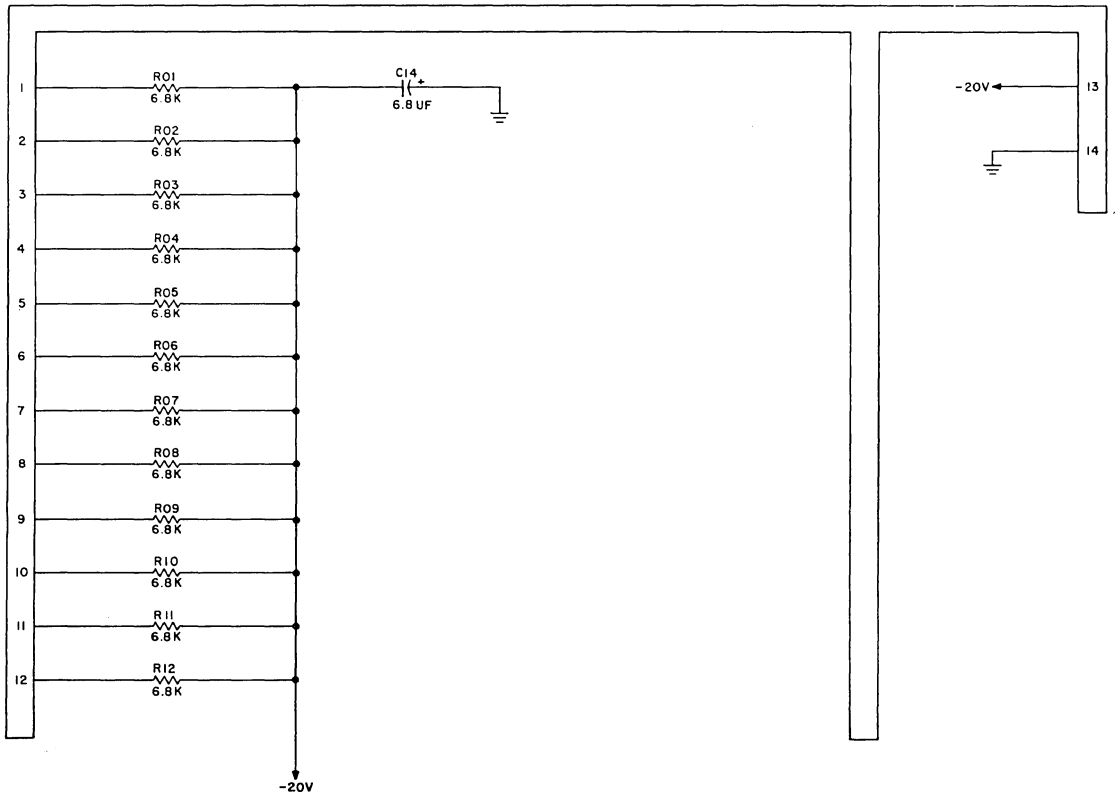


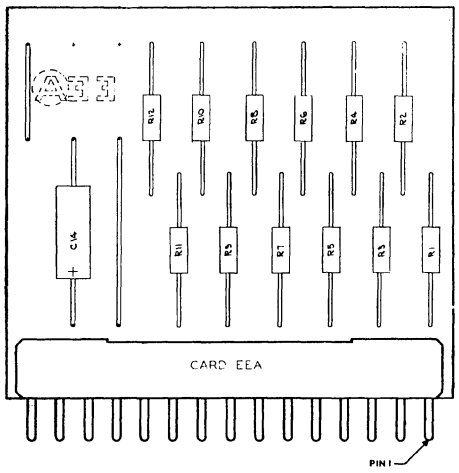



# RESISTOR TERMINATION

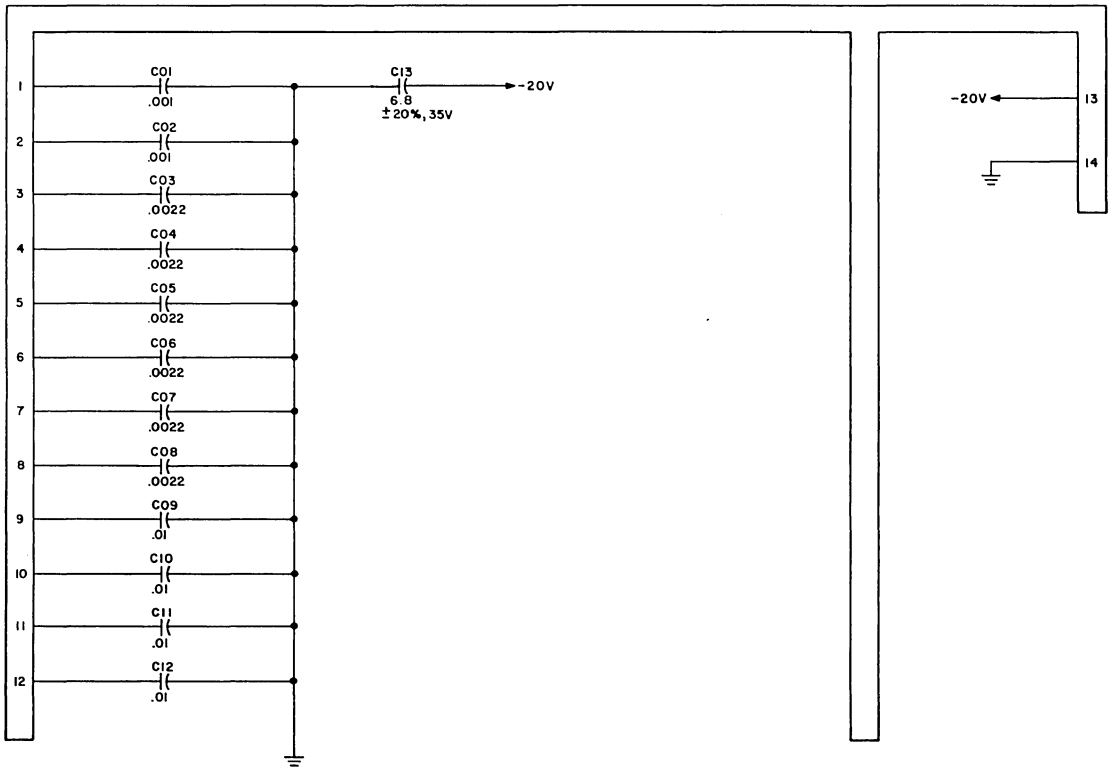
## EEA

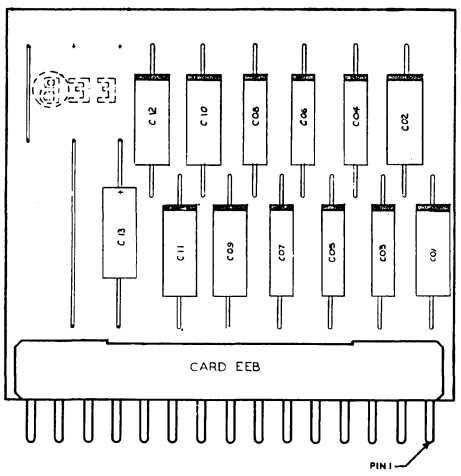


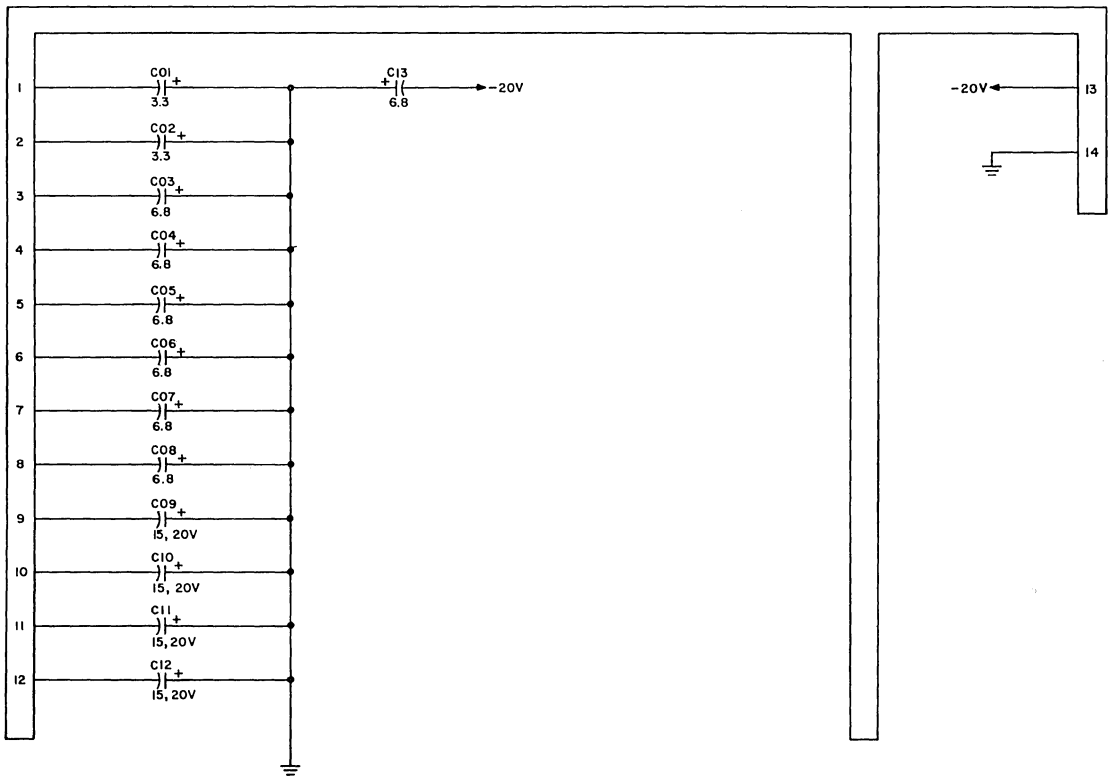
# CAPACITOR TERMINATION

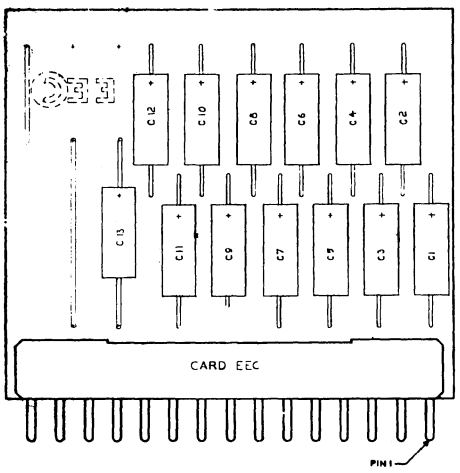
## EEB



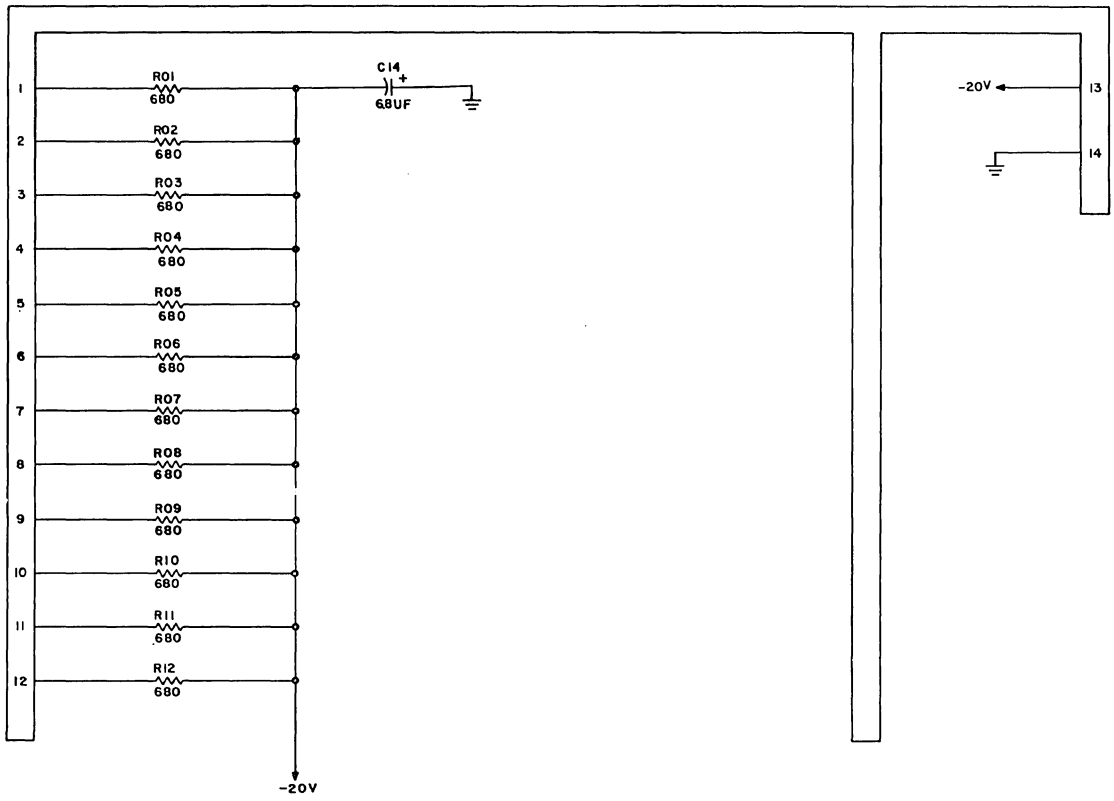



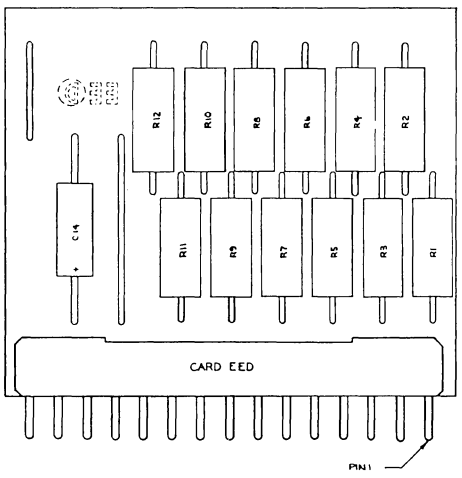
# CAPACITOR TERMINATION
# EEC



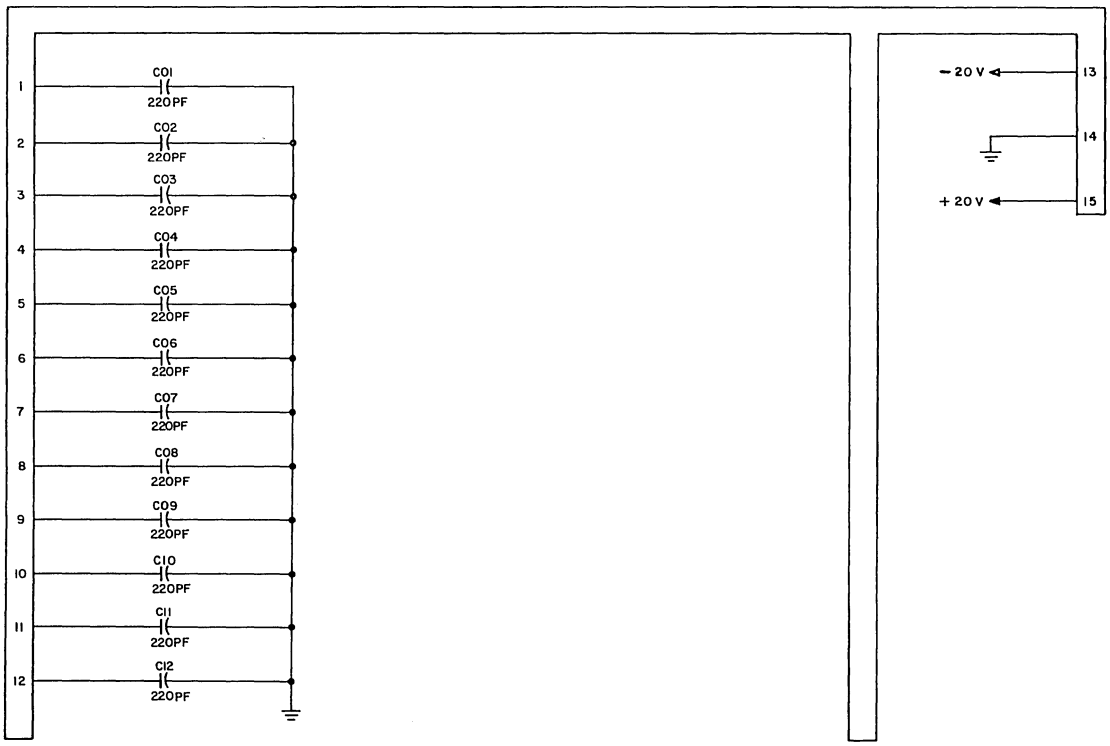



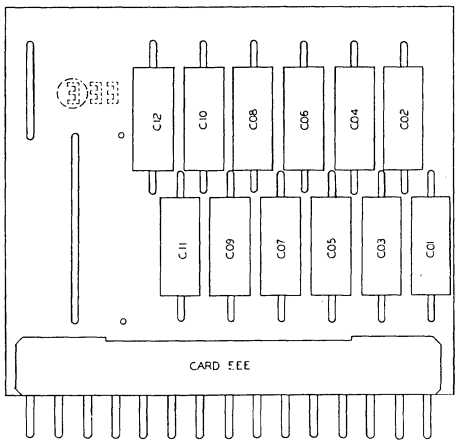
# RESISTOR TERMINATION
## EED



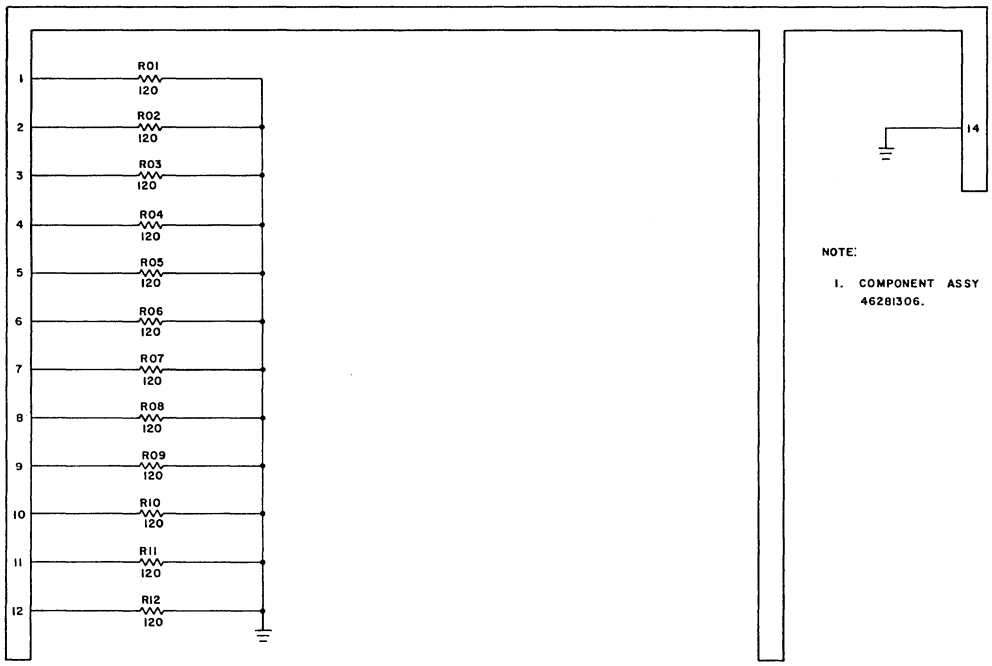



# CAPACITOR TERMINATION
# EEE



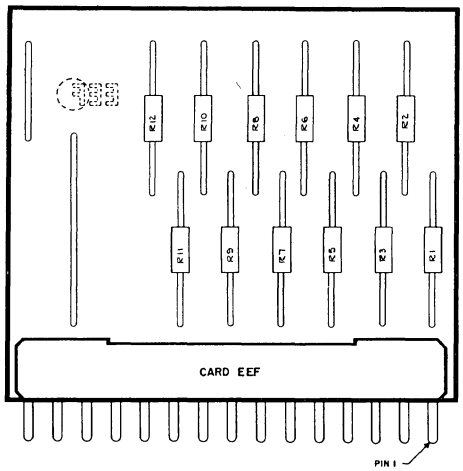



# RESISTOR TERMINATION
# EEF



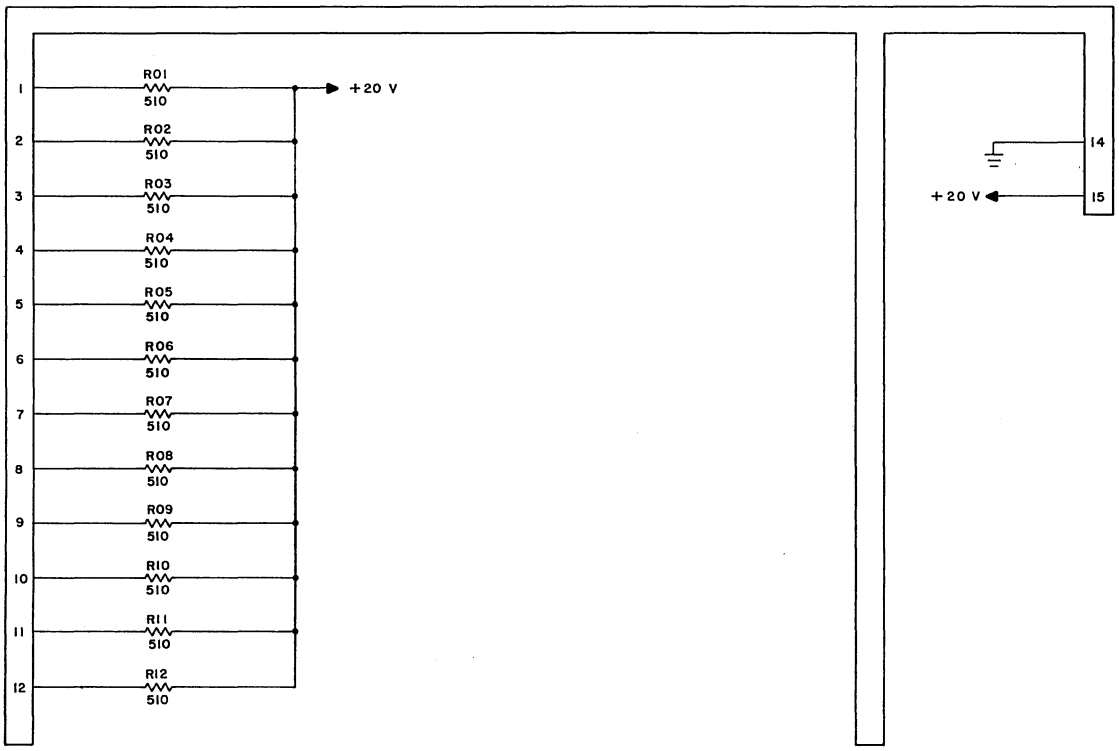

NOTE:

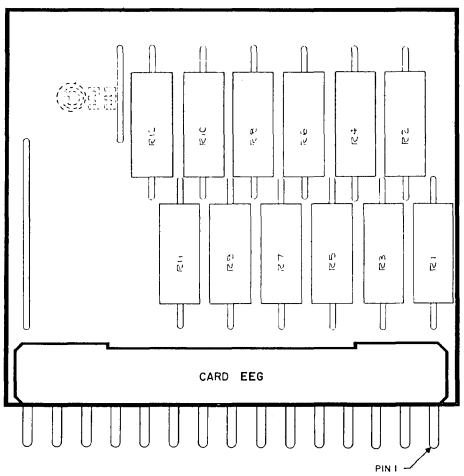
1. COMPONENT ASSY NO. 46281306.



# RESISTOR TERMINATION

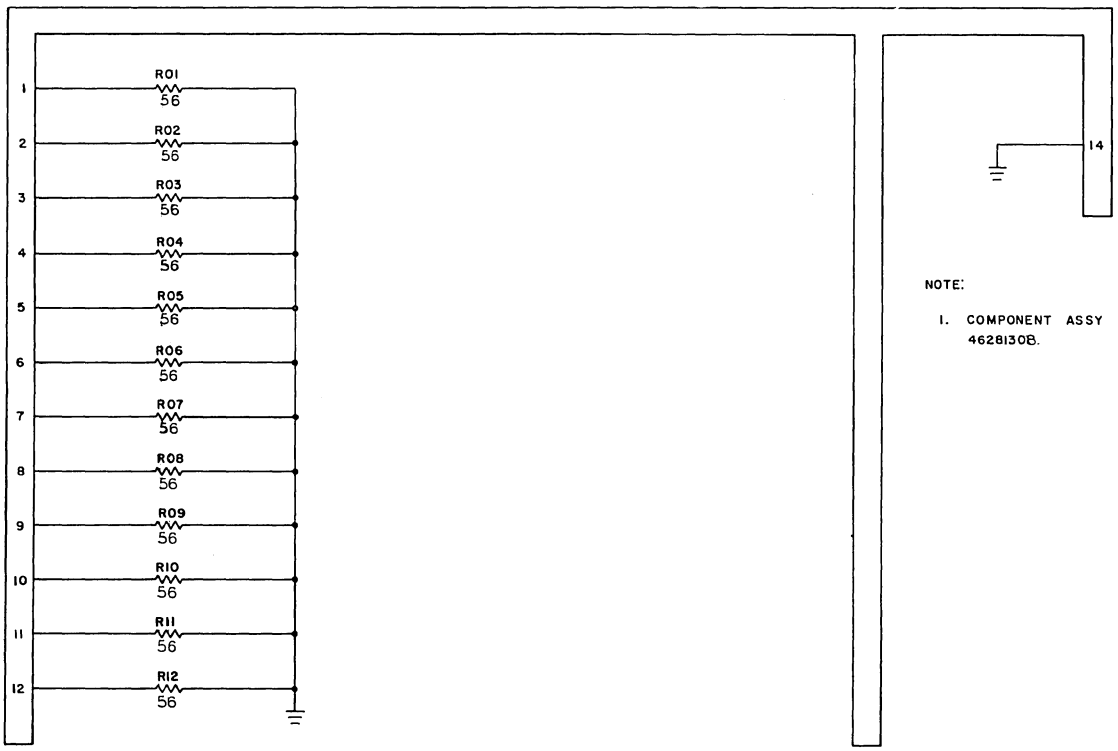
## EEG



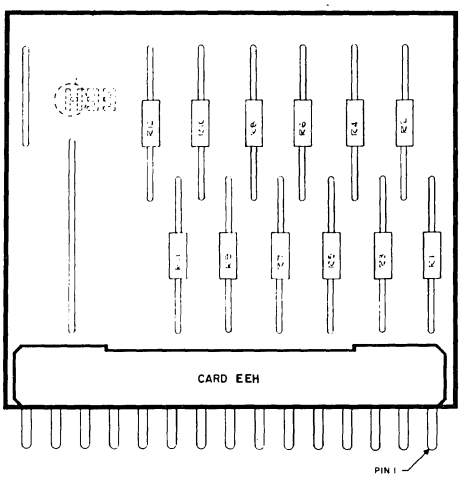
# RESISTOR TERMINATION

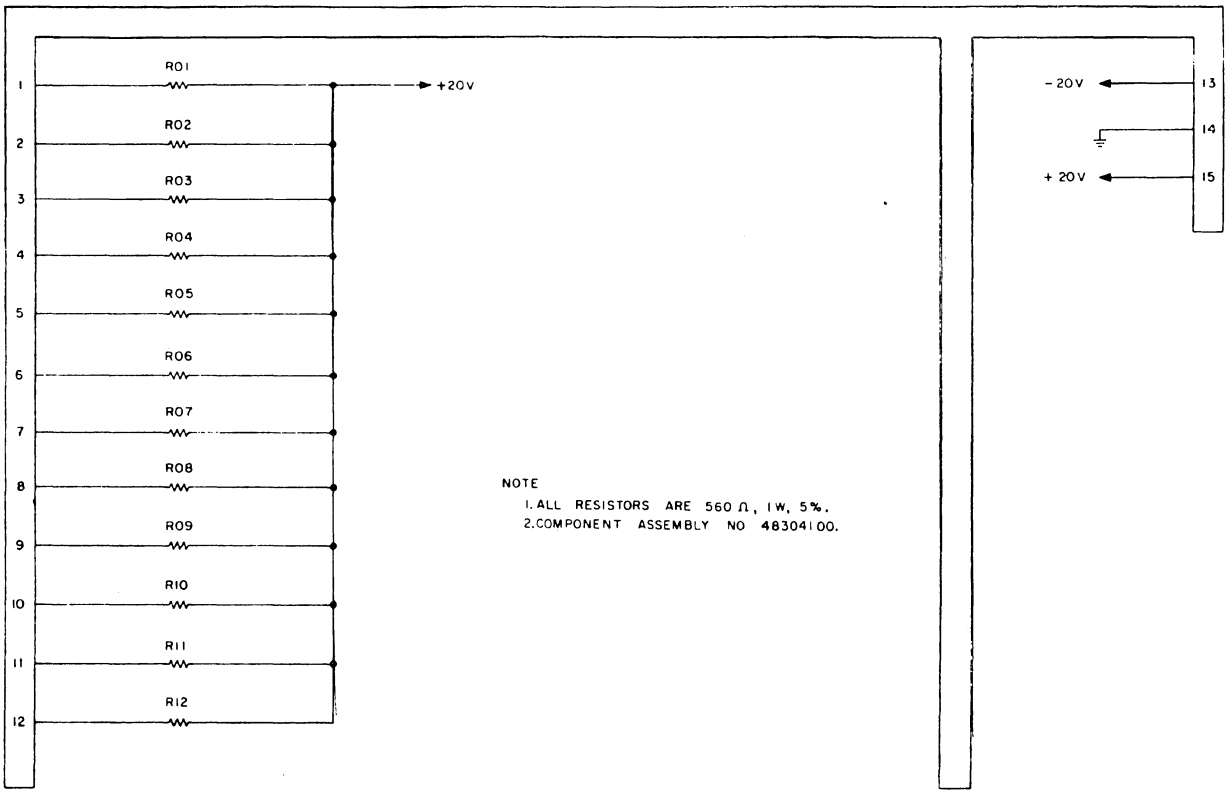
## EEH



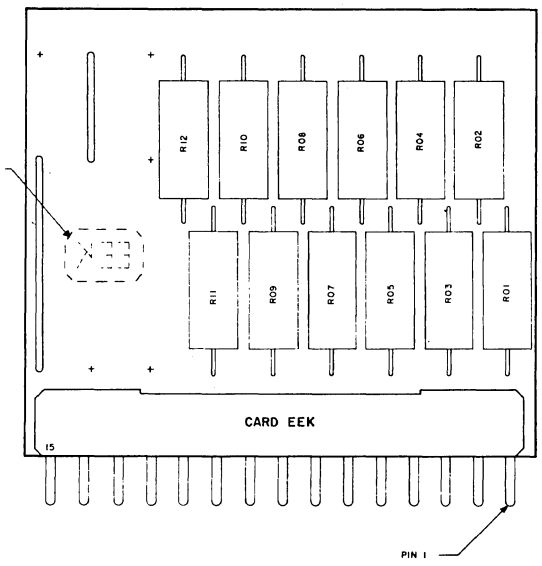

NOTE:

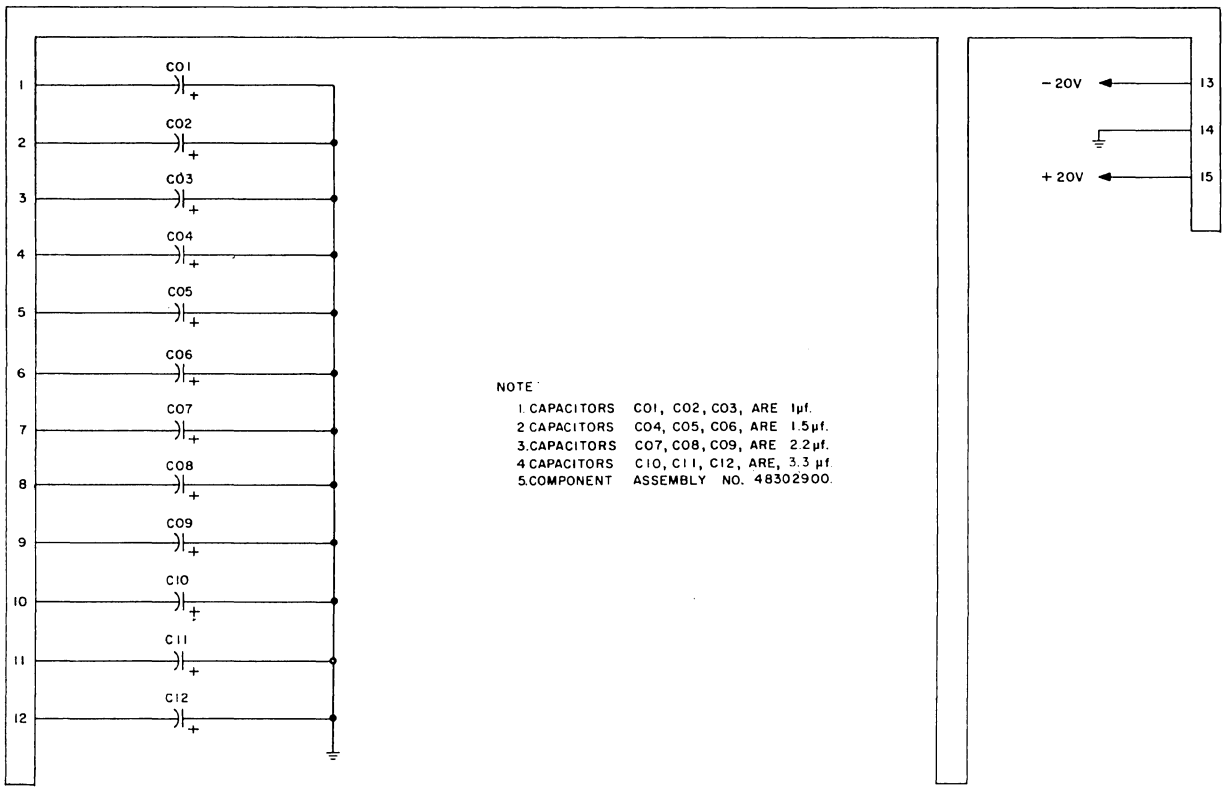
1. COMPONENT ASSY NO. 4628130B.




R01
R02
R03
R04
R05
R06
R07
R08
R09
R10
R11
R12
1
2
3
4
5
6
7
8
9
10
11
12
+20V
-20V
+ 20V
13
14
15
NOTE
1. ALL RESISTORS ARE 560 Ω, 1W, 5%.
2. COMPONENT ASSEMBLY NO 48304100.

EEK

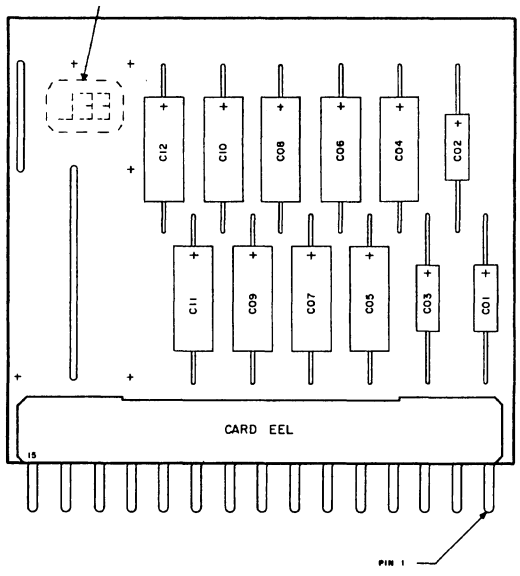

R12
R10
R08
R06
R04
R02
R11
R09
R07
R05
R03
R01
CARD EEK
15
PIN 1

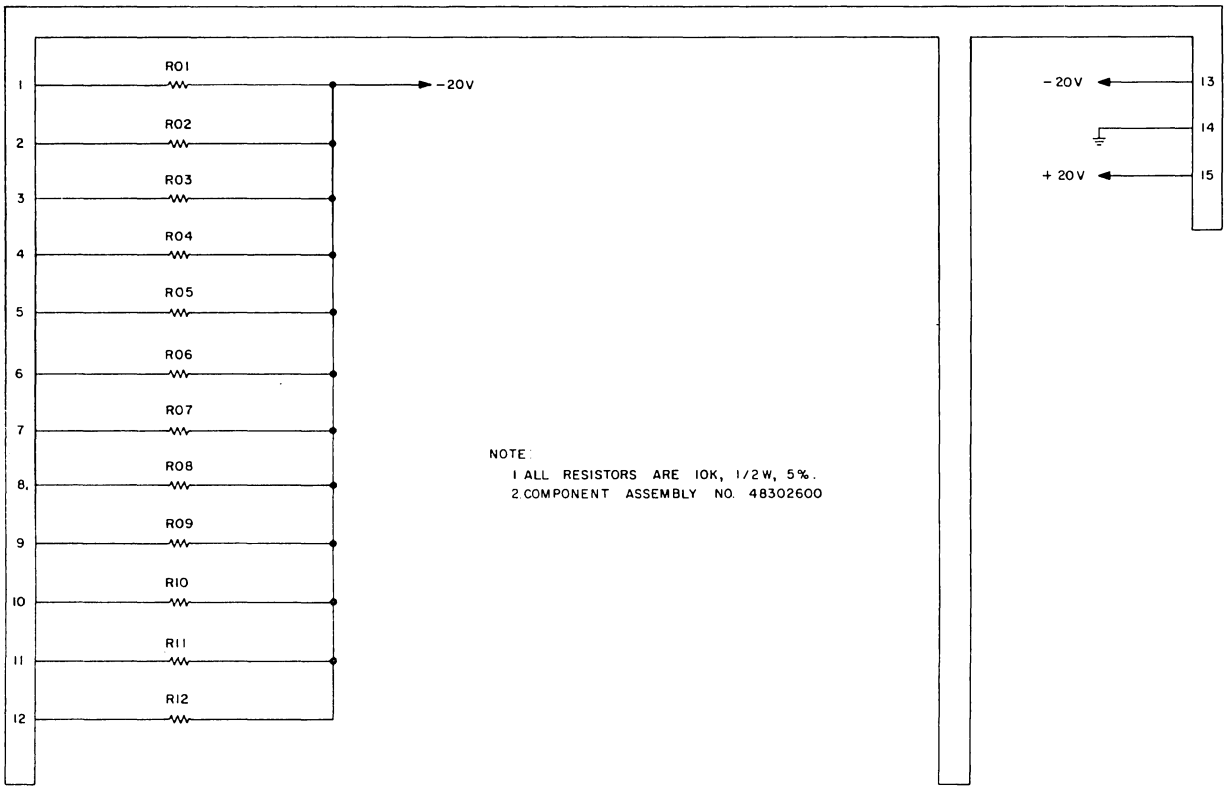



NOTE

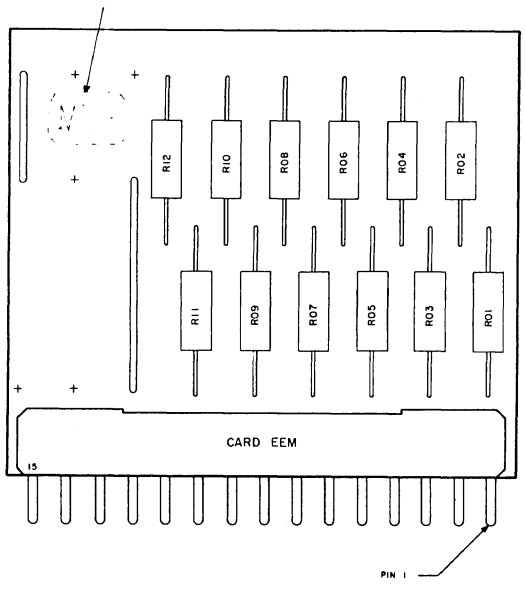
1. CAPACITORS C01, C02, C03, ARE 1μf.
2. CAPACITORS C04, C05, C06, ARE 1.5μf.
3. CAPACITORS C07, C08, C09, ARE 2.2μf.
4. CAPACITORS C10, C11, C12, ARE, 3.3 μf.
5. COMPONENT ASSEMBLY NO. 48302900.

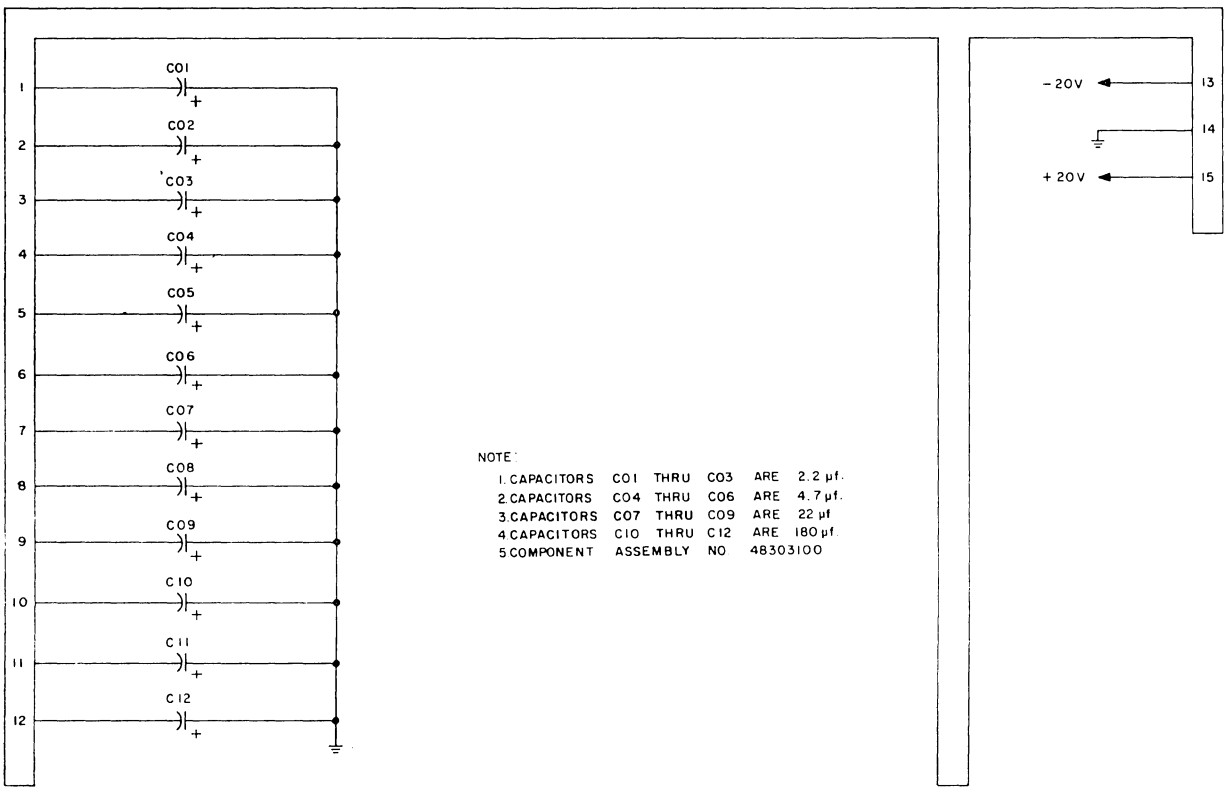
# EEL




R01
R02
R03
R04
R05
R06
R07
R08
R09
R10
R11
R12
1
2
3
4
5
6
7
8.
9
10
11
12
-20V
-20V
+20V
13
14
15
NOTE:
1 ALL RESISTORS ARE 10K, 1/2W, 5%.
2 COMPONENT ASSEMBLY NO. 48302600

EEM

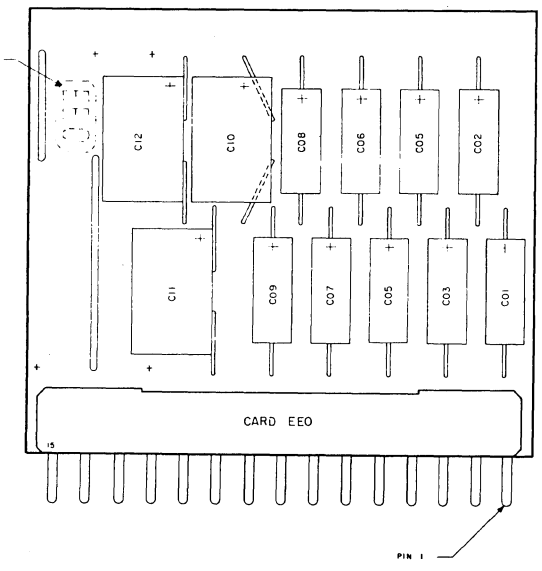

R12
R10
R08
R06
R04
R02
R11
R09
R07
R05
R03
R01
CARD EEM
15
PIN 1




NOTE:

1. CAPACITORS C01 THRU C03 ARE 2.2 µf.
2. CAPACITORS C04 THRU C06 ARE 4.7 µf.
3. CAPACITORS C07 THRU C09 ARE 22 µf
4. CAPACITORS C10 THRU C12 ARE 180 µf.
5. COMPONENT ASSEMBLY NO 48303100

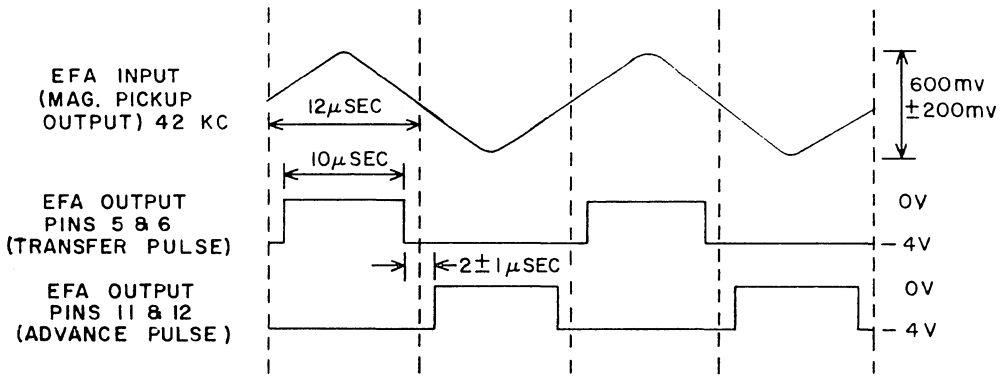
# EEO

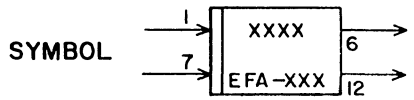


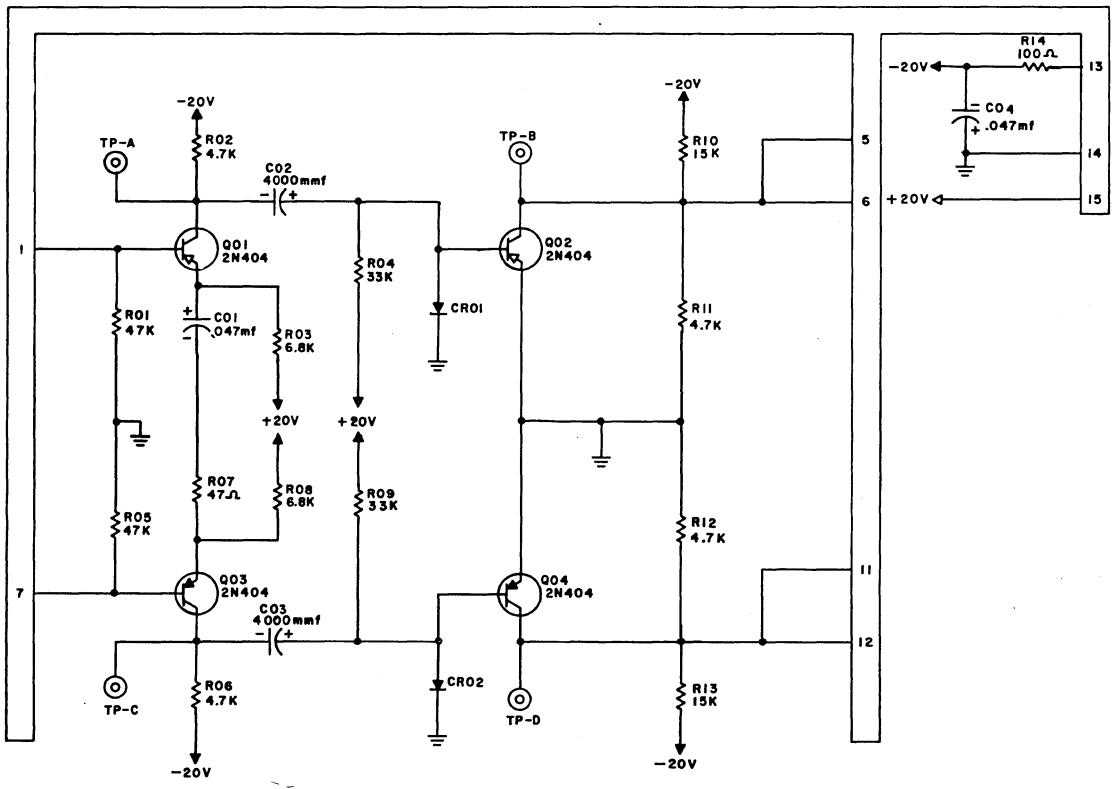
# CLOCK AMPLIFIER
## EFA

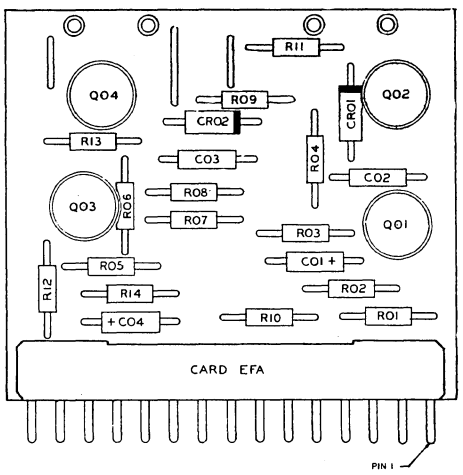
The clock amplifier circuit is intended for use in shaping a magnetic pickup signal into two nonoverlapping output pulses in a card reader. The output pulses are designed as signal sources to drive a clock counter. Typical waveforms are shown below. The circuit is designed for a 42-kc sine wave input, and the output interfaces with standard logic but does not include output diodes for AND terms.

A balanced class A amplifier circuit is used with emitter degeneration and common mode noise rejection in the first stage consisting of Q01 and Q02. A network couples and shapes the waveform to drive the output switching stage which consists of Q03 and Q04.




-20V
TP-A
R02 4.7K
C02 4000mmf
Q01 2N404
R01 47K
C01 .047mf
R03 6.8K
R04 33K
CR01
+20V
R07 47Ω
R08 6.8K
R09 33K
R05 47K
Q03 2N404
C03 4000mmf
TP-C
R06 4.7K
CR02
-20V
TP-B
R10 15K
Q02 2N404
R11 4.7K
R12 4.7K
Q04 2N404
TP-D
R13 15K
-20V
R14 100Ω
-20V
C04 .047mf
+20V
1
5
6
7
11
12
13
14
15


Q04
R09
R11
Q02
CR02
CR01
R13
C03
R04
C02
Q03
R06
R08
R07
R03
Q01
R05
C01 +
R12
R14
R02
+C04
R10
R01
CARD EFA
PIN 1

# READ LEVEL DETECTOR
## EGA

This circuit is a modification of the EDA level detector card with the following differences:

1) The gain can be selected by external jumpers (pins 3, 4, 5, and 8) to allow any of five feedback combinations of the network consisting of resistors R03, R04, R18, and R19. This increases the choice of head turns and tape speeds.

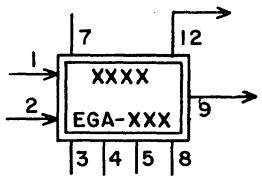
2) The level detection or threshold point is not fixed by components on the card but is selected by a reference voltage that is obtained externally (pin 7). This feature allows a vernier adjustment of the threshold point to match variations in head output or type of tape used.

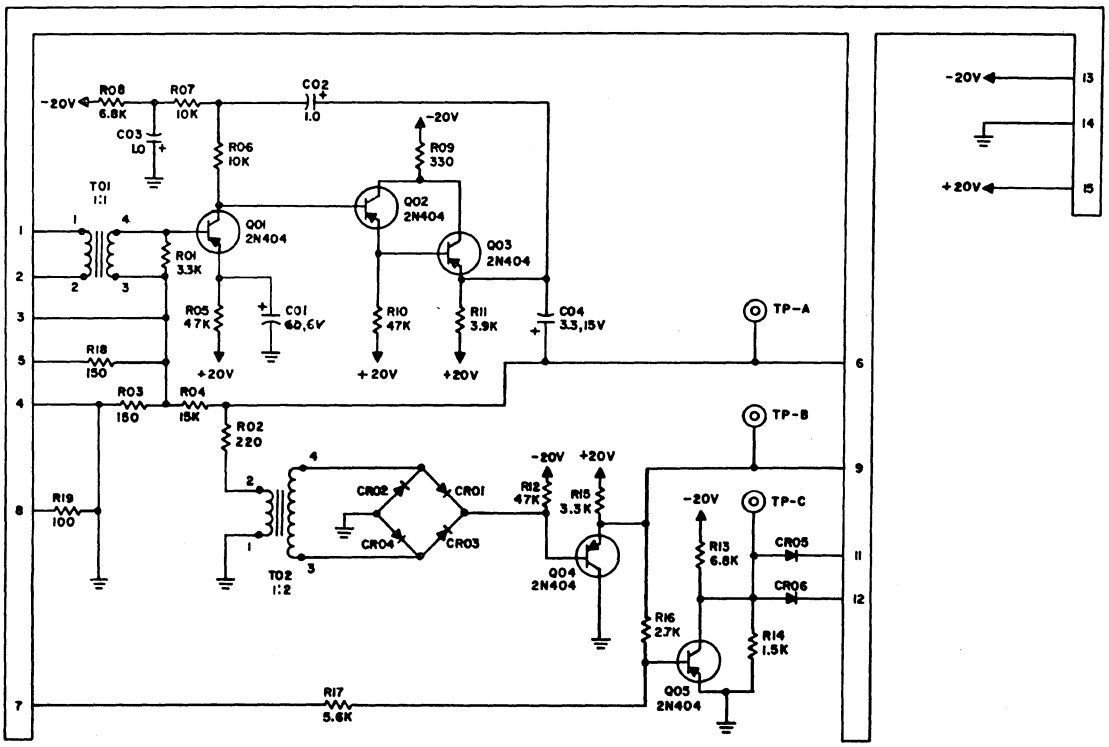
3) Two level detection diodes CR05 and CR06 are available for separate AND terms with the peak detector output.

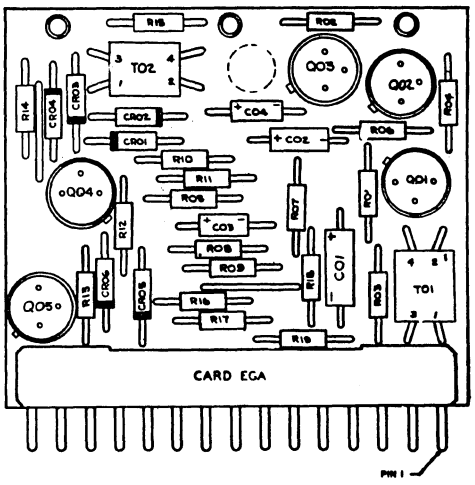
4) The rectifying circuit makes available the whole signal to the peak detector instead of passing only the part in excess of the threshold point. This reduces the ratio of minimum to maximum signal that must be accepted by the peak detector.

5) The class A overload point has been increased to approximately 11 volts in the peak-to-peak output signal.

SYMBOL




-20V
+20V
R08 6.8K
R07 10K
C02 1.0
C03 1.0
R06 10K
R09 330
T01 1:1
Q01 2N404
Q02 2N404
Q03 2N404
R01 3.3K
R05 47K
C01 60,6V
R10 47K
R11 3.9K
C04 3.3,15V
TP-A
R18 150
R03 150
R04 15K
R02 220
TP-B
CR02
CR01
CR04
CR03
R12 47K
R15 3.3K
R19 100
T02 1:2
Q04 2N404
TP-C
R13 6.8K
CR05
CR06
R16 2.7K
R14 1.5K
Q05 2N404
R17 5.6K


T02
Q03
Q02
Q04
Q01
Q05
T01
CARD EGA
PIN 1

# READ PREAMPLIFIER

## EHA, EHB, EHC

The read preamplifier is used in the read data circuit to amplify NRZ1 information recorded on magnetic tape for use in subsequent level and peak detecting circuits. The amplifier circuit includes provision f a differential input and a balanced push-pull output.

The preamplifier has two differential stages of gain (Q01, 02, and Q05, 06) to minimize common mode signal interference. Each differential stage includes an isolating emitter follower output (Q03,04,07,08) to re duce loading effects on the inverting amplifier.

Coarse and fine gain adjustments are provided by negative feedback in the emitter of each stage of gain. Two steps of coarse gain may be selected in the first stage by external jumpers. Connecting pin 5 to pi 7 provides minimum gain and connecting pin 5 to pin 8 provides maximum gain. Fine gain is provided by adjusting the potentiometer R22 in the second stage. This adjustment provides the following gains:

| | Jumper Pins |
|---|---|
| EHA - 150 to 550 | 5-7 |
| 350 to 1300 | 5-8 |
| EHB - 200 to 800 | 5-7 |
| 500 to 1800 | 5-8 |

Except for the output and the emitter degeneration, the amplifier i direct-coupled to reduce recovery time. Power supply transients are min imized by the common mode rejection of the differential amplifier. In addition, R21 and C03 filter the negative supply for both stages; CR01 a R18 reduce the voltage for the first stage.

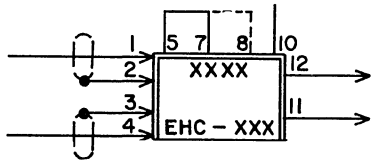
The EHC circuit differs from the EHB as follows:

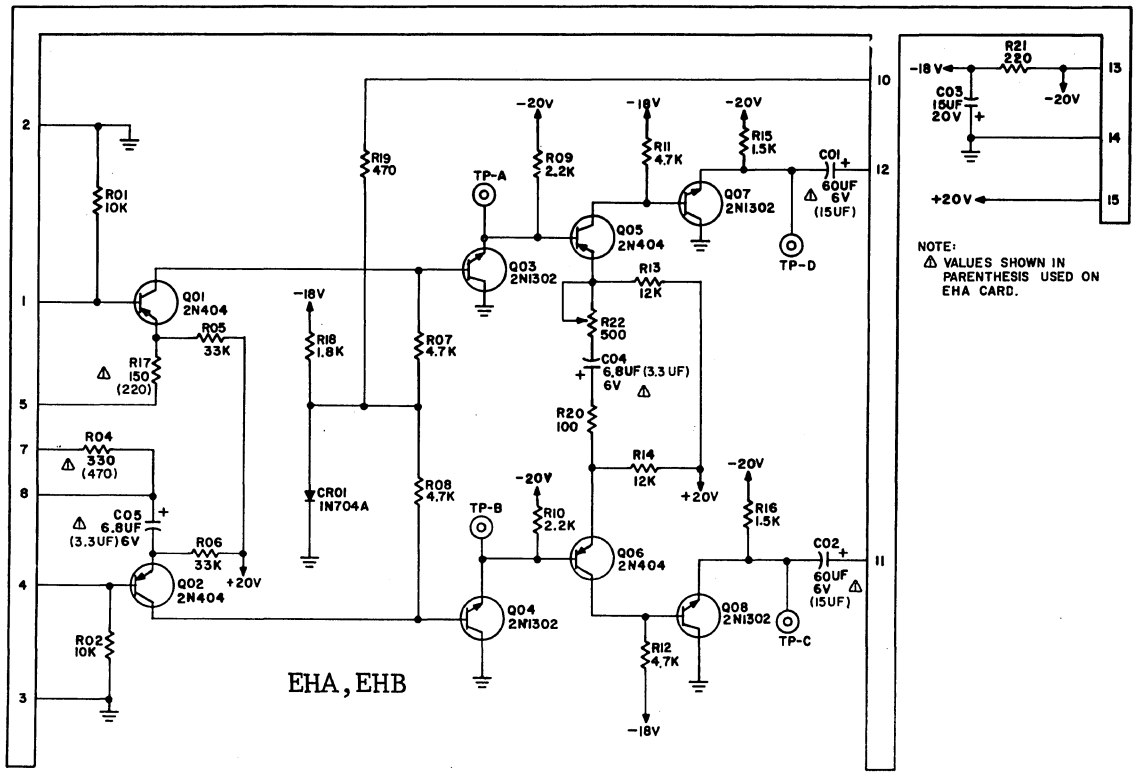
1. Capacitors C06 and C07 provide two stages of high frequenc roll-off. Each capacitor reduces gain by about 3 db at 100 kc (sine wave).
2. Output capacitors C01 and C02 are polarized for load termi ations of -10 to -16 volts or for isolated transformer windings such as those on EI-series cards.
3. Gain jumpering options are not interchangeable with the EH except when pin 5-7 is used at frequencies of 30 kc and lo Gain ranges for sine-wave frequencies of 5 to 30 kc are

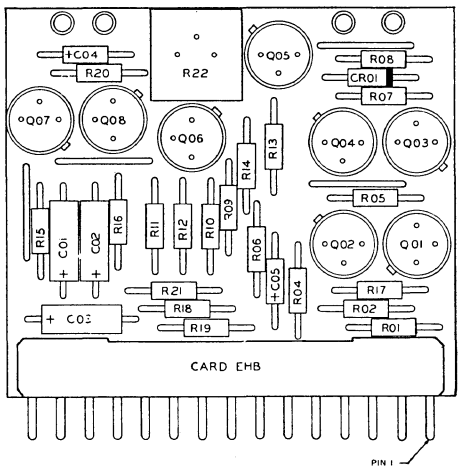
tabulated below:

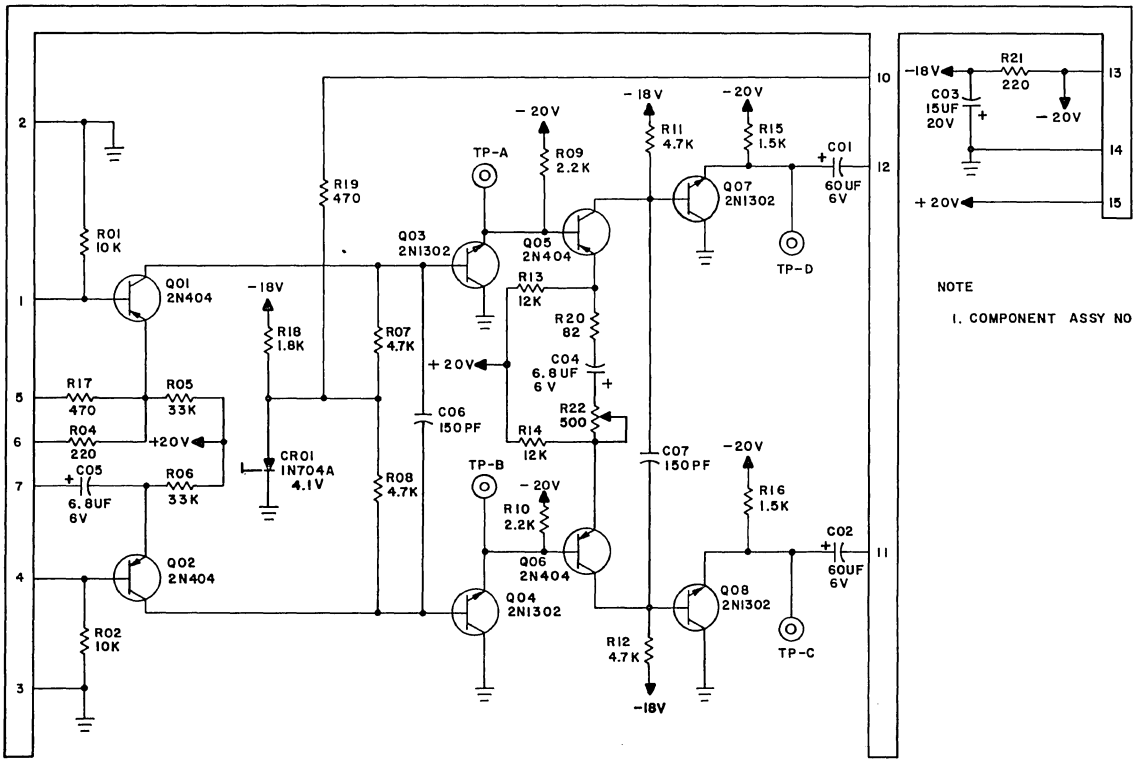
| | Jumper Pins |
|---|---|
| EHC - 200-800 | 5-7 |
| 360-1400 | 6-7 |
| 500-1800 | 5-6-7 |

SYMBOL

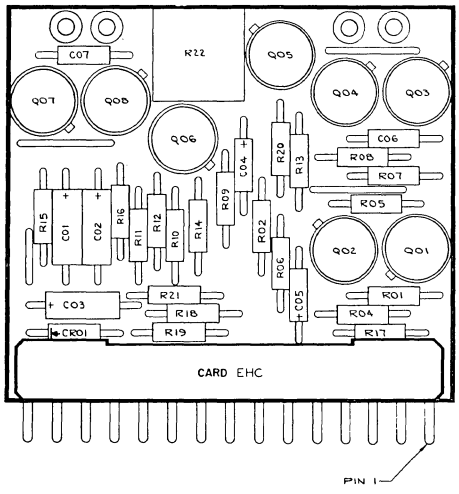



R01 10K
Q01 2N404
R17 470
R04 220
C05 6.8UF 6V
R05 33K
R06 33K
Q02 2N404
R02 10K
R18 1.8K
CR01 IN704A 4.1V
R19 470
R07 4.7K
R08 4.7K
Q03 2N1302
Q04 2N1302
C06 150PF
TP-A
TP-B
R09 2.2K
R10 2.2K
Q05 2N404
Q06 2N404
R13 12K
R20 82
C04 6.8UF 6V
R22 500
R14 12K
C07 150PF
R11 4.7K
R12 4.7K
R15 1.5K
R16 1.5K
Q07 2N1302
Q08 2N1302
C01 60UF 6V
C02 60UF 6V
TP-C
TP-D
-18V
-20V
+20V
R21 220
C03 15UF 20V
NOTE
1. COMPONENT ASSY NO 5000860I.

EHC


C07
R22
Q05
Q07
Q08
Q04
Q03
Q06
C06
R08
R07
R05
R20
R13
C04
R09
R15
C01
C02
R16
R11
R12
R10
R14
R02
R06
C05
Q02
Q01
R21
C03
R18
CR01
R19
R01
R04
R17
CARD EHC
PIN 1

# READ LEVEL DETECTOR
## EIA, EIB, EID, EIE

The read level detector receives the amplifed signal from the read preamplifier (EH-series) and provides a rectified signal and a threshold enable for the peak detector (OG-series) in the recovery of NRZ1 information from the magnetic tape.

The rectifying circuit is composed of transformer T01, diodes CR01 and CR02, and transistors Q01 and Q02. The negative rectified signal is then routed to the differential input stage of the level detecting circuit (Q04 and Q05). The signal is compared to the threshold input reference voltage on pin 7. The switching point is further enhanced and referenced to ground by the amplifiers consisting of transistors Q06 and Q07, in a form usable as an enable in the peak detector.

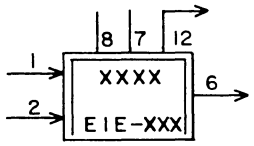
The rectified signal is also routed to an output emitter follower (Q03) which drives the RC differentiating circuit in the input stage of the peak detector.

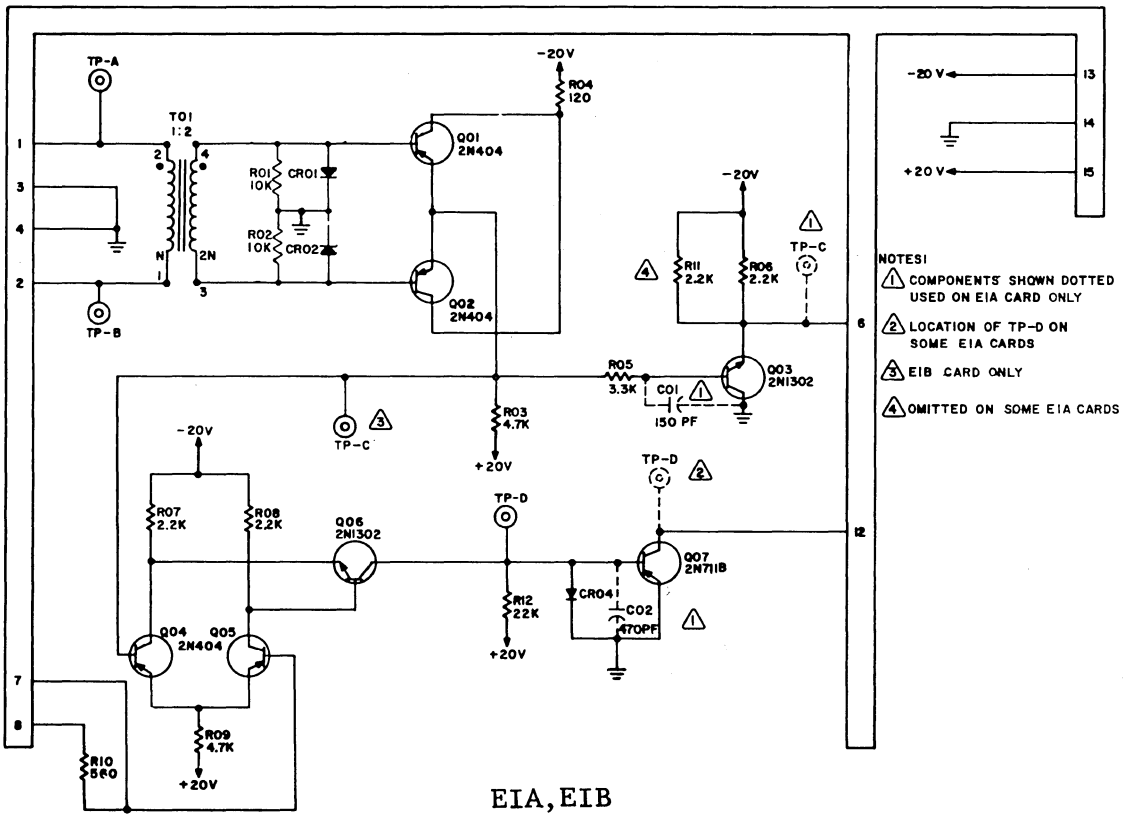
The EID and EIE circuits differ from the EIB as follows:

1. Rectifier transformer T01 is designed to pass 5 kc sine-wave signals compared to 20 kc as a lower limit on the EIB card. This delays and filters some of the higher frequency components and is intended primarily for fundamental signals not exceeding 45 kc sine-wave frequency (90 kc NRZ1 data rate).
2. Resistors R13 and R14 are added to cause diodes CR01 and CR02 to maintain a lower transformer secondary impedance during zero or weak signals.
3. Q01 and Q02 are matched transistors to assure better signal balance of both polarities of input. Transistors Q04 and Q05 are matched to provide more accurate level detection thresholds.

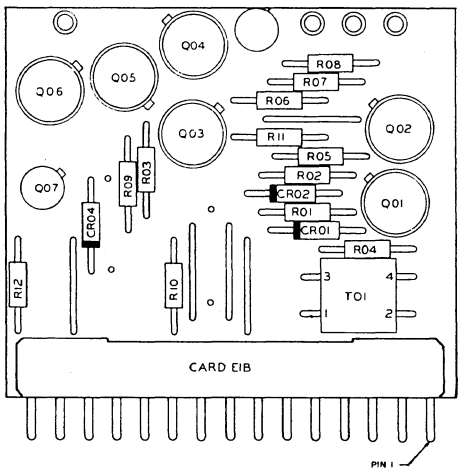
The EIE card differs from the EID only in the addition of C01, which provides one RC stage of additional high frequency roll-off (down 3 db at 200 kc data rate).

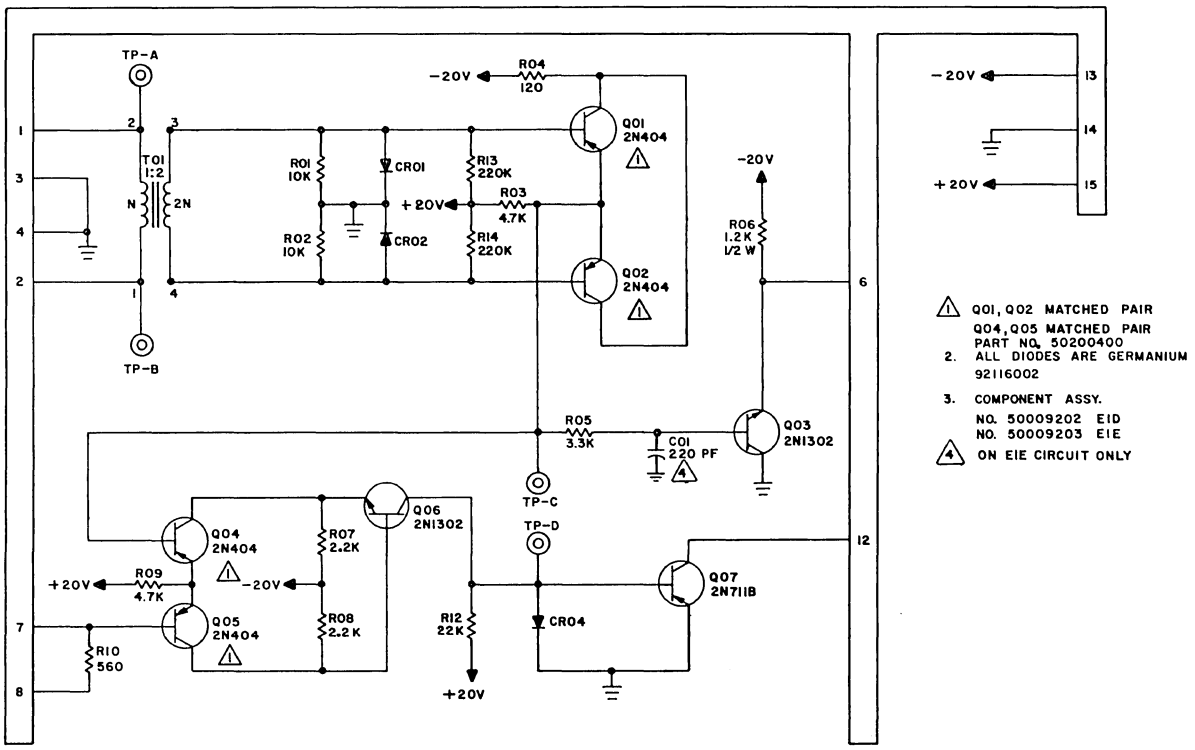
SYMBOL



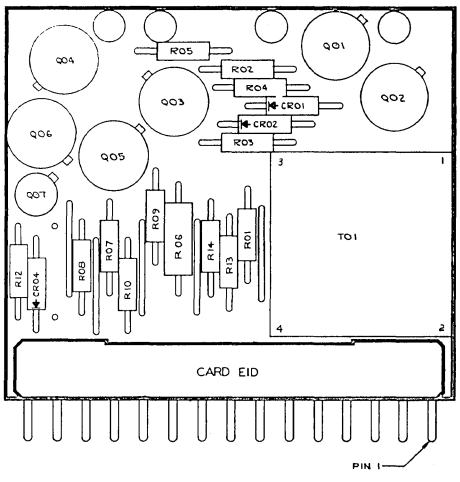



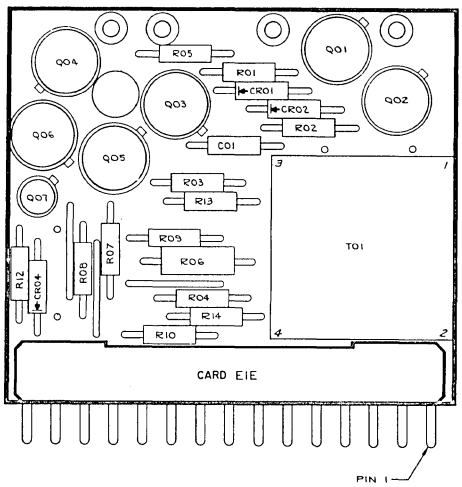

EIA, EIB




TP-A
TP-B
TP-C
TP-D
T01
1:2
N
2N
R01
10K
R02
10K
CR01
CR02
R13
220K
R14
220K
+20V
R03
4.7K
-20V
R04
120
Q01
2N404
Q02
2N404
R06
1.2K
1/2 W
R05
3.3K
C01
220 PF
Q03
2N1302
Q04
2N404
Q05
2N404
R07
2.2K
R08
2.2K
Q06
2N1302
R09
4.7K
R10
560
R12
22K
CR04
Q07
2N711B
+20V
-20V
13
14
15
1
2
3
4
6
7
8
12
Q01, Q02 MATCHED PAIR
Q04, Q05 MATCHED PAIR
PART NO. 50200400
2. ALL DIODES ARE GERMANIUM
92116002
3. COMPONENT ASSY.
NO. 50009202 EID
NO. 50009203 EIE
4 ON EIE CIRCUIT ONLY

EID, EIE


Q04
R05
Q01
R02
R04
Q03
Q02
CR01
CR02
Q06
Q05
R03
Q07
T01
R09
R08
R07
R06
R14
R13
R01
R12
CR04
R10
CARD EID
PIN 1


Q04
R05
Q01
R01
CR01
Q03
CR02
Q02
R02
Q06
C01
Q05
R03
Q07
R13
T01
R09
R08
R07
R06
R12
CR04
R04
R14
R10
CARD EIE
PIN 1

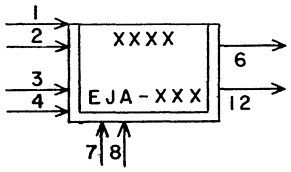
# RECTIFIER AND THRESHOLD DETECTOR

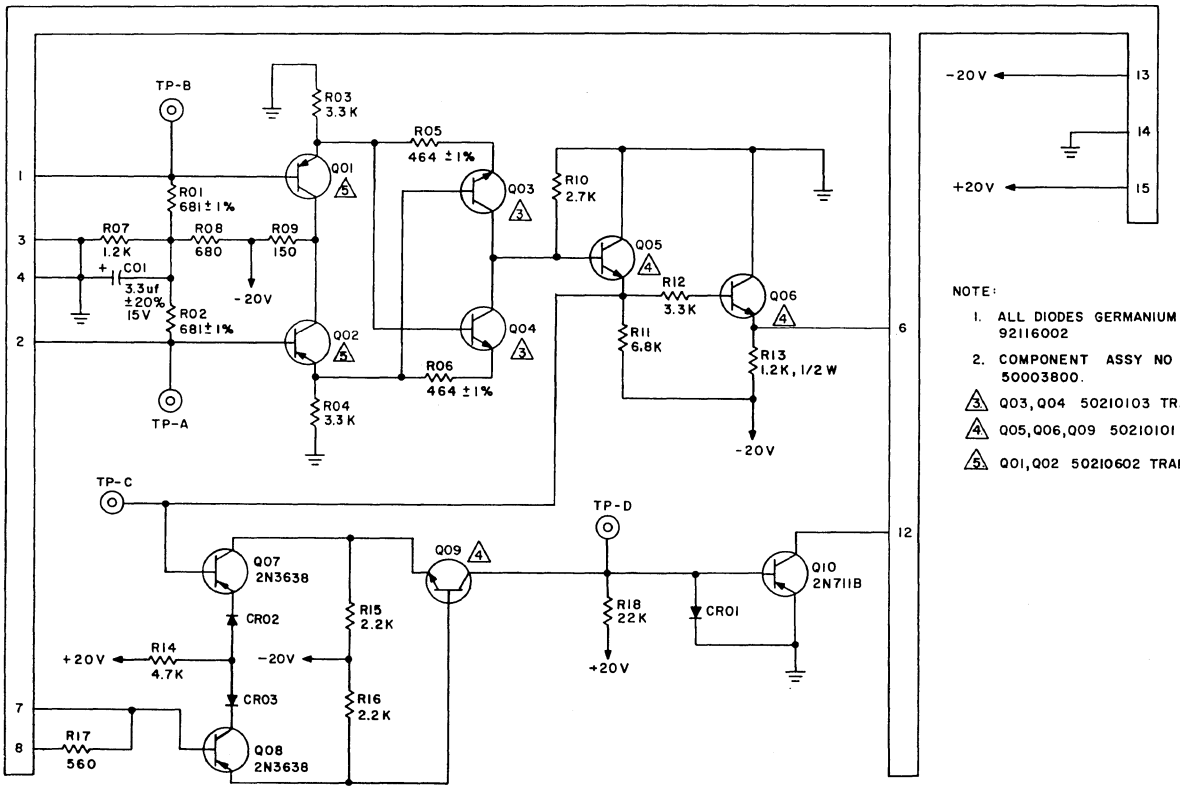
## EJA

The EJA contains two different (but interconnected) circuits per card. The 1st circuit (consisting of Q01 through Q06) constitutes a full wave rectifier (Q01-Q04) feed through two buffer amplifiers (Q05, Q06). The output on pin 6 is essentially the same as the output of the rectifier circuit. The output of the rectifier circuit at the base of Q05 is a negative-going full wave rectified signal (referenced to ground).

The 2nd circuit (consisting of Q07, Q08 and Q09) compares the rectified output of the 1st circuit to a reference (threshold) voltage via input pins 7 or 8. If the rectifier signal (TPC) is more negative than the threshold voltage, Q09 and Q10 are turned OFF.

When Q10 is OFF, output pin 12 is floating; when Q10 is ON, pin 12 is grounded. The output of pin 12 is used to enable a OGD card in the Read chain of an 852 disk storage drive. When pin 12 is floating, the OGD is enabled; when pin 12 is grounded, the OGD is disabled.






NOTE:

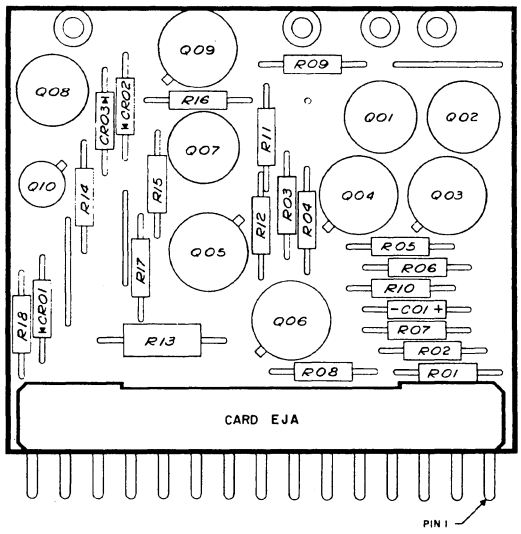
1. ALL DIODES GERMANIUM 92116002
2. COMPONENT ASSY NO 50003800.

△3 Q03, Q04 50210103 TRANSISTOR.

△4 Q05, Q06, Q09 50210101 TRANSISTOR.

△5 Q01, Q02 50210602 TRANSISTOR.

EJA



POTENTIOMETER

EPA

The potentiometer card is designed for use with the EGA read level detector in the recovery of NRZ1 information on magnetic tape. It provides an external gain adjustment for 7 circuits when properly connected in the negative feedback loop of the preamplifier circuit of the EGA card. This allows amplifier output amplitude to be equalized for variations in head output and circuits.

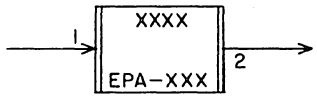
Each EPA circuit includes 7 potentiometers, connected as rheostats, one for each of the 7 bits recorded on 1/2 inch compatible tape. Five of the potentiometers have both ends brought out to external pins; the other two have 100-ohm resistors to ground to simulate R19 (pin 8) of the EGA card. This utilizes the 12 signal pins on the card.

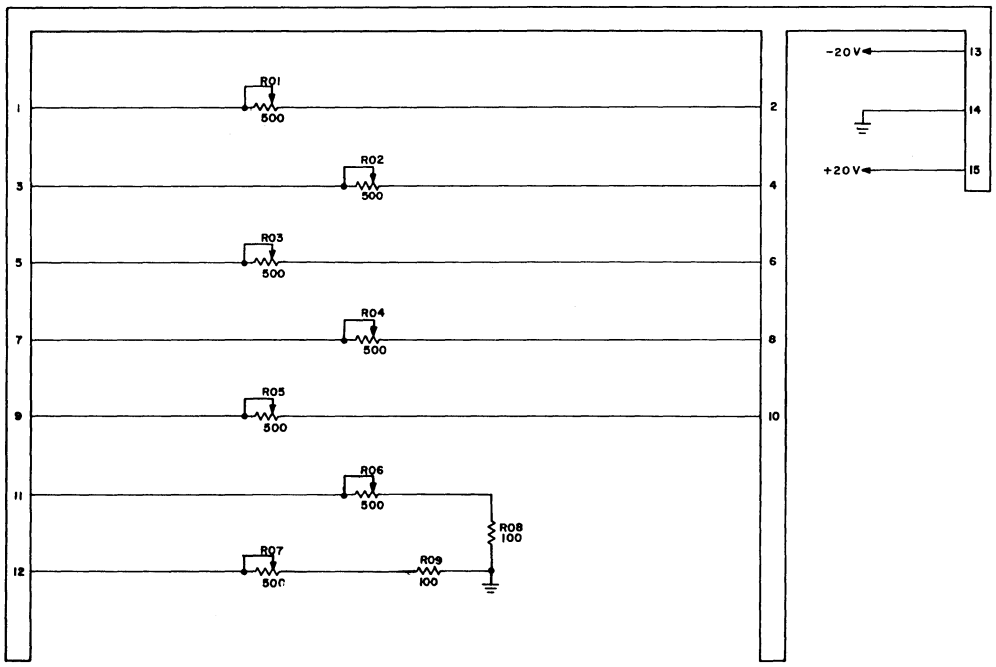
CAUTION: The height of potentiometers used on the EPA card requires that the adjacent card slot on the component side of the card be left empty. In removing and replacing the card, care should be given to minimize mechanical stress on the potentiometer cases or the internal element may be cracked.

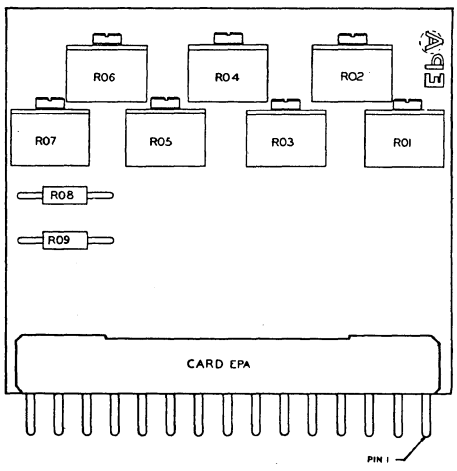
A typical connection is as follows:

| EPA Pin No. | | |
|---|---|---|
| 1 | 3 | EGA, track 0 |
| 2 | 8 | |
| 3 | 3 | EGA, track 1 |
| 4 | 8 | |
| 5 | 3 | EGA, track 2 |
| 6 | 8 | |
| 7 | 3 | EGA, track 3 |
| 8 | 8 | |
| 9 | 3 | EGA, track 4 |
| 10 | 8 | |
| 11 | 3 | EGA, track 5 |
| 12 | 3 | EGA, track 6 |

SYMBOL




R01
500
R02
500
R03
500
R04
500
R05
500
R06
500
R08
100
R07
500
R09
100
1
2
3
4
5
6
7
8
9
10
11
12
-20V
+20V
13
14
15


A15
R06
R04
R02
R07
R05
R03
R01
R08
R09
CARD EPA
PIN 1

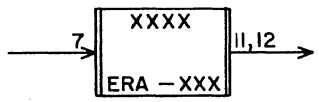
# SOLENOID DRIVER
## ERA

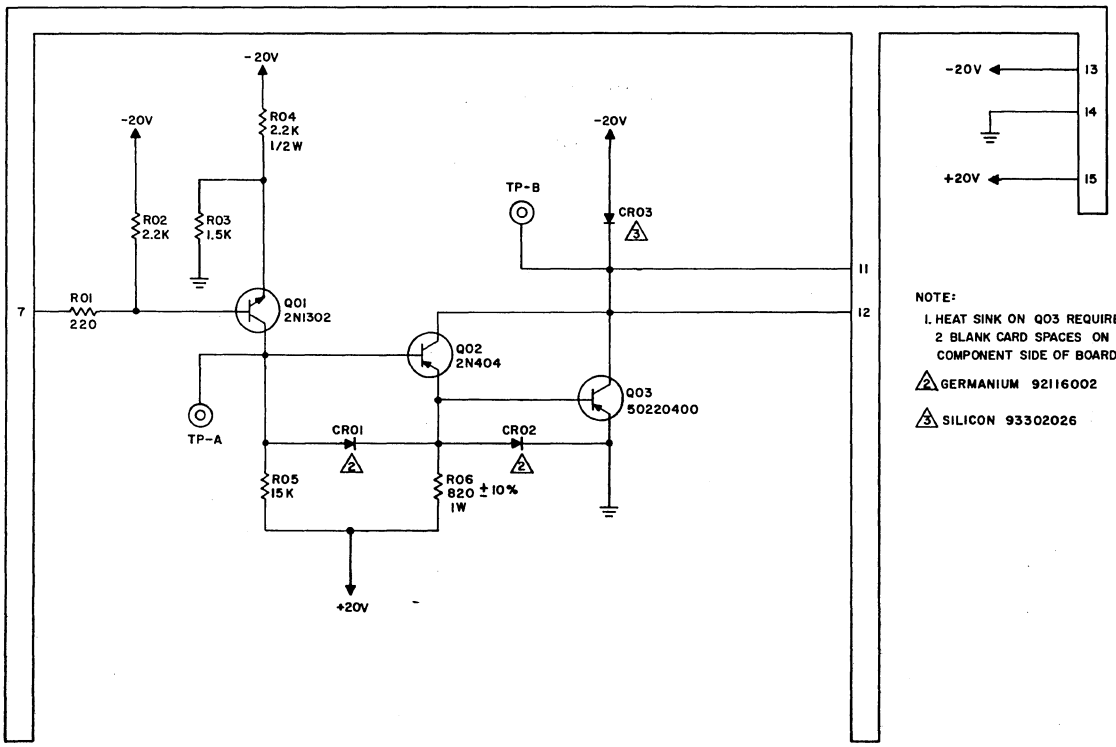
The solenoid driver is designed to switch a 2¼ ampere load terminated at a negative voltage between -2v and -20v. Its input is intended to match that of an "L" card output. When the input is at ground the output is driven to ground. Thus an open input turns the circuit off.

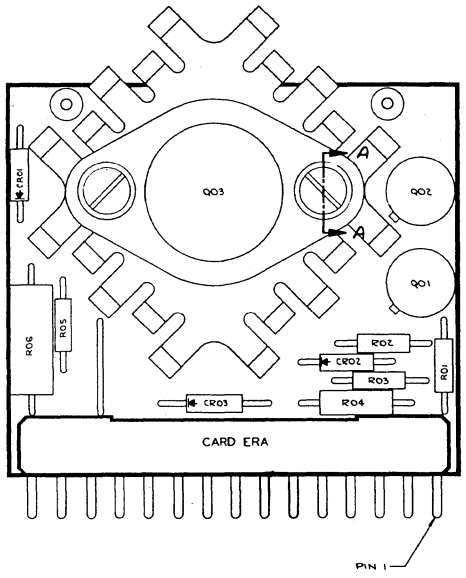
The circuit is intended to operate the tape unit capstan solenoid. In this application it is located apart from the general logic. The high steady state current capability of the circuit requires special heat sinking of the output transistor. The "claw" type heat sink is mounted on standard logic card hardware, but requires space equivalent to three card slots. No signals are placed on pins 1-3 to eliminate the possibility of damage if the card is inserted upside down in the normal logic connector.

Circuit operation is as follows. A ground on the input turns Q01 on. Q01 collector current turns Q02 on, which in turn turns on Q03. R03 and R04 in the emitter circuit of Q01 determine the switching point of the input signal. CR03 acts as a suppression circuit for inductive loads. Other components have functions similar to those in ordinary inverter circuits.

SYMBOL




-20V
R04
2.2K
1/2W
-20V
R02
2.2K
R03
1.5K
-20V
TP-B
CR03
3
11
7
R01
220
Q01
2N1302
12
Q02
2N404
Q03
50220400
TP-A
CR01
2
CR02
2
R05
15K
R06
820 ± 10%
1W
+20V
-20V
13
14
+20V
15
NOTE:
1. HEAT SINK ON Q03 REQUIRES 2 BLANK CARD SPACES ON COMPONENT SIDE OF BOARD.
2 GERMANIUM 92116002
3 SILICON 93302026


CR01
Q03
A
A
Q02
Q01
R06
R05
R02
CR02
R03
R01
CR03
R04
CARD ERA
PIN 1

## DIFFERENTIAL AMPLIFIER
## EUA

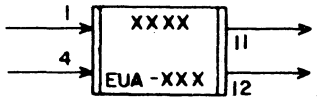
The EUA card is a differential 2-stage amplifier. The output is an amplifier reproduction of the input.

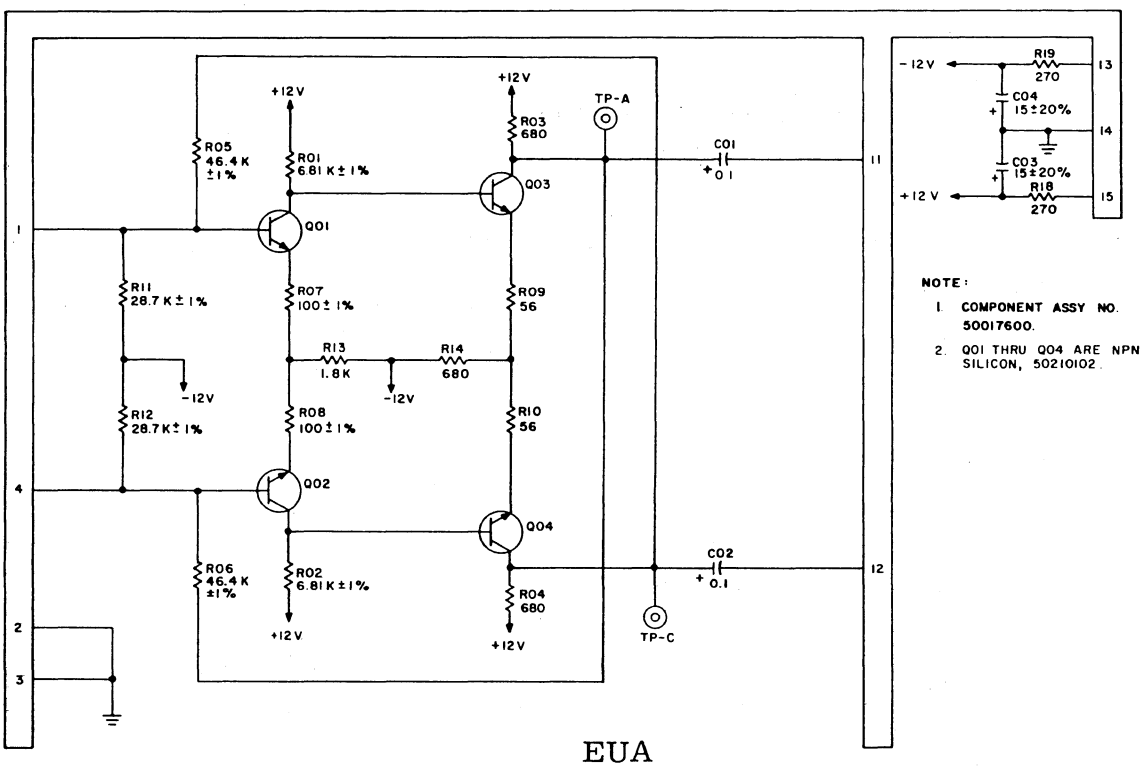
To improve operation, internal voltages are isolated from machine power supply by R-C filters. The circuit is designed to operate from a source impedance of approximately 1 K, and to drive a load of approximately 1.2 K. Bandpass is from 10 KC to 5 MC.

## DIFFERENTIAL AMPLIFIER
## EUC, EUD

This card is similar to the EUA card. The two significant differences are: feedback paths were added from collector to base of Q01 and Q02 to reduce high frequency gain, and an output power-amplifier stage (Q05 and Q06) was added to allow the circuit to drive a low impedance load. Design source impedance is approximately 1 K, and load impedance is 500 ohms. Bandpass is from 10 KC to 2 MC.

SYMBOL

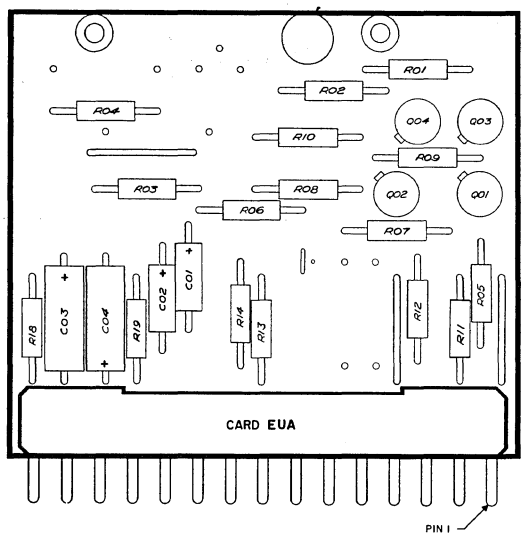


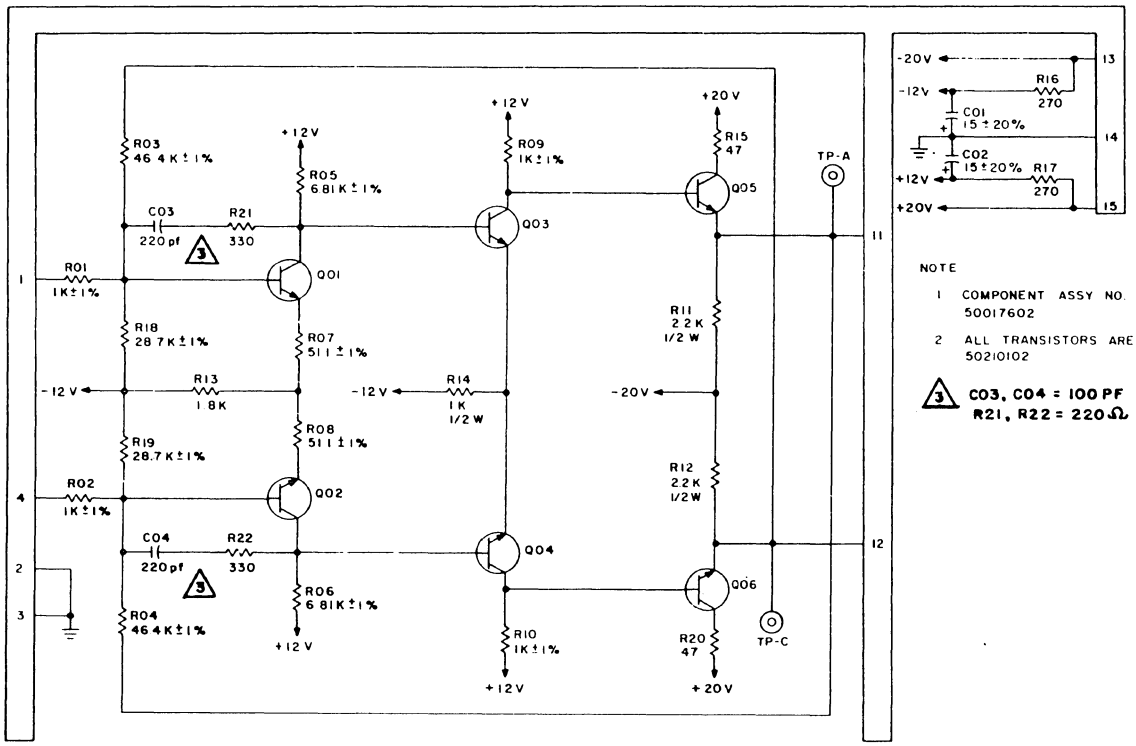



NOTE:

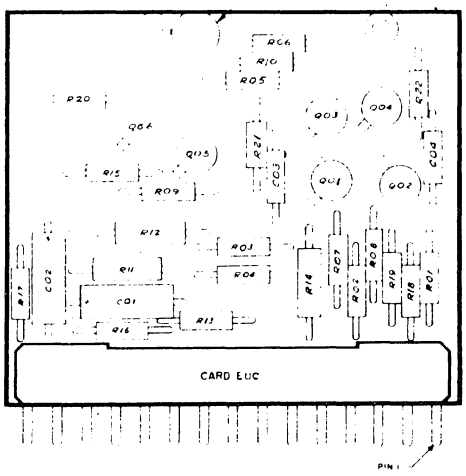
1. COMPONENT ASSY NO. 50017600.
2. Q01 THRU Q04 ARE NPN SILICON, 50210102.

EUA




+12V
+20V
-20V
-12V
R03 46.4K ±1%
R05 6.81K ±1%
R09 1K ±1%
R15 47
TP-A
C03 220pf
R21 330
Q03
Q05
R01 1K ±1%
Q01
R18 28.7K ±1%
R07 511 ±1%
R11 2.2K 1/2W
R13 1.8K
R14 1K 1/2W
R08 511 ±1%
R19 28.7K ±1%
R12 2.2K 1/2W
R02 1K ±1%
Q02
C04 220pf
R22 330
Q04
Q06
R06 6.81K ±1%
R04 46.4K ±1%
R10 1K ±1%
R20 47
TP-C
C01 15 ±20%
C02 15 ±20%
R16 270
R17 270
NOTE
1 COMPONENT ASSY NO. 50017602
2 ALL TRANSISTORS ARE 50210102
3 C03, C04 = 100 PF R21, R22 = 220Ω

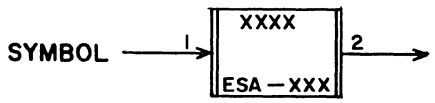
EUC, EUD

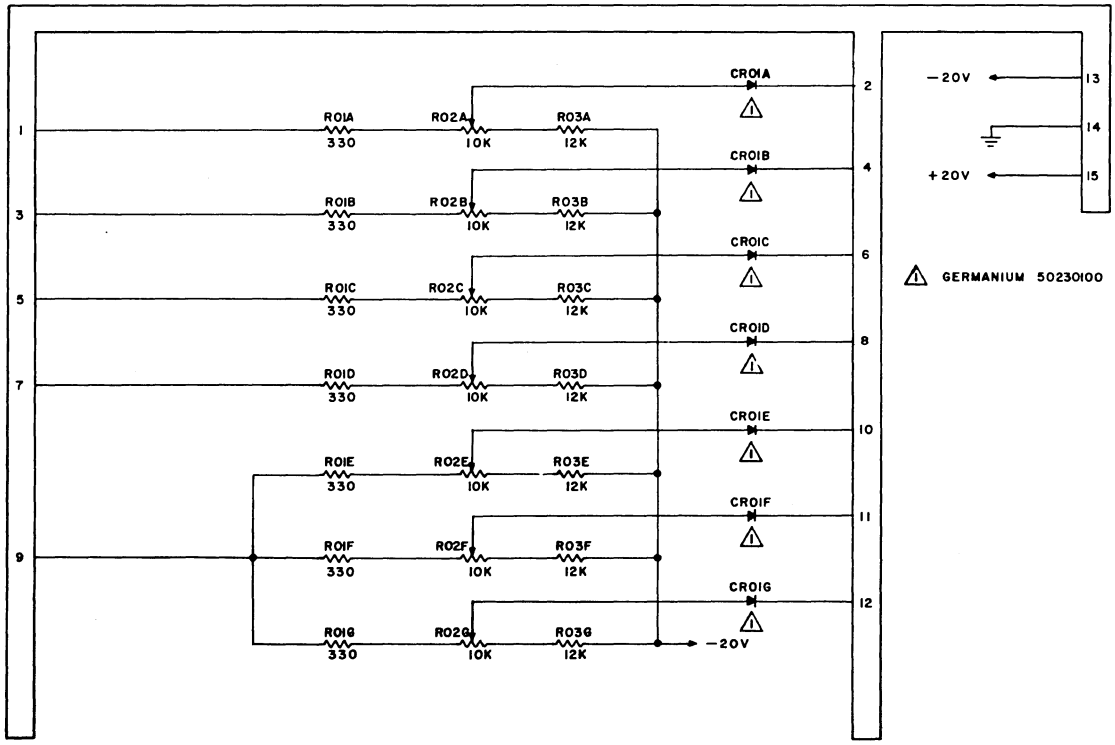

CARD EUC
PIN 1

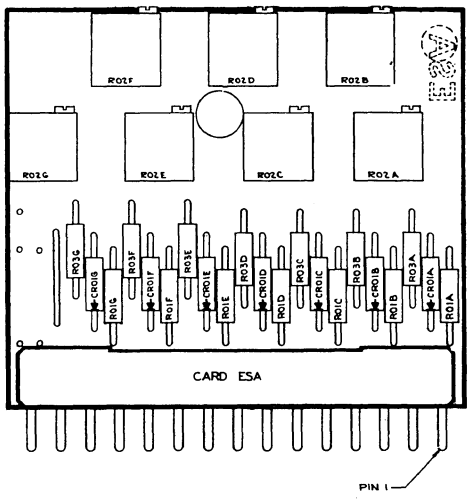
# DELAY CONTROL POTENTIOMETERS
# ESA

The delay control potentiometer circuit is designed for use with voltage-controlled delay circuits such as the UGA, in which it is desired to obtain one or more additional selected delays from a single delay circuit and still maintain good precision. It acts as a gating circuit to work into a positive OR terminating resistor that does not require a low-impedance input.

The card contains seven like circuits. All outputs are isolated from each other, but three of the seven inputs are paralleled to reduce the connections to the twelve pins available for signals. The seven circuits are sufficient for use with a seven-channel read recovery system in tape units. Input signals should have an excursion of 0 to -12v (or more negative) and require about 2 ma drive for a -20v terminated load on each of the seven circuits. Normally, all inputs are parallel connected and used for read reverse deskew while the potentiometers on the UGA cards are used for read forward deskew. The circuits can also be used as a voltage-reference circuit for other applications whether gated or permanently grounded on its input.




CR01A
CR01B
CR01C
CR01D
CR01E
CR01F
CR01G
R01A
R01B
R01C
R01D
R01E
R01F
R01G
R02A
R02B
R02C
R02D
R02E
R02F
R02G
R03A
R03B
R03C
R03D
R03E
R03F
R03G
330
10K
12K
1
2
3
4
5
6
7
8
9
10
11
12
-20V
+20V
13
14
15
GERMANIUM 50230100


R01F
R02D
R02B
R02G
R02E
R02C
R02A
R03G
CR01G
R01G
R03F
CR01F
R01F
R03E
CR01E
R01E
R03D
CR01D
R01D
R03C
CR01C
R01C
R03B
CR01B
R01B
R03A
CR01A
R01A
CARD ESA
PIN 1

## RECEIVER FLIP-FLOP
## EVB

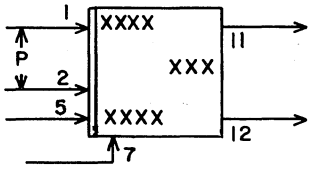
This card has a balanced twisted-pair line input, which is transferred to an internal flip-flop by an external pulse. An external gate level can inhibit transfer from the input to the flip-flop, and force both outputs to logical "0". The outputs do not have AND diodes.

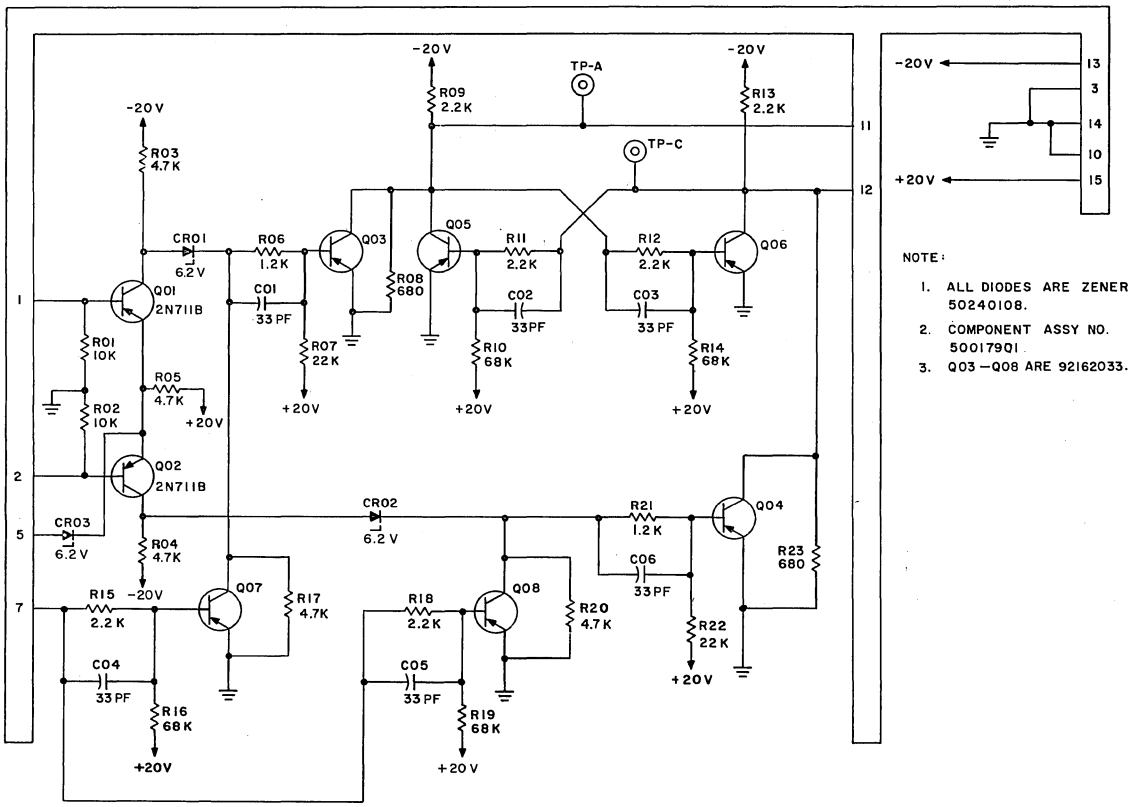
In normal operation, the Q01 and Q02 stage is the 3000 Interface receiver. With pin 5 at ground, transfer of the input at pins 1 and 2 to the flip-flop is controlled by the transfer pulse applied to pin 7. When pin 7 is at -3v or more negative, Q07 and Q08 are on, so Q03 and Q04 are turned off. Thus the flip-flop (Q05 and Q06) cannot be effected by Q01 and Q02, so it stays in its last previous state. When pin 7 goes to ground, Q07 and Q08 turn off. Then either Q03 or Q04 turns on (depending on the state of Q01 and Q02), and the state of pins 1 and 2 is transferred to pins 11 and 12. If pin 1 is more positive than pin 2, Q03 will turn on, and pin 11 will go to logical "0". Pin 12 will then be at logical "1". If pin 2 is more positive than pin 1, pin 11 will be at logical "1", and pin 12 at logical "0".

If pin 5 goes to -7v or more negative, Q01 and Q02 turn off, so the state of pins 1 and 2 cannot effect the EVB card. If pin 7 is at ground, Q03 and Q04 are turned on by CR01, CR02, R03, and R04. Both pin 11 and pin 12 will be at logical "0". If pin 7 is at -3v or more negative while pin 5 is at -7v or more negative, pins 11 and 12 will go into complementary states. However, either output could end up at logical "1" or logical "0".

| Input (voltage) | | | Output (logic) | |
|---|---|---|---|---|
| State of pin 1 vs. pin 2 | Pin 5 | Pin 7 | Pin 11 | Pin 12 |
| + | gnd | gnd | "0" | "1" |
| - | gnd | gnd | "1" | "0" |
| + or - | gnd | -3v | last previous state | |
| + or - | -7v | gnd | "0" | "0" |
| + or - | -7v | -3v | complementary | |

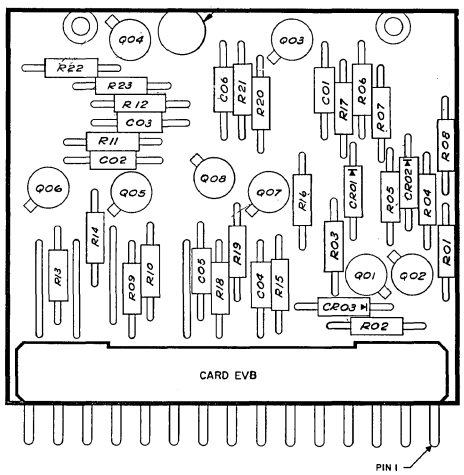
SYMBOL




NOTE:

1. ALL DIODES ARE ZENER 50240108.
2. COMPONENT ASSY NO. 50017901.
3. Q03 – Q08 ARE 92162033.



# ZERO-CROSSING DETECTOR/SHAPER
# EWA, EWC

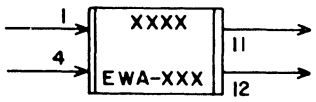
The EWA card detects zero-crossings of an input waveform. The output is a rectangular wave centered at +8v, which changes state whenever the input waveform goes through zero.

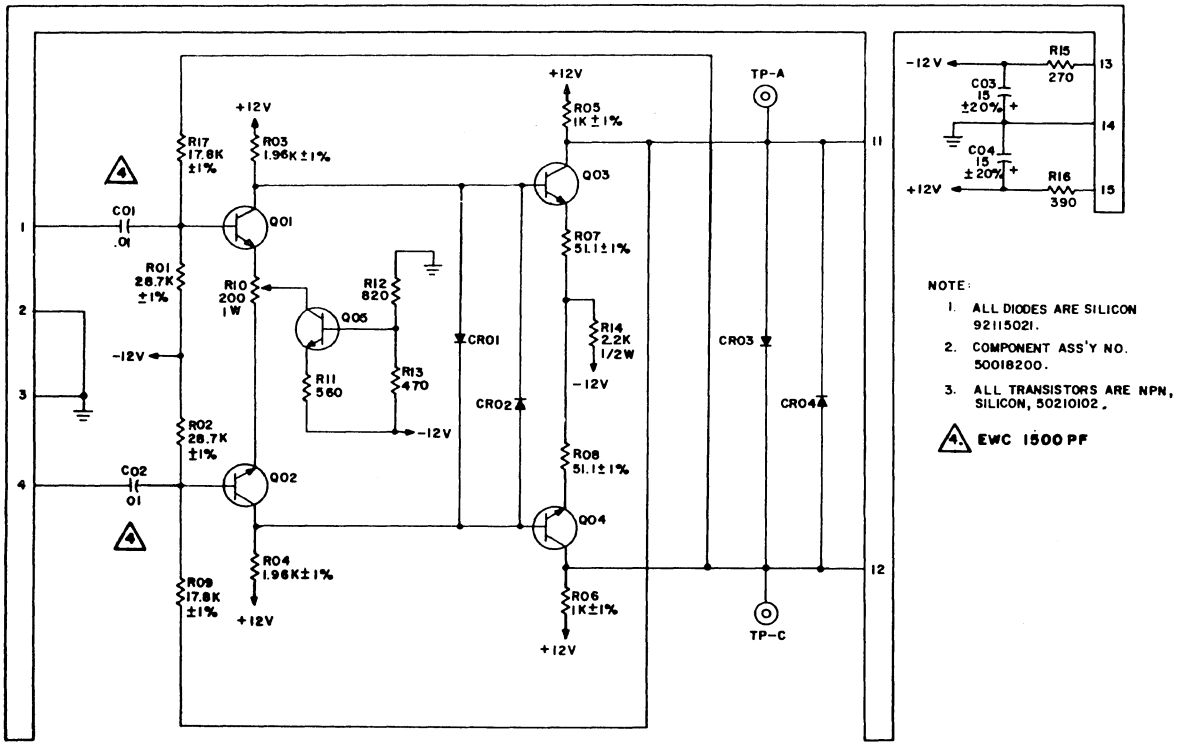
If the input is a differential signal, it is applied through C01 and C02 to the bases of Q01 and Q02. (The circuit could also be used to detect zero-crossings of a one-sided signal, by grounding the unused input pin.) If Q01 base is more positive than Q02 base, Q01 will turn on. This turns on CR02. If Q02 base goes more positive than Q01 base, Q02 and CR01 will turn on. The second differential pair, Q03 and Q04, sharpens up the resultant rectangular wave since the voltage gain is one. Either CR03 or CR04 is on so that the output between pin 11 and pin 12 is a rectangular wave of 0.6v, centered at +8v.

Internal voltages are isolated from the machine power supplies by R-C filters. Resistor R10 is adjusted for symmetrical operation over an amplitude range of input signals.

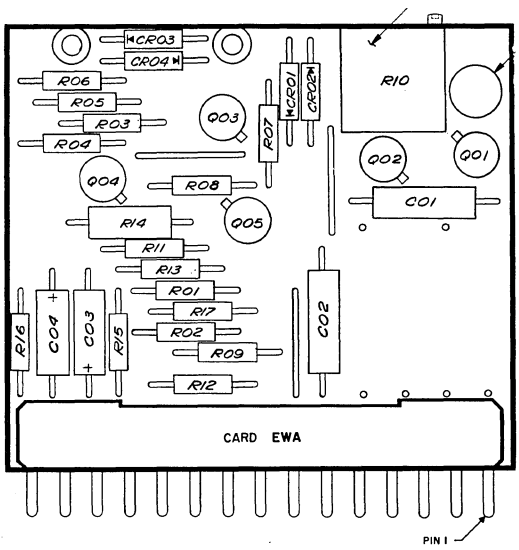
The values of C01 and C02 are changed for the EWC.

SYMBOL




+12V
R17 17.8K ±1%
R03 1.96K ±1%
C01 .01
Q01
R01 28.7K ±1%
R10 200 1W
R12 820
Q05
R11 560
R13 470
-12V
R02 28.7K ±1%
C02 01
Q02
R04 1.96K ±1%
R09 17.8K ±1%
+12V
CR01
CR02
+12V
R05 1K ±1%
Q03
R07 51.1 ±1%
R14 2.2K 1/2W
-12V
R08 51.1 ±1%
Q04
R06 1K ±1%
+12V
TP-A
TP-C
CR03
CR04
11
12
1
2
3
4
-12V
R15 270
C03 15 ±20%
C04 15 ±20%
+12V
R16 390
13
14
15
NOTE:
1. ALL DIODES ARE SILICON 92115021.
2. COMPONENT ASS'Y NO. 50018200.
3. ALL TRANSISTORS ARE NPN, SILICON, 50210102.
4. EWC 1500 PF

EWA, EWC


CR03
CR04
R06
R05
R03
R04
Q03
R07
CR01
CR02
R10
Q02
Q01
Q04
R08
C01
Q05
R14
R11
R13
R01
R17
R02
R09
R12
R16
C04
C03
R15
C02
CARD EWA
PIN 1

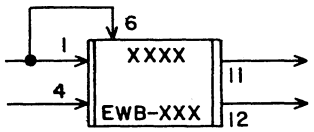
# PEAK DETECTOR
## EWB

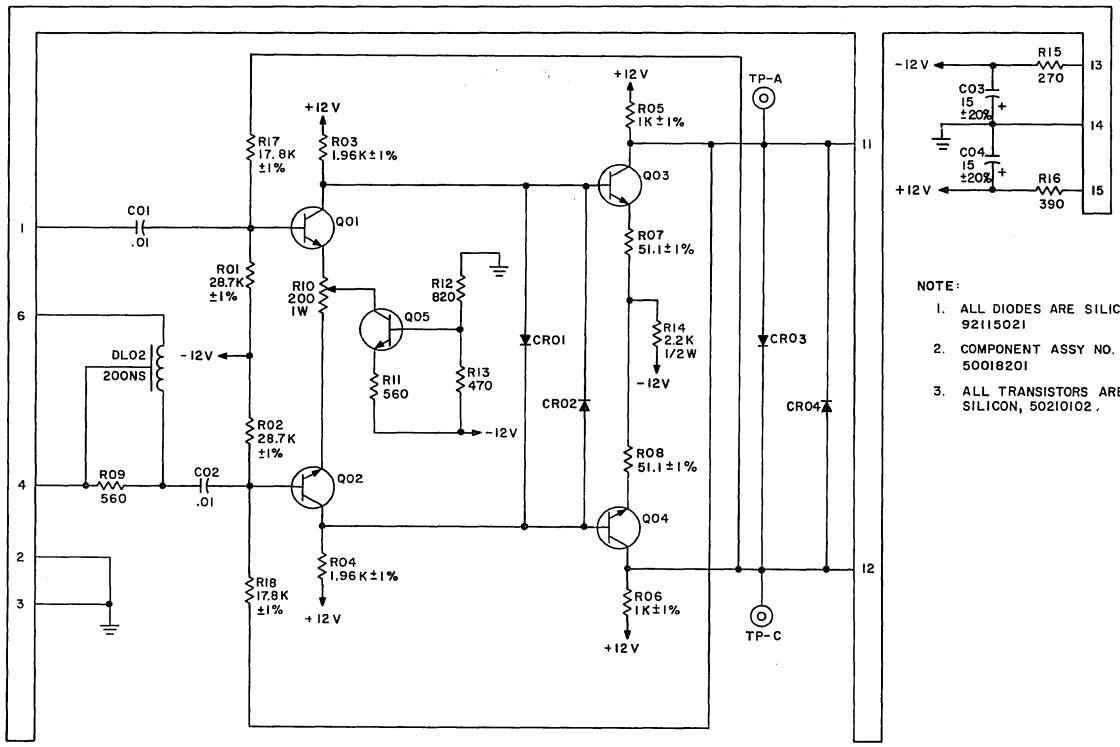
The EWB card detects peaks in read data; its output is a rectangular pulse.

The circuit uses a delay line and a differential amplifier to serve as a peak detector. The differential signal from a EUC card is applied to pins 1 and 4. The signal at pin 1 is applied directly through C01 to one base of the first differential stage. This signal is also delayed through DL02, then applied through C02 to the other base of the differential stage. The more positive base will turn on that transistor, and either CR01 and CR02 will be on. When the other base goes more positive, the other diode of the CR01 - CR02 pair will come on. The second differential stage sharpens up the resultant rectangular wave, since the voltage gain is one. Either CR03 or CR04 is on, so the output between pin 11 and pin 12 is a rectangular wave of 0.6v, centered around +8v.

Pins 1 and 6 must be tied together. Resistor R10 is adjusted for symmetrical operation over an amplitude range of input signals. The circuit tends to oscillate if the input frequency is greater than $\frac{1}{2\ (\text{delay time})}$.

SYMBOL

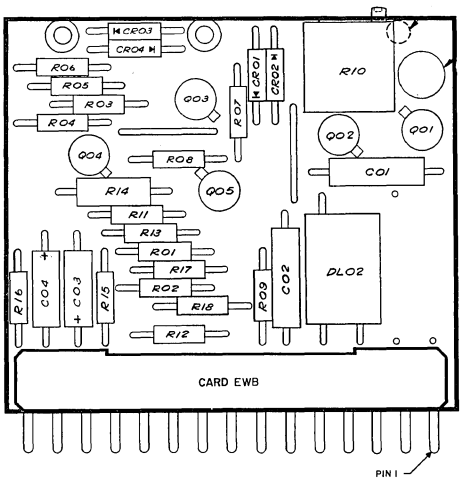





NOTE:

1. ALL DIODES ARE SILICON 92115021
2. COMPONENT ASSY NO. 50018201
3. ALL TRANSISTORS ARE SILICON, 50210102.

EWB



AGC ATTENUATOR

EZA

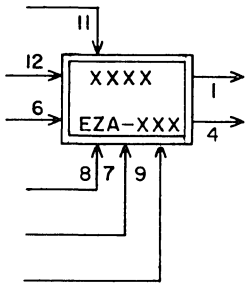
The EZA card attentuates the read signals applied to pins 11 and 12 in accordance with the control signal at pin 9, which comes from the FYA card. R07, R08, R09, and R10 present the proper load to the preceding card. Q03 and Q04 are emitter followers to reduce the load on the preceding card, and to present a low source impedance to CR01 and CR02.

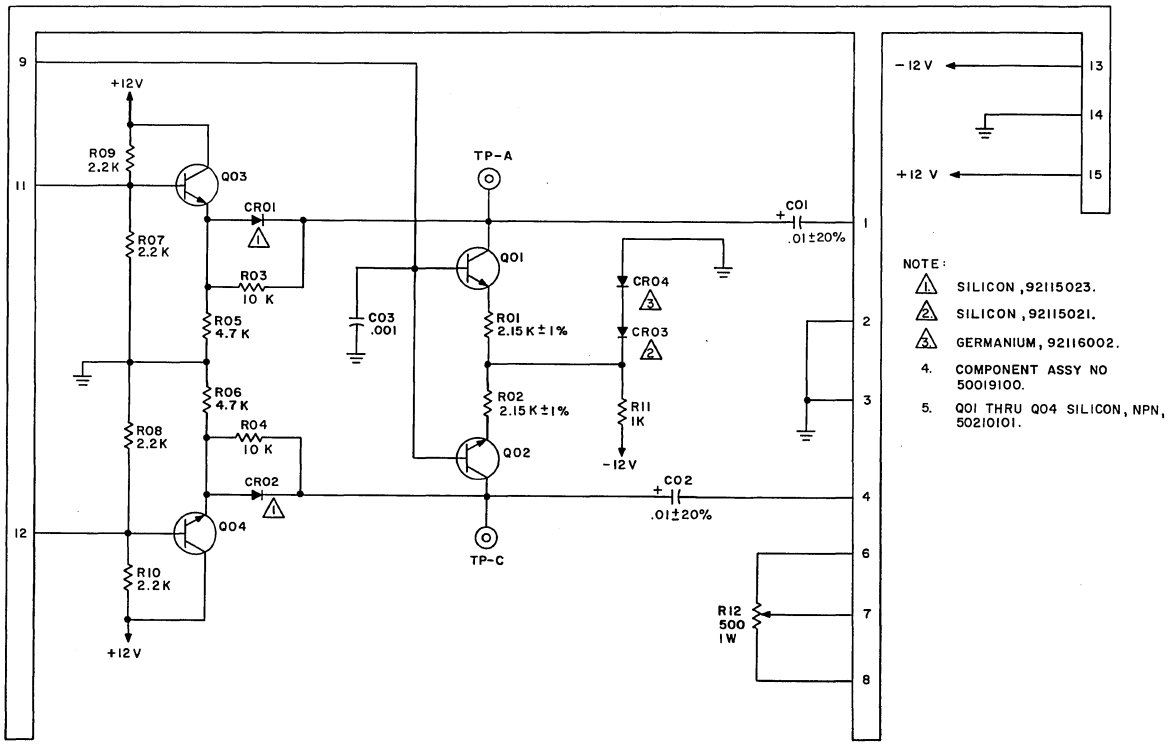
Q01 and Q02 control the bias current through CR01 and CR02 in accordance with the dc signal on pin 9. The dynamic impedance of CR01 and CR02 varies inversely with the bias current through them. When the dynamic impedance of the two diodes is large compared to the input impedance of the next card, the signal presented to the next card at pins 1 and 4 is small compared to the input signal at pins 11 and 12. When the dynamic impedance is small, the input signal is passed to the output pins unattenuated.

If the input signals are large, they may be distorted, since the impedance vs bias current curve of the diodes is not linear. If signals are on the order of 100 mv peak-to-peak, the distortion is minimized.

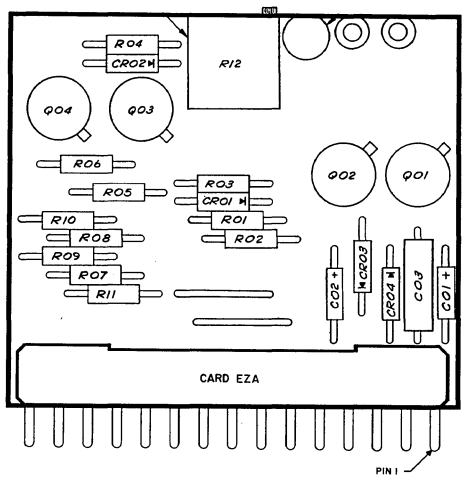
R12 is used at a different point in the 852 Disc Pak read chain.

SYMBOL




9
11
12
+12V
R09 2.2K
Q03
CR01
R07 2.2K
R03 10 K
R05 4.7 K
R06 4.7K
R08 2.2K
R04 10 K
CR02
Q04
R10 2.2K
+12V
TP-A
C03 .001
Q01
R01 2.15K ± 1%
R02 2.15K ± 1%
Q02
TP-C
CR04
CR03
R11 1K
-12V
C01 .01 ±20%
C02 .01 ±20%
R12 500 1W
1
2
3
4
6
7
8
-12 V
+12 V
13
14
15
NOTE:
1. SILICON, 92115023.
2. SILICON, 92115021.
3. GERMANIUM, 92116002.
4. COMPONENT ASSY NO 50019100.
5. Q01 THRU Q04 SILICON, NPN, 50210101.

EZA


R04
CR02
R12
Q04
Q03
R06
R05
R10
R08
R09
R07
R11
R03
CR01
R01
R02
Q02
Q01
CR03
CR04
C03
C02
C01
CARD EZA
PIN 1

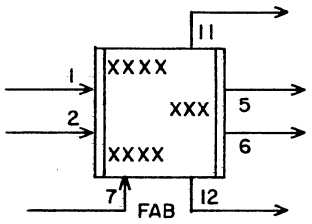
SHAPER FLIP-FLOP
FAB

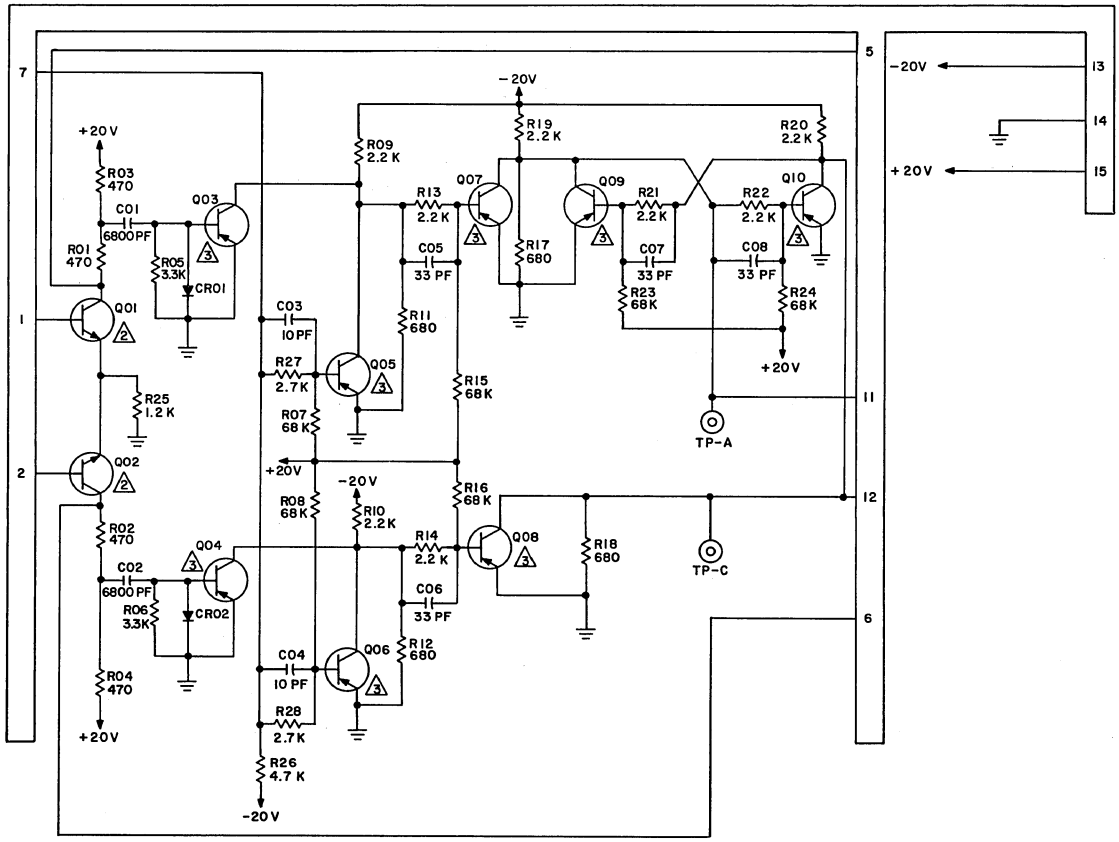
The FAB card transfers the EWA/B card output into a flip-flop, unless pin 7 is at logic one (-3V). Output pins do not have logic AND diodes.

The EWA/B card output, operating around +8v, is applied to pins 1 and 2. It is amplified and goes out on pins 5 and 6. It is also passed through C01 and C02, which cause Q03 or Q04 to turn on for negative-going edges. Positive going edges are dissipated in CR01 and CR02. The signals at the collectors of Q03 and Q04 are applied to Q07, Q08, Q09, and Q10, which constitute a flip-flop. Thus, each change of state at the output of the EWA/B card causes the flip-flop to change its state. Note that there are no AND diodes at the outputs from the flip-flop, pins 11 and 12.

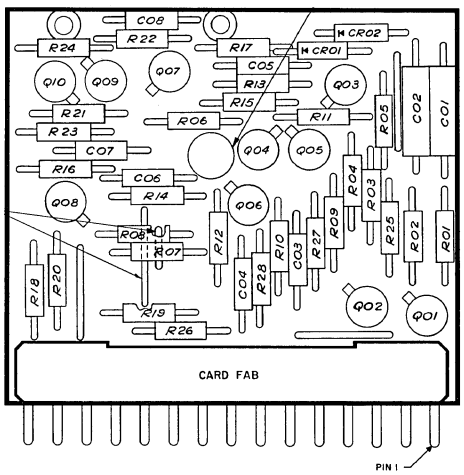
If pin 7 is at ground, the operation of the circuit is as described. If pin 7 is at -3V, Q05, and Q06 turn on, which keeps the flip-flop from responding to inputs on pins 1 and 2. Thus, pin 7 enables or disables the circuit.

SYMBOL




7
1
2
5
11
12
6
-20V
13
14
+20V
15
+20V
R03 470
C01 6800PF
R01 470
R05 3.3K
CR01
Q03
Q01
R25 1.2K
Q02
R02 470
C02 6800PF
R06 3.3K
CR02
Q04
R04 470
+20V
R09 2.2K
R19 2.2K
R20 2.2K
Q07
Q09
Q10
R13 2.2K
R21 2.2K
R22 2.2K
C05 33 PF
R17 680
C07 33 PF
C08 33 PF
R23 68K
R24 68K
+20V
R11 680
C03 10PF
R27 2.7K
Q05
R15 68K
R07 68K
TP-A
+20V
-20V
R08 68K
R10 2.2K
R16 68K
R14 2.2K
Q08
R18 680
TP-C
C06 33 PF
C04 10 PF
R12 680
Q06
R28 2.7K
R26 4.7 K
-20V

FAB


C08
R22
R24
R17
CR02
CR01
C05
R13
Q10
Q09
Q07
Q03
R21
R15
R06
R11
R23
C07
R16
Q04
Q05
C06
R14
Q08
Q06
R08
R07
R12
R10
C03
R27
R09
R04
R03
R25
R02
R01
C02
C01
R05
R18
R20
C04
R28
R19
R26
Q02
Q01
CARD FAB
PIN 1

# INNER AND OUTER TRACK SELECT AND SUMMING NETWORKS FCA, FCB, FCC, FCD, FCE

These cards contain resistor networks which are used in the coarse control (long stroke) mode of the disk file servo actuator. Each circuit has four input lines and one output line. The output line is common to all inputs via an appropriate resistor. This output line is normally connected to the summing point of the long stroke position operational amplifier. When a voltage of ±8v is applied from a JBA or JCA card to one of the input pins (1 through 4), a current flows through the resistor and into the summing point. The current level is trimmed by the appropriate potentiometer. This current represents the coarse command to the servo actuator for ultimate positioning at one of 14 locations (for the FCA and FCB code) or one of 20 locations (for the FCC, FCD, and FCE codes).

## FCA, FCB

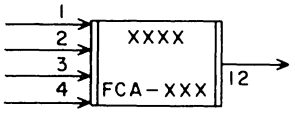
The four farthest locations from the midpoint between locations 6 and 8 are termed "outer" tracks, and the three closest locations are termed "inner" tracks. The FCA card is used for the "outer" locations, and the FCB card for the "inner" locations.

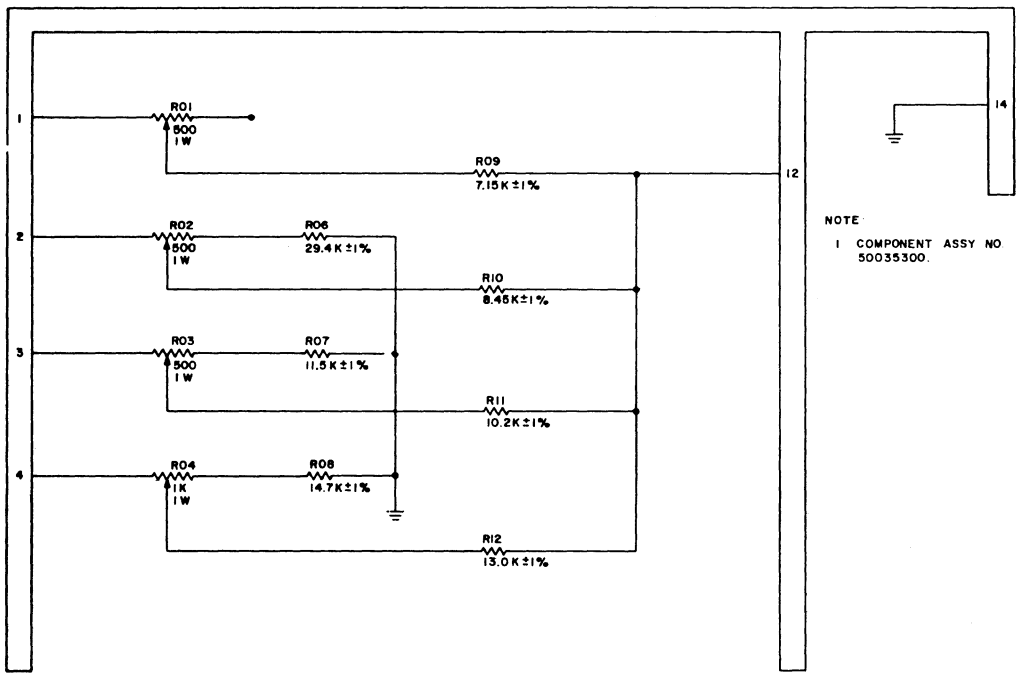
Pin number 4 on the FCB card is used for modifying the coarse control signal when positioning ±0.020 inches on either side of the 14 main locations. There are 3 tracks at each location.

## FCC, FCD, FCE

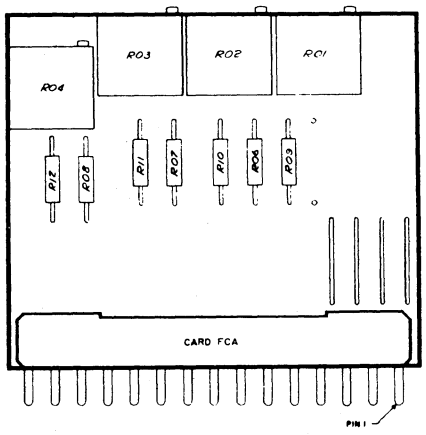
The four farthest locations on either side of the midpoint of the recording surface are set by the FCC card. The next four locations on either side and toward the middle of the disk are set by the FCD card. The FCE card sets the remaining two locations on either side and adjacent to the midpoint of the disk, and also modifies the coarse control signal by ±0.0075 and ±0.0225 inches either side of the 20 main track positions.

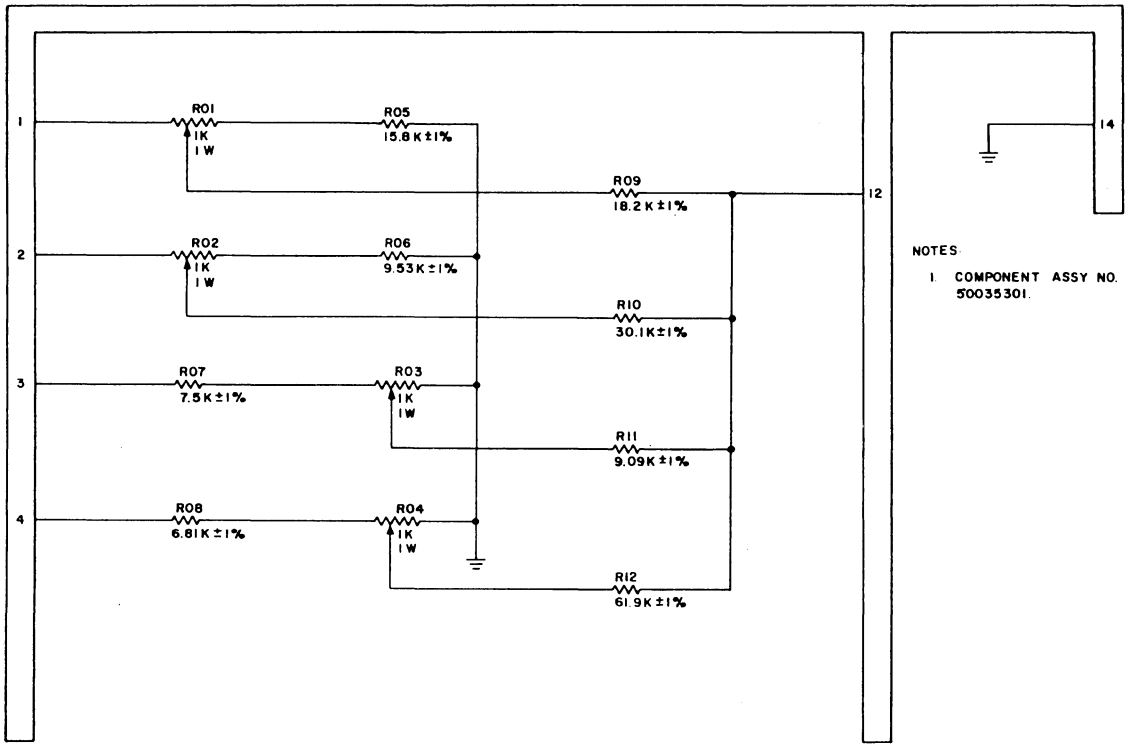
SYMBOL



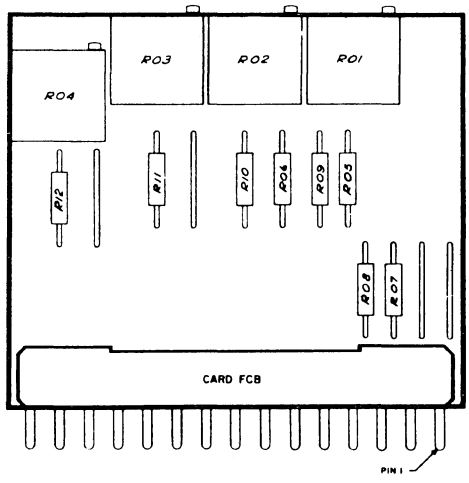

1
2
3
4
R01
500
1W
R02
500
1W
R03
500
1W
R04
1K
1W
R06
29.4K±1%
R07
11.5K±1%
R08
14.7K±1%
R09
7.15K±1%
R10
8.45K±1%
R11
10.2K±1%
R12
13.0K±1%
12
14
NOTE
1 COMPONENT ASSY NO. 50035300.

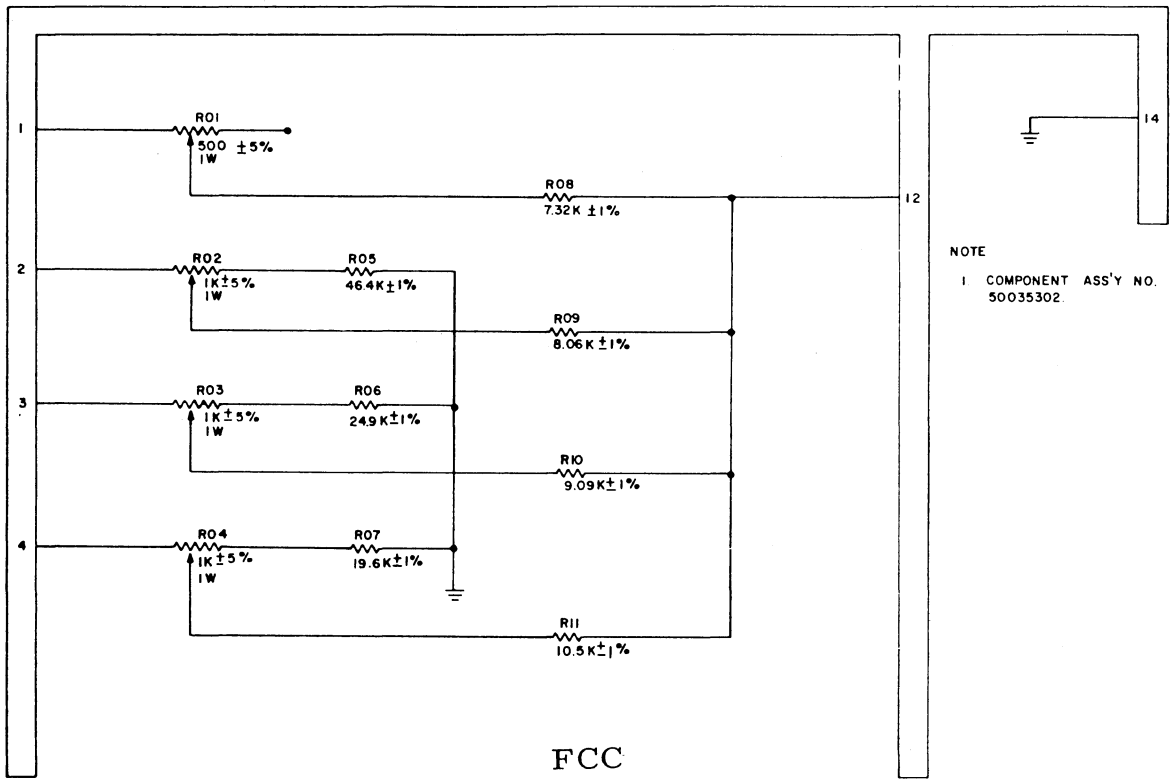
FCA


R04
R03
R02
R01
R12
R08
R11
R07
R10
R06
R03
CARD FCA
PIN 1

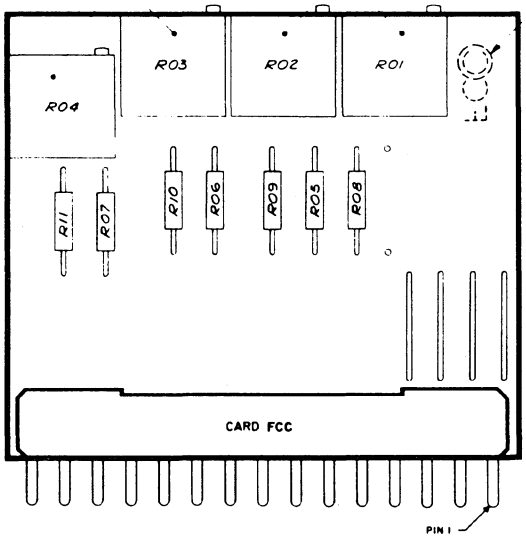

1
2
3
4
R01
1K
1W
R05
15.8K±1%
R09
18.2K±1%
12
14
R02
1K
1W
R06
9.53K±1%
R10
30.1K±1%
R07
7.5K±1%
R03
1K
1W
R11
9.09K±1%
R08
6.81K±1%
R04
1K
1W
R12
61.9K±1%
NOTES:
1. COMPONENT ASSY NO. 50035301.

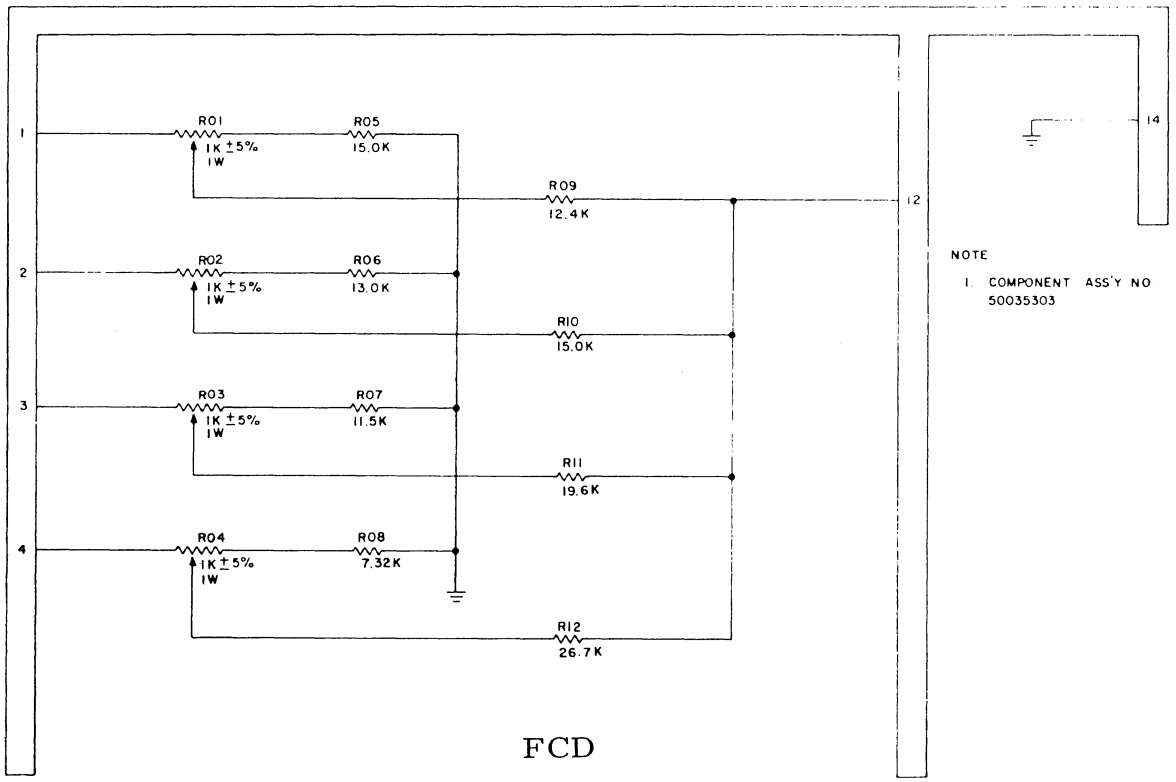
FCB


R03
R02
R01
R04
R12
R11
R10
R04
R09
R05
R08
R07
CARD FCB
PIN 1

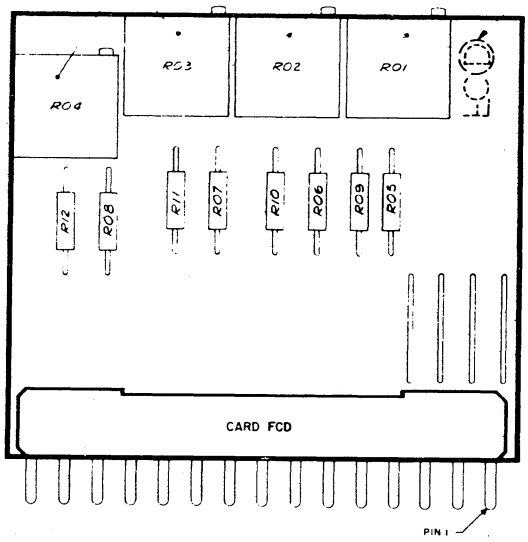

1
2
3
4
R01
500 ±5%
1W
R02
1K±5%
1W
R03
1K±5%
1W
R04
1K±5%
1W
R05
46.4K±1%
R06
24.9K±1%
R07
19.6K±1%
R08
7.32K ±1%
R09
8.06K ±1%
R10
9.09K±1%
R11
10.5K±1%
12
14
NOTE
1 COMPONENT ASS'Y NO. 50035302.

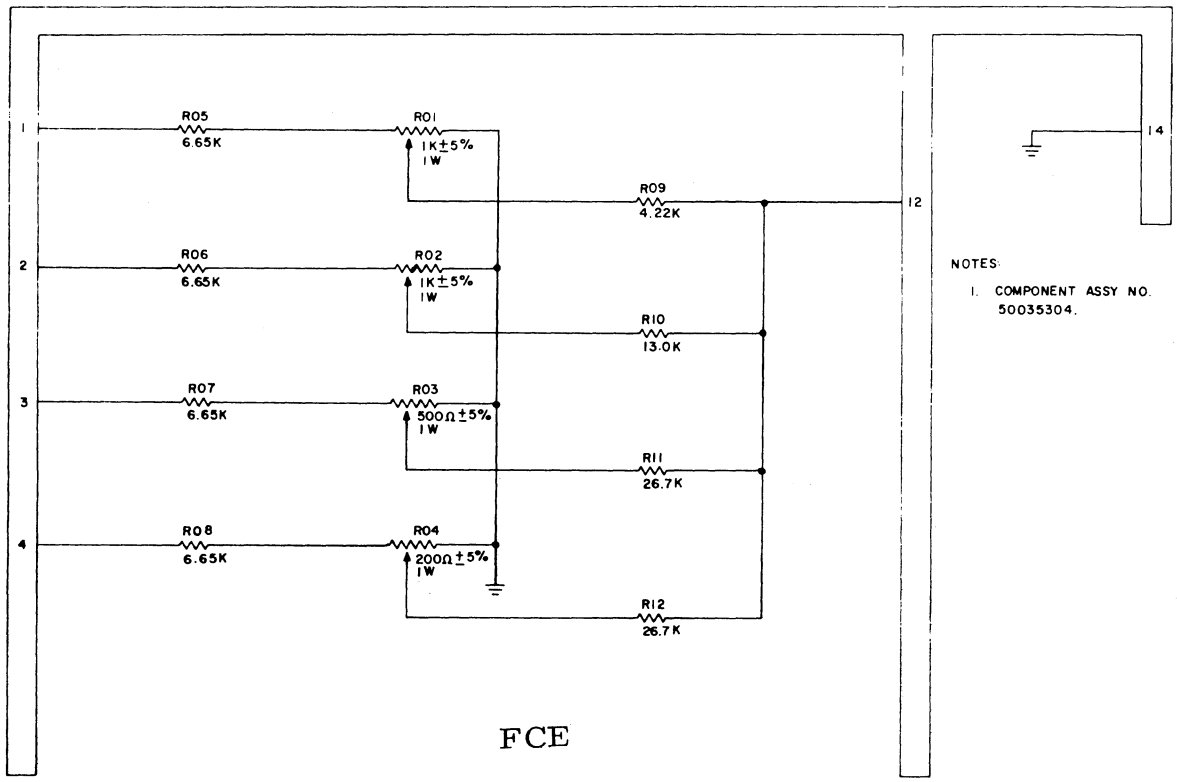
FCC


R03
R02
R01
R04
R11
R07
R10
R06
R09
R05
R08
CARD FCC
PIN 1

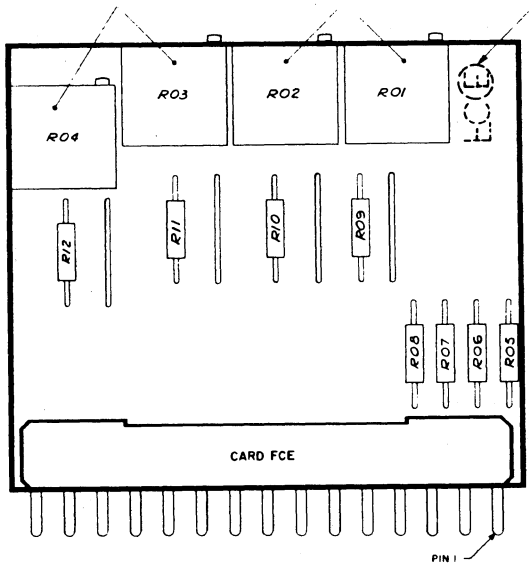

1
2
3
4
R01
1K ±5%
1W
R05
15.0K
R09
12.4K
12
14
R02
1K ±5%
1W
R06
13.0K
R10
15.0K
R03
1K ±5%
1W
R07
11.5K
R11
19.6K
R04
1K ±5%
1W
R08
7.32K
R12
26.7K
NOTE
1. COMPONENT ASS'Y NO
50035303

FCD


R03
R02
R01
R04
R12
R08
R11
R07
R10
R06
R09
R05
CARD FCD
PIN 1


1
2
3
4
R05
6.65K
R01
1K±5%
1W
R09
4.22K
12
14
R06
6.65K
R02
1K±5%
1W
R10
13.0K
R07
6.65K
R03
500Ω±5%
1W
R11
26.7K
R08
6.65K
R04
200Ω±5%
1W
R12
26.7K
NOTES:
1. COMPONENT ASSY NO. 50035304.

FCE


R04
R03
R02
R01
R12
R11
R10
R09
R05
R07
R06
R05
CARD FCE
PIN 1

## OSCILLATOR

### FDA

The FDA card provides a 10 KC signal which, when properly amplified, becomes the carrier for the long stroke and short stroke transducers in the disk file servo actuator. The 10 KC signal is also converted into a dc reference voltage for the servo.

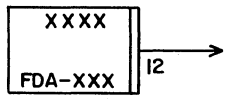
The oscillator contains an amplifying stage consisting of transistors Q01 and Q03. The output of Q03 goes to two other circuits; one containing a twin tee network and Q04, and the other containing another stage of amplification (Q02) and the amplitude regulating circuit (Q05).

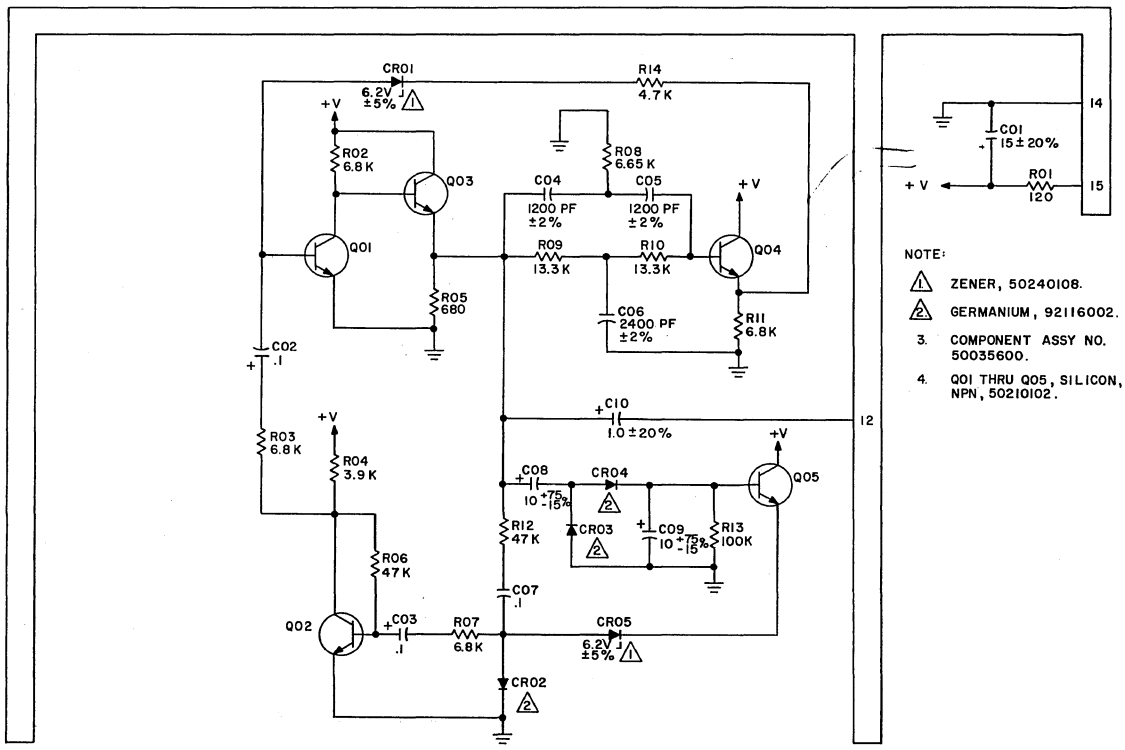
Positive feedback, which provides the necessary gain for oscillation, is provided by the two amplifying stages (Q01 and Q02). The frequency selective portion is provided by the negative feedback loop containing the twin tee, Q04, CR01, and R14. Zener diode CR01 provides dc coupling for stability.

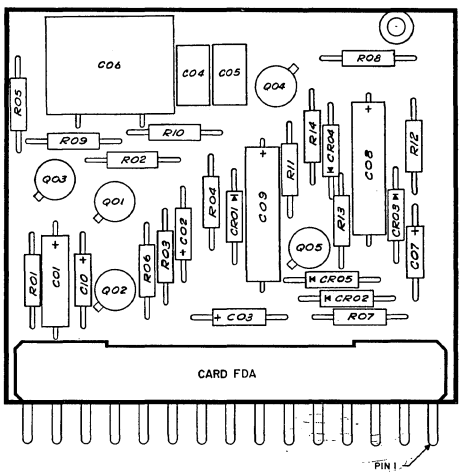
The twin tee has a null frequency of 10 KC. At this frequency no signal passes through the network, hence there is no negative feedback. At all other frequencies there is considerable negative feedback. The result of the two feedback paths is that there is positive feedback for 10 KC and negative feedback outside of a small band of frequencies as determined by the Q factor of the twin tee.

The amplitude regulating portion of the circuit consists of a voltage doubler (C08, C09, CR03, and CR04), and the emitter follower (Q05). The signal from Q03 is fed to Q02 via R12, C07, CR02, and the base network (C03 and R07). If diode CR02 is biased more or less, its impedance is decreased or increased, and therby controls the signal into Q02. The diode current is the emitter current of Q05 and is controlled by the base voltage, which is proportional to the signal. Therefore, if the output voltage rises, the base voltage and emitter current of Q05 increases. Diode CR02 current goes up and its impedance goes down. Consequently, the portion of the signal to Q02 goes down, which lowers the drive to Q01 and brings the output back down to the controlled level. This level is established by diode drop CR02, zener diode CR05, and the base-emitter drop of Q05. This is approximately 7v at the base of Q05, which is twice the peak output voltage.

SYMBOL


XXXX
FDA-XXX
12


CR01
6.2V ±5% 1
R14
4.7K
+V
R02
6.8K
Q03
R08
6.65K
C04
1200 PF ±2%
C05
1200 PF ±2%
+V
Q01
R09
13.3K
R10
13.3K
Q04
R05
680
C06
2400 PF ±2%
R11
6.8K
C02
.1
+C10
1.0 ±20%
12
+V
R03
6.8K
+V
R04
3.9K
C08
10 +75 -15%
CR04
2
Q05
R12
47K
CR03
2
C09
10 +75 -15%
R13
100K
R06
47K
C07
.1
Q02
C03
.1
R07
6.8K
CR05
6.2V ±5% 1
CR02
2
14
C01
15±20%
+V
R01
120
15
NOTE:
1. ZENER, 50240108.
2. GERMANIUM, 92116002.
3. COMPONENT ASSY NO. 50035600.
4. Q01 THRU Q05, SILICON, NPN, 50210102.


C06
C04
C05
Q04
R08
R05
R09
R10
R02
Q03
Q01
R04
CR01
C09
R11
R14
CR04
C08
R12
R13
CR03
C07
R01
C01
C10
Q02
R06
R03
C02
Q05
CR05
CR02
C03
R07
CARD FDA
PIN 1

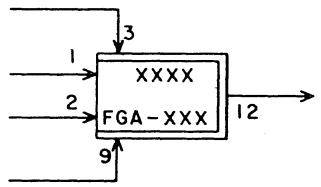
# CLAMP AND SUMMING
## FGA, FGB, FGC

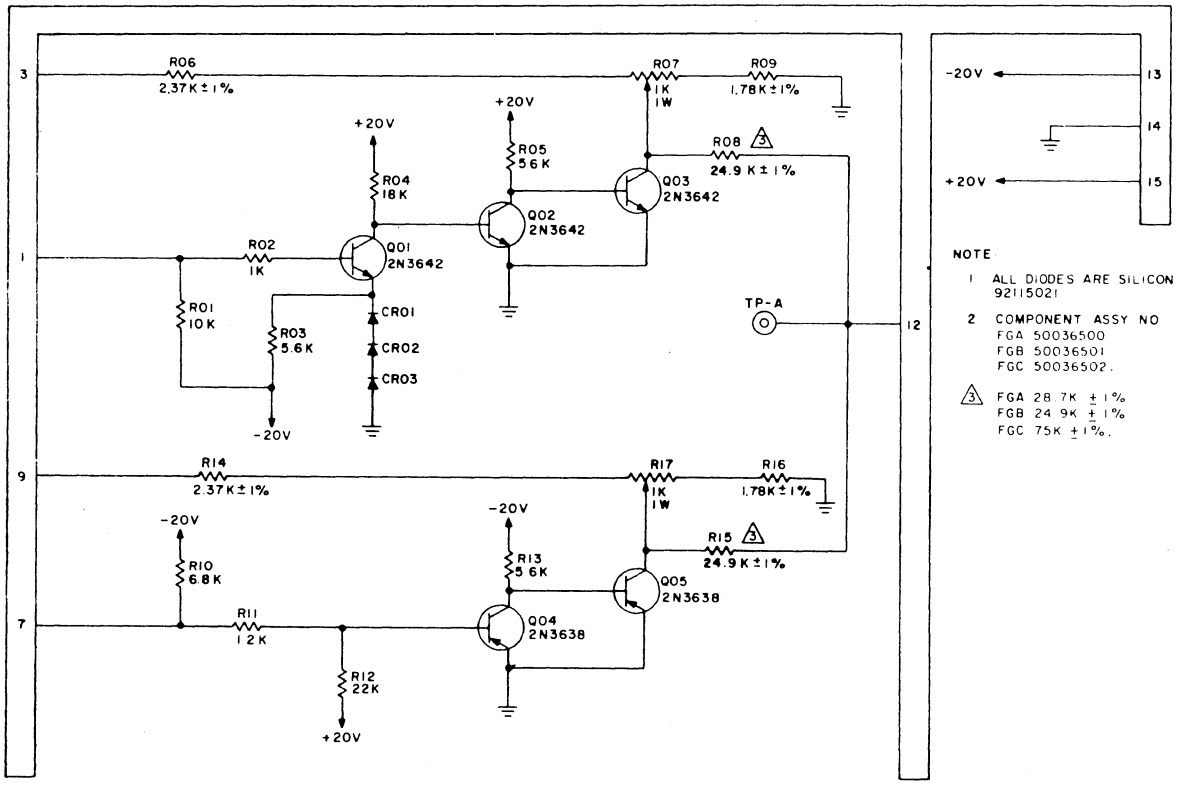
These cards are used in the disk file servo actuator fine control (short stroke) loop. The cards provide a current, which is summed with the short stroke signal, to provide positioning within ± 0.020 (FGA), ± 0.0225 (FGB), or ± 0.0075 inches (FGC) respectively on either side of a main track. The cards are identical except for the values of R08 and R15.

The circuit is provided with reference voltages of plus and minus 8v at pins 3 and 9 respectively. The output is taken from pin 12 and normally goes to the summing point, or virtual ground, of the short stroke operational amplifier. The output is a plus or minus short circuit current of approximately 125 ua, depending on whether Q03 or Q05 is on. A logical "1" on pin 1 turns Q01 off, Q02 on, and Q03 off, giving a plus current out. A logical "1" on pin 2 turns Q04 on and Q05 off, giving a minus current out.

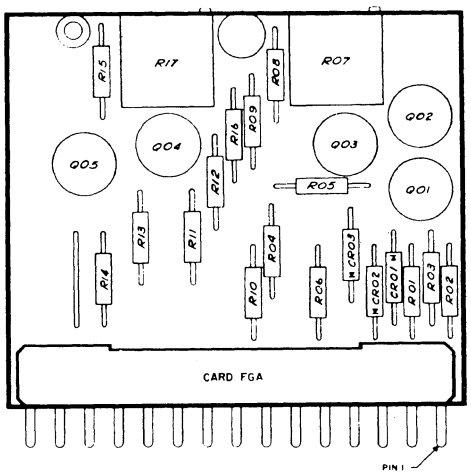
Timmer potentiometers R07 and R17 provide adjustment so the ± 0.020, ± 0.0225, or ± 0.0075 inches will be realized.

SYMBOL




R06
2.37K ± 1%
R07
1K
1W
R09
1.78K ± 1%
+20V
R05
5.6K
+20V
R04
18K
R08 3
24.9 K ± 1%
Q03
2N3642
Q02
2N3642
Q01
2N3642
R02
1K
R01
10K
R03
5.6K
CR01
CR02
CR03
-20V
TP-A
R14
2.37K ± 1%
R17
1K
1W
R16
1.78K ± 1%
-20V
R15 3
24.9K ± 1%
R13
5.6K
-20V
R10
6.8K
Q05
2N3638
R11
1.2K
Q04
2N3638
R12
22K
+20V
-20V
+20V
NOTE
1 ALL DIODES ARE SILICON 92115021
2 COMPONENT ASSY NO
FGA 50036500
FGB 50036501
FGC 50036502.
3 FGA 28.7K ± 1%
FGB 24.9K ± 1%
FGC 75K ± 1%.

FGA, FGB, FGC


R17
R07
R15
R08
R16
R09
Q02
Q04
Q03
R12
R05
Q05
Q01
R13
R11
R04
R14
R10
R06
CR03
CR02
CR01
R01
R03
R02
CARD FGA
PIN 1

# VALVE AMPLIFIER
## FHA

The FHA card is used in conjunction with a FMA card. They provide the control current to the short and long stroke valves in the disk file servo actuator.

The circuit is a feedback amplifier when used with the FMA card and the loop is closed with the valve. The valve is connected to pin 4 on the FHA card, and pin 6 on the FMA card. Pins 11 and 12 connect to pins 1 and 2 respectively on the FMA card. The closed loop current gain is 91 ma as given by the ratio of R12 to R13. Therefore, a voltage at pin 1 of $\pm$6.8v peak will give a 1 ma input current. This will cause the current through the valve to be approximately 91 ma.

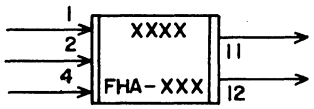
The circuit consists of the differential input stage, using a matched pair of transistors in a single TO-5 case. Potentiometer R03 allows the output current to be set at zero. Voltage applied to R03 is regulated by zener diodes CR01 and CR02. Therefore, no drift is introduced at this point. Transistors Q03 and Q04 are a Darlington pair in a common emitter circuit, whose collector load is the FMA card input impedance.

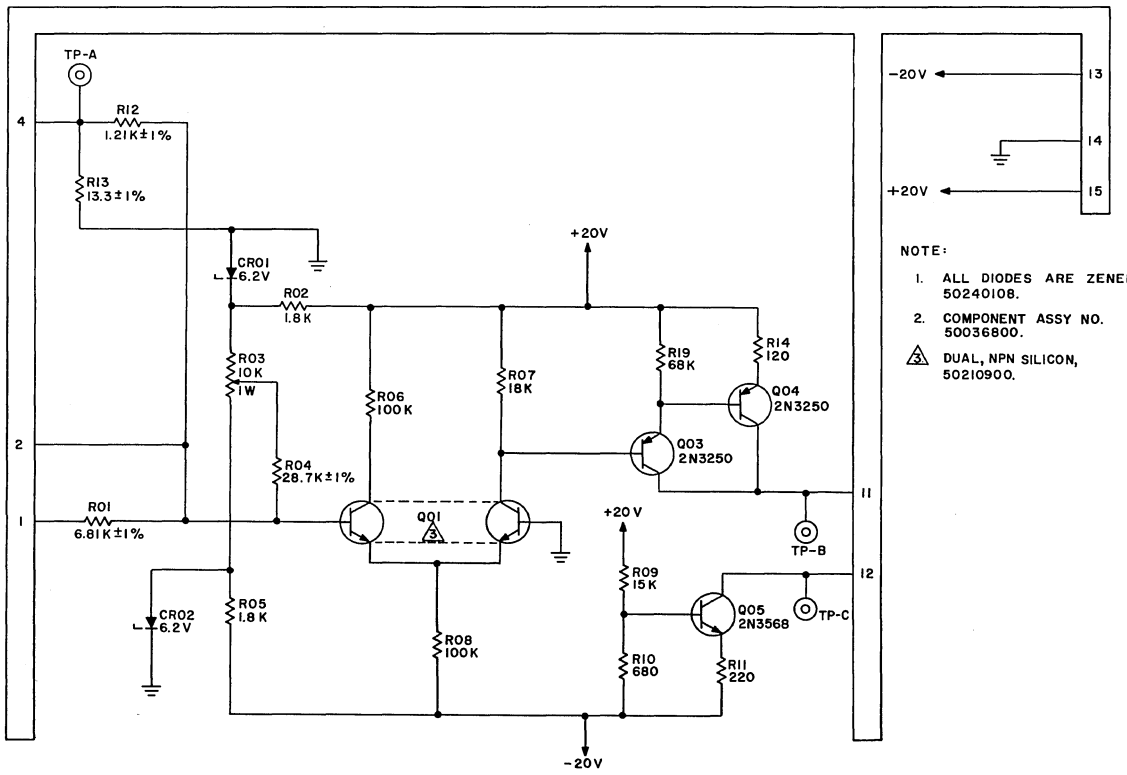
Transistor Q05 is a constant current generator, which supplies 5.2 ma nominally to diodes CR01 and CR02 on the FMA card. These diodes bias transistors Q01 and Q02 on the FMA card for class AB operation. By means of R03, the base drives to Q01 and Q02 (FMA) are adjusted to give a zero output. The current out of pin 11 is now equal to the current into pin 12 (assuming the transistors on card FMA are matched). If the input is driven positive, pin 11 goes positive and the collector current will increase on Q04. Since the current generator current is constant, the excess above 5.2 ma goes into positive drive for Q01 on the FMA card.

To obtain negative swings, the collector current on Q04 is reduced below 5.2 ma. Since Q05 requires 5.2 ma, the deficiency is made up by pulling current from ground through the base-emitter on card FMA.

For this combination of cards, the feedback is taken from a voltage proportional to the output current. As a result, the current through the valve will be sinusoidal for a sine wave input, but the voltage out of the FMA card will be determined by the load impedance. In this case the valve is a nonlinear inductor, so the voltage is very distorted.

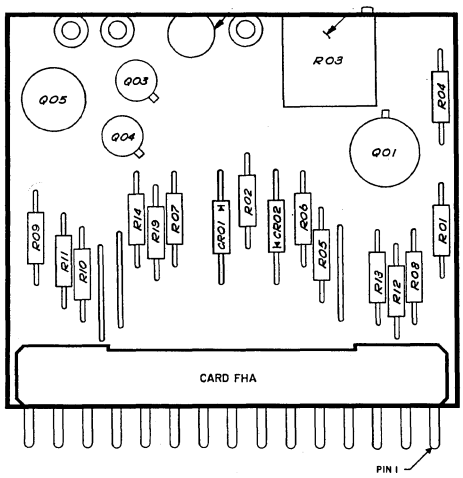
SYMBOL




NOTE:

1. ALL DIODES ARE ZENER 50240108.
2. COMPONENT ASSY NO. 50036800.
3. DUAL, NPN SILICON, 50210900.



POWER AMPLIFIER
FIA

This card is used with the output stage of the FMA card to form a 10 KC power amplifier. The FIA card is basically the same as the FHA card. However, it does not have a zero adjustment, and the feedback loop is modified to sense output voltage instead of current.

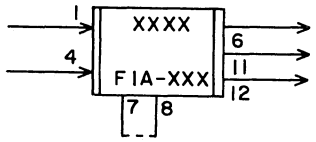
Pins 11 and 12 connect to pins 1 and 2 respectively on the FMA card. The output pin 6 of the FMA card connects to pin 4, and the output is taken off pin 6 (FIA). The load will be either a short stroke transducer and bridge rectifier, or a long stroke transformer and bridge rectifier. When the short stroke transducer load is used, it is necessary to jumper pins 7 and 8.

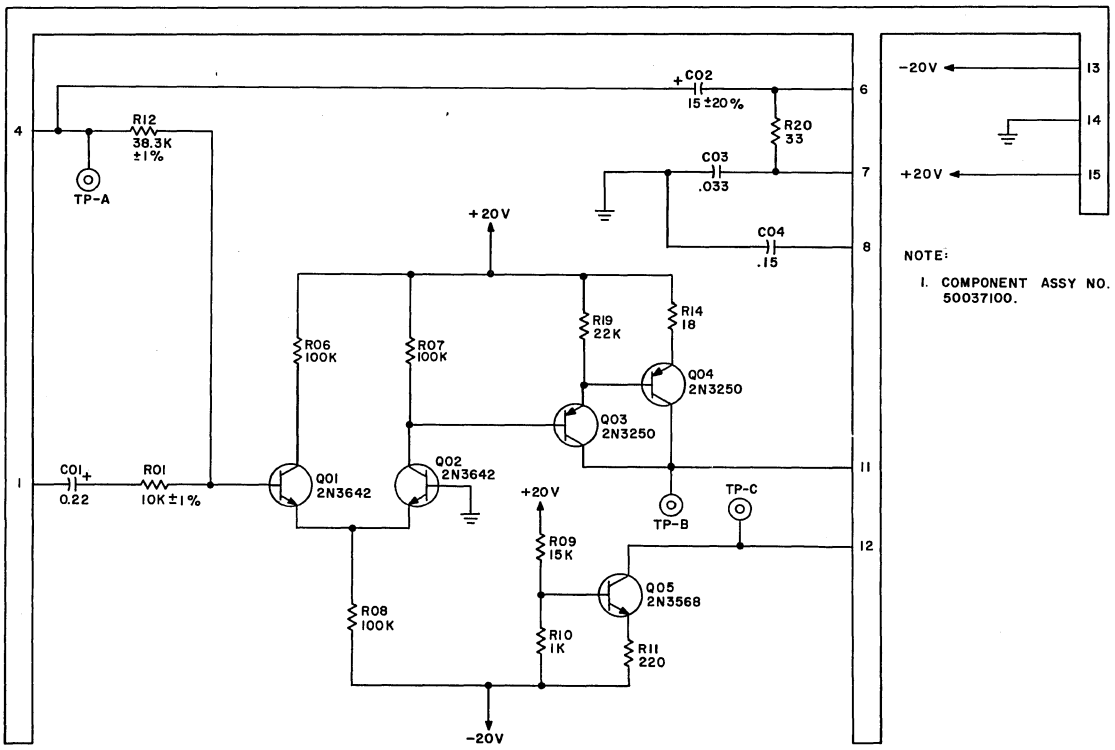
The circuit is a feedback amplifier with a voltage gain of 3.83v as determined by the ratio of R12 to R01. The 10 KC oscillator (card FDA) supplies approximately 3.5v peak to this circuit, so the output will be 13.4v peak. Since the circuit is ac coupled, a zero adjustment feature is not necessary.

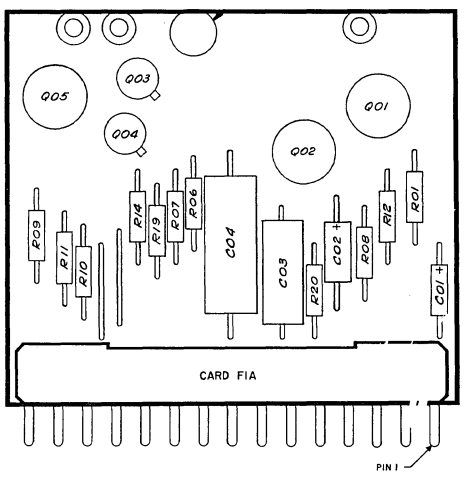
The circuit consists of a differential amplifier, transistors Q01 and Q02, and a Darlington pair (Q03 and Q04) in a common emitter configuration. These stages provide the necessary open loop gain. A current generator (Q05) is used to supply approximately 8.7 ma nominally to the FMA card diodes CR01 and CR02. These diodes bias transistors Q01 and Q02 (card FMA) for class AB operation. When the input voltage at pin 1 swings -3.5v, transistors Q03 and Q04 are driven so the collector current is greater than 8.7 ma. Since Q05 can only pass 8.7 ma, the excess becomes base drive for transistor Q01 (card FMA) and the output goes to +13.4v. If the input swings +3.5v, transistors Q03 and Q04 are driven less, so the collector current goes below 8.7 ma. However, Q05 still requires 8.7 ma, so the deficiency is made up by pulling current from ground through the transistor Q02 base-emitter junctions (card FMA). The output then goes to -13.4v.

The load on the FIA/FMA combination can be approximately 30v peak-to-peak into 150 ohms.

SYMBOL


1
4
XXXX
FIA-XXX
6
11
12
7
8


+C02
15 ±20%
R20
33
C03
.033
C04
.15
R12
38.3K
±1%
TP-A
+20V
R06
100K
R07
100K
R19
22K
R14
18
Q04
2N3250
Q03
2N3250
C01
0.22
R01
10K ±1%
Q01
2N3642
Q02
2N3642
TP-B
TP-C
R09
15K
Q05
2N3568
R08
100K
R10
1K
R11
220
-20V
-20V
+20V
NOTE:
1. COMPONENT ASSY NO. 50037100.


Q05
Q03
Q04
Q01
Q02
R09
R11
R10
R14
R19
R07
R06
C04
C03
R20
C02
R08
R12
R01
C01
CARD FIA
PIN 1

SERVO CYCLING GENERATOR

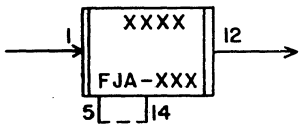
FJA

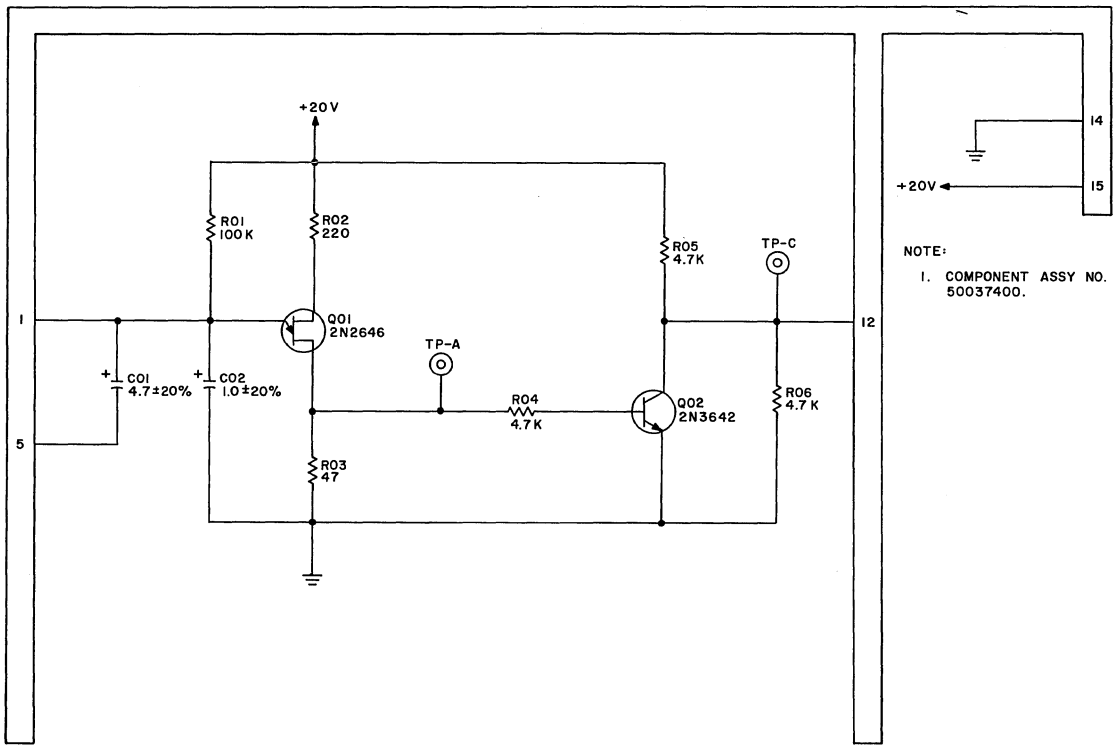
The FJA card is used to drive an OLA flip-flop card. The card generates a series of pulses for cycling the disk file servo actuator. This is necessary for maintenance purposes.

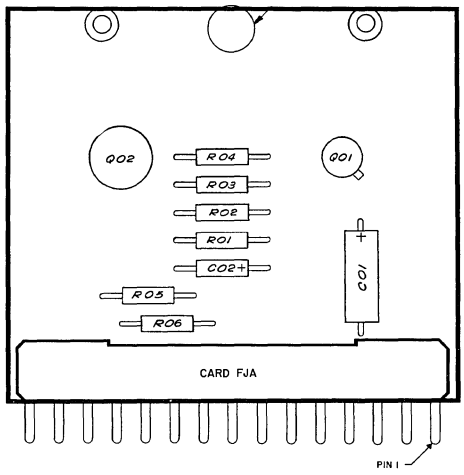
If input pin 1 is held at ground, unijunction transistor Q01 and transistor Q02 will be off. The output will be 10v.

When the input is opened, capacitor C02 (or C01 and C02 in parallel with pin 5 grounded) charges positive until a voltage of approximately 10v is reached. At this time the unijunction will fire, discharging the capacitor via the emitter to base 1 diode of Q01 and resistor R03. A positive pulse occurs across R03 which turns on Q02, driving the output from 10v to ground. The cycle will repeat as long as the input is open. The output is a series of negative going pulses approximately 50 to 100 usec wide. The pulses are spaced either 100 or 600 msec, depending on whether C02 is used, or C01 and C02 are used by grounding pin 5.

SYMBOL




+20V
R01
100K
R02
220
R05
4.7K
TP-C
Q01
2N2646
TP-A
C01
4.7±20%
C02
1.0±20%
R04
4.7K
Q02
2N3642
R06
4.7K
R03
47
1
5
12
14
15
+20V
NOTE:
1. COMPONENT ASSY NO. 50037400.


Q02
R04
R03
R02
R01
C02+
R05
R06
Q01
C01
CARD FJA
PIN 1

DEMODULATOR

FKA

The FKA card is used to convert an amplitude modulated 10 KC into a varying dc signal. This signal represents either coarse or fine position signals for the disk file servo actuator.

The input signal comes from either the short stroke or long stroke transducer. The transducer center tap goes to ground and the ends connect to pins 8 and 9. The output pin (pin 1) goes to the summing point of an operational amplifier.

When the short stroke or long stroke transducers are nulled, the voltage at pins 8 and 9 are equal in magnitude and opposite in phase. The voltages are applied to transformers T01 and T02, and are full wave rectified by the rectifiers in DA01. The voltage at test point A is then full wave positive, and at test point C full wave negative. Therefore, the output is at zero.

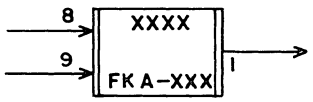
If the transducers are not nulled so the voltage at pin 8 is greater than at pin 9, the voltage at test point A is positive and greater by $+\Delta E$ than it was at null. At test point C the voltage is negative and less in magnitude (i.e. $+\Delta E$) than it was at null. The effect is that $+2\Delta E$ is realized across 10 K, or an equivalent of $\Delta E$ across 5 K.

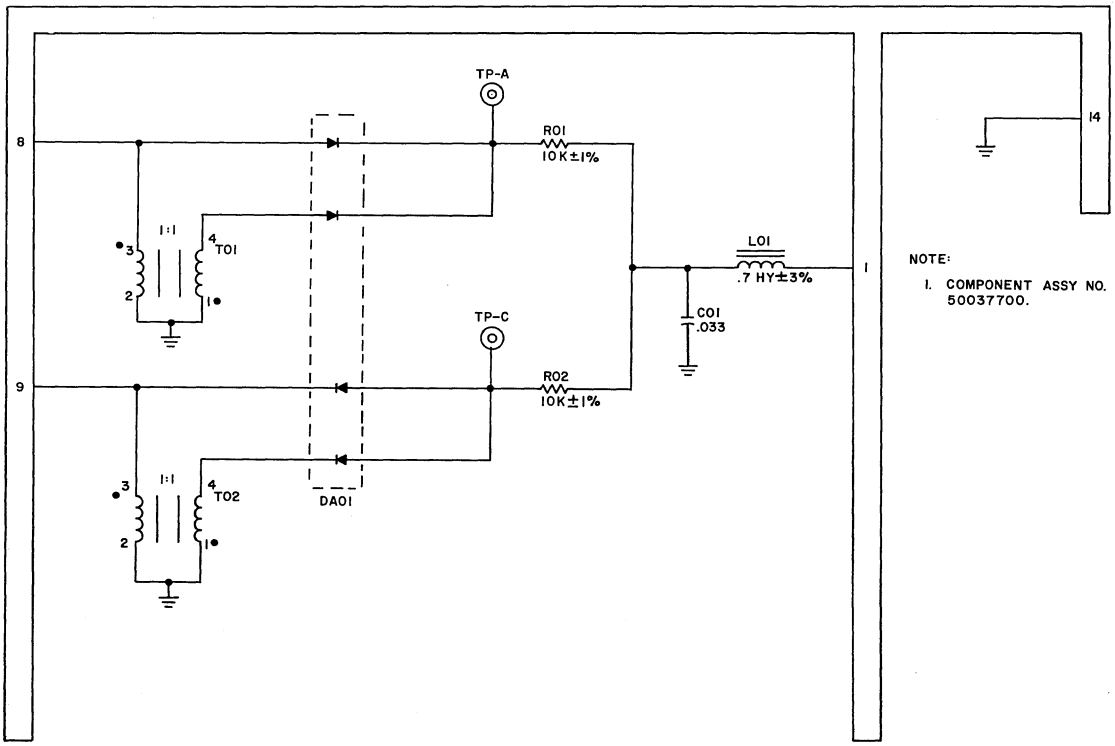
A filter composed of L01 and C01 has a cutoff frequency of approximately 1 KC to filter out the carrier and its harmonies, but pass dc and the modulation frequencies.

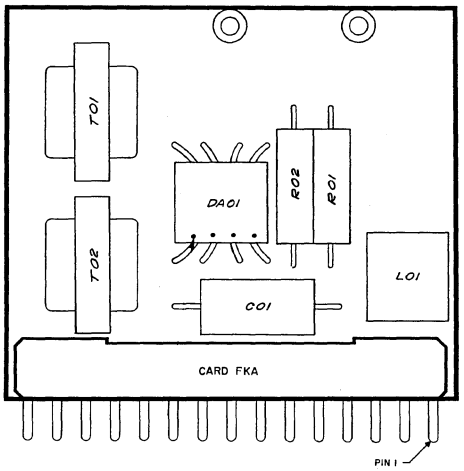
The circuit delivers approximately $\pm 1.4$ ma maximum.

NOTE: This card requires two card slots.

SYMBOL




TP-A
R01
10K±1%
8
14
1:1
4
T01
3
2
1
L01
.7 HY±3%
1
NOTE:
1. COMPONENT ASSY NO. 50037700.
C01
.033
TP-C
R02
10K±1%
9
3
1:1
4
T02
2
1
DA01


T01
T02
DA01
R02
R01
L01
C01
CARD FKA
PIN 1

BRIDGE RECTIFIER

FLA, FLB

The FLA and FLB cards provides a dc reference voltage to the long stroke and short stroke loops of the disk file servo actuator. The short circuit current is approximately 1.6 ma.

A 10 KC, 10 VRMS signal is applied to pins 1 and 2, and is full wave rectified by diodes CR01 through CR04. The LC filter converts the rectified wave to dc.

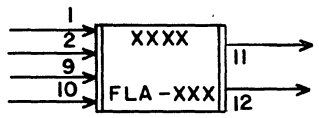
The FLA card uses a matched diode quad to obtain stability of the dc. Resistors R01 and R02 are part of the feedback network for the reference amplifier card (FPA). Diodes between pins 9 and 11, and pins 10 and 12, are used in the feedback network. They compensate for temperature effects in the rectifiers.

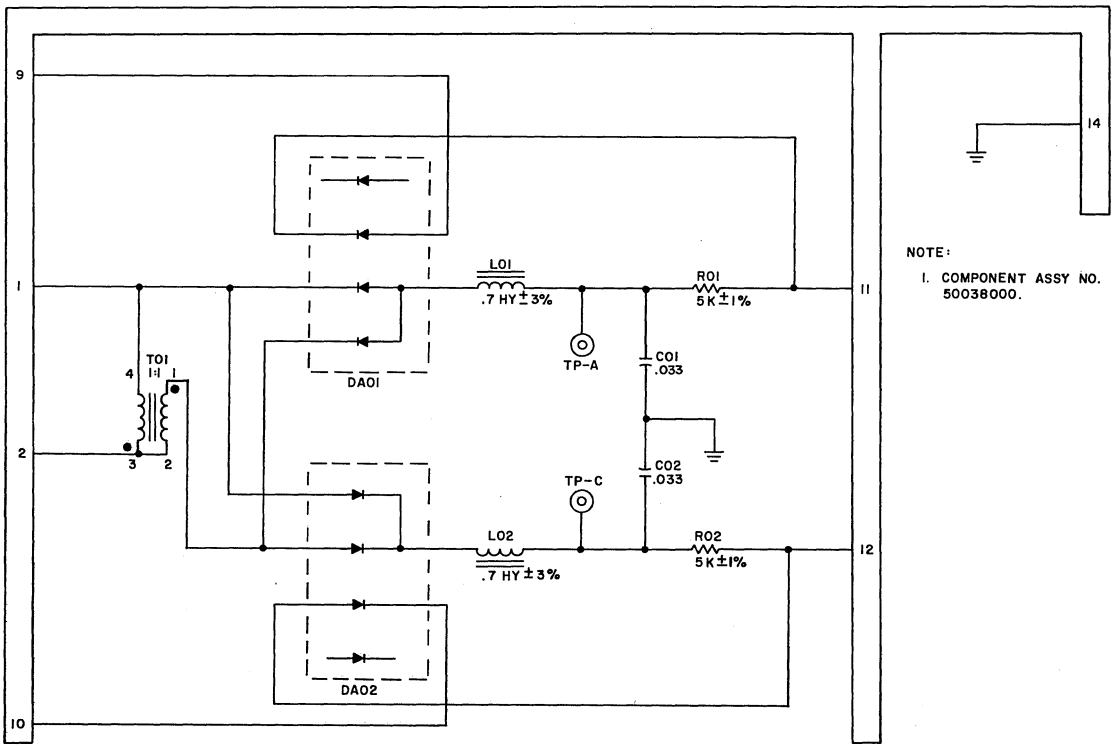
When used to drive a reference amplifier card (FPA), pin 11 connected to pin 1 on the FPA card will result in a plus reference voltage. Pin 9 must be connected to pin 2 on the FPA card to close the feedback loop. If a minus reference voltage is desired, pin 12 is connected to pin 1 (card FPA), and pin 10 is connected to pin 2 (card FPA) to close the feedback loop.

The FLB card does not contain the diodes between pins 9 and 11, and pins 10 and 12. Also, resistors R01 and R02 are replaced with jumpers. Pins 11 and 12 are connected to the load (card FGA, pins 9 and 3 respectively).

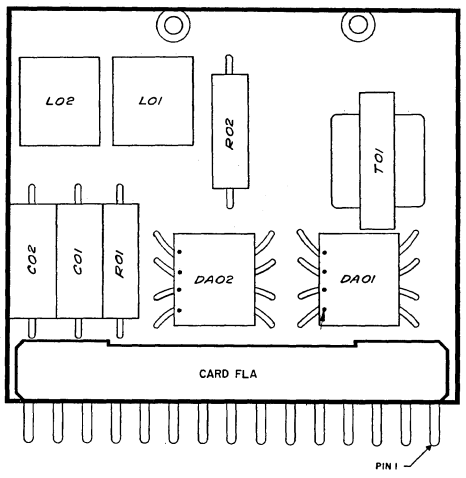
NOTE: This card requires two card slots.

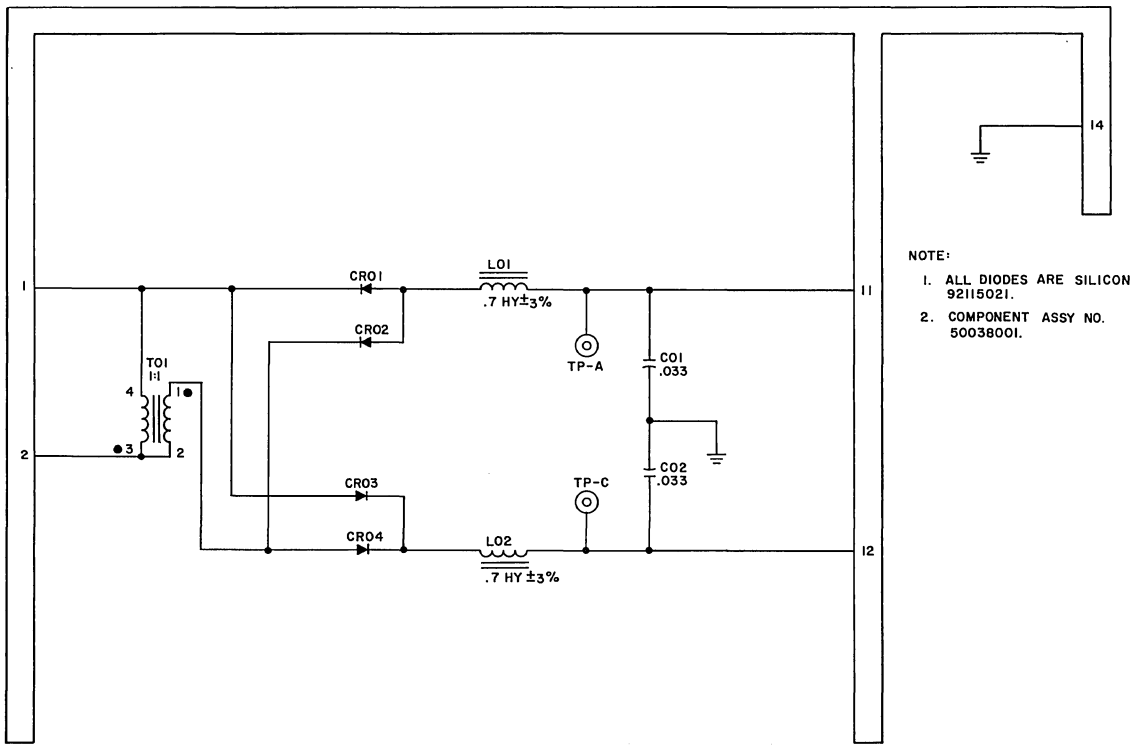
SYMBOL




9
1
2
10
11
12
14
LO1
.7 HY ± 3%
RO1
5K ± 1%
TP-A
CO1
.033
TO1
1:1
4
3
2
DAO1
CO2
.033
TP-C
LO2
.7 HY ± 3%
RO2
5K ± 1%
DAO2
NOTE:
1. COMPONENT ASSY NO. 50038000.

FLA

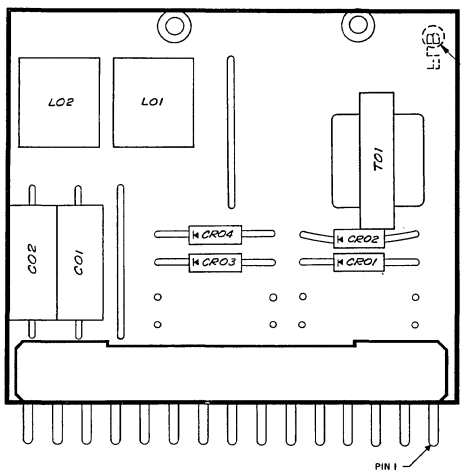

LO2
LO1
RO2
TO1
CO2
CO1
RO1
DAO2
DAO1
CARD FLA
PIN 1




NOTE:

1. ALL DIODES ARE SILICON 92115021.
2. COMPONENT ASSY NO. 5003800I.

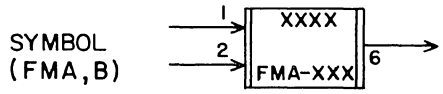
FLB

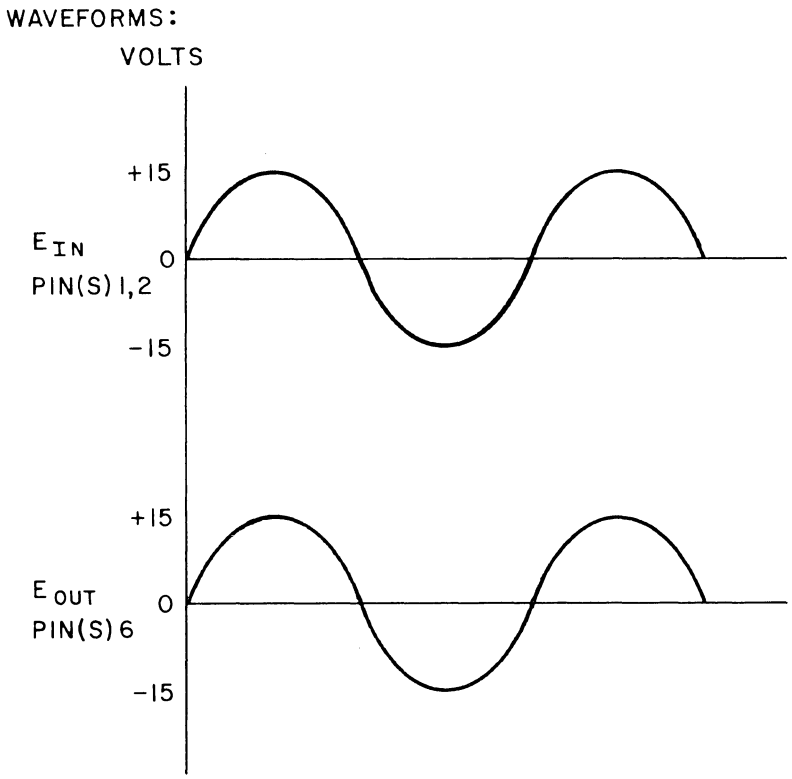


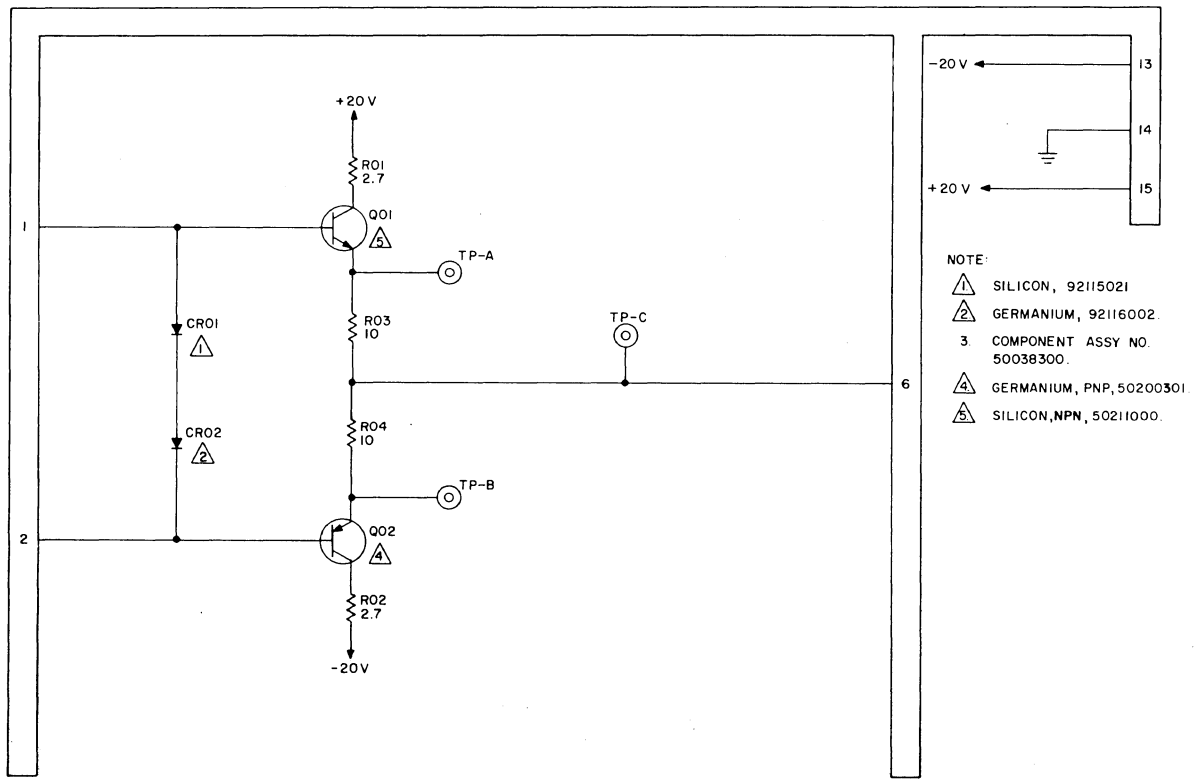
# POWER AMPLIFIER OUTPUT STAGE
## FMA, FMB

Each of these cards can be used as a power-output stage for the FHA, the FIA, or the FLA/B cards. Transistors Q01 and Q02 are direct-coupled, complementary, emitter followers operating approximately class AB when used with either the FHA or the FIA card. The output voltage at pin 6 is in phase with the input voltage at pins 1 and 2.

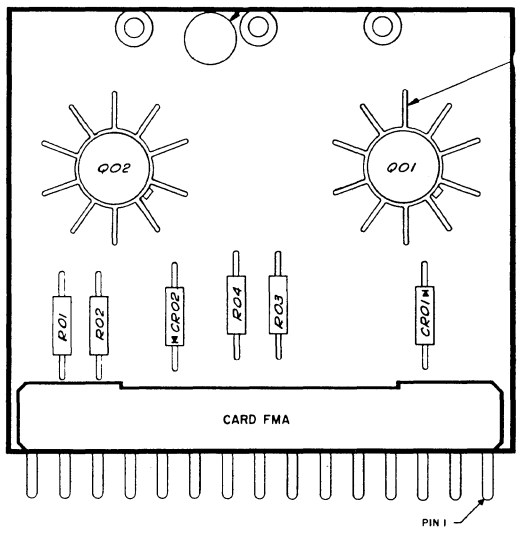
For information on input bias and output load conditions, refer to FHA and FIA circuit descriptions.

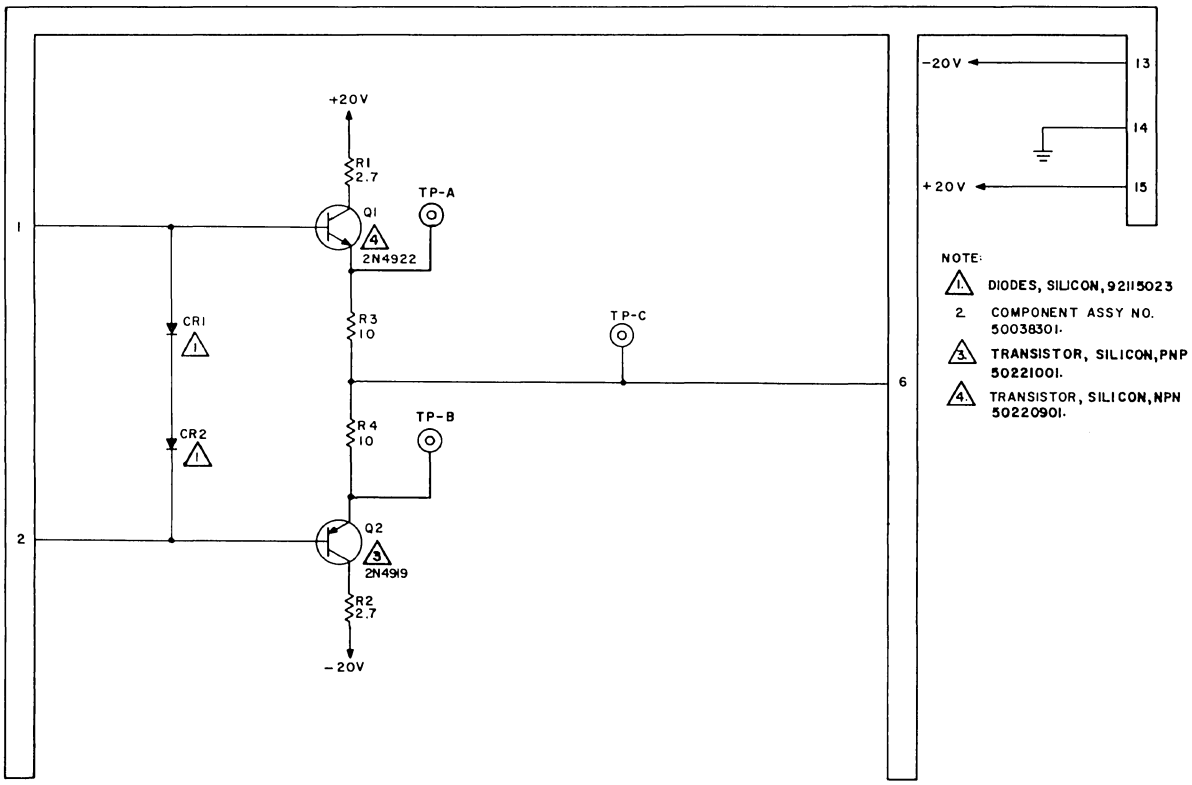


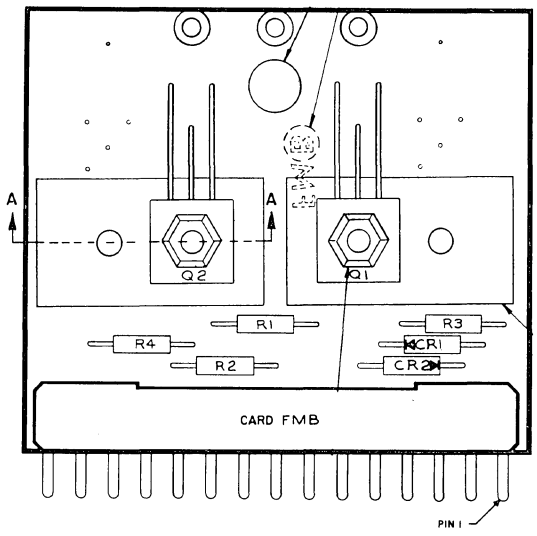

+20 V
R01
2.7
Q01
TP-A
R03
10
TP-C
CR01
CR02
R04
10
TP-B
Q02
R02
2.7
-20V
1
2
6
-20 V
13
14
+20 V
15
NOTE:
1 SILICON, 92115021
2 GERMANIUM, 92116002.
3 COMPONENT ASSY NO. 50038300.
4 GERMANIUM, PNP, 50200301
5 SILICON, NPN, 50211000.

FMA


Q02
Q01
R01
R02
CR02
R04
R03
CR01
CARD FMA
PIN 1


+20V
R1
2.7
TP-A
Q1
4
2N4922
1
CR1
1
R3
10
TP-C
6
CR2
1
R4
10
TP-B
2
Q2
3
2N4919
R2
2.7
-20V
-20V
13
14
+20V
15
NOTE:
1. DIODES, SILICON, 92115023
2. COMPONENT ASSY NO. 50038301.
3. TRANSISTOR, SILICON, PNP 50221001.
4. TRANSISTOR, SILICON, NPN 50220901.

FMB

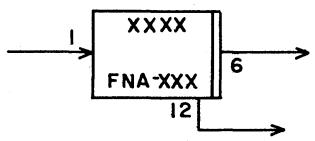

A
A
Q2
Q1
R1
R3
R4
CR1
R2
CR2
CARD FMB
PIN 1

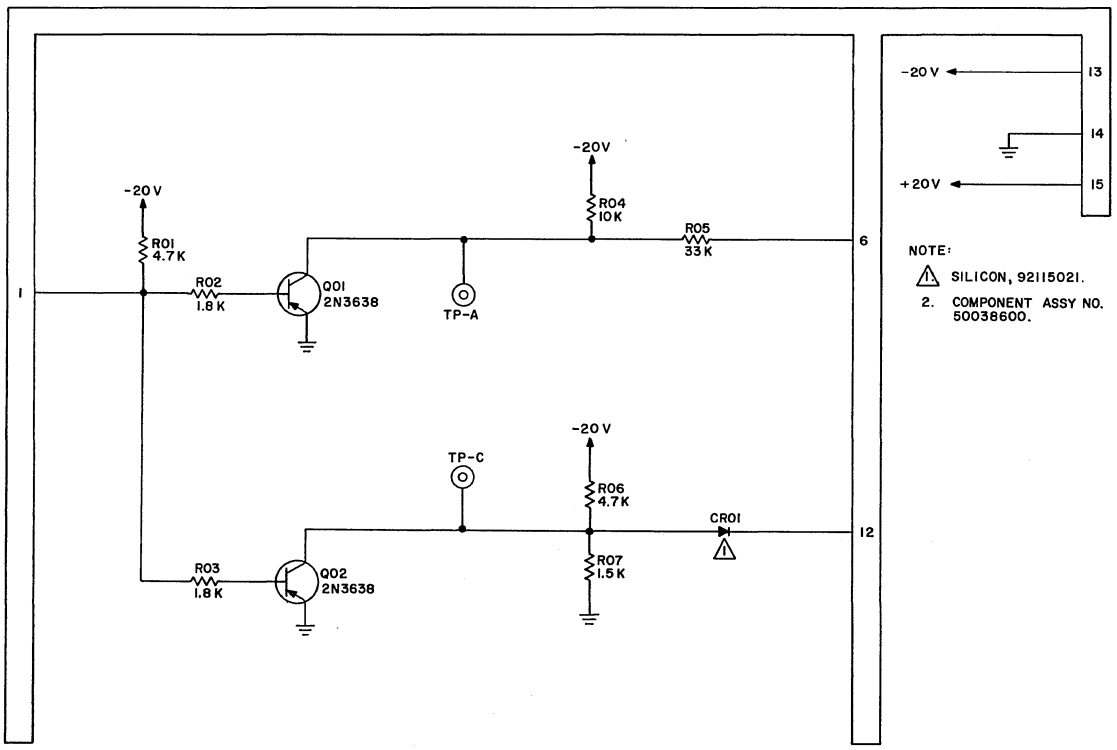
RETRACT INVERTER AND CURRENT SOURCE
FNA

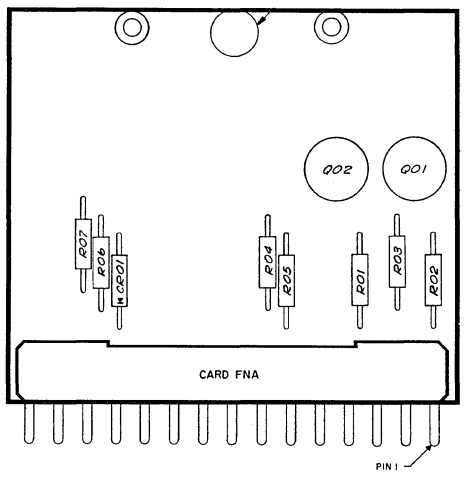
The FNA card is used in the disk file servo actuator. When supplied with relay contacts or logic signals, it causes the servo to retract the magnetic heads from between the disks.

The circuit is two common emitter switches with a common input and separate outputs. With the input pin 1 at ground (or logical "0"), the output at pin 6 provides a ½ ma short circuit current to an operational amplifier virtual ground or summing point; the output at pin 12 is -3v (or logical "1"). When the input is open (or logical "1"), transistors Q01 and Q02 are on (or logical "0"), so both outputs are at zero. This circuit is normally driven from a set of relay contacts, but can also be driven with an output card or inverter card.

SYMBOL




-20 V
13
14
+20V
15
NOTE:
1. SILICON, 92115021.
2. COMPONENT ASSY NO. 50038600.
-20V
R04
10K
R05
33K
6
-20 V
R01
4.7K
R02
1.8K
Q01
2N3638
TP-A
1
TP-C
-20 V
R06
4.7K
CR01
12
R07
1.5K
R03
1.8K
Q02
2N3638


Q02
Q01
R07
R06
CR01
R04
R05
R01
R03
R02
CARD FNA
PIN 1

# FUNCTION GENERATORS
## FOA, FOB, FOC, FOD, FOE, FOF, FOG, FOH

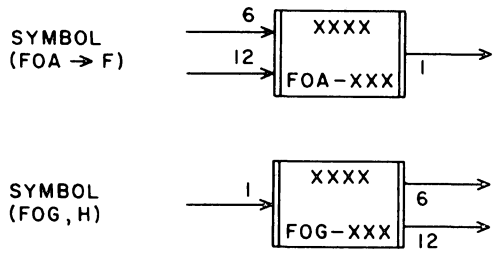
These cards are used in the disk file servo actuator in the coarse (long stroke) positioning loop to shape the gain curve. For commands requiring a large signal, the gain is reduced.

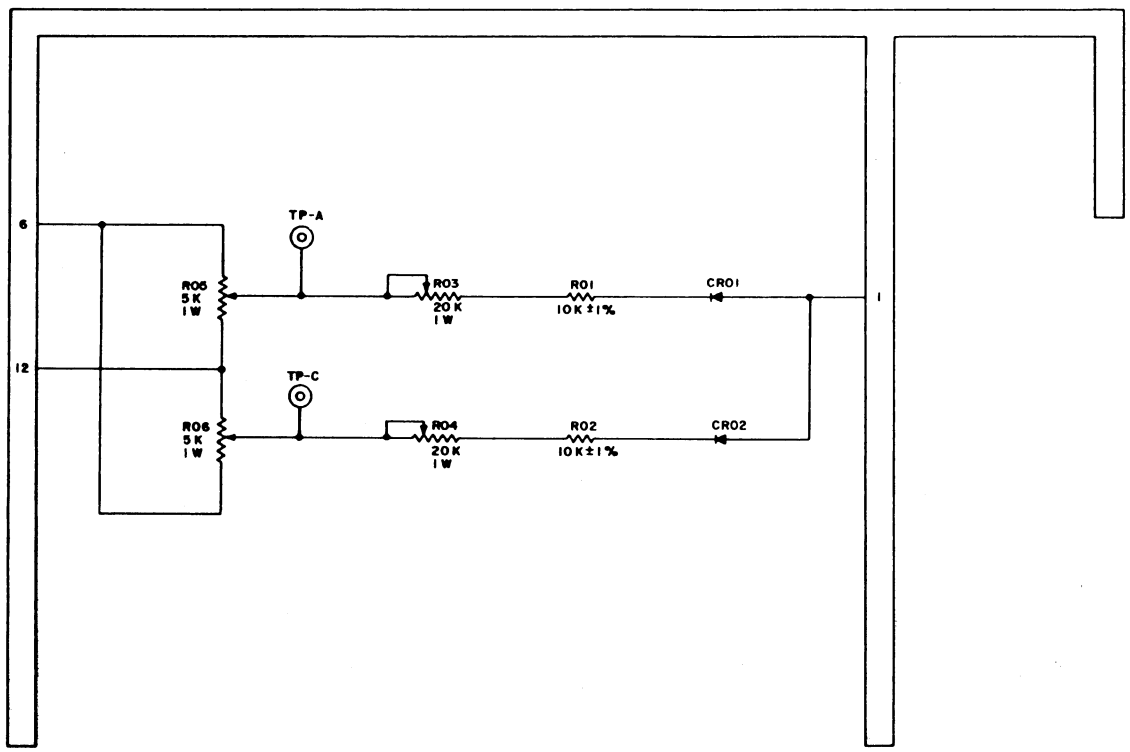
These cards are connected around an operational amplifier by connecting pin 1 to the operational amplifier summing point and pin 12 to the operational amplifier output. A floating power supply (ALA card) connects from pins 6 to 12 such that for the FOA, C, D and G cards pin 6 is positive, relative to pin 12 and for the FOB, G, E, and H cards pin 6 is negative. By adjusting potentiometers R05 and R06, the two diodes CR01 and CR02 are back biased to different levels. As the operational amplifier output swings negative, pin 6 of the FOA, C, D or G voltage lowers until it reaches ground. At this point, either or both diodes conduct, depending on the potentiometer settings since the input is at the operational amplifier summing point (virtual ground). As the diodes conduct, the gain is reduced because one or more resistors are connected in parallel with the normal feedback resistors around the operational amplifier.

The FOB, E, F, and H cards operate in a similar manner for a positive swing of the operational amplifier output.

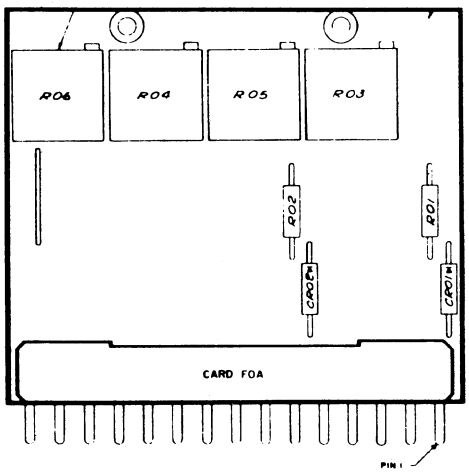
The FOC, D, E, F, G and H cards use a fixed resistor in place of the gain setting potentiometers (R03 and R04) used on the FOA and B cards. The difference between the cards is the value of the fixed resistors R01 and R02.

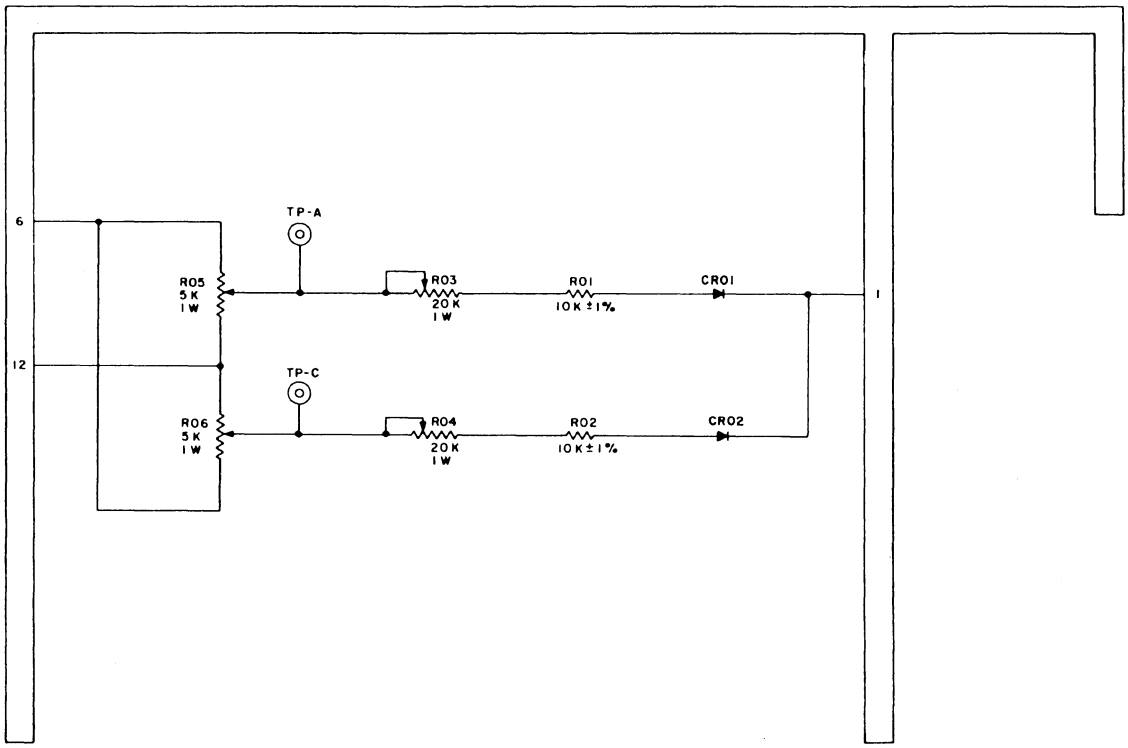
The FOG and H cards have equal values for R01 and R02. These two cards generate an approximate square root function (i.e., the output voltage is the square root of the input voltage). This is accomplished by setting the diode conduction levels (via potentiometers R03 and R04) at equal intervals.



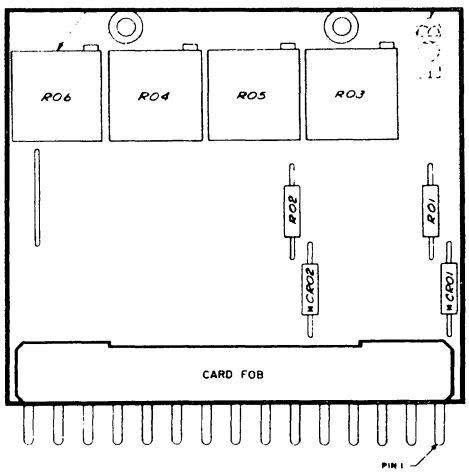

6
12
TP-A
TP-C
RO5
5K
1W
RO6
5K
1W
RO3
20K
1W
RO4
20K
1W
RO1
10K ±1%
RO2
10K ±1%
CRO1
CRO2
1

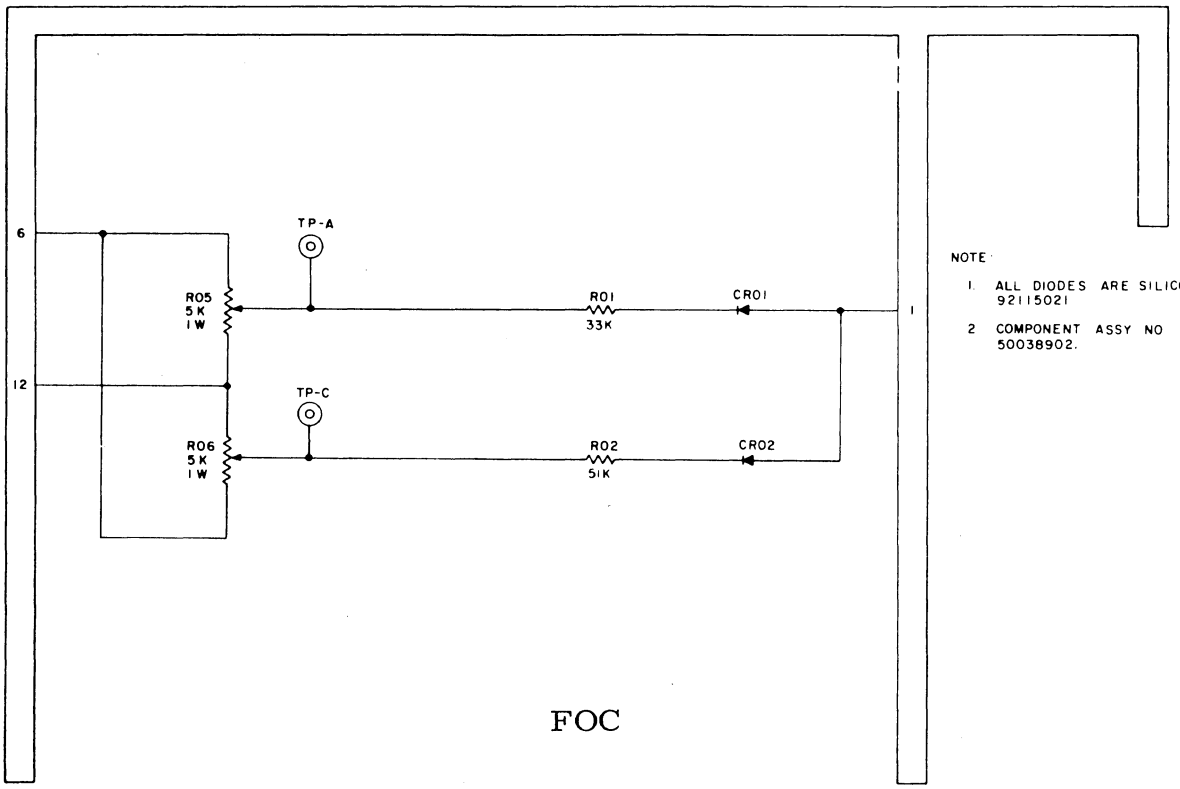
FOA


RO6
RO4
RO5
RO3
RO2
RO1
CRO2
CRO1
CARD FOA
PIN 1

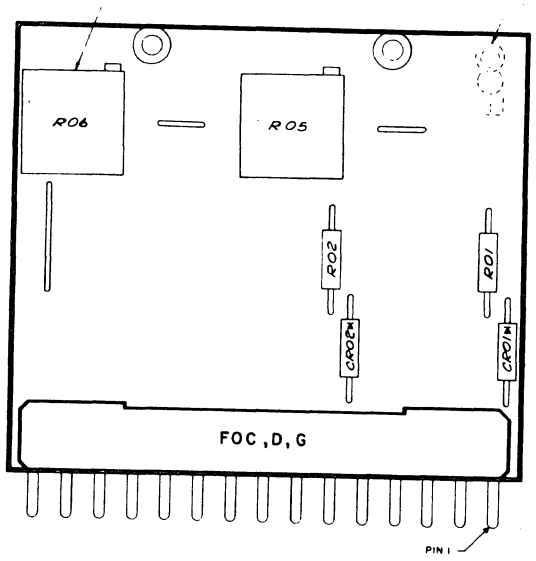

6
12
TP-A
TP-C
R05
5K
1W
R06
5K
1W
R03
20K
1W
R04
20K
1W
R01
10K ±1%
R02
10K ±1%
CR01
CR02
1

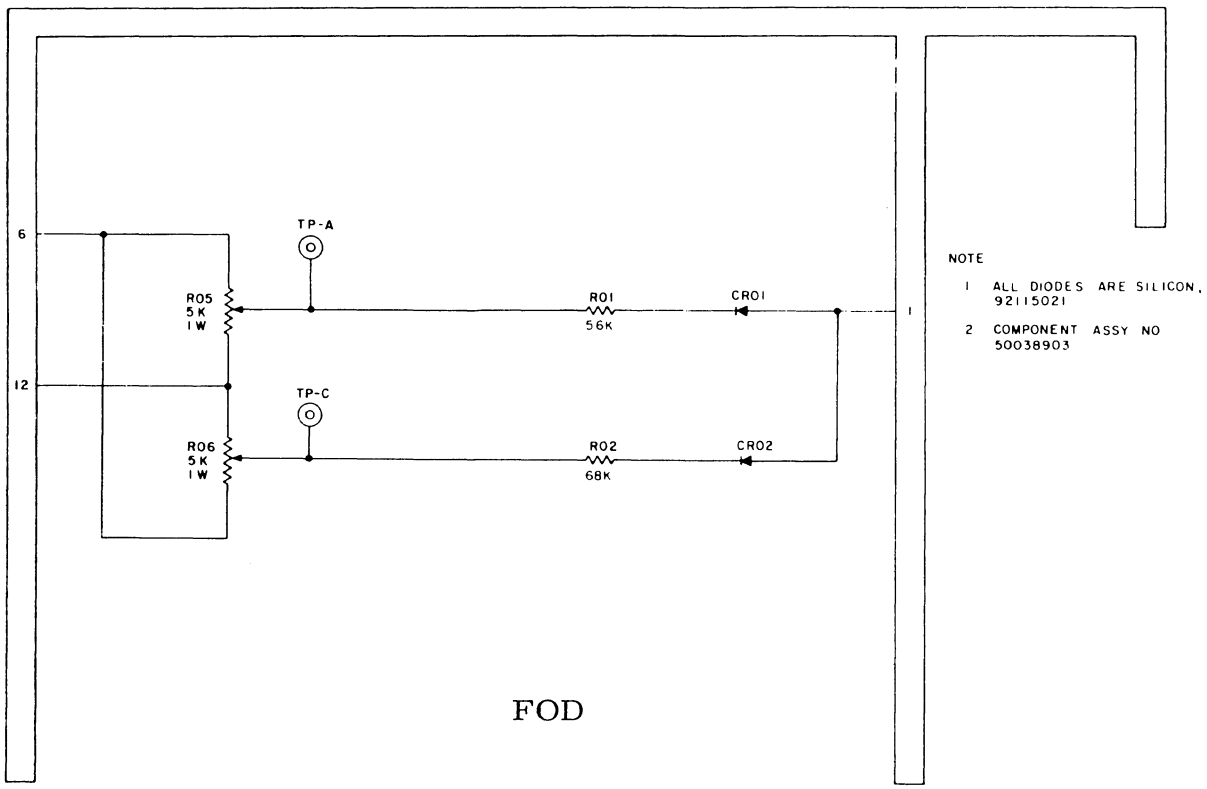
FOB


R06
R04
R05
R03
R02
R01
CR02
CR01
CARD FOB
PIN 1

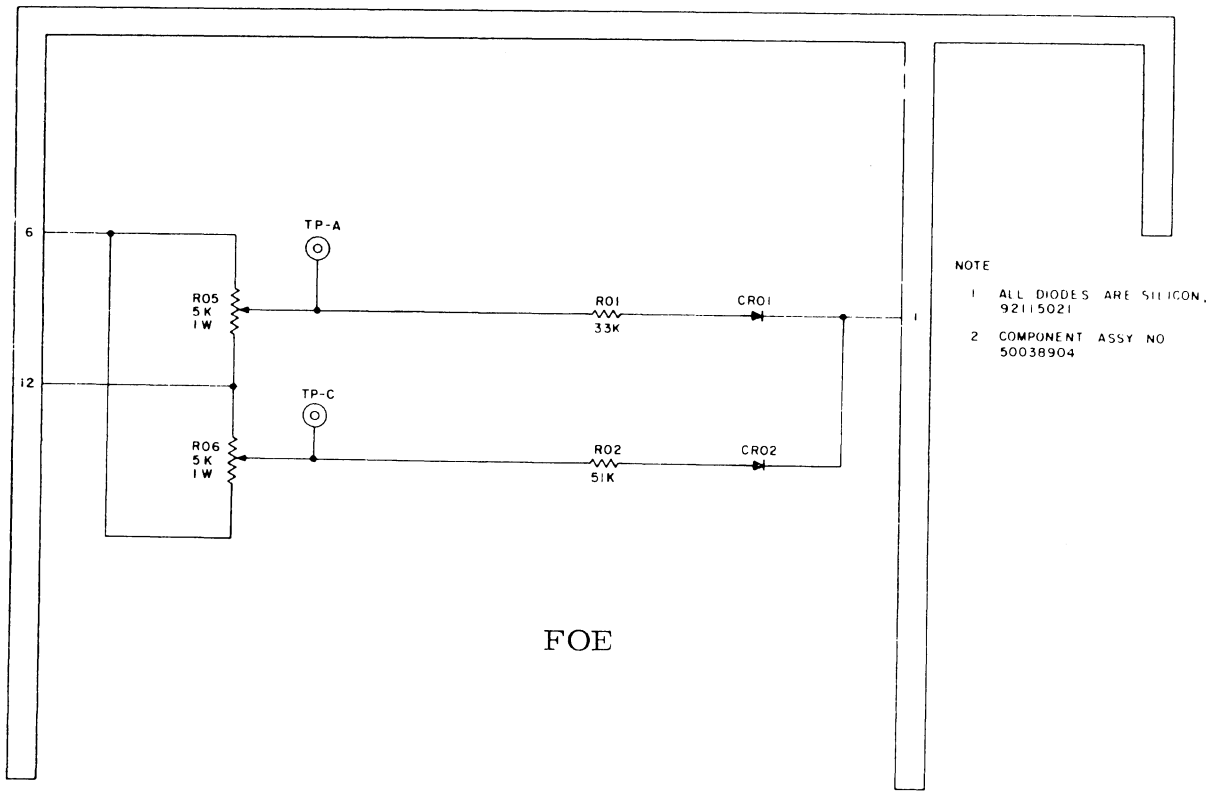

6
12
TP-A
TP-C
R05
5K
1W
R06
5K
1W
R01
33K
R02
51K
CR01
CR02
1
NOTE
1. ALL DIODES ARE SILICON, 92115021
2. COMPONENT ASSY NO 50038902.

FOC

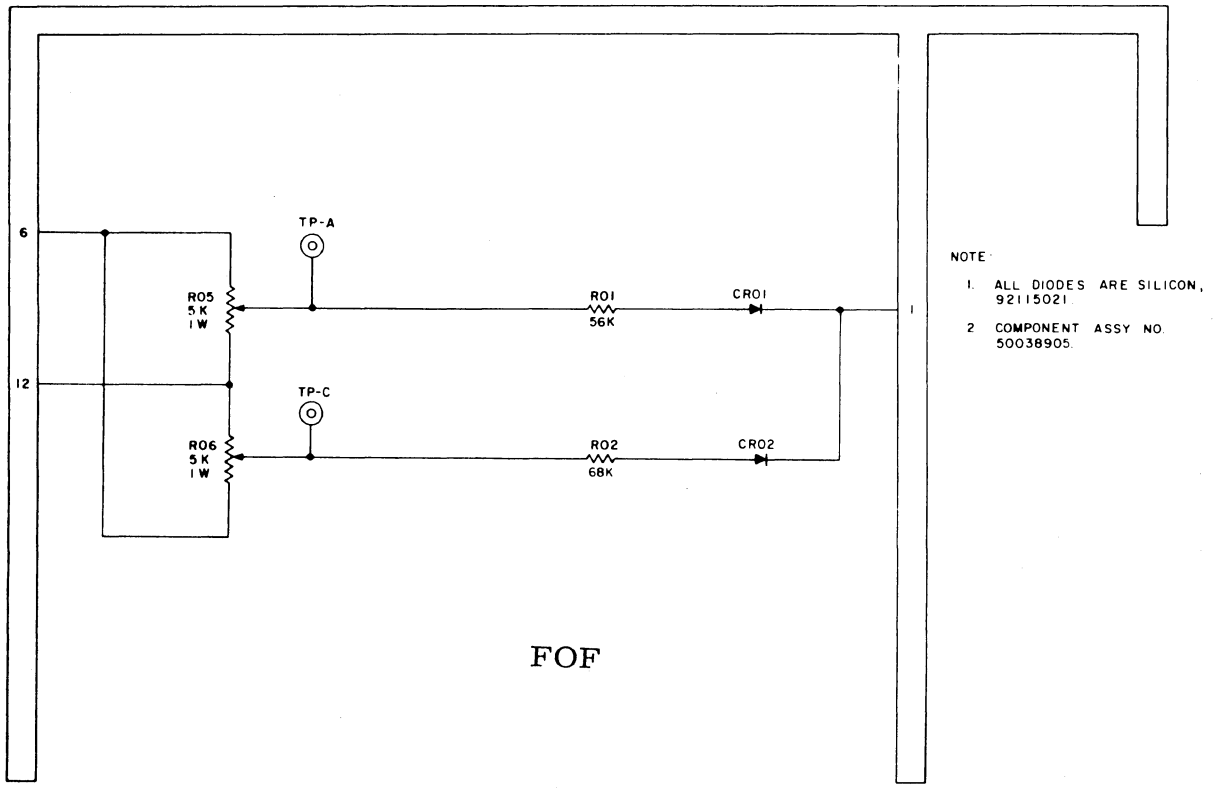

R06
R05
R02
R01
CR02
CR01
FOC,D,G
PIN 1


6
12
TP-A
TP-C
R05
5K
1W
R06
5K
1W
R01
56K
R02
68K
CR01
CR02
1
NOTE
1 ALL DIODES ARE SILICON, 92115021
2 COMPONENT ASSY NO 50038903

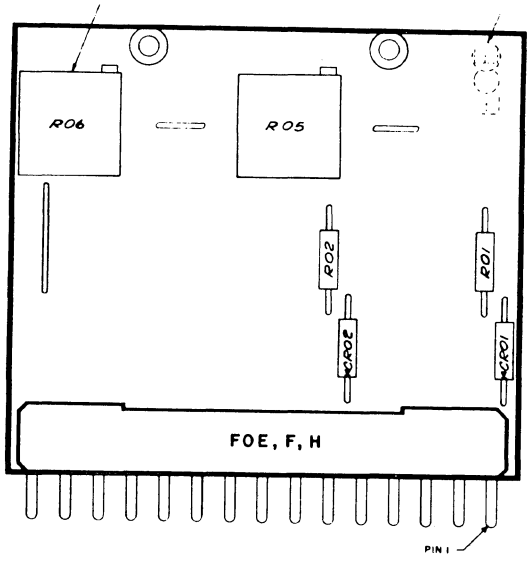
FOD

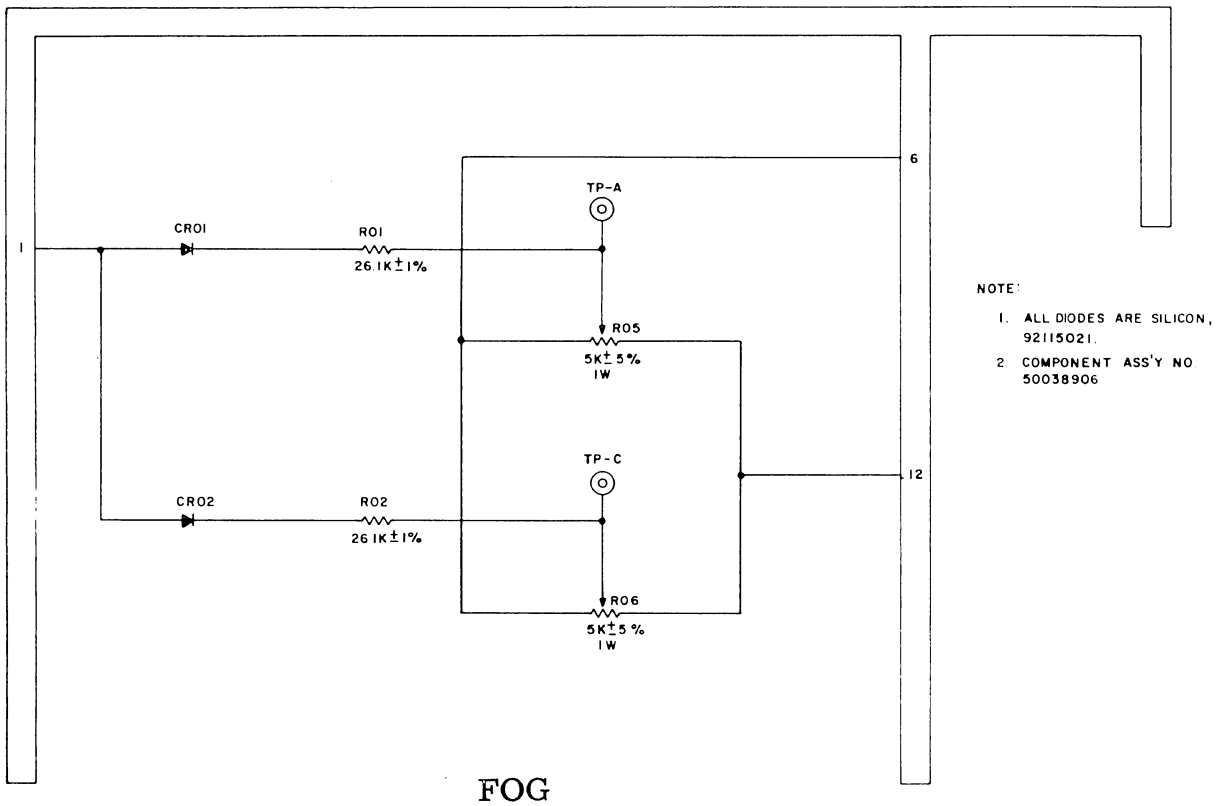

6
12
TP-A
TP-C
R05
5K
1W
R06
5K
1W
R01
33K
R02
51K
CR01
CR02
1
NOTE
1 ALL DIODES ARE SILICON, 92115021
2 COMPONENT ASSY NO 50038904

FOE

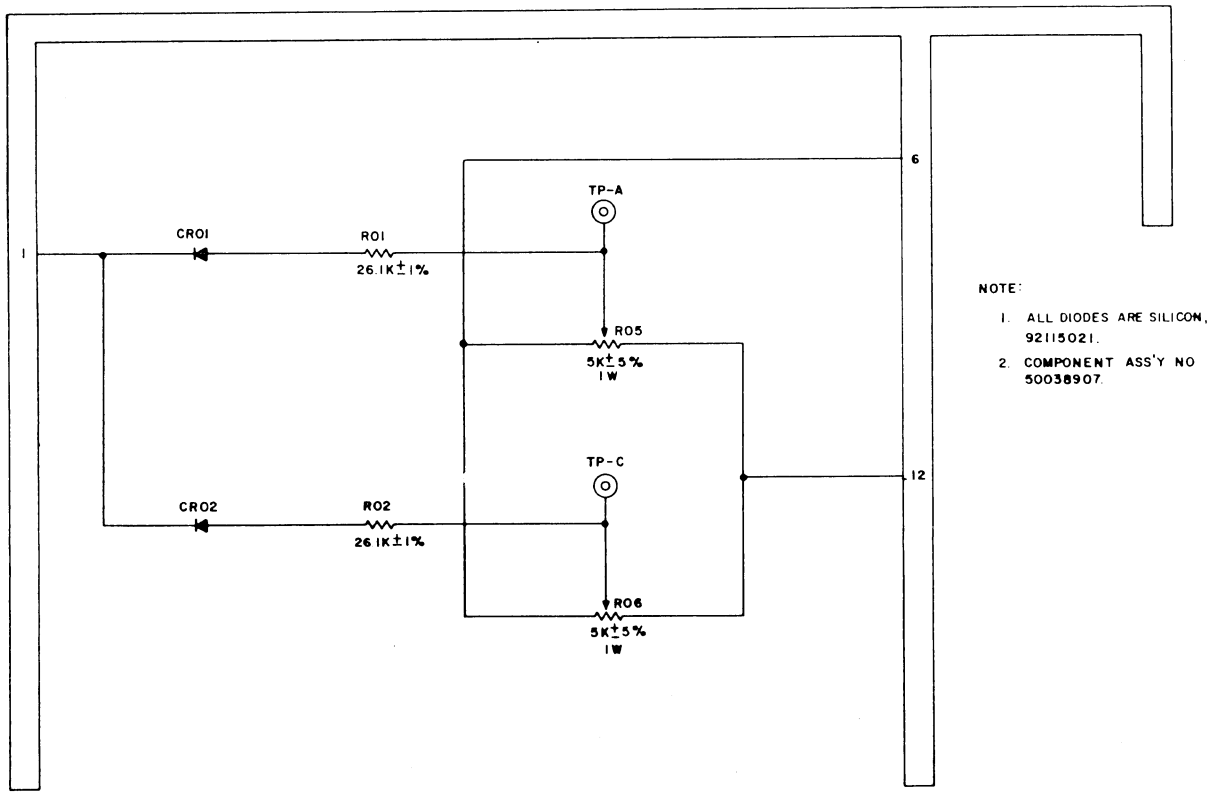

6
12
TP-A
TP-C
R05
5K
1W
R06
5K
1W
R01
56K
R02
68K
CR01
CR02
1
NOTE
1. ALL DIODES ARE SILICON, 9211502I.
2 COMPONENT ASSY NO. 50038905.

FOF


R06
R05
R02
R01
CR02
CR01
FOE, F, H
PIN 1


1
6
12
TP-A
TP-C
CR01
CR02
R01
26.1K±1%
R02
26.1K±1%
R05
5K±5%
1W
R06
5K±5%
1W
NOTE:
1. ALL DIODES ARE SILICON, 92115021.
2. COMPONENT ASS'Y NO 50038906

FOG


1
6
12
TP-A
TP-C
CR01
CR02
R01
26.1K±1%
R02
26.1K±1%
R05
5K±5%
1W
R06
5K±5%
1W
NOTE:
1. ALL DIODES ARE SILICON, 92115021.
2. COMPONENT ASS'Y NO 50038907.

FOH

# REFERENCE AMPLIFIER
## FPA

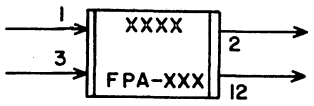
The FPA card is used in the disk file servo actuator. The circuit supplies a plus or minus 8 volt reference to the coarse positioning loop. This voltage must be stable, because it represents the coarse command to the system. The output load is approximately 10 ma maximum.

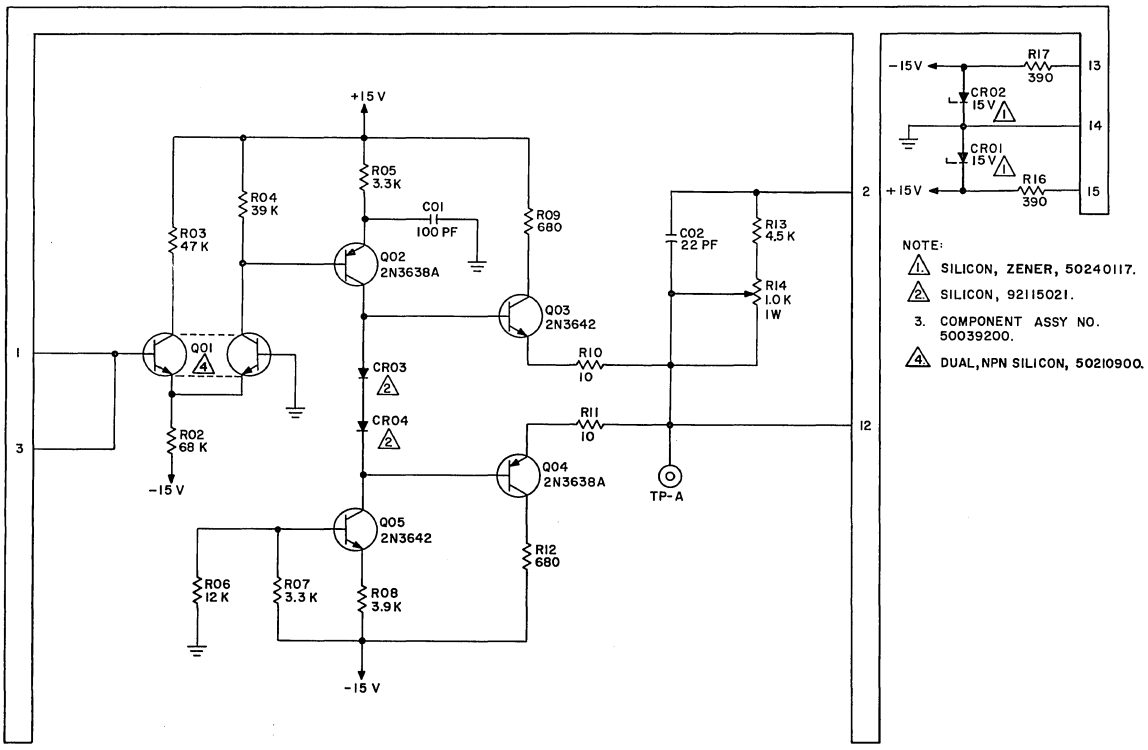
The FPA card is supplied by a FLA bridge rectifier card. Pins 1 and 2 connect with either pins 11 and 9, or 12 and 10 respectively (card FLA), for a +8v or -8v output. This combination is an operational amplifier with closed loop gain of unity, but can be varied ±10% by R14.

The first stage of the amplifier is a differential stage. This stage uses a matched pair of transistors in a single TO -5 can, for best temperature stability. Transistors Q01 and Q02 provide the necessary closed loop gain. Transistor Q05 is a constant current source to provide negative drive for Q04. The positive drive for Q03 comes from Q02. If the +8v output is desired, pin 1 is driven from the negative voltage pin (pin 11, FLA card). Pin 2 is connected to pin 9 of the FLA card. The negative voltage is used to give a positive voltage, because the circuit has negative gain. Under these conditions, Q03 supplies the load and Q04 is near cut-off.

If the output is to be -8v, pins 1 and 2 connect to pins 12 and 10 respectively (card FLA). Under these conditions, Q04 supplies the load and receives its base drive from the current source (Q05). Transistor Q03 is near cut-off.

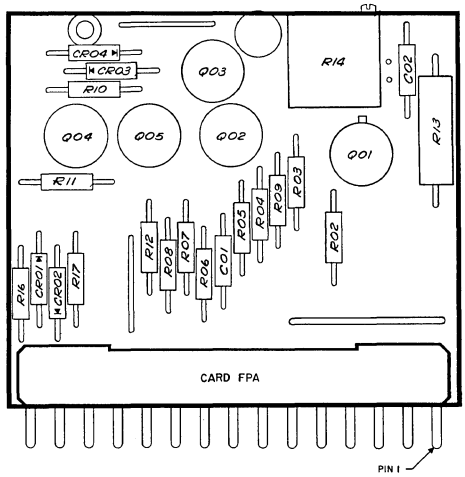
SYMBOL






NOTE:

1. SILICON, ZENER, 50240117.
2. SILICON, 92115021.
3. COMPONENT ASSY NO. 50039200.
4. DUAL, NPN SILICON, 50210900.



# VELOCITY, ACCELERATION SUMMING NETWORK
## FRA, FRB, FRC, FRD

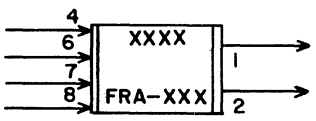
The FRA through FRD cards contain a passive circuit of resistors, capacitors, and zener diodes to be used with operational amplifiers in the disk file servo actuator.

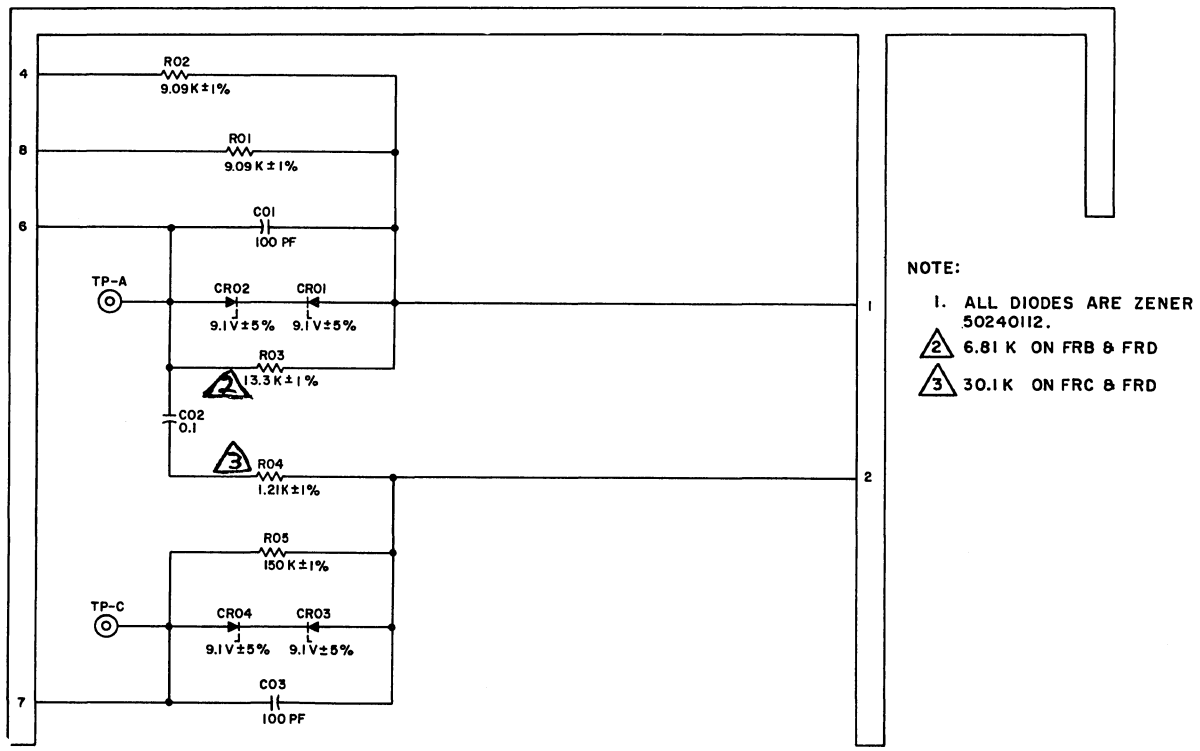
The circuit is supplied at pins 4 and 8 with voltages from velocity transducers, one end of each being grounded (the FRD is supplied from two velocity transducers). An operational amplifier connects between pins 1 and 6 (input at 1), giving an output proportional to the sum of the velocity signals at pin 6.

Zener diodes CR01 and CR02 limit the output voltage of the amplifier to about ±10 volts peak. Capacitor C01 provides high frequency cutoff at approximately 120KC.

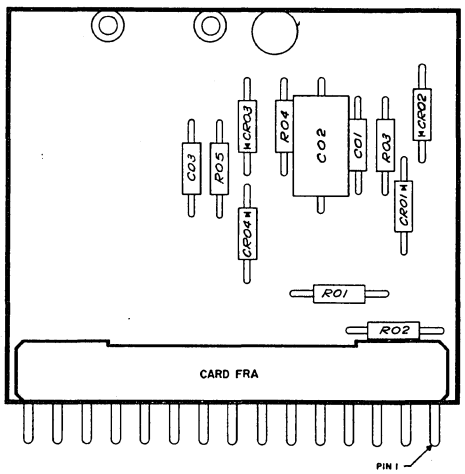
Another operational amplifier connects between pins 2 and 7 (input at 2). With the velocity signal at pin 6 also being applied to the differentiating network (C02 and R04), the output at pin 7 becomes a signal proportional to acceleration for frequencies below 13KC (50 CPS for FRC & D). Beyond 13KC (50 CPS for FRC & D) the gain levels off so the output is somewhat proportional to velocity. The useful range of frequencies for the system however is below 300 cycles. Capacitor C03 provides for frequency cutoff at approximately 16KC, and the zener diodes limit the output swing to approximately ±10 volts peak.

SYMBOL




R02
9.09K±1%
R01
9.09K±1%
C01
100 PF
TP-A
CR02
CR01
9.1V±5%
9.1V±5%
R03
13.3K±1%
C02
0.1
R04
1.21K±1%
R05
150K±1%
TP-C
CR04
CR03
9.1V±5%
9.1V±5%
C03
100 PF
4
8
6
7
1
2
NOTE:
1. ALL DIODES ARE ZENER 50240112.
2 6.81 K ON FRB & FRD
3 30.1 K ON FRC & FRD

FRA


C03
R05
CR03
CR04
R04
C02
C01
R03
CR01
CR02
R01
R02
CARD FRA
PIN 1

# OPERATIONAL AMPLIFIER

## FSA, FSB

The FSA card contains the operational amplifier used as the main building block in the disk file servo actuator.

This card has on it the purchased modular amplifier, plus the discrete component power booster. The input to the amplifier is of a differential nature, but as used in the servo, one side (pin 5) is grounded. Pin 1 is driven and the inverted output is taken from pin 7. The amplifier cannot be used by itself in an open loop manner because the output drifts between + and -15 volts. Normally one of the feedback network cards is used (FRA, FTA, FUA, or FVA) around the amplifier between pins 1 and 7 to close the feedback loop. The output is then near zero and can be set there by the adjustment pot on the module (assuming the input resistor is grounded on the end opposite pin 1).

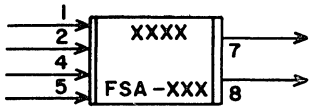
The booster stage is a complimentary emitter follower Q01 and Q03 operating approximately class AB. A constant current source is used to get positive drive for Q03. This is basically the same circuit as used on the FPA and FMA cards and discussed under FHA or FIA. The load on this card can be approximately $\pm$ 10V peak into 500 ohms.

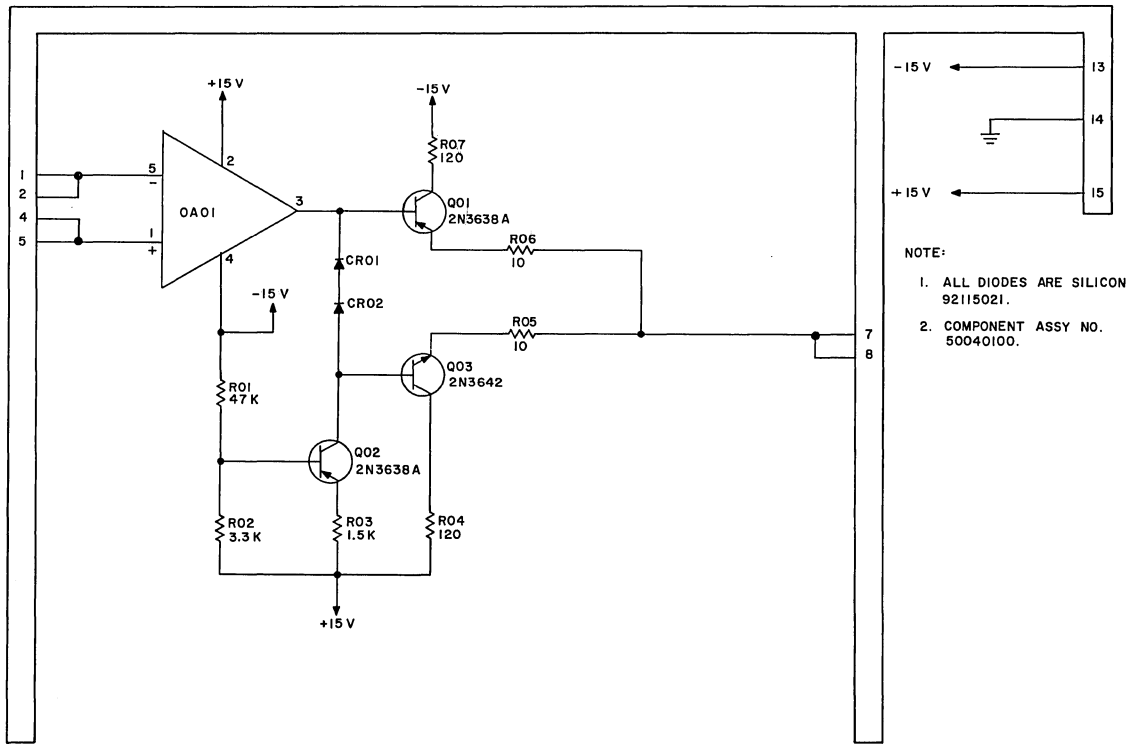
The above discussion also applies to the FSB card.

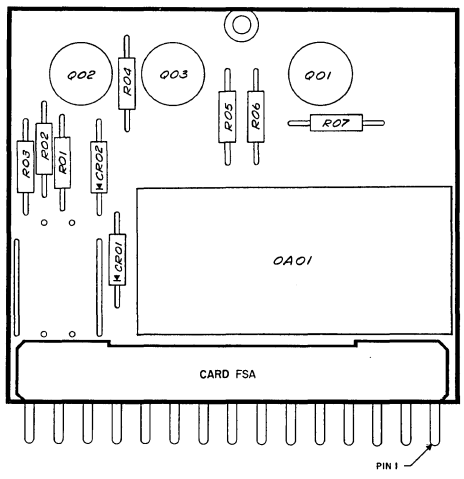
The FSB card uses a purchased op. amp. module plus the discrete component power booster. In addition, a + and -15 volt regulated power supply has been incorporated on the card. A balance pot was added to the card because the less expensive op. amp. module did not contain this balance adjustment.

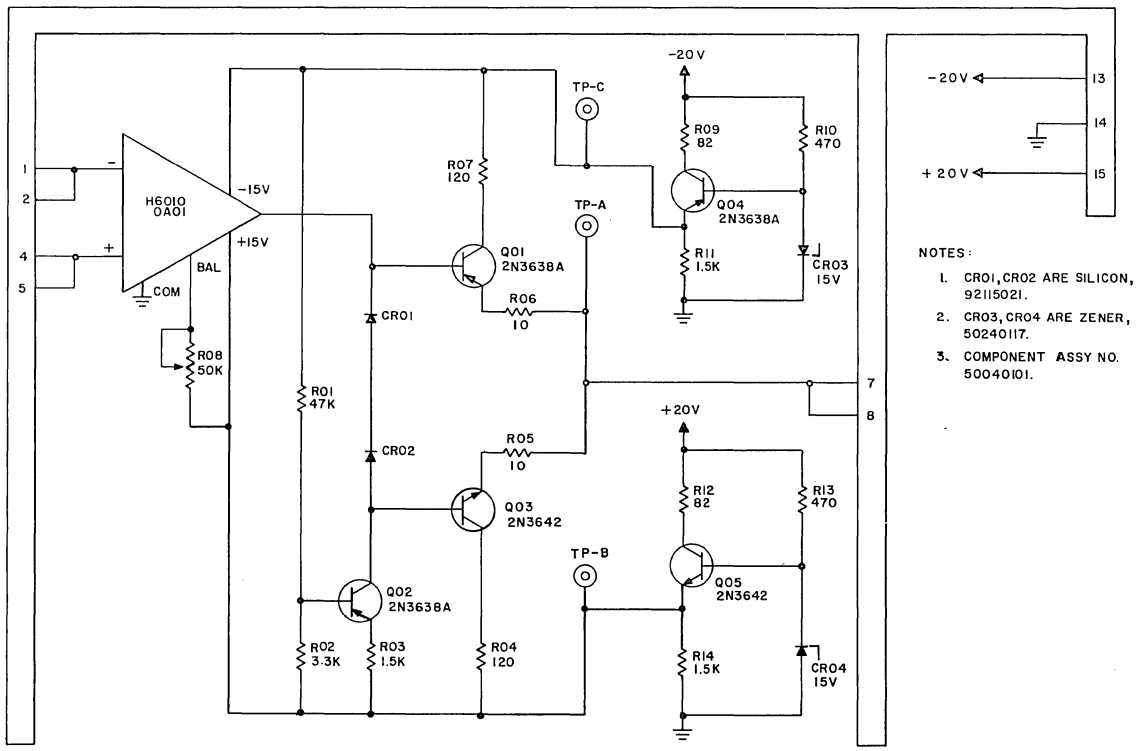
Caution: The FSA card requires three card slots. The FSB card requires two card slots.

SYMBOL

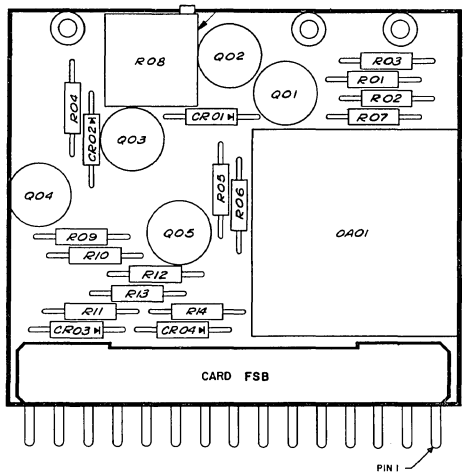



+15 V
-15 V
R07
120
Q01
2N3638A
R06
10
CR01
CR02
R05
10
Q03
2N3642
R01
47K
Q02
2N3638A
R02
3.3K
R03
1.5K
R04
120
OA01
+15 V
-15 V
13
14
15
7
8
1
2
4
5
NOTE:
1. ALL DIODES ARE SILICON, 92115021.
2. COMPONENT ASSY NO. 50040100.


Q02
R04
Q03
R05
R06
Q01
R07
R03
R02
R01
CR02
CR01
OA01
CARD FSA
PIN 1


-20V
TP-C
R09
82
R10
470
R07
120
Q04
2N3638A
TP-A
H6010
0A01
-15V
+15V
Q01
2N3638A
R11
1.5K
CR03
15V
BAL
COM
CR01
R06
10
R08
50K
R01
47K
7
8
+20V
CR02
R05
10
R12
82
R13
470
Q03
2N3642
TP-B
Q05
2N3642
Q02
2N3638A
R02
3.3K
R03
1.5K
R04
120
R14
1.5K
CR04
15V
-20V
+20V
13
14
15
NOTES:
1. CR01, CR02 ARE SILICON, 92115021.
2. CR03, CR04 ARE ZENER, 50240117.
3. COMPONENT ASSY NO. 50040101.

FSB


R08
Q02
Q01
R03
R01
R02
R07
R04
CR02
CR01
Q03
Q04
R05
R06
Q05
0A01
R09
R10
R12
R13
R11
R14
CR03
CR04
CARD FSB
PIN 1

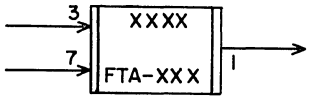
VELOCITY SUMMING NETWORK

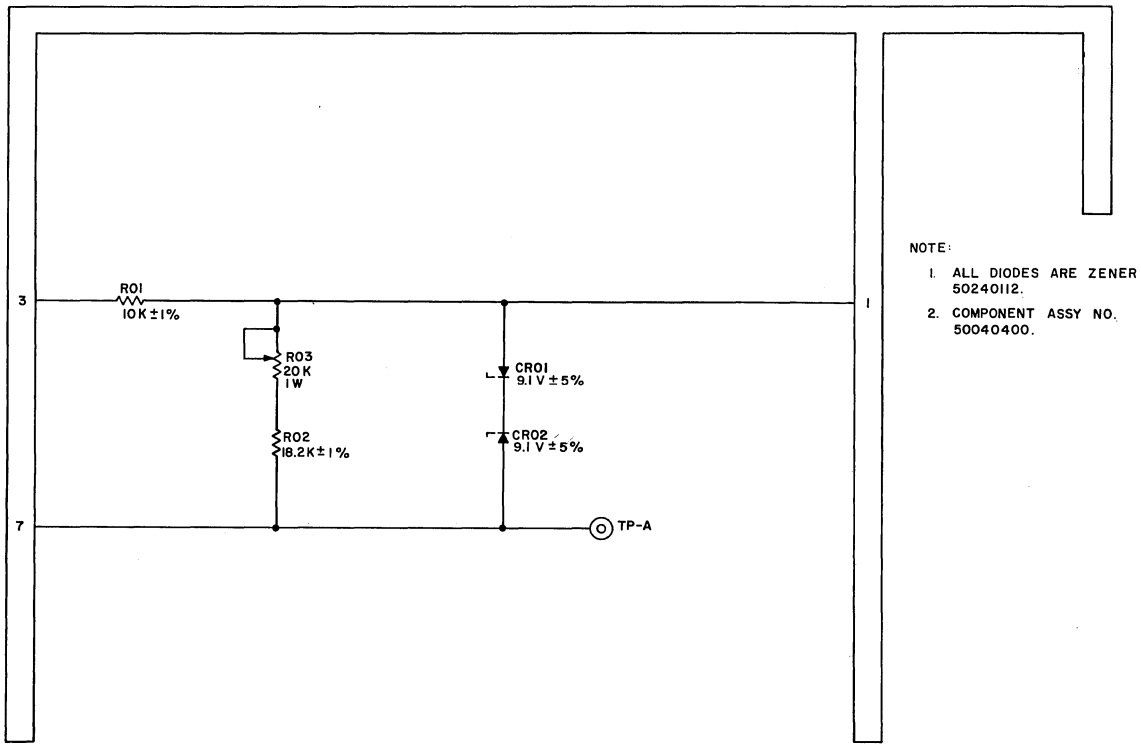
FTA

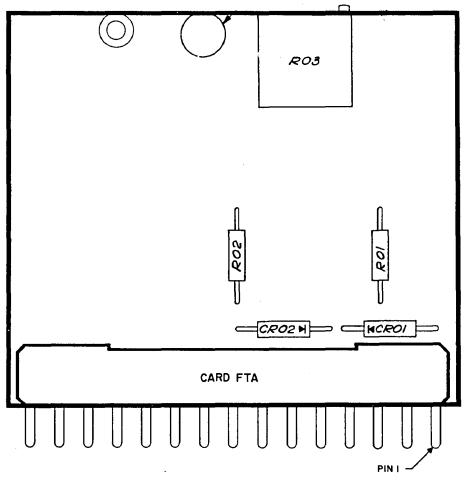
This card is used in the disk file servo actuator as a feedback network for an operational amplifier.

The circuit is supplied with a velocity signal, which is applied at pin 3. An operational amplifier is connected from pins 1 to 7, with the input at pin 1. The closed loop gain is given by the ratio of R02 plus R03 to R01. This is adjustable from 1 to 2. The output is a velocity signal with a phase inversion. Zener diodes CR01 and CR02 limit the output voltage to ±10v peak.

SYMBOL




3
7
1
R01
10K ±1%
R03
20K
1W
R02
18.2K ±1%
CR01
9.1 V ±5%
CR02
9.1 V ±5%
TP-A
NOTE:
1. ALL DIODES ARE ZENER 50240112.
2. COMPONENT ASSY NO. 50040400.


R03
R02
R01
CR02
CR01
CARD FTA
PIN 1

SUMMING NETWORK A,V,X
FUA, FUB

This passive feedback network is used in the disk file servo actuator in conjunction with three operational amplifiers. One amplifier sums acceleration (A), velocity (V), and fine position (X) signals. This signal becomes the control signal for the accurate positioning of the magnetic recording heads in the file. A second amplifier is used for amplifying the fine positioning (short stroke) signal. The third amplifier is used for the generation of an on point signal which tells the computer with the disk file that the servo is at the proper location.

The short stroke amplifier connects between pins 1 and 7 with 1 to the input. The closed loop gain of 3.25 is given by R01 divided by the demodulation output impedance of 5K.

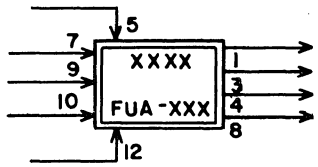
An on point amplifier connects between 8 and 9 with 8 being the input. This has a closed loop gain given by R07 over R08 which is 1.82.

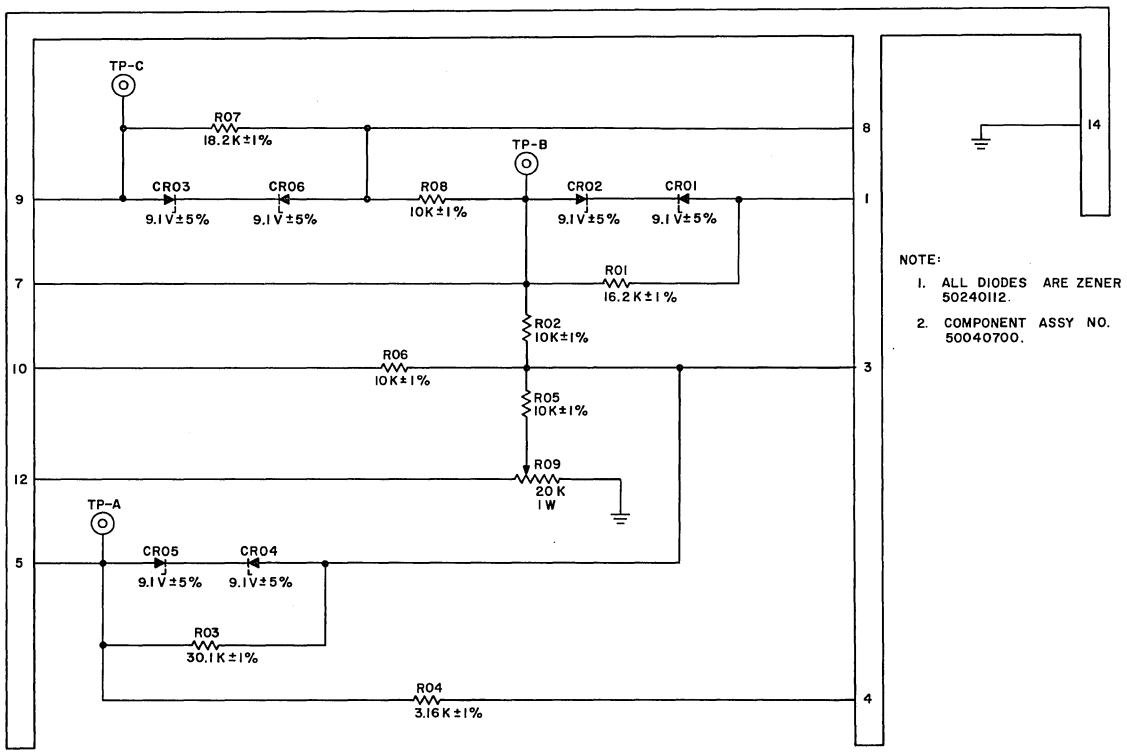
A summing amplifier connects between 3 and 5 with 3 being the input. The acceleration signal connects to pin 12, the velocity signal goes to pin 10, and the short stroke displacement is at pin 7. Adjustment of pot R09 adjusts the gain for the acceleration signal. Resistor R03 divided by R02, R05 or R06 give a closed loop gain of 3.01. The FUB card uses another pot R10 to adjust the servo loop gain to compensate for hydraulic servo valve variations.

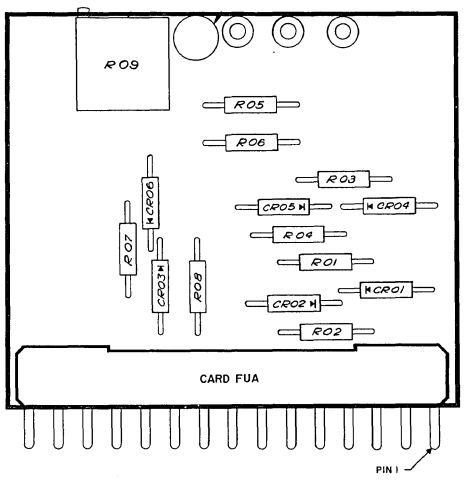
Resistor R04 is part of the input resistor for the short stroke valve amplifier (FHA).

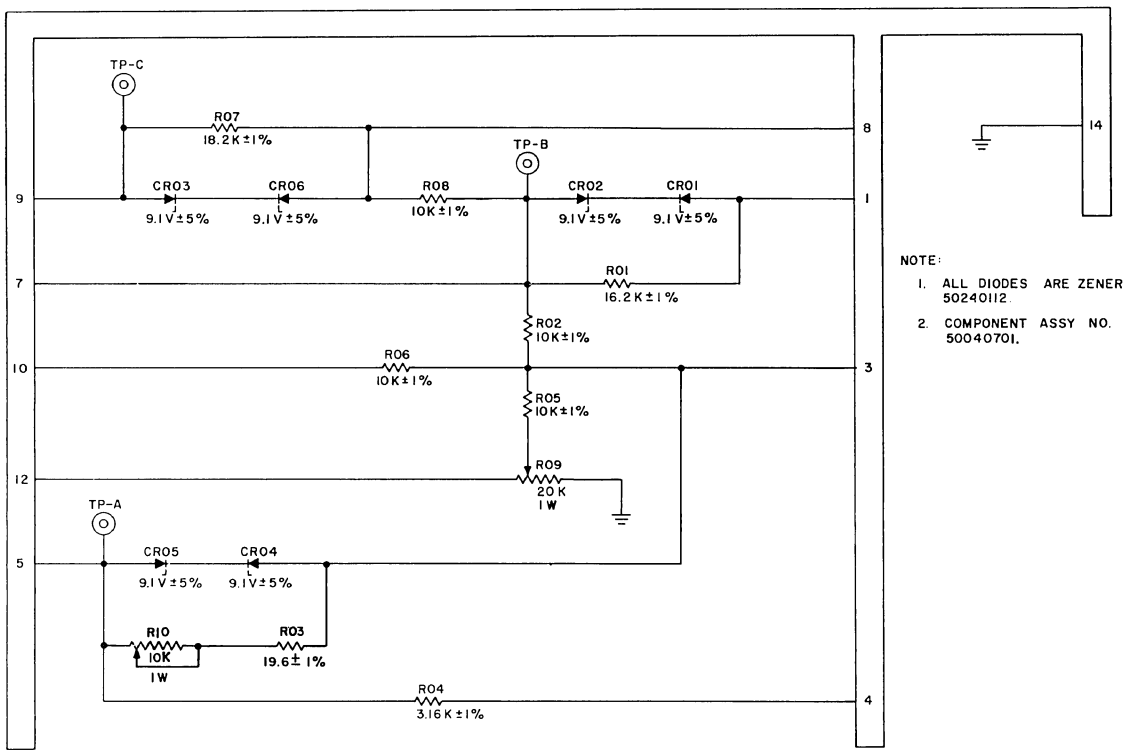
The zener diodes CR01 through CR06 limit the amplifier output voltage to ± 10V peak.

SYMBOL

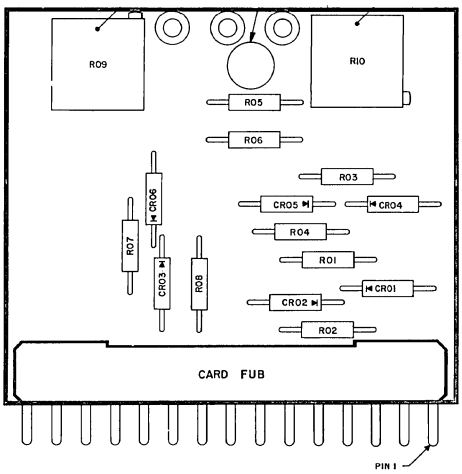



TP-C
R07
18.2K±1%
TP-B
CR03
9.1V±5%
CR06
9.1V±5%
R08
10K±1%
CR02
9.1V±5%
CR01
9.1V±5%
R01
16.2K±1%
R02
10K±1%
R06
10K±1%
R05
10K±1%
R09
20K
1W
TP-A
CR05
9.1V±5%
CR04
9.1V±5%
R03
30.1K±1%
R04
3.16K±1%
8
14
9
1
7
10
3
12
5
4
NOTE:
1. ALL DIODES ARE ZENER 50240112.
2. COMPONENT ASSY NO. 50040700.


R09
R05
R06
R03
CR05
CR04
R04
R01
CR01
CR02
R02
R07
CR06
CR03
R08
CARD FUA
PIN 1


TP-C
R07
18.2K±1%
TP-B
CR03
9.1V±5%
CR06
9.1V±5%
R08
10K±1%
CR02
9.1V±5%
CR01
9.1V±5%
R01
16.2K±1%
R02
10K±1%
R06
10K±1%
R05
10K±1%
R09
20K
1W
TP-A
CR05
9.1V±5%
CR04
9.1V±5%
R10
10K
1W
R03
19.6±1%
R04
3.16K±1%
8
14
9
1
7
10
3
12
5
4
NOTE:
1. ALL DIODES ARE ZENER 50240112.
2. COMPONENT ASSY NO. 50040701.

FUB


R09
R10
R05
R06
R03
CR05
CR04
R04
R01
CR01
CR02
R02
R07
CR06
CR03
R08
CARD FUB
PIN 1

# POSITION AND ACCELERATION NETWORK
## FVA, FVB

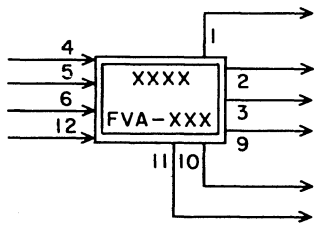
The FVA and FVB passive networks are used with three operational amplifiers in the disk file servo actuator. The circuit forms the coarse control signal from the position (long stroke) and acceleration signals in the disk files.

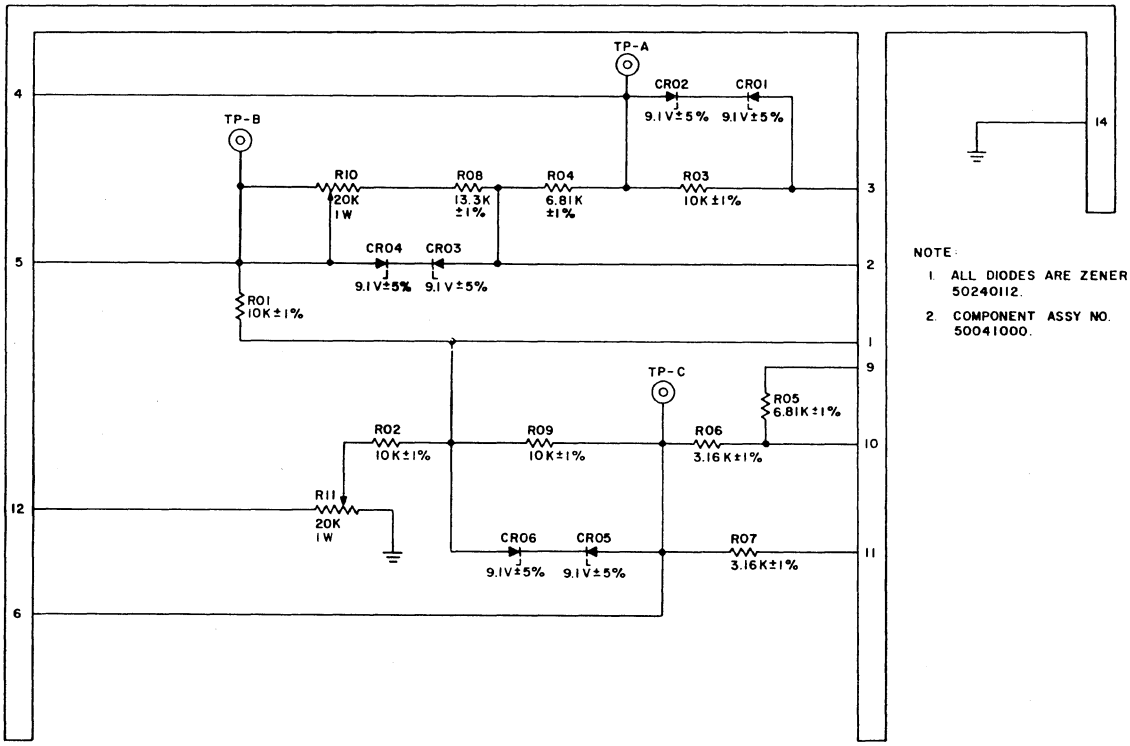
The operational amplifiers connect between pins 1 and 6, 2 and 5, and 3 and 4 (inputs at pins 1, 2, and 3). The long stroke signal enters pin 3 and is amplified with a gain of 2 (given by the ratio of R03 and the demodulator output impedance of 5 K). This is again amplified via pins 2 and 5, which use the function generator cards FOA and FOB (FOG and FOH for the FVB) to shape the gain curve. The low signal gain is adjustable between 1.95 and 4.9, as given by the ratio of R08 plus R10 to R04.

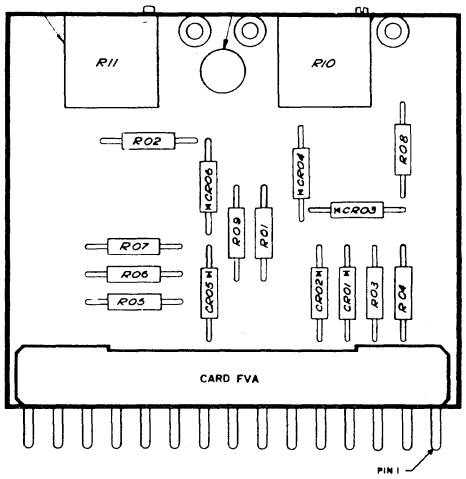
An acceleration signal is applied at pin 12 and is summed with the long stroke signal in the operational amplifier between pins 1 and 6. The acceleration gain can be adjusted by potentiometer R11. The output signal on pin 6 is applied to the short and long stroke valves via resistors R05, R06, and R07. (R07 is not used in the FVB).

The zener diodes limit the output swing of the operational amplifiers to ±10v peak.

SYMBOL




TP-A
TP-B
TP-C
CR02
CR01
9.1V±5%
9.1V±5%
R10
20K
1W
R08
13.3K
±1%
R04
6.81K
±1%
R03
10K±1%
CR04
CR03
9.1V±5%
9.1V±5%
R01
10K±1%
R05
6.81K±1%
R02
10K±1%
R09
10K±1%
R06
3.16K±1%
R11
20K
1W
CR06
CR05
9.1V±5%
9.1V±5%
R07
3.16K±1%
1
2
3
4
5
6
9
10
11
12
14
NOTE:
1. ALL DIODES ARE ZENER 50240112.
2. COMPONENT ASSY NO. 50041000.


R11
R10
R02
R08
CR06
CR04
R09
R01
R07
R06
R05
CR05
CR02
CR01
R03
R04
CARD FVA
PIN 1

# TEMPERATURE SERVO AMPLIFIER
## FWA

A temperature servo controls the air temperature in the vicinity of the disks in the disk file. The servo consists of the FWA amplifier, a thermistor bridge, and a shaded pole motor.

The thermistor connects between pins 1 and ground. Motor shading coils, used to reverse the motor, are connected to pins 11 and 12 via the limit switches (S01 and S02) on the motor assembly. The coil end labeled CW goes to the normally closed contact on S01, and from S01 common to pin 12. The coil end labeled CCW goes to the normally closed contact on S02, and from S02 common to pin 11.

At the operating temperature of 92°F, the thermistor bridge consisting of the thermistor, R01, R03, R04, R05, R06, and CR01 is balanced, and no signal is applied to the differential amplifier (Q01 and Q02). Therefore, the output transistors (Q05 and Q06) are off, so no unbalance exists in the motor shading coil currents. The motor will be off, allowing the proper flow of air to the disks.

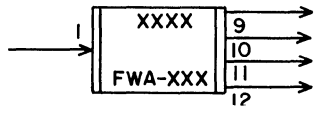
If the temperature increases, an unbalance will exist which drives Q02 base positive and Q01 base negative. The collector of Q02 goes negative and the collector of Q01 goes positive. Normally, transistors Q03 and Q04 are biased, so their collectors are at approximately zero to keep Q05 and Q06 off. Since the collector of Q02 is going negative, Q04 will be driven on so its collector goes positive and turns on Q06. The collector of Q01 is positive going, so Q03 turns further off driving Q05 further off.

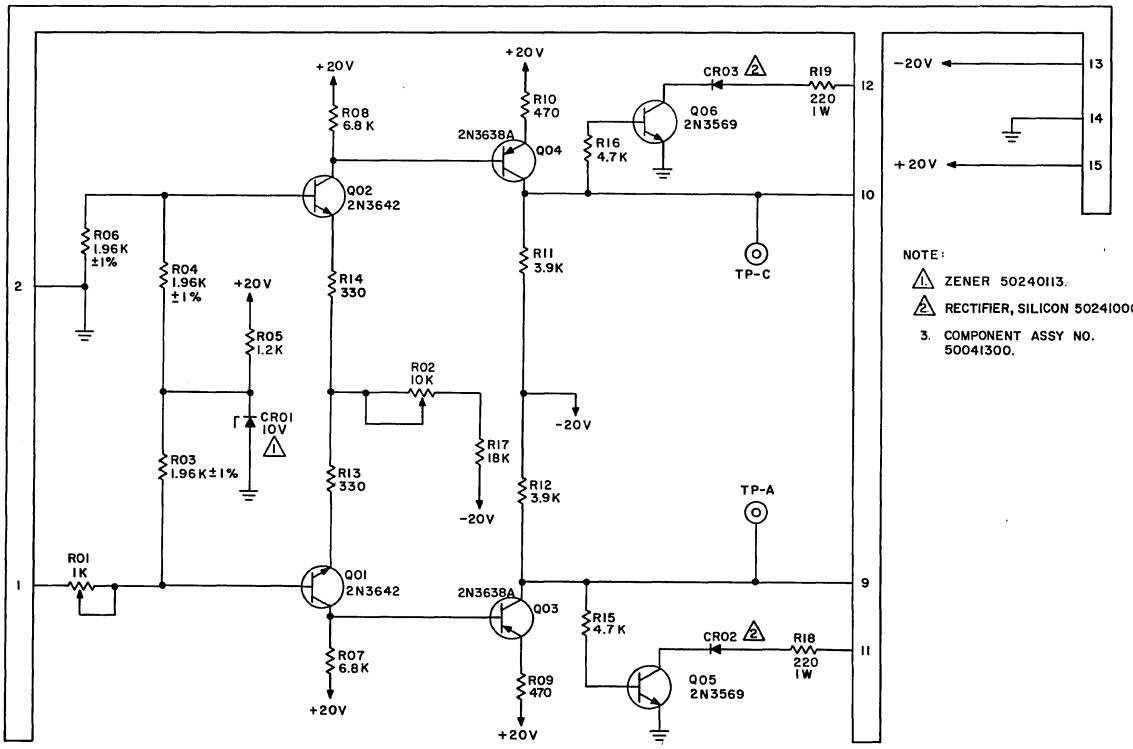
The amount Q06 turns on is proportional to the temperature change. Therefore, the motor will run at a speed proportional to the temperature difference, and in the direction that increases the air flow. This will allow the file and thermistor to cool. When a balance is again achieved, the motor will stop.

For temperatures below the control point, Q03 and Q05 turn on and reverse motor operation occurs. Air flow is reduced until the temperature rises.

A zero set condition at the desired quiescent temperature is setup by adjustment of the bridge potentiometer (R01), and the differential amplifier potentiometer (R02).

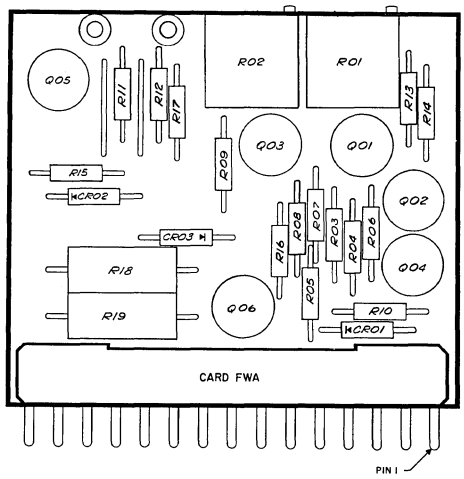
SYMBOL




NOTE:

1. ZENER 50240113.
2. RECTIFIER, SILICON 50241000.
3. COMPONENT ASSY NO. 50041300.



# TEMPERATURE SENSING AMPLIFIER
## FWB

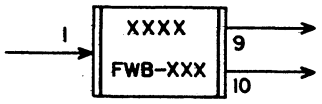
The FWB is used to sense the temperature in the vicinity of the disks in the disk file.

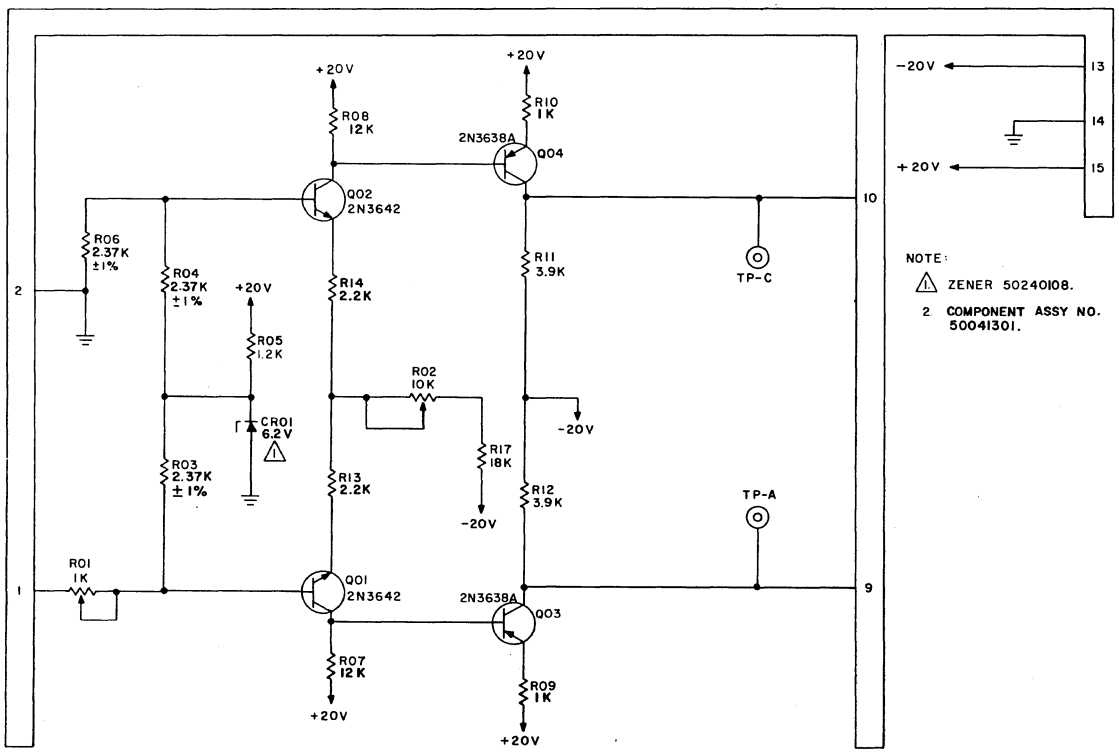
A bridge consisting of a thermistor and R01, R03, R04, and R06 is balanced near 75°F by adjusting R01. At temperatures above and below 75°F the thermistor unbalances the bridge. The unbalance in voltage is amplified by the differential amplifier consisting of Q01, Q02, Q03, and Q04.

Outputs of the amplifier are pins 9 and 10. When the temperature goes higher than 75°F (resistance of thermistor decreases), pin 9 goes negative and pin 10 goes positive. When the temperature goes lower than 75°F (resistance of thermistor increases), pin 9 goes positive and pin 10 goes negative.

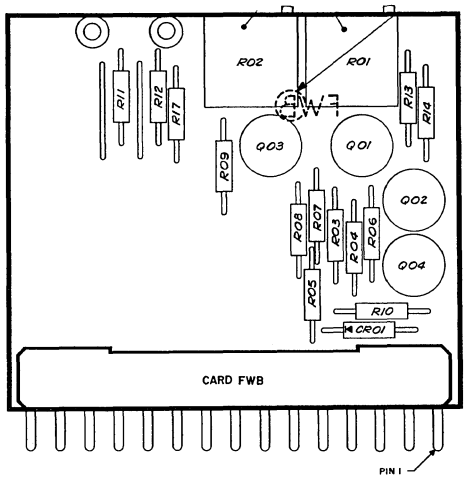
Potentiometer R02 is used to set the bias level of the outputs positive or negative.

SYMBOL




+20V
R08
12K
Q02
2N3638
R06
2.37K
±1%
R04
2.37K
±1%
+20V
R05
1.2K
CR01
6.2V
R03
2.37K
±1%
R01
1K
Q01
2N3638
R07
12K
+20V
R14
2.2K
R13
2.2K
R02
10K
R17
18K
-20V
+20V
R10
1K
2N3638A
Q04
R11
3.9K
R12
3.9K
-20V
2N3638A
Q03
R09
1K
+20V
TP-C
TP-A
10
9
2
1
-20V
13
14
+20V
15
NOTE:
1 ZENER 50240108.
2 COMPONENT ASSY NO. 50041301.

FWB


R02
R01
R11
R12
R17
R13
R14
Q03
Q01
R09
Q02
R08
R07
R03
R04
R06
Q04
R05
R10
CR01
CARD FWB
PIN 1

# GATED AMPLIFIER
# FXB, FXC

## FXB

This card is similar to the ATA card. The differences are:

1. Jumpers can short out diodes CR03 and CR04.
2. Feedback capacitors C09 and C10 were added to decrease high-frequency gain.
3. Gain adjusting potentiometer R23 was removed.
4. R-C filters were added, so that the card operates off standard machine power supplies.
5. A fixed resistor R23 was added, so that the card could be set up to have the gate open permanently to read timing tracks.
6. Coupling capacitors were chosen for the particular applications (807/8 Disc File).

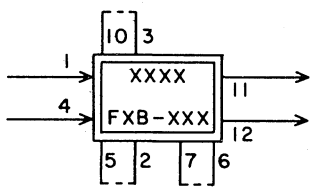
Backpass is from 30 Kc to 2Mc.

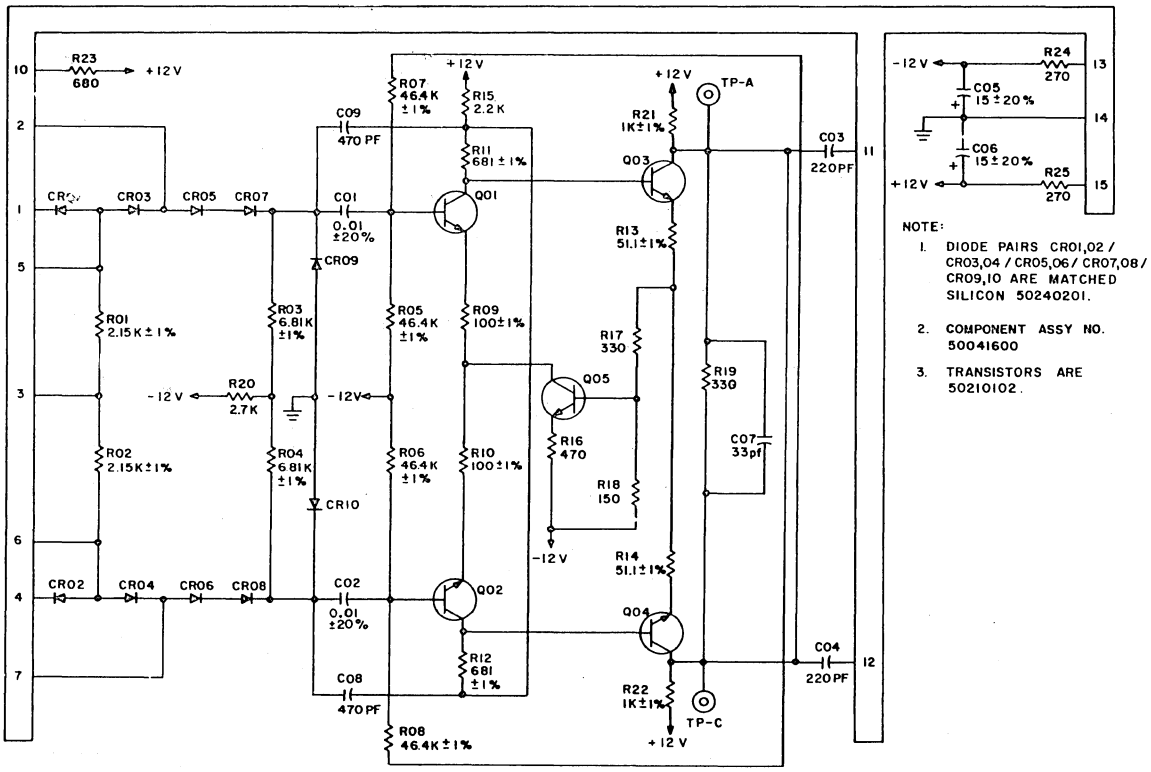
If pin 3 is at +5v or more positive, this card amplifies a signal put in on pins 1 and 4 from a center-tapped to ground read head. Pin 3 can be held positive by jumpering to pin 10.

## FXC

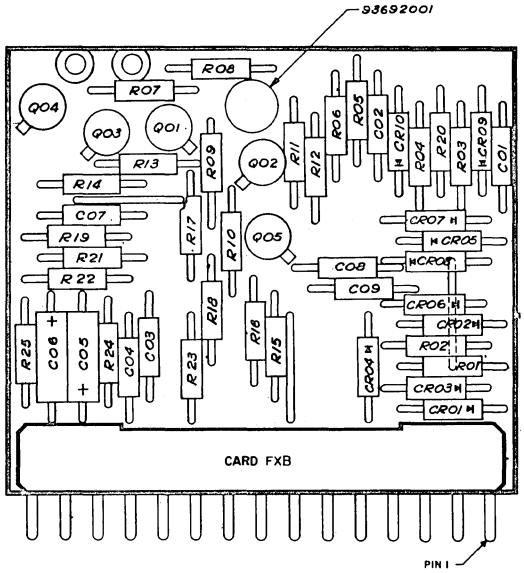
The only difference between the two cards are the condensers C01, C02, and C09, C10. On the FXC card C01 and C02 are 0.001 and C09 and C10 are not used.

SYMBOL




R23
680
+12V
R07
46.4K
±1%
R15
2.2K
C09
470 PF
R11
681 ±1%
Q01
C01
0.01
±20%
CR09
R01
2.15K±1%
R03
6.81K
±1%
R05
46.4K
±1%
R09
100±1%
R20
2.7K
-12V
R02
2.15K±1%
R04
6.81K
±1%
R06
46.4K
±1%
R10
100±1%
CR10
CR02
CR04
CR06
CR08
C02
0.01
±20%
Q02
R12
681
±1%
C08
470PF
R08
46.4K±1%
R21
1K±1%
TP-A
Q03
C03
220PF
R13
51.1±1%
R17
330
Q05
R19
330
R16
470
C07
33pf
R18
150
R14
51.1±1%
Q04
R22
1K±1%
TP-C
C04
220PF
R24
270
C05
15±20%
C06
15±20%
R25
270
NOTE:
1. DIODE PAIRS CR01,02 / CR03,04 / CR05,06 / CR07,08 / CR09,10 ARE MATCHED SILICON 50240201.
2. COMPONENT ASSY NO. 50041600
3. TRANSISTORS ARE 50210102.

FXB


93692001
R08
R07
Q04
Q03
Q01
R13
R14
C07
R19
R21
R22
R09
Q02
R17
R10
Q05
R18
R16
R15
R11
R12
R06
R05
C02
CR10
R04
R20
R03
CR09
C01
CR07
CR05
C08
C09
CR06
CR02
R02
CR04
CR03
CR01
R25
C06
C05
R24
C04
C03
R23
CARD FXB
PIN 1

# AGC RECTIFIER

## FYA/FYB

### FYA

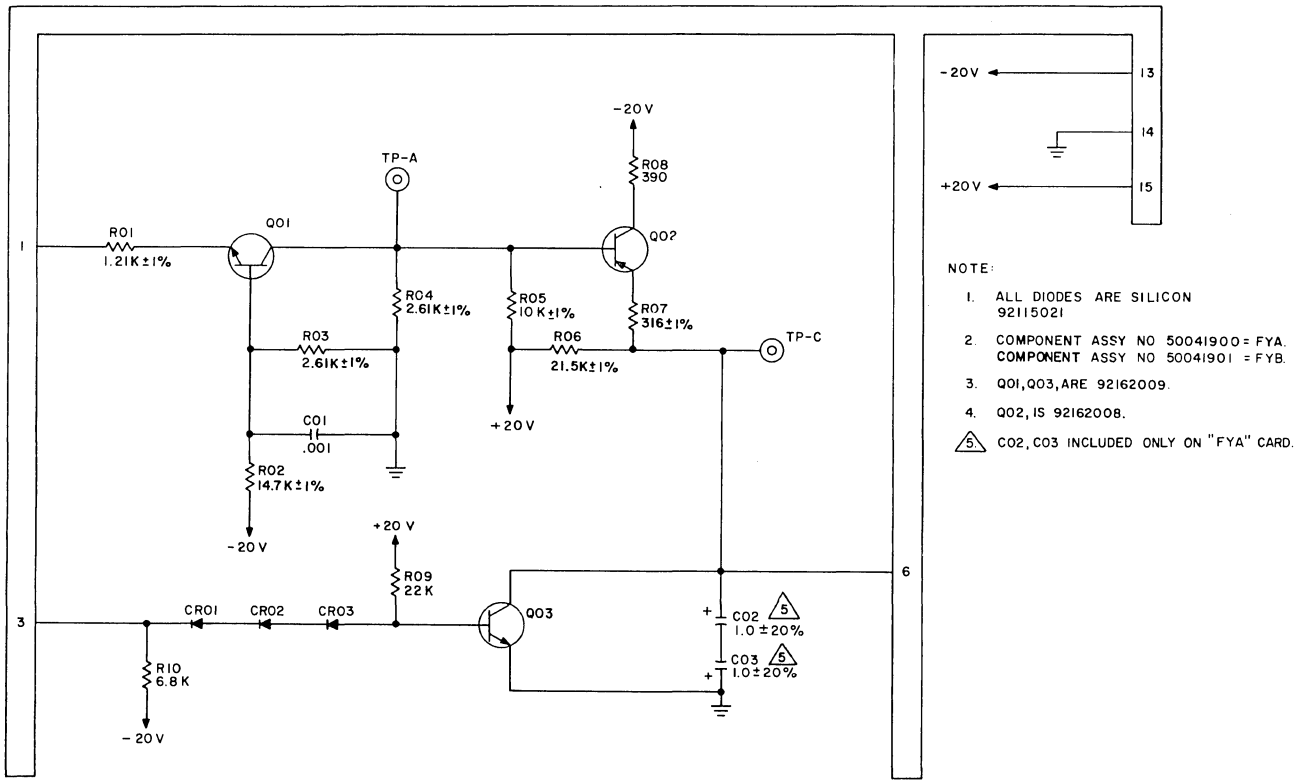
The FYA card generates a control signal for the EZA card in accordance with the average signal level of the input. The full-wave rectified output (pin 6, EJA card) is applied to pin 1. Resistors R02 and R03 define a reference voltage at the base of transistor Q01. The input signal must be more negative than this reference voltage if Q01 is to be turned on. Therefore, small disturbances at the input will be ignored.

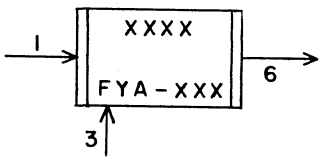
In the absence of a signal from Q01, resistors R04 and R05 will establish a steady-state voltage at the base of Q02. Resistors R06 and R07 will establish the voltage on capacitors C02 and C03. When a signal is applied at pin 1, which is more negative than the voltage on the base of Q01, Q01 will conduct. The base of Q02 goes more negative and causes Q02 to pull charge out of capacitors C02 and C03, making the voltage on pin 6 more negative. The time constant for pulling this point more negative is determined by R07, C02, and C03. Resistor R01 increases the input impedance seen by the EJA card, and helps determine the voltage transfer ratio of the Q01 circuit.

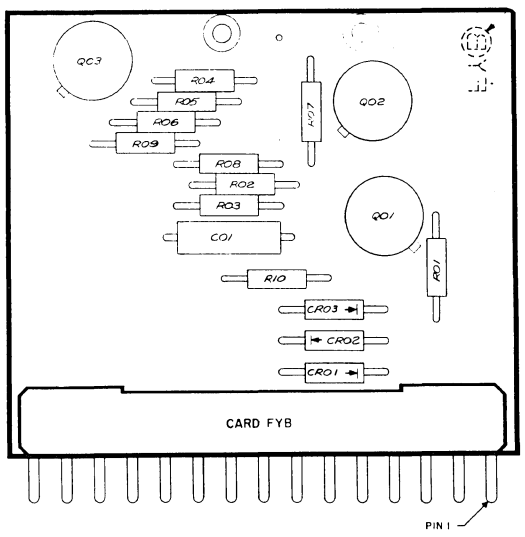
When the signal at pin 1 is no longer more negative than the voltage on the base of Q01, the voltage at pin 6 will return to its steady-state condition. The time constant for this change is determined by R06, C02, and C03. Since the value of R06 is considerably more than R07, the voltage on pin 6 can go negative more rapidly than it can go positive. This was necessary because of the data format used in the 852 Disk Pack. In this format there are 180 AGC bits, which determine the gain of the read chain for the following 900 data bits. The data in the 852 is in an NRZI recording technique. Therefore, since there may be only 300 "1's" in the 900 data bits, the time constants were adjusted to insure the voltage at pin 6 (determined by the 180 AGC bits) will not decay during the 900 data bits.

The above information applies if pin 3 is at -3v. If pin 3 is brought to ground, Q03 forces the voltage at pin 6 to ground, setting the attenuation of the EZA card to a nominal level. This is an "AGC Disable" function. The pin 6 voltage is applied to pin 9 of the EZA card as a gain control signal.

This card is identical to the FYA with the exception that C02 and C03 have been removed from the FYB card.



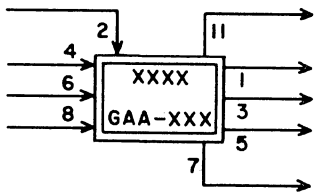



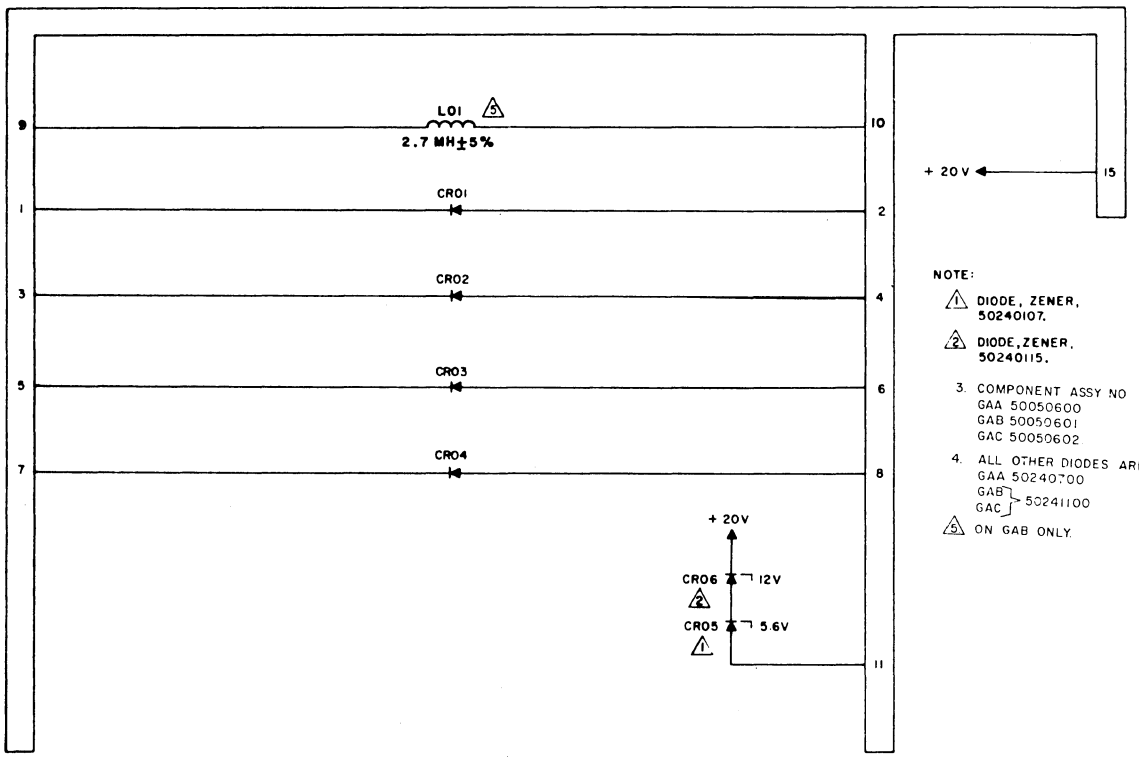
# DIODE CARDS
## GAA, GAB, GAC

Each card has four diodes with space for an additional diode. The diodes are used in series with write and erase heads to give the proper voltage levels necessary to prohibit the flow of current to the heads when a voltage checker system (BAA, BBA, BCA, or AYA) fires.

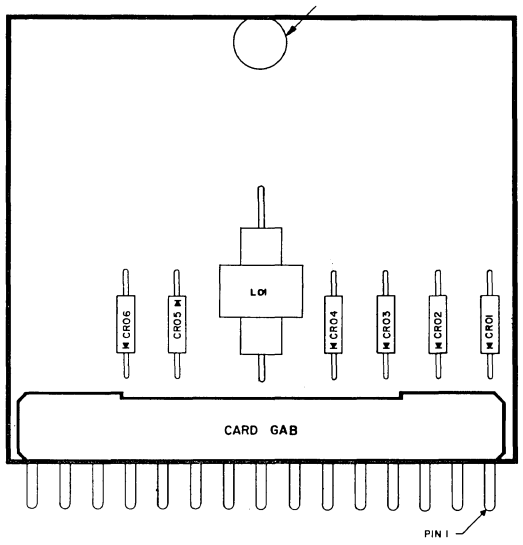
Diodes CR05 and CR06 are used in conjunction with the pin 1 input of the BAA card, or the pin 2 input of the AYA card to detect the state of the +20v supply.

SYMBOL




9
L01 ⚠5
2.7 MH±5%
10
+ 20 V
15
1
CR01
2
3
CR02
4
5
CR03
6
7
CR04
8
+ 20V
CR06 ⚠2 12V
CR05 ⚠1 5.6V
11
NOTE:
⚠1 DIODE, ZENER, 50240107.
⚠2 DIODE, ZENER, 50240115.
3. COMPONENT ASSY NO
GAA 50050600
GAB 50050601
GAC 50050602
4. ALL OTHER DIODES ARE
GAA 50240700
GAB, GAC 50241100
⚠5 ON GAB ONLY.

GAA, GAB, GAC


CR06
CR05
L01
CR04
CR03
CR02
CR01
CARD GAB
PIN 1

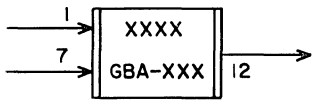
BRAKE-CLUTCH DRIVER

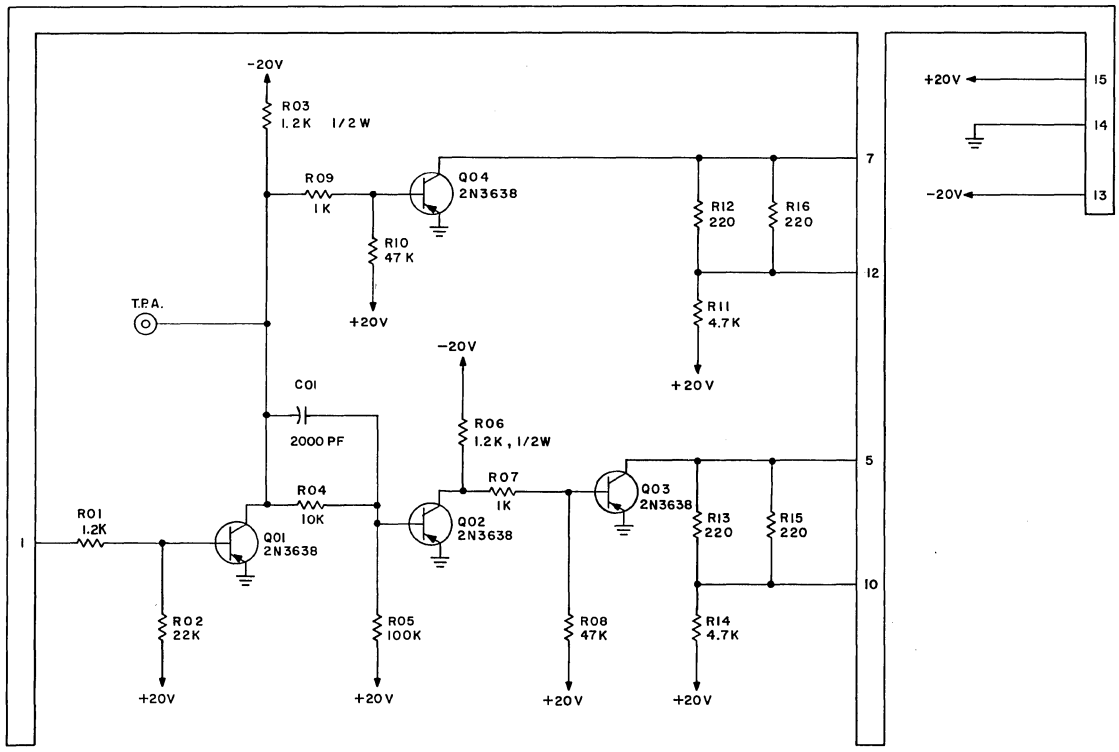
GBA

This circuit is designed for use in the 350 Paper Tape Reader when used with a 1700 Computer. It is similar to the 76A and 76B cards except the input circuit is designed for an input switching excursion of 0.3V at 0 ohm, and -5.4V at 470 ohm.

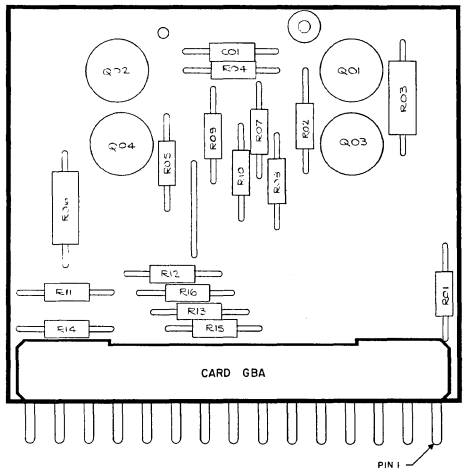
The input signal is inverted twice for the outputs at pins 7 and 12, and three times for the outputs at pins 5 and 10. Thus, one output circuit will always be on and the other off for either polarity of input. Pins 5 and 7 are normally returned to -25V via separate external 200 ohm resistors. Pins 10 and 12 are biased suitably for direct connection to the bases of separate external PNP germanium power transistors operated with grounded emitters. In this intended application, the ON condition is -0.5V max at 125 ma and the OFF condition is -9V (pins 5 and 7). The biased outputs (pins 10 and 12), when operated into the base of external PNP germanium power transistors, have approximate excursions from -1V at -75 ma to 0V at + 1ma.

SYMBOL




-20V
R03
1.2K 1/2W
R09
1K
Q04
2N3638
R10
47K
+20V
T.P.A.
C01
2000 PF
-20V
R06
1.2K, 1/2W
R07
1K
R04
10K
Q02
2N3638
Q03
2N3638
R01
1.2K
Q01
2N3638
R02
22K
R05
100K
R08
47K
R12
220
R16
220
R11
4.7K
R13
220
R15
220
R14
4.7K
+20V
+20V
+20V
+20V
+20V
+20V
+20V
-20V
15
14
13
7
12
5
10
1

GBA


C01
R04
Q02
Q01
R03
Q04
Q03
R09
R07
R02
R05
R13
R08
R12
R16
R11
R13
R15
R14
R01
CARD GBA
PIN 1

## 500 CYCLE TWIN "T" NOTCH NETWORK
## GCA

The twin "T" network is used in the disc file servo actuator to "kill" the servo response to an undesirable mechanical response in the carriage.

An operational amplifier is connected between pins 2 and 7 with input at pin 2. The velocity signal from the servo is put into pin 1, and the output from pin 10 is put into the summing point of the servo acceleration operational amplifier.

If the velocity is assumed to be sinusoidal of constant amplitude but varying frequency, the voltage at pin 7 (with the operational amplifier connected) will be a linear increasing function of frequency for frequencies below the twin "T" notch frequency which is set to the unwanted frequency. However, the gain will be less than unity. This occurs because for frequencies below approximately 400 cycles, there is little or no attentuation thru the twin "T". Therefore, resistor R02 divided by R01 + jXc01 determines the gain. At the notch frequency of 500 cycles, no signal gets thru the twin "T", so the gain is determined by R08 divided by R01 + jXc01. At this point the gain rises to approximately 3. Thus, the output at pin 10 is seen to peak-up at 500 cycles. This peaked up signal is added in with the normal acceleration signal. However, since it has undergone one additional phase inversion in the operational amplifier, it will be out of phase with the acceleration signal and thereby subtract out the undesired 500 cycle signal. Potentiometer R03 allows for adjustment of the null depth at 500 cycles.

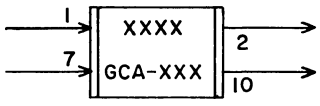
The emitter follower is used to prevent loading on the twin "T", and provide a low impedance driver for the suming resistor R02.

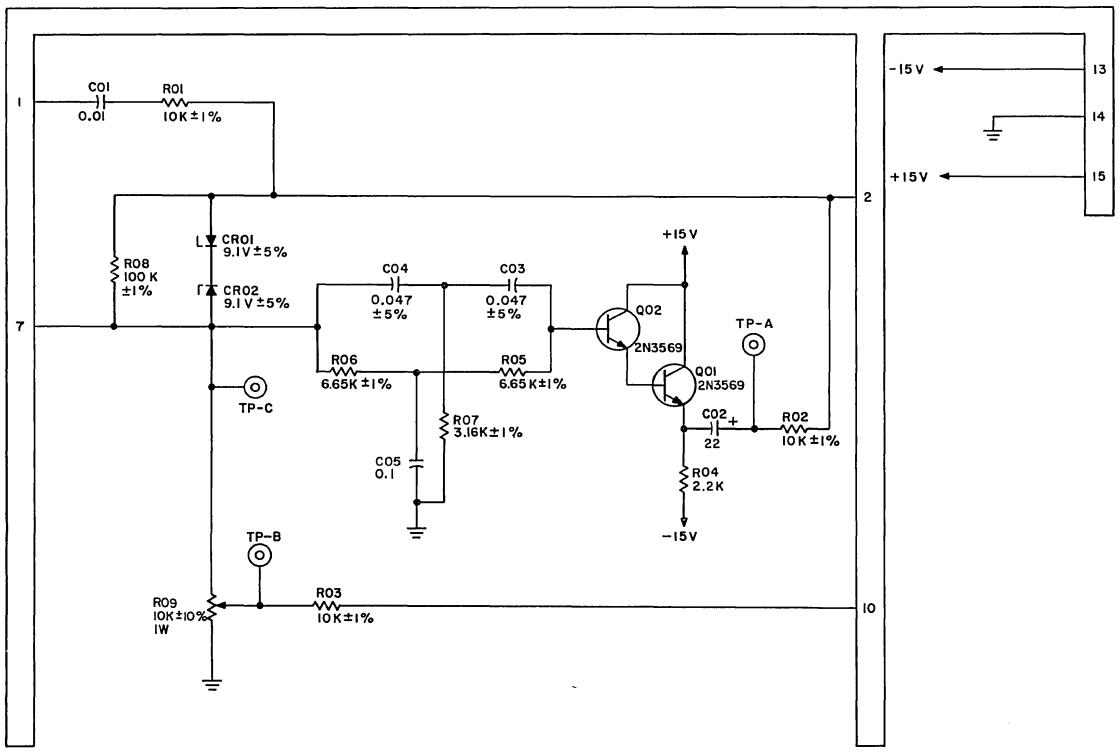
Zerner diodes CR01 and CR02 limit the output voltage of the operational amplifier to approximately $\pm$10v.

## VARIABLE FREQUENCY TWIN "T" NOTCH NETWORK
## GCB

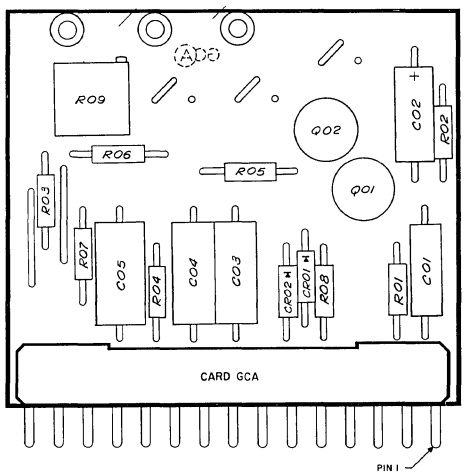
The GCB card is the same as the GCA, except that the null frequency can be adjusted by means of R10, R11, and R12 between approximately 350 and 800 cycles.

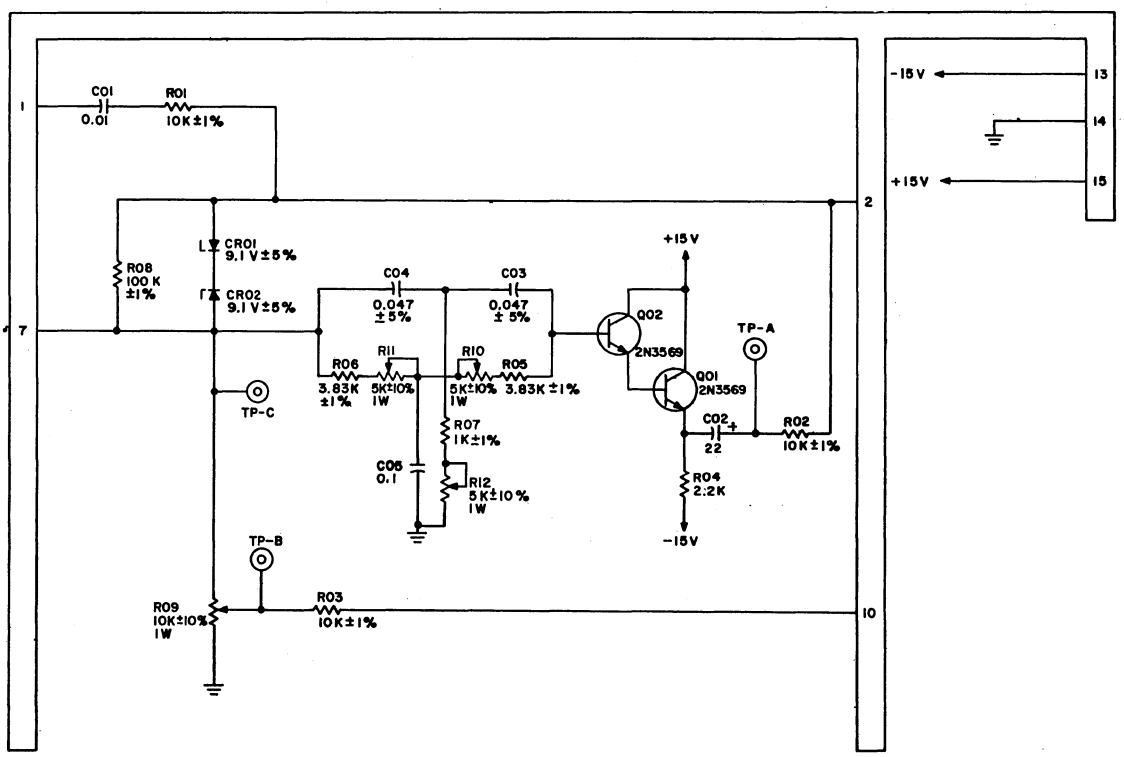
SYMBOL



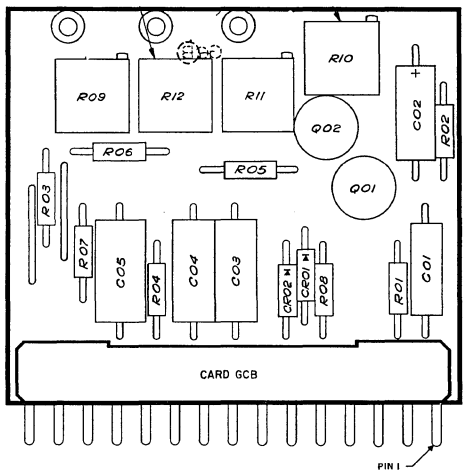

C01
0.01
R01
10K ±1%
CR01
9.1V ±5%
CR02
9.1V ±5%
R08
100 K
±1%
C04
0.047
±5%
C03
0.047
±5%
R06
6.65K ±1%
R05
6.65K ±1%
R07
3.16K ±1%
C05
0.1
+15V
Q02
2N3569
Q01
2N3569
TP-A
C02
22
R02
10K ±1%
R04
2.2K
-15V
TP-C
TP-B
R09
10K ±10%
1W
R03
10K ±1%
-15V
+15V
1
2
7
10
13
14
15

GCA


R09
R06
R05
R03
R07
C05
R04
C04
C03
CR02
CR01
R08
R01
C01
Q02
Q01
C02
R02
CARD GCA
PIN 1


C01
0.01
R01
10K±1%
CR01
9.1V±5%
CR02
9.1V±5%
R08
100K
±1%
C04
0.047
±5%
C03
0.047
±5%
R06
3.83K
±1%
R11
5K±10%
1W
R10
5K±10%
1W
R05
3.83K±1%
Q02
2N3569
Q01
2N3569
TP-A
TP-C
R07
1K±1%
C05
0.1
R12
5K±10%
1W
C02
22
R02
10K±1%
R04
2.2K
+15V
-15V
TP-B
R09
10K±10%
1W
R03
10K±1%
-15V
+15V
1
2
7
10
13
14
15

GCB


R09
R12
R11
R10
C02
R02
Q02
R06
R05
Q01
R03
R07
C05
R04
C04
C03
CR02
CR01
R08
R01
C01
CARD GCB
PIN 1

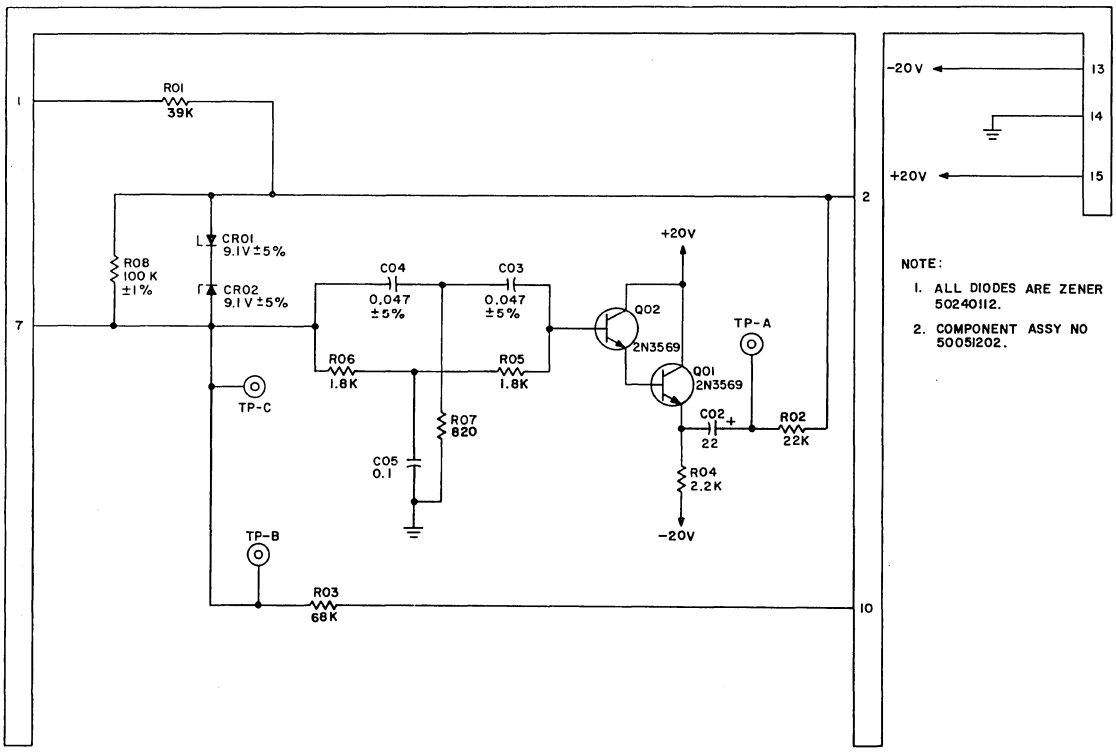
# NOTCH NETWORKS
## GCC, GCD

The twin "T" networks are intended to be used in cascade to attenuate the disk file servo response at frequencies of undesirable mechanical resonances of the carriage.

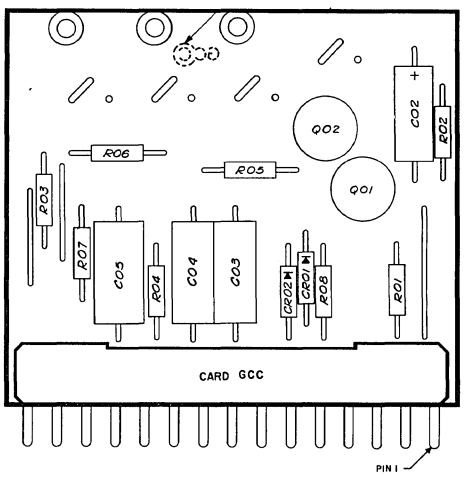
An operational amplifier is connected between pins 2 and 7 of both the GCC and GCD cards with input at pin 2. Pin 1 of the GCD is connected to the output of the acceleration amplifier. Pin 7 or 10 of the GCD is connected to pin 1 of the GCC. Pin 10 of the GCC is then connected to the input of the acceleration amplifier. This arrangement provides attenuation of the acceleration signal from approximately 450 cycles to approximately 2 KC.

At the notch frequency, 500 cycles for the GCD and 1800 cycles for the GCC, there is very little attenuation through the twin "T". The signal at these frequencies is fed back out of phase with the input signal, thereby attenuating the output of the acceleration signal.

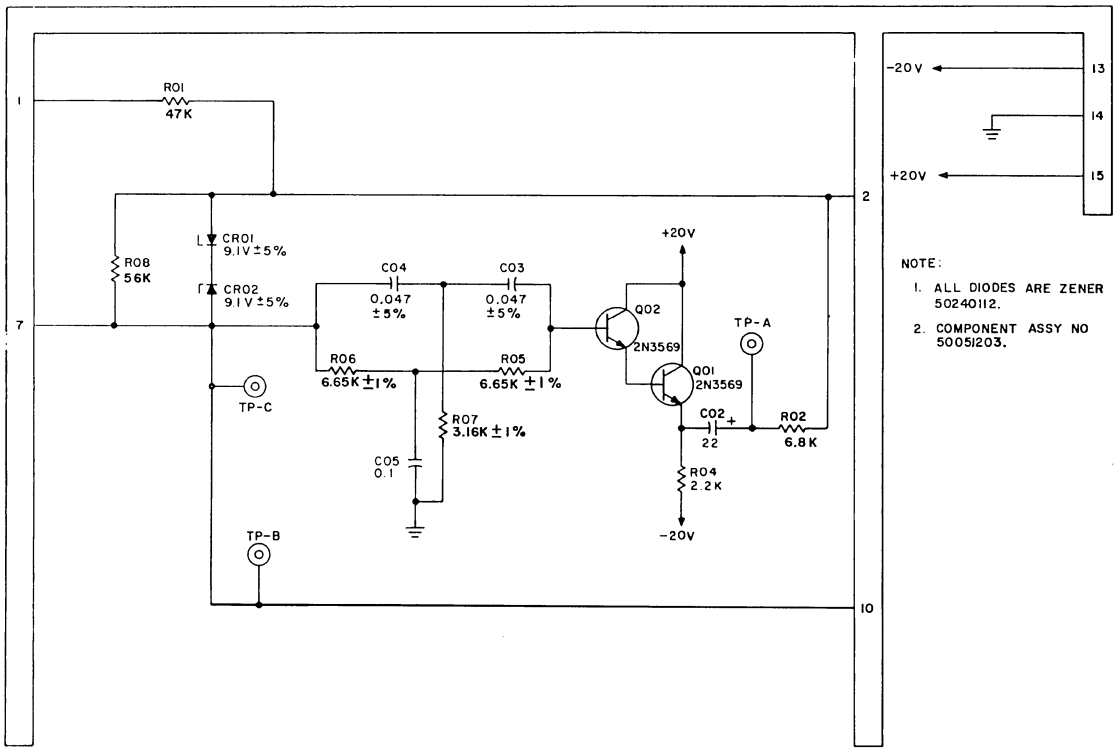
SYMBOL



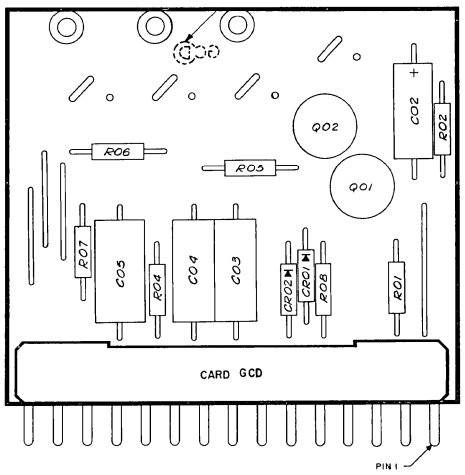

GCC




6-GCC, GCD-2


R01
47K
R08
56K
CR01
9.1V±5%
CR02
9.1V±5%
C04
0.047
±5%
C03
0.047
±5%
R06
6.65K±1%
R05
6.65K±1%
R07
3.16K±1%
C05
0.1
TP-C
TP-B
+20V
Q02
2N3569
Q01
2N3569
TP-A
C02
22
R02
6.8K
R04
2.2K
-20V
-20V
+20V
1
2
7
10
13
14
15
NOTE:
1. ALL DIODES ARE ZENER 50240112.
2. COMPONENT ASSY NO 50051203.

GCD


Q02
C02
R02
R06
R03
Q01
R07
C05
R04
C04
C03
CR02
CR01
R08
R01
CARD GCD
PIN 1

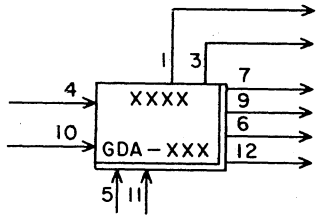
# PRESSURE TRANSDUCER CIRCUIT
## GDA

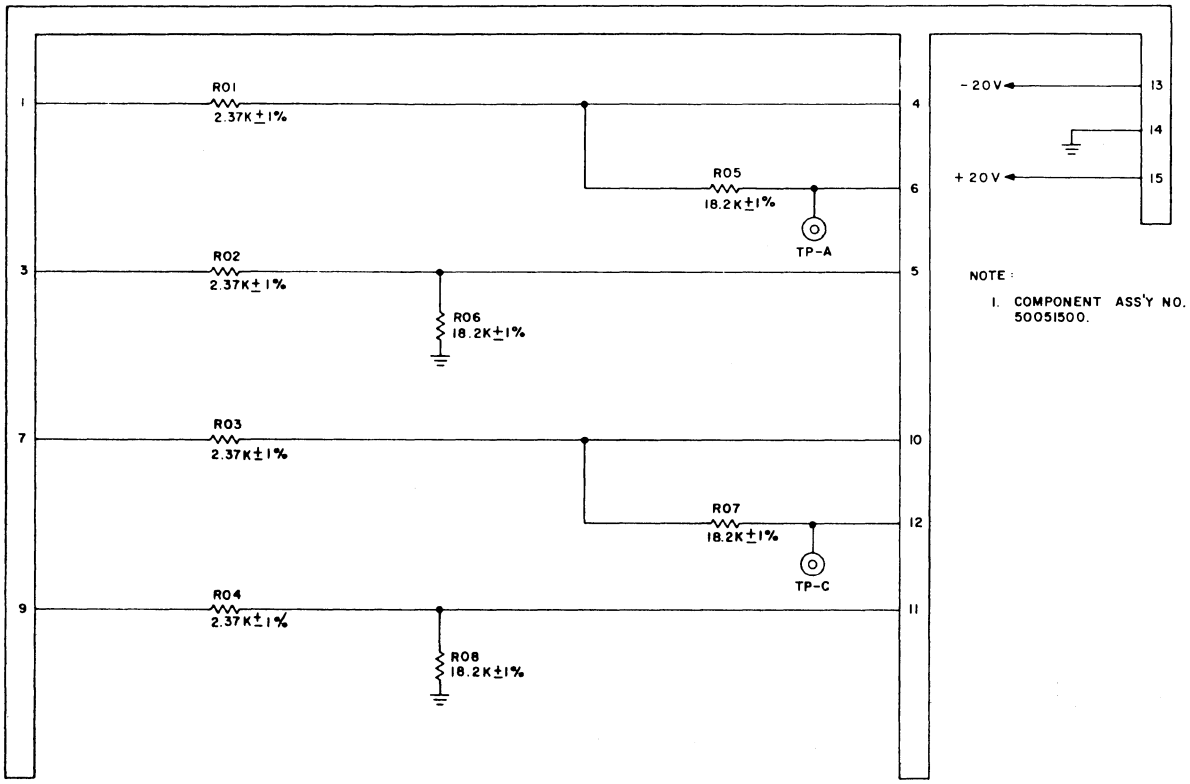
The GDA consists of resistors and is intended to be used with operational amplifiers to derive a signal from bridge type transducers.

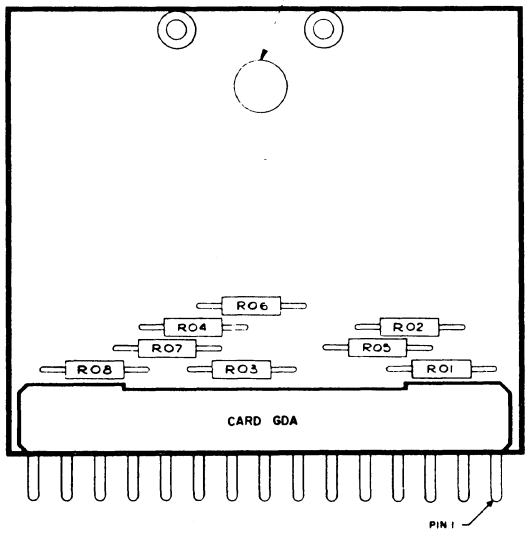
The outputs of the transducer bridge are connected to pins 1 and 3 or pins 7 and 9. The noninverting input of an operational amplifier is connected to pin 5 or 11 and the inverting input is connected to pin 4 or 10. The output of the amplifier is connected to pin 6 or 12.

The operational amplifier is being used in the differential mode and provides a voltage output proportional to the hydraulic pressure. The differential gain is equal to: R05/R01 = R06/R02 = R07/R03 = R08/R04.

SYMBOL




R01
2.37K±1%
R05
18.2K±1%
TP-A
R02
2.37K±1%
R06
18.2K±1%
R03
2.37K±1%
R07
18.2K±1%
TP-C
R04
2.37K±1%
R08
18.2K±1%
1
3
4
5
6
7
9
10
11
12
-20V
+20V
13
14
15
NOTE:
1. COMPONENT ASS'Y NO. 50051500.


R06
R04
R02
R07
R05
R08
R03
R01
CARD GDA
PIN 1

# DIFFERENTIAL PRESSURE GAIN AND BALANCE
## GEA

The GEA contains passive elements used with an operational amplifier and an active voltage source to supply D. C. excitation to two bridge circuits. The circuit is used on the disk file actuator servo.

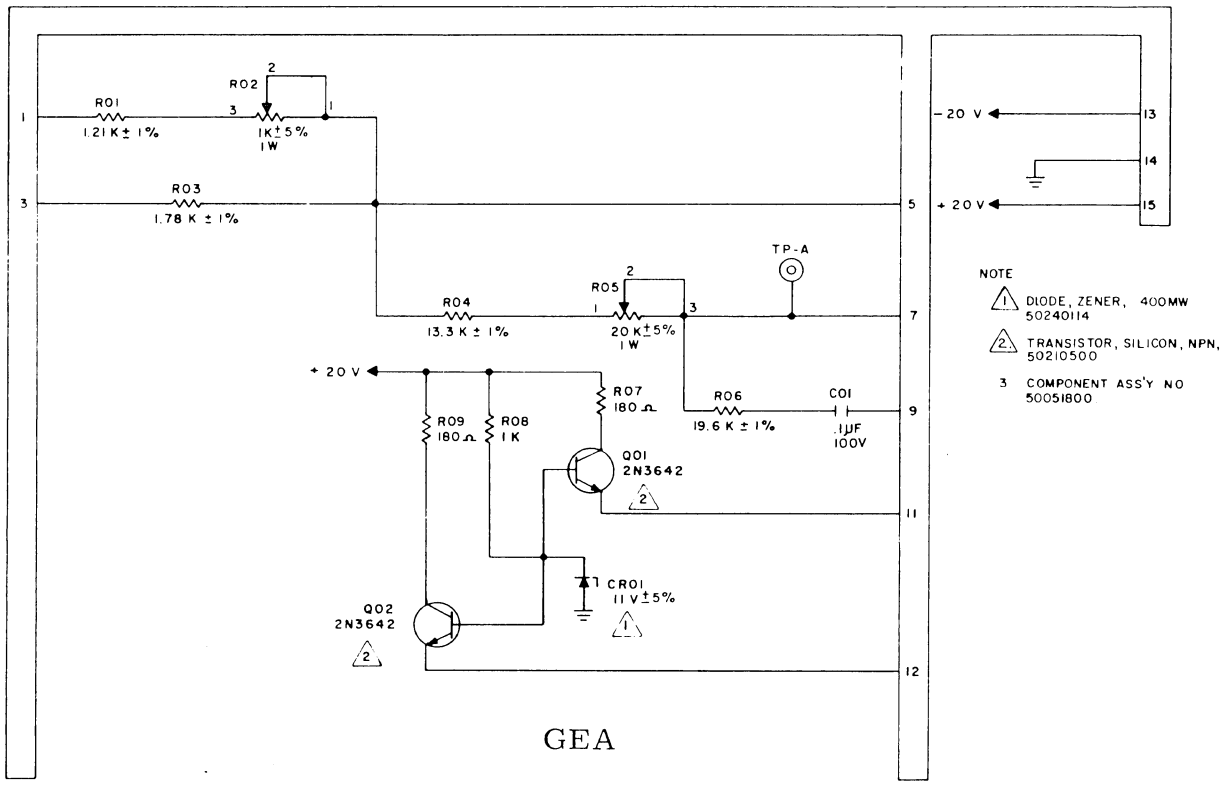
The inputs at pins 1 and 3 are supplied from operational amplifiers whose outputs are proportional to the hydraulic pressure. These are added "out of phase" to give the difference in pressures.

The potentiometer R02 balances the gain of the two pressure transducers. The amplifie input is connected to pin 5 and output to pin 7. The gain of the amplifier is R04 plus R05 divided by R01 plus R02 or R03.

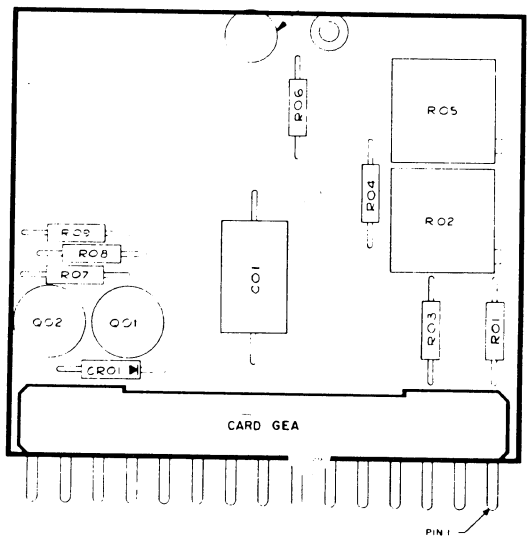
The output of the amplifier is connected to R06 and C01 and is intended to be connected to the input of another operational amplifier.

The zener diode CR01 and Q01 and Q02 are intended to provide a nominal 10v D. C. excitation voltage to the nominal 350-ohm transducer bridge.

SYMBOL


R01
1.21 K ± 1%
R02
1K ± 5%
1W
R03
1.78 K ± 1%
R04
13.3 K ± 1%
R05
20 K ± 5%
1W
TP-A
R06
19.6 K ± 1%
C01
.1 µF
100V
R07
180 Ω
R08
1 K
R09
180 Ω
Q01
2N3642
Q02
2N3642
CR01
11 V ± 5%
+ 20 V
- 20 V
+ 20 V
NOTE
1. DIODE, ZENER, 400MW
50240114
2. TRANSISTOR, SILICON, NPN,
50210500
3 COMPONENT ASS'Y NO
50051800

GEA


R06
R05
R04
R02
R09
R08
R07
C01
Q02
Q01
R03
R01
CR01
CARD GEA
PIN 1

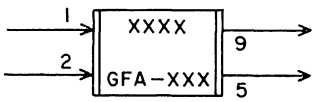
# LONG STROKE ACCELERATION
## GFA, GFB

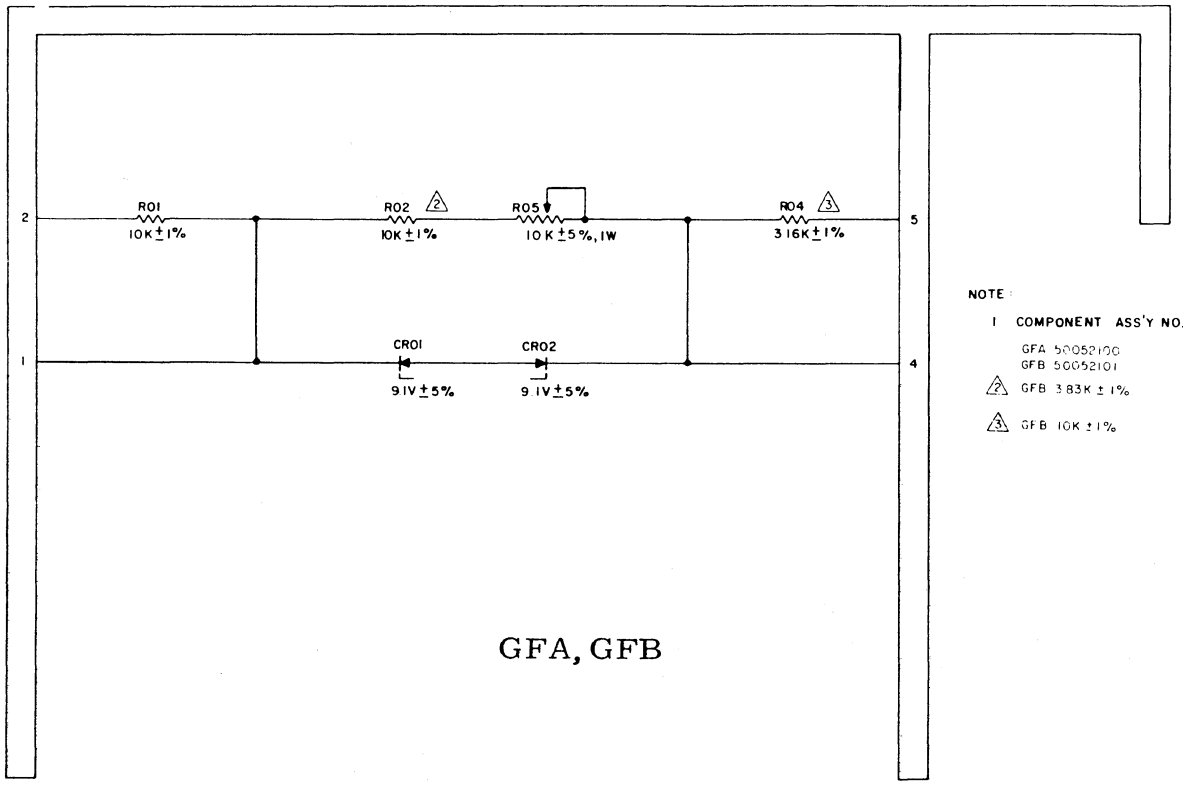
These cards contain passive feedback networks intended to be used with an operational amplifier in the disk file actuator servo.

The cards provide the necessary acceleration gain for long stroke operation. The input at pin 2 is fed to the acceleration amplifier, and the output at pin 5 is connected to the input of the long stroke summing amplifier.

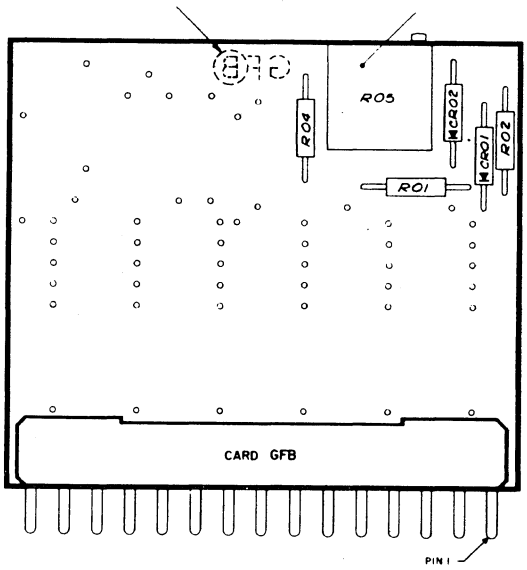
The gain of the feedback is: R05 plus R02 divided by R01. The zener diodes CR01 and CR02 limit the output of the amplifier to approximately $\pm$ 10v.

SYMBOL




R01
10K ± 1%
R02
10K ± 1%
R05
10 K ± 5%, 1W
R04
3.16K ± 1%
CR01
9.1V ± 5%
CR02
9.1V ± 5%
2
1
5
4
NOTE:
1 COMPONENT ASS'Y NO.
GFA 50052100
GFB 50052101
2 GFB 3.83K ± 1%
3 GFB 10K ± 1%

GFA, GFB


R04
R05
CR02
CR01
R02
R01
CARD GFB
PIN 1

# DIFFERENTIAL PRESSURE AND ACCELERATION CROSSOVER TRIM

## GFC

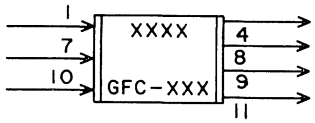
The GFC is a passive network used to trim the acceleration signal in the disk file actuator servo.

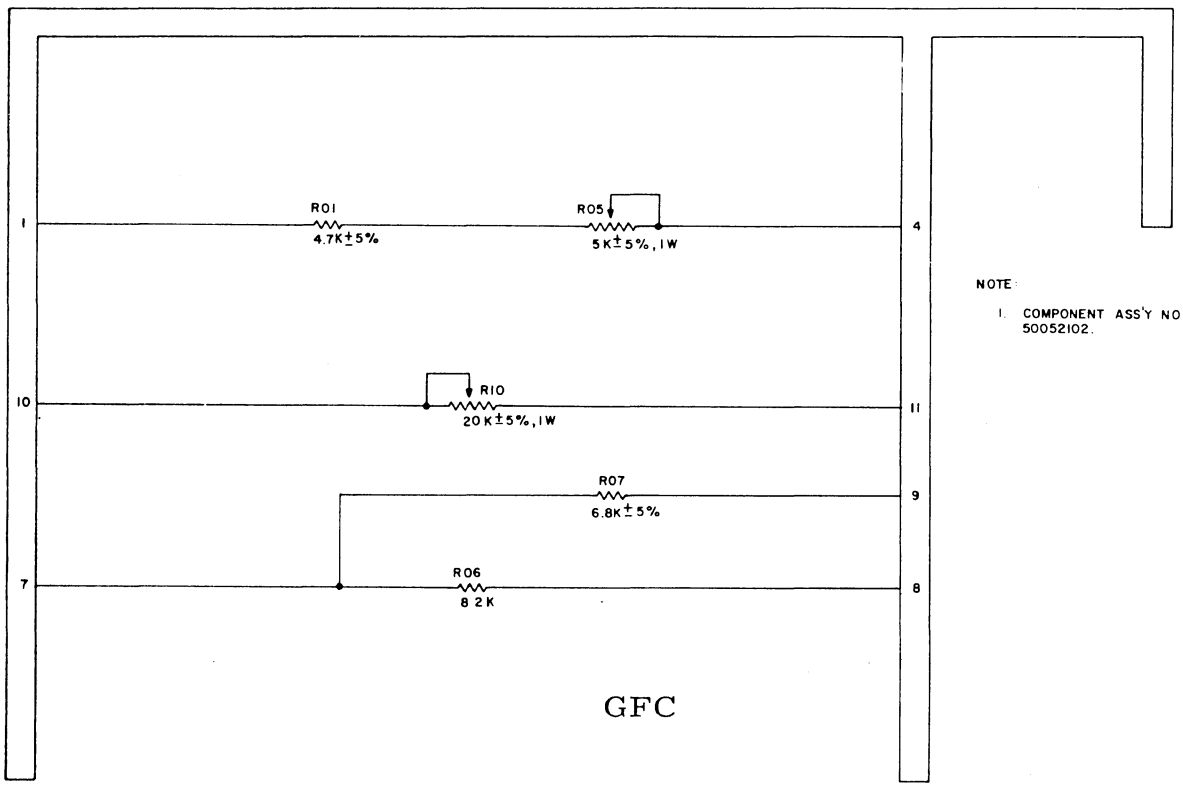
The acceleration signal used in the servo system is derived from two sources. Below 50 cycles, the acceleration is derived by differentiating the velocity signal. Above 50 cycles, the acceleration signal is derived from a differential the hydraulic pressure.

For satisfactory transient response, it is necessary to closely match the RC time constants of the acceleration circuit. Potentiometer R10 is used to match the time constant of the acceleration and differential pressure crossover network.

Potentiometer R05 and R01 and R06 are used in the time constant matching procedure.

SYMBOL

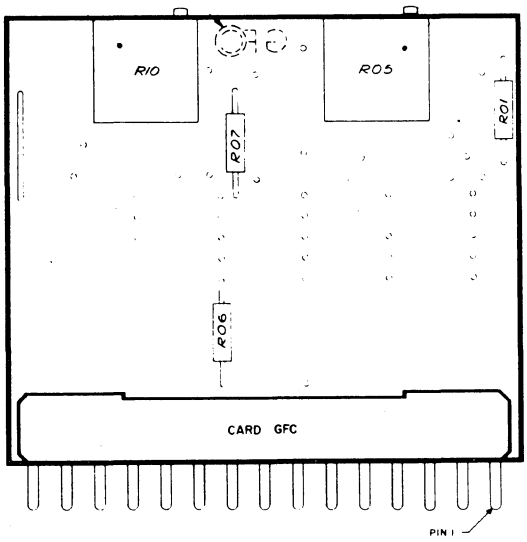





NOTE:

1. COMPONENT ASS'Y NO 50052102.

GFC



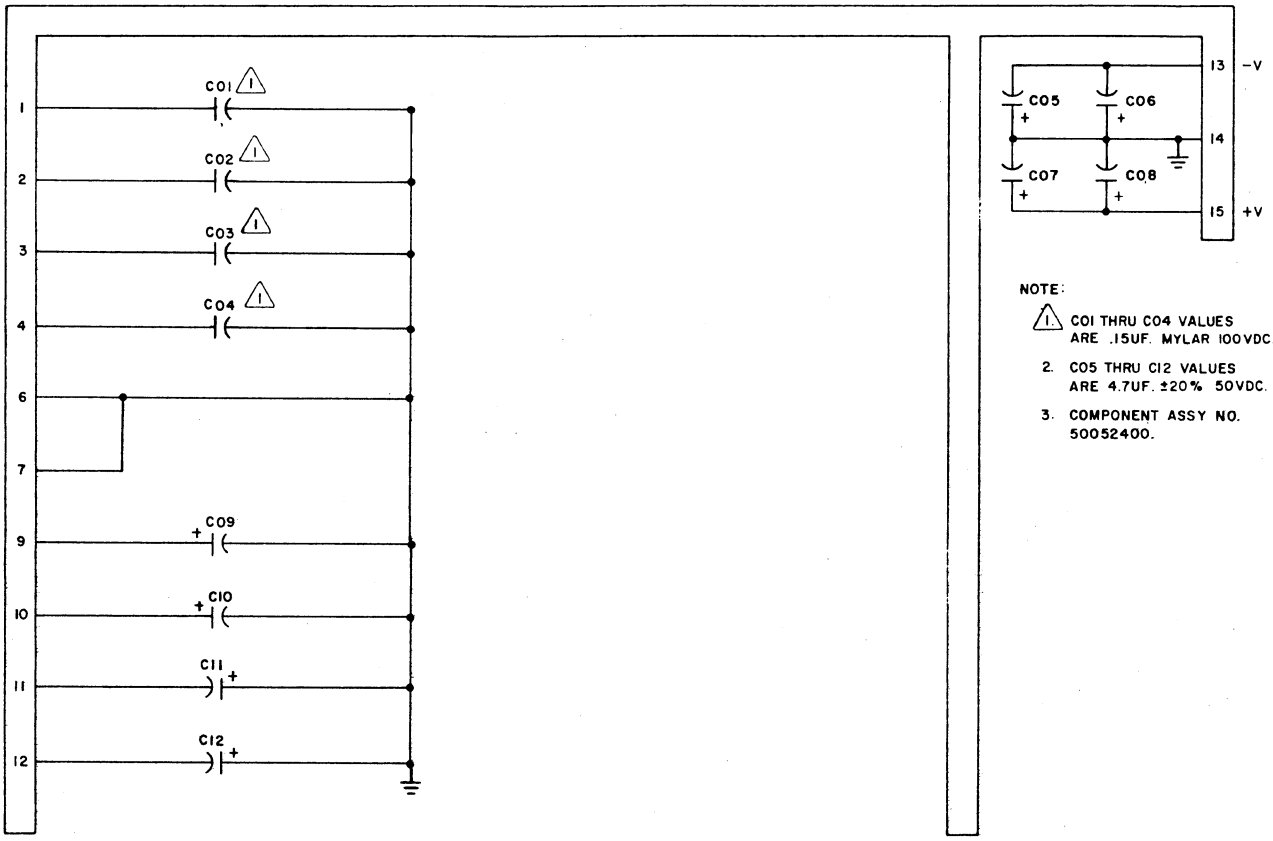
# CAPACITOR CARD

## GGA

This card is designed for use in the disk storage drives for decoupling purposes.

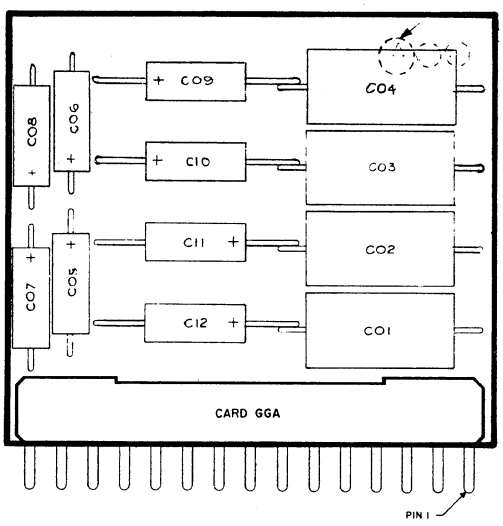
The card consists of four .15 uf @ 100-vdc Mylar capacitors from pins 1 through 4 to ground and four 4.7 uf @ 50-vdc tantalum electrolytic capacitors from pins 9 through 12 to ground. The capacitors on pins 9 and 10 have their negative sides grounded and those on pins 11 and 12 have their positive sides grounded. Pin 13 has two 4.7 uf @ 50-vdc tantalum capacitors in parallel with the positive side grounded and pin 15 has two 4.7 uf tantalum units with the negative side grounded.

The tantalum capacitors are used for frequencies below 1 MHz (which is near the self resonant frequency at which the units are essentially 0.2-ohm resistor for ac). Beyond this frequency they appear inductive and can cause trouble unless bypassed for the higher frequencies. The 0.15 uf Mylar capacitors are useful to frequencies up to about 5 MHz.




NOTE:

1. C01 THRU C04 VALUES ARE .15UF. MYLAR 100VDC
2. C05 THRU C12 VALUES ARE 4.7UF. ±20% 50VDC.
3. COMPONENT ASSY NO. 50052400.



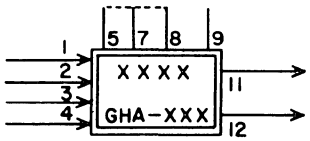
# PREAMPLIFIER
## GHA

This card normally drives the EJA* (peak level detector card) and is operable either as a differential amplifier or as a single-ended amplifier. The nominal differential voltage gain ranges from 50 to 4700, with 50 to 2000 as a suggested range. Nominal differential input and output impedances are 8K ohms and 56 ohms respectively at 250 KHz. The frequency response band pass is from 280 Hz to 520 KHz at a gain value of 1000. Low frequency response improves with a lower gain value setting such as 80 Hz to 470 Hz at a gain value of 100. The single-ended amplifier configuration output and input impedances are nominally 30 ohms and 8K ohms respectively at 250 KHz. When operating as a single-ended amplifier, a bias supply voltage of -12v must be connected in series with the load (applied to pins 11 or 12) and ground.

The complete preamplifier circuit employs two differential amplifier stages with emitter amplifiers cascaded. Transistors Q01 and Q02 are in the first stage with Q03 and Q04, respectively, as emitter followers; Q05 and Q06 are in the second stage with Q07 and Q08 as the respective emitter followers. The emitter follower transistors provide a low output impedance. Negative feedback stablizes the voltage gain of the preamplifier. In the first stage, R15 provides local negative feedback; while in the second stage, potentiometers R19 and R20 are utilized to adjust the preamplifier gain and provide some local negative feedback, respectively.

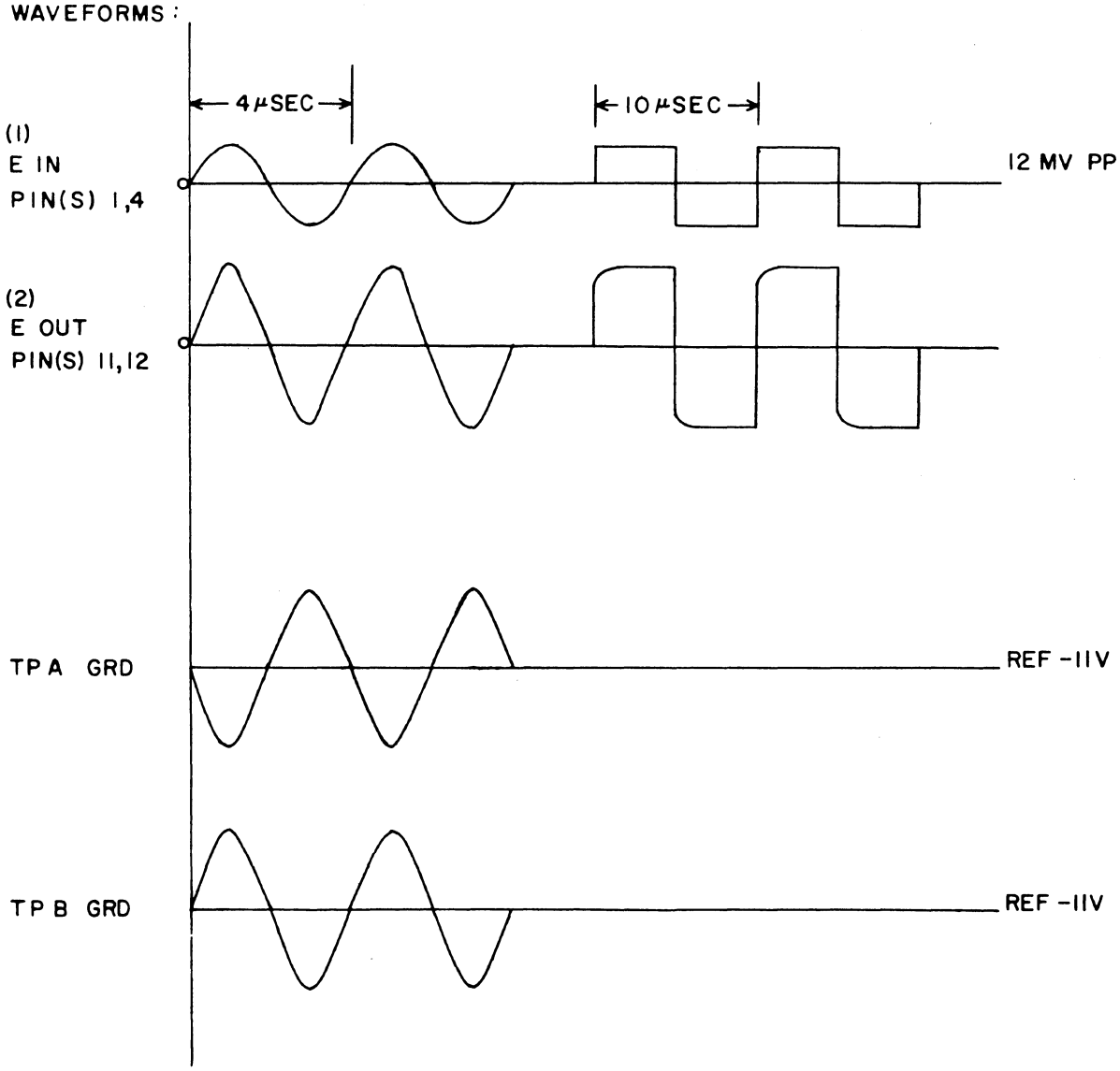
The voltage regulator circuit consisting of zener diodes CR1 and CR2 and resistors R16 and R18 gives a voltage gain stability of 1% for a 10% change in the ±20v power supply. The common mode rejection ratio is 65 d. b. at 60 KHz and 27 d. b. at 250 KHz.

The GHA may be used to amplify square wave or pulse signals. The pulse shape will be preserved for pulse widths from 2 usec to 100 usec. The square wave output signal will show a tilt that is inversely proportional to the applied input signal frequency. A 1 KHz input square wave signal will result in an output square wave signal with 25% tilt.



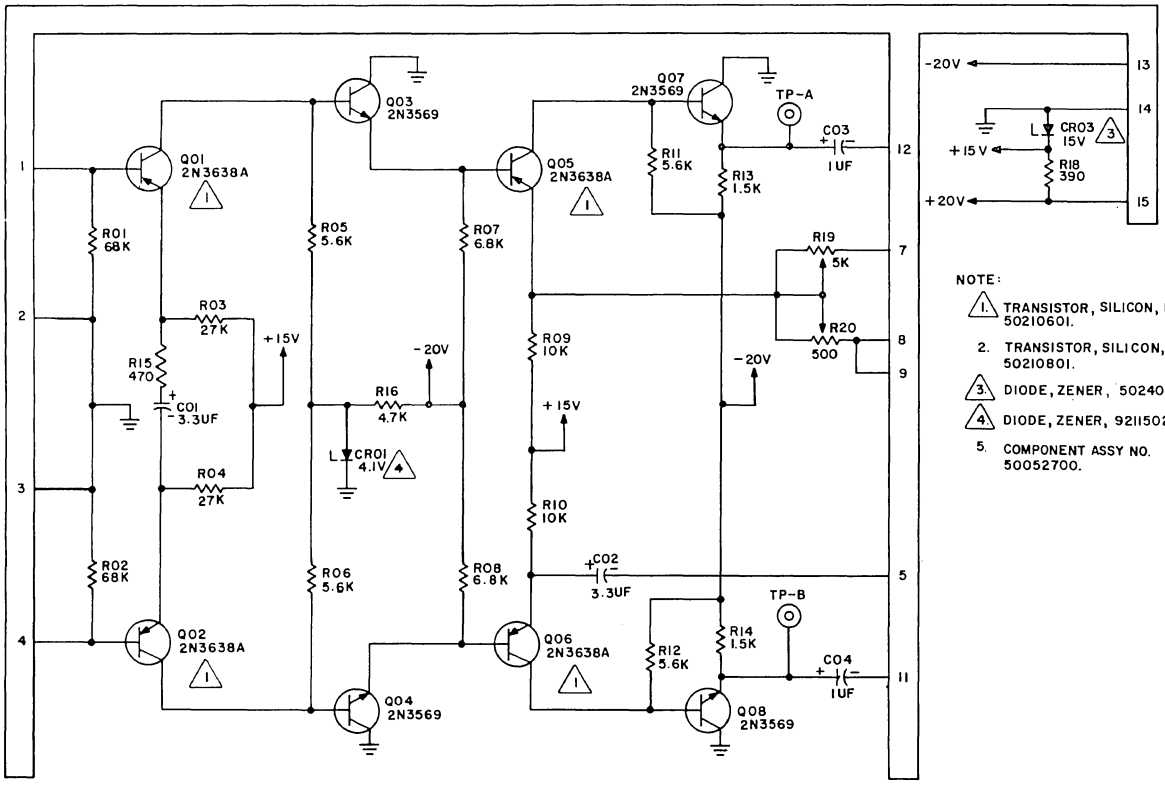

*CAUTION: Output pins 11 and 12 must be biased to -12v thru 680 ohms if the load is other than the EJA.

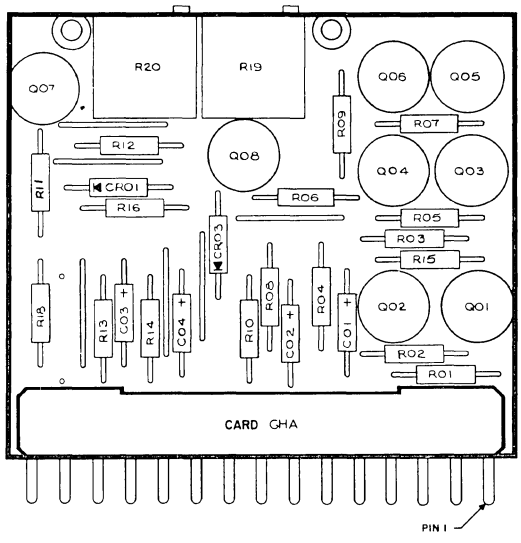
WAVEFORMS :




(1) Input Pin Numbers 1 to 4 (differential)
Voltage Excursion: 21.4 MVpp (Max.) Pins 5 & 8 jumpered
400 MVpp (Max.) Pins 5 & 7 jumpered

(2) Output Pin Numbers 11 to 12 (differential)
Voltage Excursion: 25 Vpp (Max.) No Load
10 Vpp (Max.) Load of 1362 ohms


Q01 2N3638A
Q02 2N3638A
Q03 2N3569
Q04 2N3569
Q05 2N3638A
Q06 2N3638A
Q07 2N3569
Q08 2N3569
R01 68K
R02 68K
R03 27K
R04 27K
R05 5.6K
R06 5.6K
R07 6.8K
R08 6.8K
R09 10K
R10 10K
R11 5.6K
R12 5.6K
R13 1.5K
R14 1.5K
R15 470
R16 4.7K
R18 390
R19 5K
R20 500
C01 3.3UF
C02 3.3UF
C03 1UF
C04 1UF
CR01 4.1V
CR03 15V
TP-A
TP-B
+15V
-20V
+20V
NOTE:
1. TRANSISTOR, SILICON, PNP 50210601.
2. TRANSISTOR, SILICON, NPN 50210801.
3. DIODE, ZENER, 50240117.
4. DIODE, ZENER, 92115027.
5. COMPONENT ASSY NO. 50052700.


CARD GHA
PIN 1

# READ LEVEL DETECTOR
## GIA, GIB

The function of these cards is to detect the amplitude of incoming read signals and to initiate enabling pulses whenever the amplitude of the read signals exceeds a predetermined threshold voltage.

These cards are identical in operation to the EJA with the following exceptions:

(1) The linearity has been improved for the operating range of 0.8 Vp to 8.0 Vp output.

(2) The input level required to give an 8.0 Vp output is 7.4 Vpp on pins 1 and 2 while the input on the EJA is 4.0 Vpp to give an 8.0 Vp output;

(3) The GIA is designed to operate to 500 KHz, to maintain linearity, and to balance peak outputs;

(4) The GIB is designed to operate with the OGC at 3200 FCI (240 KHz).

A preamplifier card supplies the read level detector with a differential input signal at levels ranging from 0v to 10v peak to peak. As each peak is detected, a rectified negative-going waveform can be seen at TP-A. This waveform is buffered and fed to both a peak detector (thru pin 6) and the comparator circuit (Q7 and Q8). The comparator circuit generates an enabling pulse (TP-B) whenever the amplitude exceeds the dc reference level applied at pin 7. Pin 8 may be grounded through a switch to allow R11 to serve as part of a voltage divider network connected to pin 7. This enabling pulse is fed by the switching circuit (Q9 and Q10) to the OGD, triggering a constant-width pulse.

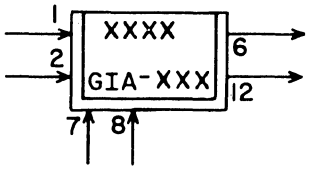
Transistors Z1-Q2 and Z2-Q2 are used as diodes to forward-bias Z1-Q1 and Z2-Q1 for collector currents of 0.25 ma each. This bias current develops a dc voltage of -0.35v at TP-A with a zero level signal at the input. The circuit is linear between 0.8v and 8v at TP-A.

The voltage comparator circuit consists of Q7 and Q8 with the reference dc voltage applied at either pin 7 or 8. Transistors Q9 and Q10 make up the switching circuit which delivers the enable pulse.

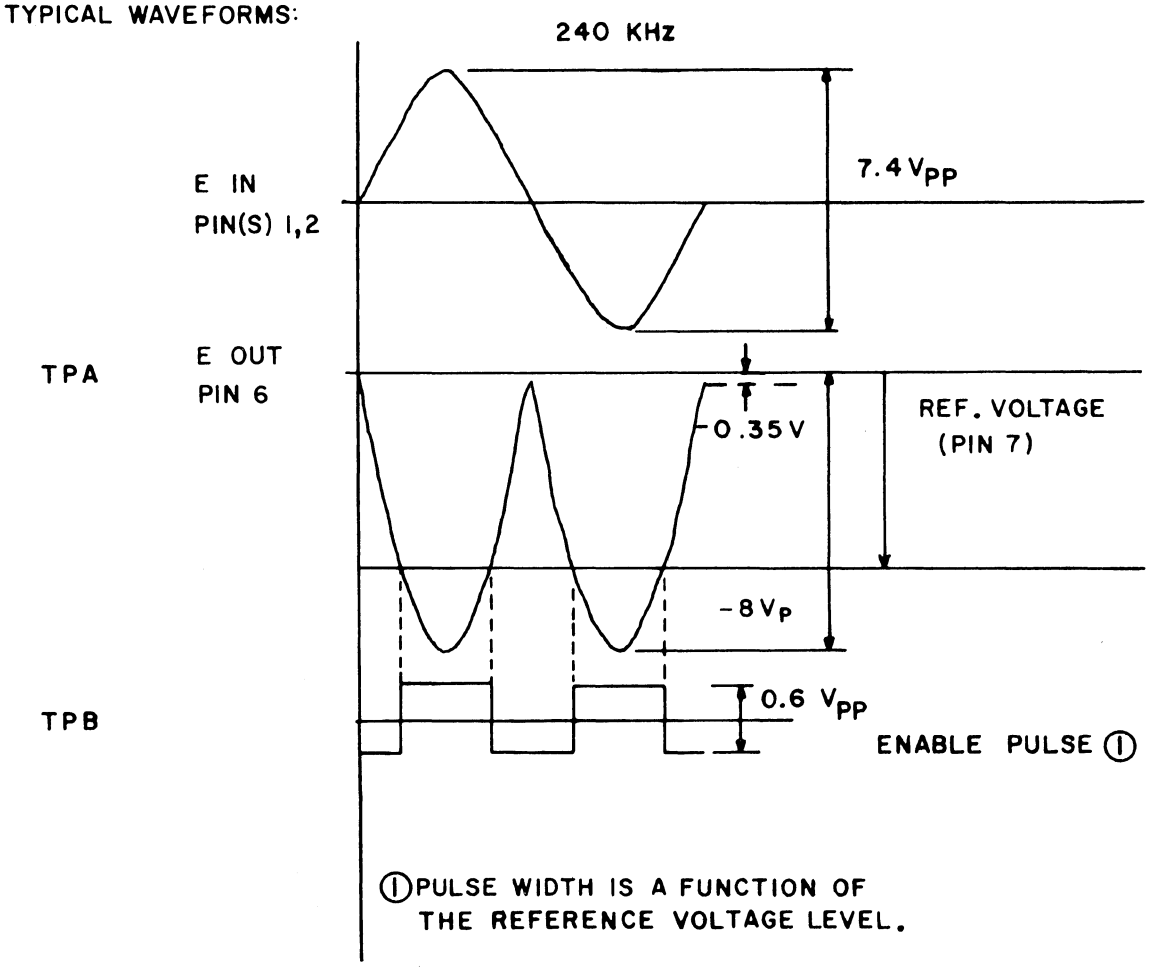
Resistor R20 may be used as a test variable to select the desired offset voltage and

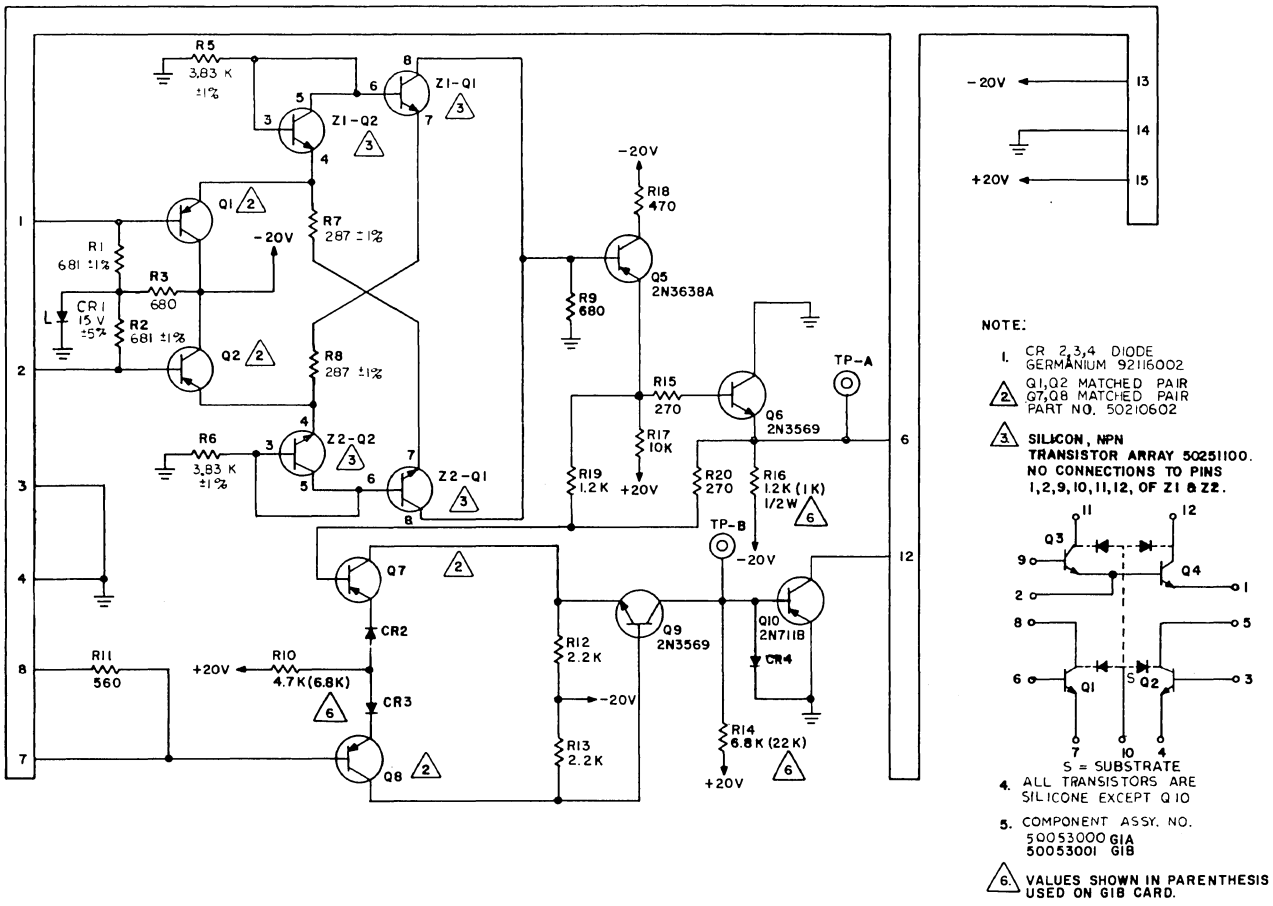
enhance the linearity of the entire read chain. This effect will cancel the initial small non-response required to take either Q5 or Q6 out of conduction as each peak is detected. An offset of -0.3v best linearizes the level detector. This voltage level is obtained by giving R20 a value of 270 ohms. Reference comparison voltages at this offset level are possible but detection below -0.5 is not recommended.

The OGD is the normal load for the GIA. Pins 6 and 12 are connected to pins 4 and 8 of the OGD respectively.




TYPICAL WAVEFORMS:






NOTE:

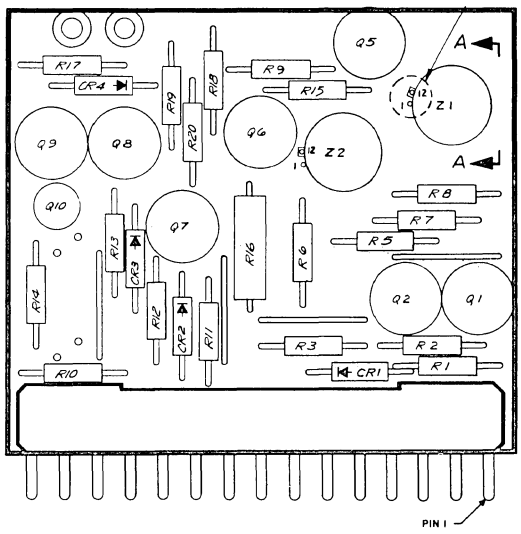
1. CR 2,3,4 DIODE GERMANIUM 92116002
2. Q1,Q2 MATCHED PAIR Q7,Q8 MATCHED PAIR PART NO. 50210602
3. SILICON, NPN TRANSISTOR ARRAY 50251100. NO CONNECTIONS TO PINS 1,2,9,10,11,12, OF Z1 & Z2.




S = SUBSTRATE

4. ALL TRANSISTORS ARE SILICONE EXCEPT Q10
5. COMPONENT ASSY. NO. 50053000 GIA 50053001 GIB
6. VALUES SHOWN IN PARENTHESIS USED ON GIB CARD.

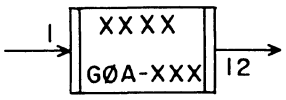
GIA, GIB

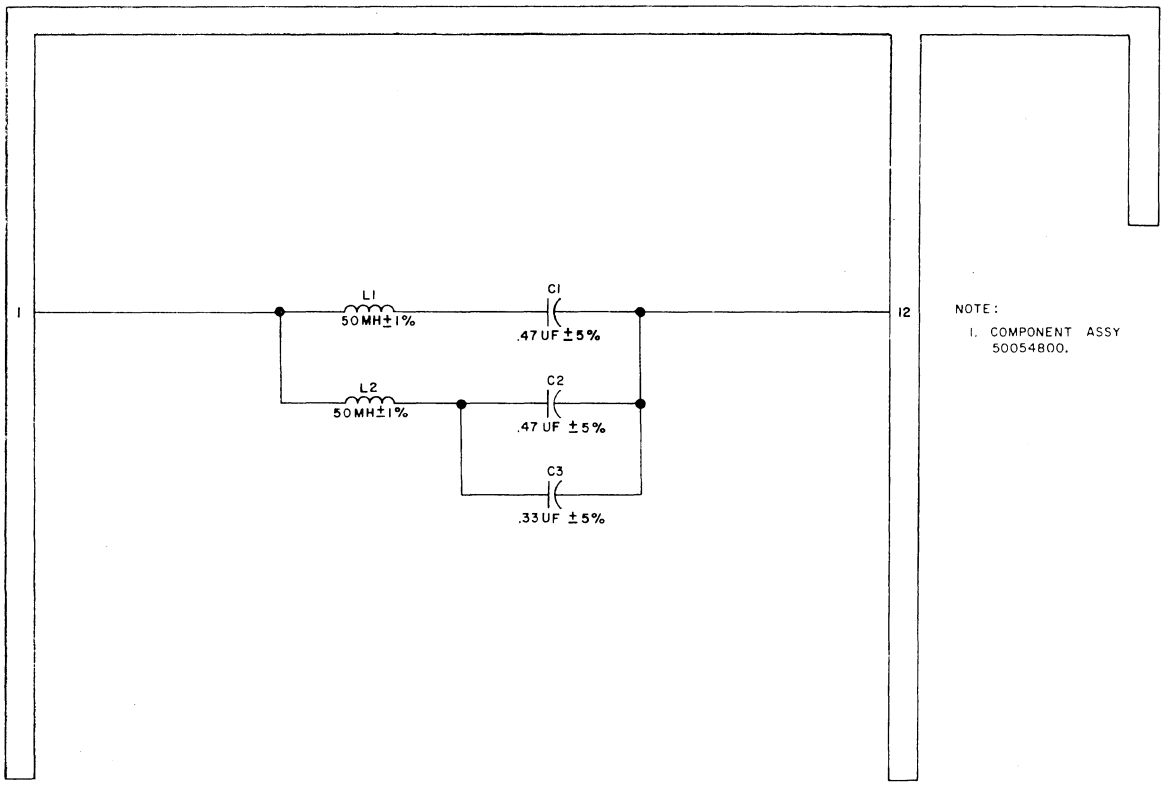


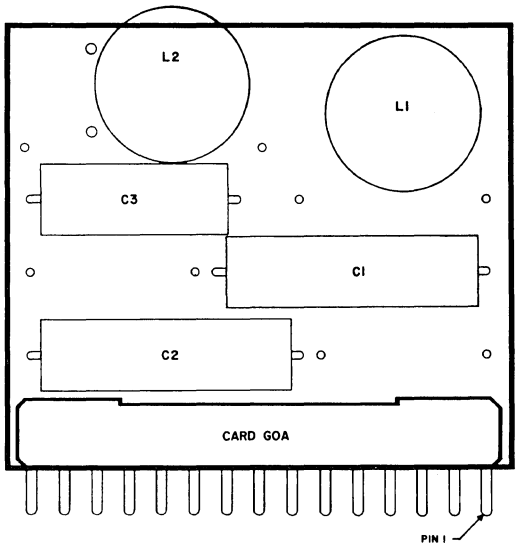
800 & 1050 HZ FILTER
GOA

This filter circuit damps undesirable resonant points in the closed loop of a high performance servo actuator such as in a disk file. The circuits are placed in parallel with each other and with the hydraulic valve, thereby reducing servo gain at the series resonant points of 800 Hz (C2, C3 and L2) and 1050 Hz (C1 and L1). Normally, the output line of a valve operational amplifier such as the FMA drives the filter circuit. The other ends of the filter and the valve are returned to ground through a resistor which provides feedback for a constant current drive source.

At the two resonant points, the filter presents an effective total impedance of approximately 25 ohms. This impedance rises to approximately 42 ohms at the midpoint between the two resonant points.




1
L1
50MH±1%
C1
.47UF ±5%
L2
50MH±1%
C2
.47UF ±5%
C3
.33UF ±5%
12
NOTE:
1. COMPONENT ASSY 50054800.


L2
L1
C3
C1
C2
CARD GOA
PIN 1

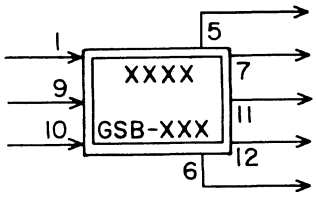
# LEVEL MONITOR
## GSB

This card is used with the GIB (level detector card) to provide both level detection and monitoring of sine wave clock track signals.

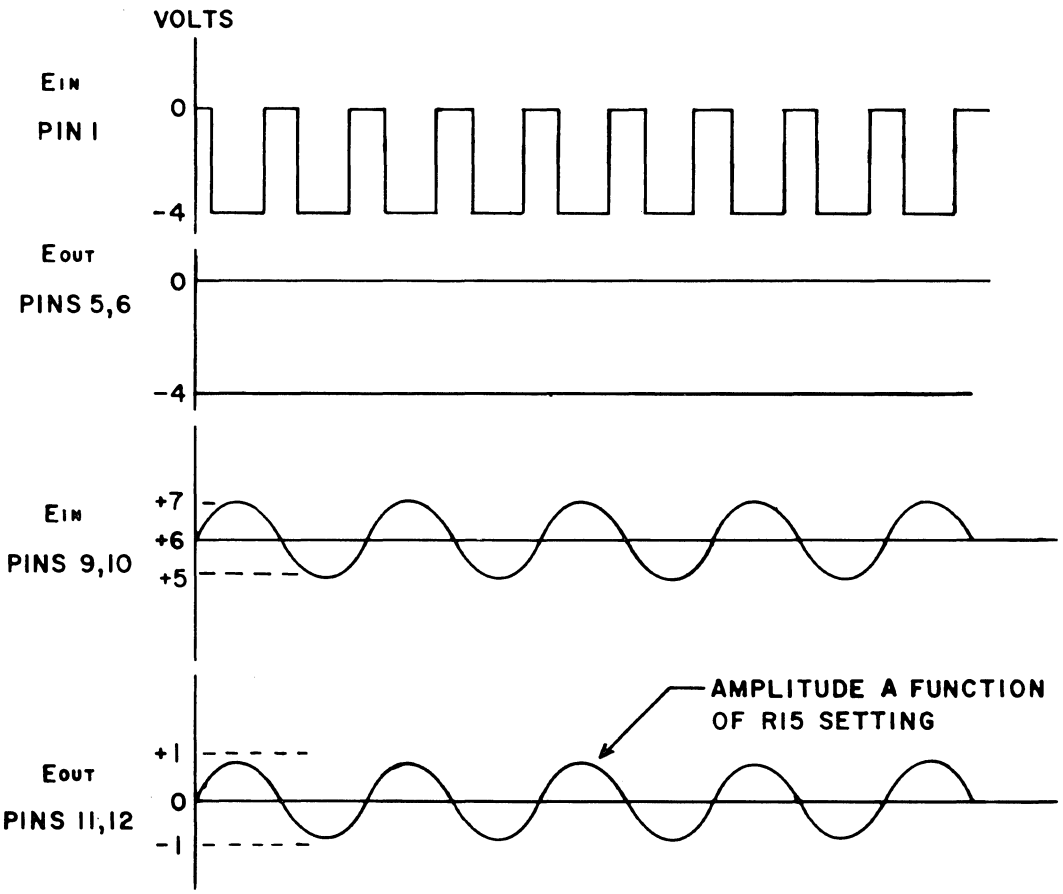
The circuitry of the GSB consists of the following: 1) a potentiometer attenuator circuit followed by a differential emitter follower output; 2) a dc-level adjustable potentiometer circuit; and 3) a pulse integrator-comparator circuit with 1604-type logic level output. Normally, a signal from the EUC (amplifier card) is received by the attenuator circuit, which feeds the GIB. Pulses out of the GIB are returned to the GSB, where they are integrated into an average voltage, holding the output to a "0" or non-fault condition. The dc-level adjustable potentiometer on the GSB determines the reference level at which GIB will produce pulses.

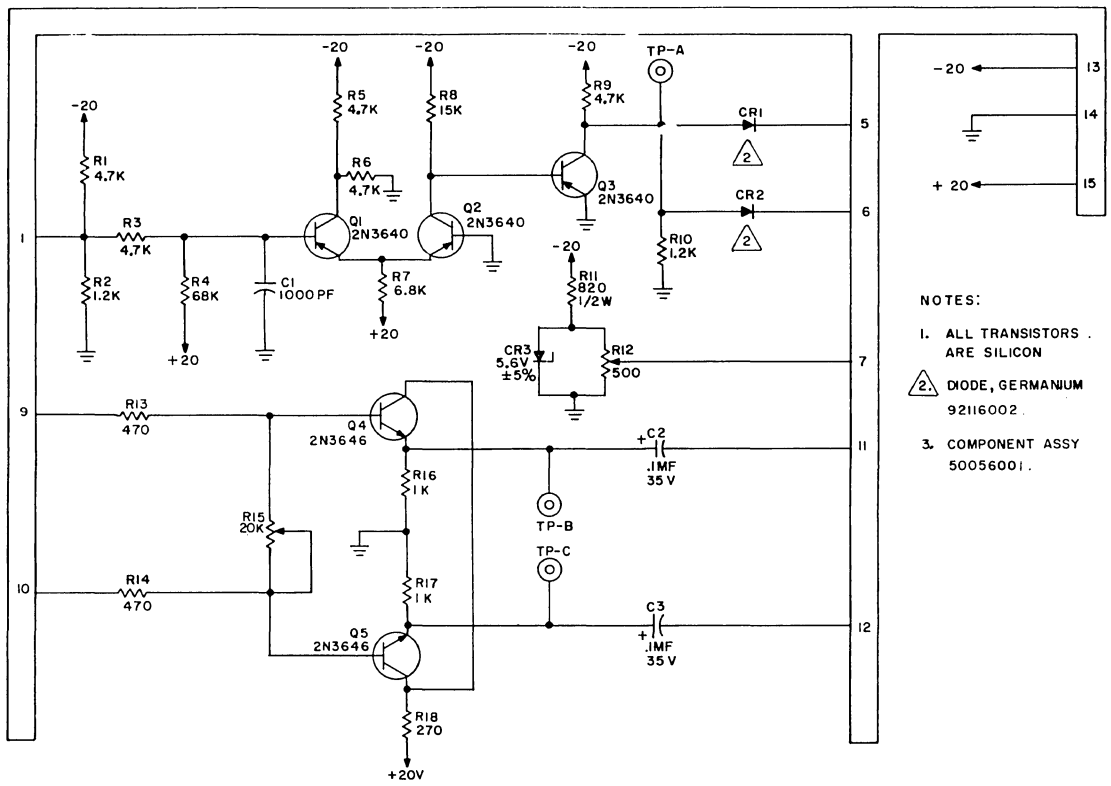
The input on pin 1 comes from the GIB card. Resistors R1 and R2 act as the collector termination for the GIB output pulses (0, -4v). These pulses are integrated into an average dc voltage by R3, R4 and C1. Transistors Q1 and Q2 form a voltage comparator stage. In normal operation, pulses are present on pin 1 and Q1 is turned on. When these input pulses become narrow or non-existent, Q1 turns off, causing Q2 to turn on and Q3 to turn off, and resulting in a "1" (fault) at pins 5 and 6. The maximum time to fault (as determined by R3, R4 and C1) is 5 usec. Resistor R12 permits adjustment of the reference clipping level of the GIB. This adjustment determines the minimum peak to peak voltage into the GIB while still producing pulses at pin 1 of the GSB. The input which is differentially applied at pins 9 and 10 is adjustable by potentiometer R15. Transistors Q4 and Q5 are emitter followers that drive the 680 ohm termination in the GIB.

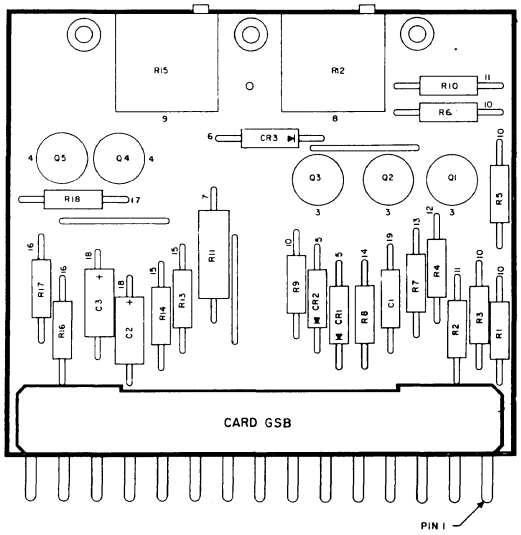
The following procedure is normally used when adjusting potentiometers R12 and R15: 1) measure differential voltage across TP-B and TP-C and adjust R15 to give the peak to peak voltage desired to indicate a fault condition; 2) adjust R12 to the transition point between fault and non-fault; and 3) readjust R15 to minimum attenuation.


1
9
10
XXXX
GSB-XXX
5
7
11
12
6

**WAVEFORMS:**


VOLTS
EIN
PIN 1
0
-4
EOUT
PINS 5,6
0
-4
EIN
PINS 9,10
+7
+6
+5
AMPLITUDE A FUNCTION
OF R15 SETTING
EOUT
PINS 11,12
+1
0
-1


-20
-20
-20
TP-A
R5 4.7K
R8 15K
R9 4.7K
CR1
R1 4.7K
R6 4.7K
Q3 2N3640
CR2
R3 4.7K
Q1 2N3640
Q2 2N3640
R10 1.2K
R2 1.2K
R4 68K
C1 1000 PF
R7 6.8K
R11 820 1/2W
+20
+20
CR3 5.6V ±5%
R12 500
R13 470
Q4 2N3646
+C2 .1MF 35V
R16 1K
TP-B
R15 20K
TP-C
R14 470
R17 1K
C3 .1MF 35V
Q5 2N3646
R18 270
+20V
-20
+20
NOTES:
1. ALL TRANSISTORS ARE SILICON
2. DIODE, GERMANIUM 92116002.
3. COMPONENT ASSY 50056001.


CARD GSB
PIN 1

## COMMENT SHEET

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