CONTROL DATA
CORPORATION

CONTROL DATA® 3276-A
COMMUNICATION TERMINAL CONTROLLER

REFERENCE MANUAL

March 8, 1966

Ed Salter

K. M. Lampert

3276 Manuals

Reference manuals for the 3276 Multiplexor are in short supply; single copies have been mailed to you and to John Henderson. IDP is in the process of revising this publication and is reluctant to print additional copies of the present version.

Users of this manual are sometimes confused by a barrage of equipment numbers which are not related to pricing manual numbers and descriptions. The 3276 is composed of the following units:

1 8165 Master Multiplexor (MUX)
2 8166 Input Slave MUX
2 8167 Output Slave MUX

The 321 Teletype Terminal Unit (TTU) is composed of the following units:

1 85X8 Low Speed Input Unit (LSIU)
1 85X9 Low Speed Output Unit (LSOU)

The input/output units are selected to match the terminal equipment; 8508 LSIU's and 8509 LSOU's are used with five level teletype and 8518 LSIU's and 8519 LSOU's are used with eight level teletypes. Other terminal units are used with higher speed equipment.

K. M. Lampert

/dd
cc: John Henderson
File

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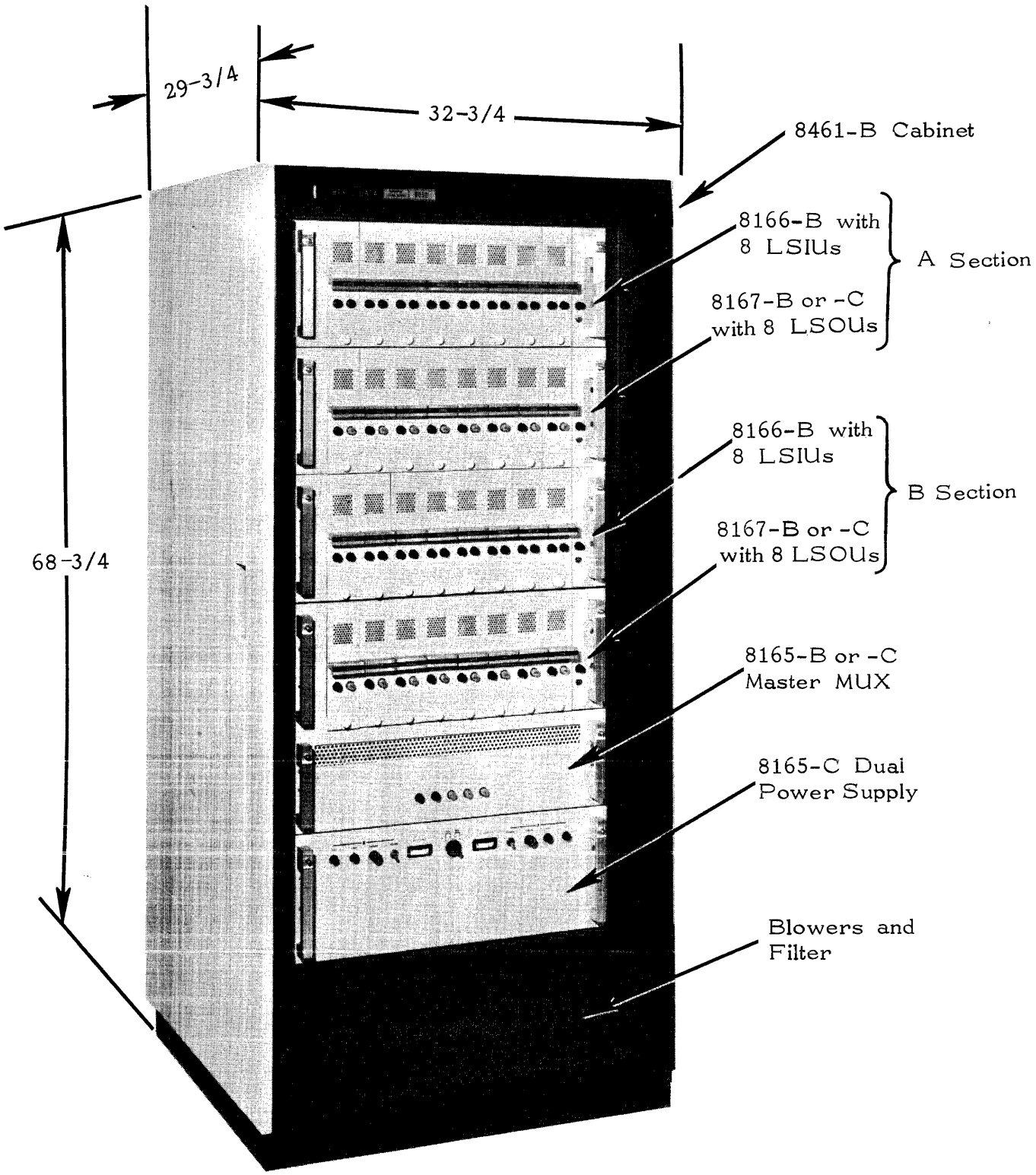


Figure 1. 3276-A Communication Terminal Controller

3276-A COMMUNICATION TERMINAL CONTROLLER

INTRODUCTION

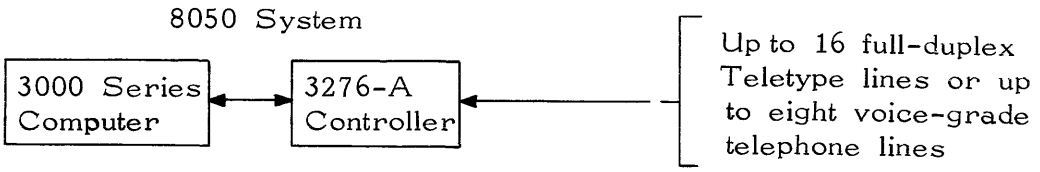
The role of the CONTROL DATA 3276-A Communication Terminal Controller (see figure 1) is that of a channelizing or circuit selector for the processing element of the CONTROL DATA 8050 System. It is a selector switch which connects, one at a time, all of the subscriber (remote, local, message assembly and off-line crypto) circuits terminated to the 8050 System. It interfaces the processor to each Teletype circuit on either a simplex, half-duplex or a full-duplex basis (whichever is required). Speed conversion from computer speeds to Teletype speeds is performed. The required serial-to-parallel conversion is provided by the Controller (serial on the lines, parallel to the processor) and the required parallel-to-serial conversion (parallel from the processor, serial to the lines).

Each Controller can handle up to eight full-duplex DATA-PHONE lines or 16 full-duplex Teletype channels. For more than 16 channels more Controllers can be added to the system. More than one Teletype unit at different remote and/or local stations can be placed on each channel; thus, the system is flexible and expandable.

CONTROLLER DESCRIPTION

The Controller is a solid-state electronic device which regulates data transmission between a Control Data computation module and several communication channels. The Controller's position between the computation module and the communication channels is illustrated below.

The Controller is highly flexible and can handle up to 16 full-duplex Teletype lines or up to eight full-duplex, high-speed, voice-grade lines.



PERFORMANCE

The 3276-A Communication Terminal Controller:

1. Interrupts the computer periodically to ask the computer to enter a Read/Write subroutine with the multiplexer (MUX).

2. Decodes the connect codes sent by the computer to the individual input/output (I/O) units. For the Read Connect code the MUX scans the low-speed input units (LSIUs).

3. Converts the input serial characters (one bit at a time) to parallel characters (up to eight bits at a time) for the computer to read.

4. Serializes the parallel characters sent by the computer and transmits them, one bit at a time, to the external communication channels.

5. Connects the computer to external channels of various speeds.

6. Sends status response codes such as Character Ready, Character Request, Character Lost, Idle, or Break to the computer.

7. Distributes Read/Write data between the computer and the external communication lines.

PHYSICAL COMPOSITION

The 3276 Controller is modular in construction. The Master MUX, Slave MUXs, I/O units and power supply are drawer-type modules. The composition of the Controller is variable, due to the flexible arrangement of the modules (see figure 2).

INDIVIDUAL CONTROLLER UNITS

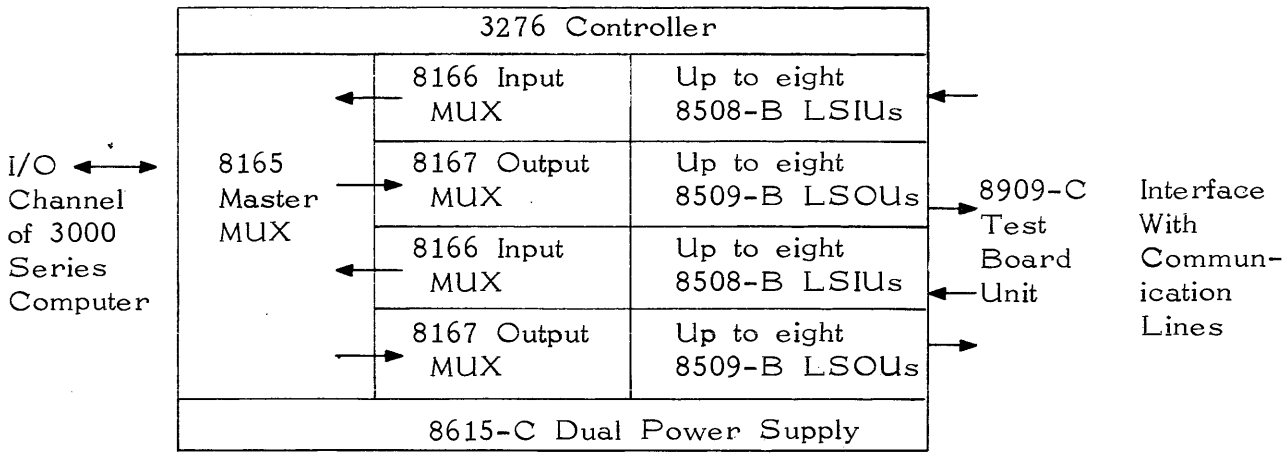
Table 1 lists the units which are modular parts of the Controller.

8165-C MASTER MUX WITH READ SCANNER

The 8165-C Master MUX matches the interface of the computer, two slave input MUXs and two slave output MUXs. It generates and sends the channel Interrupt signal to the computer. The 8165-C decodes the connect code to select the A or B section slave MUX as well as each I/O unit. It also regulates the connect code and Read and Write Data signals all of which use the same lines. It sends a Reply signal to the computer when data or code is on the channel. It passes status response codes to the computer.

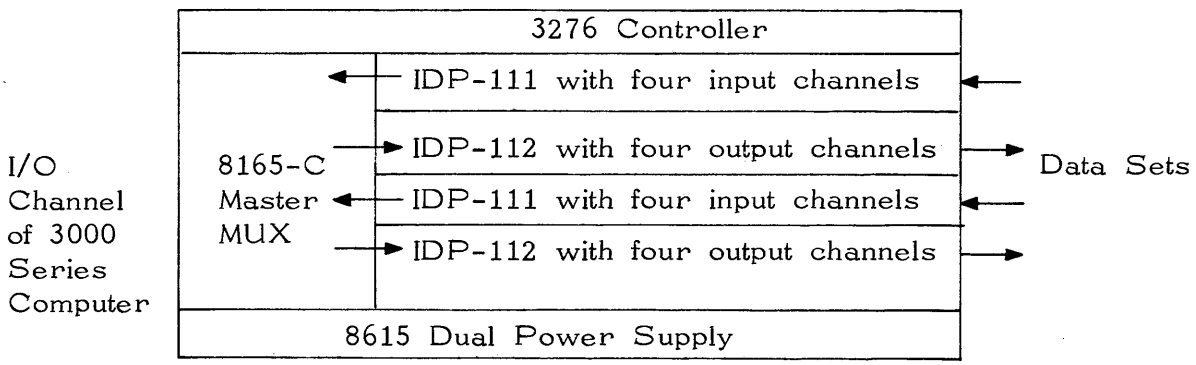
When the MUX is connected and a Read signal is present, the MUX automatically scans all 16 LSIUs for information. When a Write signal is present, the LSOUs are selected individually under computer control.

For Communication between Computer and Teletype Lines (five-level)



NOTE: For eight-level lines substitute these model numbers for the LSOUs and LSIUs; 8518 and 8519 . Future high-speed I/O units will fit into the 8166 and 8167 slaves MUXs.

For Communication between Computer and Voice-Grade Lines



NOTE: Other high-speed units can be substituted.

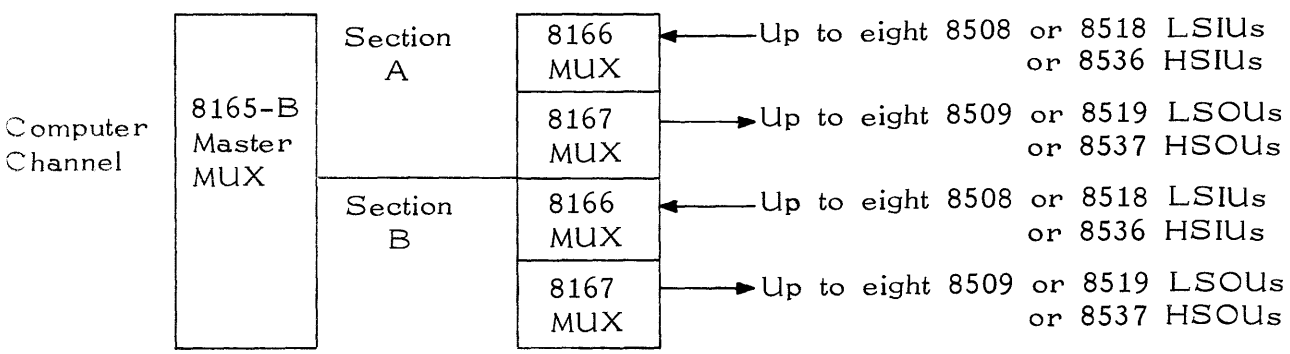
Figure 2. Composition of 3276-A Controller (typical examples)

TABLE 1. 3276-A CONTROLLER COMPONENTS

Cabinet	8461-B Cabinet (including blower and wiring)
MUX Drawers	8165-B Master MUX (without read scanner) 8165-C Master MUX (with read scanner) 8166-B Input Slave MUX 8167-B Output Slave MUX 8167-C Output Slave MUX with start-motor delay
Low-Speed Teletype Terminals used in Slave MUXs	8508-B LSIU (five bits) 8509-B LSOU (five bits) 8518 LSIU (up to eight bits) 8519 LSOU (up to eight bits)
High-Speed Input/Output Units used in Slave MUXs	8536 HSIU (up to eight bits) 8537 HSOU (up to eight bits)
High-Speed Communication Adapters (Drawers)	IDP-111 Data Set Adapter (receive) IDP-112 Data Set Adapter (send) IDP-113 Data Set Adapter (receive) IDP-114 Data Set Adapter (send)
Other Drawer Modules	8615-C Dual Power Supply (separate manual) 8908-E LSI/O Unit Tester 8909-E Test Board Unit

8165-B MASTER MUX

The 8165-B Master MUX is similar to the 8165-C except that it does not initiate scanning of the input units. Scanning is accomplished by the computer or a separate scanning device. The MUX arrangement in the Controller is as follows:



8166-B INPUT SLAVE MULTIPLEXER (INPUT MUX)

The 8166-B Input MUX matches the interface of the 8165 (-B or -C) Master MUX and also of the 8508-B or 8518 LSIU. The 8166-B is basically a fan-in unit which receives the decoded connect code from the 8165 Master MUX and selects the proper LSIU. It receives data from the connected LSIU and sends it to the computer via the 8165 Master MUX. There is space for two 8166-Bs in each Controller cabinet; one in section A, and one in section B. Each 8166-B can hold up to eight LSIUs.

8167-B OUTPUT SLAVE MULTIPLEXER (OUTPUT MUX)

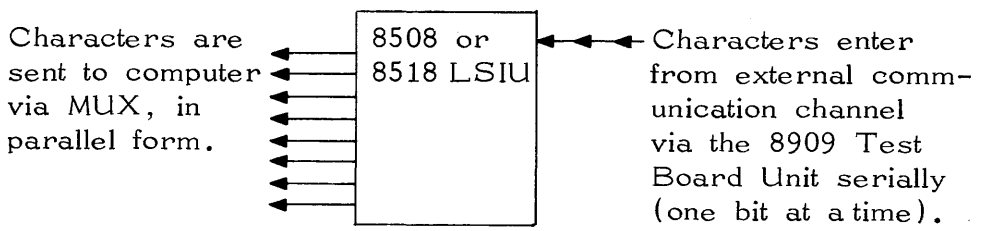
The 8167-B Output MUX matches the interface of the 8165 (-B or -C) Master MUX and also of the 8509-B or 8519 LSOU. It receives the decoded connect code from the 8165 Master MUX and selects the proper LSOU. The 8167 enables data to enter the connected LSOU. There is space for two 8167s in each 3276-A MUX cabinet; one in section A, and one in section B.

8167-C OUTPUT SLAVE MULTIPLEXER (OUTPUT MUX)

The 8167-C Output MUX is similar to the 8167-B except that it contains a 4-second motor-start delay circuit for each channel. This circuit allows remote teletypewriter motors to reach operating speed before receiving transmission.

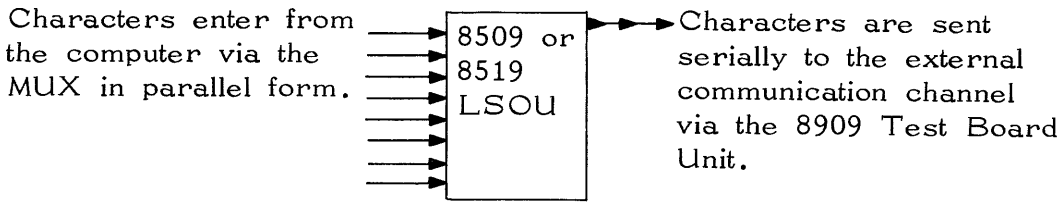
8508-B AND 8518 LSIU(S)

The 8508-B five-bit LSIU converts the incoming serial Teletype characters to parallel form for the computer to read (see the example following this paragraph). The 8518 LSIU differs from the 8508-B in that it can be adjusted to handle up to eight-bit characters.



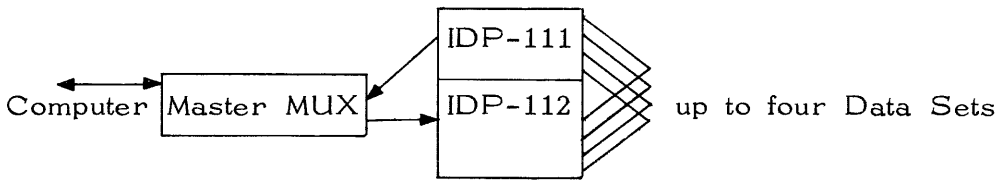
8509-B AND 8519 LSOU(S)

The 8509-B five-bit LSOU serializes the characters which come from the computer in parallel form. The 8519 LSOU can assemble up to eight-bit characters. The LSOUs function as shown in the following example:



IDP-111 DATA SET ADAPTER

The IDP-111 Data Set Adapter is a high-speed input multiplexing unit which matches the interface of the computer (via the Master MUX) with that of up to four 202-C1 Data Sets as shown in the example.

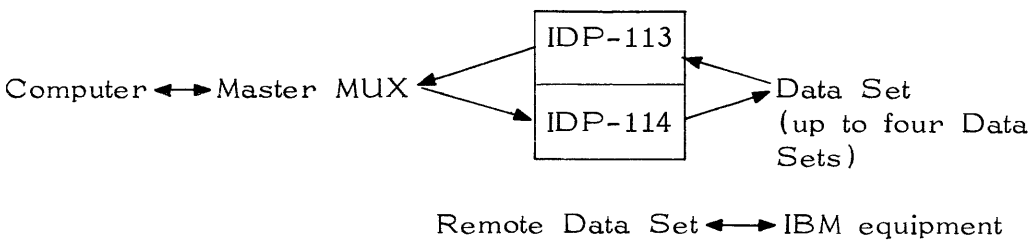


IDP-112 DATA SET ADAPTER

The IDP-112 Data Set Adapter is a high-speed output multiplexing unit which matches the interface of the computer (via the Master MUX) with that of up to four data sets for communication on voice-grade lines.

IDP-113 DATA SET ADAPTER

The IDP-113 Data Set Adapter is a high-speed input multiplexing unit which matches the interface of the computer (via the Master MUX) with that of up to four data sets. Its main purpose is to facilitate communication between an 8050 System and certain IBM devices. The IDP-113 converts characters from serial to parallel form as shown in the example.



IDP-114 DATA SET ADAPTER

The IDP-114 Data Set Adapter is a high-speed output multiplexing unit which matches four data sets to the computer interface. The IDP-114 facilitates communication to IBM devices from the 8050 System. It converts characters from parallel to serial form.

8536-A HIGH-SPEED INPUT UNIT

The 8536-A High-Speed Input Unit (HSIU) is similar to the 8518 LSIU except that it is adaptable to higher communication speeds (up to 1200 words per minute). The 8536-A HSIU receives data serially, assembles each character, and sends it in parallel form to one of eight channels in an 8166 IMUX.

8537-A HIGH-SPEED OUTPUT UNIT

The 8537-A High-Speed Output Unit (HSOU) is similar to the 8519 LSOU except that it is adaptable to higher communication speeds (up to 1200 words per minute). The 8537-A HSOU receives parallel-bit characters from the MUX, and sends the bits serially to the data set.

I/O CABLES

The computation module of the computer communicates with the 3276 Controller through a standard 12-bit channel interface on two bidirectional cables. Each cable contains 29 transmission lines. Each transmission line consists of two twisted pairs of 24-gauge conductors.

Data I/O Cable

The data I/O cable (see table 2) uses its 12 data lines to carry the 12-bit connect code as well as data (both Read and Write). This cable also carries signals such as Connect, Data, Read, Write and Reply.

Status I/O Cable

The status I/O cable (see table 3) uses three status response lines and one interrupt line. Figure 3 describes each signal sent between the computer and the MUX. Table 4 shows graphically the sequence of signals between the computer and the MUX.

THREE-DIGIT MODEL NUMBERS

The three-digit numbers listed in the table below represent combinations and choices of input/output units that fit into the slave-MUX drawers of the 3276 Communication Terminal Controller.

At the time of this printing only the 321 and 323 Units are available. The other units will be covered in supplements to this manual whenever the units become available.

3-DIGIT NUMBER	MODEL CONFIGURATION	COMPATIBLE DATA SET
311	8546 + 8547 High-Speed I/O Units*	201
312	311 + Automatic Dialer	201 + 801
313	8536 + 8537 High-Speed I/O Units** + 8538 + 8539 Data Set Control Units	103
314	313 + Automatic Dialer	103 + 801
315	High-Speed Data (750 wpm) Output Unit	402C
316	High-Speed Data (750 wpm) Input Unit	402D
317	8536 + 8537 High-Speed I/O Units** + 8538 + 8539 Data Set Control Units	202
318	317 + Automatic Dialer	202 + 801

TELETYPE WRITER LINE TERMINAL	
321	8508 + 8509 or 8518 + 8519 LSI/Os
323	8508 or 8509 or 8518 or 8519 LSI/Os

TELEX LINE TERMINALS	
324	8548 + 8549 or 8558 + 8559***
325	8548 or 8549 or 8558 or 8559

---

* 8546 (+ 8166 MUX is similar in operation to interim model IDP 113

* 8547 (+ 8167 OMUX) is similar in operation to interim model IDP 114

** 8536 (+ 8538 + 8166) is similar in operation to interim model IDP 111

** 8537 (+ 8539 + 8167) is similar in operation to interim model IDP 112

*** 8548 is similar in operation to an 8508 + Telex sensor

*** 8549 is similar in operation to an 8509 + Telex sensor

*** 8558 is similar in operation to an 8518 + Telex sensor

*** 8559 is similar in operation to an 8519 + Telex sensor

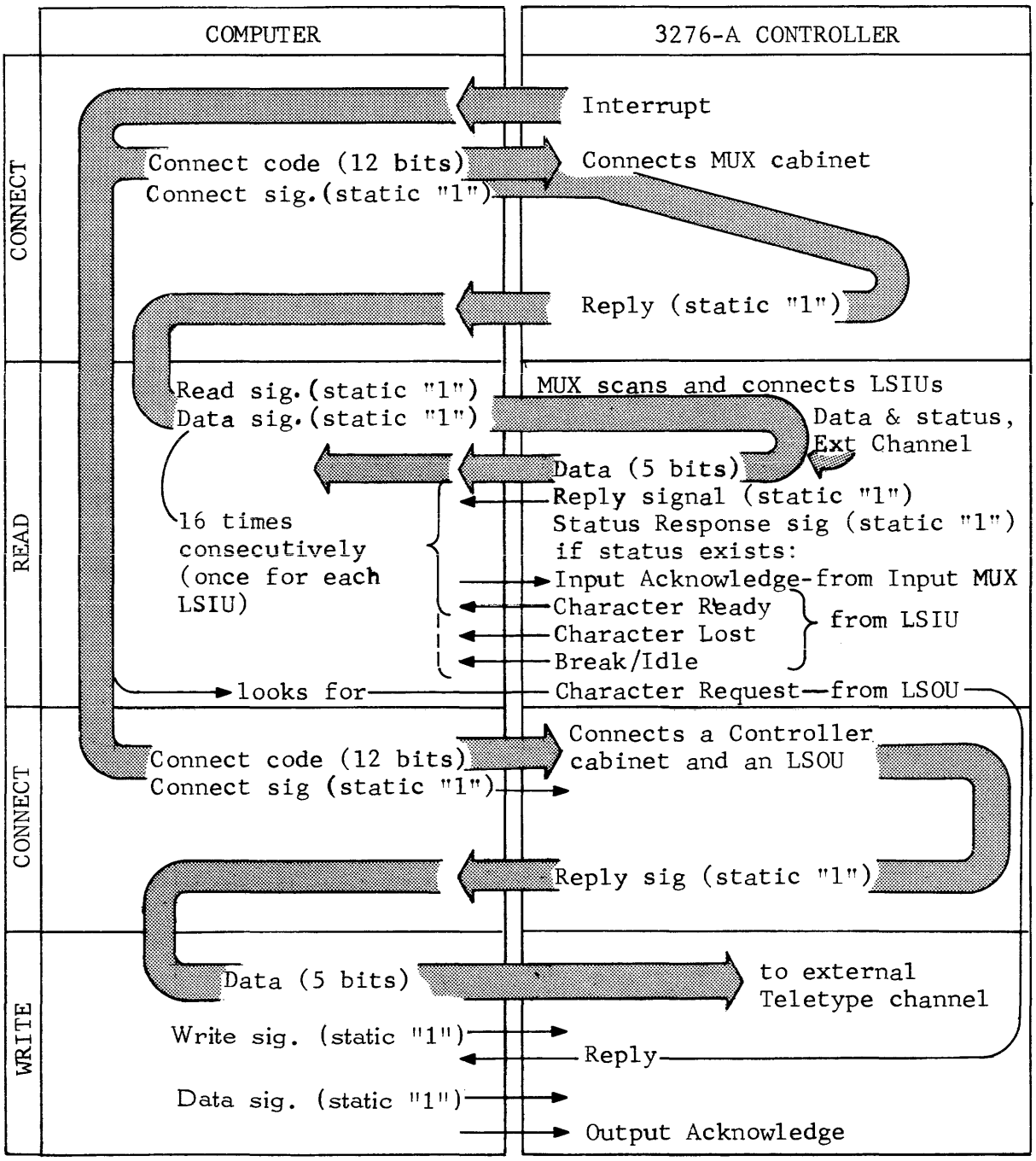


Figure 3. I/O Signal Sequence - Computer Interface

TABLE 2. INTERFACE WITH 3000 SERIES COMPUTER

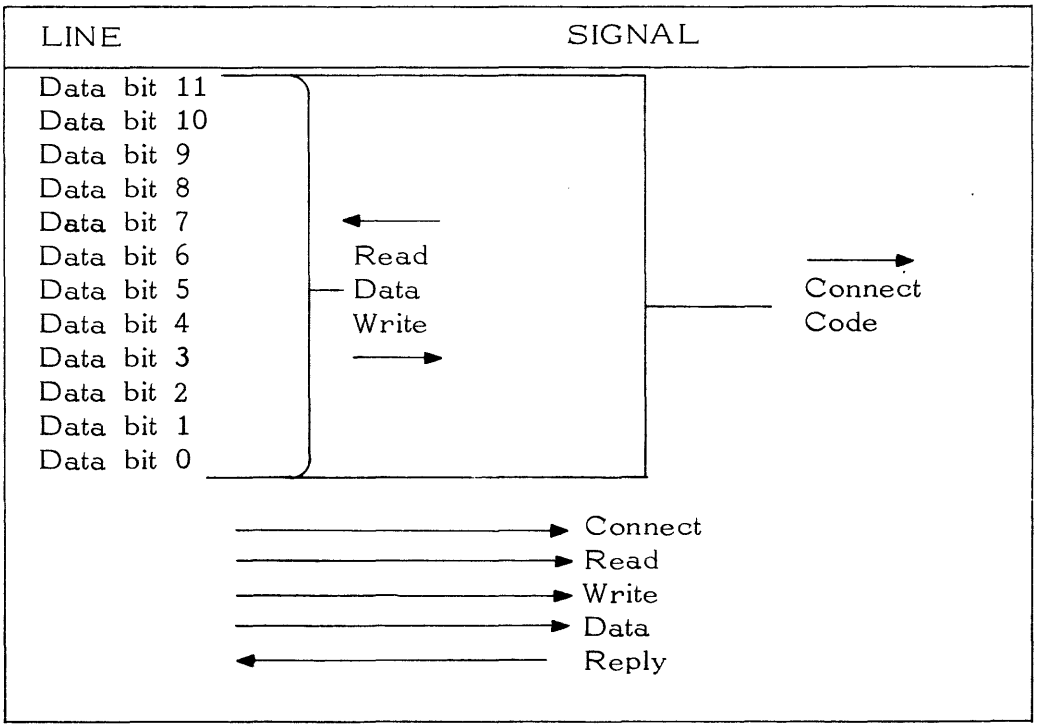


TABLE 3. COMPUTATION MODULE OF 3000 SERIES COMPUTER CONTROL I/O CABLE

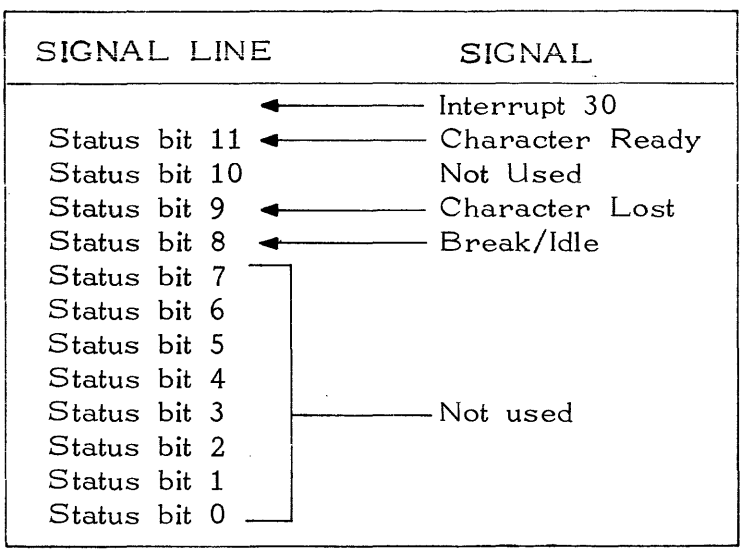


TABLE 4. I/O INTERFACE SIGNALS BETWEEN COMPUTER AND MUX

Bidirectional Signals	
Data Lines	The 12 lines which carry data are bidirectional, and perform as follows: 1. In a Read (input) operation, data is transmitted from MUX to the computer. 2. In a Write (output) operation, data is transmitted from the computer to the MUX. 3. The connect code is transmitted from the computer to the MUX via the 12 data lines.
Computer to MUX Signals	
Connect	Status "1" signal sent to the MUX when 12-bit connect code is available on data lines. Signal drops when MUX returns Reply.
Read	Static "1" signal produced by computer during a Read operation.
Write	Static "1" signal produced by computer during a Write operation.
Data Signal	Static "1" signal sent to external equipment during both Read and Write operations. Signal drops conditionally when Reply is received from the MUX. 1. In a Read operation, Data signal indicates that the computer is read to accept a 12-bit word from the MUX. Only a maximum of eight of the 12 lines are used for data bits. 2. In a Write operation, Data signal indicates the computer has placed a 12-bit word on the data lines.
MUX to Computer Signals	
Interrupt	A "1" signal which periodically asks the computer to go into an I/O subroutine with the MUX. The period is adjustable (by logic-card substitution) to either high- or low-speed transmission.

TABLE 4. I/O INTERFACE SIGNALS BETWEEN COMPUTER AND MUX (CONT)

Reply	Static "1" signal produced by the MUX in response to a Connect or Data signal. Signal drops when Connect or Data signal drops. 1. If connection can be made when Connect Signal is received, an LSI/O unit connects and returns a Reply. 2. In a Read operation the MUX sends a Reply as soon as it has placed a 12-bit word on data lines in response to the Data signal. Note that a data character uses only the eight lowest bits. 3. In a Write operation, the MUX sends a Reply as soon as it samples the data lines in response to the Data signal.
Status Bits	Static "1" signal is produced by a connected LSIU and sent to the computer only if one of the five following conditions exists: 1. Character Ready 2. Character Lost 3. Break 4. Idle 5. Character Request is produced by an LSOU but is sensed by the computer along with LSIU Status Response signals.

CONTROL DATA
CORPORATION

CONTROL DATA 8165
MASTER MULTIPLEXER

Pub. No. 368 161 00 (02)

8165 MASTER MULTIPLEXER

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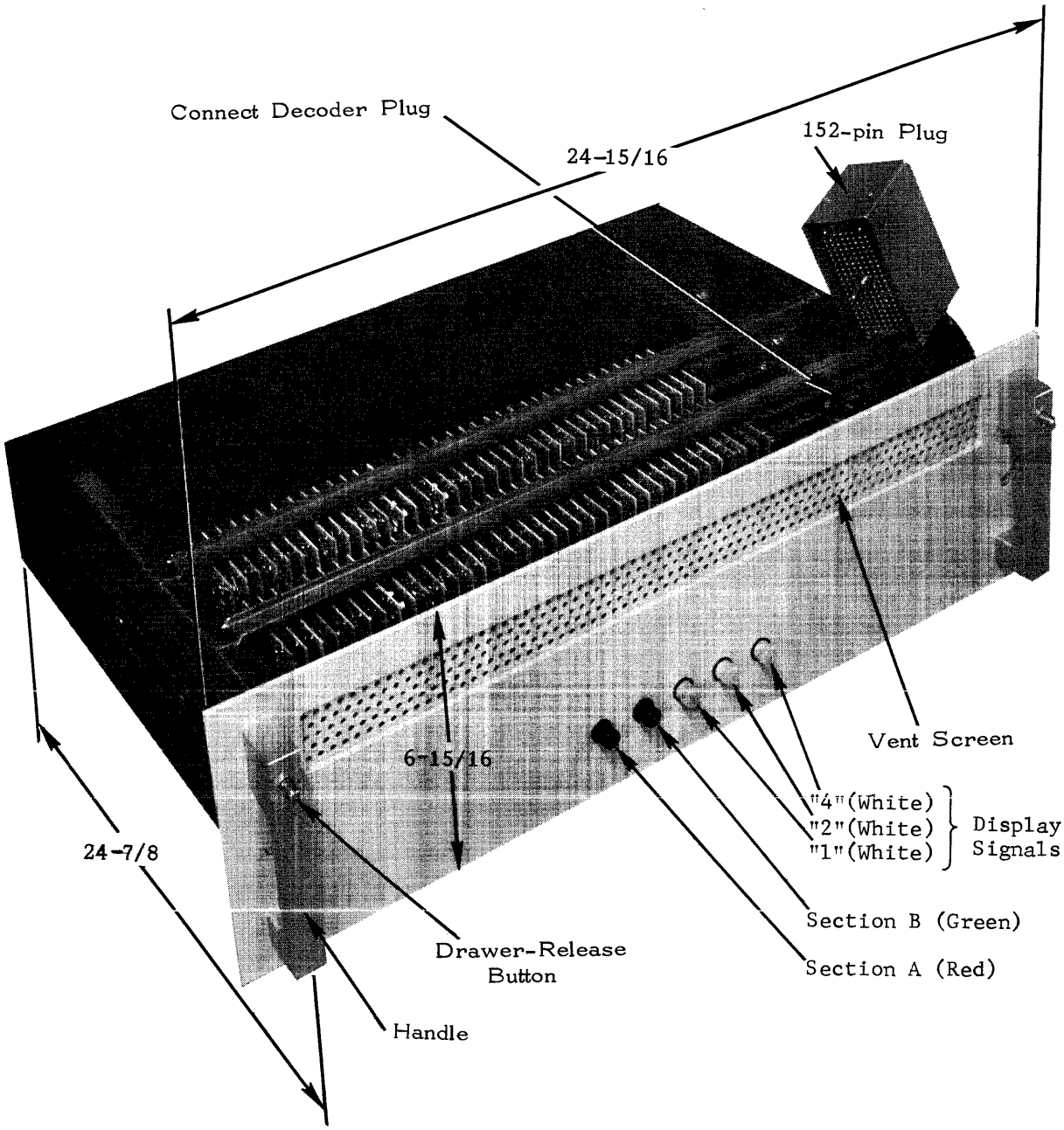

Figure 1. 8165 Master Multiplexer

8165 MASTER MULTIPLEXER

DESCRIPTION

The CONTROL DATA 8165 Master Multiplexer (Master MUX), figure 1, is a high-speed data switch that distributes messages between a computer in a CONTROL DATA 8050 System and two pairs of input/output slave MUXs. It interrupts a computer channel periodically for input/output (I/O) operations. It decodes connect codes for the 32 I/O units in the cabinet. Physically the 8165 Master MUX is a drawer (containing logic cards, controls and wiring) that fits into the 3276-A Communication Terminal Controller cabinet assembly. The 8165-A interfaces the CONTROL DATA 160-A or 8090 Computer. The 8165-B and 8165-C models interface the 3000 series Computers.

This manual covers both the 8165-B and 8165-C Master MUXs which are alike except for read scanning. The 8165-B does not have a read scanner. Therefore, the computer or an external scanner sends connect codes to all the input units in sequence. The 8165-B Master MUX decodes the connect code for each unit.

The 8165-C has a read scanner. The computer sends only one connect code per cabinet. The 8165-C Master MUX in any controller cabinet decodes the connect code and scans all the input units.

OPERATION

The 8165 Master MUX performs the following operations:

1. Initiates the channel Interrupt signal which periodically asks the computer to enter an I/O routine with the MUX.
2. Decodes its own connect code.
3. Scans all input units (8165-C).
4. Decodes connect codes to input units (8165-B).
5. Sends any data which is available from a low-speed input unit (LSIU) to the computer.
6. Decodes connect codes to output units.
7. Replies to Connect, Read or Write signal from the computer.
8. Sends the computer the status code indicating Character Ready, Character Lost, Break or Idle received from the LSIUs.

PANEL

The 8165 Master MUX panel serves as a display board for the A and B sections and LSI/O unit connect decoders.

LAMPS

There are five indicator lamps in a horizontal row on the panel. They display the decoder connect code. The left two lamps indicate which section (A or B) is communicating with the computer. The first lamp (red) designates the A section. The second lamp (green) indicates the B section. The right three lamps (white) indicate in octal code which of eight pairs of LSI/O units in the module is selected. The lamps are lighted by the connect code from the computer. They go off when the connect code and Connect signal stop.

WRITE LOGIC

CHANNEL INTERRUPT

The MUX operates on a computer-interrupt basis (see diagrams 364561500 and 36461600 in pub. no. 368 165 00). The interrupt clock in the Master MUX is a free-running multivibrator. It sets the interval between interrupts at slightly less than the mimimum character interval. For example, with a Teletype (TTY) rate of 100 words per minute where the character interval is 100 ms, the interrupt clock is set to cycle once every 90 ms. Once each cycle, the clock sets the Interrupt flip-flop (FF), which notifies the computer that an Interrupt is generated. The computer enters the interrupt routine.

CONNECT SIGNAL

The computer sends out a Connect signal along with a connect code. The Connect signal is used throughout the 8165 circuit to enable and/or disable decoding. The programmed connect code selects the assigned output section (A or B) and output unit (one of eight).

READ LOGIC

The 8165 read logic has a threefold purpose; it is a channel for parallel-bit transmission of each input character from an 8508-B Low-Speed Input Unit to the computer. When alarm status signals, such as Character Lost or Break/Idle, are generated in an input unit they pass through the Master MUX to the computer.

CHARACTER READY

When an input unit sends a Character Ready bit through the 8165 to the computer, the computer returns a Read signal via the 8165 to the read unit.

The Read signal enables the Reply signal to return to the computer if data is ready. This allows a character to leave an LSIU and enter the computer. In the 8165-C, the Read signal starts the counter which scans all input units for any available Read data.

3000 SERIES COMPUTER INTERFACE

The I/O section of the computer provides the methods for data exchange and for control of information transmission between the computer and the various external equipments. All information from the externally located peripheral equipments must enter or leave the computer through these cables.

Information passes between the computer and the external equipment as a block of information at a word-by-word rate or as a single word input or output. The speed of the particular equipment in communication with the computer determines the data exchange rate.

INTERRUPT

Description

An Interrupt signal jumps the computer main program and initiates an interrupt subroutine. At the completion of the interrupt subroutine the main program can be resumed. Each Interrupt signal transfers computer control to a distinct location in memory (refer to Execution paragraph).

To use the interrupt feature, every connect command must be followed by a Clear Interrupt Lockout (CIL) command, but not until the completion of any I/O sequence related to that connect command.

The interrupt clock in the 8165 Master MUX is set at a cycle time just under the character rate. The clock is adjustable from low Teletype speed (60 to 100 words per minute) to high telephone speed (1050 words per minute) by replacing the type CC82-5 card in location B20 with a type CC82-4 card, and readjusting the delay in location B21 to the desired time.

Recognition

Interrupt FFs are activated by an internal 8165 Master MUX clock. The routine must branch to an interrupt subroutine. The Interrupt signal is removed from the line by the external equipment.

Execution

During the execution portion of the interrupt, the computer stores the contents of P at location 00004, and then takes its next instruction from 00005 to enter the subroutine.

The Master MUX is connected to the computer's data and control I/O cables. Cables with 152-pin plugs are used to connect the slave MUX and the Master MUX to common cabinet wiring and receptacles.

The MUX word is 12 bits long of which up to eight bits are communications data (see figure 2).

CONNECT CODE

The connect codes 00XX, 01XX and 02XX are reserved for addressing as high as a 12-cabinet MUX system. Each octal digit represents three bits. MUX systems can be addressed in groups of four 8165 Master MUXs.

In the read mode the computer connects an 8165-C Master MUX which in turn scans eight LSIUs in each section (A and B), and each LSOU for Character Request. In the write mode the computer connects each LSOU for which there is data.

The first and second digits of the code (00, 01 or 02) direct the computer communication to one of the three groups of 8155 cabinets (four cabinets maximum to a group).

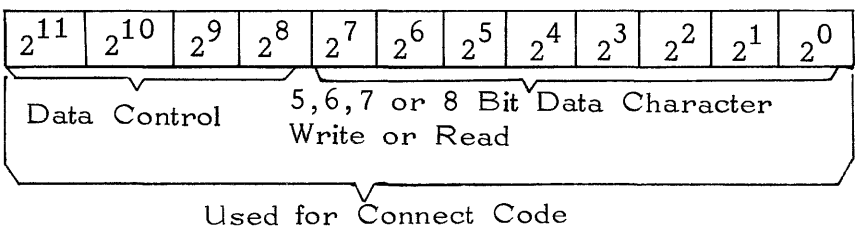

Figure 2. MUX Word

The third octal digit chooses not only a cabinet but also a section (A or B) within the cabinet (see figure 3). The first two bits select a cabinet (the binary count limit of two bits is four). The third bit selects the A or B section.

The fourth octal digit of this code selects one of eight pairs (one input and one output) of LSI/O units by octal numbers 0 through 7.

To show the exact selection, divide the octal code into its binary equivalent as shown in table 1.

Example: The computer has a character ready to send to a teletypewriter way station which is connected to LSOU no. 5 in section B in the second cabinet. What is the connect code to address this LSOU?

Solution: The first and second octal digits (01) are give. The bits of the third octal digit (01XX) are "01" for the second cabinet and "1" for section B. The fourth octal digit is composed of bits 101 representing unit no. 5, thus:

Binary	000 001 011 101
Octal	0135 = connect code

The decoder plug is a 24-pin twist-lock cylinder which is wired to decode the first three octal digits of the connect code. It plugs into the panel of each 8165 Master MUX, and is wired to select the correct cabinet and section, for example 010X.
011X

The 8165 decodes the third digit as to odd or even (0 or 1). The fourth digit is decoded in the internal logic of the MUX to select one of eight of LSOUs units in a section.

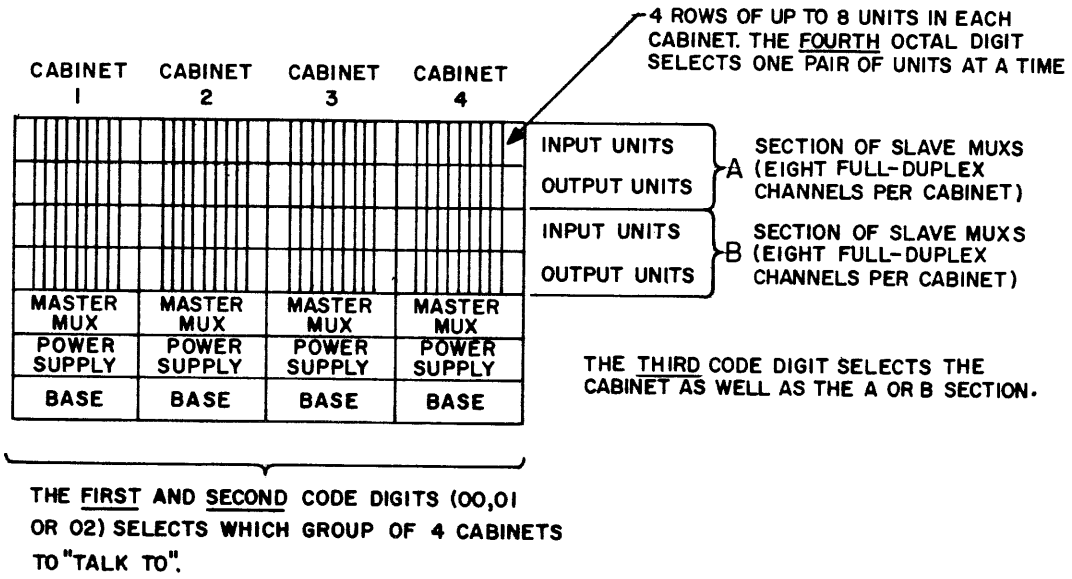

Figure 3. Connect Code Configuration

TABLE 1. CONNECT CODE DECIPHERING

Octal	0	0, 1, or 2	X	X	
	$(2^{11}\ 2^{10}\ 2^{9})$	$(2^{8}\ 2^{7}\ 2^{6})$	$(2^{5}2^{4}2^{3})$	$(2^{2}2^{1}2^{0})$	LSI/O unit no.
Binary	000	001,000,010		0 0 0	0
	MUX system	Groups of 4 cabinets			
			Section	0 0 1	1
		Cabinet 1: 0 0 0	A	0 1 0	2
		0 0 1	B		
		Cabinet 2: 0 1 0	A	0 1 1	3
		0 1 1	B	1 0 0	4
		Cabinet 3: 1 0 0	A	1 0 1	5
		1 0 1	B	1 1 0	6
		Cabinet 4: 1 1 0	A	1 1 1	7
		1 1 1	B		

CONTROL DATA
CORPORATION

CONTROL DATA 8166-B
INPUT SLAVE MULTIPLEXER

Pub. No. 368 161 00 (03)

8166-B INPUT SLAVE MULTIPLEXER

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Introduction	1 (8166-B)
Description	1 (8166-B)
Logic Cards	1 (8166-B)
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Character Lost	2 (8166-B)
Break	2 (8166-B)
Idle	2 (8166-B)
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LSIU Interface	3 (8166-B)
Fan In	3 (8166-B)

FIGURES

1	8166-B Input Slave Multiplexer	ii (8166-B)

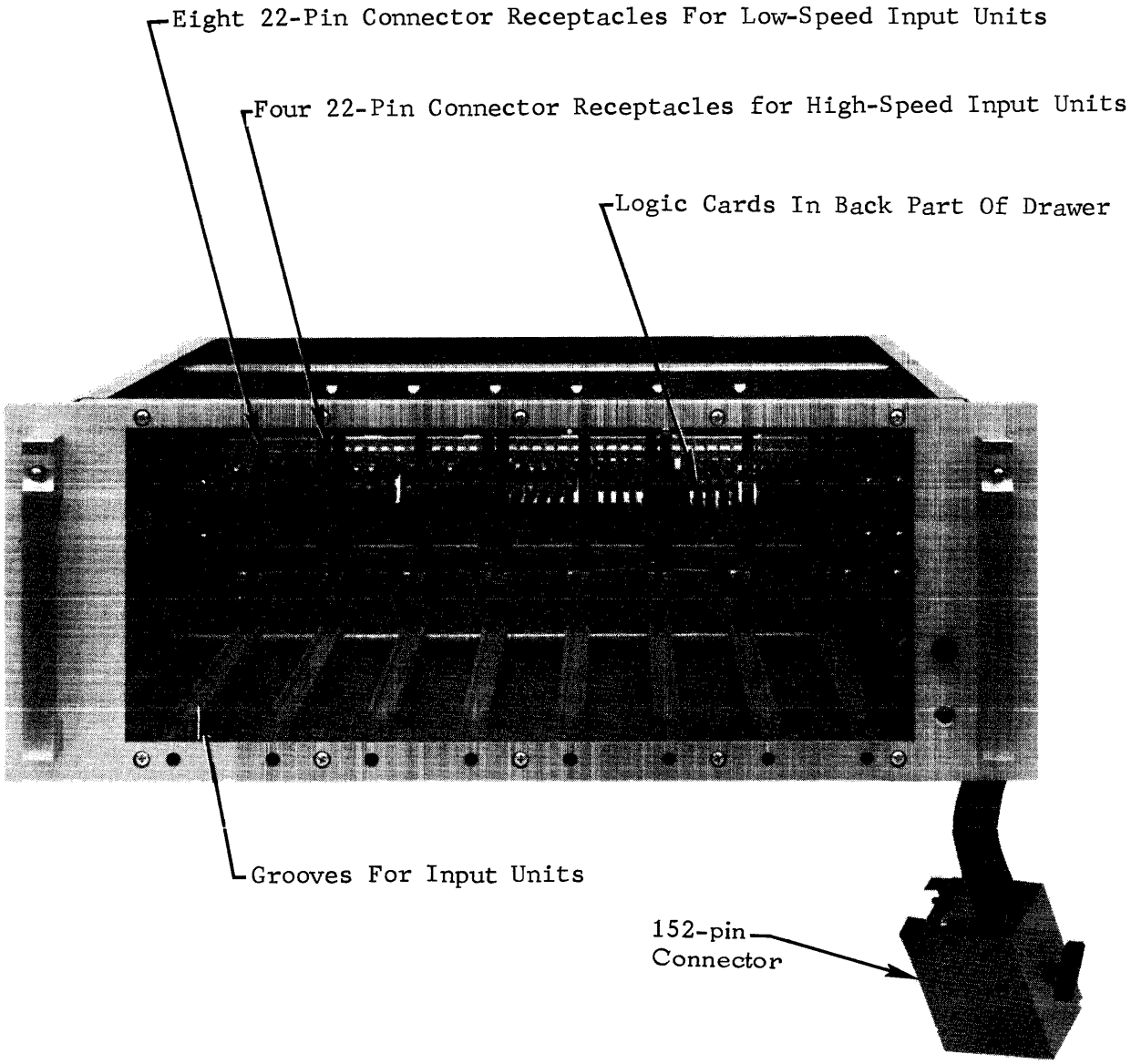

Figure 1. 8166-B Input Slave Multiplexer

8166-B INPUT SLAVE MULTIPLEXER

INTRODUCTION

The CONTROL DATA 8166-B Input Slave Multiplexer (Input MUX), figure 1, is a data handling device which collects data from each of its eight connected low-speed input units (LSIUs) and fans in the data to the computer by way of the Master MUX.

DESCRIPTION

The 8166-B is a drawer-type module which fits into the 3276-A cabinet. It slides out on telescoping channels, and locks in either the extended or closed position. Before the drawer can be opened, the 152-pin plug must be disconnected, and the release buttons on the two pull handles must be pressed. The plug is disconnected simply by unscrewing the wing screw until it is free, and pulling the plug out.

LOGIC CARDS

The back part of the modules contains two rows, of logic cards, the eight 22-conductor receptacles for the LSIUs, and four receptacles for high-speed input units.

LSIU(S)

Eight 8508-B or 8518 LSIUs slide into channels in the front of the 8166-B like books on a shelf. When the LSIUs are pushed all the way in, they mate with the matching receptacles. An LSIU is locked in with a plastic button which snaps in.

STATUS CODES

The following four status bits enter the 8166-B from its LSIUs. Each status bit is fanned in from eight LSIUs to a single signal line. The fan-in takes place in the 8166-B.

Character Ready
Character Lost
Break
Idle

CHARACTER READY

The Character Ready is a "1" signal which accompanies a parallel-bit character from an LSIU. The computer selects each LSIU individually (8165-B) or by means of a read scanner in the 8165-C. When the computer enables an LSIU which has a Character Ready signal, it receives the signal on bit 11 and accepts the character.

NOTE

Input Acknowledge is a short pulse generated in the 8166-B after the computer accepts the character. The Input Acknowledge signal is sent to the selected LSIU to clear the Character Ready, Character Lòst, and Break status flip-flops.

CHARACTER LOST

The Character Lost is a "1" signal sent from a connected LSIU through the 8166-B fan-in to the computer. If the computer fails to accept a character from theLSIU before the next character arrives, the Character Lost signal is sent to the computer.

BREAK

The Break is a "1" signal which indicates to the LSIU that there is a broken Teletype circuit. When a connected input unit has a Break signal set, it sends the signal to the computer and the operator is alerted. The Break signal is accompanied by a data character of all zeros.

IDLE

The Idle signal is sent by an LSIU when an idle line is detected. If the telegraph channel remains marking for 5 seconds, a thermal delay relay in the LSIU sends the Idle signal to the computer. The Idle and Break signals are joined in the 8166-B Input MUX as one signal, which can be logically separated by the computer. The Idle signal is accompanied by a continuous repetition of the last previous character in the holding register.

LOGIC

LSIU INTERFACE *

Each 3276 MUX cabinet can contain two 8166s, each of which can hold up to eight LSIUs (see logic diagram 36449500 in pub. no. 368 165 00). Each LSIU plugs into a separate 22-conductor receptacle. This is the LSIU interface. Through this connection pass the data bits, the four status signals, the dc electric power, the teletypewriter signals, signal-monitor line, and the Input Acknowledge. All these signals, except Input Acknowledge, travel from the LSIU into the 8166-B. The Input Acknowledge is generated within the 8166-B and sent to the LSIU to clear the status flip-flops.

FAN IN

The 8166-B Input MUX takes the data-bit signals and the status-bit signals from all eight of its LSIUs and fans them into a common signal channel. Thus, data from any of the eight LSIUs is sent to the computer over a single group of wires. LSIUs are connected consecutively. Each LSIU sends its signals to the computer separately as it is connected in its turn.

---

* The 8536 High-Speed Input Unit (HSIU) is so similar to the 8518 LSIU that references to LSIU also apply to the 8536 HSIUs.

CONTROL DATA
CORPORATION

CONTROL DATA 8167

OUTPUT SLAVE MULTIPLEXER

Pub. No. 368 161 00 (04)

8167 OUTPUT SLAVE MULTIPLEXER

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Description	1 (8167-B/C)
8167-B Output MUX	1 (8167-B/C)
8167-C Output MUX	1 (8167-B/C)
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Connect LSOU (bits 0, 1, 2)	3 (8167-B/C)
Reset Timer	3 (8167-B/C)

FIGURES

1	8167 Output Slave Multiplexer	ii (8167-B/C)

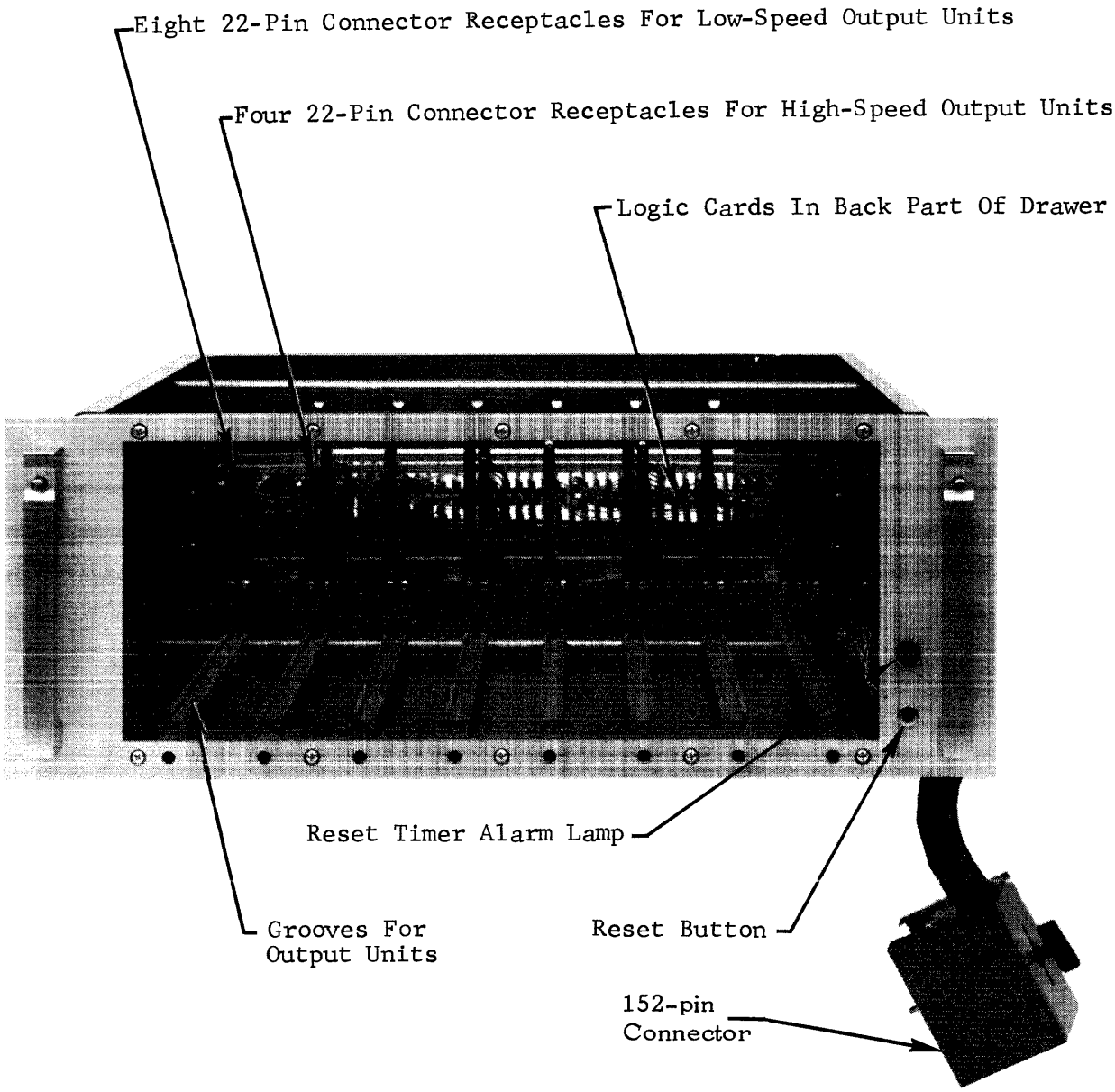
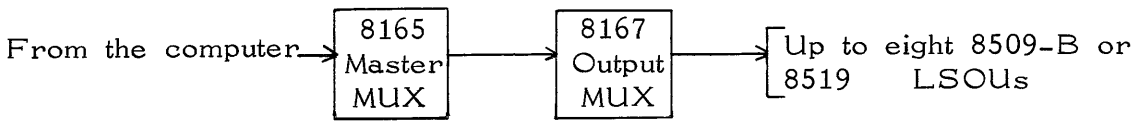


Figure 1. 8167 Output Slave Multiplexer

8167 OUTPUT SLAVE MULTIPLEXER

DESCRIPTION

The CONTROL DATA 8167 Output Slave Multiplexer (Output MUX), figure 1, is a drawer-type modular part of the 3276 Controller. It matches the interfaces of the 8165 Master MUX and eight low-speed output units (LSOUs). This manual covers both the 8167-B and the 8167-C Output MUX models.



8167-B OUTPUT MUX

The 8167-B Output MUX performs as follows:

1. It directs the connect code to the proper LSOU to enable data to enter the LSOU.

2. It distributes the Start-of-Day signal to all eight of its LSOUs.

3. It fans in the Character Request signals from the LSOUs (up to 16 in a cabinet) to one signal line to Master MUX.

4. It sends an alarm if the computer fails to periodically service the MUX.

8167-C OUTPUT MUX

The 8167-C operates in the same manner as the 8167-B with the following exception. The 8167-C has additional logic circuitry to provide a 4-second delay. This delay holds back transmission until the motors in the receiving Teletype units have had time to accelerate to operating speed.

PHYSICAL DESCRIPTION

The 8167 chassis is in drawer form and fits into the 3276 cabinet. The entire 8167 module slides out on telescoping channels and locks in either the extended or the closed position. Before the drawer can be opened, the 152-pin plug must be disconnected, and the release buttons on the two pull handles must be pressed. The plug is disconnected simply by unscrewing the wing screw, and pulling out the plug.

The back of the module contains the logic cards, and the 22-conductor LSOU receptacles.

Eight LSOUs slide into channels in the front portion of the 8167 like books on a shelf. When the LSOUs are pushed all the way in they plug into the matching sockets. Each LSOU is locked in with a plastic button.

OUTPUT LOGIC

An 8167 Output MUX directs the outgoing communication from the 8165 Master MUX to the eight LSOUs one at a time (see diagram no. 36448700 and 36713000 in pub. no. 368 165 00).

CHARACTER REQUEST

Each channel which is ready to accept data from the MUX, sends a Character Request signal to the 8167. All of these signals (up to eight) are fanned in to a single Character Request signal and sent to the 8165. If the computer has an output message ready to send, it sends a data character along with Write and Data signals to the 8165. These signals combine with Character Request in the 8165 to form an Output Ready. This signal has two main purposes:

1. To enable the data character to move on through the connected 8167 to (but not into) all eight LSOUs.

2. To send an Output Acknowledge signal to each connected output unit, enabling the data character enter the output unit.

OUTPUT ACKNOWLEDGE

This signal enters the 8167 Output MUX from the 8165 Master MUX indicating that the computer has sent a character. The Output Acknowledge combines with the Select Output signal and the selected LSOU address to direct the Output Acknowledge to the specific LSOU which has been addressed by the computer.

SELECT OUTPUT

The computer program directs the 8165 Master MUX to select one of the two 8167 Output MUXs. Both 8167 modules receive the data, the LSOU connect

code and Output Acknowledge. Only the connected 8167 receives a Select Output function code. Select Output plays the important dual role of enabling the Output Acknowledge to the selected LSOU and enabling any existing Character Request in the selected 8167 module.

CONNECT LSOU (BITS 0, 1, 2)*

The LSOU connect code is sent from the computer, decoded in the Master MUX, and sent to the 8167 in three parallel bits. These three bits are coded (0 through 7) to represent the octal number of the selected LSOU. The three bits and their complements are multiplexed for two purposes:

1. To enable a Character Request coming from any individual LSOU before it is fanned in to a single combined signal from all LSOUs in the module.

2. To address only the connected LSOU by allowing the Output Acknowledge signal to reach only the one LSOU.

When the Output Acknowledge enters the selected LSOU it enables the data character to enter the LSOU transfer register and starts the character clock.

The LSOU converts the character from parallel to serial form and sends it out on the teletypewriter communication line. The LSOU transfer register is cleared. The LSOU sends back another Character Request to the 8167. This enables the output cycle to continue.

RESET TIMER

The reset timer section of the logic in the 8167 is a delayed-alarm device which is periodically reset by the computer. If the computer fails or detects a failure in the 8050 System the computer will not reset the timer. If a reset signal is not received for 227 ms, the reset timer lights the alarm lamp and sends an Alarm signal to the console. The alarm lamp (red) is located on the right hand side of the 8167 Output MUX front panel. The reset button is below the alarm lamp.

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* The 8537 High-Speed Output Unit (HSOU) is so similar to the 8519 LSOU that reference to LSOUs also applies to the 8537 HSOU.

CONTROL DATA
CORPORATION

CONTROL DATA 8508

LOW-SPEED INPUT UNIT

Pub. No. 368 161 00 (05)

8508-B LOW-SPEED INPUT UNIT

CONTENTS

Introduction	1 (8508-B)
Panel	1 (8508-B)
Behind Panel	1 (8508-B)
Logic Cards	2 (8508-B)
Characteristics	3 (8508-B)
General Description	4 (8508-B)
Status Codes	4 (8508-B)
Logic Description	5 (8508-B)
Clock	5 (8508-B)
Counter	6 (8508-B)
Register A (Staticizer)	6 (8508-B)
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Status Codes in the Logic Diagram	6 (8508-B)

FIGURES

1	8508-B Low-Speed Input Unit (5 bits)	ii (8508-B)
2	Switches Behind Panel	2 (8508-B)
3	Data Path through an LSIU	3 (8508-B)
4	Clock Pulsing of Character	5 (8508-B)

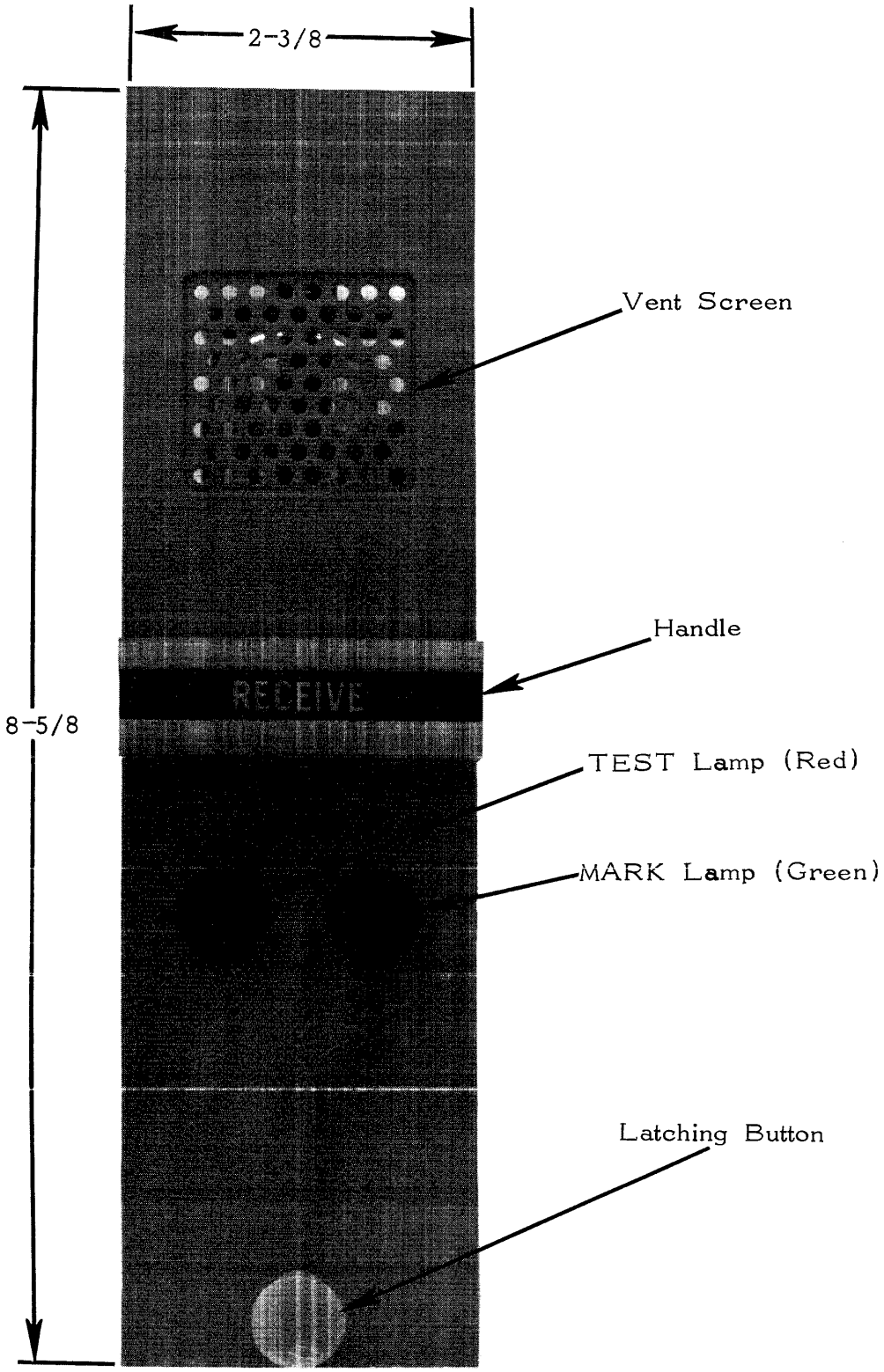
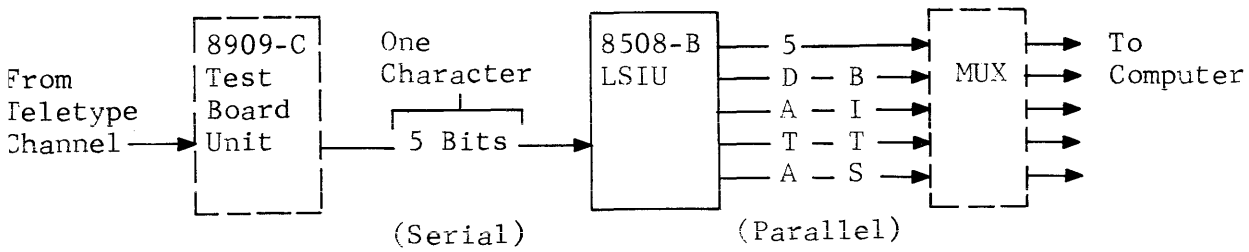


Figure 1. 8508-B Low-Speed Input Unit (5 bits)

8508-B LOW-SPEED INPUT UNIT

INTRODUCTION

The CONTROL DATA 8508-B Low-Speed Input Unit (LSIU), figure 1, is a signal coverter interposed between a teletypewriter communication channel and one input channel of an 8166-B Input Slave Multiplexer (Input MUX). The LSIU receives a message serially (one teletypewriter bit at a time), assembles each character, and sends it in parallel form to the MUX (see example). It notifies the operator in case of a broken or inactive teletypewriter line, or of a lost character.



PANEL

The 8508-B LSIU display panel (see figure 1) is actually the front surface of the 8166-B Input MUX. It contains the following lamps and switches.

MARK Lamp

This green lamp flickers while the LSIU is receiving a message. It lights every time a marking pulse is received. A steady green light indicates a marking current (no Teletype characters are being received, although the LSIU and sending teletypewriter are connected and turned on).

TEST Lamp

This red lamp lights when the OPER/TEST toggle switch is at TEST. It warns the operator that the LSIU is in test condition and is inoperative.

BEHIND PANEL

Behind the panel are the following switches (see figure 2):

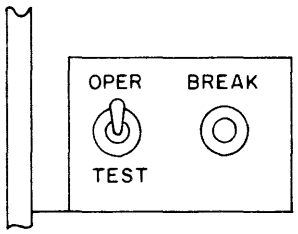


Figure 2. Switches Behind Panel

OPER/TEST Toggle Switch

This switch must be at OPER during the normal receiving operation of the LSIU. The TEST position of the switch lights the red TEST panel lamp.

This switch is used during maintenance checks or tests within the machine. Setting the switch at TEST starts the LSIU clock and counter. It may or may not set the registers, depending on whether the BREAK button is pressed.

BREAK Push-Button Switch

Pressing this button sets all registers to 1. Conversely, if this button is not pressed all registers remain cleared. However, if the LSIU is not in the marking condition this button is ineffective.

LOGIC CARDS

Each LSIU fits into an 8166-B Input MUX like one of eight books on a shelf. The LSIU contains three parallel printed-circuit cards.

Card A contains the inverters, flip-flops (FFs) and other components of the clock and counter.

Card B contains the components that clear or shift the registers, plus the Character Lost, Break FFs, and Idle relays.

Card C contains the components of the clock control and the A and B registers as well as data output circuits.

The two outer cards are hinged at the rear for easy access.

All logic signals, power, and telegraph circuits enter through the 22-pin connector on the rear of the LSIU.

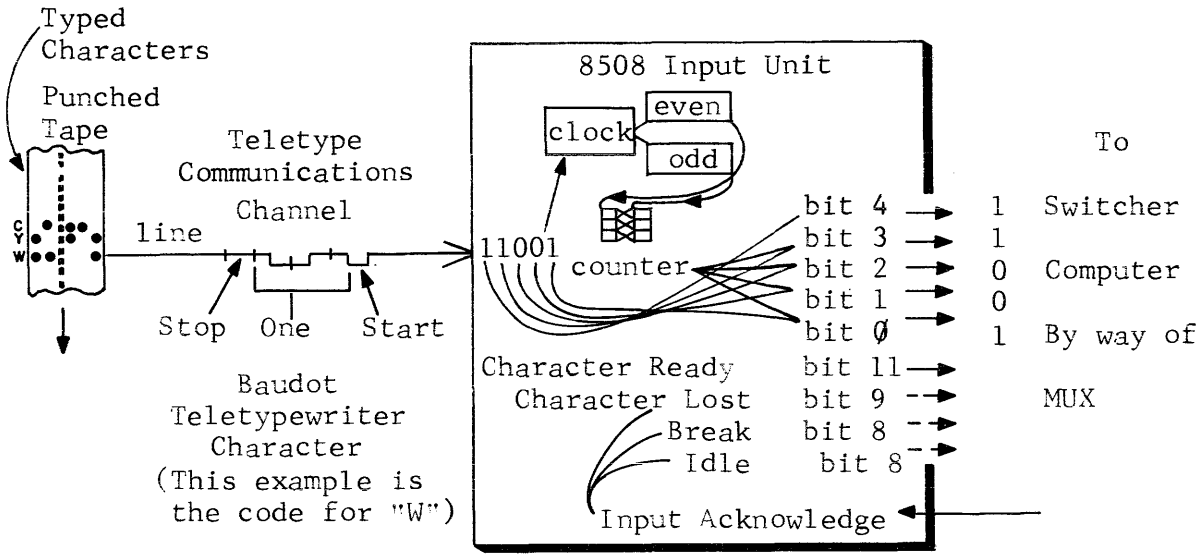


Figure 3. Data Path through an LSIU

CHARACTERISTICS

The LSIU performs the following functions (see figure 3):

1. It receives teletypewriter characters in a 7.42-unit, start-stop, Baudot code, serially, one bit at a time.

2. It drops the Start (1 bit) and Stop (1.42 bits) leaving just five data bits.

3. It distributes the five data bits of each character into the intermediate assembly register A.

4. It informs the computer through the 8166-B Input MUX that a five-bit character is ready in parallel form.

5. It reports a Character Lost in bit-9 position if the condition exists.

6. It reports a line break as well as an idle line or noncycling status. This status is inserted into bit-8 position by means of the 8166-B Input MUX.

GENERAL DESCRIPTION

An LSIU is an electronic receiving device compatible with teletypewriter communication channels, codes, and speeds. It accepts Start/Stop signals as serial-bit pulses derived from a channel with a line relay. These pulses are strobed to convert each incoming character to parallel data bits. The bits are stored in a transfer register for a maximum of one character period, awaiting withdrawal by the computer, by way of the MUX.

An LSIU is adjustable to accommodate teletypewriter speeds of 60, 66, 75, or 100 words per minute.

Like a teletypewriter printer, an LSIU responds to a start pulse. Whenever a start pulse is recognized, the internal clock executes the timing function for the serial-to-parallel conversion, stopping at the predicted end of character to await the next start pulse.

The LSIU passes electrical signals to the computer through the MUX. These signals are of two kinds: status codes and data characters.

STATUS CODES

The LSIU generates input status codes which are sent on signal lines to the computer through the 8166-B Input MUX and the Master MUX.

Character Ready

The Character Ready signal tells the computer that a character has been assembled in the holding register and is ready to be withdrawn. The Character Ready is generated by the stop pulse after the last character bit enters the B register. The signal is sent to the 8165 Master MUX through the 8166-B Input MUX.

Character Lost

The Character Lost signal is sent to the computer if the computer does not pick up a character before the next character arrives at the holding register. The second character will destroy the previous character.

Break Signal

The Break signal indicates a break in line current from a remote station. It is sent to the computer if there is no Stop signal at the end of a character, but just one continuous space (absence of marking current). A Break signal is generated also if a remote station activates a break key. A Break signal is accompanied by an all-zero-bit character.

Idle Signal

The Idle signal is generated by R^{203} thermal relay. If the teletypewriter circuit is apparently intact, and no character is received for a specified period (5 to 10 seconds for example), the thermal relay sets the idle bit in the LSIU. See paragraph on "Status Codes in the Logic Diagram" in this book.

Whenever the computer accepts a data/status word from the LSIU, it acknowledges the event with an Input Acknowledge signal that clears the LSIU's status bits. Thus, subsequent interrogations of the LSIU result in no new information until the next event (character arrival) occurs.

LOGIC DESCRIPTION

The LSIU receives a teletypewriter character in a 7.42-unit start-stop code (see logic drawing no. 36461700 in pub. no. 368 165 00). The message comes in serially one bit at a time. A start pulse, or line-logic "0" causes the input relay R200 to be de-energized, and the normally open contacts are opened. The resultant logic"1" activates the internal circuit of the LSIU. After a half-start-pulse delay, a "1" signal sets the clock-control FF. The clock control sends out a "1" which starts the clock.

CLOCK

The clock of the LSIU is a free running multivibrator. As it cycles it sends out even and odd pulses. When the Clock FF is set, it sends out a short pulse through the even-clock circuit. When the clock is cleared it sends a short pulse ("1") to the odd-clock circuit (N^{205} and N^{207}). The clock-produced even and odd pulses are clearly separated in time. The clock cycles seven times for each character. Then it is turned off by the stop pulse (coded 7 count). See figure 4.

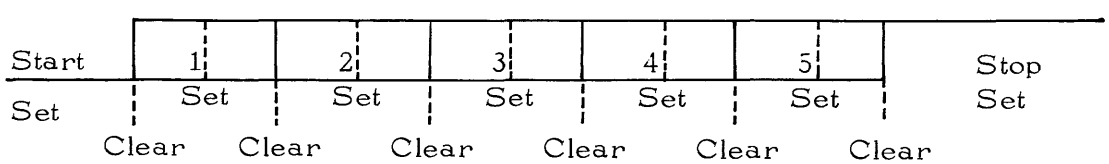


Figure 4. Clock Pulsing of Character

Even Clock and Odd Clock

The alternating pulses from the even and odd clocks feed into the counter. The even clock enables the left rank FFs of the counter to be set or cleared if other AND conditions are met. The odd clock transfers the count from left to right FFs.

COUNTER

The left rank of the counter counts in binary. The right rank accepts the count and gates the advance. The even/odd pulses alternate back and forth between the left and right ranks advancing the count by one for each cycle. The seven count and the even-clock pulse clear the clock control, and the clock.

REGISTER A (STATICIZER)

The register A is loaded with five data bits corresponding to a Baudot character. The counter establishes the sequence of loading the Register FFs. The clock provides the register-loading pulse. The output of diode card Z^{200} provides the identity ("1" or "0") of each bit of each character.

STOP PULSE

The stop pulse is energized by the even clock and by the counter at the count of seven. It performs the following functions:

1. After 120 usec, it shifts the data from register A to register B.
2. It clears or turns off the clock control.
3. It clears or stops the clock.
4. It clears the counter.
5. It gates the Character Lost and Break alarm signal FFs.
6. After another 26 usec, a 19-usec pulse clears register A, and sets the Character Ready FF.

STATUS CODES IN THE LOGIC DIAGRAM

The Input Acknowledge signal from the computer clears the Character Ready, Character Lost and Break FFs. However, if the computer fails to acknowledge

the character from register B before the next character arrives, the Character Ready FF will not be cleared. The Character Lost FF then will be set when the next character is assembled in the LSIU.

If the Teletype circuit is disrupted and all the bits in register A are"1"s, the Break FF is set. The Break signal is sent by way of the MUX to the computer.

If one character is not followed by another within an interval controlled by thermal relay R^{203}, the relay will send an Idle signal. The time delay which sets off the thermal relay is set at a length of time just longer than one character cycle.

The Break and Idle outputs are combined in the MUX. To test for Break or Idle, examine the input data. If the bits are not all "0"s, the condition is idle. When all bits are "0"s the condition is Break.

CONTROL DATA
CORPORATION

CONTROL DATA 8509

LOW-SPEED OUTPUT UNIT

Pub. No. 368 161 00 (06)

8509-B LOW-SPEED OUTPUT UNIT

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Panel	1 (8509-B)
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FIGURES

1	8509-B Low-Speed Output Unit	ii (8509-B)
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4	Clock Pulsing of Character	6 (8509-B)

TABLES

1	Order of Serialized Bits (five-level)	6 (8509-B)

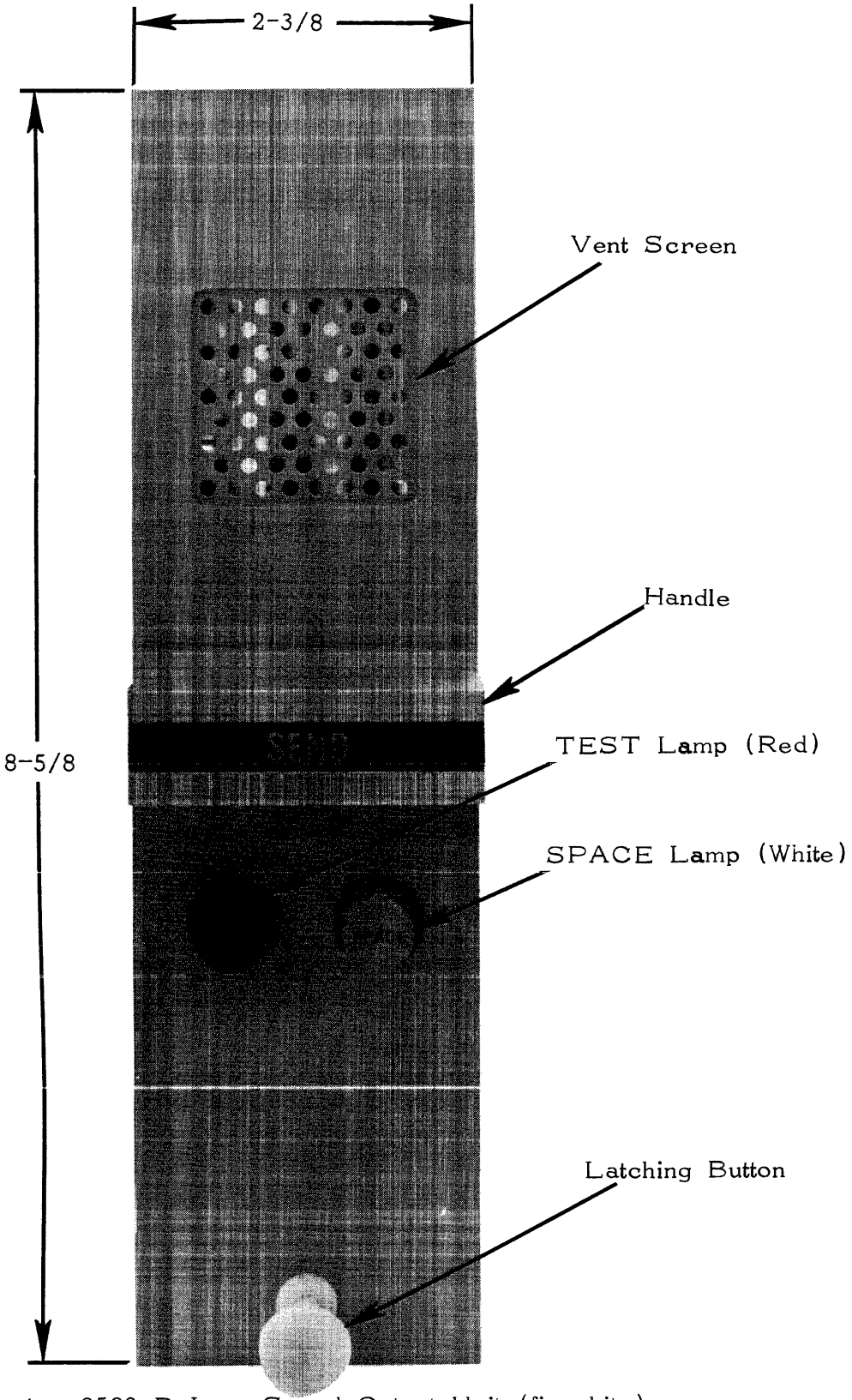
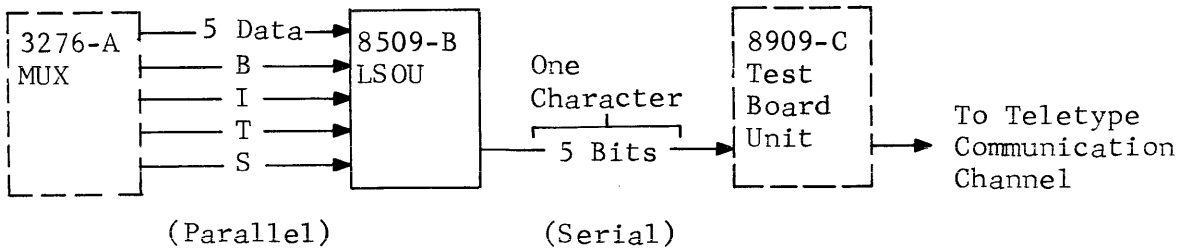


Figure 1. 8509-B Low-Speed Output Unit (five bits)

8509-B LOW-SPEED OUTPUT UNIT

INTRODUCTION

The CONTROL DATA 8509-B Low-Speed Ouput Unit (LSOU), figure 1, is a signal converter interposed between one output point on an 8167 Output Slave Multiplexer (Output MUX) and a teletypewriter communication channel. The LSOU receives parallel-bit characters from the MUX. By means of a clock and counter, the LSOU sends the bits serially to the telegraph circuit in the 7.5-unit start-stop teletypewriter code.



PANEL

The 8509-B LSOU control panel (see figure 1) mounts flush against the front surface of the 8167 Output MUX. It contains the following labeled lamps and switches:

SPACE LAMP

This white lamp flickers while the LSOU is sending a message. It lights every time there is a break or space pulse in the teletypewriter communications line.

TEST LAMP

This red lamp lights when the OPER/TEST toggle switch (behind panel) is at TEST. The lighted lamp warns the operator that the LSOU is in test condition and therefore inoperative.

BEHIND PANEL

Behind the panel on the right side are the following switches (see figure 2):

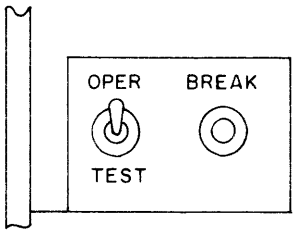


Figure 2. Switches behind the Panel

OPER/TEST TOGGLE SWITCH

This switch must be at OPER during the normal operation of the LSOU. The TEST position lights the red TEST lamp (on the panel front). It sets the clock control which in turn starts the clock. This switch can be used during maintenance checks and tests.

BREAK PUSH-BUTTON SWITCH

When this push button is pressed it actuates relay R^{100} which cuts the teletypewriter circuit. It also lights the SPACE lamp.

LOGIC CARDS

Each LSOU fits into an 8167-B Output MUX like one of eight books on a shelf. The LSOU consists of three printed-circuit cards. The two outer cards are hinged at the rear for easy access.

Card A contains (Transfer) register A and (Holding) register B as well as the status code flip-flop (FF).

Card B contains the character serializer.

Card C contains the clock and counter.

Since the 8509-A LSOU is a pluggable unit, all logic signals, power, and telegraph circuits enter through the 22-pin connector on the rear of the LSOU.

CHARACTERISTICS

The LSOU performs as follows when it is connected to send a character:

1. It receives five parallel data bits from the computer by way of the MUX.

2. Simultaneously it receives an Output Acknowledge signal. This enables the five-bit character to enter register A.

3. It shifts the character from register A to B (if the clock is stopped) and clears register A.

4. It requests the next five-bit character by generating a Character Request signal.

5. It starts the multivibrator clock.

6. The clock counter sends one bit at a time in sequence and adds start and stop units.

7. The serializer "ands" the counter and bit register sequentially, thus regulating the consecutive order of the bits.

8. It sends the 7.5-unit code to the output keyer in the test board unit.

Each character in a 100-wpm (for example) system has a duration of 100 ms including start and stop pulses.

GENERAL DESCRIPTION

An LSOU is an electronic parallel-to-serial converter that is compatible with teletypewriter communication channels, codes, and speeds (see figure 3). The 8509-B LSOU accepts one five-bit character at a time by way of the MUX. Each character is stored in a register before it is "clocked out". A series of pulses is produced which contains the data bits and the start and stop pulses required by the teletypewriter circuit driven by the LSOU. An 8509-B LSOU can generate 7.42- or 7.5-unit characters with five information pulses. The clock is adjustable to provide output rates within the range of 60 to 100 wpm.

An internal five-bit register stores one five-bit character in addition to the character undergoing parallel-to-serial conversion. For this reason, the computer has the time of one character cycle to respond to a Character Request from the LSOU while maintaining the maximum output rate.

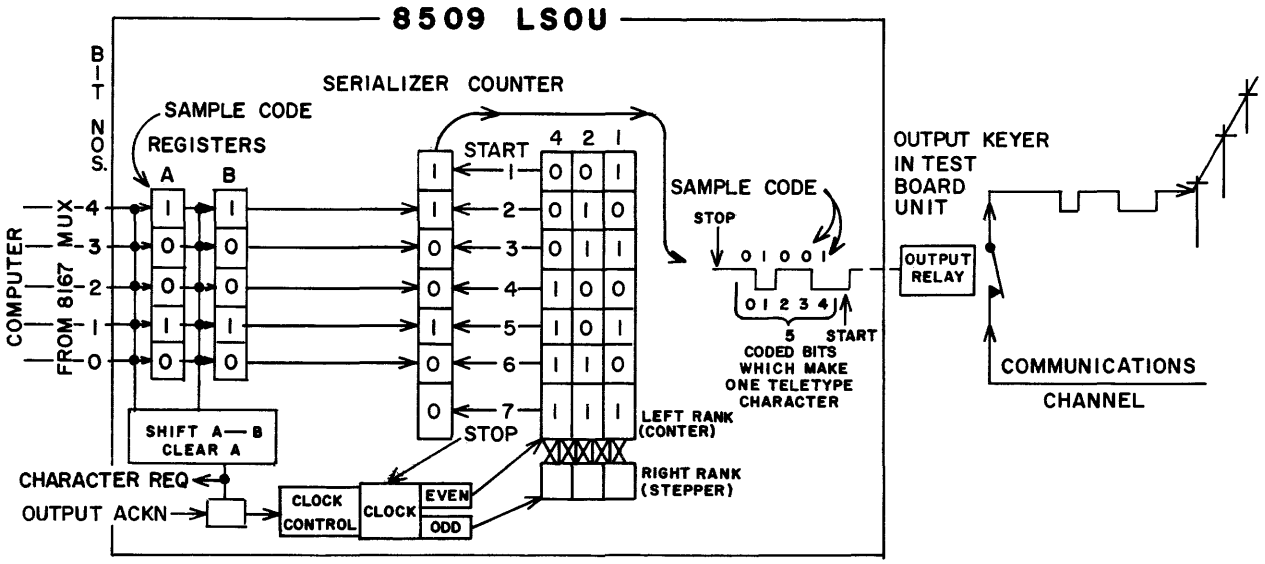


Figure 3. Data Path through an LSOU

An LSOU generates only one status code, Character Request. When the computer responds with Information Ready, the MUX enables the data character and Output Acknowledge to be sent to the LSOU. This event causes the Request to drop and the serializing function to start in the LSOU. If no character is transferred with the acknowledgement, a blank character is generated and sent by the LSOU. Failure of the computer to acknowledge a Request merely extends the stop pulse.

LOGIC DESCRIPTION

When the LSOU is not sending data, the relay puller P100 is de-energized (see logic diagram no. 36461800 in pub. no. 368 165 00). The telegraph communication channel is a closed circuit. A marking line current passes through the circuit. This holds true until the start pulse of a character reaches the relay puller P100 which energizes the output keyer in the test board unit.

When a five-bit character passes through the LSOU, the five bits reach the LSOU in parallel in external voltage levels ("1" = -0.5v, "0" = -16v). Each bit passes through an M card and is converted to internal voltage levels ("1" = 3.5v, "0" = nominal 0v).

OUTPUT ACKNOWLEDGE SIGNAL

Whenever an 8509-B LSOU receives a five-bit character from the computer, it also receives an Output Acknowledge signal. The Output Acknowledge is a logic "1" signal which has the following functions within the LSOU:

1. It enables the data character to enter register A.
2. It sets a FF A^{110}/A^{111} which in turn gates the clock control K^{100}/K^{101}.

CLOCK CONTROL (STARTS AND STOPS CLOCK)

With the clock stopped between data characters, the outputs of inverter I^{104} and N103 are "1"s. These "1"s are gated with the "1" from A^{111} to set the the clock Control FF K^{100}/K^{101}. When the clock control is set it does the following:

1. It forms a 19-usec pulse to enter the register control (shift (A) B, Clear A).
2. It forms a 19-usec pulse which starts the clock on the even pulse.
3. It enables the clock to cycle at a frequency regulated by two adjustable delay cards. Each delay is set to one-half-bit pulse duration.

REGISTER CONTROL

The register control has these main purposes.

1. To shift the contents of register A into register B when the clock starts.
2. To clear register A 6 usec after register A has been shifted to B.
3. To enable the next Character Request to be sent to the 8165 MUX.

CLOCK

The clock of the LSOU is a free-running multivibrator. As it cycles it sends out even and odd pulses. When the clock is set it sends a short pulse ("1") out through the even-clock circuit. When the clock is cleared it sends a short pulse ("1") to the odd-clock circuit. The clock produces clearly separated even and odd pulses (see figure 4). The clock cycles eight times for each character. These pulses act to set and shift the counter FFs and to clear the clock control after the last data bit. The clock control in turn stops the clock.

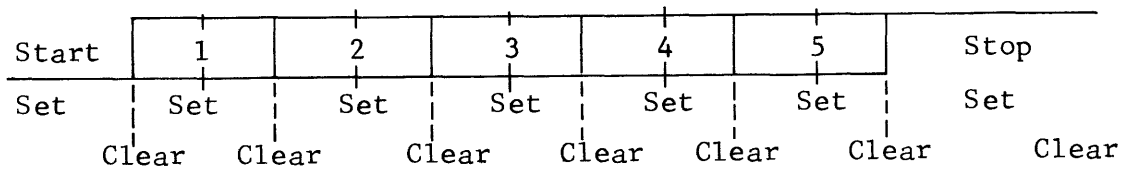


Figure 4. Clock Pulsing of Character

EVEN CLOCK AND ODD CLOCK

The alternating pulses from the even and odd clocks feed into the counter. The even clock enables the left rank FFs of the counter to be set or cleared if other AND conditions are met. The odd clock transfers the count from left to right rank FFs. The even- and odd-clock slaves send pulses alternately to the left and right ranks of the counter.

COUNTER

The left rank of the counter counts in binary. The right rank stores the count and gates the advance. The even/odd pulses alternate back and forth between the left and right ranks advancing the count by one for each cycle. The counter couts up to 8. The 8 count with odd clock clears the clock control which in turn clears, or turns off, the clock.

SERIALIZER

The counter is part of the serializer circuit. The counter provides binary count codes for the serializer. Through AND gates the codes enable six gates (a start pulse and five bits from register B) one at a time in the serializer to provide the character format in table 1.

TABLE 1. ORDER OF SERIALIZED BITS (FIVE-LEVEL)

COUNTER COUNT	SERIALIZER CONNECTION	DATA
1	1	"0" (START)
2	2	Bit 4 binary code ("1" or "0")
3	3	Bit 3 binary code ("1" or "0")
4	4	Bit 2 binary code ("1" or "0")
5	5	Bit 1 binary code ("1" or "0")
6	6	Bit 0 binary code ("1" or "0")
7.5	no connection	"1" (STOP)

CONTROL DATA
CORPORATION

CONTROL DATA 8518

LOW-SPEED INPUT UNIT

Pub. No. 368 161 00 (07)

8518-B LOW-SPEED INPUT UNIT

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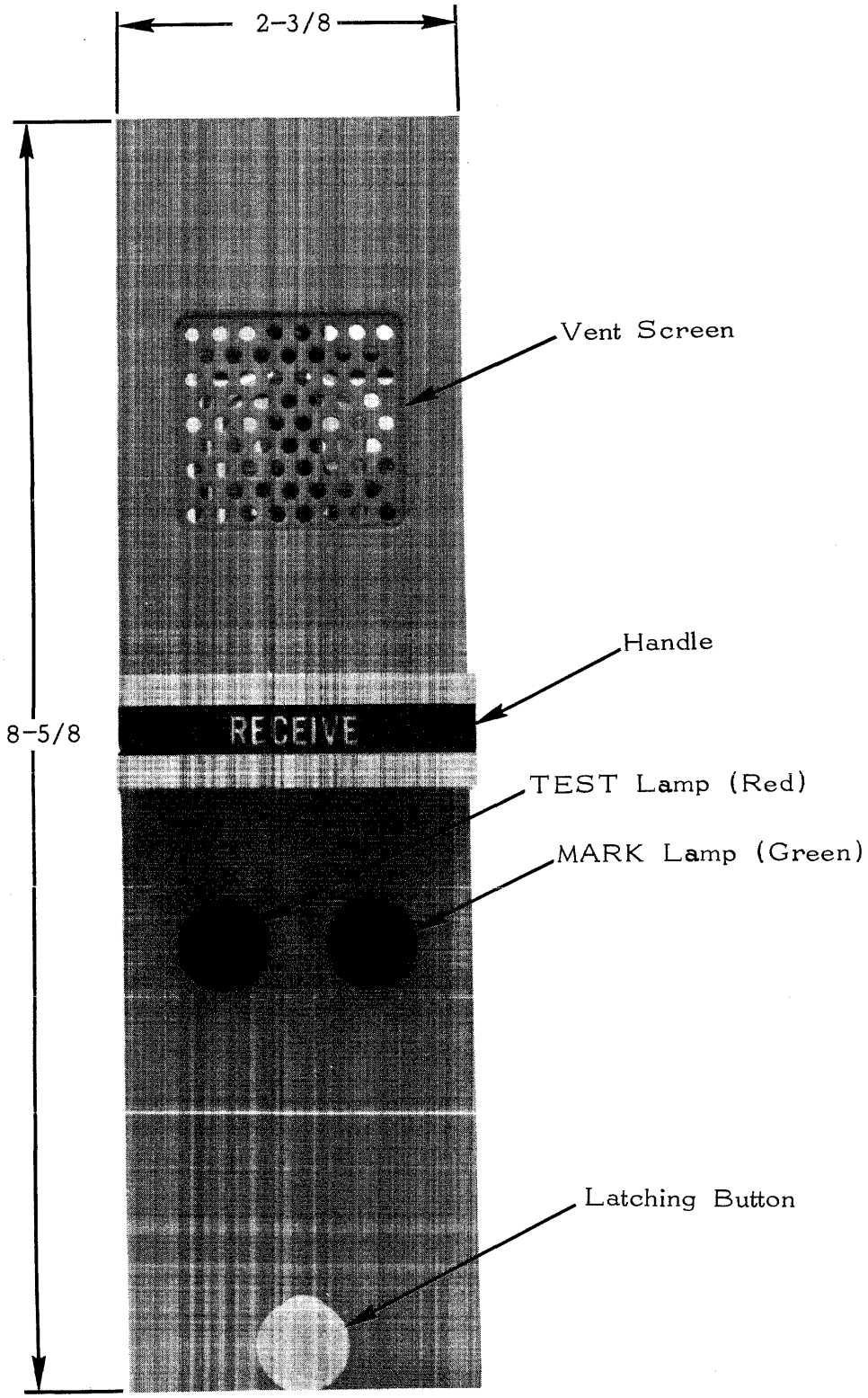
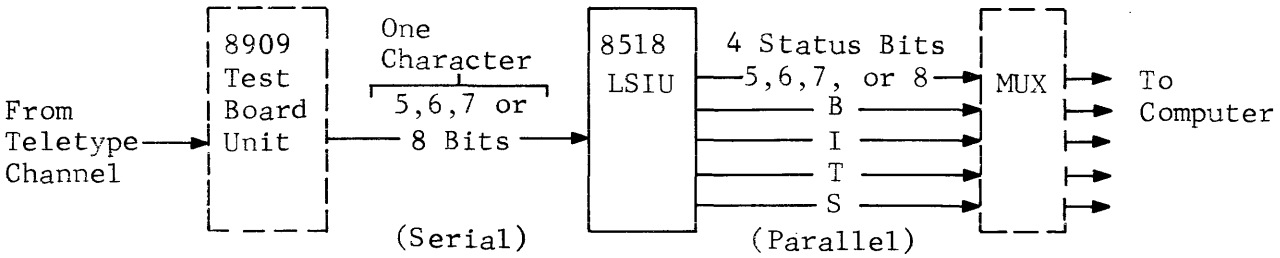


Figure 1. 8518-B Low-Speed Input Unit

8518 LOW-SPEED INPUT UNIT

INTRODUCTION

The CONTROL DATA 8518 Low-Speed Input Unit (LSIU), figure 1, is a signal converter interposed between a teletypewriter communication channel and one input channel of an 8166-B Input Slave Multiplexer (Input MUX). The LSIU receives a message serially (one teletypewriter bit at a time). It assembles each character and sends it in parallel form to the MUX. It notifies the operator of a broken or inactive teletypewriter line, or a lost character.



PANEL

The 8518 display panel (see figure 1) is actually the front surface of the 8166-B Input MUX. It contains the following lamps and switches:

MARK LAMP

This green lamp flickers while the LSIU is receiving a message. It lights every time a marking pulse is received. A steady green light indicates a marking current (no characters are being received, although the LSIU and sending device are connected and turned on).

TEST LAMP

This red lamp lights when the OPER/TEST toggle switch is at TEST warning the operator that the LSIU is in test condition and is inoperative.

BEHIND PANEL

Behind the panel are the following switches (see figure 2).

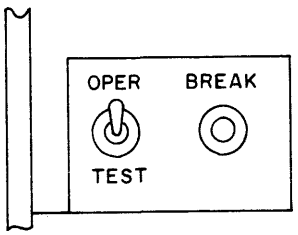


Figure 2. Switches behind the Panel

OPER/TEST TOGGLE SWITCH

This switch must be at OPER during the normal receiving operation of the LSIU. The TEST position of the switch lights the red TEST panel lamp. This switch is used during maintenance checks or tests within the machine. Setting the switch at TEST starts the LSIU clock and counter. It may or may not set the registers depending on whether the BREAK button is pressed.

BREAK PUSH-BUTTON SWITCH

Pressing this button down sets all registers to 1. Conversely, if this button is not pressed all registers remain cleared. However, if the LSIU is not in the marking condition this button is ineffective.

LOGIC CARDS

Each LSIU fits into an 8166-B Input MUX like one of eight books on a shelf. The LSIU contains three parallel printed-circuit cards.

Card A contains the inverters, flip-flops (FFs) and other components of the clock and counter.

Card B contains the components that clear or shift the registers, plus the Character Lost, Break, and Idle FFs, and the clock control.

Card C contains the components of the clock control and the A and B register, and data output circuits.

The two outer cards are hinged at the rear for easy access .

CHARACTERISTICS

The LSIU performs the following functions (see figure 3):

1. It receives teletypewriter characters serially one bit at a time in a start-stop Baudot code, or any code using five-, six-, seven- or eight-bit characteristics and any number of pulses from 7 to 11.

2. It drops the start (one bit) and stop (one, one and a half, or two bits) leaving just the required data bits.

3. It distributes the eight data bits of each character into the intermediate assembly register A.

4. It informs the computer through the 8166-B Slave MUX that a character is ready in parallel form.

5. It reports a Character Lost in bit-9 position if the condition exists.

6. It reports a line break as well as an idle line or noncycling status. This status is inserted into bit-8 position by means of the 8166-B.

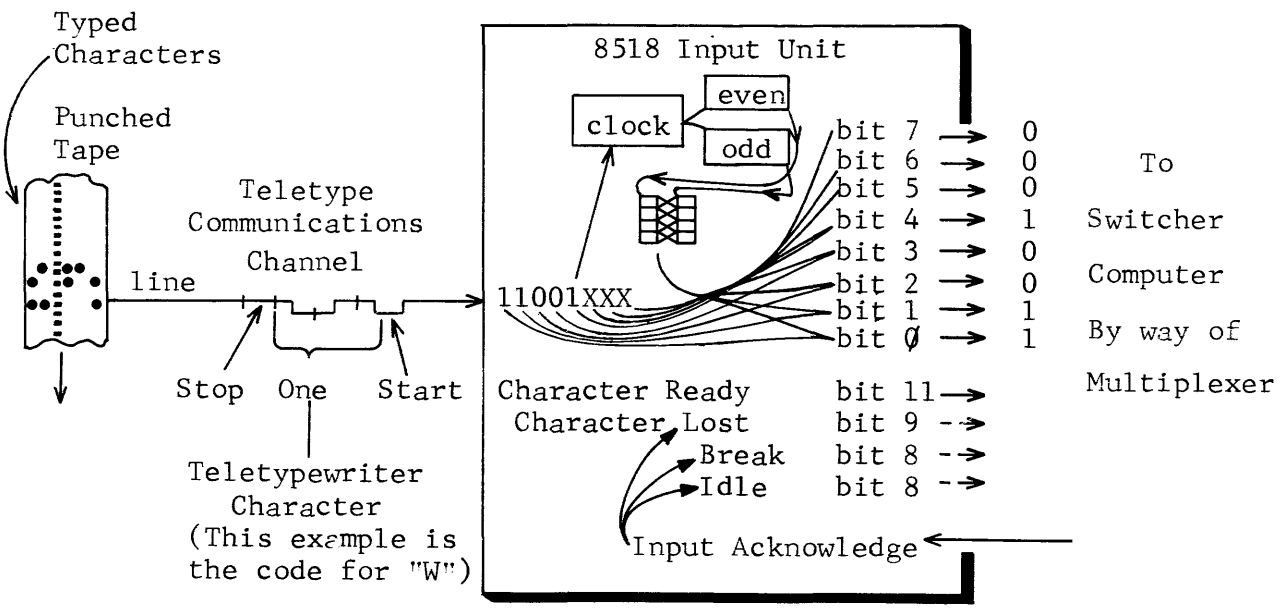


Figure 3. Path of Data through an LSIU

GENERAL DESCRIPTION

An LSIU is an electronic receiving device compatible with teletypewriter communication channels, codes, and speeds. It accepts Start/Stop signals as serial-bit pulses derived from a channel with a line relay. These pulses are strobed to convert each incoming character to parallel data bits. The bits are stored in a transfer register for a maximum of one character period, awaiting withdrawal by the computer, by way of the MUX.

An LSIU is adjustable to accommodate teletypewriter speeds of 60, 66, 75, or 100 words per minute.

Like a teletypewriter printer, an LSIU responds to a start pulse. Whenever a start pulse is recognized, the internal clock executes the timing function for the serial-to-parallel conversion, stopping at the predicted end of character to await the next start pulse.

The LSIU passes electrical signals on to the computer through the MUX. These signals are of two kinds; status codes and data characters.

STATUS CODES

The LSIU generates input status codes which are sent on signal lines to the computer through the 8166-B Input MUX and the Master MUX.

CHARACTER READY

The Character Ready signal tells the computer that a character has been assembled in the holding register and is ready to be withdrawn. The Character Ready is generated by the stop pulse after the last character bit enters the B register. The signal is sent to the 8165 Master MUX through the 8166-B Input MUX.

CHARACTER LOST

The Character Lost signal is sent to the switcher computer if the computer does not pick up a character before the next character arrives at the holding register. The second character will destroy the previous character.

BREAK

The Break Signal indicates a break in line current from a remote station. It is sent to the computer if there is no Stop signal at the end of a character, but just one continuous space (absence of marking current). A Break signal is generated also if a remote station activates a break key. A Break signal is accompanied by an all-zero bit character.

IDLE

The Idle signal is generated by R303 thermal relay. If the teletypewriter circuit is apparently intact, and no character is received for a specified period (5 to 10 seconds for example), the thermal relay sets the idle bit in the LSIU. See the paragraph on "Status Codes in the Logic Diagram" in this book.

Whenever the computer accepts a data/status word from the LSIU, it acknowledges the event with an Input Acknowledge signal that clears the LSIUs status bits. Thus, subsequent interrogations of the LSIU result in no new information until the next event (character arrival) occurs.

LOGIC DESCRIPTION

The LSIU receives a teletypewriter character in a start/stop code (see logic drawing no. 36461900 in pub. no. 368 165 00). The message comes in serially one bit at a time. A start pulse, or line-logic "0" causes the input relay R300 to be de-energized and the normally open contacts are opened. The resultant logic "1" activates the internal circuit of the LSIU. After a half-start-pulse delay a "1" signal sets the clock control. The clock control sends out a "1" which starts the clock.

CLOCK

The clock of the LSIU is a free-running multivibrator. As it cycles it sends out even and odd pulses. When the clock FF is set, it sends a short pulse out through the even-clock circuit. When the clock is cleared it sends a short pulse ("1") to the odd-clock circuit. The clock-produced even and odd pulses are clearly separated in time. The clock cycles a preset number of times for each character (see figure 4). Then it is turned off by the stop pulse.

EVEN CLOCK AND ODD CLOCK

The alternating pulses from the even and odd clocks feed into the counter. The even clock enables the left rank FF of the counter to be set or cleared if other

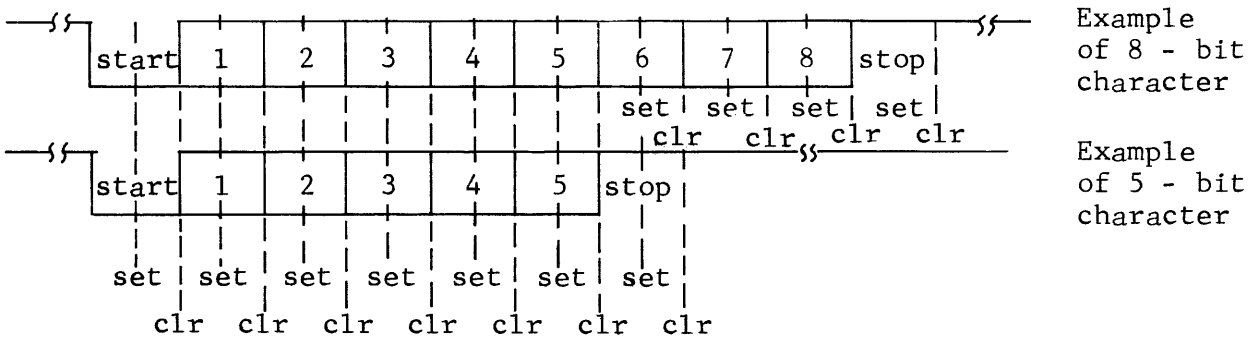


Figure 4. Clock Pulsing of Character

AND conditions are met. The odd clock transfers the count from left to right rank FF.

COUNTER

The left rank of the counter counts in binary. The right rank accepts the count and gates the advance. The even/odd pulses alternate back and forth between the left and right ranks advancing the count by one, for each cycle. A preset count and the even-clock pulse clear the clock control, and stop the clock.

REGISTER A (STATICIZER)

The register A is loaded with eight data bits corresponding to the code character. The counter establishes the sequence of loading the register FFs. The clock provides the register-loading pulse. The output of diode card Z300 provides the identity ("1" or "0") of each bit of each character.

STOP PULSE

The stop pulse is energized by the even clock and by the counter at the desired count. It performs the following functions on the desired even-clock pulse:

1. It shifts the data from register A to register B.
2. It gates the Character Lost and Break Alarm signal FFs.
3. It sets the Character Ready FF.

The stop pulse performs the following functions on the next odd-clock pulse.

1. It clears the clock control, stopping the clock.
2. It clears the register A.

STATUS CODES IN THE LOGIC DIAGRAM

The Input Acknowledge signal from the computer clears the Character Ready, Character Lost and Break FFs. However, if the computer fails to acknowledge the character from register B before the next character arrives, the Character Ready FF will not be cleared. The Character Lost FF then will be set when the next character is assembled in the LSIU.

If the Teletype circuit is disrupted and all the bits in register A are "1"s, the Break FF is set. This signal is sent by way of the MUX to the computer.

If one character is not followed by another within an interval controlled by thermal relay R303, the relay will send an Idle signal to the computer. The time delay which sets off the thermal relay is set at a length of time just longer than one character cycle.

The Break and Idle signal lines are joined into one line (bit 8) in the MUX. To test for Break or Idle, examine the input data. If the bits are not all "0"s the condition is idle. When all bits are "0"s the condition is Break.

CONTROL DATA
CORPORATION

CONTROL DATA 8519

LOW-SPEED INPUT UNIT

Pub. No. 368 161 00 (08)

8519-B LOW-SPEED OUTPUT UNIT

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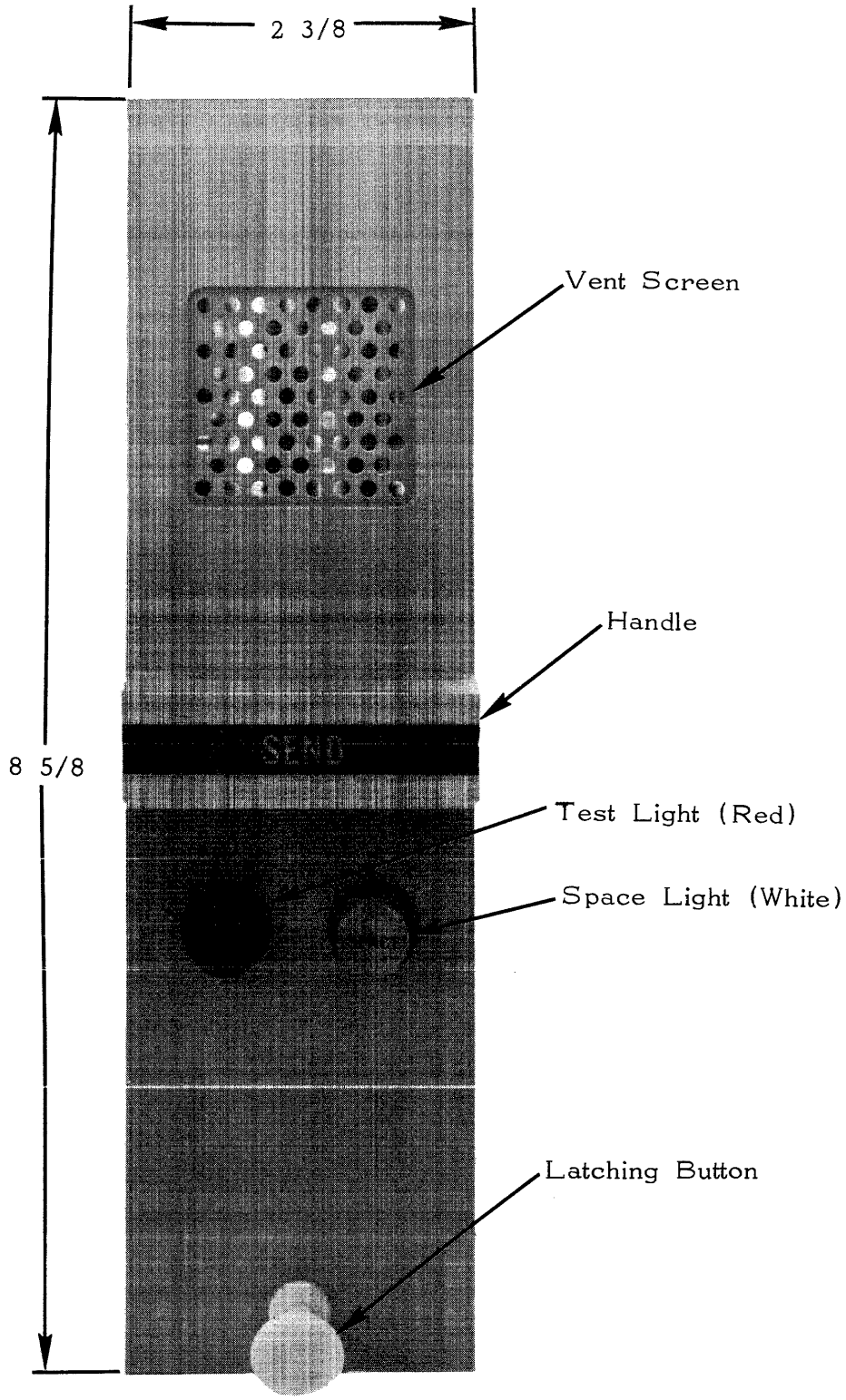
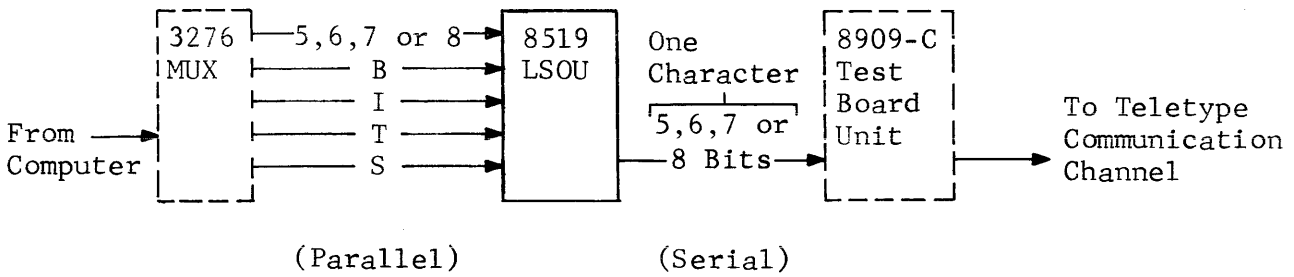


Figure 1. 8519-B Low-Speed Output Unit

8519 LOW-SPEED OUTPUT UNIT

INTRODUCTION

The CONTROL DATA 8519 Low-Speed Output Unit (LSOU), figure 1, is a signal converter interposed between one output point on an 8167 Output Slave Multiplexer (Output MUX) and a teletypewriter communication channel (see example). The LSOU receives parallel bit characters from the MUX. By means of a clock and counter, it sends the bits serially to the telegraph circuit in the 10-unit, start-stop, teletypewriter code.



PANEL

The 8519 LSOU control panel (see figure 1) mounts flush against the front surface of the 8167 Output MUX. It contains the following labeled lamps and switches:

SPACE LAMP

This white lamp flickers while the LSOU is sending a message. It lights every time there is a break or space pulse in the teletypewriter communications line.

TEST LAMP

This red lamp lights when the OPER/TEST toggle switch is at TEST, warning the operator that the LSOU is in test condition and therefore inoperative.

BEHIND PANEL

Behind the panel on the right side are the following switches (see figure 2):

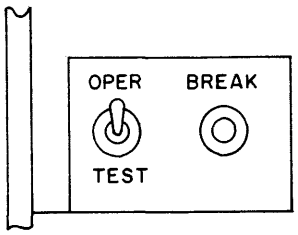


Figure 2. Switches behind the Panel

OPER/TEST TOGGLE SWITCH

This switch must be at OPER during the normal operation of the LSOU. The TEST position lights the red TEST lamp. It sets the clock control which in turn starts the clock. This switch can be used during maintenance checks and tests.

BREAK PUSH-BUTTON SWITCH

When this button is pressed, it cuts the teletypewriter circuit. It also lights the SPACE lamp.

LOGIC CARDS

Each LSOU fits into an 8167-B Output MUX like one of eight books on a shelf. The LSOU consists of three printed circuit cards.

Card A contains Transfer register A and Holding register B as well as the input circuits.

Card B contains the character serializer and counter.

Card C contains the clock, shift and clear circuits.

The two outer cards are hinged at the rear for easy access. Since the 8519-A LSOU is a pluggable unit, all logic signals, power, and telegraph circuits enter through the 22-pin connector on the rear of the LSOU.

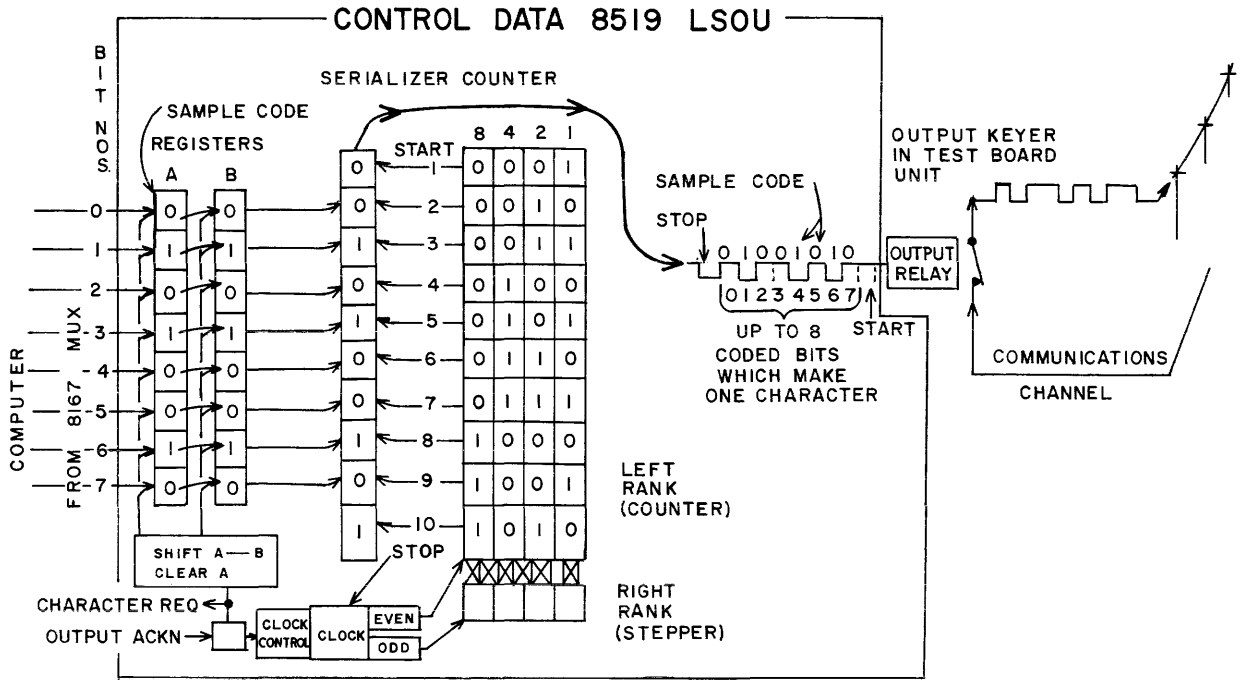


Figure 3. Path of Data through an LSOU

CHARACTERISTICS

The LSOU performs as follows (see figure 3) when it is connected to send a character:

1. It receives up to eight parallel data bits.

2. Simultaneously it receives an Output Acknowledge signal. This enables the character to enter register A.

3. It shifts the character from register A to B (if the clock is stopped) and clears register A.

4. It requests the next eight-bit character by generating a Character Request signal.

5. It starts the multivibrator.

6. The clock counter gates the serializer.

7. The serializer "ands" the counter and bit register sequentially, thereby regulating the consecutive order of the bits.

8. The output keyer puts the start/stop code on the communications line. It sends a start/stop code to the output keyer in the test board unit.

Each character in a 100-wpm (for example) system has a duration of 100 ms including start and stop pulses.

GENERAL DESCRIPTION

An LSOU is an electronic parallel-to-serial converter that is compatible with teletypewriter communication channels, codes and speeds. The 8519 LSOU accepts one parallel-bit character at a time by way of the MUX. Each character is stored in a register before it is "clocked out". A series of pulses is produced containing the data bits and the start and stop pulses required by the teletypewriter circuit driven by the LSOU. An 8519 LSOU can generate characters with five, six, seven, or eight information pulses. The clock is adjustable to provide output rates within the range of 60 to 100 wpm.

An internal single-character register stores one eight-bit character in addition to the character undergoing parallel-to-serial conversions. For this reason, the computer has the time of one character cycle to respond to a Character Request from the LSOU while maintaining the maximum output rate.

An LSOU generates only one status code, Character Request. When the computer responds with Information Ready, the MUX enables the data character and Output Acknowledge to be sent to the LSOU. This event causes the Request to drop and the serializing function to start in the LSOU. If no character is transferred with the acknowledgement, a blank character is generated and sent by the LSOU. Failure of the computer to acknowledge a Request, merely extends the stop pulse.

LOGIC DESCRIPTION

When the LSOU is not sending data the relay puller P^{200} is de-energized (see logic diagram no. 36462000 in pub. no. 368 165 00). The telegraph communication channel is a closed circuit. A marking line current passes through the circuit. This holds true until the start pulse of a character reaches the relay puller P^{200}, which energizes the output keyer in the test board unit.

When a character passes through the LSOU, the eight bits reach the LSOU in parallel, in external voltage levels ("1" = -0v, "0" = -16v). Each bit passes through an M card and is converted to internal voltage levels ("1" = -3.5v, "0" = nominal 0v).

OUTPUT ACKNOWLEDGE

Whenever an LSOU receives a character from the computer, it also receives an Output Acknowledge signal. The Output Acknowledge is a logic "1" signal which has the following functions within the LSOU:

1. It enables the data character to enter register A.
2. It sets the flip-flop (FF) A^{216}/A^{217} which in turn gates the clock control K^{200}/K^{201}.

CLOCK CONTROL (STARTS AND STOPS THE CLOCK)

With the clock stopped between data characters, the outputs of inverter I^{200} and N^{203} are "1"s. These "1"s are gated with the "1" from A^{217} to set the clock control FF K^{200}/K^{201}.

When the clock control is set it does the following:

1. It forms the 19-usec pulse to enter the register control (shift (A)→B), and after 6 usec more, clears A.
2. It forms a 19-usec pulse which starts the clock on the even pulse.
3. It enables the clock to cycle at a frequency regulated by two adjustable delay cards. Each delay is set to 1/2-bit pulse duration.

REGISTER CONTROL

The register control has these main purposes:

1. To shift the contents of register A into register B at the same time that the clock starts.
2. To clear register A, 6 usec after (A) has been shifted to B.
3. To enable the next Character Request to be sent to the 8165 MUX.

CLOCK

The clock of the LSOU is a free-running multivibrator. As it cycles it sends out even and odd pulses. When the clock is set it sends a short pulse ("1")

out through the even-clock slaves. When the clock is cleared it sends a short pulse ("1") through the odd-clock slaves. The clock produces clearly separated even and odd pulses. It cycles a preset number of times for each character (see figure 4). These pulses act to set and shift the counter FFs and to clear the clock control after the last data bit. The clock control in turn stops the clock.

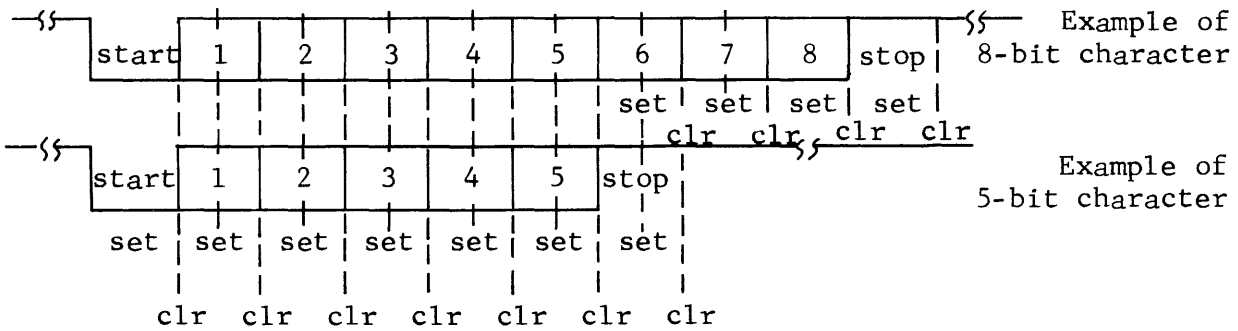


Figure 4. Clock Pulsing of a Character

EVEN CLOCK AND ODD CLOCK

The alternating pulses from the even and odd clocks feed into the counter. The even clock enables the left rank FFs of the counter to be set or cleared if other AND conditions are met. The odd clock transfers the count from left to right FFs. The even and odd clocks send pulses alternately to the left and right ranks of the counter.

COUNTER

The left rank of the counter counts in binary. The right rank stores the count and gates the advance. The even/odd pulses alternate back and forth between the left and right ranks advancing the count by one for each cycle. The counter counts up to 12 as a maximum. A predetermined count, with odd or even clock, clears the clock control which in turn clears, or turns off the clock.

SERIALIZER

The counter is part of the serializer circuit. The counter provides binary count codes for the serializer. Through AND gates the codes enable up to nine gates (a start pulse and up to eight bits from the B register) one at a time in the serializer to provide the character format in table 1.

OUTPUT KEYER

Output pulses are sent to output relay puller P^{200}. A "zero" bit in the character from the computer produces a logical "1" signal in the LSOU and actuates the output relay in the test board unit. This breaks the line current causing a logical "zero" to be transmitted on the line. Through the output keyer the LSOU sends out the code character in start/stop serial form.

TABLE 1. ORDER OF SERIALIZED BITS (EIGHT-LEVEL)

COUNTER COUNT	SERIALIZER CONNECTION	DATA
1	1	"0" (START)
2	2	Bit 0 binary code
3	3	Bit 1 binary code
4	4	Bit 2 binary code
5	5	Bit 3 binary code
6	6	Bit 4 binary code
7	7	+ Bit 5 binary code
* 8	8	+ Bit 6 binary code
* 9	9	+ Bit 7 binary code
* 10	no connection	"1" (STOP)
* 11	no connection	"1" (STOP)

NOTES: * Stop pulse can be initiated on this count.

\+ These bits are selective, depending on the length of the character in effect.

CONTROL DATA
CORPORATION

CONTROL DATA 8536

HIGH-SPEED INPUT UNIT

Pub. No. 368 161 00 (10)

8536-A HIGH-SPEED INPUT UNIT

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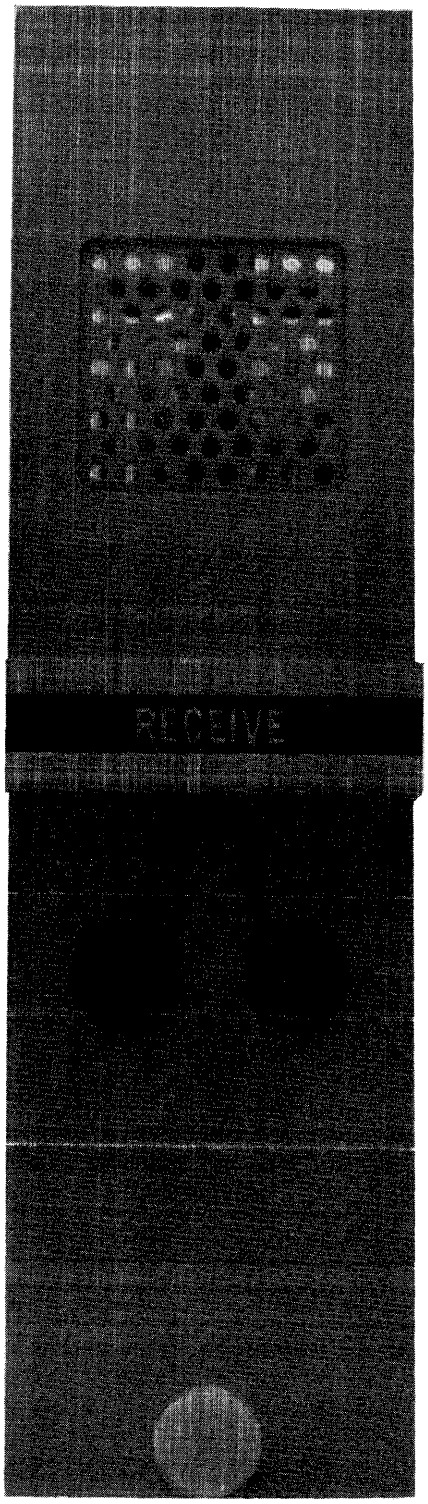
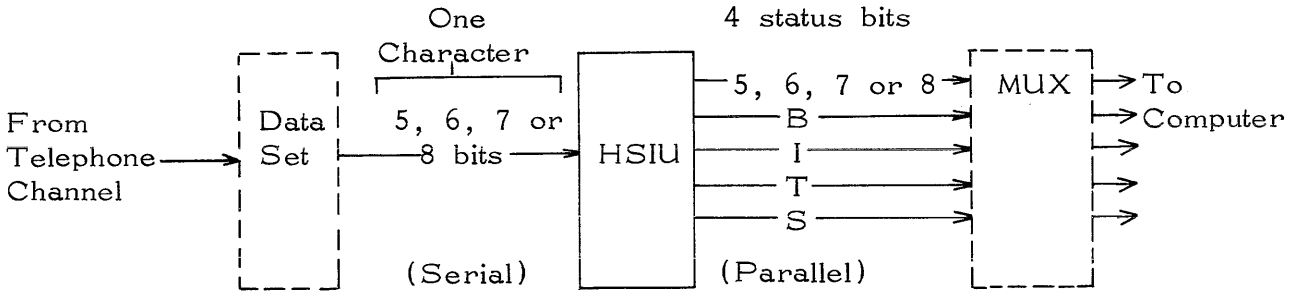


Figure 1. 8536-A High-Speed Input Unit

8536-A HIGH-SPEED INPUT UNIT

INTRODUCTION

The CONTROL DATA 8536-A High-Speed Input Unit (HSIU), figure 1, is a signal converter interposed between a DATA-PHONE communication channel and one input channel of an 8166-B Input Slave Multiplexer (Input MUX). The HSIU receives a message serially (one character bit at a time). It assembles each character and sends it in parallel form to the MUX. It notifies the operator of a broken or inactive line, or a lost character.



PANEL

The 8536-A display panel (figure 1) is actually the front surface of the 8166-B Input MUX. It contains the following lamps and switches:

MARK LAMP

This green lamp flickers while the HSIU is receiving a message. It lights every time a marking pulse is received. A steady green light indicates a steady marking signal (no characters are being received, although the HSIU and sending device are connected and turned on).

TEST LAMP

This red lamp lights when the OPER/TEST toggle switch is at TEST, warning the operator that the HSIU is in test condition and is inoperative.

BEHIND PANEL

Behind the panel are the following switches (figure 2).

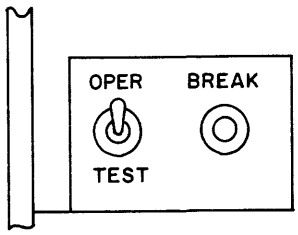


Figure 2. Switches Behind the Panel

OPER/TEST TOGGLE SWITCH

This switch must be at OPER during the normal receiving operation of the HSIU. The TEST position of the switch lights the red TEST panel lamp. This switch is used during maintenance checks or tests within the machine. Setting the switch at TEST starts the HSIU clock and counter. It may or may not set the registers depending on whether the BREAK button is pressed.

BREAK PUSH-BUTTON SWITCH

Pressing this button down sets all registers to 1. Conversely, if this button is not pressed all registers remain cleared. However, if the HSIU is not in the marking condition this button is ineffective.

LOGIC CARDS

Each HSIU fits into an 8166-B Input MUX like one of eight books on a shelf. The HSIU contains three parallel printed-circuit cards.

Card A contains the inverters, flip-flops (FFs) and other components of the clock and counter.

Card B contains the components that clear or shift the registers, plus the Character Lost, Break, and Idle FFs, and the clock control.

Card C contains the components of the clock control and the A and B register, and data output circuits.

The two outer cards are hinged at the rear for easy access.

CHARACTERISTICS

The HSIU performs the following functions (see figure 3):

1. It receives data characters serially one bit at a time in a start-stop Baudot code, or any code using five-, six-, seven- or eight-bit characteristics and any number of pulses from 7 to 11.

2. It drops the start (one bit) and stop (one, one and a half, or two bits) leaving just the required data bits.

3. It distributes the eight data bits of each character into the intermediate assembly register A.

4. It informs the computer through the 8166-B Slave MUX that a character is ready in parallel form (bit 11).

5. It reports a Character Lost in bit-9 position if the condition exists.

6. It reports a line break as well as an idle line or noncycling status. This status is inserted into bit-8 position by means of the 8166-B.

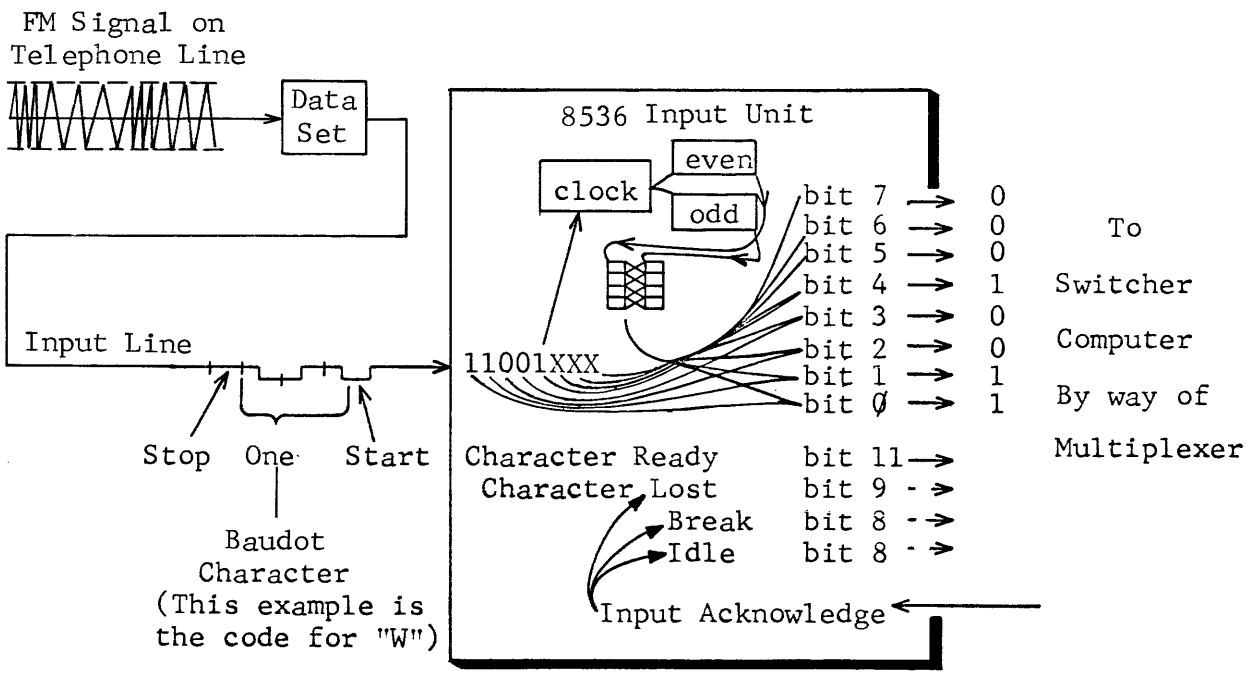


Figure 3. Path of Data Through an HSIU

GENERAL DESCRIPTION

An HSIU is an electronic receiving device compatible with teletypewriter communication codes, and speeds, and with DATA-PHONE data sets. It accepts Start/Stop signals as serial-bit pulses derived from an audio channel with a data receiver. These pulses are strobed to convert each incoming character to parallel data bits. The bits are stored in a transfer register for a maximum of one character period, awaiting withdrawal by the computer, by way of the MUX.

An HSIU is adjustable to accommodate data speeds of 60 to 1200 words per minute.

Like a teletypewriter printer, an HSIU responds to a start pulse. Whenever a start pulse is recognized, the internal clock executes the timing function for the serial-to-parallel convertsion, stopping at the predicted end of character to await the next start pulse.

The HSIU passes electrical signals on to the computer through the MUX. These signals are of two kinds; status codes and data characters.

STATUS CODES

The HSIU generates input status codes which are sent on signal lines to the computer through the 8166-B Input MUX and the Master MUX.

CHARACTER READY

The Character Ready signal tells the computer that a character has been assembled in the holding register and is ready to be withdrawn. The Character Ready is generated by the stop pulse after the last character bit enters the B register. The signal is sent to the 8165 Master MUX through the 8166-B Input MUX.

CHARACTER LOST

The Character Lost signal is sent to the switcher computer if the computer does not pick up a character before the next character arrives at the holding register. The new character will destroy the previous character.

BREAK

The Break signal indicates a break in line current from a remote station. It is sent to the computer if there is no Stop signal at the end of a character, but just one continuous spacing (absense of marking current). A Break signal is generated also if a remote station activates a break key. A Break signal is accompanied by an all-zero-bit character.

IDLE

The Idle signal is generated by R303 thermal relay. If the teletypewriter circuit is apparently intact, and no character is received for a specified period (5 to 10 seconds for example), the thermal relay sets the idle bit in the HSIU. See the paragraph on "Status Codes in the Logic Diagram" in this book.

Whenever the computer accepts a data/status word from the HSIU, it acknowledges the event with an Input Acknowledge signal that clears the HSIU status bits. Thus subsequent interrogations of the HSIU result in no new information until the next even (character arrival) occurs.

LOGIC DESCRIPTION

The HSIU receives a teletypewriter character in a start/stop code (see logic drawing no. 36755700 in pub. no. 368 165 00). The message comes in serially one bit at a time. A start pulse, or line-logic "0" causes the input circuit M301 to switch, producing a logical "1" output. The resultant logic "1" activates the internal circuit of the HSIU. After a half-start-pulse delay a "1" signal sets the clock control. The clock control sends out a "1" which starts the clock.

CLOCK

The clock of the HSIU is a free-running multivibrator. As it cycles it produces clearly separated even and odd pulses. When the clock FF is set, it sends a short pulse out through the even-clock circuit. When the clock is cleared it sends a short pulse ("1") to the odd-clock circuit. The clock cycles a preset number of times for each character (see figure 4). Then it is turned off by the stop pulse.

EVEN CLOCK AND ODD CLOCK

The alternating pulses from the even and odd clocks feed into the counter. The even clock enables the left rank FF of the counter to be set or cleared if other

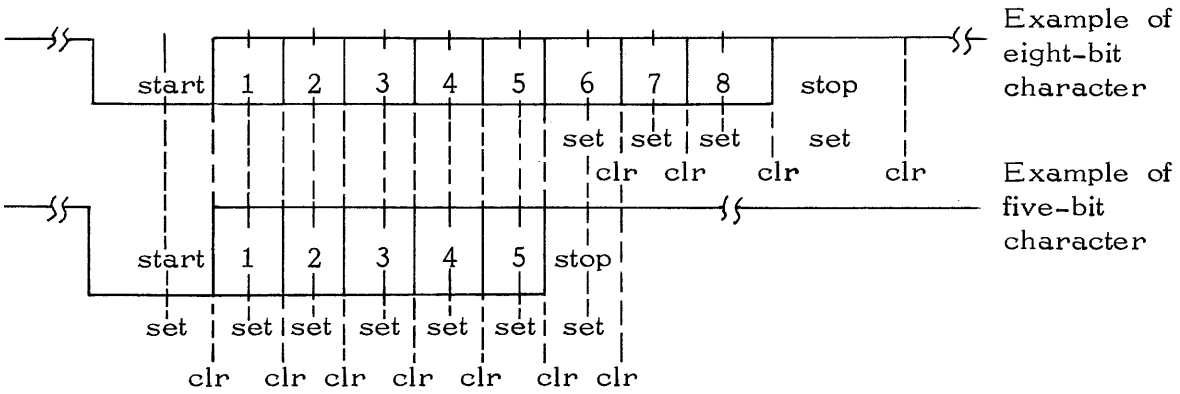


Figure 4. Clock Pulsing of Character

AND conditions are met. The odd clock transfers the count from left to right rank FF.

COUNTER

The left rank of the counter counts in binary. The right rank stores the count and gates the advance. The even/odd pulses alternate back and forth between the left and right ranks advancing the count by one, for each cycle. A preset count and the even-clock pulse clear the clock control, and stop the clock.

REGISTER A (STATICIZER)

The register A is loaded with eight data bits corresponding to the code character. The counter establishes the sequence of loading the register FFs. The clock provides the register-loading pulse. The isolation diodes of Z300 provide the identity ("1" or "0") of each bit of each character.

STOP PULSE

The stop pulse is energized by the even clock and by the counter at the desired count. It performs the following functions at the desired even-clock pulse:

1. It shifts the data from register A to register B.
2. It gates the Character Lost and Break Alarm Signal FFs.
3. It sets the Character Ready FF.

The stop pulse performs the following functions on the next odd-clock pulse:

1. It clears the clock control and stops the clock.

2. It clears the register A.

STATUS CODES IN THE LOGIC DIAGRAM

The Input Acknowledge signal from the computer clears the Character Ready, Character Lost and Break FFs. However, if the computer fails to acknowledge the character from register B before the next character arrives, the Character Ready FF will not be cleared. The Character Lost FF then will be set when the next character is assembled in the HSIU. The computer inserts a space character to replace the lost character.

If the communications circuit is disrupted and all the bits in register A are "1"s, the Break FF is set. This signal is sent by way of the MUX to the computer.

If one character is not followed by another within an interval controlled by thermal relay R303, the relay will send an Idle signal to the computer. The time delay which sets off the thermal relay is set at a length of time just longer than one character cycle.

The Break and Idle signal lines are joined into one line (bit 8) in the MUX. To test for Break or Idle, examine the input data. If the bits are not all "0"s the condition is idle. When all bits are "0"s the condition is Break.

CONTROL DATA
CORPORATION

CONTROL DATA 8537

HIGH-SPEED OUTPUT UNIT

Pub. No. 368 161 00 (11)

8537-A HIGH-SPEED OUTPUT UNIT

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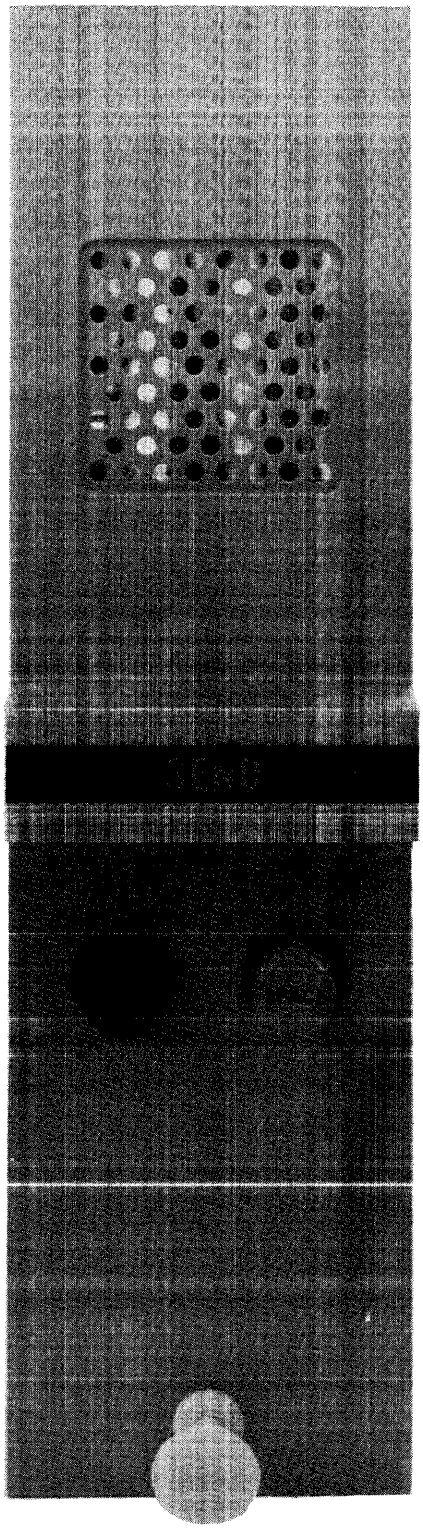
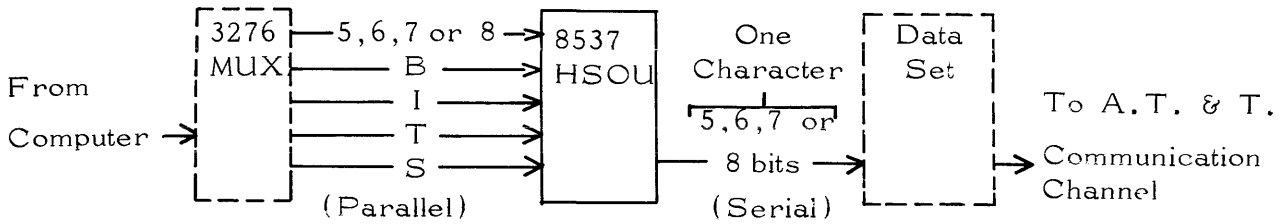


Figure 1. 8537-A High-Speed Output Unit

8537-A HIGH-SPEED OUTPUT UNIT

INTRODUCTION

The CONTROL DATA 8537-A High-Speed Output Unit (HSOU), figure 1, is a signal converter interposed between one output point on an 8167 Output Slave Multiplexer (Output MUX) and a DATA-PHONE communication channel (see example). The HSOU receives parallel-bit characters from the MUX. By means of a clock and counter, it sends the bits serially to the data set model circuit in the 10-unit, start-stop, teletypewriter code.



PANEL

The 8537-A HSOU control panel (see figure 1) mounts flush against the front surface of the 8167 Output MUX. It contains the following labeled lamps and switches:

SPACE LAMP

This white lamp flickers while the HSOU is sending a message. It lights every time there is a "space" pulse in the teletypewriter serialized character.

TEST LAMP

This red lamp lights when the OPER/TEST toggle switch is at TEST, warning the operator that the HSOU is in test condition and therefore inoperative.

BEHIND PANEL

Behind the panel on the right side are the following switches (see figure 2):

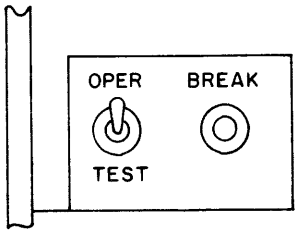


Figure 2. Switches behind the Panel

OPER/TEST TOGGLE SWITCH

This switch must be at OPER during the normal operation of the HSOU. The TEST position lights the red TEST lamp and sets the clock control which in turn starts the clock. This switch can be used during maintenance checks and tests.

BREAK PUSH-BUTTON SWITCH

When this button is pressed, it generates a "space" to the output circuit. It also lights the SPACE lamp.

LOGIC CARDS

Each HSOU fits into an 8167-B Output MUX like one of eight books on a shelf. The HSOU consists of three printed circuit cards.

Card A contains Transfer register A and Holding register B as well as the input circuits.

Card B contains the character serializer and counter.

Card C contains the clock, shift and clear circuits.

The two outer cards are hinged at the rear for easy access. Since the 8537-A HSOU is a pluggable unit, all logic signals, power, and output circuits enter through the 22-pin connector on the rear of the module.

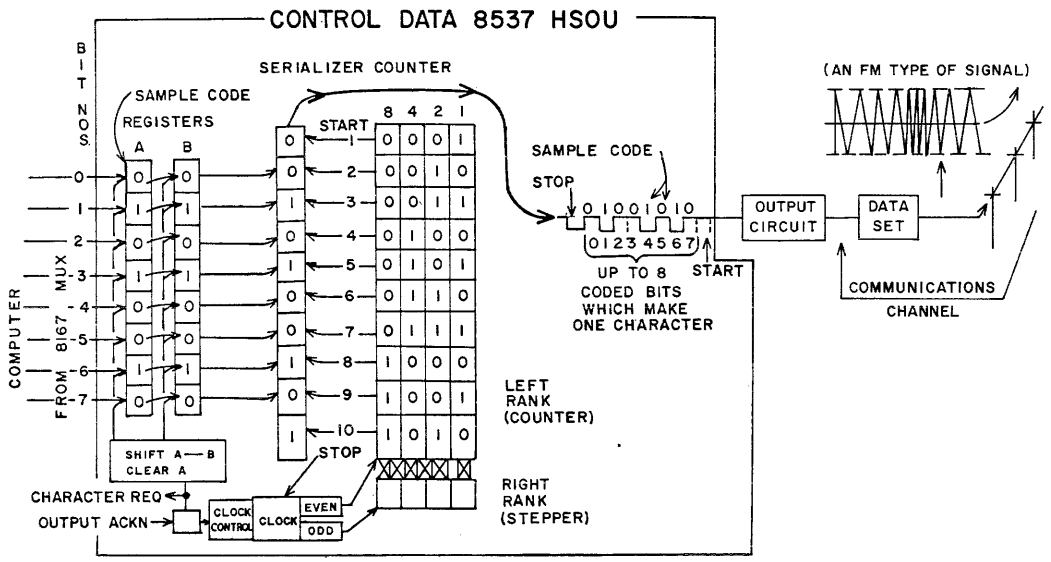


Figure 3. Data Path Through an HSOU

CHARACTERISTICS

The HSOU performs as follows (see figure 3) when it is connected to send a character:

1. It receives up to eight parallel data bits if Character Request is present.

2. Simultaneously it receives an Output Acknowledge signal. This enables the character to enter register A and cancels Character Request.

3. It shifts the character from register A to B (if the clock is stopped) and clears register A.

4. It requests the next eight-bit character by generating a Character Request signal.

5. It starts the multivibrator.

6. The clock counter gates the serializer.

7. The serializer is enabled by the counter and bit register sequentially, thereby regulating the consecutive order of the bits.

8. The output circuit sends the start/stop code to the data set input line, which in turn sends a modulated audio signal to the telephone line.

Each character in a 100-wpm (for example) system has a duration of 100 ms including start and stop pulses.

GENERAL DESCRIPTION

An HSOU is an electronic parallel-to-serial converter that is compatible with teletypewriter communication codes and speeds and with DATA-PHONE data sets. The 8537 HSOU accepts one parallel-bit character at a time by way of the MUX. Each character is stored in a register before it is "clocked out". A series of pulses is produced containing the data bits and the start and stop pulses required by the communications channel driven by the HSOU. An 8537-A HSOU can generate characters with five, six, seven, or eight information pulses. The clock is adjustable to provide output rates within the range of 60 to 1200 wpm.

An internal single-character register stores one eight-bit character in addition to the character undergoing parallel-to-serial conversions. For this reason, the computer has the time of one character cycle to repond to a Character Request from the HSOU while maintaining the maximum output rate.

An HSOU generates only one status code, Character Request. When the computer responds with Information Ready, the MUX enables the data character and Output Acknowledge to be sent to the HSOU. This event causes the Request to drop and the serializing function to start in the HSOU. If no character is transferred with the acknowledgement, a blank character is generated and sent by the HSOU. Failure of the computer to acknowledge a Request merely extends the stop pulse.

LOGIC DESCRIPTION

When the HSOU is not sending data the line driver L200 is in the off condition (-) (see logic diagram No. 36755800 in pub. No. 368 165 00). The communication channel is an audio circuit. A marking frequency passes through the circuit until the start pulse of a character reaches the line driver L200, which switches ON (+) causing the data set to change its output to the spacing frequency.

When a character passes through the HSOU, the eight bits reach the HSOU in parallel, in external voltage levels ("1" = -0v, "0" = -16v). Each bit passes through an M card and is converted to internal voltage levels ("1" = -3.5v, "0" = nominal 0v).

OUTPUT ACKNOWLEDGE

Whenever an HSOU receives a character from the computer, it also receives an Output Acknowledge signal. The Output Acknowledge is a logic "1" signal which has the following functions within the HSOU:

1. It enables the data character to enter register A.

2. It sets the flip-flop (FF) A216/A217 which in turn gates the clock control K200/K201.

CLOCK CONTROL (STARTS AND STOPS THE CLOCK)

With the clock stopped between data characters, the outputs inverter I200 and N203 are "1"s. These "1"s are gated with the "1" from A217 to set the clock control FF K200/K201.

When the clock control is set it does the following:

1. It enables a 19-usec pulse to enter the register control (shift (A)$\longrightarrow$B), and after 6 usec more, clears A.

2. It enables a 19-usec pulse which starts the clock on the even pulse.

3. It enables the clock to cycle at a frequency regulated by two adjustable delay cards. Each delay is set to 1/2-bit pulse duration.

REGISTER CONTROL

The register control has these main purposes:

1. To shift the contents of register A into register B at the same time that the clock starts.

2. To clear register A, 6 usec after (A) has been shifted to B.

3. To enable the next Character Request to be sent to the 8165 MUX.

CLOCK

The clock of the HSOU is a free-running multivibrator. As it cycles it produces clearly separated even and odd pulses. When the clock is set it sends a short

pulse ("1") out through the even-clock slaves. When the clock is cleared it sends a short pulse ("1") through the odd-clock slaves. The clock cycles a preset number of times for each character (see figure 4). These pulses act to set and shift the counter FFs and to clear the clock control after the last data bit. The clock control in turn stops the clock.

EVEN CLOCK AND ODD CLOCK

The alternating pulses from the even and odd clocks feed into the counter. The even clock enables the left rank FFs of the counter to be set or cleared if other AND conditions are met. The odd clock transfers the count from left to right FFs. The even and odd clocks send pulses alternately to the left and right ranks of the counter.

COUNTER

The left rank of the counter counts in binary. The right rank stores the count and gates the advance. The even/odd pulses alternate back and forth between the left and right ranks advancing the count by one for each cycle. The counter counts up to 12 as a maximum. A predetermined count, with odd or even clock, clears the clock control which in turn clears, or turns off the clock.

SERIALIZER

The counter is part of the serializer circuit. The counter provides binary count codes for the serializer. Through AND gates the codes enable up to nine gates (a start pulse and up to eight bits from the B register) one at a time in the serializer to provide the character format in table 1.

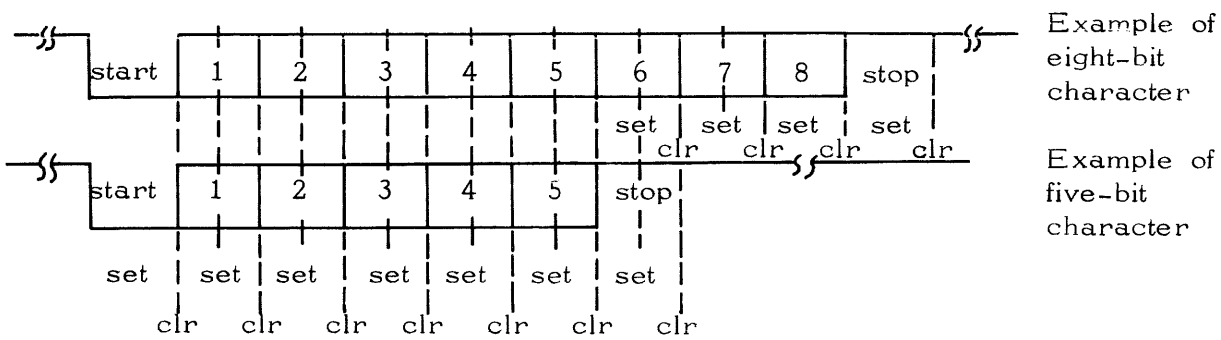


Figure 4. Clock Pulsing of a Character

OUTPUT

Output pulses are sent to output line driver L200. A "zero" bit in the character from the computer produces a logical "1" signal in the HSOU serializer and actuates the output line driver to generate a (=) "b" signal. The data set detects the (=) potential and switches to spacing frequency (= logical zero). Through the output line driver the HSOU sends out the code character in start/stop serial form.

TABLE 1. ORDER OF SERIALIZED BITS (EIGHT-LEVEL)

COUNTER COUNT	SERIALIZER CONNECTION	DATA
1	1	"0" (Start)
2	2	Bit 0 binary code
3	3	Bit 1 binary code
4	4	Bit 2 binary code
5	5	Bit 3 binary code
6	6	Bit 4 binary code
7	7	+ Bit 5 binary code
*8	8	+ Bit 6 binary code
*9	9	+ Bit 7 binary code
*10	no connection	"1" (Stop)
*11	no connection	"1" (Stop)

NOTES: * Stop pulse can be initiated on this count.

\+ These bits are selective, depending on the length of the character in effect.

CONTROL DATA
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CONTROL DATA 8908

LOW-SPEED INPUT/OUTPUT UNIT TESTER

Pub. No. 368 161 00 (09)

8908-A LOW-SPEED INPUT/OUTPUT UNIT TESTER

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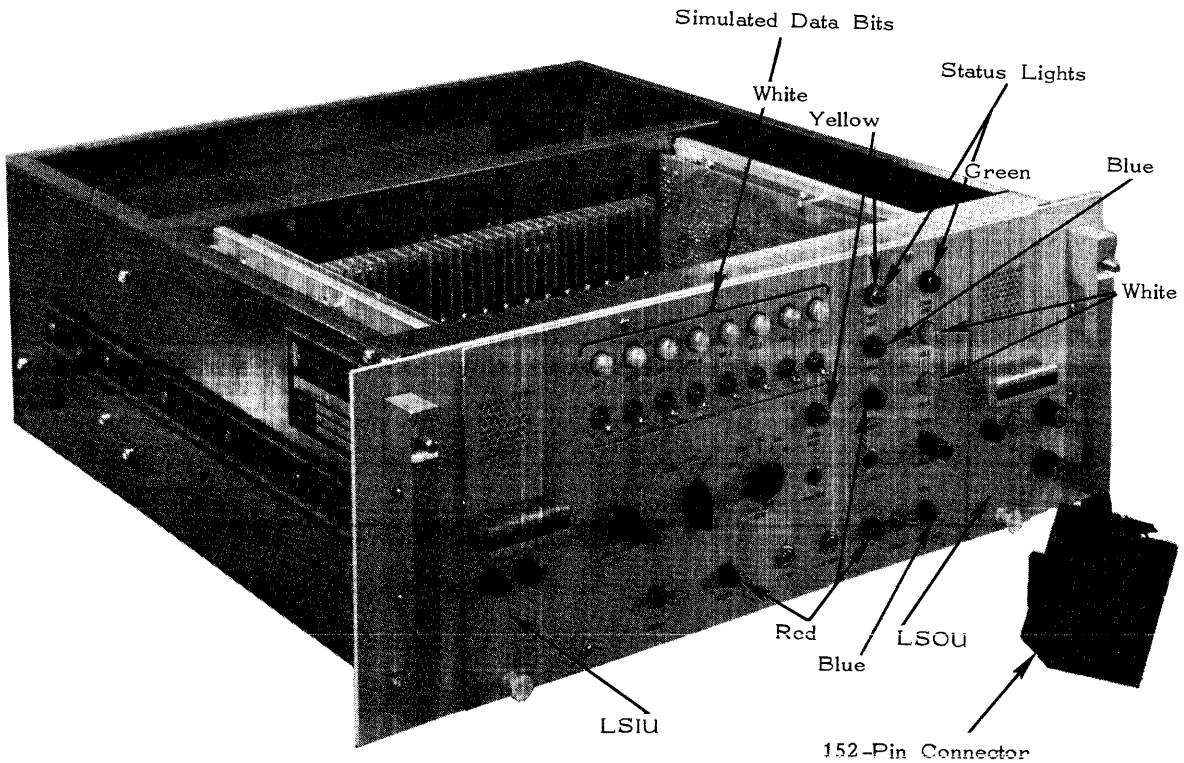

Figure 1. 8908-A Low-Speed Input/Output Unit Tester

8908-A LOW-SPEED INPUT/OUTPUT UNIT TESTER

INTRODUCTION

The CONTROL DATA 8908-A Low-Speed Input/Output Unit Tester (8908-A Tester) provides a testing facility for the LSI/O units in the 8050 Information Control System. The 8908-A Tester simulates the operation of an LSI/O unit in a multiplexer (MUX) cabinet.

DESCRIPTION

The 8908-A Tester is built into a standard-size drawer of the 3276 MUX cabinet (figure 1). Controls and indicators for operation of the 8908-A Tester are located on the front panel. A mounting facility for one LSOU and one LSIU is provided at the front panel.

PHYSICAL CHARACTERISTICS

The tester is completely self-contained, except for dc power. The standard 152-pin connector provides only the ±20-volt dc power to the Tester logic from the MUX cabinet. If the Tester is bench-mounted, any laboratory power supply of proper voltage and current capacity can be substituted. Table 1 lists the dimensions, power requirements and cooling requirements of the 8908-A.

TABLE 1. 8908-A PHYSICAL CHARACTERISTICS

Dimensions:	
Height	8-11/16 inches
Width	24-7/8 inches
Depth	23-5/16 inches
Power Requirements (including LSIU and LSOU):	+20 vdc at 1 amp -20 vdc at 4 amp
Cooling Requirements (including LSIU and LSOU):	340 Btu/hr

ENVIRONMENTAL CHARACTERISTICS

Table 2 lists the environmental characteristics of the 8908-A.

TABLE 2. 8908-A ENVIRONMENTAL CHARACTERISTICS

Operating Environment:	
Temperature Range	+32° to +110°F
Relative Humidity	10 to 90%
Storage and Shipping Environment:	
Temperature Range	-40° to +150°F
Relative Humidity	10 to 90%

FUNCTIONAL DESCRIPTION

The following logical circuits are provided as a part of the 8908-A Tester.

Clock

The clock provides Interrupt signals (Acknowledge signals) to the LSI/O unit to simulate those provided by the 8050 System. Clock rates are:

a. 1050 wpm, 9 ms (used only with 8536 and 8537)

b. 150 wpm, 63 ms

c. 100 wpm, 90 ms

d. 75 wpm, 126 ms

e. 66.5 and 60 wpm at 126-ms rate

The clock uses an improved unijunction pulse circuit.

Counter

The counter is used to divide the basic 9-ms repetition rate of the clock into slower word rates. No clock adjustment is required after initial setup at the 9-ms repetition rate.

Character Generator

The character generator generates two alternate Teletype characters for transmission to the LSOU. These characters of alternate ones and zeros force the LSOU registers to alternately set and clear, and allow for oscilloscope testing of the register action.

Character Fail Circuit

When the character generator is active, the character fail circuit is also made active to give a visual indication any time the LSI/O unit loop fails to accurately transmit the proper character. The Character Fail flip-flop (FF) is manually cleared each time a failure is observed.

Visual Indicators

A lamp is provided for each data and status bit location to indicate whether the LSI/O unit loop is active. The lamps indicate whether alternate LSI/O unit characters are being properly transmitted.

Transmitter Distributor (TD) Input

A ground loop is provided at the LSIU input, through a closed-circuit phone jack, to allow for transmitting punched paper-tape messages through the LSIU from a TD. When the TD input is not used, the LSOU output drives the LSIU input.

Receive-Only (RO) Monitor Output

A 60-ma current source is provided at the LSOU output, through a closed-circuit phone jack, to allow for connecting an RO Teletype monitor at this point. The use of the monitor loop in no way affects any other function of the 8908-A Tester.

LSOU Output Circuit

The output circuit of the 8509-A LSOU has been modified by removing the relay from the LSOU and substituting one in the test board unit. The resulting module is an 8509-B. The 8908-A Tester incorporates a relay in such a manner that either the A or B module can be properly tested without the need for switching.

OPERATION

This section divides the 8908-A operating instructions into three parts that correspond to the three possible testing modes. In general, the technician must do the following things.

1. Plug an LSIU into the left side of the Tester and an LSOU into the right side of the Tester. One of the two units must be known to be in good working order. The pair of units must be of the same speed and character length.

2. Plug an RO monitor teleprinter into the Tester which has a speed and format that matches the pair of units in the Tester.

3. Set the POWER switch to ON. Both the +20 V and -20 V indicators should light.

An OUTPUT TEST POINT terminal on the Tester allows the technician to measure the local loop line voltage at the output of the LSOU.

MANUAL (MAN) MODE

In this mode the parallel character code corresponding to the MANUAL SET switch settings is placed on the data lines that run to the LSOU. The LSOU samples the lines and converts the signal into a serialized teleprinter code at a rate determined by the operator's use of the MAN ACK switch. The serialized teleprinter codes simultaneously operate the RO monitor and feed the input line of the LSIU. The LSIU reconverts each serialized teleprinter code into a parallel computer code and returns it to the Tester. The code for a character, bits 0 through 8, is represented by lights above the MANUAL SET switches. These switches remain lit until the next character is transmitted by the LSOU.

The switches used in this mode and their correct positions are:

MODE	Set to MAN.
MANUAL SET	Set to desired code.
SPEED	Set to LO for 8508 and 8509, or 8518 and 8519. Set to HI for 8536 and 8537.
CHAR LENGTH BITS	Set to correspond to character length of five, six, seven, or eight bits.

CLOCK RATE WPM	Set to 1050, 150, 100 or 75 to send the MANUAL SET character over the local loop at the proper clock rate. Set to OFF to use the MAN ACK switch.
MAN ACK	Push to transmit a MANUAL SET character over the local loop connecting the Tester and LSI/O units.
CLEAR	Push to clear Character Lost, Break or Character Fail FFs.

The indicators used in this mode and their meanings are:

MANUAL SET (bits 0 throu 7)	The bits which are lit should correspond to the MANUAL SET switch settings if both units are operating correctly.
CHAR RDY	Indicates that data is present at the interface of the LSIU and Tester.
CHAR LOST	Indicates that LSIU has sent a character to the Tester, but did not receive a response (MAN ACK).
BREAK	Indicates that the LSIU has detected a character consisting of all zeroes (an illegal character).
IDLE	Indicates that 5 seconds have passed since a character was received by the LSIU.
CHAR RQST	Indicates the LSOU is prepared to receive a character from the Tester.
SPACE	Indicates that the line loop current is zero.

AUTOMATIC (AUTO) MODE

In this mode the Tester alternately generates the codes for characters R and Y, five-bit character length, or J and 5 for six-, seven, or eight-bit character lengths. The parallel codes from the character generator are gated to the LSOU which converts the signal into a serialized teleprinter code that operates the RO monitor and feeds the input line of the LSIU. The LSIU reconverts each serialized teleprinter code into a parallel computer code and returns it to the Tester. The Tester senses each incoming character for a loss or gain of bits, and sets the Character Fail FF.

The switches used in this mode and their correct positions are:

MODE	Set to AUTO.
MANUAL SET	Must all be set to "0".
SPEED	Set to LO for 8508 and 8509, or 8518 and 8519. Set to HI for 8536 and 8537.
CHAR LENGTH BITS	Set to correspond to character lengths of five, six, seven, or eight bits.
CLOCK RATE WPM	Set to 75, 100, or 150 wpm for 8508 and 8509, or 8518 and 8519. Set to 75, 100, 150, or 1050 wpm for 8536 and 8537. Set to OFF for using MAN ACK with all LSI/O units.
MAN ACK	Push to manually step the Character Generator and transmit a character over local loop in the Tester.
CLEAR	Push to clear Character Lost, Break or Character Fail FFs.

The indicators used in this mode and their meanings are:

CHAR RDY	Indicates that data is present at interface of LSIU and Tester.
CHAR LOST	Indicates that the LSIU has sent a character to the Tester, but did not receive a response (MAN ACK or clock pulse).
BREAK	Indicates that the LSIU has detected a character consisting of all zeroes.
IDLE	Indicates that 5 seconds have passed since a character was received by the LSIU.
CHAR RQST	Indicates the LSOU is prepared to receive a character from the Tester.
SPACE	Indicates that the line loop current is zero.
CLOCK	Indicates that the clock is running.

TD MODE

In this mode a TD and RO monitor are plugged into the Tester. The serialized codes from the TD go to the LSIU which converts each serial code into a parallel computer code and returns it to the Tester. The Tester gates each parallel code directly to the LSOU which reconverts the signal into a serialized teleprinter code that operates the RO monitor.

The switches used in this mode and their correct positions are:

MODE	Set to TD.
MANUAL SET	Must all be set to "0".
SPEED	Set to LO for 8508 and 8509, or 8518 and 8519. Set to HI for 8536 and 8537.
CLOCK RATE	Set to rate corresponding to that of TD and RO monitor.
CLEAR	Push to clear Character Lost, Break, or Character Fail FFs.

The indicators used in this mode and their meanings are:

CHAR RDY	Indicates that data is present at interface of the LSIU and Tester.
CHAR LOST	Indicates that LSIU has sent a character to the Tester, but did not receive a response (INPUT ACK).
BREAK	Indicates that LSIU has detected a character consisting of all zeroes.
IDLE	Indicates that 5 seconds have passed since a character was received by the LSIU.
CHAR RQST	Indicates that the LSOU is prepared to receive a character from the Tester.
SPACE	Indicates that line loop current is zero.

THEORY OF OPERATION

CLOCK

Figure 2 shows the flow of signals between the LSI/O units and the 8908-A Tester.

The clock C100/C101 is made up of a unijunction logic card (G-83) which provides proper timing pulses through the action of a unijunction transistor. The circuit is relatively insensitive to voltage variations.

With the CLOCK RATE WPM switch at OFF, a ground (logical zero) is at C100. This prevents the clock from pulsing. Turning the CLOCK RATE WPM

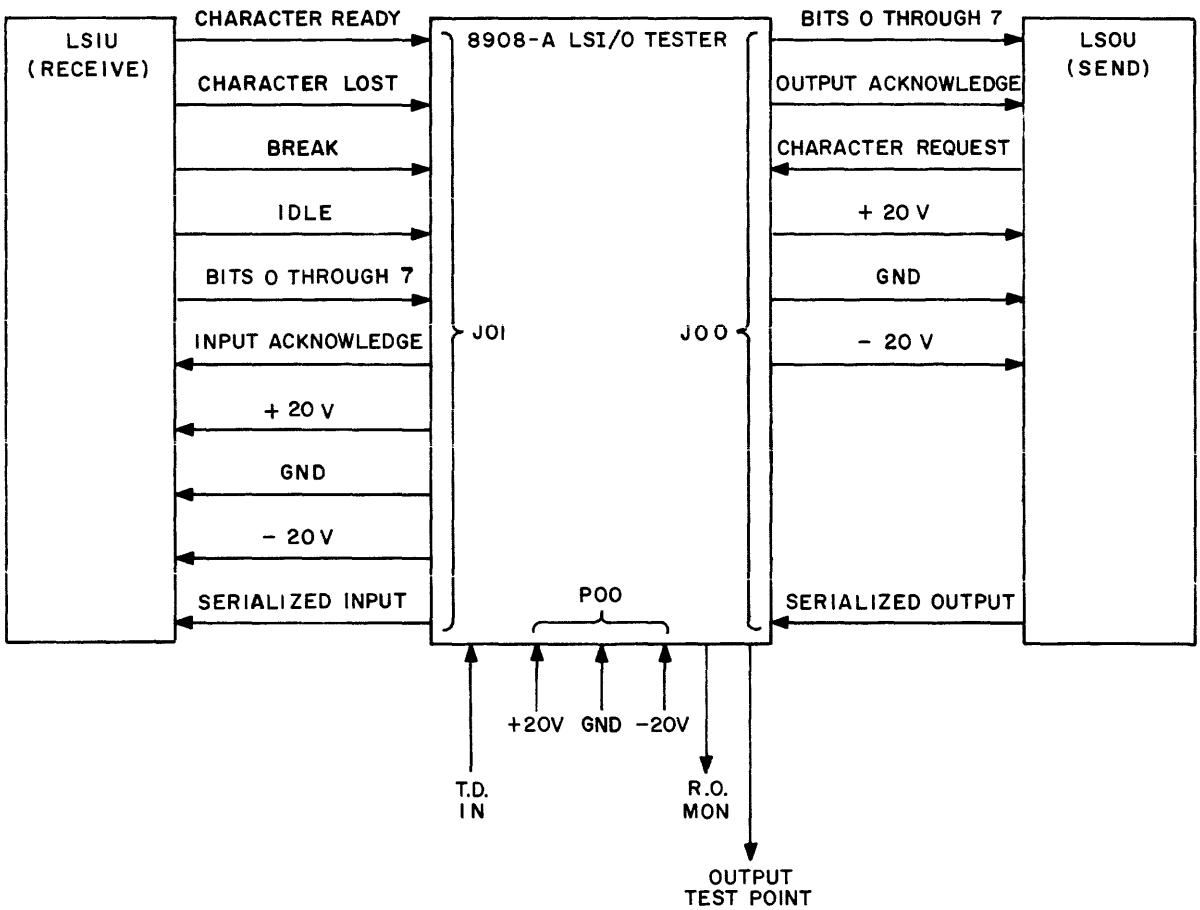

Figure 2. Signal Flow between LSI/O Units and 8908-A Tester

switch to a selected words-per-minute rate places an open circuit (logical one) into C100 and causes the clock to pulse. The clock is adjusted for a repetition rate of 9 ms, which is the fastest interrupt rate for high-speed MUX operation. This rate corresponds to 1050 words per minute. Clock pulses are logical "1" of approximately a 50-usec duration.

The counter, S100 through S115, allows the use of one standard clock frequency for all applications by dividing the standard to slower repetition rates. At 1050 wpm the clock provides pulses every 9 ms without modification. This corresponds exactly with the acknowledge rate in a high-speed MUX cabinet.

For 150-wpm operation (66.67-ms character length) every seventh clock pulse is enabled to give a 63-ms sample rate. The left rank of the counter is stepped at each clock pulse via I104 and I105. The advance to the right rank is delayed 6 usec after the drop of the clock pulse via D100. A 19-usec pulse is generated via I100/I102/I101 and I100/I102/I106, and their associated delays. At the count of 7, S103, S107 and S111 enable I108 to generate a reset pulse into the left rank of the counter. Since the 19-usec advance pulse has not yet dropped, the reset condition will be advanced to the right rank. As the right-rank FFs are reset, D103 acts to maintain the reset pulse for 6 usec.

Since the right rank of the counter has been driven to the reset (zero) condition, the input to I111 is now enabled except for the output of I110. When the clock again pulses, the I111 AND gate is completed, and a clock pulse is transmitted via I112/I113. Concurrently the counter again starts its count toward 7. (Note that the count of 7 automatically returns the counter to zero. The count of zero enables the next clock pulse.)

The above operation is also true for 100-wpm and 75-wpm operation. At the 100-wpm rate (100-ms character length, 90-ms sample rate) every tenth clock pulse resets the counter; S107 and S115 enable the I108 input. At the 75-wpm rate (133-ms character length) every 14th clock pulse resets the counter, to provide a 126-ms sample rate; S107, S111 and S115 enable the I108 input.

CHARACTER GENERATOR

FF K100/K101 and its associated inverters I114, I115, I116, and I117, generate code characters to be applied to an LSOU in parallel form. The characters are applied to L100 through L107 and then to the input of the LSOU. The characters are alternately R and Y, R and Y (Baudot), or J and 5 (eight-level).

These characters are made up of alternate binary digits, and can be used to force the LSOU registers to constantly change condition for easy testing. Any register FF which is sluggish, or fails to switch properly can be checked with an oscilloscope.

Depending upon its current state, FF K100/K101 is either set by inverters I113 and I117 or cleared by inverters I113 and I116. A "1" output from I113 depends upon a clock pulse via I111 and simultaneously a CHAR RQST input via I136. Consequently, the circuit will not present the same character twice in succession to the output LSOU, nor will it change character until the LSOU is clearly ready for a change.

D104 and D105 delay for 25 usec a change to a "1" at the input to I114 or I115, thereby inhibiting a change in the FF or in the character pattern for the duration ot the clock pulse. D106 and D107 give the same result by delaying the complement of the above change at the input to I116 or I117.

MANUAL SELECTION

The MAN position of the MODE switch (S8) allows the operator to test individual bit positions more closely or at a manually induced rate. The MANUAL SET switches (S0 through S7) are enabled by setting the MODE switch to MAN. With the switch in this position, inverters I116 and I117 outputs are held at logical "0" and any desired character pattern may be set up using the MANUAL SET switches.

During manual operation, acknowledge pulses can be generated by the clock at the normal rate for the LSI/O unit under test or the CLOCK RATE WPM switch (S9) can be set to OFF and the acknowledge pulses generated manually by pressing the MAN ACK switch (S11). Inverters I135 and I134 will generate only one pulse each time the MAN ACK switch is pressed.

CHARACTER FAIL CIRCUIT

The CHAR FAILURE lamp (DS14) is lighted via P102 any time the Character Fail FF K108/K109 is set. This FF is manually cleared by pressing the CLEAR switch (S10). It is locked in the clear condition by inverter I119 any time the MODE switch (S8) is set to TD.

The character pattern from the character generator is transmitted via M100 through M107 to either the set or clear input of FF K106/K107. The character

pattern is gated by the acknowledge clock pulses from I112. The FF alternately sets and clears as the character changes following a 25-usec delay.

Both the set and clear outputs from FF K106/K107 are fed to the set inputs of K108/K109 after a delay of 37 usec. The inputs to this FF are gated by the acknowledge clock pulse (I112) and character ready pulse (M108). The total of the delays into the two FFs exceeds the duration of a clock pulse preventing FF K108/K109 from setting after FF K106/K107 changes state. If FF K106/K107 fails to switch, FF K108/K109 will set and the CHAR FAILURE lamp (DS14) will light indicating the failure.

TRANSMITTER DISTRIBUTOR INPUT

Setting the MODE switch S8B-3 to TD connects the closed-circuit phone jack J-03 to the LSIU at LSIU connector pin J01-W. The output of a punched paper-tape transmitter distributor can be plugged into this jack and taped messages sent into the LSIU.

The make/break characteristics of the trasmitter-distributor output energizes the input circuit of the LSIU.

With the MODE switch (S8) at TD, the inputs of inverters I118 and I119 are grounded. Since the resulting logical "1" output from these inverters enables the inputs of L110 through L117, the parallel characters assembled in the LSIU are transmitted to the LSOU. A teleprinter monitor can be used to print out the test messages.

RO MONITOR

Closed-circuit phone jack (J-02) provides a 60-ma current source to drive the input circuit of a teleprinter monitor. Relay R100 modulates the current at the teleprinter character rate. Z-100 is a filter and arc suppressor.

The resistance of the input coil of the teleprinter is approximately 180 ohms. When the monitor plug is inserted into J-02, the closed-circuit jack opens the contacts to a 180-ohm, 2-watt resistor, and substitutes the relay coil. No other circuit is affected by the use of the monitor. A 470-ohm potentiometer is available to adjust the current to the proper value.

CHARACTER LENGTH

The CHAR LENGTH BITS switch (S13) assures action of the character fail circuit under conditions of short character length. This switch grounds out any unused bits at the inputs to various inverters preventing malfunction of the switching action of FF K106/K107.

INDICATORS

Indicator lamps are provided (on the 8908-A Tester panel) which indicate circuit functions and failures. The indicators and their functions are as follows:

1. Character Bit (MANUAL SET) Indicators (DS0 through DS7) - These lamps are driven by output cards in the LSIU and they indicate that the associated binary digit is set.

2. CHAR RDY Indicator (DS8) - Lights when a signal is generated in the LSIU when a character is acquired by the output holding register.

3. CHAR LOST Indicator (DS9) - Indicates that a character is placed in the ouput holding register of the LSIU and not acquired by the computer before the next input character is received.

4. BREAK Indicator (DS10) - Indicates a circuit failure that results in loss of line current.

5. IDLE Indicator (DS11) - Indicates that the LSIU has not received a data character for a predetermined period, usually several character lengths.

6. SPACE Indicator (DS12) - Activated by actions of line relay (R100).

7. CLOCK Indicator (DS13) - Indicates the clock is active. The indicator is lighted by P103 via the clock divider logic from S101.

8. CHAR FAIL Indicator (DS14) - Indicates a character failure from the character failure circuit.

9. CHAR RQST Indicator (DS15) - Signal generated in the LSOU when a character has been shifted from the transfer register to the holding register. Indicates that LSOU is prepared to receive next character.

10. +20 V and -20 V Indicators - Indicate that +20 and -20 volts dc are present, that the POWER switch (S14) is ON, and that fuses F1 and F2 are functional.

CONTROL DATA
CORPORATION

CONTROL DATA 8909-D/E
TEST BOARD UNITS

Pub. No. 368 161 00 (01)

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TEST BOARD UNITS

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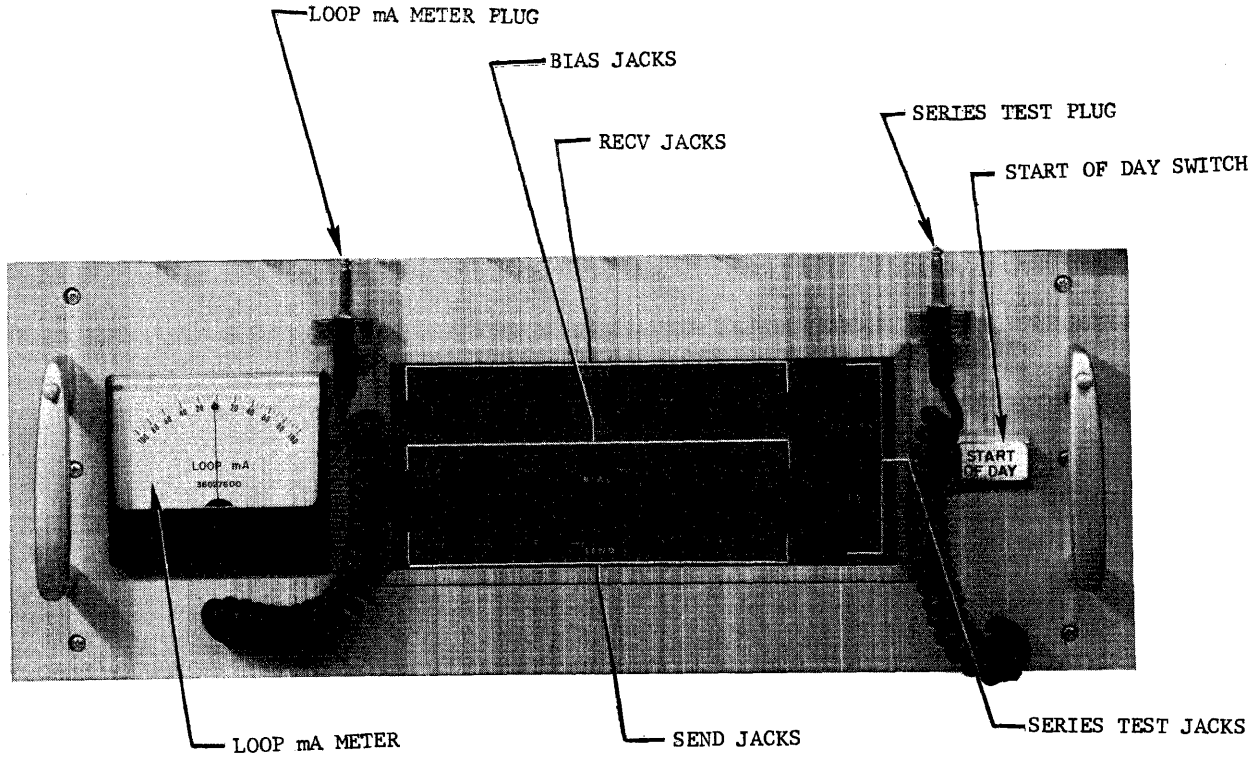


Figure 1. 8909-D01 Test Board Unit

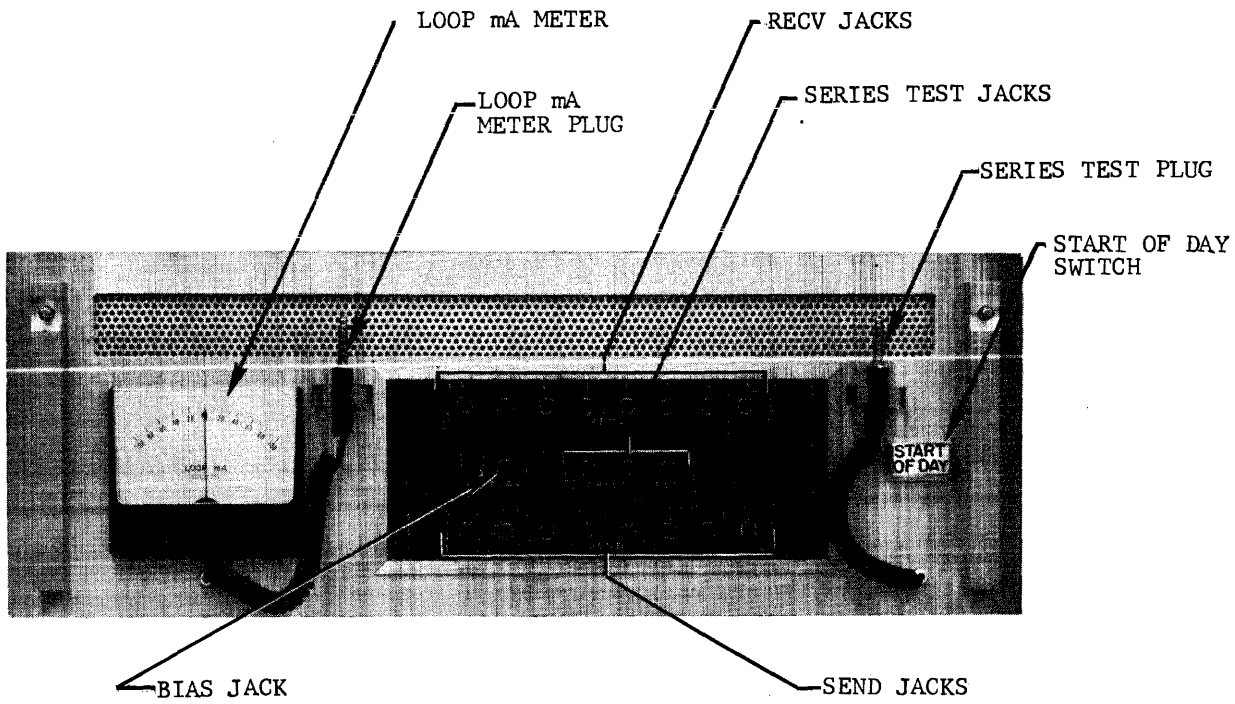


Figure 2. 8909-E02 Test Board Unit

8909-D AND 8909-E
TEST BOARD UNITS

GENERAL

The CONTROL DATA 8909-D and 8909-E Test Board Units (figures 1 and 2) are drawer-type modules used with a multiplexer cabinet. The 8909-D is designed to be installed in the 8076 Multiplexer cabinet (8461-A). The 8909-E is installed in the 3276-A Communication Terminal Controller cabinet (8461-B). The two Test Board Units are generally, physically, and electrically identical except for the cabinet latching mechanisms necessary to install the units in the applicable cabinets. Table 1 lists specific differences between individual Test Board Unit models.

The 8909-D and 8909-E are used in those systems with a maximum of eight receive and eight send teletypewriter signal lines (figure 3). The primary function of the Test Board Unit is to provide circuit isolation between low-speed high-voltage teletypewriter signal lines and the system multiplexer (MUX) logic circuits. This isolation is accomplished by the use of relays in both the send and receive circuits.

SUMMARY OF CHARACTERISTICS

PHYSICAL CHARACTERISTICS

Height:	8-11/16 inches
Width:	24 inches
Depth:	23-1/4 inches
Weight:	30 pounds

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature:	+32° to +110°F
Operating Relative Humidity:	10 to 90 percent
Storage Temperature:	-20° to +150°F
Storage Relative Humidity:	10 to 95 percent
Heat Dissipation:	negligible

TABLE 1. TEST BOARD UNIT MODEL DIFFERENCES

TEST BOARD UNIT	CABINET MOUNTING	NO. OF BIAS JACKS & BIAS RHEOSTATS	LINE CURRENT POWER SUPPLY PLUG-IN CAPABILITY	* PWR REQ
8909-D01	8461-A	8	No	+20,-20
8909-D02	8461-A	1	Yes	-20
8909-E01	8461-B	8	No	+20,-20
8909-E02	8461-B	1	Yes	-20

NOTE: * Power requirements are all vdc.

DESCRIPTION

The Test Board Units mount in their respective MUX cabinets by means of standard cabinet latching mechanisms. The handles on each side of the cabinet contain a latch release button. Pressing these buttons releases the latching mechanism and allows the unit to slide out of the cabinet. The panel of the unit contains the following switches, meters, and jacks:

The LOOP mA meter is used to determine proper magnitude and polarity of low-speed teletypewriter signal current and relay bias current.

The RECV jacks are used to monitor input (received) signals on the low-speed teletypewriter signal lines.

The BIAS jacks are used to monitor bias current to receive relays.

The SEND jacks are used to monitor output (sent) signals on the low-speed teletypewriter signal lines.

The SERIES TEST jacks are used to connect multiple external test equipment to monitor either input or output lines.

The START OF DAY switch is used to enable the output relays after equipment is first turned on for the day.

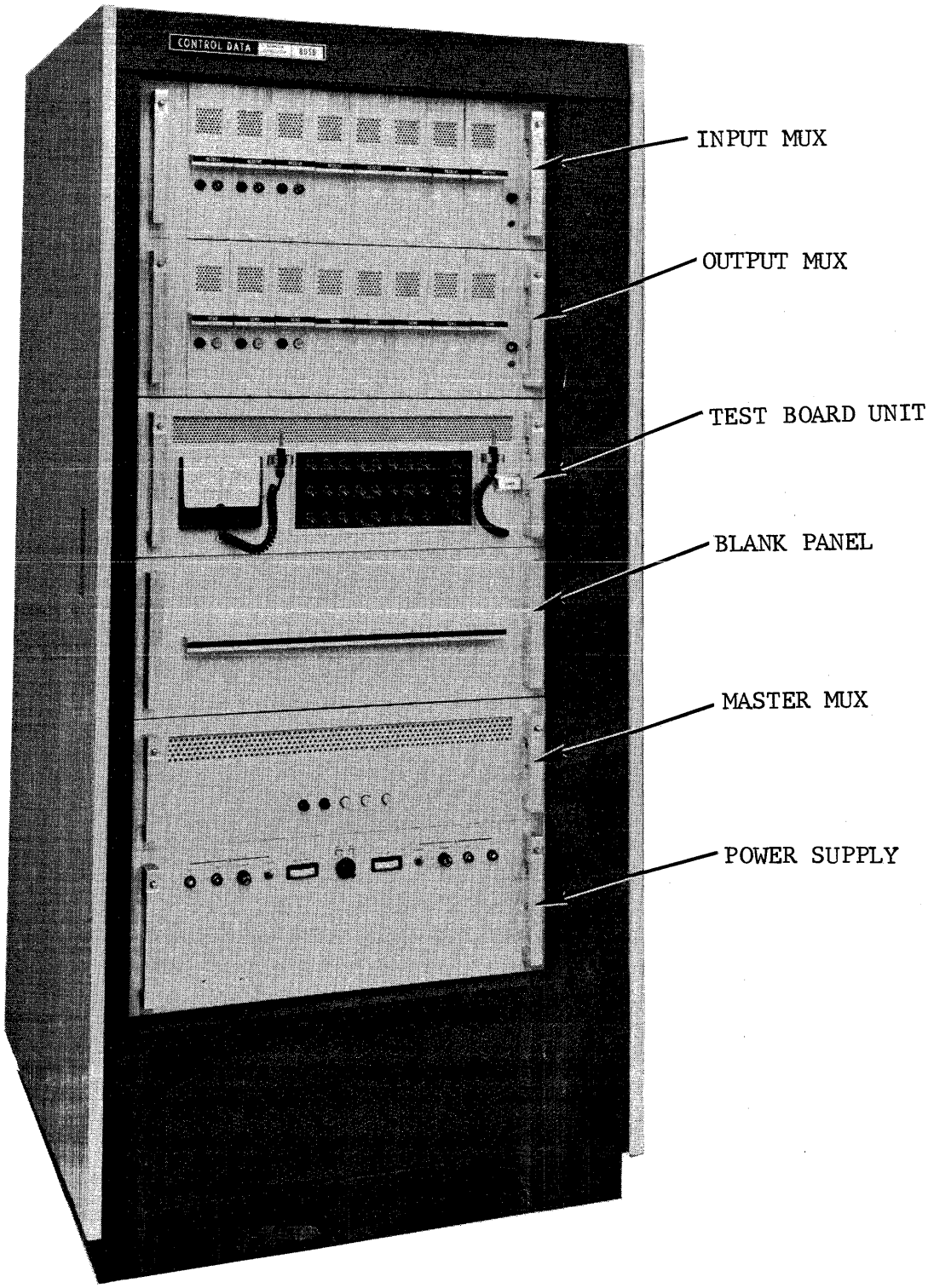


Figure 3. Typical Test Board Unit Installation (8909-E01)

INSTALLATION

INTERCONNECTION

The Test Board Units mount in their respective MUX cabinets using standard drawer latching mechanisms. Figure 4 is an interconnecting diagram illustrating the interconnection of the Test Board Unit, the MUX cabinet, and the teletypewriter equipments. The 8909-E connects to the MUX cabinet by standard 24-pair, input/output logic cables. These cables are connected from connectors J100 and J101 on the 8909-E to Input MUX rack assembly connector J201 and Output MUX rack assembly connector J201. Power is connected to terminal board 3 on the 8909-E from terminal 12 on the MUX cabinet. The 8909-E01 requires both +20 and -20 vdc and the 8909-E02 requires only -20 vdc.

The 8909-E connects to the MUX cabinet by standard 24-pair, input/output cables. These cables are connected from connectors J100 and J101 on the 8909-E to connectors JM100 and JM101 on the 8461-A cabinet. Connectors JM100 and JM101 are mounted on the terminal board rack on the top of the cabinet. Figure 5 is a wiring diagram of the interconnection of connectors JM100 and JM101 and their respective terminal boards. These terminal boards furnish interconnection to the input and output channels of the slave MUXs. Power is connected to terminal board 3 on the 8909-D from the power terminal strip on the side of the cabinet. The 8909-D01 requires both +20 and -20 vdc and the 8909-D02 requires only -20 vdc.

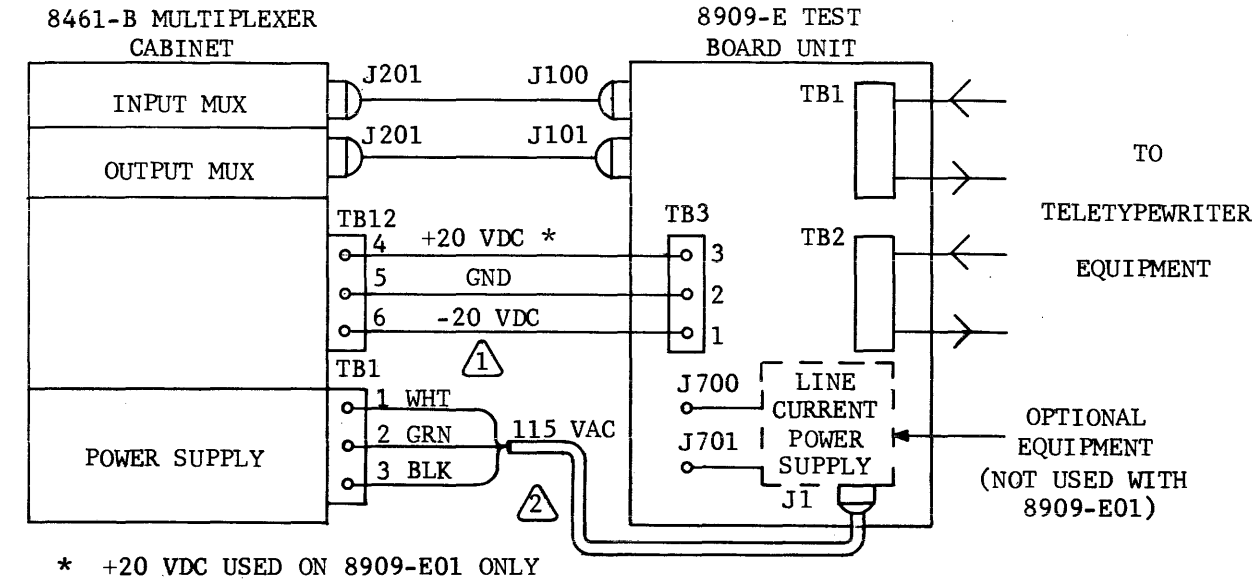
WARNING

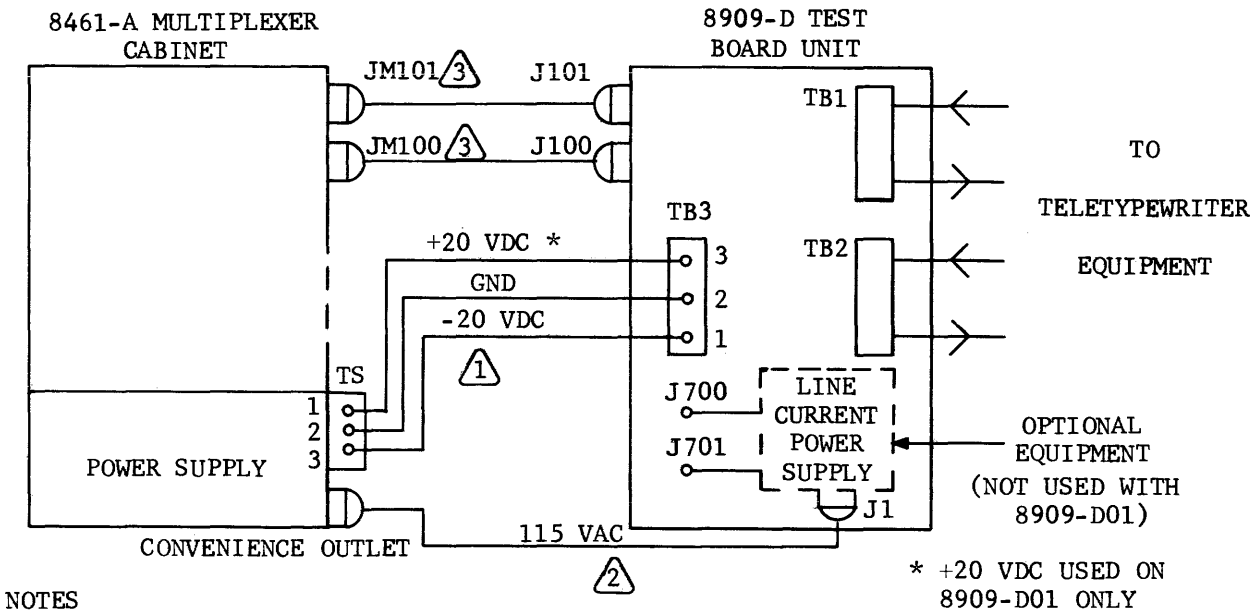
Use caution not to come in contact with the 120-vdc input lines on TB1 and TB2.

The Test Board Unit connects to the teletypewriter at terminal boards 1 and 2. Tables 2 and 3 list the terminal board connections for the channels. The Test Board Units can be used for either unipolar or bipolar teletypewriter line operation. Each input/output channel is connected via a maximum of five terminals on terminal boards 1 and 2. Using channel Ø as an example, terminals 1 and 2 are receive lines. For unipolar operation for the 8909-E, connect the send lines to terminals 3 and 4. For unipolar operation of the 8909-D, connect the send lines to terminals 4 and 5. For bipolar operation terminals 3, 4, and 5 are connected to the send lines.

ADJUSTMENTS

The following adjustments are necessary when connecting the Test Board Unit to a line-current power supply in the MUX cabinet. When the line-current power supply is not used, the send potentiometers (P20 through P27) and the receive potentiometers (P00 through P07) are adjusted to full counterclockwise.





NOTES

1 WIRING SUPPLIED WITH 8909-D,-E

2 POWER CORD SUPPLIED WITH LINE CURRENT POWER SUPPLY

3 CABLE SUPPLIED WITH 8909-D. SEE FIGURE 5 FOR WIRING TO CABINET TERMINAL BOARD

Figure 4. 8909-D/E Interconnecting Diagram

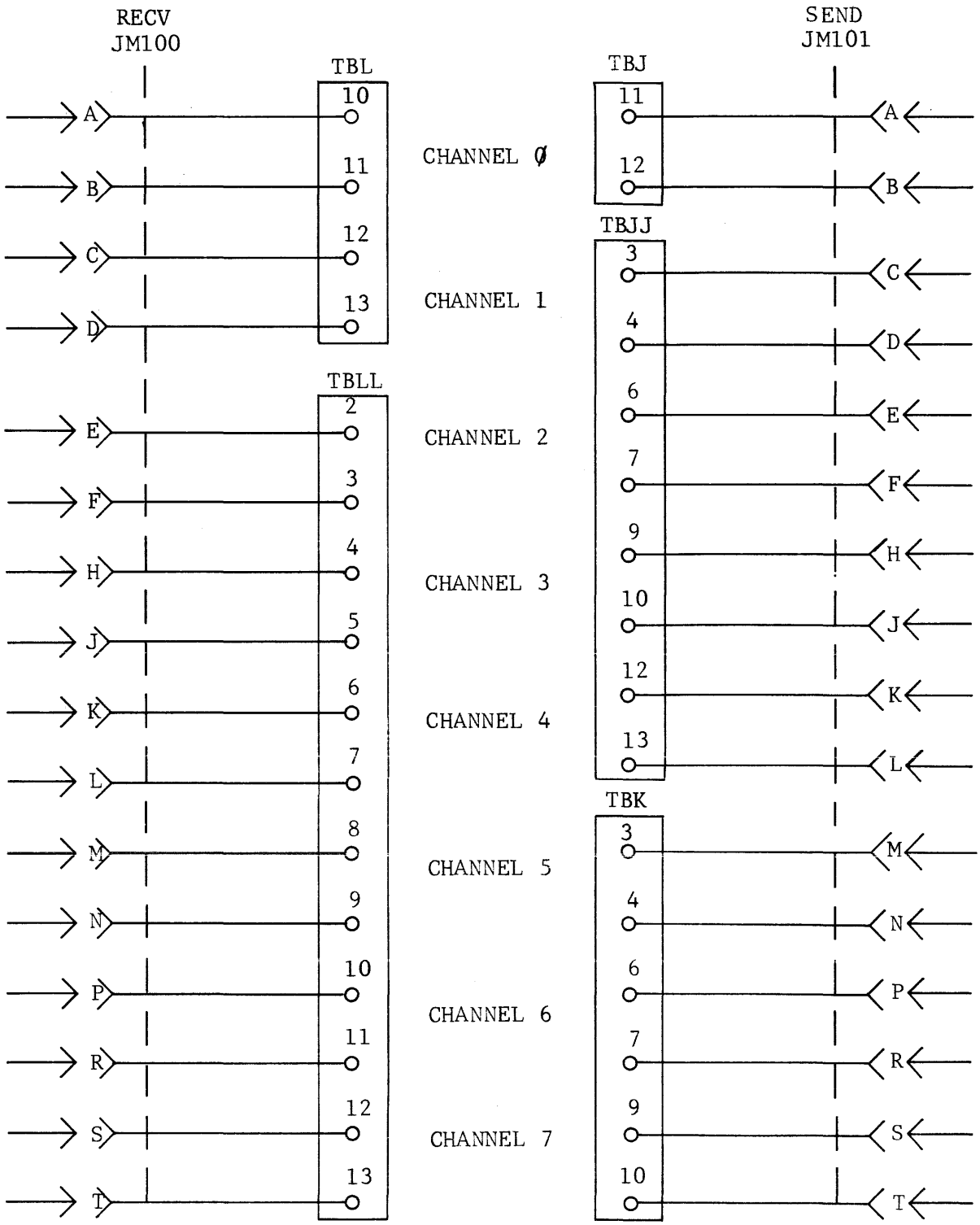


Figure 5. 8909-D - 8461-A Interface Wiring

TABLE 2. TEST BOARD UNIT AND TELETYPEWRITER EQUIPMENT INTERFACE (TERMINAL BOARD 1)

TERMINAL BOARD NO. 1 CONNECTOR	FUNCTION
1	Receive - Channel Ø
2	Receive - Channel Ø
3	Send - Channel Ø (8909-E unipolar)
4	Send - Channel Ø (8909-E and 8909-D unipolar + bipolar)
5	Send - Channel Ø (8909-D unipolar + bipolar)
6	Receive - Channel 1
7	Receive - Channel 1
8	Send - Channel 1 (8909-E unipolar + bipolar)
9	Send - Channel 1 (8909-E and 8909-D unipolar + bipolar)
10	Send - Channel 1 (8909-D unipolar + bipolar)
11	Receive - Channel 2
12	Receive - Channel 2
13	Send - Channel 2 (8909-E unipolar + bipolar)
14	Send - Channel 2 (8909-E and 8909-D unipolar + bipolar)
15	Send - Channel 2 (8909-D unipolar + bipolar)
16	Receive - Channel 3
17	Receive - Channel 3
18	Send - Channel 3 (8909-E unipolar + bipolar)
19	Send - Channel 3 (8909-E and 8909-D unipolar + bipolar)
20	Send - Channel 3 (8909-D unipolar + bipolar)

Send Potentiometer

With power connected to the system, insert the LOOP mA meter plug into each SEND jack and adjust the corresponding potentiometer (P20 through P27) for an indication of 60 ma on the LOOP mA meter.

Receive Potentiometer

With power connected to the system, insert the LOOP mA meter plug into each RECV jack and adjust the corresponding potentiometer (P00 through P07) for an indication of 60 ma on the LOOP mA meter.

TABLE 3. TEST BOARD UNIT AND TELETYPEWRITER EQUIPMENT INTERFACE (TERMINAL BOARD 2)

TERMINAL BOARD NO. 2 CONNECTOR	FUNCTION
1	Receive - Channel 4
2	Receive - Channel 4
3	Send - Channel 4 (8909-E unipolar + bipolar)
4	Send - Channel 4 (8909-E and 8909-D unipolar + bipolar)
5	Send - Channel 4 (8909-D unipolar + bipolar)
6	Receive - Channel 5
7	Receive - Channel 5
8	Send - Channel 5 (8909-E unipolar + bipolar)
9	Send - Channel 5 (8909-E and 8909-D unipolar + bipolar)
10	Send - Channel 5 (8909-D unipolar + bipolar)
11	Receive - Channel 6
12	Receive - Channel 6
13	Send - Channel 6 (8909-E unipolar + bipolar)
14	Send - Channel 6 (8909-E and 8909-D unipolar + bipolar)
15	Send - Channel 6 (8909-D unipolar + bipolar)
16	Receive - Channel 7
17	Receive - Channel 7
18	Send - Channel 7 (8909-E unipolar + bipolar)
19	Send - Channel 7 (8909-E and 8909-D unipolar + bipolar)
20	Send - Channel 7 (8909-D unipolar + bipolar)

Bias Potentiometer

With power connected to the system, insert the LOOP mA meter plug into each BIAS jack (8 on 8909-D01, 8909-E01; and 1 on 8909-D02, 8909-E02) and adjust the corresponding potentiometer for an indication of 30 ma on the LOOP mA meter.

PRINCIPLES OF OPERATION

OUTPUT CIRCUITS

Figure 6 is a schematic diagram of the 8909-D01 and 8909-E01 Test Board Units and figure 7 is a schematic diagram of the 8909-D02 and 8909-E02 Test Board Units. The output from the LSOU is received by the Test Board Unit on the applicable pin of connector J101. This output completes the circuit to the applicable send relay coil and closes the relay. When the relay is closed, the circuit between the Test Board Unit and the external communications line is completed via the applicable SEND jack (J20 through J27) and terminal board 1 or 2.

INPUT CIRCUITS

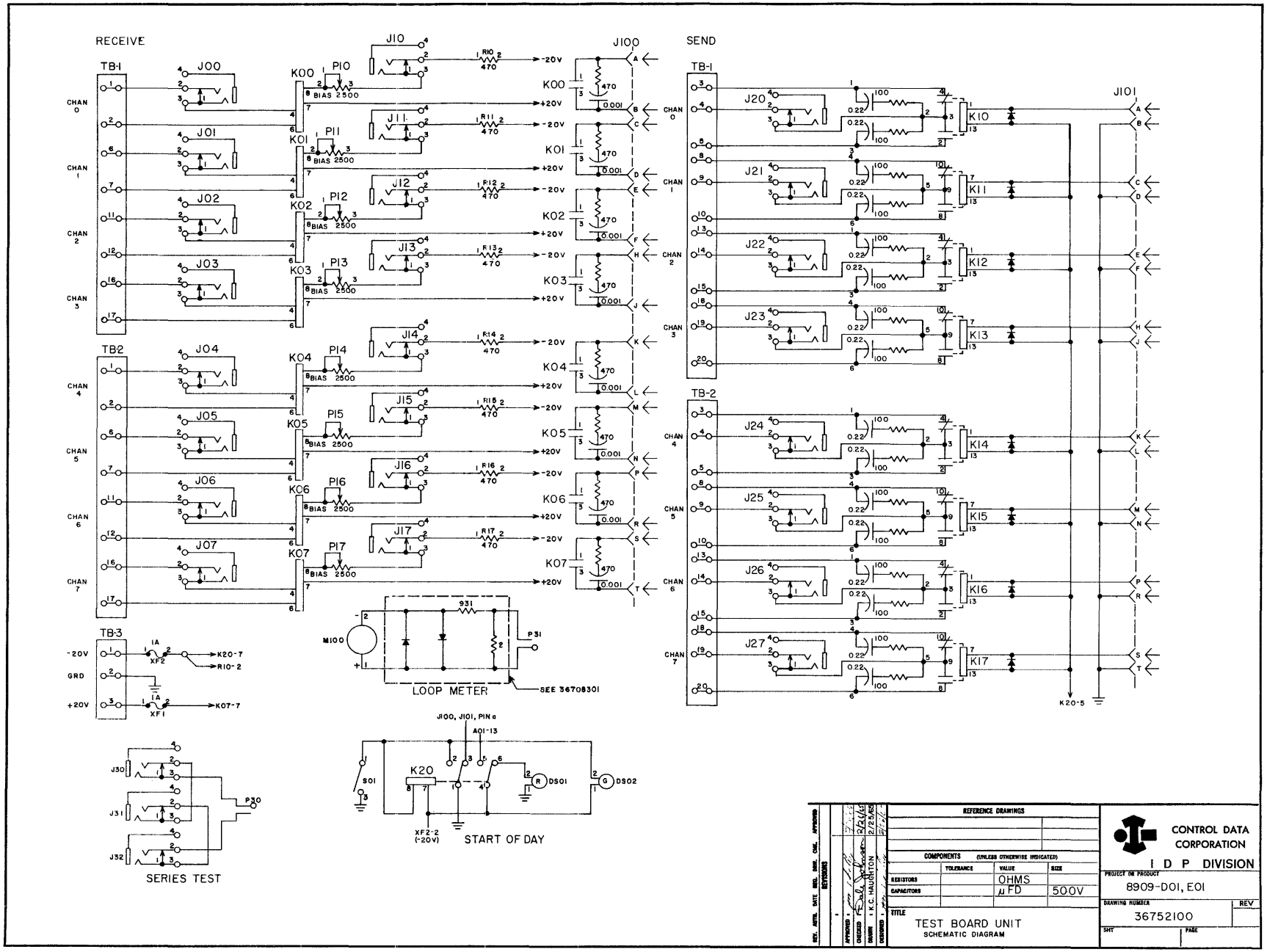
The input circuits enter the Test Board Unit through terminal board 1 or 2, pass through the RECV jack (J00 through J07) and energize one of the biased mercury relays. The closed relay completes the input circuit sending -20 vdc through the applicable pin of connector J100 to the corresponding LSIU.

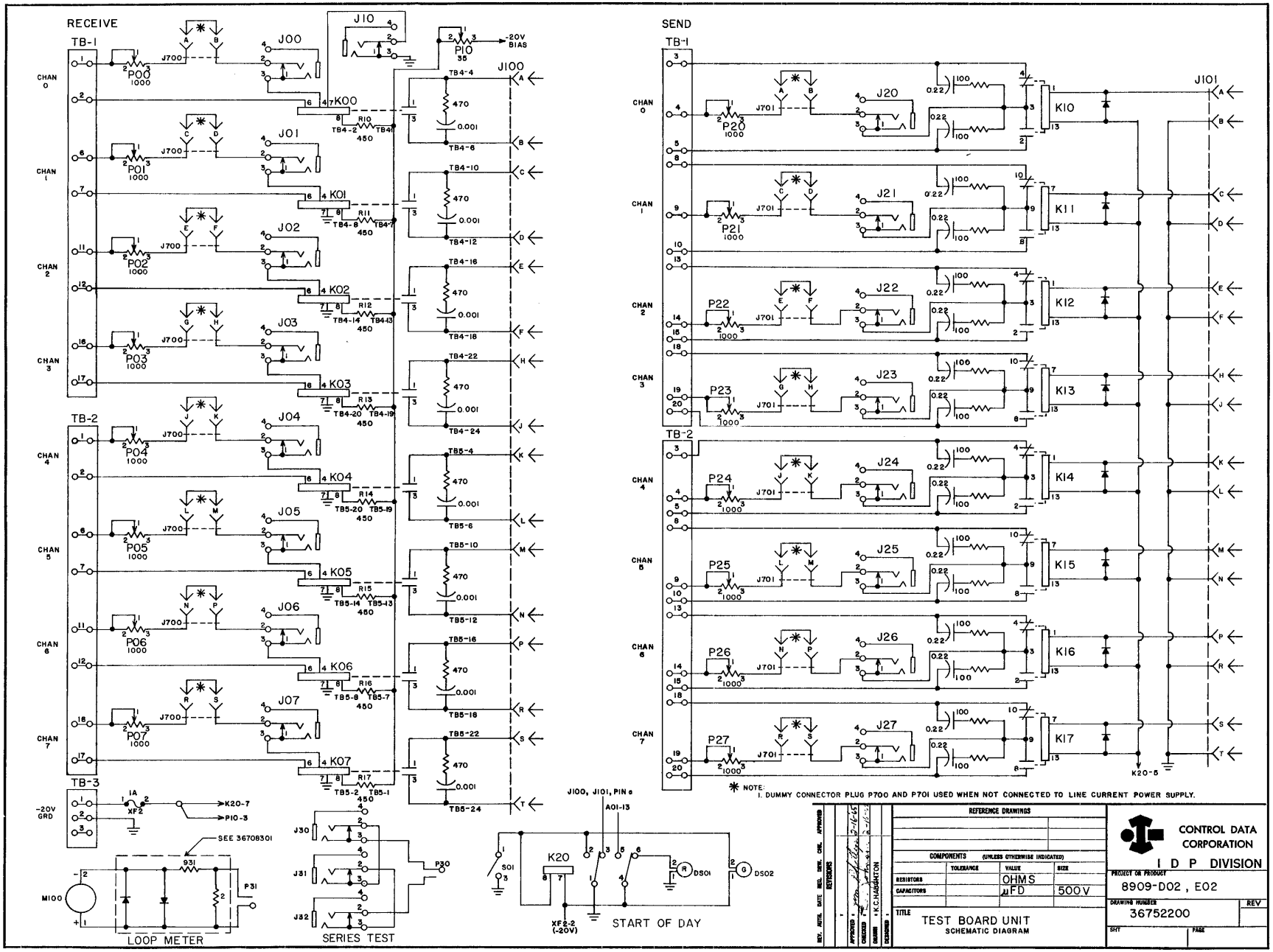
RELAY BIAS CURRENT

The relay bias current is provided in the 8909-D01 and 8909-E01 by the 8615-C Power Supply via terminal board 3 and a separate 470-ohm resistor for each relay. Potentiometers P10 through P17 are used to adjust the relay bias current to (a value equal to) one-half the current received on the external communication lines. Jacks J10 through J17 and the LOOP mA meter on the panel are used to monitor the bias current on the relays. The relay bias current is provided in the 8909-D02 and 8909-E02, via terminal board 3 to potentiometer P10 and a separate 450-ohm resistor for each relay. Potentiometer P10 is used to adjust the relay bias current to a value equal to one-half the current received on the external communication lines. Jack J10 and the LOOP mA meter on the panel are used to monitor the bias current on the relays.

SEND AND RECV JACKS

Jacks J00 through J07 are RECV jacks used with LOOP mA meter plug P31, to monitor the line current of the incoming signal. Jacks J20 through J27 are Send jacks used with the LOOP mA meter plug P31, to monitor the line current of the outgoing signal. Jacks J30 through J32 are SERIES TEST jacks which are used to connect external test equipment to either the SEND, RECV, or BIAS circuits. These circuits are selected by using the SERIES TEST plug P30.


RECEIVE
SEND
TB-1
TB-2
TB-3
J100
J101
CHAN 0
CHAN 1
CHAN 2
CHAN 3
CHAN 4
CHAN 5
CHAN 6
CHAN 7
BIAS 2500
-20V
+20V
GRD
LOOP METER
SEE 36708301
M100
P31
START OF DAY
SERIES TEST
P30
J100, J101, PIN a
A01-13
K20
S01
DS01
DS02
XF2-2 (-20V)
K20-5
K20-7
R10-2
K07-7
REFERENCE DRAWINGS
COMPONENTS (UNLESS OTHERWISE INDICATED)
TOLERANCE
VALUE
SIZE
RESISTORS
OHMS
CAPACITORS
μFD
500V
TITLE
TEST BOARD UNIT
SCHEMATIC DIAGRAM
CONTROL DATA CORPORATION
I D P DIVISION
PROJECT OR PRODUCT
8909-D01, E01
DRAWING NUMBER
36752100
REV
SHT
PAGE
REVISIONS
APPROVED
CHECKED
DRAWN
DESIGNED
K.C. HAUGHTON
2/25/65


RECEIVE
SEND
TB-1
TB-2
TB-3
CHAN 0
CHAN 1
CHAN 2
CHAN 3
CHAN 4
CHAN 5
CHAN 6
CHAN 7
J10
J00
J01
J02
J03
J04
J05
J06
J07
J100
J101
J20
J21
J22
J23
J24
J25
J26
J27
P10
P00
P01
P02
P03
P04
P05
P06
P07
P20
P21
P22
P23
P24
P25
P26
P27
K00
K01
K02
K03
K04
K05
K06
K07
K10
K11
K12
K13
K14
K15
K16
K17
-20V BIAS
-20V GRD
K20-7
P10-3
K20-5
SEE 36708301
M100
P31
P30
J30
J31
J32
LOOP METER
SERIES TEST
K20
S01
DS01
DS02
XF2-2 (-20V)
START OF DAY
J100, J101, PIN s
A01-13
* NOTE:
1. DUMMY CONNECTOR PLUG P700 AND P701 USED WHEN NOT CONNECTED TO LINE CURRENT POWER SUPPLY.
REFERENCE DRAWINGS
COMPONENTS (UNLESS OTHERWISE INDICATED)
TOLERANCE
VALUE
SIZE
RESISTORS
OHMS
CAPACITORS
μFD
500V
TITLE
TEST BOARD UNIT
SCHEMATIC DIAGRAM
CONTROL DATA CORPORATION
I D P DIVISION
PROJECT OR PRODUCT
8909-D02, E02
DRAWING NUMBER
36752200
REV
SHT
PAGE
K.C. HAGGERTON

SUPPRESSION CIRCUIT

A suppression circuit is incorporated in each input and output relay circuit. These circuits prevent high transient voltages from damaging relay contacts. The circuits consist of a diode across the relay coil or a capacitor-resistor series connected in parallel with the relay contacts.

START-OF-DAY CIRCUIT

The start-of-day circuit is used to de-energize the output relays of the LSOUs and prevent a free-running LSOU from placing an erroneous signal on the teletypewriter signal line when system power is first applied at the start of a day's operation. When power to the system is interrupted the START OF DAY relay (K20) releases and the switch lamp lights red. In this condition, the -20 vdc to the coils of the output relays is interrupted. This interruption prevents sending by the LSOUs. When power is applied to the system, pressing S01 energizes relay K20. In this condition the switch lamp lights green and -20 vdc is supplied to the coils of the output relays. The state of relay K20 also controls the application of ground on pin "a" of J100 and J101. This ground enables or disables the start-of-day circuitry in the input and output MUXs.

LINE-CURRENT POWER SUPPLY

The 8909-D02 and 8909-E02 provide for connecting a system line-current power supply used to provide teletypewriter loop current when connecting to external communication lines that do not provide power. In this case, the line-current power supply is connected to connectors J700 and J701. Potentiometers P00 through P07 and P20 through P27 are used to adjust the line current of the power supply to the desired level. When the line-current power supply is not used, potentiometers P00 through P07 and P20 through P27 shall be adjusted to full counterclockwise. In addition, dummy connectors P700 and P701 shall be connected to connector J700 and J701.

MAINTENANCE

If all channels fail to receive messages, check the power supplied to terminal board 3. If only one input channel is out, check that relay first and then the 470- (450-) ohm resistor for that relay. The input power to the Test Board Unit is protected by a one-amp fuse on the power supply line for both +20 and -20 vdc. The 8909-E02 and 8909-D02 require only one fuse since only -20-vdc power is used.

PIN ASSIGNMENTS

Table 4 lists the function of each pin of connectors J100 and J101.

TABLE 4. PIN ASSIGNMENTS - J100 AND J101

PIN	SIGNAL	PIN	SIGNAL
J100-A	Signal In - Channel Ø	J101-A	Signal Out - Channel Ø
J100-B	Return - Channel Ø	J101-B	Ground - Channel Ø
J100-C	Signal In - Channel 1	J101-C	Signal Out - Channel 1
J100-D	Return - Channel 1	J101-D	Ground - Channel 1
J100-E	Signal In - Channel 2	J101-E	Signal Out - Channel 2
J100-F	Return - Channel 2	J101-F	Ground - Channel 2
J100-H	Signal In - Channel 3	J101-H	Signal Out - Channel 3
J100-J	Return - Channel 3	J101-J	Ground - Channel 3
J100-K	Signal In - Channel 4	J101-K	Signal Out - Channel 4
J100-L	Return - Channel 4	J101-L	Ground - Channel 4
J100-M	Signal In - Channel 5	J101-M	Signal Out - Channel 5
J100-N	Return - Channel 5	J101-N	Ground - Channel 5
J100-P	Signal In - Channel 6	J101-P	Signal Out - Channel 6
J100-R	Return - Channel 6	J101-R	Ground - Channel 6
J100-S	Signal In - Channel 7	J101-S	Signal Out - Channel 7
J100-T	Return - Channel 7	J101-T	Ground - Channel 7
J100-a	Start-of-Day Control	J101-a	Start-of-Day Control

COMMENT SHEET

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Publication No. 368 161 00

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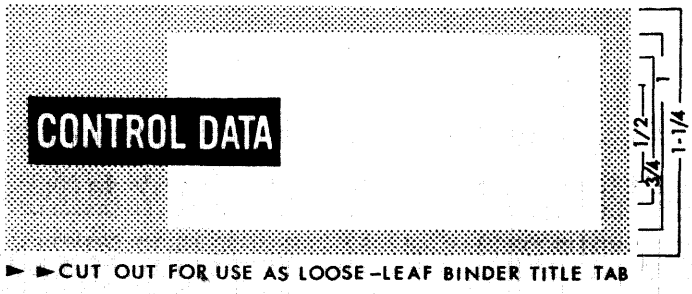

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