74879600

CONTROL DATA CORPORATION

CDC® EMULATION COUPLER

DY159-A/B

HARDWARE MAINTENANCE MANUAL

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HARDWARE MAINTENANCE MANUAL

REVISION RECORD

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	back for repair, 4) Clock adjustment procedures for new
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or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an ECO or FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCO'S	COMMENTS
DY159-A	01	06001	
	02	06568	
	03	06612	
	04		
DY159-B	01		

LIST OF EFFECTIVE PAGES

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

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PREFACE

This manual provides basic information on the CDC® Emulation Couplers DY159-A and DY159-B which are part of a Network Processor Unit. Sufficient data is included in this document to enable customer engineers to install and service the coupler.

The network processor unit with the emulation coupler emulates 6671 and 6676 data set controllers to permit direct replacement.

The A and B version cabinets referenced in this manual are described in the Network Processor Unit Equipment Cabinets manual. Changes to the coupler cables were made to accommodate the B version cabinet, which contains electromagnetic interference protection features.

The related publications listed below are available through the CDC Literature and Distribution Services, 308 North Dale Street, St. Paul, Minnesota 55103.

Publication Title	Publication Number
6671/6676 Emulation Controlware, Reference Manual	74750800
2550-100 Emulator 6671/6676, Installation Handbook	74750900
255X Network Processor Unit, Hardware Maintenance Manual	60472000
255X Network Processor Unit, Hardware Reference Manual	60472800
255X Network Processor Unit, Site Preparation Manual	74641200
Controlware Product Configurator 2550-100	74750600
CYBER 70, Models 72/73/74 Computer Systems, Instruction Description	60347300
6000/CYBER 70 System Maintenance Monitor, Reference Manual, Volume 5	60160600
CYBER 70, Model 72 Computer System, Reference Manual, Volume 1	60347000
6400/6500/6600 Computer Systems, Reference Manual	60100000
MP17 I/O Extender Unit, Hardware Reference Manual	39566900
255X Network Processor Unit Equipment Cabinets, Hardware Maintenance Manual	74873971

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FIGURES

TABLES

The network processor unit (NPU) handles all communications between a host and a network of terminals. The coupler acts as a go-between for the host and the processor within the NPU. In this capacity the coupler buffers all signals from the host to the processor and all signals from the processor to the host.

A typical NPU is illustrated in figure 1-1. As shown in figure 1-2, the NPU contains eight basic blocks: the coupler, processor, memory, cassette, multiplexer, cyclic encoder, line adapter, and multiplex adapter. A separate hardware maintenance manual is available on each of these items. The overall function of the coupler is clearly shown in figure 1-3. The following paragraphs describe the physical and functional characteristics of the coupler.

PHYSICAL DESCRIPTION

The coupler consists of two circuit cards and associated cables. Each circuit card fits into the processor card cage, which is located at the top of the NPU cabinet. See figure 1-4.

The coupler occupies slots C and B. If two couplers are included in the NPU, the second one occupies slots AA and AB. The circuit card on the left or in slot C is the NPU interface. The circuit card on the right or in slot B is the channel synchronizer. Circuit card locations are shown in figure 1-5.

Both circuit cards have edge connectors which plug into mating connectors in the backplane of the card cage. Three jumper cables at the front of the bay connect the two cards together. Backplane wiring and a jumper cable connect the interface to the processor. Cables from the host connect to the synchronizer at the back of the card cage. The following paragraphs describe the synchronizer, the interface, and major cables.

SYNCHRONIZER

The synchronizer is a printed circuit card containing mostly integrated circuits in standard packages. Some discrete-component circuits are also on the card. Five DIP-type switches on the synchronizer must be set prior to installation. A potentiometer is located on the front edge of the card so that it is accessible after the coupler is installed. All connections between the host and coupler are made to the synchronizer.

INTERFACE

The interface is a printed circuit card containing mostly integrated circuits in standard packages. A toggle switch is located on the front edge of the card so that it is accessible after the coupler is installed. All connections between the coupler and the processor are made to the interface.

MAJOR CABLES

Three short ribbon cables connect J1, J2, and J3 of the synchronizer to J1, J2, and J3 of the interface. The J] cable has 20 conductors and is mainly used for spares and modifications. Both the J2 and J3 cables contain 50 conductors each and carry the major signals between circuit cards. J1, J2, and J3 are mounted on the front edge of each circuit card.

Two 19-conductor coaxial cables connect the synchronizer to the host. The length of each cable must be exactly 75 feet (22.8 m) and is made from three sections. A 5-foot (1.5-m) section is directly connected to the coupler for each cable, or in the B version NPU cabinets, the 5-foot cable connects to a cable enclosure assembly and then to the 65-foot (19.8-m) cable. This section is then connected to a 65-foot section, which would be connected to another 5-foot section before connecting to the host.

A typical installation of two couplers is shown in figure 1-6; cabling to coupler 1 shows the 65-foot cable combined with an optional 5-foot cable provided in the cable set.

FUNCTIONAL DESCRIPTION

The host can be connected to from one to eight external equipments. Each equipment connected to it is assigned a mutually exclusive address number of 0 to 7. The coupler has four such addresses, which the host recognizes as four separate equipments. One or more of these addresses can be turned off if it is not to be used. Equipment switches on the synchronizer are preset to the addresses assigned to the NPU.

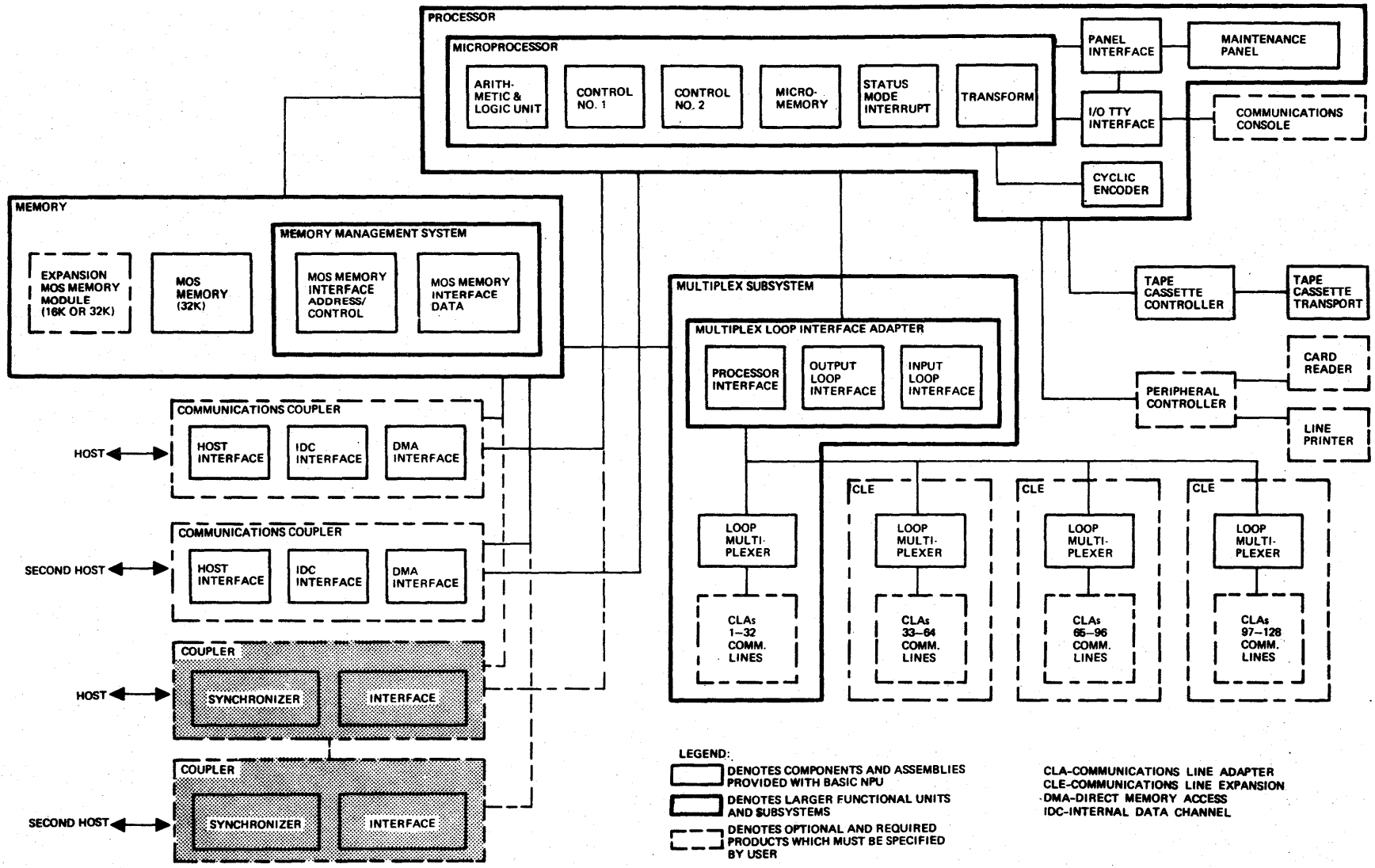


Figure 1-1. Network Processor Unit

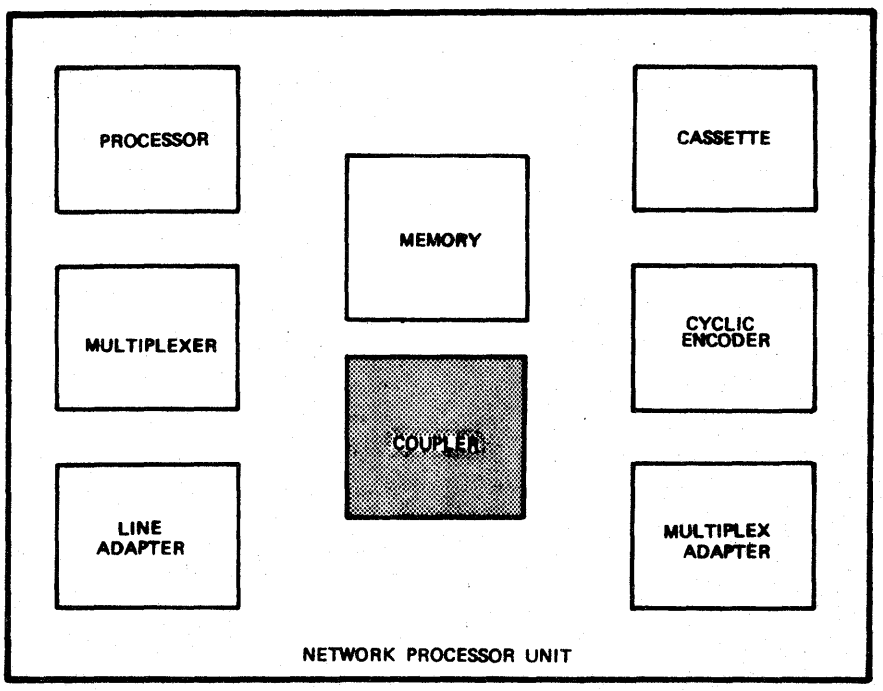


Figure 1-2. Functional Blocks of the NPU

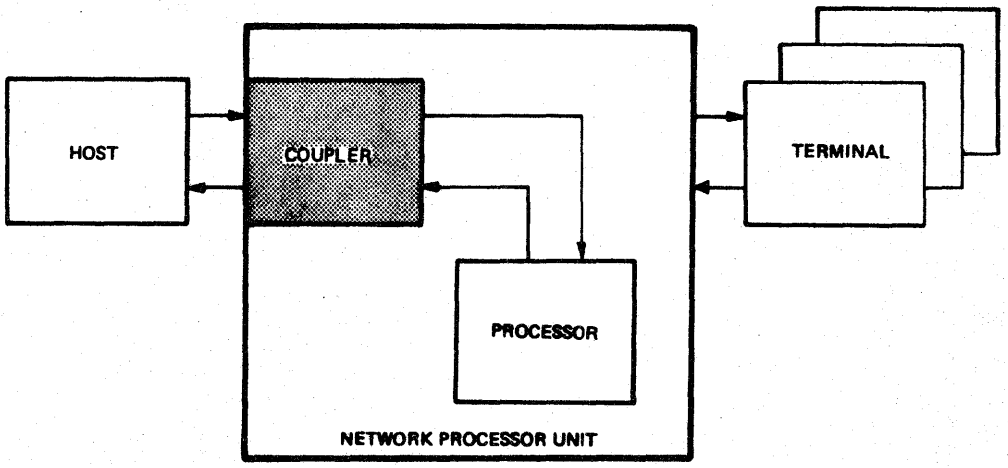


Figure 1-3. Coupler Function

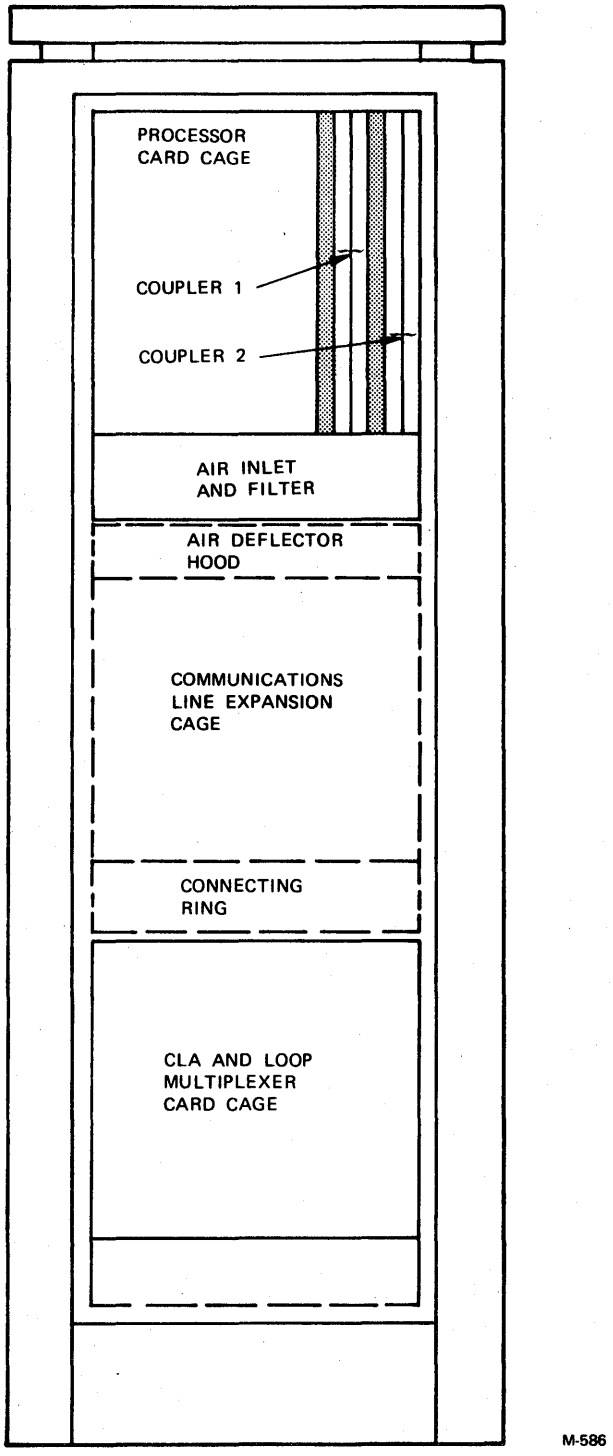


Figure 1-4. Front View of NPU Cabinet

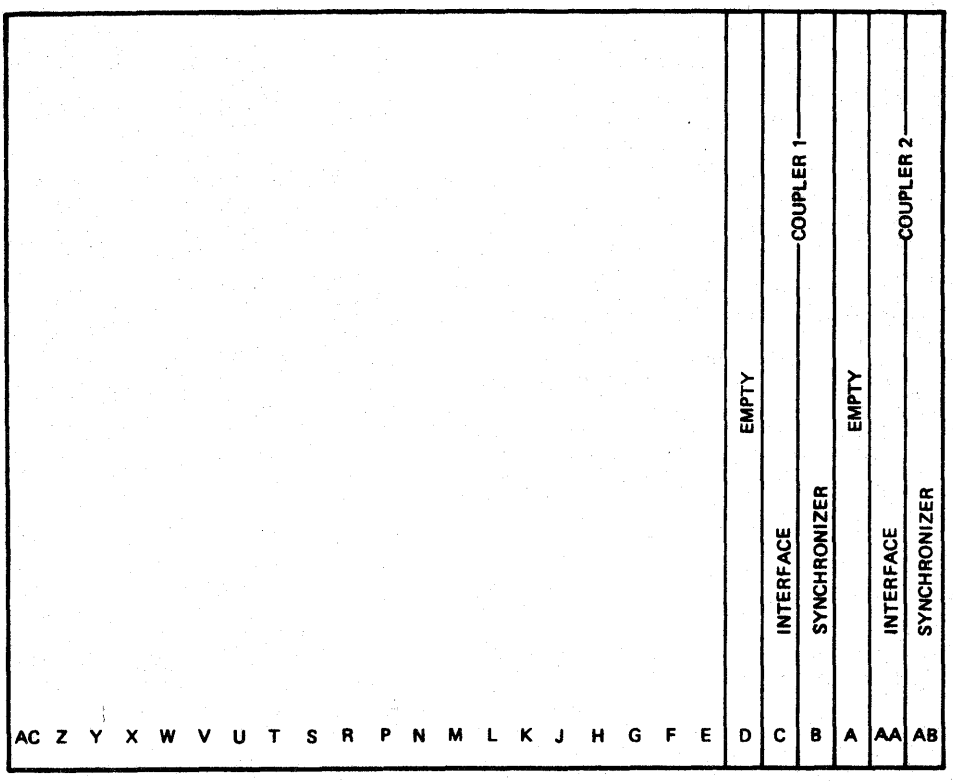


Figure 1-5. Circuit Card Locations

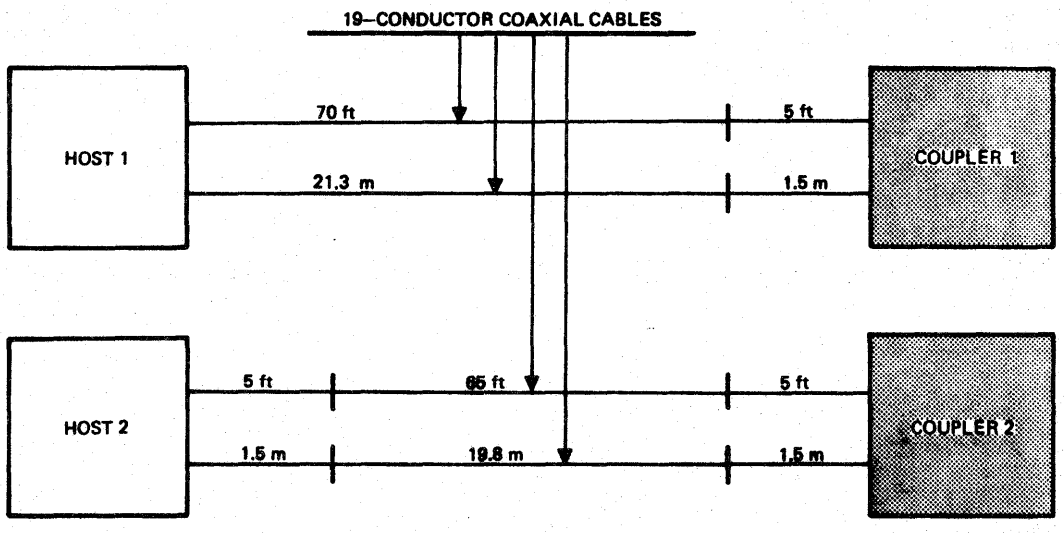


Figure 1-6. Two Couplers in a Typical Installation

All external equipments connected to the host are daisy chained and separated by 75 feet (22.8 m) of coaxial cable. The NPU may be directly connected to the host as shown in figure 1-6 or it may be anywhere in the daisy chain. The precise requirement of 75 feet (22.8 m) for cable length constitutes a propagation delay of 100 nanoseconds. When the host puts a word on the communications channel, it asks of each equipment, "Are you the equipment that I want to talk to? If you are or not, pass on this word to the next equipment in exactly 100 nanoseconds. If you are, then process this word and pass back the information that I want." See figure 1-7.

The coupler is controlled by the host, and the direction of data and signals refer to the host. Output data travels from the host to the coupler via the pass-on cable. Input data travels to the host from the coupler via the pass-back cable.

Before sending or receiving data, the host sends a function signal and a 12-bit function word to the coupler. Bits 9 through 11 contain the equipment number, Bits 0 and 1 contain one of three commands: output data, send status, or input data. If the equipment number is one that has been assigned to the coupler, the coupler will send an inactive signal to the host. Further transmission between coupler and host depends on the command in the function word.

OUTPUT DATA

If the command is to output data, the host sends a full signal and a data word to the coupler. The coupler then sends a empty signal to the host, stores the data word, and waits for the next data word. This process is repeated until all data has been transmitted, which is indicated when the host sends an inactive signal to the coupler. Data may be transferred at a rate of one million characters per second or two million characters per second depending on the type of host. Both transfer rates use the same basic timing sequence for data output. See figure 1-8.

Because terminals connected to the NPU may transfer data at a slower rate then the host, the output data must be protected. This is done as follows. When the coupler stores the output data, a protect bit is set. When this same data goes out to a terminal device, the protect bit is cleared. If the host tries to output additional data to the same terminal device before the protect bit is cleared, a character reject bit is set. The new data is rejected, and this fact is sent to the host on the next input data command. The host will then keep sending the same data until the protect bit is cleared.

INPUT DATA

If the command is to input data, the coupler sends a full signal and a data word to the host. The host then sends an empty signal to the coupler. This process is repeated until all data has been transmitted, which is indicated when the coupler sends an inactive signal to the host. However, the input data process can be terminated at any time by the host sending an inactive signal to the coupler. The timing sequence for data input is shown in figure 1-9.

Because terminals connected to the NPU may transfer data when the host is busy, the input data must be protected. This is done as follows. When the coupler stores the input data, a protect bit is set. When this same data is transferred to the host, the protect bit is cleared. If the terminal device sends input data before the protect bit is cleared, the coupler will reject the data. However, the new input data is held in the processor until the protect bit is cleared.

SEND STATUS

If the command is to send status, the coupler sends a full signal and a data word

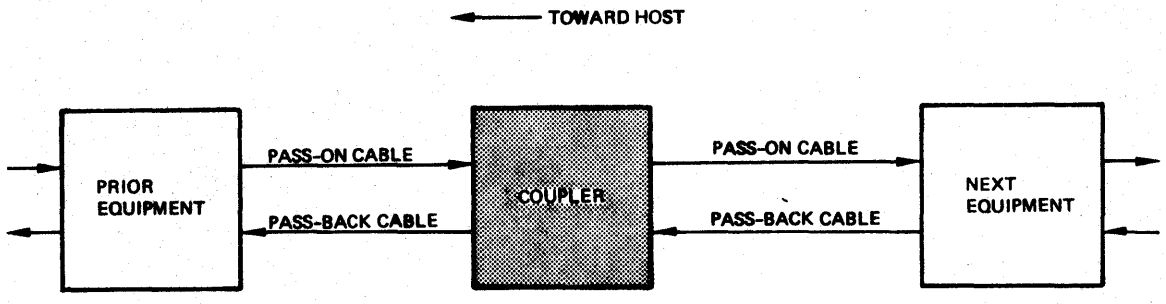
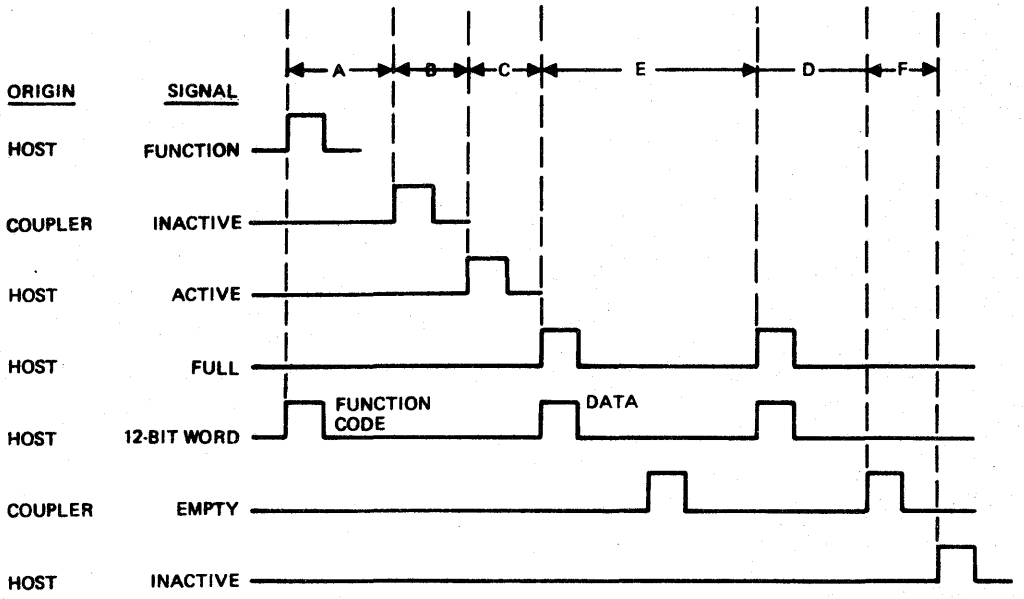


Figure 1-7. Coupler in a Typical Daisy Chain



TIME	FUNCTION OF	1 Mc/s	2 Mc/s	NOTES
A	COUPLER	1.0 μs	0.5 μs	2
B	HOST	100 ns	50 ns	
C	HOST	2 or 4 μs	1 or 2 μs	
D	COUPLER		50 ns	2, 3
E	COUPLER	1.0 μs	0.5 μs	
F	HOST	2.0 μs	1.0 μs	

NOTES: 1. MINIMUM TIMES ARE GIVEN ABOVE FOR TWO RATES OF DATA TRANSFER. THE ACTUAL TIMES ARE DEPENDENT ON SOFTWARE.

2. ACTUAL TIME IS A MULTIPLE OF THE MINIMUM TIME.

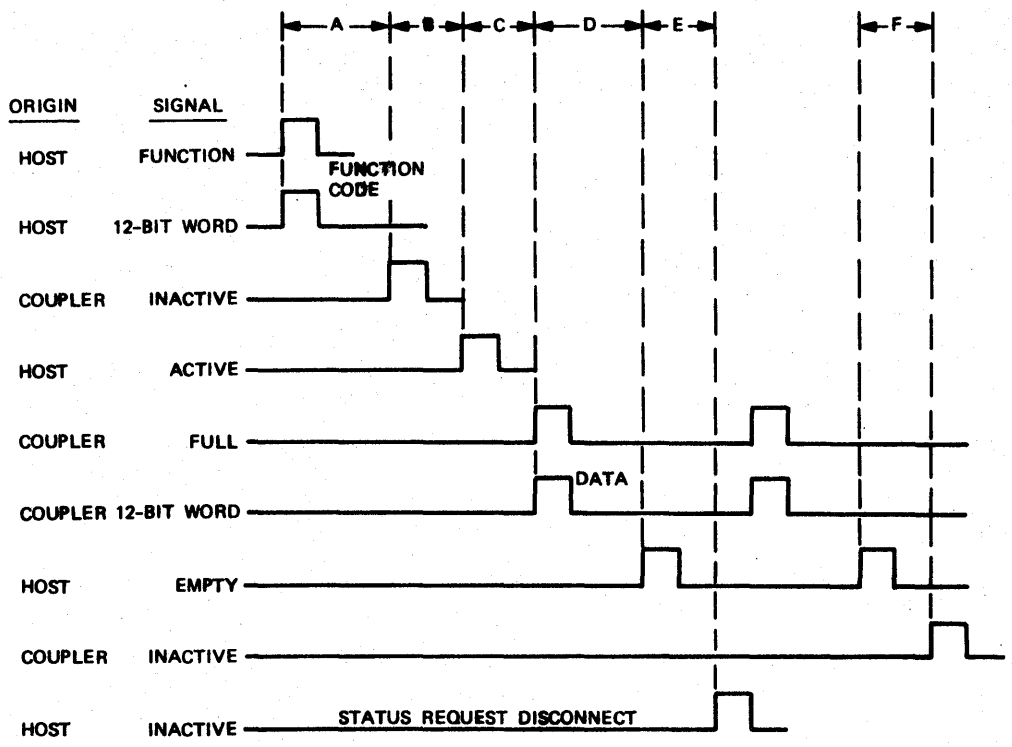
3. MAXIMUM TIME IS 450 ns FOR THE TRANSFER RATE OF 2 Mc/s.

Figure 1-8. Data Output Sequence

to the host. This data word contains the requested status. The host will then terminate the communications by sending an inactive signal to the coupler. The timing sequence for status requests is the same as for data input (figure 1-9).

CHARACTERISTICS

The electrical, physical, and environmental characteristics of the coupler are given in table 1-1.



TIME	FUNCTION OF	1 Mc/s	2 Mc/s	NOTES
A	COUPLER	1.0 μs	0.5 μs	2
B	HOST	100 ns	50 ns	
C	COUPLER			
D	HOST			2, 3
E	HOST	100 ns	50 ns	4
F	COUPLER	3.0 μs	1.5 μs	

NOTES:
1. MINIMUM TIMES ARE GIVEN ABOVE FOR TWO RATES OF DATA TRANSFER. THE ACTUAL TIMES ARE DEPENDENT ON SOFTWARE.
2. ACTUAL TIME IS A MULTIPLE OF THE MINIMUM TIME.
3. MAXIMUM TIME IS 450 ns FOR THE TRANSFER RATE OF 2 Mc/s.
4. MAXIMUM TIME IS A MULTIPLE OF ONE-THIRD THE MINIMUM TIME.

Figure 1-9. Data Input Sequence

TABLE 1-1. COUPLER CHARACTERISTICS

Parameter	Value
Electrical	
Input Voltage	+5.0 ±.25 V dc, 6.0 amp
Logic Levels	standard TTL
Logic Polarity	positive
Data Transfer Rate	1M or 2M C/S maximum
Physical	
Circuit Cards	2 each
Length	14 inches (356 mm)
Width	11 inches (279 mm)
Thickness	0.063 inches (1.6 mm)
Weight (2 cards)	2.4 lb (1.1 kg)
Coaxial Cables	2 each 70 feet (21.3 m)
	or 65 feet (19.8 m)
	4 each 5 feet (1.5 m)
Ribbon Cables	1 each 20-conductors
	2 each 50-conductors
Jumper Cable	1 each
Power Jumper	1 each (optional)
Environmental	
Temperature Range	50 to 95°F (10 to 35°C) operating
	14 to 122°F (-10 to 50°C) nonoperating
Temperature Change	18°F/h (10°C/h) operating
	27°F/h (15°C/h) nonoperating
Humidity Range	20 to 80% operating
	10 to 90% nonoperating
Humidity Change	10%/h operating
Dew-point Temperature	79°F (26°C) maximum
	25°F (-4°C) minimum
Altitude above Sea Level	6000 ft (1830 m) maximum
Altitude below Sea Level	1000 ft (305 m) maximum

The coupler has no operating controls and does not require programming. However, there are seven controls in the coupler; and the Network Processor Unit, of which the coupler is a part, does require programming. This section describes controls and delineates word formats.

CONTROLS

The location and function of the controls on the two circuit cards are given in the following paragraphs. These controls are the equipment switches, the clock adjustment controls, and the coupler select switch.

EQUIPMENT SWITCHES

The four equipment switches, S1 through S4, are located on the synchronizer. See figure 2-1. Each of these switches have eight individually selectable positions contained in a single package. See figure 2-2. The positions are numbered from 0 to 7, and one of them may be selected by setting it to ON. After selecting one position, set all other positions of that switch to OFF. No two switches should have the same position selected.

Each equipment switch if selected by the host will in effect connect the host to a particular set of terminals. Switch S1 is associated with one set of terminals; switch S2 is associated with another set; and switches S3 and S4 are each associated with still other sets. The position to which each switch is set depends on the program in the host. Setting all positions of an equipment switch of OFF will in effect disconnect a set of terminals.

CLOCK ADJUSTMENT

The clock adjustment switch S5 and the clock adjustment R6 are located on the synchronizer. Switch S5 has eight individually-selectable positions contained in a single package (figure 2-2). The positions are labeled A through H, and one or more of them may be selected by setting them to ON. This switch, which is preset at the factory, provides for an adjustment of clock pulse width and leading edge. Potentiometer R6, which is also preset at the factory, is a fine adjustment of the leading edge of the clock pulse. This adjustment can be made with the coupler installed.

COUPLER SELECT SWITCH

The coupler select switch S1 is a two position toggle located on the interface. See figure 2-3. Switch S1 enables the processor to differentiate between two couplers in the same network processor unit. The two switch positions are labeled 3 (for up) and 2 (for down). The position to which the switch is set depends on the program in the NPU.

WORD FORMATS

The formats of the function word and the status word are given in the following paragraphs.

FUNCTION WORD

The function word contains 12 bits and originates in the host. Bit zero is the least significant. The format of the function word is shown in figure 2-4. Binary command codes contained in bits 0 and 1 are: 00 is no action; 01 is output data; 10 is send status; and 11 is input data. Bits 3 through 8 are used for maintenance. The equipment number, as defined by the host program, is contained in bit 9 through 11.

The word stored in the F register is principally the same as the function word with the following exceptions. Bits 9 and 10 contain an equipment address which defines which set of terminals the host is addressing. Bit 11 indicates that the coupler has been selected by the host for communications.

STATUS WORD

The status word contains 12 bits and originates in the coupler. Bit zero is the least significant. The format of the status word is shown in figure 2-5. Status bits 0, 1, 4, and 5 carry information on one of four sets of terminals. Bit 1 indicates that data from one of the terminals is waiting to be transmitted to the host. Bit 0 says that the host did not input data before additional data arrived from that same terminal; as a result, the new data was lost. Actually the new data was retained in a register.

If the host does not output data within a specific time frame, bit 4 indicates that an output data failure has occurred.

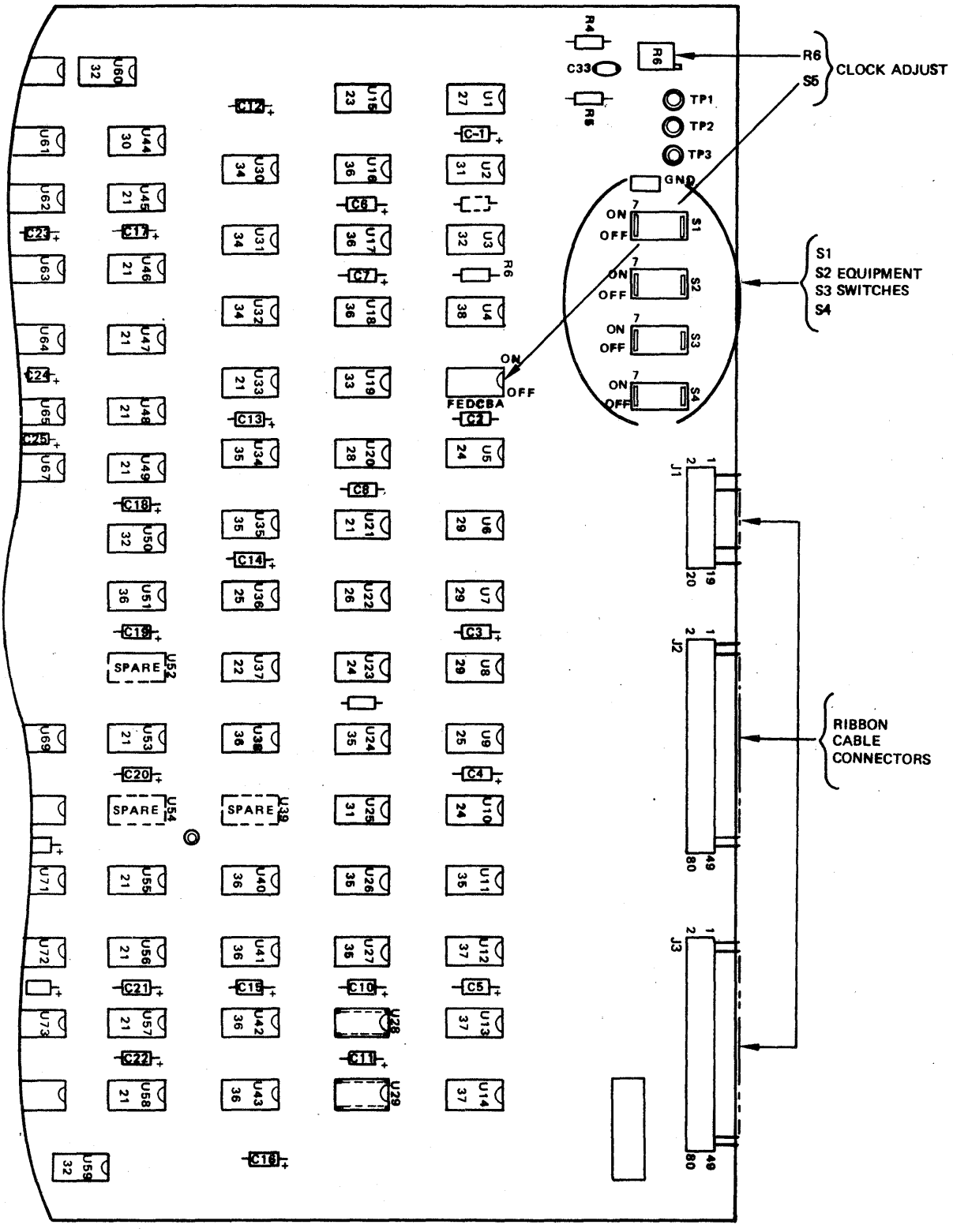
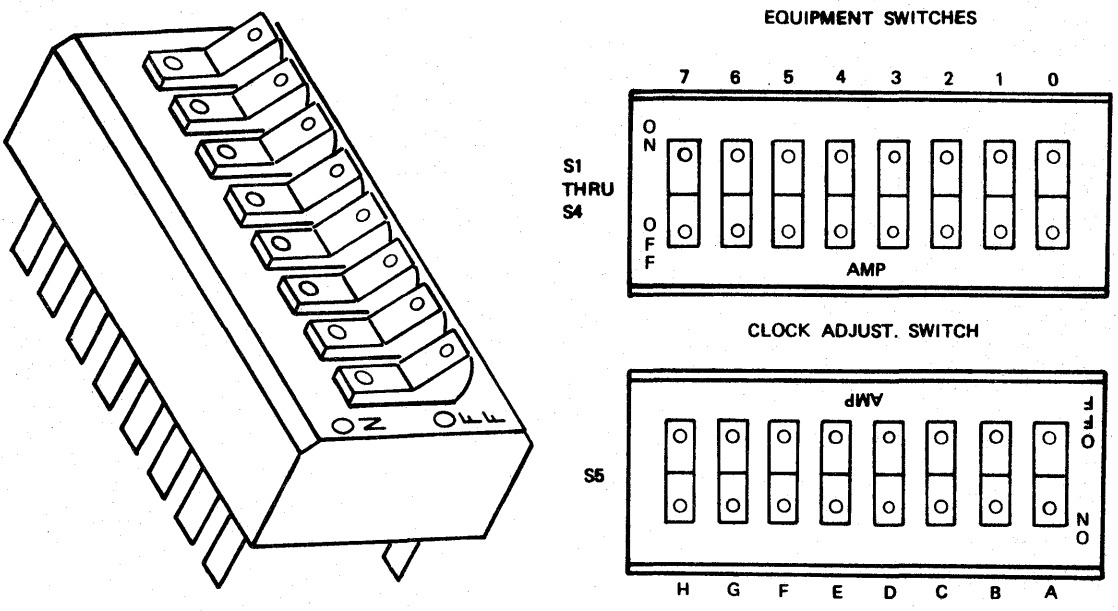


Figure 2-1. Synchronizer Controls

This time frame is determined by the data transfer rate of the receiving terminal. Bit 5 indicates that a parity error exists in memory.

Function word commands clear the status bits. Input data clears bits 0 and 1; output data clear bit 4; and send status clear bit 5.

A. SYNCHRONIZER 74873039



B. SYNCHRONIZER 74873041

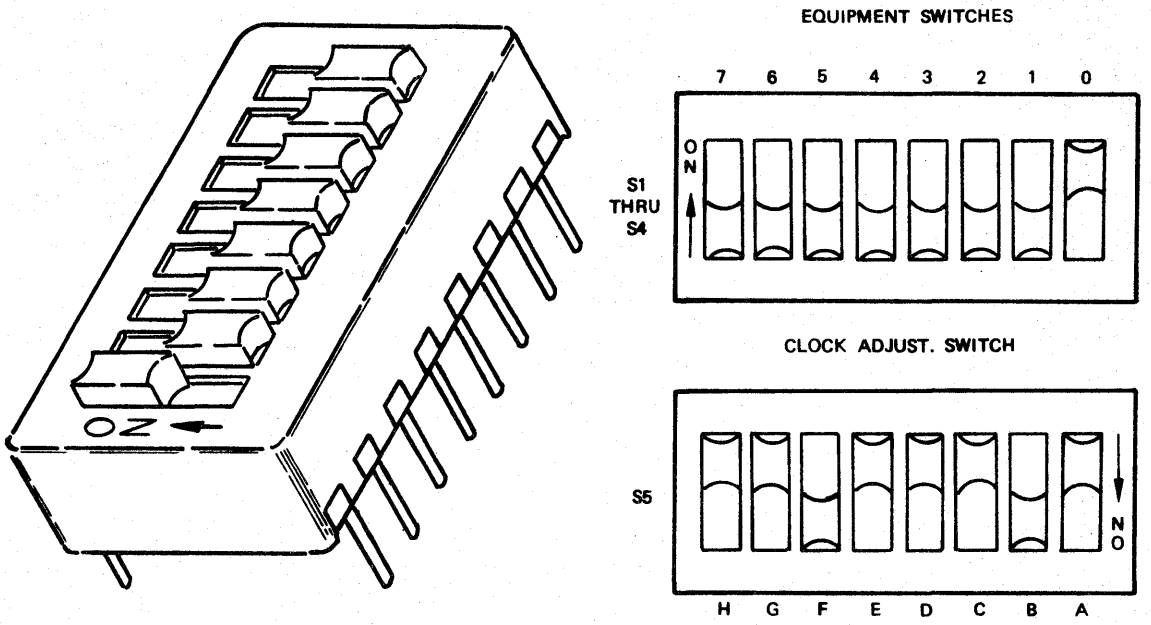


Figure 2-2. DIP Switches

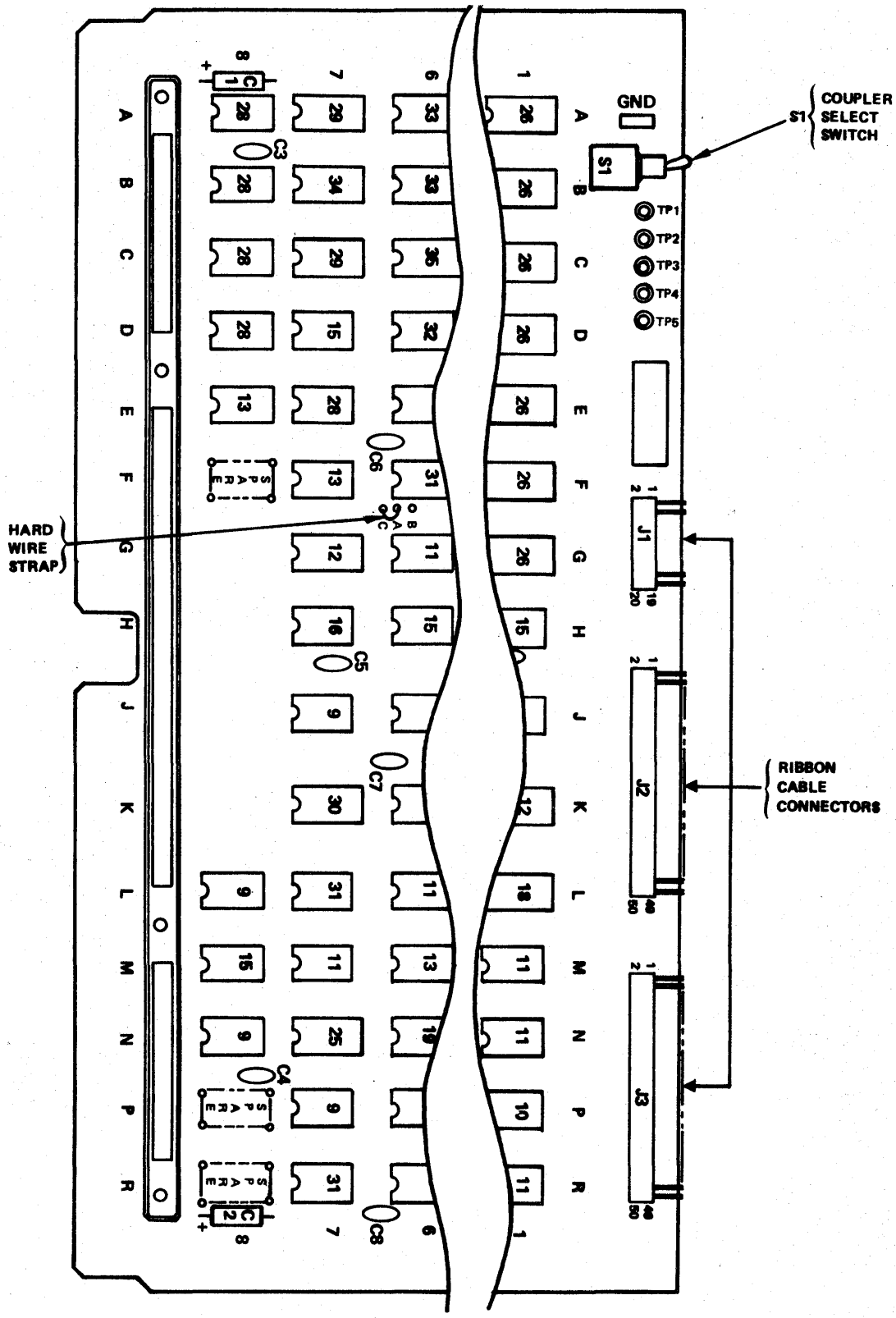
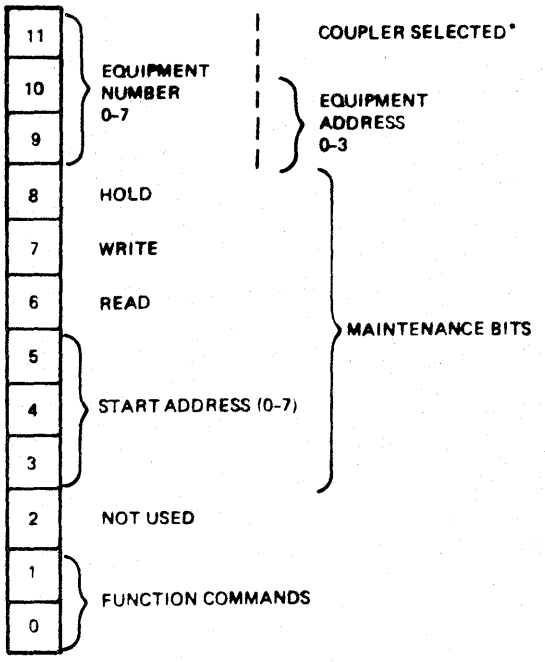


Figure 2-3. Interface Controls



*CHANGES IN FUNCTION WORD AS STORED IN F REGISTER.

Figure 2-4. Function Word Format

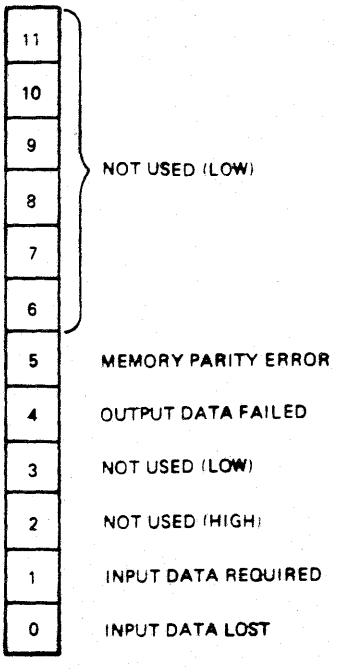


Figure 2-5. Status Word Format

Installation and checkout of the coupler is usually performed as a part of the installation and checkout of a Network Processor Unit. The NPU installation procedure includes a thorough checkout at the factory and on the site. The procedures in this section are for installing a coupler as an add-on or replacement to an existing subsystem. The following paragraphs contain data on uncrating, installing and checking out a coupler.

UNCRATING

If the coupler is received already installed in a card cage, refer to the NPU hardware maintenance manual for uncrating instructions. If the coupler is received in a padded container, carefully unpack the major parts and check them for damage. See tables 3-1 and 3-2. If anything is damaged, refer to the field procedures guide for disposition of damaged equipment.

INSTALLATION

Perform the installation in the order given, skipping over paragraphs that are not applicable. Refer to the site preparation documents as needed. The installation sequence is given first, and then each item in the sequence is expanded to a complete procedure. Identify each item from the table of major components, tables 3-1 and 3-2.

INSTALLATION SEQUENCE

1. Install power jumper cable (figure 3-1) at rear of card cage.

   NOTE

   The power jumper is only installed if an external 5 V dc supply is not wired to the coupler. Normally the external supply is used to permit pass-on and pass-back operations when NPU power is removed.

2. Install jumper cable (figure 3-1) at rear of card cage.
3. Install coaxial cables (figure 3-2) on connectors at rear of card cage.
4. Set equipment switches (figure 2-1) on synchronizer.
5. Install ribbon cables (figure 3-3) between synchronizer and interface.
6. Install both circuit cards concurrently into card cage (figure 1-5).
7. Set coupler select switch on interface card.

TABLE 3-1. DY159-A EMULATION COUPLER AND CABLE SET, MAJOR COMPONENTS

Description	Part Number	Quantity
Synchronizer circuit card } 1st version†	74873038	1
Interface circuit card } 1st version†	74872961	1
or		
Synchronizer circuit card } 2nd version†	74873040	1
Interface circuit card } 2nd version†	74872963	1
Ribbon cable, 50 conductors	74843700	2
Ribbon cable, 20 conductors	74845800	1
Jumper cable, 3 connectors	74870828	1
Power jumper (optional)	88964500	1
Cable set (purchased separately with DY159-A)		
- Coaxial cable, 65 ft (19.8 m)	19191600	2
- Coaxial cable, 5 ft (1.5 m)	52675100	2
- Coaxial cable, 5 ft (1.5 m)	88947800	4
	††74875766	

†Only one first version or second version card set is required. First version and second version cards in combination are not compatible.
††Used with EMI (B version) cabinets

TABLE 3-2. DY159-B EMULATION COUPLER, MAJOR COMPONENTS

Description	Part Number	Quantity
Synchronizer circuit card	74873040	1
Interface circuit card	74872963	1
Ribbon cable, 50 conductors	74843700	1
Ribbon cable, 20 conductors	74845800	1
Jumper cable, 3 connectors	74870828	1
Power cable (optional)	88964500	1
Cable set (supplied with DY159-B)		
- Coaxial cable, 65 ft (19.8 m)	19191600	2
- Coaxial cable, 5 ft (1.5 m)	52675100	2
- Coaxial cable, 5 ft (1.5 m)	74875766	4

POWER JUMPER

1. Plug power jumper 88964500 into pins 1 through 4 of slot B. See figure 3-1.

2. If two couplers are to be installed, plug another power jumper 88964500 into pins 1 through 4 of slot AB (figure 3-1).

JUMPER CABLE

1. Plug P1 of jumper cable 74870828 into pins 280 through 294 of slot AA (figure 3-2). The top conductor should be connected to the top pin.

2. Plug P2 of the jumper cable into pins 280 through 294 of slot C.

3. Plug P3 of the jumper cable into pins 280 through 294 of slot G.

COAXIAL CABLES

The DY159-A coupler cables are installed in the A version cabinet as shown in figure 3-4. The DY159-B coupler cables are installed in the B version cabinet as shown in figure 3-5.

CAUTION

When installing pass-on and pass-back cable connectors to the backplane pins, tie each 5-foot coaxial cable to the supporting structure of the bay. If this is not done, backplane pins may be bent or permanently damaged.

NOTE

If the coupler is the only equipment to be connected to the host or the last one on the daisy chain, the pass-on and pass-back cables to the next equipment are not required.

If the host is provided with two 5-foot cables, they can be used in place of the 5-foot cables extending from the 65-foot pass-on and pass-back cables to the host.

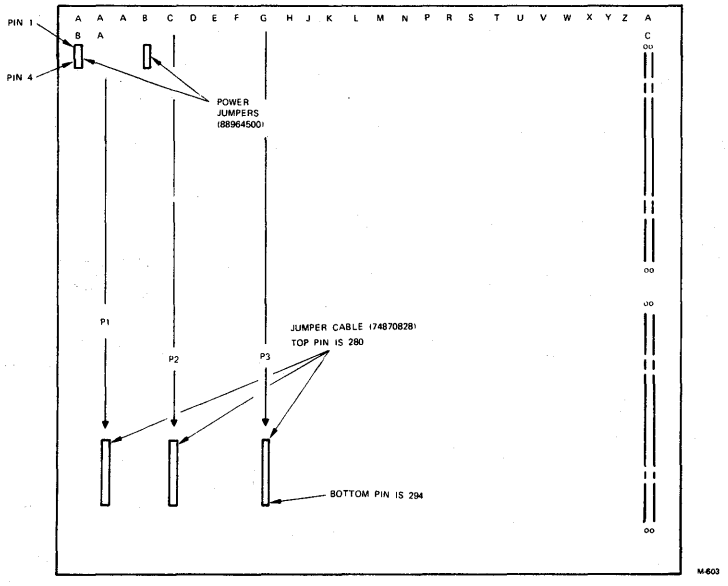


Figure 3-1. Jumper Cable Connectors

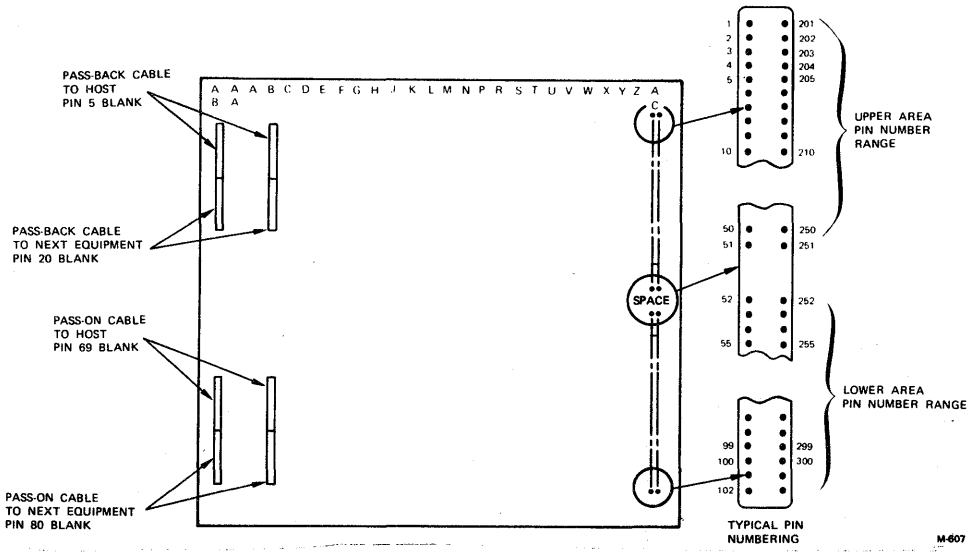


Figure 3-2. 5-Foot Coaxial Cables on Synchronizer

EQUIPMENT SWITCHES

1. Set all positions of equipment switch S1 to OFF (figures 2-1 and 2-2).
2. Set all positions of S2 to OFF.
3. Set all positions of S3 to OFF.
4. Set all positions of S4 to OFF.
5. Refer to NPU program and determine which of four sets of terminals are connected, and to which equipment switch each set of terminals correspond.
6. Refer to host program and determine which equipment addresses are assigned to the coupler.
7. Select an equipment switch to be used (step 5) and set its host-assigned position (step 6) to ON.
8. Repeat step 7 for each assigned equipment switch.

NOTE

All equipment switches cannot be used. Those switches not in use must be set to OFF. No switch in use can have more than one position set to ON. No two switches can have the same position set to ON.

9. If two couplers are to be installed, repeat steps 1 through 8 for the second coupler.

RIBBON CABLES

1. Place synchronizer (figure 2-1) on a flat surface with its components facing up.
2. Connect three ribbon cables to synchronizer as follows (figure 3-3):

NOTE

If no modifications have been made to the coupler, omit steps 2a and 4a which install the J1 cable. The J1 cable is provided for spares.

   a. Plug cable 74845800 into J1 of synchronizer so that blue stripe is facing away from J2.
   b. Plug cable 74843700 into J2 of synchronizer so that blue stripe is facing J1.
   c. Plug cable 74843700 into J3 of synchronizer so that blue stripe is facing J2.

3. Place interface (figure 2-3) on top of synchronizer with components facing up so that J1 of the interface is directly over J1 of synchronizer.
4. Connect three ribbon cables to interface as follows (figure 3-3):
   a. Plug cable from J1 of synchronizer into J1 of interface.
   b. Plug cable from J2 of synchronizer into J2 of interface.
   c. Plug cable from J3 of synchronizer into J3 of interface.
5. If two couplers are to be installed, repeat steps 1 through 4 for the second coupler.

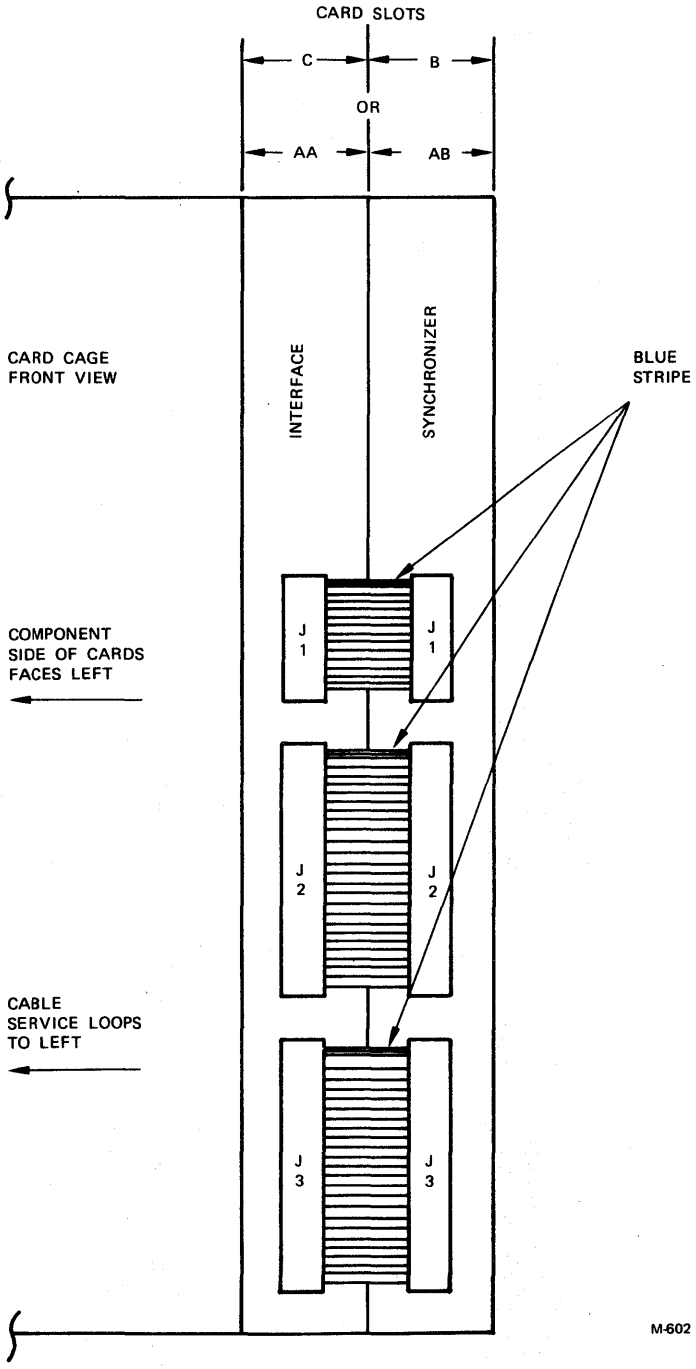


Figure 3-3. Ribbon Cables Installed

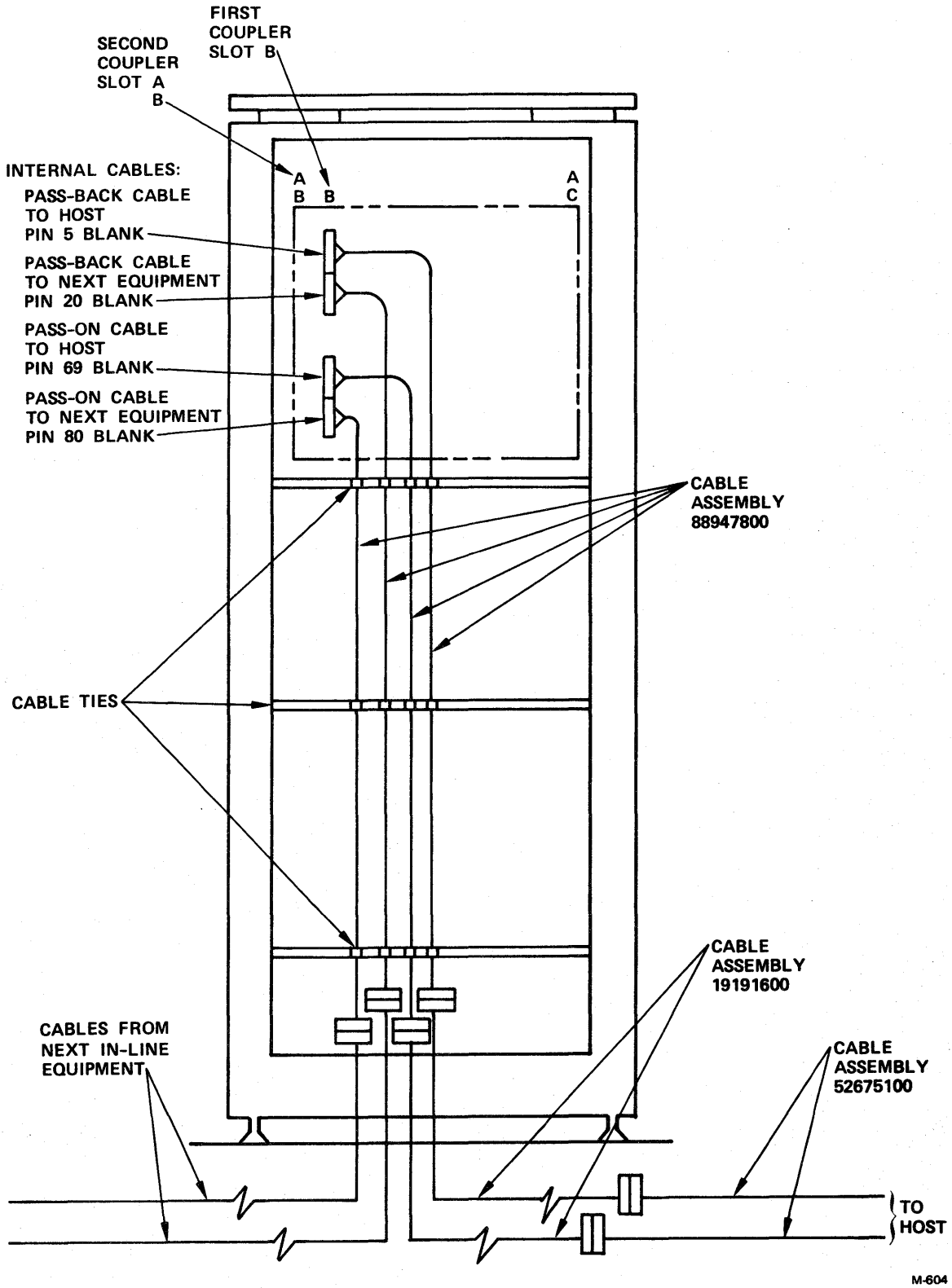


Figure 3-4. DY159-A Coupler Coaxial Cable Layout
(A Version Cabinet, Rear View)

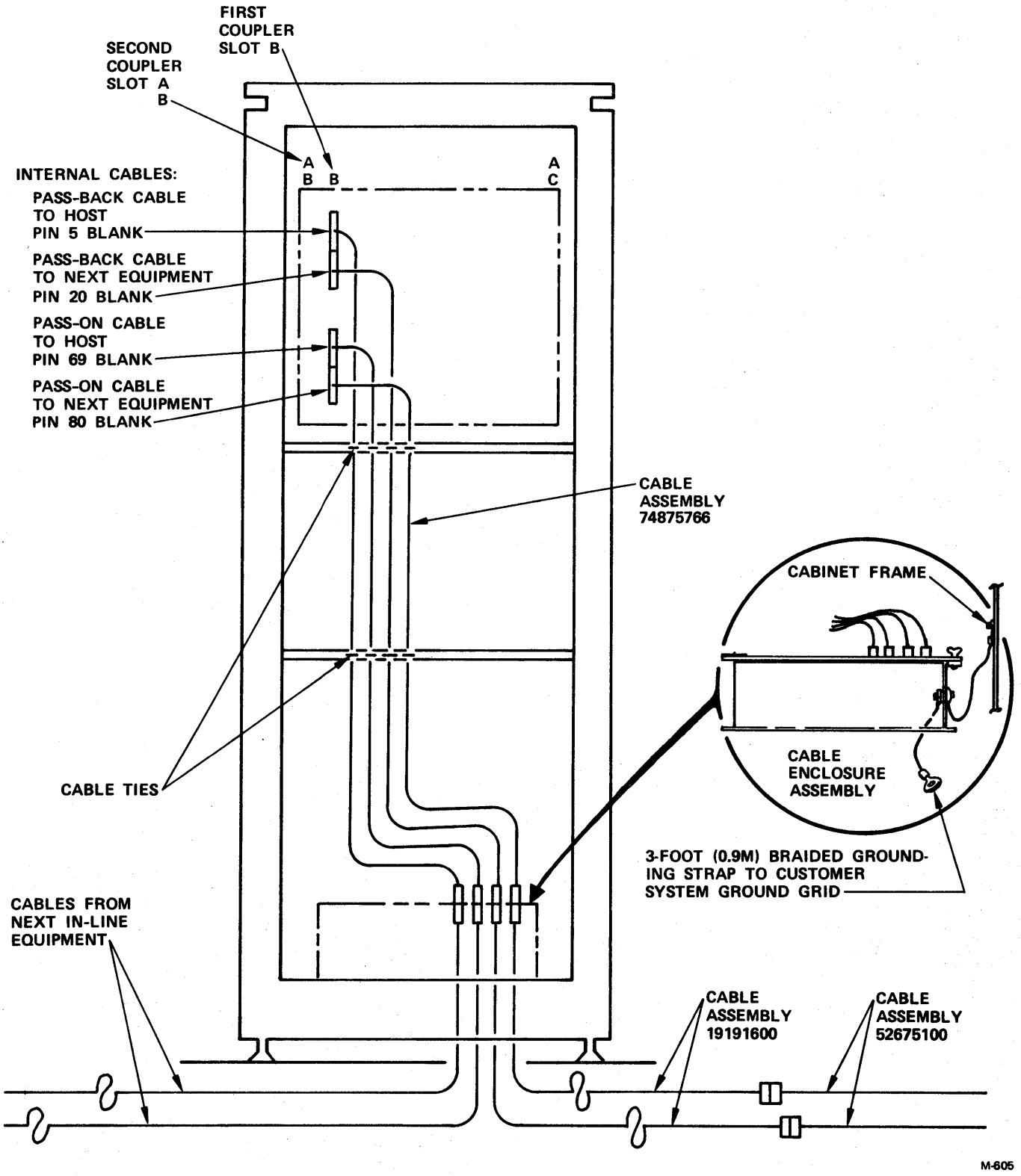


Figure 3-5. DY159-B Coupler Coaxial Cable Layout
(B Version Cabinet, Rear View)

CIRCUIT CARDS

1. Insert the two circuit cards into slots B and C of the card cage (figure 1-5). Continue insertion until connectors mate with connectors at rear of card cage.

2. If two couplers are to be installed, insert second coupler into slots AA and AB of card cage (figure 1-5). Continue insertion until tab connectors mate with connectors at rear of card cage.

COUPLER SELECT SWITCH

1. Refer to NPU program and determine which coupler address has been assigned to coupler 1.

2. Set coupler select switch S1 on coupler 1 (figure 2-3) to its assigned position: up for 2, down for 3.

3. If two couplers have been installed, set S1 of interface on coupler 2 to opposite position of S1 of interface on coupler 1.

CHECKOUT

After completing all installation procedures, perform subsystem diagnostics to check out the coupler. Refer to the NPU hardware maintenance manual for complete checkout procedures using the proper diagnostics.

The coupler temporarily stores data that is being transferred between the host and a terminal. At a precise time and under control of the host, it releases this data in the proper direction. The words input and output are always used in reference to the host. Thus output data travels from the host, through the coupler, to the processor, and eventually to a terminal. And input data comes from a terminal, eventually to the processor, through the coupler, and to the host.

This section contains descriptions of the circuits that make up the coupler. The theory of operation is divided into discussions of: the pass-on and pass-back block diagram; the coupler block diagram; and timing and control. Each circuit is discussed as a block within a block diagram. Detail circuit logic can be found on the logic diagrams of the two circuit cards: the synchronizer and the interface. A particular circuit can be located within the logic diagrams by referring to the block diagrams. A corner of each block contains the logic diagram sheet number. If the circuit is on the synchronizer, the number appears in the lower right-hand corner. If the circuit is on the interface, the number appears in the upper left-hand corner.

The distribution of signals to and from each circuit is shown on the block diagram. These signals are only described in this section when referring to their source or to their ultimate use. The number on the lines within the block diagram refer to the number of signals entering or leaving a particular block or circuit. Where no number is shown, only one signal is on that particular line.

To clarify the meaning of abbreviation, in the text and on logic diagrams, refer to the list of mnemonics in the appendix. Wherever a word or group of bits is described, bit zero is the least significant unless noted otherwise.

PASS–ON & PASS–BACK BLOCK DIAGRAM

The following paragraphs describe the functions of individual circuits within the pass-on and pass-back block diagram. These circuits form three major groups: the pass-on circuits, the pass-back circuits, and the clock circuits. To clarify the relationship of these circuits to one another, refer to figure 4-1.

PASS-ON CIRCUITS

Receivers, registers, and drivers constitute the pass-on circuits. The detail logic for all of these circuits is on synchronizer logic sheet 4. The pass-on cable to the host brings 19 lines into the coupler. Each of these lines connect directly to a receiver.

Receiver

The receiver converts the logic level from the host into TTL compatible levels. A logic 1 from the host is a positive pulse that is 25 to 40 ns wide and 1.3 V in amplitude. A logic 0 is merely the absence of a pulse. The receiver sends the converted pulse to a catch register.

Catch Register

The catch register captures the pulse from the host to enable the coupler to operate over a wide range of pulse widths and pulse skew. The catch register is connected to a transfer register.

Transfer Register

When a $\overline{T70}$ clock pulse occurs, the transfer register stores the signal for 100 ns, the time between clock pulses. During this time, the signal is made available to other coupler circuits and to a driver.

Only 18 of the 19 lines are made available to the other coupler circuits, as the coupler has no use for the parity signal. The coupler does use the 12 data lines and the 6 signals: active, inactive, full, empty, function, and master clear. These 18 lines plus the parity line are connected to drivers.

Driver

The driver converts the TTL level to the logic level compatible with the communication channel. A logic 1 is a positive pulse that is 35 ns wide and 1.4 V in amplitude. A logic 0 is merely the absence of a pulse. The driver is connected to the pass-on cable to the next equipment.

PASS-BACK CIRCUITS

Receivers, registers, drivers, and multiplexers constitute the pass-back circuits.

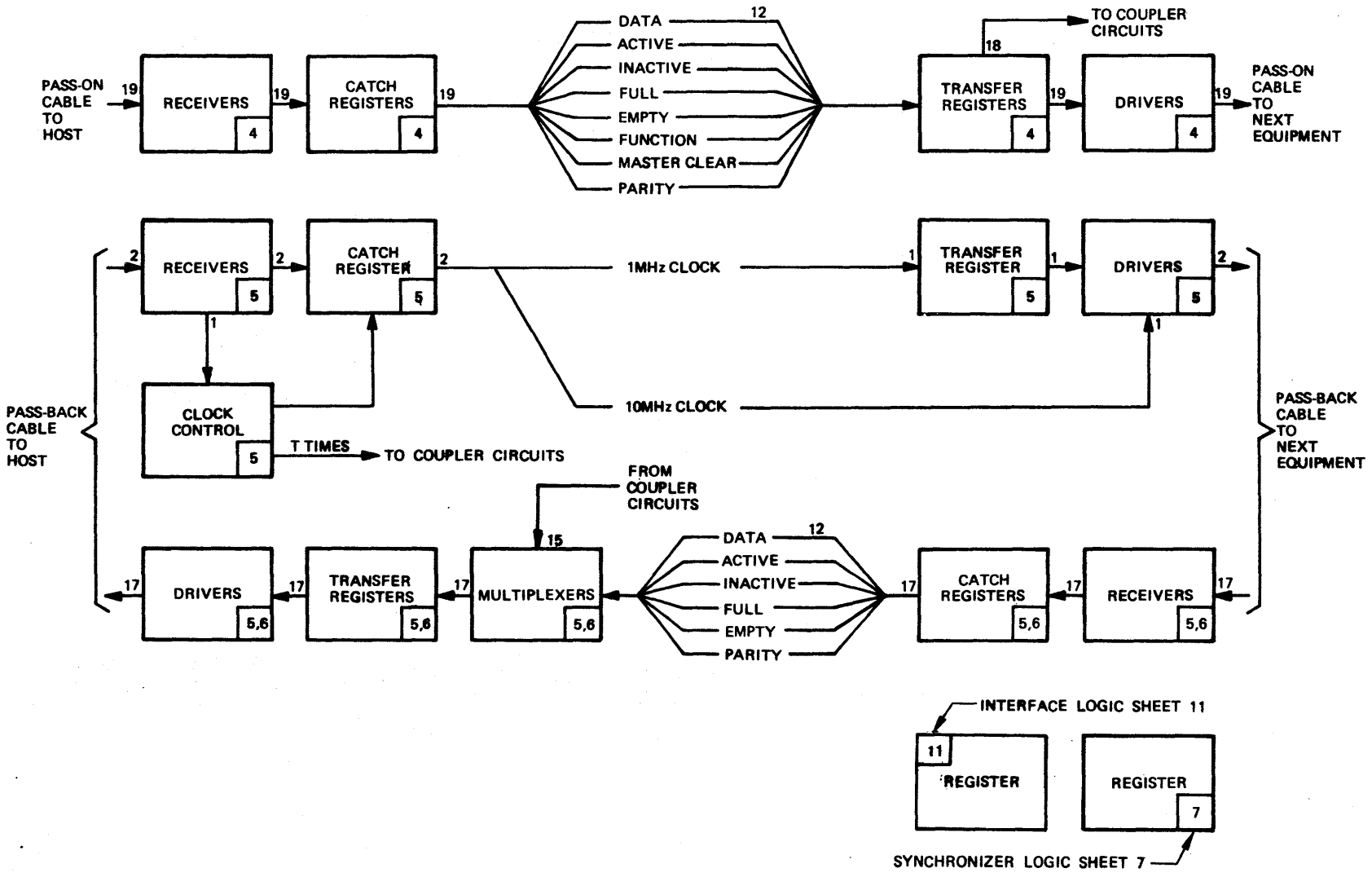


Figure 4-1. Pass-on and Pass-back Block Diagram

The pass-back cable to the next equipment brings 17 lines into the coupler. Each of these lines connect directly to a receiver.

Receiver

The receiver converts the logic level from the next equipment into TTL compatible levels. A logic 1 from the next equipment is a positive pulse that is 25 to 40 ns wide and 1.3 V in amplitude. A logic 0 is merely the absence of a pulse. The receiver sends the converted pulse to a catch register.

Catch Register

The catch register captures the pulse from the next equipment to enable the coupler to operate over a wide range of pulse widths and pulse skew. The catch register is connected to a multiplexer.

Multiplexers

From the catch registers, the multiplexers receive 12 data lines and 5 signals: active, inactive, full, empty, and parity. From other coupler circuits, they receive 12 data lines and 3 signals: inactive, full, and empty.

The data lines from the catch registers are connected by the multiplexer to transfer registers unless the coupler is selected for communication by the host. In this case a SENDF signal causes the multiplexer to disconnect data from the catch registers and connect data from the coupler circuits to the transfer registers.

The multiplexers handle the signal lines differently. Only the equipment that is communicating with the host will have high signals. Therefore, the multiplexers select signals from the coupler circuits or the catch register by connecting the high signals to the transfer registers.

Transfer Register

When a T70 clock pulse occurs. the transfer stores the signal for 100 ns, the time between clock pulses. During this time, the signal is made available to a driver.

Driver

The driver converts the TTL level to the logic level compatible with the communication channel. A logic 1 is a positive pulse that is 35 ns wide and 1.4 V in amplitude. A logic 0 is merely the absence of a pulse. The driver is connected to the pass-back cable to the host.

CLOCK CIRCUITS

Receivers, registers, drivers, and clock control constitute the clock circuits. The detail logic for all of these circuits is on synchronizer logic sheet 5. The pass-back cable to the host brings two lines, a 10 MHz clock and a 1 MHz clock, into the coupler. Each of these lines connect directly to a receiver.

Receiver

The receiver converts the logic level from the host into TTL compatible levels. The clock pulse from the host is a positive 1.3 V in amplitude and 35 ns wide. The receiver sends the converted pulse to a catch register. The receiver for the 10 MHz clock also sends the clock pulse to clock control.

Catch Register

The catch register captures the clock pulse to enable the coupler to operate over a side range of pulse widths and pulse skew. The catch register for the 1 MHz clock is connected to a transfer register.

Transfer Register

When a $\overline{T70}$ clock pulse occurs, the transfer register stores the 1 MHz clock pulse for 100 ns, the time between $\overline{T70}$ clock pulses. During this time, the 1 MHz clock pulse is made available to a driver.

Driver

The driver converts the TTL level to the logic compatible with the communications channel. The converted clock pulse is a positive 1.4 V in amplitude and 35 ns wide. The driver is connected to the pass-back cable to the next equipment. Both the 1 MHz and the 10 MHz clocks are sent to the next equipment 70 ns after they arrive from the host.

Clock Control

Clock control provides timing signals or clocks for all coupler operations. These clocks are derived from the 10 MHz clock. One adjustable delay circuit and one fixed delay line split the 100 ns period of the 10 MHz clock into 5 ns intervals. At each one of these intervals which are called T times, a 10 MHz positive-going clock pulse of 25 ns duration may be derived.

Only a few of the T times are used in the coupler and some of these are inverted or negative-going clocks. Whenever a clock is inverted, 5 ns is added to its T time. Some of the clocks used in the coupler are TO, T40, T90, $\overline{TO}$, $\overline{T35}$, and $\overline{T70}$.

There are two adjustments in clock control. Switch S5 provides for an adjustment of clock pulse width and a coarse adjustment of leading edge. Potentiometer R6 provides for a finer adjustment of the leading edge. Both of these controls are adjusted at the factory and should not be changed during installation. Clock pulse width is adjusted by setting to ON one of four S5 positions: A, B, C, or D. Leading edge is adjusted by setting to ON one of the other four S5 positions: E, F, G, or H.

COUPLER BLOCK DIAGRAM

The following paragraphs describe the functions of individual circuits within the coupler block diagram. These circuits form several major groups: the equipment address circuits; the memory address circuits; the data-to-memory circuits; the memory circuits. To clarify the relationship of these circuits to one another, refer to figure 4-2. This figure and the pass-on and pass-back block diagram contain all of the circuits that make up the coupler.

EQUIPMENT ADDRESS CIRCUITS

A decoder, 4 switches, a converter, and the select control constitute the equipment address circuits. The detail logic for all of these circuits is on synchronizer logic sheet 7. Circuit functions are shown on figure 4-3. The pass-on circuits send a function signal and 3 data lines to the decoder.

Decoder

From the transfer registers, the decoder receives the function signal and the 3 data lines that carry the equipment address. These lines, PO09X through PO11X, are decoded from binary to decimal. The 8 decimal outputs, 0 through 7, of the decoder are connected respectively to the 8 positions of each equipment switch. The one line that corresponds to the correct equipment address will have a signal transition from 1 to 0 when the function signal POFNX is high.

Equipment Switches

The four equipment switches have each been preset prior to installation. If any of them is set to the equipment address received from the decoder, this information is sent to the converter and select control.

Converter

If the converter receives a signal from the equipment switches, it converts that signal from decimal into binary. This 2-bit equipment address is sent to the F register to become signals FR09 and FR10. The number, 0 to 3, contained in these two bits correspond directly to the number assigned to one of four sets of terminals connected to the NPU. It is these four sets of terminals that are referred to as internal equipment. Address switches 1 through 4 are respectively related to internal equipments 0 through 3.

Select Control

The select control generates signal CSEL if the coupler has been selected to communicate with the host. A signal from any equipment switch would indicate that fact. Signal CSEL is sent to the F register to become signal FR11, and to coupler control where it enables the decoding of the function command.

MEMORY ADDRESS CIRCUITS

The F register, two ROMs, the counter, the MAB multiplexer, and 15 Y-line inverters constitute the memory address circuits. The pass-on circuits send 9 data lines to the F register. The equipment address circuits send an additional three delta lines to the F register.

F Register

The F register stores a 12-bit function word slightly modified from the one received from the host (figure 2-4). The equipment address circuits have converted the 3-bit equipment number, which was in bits 9 through 11, to a 2-bit equipment address. These two bits stored in bits 9 and 10, and the CSEL signal is stored in bit 11. The F register sends one or more of its bits, FR00 through FR11, to the ROMs, the counter, coupler control, and the MH register.

The ROMS

The two ROMs store starting locations for the coupler buffer. One ROM is for normal operation, and the other ROM is for maintenance. Each ROM depends on bits from the F register to determine which starting address it sends to the counter.

The operational ROM provides the starting address, location 0, for one of eight areas in the coupler buffer. Four of these areas store output data (from the host), and the other four areas store input data (from the processor). Two areas, input and output, are assigned to each equipment. Bits FR09 and FR10 select an equipment address from 0 through 3. Whether an input or an output area for that equipment is selected depends on the command in bits FR00 and FR01. Command 1 selects an output area; commands 2 and 3 select an input area. Figure 4-4 illustrates the eight areas addressed by the operational ROM and the signals required by the ROM to send an address to the counter. Each area in the coupler buffer contains 64 word locations.

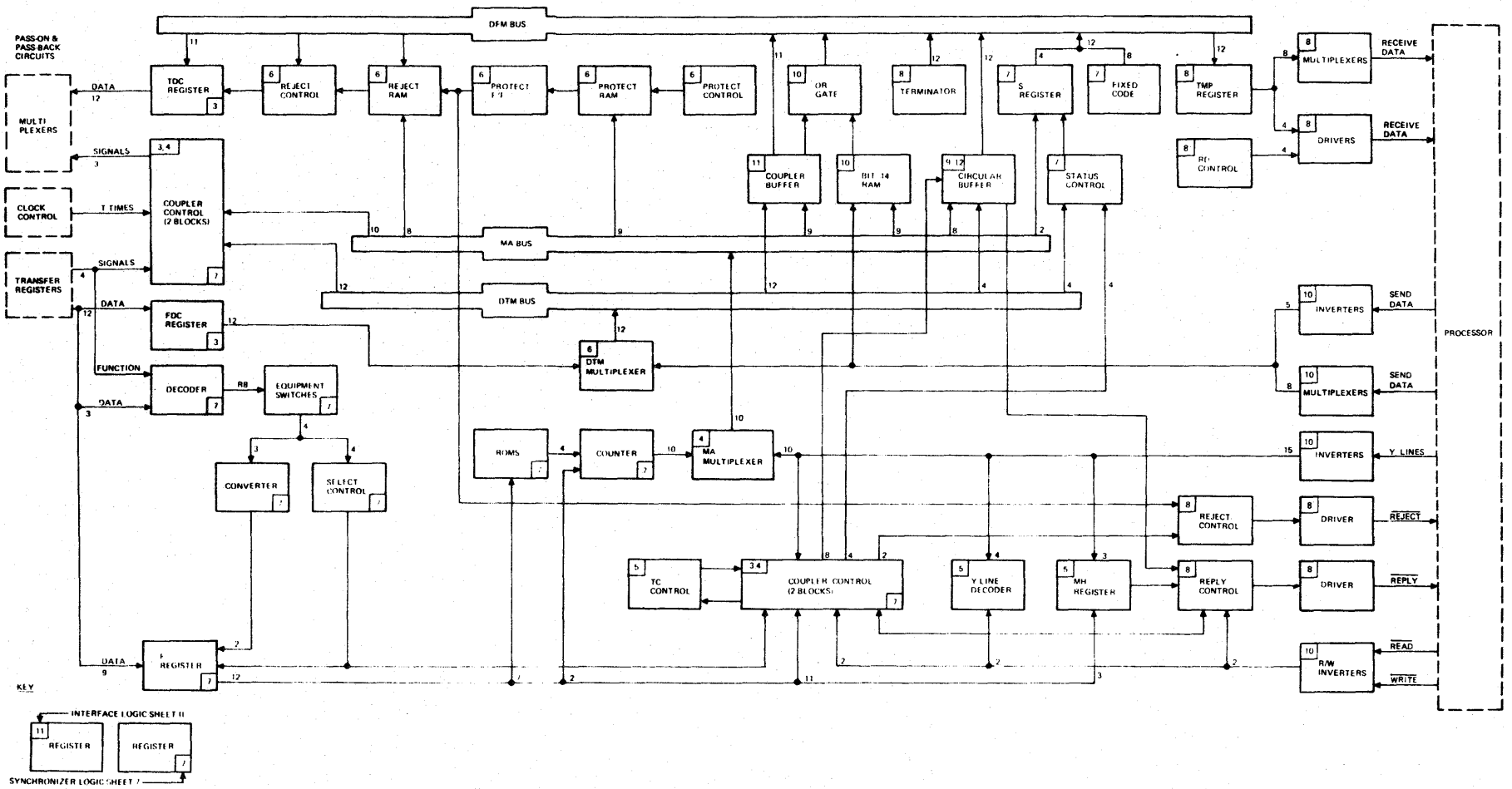


Figure 4-2. Coupler Block Diagram

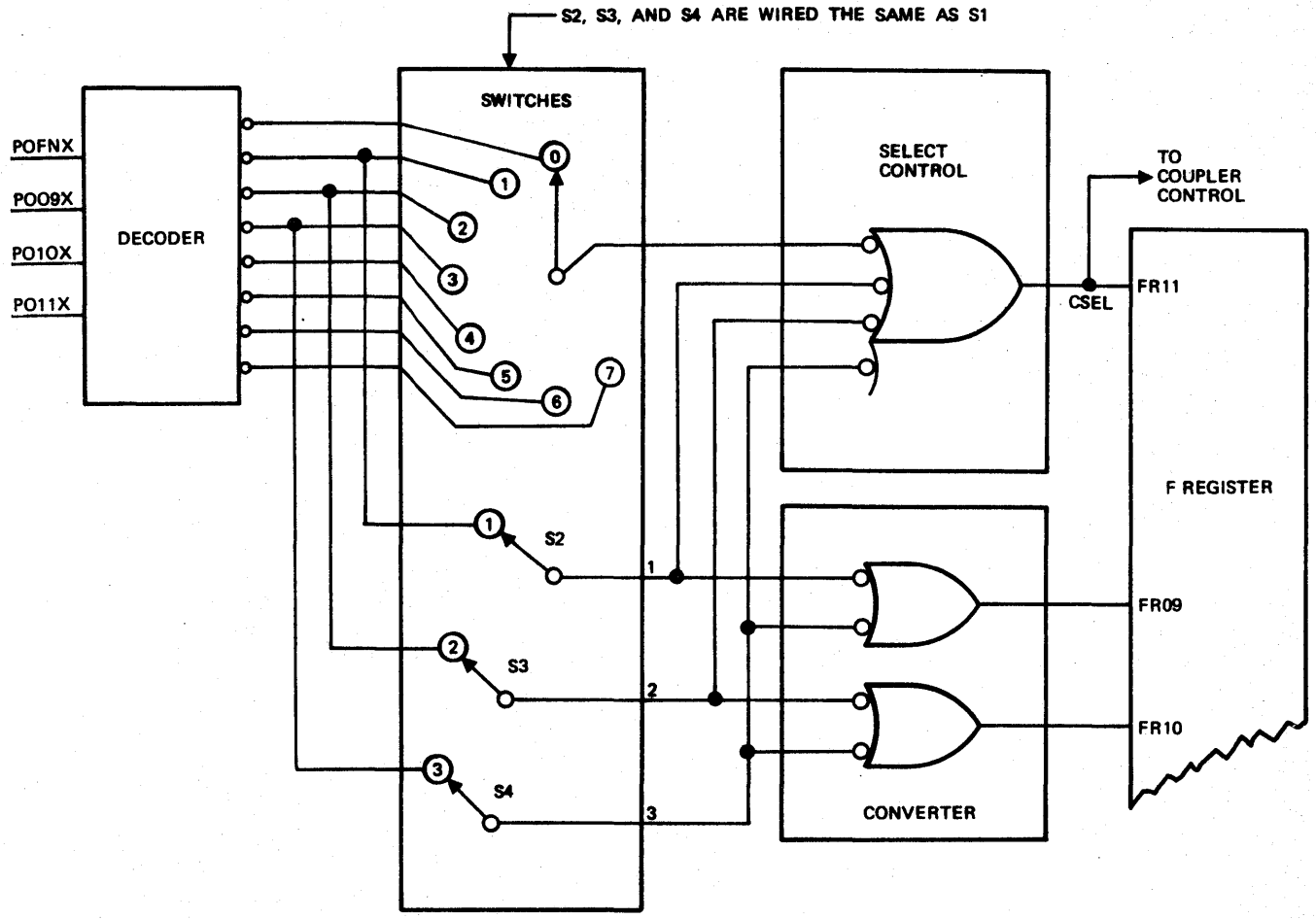


Figure 4-3. Equipment Address Circuits

The maintenance ROM provides the starting address, location 0, for one of 32 bytes in the coupler buffer. For the purpose of running diagnostics, the 128 word locations for each equipment have been divided into bytes of 16 locations each. These bytes are numbered 0 through 7. Bits FR09 and FR10 select an equipment address from 0 through 3. Bits FR03, FR04, and FR05 select a byte from 0 through 7. Figure 4-5 illustrates the 32 bytes addressed by the maintenance ROM and the signals required by the ROM to send an address to the counter.

Counter

The counter contains the address of data to be transferred into or out of the coupler buffer. This 10-bit binary counter parallel loads the starting address received from the ROM and is incremented following each read or write command from the host. Note that output data is a write command; also note that input data and send status are both read commands. The counter sends its 10 bits, MAC00 through MAC09, to the MAB multiplexer (figures 4-4 and 4-5).

MAB Multiplexer

The MAB multiplexer selects one of two addresses to be sent to the MA bus. One of these addresses is stored in the counter. The other address is on the Y lines from the processor. When the host accesses the coupler, the MAB multiplexer selects the address in the counter. When the processor accesses the coupler, the MAB multiplexer selects the address on the Y lines.

Each of the two address sources supply 10 bits of information to the MAB multiplexer.

A. ADDRESSED AREAS OF THE COUPLER BUFFER

EQUIPMENT 0 OUTPUT	EQUIPMENT 1 OUTPUT	EQUIPMENT 2 OUTPUT	EQUIPMENT 3 OUTPUT
EQUIPMENT 0 INPUT	EQUIPMENT 1 INPUT	EQUIPMENT 2 INPUT	EQUIPMENT 3 INPUT

NOTE Each area contains locations 0-63.

B. REQUIRED SIGNALS FOR ADDRESSING

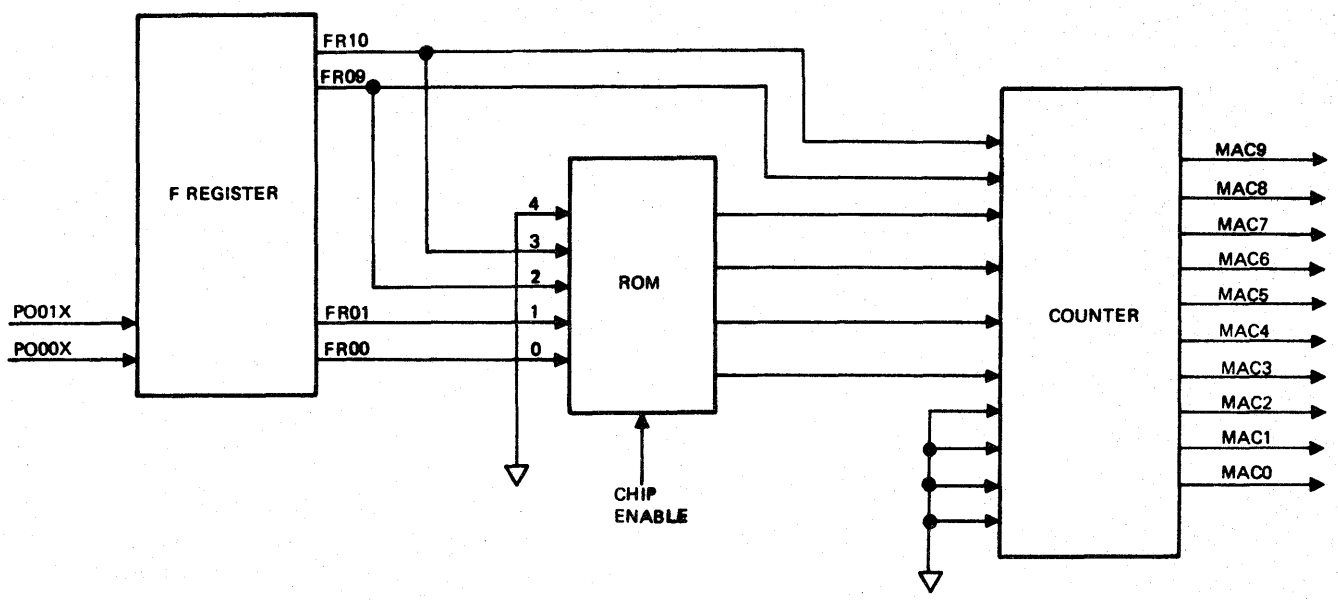


Figure 4-4. Operational ROM

A. ADDRESSED BYTES OF THE COUPLER BUFFER

EQUIPMENT: 0	1	2	3
BYTE 0	BYTE 0	BYTE 0	BYTE 0
BYTE 1	BYTE 1	BYTE 1	BYTE 1
BYTE 2	BYTE 2	BYTE 2	BYTE 2
BYTE 3	BYTE 3	BYTE 3	BYTE 3
BYTE 4	BYTE 4	BYTE 4	BYTE 4
BYTE 5	BYTE 5	BYTE 5	BYTE 5
BYTE 6	BYTE 6	BYTE 6	BYTE 6
BYTE 7	BYTE 7	BYTE 7	BYTE 7

NOTE: EACH BYTE CONTAINS LOCATIONS 0-15.

B. REQUIRED SIGNALS FOR ADDRESSING

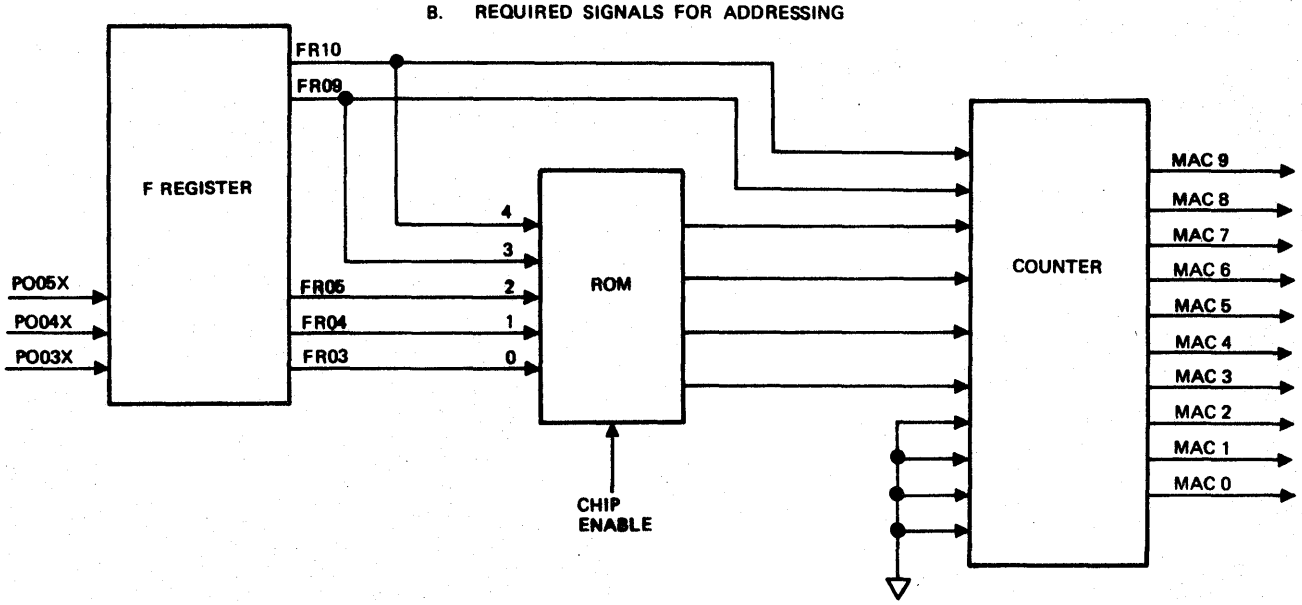


Figure 4-5. Maintenance ROM

The 10 address bits that are sent to the MA bus are shown in figure 4-6. Bit zero is the least significant. From the MA bus this address, MAB00 through MAB09, is distributed to the: reject RAM, protect RAM, bit 14 RAM, S register, coupler control, coupler buffer, and circular buffer. When the circular buffer is selected, the MAB lines contain data rather than an address. Figure 4-7 shows all uses of the MAB lines.

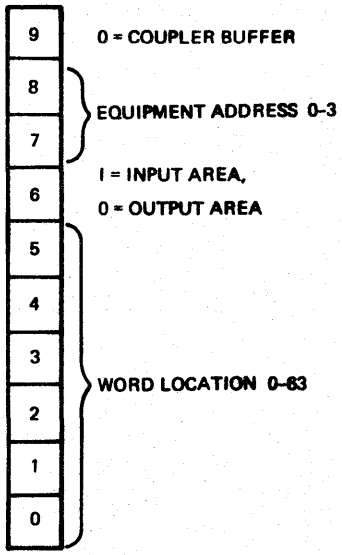


Figure 4-6. MAB Address Format

Y Lines

The Y lines bring addressing information from the processor into the coupler. These 15 Y-bits, $\overline{Y0}$ through Y14, are sent directly to inverters. Bit zero is the least significant.

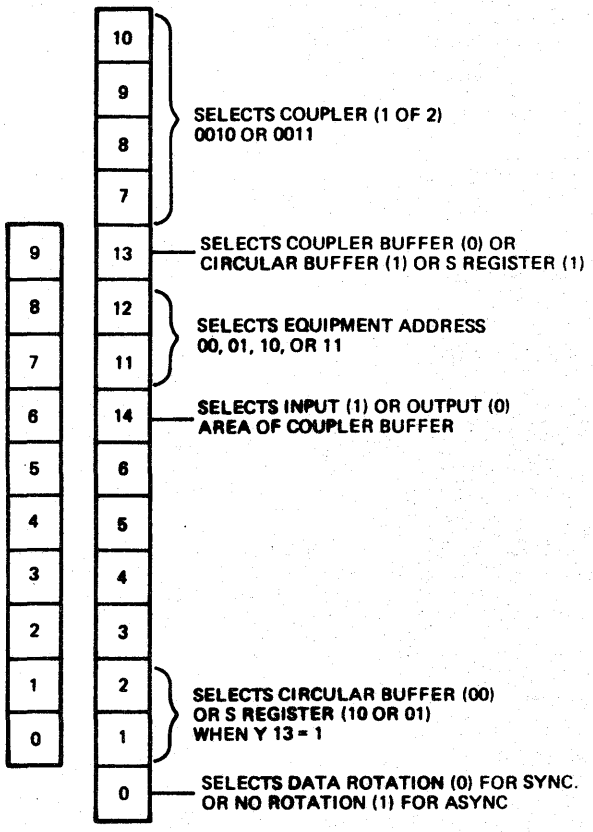


Figure 4-7. Uses of MAB and Y Lines

Inverter

The inverter receives a Y bit, inverts it, and sends it to one or more of four destinations. Ten Y bits go directly to the MAB multiplexer. Three of these same ten bits are used by the MH register. Coupler control uses Y0, and the decoder uses Y7 through Y10 (figure 4-7).

DATA TO MEMORY CIRCUIT

The FDC register, the DTM multiplexer, and the send data inverters and multiplexers constitute the data-to-memory circuits. The pass-on circuits send 12 data lines to the FDC register.

FDC Register

The FDC register holds 12 bits of data from the host. These 12 bits, P000X through P011X, come directly from the transfer registers. These same 12 bits change to FDC0 through FDC11 before they are sent to the DTM multiplexer.

DTM Multiplexer

The DTM multiplexer selects one of two sets of data to be sent to the DTM bus. One set of data is held in the FDC register. The other data is on the FMP lines from the processor. When the host accesses the coupler, the DTM multiplexer selects the data in the FDC register. When the processor accesses the coupler, the DTM multiplexer selects the data on the FMP lines. Each of the two data sources supply 12 bits of information to the DTM multiplexer. The 12 data bits that are sent to the DTM bus are DTM00 through DTM11.

FMP Lines

The FMP lines do not bring data directly from the processor but via inverters and multiplexers. The SD lines from the processor bring the data into the coupler. SD bits 1 through 8 go to multiplexers; 9 through 12 and 15 go to inverters.

Inverters

The inverters receive $\overline{SD09}$ through $\overline{SD12}$ and $\overline{SD15}$, invert each of these data lines, and send FMP08 through FMP11 to the DTM multiplexer. Note that the FMP data bits are renumbered by subtracting one from the number of each corresponding SD bit. Bit $\overline{SD15}$ is inverted and sent to the bit 14 RAM.

Multiplexers

The multiplexers either sends the data on the SD lines directly to the DTM multiplexer or rotates the data before sending it. See figure 4-8. Whether bits SD01 through SD08 are rotated or not depends on whether or not the host is communicating with an asynchronous terminal. The selection of direct data or rotated data is controlled by signal Y0.

MEMORY CIRCUITS

The coupler buffer, the bit 14 RAM, the circular buffer, the protect RAM, and the reject RAM constitute the memory circuits. With the exception of the circular buffer, each of these circuits receive an address from the MA bus.

Coupler Buffer

The coupler buffer is a random access memory with capacity for 512 12-bit words. It can be addressed by the host or by the processor. For the purpose of addressing, the coupler buffer is divided into 8 areas: one input area and one output area for each of 4 equipments (figure 4-4). Each of the 8 areas contain 64 word locations.

The 9 MAB bits address one of the 512 locations in the coupler buffer. Then the 12 bits of data on the DTM bus may be written into the addressed location and stored until needed. Or data may be read from the selected location and sent to the DFM bus. Data from the coupler buffer to the DFM bus is contained in bits DFM0 through DMF9 and bit DFM11. An additional bit, CBM10, is ORed with the CBM14 to become bit DFM10.

When diagnostics are being performed on the NPU, the coupler buffer is divided into 32 bytes: 8 bytes for each of 4 equipments (figure 4-5). Each of the 32 bytes contain 16 word locations.

Bit 14 RAM

The bit 14 RAM is a random access memory with capacity for 512 single bits. It receives the result of ANDing signals $\overline{SD15}$ and $\overline{MPWC}$. This result is written into the location addressed by the 9 MAB bits. When data is read from the bit 14 RAM, signal CBM14 is sent from the selected location to an OR gate where it is ORed with signal CBM10. The resultant signal DFM10, is sent to the DFM bus.

Circular Buffer

The circular buffer is a random access memory with capacity for 256 12-bit words. It is addressed by the 8 CBA bits from coupler control. Figure 4-9 shows a partial block diagram of coupler control. The CBA lines originate in one of two counters selected by the CBA multiplexer. Both counters are returned to zero by the processor during an initialization process. After the host

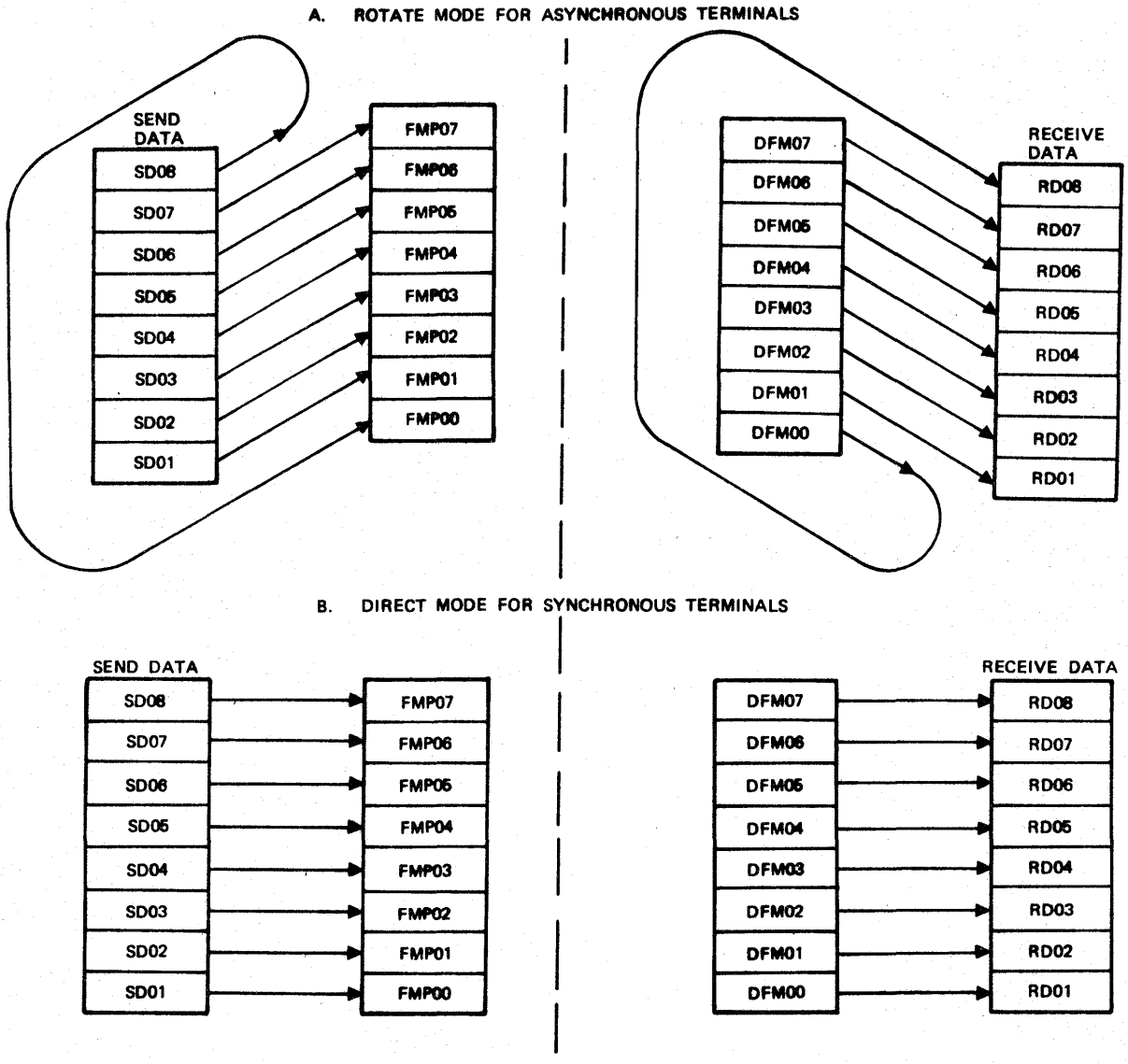


Figure 4-8. Send and Receive Data Modes

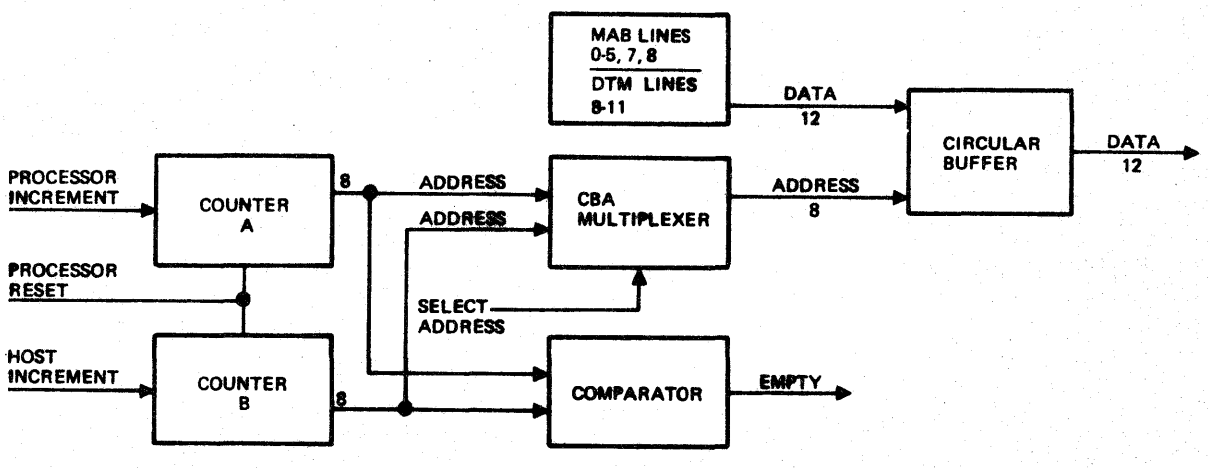


Figure 4-9. Signals of Circular Buffer

writes into the circular buffer, counter A is incremented. After the processor reads the output data, counter B is incremented. Under the direction of memory cycle control, the CBA multiplexer selects one of these counters as the source for an address. A comparator determines whether the circular buffer is full or empty and sends this information to the processor.

The 12 data bits received by the circular buffer come from the MAB and DTM lines. MAB lines 0 through 5 and 7 and 8 locate the area of the coupler buffer that has output data being written ito it (figure 4-7). DTM lines 8 through 11 are I/O control bits. The format of the data bits in the circular buffer is shown in figure 4-10.

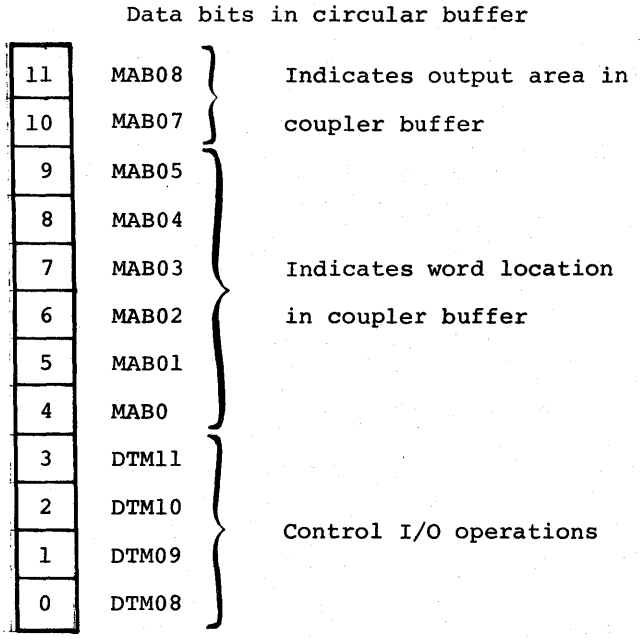


Figure 4-10. Word Format in Circular Buffer

Protect RAM

The protect RAM is a random access memory with capacity for 512 single bits. Whenever data is written into the coupler buffer, signal PROT is written into the protect RAM location addressed by the 9 MAB bits. This signal is generated in protect control. From the protect RAM signal PROT is used to set the protect flip-flop, which then sends signal $\overline{\text{PROTF}}$ to the reject RAM.

Reject RAM

The reject RAM is a random access memory with capacity for 256 single bits. When output data is written into the coupler buffer, signal $\overline{\text{PROTF}}$ is written into the reject RAM location addressed by the 8 MAB bits. Note that MAB06 is not needed. During a read cycle by the host, the reject signal in the selected location is sent to reject control. There it is ORed with signal DFM8, and the resultant signal, DFM8M, is sent to the TDC register.

DATA FROM MEMORY CIRCUITS

The RCD register, the S register, the TMP register, a terminator, RD control, and receive data multiplexers and drivers constitute the data from memory circuits. The DFM bus sends 11 lines of data to the TDC register. An additional line of data is sent from reject control.

TDC Register

The TDC register stores a 12-bit word that is to be transferred to the host. Its immediate destination is the multiplexers in the pass-back circuits. These 12 bits are TDC00 through TDC11. The TDC register receives its word from one of two sources: the coupler buffer or the S register.

S Register

The S register stores 4 bits of the status word: bits 0, 1, 4 and 5 (figure 2-5). It has four sections which correspond to the four equipments, 0 through 3. When a send status command is received from the host, status control selects the proper section of the S register. The pertinent 4 bits are then sent to the DFM bus. The other 8 bits that make up the status word are a fixed code.

The processor can also access the S register. A request for status from the processor is handled in the same manner as one from the host. In this case the destination of the status word would be the TMP register.

TMP Register

The TMP register stores a 12-bit word that is to be transferred to the processor. Its immediate destination is the multiplexers and drivers for the receive data lines. The TMP register receives its word from one of three sources: the circular buffer, the coupler buffer, or the S register.

Drivers

The drivers receive the upper 4 bits from the TMP register and the 4 upper most bits of the RD lines from driver control. Each driver inverts its data bit and sends it to the processor on an RD line. The 8 bits from the drivers are $\overline{\text{RD09}}$ through $\overline{\text{RD16}}$.

Multiplexers

The multiplexers either sends the data directly out on the RD lines or rotates the data before sending it (figure 4-8). Whether bits $\overline{RD0I}$ through $\overline{RD08}$ are rotated or not depends on whether or not the host is communicating with an asynchronous terminal. The selection of direct data or rotated data is controlled by signal Y0.

Terminators

The DFM bus is terminated through resistors to plus five volts at the terminator.

CONTROL CIRCUITS

The coupler control, TC control, the Y-line decoder, the MH register, reject control and driver, reply control and driver, and the R/W inverters constitute the control circuits. Most of the operations that take place in the coupler are controlled by circuitry of the coupler control.

Coupler Control

Coupler control receives T times from clock control, signals from transfer registers and Y lines, and several other signals from within the coupler. With these control and timing signals, coupler control establishes the direction of data flow between the host and the processor.

Either the processor or the host may request a memory cycle or both requests may come simultaneously. In any case, only one is allowed at one time. In the case of simultaneous requests, the processor must wait up to 450 ns until the host's request has been serviced. When one of these requestors is allowed access, coupler control sends a signal to the MAB and DTM multiplexers that selects the proper source of address and data.

TC Control

TC control counts the number of locations read in the coupler buffer until the maximum is reached. When the terminal count is complete for that particular equipment, signal TCC is generated. See figure 4-11. A counter supplies inputs to two gates: a 64 count and a 16 count. One gate is enabled by an operational read from the host. The other gate is enabled by a maintenance read from the host. When 64 locations have been read during normal operations, the TCC flip-flop is set and signal TCC is generated. Reading 16 locations during diagnostics causes the setting of the TCC flip-flop. Signal TCC clears the F register and inhibits write enable to the coupler buffer. The counter is incremented by signal MACI which also increments the counter in memory address circuits. The counter is cleared by signal TCC or by a new function word.

Y-Line Decoder

The Y-line decoder receives signals Y07 through Y10 and decodes them to select one of two couplers. The coupler select switch has been set to the position assigned by the processor. This position is either address 2 or address 3. If the hexidecimal address on the Y lines is the same as the address of the positioned switch, this coupler is selected for processor operations. The presence of a write or read signal along with the proper address indicates that the processor desires communication.

R/W Inverters

An inverter receives the read signal from the processor, inverts it, and sends it to coupler control and other circuits. An identical inverter treats the write signal in an identical manner.

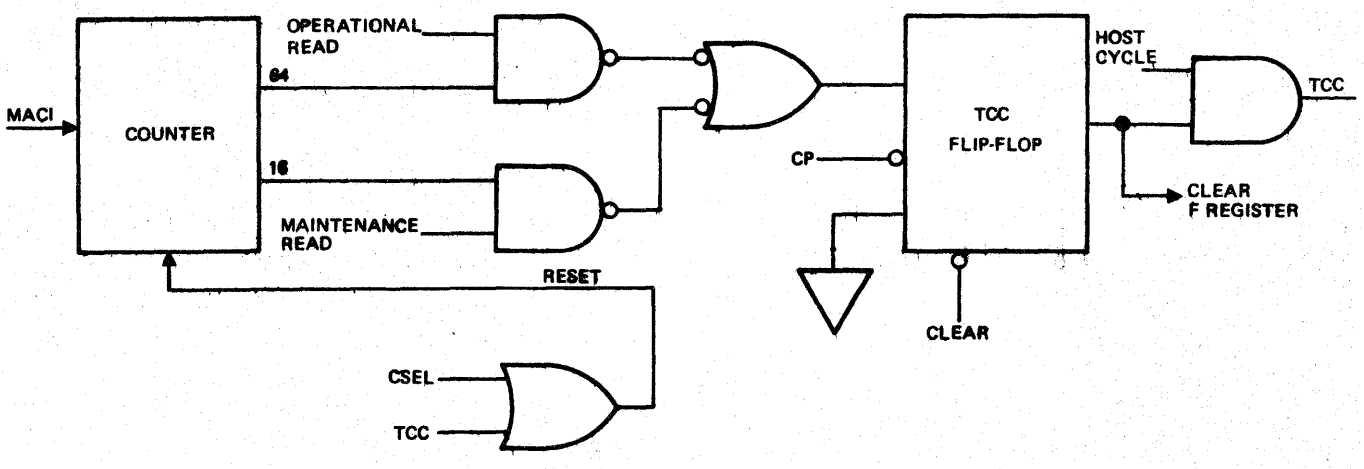


Figure 4-11. Terminal Count Logic

MH Register

The MH register stores signal FR08 in one of four sections that correspond to the four equipments. During diagnostics this signal holds the coupler buffer for maintenance tests (figure 2-4). The state of the MH register is sent to reply control where a negative reply is generated in response to an access request from the processor.

Reply Control

Reply control answers a request from the processor with either a positive or a negative reply. The types of requests are: read the coupler buffer, write in the coupler buffer, write in the status register, and read the circular buffer. Reply control sends a negative response to a read or write request for the coupler buffer when the MH bit is set. The processor also gets a negative response to a request to read the circular buffer when the circular buffer is empty. Signal REPLY is sent through a driver to the processor.

Controlware interprets the RD lines to determine the reply from the coupler. When a negative response is sent, all 16 RD lines are at the 0 level. This is read as a hexidecimal 0000. When a positive response is sent, a hexidecimal Fxxx is on the RD lines: $\overline{RD13}$ through $\overline{RD16}$ are set to the 1 level.

Reject Control

Reject control contains the reject flip-flop which is set during a processor write request if the protect bit is set. The state of the reject flip-flop is sent through a driver to the processor as signal $\overline{REJECT}$.

MEMORY CYCLE FLOW DIAGRAM

The following paragraphs describe the sequence of events within the memory cycle flow diagram. These events form four major groups: processor write cycle, processor read cycle, host write cycle, and host read cycle. To clarify the relationship of these events to one another, refer to figure 4-12.

To better understand the overall operation of the coupler, a short review is given here of some pertinent facts. The coupler is a slave to the programs of the host and the processor. Its task is to transfer data between the host and the proceseor upon command. The coupler and the processor are merely parts of the NPU which enables the host to communicate with up to 256 terminals. Up to 64 of these terminals are assigned to one of four equipments. When data is transferred, it is done a block at a time. That is, one character from or to each of 64 terminals is transferred in a block of data.

Either the processor or the host may request a memory cycle or both requests may come simultaneously. In any case only one is allowed at one time. In the case of simultaneous requests, the processor must wait until the host's request has been serviced. The memory that is being accessed is the coupler buffer and related memories within the coupler.

PROCESSOR WRITE CYCLE

From the start of the flow diagram, the first decision is whether or not the host or the processor is selecting. If the answer is neither, then return to start. If the answer is yes, it must be decided which of the two is selecting to communicate. Assume for now that the processor selects the coupler.

Do negative response conditions exist? If the answer is yes, send a hexidecimal 0000 back to the processor and return to start. If the circular buffer is not empty and there is not a maintenance hold on the coupler, then answer will be no. The processor then requests a memory cycle.

The processor may be locked out from accessing the coupler buffer because the host is being serviced. If it is, it will continually ask whether it is locked out until the answer is no. Then the memory cycle will start and the host will be locked out. The next decision is whether a read or write cycle is desired. Assume for now that the processor requests a write cycle.

Is the S register selected? Does the processor wish to store status? If the answer is yes, the data on the FMP lines are stored in the S register. If the answer is no, another decision is made.

Is the protect flip-flop set? If the data character previously written into memory has not been ready by the host, the answer will be yes. This data must be protected; therefore, further writing is inhibited at this point in time. A reject is sent to the processor, and host access to memory is unlocked. If the protect flip-flop is not set, the data on the FMP lines are stored in input areas of the coupler buffer. Host access is then unlocked, and a positive reply of hexadecimal Fxxx is sent to the processor.

PROCESSOR READ CYCLE

Is a read cycle or a write cycle desired by the processor? Assume for now that the processor requests a read cycle. The circular buffer is read. Then the output

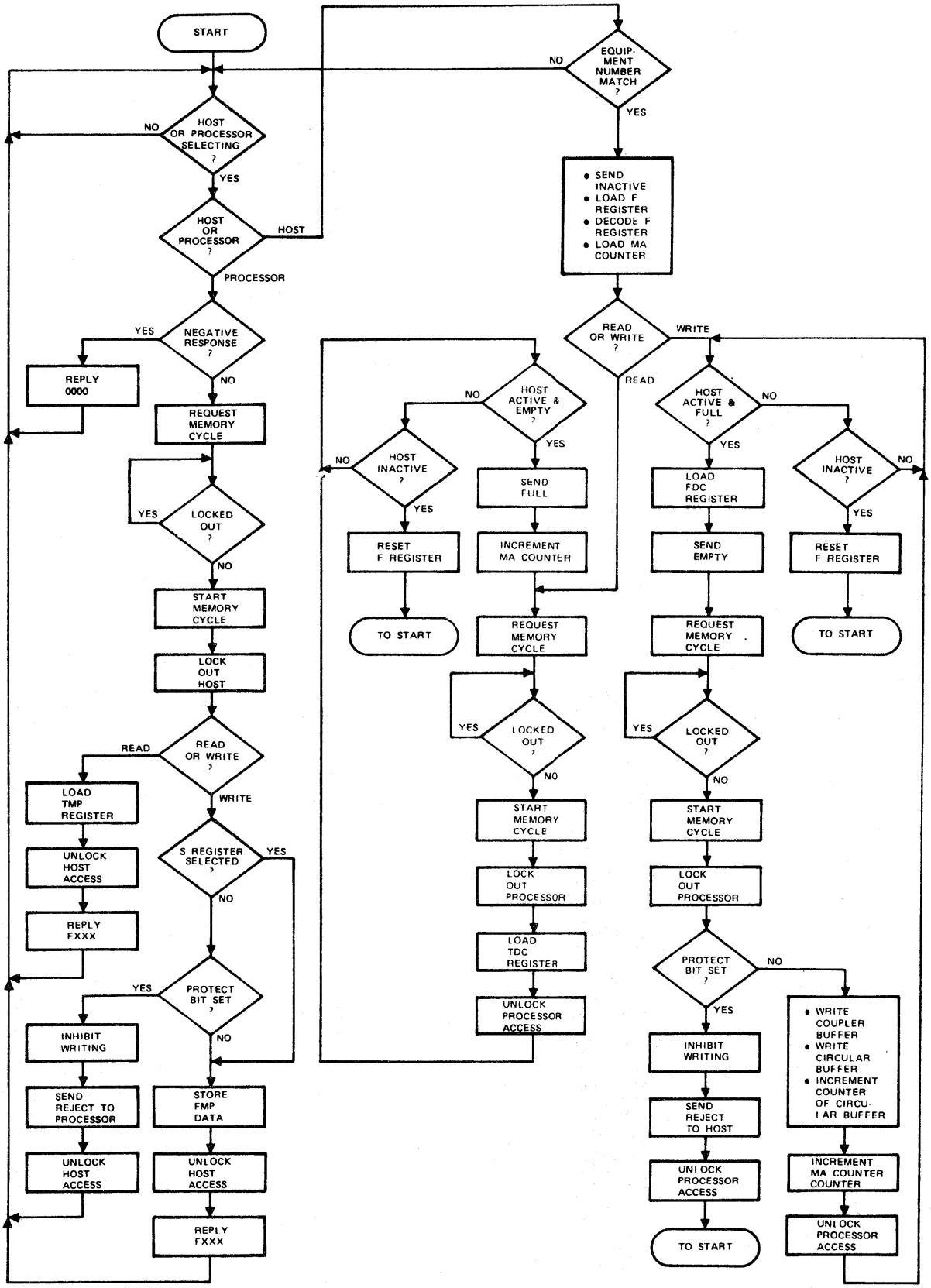


Figure 4-12. Memory Cycle Flow Diagram

areas of the coupler buffer are read and loaded into the TMP register. After memory has been read, the processor clears both the coupler buffer and the protect RAM. Host access is then unlocked, and a positive reply of hexidecimal Fxxx is sent to the processor.

HOST WRITE CYCLE

Is it the host or the processor that is selecting? Assume for now that the host is selecting. Is there a match between the equipment number sent by the host and the equipment number assigned to the coupler? If the answer is no, ignore the host and return to start. If the answer is yes, load the F register with the function word and send an inactive signal back to the host. Also decode the function word and load the MA counter with a memory address. The next decision is whether a read or write cycle is desired. Assume for now that the host requests a write cycle.

Has the host sent an active signal and a full signal? If the answer is no, has the host sent an inactive signal signifying the end of communications? If an inactive signal has been received, reset the F register and go back to start. If an inactive signal has not been received, recheck for active and full signals. If these two signals are present, load data into the FDC register and send an empty signal to the host. The host will then request a memory cycle.

The host may be locked out from accessing the coupler buffer because the processor is being serviced. If it is, it will continually ask whether it is locked out until the answer is no. Then the memory cycle will start and the processor will be locked out.

The next question is whether or not the protect flip-flop has been set. If the data character previously written into memory has not been read by the processor, the answer will be yes. This data must be protected; therefore, further writing is inhibited at this point in time. A reject is sent to the host, and processor access to memory is unlocked. If the protect flip-flop is not set, data is wrtten into the output areas of the coupler buffer. Information is also written into the circular buffer, and the counter of the circular buffer is incremented. The MA counter is then incremented, and the processor access to memory is unlocked.

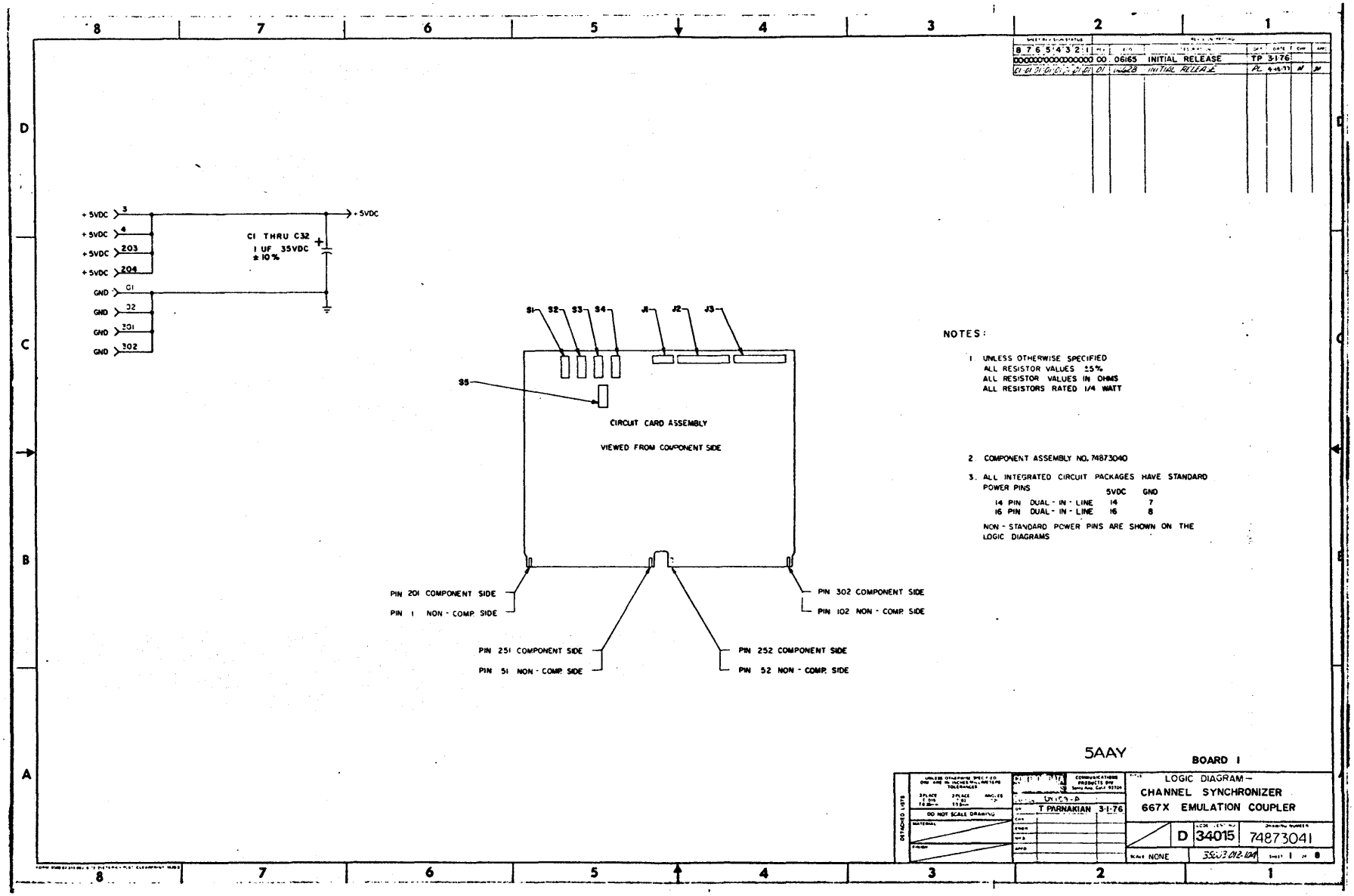
HOST READ CYCLE

Is a read cycle or a write cycle desired by the host? Assume for now that the host requests a read memory cycle. If the host is not locked out, a memory cycle will start and the processor will be locked out. Data from an input area of the coupler buffer or status from the status register will be loaded into the TDC register. After memory has been read, the host clears both the coupler buffer and the protect RAM. Processor access to memory is then unlocked.

Has the host sent an active signal and an empty signal? If the answer is no, has the host sent an inactive signal signifying the end of communications? If an inactive signal has been received, reset the F register and go back to start. If an inactive has not been received, recheck for active and empty signals. If these two signals are present, send a full signal to the host and increment the MA counter. The memory cycle request will then be serviced as in the previous paragraph.

There are two versions of the coupler. Logic diagrams for both versions are included in this section. When using the diagrams as a trouble-shooting aid, verify that the component locators on the circuit card agree with those on the logic diagram.

The logic diagram for the first version of the synchronizer is drawing number 74850100. The logic diagram for the first version of the interface is drawing number 74846100. The second version of the coupler is logically shown in drawings numbered 74850101 and 74846101.



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTOR VALUES ±5%
   ALL RESISTOR VALUES IN OHMS
   ALL RESISTORS RATED 1/4 WATT

2. COMPONENT ASSEMBLY NO. 74873040

3. ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS

	5VDC	GND
14 PIN DUAL-IN-LINE	14	7
16 PIN DUAL-IN-LINE	16	8

NON-STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS

SHEET REVISION STATUS	REVISIONS				
8 7 6 5 4 3 2 1	REV	ECO	DESCRIPTION	DATE	APPD
00000000000000	00	06165	INITIAL RELEASE	TP 3-1-76	
01 01 01 01 01 01 01 01	01	[illegible]	INITIAL RELEASE	PL 4-16-76	

5AAY

BOARD 1

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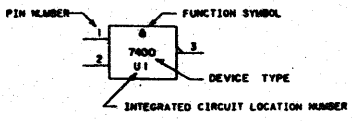
DO NOT SCALE DRAWING	UNLESS - A	
MATERIAL	T PARNAKIAN 3-1-76	
FINISH		D 34015 74873041
DETACH & LIFT		SCALE NONE 35033012-104 SHEET 1 OF 8

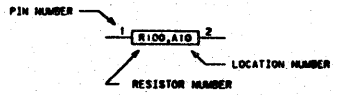
6650

REVISIONS					
REV	ECO	DESCRIPTION	DFT	DATE	LTR
		SEE SHEET 1			

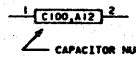
CIRCUIT ELEMENT SYMBOLOGY

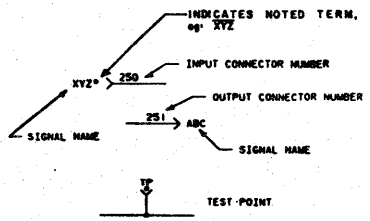


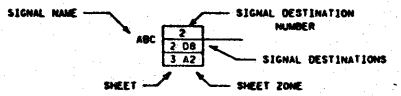
RESISTOR INTEGRATED SYMBOLOGY



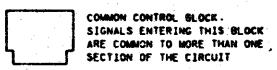
CAPACITOR INTEGRATED SYMBOLOGY

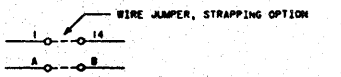


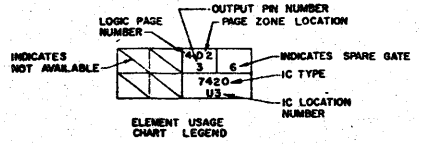




N/C DENOTES NO CONNECTION







IDENTIFIER LIST

CDC ELEMENT IDENTIFIER	VENDOR TYPE NUMBER	FUNCTION
	74S00	TTL QUAD 2-INPUT NAND
	74S02	TTL QUAD 2-INPUT NOR
	74SC3	TTL QUAD 2-INPUT NAND (C-EN COLL)
	74S04	TTL HEX INVERTER
	74S08	TTL QUAD 2-INPUT AND
	74S10	TTL TRIPLE 3-INPUT NAND
	74S20	TTL DUAL 4-INPUT NAND
	74S40	TTL DUAL 4-INPUT NAND BUFFER
	74S74	TTL DUAL T-TYPE F/F
	74S112	TTL DUAL J-K NEG F/F
	74S139	DECODER, TTL (1 OF 8)
	74S157	MUX, TTL QUAD 2 INPUT
	74S174	LATCH, TTL 6-BIT D-TYPE
	74S175	LATCH, TTL 4 BIT D-TYPE
	74S16	COUNTER, TTL 4 BIT BINARY
	7413	SCHMITT TRIGGER, TTL DUAL NAND
	74S03	LINE DRIVER, QUAD 2-INPUT NOR
	5610	MEMORY, TTL ROM

QUALIFYING FUNCTION SYMBOLS

SYMBOL	DESCRIPTION
&	AND ALL INPUTS ACTIVE
1	ONE OR MORE (OR) ANY INPUT ACTIVE
≥2	TWO OR MORE INPUTS ACTIVE
=1	ONLY ONE INPUT ACTIVE (EXCLUSIVE OR)
=	ALL INPUTS EQUAL
=2	ONLY TWO INPUTS ACTIVE, NO MORE, NO LESS
G	GENERATOR OR OSCILLATOR (WAVEFORM MAY BE ADDED)
⊓	SCHMITT TRIGGER
1⊓	ONE-SHOT MULTIVIBRATOR
⊢	TIME DELAY
00	EVEN PARITY
000	ODD PARITY
X→Y	X INPUTS, DECODED OR ENCODED TO, Y OUTPUTS
X/Y	X INPUT LEVEL CONVERTED TO Y OUTPUT LEVEL
Σ	ARITHMETIC SUMMING CIRCUIT
F	COMPLEX FUNCTION

INPUT / OUTPUT DESIGNATORS

R	RESET
S	SET
G	GATING TYPE INPUT THAT OFFSETS OTHER INPUTS OR OUTPUTS
J	J INPUT OF J-K FLIP FLOP
K	K INPUT OF J-K FLIP FLOP
T	TOGGLE OR COMPLEMENT INPUT
D	DATA INPUT OF TYPE FLIP FLOP
C	GATING (CLOCK) INPUT FOR A "D" INPUT ONLY
L	USED ONLY WITH INHIBIT INPUT: ALL LOW STATE OUTPUTS ARE INHIBITED
H	USED ONLY WITH INHIBIT INPUT: ALL HIGH STATE OUTPUTS ARE INHIBITED
⌝	DELAY INDICATOR, FOR OUTPUT HAVING INPUT CONTROLLED DELAY
E	EXTENDER FOR EXPANDING THE NUMBER OF INPUTS
⊐	INDICATES GROUPED INPUTS THAT MAINTAIN FIXED RELATIONSHIP
C	INDICATES GROUPED OUTPUTS
→	SHIFT RIGHT (OR DOWN)
←	SHIFT LEFT (OR UP)
+1	INCREASE CONTENTS BY ONE (COUNT UP)
−1	DECREASE CONTENTS BY ONE (COUNT DOWN)
1, 2, 4, 8	INDICATES RELATIVE WEIGHTING OF INPUTS OR OUTPUTS IN CODES*
A, B, C, ETC	INDIVIDUAL SIGNALS OR GROUPS OF SIGNALS WHEN TWO OR MORE

SIGNAL LINE INDICATORS

◇& OR ◇1	DOT-AND OR DOT-OR (WIRED AND, OR)
▷	POLARITY CONVENTION, NEGATIVE POTENTIAL
▷	DYNAMIC INPUT, TRANSITION FROM "0" STATE TO "1" STATE
—/—	NON-STANDARD LOGIC LEVEL
—×—	ANALOG OR NON-LOGIC LEVEL
—↙—	VARIABLE PARAMETER CONTROL
—○—	INHIBIT DESIGNATOR WITH POLARITY INDICATOR
—○	INHIBIT DESIGNATOR

FUNCTION ABBREVIATIONS

ALU	ARITHMETIC AND LOGIC UNIT
MCNTR	COUNTER, CHARACTER M IS MAX. NO. COUNTS (E.G. 10CNTR OR 16CNTR)
DCDR	DECODER AND/OR ENCODER
DRVR	DRIVER
MEM	MEMORY
MUX	MULTIPLEXER
RCVR	RECEIVER
RGTR	REGISTER
SRN-M	SHIFT REGISTER
DEMUX	DEMULTIPLEXER

	TITLE	CDC TEST NO		DRAWING NUMBER	
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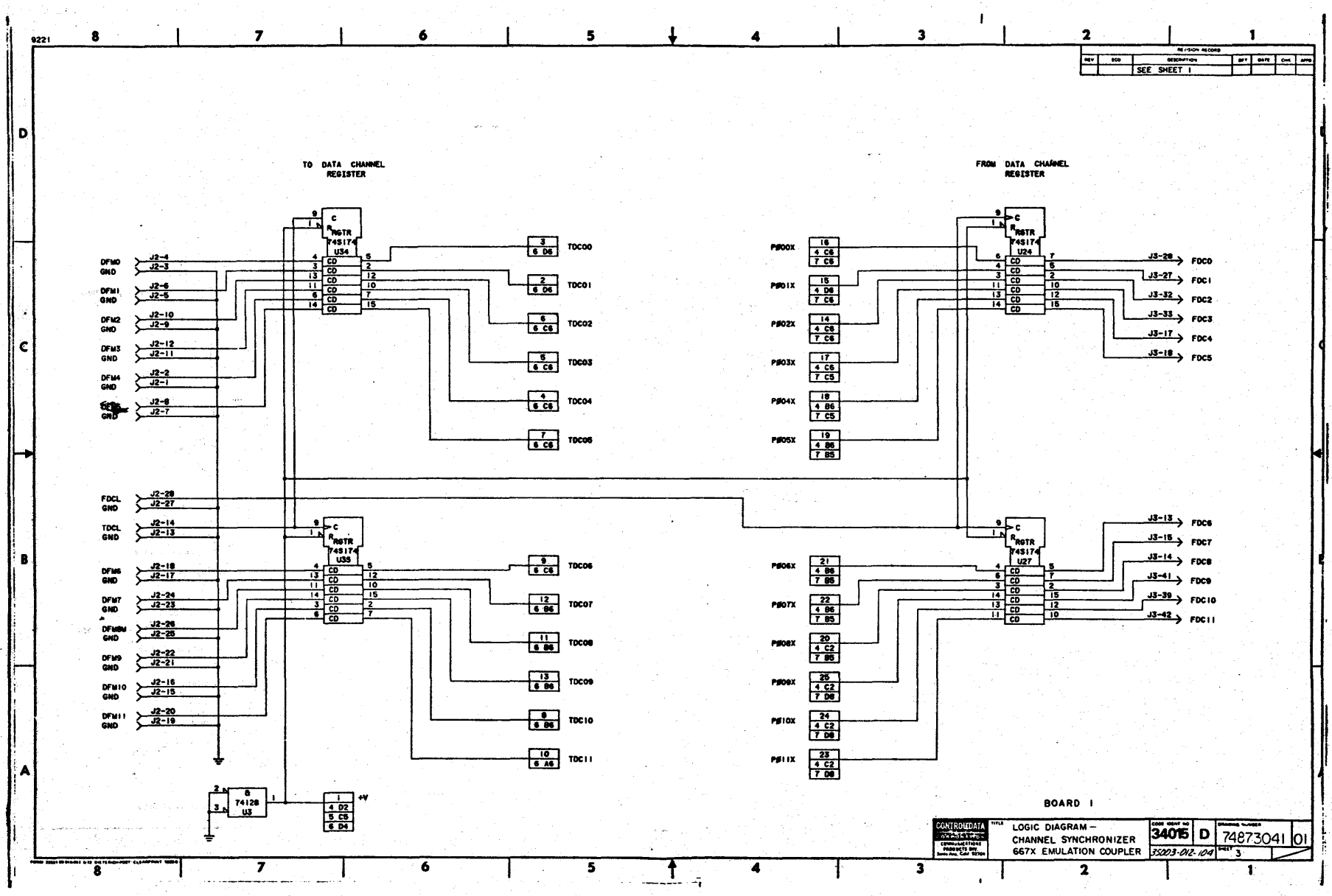
		15203-012-104		SHEET 2	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REVISION RECORD
REV ECO DESCRIPTION BY DATE CHK APPD
SEE SHEET 1
TO DATA CHANNEL REGISTER
FROM DATA CHANNEL REGISTER
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DFM1 J2-6 GND J2-5
DFM2 J2-10 GND J2-9
DFM3 J2-12 GND J2-11
DFM4 J2-2 GND J2-1
SET GND J2-8 J2-7
FDCL J2-28 GND J2-27
TDCL J2-14 GND J2-13
DFM6 J2-18 GND J2-17
DFM7 J2-24 GND J2-23
DFM8M J2-26 GND J2-25
DFM9 J2-22 GND J2-21
DFM10 J2-16 GND J2-15
DFM11 J2-20 GND J2-19
RGTR 74S174 U34
RGTR 74S174 U35
RGTR 74S174 U24
RGTR 74S174 U27
TDC00 TDC01 TDC02 TDC03 TDC04 TDC05
TDC06 TDC07 TDC08 TDC09 TDC10 TDC11
PS00X PS01X PS02X PS03X PS04X PS05X
PS06X PS07X PS08X PS09X PS10X PS11X
FDC0 FDC1 FDC2 FDC3 FDC4 FDC5
FDC6 FDC7 FDC8 FDC9 FDC10 FDC11
J3-28 J3-27 J3-32 J3-33 J3-17 J3-18
J3-13 J3-15 J3-14 J3-41 J3-39 J3-42
74128 U3
+V
BOARD 1
CONTROL DATA
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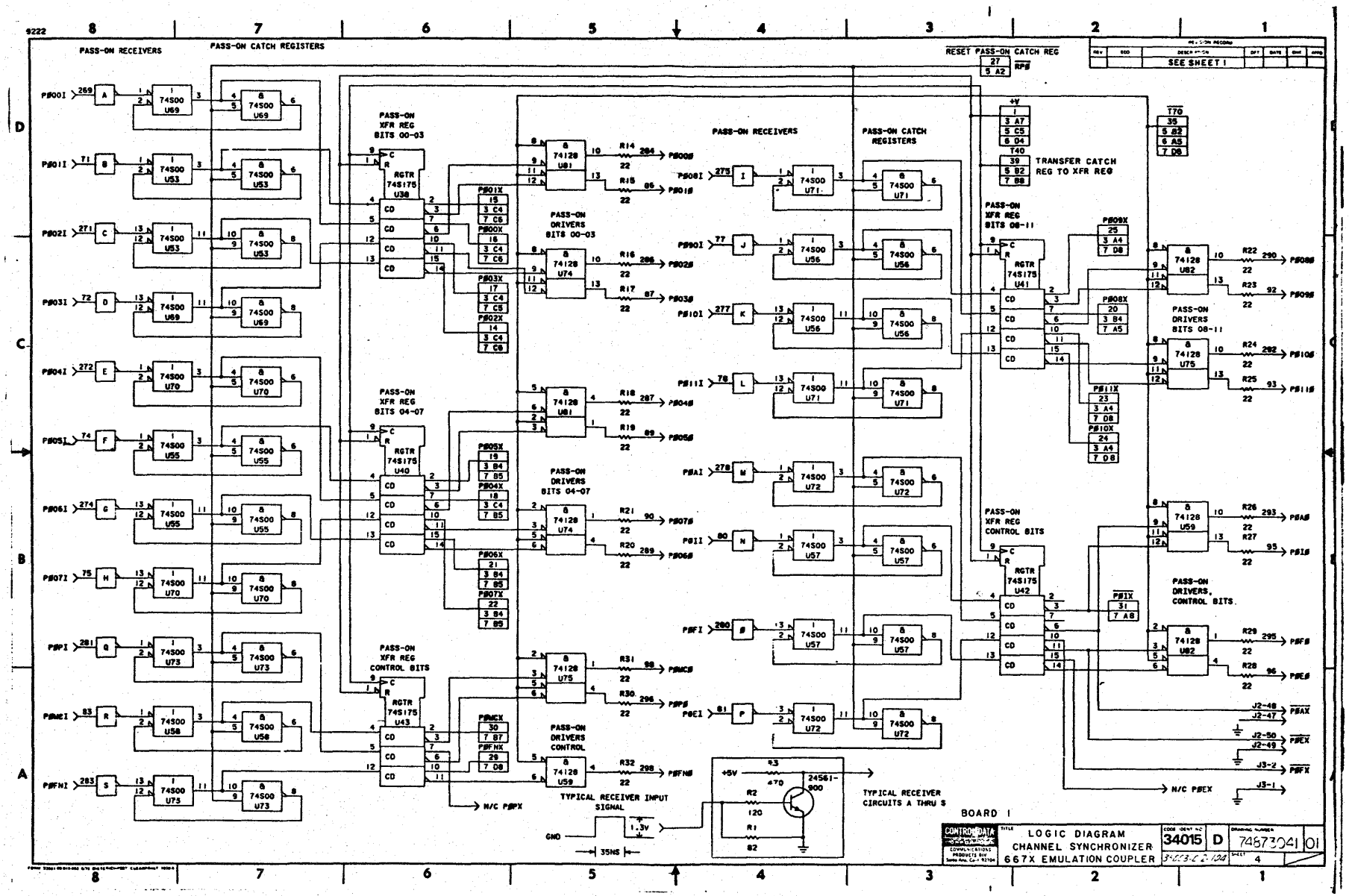
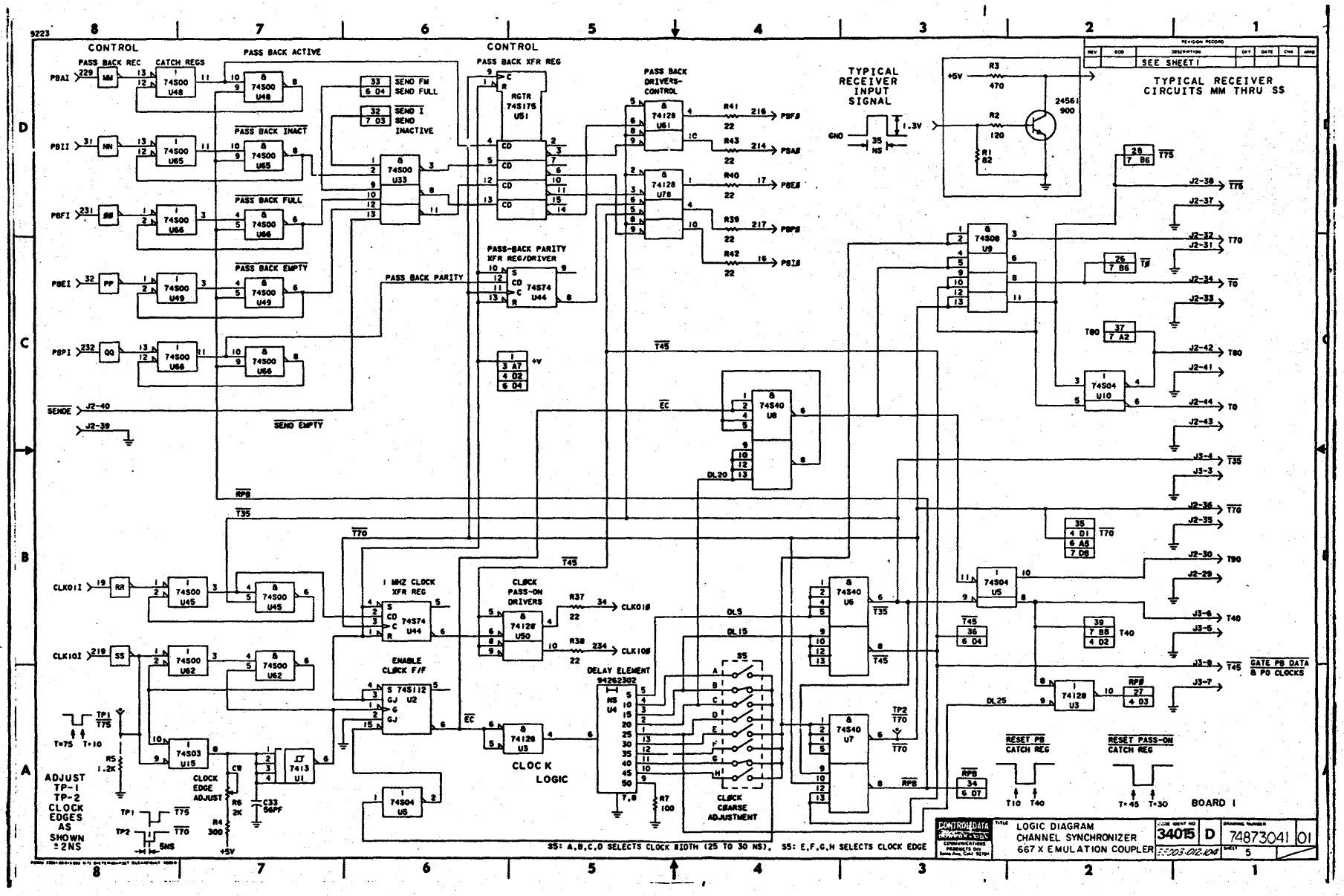
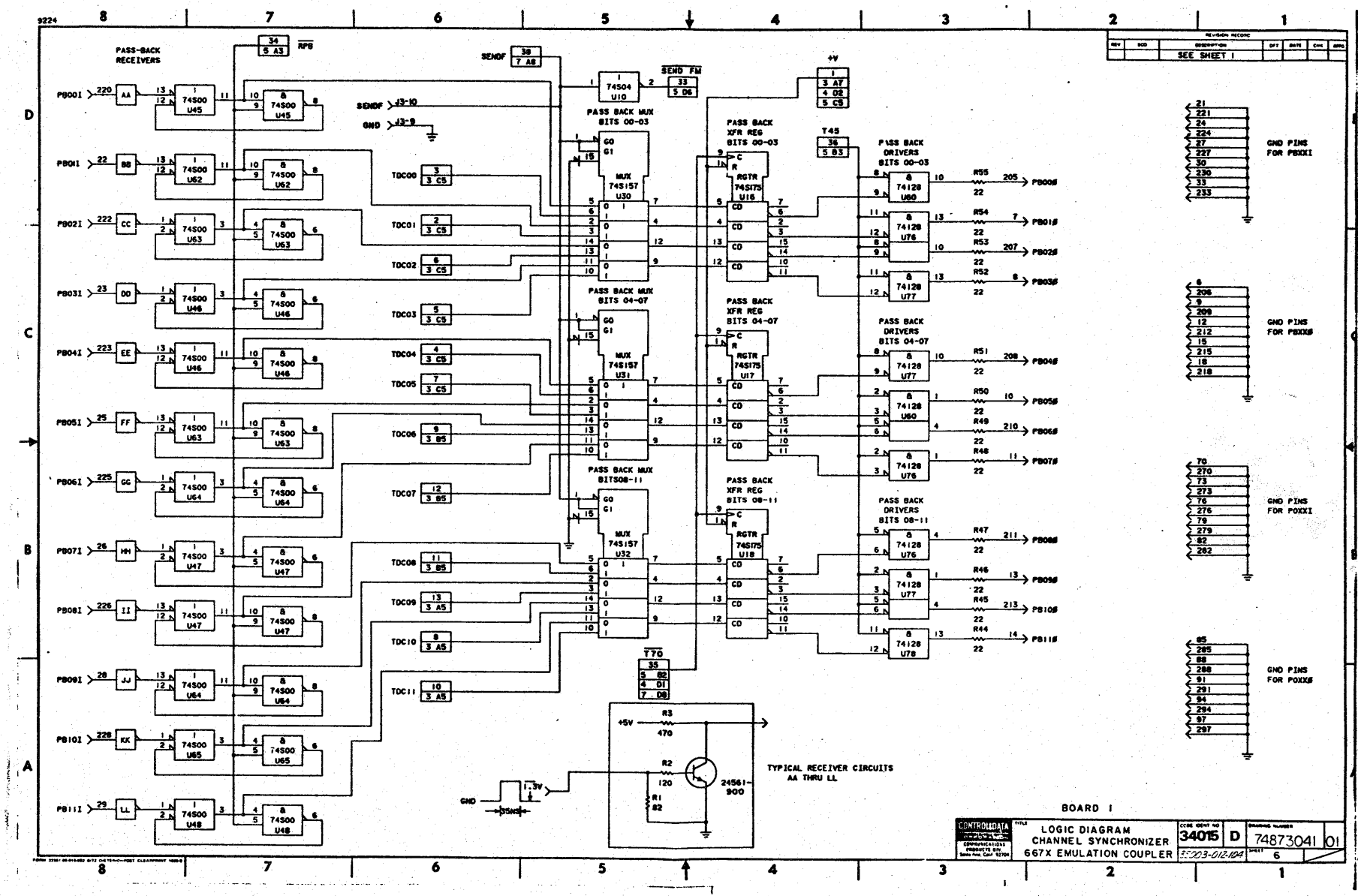
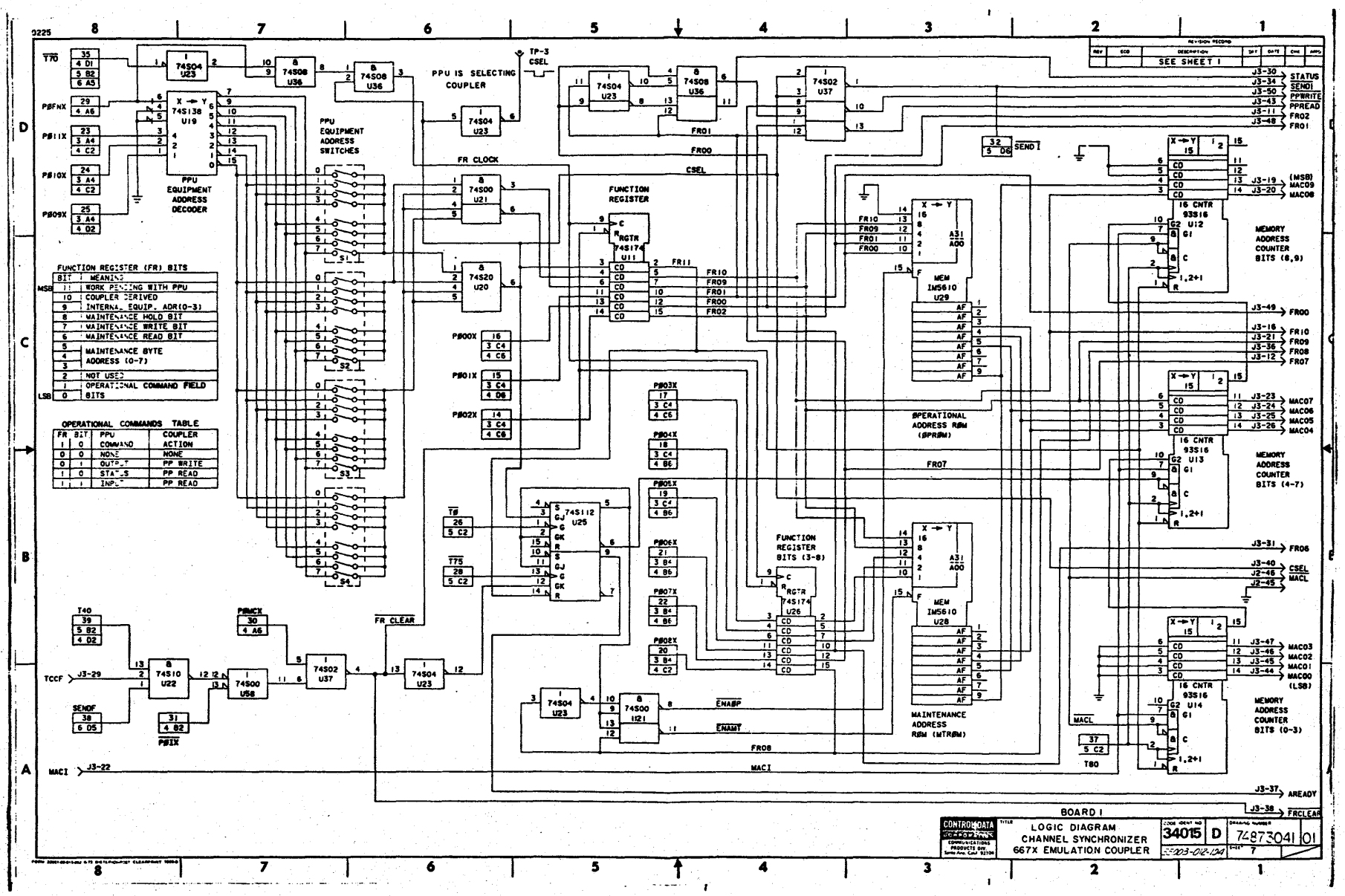
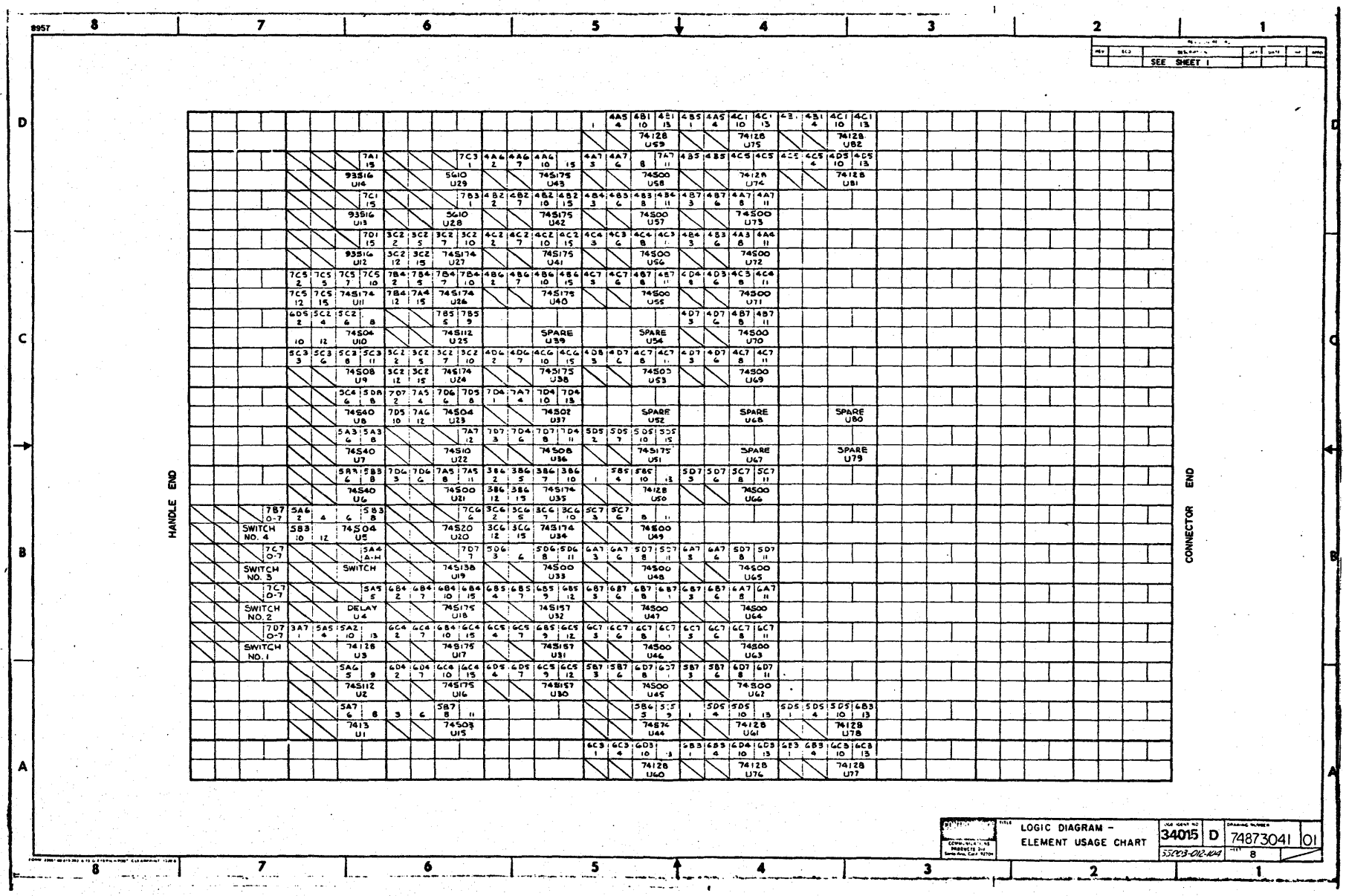
CODE IDENT NO 34015
D
74873041 01
SHEET 3
35203-012-104


PASS-ON RECEIVERS
PASS-ON CATCH REGISTERS
RESET PASS-ON CATCH REG
SEE SHEET 1
PASS-ON XFR REG BITS 00-03
PASS-ON XFR REG BITS 04-07
PASS-ON XFR REG CONTROL BITS
PASS-ON DRIVERS BITS 00-03
PASS-ON DRIVERS BITS 04-07
PASS-ON DRIVERS CONTROL
PASS-ON XFR REG BITS 08-11
PASS-ON DRIVERS BITS 08-11
PASS-ON DRIVERS, CONTROL BITS
TRANSFER CATCH REG TO XFR REG
TYPICAL RECEIVER INPUT SIGNAL
TYPICAL RECEIVER CIRCUITS A THRU S
N/C PBPX
N/C PBEX
BOARD 1
LOGIC DIAGRAM
CHANNEL SYNCHRONIZER
667X EMULATION COUPLER
34015
74873041 01


CONTROL
PASS BACK REC
CATCH REGS
PASS BACK ACTIVE
CONTROL
PASS BACK XFR REG
PASS BACK DRIVERS-CONTROL
TYPICAL RECEIVER INPUT SIGNAL
TYPICAL RECEIVER CIRCUITS MM THRU SS
PASS BACK INACT
PASS BACK FULL
PASS BACK EMPTY
PASS BACK PARITY
PASS-BACK PARITY XFR REG/DRIVER
SEND FM
SEND FULL
SEND I
SEND INACTIVE
SEND EMPTY
1 MHZ CLOCK XFR REG
CLOCK PASS-ON DRIVERS
ENABLE CLOCK F/F
DELAY ELEMENT 94262302
CLOCK COARSE ADJUSTMENT
CLOCK LOGIC
CLOCK EDGE ADJUST
ADJUST TP-1 TP-2 CLOCK EDGES AS SHOWN ±2NS
RESET PB CATCH REG
RESET PASS-ON CATCH REG
GATE PB DATA & PO CLOCKS
SS: A,B,C,D SELECTS CLOCK BIOTH (25 TO 30 NS), SS: E,F,G,H SELECTS CLOCK EDGE
BOARD I
TITLE LOGIC DIAGRAM CHANNEL SYNCHRONIZER 667 X EMULATION COUPLER
34015 D
74873041 01
SHEET 5

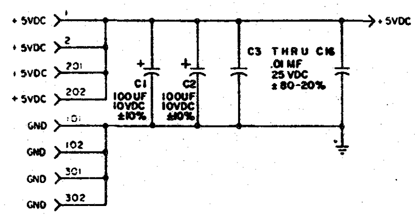

PASS-BACK RECEIVERS
PASS BACK MUX BITS 00-03
PASS BACK MUX BITS 04-07
PASS BACK MUX BITS08-11
PASS BACK XFR REG BITS 00-03
PASS BACK XFR REG BITS 04-07
PASS BACK XFR REG BITS 08-11
PASS BACK DRIVERS BITS 00-03
PASS BACK DRIVERS BITS 04-07
PASS BACK DRIVERS BITS 08-11
SEE SHEET 1
GND PINS FOR PBXXI
GND PINS FOR PBXXB
GND PINS FOR POXXI
GND PINS FOR POXXB
TYPICAL RECEIVER CIRCUITS AA THRU LL
BOARD I
LOGIC DIAGRAM
CHANNEL SYNCHRONIZER
667X EMULATION COUPLER
34015
74873041
01

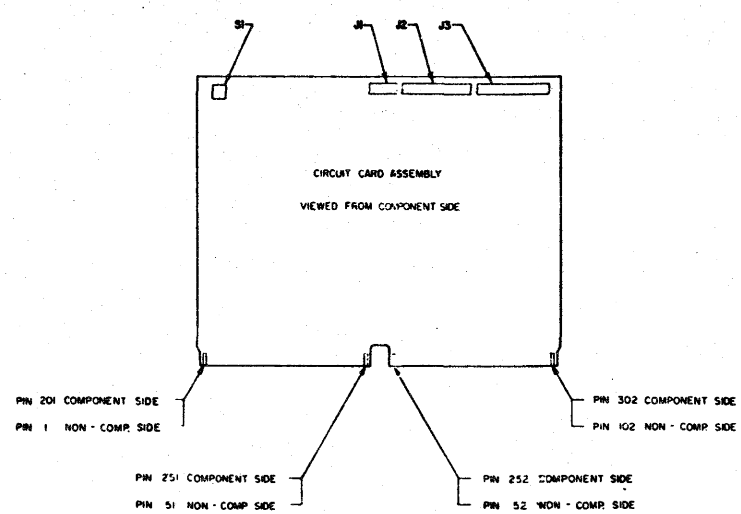

PPU EQUIPMENT ADDRESS DECODER
PPU EQUIPMENT ADDRESS SWITCHES
PPU IS SELECTING COUPLER
FR CLOCK
FUNCTION REGISTER
FUNCTION REGISTER (FR) BITS
OPERATIONAL COMMANDS TABLE
FR CLEAR
FUNCTION REGISTER BITS (3-8)
OPERATIONAL ADDRESS RAM (OPRAM)
MAINTENANCE ADDRESS RAM (MTRAM)
MEMORY ADDRESS COUNTER BITS (8,9)
MEMORY ADDRESS COUNTER BITS (4-7)
MEMORY ADDRESS COUNTER BITS (0-3)
BOARD 1
LOGIC DIAGRAM
CHANNEL SYNCHRONIZER
667X EMULATION COUPLER
34015
D
74873041 01
SEE SHEET 1


8957
8
7
6
5
4
3
2
1
D
C
B
A
HANDLE END
CONNECTOR END
SEE SHEET 1
SWITCH NO. 4
SWITCH NO. 3
SWITCH NO. 2
SWITCH NO. 1
LOGIC DIAGRAM – ELEMENT USAGE CHART
34015
D
74873041
01
55003-012-104
SHEET 8

74879600 C

REV	ECO	DESCRIPTION	DR	DATE
00	08165	INITIAL RELEASE	TP	3-1-76
01	[illegible]	REVISED PER ECO	PL	
02	08512	INITIAL RELEASE	PL	[illegible]





NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTOR VALUES ±5%
   ALL RESISTOR VALUES IN OHMS
   ALL RESISTORS RATED 1/4 WATT
   ALL CAPACITOR VALUES: 200 PF. 500 VDC, ±5 %
   ALL DIODES:
   ALL TRANSISTORS:

2. COMPONENT ASSEMBLY NO. 74872963

3. ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS

	5VDC	GND
14 PIN DUAL - IN - LINE	14	7
16 PIN DUAL - IN - LINE	16	8

NON - STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS

5AAY

BOARD 2

UNLESS OTHERWISE SPECIFIED DIM ARE IN INCHES/MILLIMETERS TOLERANCES

DO NOT SCALE DRAWING

COMMUNICATIONS PRODUCTS DIV

DN-54-A

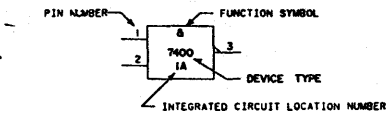
T. PARNAKIAN 3-1-76

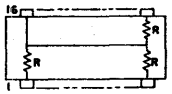
LOGIC DIAGRAM—
2550 INTERFACE 667X
EMULATION COUPLER

D 34015 74872964

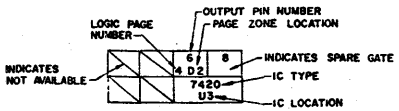
SCALE NONE 349ET -012-104 SHEET 1 OF 13

CIRCUIT ELEMENT SYMBOLOGY



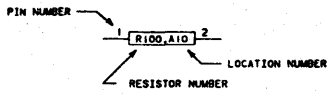


IC. RESISTOR PACK
LOCATION C6-2K
B7-1K

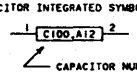


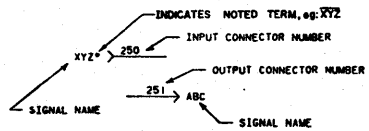
ELEMENT USAGE
CHART LEGEND

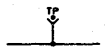
RESISTOR INTEGRATED SYMBOLOGY

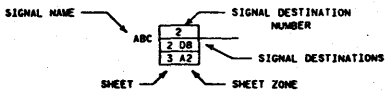


CAPACITOR INTEGRATED SYMBOLOGY

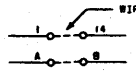








COMMON CONTROL BLOCK.
SIGNALS ENTERING THIS BLOCK
ARE COMMON TO MORE THAN ONE
SECTION OF THE CIRCUIT



IDENTIFIER LIST

CDC ELEMENT IDENTIFIER	VENDOR TYPE NUMBER	FUNCTION
	74S00	TTL QUAD 2-INPUT NAND
	74S02	TTL QUAD 2-INPUT NOR
	8234	TTL QUAD 2-INPUT MULTIPLEXER OPEN COLLECTOR
	74S04	TTL HEX INVERTER
	74S08	TTL QUAD 2-INPUT AND
	74S10	TTL TRIPLE 3-INPUT NAND
	74S20	TTL DUAL 4-INPUT NAND
	74S40	TTL DUAL 4-INPUT NAND BUFFER
	74393	TTL DUAL 4-BIT BINARY COUNTER
	74S112	TTL DUAL J-K NET F/F
	8097	DRIVER, TTL HEX TRISTATE
	74S157	MUX, TTL QUAD 2-INPUT
	74S174	LATCH, TTL 6-BIT D-TYPE
	7451	TTL TRIPLE 3-INPUT AND
	7432	TTL QUAD 2-INPUT OR
	74S35	TTL QUAD 2 INPUT EXCLUSIVE OR/NOR
	74S30	TTL 8-INPUT NAND
	74S260	TTL DUAL 5-INPUT NOR
	93421	RAM - 256 X 1 BIT ACTIVE LOW OUTPUT
	7427	TTL TRIPLE 3-INPUT NOR
	8098	HEX TRI-STATE INVERTING GATE
	74170	REG/MEMORY, TTL 16 BIT 4X4 RAM
	93415	MEMORY, TTL 1024-BIT 1024 X1 RAM (BS)
	74S158	MUX, TTL QUAD 2-INPUT
	74S38	TTL QUAD 2-INPUT NAND BUFFER (OC)
	74S139	DECODER, TTL DUAL (1 OF 4)

QUALIFYING FUNCTION SYMBOLS

SYMBOL	DESCRIPTION
8	AND ALL INPUTS ACTIVE
1	ONE OR MORE (OR) ANY INPUT ACTIVE
≥2	TWO OR MORE INPUTS ACTIVE
=1	ONLY ONE INPUT ACTIVE (EXCLUSIVE OR)
=	ALL INPUTS EQUAL
=2	ONLY TWO INPUTS ACTIVE, NO MORE, NO LESS
G	GENERATOR OR OSCILLATOR (WAVEFORM MAY BE ADDED)
⊓	SCHMITT TRIGGER
⊓	ONE-SHOT MULTIVIBRATOR
⊢⊣	TIME DELAY
00	EVEN PARITY
000	ODD PARITY
X → Y	X INPUTS, DECODED OR ENCODED TO, Y OUTPUTS
X/Y	X INPUT LEVEL CONVERTED TO Y OUTPUT LEVEL
Σ	ARITHMETIC SUMMING CIRCUIT
F	COMPLEX FUNCTION

INPUT / OUTPUT DESIGNATORS

R	RESET
S	SET
G	GATING TYPE INPUT THAT OFFSETS OTHER INPUTS OR OUTPUTS
J	J INPUT OF J-K FLIP FLOP
K	K INPUT OF J-K FLIP FLOP
T	TOGGLE OR COMPLEMENT INPUT
D	DATA INPUT OF TYPE FLIP FLOP
C	GATING (CLOCK) INPUT FOR A "D" INPUT ONLY
L	USED ONLY WITH INHIBIT INPUT; ALL LOW STATE OUTPUTS ARE INHIBITED
H	USED ONLY WITH INHIBIT INPUT; ALL HIGH STATE OUTPUTS ARE INHIBITED
⊓	DELAY INDICATOR, FOR OUTPUT HAVING INPUT CONTROLLED DELAY
E	EXTENDER FOR EXPANDING THE NUMBER OF INPUTS
⊐	INDICATES GROUPED INPUTS THAT MAINTAIN FIXED RELATIONSHIP
⊏	INDICATES GROUPED OUTPUTS
→	SHIFT RIGHT (OR DOWN)
←	SHIFT LEFT (OR UP)
+1	INCREASE CONTENTS BY ONE (COUNT UP)
-1	DECREASE CONTENTS BY ONE (COUNT DOWN)
1, 2, 4, 8	INDICATES RELATIVE WEIGHTING OF INPUTS OR OUTPUTS IN CODES
A, B, C, ETC	INDIVIDUAL SIGNALS OR GROUPS OF SIGNALS WHEN TWO OR MORE

SIGNAL LINE INDICATORS

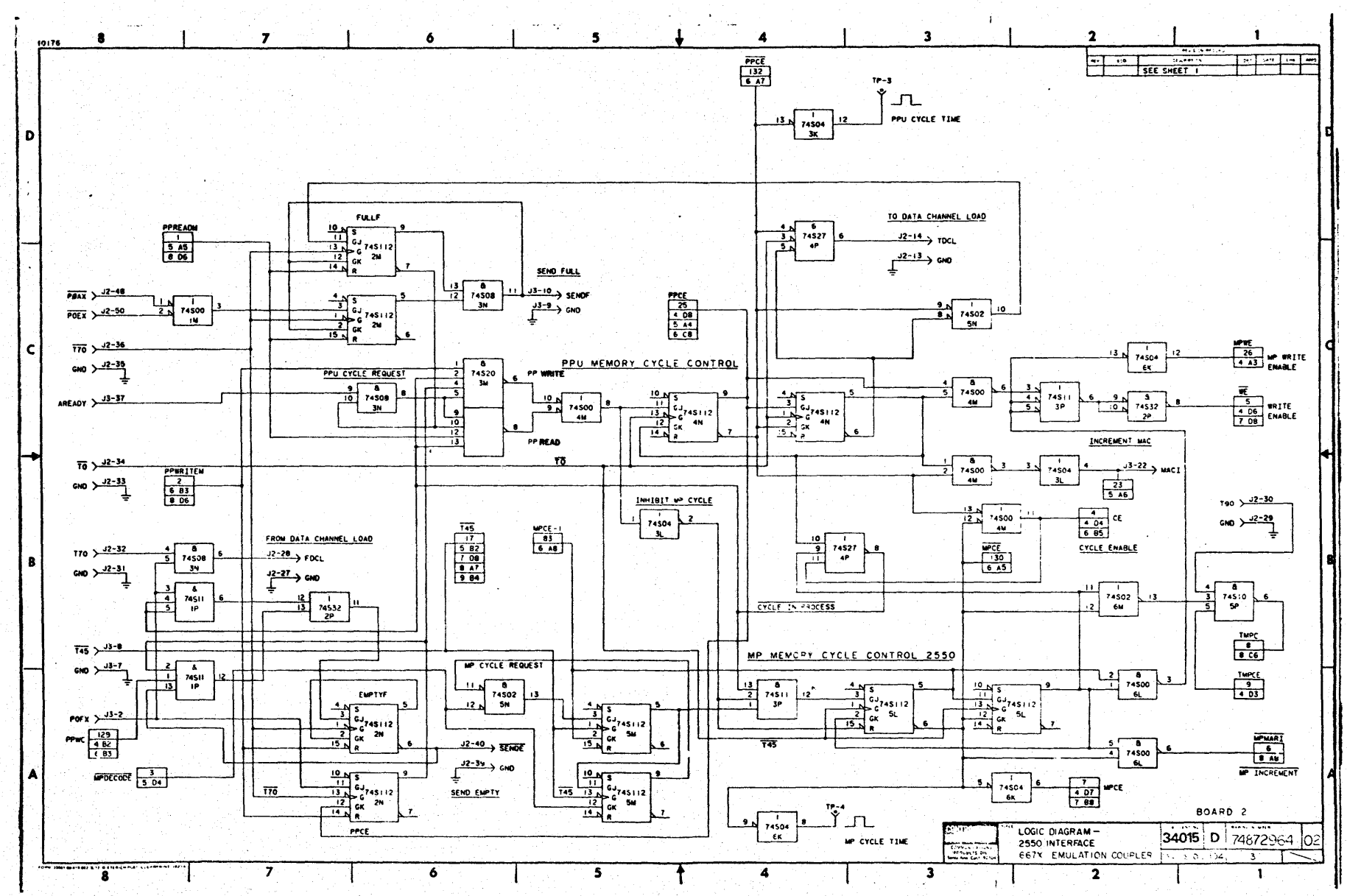
◇8 OR ◇1	DOT-AND OR DOT-OR (WIRED AND, OR)
◺	POLARITY CONVENTION, NEGATIVE POTENTIAL
▷	DYNAMIC INPUT, TRANSITION FROM "0" STATE TO "1" STATE
—/—	NON-STANDARD LOGIC LEVEL
—+—	ANALOG OR NON-LOGIC LEVEL
—↗—	VARIABLE PERAMETER CONTROL
—○—	INHIBIT DESIGNATOR WITH POLARITY INDICATOR
—○—	INHIBIT DESIGNATOR

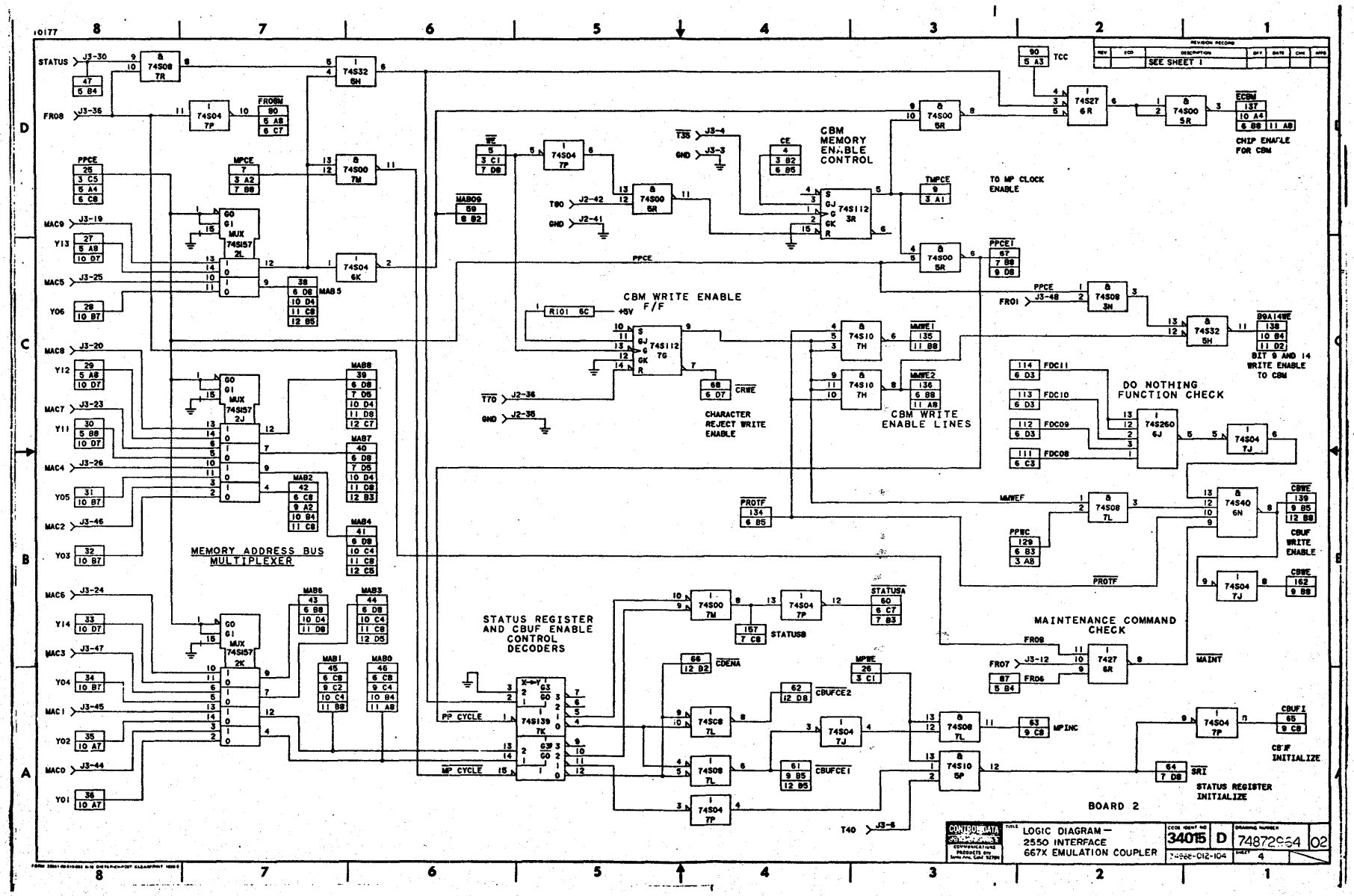
FUNCTION ABBREVIATIONS

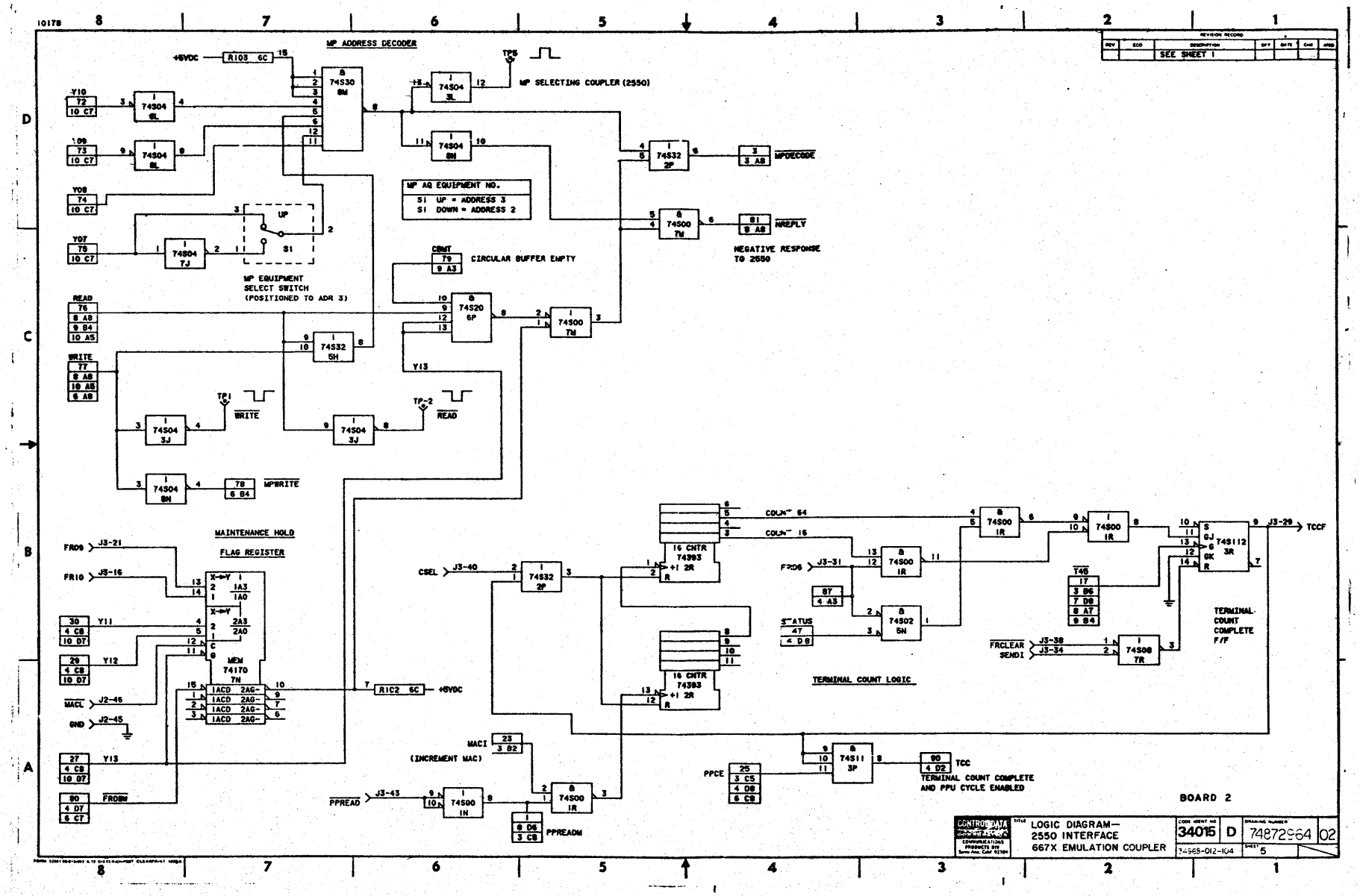
ALU	ARITHMETIC AND LOGIC UNIT
MCNTR	COUNTER, CHARACTER M IS MAX, NO. COUNTS (E.G. 10CNTR OR 16CNTR)
DCDR	DECODER AND/OR ENCODER
DRVR	DRIVER
MEM	MEMORY
MUX	MULTIPLEXER
RCVR	RECEIVER
RGTR	REGISTER
SRM-M	SHIFT REGISTER
DEMUX	DEMULTIPLEXER

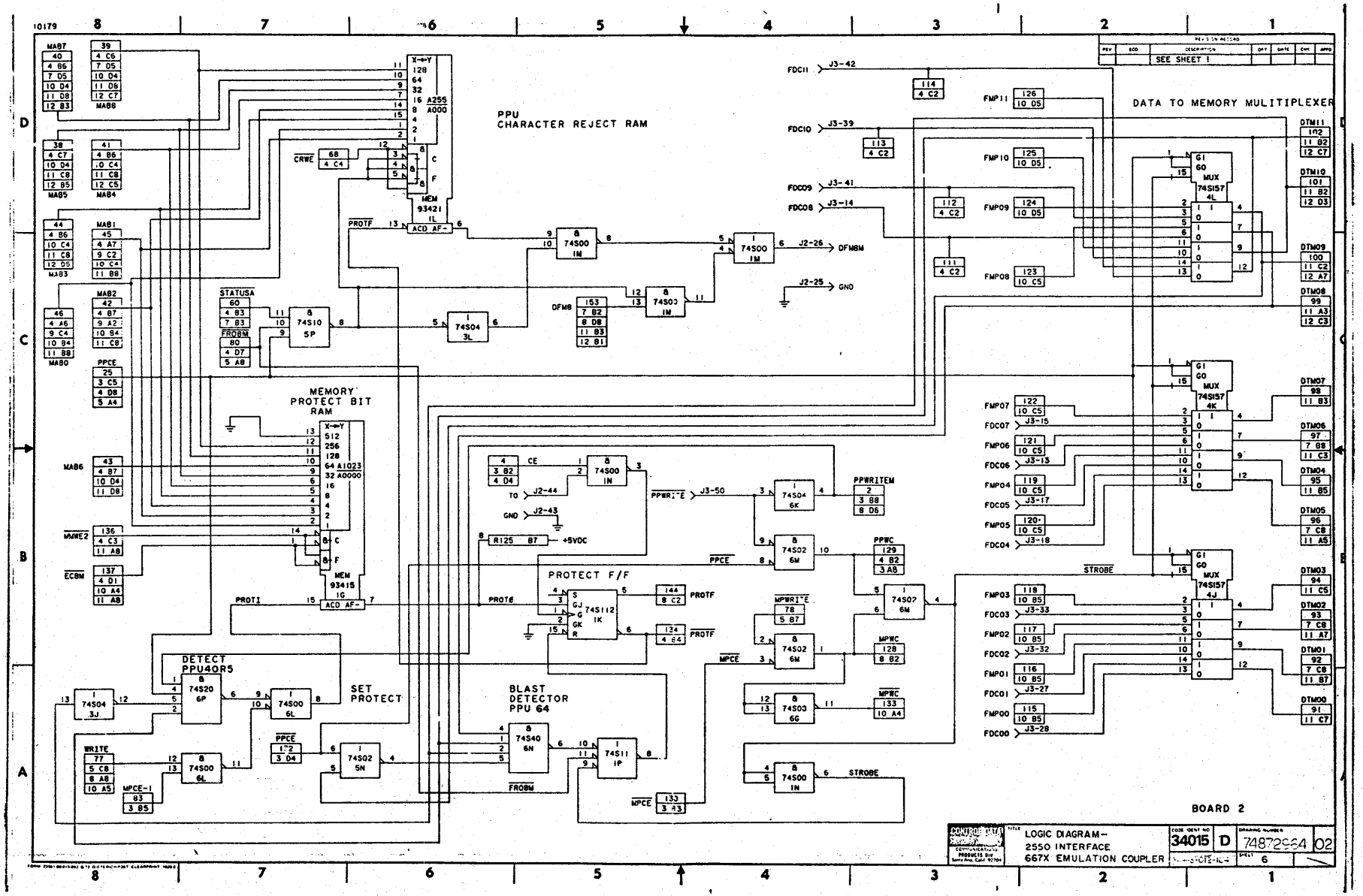
REV	ECO	DESCRIPTION	BY	DATE	CHK	APPD
		SEE SHEET 1				

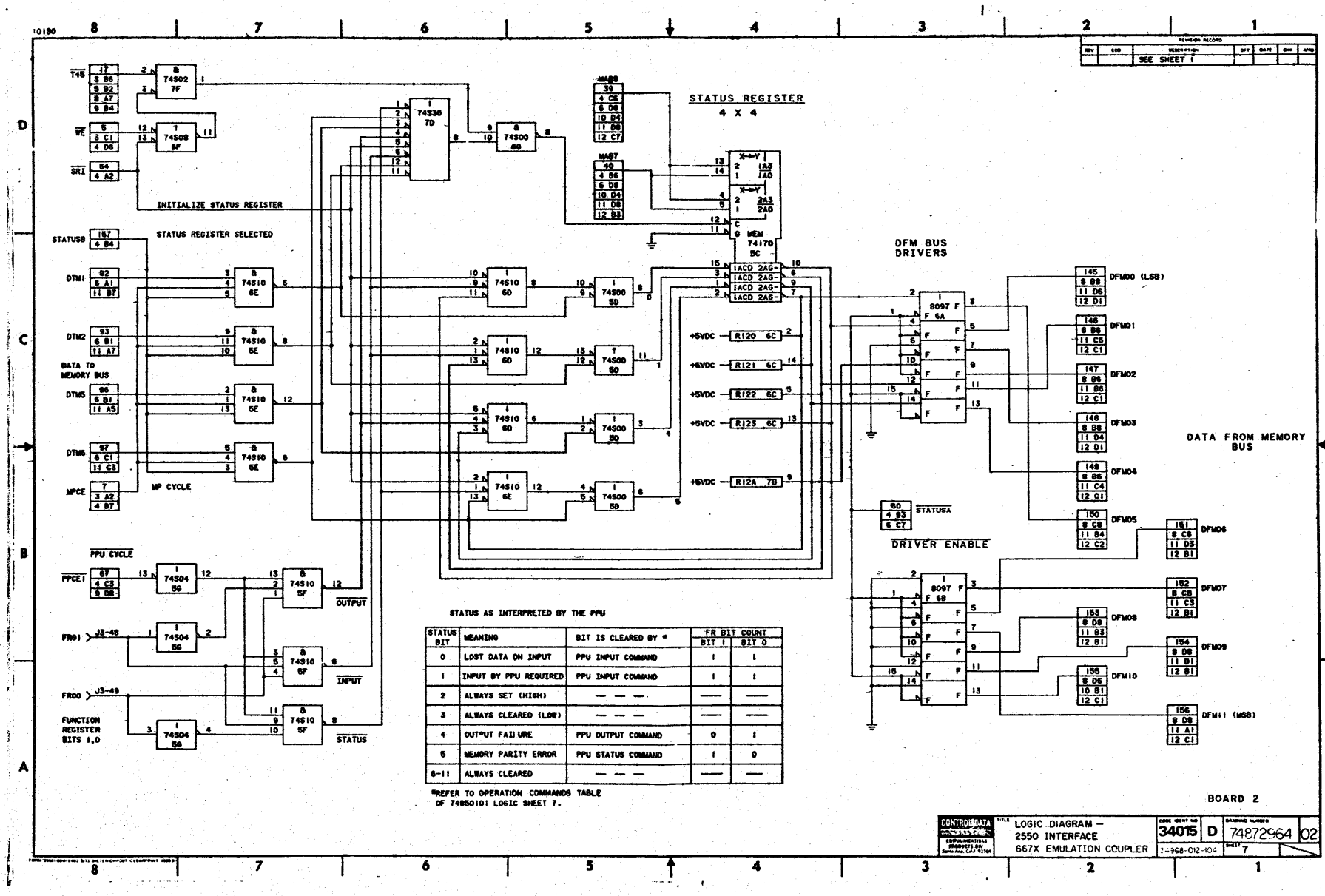
TITLE	CODE IDENT NO	SIZE	DRAWING NUMBER	REV
LOGIC DIAGRAM— KEY TO SYMBOLS	34015	D	74872964	02
	34568-012-104	SHEET 2		


SEE SHEET 1
PPCE
TP-3
PPU CYCLE TIME
TO DATA CHANNEL LOAD
PPREADM
FULLF
SEND FULL
PPU MEMORY CYCLE CONTROL
PPU CYCLE REQUEST
PP WRITE
PP READ
INCREMENT MAC
INHIBIT MP CYCLE
FROM DATA CHANNEL LOAD
CYCLE ENABLE
CYCLE IN PROCESS
MP MEMORY CYCLE CONTROL 2550
MP CYCLE REQUEST
EMPTYF
SEND EMPTY
MP WRITE ENABLE
WRITE ENABLE
MP INCREMENT
TP-4
MP CYCLE TIME
BOARD 2
LOGIC DIAGRAM – 2550 INTERFACE 667X EMULATION COUPLER
34015 D 74872964 02


MEMORY ADDRESS BUS MULTIPLEXER
STATUS REGISTER AND CBUF ENABLE CONTROL DECODERS
CBM MEMORY ENABLE CONTROL
CBM WRITE ENABLE F/F
CBM WRITE ENABLE LINES
CHARACTER REJECT WRITE ENABLE
DO NOTHING FUNCTION CHECK
MAINTENANCE COMMAND CHECK
TO MP CLOCK ENABLE
CHIP ENABLE FOR CBM
BIT 9 AND 14 WRITE ENABLE TO CBM
CBUF WRITE ENABLE
CBUF INITIALIZE
STATUS REGISTER INITIALIZE
BOARD 2
LOGIC DIAGRAM — 2550 INTERFACE 667X EMULATION COUPLER
34015
D
74879600
02


MP ADDRESS DECODER
+5VDC
R105 6C
MP SELECTING COUPLER (2550)
MP AQ EQUIPMENT NO.
S1 UP = ADDRESS 3
S1 DOWN = ADDRESS 2
MP EQUIPMENT SELECT SWITCH (POSITIONED TO ADR 3)
CIRCULAR BUFFER EMPTY
MPDECODE
NREPLY
NEGATIVE RESPONSE TO 2550
READ
WRITE
MPWRITE
MAINTENANCE HOLD FLAG REGISTER
MEM 74170 7N
R1C2 6C
+5VDC
MACL
GND
FROSW
MACI
(INCREMENT MAC)
PPREAD
PPREADM
CSEL
16 CNTR 74393
COUNT 64
COUNT 16
FROS
STATUS
TERMINAL COUNT LOGIC
FRCLEAR
SENDI
TERMINAL COUNT COMPLETE F/F
TCCF
PPCE
TCC
TERMINAL COUNT COMPLETE AND PPU CYCLE ENABLED
BOARD 2
LOGIC DIAGRAM— 2550 INTERFACE 667X EMULATION COUPLER
34015
D
74872564
02
SHEET 5


PPU
CHARACTER REJECT RAM
DATA TO MEMORY MULITIPLEXER
MEMORY
PROTECT BIT
RAM
PROTECT F/F
DETECT
PPU4OR5
SET
PROTECT
BLAST
DETECTOR
PPU 64
BOARD 2
LOGIC DIAGRAM-
2550 INTERFACE
667X EMULATION COUPLER
CONTROL DATA
34015
D
74872884
02
SEE SHEET 1



STATUS AS INTERPRETED BY THE PPU

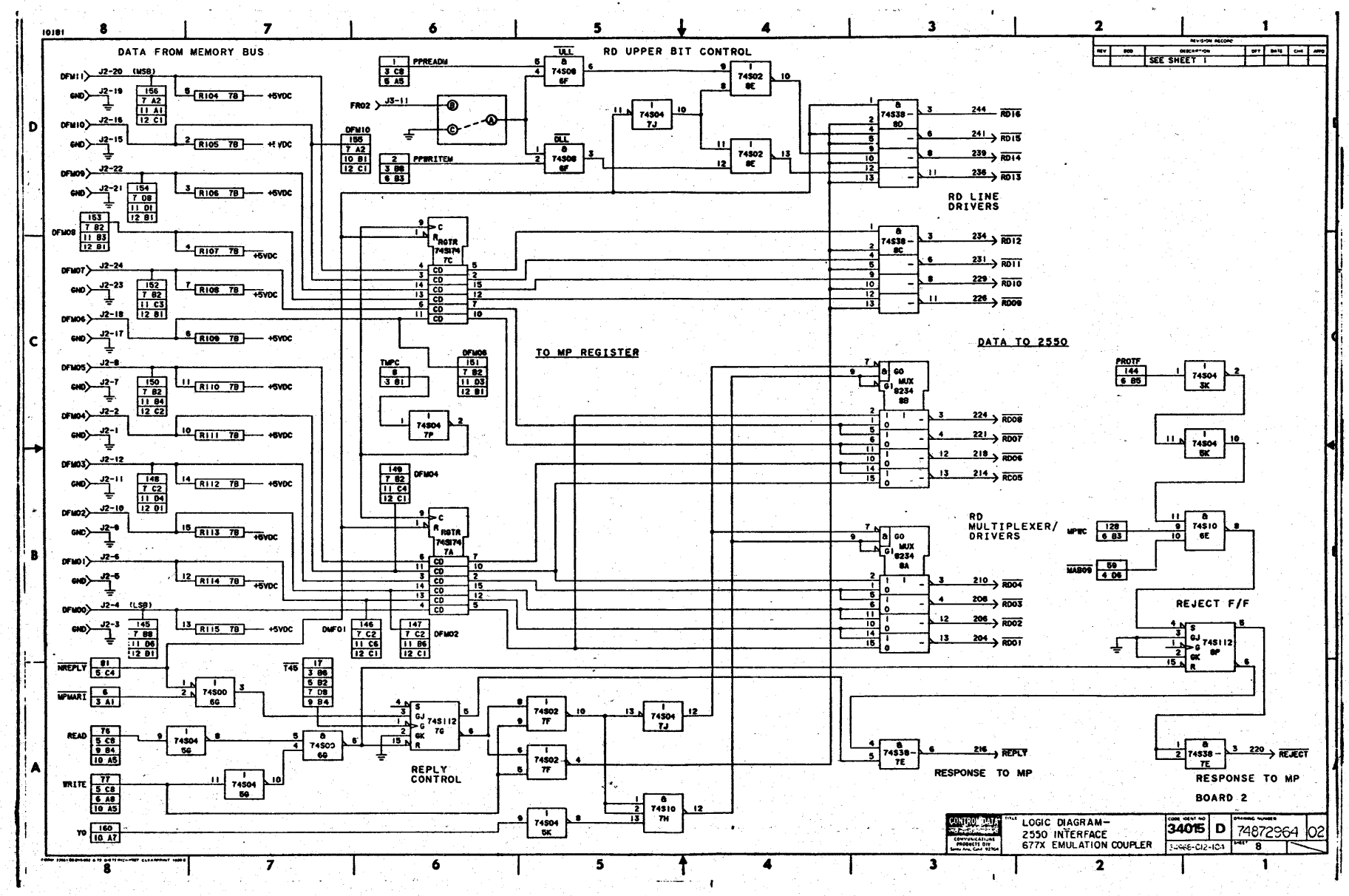
STATUS BIT	MEANING	BIT IS CLEARED BY *	FR BIT COUNT BIT 1	FR BIT COUNT BIT 0
0	LOST DATA ON INPUT	PPU INPUT COMMAND	1	1
1	INPUT BY PPU REQUIRED	PPU INPUT COMMAND	1	1
2	ALWAYS SET (HIGH)	— — —	——	——
3	ALWAYS CLEARED (LOW)	— — —	——	——
4	OUTPUT FAILURE	PPU OUTPUT COMMAND	0	1
5	MEMORY PARITY ERROR	PPU STATUS COMMAND	1	0
6-11	ALWAYS CLEARED	— — —	——	——

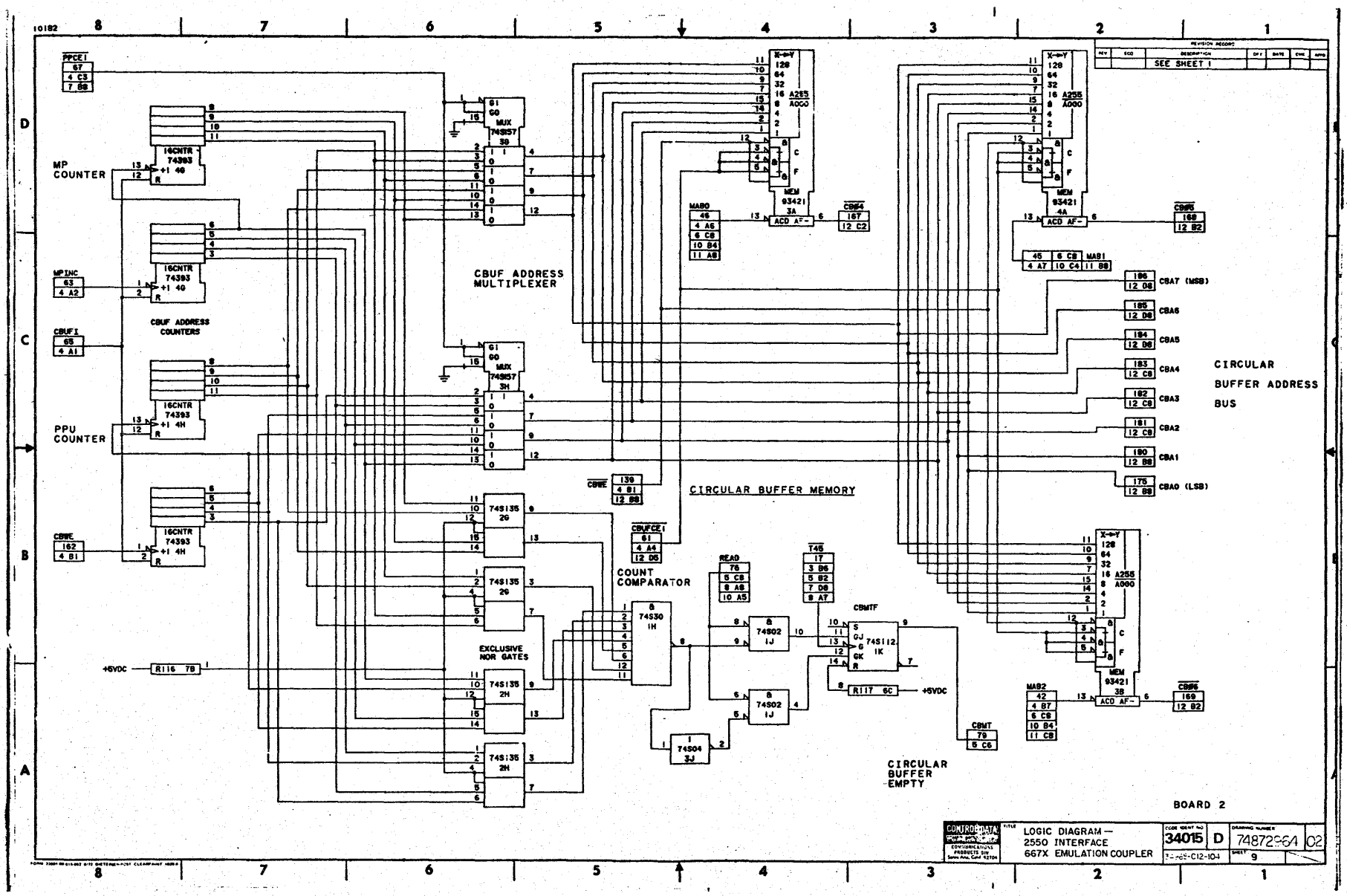
*REFER TO OPERATION COMMANDS TABLE OF 74850101 LOGIC SHEET 7.

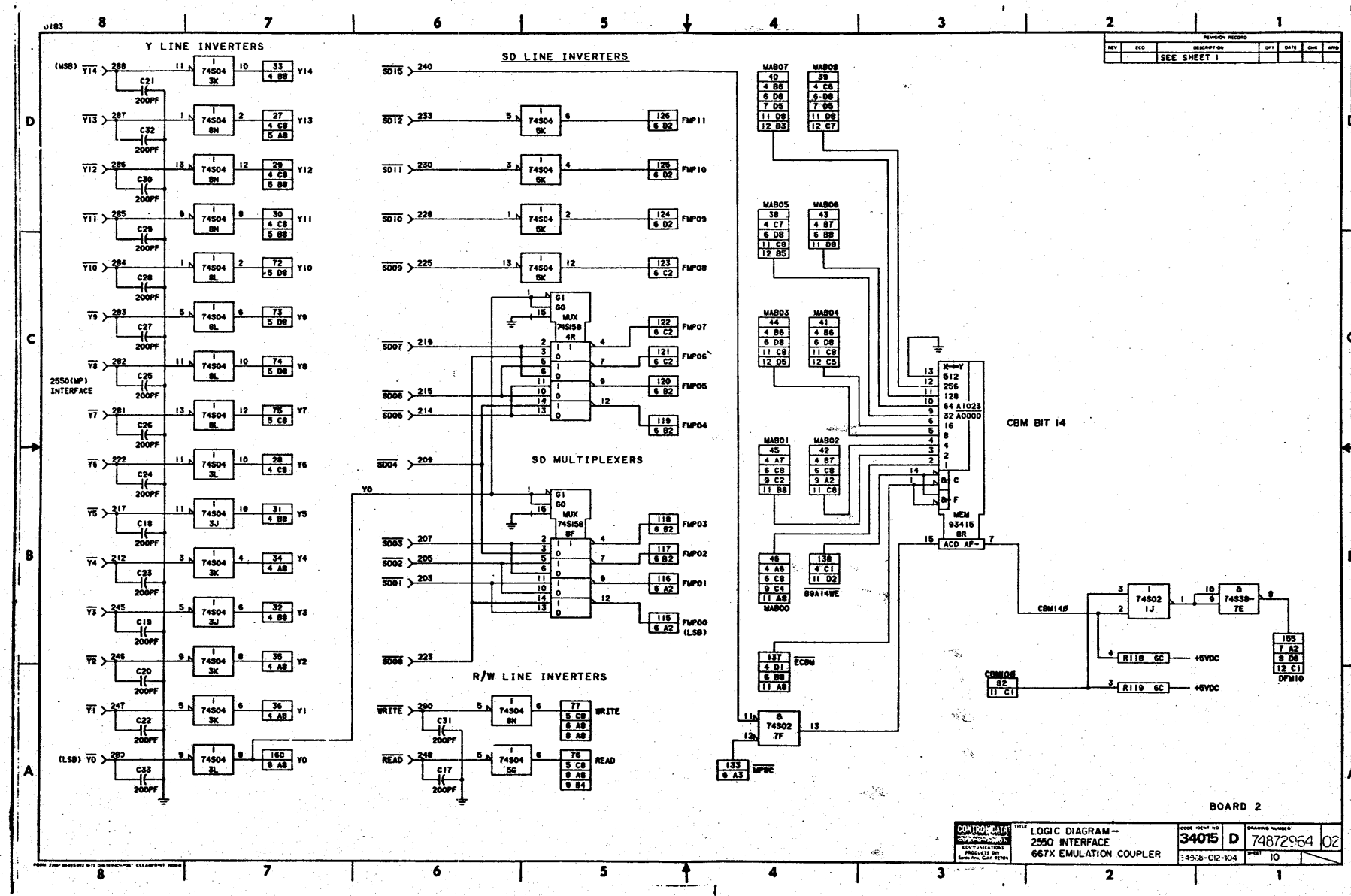
CONTROL DATA — COMMUNICATIONS PRODUCTS DIV

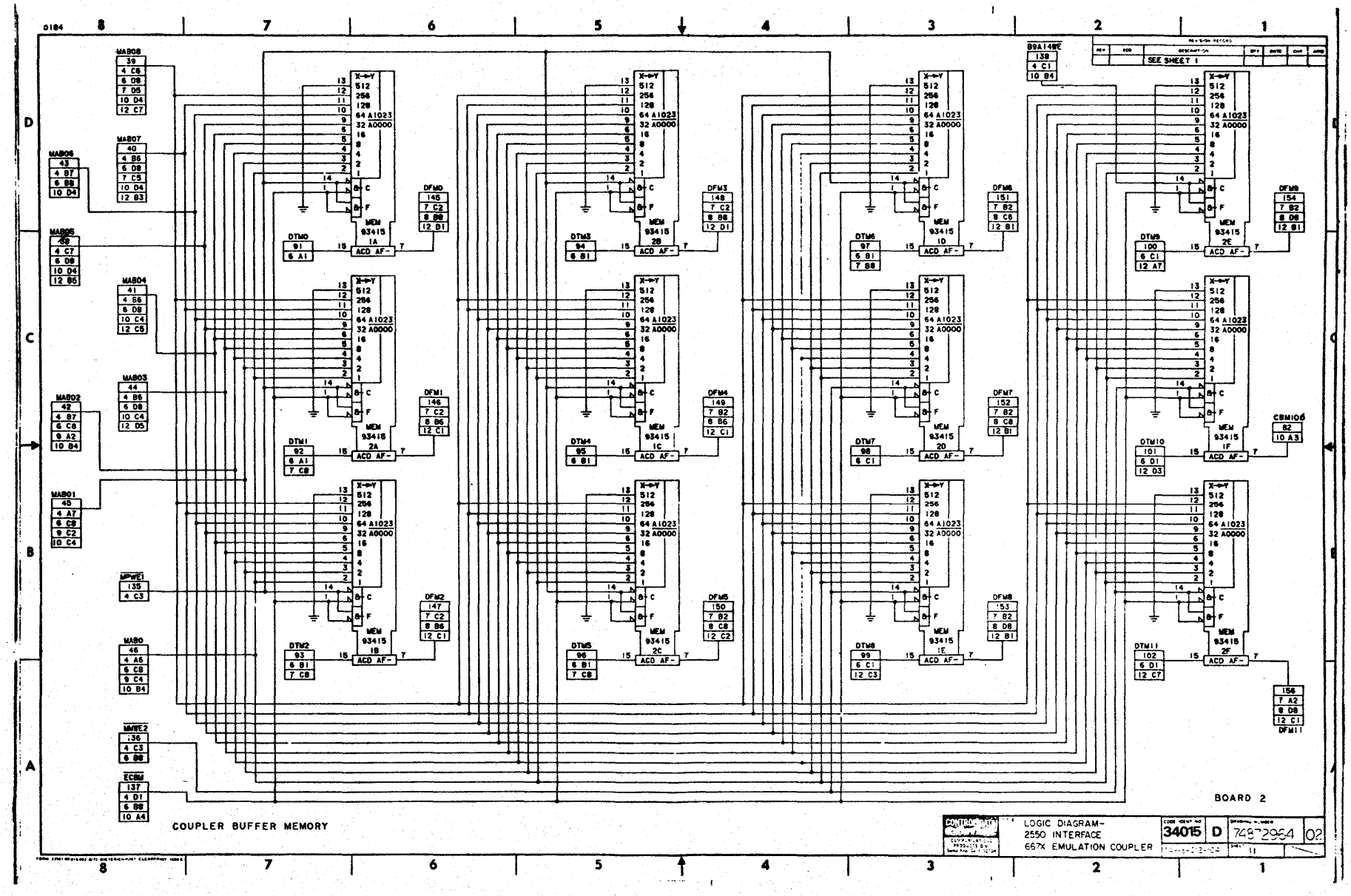
LOGIC DIAGRAM — 2550 INTERFACE 667X EMULATION COUPLER

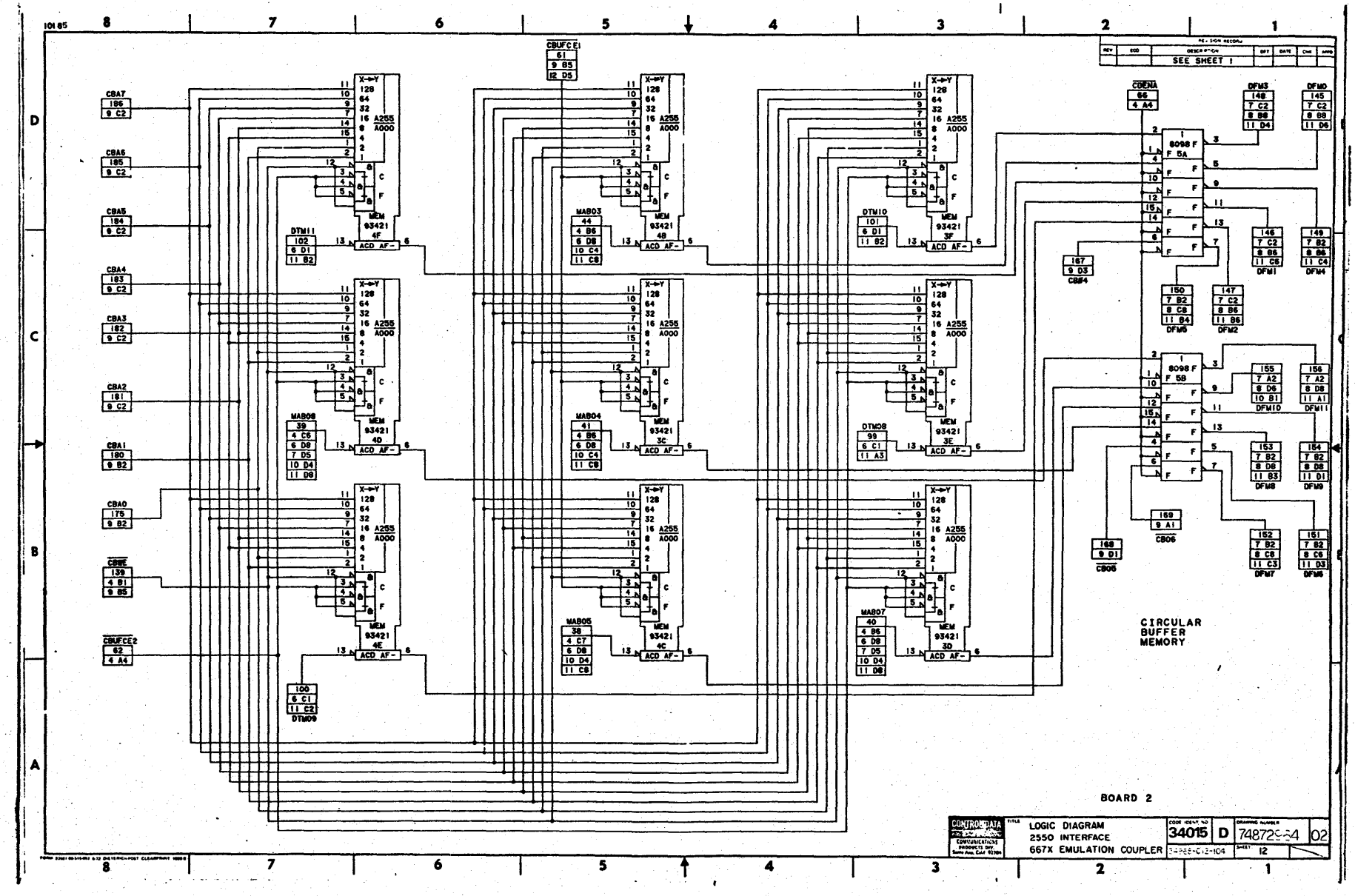
CODE IDENT NO 34015 | D | 74872964 | 02 | SHEET 7

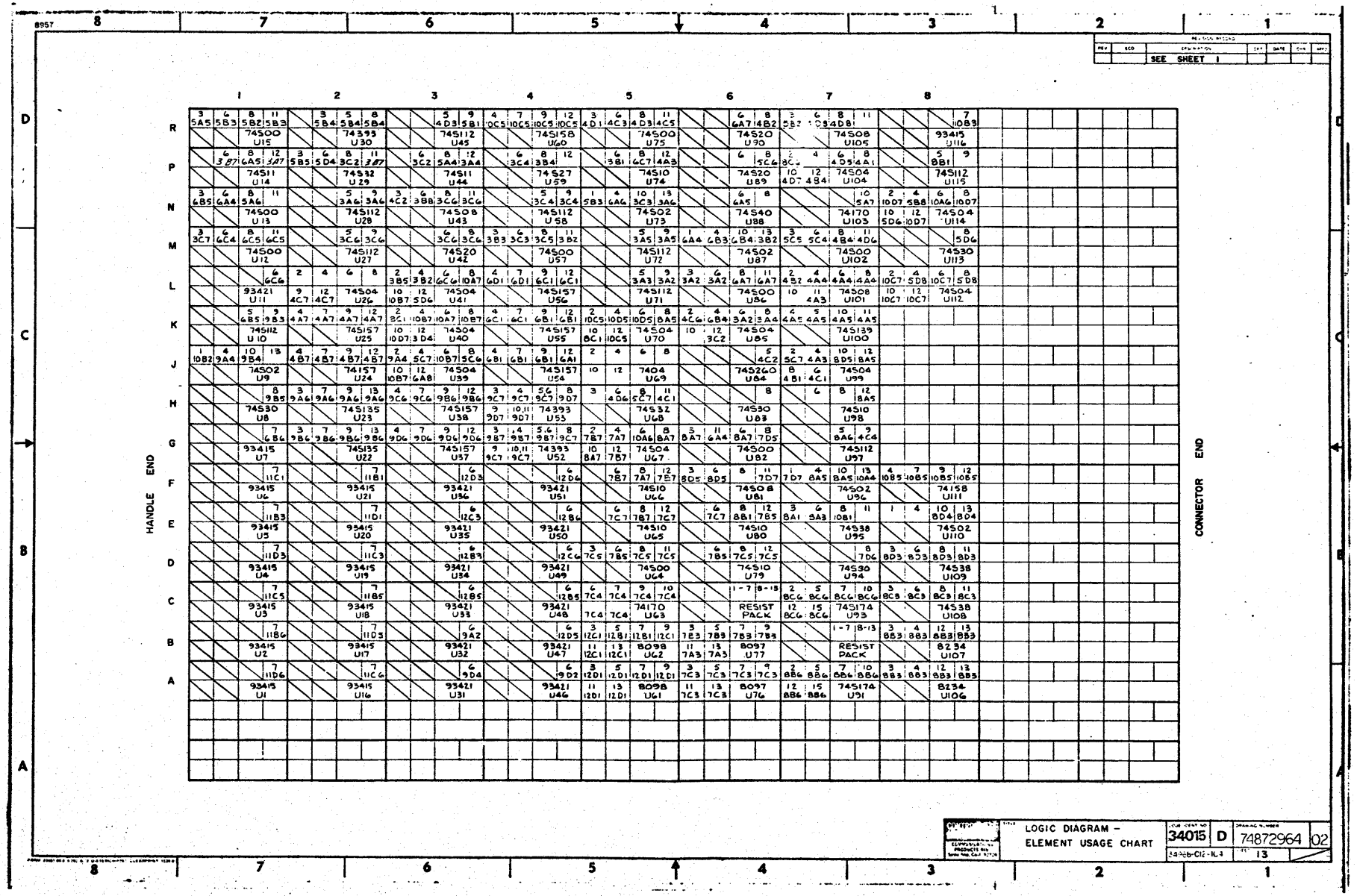

DATA FROM MEMORY BUS
RD UPPER BIT CONTROL
RD LINE DRIVERS
DATA TO 2550
TO MP REGISTER
RD MULTIPLEXER/ DRIVERS
REJECT F/F
REPLY CONTROL
RESPONSE TO MP
RESPONSE TO MP
BOARD 2
SEE SHEET 1
LOGIC DIAGRAM- 2550 INTERFACE 677X EMULATION COUPLER
34015
74872364
02

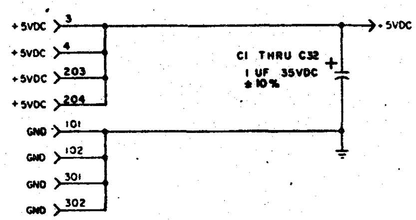

MP COUNTER
MPINC
CBUF ADDRESS COUNTERS
CBUFI
PPU COUNTER
CBWE
+5VDC
CBUF ADDRESS MULTIPLEXER
CIRCULAR BUFFER MEMORY
COUNT COMPARATOR
EXCLUSIVE NOR GATES
CIRCULAR BUFFER EMPTY
CIRCULAR BUFFER ADDRESS BUS
CBA7 (MSB)
CBA6
CBA5
CBA4
CBA3
CBA2
CBA1
CBA0 (LSB)
BOARD 2
SEE SHEET 1
LOGIC DIAGRAM — 2550 INTERFACE 667X EMULATION COUPLER
34015
D
9

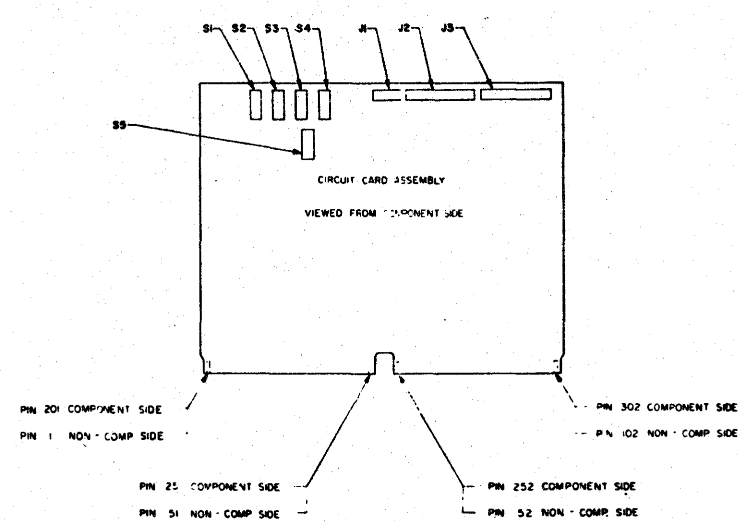

Y LINE INVERTERS
SD LINE INVERTERS
SD MULTIPLEXERS
R/W LINE INVERTERS
2550(MP) INTERFACE
CBM BIT 14
BOARD 2
LOGIC DIAGRAM—
2550 INTERFACE
667X EMULATION COUPLER
34015
D
74872964
02
SEE SHEET 1


SEE SHEET 1
COUPLER BUFFER MEMORY
BOARD 2
LOGIC DIAGRAM-
2550 INTERFACE
667X EMULATION COUPLER
34015
D
74872964
02


CBUFCE1
CBA7
CBA6
CBA5
CBA4
CBA3
CBA2
CBA1
CBA0
CBWE
CBUFCE2
DTM11
DTM10
DTM09
DTM08
MAB03
MAB04
MAB05
MAB06
MAB07
CDENA
DFM3
DFM0
DFM1
DFM4
DFM5
DFM2
DFM10
DFM11
DFM8
DFM9
DFM7
DFM6
CBF4
CBD6
CBD5
SEE SHEET 1
X←Y
128
64
32
16
8
4
2
1
A255
A000
MEM
93421
ACD AF-
8098 F
F 5A
F 5B
CIRCULAR
BUFFER
MEMORY
BOARD 2
LOGIC DIAGRAM
2550 INTERFACE
667X EMULATION COUPLER
34015
D
74872934
02
12


8957
SEE SHEET 1
HANDLE END
CONNECTOR END
LOGIC DIAGRAM – ELEMENT USAGE CHART
34015
D
74872964
02
13





NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTOR VALUES ±5%
   ALL RESISTOR VALUES IN OHMS
   ALL RESISTORS RATED 1/4 WATT

2. COMPONENT ASSEMBLY NO. 74873038

3. ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS

	5VDC	GND
14 PIN DUAL - IN - LINE	14	7
16 PIN DUAL - IN - LINE	16	8

NON - STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS

REV	ECO	DESCRIPTION	DFT	DATE
01	05893	INITIAL RELEASE	TP	8-27-75
02	05165	SEE ECO	TP	3-5-76
03	06628	INITIAL RELEASE	PL	4-16-76

5AAY

BOARD 1

LOGIC DIAGRAM—
CHANNEL SYNCHRONIZER
667X EMULATION COUPLER

DO NOT SCALE DRAWING

COMMUNICATIONS PRODUCTS DIV

DY159-A

T PARNAKIAN 3-1-76

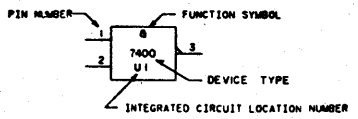
D 34015 74873039

SCALE NONE 3500Z-012-104 SHEET 1 OF 7

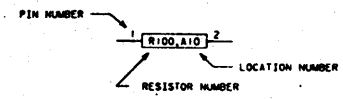
6650

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
		SEE SHEET 1				

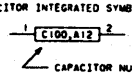
CIRCUIT ELEMENT SYMBOLOGY

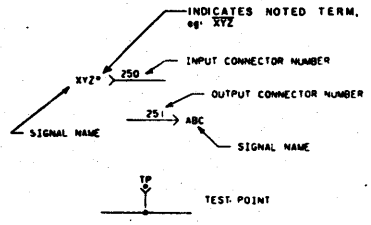


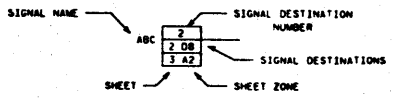
RESISTOR INTEGRATED SYMBOLOGY



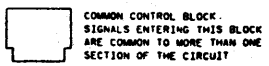
CAPACITOR INTEGRATED SYMBOLOGY

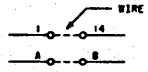






N/C DENOTES NO CONNECTION





IDENTIFIER LIST

CDC ELEMENT IDENTIFIER	VENDOR TYPE NUMBER	FUNCTION
	74500	TTL QUAD 2-INPUT NAND
	74502	TTL QUAD 2-INPUT NOR
	74503	TTL QUAD 2 INPUT NAND (OPEN COLL)
	74504	TTL HEX INVERTER
	74508	TTL QUAD 2 INPUT AND
	74510	TTL TRIPLE 3-INPUT NAND
	74520	TTL DUAL 4-INPUT NAND
	74540	TTL DUAL 4 INPUT NAND BUFFER
	74574	TTL DUAL T-TYPE F/F
	745112	TTL DUAL J-K NET F/F
	745138	DECODER, TTL (1 OF 8)
	745157	MUX, TTL QUAD 2 INPUT
	745174	LATCH, TTL 6 BIT D-TYPE
	745175	LATCH, TTL 4 BIT D-TYPE
	93516	COUNTER, TTL 4 BIT BINARY
	7413	SCHMITT TRIGGER TTL DUAL NAND
	74128	LINE DRIVER QUAD 2-INPUT NOR
	5610	MEMORY, TTL ROM

QUALIFYING FUNCTION SYMBOLS

SYMBOL	DESCRIPTION
8	AND ALL INPUTS ACTIVE
1	ONE OR MORE (OR) ANY INPUT ACTIVE
≥2	TWO OR MORE INPUTS ACTIVE
=1	ONLY ONE INPUT ACTIVE (EXCLUSIVE OR)
=	ALL INPUTS EQUAL
=2	ONLY TWO INPUTS ACTIVE, NO MORE, NO LESS
G	GENERATOR OR OSCILLATOR (WAVEFORM MAY BE ADDED)
⊓	SCHMITT TRIGGER
⊓⊔	ONE-SHOT MULTIVIBRATOR
⊢⊣	TIME DELAY
00'	EVEN PARITY
000	ODD PARITY
X→Y	X INPUTS, DECODED OR ENCODED TO, Y OUTPUTS
X/Y	X INPUT LEVEL CONVERTED TO Y OUTPUT LEVEL
Σ	ARITHMETIC SUMMING CIRCUIT
F	COMPLEX FUNCTION

INPUT / OUTPUT DESIGNATORS

R	RESET
S	SET
G	GATING TYPE INPUT THAT OFFSETS OTHER INPUTS OR OUTPUTS
J	J INPUT OF J-K FLIP FLOP
K	K INPUT OF J-K FLIP FLOP
T	TOGGLE OR COMPLEMENT INPUT
D	DATA INPUT OF TYPE FLIP FLOP
C	GATING (CLOCK) INPUT FOR A 'D' INPUT ONLY
L	USED ONLY WITH INHIBIT INPUT; ALL LOW STATE OUTPUTS ARE INHIBITED
H	USED ONLY WITH INHIBIT INPUT; ALL HIGH STATE OUTPUTS ARE INHIBITED
⊓	DELAY INDICATOR, FOR OUTPUT HAVING INPUT CONTROLLED DELAY
E	EXTENDER FOR EXPANDING THE NUMBER OF INPUTS
⊐	INDICATES GROUPED INPUTS THAT MAINTAIN FIXED RELATIONSHIP
⊐	INDICATES GROUPED OUTPUTS
→	SHIFT RIGHT (OR DOWN)
←	SHIFT LEFT (OR UP)
+1	INCREASE CONTENTS BY ONE (COUNT UP)
-1	DECREASE CONTENTS BY ONE (COUNT DOWN)
1, 2, 4, 8	INDICATES RELATIVE WEIGHTING OF INPUTS OR OUTPUTS IN CODES
A, B, C, ETC	INDIVIDUAL SIGNALS OR GROUPS OF SIGNALS WHEN TWO OR MORE

SIGNAL LINE INDICATORS

◇8 OR ◇1	DOT-AND OR DOT-OR (WIRED AND, OR)
◿	POLARITY CONVENTION, NEGATIVE POTENTIAL
◺	DYNAMIC INPUT, TRANSITION FROM '0' STATE TO '1' STATE
—+—	NON-STANDARD LOGIC LEVEL
—#—	ANALOG OR NON-LOGIC LEVEL
—↗—	VARIABLE PARAMETER CONTROL
—○—	INHIBIT DESIGNATOR WITH POLARITY INDICATOR
—○—	INHIBIT DESIGNATOR

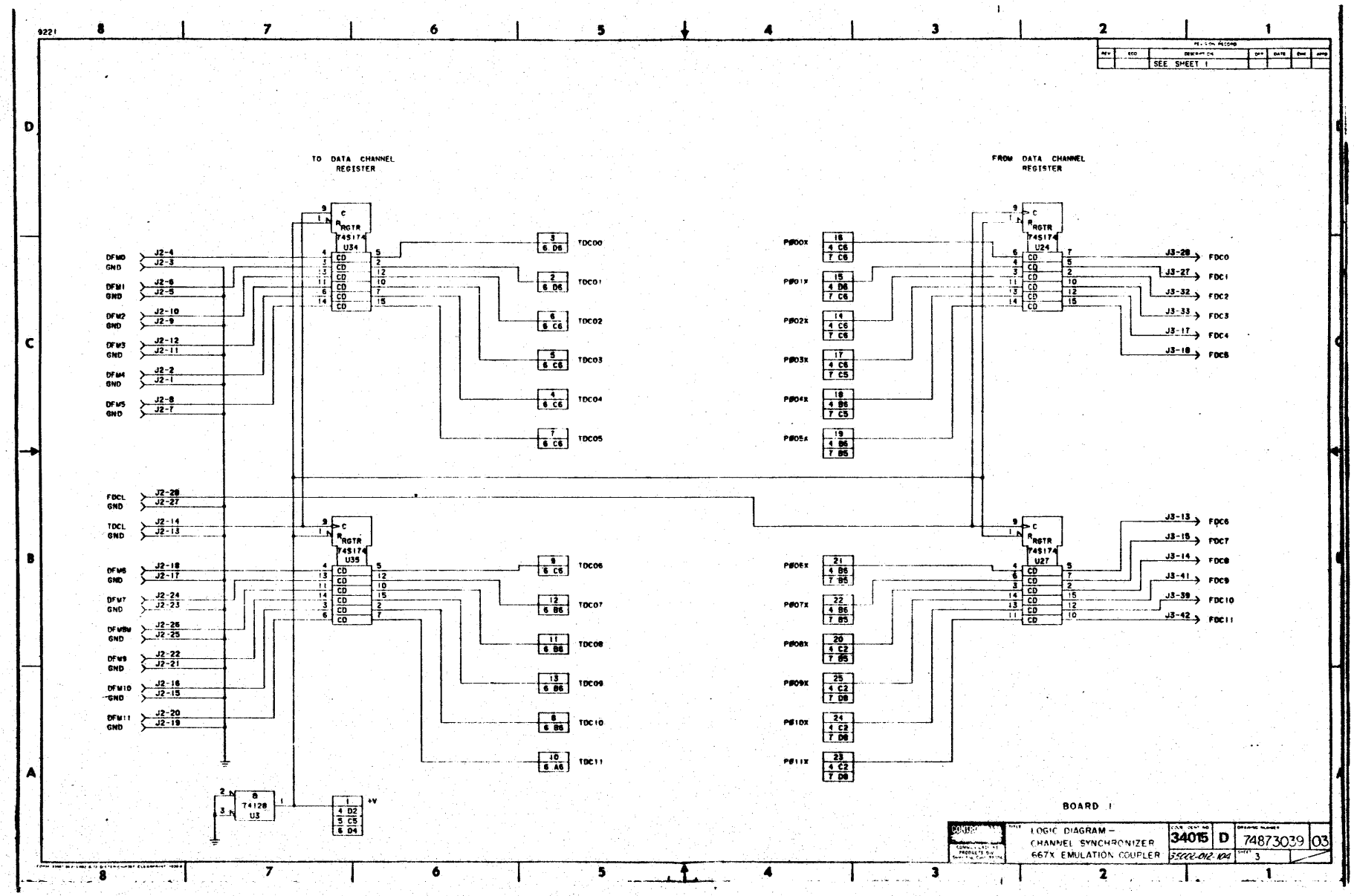
FUNCTION ABBREVIATIONS

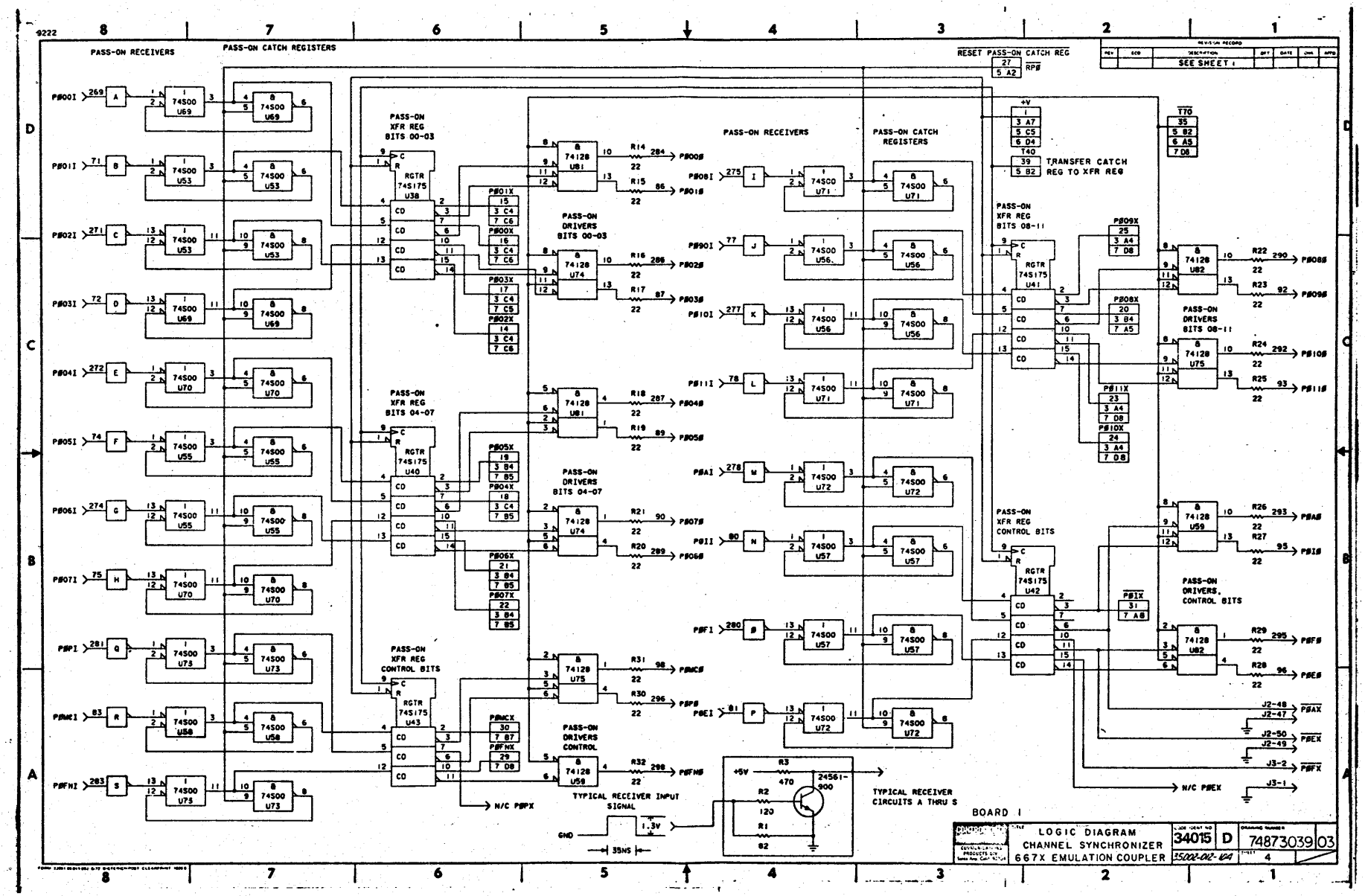
ALU	ARITHMETIC AND LOGIC UNIT
MCNTR	COUNTER, CHARACTER M IS MAX, NO. COUNTS (E.G. 10CNTR OR 16CNTR)
DCDR	DECODER AND/OR ENCODER
DRVR	DRIVER
MEM	MEMORY
MUX	MULTIPLEXER
RCVR	RECEIVER
RGTR	REGISTER
SHN-M	SHIFT REGISTER
DEMUX	DEMULTIPLEXER

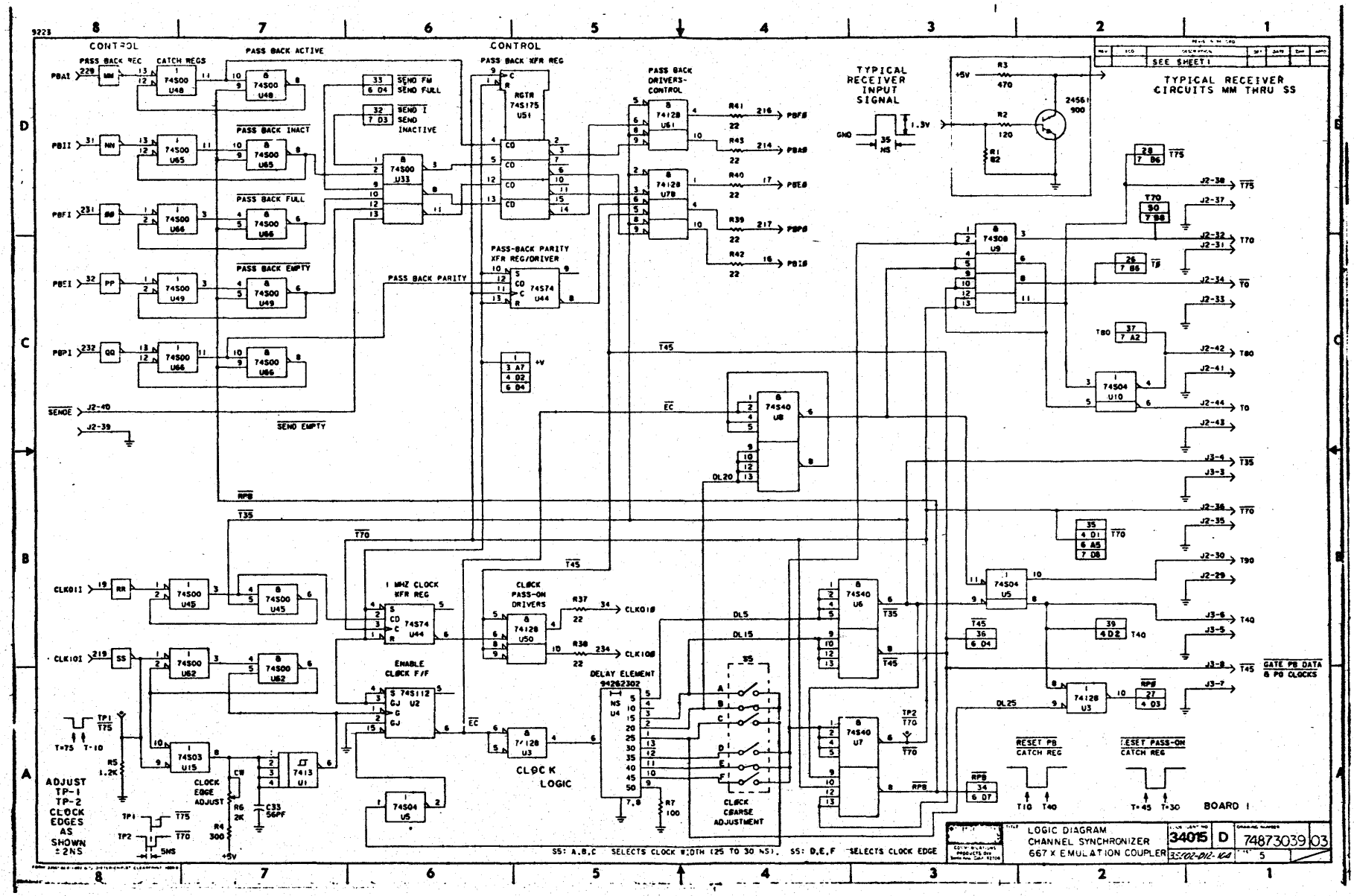
CONTROL DATA CORPORATION — PRODUCED BY PUBLICATIONS — Santa Ana, Calif. 92705

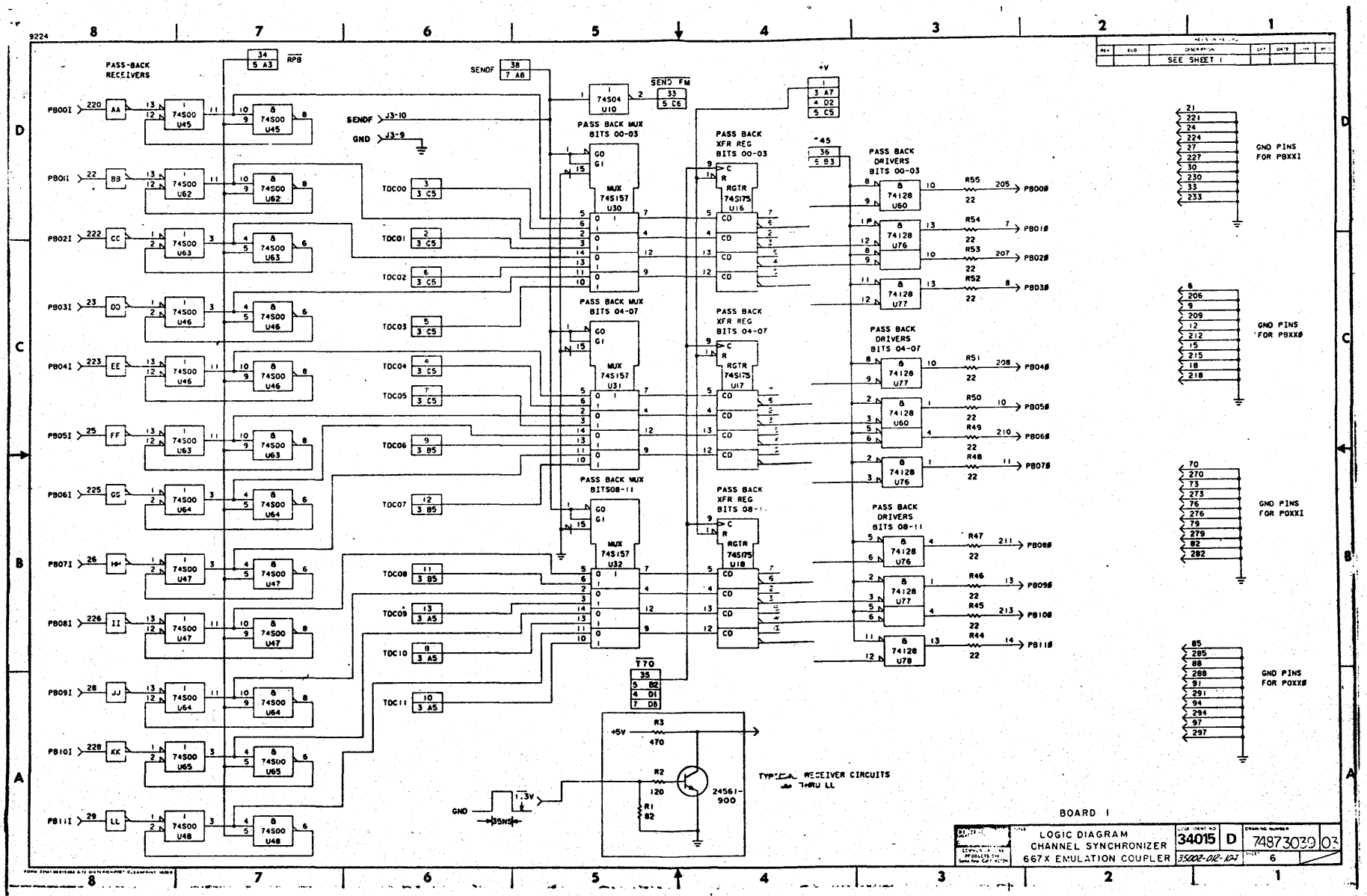
TITLE: LOGIC DIAGRAM— KEY TO SYMBOLS

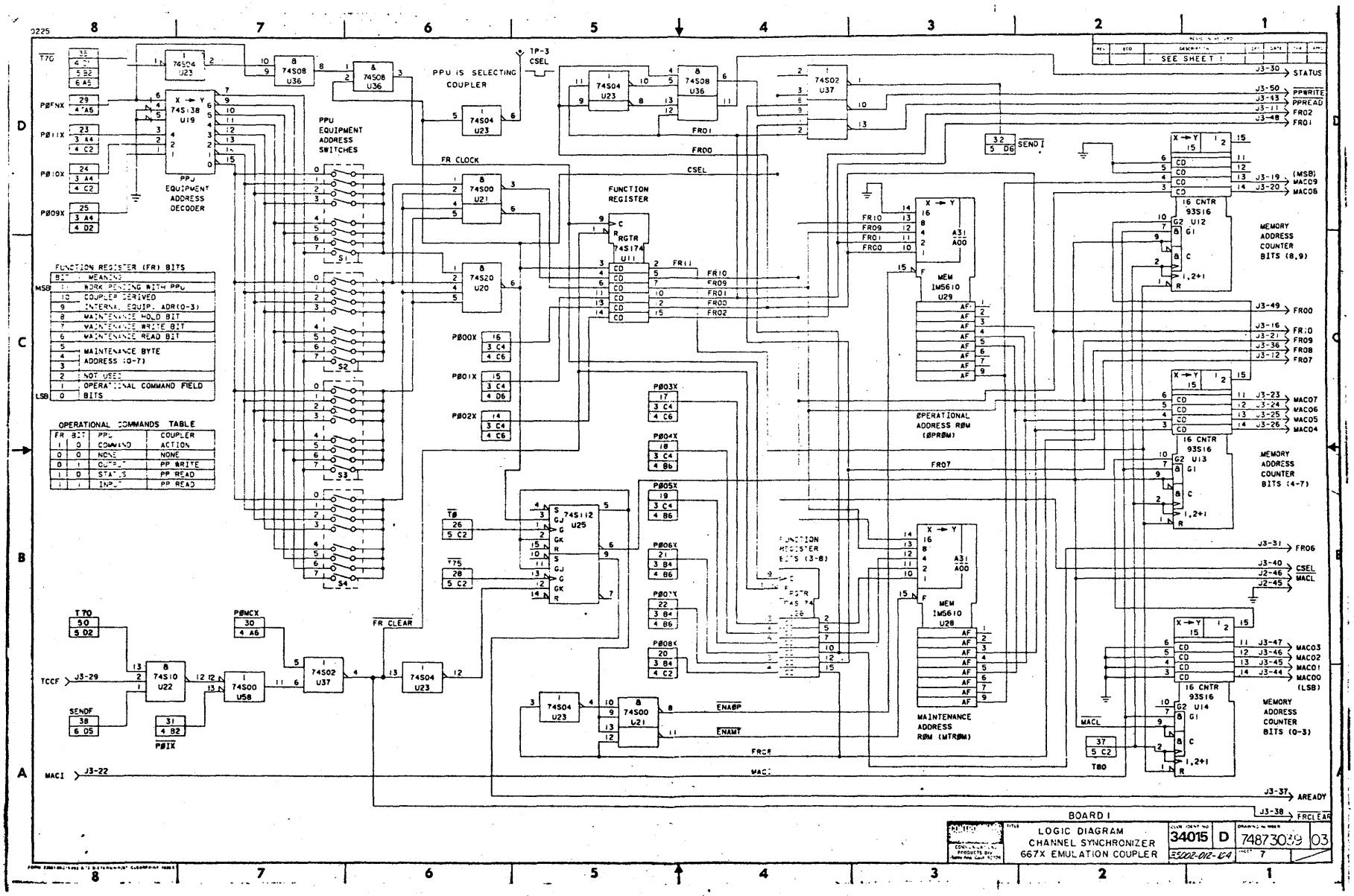
CDC GENT NO		DRAWING NUMBER
34015	D	74873039 03
35002-012-104		SHEET 2

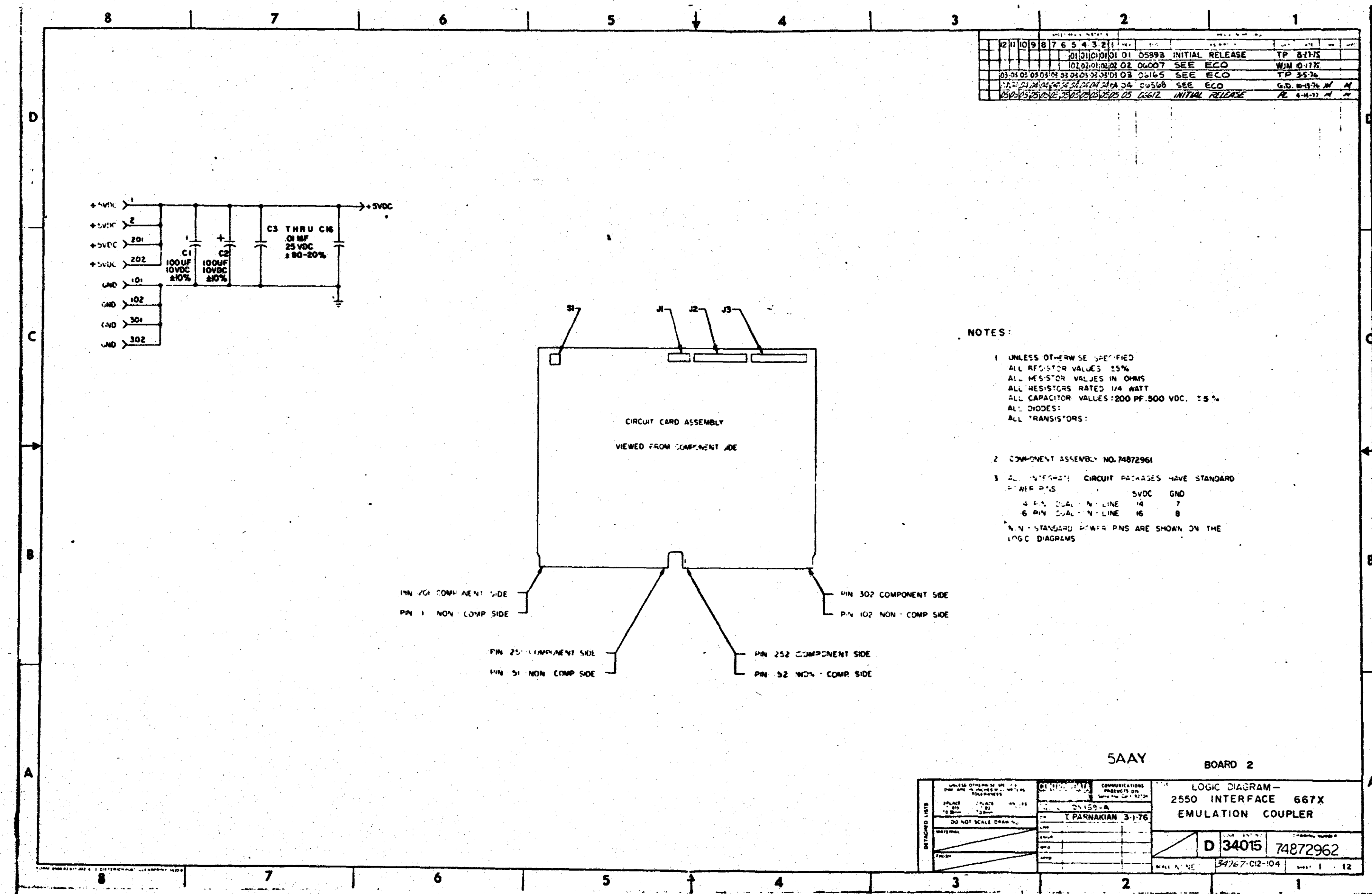

TO DATA CHANNEL REGISTER
FROM DATA CHANNEL REGISTER
SEE SHEET 1
DFM0 J2-4 GND J2-3
DFM1 J2-6 GND J2-5
DFM2 J2-10 GND J2-9
DFM3 J2-12 GND J2-11
DFM4 J2-2 GND J2-1
DFM5 J2-8 GND J2-7
DFM6 J2-18 GND J2-17
DFM7 J2-24 GND J2-23
DFMBW J2-26 GND J2-25
DFM9 J2-22 GND J2-21
DFM10 J2-16 GND J2-15
DFM11 J2-20 GND J2-19
FDCL J2-28 GND J2-27
TDCL J2-14 GND J2-13
RGTR 74S174 U34
RGTR 74S174 U35
RGTR 74S174 U24
RGTR 74S174 U27
TDC00
TDC01
TDC02
TDC03
TDC04
TDC05
TDC06
TDC07
TDC08
TDC09
TDC10
TDC11
P#00X
P#01X
P#02X
P#03X
P#04X
P#05X
P#06X
P#07X
P#08X
P#09X
P#10X
P#11X
J3-28 FDC0
J3-27 FDC1
J3-32 FDC2
J3-33 FDC3
J3-17 FDC4
J3-18 FDC5
J3-13 FDC6
J3-15 FDC7
J3-14 FDC8
J3-41 FDC9
J3-39 FDC10
J3-42 FDC11
74128 U3
+V
BOARD 1
LOGIC DIAGRAM – CHANNEL SYNCHRONIZER 667X EMULATION COUPLER
34015 D 74873039 03
SHEET 3


PASS-ON RECEIVERS
PASS-ON CATCH REGISTERS
RESET PASS-ON CATCH REG
PASS-ON XFR REG BITS 00-03
PASS-ON DRIVERS BITS 00-03
PASS-ON XFR REG BITS 04-07
PASS-ON DRIVERS BITS 04-07
PASS-ON XFR REG CONTROL BITS
PASS-ON DRIVERS CONTROL
PASS-ON XFR REG BITS 08-11
PASS-ON DRIVERS BITS 08-11
PASS-ON XFR REG CONTROL BITS
PASS-ON DRIVERS, CONTROL BITS
TRANSFER CATCH REG TO XFR REG
TYPICAL RECEIVER INPUT SIGNAL
TYPICAL RECEIVER CIRCUITS A THRU S
N/C PBPX
N/C PBEX
BOARD 1
LOGIC DIAGRAM
CHANNEL SYNCHRONIZER
667X EMULATION COUPLER
34015
D
74873039
03


CONTROL
PASS BACK REC
CATCH REGS
PASS BACK ACTIVE
PASS BACK INACT
PASS BACK FULL
PASS BACK EMPTY
SEND FM
SEND FULL
SEND I
SEND INACTIVE
SEND EMPTY
PASS BACK PARITY
PASS BACK XFR REG
PASS BACK DRIVERS-CONTROL
PASS-BACK PARITY XFR REG/DRIVER
TYPICAL RECEIVER INPUT SIGNAL
TYPICAL RECEIVER CIRCUITS MM THRU SS
1 MHZ CLOCK XFR REG
CLOCK PASS-ON DRIVERS
ENABLE CLOCK F/F
DELAY ELEMENT 94262302
CLOCK LOGIC
CLOCK COARSE ADJUSTMENT
CLOCK EDGE ADJUST
ADJUST TP-1 TP-2 CLOCK EDGES AS SHOWN ±2NS
RESET PB CATCH REG
RESET PASS-ON CATCH REG
GATE PB DATA & PB CLOCKS
SS: A,B,C SELECTS CLOCK WIDTH (25 TO 30 NS). SS: D,E,F SELECTS CLOCK EDGE
LOGIC DIAGRAM
CHANNEL SYNCHRONIZER
667 X EMULATION COUPLER
34015
D
74873039 03
BOARD 1

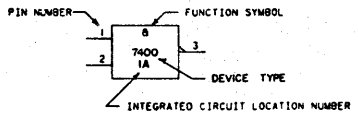

9224
PASS-BACK RECEIVERS
RPB
SENDF
SENDF J3-10
GND J3-9
SEND FM
+V
PASS BACK MUX BITS 00-03
PASS BACK MUX BITS 04-07
PASS BACK MUX BITS08-11
PASS BACK XFR REG BITS 00-03
PASS BACK XFR REG BITS 04-07
PASS BACK XFR REG BITS 08-11
PASS BACK DRIVERS BITS 00-03
PASS BACK DRIVERS BITS 04-07
PASS BACK DRIVERS BITS 08-11
GND PINS FOR PBXXI
GND PINS FOR PBXX0
GND PINS FOR POXXI
GND PINS FOR POXX0
TYPICAL RECEIVER CIRCUITS
THRU LL
BOARD 1
LOGIC DIAGRAM
CHANNEL SYNCHRONIZER
667X EMULATION COUPLER
34015
D
74873039 03
6

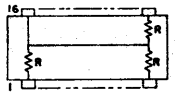

PPU EQUIPMENT ADDRESS SWITCHES
PPU EQUIPMENT ADDRESS DECODER
PPU IS SELECTING COUPLER
FUNCTION REGISTER
FR CLOCK
FR CLEAR
CSEL
FRO0
FRO1
FRO7
SEND I
SEND F
FUNCTION REGISTER (FR) BITS
OPERATIONAL COMMANDS TABLE
OPERATIONAL ADDRESS RAM (OPRAM)
MAINTENANCE ADDRESS RAM (MTRAM)
MEMORY ADDRESS COUNTER BITS (8,9)
MEMORY ADDRESS COUNTER BITS (4-7)
MEMORY ADDRESS COUNTER BITS (0-3)
STATUS
PPWRITE
PPREAD
FRO2
FRO1
FRO0
FR10
FR09
FR08
FR07
FR06
CSEL
MACL
MACI
AREADY
FRCLEAR
BOARD I
LOGIC DIAGRAM
CHANNEL SYNCHRONIZER
667X EMULATION COUPLER
34015 D
74873039 03


+5VDC
GND
1
2
201
202
101
102
301
302
C1
100UF
10VDC
±10%
C2
100UF
10VDC
±10%
C3 THRU C16
.01 MF
25 VDC
+80-20%
+5VDC
S1
J1
J2
J3
CIRCUIT CARD ASSEMBLY
VIEWED FROM COMPONENT SIDE
PIN 201 COMPONENT SIDE
PIN 1 NON - COMP SIDE
PIN 251 COMPONENT SIDE
PIN 51 NON COMP SIDE
PIN 252 COMPONENT SIDE
PIN 52 NON - COMP SIDE
PIN 302 COMPONENT SIDE
PIN 102 NON - COMP SIDE
01 05893 INITIAL RELEASE
02 06007 SEE ECO
03 06165 SEE ECO
04 06568 SEE ECO
05 06612 INITIAL RELEASE
NOTES:
1 UNLESS OTHERWISE SPECIFIED
ALL RESISTOR VALUES ±5%
ALL RESISTOR VALUES IN OHMS
ALL RESISTORS RATED 1/4 WATT
ALL CAPACITOR VALUES : 200 PF.500 VDC. ±5%
ALL DIODES:
ALL TRANSISTORS:
2 COMPONENT ASSEMBLY NO. 74872961
3 ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS
5VDC GND
14 PIN DUAL - IN - LINE 14 7
16 PIN DUAL - IN - LINE 16 8
NON - STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS
5AAY
BOARD 2
DO NOT SCALE DRAWING
COMMUNICATIONS PRODUCTS DIV
T. PARNAKIAN 3-1-76
LOGIC DIAGRAM—
2550 INTERFACE 667X
EMULATION COUPLER
D
34015
74872962
34767-C12-104
1
12

6650

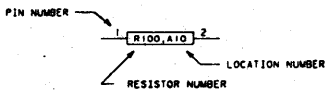
CIRCUIT ELEMENT SYMBOLOGY



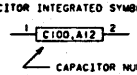


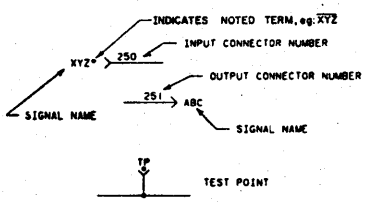
LC. RESISTOR PACK
LOCATION C6-2K
B7-1K

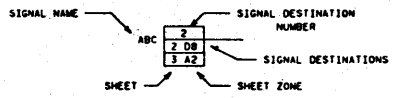
RESISTOR INTEGRATED SYMBOLOGY



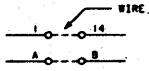
CAPACITOR INTEGRATED SYMBOLOGY







COMMON CONTROL BLOCK.
SIGNALS ENTERING THIS BLOCK
ARE COMMON TO MORE THAN ONE
SECTION OF THE CIRCUIT



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	74	TTL DUAL 2-INPUT NOR
	7434	TTL QUAD 2-INPUT MULTIPLEXER OPN COLLECTOR
	74504	TTL HEX INVERTER
	74	TTL DUAL 4-INPUT NAND
	7412	TTL TRIPLE 3-INPUT NAND
	74	TTL DUAL 4-INPUT NAND
	74	TTL QUAD 4-INPUT NAND BUFFER
	7493	TTL DUAL 4 BIT BINARY COUNTER
	74	TTL DUAL D-TYPE FLIP FLOP
	8T97	DRIVER, TTL HEX TRISTATE
	745157	MUX, TTL QUAD 2 INPUT
	74	LATCH, TTL 8 BIT D-TYPE
	7451	TTL TRIPLE 3-INPUT AND
	74532	TTL QUAD 2-INPUT OR
	745136	TTL QUAD 2-INPUT EXCLUSIVE OR / NOR
	74530	TTL 8-INPUT NAND
	745260	TTL 5-INPUT NOR
	93421	1/(n) - 256 X 1 BIT ACTIVE LOW OUTPUT
		TTL TRIPLE 3-INPUT AND
	8T94	HEX TRI-STATE INVERTING GATE
	7417	REGISTER, TTL HEX BUFFER (OC)
	9101S	MEMORY, TTL 16-4 BIT (1024 BIT RAM (DE)
	745154	MUX, TTL QUAD 2-INPUT
	74538	TTL QUAD 2-INPUT NAND BUFFER (OC)
	745139	DECODER, TTL DUAL (1 OF 4)

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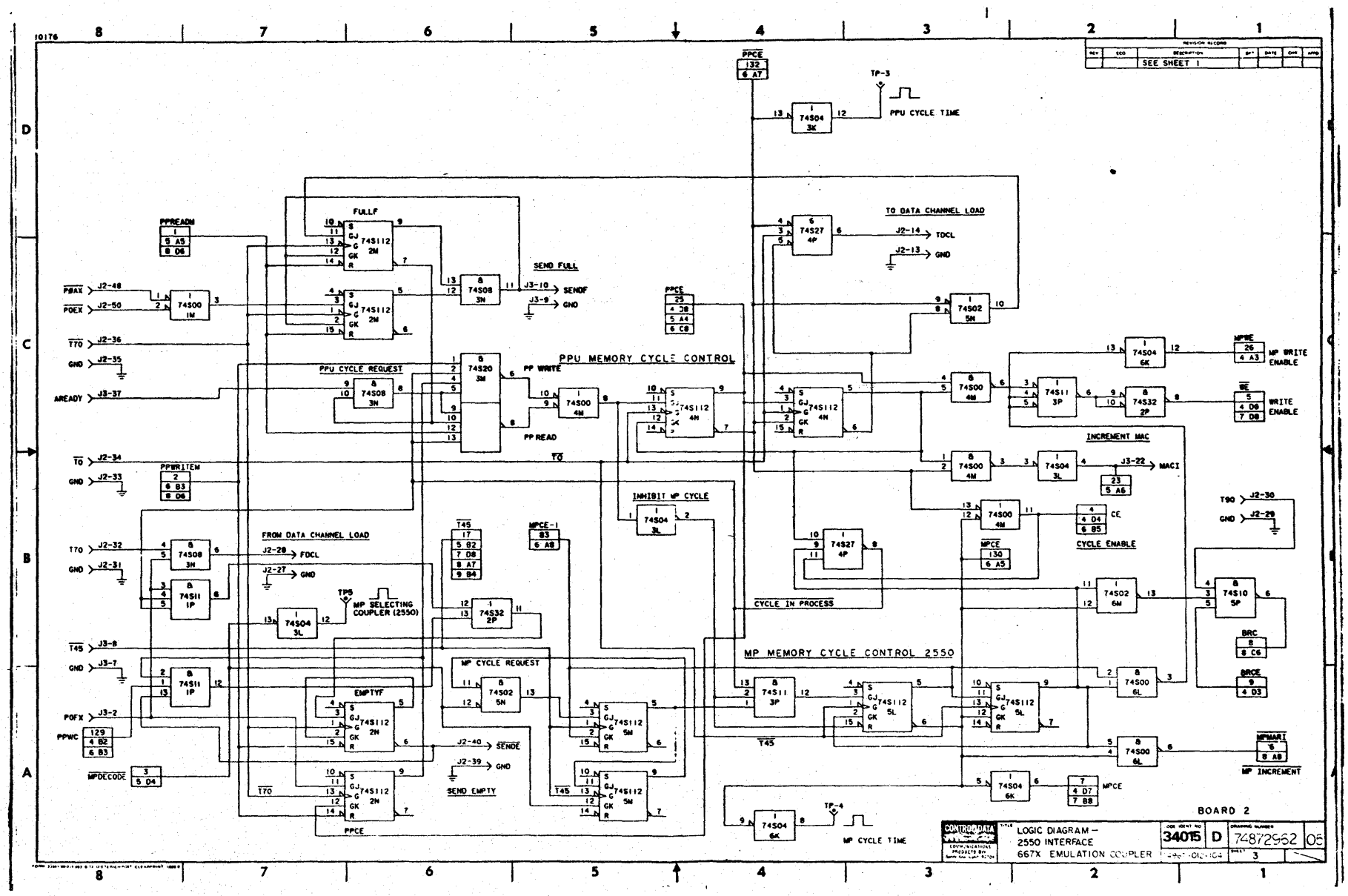
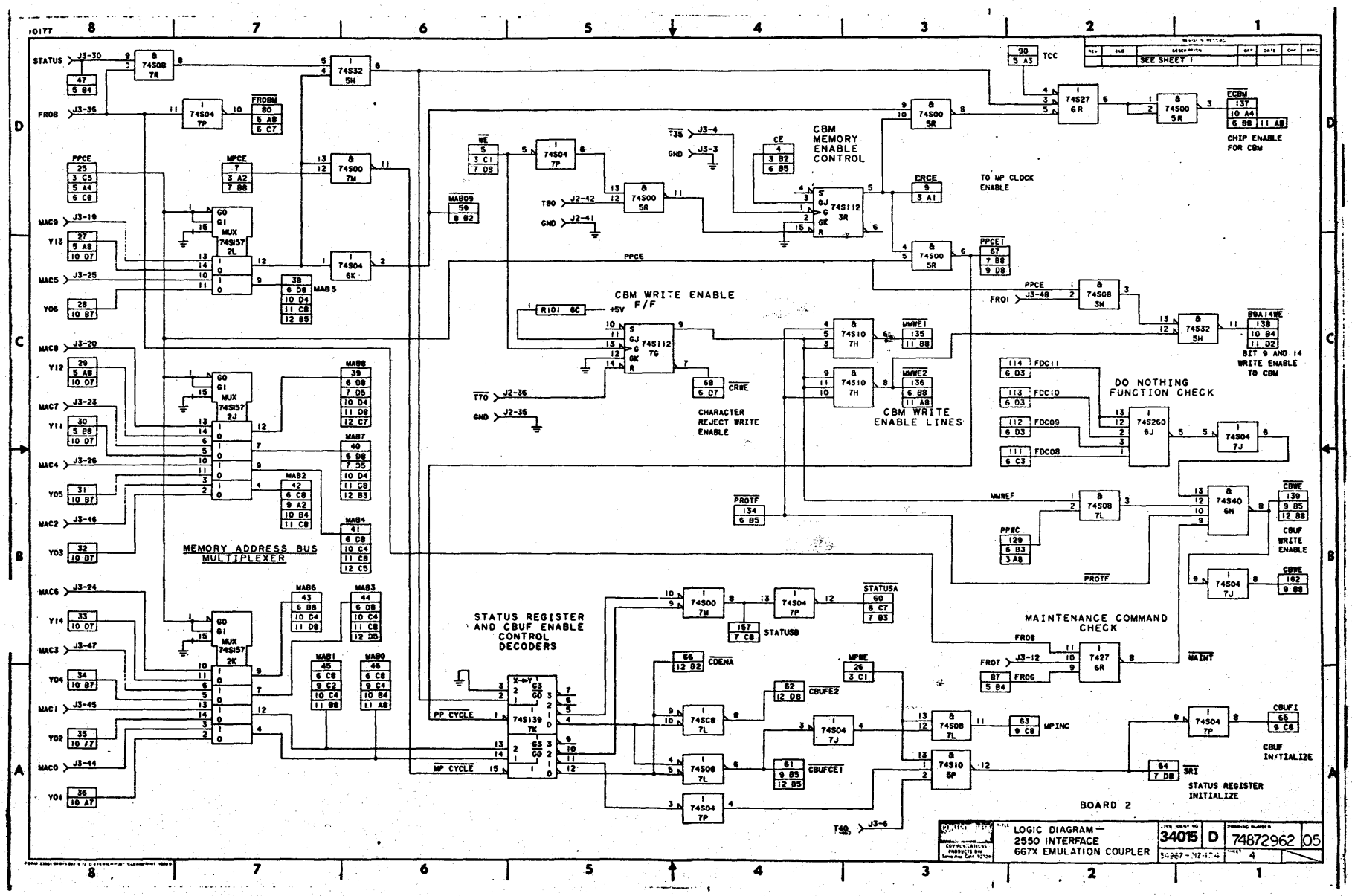
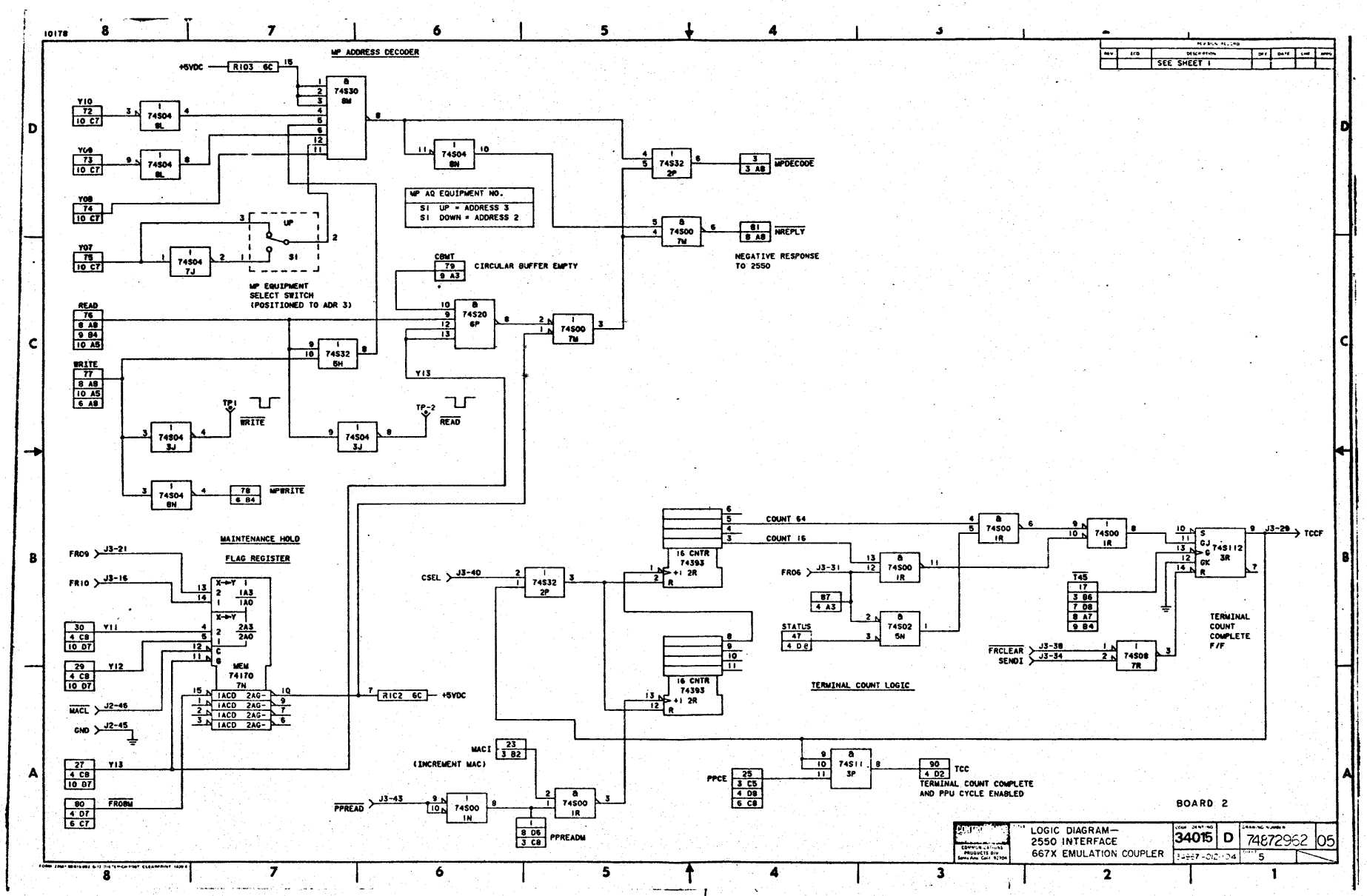
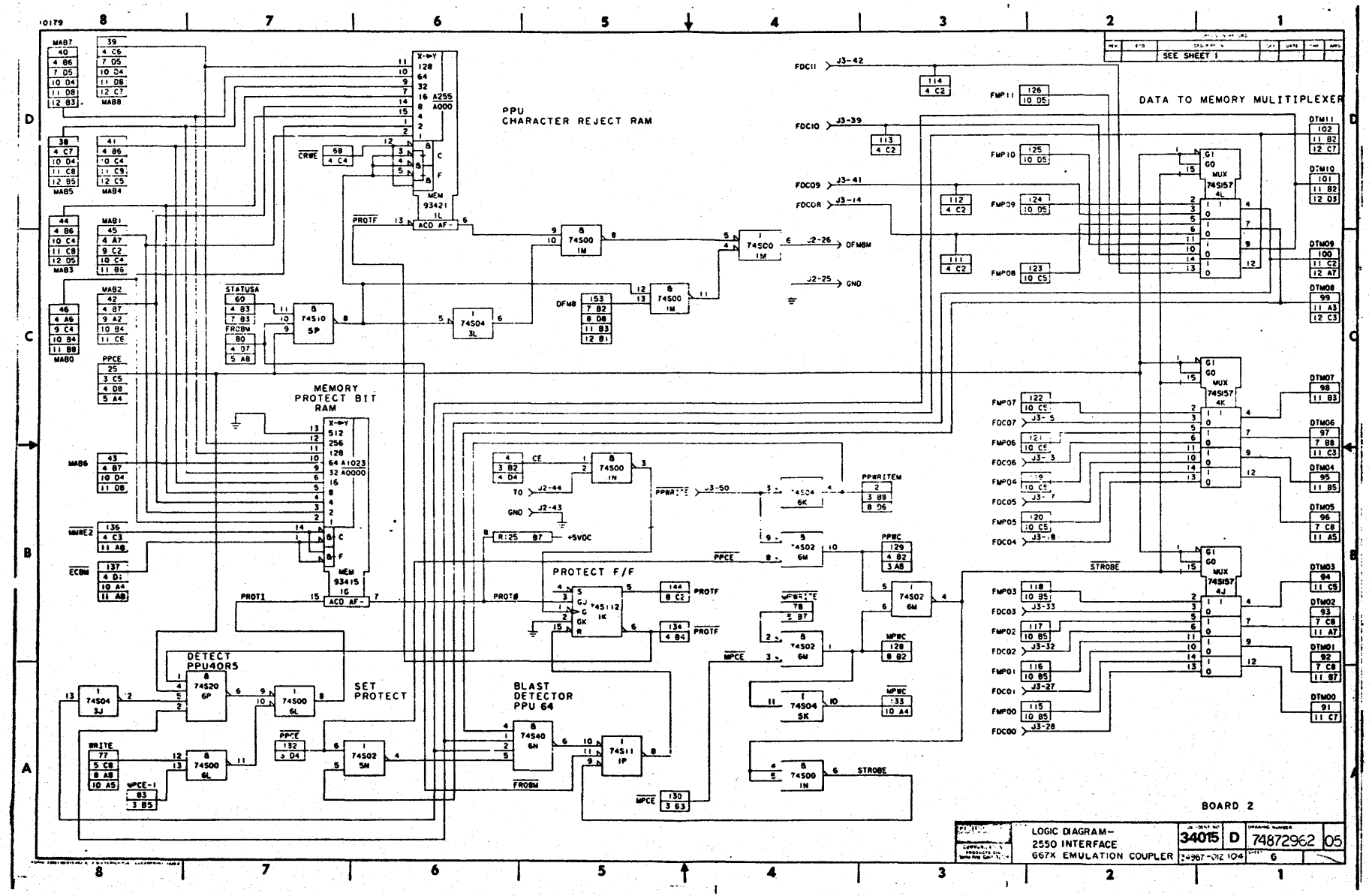
RGTR	REGISTER
SHN-M	SHIFT REGISTER
DEMUX	DEMULTIPLEXER

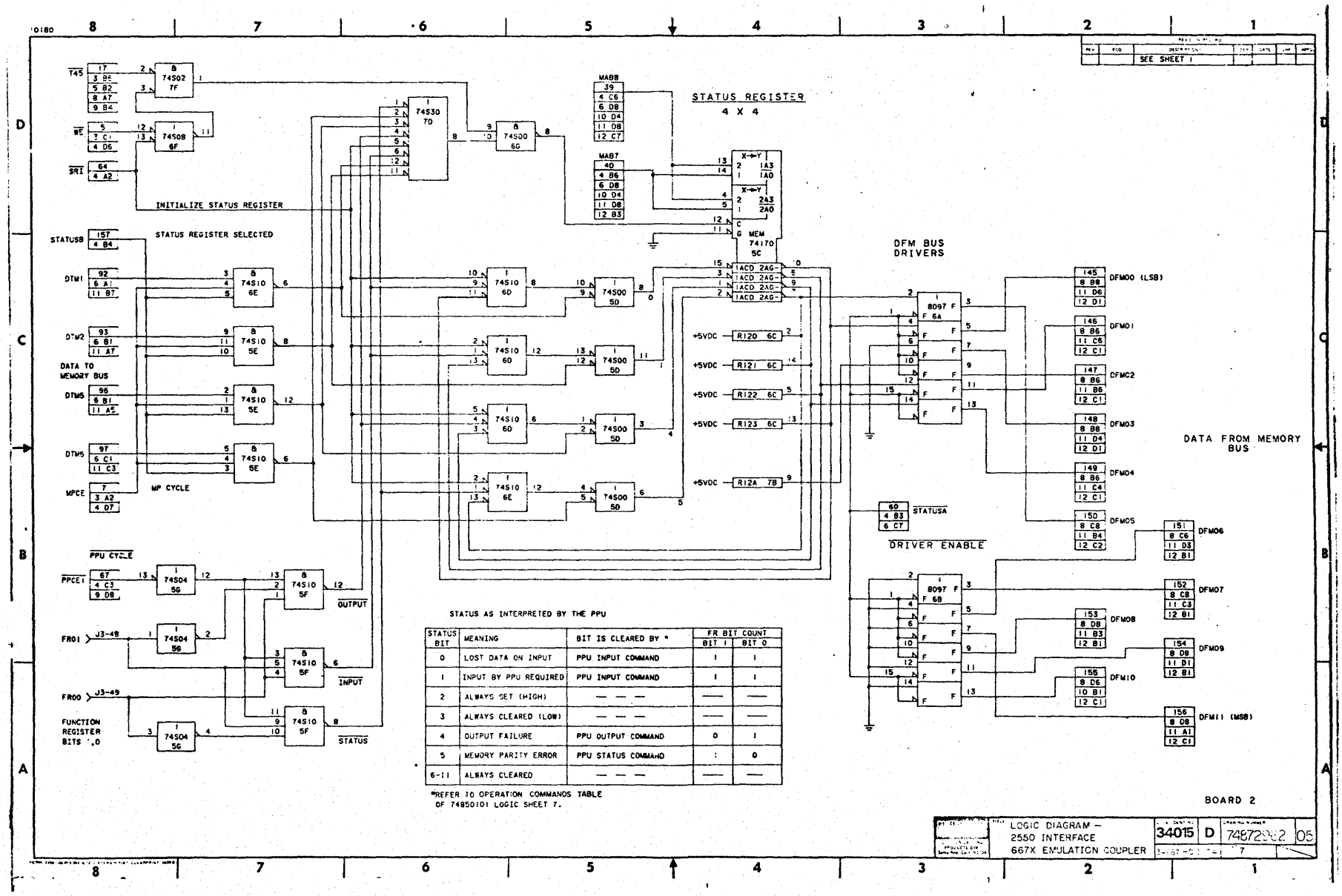
CONTROL DATA CORPORATION COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92705	TITLE: LOGIC DIAGRAM— KEY TO SYMBOLS	DWN DEPT NO 34015	D	DRAWING NUMBER 74872962	05
				SHEET 2	


PPCE
TP-3
PPU CYCLE TIME
SEE SHEET 1
TO DATA CHANNEL LOAD
J2-14 TDCL
J2-13 GND
FULLF
SEND FULL
J3-10 SENDF
J3-9 GND
PPREADM
PBAX J2-48
PDEX J2-50
T70 J2-36
GND J2-35
AREADY J3-37
PPU MEMORY CYCLE CONTROL
PPU CYCLE REQUEST
PP WRITE
PP READ
T0 J2-34
GND J2-33
PPWRITEM
INHIBIT MP CYCLE
INCREMENT MAC
J3-22 MACI
MPWE
MP WRITE ENABLE
WE
WRITE ENABLE
T90 J2-30
GND J2-29
CE
CYCLE ENABLE
MPCE
CYCLE IN PROCESS
FROM DATA CHANNEL LOAD
J2-28 FDCL
J2-27 GND
TP5
MP SELECTING COUPLER (2550)
MPCE-1
T45
MP MEMORY CYCLE CONTROL 2550
BRC
BRCE
T45 J3-8
GND J3-7
MP CYCLE REQUEST
EMPTYF
PDFX J3-2
PPWC
MPDECODE
J2-40 SENDE
J2-39 GND
SEND EMPTY
MPMARI
MP INCREMENT
TP-4
MP CYCLE TIME
BOARD 2
LOGIC DIAGRAM — 2550 INTERFACE 667X EMULATION COUPLER
34015 D 74872952 05
SHEET 3


STATUS
FRO8
MEMORY ADDRESS BUS MULTIPLEXER
CBM MEMORY ENABLE CONTROL
CBM WRITE ENABLE F/F
CBM WRITE ENABLE LINES
CHARACTER REJECT WRITE ENABLE
DO NOTHING FUNCTION CHECK
STATUS REGISTER AND CBUF ENABLE CONTROL DECODERS
MAINTENANCE COMMAND CHECK
CHIP ENABLE FOR CBM
TO MP CLOCK ENABLE
BIT 9 AND 14 WRITE ENABLE TO CBM
CBUF WRITE ENABLE
CBUF INITIALIZE
STATUS REGISTER INITIALIZE
BOARD 2
LOGIC DIAGRAM — 2550 INTERFACE 667X EMULATION COUPLER
34015 D 74872962 05
SHEET 4


MP ADDRESS DECODER
+5VDC
R103 6C
SEE SHEET 1
MP AQ EQUIPMENT NO.
S1 UP = ADDRESS 3
S1 DOWN = ADDRESS 2
MP EQUIPMENT SELECT SWITCH (POSITIONED TO ADR 3)
MPDECODE
NREPLY
NEGATIVE RESPONSE TO 2550
CBMT
CIRCULAR BUFFER EMPTY
READ
WRITE
MPWRITE
MAINTENANCE HOLD FLAG REGISTER
COUNT 64
COUNT 16
TERMINAL COUNT LOGIC
TERMINAL COUNT COMPLETE F/F
TCCF
TCC
TERMINAL COUNT COMPLETE AND PPU CYCLE ENABLED
MACI
(INCREMENT MAC)
PPREADM
BOARD 2
LOGIC DIAGRAM— 2550 INTERFACE 667X EMULATION COUPLER
34015 D 74872962 05

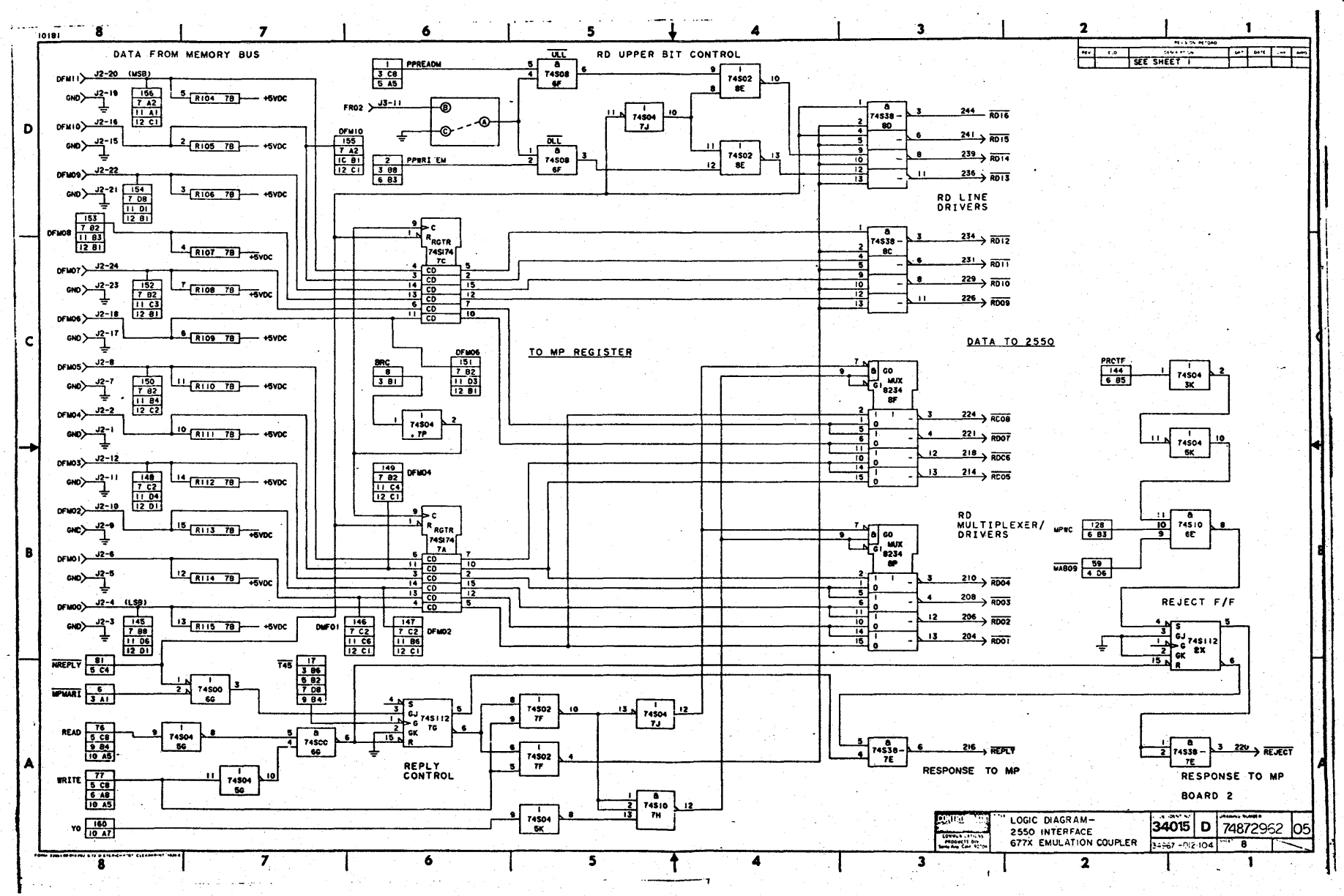

PPU
CHARACTER REJECT RAM
DATA TO MEMORY MULITIPLEXER
MEMORY
PROTECT BIT
RAM
PROTECT F/F
DETECT
PPU4OR5
SET
PROTECT
BLAST
DETECTOR
PPU 64
SEE SHEET 1
BOARD 2
LOGIC DIAGRAM-
2550 INTERFACE
667X EMULATION COUPLER
34015
D
74872962
05
6

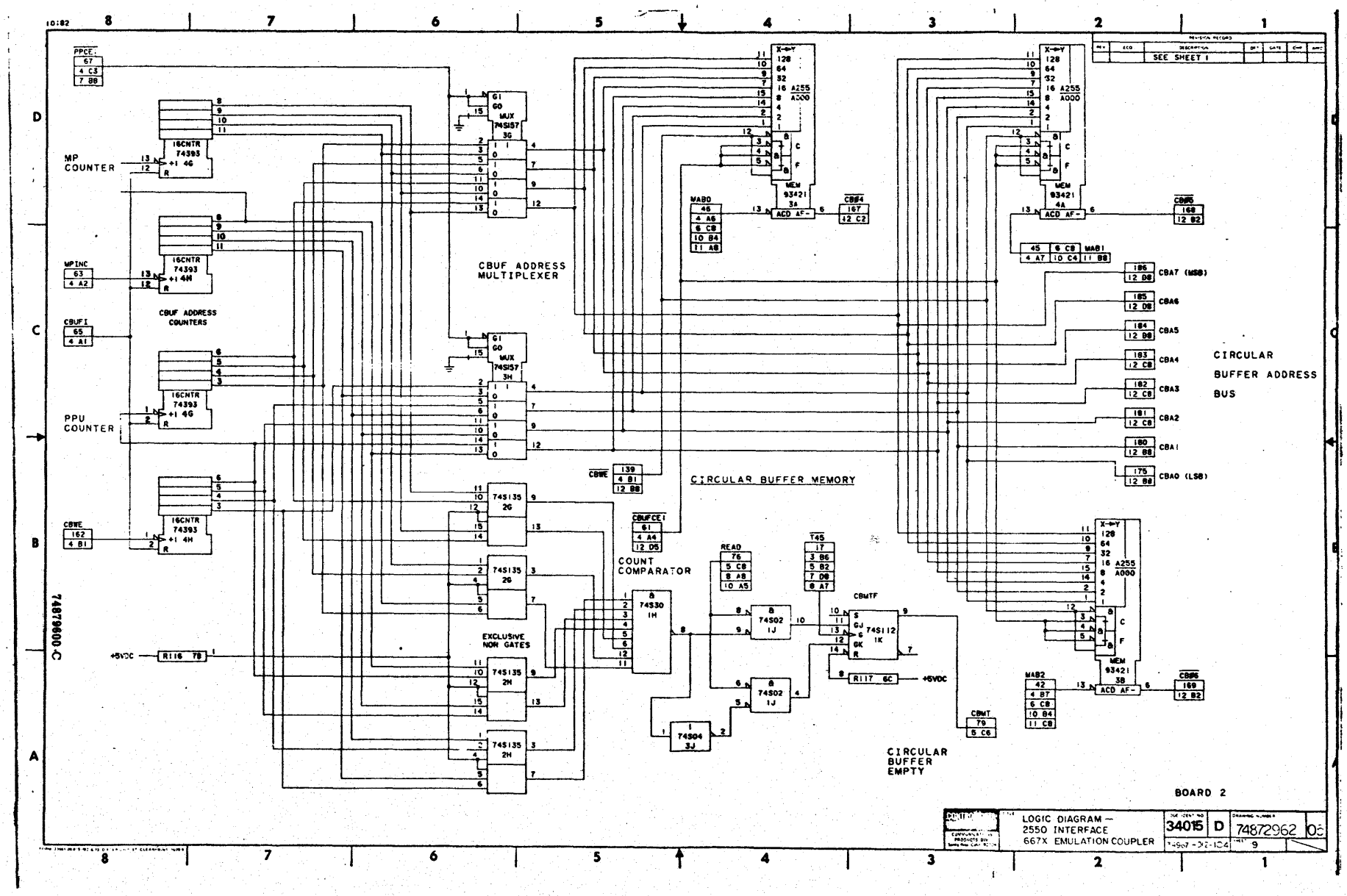


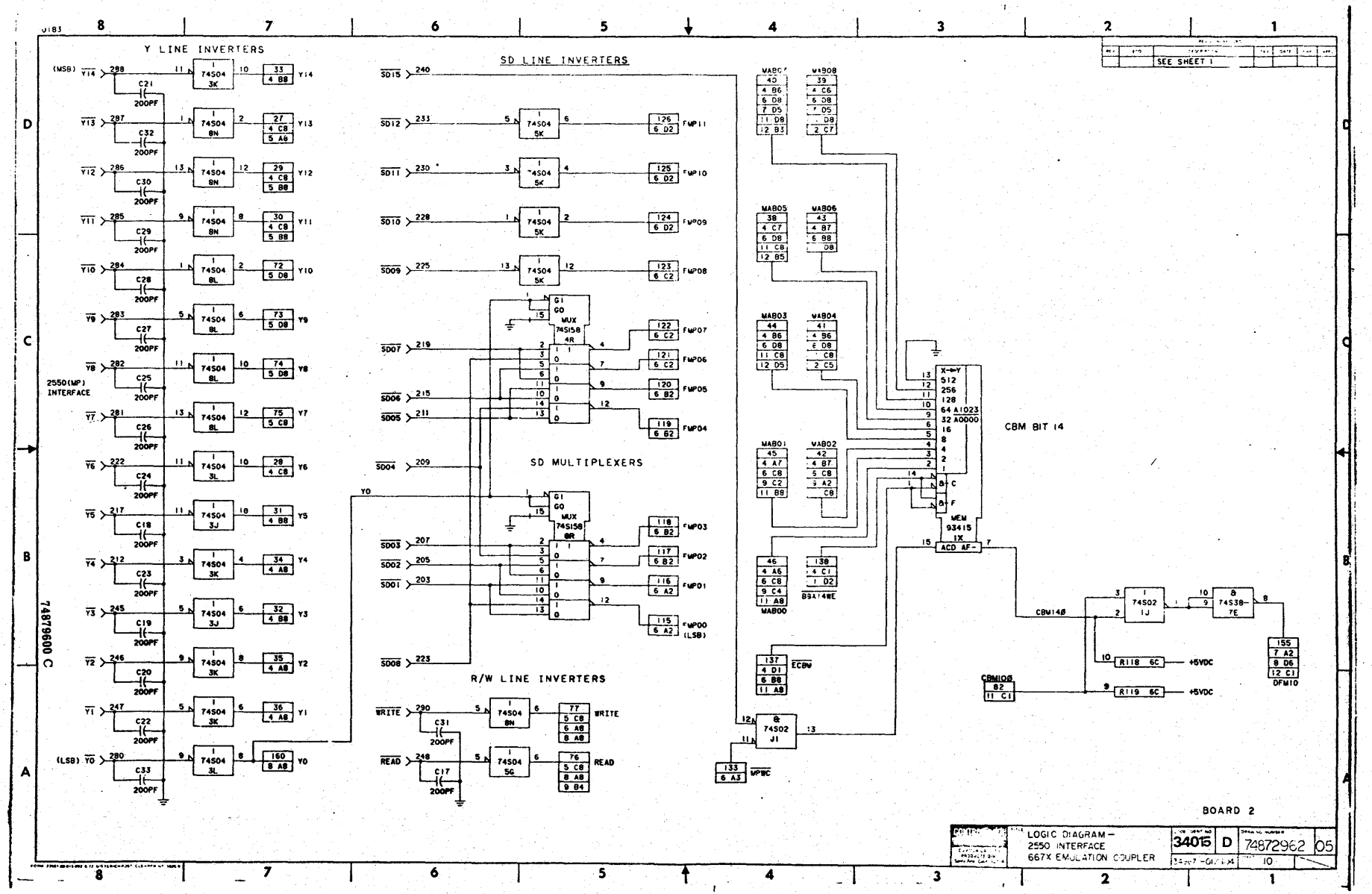
STATUS AS INTERPRETED BY THE PPU

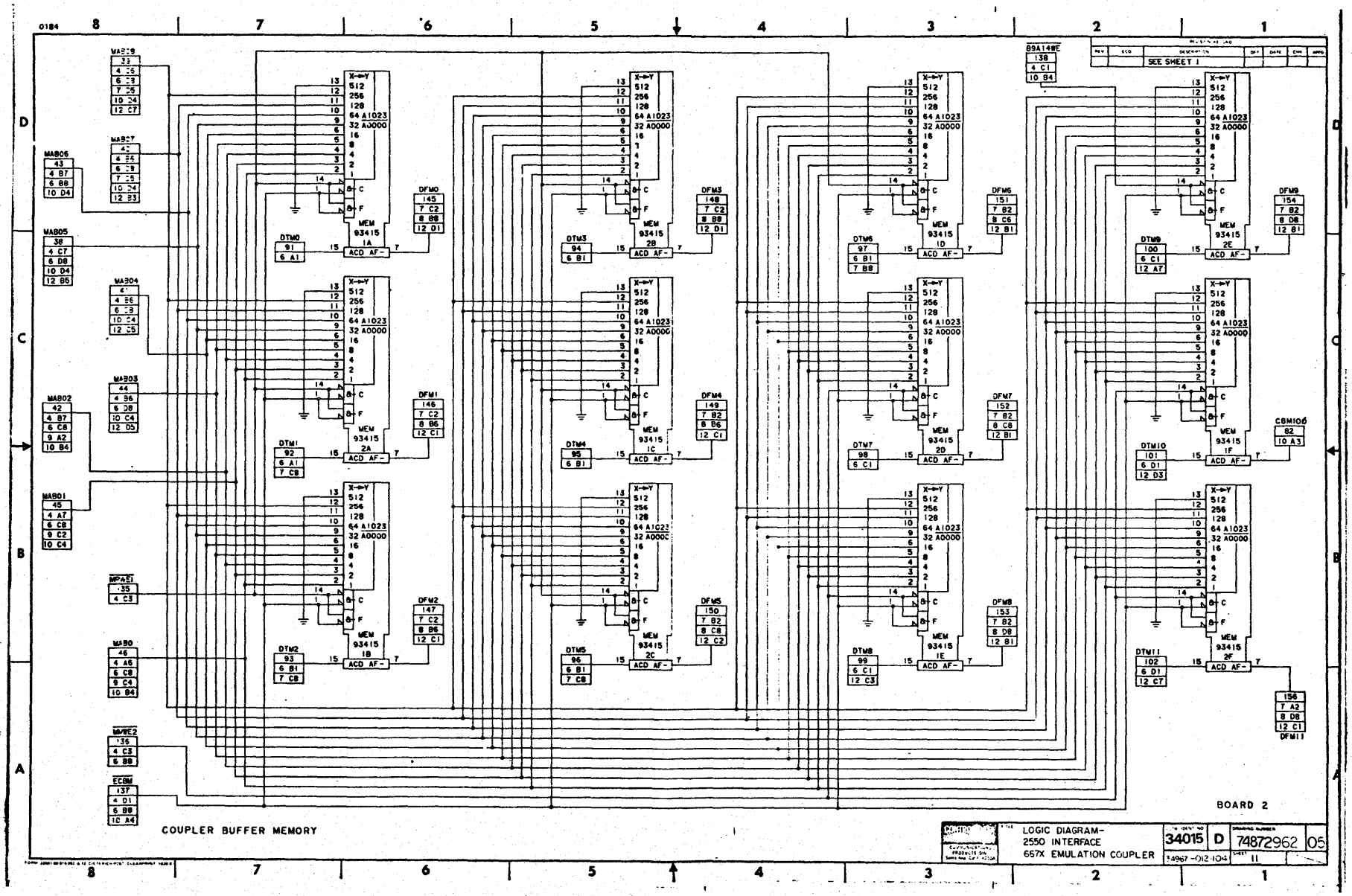
STATUS BIT	MEANING	BIT IS CLEARED BY *	FR BIT COUNT BIT 1	FR BIT COUNT BIT 0
0	LOST DATA ON INPUT	PPU INPUT COMMAND	1	1
1	INPUT BY PPU REQUIRED	PPU INPUT COMMAND	1	1
2	ALWAYS SET (HIGH)	— — —	——	——
3	ALWAYS CLEARED (LOW)	— — —	——	——
4	OUTPUT FAILURE	PPU OUTPUT COMMAND	0	1
5	MEMORY PARITY ERROR	PPU STATUS COMMAND	1	0
6-11	ALWAYS CLEARED	— — —	——	——

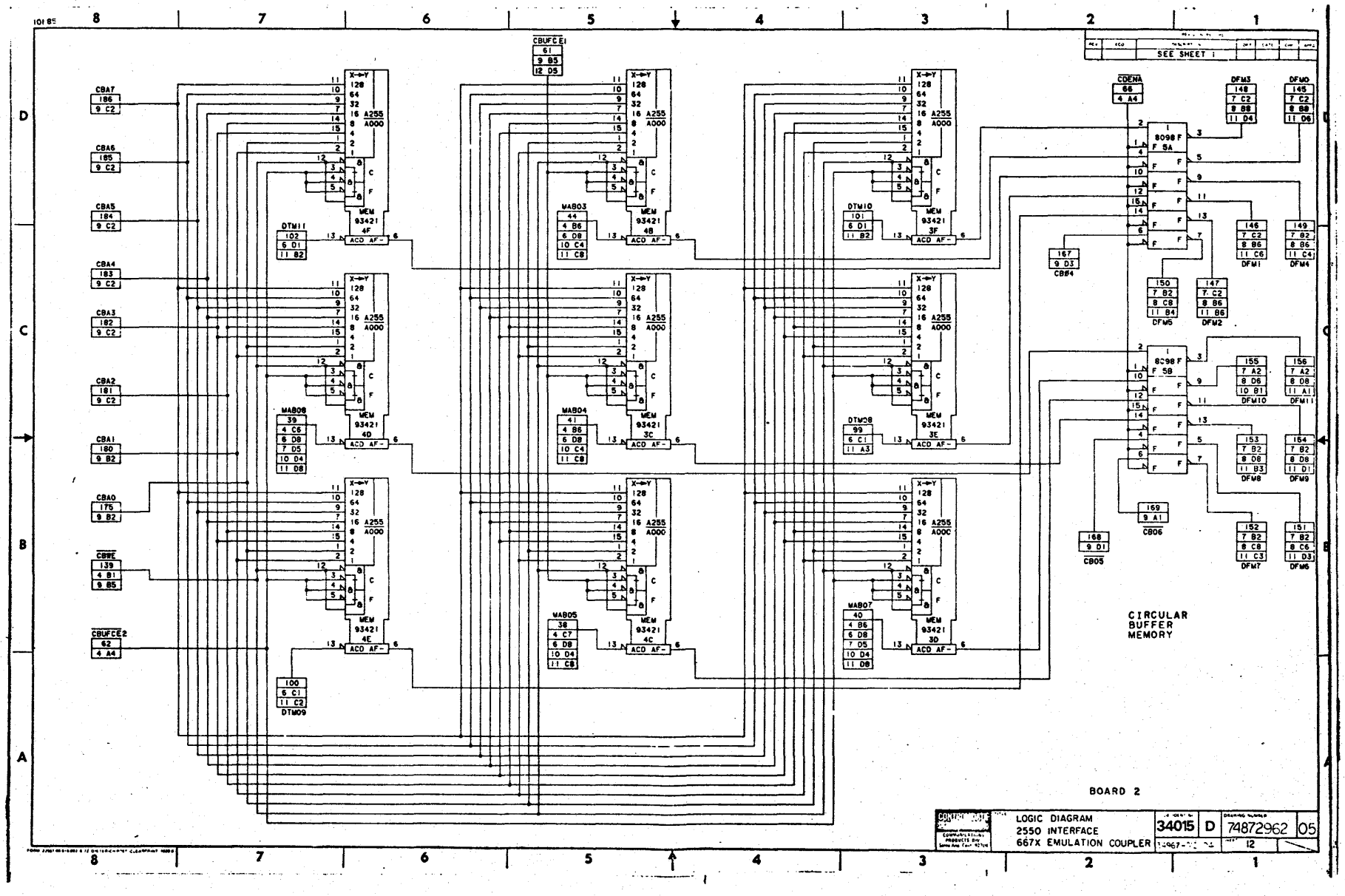
*REFER TO OPERATION COMMANDS TABLE OF 74850101 LOGIC SHEET 7.


DATA FROM MEMORY BUS
RD UPPER BIT CONTROL
SEE SHEET 1
RD LINE DRIVERS
TO MP REGISTER
DATA TO 2550
RD MULTIPLEXER/ DRIVERS
REJECT F/F
REPLY CONTROL
RESPONSE TO MP
RESPONSE TO MP
BOARD 2
LOGIC DIAGRAM- 2550 INTERFACE 677X EMULATION COUPLER
34015
D
74872962
05


MP COUNTER
MPINC
CBUFI
PPU COUNTER
CBWE
CBUF ADDRESS COUNTERS
16CNTR 74393
CBUF ADDRESS MULTIPLEXER
MUX 74S157
CIRCULAR BUFFER MEMORY
CIRCULAR BUFFER ADDRESS BUS
CBAT (MSB)
CBA6
CBA5
CBA4
CBA3
CBA2
CBA1
CBA0 (LSB)
COUNT COMPARATOR
EXCLUSIVE NOR GATES
CIRCULAR BUFFER EMPTY
CBMTF
READ
T45
MEM 93421
ACD AF-
SEE SHEET 1
BOARD 2
LOGIC DIAGRAM — 2550 INTERFACE 667X EMULATION COUPLER
34015
D
74872962
05
9


Y LINE INVERTERS
SD LINE INVERTERS
SD MULTIPLEXERS
R/W LINE INVERTERS
2550(MP) INTERFACE
CBM BIT 14
SEE SHEET 1
BOARD 2
LOGIC DIAGRAM — 2550 INTERFACE 667X EMULATION COUPLER
34015
D
74872962
05
74879600 C


SEE SHEET 1
COUPLER BUFFER MEMORY
BOARD 2
LOGIC DIAGRAM-
2550 INTERFACE
667X EMULATION COUPLER
34015
D
74872962
05


SEE SHEET 1
CBUFCE1
CBA7
CBA6
CBA5
CBA4
CBA3
CBA2
CBA1
CBA0
CBWE
CBUFCE2
CDENA
DFM3
DFM0
DFM1
DFM4
DFM5
DFM2
DFM10
DFM11
DFM8
DFM9
DFM7
DFM6
CB04
CB06
CB05
DTM11
DTM10
DTM08
DTM09
MAB06
MAB03
MAB04
MAB05
MAB07
X→Y
128
64
32
16 A255
8 A000
4
2
1
MEM
93421
ACD AF-
4F
4B
3F
4D
3C
3E
4E
4C
3D
8098 F
F 5A
F 5B
CIRCULAR
BUFFER
MEMORY
BOARD 2
LOGIC DIAGRAM
2550 INTERFACE
667X EMULATION COUPLER
34015
D
74872962
05

This section contains preventive maintenance procedures and corrective maintenance aids. When trouble-shooting a defective coupler, refer to theory of operation and logic diagrams. Supplementary maintenance aids are included in appendices.

PREVENTIVE MAINTENANCE

The following paragraphs contain procedures which if performed periodically will minimize subsystem down-time due to coupler malfunctions. Maintain a log to ensure faithful observance of maintenance periods. Wherever maintenance periods are not given, refer to subsystem maintenance procedures.

TEST EQUIPMENT

The following items are needed to maintain the coupler.

1. One spare coupler including items 1 through 4 in table 3-1.
2. Two card extenders, part number 74537300.
3. One hardware maintenance manual, number 74849600.
4. One dual-trace, high-frequency oscilloscope, Tektronix 453 for example.
5. One complete set of subsystem diagnostic tapes, listed in NPU hardware maintenance manual.
6. One set of tools including a DIP clip and an acid brush.

EDGE CONNECTOR CLEANING

1. Remove subsystem power when cleaning edge connectors.
2. Pull the two circuit cards approximately two inches (50 mm) away from their mating connectors.
3. Re-insert the circuit cards until they once again mate with the connectors at the back of the card cage. Thus the connectors are cleaned by the wiping action of the connector contacts.
4. Whenever circuit cards are removed from the card cage, further clean the edge connectors with a magic-rub eraser. Use a clean acid brush to remove all eraser crumbs before re-inserting the circuit cards.

DIAGNOSTIC PROGRAMS

Perform subsystem diagnostics to check out the coupler at regular intervals. Refer to the NPU hardware maintenance manual for complete checkout procedures using the proper diagnostics. Perform these same checks substituting the spare coupler to ensure the integrity of the spare.

CLOCK ADJUSTMENTS

Annually check the clock adjustments on the synchronizer (figure 2-1) as follows.

1. Connect the channel 1 probe of the oscilloscope to TP-2.
2. Connect the channel 2 probe of the oscilloscope to TP-1.
3. Sync the oscilloscope on channel 1 on the negative-going edge.
4. Adjust R6 until the negative-going edge of channel 2 waveform lags the negative-going edge of channel 1 waveform by 5 $\pm$ 2 ns.
5. Verify that the width of the negative pulse of channel 1 is between 25 and 35 ns.

NOTE

This pulse width has been set at the factory. If it is less than 25 ns, it can be increased by changing the setting of S5 (figure 2-2). To do this, it may be necessary to remove power and pull the synchronizer out until S5 is accessible. S5-A through S5-D adjust pulse width. Position A is the narrowest, and each succeeding position increases pulse width by 5 ns. Only one of four positions should be ON.

6. If the clock adjustments cannot be made, check pin 219 of the synchronizer edge connector for a minimum pulse amplitude of 1.3 volts. If this 10 MHz incoming clock amplitude is OK, replace the synchronizer.

CORRECTIVE MAINTENANCE

The following paragraphs contain information that will aid you in trouble-shooting a suspected coupler malfunction. On-site maintenance consists of isolating and replacing a defective circuit card. The defective circuit card is then sent to a repair center where the defect is further isolated and repaired. The repaired circuit card is thoroughly tested before it is returned to the site.

TEST POINTS

The synchronizer has three test points which are accessible from the front of the card cage with the circuit card installed (figure 2-1). The interface has five test points which are similarly accessible (figure 2-2). Both circuit cards also have an accessible ground point. These eight test points are listed and explained.

Synchronizer Test Points

1. Signal $\overline{T75}$ is a 10 MHz clock. TP-1 is on sheet 5 of the logic diagram.

2. Signal $\overline{T70}$ is a 10 MHz clock. TP-2 is on sheet 5 of the logic diagram.

3. Signal $\overline{CSEL}$ goes low for the duration of the function signal when the host has selected the coupler for communications. TP-3 is on sheet 7 of the logic diagram.

Interface Test Points

1. Signal $\overline{WRITE}$ goes low when the processor requests a write memory cycle. TP-1 is on sheet 5 of the logic diagram.

2. Signal $\overline{READ}$ goes low when the processor requests a read memory cycle. TP-2 is on sheet 5 of the logic diagram.

3. Signal PPCE goes high when the coupler services a memory cycle request from the host. TP-3 is on sheet 3 of the logic diagram.

4. Signal MPCE goes high when the coupler services a memory cycle request from the processor. TP-4 is on sheet 3 of the logic diagram.

5. Signal MPDECODE goes high when the processor selects the coupler for communications. TP-5 is on sheet 5 of the logic diagram.

CIRCUIT CARD EXTENSION

1. Remove subsystem power when extending circuit cards.

2. Remove both circuit cards from the card cage at the same time without removing ribbon cables.

3. Install two card extenders in the card cage in place of the circuit cards.

4. Insert both circuit cards into the card extenders at the same time.

CONNECTOR PIN ASSIGNMENTS

A list of signals assigned to the connector pins of the ribbon cables is given in table 6-1. The pin assignments for the edge connectors of the synchronizer is given in table 6-2. Signals assigned to the edge connectors of the interface are listed in table 6-3. Edge connector signals can be accessed at the back of the card cage (figure 3-2).

CIRCUIT CARD SUBSTITUTION

Whenever a circuit card is suspected to be defective, the quickest way to test it is to substitute one of the spare circuit cards. It is recommended that both spare circuit cards be substituted at the same time as an initial test. If the substitution results in a correction of the malfunction, the defect can be further isolated to a single circuit card. Follow installation procedure when substituting the spares. It may not be desirable to further isolate the malfunction at the site, as removal of the synchronizer for any length of time may disturb channel communications. Both suspect circuit cards may be shipped to a repair center with the ribbon cables installed.

SHIPPING CONSIDERATIONS

1. Tag the two boards with a red defective parts tag.

2. Thoroughly describe all fault symptoms on the red tag or attach the description to it.

3. Carefully pack the two circuit boards so that no damage can result during transit.

4. Conform to packaging procedure, CDC 13-004.

TABLE 6-1. RIBBON CABLES CONNECTOR PINS

J1		J2				J3			
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	Spare	1	GND	26	DFM8M	1	GND	26	MAC4
2	Spare	2	DFM4	27	GND	2	POFX	27	FDC1
3	Spare	3	GND	28	FDCL	3	GND	28	FDC0
4	Spare	4	DFM0	29	GND	4	$\overline{\text{T35}}$	29	TCCF
5	Spare	5	GND	30	T90	5	GND	30	STATUS
6	Spare	6	DFM1	31	GND	6	T40	31	FRO6
7	Spare	7	GND	32	T70	7	GND	32	FDC2
8	Spare	8	DFM5	33	GND	8	$\overline{\text{T45}}$	33	FDC3
9	Spare	9	GND	34	$\overline{\text{T0}}$	9	GND	34	$\overline{\text{SENDI}}$
10	Spare	10	DFM2	35	GND	10	SENDF	35	SPARE
11	Spare	11	GND	36	$\overline{\text{T70}}$	11	FRO2	36	FRO8
12	Spare	12	DFM3	37	GND	12	FRO7	37	AREADY
13	Spare	13	GND	38	$\overline{\text{T75}}$	13	FDC6	38	$\overline{\text{FRCLEAR}}$
14	Spare	14	TDCL	39	GND	14	FDC8	39	FDC10
15	Spare	15	GND	40	$\overline{\text{SENDE}}$	15	FDC7	40	CSEL
16	Spare	16	DFM10	41	GND	16	FR10	41	FDC9
17	Spare	17	GND	42	T80	17	FDC4	42	FDC11
18	Spare	18	DFM6	43	GND	18	FDC5	43	$\overline{\text{PPREAD}}$
19	Spare	19	GND	44	T0	19	MAC9	44	MAC0
20	Spare	20	DFM11	45	GND	20	MAC8	45	MAC1
		21	GND	46	$\overline{\text{MACL}}$	21	FRO9	46	MAC2
		22	DFM9	47	GND	22	MACI	47	MAC3
		23	GND	48	POAX	23	MAC7	48	FRO1
		24	DFM7	49	GND	24	MAC6	49	FR00
		25	GND	50	POEX	25	MAC5	50	$\overline{\text{PPWRITE}}$

TABLE 6-2. PIN ASSIGNMENTS FOR SYNCHRONIZER

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1		201		27	GND	227	GND
2		202		28	PB09I	228	PB10I
3	+5V	203	+5V	29	PB11I	229	PBAI
4	+5V	204	+5V	30	GND	230	GND
5		205	PB00O	31	PBII	231	PBFI
6	GND	206	GND	32	PBEI	232	PBPI
7	PB01O	207	PB02O	33	GND	233	GND
8	PB03O	208	PB04O	34	CLK01O	234	CLK10O
9	GND	209	GND	35		235	
10	PB05O	210	PB06O	36		236	
11	PB07O	211	PB08O	37		237	
12	GND	212	GND	38		238	
13	PB09O	213	PB10O	39		239	
14	PB11O	214	PBAO	40		240	
15	GND	215	GND	41		241	
16	PBIO	216	PBFO	42		242	
17	PBEO	217	PBPO	43		243	
18	GND	218	GND	44		244	
19	CLK01I	219	CLK10I	45		245	
20		220	PB00I	46		246	
21	GND	221	GND	47		247	
22	PB01I	222	PB02I	48		248	
23	PO03I	223	PB04I	49		249	
24	GND	224	GND	50		250	
25	PB05I	225	PB06I	51		251	
26	PB07I	226	PB08I				

TABLE 6-2. PIN ASSIGNMENTS FOR SYNCRHONIZER (contd)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
52		252		78	PO11I	278	POAI
53		253		79	GND	279	GND
54		254		80	POII	280	POFI
55		255		81	POEI	281	POPI
56		256		82	GND	282	GND
57		257		83	POMCI	283	POFNI
58		258		84		284	PO00O
59		259		85	GND	285	GND
60		260		86	PO01O	286	PO02O
61		261		87	PO03O	287	PO04O
62		262		88	GND	288	GND
63		263		89	PO05O	289	PO06O
64		264		90	PO07O	290	PO08O
65		265		91	GND	291	GND
66		266		92	PO09O	292	PO10O
67		267		93	PO11O	293	POAO
68		268		94	GND	294	GND
69		269	PO00I	95	POIO	295	POFO
70	GND	270	GND	96	POEO	296	POPO
71	PO01I	271	PO02I	97	GND	297	GND
72	PO03I	272	PO04I	98	POMCO	298	POFNO
73	GND	273	GND	99		299	
74	PO05I	274	PO06I	100		300	
75	PO07I	275	PO08I	101	GND	301	GND
76	GND	276	GND	102	GND	302	GND
77	PO09I	277	PO10I				

TABLE 6-3. PIN ASSIGNMENTS FOR INTERFACE

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	+5V	201	+5V	27		227	
2	+5V	202	+5V	28		228	$\overline{\text{SD10}}$
3		203	$\overline{\text{SD01}}$	29		229	$\overline{\text{RD10}}$
4		204	$\overline{\text{RD01}}$	30		230	$\overline{\text{SD11}}$
5		205	$\overline{\text{SD02}}$	31		231	$\overline{\text{RD11}}$
6		206	$\overline{\text{RD02}}$	32		232	
7		207	$\overline{\text{SD03}}$	33		233	$\overline{\text{SD12}}$
8		208	$\overline{\text{RD03}}$	34		234	$\overline{\text{RD12}}$
9		209	$\overline{\text{SD04}}$	35		235	
10		210	$\overline{\text{RD04}}$	36		236	$\overline{\text{RD13}}$
11		211	$\overline{\text{SD05}}$	37		237	
12		212	$\overline{\text{Y04}}$	38		238	
13		213		39		239	$\overline{\text{RD14}}$
14		214	$\overline{\text{RD05}}$	40		240	$\overline{\text{SD15}}$
15		215	$\overline{\text{SD06}}$	41		241	$\overline{\text{RD15}}$
16		216	$\overline{\text{REPLY}}$	42		242	
17		217	$\overline{\text{Y05}}$	43		243	
18		218	$\overline{\text{RD06}}$	44		244	$\overline{\text{RD16}}$
19		219	$\overline{\text{SD07}}$	45		245	$\overline{\text{Y3}}$
20		220	$\overline{\text{REJECT}}$	46		246	$\overline{\text{Y2}}$
21		221	$\overline{\text{RD07}}$	47		247	$\overline{\text{Y1}}$
22		222	$\overline{\text{Y06}}$	48		248	$\overline{\text{READ}}$
23		223	$\overline{\text{SD08}}$	49		249	
24		224	$\overline{\text{RD08}}$	50		250	
25		225	$\overline{\text{SD09}}$	51		251	
26		226	$\overline{\text{RD09}}$				

TABLE 6-3. PIN ASSIGNMENTS FOR INTERFACE (contd)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
52		252		78		278	
53		253		79		279	
54		254		80		280	$\overline{Y0}$
55		255		81		281	$\overline{Y07}$
56		256		82		282	$\overline{Y08}$
57		257		83		283	$\overline{Y09}$
58		258		84		284	$\overline{Y10}$
59		259		85		285	$\overline{Y11}$
60		260		86		286	$\overline{Y12}$
61		261		87		287	$\overline{Y13}$
62		262		88		288	$\overline{Y14}$
63		263		89		289	$\overline{Y15}$
64		264		90		290	$\overline{WRITE}$
65		265		91		291	
66		266		92		292	
67		267		93		293	
68		268		94		294	
69		269		95		295	
70		270		96		296	
71		271		97		297	
72		272		98		298	
73		273		99		299	
74		274		100		300	
75		275		101	GND	301	GND
76		276		102	GND	302	GND
77		277					

This section contains the assembly drawings and parts lists for the Emulation Coupler and Cable Set.

DWN	T. PARNAKIAN	2-78	CONTROL DATA	TITLE	TOP ASSEMBLY 667X COUPLER	PREFIX	DOCUMENT NO. 74873722	REV A
CHKD							
ENG	J. HURST	4-13-77	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG				FIRST USED ON			SHEET 1 OF 1
APPR			CODE IDENT 34015	DY159-A	35398-111-504		

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
03	06612	INITIAL RELEASE	PL	4-18-77	
A	08063	CL. A RELEASE CBM	TP	2-2-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA

AA6030

NOTES:

PL 74873722
DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74873722	A	CLA	A	667X COUPLER	DW	2551	02/04/78	02/04/78	1/ 1

MF

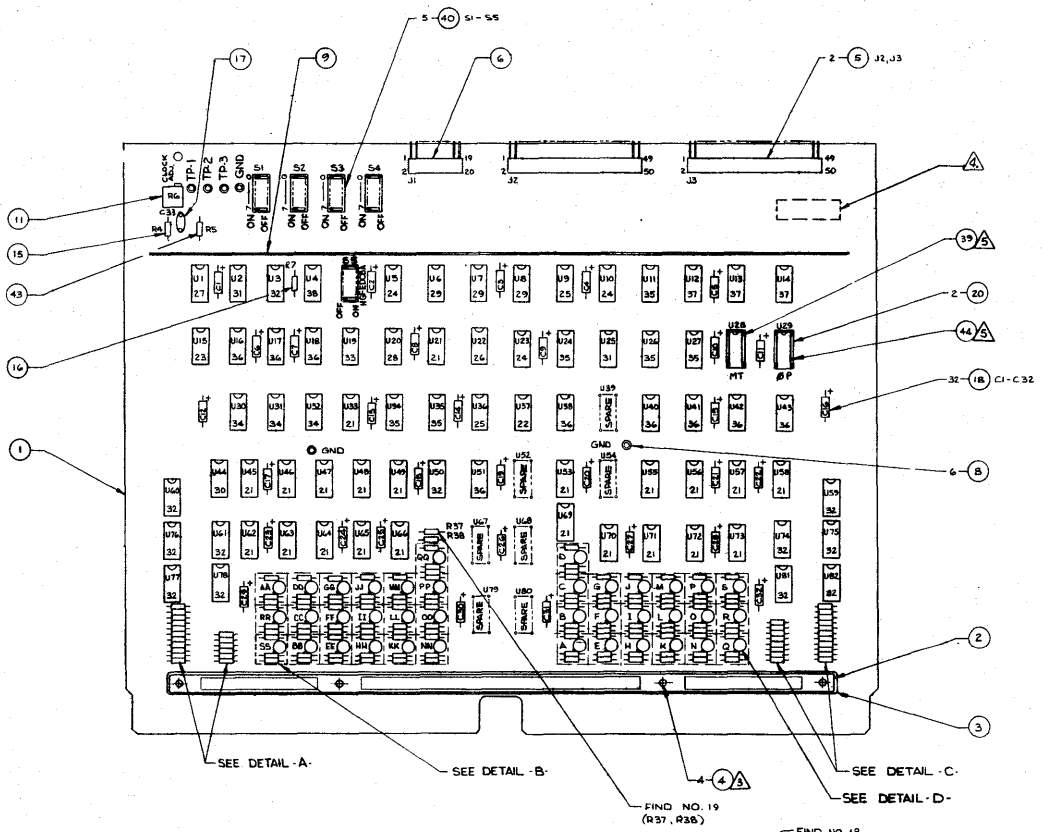
FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
3	C	74843700	2	PC	CBL ASSY FLAT 50 CONDUCTOR	IN					N
4	C	74845800	1	PC	CBL ASSY FLAT 20 CONDUCTOR	IN					N
5	A	74870828	1	PC	DAISY CHAINED 667X EMULATION	IN					N
2	D	74872963	1	PC	COUPLER 667X EMULTR 2550 INTRF	IN					N
1	D	74873040	1	PC	667X CHANNEL SYNCH	IN					N
6	A	88964500	1	PC	JUMPER INTERNAL 5V CYBER COUPL	IN			AYM4		N

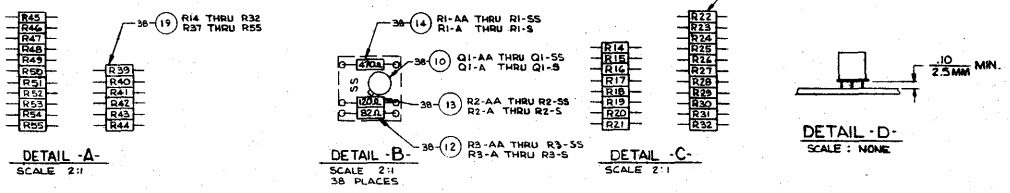
NUMBER OF LINE ITEMS = 6
HIGHEST FIND NUMBER = 6

PROJECT ENGINEER ARDEN HILLS

AA 2709 REV. 7-78

SHEET REVISION STATUS							REVISION RECORD						
						2	1	REV.	ECO	DESCRIPTION	ORIG.	DATE	CHK	APPD
						-	00	00	——	PRELIMINARY RELEASE	JTP	10-17-73		
						-	01	01	——	ADDED DETAIL - E	JTP	11-6-73		
						-	02	02	06001	INITIAL RELEASE	JTP	1-27-74	JN	JW
						-	03	03	06208	SEE ECO	JTP	2-24-74	JF	WF
						-	04	04	06628	INITIAL RELEASE	PL	6-18-74	JN	JW
						A	A	A	08063	CLASS 'A' RELEASE	TP	1-17-78	WF	WD
						A	B	B	08210	REVISE PARTS LIST	TP	6-20-78	VR	VR
						A	C	C	08454	ADD NOTE # 4	CT	10-3-78	JF	JA





NOTES:

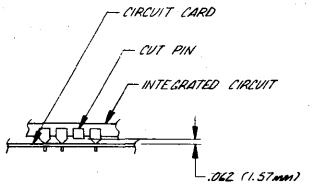
1. WORKMANSHIP PER CDC MFG SPEC 10120300
2. NUMBERS INSIDE IC OUTLINES ARE ITEM FIND NUMBERS.
3. INSERT RIVETS FROM NON-COMPONENT SIDE OF CIRCUIT CARD.
4. STAMP PART NO. 74873040 AND TYPE CODE 5AAY PER CDC SPEC 10121508. LOCATE APPROX. AS SHOWN.
5. U28 & U29 UNPROGRAMMED ROMS ARE IM5610 ICS (RTN 27206-002) FOR PROGRAMMING INSTRUCTION SEE FUNCTIONAL ELEMENT SPEC 33101-042-351. PROGRAMMED ROMS LABELED (RTN 33102-002) ARE TO BE INSERTED INTO SOCKET U29, INSERT ROMS LABELED (RTN 33103-002) INTO SOCKET U28.
6. TO PRE PARE SWITCHES FOR INSTALLATION FIRST REMOVE NUMBERS 1 THRU 8 ON SWITCHES (5 PLACES). INSTALL SWITCHES WITH 'ON' DESIGNATION OF SWITCH TOWARDS NUMBERING OR LETTERING ETCHED ON CIRCUIT CARD.
7. WHEN USING FAB 33402.01 / 74850201 REWORK PER INSTRUCTIONS ON SHEET 2 OF 2.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
C4
A4A030

5AAY

DETACHED LISTS	UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES/MILLIMETERS TOLERANCES: 3 PLACE ± .005 / ± .13; 2 PLACE ± .02 / ± .5; ANGLES ± 2°	CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Sunnyvale, Calif. 94086	TITLE: CKT CARD ASSEMBLY, 667X CHANNEL SYNCHPONIZER	
	DO NOT SCALE DRAWING	FIRST USED ON: DY159-A			
	MATERIAL	DR: PARNAKIAN 6-13-75			
		CHK: W STALLER 8-27-75			
	FINISH	ENGR: KELSTENSEN 8-27-75		D 34015	74873040
		MFG		SCALE 1/1	SHEET 1 OF 2
		APPD			

REV					
		SEE SHEET 1			



CUT PIN DIAGRAM (TYP)
SCALE: NONE

CUT THE FOLLOWING PINS:

I.C.	PINS
U34	8,10

ADD THE FOLLOWING JUMPERS USING FIND NO. 45:

ITEM	FROM	PIN	TO	PIN
1	U36	8 (VM)	U36	1
2	U36	2	U37	2
3	U23	1	U9	13
4	U23	2	U36	10 (VM)
5	U36	3	U36	8 (VM)

CONTROL DATA COMMUNICATIONS PRODUCTS DIV Santa Ana, Calif. 92704	TITLE: CIRCUIT CARD ASSEMBLY - 667X CHANNEL SYNCHRONIZER	SIZE	CAGE NO. 34015	D	DRAWING NUMBER 14879040 A
		SCALE: NONE	SHEET 2 OF 2		

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74873040	C	CLA	D	667X CHANNEL SYNCH	DM	2551	02/04/78	10/04/78	1/ 2

MF
15003-009

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
24	A	15109200	300	PC	IC HEX INVERTER TYPE 74S04	OUT	00A210	062078	PPP5		N
31	A	15109400	200	PC	IC DUAL J-K EDGE TR FF 74S112	OUT	00A210	062078	PPP5		N
30	A	15109700	100	PC	I.C. DUAL D-TYPE EDGE TRIG F.F	OUT	00A210	062078	PPP5		N
27	A	15110100	100	PC	INT CKT 7413	IN			PPP4		N
32	A	15115800	1200	PC	DRIVER, QUAD 2-INPUT NOR LINE	IN			PPP5		N
34	A	15117400	300	PC	I-C TTL AMUX 2-1	IN			PPP5		N
22	A	15125300	100	PC	MICROCIRCUIT	IN			PPP5		N
23	A	15128800	100	PC	INTEGRATED CIRCUIT	IN			PPP4		N
36	A	15132000	900	PC	I.C. 74S175	IN			PPP5		N
35	A	15138800	600	PC	IC 74S174J	IN			PPP4		N
33	A	15142500	100	PC	1-C DECODER 74S138	IN			PPP4		N
37	A	15150400	300	PC	MICROCIRCUIT TYPE 99S16 4 BIT	IN			PPP4		N
25	A	15150900	200	PC	I.C. 74S08	OUT	00A210	062078	PPP4		N
31	A	15158600	200	PC	I C 74S112	IN	00A210	062078	PPP4		N
29	A	15161400	300	PC	I.C. 74S40	IN	00A210	062078	PPP4		N
25	A	15163600	200	PC	IC 74S08	IN	00A210	062078	PPP4		N
19	C	24500023	3800	PC	RES FXD .25W 22 OHMS	IN			PPP5		N
12	C	24500037	3800	PC	RES FXD .25W 82 OHMS	IN			PPP5		N
16	C	24500039	100	PC	RES FXD .25W 100 OHMS	IN			PPP5		N
13	C	24500041	3800	PC	RES FXD .25W 120 OHMS	IN			PPP5		N
15	C	24500050	100	PC	RES FXD .25W 300 OHMS	IN			PPP4		N
14	C	24500055	3800	PC	RES FXD .25W 470 OHMS	IN			PPP5		N
43	C	24500065	100	PC	RES FXD .25W 1200 OHMS	IN			PPP5		N
18	C	24505229	3200	PC	CAP,FXD SOL TA 35V 1.0UF 10PCT	IN			PPP4		N
45	C	24548306	1800	IN	WIRE,ELECT,24 GA,PVC,UL,GRN	IN			PPP5		N
10	C	24561900	3800	PC	TRANSISTOR SILICON NPN,PLANAR	IN			PPP5		N
8	A	38807901	600	PC	TERMINAL HOLLOW SNGL E END,105	IN			PPP3		N
40	A	39996406	500	PC	SWITCH,ROCKER-DUAL,SPST 9POSNS	IN			PPP4		N
21	A	50254600	2200	PC	TTL QUAD 2 INPUT NAND 74S00	OUT	00A210	062078	PPP5		N
26	A	50254700	100	PC	INTEGRATED CIRCUIT 74S10	OUT	00A210	062078	PPP4		N
29	A	50254800	300	PC	IC DUAL-4 INPUT POS-NAND	OUT	00A210	062078	PPP4		N
28		50254900	100	PC	I.C. DUAL 4-IN NAND (74S20)	OUT	00A210	062078	PPP4		N
1	D	74850201	100	PC	667X EMULATOR SYNCH FAB	IN			PYP4		N
41	A	74862000	RFF	PC	667X EMULATOR COUPLER ADDRESS	IN			RFF4		N
44	A	74862001	100	PC	PROGRAMED PROM OPROM OPERATI	IN			PPP4		N
39	A	74862002	100	PC	PROGRAMED PROM MTROM MAINTEN	IN			PPP4		N

PROJECT ENGINEER ARDEN HILI S

AA 2709 REV. 7-78

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74873040	C	CLA	D	667X CHANNEL SYNCH	DM	2551	02/04/78	10/04/78	2/ 2

MF

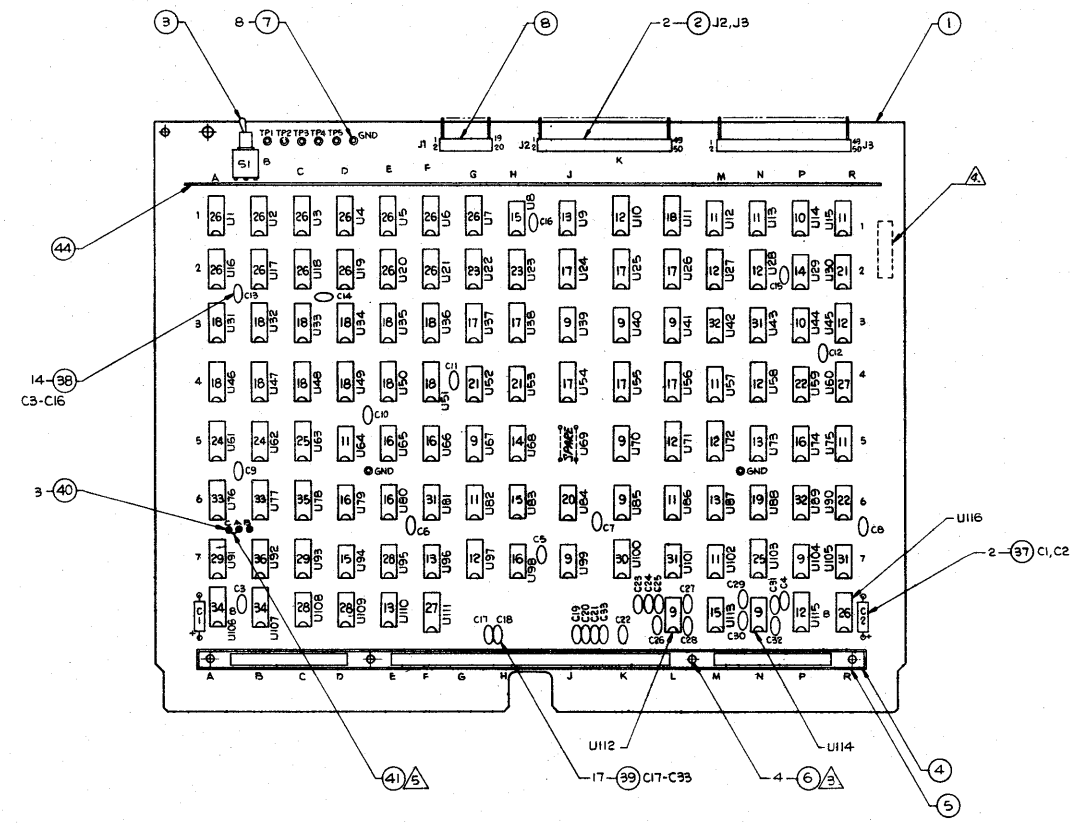
FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
42	D	74873041	RFF	PC	667X EMULATOR SYNCH LOGIC	IN			RFF4		N
11	A	84605207	100	PC	POT, TRIM, CER, 2K OHMS	IN			PPP4		N
17	A	84996709	100	PC	CAP,CER 100V 56 PF	IN			PPP4		N
4	A	88812400	400	PC	RIVET-SEMI-TUBULAR,BRS .312 LG	IN			PPP3		N
9	D	88875500	100	PC	BUS BAR (13 IN)	IN			PPP5		N
24	A	88883700	300	PC	IC 74S04 SCHOTTKY TTL HEX INV	IN	00A210	062078	PPP5		N
26	A	88884200	100	PC	IC 74S10 SCHOTTKY TTL 3-I NAND	IN	00A210	062078	PPP5		N
21	A	88884500	2200	PC	IC 74S00 SCHOTTKY TTL QUAD 2-I	IN	00A210	062078	PPP5		N
28	A	88885300	100	PC	IC 74S20 SCHOTTKY TTL DUAL 4-I	IN	00A210	062078	PPP5		N
2	D	88895400	100	PC	STIFFENER-PC BOARD (CASTING)	IN			PPP5		N
3	C	88895500	100	PC	INSULATOR-CARD STIFFENER	IN			PPP5		N
30	A	88923000	100	PC	IC 74S74 TTL DUAL D EDGE F/F	IN	00A210	062078	PPP5		N
20	C	94260301	200	PC	SOCKET I.C.	IN			PPP4		N
38	A	94262302	100	PC	DELAYLINE TAPPED	IN			PPP4		N
5		94369803	200	PC	HEADER RT ANGL 50 POS	IN			PPP4		N
6		94369805	100	PC	HEADER RT ANGL 20 POS	IN			PPP4		N

NUMBER OF LINE ITEMS = 52
HIGHEST FIND NUMBER = 45

PROJECT ENGINEER ARDEN HILI S

AA 2709 REV. 7-78

SHEET REVISION STATUS			REVISION HISTORY				
Z	/	REV	ECO	DESCRIPTION	BY	DATE	APPD
-	-	00	—	PRELIMINARY RELEASE	WJM	10-14-75	
-	-	01	06001	INITIAL RELEASE	TP	12-16-75	
-	-	02	06269	SEE ECO	TP	5-17-76	
03	03	03	06568	REVISED PER ECO	PL	10-18-76	
04	04	04	06612	INITIAL RELEASE	PL	11-16-77	
A	A	A	08063	CLASS A RELEASE	TP	1-22-79	
A	B	B	08210	REVISED PARTS LIST	TP	6-20-78	
A	C	C	08411	REVISED PL	CT	9-25-78	
A	D	D	08454	ADDED NOTE #6	CT	10-3-78	



NOTES:

1. WORKMANSHIP PER CDC MFG SPEC 10120300
2. NUMBERS INSIDE I.C. OUTLINES ARE ITEM FIND NOS.
3. INSERT RIVETS FROM NON-COMPONENT SIDE OF CIRCUIT CARD
4. STAMP PART NO. 74872963 AND TYPE CODE 5AAY PER CDC SPEC 10121508. LOCATE APPROX AS SHOWN.
5. WIRE 'A' TO 'C' AS SHOWN USING FIND NO. 41
6. WHEN USING FAB 74846201 / 33392-02 CHANGE PER REWORK INSTRUCTIONS ON SHEET 2 OF 2.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STB 1.01.024.
CA
AALD30

5AAY

PL 74872963
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIM ARE IN INCHES MILLIMETERS TOLERANCES
3 PLACE .XXX ±.010mm | 2 PLACE .XX ±.03 ±.08mm | ANGLES ±°
DO NOT SCALE DRAWING
MATERIAL
FINISH

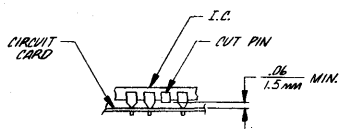
CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	
LATEST USE ON	DY 153-A	
DR	R. McGEE	10-14-75
CHK		10-21-75
ENGR		10-29-75
MFG		
APPD		

TITLE: CIRCUIT CARD ASSY, COUPLER-667X EMUL, 2550 INTERFACE

CODE IDENT NO.	DRAWING NUMBER
D 34015	74872963

SCALE 1/1 | 3-76 F-009-104 | SHEET 1 OF 2

REVISION HISTORY						
REV	ECO	DESCRIPTION	DATE	CHK	APPD	
		SEE SHEET 1				



CUT PIN
SCALE: NONE

1. CLIP THE FOLLOWING PINS FROM I.C.'S NOTED:

I.C. LOC	PIN NOS.
5N	8
2N	3

2. ADD THE FOLLOWING JUMPERS:

ITEM	FROM	PIN	TO	PIN	WIRE GAGE
1	5N	8	4N	6	45
2	1P	3	2N	11	45
3	1P	4	3P	13	45
4	1P	4	1P	5	45
5	1P	6	2P	12	45
6	1P	1	LM	10	45
7	1P	2	2N	9	45
8	1P	13	2N	6	45
9	1P	12	2P	13	45
10	2P	11	2N	3(PIN)	45

CONTROL DATA COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	TITLE CIRCUIT CARD ASSEMBLY - COUPLER-6671X EMUL, 2550 INTERFACE	CODE IDENT NO 34015	D	DRAWING NUMBER 74872963 A
		34015 177-114		SHEET 2 OF 2

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74872963	D	CLA	D	COUPLER 667X EMULTR 2550 INTRF	DM	2551	02/06/78	10/09/78	1/ 2

MF
24968.009

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
25	A	15104000	200	PC	4X4 REGISTER FILE,16PIN	IN			PPP4		N
22	C	15106800	200	PC	IC GATE	IN			PPP4		N
9	A	15109200	1100	PC	IC HEX INVERTER TYPE 74S04	OUT	008210	062078	PPP5		N
12	A	15109400	900	PC	IC DUAL J-K EDGE TR FF 74S112	OUT	008210	062078	PPP5		N
26	A	15114900	1400	PC	IC TTL 1024 BIT RAM 93415	IN			PPP5		N
10	A	15116400	200	PC	IC GATE TPL 3 INP POS-AND	IN			PPP5		N
30	A	15117200	100	PC	1-C TTL DCRD2	IN			PPP4		N
17	A	15117400	600	PC	I-C TTL 8MUX 2-1	IN			PPP5		N
27	A	15117500	200	PC	INTEGRATED CIRCUIT	IN			PPP4		N
20	A	15125100	100	PC	1-C TTL2 5I-1A NOR 2265 D1C14	IN			PPP5		N
13	A	15125300	500	PC	MICROCIRCUIT	IN			PPP5		N
15	A	15125400	400	PC	I.C. 74S30	IN			PPP5		N
18	A	15132100	1300	PC	IC TTL RAM 256 BIT 82S06	IN	008411	092678			N
29	A	15138800	200	PC	IC 74S174J	IN			PPP4		N
33	A	15140400	200	PC	IC 8097, 939 TTL TRI-ST HEX	IN			PPP5		N
31	A	15150900	400	PC	I.C. 74S08	OUT	008210	062078	PPP4		N
28	A	15151100	300	PC	I.C. 74S38	IN			PPP5		N
23	A	15151800	200	PC	IC 745135	IN			PPP4		N
24	A	15154500	200	PC	74368/8098 HEX BUS DRIVERS	IN			PPP4		N
14	A	15154800	200	PC	IC 74S32	IN			PPP4		N
12	A	15158600	900	PC	I C 74S112	IN	008210	062078	PPP4		N
21	A	15160000	300	PC	IC-74393 DUAL 4 BIT BIN COUNTR	IN			PPP5		N
34		15160100	200	PC	I.C. 8234 TYPE	IN			PPP4		N
19	A	15161400	100	PC	I.C. 74S40	IN	008210	062078	PPP4		N
31	A	15163600	400	PC	IC 74S08	IN	008210	062078	PPP4		N
45	C	18563105	300	IN	WIRE ELEC 26 AWG INSULATED	IN			PPP2		N
41	C	24548306	200	IN	WIRE,ELECT,24 GA,PVC,UL,GRN	IN			PPP5		N
40	A	25186108	300	PC	TERMINAL, BIFURCATED L=.115	IN			PPP4		N
7	A	38807901	800	PC	TERMINAL HOLLOW SINGLE END,105	IN			PPP3		N
39	A	38836933	1700	PC	CAP SILVERED MICA 200PF 500V	IN			PPP4		N
11	A	50254600	900	PC	TTL QUAD 2 INPUT NAND 74S00	OUT	008210	062078	PPP5		N
16	A	50254700	600	PC	INTEGRATED CIRCUIT 74S10	OUT	008210	062078	PPP4		N
19	A	50254800	100	PC	IC DUAL-4 INPUT POS-NAND	OUT	008210	062078	PPP4		N
32		50254900	200	PC	I.C. DUAL 4-IN NAND (74S20)	OUT	008210	062078	PPP4		N
36	A	62012906	100	PC	RES MOD DUALI 1K OHMS 125MW	IN			PPP4		N
35	A	62012907	100	PC	RES MOD DUALI 2K OHMS 125MW	IN			PPP4		N

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74872963	D	CLA	D	COUPLER 667X EMULTR 2550 INTRF	DM	2551	02/06/78	10/09/78	2/ 2

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
37	A	72003528	200	PC	CAPACITOR 100 UF 10V	IN			PPP4		N
1	D	74846201	100	PC	667X EMULATOR 2550 INTFC FAB	IN			PYP4		N
38	A	74870616	1400	PC	CAPACITOR CER DISC .01UF 25VDC	IN			PPP5		N
43	D	74872964	REF	PC	667X EMULATOR 2550 INTFC LOGIC	IN			RFE4		N
6	A	88812400	400	PC	RIVET-SEMI-TUBULAR,ARS .312 LG	IN			PPP3		N
44	D	88875500	100	PC	BUS BAR (13 IN)	IN			PPP5		N
9	A	88883700	1000	PC	IC 74S04 SCHOTTKY TTL HEX INV	IN	008454	100478	PPP5		N
16	A	88884200	600	PC	IC 74S10 SCHOTTKY TTL 3-I NAND	IN	008210	062078	PPP5		N
11	A	88884500	900	PC	IC 74S00 SCHOTTKY TTL QUAD 2-I	IN	008210	062078	PPP5		N
32	A	88885300	200	PC	IC 74S20 SCHOTTKY TTL DUAL 4-I	IN	008210	062078	PPP5		N
4	D	88895400	100	PC	STIFFENER-PC BOARD (CASTING)	IN			PPP5		N
5	C	88895500	100	PC	INSULATOR-CARD STIFFENER	IN			PPP5		N
3		94263907	100	PC	SWITCH TOGGLE	IN			PPP4		N
2		94369803	200	PC	HEADER RT ANGL 50 POS	IN			PPP4		N
8		94369805	100	PC	HEADER RT ANGL 20 POS	IN			PPP4		N

NUMBER OF LINE ITEMS = 51
HIGHEST FIND NUMBER = 45

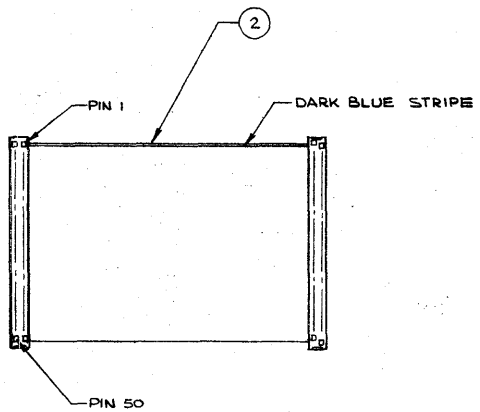
PROJECT ENGINEER

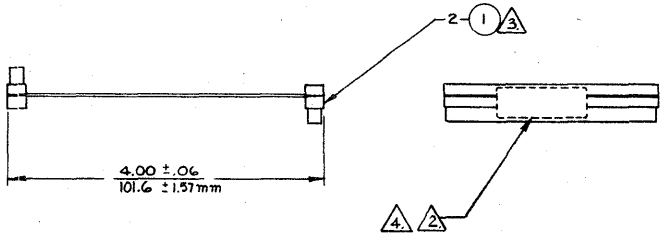
ARDEN HILLS

AA 2709 REV. 7-75

SHEET REVISION STATUS							

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
00	05893	INITIAL RELEASE	JTP	6-24-75		
01	08082	REVISED PL ONLY	TP	11-21-77		
A	08063	CLASS 'A' RELEASE	TP	1-27-78		
B	08502	REVISED NOTE 4	TP	11-7-78		





NOTES:

1. WORKMANSHIP PER CDC MFG SPEC 10120300
2. LOCATE APPROX AS SHOWN
3. ASSEMBLE ITEM 2 TO ITEM 1 USING 3M NO. 3440 PRESS RTN 18844 WITH 3M NO. 3425-0000 RTN 27614 LOCATOR PLATE OR EQUIVALENT TOOLING.
4. MARK PER CDC SPEC 10121508 WITH PART NO. 74843700 AND REVISION.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CB
AA6030

PL 74843700
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES/MILLIMETERS TOLERANCES
3 PLACE ±.015 ±0.38mm | 2 PLACE ±.03 ±0.8mm | ANGLES ±2°
DO NOT SCALE DRAWING
MATERIAL
FINISH

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704

	FIRST USED ON		
DR		PARNAKIAN	6-24-75
CHK		D. Sands	8-25-75
ENGR		D. Sands	8-25-75
MFG			
APPD			

TITLE: CABLE ASSY, FLAT 50-CONDUCTOR

CODE IDENT NO. C 34015 | DRAWING NUMBER 74843700

SCALE 1/1 | 32866-009-070 | SHEET 1 OF 1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74843700	B	CLA	C	CBL ASSY FLAT 50-CONDUCTOR	DM	2551	02/04/78	11/06/78	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
2	C	65832240	600	IN	CABLE	IN			PPP4		N
1	A	65853411	200	PC	CONNECTOR	IN	008502	110678			N

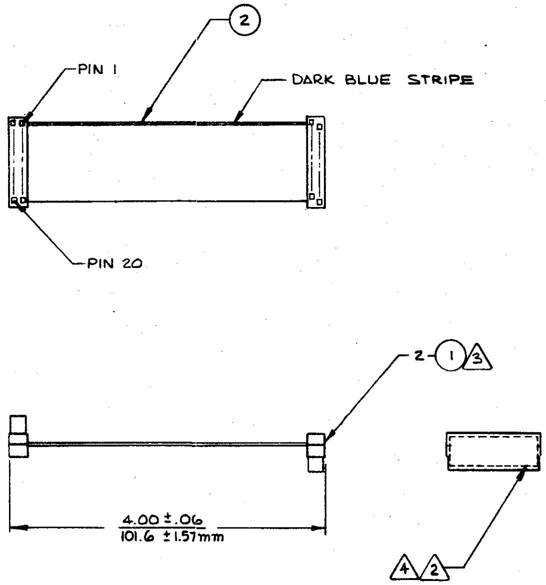
NUMBER OF LINE ITEMS = 2
HIGHEST FIND NUMBER = 2

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-78

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
	00	05893	INITIAL RELEASE	JTP	6-24-75		
	A	08063	CLASS "A" RELEASE	TP	1-27-78		
	B	08502	REVISED NOTE 4	TP	11-7-78		



NOTES:

1. WORKMANSHIP PER CDC MFG SPEC 10120300
2. LOCATE APPROX AS SHOWN
3. ASSEMBLE ITEM 2 TO ITEM 1 USING 3M NO. 3440 PRESS RTN 18844 WITH 3M NO. 3425-0000 RTN 27614 LOCATOR PLATE OR EQUIVALENT TOOLING.
4. MARK PER CDC SPEC 10121508 WITH PART NO. 74845800 AND REVISION.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
C4
AA6030

PL 74845800 | DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES/MILLIMETERS TOLERANCES
3 PLACE ±.015 ±0.38mm | 2 PLACE ±.03 ±0.8mm | ANGLES ±2°

DO NOT SCALE DRAWING

MATERIAL

FINISH

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704

FIRST USED ON		
DR	PARNAKIAN	6-24-75
CHK		8-25-75
ENGR		8-25-75
MFG		
APPD		

TITLE: CABLE ASSY, FLAT 20-CONDUCTOR

SIZE	CODE IDENT NO.	DRAWING NUMBER
C	34015	74845800

SCALE 1/1 | 32915-009-070 | SHEET 1 OF 1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74[illegible]5800	B	CLA	C	CBL ASSY FLAT 20-CONDUCTOR	UM	2551	02/08/78	11/06/78	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
2	C	53532210	500	IN	CABLE	IN			PRP4		N
1	A	53533405	200	PC	CONNECTOR	IN	008502	110678	CAWA		N

NUMBER OF LINE ITEMS = 2
HIGHEST FIND NUMBER = 2

PROJECT ENGINEER

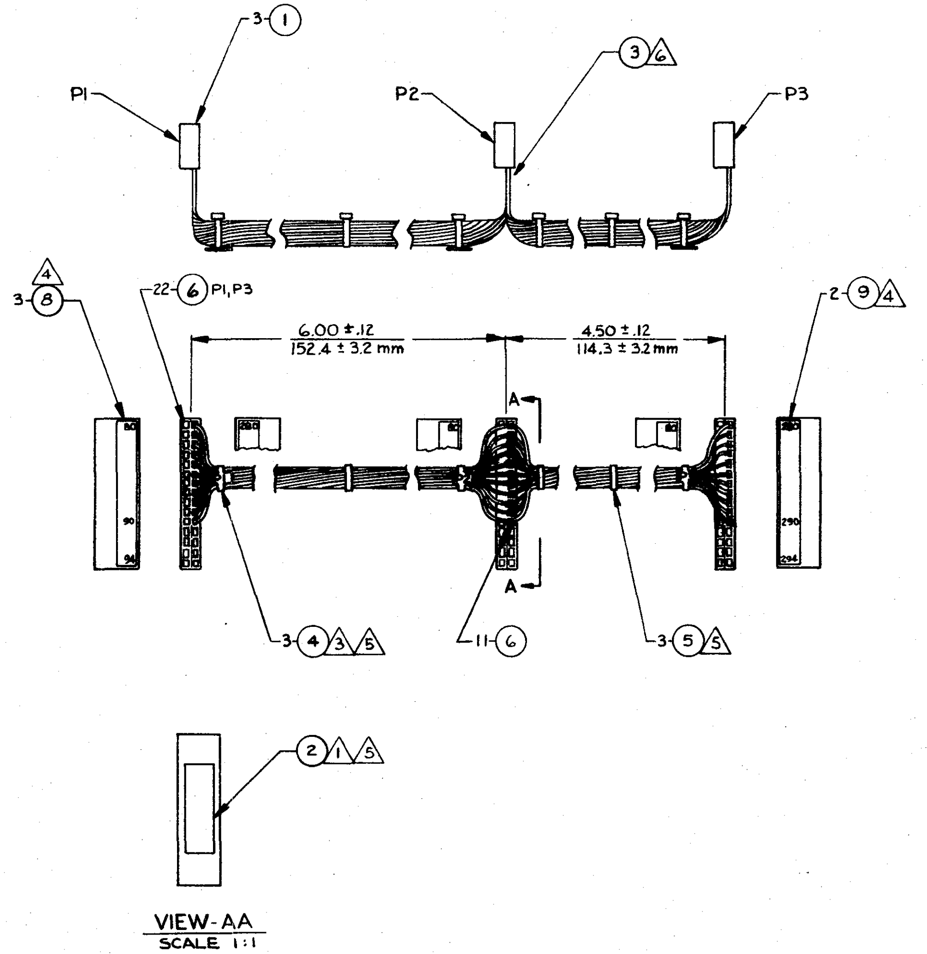
ARDEN HILLS

AA 2700 REV. 7-75

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
01	06001	INITIAL RELEASE	TP	11-4-75	2-9-76	
C	06247	SEE ECO	LA	3-5-76		
D	06331	SEE ECO	LA	4-21-76		
E	08063	CLASS A RELEASE	TP	1-27-78		
F	08454	REV. PL & NOTE #6	CT	9-3-78		



NOTES:

1. MARK PART NO. 74870828 AND SERIAL NUMBER PER CDC SPEC 10121508.
2. WORKMANSHIP PER CDC MFG SPEC 10120300.
3. INK STAMP PER CDC SPEC 10121502. LOCATE APPROX AS SHOWN.
4. TRIM TO FIT CONNECTOR AS SHOWN.
5. LOCATE APPROX AS SHOWN
6. WIRE P2 PINS 280 THRU 290 TO P1 AND P3 PINS 280 THRU 290 AS SHOWN USING FIND NO. 3. NOTE: 24 AWG CRIMPS (FIND NO.6) ARE USED IN CONNECTOR P2 TO HOLD TWO 26AWG WIRES IN EACH PIN POSITION GOING TO P1 AND P3.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA

AA6030

PL 74870828

DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES/MILLIMETERS TOLERANCES
3 PLACE ±.015 ±0.38mm; 2 PLACE ±.03 ±0.8mm; ANGLES ±2°

DO NOT SCALE DRAWING

MATERIAL

FINISH

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704

FIRST USED ON

DR	T. PARNAKIAN	11-3-75
CHK		2-9-76
ENGR		2-9-76
MFG		
APPD		

TITLE: CABLE ASSY, DAISY CHAINED 667X EMULATION (REAR PANEL)

C — CODE IDENT NO. 34015 — DRAWING NUMBER 74870828

SCALE 1/1 — 33750-009-070 — SHEET 1 OF 1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74870828	F	CLA	A	DAISY CHAINED 667X EMULATION	DM	2551	01/25/78	10/04/78	1/ 1

MF
37750-909

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
3	C	18563109	1500	IN	WIRE ELEC 26 AWG INSULATED	IN	00A454	100478	PPP2		N
8	C	74842800	300	PC	LABEL CONTACT CAVITY 52 102	IN			PPP4		N
9	C	74843000	200	PC	LABEL CONTACT CAVITY 252 302	IN			PPP4		N
6	C	94245601	3300	PC	CONTACT-CRIMP INSERT SOCKET	IN	00A454	100478	PPP4		N
4	C	94277407	300	PC	STRAP CABLE TIE	IN			PPP1		N
5	C	94277416	300	PC	STRAP CABLE TIE	IN			PPP1		N
1	C	94360807	300	PC	HOUSING-CONN.SOCKET .125 30CAV	IN			PPP4		N

NUMBER OF LINE ITEMS = 7
HIGHEST FIND NUMBER = 9

PROJECT ENGINEER ARDEN HILLS

AA 2709 REV. 7-75

DWN	MASTELL	3-12-75	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD			COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704	JUMPER, INTERNAL 5V-CYBER COUPLER		88964500	H
ENG							
MFG			CODE IDENT 34015	FIRST USED ON DK106	31395-009-370		SHEET 1 OF 4
APPR							

SHEET REVISION STATUS

2	/
04	04
05	05
G	G
	H

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
04	05549	SEE ECO	DPM	3-19-75	
05	05743	SEE ECO	DPM	5-20-75	
G	06414	SEE ECO	44	6-24-76	
H	08063	CLASS "A" RELEASE	TP	1-27-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA

AA6030

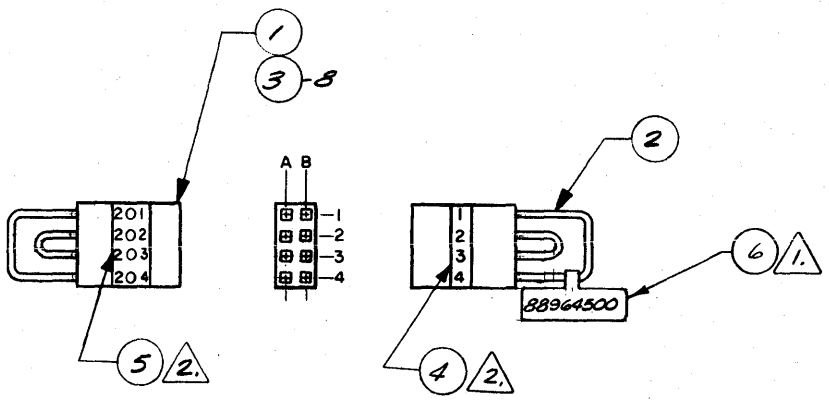
NOTES:

PL 88964500
DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31395-009-370

CONTROL DATA	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 4	DOCUMENT NO. 88964500	REV. G



FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA	SMALL COMPUTER DEVELOPMENT DIVISION La Jolla, Ca 92037	CODE IDENT 09132	SHEET 3 OF 4	WL	DOCUMENT NO. 88964500	REV G

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
1	2	22 AWG	RED	2 IN	A1			A4			
2	↕	↕	↕	↕	A2			A3			
3	↕	↕	↕	↕	B1			B4			
4	2	22AWG	RED	2 IN	B2			B3			

AA0109 REV. 8/71 PRINTED IN U.S.A.

REVISION RECORD						
REV	CO	DESCRIPTION	DRFT	DATE	CHKD	APP
		FOR REVISIONS SEE SH 1				

NOTES: UNLESS OTHERWISE SPECIFIED.

1. MARK PER CDC SPEC 10121508, PART NO. 88964500.
2. TRIM FIND NUMBERS 4 AND 5 TO INDICATED NUMBERS AND AFFIX TO CONNECTOR AS SHOWN.

STAPOS Division controls this document as of JULY 2, 1974

AA4291

DWN	L. V. Poletis	6/27/74
CHKD	T. Cunnan	1-2-74
ENG	[illegible]	6-28-74
MFG		
APP	[illegible]	7-2-74

CONTROL DATA — SMALL COMPUTER DEVELOPMENT DIVISION La Jolla, CA 92037

TITLE: JUMPER, INTERNAL 5V - CYBER COUPLER

CODE IDENT 09132 | A | DWG No 88964500

SCALE NONE | 31395-009-370 | SHEET 4 OF 4

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
88964500	H	CLA	A	JUMPER INTERNAL 5V CYBER COMPL	DM	2551	01/25/78	01/25/78	1/ 1

MF
31395-009

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
2	C	24548303	900	IN	WIRE,ELECT,24 GA,PVC,UL,RED	IN			PPP5		N
3	A	74718400	800	PC	CONTACT	IN			PPP4		N
1	A	74718506	100	PC	CONN HOUSING 8 CAVITY	IN			PPP4		N
4	C	74789300	100	PC	LABEL CONTACT CAVITY	IN			PPP4		N
5	C	74842900	100	PC	LABEL CONTACT CAVITY 201 251	IN			PPP4		N
6	C	94277407	100	PC	STRAP CABLE TIE	IN			PPP1		N

NUMBER OF LINE ITEMS = 6
HIGHEST FIND NUMBER = 6

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

DWN	E. Gamper	8-23-77	CONTROL DATA	TITLE TOP ASSEMBLY - CABLE SET EMULATION COUPLER -	PREFIX	DOCUMENT NO. 74873995	REV B
CHKD		9-1-77					
ENG		8-77	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG							
APPR			CODE IDENT 34015	FIRST USED ON XA226-A	35685-009-070		SHEET 1 OF 1

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	06965	INITIAL REL- CL 'B'	ELG	9-1-77	M
A	08063	CLASS A RELEASE	TED	1-20-78	BP
B	08511	CORRECT PN FIND NO. 1	TD	13 FEB 79	JK

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024,
CA

AA6030

NOTES: FOR INSTALLATION INSTRUCTIONS SEE 74873993 (35685-080-151)

PL 74873995
DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74873995	B	CLA	A	CBL SET EMULATION COUPLER	DM	2551	01/25/78	02/20/79	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN HC	S OR N
2	A	19191600	200	PC	I/O COAXIAL CABLE ASSY	IN					N
1	A	52675000	200	PC	COAXIAL CABLE WITH CONN 5 FT	OUT	008511	021579			N
1	A	52675100	200	PC	COAXIAL CABLE WITH CONNECTOR	IN	008511	021579			N
3	A	88947800	400	PC	CABLE, COAX - 5 FT.	IN			AYM4		N

NUMBER OF LINE ITEMS = 4
HIGHEST FIND NUMBER = 3

PROJECT ENGINEER

SANTA ANA

AA 2709 REV. 7-78

Printed in U.S.A.

GENERAL SUPPLEMENT SHEET

COMPUTER DIVISION

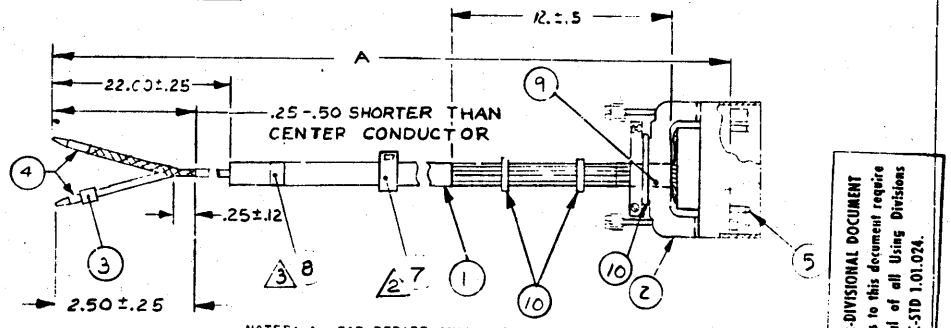
COAXIAL CABLE WITH CONNECTOR

DOCUMENT NO.	REV.
A 52675100	R

SHEET 1 OF

TO MAKE	DIMENSION A
52675000	5 FT. ± 2"
52675001	70 FT. $\pm \frac{4}{2}$
52675002	45 FT. $\pm \frac{6}{2}$
52675003	38 FT $\pm \frac{6}{2}$
52675004	50 FT $\pm \frac{6}{2}$
52675005	7 FT ± 2"

Machine crimp taper pin P/N 24500707 using the standard AMP taper pin machine, adjusted to a wire crimp height of 0.039 ± 0.002 on center conductor and 0.080 ± 0.005 insulation crimp height for insulator on center conductor. Wire crimp height for the shield should be adjusted to 0.045 ± 0.002, with the shield visible in both inspection windows.
NOTE: Strip length for conductor should be 11/64 ± 1/64.



NOTES: 1. FOR REPAIR ONLY, USE TAPER PIN P/N 24500717 AND CRIMP WITH HAND CRIMPER, AMP NUMBER 90115.
2. TYRAPS SHALL BE TIGHTENED WITH A "THOMAS & BETTS" TYRAP GUN WITH A NUMBER 4 TENSION SETTING.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

FORM 58

BY	DATE	CHKD.	DATE	APPD	DATE

ASSY 52675100 | CODE IDENT | SHEET 2 | WL | DOCUMENT NO 52675100 | REV. E

CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION	ACCESS FIND NO	REMARKS
		30	90	5FT	P1	A				
		↑	91	↑	↑	B				
			92			C				
			93			D				
			94			E				
			95			F				
			96			H				
			97			J				
			98			K				
			99			L				
			900			M				
			910			N				
			920			P				
			930			R				
			940			S				
			950			T				
			960			U				
		↓	970	↓	↓	V				
		30	980	5FT	P1	W				

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

AA 3-63

PRINTED IN USA

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

NON-SPARE PARTS

ASSEMBLY NUMBER	REV.	CLASS	CN SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	P.M.T. USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
52675100	S	CLA	A	COAXIAL CABLE WITH CONN 5-FT	CAM	663X	04/11/69	04/12/77	1/ 1

FIND NUMBER	CN SZ	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	I.D. STAT'S	CHANGE NOTICE NUMBER	PART EFFECTIVITY	MAKE OR BUY CODE	PC CC	PC CN
13	A	99031211	100	PC	RIVET POP OPEN-END .187 DIA	IN	037799	05/20/77			
14	A	10125606	100	PC	PLAIN WASHERS	IN	037799	05/20/77	PPP1		
	C	17620300	300	PC	STRAP CABLE ADJUSTABLE	OUT	037799	05/20/77	PPP3		
	C	17620301	200	PC	STRAP CABLE ADJUSTABLE	OUT	037799	05/20/77	PPP3		
11	C	17620303	100	PC	STRAP CABLE ADJUSTABLE	IN	037799	05/20/77	PPP3		
10	C	17620307	100	PC	STRAP CABLE ADJUSTABLE	IN	037799	05/20/77	PPP3		
12	C	17780211	100	PC	CABLE LOOP END	IN	037799	05/20/77	PPP4		
6	C	17944062	100	PC	LABEL,CABLE LENGTH MARKING	IN	027468	05/05/71	PPP1		
2	C	18752802	100	PC	CONN BODY,HOOD ASSY,25 POS	IN	026130	05/05/71	PPP4		
5	C	18752811	1900	PC	SINGLE PIECE CONTACT - COAX	IN	029902	12/20/71	PPP4		
7	C	18874300	100	PC	MARKER,IDENT-CABLE STRAP	IN	027468	05/05/71	PPP1		
4	C	24500707	3800	PC	PIN TAPER	IN	029902	12/20/71	PPP5		
3	C	24500802	1900	PC	INSULATION SLEEVING ELECT	IN	033767	05/24/77	PPP3		
1	C	24567000	500	FT	CABLE,COAXIAL, 19-CONDUCTOR	IN	029982	12/20/71	PPP5		

NUMBER OF LINE ITEMS = 14
HIGHEST FIND NUMBER = 14

BILL STORM ARDEN HILLS

DWN			TITLE	PREFIX	DOCUMENT NO	REV
CHKD			I/O COAXIAL CABLE ASSY	WL	19191600	B
ENG		CANADIAN DEVELOPMENT				
MFG			FIRST USED ON		SHEET 1 OF 3
APPD		CODE IDENT 34570	AA107A		

SHEET REVISION STATUS

1	2	3
1	2	2
3	3	3
4	4	02
A	A	A
B	B	A

REVISION RECORD

REV	ECC	DESCRIPTION	DRFT	DATE	APP
		CLASS B DWG			
		ADDED SOLDER			
		TAE 01 ADDED			
4	PDM00669	REVISED PER ECO	JN	24AUG74	
A	00760	CLASS A DWG	EMG	29OCT74	
B	01603	TAE 01 INACTIVATED	RW	12-27-76	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
AA6030

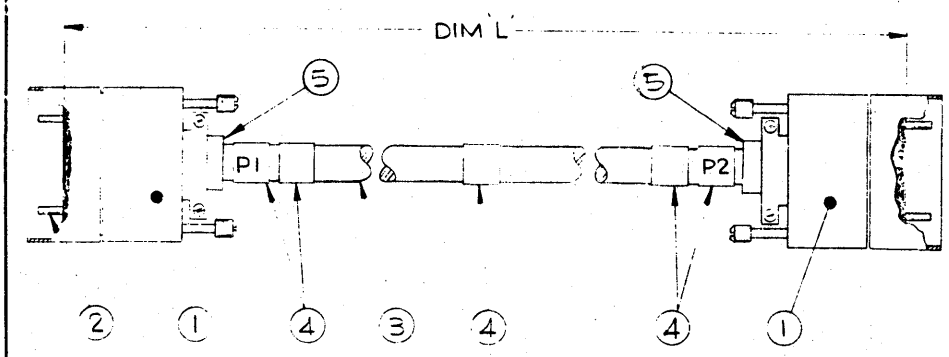
NOTES 1. NO ASSY DWG AVAILABLE.
2. FOR ALL SOLDERING USE 60/40 RESIN CORE SOLDER.

INACTIVE

PL 19 91600

DETACHED LISTS

	I/O COAXIAL CABLE ASSY	CODE IDENT 34570	SHEET 2	WL	19191600	B



CDC PART NUMBER	DIM L	TOLERANCE
19191600	65 FEET	±.5 FT
~~19191601~~	~~3 FEET~~	~~±.2 FT~~ INACTIVE
19191602	33 FEET	+.5 FT −.2 FT

CONTROL DATA	I/O COAXIAL CABLE ASSY	CODE IDENT 34570	SHEET 3	WL	DOCUMENT NO. 19191600	REV. A

CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO.	REMARKS
	3		90		P1	A	2	P2	A	2	
	↑		91		↑	B	↑	↑	B	↑	
			92			C			C		
			93			D			D		
			94			E			E		
			95			F			F		
			96			H			H		
			97			J			J		
			98			K			K		
			99			L			L		
			900			M			M		
			910			N			N		
			920			P			P		
			930			R			R		
			940			S			S		
			950			T			T		
			960			U			U		
	↓		970		↓	V	↓	↓	V	↓	
	3		980		P1	W	2	P2	W	2	

TABULATION		
PART NO.	LENGTH	RTN NO
88947800	5' ± 3"	31394
01	70' ± 6"	31398

REVISION RECORD						
REV	CO	DESCRIPTION	DRFT	DATE	CHKD	APP
E		FOR REVISIONS SEE SHT 8				

4. FIND Nº 21 TO BE MARKED PER CDC STD 1.030.008
3. TRIM FIND NUMBER 4 LABEL TO DESIRED LENGTH AND AFFIX TO CONNECTOR HOUSING MAINTAINING CONTACT ORIENTATION.
2. LENGTH OF WIRE INSULATION TO BE 1.75" BETWEEN FERRULE AND CONTACT.
1. FIND Nº 10 TO BE MARKED PER CDC SPEC 1012508 WITH APPLICABLE PART NUMBER, REVISION, DATE CODE AND P1 OR J1 AS APPLICABLE.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA
AA6030

NOTES UNLESS OTHERWISE SPECIFIED

STAOPS Division controls this document as of JULY 2, 1974
AA4291

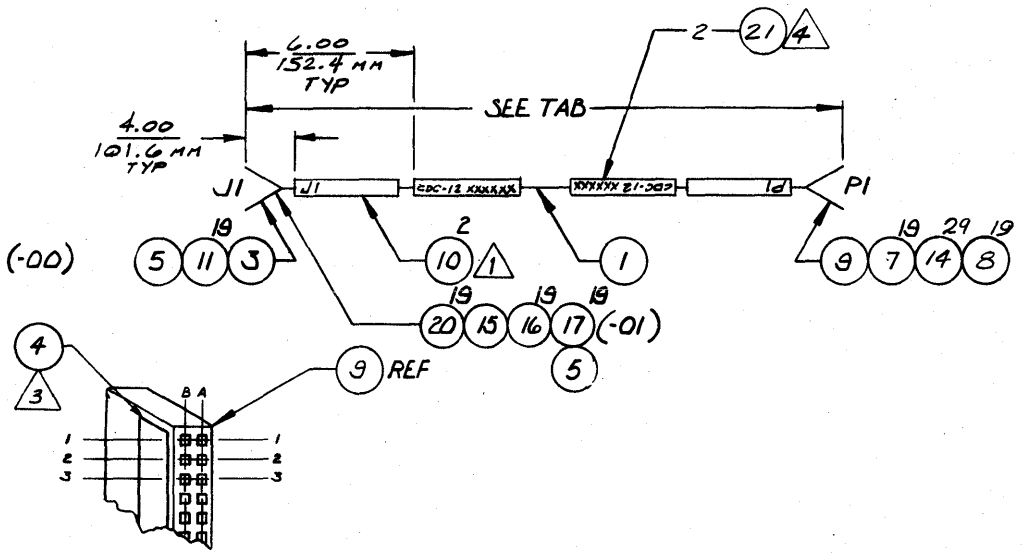
DWN	B Johnson Jr	4/17/4
CHKD		6-27-4
ENG		6-28-4
MFG		
APP		7-8-74

CONTROL DATA
SMALL COMPUTER DEVELOPMENT DIVISION
La Jolla, CA 92037

TITLE: COAX CABLE, 19-COND
CODE IDENT: 09132 | SIZE: A | DWG NO: 88947800/01
SCALE:
SHEET 1 OF 8

31394 - 009-370
31398

CONTROL DATA	SMALL COMPUTER DEVELOPMENT DIVISION La Jolla, Ca 92037	CODE IDENT 09132	SHEET 2		DOCUMENT NO. 88947800	REV. E



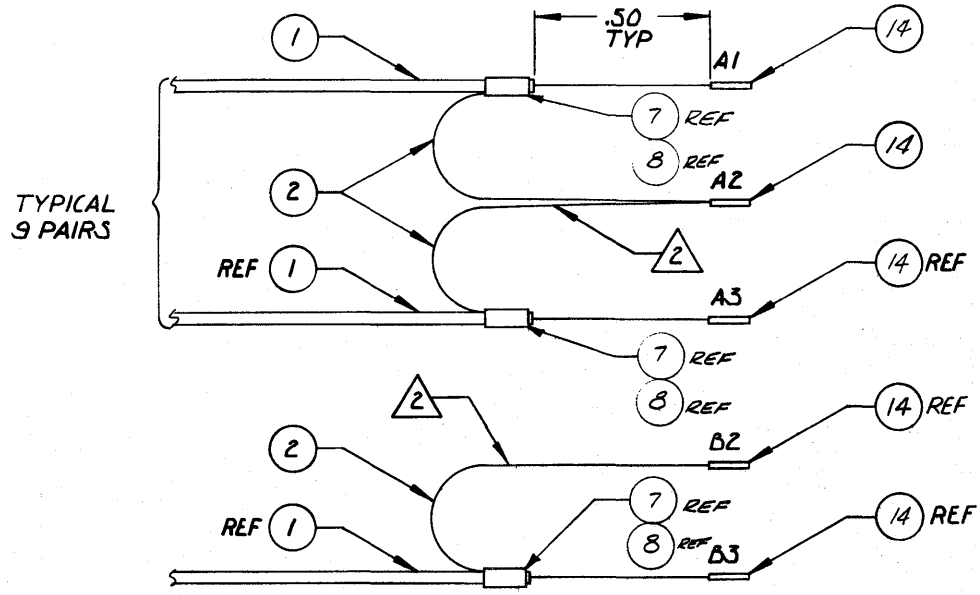
P1 END DETAIL
WIRING END

J1 END DETAIL
HAND TOOL TERMINATION (FOR REF ONLY)
18 (-00)
19 (-01)

AA3185
PRINTED IN U.S.A.

31394-009-370
31398

CONTROL DATA	SMALL COMPUTER DEVELOPMENT DIVISION La Jolla, Ca 92037	CODE IDENT 09132	SHEET 3		DOCUMENT NO. 88947800	REV D



COAX TERMINATION DETAILS FOR F/N 9

AA3185 PRINTED IN U.S.A.

31394-009-370
31398

CONTROL DATA	SMALL COMPUTER DEVELOPMENT DIVISION La Jolla, Ca 92037	CODE IDENT 09132	SHEET 4	WL	DOCUMENT NO. 88947800	REV D

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
1	1	30	90	5FT	J1	A	11	P1	A1	14,7,8	COND } TYP 10 PLCS
2	↑	↑		↑	↑		↑	↑	A2	14,2	SHIELD }
3			91			B			B3	14,7,8	
4									B2	14,2	
5			92			C			A3	14,7,8	
6									A2	14,2	
7			93			D			B4	14,7,8	
8									B5	14,2	
9			94			E			A4	14,7,8	
10									A5	14,2	
11			95			F			B6	14,7,8	
12									B5	14,2	
13			96			H			A6	14,7,8	
14									A5	14,2	
15			97			J			B7	14,7,8	
16									B8	14,2	
17			98			K			A7	14,7,8	
18	↓	↓		↓	↓		↓	↓	A8	14,2	
19	1	30	9	5FT	J1	L	11	P1	B9	14,7,8	
20									B8	14,2	

AA3183 REV. 8/71 PRINTED IN U.S.A.

3/399-009-370
3/398

CONTROL DATA	SMALL COMPUTER DEVELOPMENT DIVISION, La Jolla Ca 92037	CODE IDENT 09132	SHEET 5	WL	DOCUMENT NO 88947800	REV D

CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS
21	1	30	900	5FT	J1	M	11	P1	A9	14,7,8	COND } TYP 9 PLCS
22	↓	↓		↓	↓		↓	↓	A8	14,2	SHIELD }
23			910			N			B10	14,7,8	
24									B11	14,2	
25			920			P			A10	14,7,8	
26									A11	14,2	
27			930			R			B12	14,7,8	
28									B11	14,2	
29			940			S			A12	14,7,8	
30									A11	14,2	
31			950			T			B13	14,7,8	
32									B14	14,2	
33			960			U			A15	14,7,8	
34									A14	14,2	
35			970			V			B15	14,7,8	
36	↓	↓		↓	↓		↓	↓	B14	14,2	
37	1	30	980	5FT	J1	W	11	P1	A13	14,7,8	
38									A14	14,2	
39											
40											

AA3183 REV. 8/71 PRINTED IN U.S.A.

3/390-009-370
3/398

CONTROL DATA	SMALL COMPUTER DEVELOPMENT DIVISION, La Jolla Ca 92037	CODE IDENT 09132	SHEET 6	WL	DOCUMENT NO 88947800	REV D

CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS
41	1	30	90	70FT	J1	A	16,17,20	P1	A1	14,7,8	COND } TYP 10 PLCS
42	↓	↓		↓	↓		↓	↓	A2	14,2	SHIELD }
43			91			B			B3	14,7,8	
44									B2	14,2	
45			92			C			A3	14,7,8	
46									A2	14,2	
47			93			D			B4	14,7,8	
48									B5	14,2	
49			94			E			A4	14,7,8	
50									A5	14,2	
51			95			F			B6	14,7,8	
52									B5	14,2	
53			96			H			A6	14,7,8	
54									A5	14,2	
55			97			J			B7	14,7,8	
56									B8	14,2	
57			98			K			A7	14,7,8	
58	↓	↓		↓	↓		↓	↓	A8	14,2	
59	1	30	9	70FT	J1	L	16,17,20	P1	B9	14,7,8	
60									B8	14,2	

AA3183 REV. 8 71 PRINTED IN U.S.A.

31394-009-370
31398

CONTROL DATA	SMALL COMPUTER DEVELOPMENT DIVISION La Jolla Ca 92037	CODE IDENT 09132	SHEET 7	WL	DOCUMENT NO 88947800	REV D

CONDUCTOR IDENT	FIND NO	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS
61	1	30	900	70FT	J1	M	16,17,20	P1	A9	14,7,8	COND } TYP 9 PLCS
62	↑	↑		↑	↑		↑	↑	A8	14,2	SHIELD } TYP 9 PLCS
63			910			N			B10	14,7,8	
64									B11	14,2	
65			920			P			A10	14,7,8	
66									A11	14,2	
67			930			R			B12	14,7,8	
68									B11	14,2	
69			940			S			A12	14,7,8	
70									A11	14,2	
71			950			T			B13	14,7,8	
72									B14	14,2	
73			960			U			A15	14,7,8	
74									A14	14,2	
75			970			V			B15	14,7,8	
76	↓	↓		↓	↓		↓	↓	B14	14,2	
77	1	30	980	70FT	J1	W	16,17,20	P1	A13	14,7,8	
78									A14	14,2	
79											
80											

AA3183 REV. 8 71 PRINTED IN U.S.A.

31394-009-370
31398

DWN	CHKD	ENG	MFG	APPR	CONTROL DATA LA JOLLA DIVISION La Jolla, Calif. 92037 CODE IDENT 09132	TITLE COAX CABLE, 19 COND	PREFIX	DOCUMENT NO. 88947800/01	REV F
						FIRST USED ON		SHEET 8 OF 8	

SHEET REVISION STATUS

8	7	6	5	4	3	2	1
02	02	02	02	02	02	02	02
03	03	03	03	03	03	03	03
04	03	03	03	03	03	03	03
05	03	03	03	03	03	05	03
06	03	03	03	03	03	05	06
07	03	03	03	03	03	07	07
C	C	C	C	C	C	C	C
D	D	D	D	D	D	D	C
E	D	D	D	D	D	E	E
F	D	D	D	D	D	E	F

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP'D
A		RELEASED CL. A.	RJ/JR	7-8-74	
B	13344	TRNSFRD. TO STAOPS	LVP	7-8-74	
00	-	INITIAL RELEASE - STAOPS			
01	-	DELETE FD NO. 5; MADE P/L DETACHED LIST	LA	12-4-74	
02		CL. B PRERELEASE	LA	12-5-74	
03	05476	SEE E.C.O.	DPM	2-17-75	
04	05742	SEE E.C.O.	DPM	4-18-75	
05	05873	SEE ECO	LA	8-14-75	
06	06074	SEE ECO	LA	11-14-75	
07	06711	CL II CONN. LABEL CHG	DPM	1-11-77	
C	08218	REVISED PL. SEE ECO	TP	4-7-78	
D	8456	REV. PL PART NO	RN	9-28-78	
E	008476	REV. PL F/N 5 & 21	AV	11-78	
F	08614	REV. PL F/N 11	CT	4-16-79	

NOTES:

PL 88947801
PL 88947800
DETACHED LISTS

AA3180 REV. 8/71 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
88947800	F	CLA	A	CABLE, COAX - 5 FT.	DM	CYBR70	06/21/74	04/17/79	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN INC	S OR N
21	A	10123800	200	PC	LABEL, CABLE MARKING	IN	008476	110278	PPP4		N
2	C	18563100	4800	IN	WIRE ELEC 26 AWG INSULATED	IN	008456	092978	PPP4		N
18	C	18752700	REF	PC	CONN COAX KEYED JACKS MULT POS	IN	013303	070874	RFE4		N
3	C	18752702	100	PC	CONN BODY,HOOD ASSY 20 POS	IN			PPP4		N
11	C	18752711	1900	PC	SINGLE PIECE CONTACT - COAX	IN	008614	041679	PPP4		N
5	C	24534714	1000	IN	SLEEVING ELEC SHRINKABLE BULK	IN	008476	110278	PPP4		N
1	C	24567000	500	FT	CABLE,COAXIAL 19 COND.,73OHM	IN			PPP4		N
10		51904701	200	PC	CABLE LABLE	IN	008218	041178	PPP4		N
4	C	74789300	100	PC	LABEL CONTACT CAVITY	IN	008500	110777	PYP4		N
14	C	94245601	2900	PC	CONTACT-CRIMP INSERT SOCKET	IN	008456	092978	PPP4		N
8	A	94278613	1900	PC	FERRULE INSULATOR	IN	008500	110777	PPP4		N
9	C	94360807	100	PC	HOUSING-CONN,SOCKET .125 30CAV	IN			PPP4		N
7	C	94871108	1900	PC	FERRULES GRN UNINSULATED	IN	008218	040778	PPP4		N

NUMBER OF LINE ITEMS = 13
HIGHEST FIND NUMBER = 21

GEORGE BURN — SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
88947801	F	CLA	A	CABLE, COAX - 70 FT.	DM	CYBR70	06/21/74	04/18/79	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN INC	S OR N
21	A	10123800	200	PC	LABEL, CABLE MARKING	IN	008476	110278	PPP4		N
2	C	18563100	4800	IN	WIRE ELEC 26 AWG INSULATED	IN	008456	092978	PPP4		N
19	C	18752800	REF	PC	CONN COAX JACK SCREW MULT POS	IN					N
15	C	18752802	100	PC	CONN BODY,HOOD ASSY,20 POS	IN			PPP4		N
16	C	18752803	1900	PC	FEMALE CONTACT	IN					N
17	C	18752804	1900	PC	OUTER BODY-FEMALE CONTACT	IN					N
20	C	18752805	1900	PC	FERRULE	IN					N
5	C	24534714	1000	IN	SLEEVING ELEC SHRINKABLE BULK	IN	008476	110278	PPP4		N
1	C	24567000	7000	FT	CABLE,COAXIAL 19 COND.,73OHM	IN			PPP4		N
10		51904701	200	PC	CABLE LABLE	IN	008218	040778	PPP4		N
4	C	74789300	100	PC	LABEL CONTACT CAVITY	IN	008500	110777	PYP4		N
14	C	94245601	2900	PC	CONTACT-CRIMP INSERT SOCKET	IN	008456	092978	PPP4		N
8	A	94278613	1900	PC	FERRULE INSULATOR	IN	008500	110777	PPP4		N
9	C	94360807	100	PC	HOUSING-CONN,SOCKET .125 30CAV	IN			PPP4		N
7	C	94871108	1900	PC	FERRULES GRN UNINSULATED	IN	008218	040778	PPP4		N

NUMBER OF LINE ITEMS = 15
HIGHEST FIND NUMBER = 21

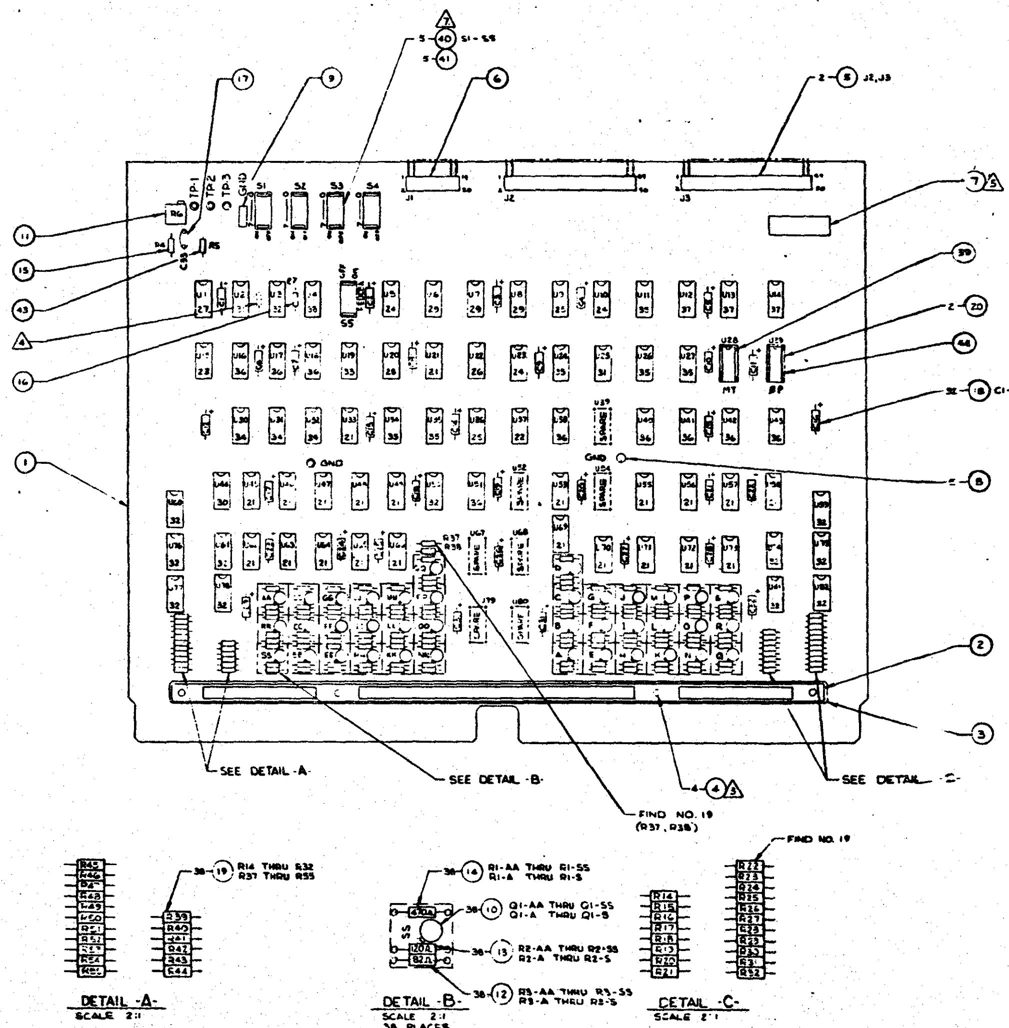
GEORGE BURN — SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.

PAGES 7-29 THROUGH 7-54 ARE DELETED.

SHEET REVISION STATUS 2	1	REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
-	00	CO	-	PRELIMINARY RELEASE	KT	[illegible]		
01	01	01	05393	INITIAL RELEASE	KT	[illegible]	[illegible]	[illegible]
01	02	02	06001	SEE ECO	TP	[illegible]	[illegible]	[illegible]
03	03	03	06628	INITIAL RELEASE	PL	[illegible]	[illegible]	[illegible]



NOTES:

1. WORKMANSHIP PER CDC MFG SPEC 10120300
2. NUMBERS INSIDE IC OUTLINES ARE ITEM FIND NUMBERS.
3. (△) INSERT RIVETS FROM NON-COMPONENT SIDE OF CIRCUIT CARD.
4. (△) CONTINGENT COMPONENT SPACE PROVIDED
5. (△) TYPE PART NO. 74273038 AND TYPE CODE 5AAY PER CDC SPEC 10121505. LOCATE APPROX AS SHOWN.
6. U28 AND U29 UNPROGRAMMED ROMS ARE IM5610 ICS (RTN 27206-002). FOR PROGRAMMING INSTRUCTIONS SEE FUNCTIONAL ELEMENT SPEC (2301-042-351).
7. (△) TO PREPARE AMP SWITCHES FOR INSTALLATION FIRST REMOVE NUMBERS 1 THRU 8 ON SWITCHES (5 PLACES). INSTALL SWITCHES WITH ON DESIGNATION OF SWITCH TOWARDS NUMBERING OR LETTERING ETCHED ON CIRCUIT CARD.
8. WHEN ASSEMBLING CIRCUIT CARD USING CDC NO. 74850200 (RTN 32872) REV 00 CARD FAB, REWORK CARD PER INSTRUCTIONS ON SHEET 2

5AAY

PL 74873038 — DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIM ARE IN INCHES/MILLIMETERS TOLERANCES

DO NOT SCALE DRAWING

MATERIAL

FINISH

DY159-A

DR PARNAK AN

CHK

ENGR KRISTENSEN

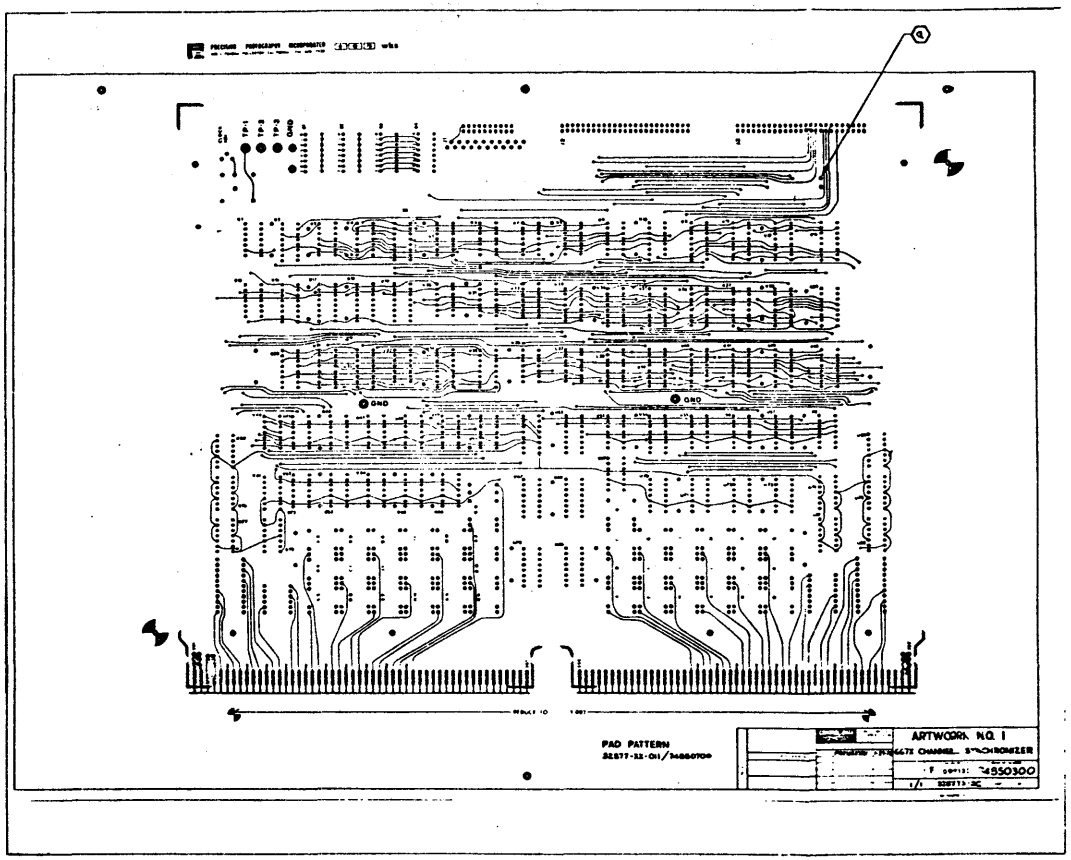
COMMUNICATIONS PRODUCTS DIV

TITLE: CKT CARD ASSEMBLY, 667X CHANNEL SYNCHRONIZER

D | CODE IDENT NO 34015 | DRAWING NUMBER 74873038

SCALE 1:1 | 35002-009-104 | SHEET 1 OF 2

REV	ECO	DESCRIPTION	DRAFT	DATE	CHK	APP'D
03		SEE SHEET 1				

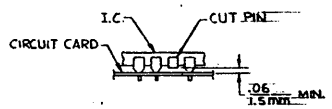


1. CLIP THE FOLLOWING PINS FROM I.C.'S NOTED:

I.C. NO.	PIN(S) NO.
U22	13
U36	8,10

2. ADD THE FOLLOWING JUMPERS (HEXAGONS DENOTE PAD IDENTICATION):

ITEM	FROM	PIN	TO	PIN	JMPR NO.
1	U11	2	U25	14	45
2	U37	1	(3)	–	45
3	U22	13	U5	6	45
4	U36	8(PIN)	U36	1	45
5	U36	2	U17	2	45
6	U13	1	U9	13	45
7	U13	2	U36	10(PIN)	45
8	U36	3	U36	9(PIN)	45



TYP CUT PIN
SCALE: NONE

DETACHED LISTS

DO NOT SCALE DRAWING

MATERIAL

FINISH

COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704

CKT CARD ASSEMBLY
667X CHANNEL SYNCHRONIZER

SIZE	DWG NO.	REV
D	34015	74873038
SCALE 1/1	3502009-104	SHEET 2 OF 2

74879600 C

D.VN	PARNAKIAN	6-11-75		TITLE CIRCUIT CARD ASSEMBLY	PREFIX	DOCUMENT NO.	REV
CHKD	W.J. ALLEN	8-27-75		667X CHANNEL SYNCHRONIZER	PL	74873038	03
ENG	KRISTENSEN	8-27-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG				FIRST USED ON		SHEET 1 OF 4	
APPR			CODE IDENT 34015	DY159-A	35002-009-104		

SHEET REVISION STATUS

4	3	2	1
00	00	00	00
01	01	01	01
01	01	01	02
03	03	03	03

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	—	PRELIMINARY RELEASE	JTP	6-11-75	
01	05893	INITIAL RELEASE	JTP	8-27-75	WJA
02	06001	SEE ECO	TP	1-21-76	WJA
03	06628	INITIAL RELEASE	PL	4-18-77	WJA

NOTES:

DETACHED LISTS

FORM 19246 01-015 092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

7-57

35002-009-104

CONTINUED	COMMUNICATIONS PRODUCTS DIV. Santa Ana Calif 92704	CODE IDENT 34015	SHEET 2 OF 4	PL	DOCUMENT NO 74873038	REV 03

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	74850200	1	PC		CKT. CARD FAB.	32872-010
2	88895400	1	PC		STIFFENER	27299-002
3	88895500	1	PC		INSULATOR	27300-002
4	88812400	4	PC		RIVETS 1/8" x 5/16"	27301-002
5		2	PC		HEADER, RT ANGLE -50	27926-002
6		1	PC		HEADER, RT ANGLE -20	28634-002
7	73954300	1	PC		NAMEPLATE	15486-010
8		5	PC		TERMINAL	01628-002
9		1	PC		TEST JACK	27765-002
10		38	PC		TRANSISTOR	23831-002
11		1	PC		RESISTOR, 2K, POT	27814-002
12	24500037	38	PC		RESISTOR, 82Ω, 1/4W	05208-002
13	24500041	38	PC		RESISTOR, 120Ω, 1/4W	03704-002
14	24500055	38	PC		RESISTOR, 470Ω, 1/4W	03708-002
15	24500050	1	PC		RESISTOR, 300Ω, 1/4W	05771-002
16	24500039	1	PC		RESISTOR, 100Ω, 1/4W	00924-002
17		1	PC		CAPACITOR, 56 Pf	27768-002
18		32	PC		CAPACITOR, IMF, 35V	20771-002
19	24500023	38	PC		RESISTOR, 22Ω, 1/4W	05761-002
20		2	PC		SOCKET, IC, 16 PIN	24158-002

33002-009-104

CONTROLLED	COMMUNICATIONS PRODUCTS DIV. Santa Ana Calif 92704	CODE IDENT 34015	SHEET 3 OF 4	PL	DOCUMENT NO 74873038	REV 03

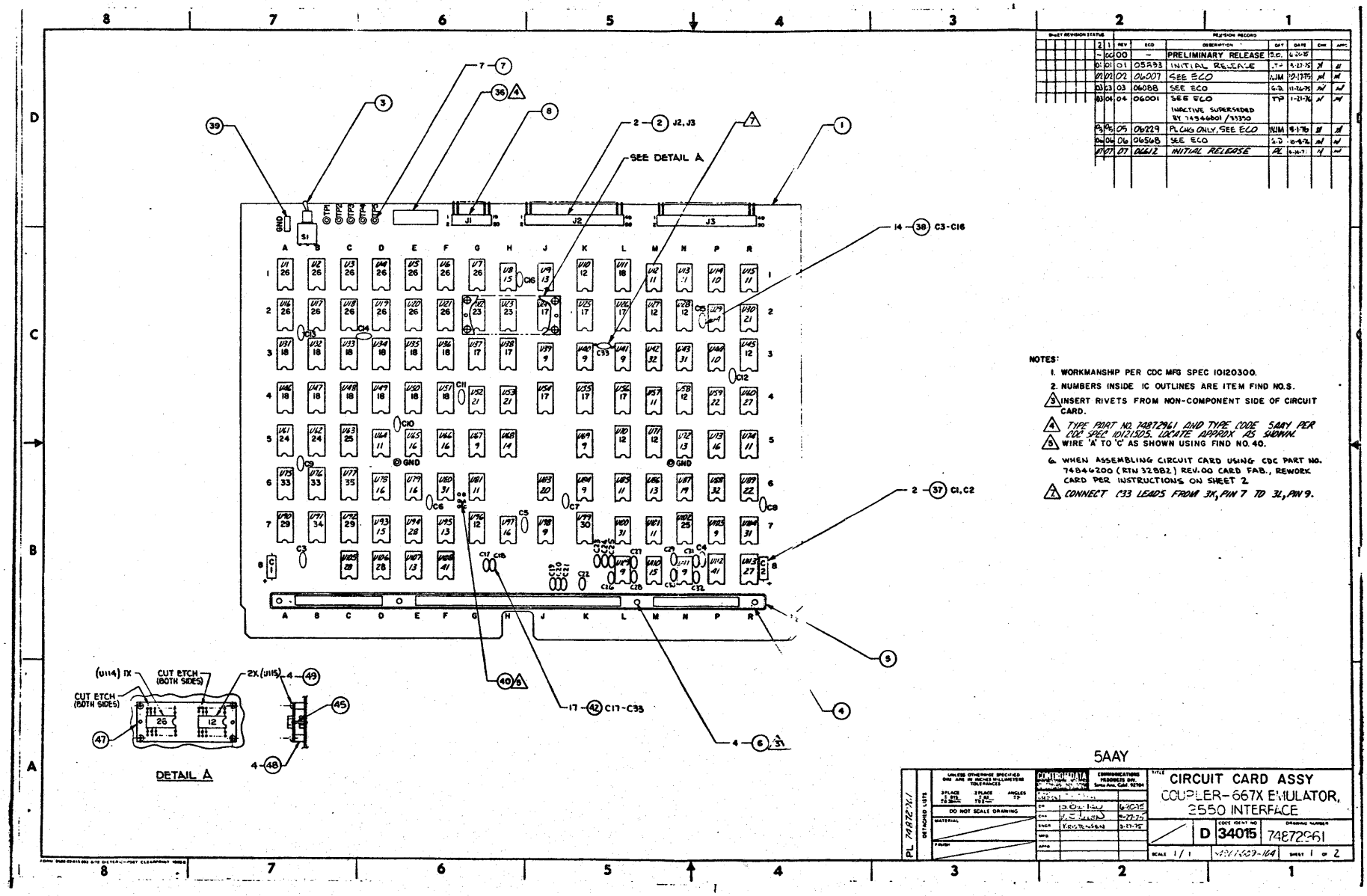
FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
21		22	PC	IC 74S00 TYPE	22124-002
22		1	PC	74S02	26100-002
23		1	PC	74S03	22948-002
24		3	PC	74S04	22125-002
25		2	PC	74S08	28452-002
26		1	PC	74S10	22949-002
27		1	PC	7413	22737-002
28		1	PC	74S20	23745-002
29		3	PC	74S40	25105-002
30		1	PC	74S74	22126-002
31	15109400	2	PC	74S112	21074-002
32		12	PC	74128	27743-002
33		1	PC	74S138	27678-002
34		3	PC	74S157	27689-002
35		6	PC	74S174	25121-002
36		9	PC	74S175	25122-002
37		3	PC	93S16	27645-002
38	94262302	1	PC	DELAY LINE	27774-002
39	74862002	1	PC	IC PROGRAMMED ROM IM5610 TYPE	33103-002 (U28)
40		5	PC	SWITCH, 8 POS, AMP	23587-002

	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 4 OF 4	PL	DOCUMENT NO 74873038	REV 03

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
41		5	PC		COVER, SWITCH	25029-002
42	74873039	REF	–		LOGIC DIAGRAM	35002-012
43	24500065	1	PC		RESISTOR, 1.2K, ¼W	03712-002
44	74862001	1	PC		IC PROGRAMMED ROM IMS610 TYPE	33102-002 (U29)
45		20	FT		WIRE, 24AWG GRN	RTA 07952-002

FORM 10247 01 015 092 DIETERICH POST CLEARPRINT 1020

PRINTED IN U.S.A.



REV	ECO	DESCRIPTION	BY	DATE
–	00	PRELIMINARY RELEASE	S.C.	6-20-75
01	01	INITIAL RELEASE	TJ	9-17-75
02	02	SEE ECO	WJM	12-1975
03	03	SEE ECO	G.D.	11-26-75
04	04	SEE ECO INACTIVE SUPERSEDED BY 74946801/93350	TP	1-21-76
05	05	PL CHG ONLY, SEE ECO	WJM	8-1-76
06	06	SEE ECO	G.D.	10-8-76
07	07	INITIAL RELEASE	PL	8-16-77

NOTES:

1. WORKMANSHIP PER CDC MFG SPEC 10120300.
2. NUMBERS INSIDE IC OUTLINES ARE ITEM FIND NO.S.
3. INSERT RIVETS FROM NON-COMPONENT SIDE OF CIRCUIT CARD.
4. TYPE PART NO. 74872961 AND TYPE CODE 5AAY PER CDC SPEC 10121505. LOCATE APPROX AS SHOWN.
5. WIRE 'A' TO 'C' AS SHOWN USING FIND NO. 40.
6. WHEN ASSEMBLING CIRCUIT CARD USING CDC PART NO. 74846200 (RTN 32882) REV. 00 CARD FAB., REWORK CARD PER INSTRUCTIONS ON SHEET 2.
7. CONNECT C33 LEADS FROM 3K, PIN 7 TO 3L, PIN 9.

5AAY

PL 74872961

DO NOT SCALE DRAWING

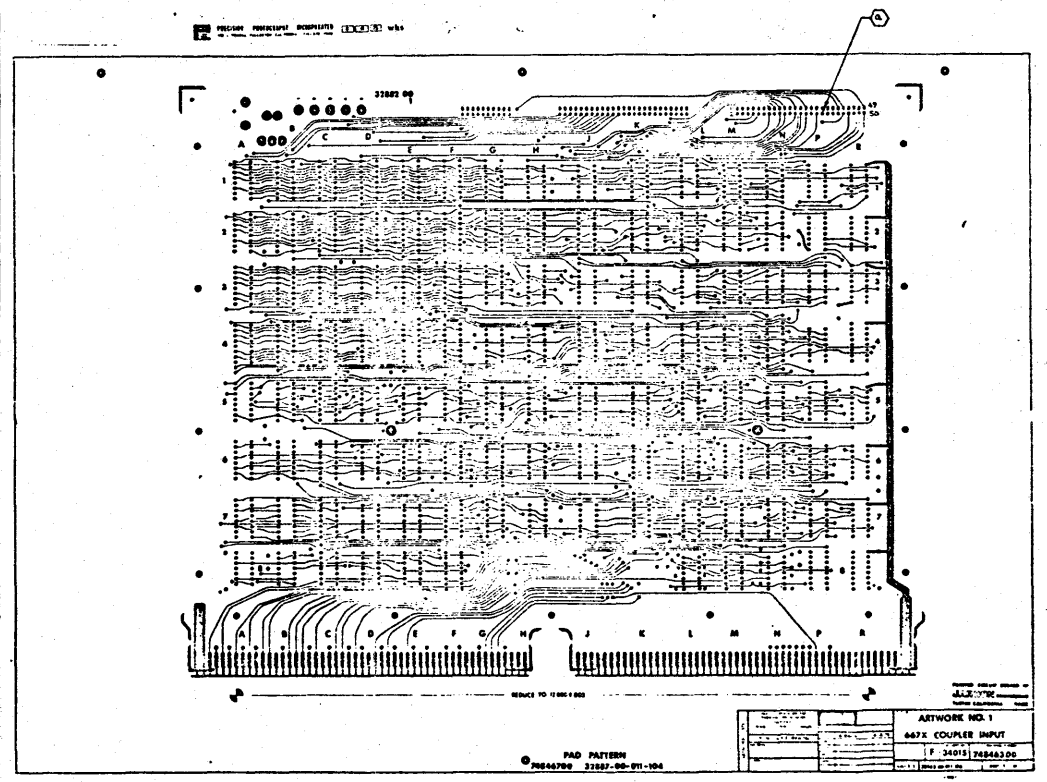
CONTROL DATA — COMMUNICATIONS PRODUCTS DIV., Santa Ana, Calif. 92704

DR	J.D. Hall	6-20-75
CHK	J.C. Allen	6-27-75
ENGR	T.R. Peterson	9-17-75

TITLE: CIRCUIT CARD ASSY
COUPLER-667X EMULATOR, 2550 INTERFACE

SIZE	CODE IDENT NO	DRAWING NUMBER
D	34015	74872961

SCALE 1/1 — 74872961-104 — SHEET 1 OF 2



PAD PATTERN
P0646700 32887-00-011-104

ARTWORK NO. 1
667X COUPLER INPUT
F 34015 74846300

SEE SHEET 1

1. CLIP THE FOLLOWING PINS FROM I.C.'S NOTED:

I.C. LOC.	PIN(S) NO
1K	14
3M	1,13
3P	6
4P	3,5
5K	8,9,10,11
6G	11,12,13
7E	5
5H	1,2,3
6F	8,9,10
5N	8

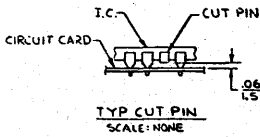
I.C. LOC.	PIN(S) NO.
9D	1
8F	15
3R	14
1N	11,12,13
6C	6
6K	10,11
6J	4,6,8,9,10,11
1F	7
3K	1,2
2N	3

2. ADD THE FOLLOWING JUMPERS: (HEXAGONS DENOTE PAD IDENTIFICATION)

ITEM	FROM	PIN	TO	PIN	FUNC
89	1K	1	5R	5	43
86	1K	14	5H	11	
85	1K	7	1J	3	
84	1K	7	6C	8	
87	1K	15	1J	15	
88	1K	2	1G	2	
89	1K	3	1G	3	
90	1K	4	1G	4	
91	1K	5	1G	5	
92	1K	6	1G	6	
93	1K	9	1G	9	
94	1K	10	1G	10	
95	1K	11	1G	11	
96	1K	12	1G	12	
97	2K	15	6G	6	43
98	2K	16	3J	14	46
99	2K	8	1H	4	46
100	2K	4	6E	8	43
101	7E	5	4K	11	43
102	2K	5	7E	1	43
103	7E	7	7E	4	43
104	2K	2	2K	1	46
105	2K	3	2K	5	46
106	1K	3	1K	8	46
107	5K	4	4K		43
108	6E	6	5D	3	
109	1J	12	240	2	
110	7H	5	7H	3	
111	6K	2	6E	2	
112	1J	11	5K	9	
113	1J	1	7E	9	
114	7E	9	7E	2	
115	1J	2	1F	7	
116	1F	7	6C	12	
117	7E	8	7B	2	
118	6M	1	6E	10	
119	1K	5	3K	1	
120	7E	3	220	2	
121	1K	6	7H	6	
122	3K	2	6K	11	
123	6K	10	6E	11	
124	5K	11	6M	6	43
125	5N	5	4N	6	43
126	1P	3	2N	11	43
127	1P	4	3P	3	43
128	1P	4	1P	5	43
129	1P	6	2P	2	43
130	1P	1	1N	10	43
131	1P	2	2N	7	43
132	1P	13	2N	6	43
133	1P	12	2P	13	43
134	2P	11	2N	12	43

ITEM	FROM	PIN	TO	PIN	FUNC
1	8F	14	5E	14	43
2	4R	15	4P	7	
3	5R	15	8P	8	
4	5T	PAD 2	4Z	3	
5	4R	3	5R	14	
6	5L	PAD 1	4R	6	
7	4Z	6	4R	2	
8	5K	3	4R	10	
9	4R	10	4R	5	
10	5T	PAD 3	4R	11	
11	4R	11	4Z	13	
12	5T	PAD 3	4R	14	
13	4R	14	5R	3	
14	5J	PAD 1	3Z	2	
15	5R	2	3R	6	
16	5J	PAD 4	5R	10	
17	5R	10	3R	5	
18	5J	PAD 4	5R	13	
19	5R	13	3R	11	
20	5J	PAD 2	3R	12	
21	5T	PAD 2	3R	9	
22	5T	PAD 2	5R	9	
23	5T	PAD 2	5R	4	
24	5T	PAD 2	4K	12	
25	5T	PAD 2	4R	9	
26	5K	PAD 4	4R	7	
27	5K	PAD 4	4Z	4	
28	4R	1	3R	1	
29	5R	1	2L	5	
30	2L	5	5K	9	
31	3L	9	TAB	250	
32	5K	3	7H	13	
33	7H	2	7H	1	
34	7H	13	7F	13	
35	7Z	13	7F	10	
36	8A	9	8P	6	
37	8P	4	8P	11	
38	8R	PAD 4	8P	15	
39	8P	15	8F	2	
40	8A	PAD 4	8P	14	
41	8P	14	8P	10	43

ITEM	FROM	PIN	TO	PIN	FUNC
42	7F	12	5P	7	43
43	8P	7	8F	7	
44	7H	12	9P	9	
45	8P	9	9F	9	
46	8A	PAD 4	8P	1	
47	8P		8P	5	
48	8A	PAD 1	8F	2	
49	8P	2	8F	15	
50	9B	PAD 3	9F	10	
51	8F	10	9F	14	
52	8B	PAD 3	8F	6	
53	9F	6	9F	11	
54	8B	PAD 4	8F	1	
55	8F	1	8F	5	
56	8B	PAD 3	8F	3	
57	8B	PAD 3	8F	4	
58	8B	PAD 3	8F	12	
59	8B	PAD 3	8F	13	
60	8A	PAD 3	8P	3	
61	8A	PAD 3	8P	4	
62	8A	PAD 3	8P	12	
63	8A	PAD 3	8P	13	
64	2R	4	7R	11	
65	3R	PAD 4	7R	13	
66	7C	12	33	(6)	
67	4N	6	4P	5	
68	4N	1	4P	3	
69	1K	15	1K	PAD 4	
70	2M	1	2M	3	
71	2M	13	2N	13	
72	3P	6	2P	10	
73	2P	10	2P	9	
74	2P	8	3P	PAD 4	
75	5D	1	5D	4	
76	7M	1	6C	7	43
77					
78					
79					
80					
81	1K	14	6C	8	43
82	3L	2	5L	15	43



TYP CUT PIN
SCALE: NONE

CIRCUIT CARD ASSY COUPLER-667X EMULATOR 2550 INTERFACE	34015	D	74872961	07
			SHEET 2 OF 2	

74879600 C

DWN	[illegible] KIAN	6-18-75
CHKD	W. JANIEC	6-27-75
ENG	KRISTENSEN	8-21-75
MFG		
APPR		

CONTROL DATA

COMMUNICATIONS PRODUCTS DIV.
Santa Ana, Ca. 92704

CODE IDENT 34015

TITLE: CIRCUIT CARD ASSY COUPLER-667X EMULATOR, 2550 INTERFACE

FIRST USED ON: DY159-A

34967-009-104

PREFIX	DOCUMENT NO.	REV
PL	74872961	07

SHEET 1 OF 4

SHEET REVISION STATUS

4	3	2	1
00	00	00	00
01	01	01	01
02	02	02	02
02	02	03	03
02	02	03	04
05	02	03	05
06	03	02	01
07	01	01	07

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	–	PRELIMINARY RELEASE	JTP	6-18-75	
01	05893	INITIAL RELEASE	JTP	8-27-75	[illegible]
02	06007	SEE ECO	WJM	10-17-75	[illegible]
03	06088	SEE ECO	G.D	11-26-75	[illegible]
04	06001	SEE ECO INACTIVE SUPERSEDED BY 74846001 / 33390	T.P	1-21-76	[illegible]
05	06229	SEE ECO	WJM	3-1-76	[illegible]
06	06568	REVISED PER ECO	PL	10-28-76	[illegible]
07	06612	INITIAL RELEASE	PL	4-14-77	[illegible]

NOTES:

DETACHED LISTS

34967-029-104

COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 4	PL	DOCUMENT NO 74872961	REV 07

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	74846200	1	PC	CKT CARD FAB	32882-010
2		2	PC	HEADER, RT ANGLE -50	27926-002
3		1	PC	SWITCH TOGGLE, (SPDT)	28629-002
4	88895400	1	PC	STIFFENER	27299-002
5	88895500	1	PC	INSULATOR	27300-002
6	88812400	4	PC	RIVET	27301-002
7		7	PC	TERMINAL	01628-002
8		1	PC	HEADER RT ANGLE -20	28634-002
9		10	PC	IC 74S04 TYPE	22125-002
10		2	PC	74S11	23305-002
11		9	PC	74S00	22124-002
12		9	PC	74S112	21074-002
13		5	PC	74S02	26100-002
14		2	PC	74S32	28459-002
15		3	PC	74S30	27440-002
16		6	PC	74S10	22949-002
17		8	PC	74S157	27689-002
18		13	PC	93421	27643-002
19		1	PC	74S40	25105-002
20		1	PC	IC 74S260 TYPE	26098-002

34967-009-104

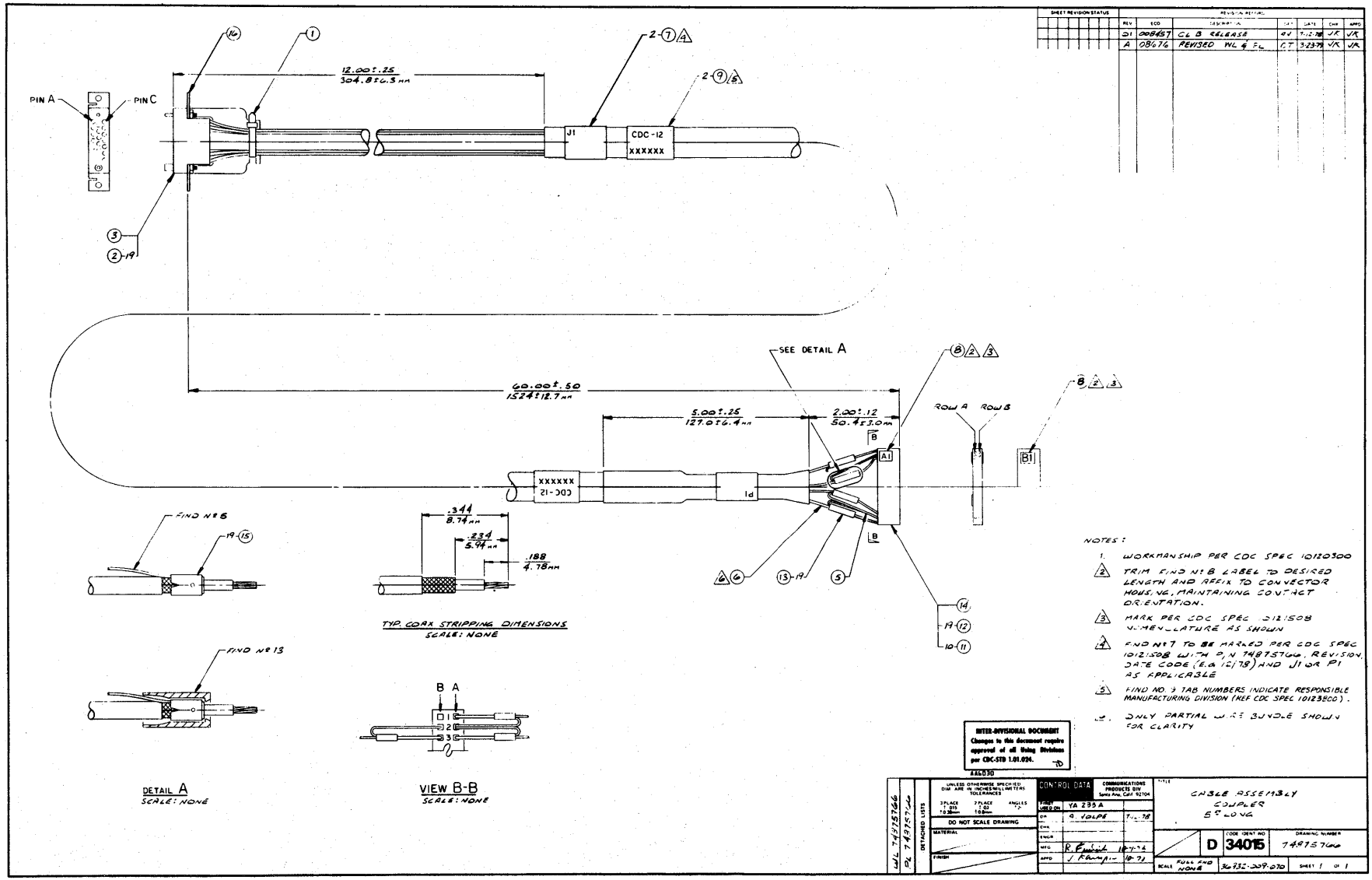
CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 3 OF 4	PL	DOCUMENT NO 74872961	REV. 07

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
21		3	FC	IC 74393 TYPE	28513-002
22		2	PC	7427	22736-002
23		2	FC	74S135	25114-002
24		2	PC	DM8098	27446-002
25		2	PC	74170	28511-002
26		14	PC	93415	23869-002
27		2	PC	74S158	28512-002
28		3	PC	74S38	27955-002
29		2	PC	74S174	25121-002
30		1	PC	74S139	25116-002
31		4	PC	74S08	28452-002
32		3	PC	74S20	23745-002
33		2	PC	IC DM8097 TYPE	27447-002
34		1	PC	RESISTOR PACK 1K Ω	27309-002
35		1	PC	RESISTOR PACK 2K Ω	27310-002
36		1	PC	NAMEPLATE	15486-010
37		2	PC	CAPACITOR, 100 Nf, 10V	19620-002
38		14	PC	CAPACITOR, .01 uf	21616-002
39		1	PC	TEST JACK	27765-002
40		.1	FT	WIRE 24AWG, GRN	15167-002

34967-009-104

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 4 OF 4	PL	DOCUMENT NO 74872961	REV. 07

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
41		2	PC	IC 8234 TYPE	28690-002
42		17	PC	CAPACITOR, 200PFD	08278-002
43		5.0	FT	WIRE, 26 GA, GRN	07952-002
44	74872962	REF	-	LOGIC DIAGRAM	RTN 34967-012
45		0.2	FT	WIRE, 22GA BUSS	0930-002
46		1.0	FT	WIRE, 22GA, GRN	15009-002
47		1	PC	ADAPTER CARD	15865-010
48		4	PC	STANDOFF	15183-002
49		4	PC	SCREW, 2-56	06293-002



SHEET REVISION STATUS	REV	ECO	DESCRIPTION	BY	DATE	CHK	APPD
	D1	008457	CL B RELEASE	AV	7-12-78	JR	JR
	A	08676	REVISED WL & FL	CT	3-23-79	JR	JR

NOTES:

1. WORKMANSHIP PER CDC SPEC 10120300
2. TRIM FIND NO 8 LABEL TO DESIRED LENGTH AND AFFIX TO CONNECTOR HOUSING, MAINTAINING CONTACT ORIENTATION.
3. MARK PER CDC SPEC 31215OB NOMENCLATURE AS SHOWN
4. FIND NO 7 TO BE MARKED PER CDC SPEC 10121508 WITH P/N 74875700, REVISION, DATE CODE (E.G. 12/78) AND J1 OR P1 AS APPLICABLE
5. FIND NO. 3 TAB NUMBERS INDICATE RESPONSIBLE MANUFACTURING DIVISION (REF. CDC SPEC 10123800).
6. ONLY PARTIAL WIRE BUNDLE SHOWN FOR CLARITY

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

UL	74975746
CL	74975744
DETACHED LISTS	

CONTROL DATA		
ISSUED ON	YA 235 A	
DR	G. VOLPE	7-12-78
CHK		
ENGR		
MFG	R. Emrich	10-7-78
APPD	J. Ramsey	10-7-78

COMMUNICATIONS PRODUCTS DIV
Santa Ana, Calif 92704

DO NOT SCALE DRAWING

MATERIAL

FINISH

TITLE: CABLE ASSEMBLY COUPLER 5" LONG

CODE IDENT NO	DRAWING NUMBER
D 34015	74875700

SCALE: FULL AND NONE | 36932-209-070 | SHEET 1 OF 1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74875766	A	CLA	A	CABLE ASSY CYBER COUPLER	DM	2551	08/30/78	03/27/79	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN INC	S OR N
4	A	10123801	2.00	PC	LABEL, CABLE MARKING	IN	08676	03/27/79			N
5	A	10123835	2.00	PC	LABEL CABLE MAP CDC 12 STAGES	IN	08676	03/27/79			N
1	C	12620301	1.00	PC	STRAP CABLE ADJUSTABLE	IN			PPP1		N
2	C	13752711	19.00	PC	SINGLE PIECE CONTACT - COAX	IN			PPP4		N
3	C	13752714	1.00	PC	CONN COAX KEYED JACKS MULT POS	IN					N
4	C	24534714	7.00	IN	SLEEVING ELEC SHRINKABLE MULK.	IN			PPP4		N
5	C	24548301	48.00	IN	WIRE-ELECT-24 GA-PVC-UL-BLK	IN			PPP4		N
6	C	24567000	5.00	FT	CABLE-COAXIAL 19 COND-.730HM	IN			PPP4		N
7		51984701	2.00	PC	CABLE LABLE	IN			PPP4		N
8	C	74749300	1.00	PC	LABEL CONTACT CAVITY	IN			PPP4		N
11	C	94245601	1.00	PC	CONTACT-CRIMP INSERT SOCKET	IN			PPP4		N
12	C	94245604	19.00	PC	CONTACT-CRIMP INSERT SOCKET	IN	08676	03/27/79			N
13	A	94278413	19.00	PC	FERRULE INSULATOR	IN			PPP4		N
14	C	94360807	1.00	PC	HOUSING-CONN-SOCKET .125 30CAV	IN			PPP4		N
15	C	94871108	19.00	PC	FERRULES GUN UNINSULATED	IN			PPP4		N
16	D	97177404	1.00	PC	STRAIN RELIEF	IN					N

NUMBER OF LINE ITEMS = 16
HIGHEST FIND NUMBER = 16

PROJECT ENGINEER SANTA ANA

AA 2709 REV. 7-78

Printed in U.S.A.

DWN	C TICE	3-79	CONTROL DATA COMMUNICATIONS SYSTEMS DIV. Santa Ana, Ca. 92704	TITLE CABLE, 19-CONDUCTOR COAX	PREFIX WL	DOCUMENT NO. 74875766	REV A
CHKD		3/79					
ENG		3/79					
MFG		3-79					
APPR		3-79	CODE IDENT 34015	FIRST USED ON YA233-A		SHEET 1 OF 3	

SHEET REVISION STATUS

3	2	1
A	A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	08676	CLASS 'A' RELEASE	CT	3-23-79	VK

NOTES:

DETACHED LISTS

FORM 19246-02-015-082 DIETERICH-POST CLEARPRINT 1020

PRINTED IN U.S.A.

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 3	WL	DOCUMENT NO. 74875766	REV. A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
1	6	30	90	5FT	J1	A	2	P1	A1	12,13,15	COND. } TYP. 13 PLCS
2	↑	↑		↑	↑			↑	A2	5,11	SHIELD } TYP. 13 PLCS
3			91			B			B3	12,13,15	
4									B2	5,11	
5			92			C			A3	12,13,15	
6									A2	5,11	
7			93			D			B4	12,13,15	
8									B5	5,11	
9			94			E			A4	12,13,15	
10									A5	5,11	
11			95			F			B6	12,13,15	
12									B5	5,11	
13			96			H			A6	12,13,15	
14									A5	5,11	
15			97			J			B7	12,13,15	
16									B8	5,11	
17			98			K			A7	12,13,15	
18									A8	5,11	
19			9			L			B9	12,13,15	
20									B8	5,11	
21			900			M			A9	12,13,15	
22									A8	5,11	
23			910			N			B10	12,13,15	
24									B11	5,11	
25	↓	↓	920	↓	↓	P		↓	A10	12,13,15	
26	6	30		5FT	J1			P1	A11	5,11	

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CD	COMMUNICATIONS SYSTEMS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 3 OF 3	WL	DOCUMENT NO. 74875766	REV. A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
27	6	30	930	5FT	J1	R	2	P1	B12	12,13,15	COND. TYP. 6 PLCS
28	↑	↑		↑	↑		↑	↑	B11	5,11	SHIELD TYP. 6 PLCS
29			940			S			A12	12,13,15	
30									A11	5,11	
31			950			T			B13	12,13,15	
32									B14	5,11	
33			960			U			A15	12,13,15	
34									A14	5,11	
35			970			V			B15	12,13,15	
36									B14	5,11	
37	↓	↓	980	↓	↓	W	↓	↓	A13	12,13,15	
38	6	30		5FT	J1		2	P1	A14	5,11	

FORM 23562-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

Some of the terminology used in the manual was shortened to simplify explanations.

Circular buffer	circular buffer memory
CLA	communications line adapter
CLE	communications line expansion
Coupler	667X Emulation Coupler
Coupler buffer	coupler buffer memory
Coupler select switch	MP equipment select switch
DFM bus	data from memory bus
DIP	dual in-line package
DMA	direct memory access
DTM bus	data to memory bus
F register	function register
FDC register	from data channel register
Host	peripheral processor
IDC	internal data channel
Interface	2550 interface circuit card
Inverter	line inverter

This glossary relates the shortened terms to the terms used on the logic diagrams.

MA bus	memory address bus
Maintenance ROM	maintenance address ROM
MH register	maintenance hold flag register
Modems	modulator and demodulator
MP	microprocessor
NPU	network processor unit
Operational ROM	operational address ROM
PPU	peripheral processor unit
Processor	microprocessor
Protect RAM	memory protect bit RAM
RAM	random-access memory
Reject RAM	PPU character reject RAM
ROM	read-only memory
S register	status register
Synchronizer	channel synchronizer circuit card
TC control	terminal count logic
TDC register	to data channel register
Y-line decoder	MP address decoder

Some of the mnemonics used in the logic diagrams of the coupler are built from a prefix, a signal, and a suffix. The prefix gives the source of the signal, and the suffix gives the location of the signal. While a third type of mnemonic includes a number which indicates that it is one of a series of bits emanating from the source. Rather than offer a complete (and redundant) list of mnemonics, this appendix lists all of the building blocks which are used to make up mnemonics. Wherever confusion could exist, entire mnemonics are listed.

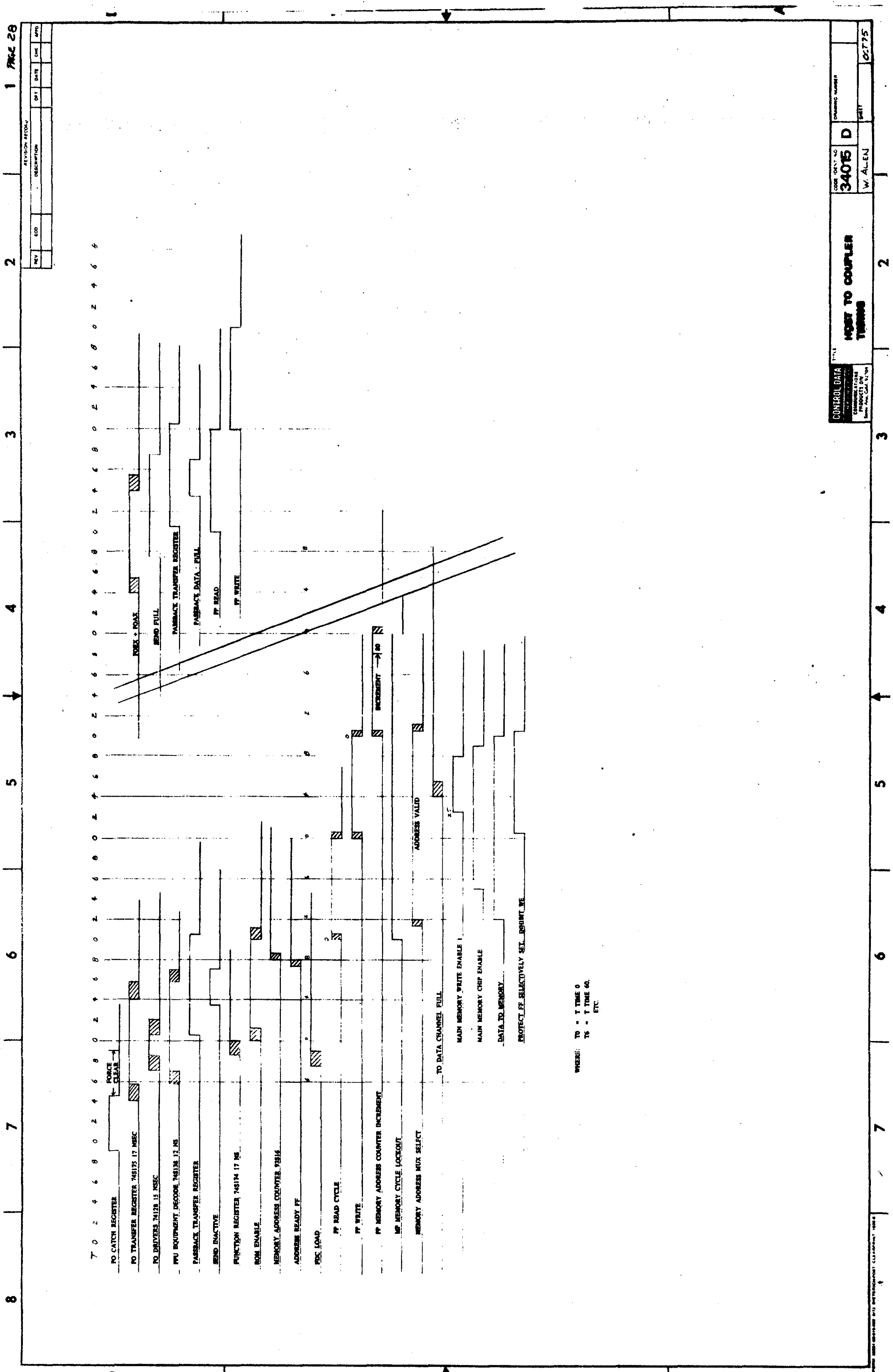
AREADY	address ready
B9A14WE	bits 9 and 14 write enable
CBA5	circular buffer address bit 5, 1 of 8
CBM100	coupler buffer memory bit 10 out
CBMT	circular buffer empty
CBMTF	circular buffer empty flip-flop
CBUF	circular buffer
CBUFCE	circular buffer cycle enable
CBUFI	circular buffer initialize
CBWE	circular buffer write enable
CDENA	control decoder enable
...CE	cycle enable
CLK01I	clock 1 MHz in
CLK10I	clock 10 MHz in
CRWE	character reject write enable
CSEL	coupler selected
DFM6	data from memory bit 6, 1 of 12
DTM7	data to memory bit 7, 1 of 12
ECBM	enable coupler buffer memory
ENAMT	enable maintenance
ENAOP	enable operation
...F	flip-flop
FDC8	from data channel bit 8, 1 of 12
FDCL	from data channel load
FMP01	from microprocessor bit 1, 1 of 12
FR09	function register bit 9, 1 of 12
FRCLEAR	function register
FULLF	full flip-flop
GND	ground
...I	in or increment (counter) or initialize (memory)
...L	load
...M	modified
MAB02	memory address bus bit 2, 1 of 10
MAC03	memory address counter bit 3, 1 of 10
MACI	memory address counter increment
MAINT	maintenance
MMWE	master memory write enable
MP...	microprocessor (the processor)
MPINC	microprocessor increment counter
MPMARI	MP memory access reply initiate
NREPLY	negative reply
...O	out
PB...	pass back
PB04I	pass-back data bit 4 in, 1 of 12
PO...	pass on
SEND...	send
...A...	active
...E...	empty
...F...	full
...FN...	function
...I...	inactive

...MC...	master clear
...P...	parity
PP...	peripheral processor (the host)
PROT	protect
RD05	receive data bit 5, 1 of 16
SD06	send data bit 6
SRI	status register initialize
T40	time 40, 1 of several 10 MHz clocks
TC	terminal count
TCC	terminal count complete
TDC07	to data channel bit 7, 1 of 12
TMPC	timed microprocessor cycle
TMPCE	timed microprocessor cycle enable
...WE	write enable
...X	coupler internal
Y12	Y line bit 12

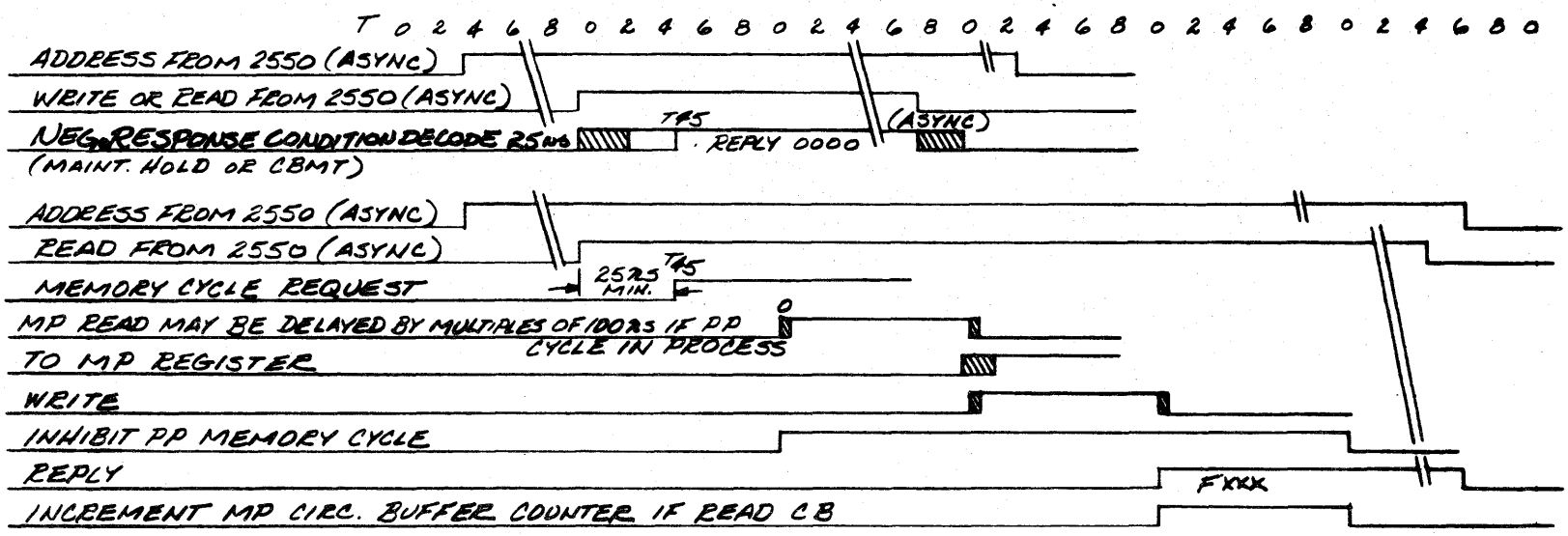
TIMING DIAGRAMS

C

The timing diagrams in this appendix relate signals to time in nanoseconds. Multiply the number at the top of the diagram by 10 to arrive at the relative time in nanoseconds.



PAGE 28
REVISION RECORD
FORCE CLEAR
PO CATCH REGISTER
PO TRANSFER REGISTER 74S175 17 NSEC
PO DRIVERS 74128 15 NSEC
PPU EQUIPMENT DECODE 74S138 12 NS
PASSBACK TRANSFER REGISTER
SEND INACTIVE
FUNCTION REGISTER 74S174 17 NS
ROM ENABLE
MEMORY ADDRESS COUNTER 93S16
ADDRESS READY FF
PDC LOAD
PP READ CYCLE
PP WRITE
PP MEMORY ADDRESS COUNTER INCREMENT
MP MEMORY CYCLE LOCKOUT
MEMORY ADDRESS MUX SELECT
TO DATA CHANNEL FULL
MAIN MEMORY WRITE ENABLE 1
MAIN MEMORY CHIP ENABLE
DATA TO MEMORY
PROTECT FF SELECTIVELY SET, INHIBIT WE
POEX + POAX
SEND FULL
PASSBACK TRANSFER REGISTER
PASSBACK DATA - FULL
PP READ
PP WRITE
INCREMENT → 80
ADDRESS VALID
WHERE: T0 = T TIME 0
T6 = T TIME 60
ETC
CONTROL DATA
HOST TO COUPLER TIMING
34015 D
W. ALEN
OCT 75



WHERE:

T0 = T TIME 0
T6 = T TIME 60, ETC.

Processor to Coupler Timing

The upper 4 bits (8 through 11) of the output word provide I/O control and act, in various combinations, either as a flag for data characters or as a control for the modem. Any data to be transmitted must be accompanied by either a 4XXX or a 5XXX function code.

Table D-1 describes the meaning of the upper four control bits. The output data word is in reference to data from the host.

TABLE D-1. DATA WORD FUNCTION CODES

Code	General Description
0XXX	A do-nothing function; no data is transferred.
1XXX	Enables the receiver section of the DCS to resync. Does not affect the carrier or the line connection. No data should be contained in this word.
2XXX	Turns off the carrier. No data should be contained in this word.
3XXX	Turns off the carrier and allows the receiver to resync. No data should be contained in this word. The valid data character preceding this function code is transmitted prior to carrier turn-off. Note that MPC's appended to a clocked-data modem message are considered to be valid data characters.
4XXX	Turns on the carrier. Must be appended to all data words (see 5XXX code description).
5XXX	Turns on the carrier and resyncs the receiver. Can contain data to be transmitted; primarily a function for Full-Duplex operation. Should be used whenever it is desirable to resync the receiver and transmit data simultaneously.
6XXX	Resyncs the receiver, turns off the carrier, and disconnects the telephone connection. No data should be contained in this word, Used primarily to disconnect the phone line. NOTE The 2XXX, 3XXX, and 6XXX codes await the disassembly of the previous valid character before they affect the carrier; 4XXX and 5XXX codes act immediately. The 6XXX code does not wait for completion of the last bit of the last output character before becoming active. Software timing for the use of the 6XXX code is desirable.
7XXX	Resyncs the receiver and enables the telephone connections for data transmissions. This word contains no information to be transmitted.
X (1xx) XX (Bit 8 set)	Used to disconnect a modem when output operation has failed in the middle of a character. Indicates that any valid character in the Output Buffer should be ignored, and that any data accompanying the function code should be transferred into the buffer memory. The DSC does not recognize that it is disassembling a character on this terminal and it executes the incoming function.

COMMENT SHEET

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