

Customer Engineering Diagrams

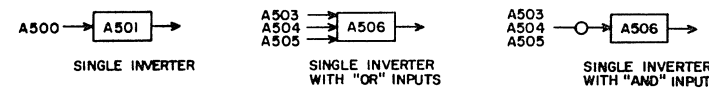
**CONTROL DATA®
169 AUXILIARY
MEMORY UNIT**

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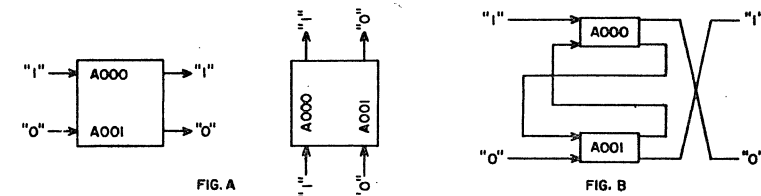
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SYMBOLS

SINGLE INVERTER - A single inverter inverts input signals so that a "1" input results in a "0" output and a "0" input results in a "1" output. Inputs to symbols are identified by arrowheads.

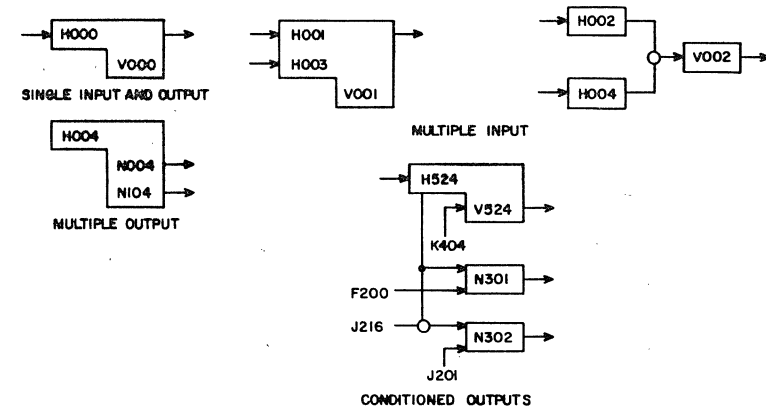


FLIP-FLOP (FF) - The flip-flop is a storage device with two stable states, designated "1" (or Set) and "0" (or Clear), and is composed of two inverters. The logical symbol (Fig. A) is a square that is formed by the combination of two single inverter symbols. By convention, "1" (or Set) inputs and outputs are shown with the upper or left half of the symbol and "0" (or Clear) inputs and outputs are shown with the lower or right half of the symbol. This diagrammatic convention simplifies the actual interconnection of the two inverters as shown in Fig. B.

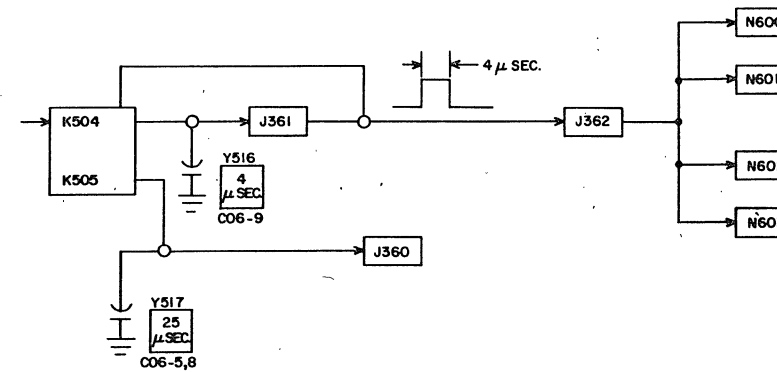


CONTROL DELAY - A control delay consists of an H--- part, which receives the input, and a V--- or N--- part, which provides the output. The output is a clocked pulse which is delayed with respect to the input pulse by one phase time of the clock (0.2 microseconds). Conventions which apply to control delays are:

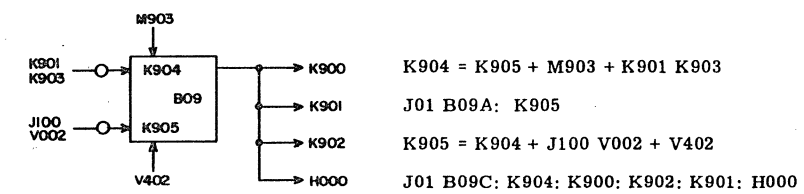
1. Clock pulse inputs to control delays are not shown on the diagrams and must be obtained from the equation file.
2. The logical number designation indicates the clock phase of the output signal. An odd number indicates an odd clock phase, and an even number indicates an even clock phase.
3. The time scales shown on all sequence diagrams are in 0.2 microsecond (1 clock phase time) intervals.



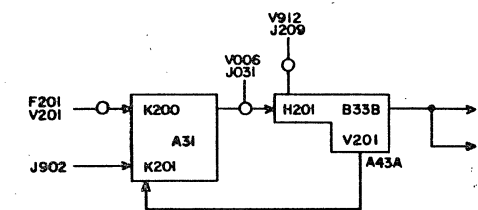
CAPACITIVE DELAY - A capacitive delay is used in an AND configuration to delay the "1" input to a logic element. The capacitor is shown with the curved (negative) plate adjoining the AND symbol. A small box shows the equation file symbol assigned to that delay, the duration of the delay, and the coordinate jack and pin number where physical connection to the capacitor(s) is made. The output waveform may be omitted.



SYMBOL REPRESENTATION OF TYPICAL EQUATIONS



$K904 = K905 + M903 + K901$
 $K905 = K904 + J100 + V002 + V402$
 J01 B09A: K905
 J01 B09C: K904; K900; K902; K901; H000

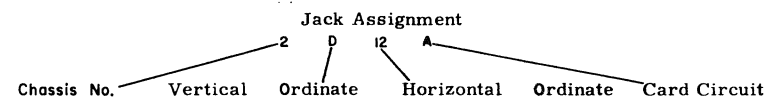


$K200 = K201 + F201 + V201$
 $K201 = K200 + V201 + J902$
 J01 A31 A: K201; J246
 J01 A31 C: K200; H201; F229; K200

$H201 = C004 + K201 + J031 + V006 + J209 + V912$
 J01 B33B: V201
 $V201 = H201 + C013$
 J01 A43A: K201; K210

JACK ASSIGNMENTS

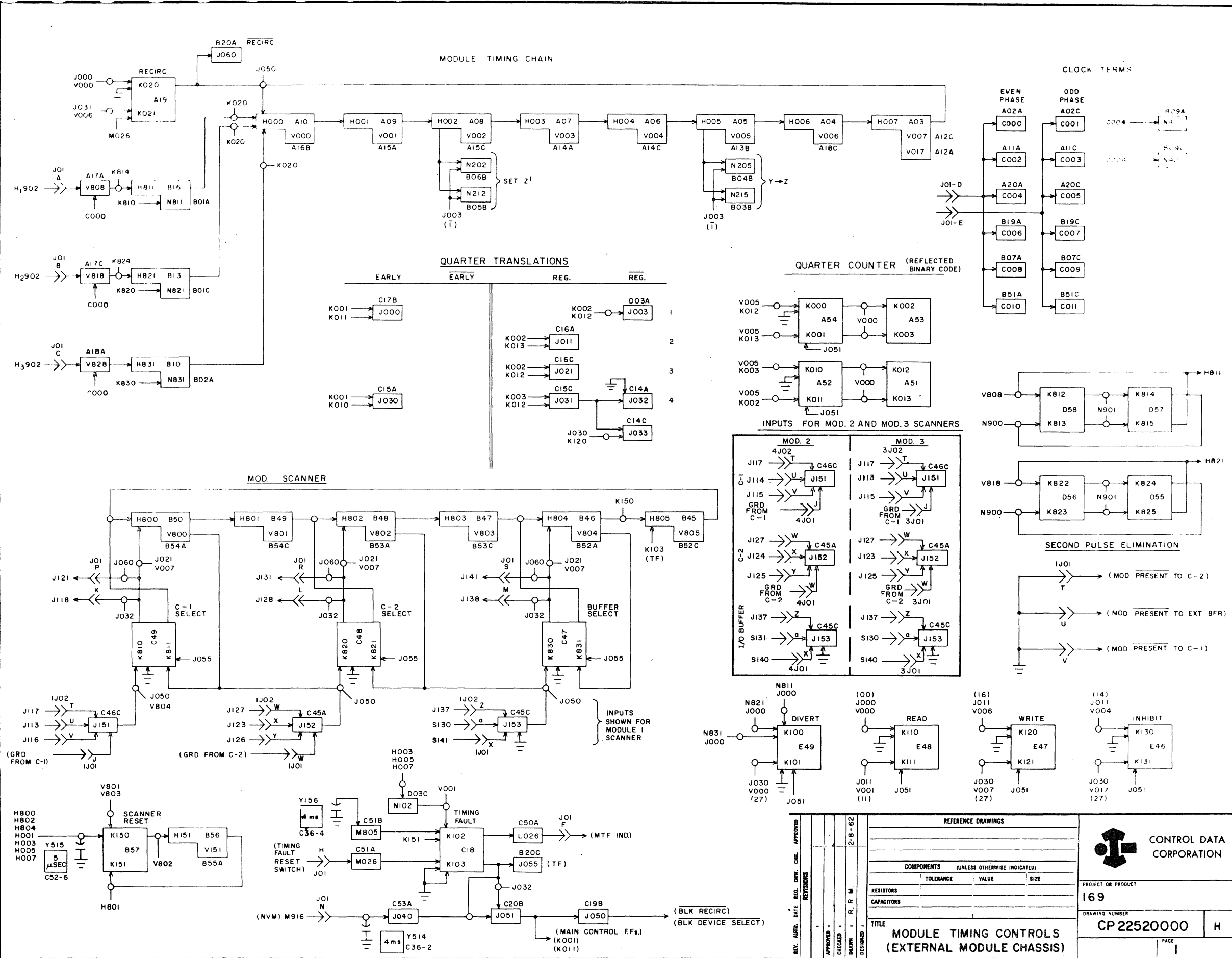
The jack assignments of the printed circuit cards associated with each logic symbol appear near the logical designation on the diagram. Jack assignments indicate the physical location of a printed circuit card.



Conventions which apply to jack assignments shown on the diagrams:

1. When most of the jack assignments on a diagram are on a common chassis, the chassis number is omitted from the jack assignments for this chassis and specified in a note on the diagram.
2. The omission of the card circuit letter from a jack assignment indicates card circuit B. (For flip-flops which indicate one jack assignment for both inverters, the omission of the card circuit letter indicates card circuit A for the even-numbered inverter and card circuit C for the odd-numbered inverter.)

KEY TO SYMBOLS USED
ON LOGIC DIAGRAMS



REFERENCE DRAWINGS	
COMPONENTS (UNLESS OTHERWISE INDICATED)	
TOLERANCE	VALUE SIZE
RESISTORS	
CAPACITORS	
TITLE	
MODULE TIMING CONTROLS (EXTERNAL MODULE CHASSIS)	
DRAWING NUMBER	
CP 22520000 H	
PAGE	
1	

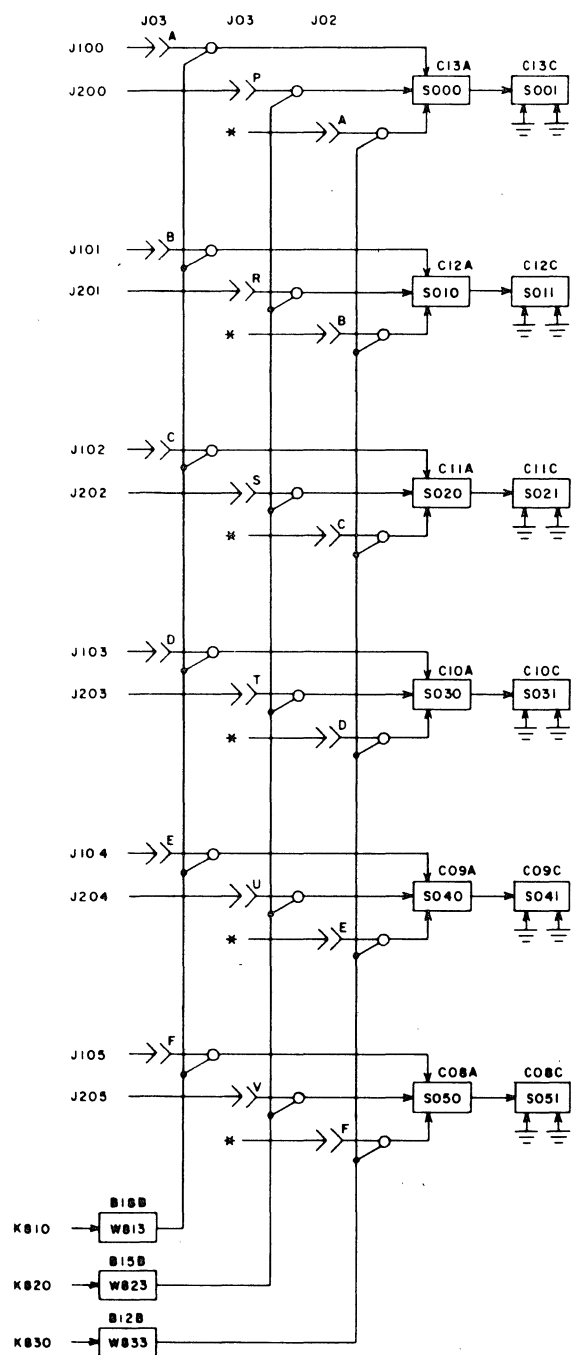


PROJECT OR PRODUCT
169

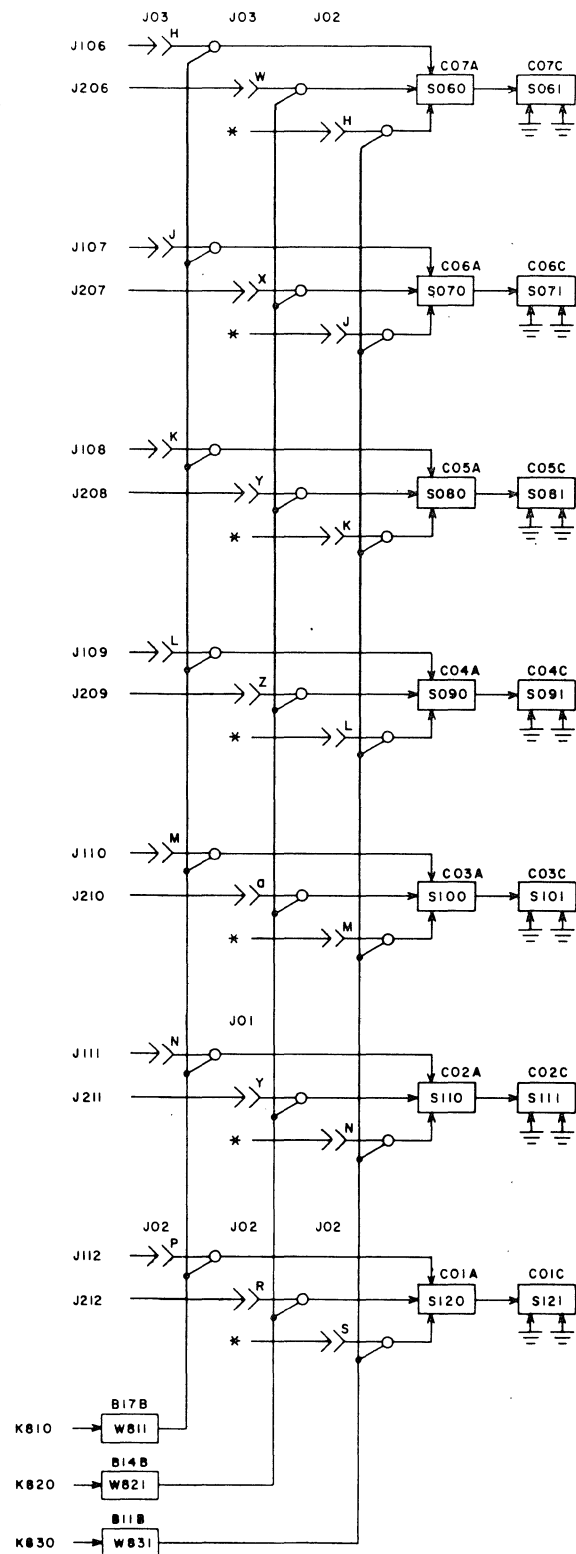
DRAWING NUMBER
CP 22520000 H

REV. AUTH. DATE. REQ. DESK. CHK. APPROVED
 DESIGNED - R. R. M.
 CHECKED -
 DRAWN -
 2-8-62

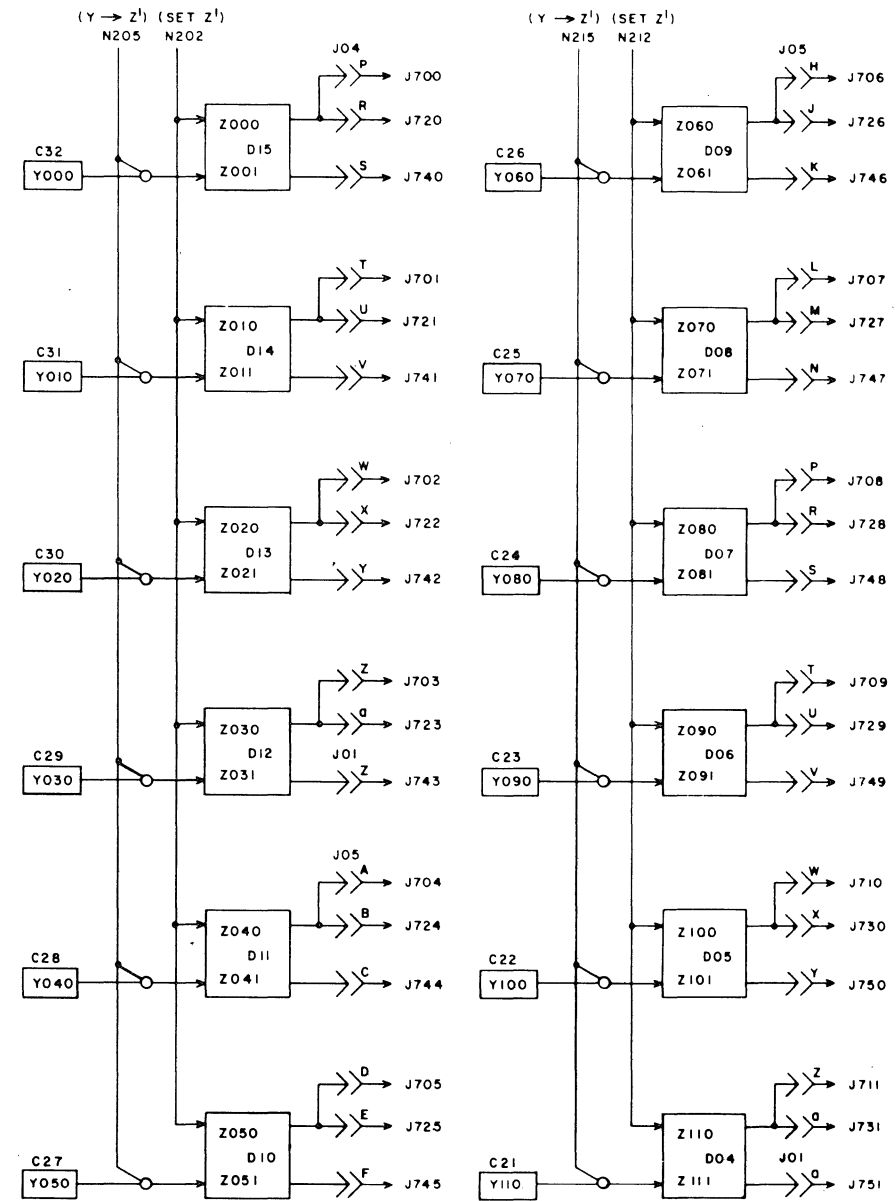
S' INVERTERS



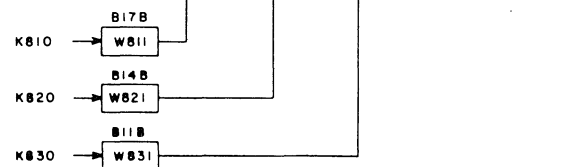
* EXTERNAL BFR INPUTS TO S' INVERTERS ARE SHOWN UNDER (BER) -> S' ON DWG XCP225204.



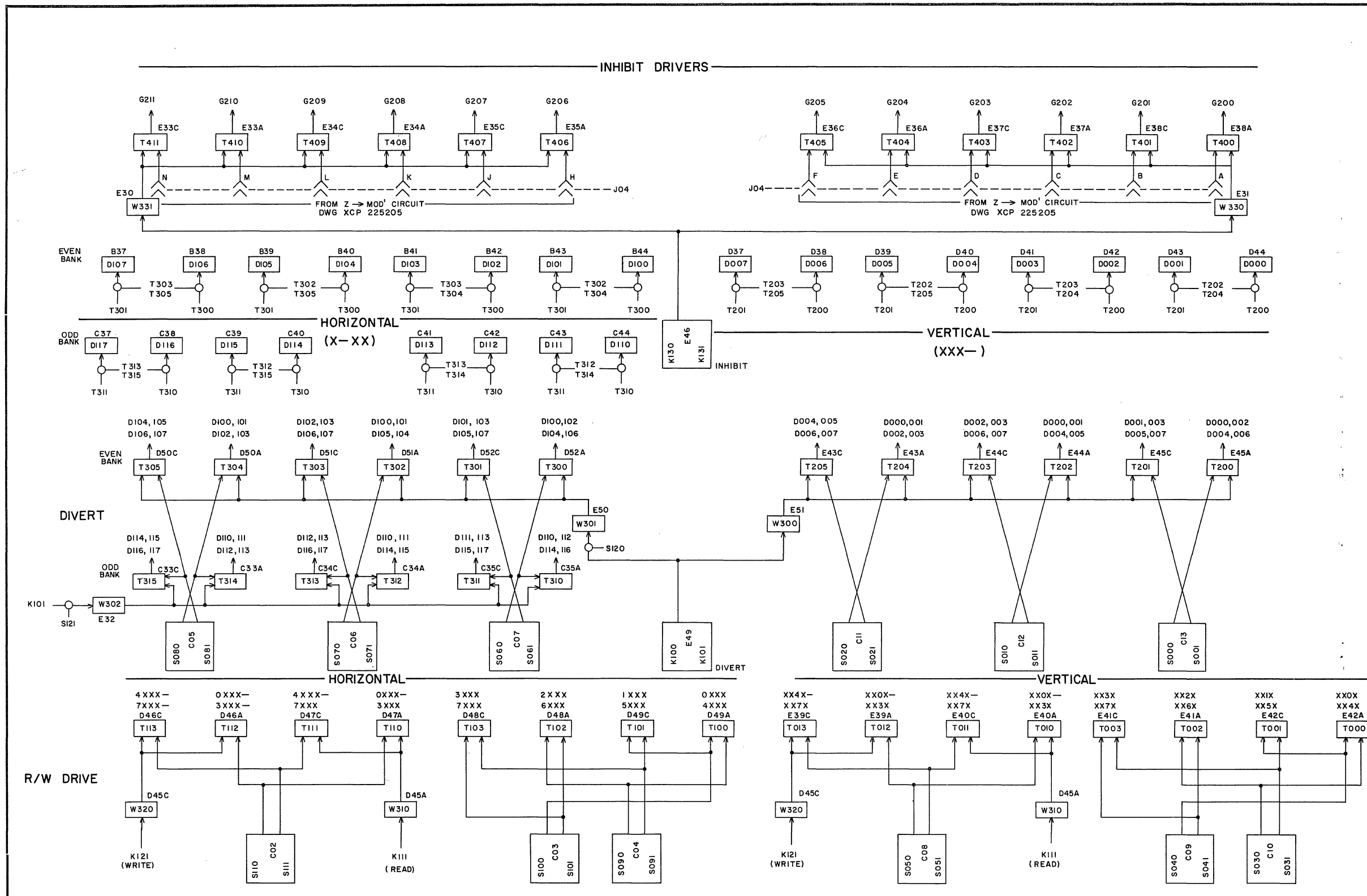
Z' REGISTER



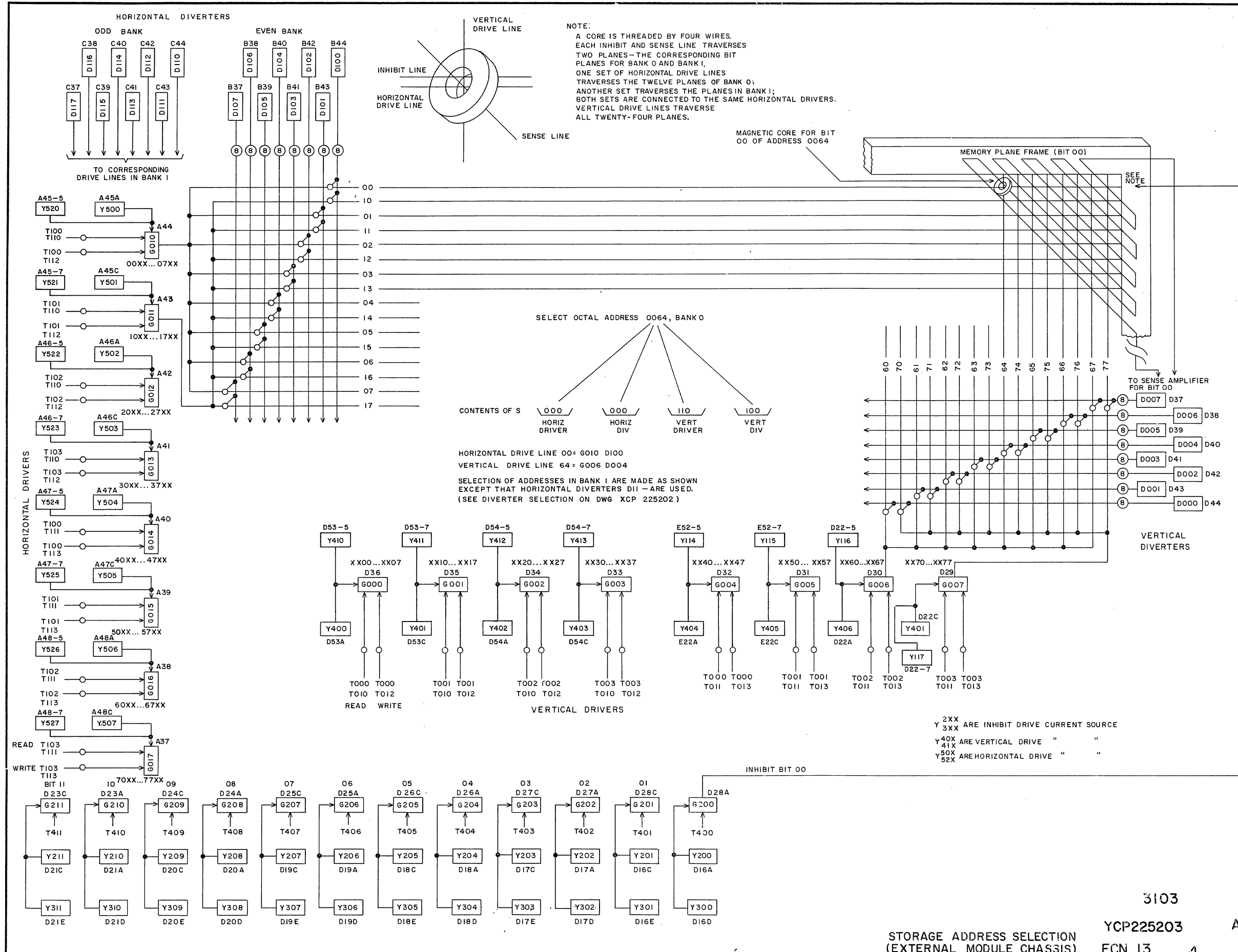
Y000 - Y110 ARE MEMORY SENSE AMPLIFIERS (TYPE 57)



REV. DATE APPROVED CHECKED DESIGNED DRAWN	REFERENCE DRAWINGS 1-26-62 3/8/64	CONTROL DATA CORPORATION COMPUTER DIVISION PRODUCT OR PRODUCT NUMBER 3103 DRAWING NUMBER YCP225201 TITLE S' INVERTERS & Z' REGISTER (EXTERNAL MODULE CHASSIS) ECN 15 PAGE 2
	COMPONENTS (UNLESS OTHERWISE INDICATED) TOLERANCE VALUE SIZE	
	RESISTORS CAPACITORS	
	FACTORY OR PRODUCT REV C	



NOTE:
 LOW-ORDER DIGIT IN DESTINATION SYMBOL SIGNIFIES
 MAGNITUDE OF DIVERTER LINE SELECTED. THUS
 D104,105= X4XX OR X5XX
 D106,107= X6XX OR X7XX
 OUTPUT DESIGNATIONS FROM T305 AND T205
 = XXX4, XXX5, XXX6, XXX7

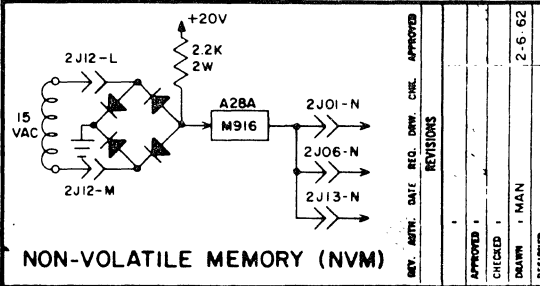
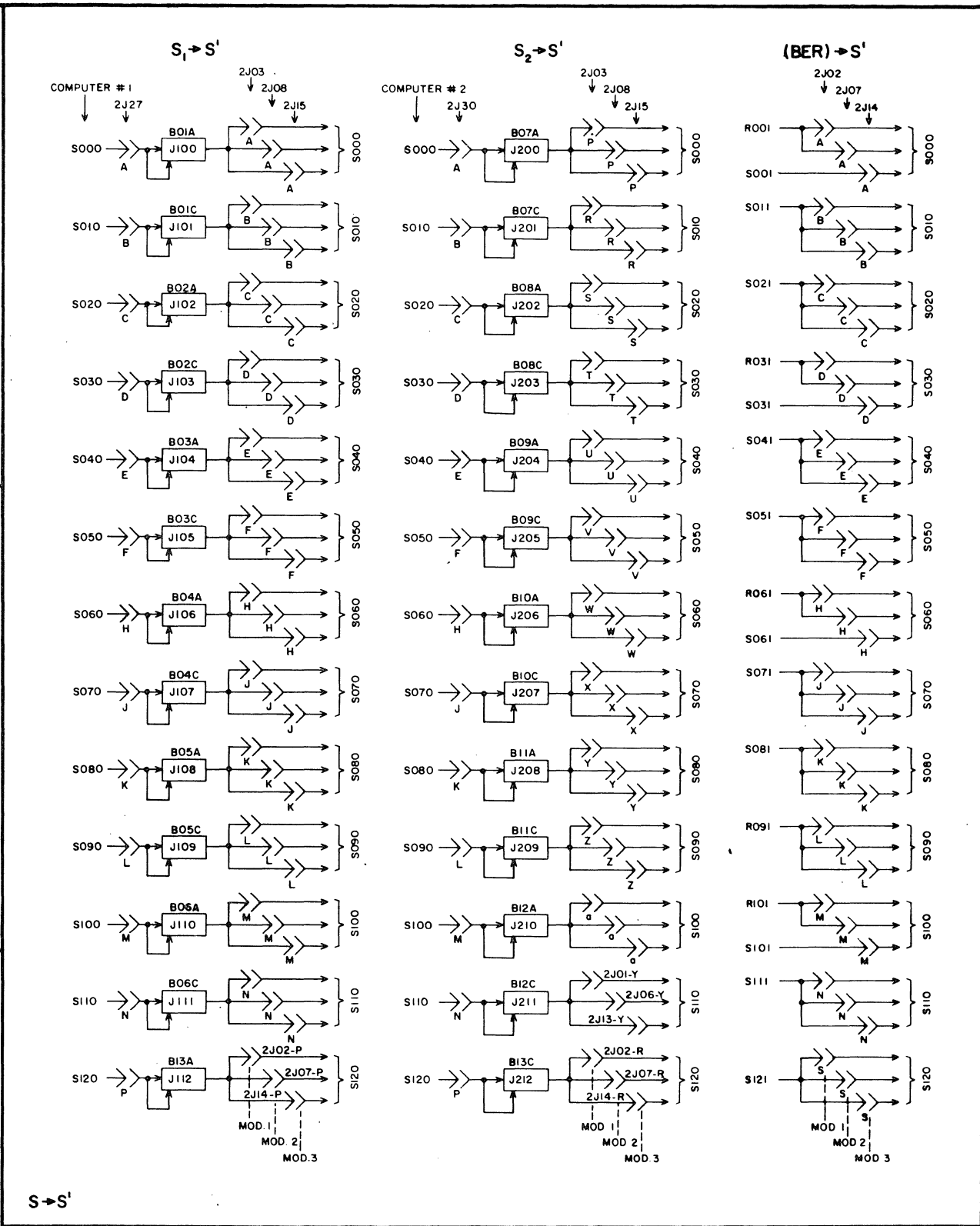
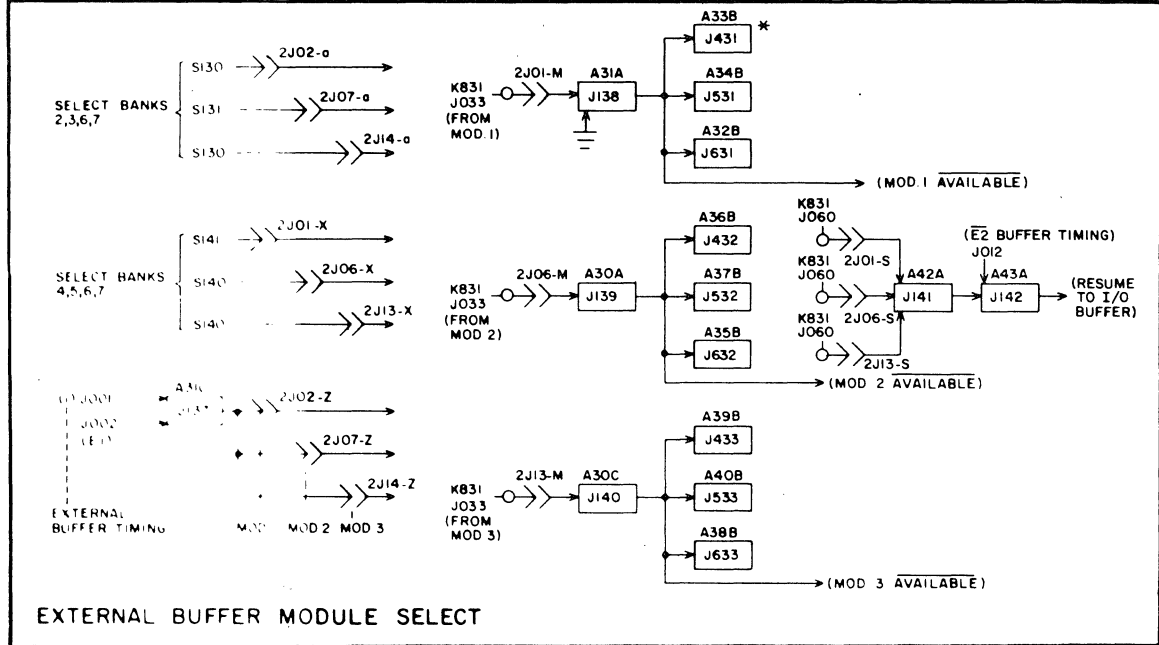
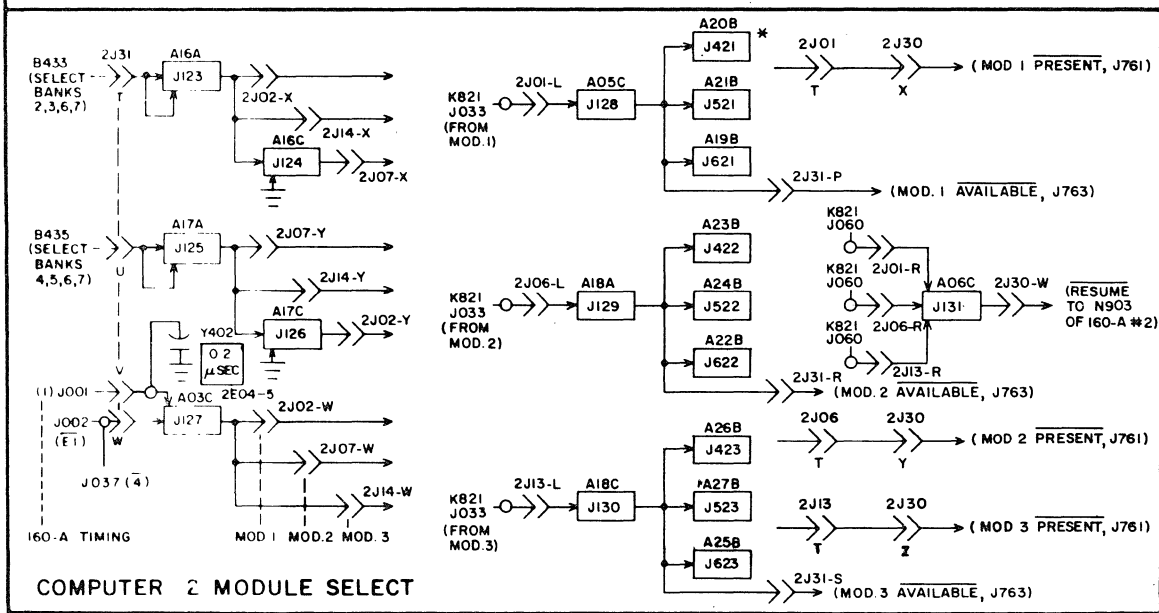
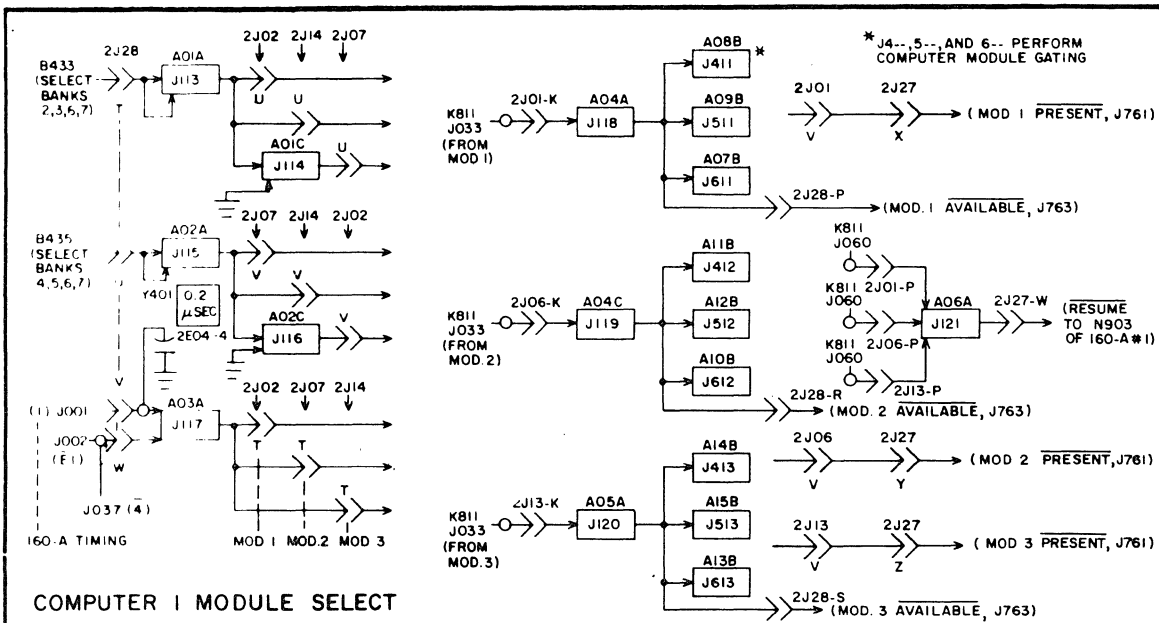


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STORAGE ADDRESS SELECTION
(EXTERNAL MODULE CHASSIS)

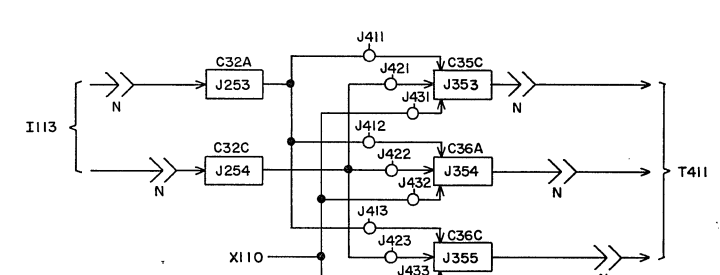
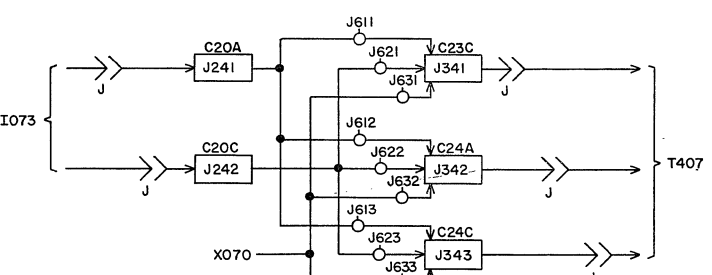
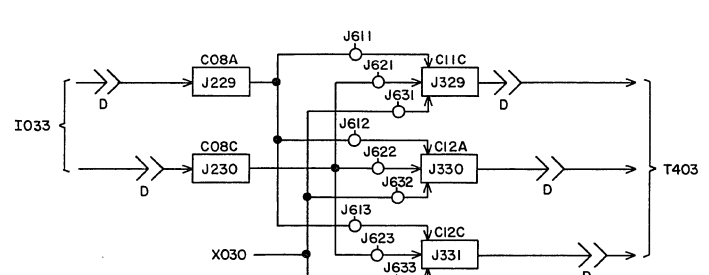
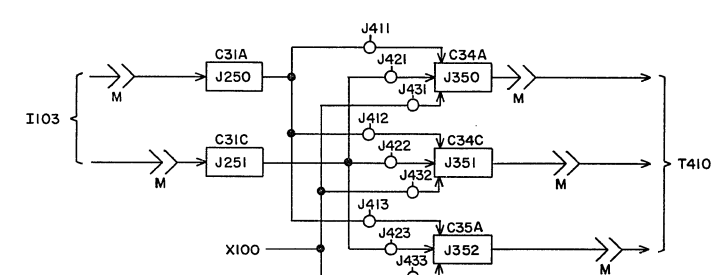
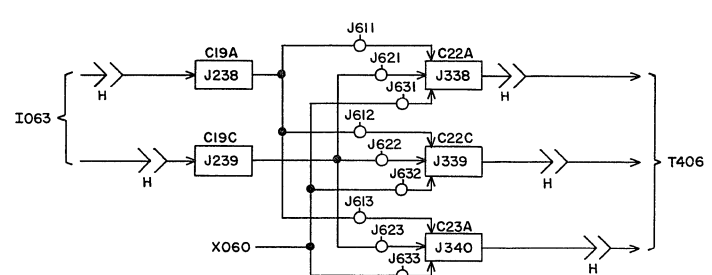
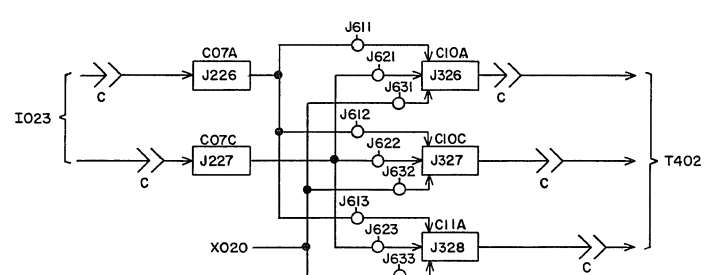
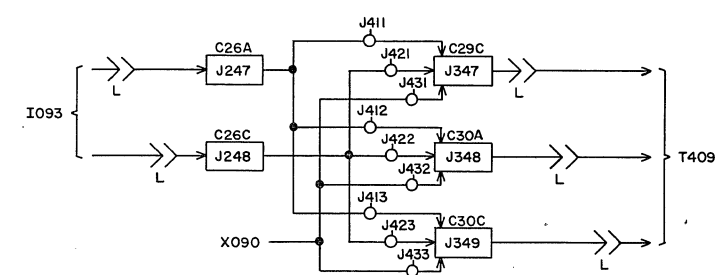
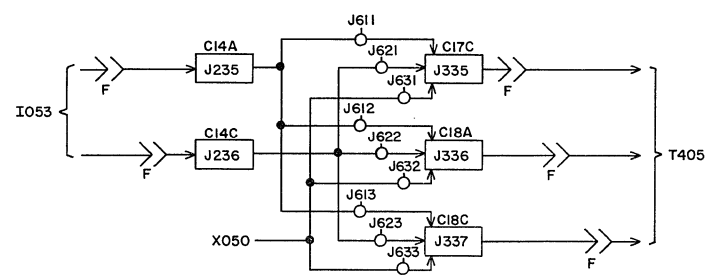
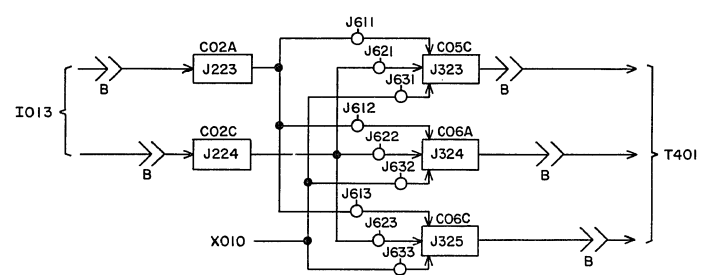
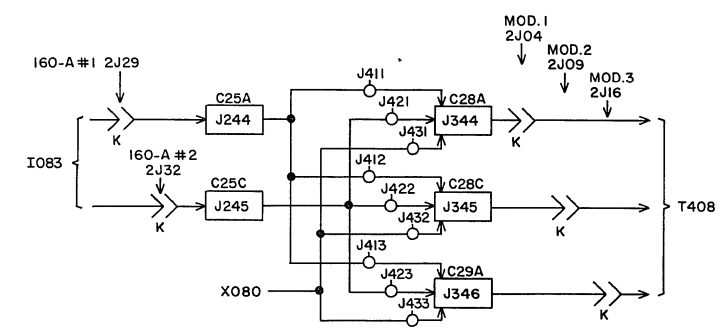
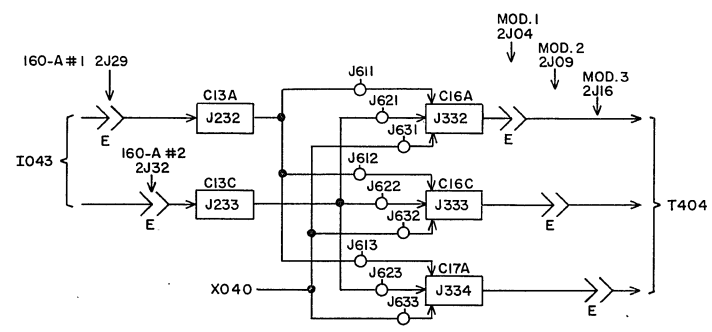
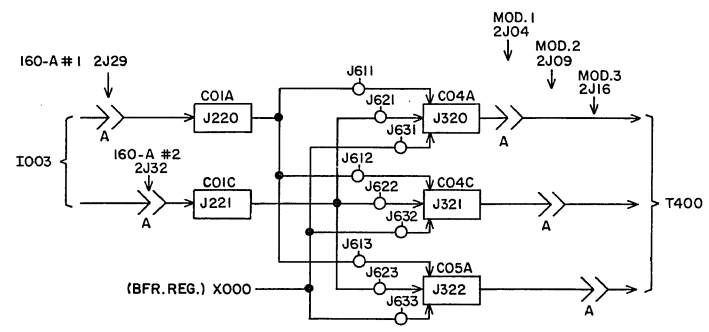
YCP225203
ECN 13

A



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CAPACITORS			
TITLE			
MODULE SELECT, S \rightarrow S', NVM (CONTROL CHASSIS)			

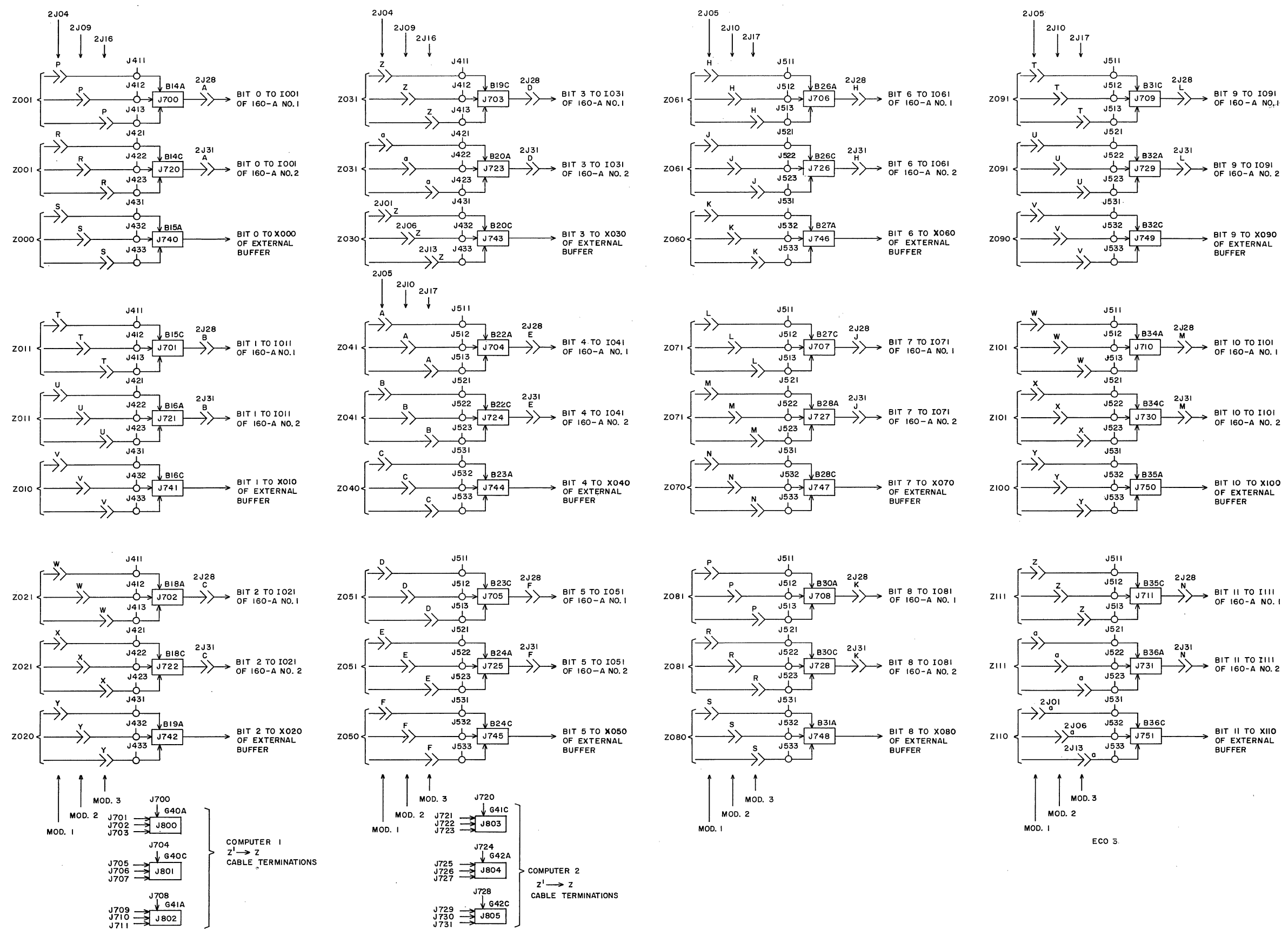
CONTROL DATA CORPORATION	
PROJECT OR PRODUCT	
169	
DRAWING NUMBER	
CP22520400	U
PAGE 5	



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YCP225205

Z → MOD'
(CONTROL CHASSIS)

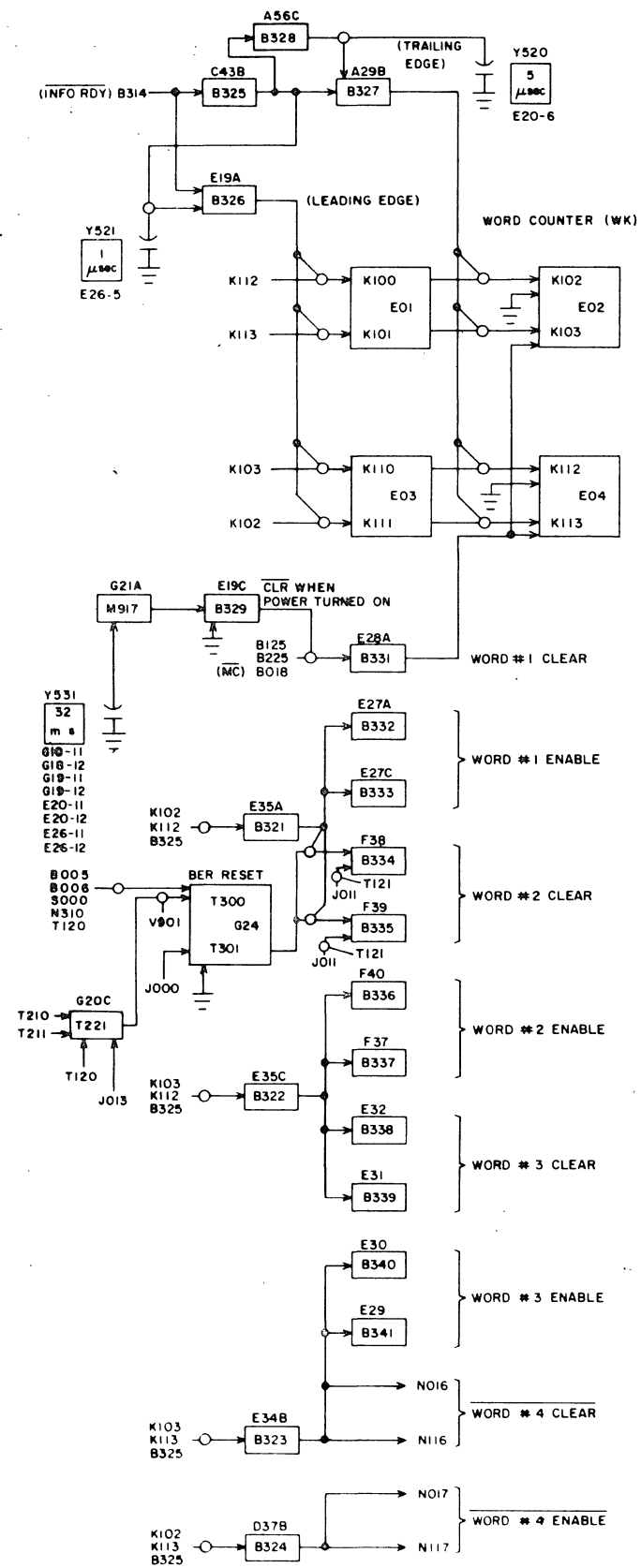


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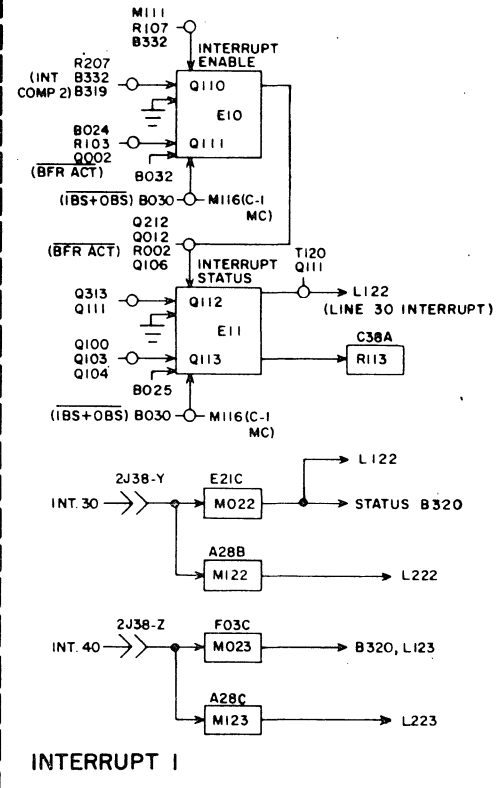
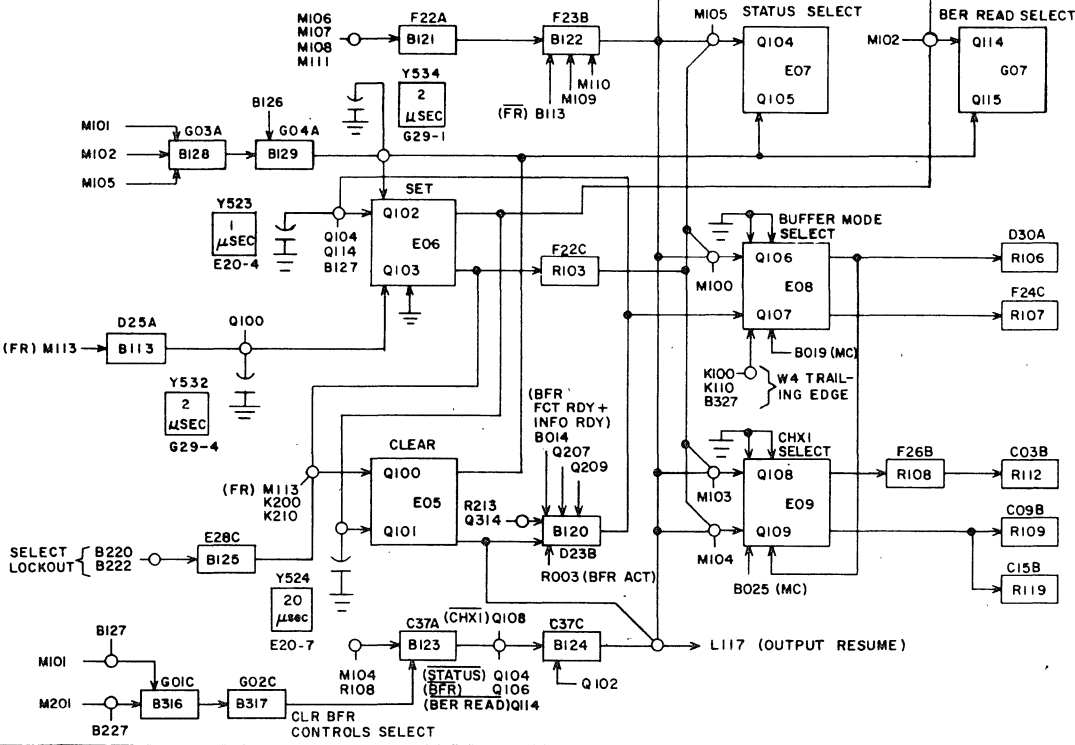
YCP225206

Z' → Z
(CONTROL CHASSIS)

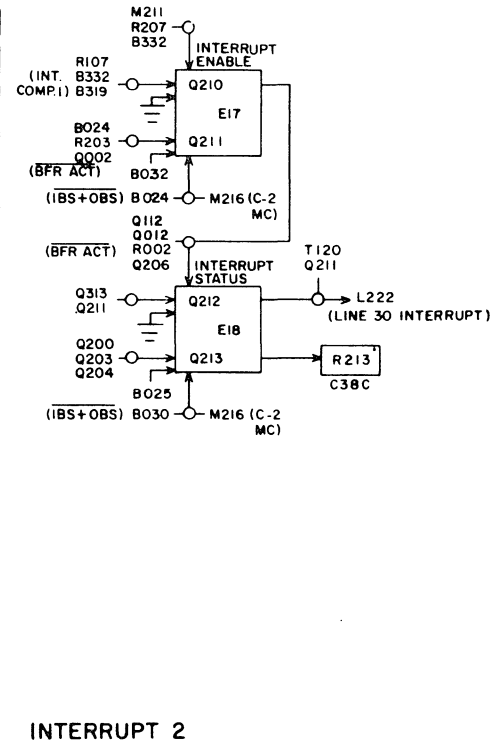
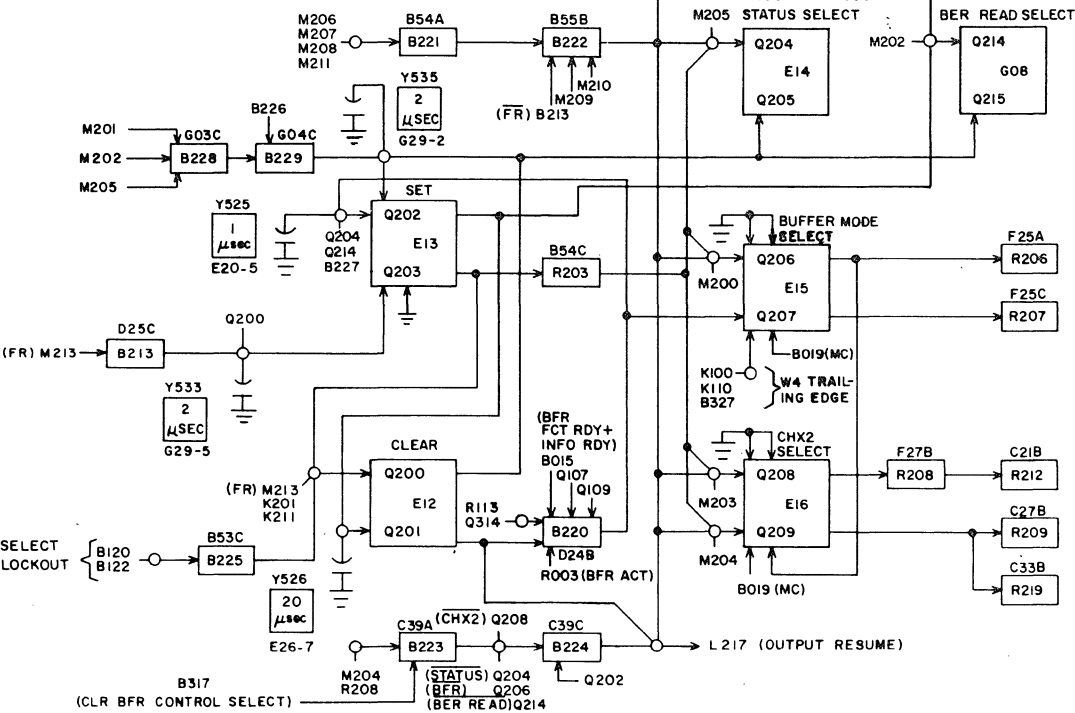
CONTROL WORD GATING



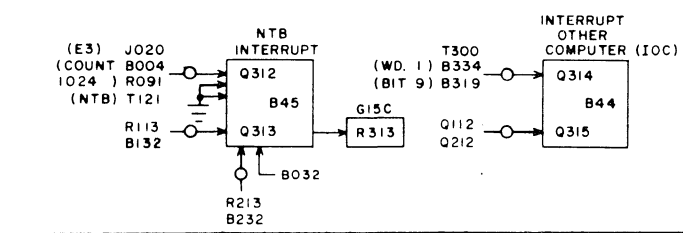
COMPUTER 1 BUFFER SELECT



COMPUTER 2 BUFFER SELECT



INTERRUPT (NTB, IOC)



APPROVED	DATE	REV.	CHK.	APP.

2-9-62

REVISIONS

REFERENCE DRAWINGS

COMPONENTS	UNLESS OTHERWISE INDICATED
TOLERANCE	VALUE
RESISTORS	VALUE
CAPACITORS	VALUE

TITLE: BUFFER SELECT, INTERRUPT, & CONTROL WORD GATING (CONTROL CHASSIS)

CONTROL DATA CORPORATION

PROJECT OR PRODUCT

3103

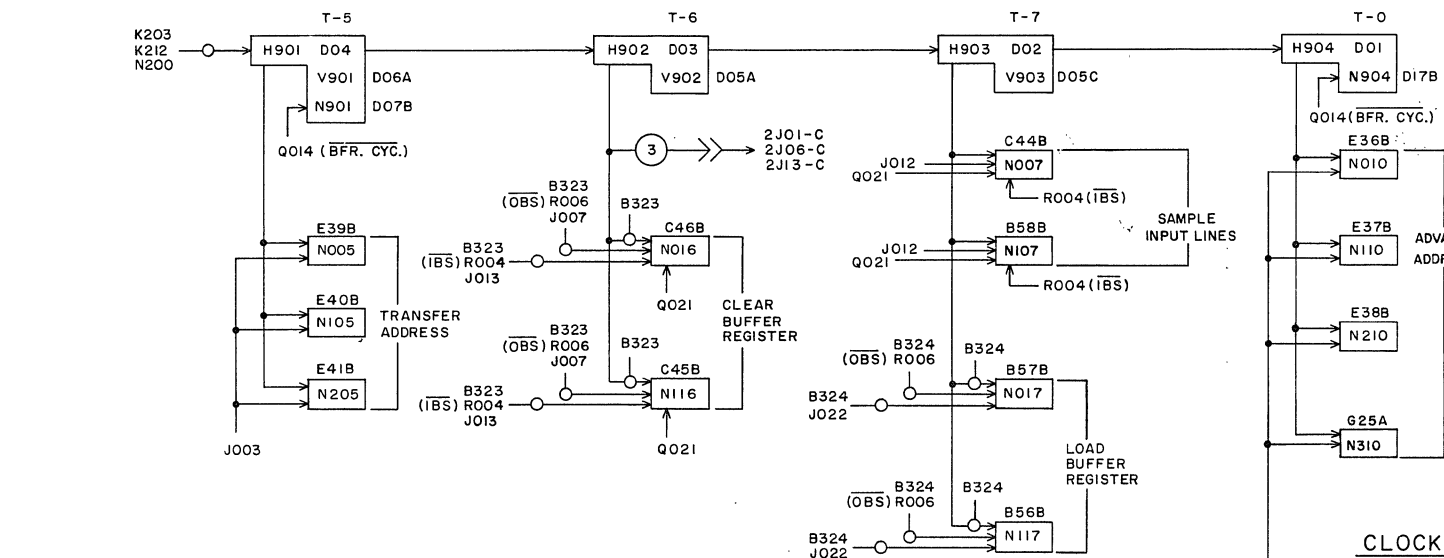
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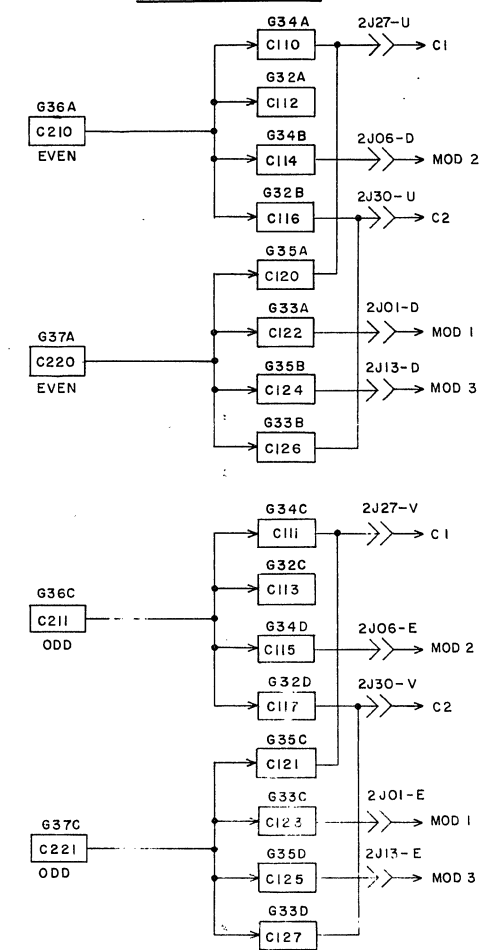
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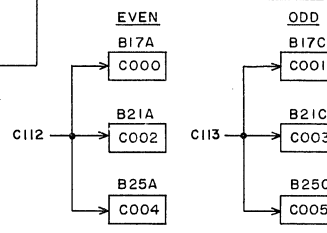
BUFFER TIMING CHAIN



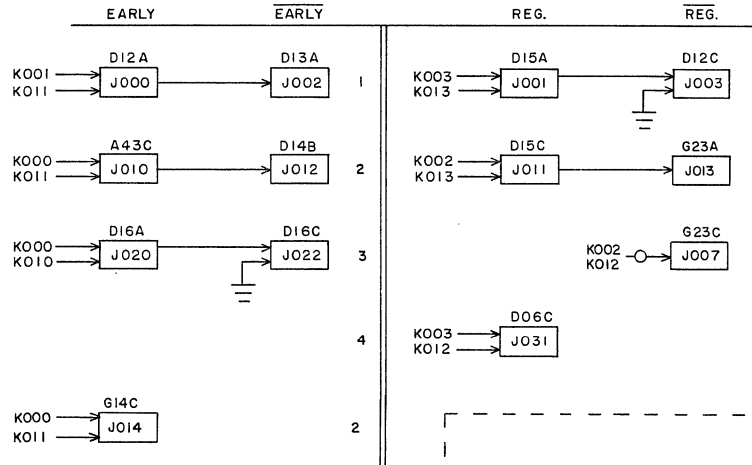
CLOCK PYRAMID



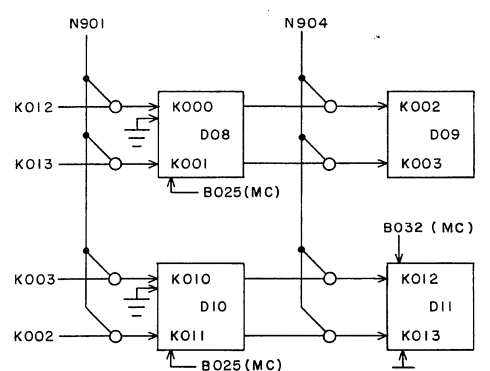
CLOCK TERMS



QUARTER TRANSLATIONS



RESYNC COUNTER (RK) REFLECTED BINARY CODE



QUARTER COUNTER (REFLECTED BINARY CODE)



3103

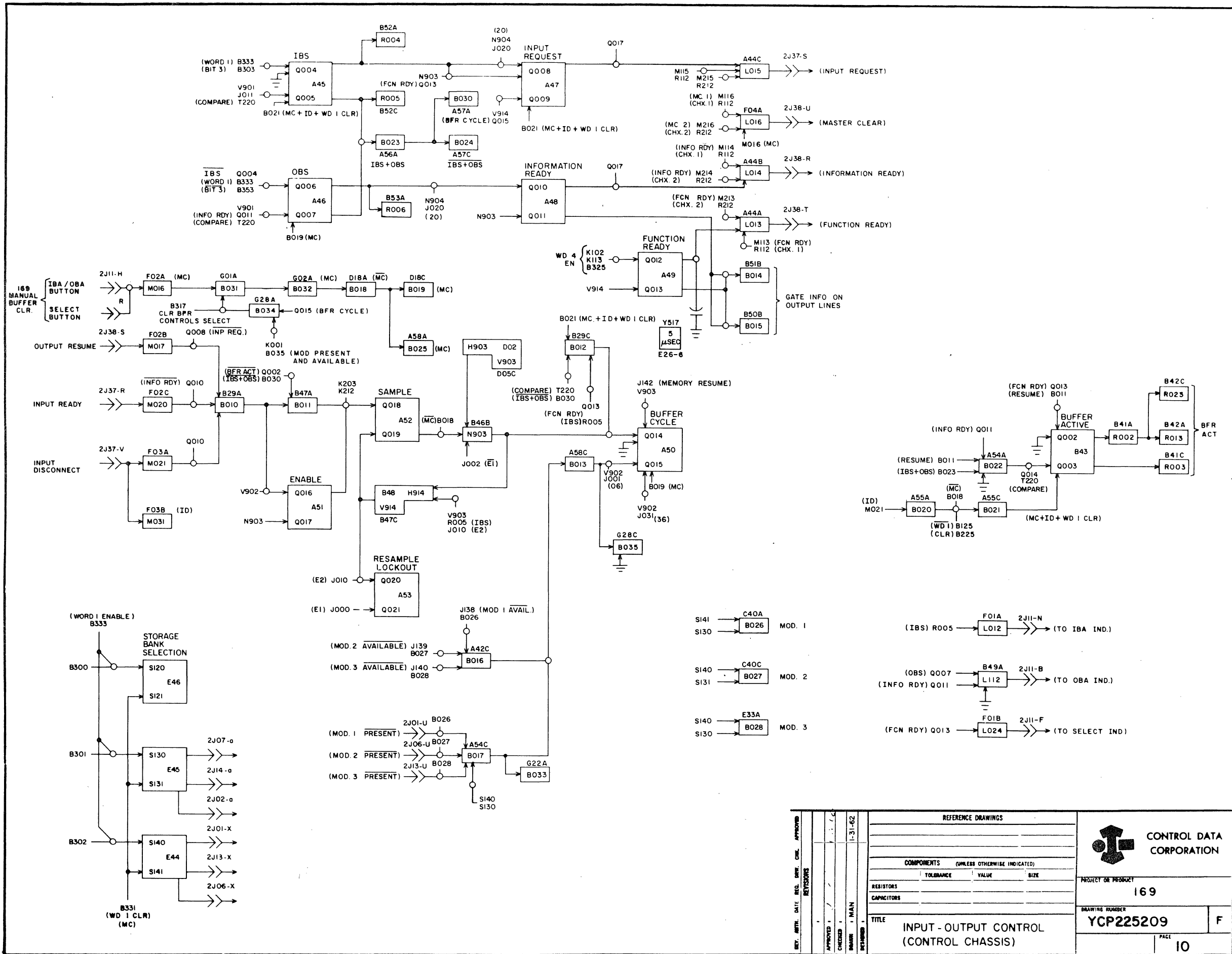
EXT BFR TIMING CONTROLS
(CONTROL CHASSIS)

YCP225208

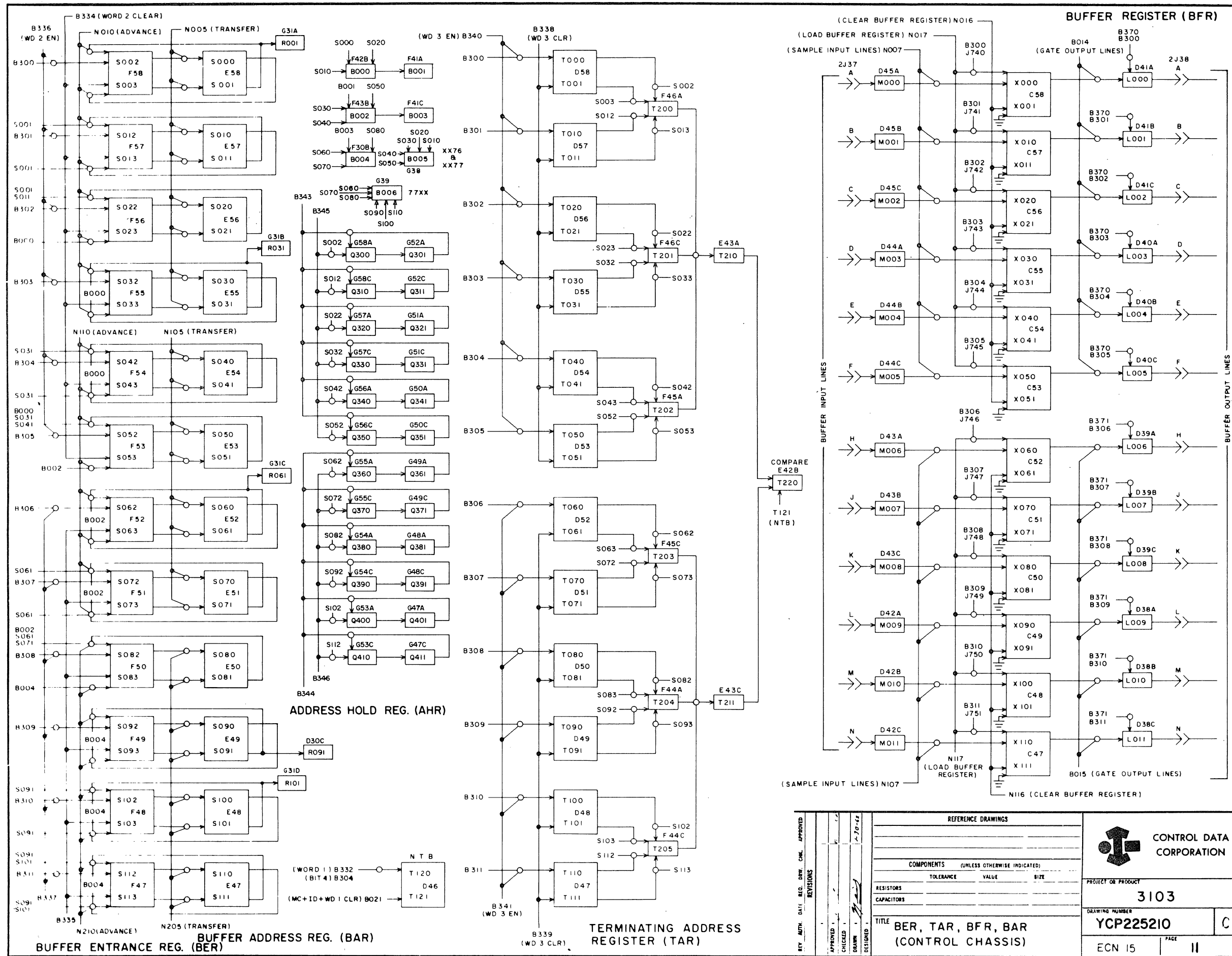
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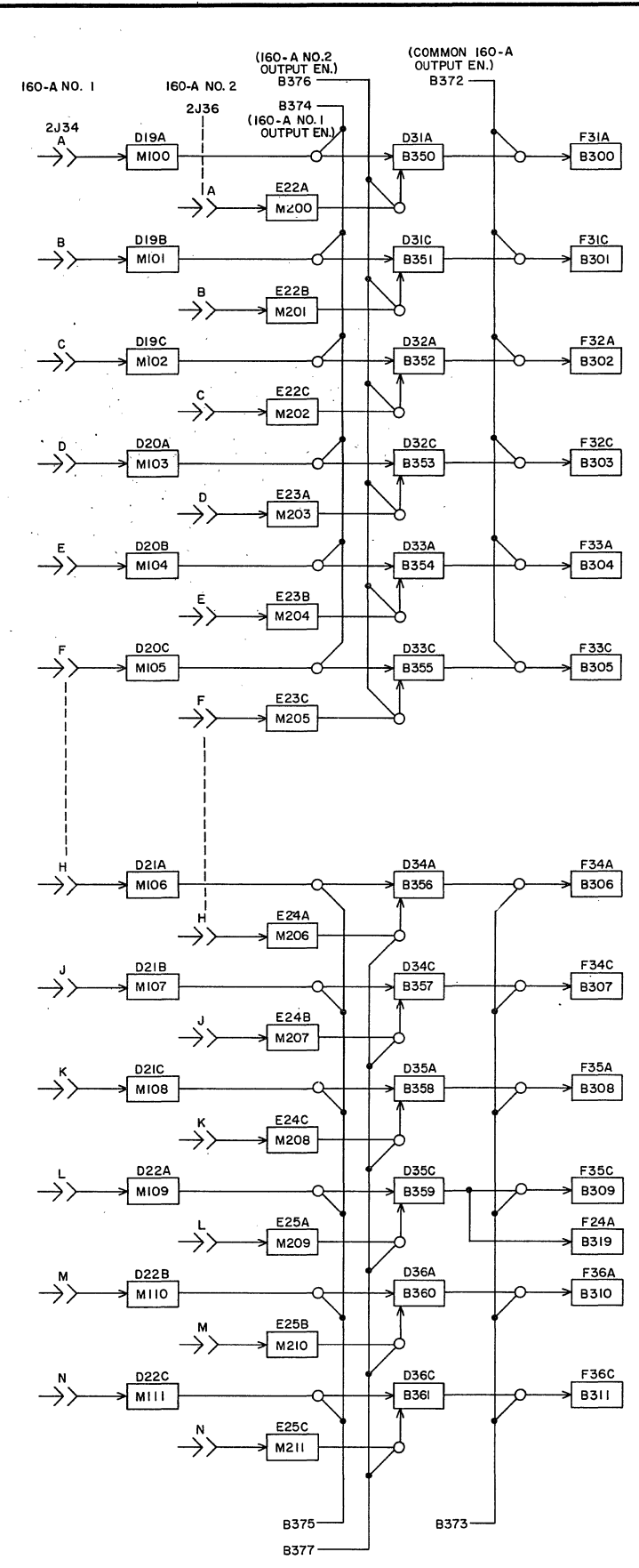
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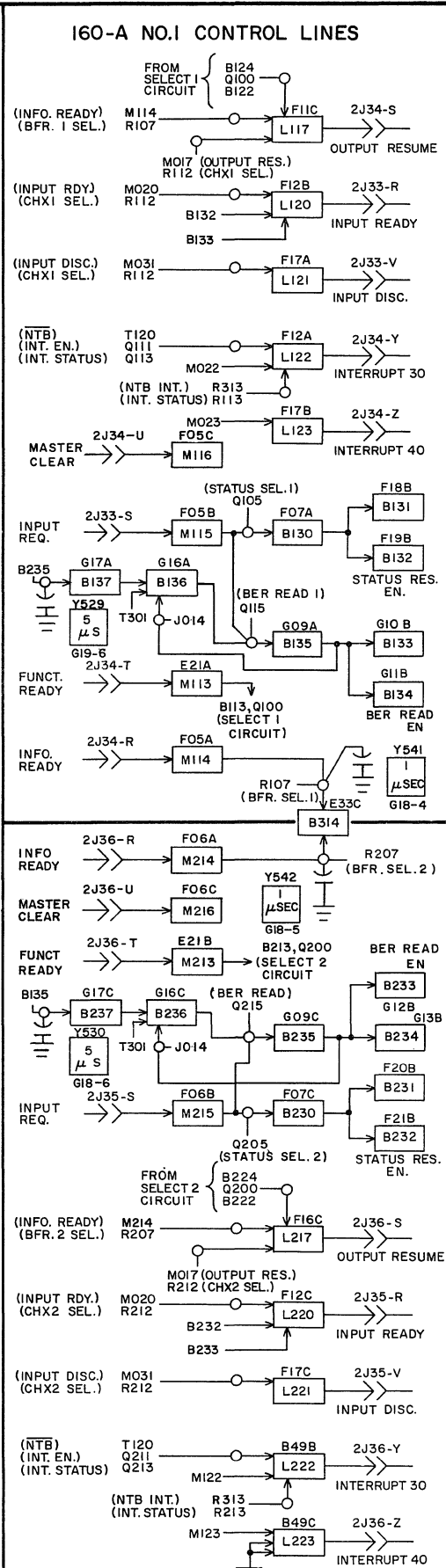
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RESISTORS	TOLERANCE	VALUE	SIZE
CAPACITORS			
TITLE		DRAWING NUMBER	
INPUT-OUTPUT CONTROL (CONTROL CHASSIS)		YCP225209	
		PAGE 10	



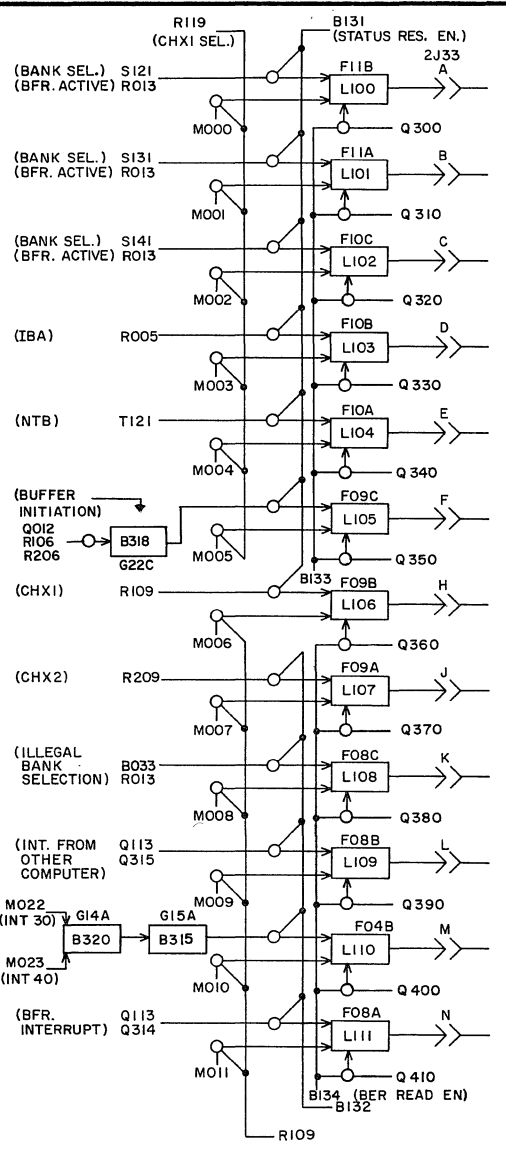
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		COMPONENTS (UNLESS OTHERWISE INDICATED) TOLERANCE VALUE SIZE RESISTORS CAPACITORS
		TITLE BER, TAR, BFR, BAR (CONTROL CHASSIS)
		ECN 15 PAGE 11



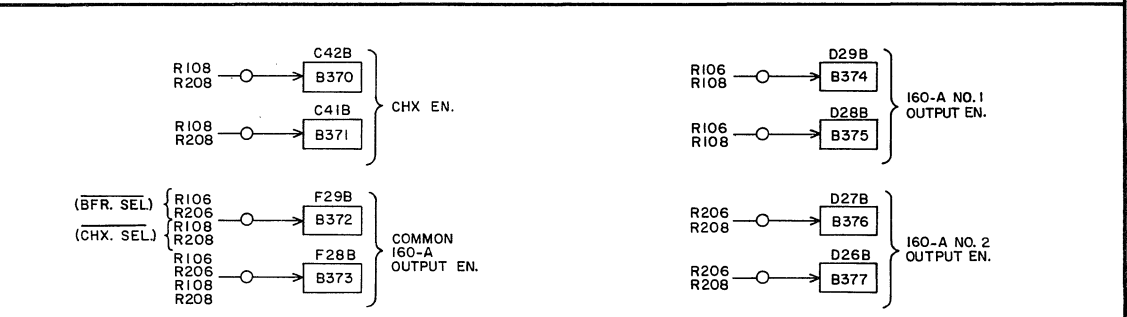
160-A OUTPUT CABLE CONNECTORS



160-A NO. 2 CONTROL LINES



160-A INPUT CABLE CONNECTIONS



ENABLES FOR OUTPUT CABLE CONNECTORS

160-A I/O CABLE CONNECTIONS AND CONTROL LINES (CONTROL CHASSIS)

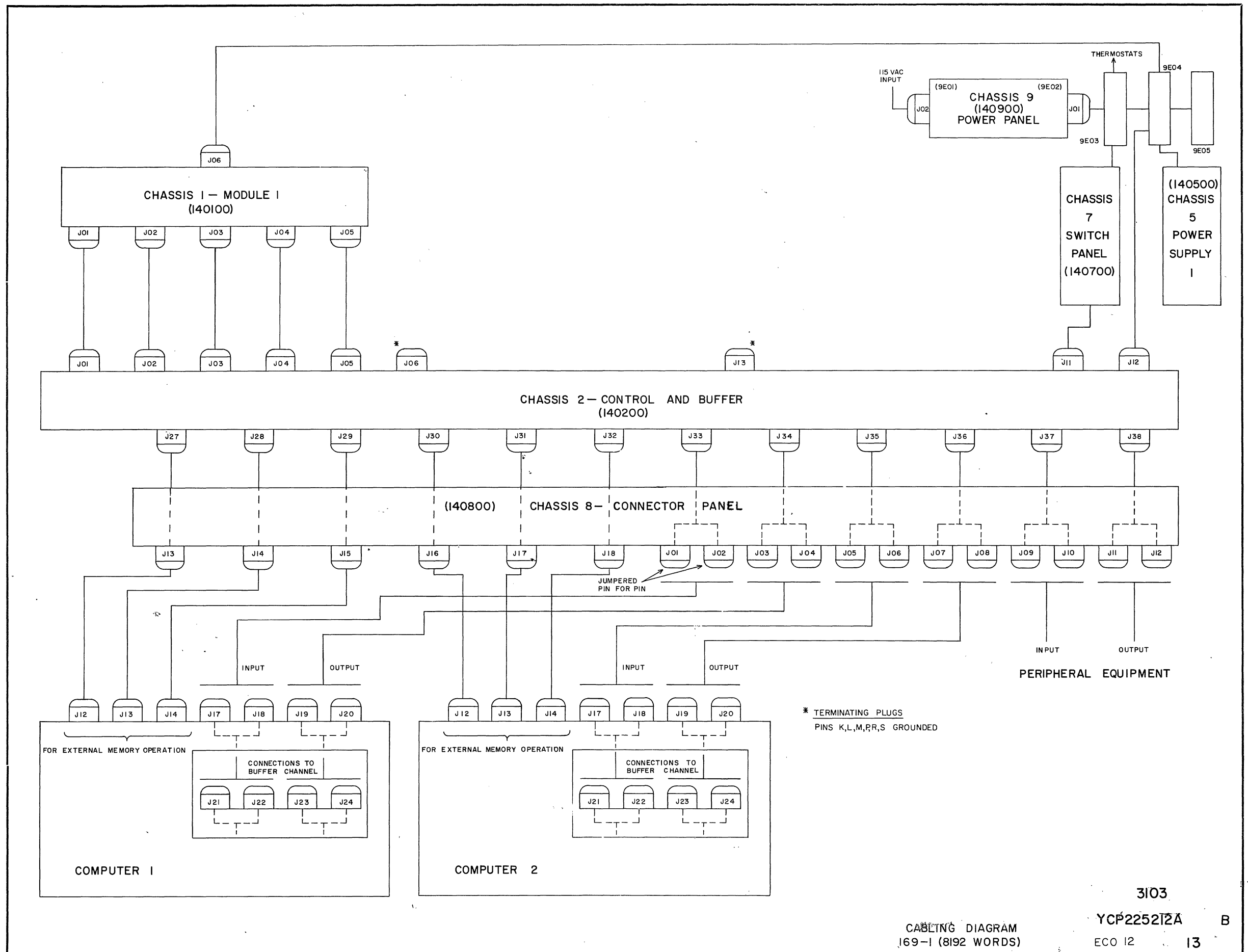
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YCP2252 11

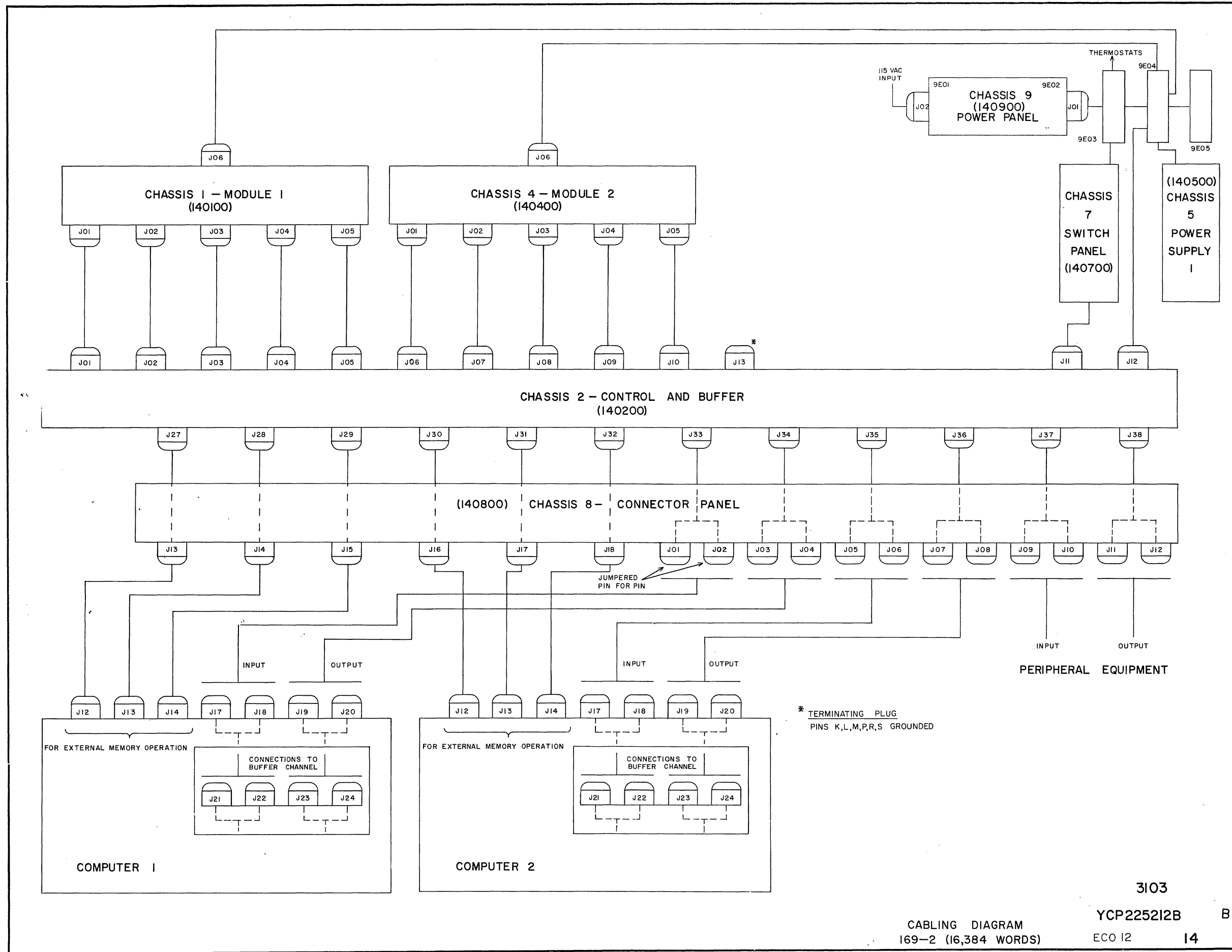
ECO 8

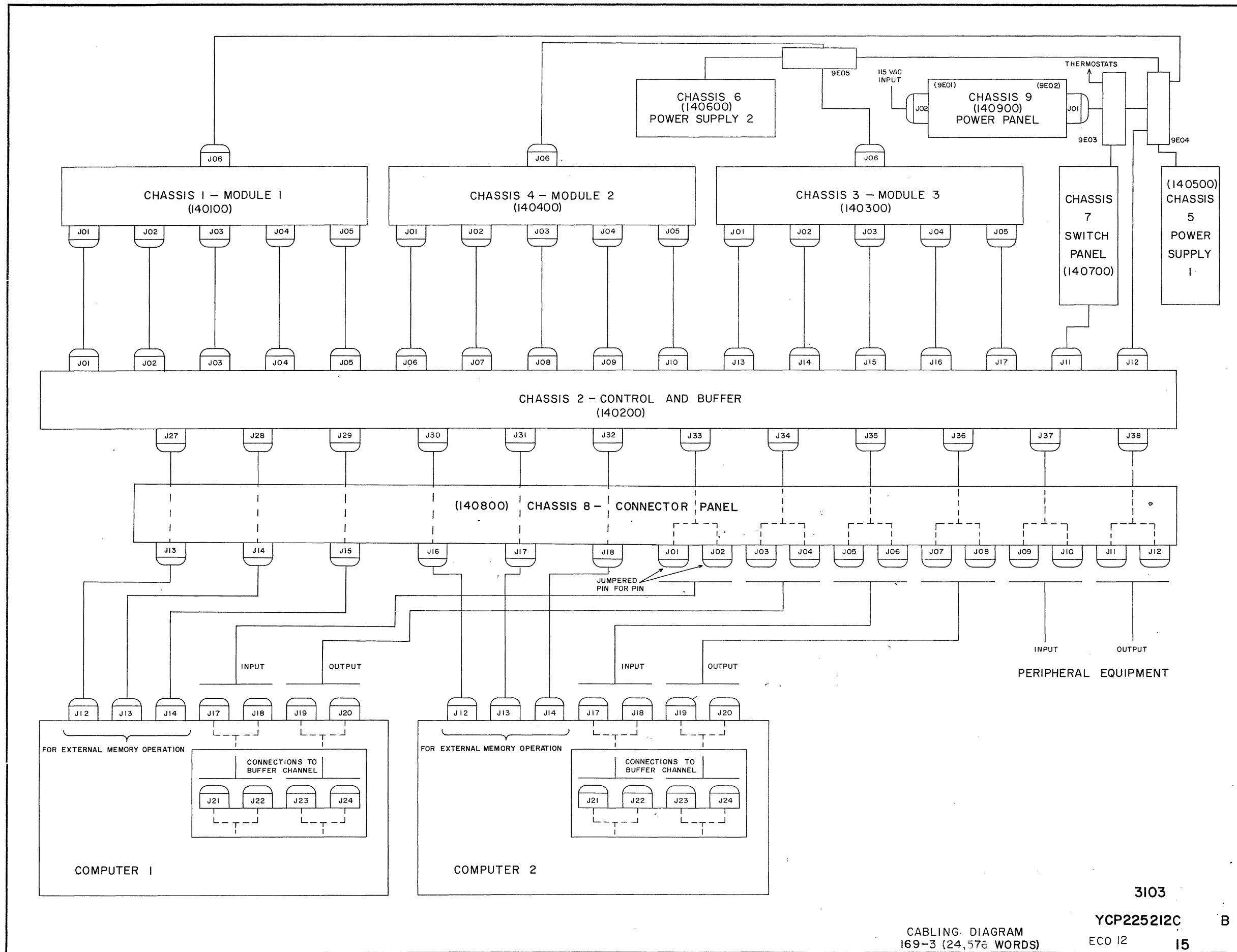
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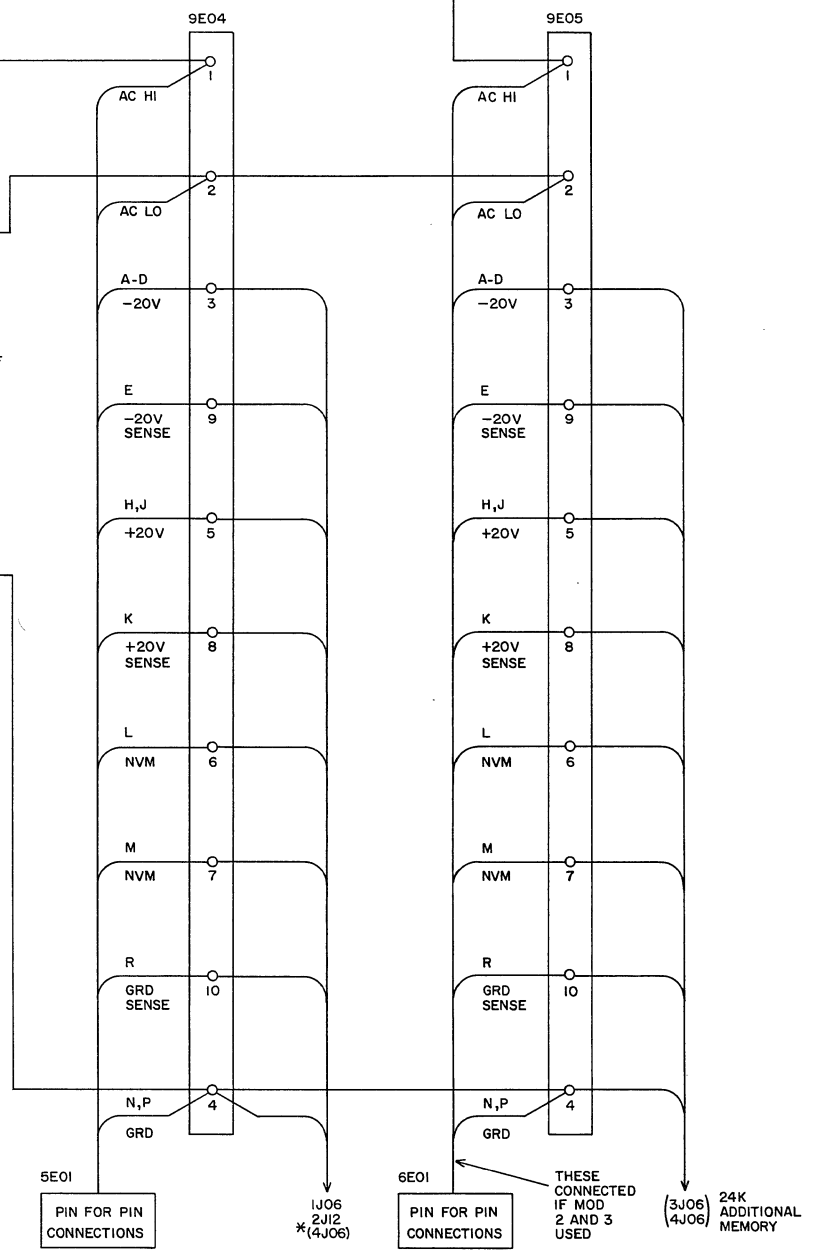
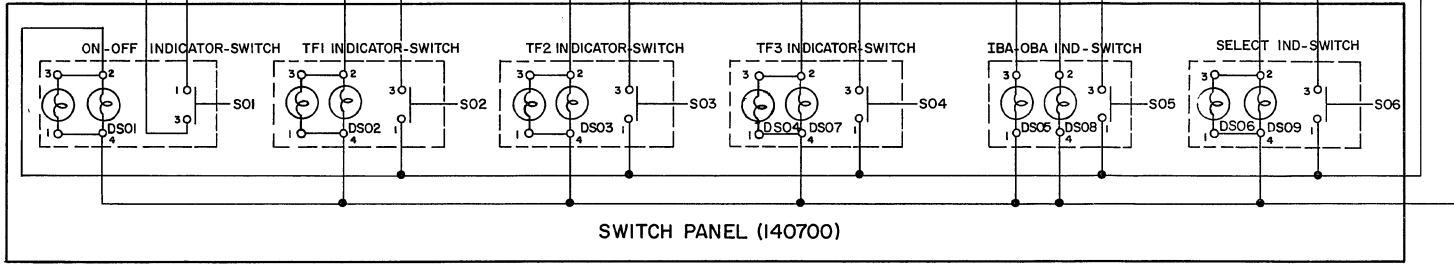
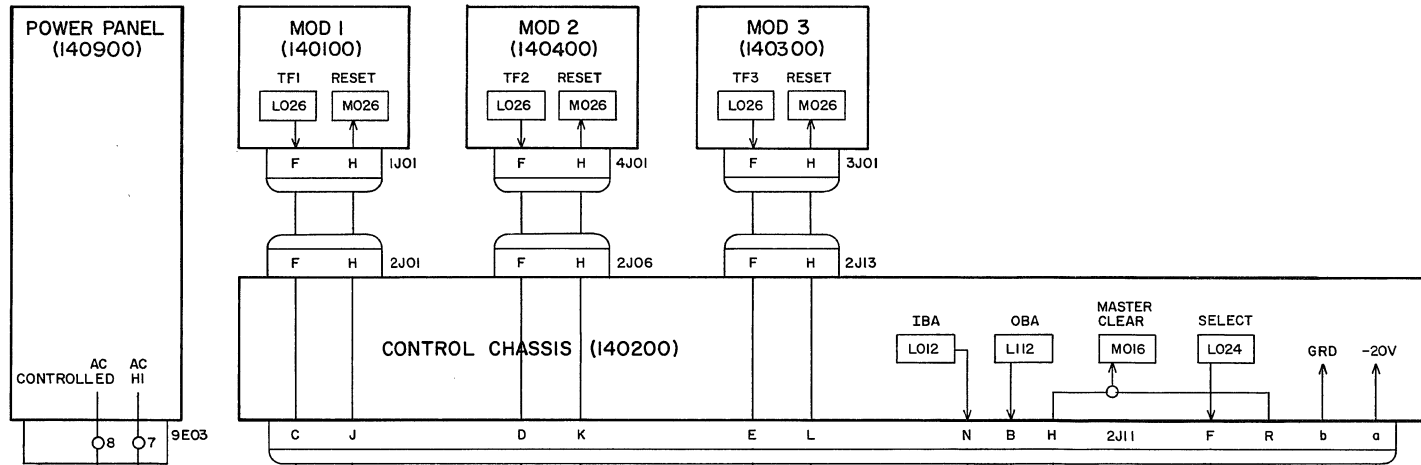
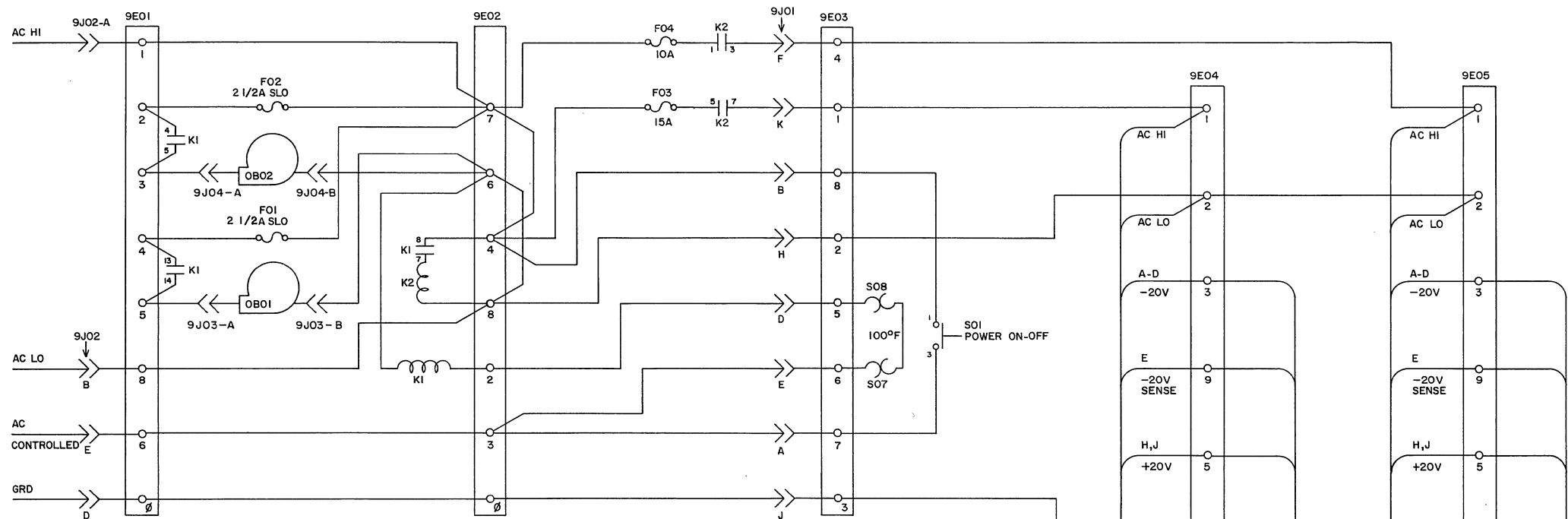
B



* TERMINATING PLUGS
PINS K,L,M,PR,S GROUNDED







COMMENT SHEET

MANUAL TITLE 169 AUXILIARY MEMORY UNIT

PUBLICATION NO. 60022300 REVISION _____

FROM: NAME: _____
BUSINESS ADDRESS: _____

COMMENTS:

This form is not intended to be used as an order blank. Your evaluation of this manual will be welcomed by Control Data Corporation. Any errors, suggested additions or deletions, or general comments may be made below. Please include page number references and fill in publication revision level as shown by the last entry on the Record of Revision page at the front of the manual. Customer engineers are urged to use the TAR.

CUT ALONG LINE

FORM CA231 REV. 1-67 PRINTED IN U.S.A.

NO POSTAGE STAMP NECESSARY IF MAILED IN U. S. A.
FOLD ON DOTTED LINES AND STAPLE

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PUBLICATION NO. 60022300 REVISION _____

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APLE

ST.

APLE

FOLD

FOLD

FOLD

FOLD

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 MINNEAPOLIS, MINN.

BUSINESS REPLY MAIL
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MINNEAPOLIS, MINNESOTA 55440

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PLANT TWO



CUT ALONG LINE

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FOLD

FOLD

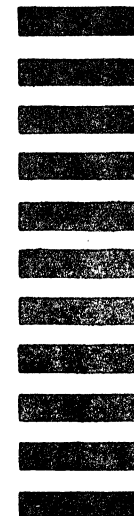
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