Customer Engineering Diagrams

CONTROL DATA® 160-A COMPUTER

Pub. No. 60014200
October, 1965

Printed in the United States of America

60014200

RECORD OF REVISIONS

REVISION	NOTES
J	ECN 39 and corrections: pages 1 through 21 affected.
K	ECN's 40 and 41: pages 1, 2A, 2B and 16 affected.
L	Change Order 8936, Product Designation 160A-A44 (the 44th change). Pages 16 and 20 revised.
(Reprint) (4-6-65)	Title block and zoning changes only. This printing does not obsolete previous editions.
M (8-19-65)	Change Order 11004, new Product Designation 160-A45. Page 19 revised.
N (9-2-65)	Change Order 11276, new Product Designation 160-A46. Page 6 revised. Misc. correction on page 19.
P (3-23-66)	Field Change Order 12661, new Product Designation 160-A47. Page 16 and 20 revised.

FORM CA 109

CONTENTS

KEY TO LOGIC SYMBOLS

(STANDARD 1604 OR 3600 CARD TYPES)

Logic diagrams represent a symbolic approach to electronic schematics. By using symbols to represent building block circuits, the schematic becomes easy to read if the reader understands the function of the symbols. In CONTROL DATA Corporation logic, two signals, a logical "0" and a logical "1", are the possible input or output conditions of a circuit. A circuit with an output of "1" is "up" and a circuit with an output of "0" is "down". Detailed descriptions of logic symbols and their associated building block circuit cards are contained in the Printed Circuit Card Manual (Pub. No. 60042900).

STANDARD LOGIC SYMBOLS

Standard logic diagram symbols for CONTROL DATA equipment using 1604- or 3600-type cards are inverters, flip-flops, control delays, and capacitive and inductive delays.

Inverters

An inverter is a logic element which provides an output that is an inversion of its input. When more than one input is provided to an inverter, 1's take precedence over 0's and drive the output of the inverter to "0". Because any "1" input of several inputs drives the output to a "0", an inverter may be considered an inverting OR (or NOR) gate when more than one input is present.

Inverters are shown in the logic diagrams as rectangles (Figure 1). J001 and J002 are arbitrarily-assigned term numbers which designate these specific inverters. Note that the output of J002 is "0" if input A, or input B or input C is a "1".

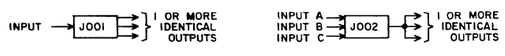


Figure 1. Inverter Symbols

Acceptable conventions for showing multiple OR inputs are given in Figure 2.

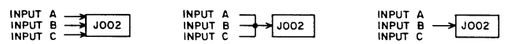


Figure 2. OR Circuit Conventions

Flip-Flops (FF)

The flip-flop (FF) is a storage device with two stable states - designated as Set and Clear - and is composed of two or more inverters. The logic symbols (Figure 3) are formed by the combination of inverter symbols. By convention, Set inputs and outputs are shown in the upper part of the symbol and Clear inputs and outputs are shown in the lower part of the symbol.

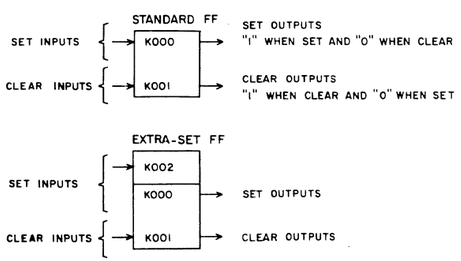


Figure 3. Flip-Flop Symbols

Figure 4 illustrates the interconnection of inverter symbols to form a flip-flop symbol. The term numbers assigned to each flip-flop are the term numbers of the internal inverters as seen by comparing the terms in Figure 3 with those in Figure 4. Notice that the Set output is the output of inverter K001, and the Clear output is the output of inverters K000 and K002.

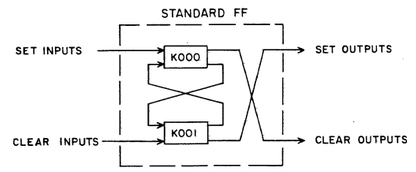


Figure 4. Internal Inverter Connections for a Flip-Flop

AND Gate

An AND gate requires that all its inputs be 1's in order that its output be a "1". If one or more of the inputs to an AND gate are "0", the output is a "0". Figure 5 illustrates conventions for showing AND gates feeding an inverter.

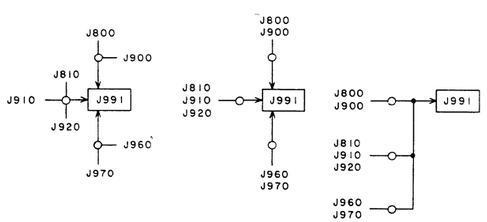


Figure 5. AND Circuit Conventions

Control Delay

A control delay is a timing device consisting of an H term which receives the input and one or more V, Y, or N terms to provide the outputs. The H term is essentially a flip-flop with controlled feedback and occupies an entire printed circuit card. The output term(s) are inverter(s) located elsewhere on the logic chassis. The "1" outputs from a control delay are clocked pulses which are delayed one phase time from the "1" inputs. Clock inputs are not shown on the logic diagrams for any H, V, Y, or N terms; these terms, which control the start and duration of the delayed output pulses, may be found in the Equation Summary. Figure 6 illustrates two representative forms of the control delay symbol, with possible inputs and outputs labelled. Figure 7 shows the electrical connections for the two forms.

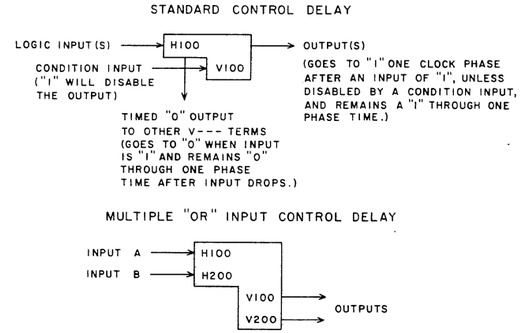


Figure 6. Control Delay Symbols

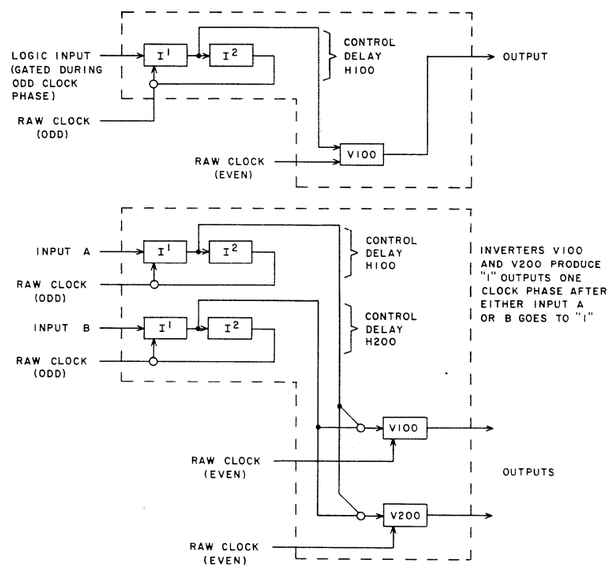


Figure 7. Electrical Connections for Control Delay

Control delays may have multiple inputs and/or multiple outputs. When a control delay has multiple output terms (i.e., more than one V, Y, or N term), each output term may have a separate conditioning input.

Capacitive Delays

A capacitive delay is used to delay the input to a logic element. Capacitive delays may be active or passive, depending upon whether or not transistors are used as part of the delaying circuit. Delay periods are checked by using a dual-trace scope connected to the input and output of the delay-producing element. The actual connection points for the scope probes will vary for different cards and should be determined by referring to the Printed Circuit Manual, Pub. No. 60042900 (Volume 2).

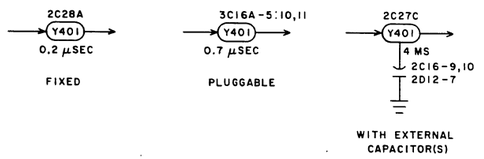


Figure 8. Active Capacitive Delays

Active delays may be recognized by the circuit letter always present as part of the card location. Pin numbers are also shown when external wiring is needed to connect the proper capacitance. In Figure 8, the pluggable delay uses this wiring to connect to capacitors on the same card. In the third example, this wiring connects to capacitors located on two separate capacitor cards.

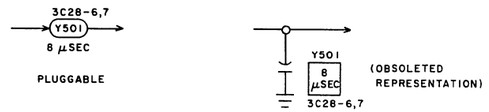


Figure 9. Passive Capacitive Delays

All passive capacitive delays (Figure 9) are formed by wiring grounded capacitors, located on one or more capacitor cards, as an AND input to the affected logic element. For this reason, all passive delays show pin numbers to provide this external wiring data.

Figure 10. Adjustable Capacitive Delays

Capacitive delays may be adjustable or non-adjustable, depending on the card type and/or the external wiring connections on the card. When it is necessary to adjust the delay period in order to obtain specified circuit operation (usually done by varying a potentiometer in the RC network), a diagonal arrow is added to the delay symbol as shown in Figure 10.

Inductive Delays

An inductive delay is used to delay the input to a logic element or as a tapped delay line for timing of operations. The symbol for this delay is an elongated oval with a double vertical line just within the input end of the oval. When used as a tapped delay line, the inductive delay is terminated in its characteristic impedance. Inductive delays are identified in the same manner as capacitive delays (except for the vertical lines) unless they are used as delay lines. On multi-section cards where no identifying circuit letters are present, pin numbers are shown adjacent to the input and output arrows. Figure 11 shows both kinds of inductive delays.

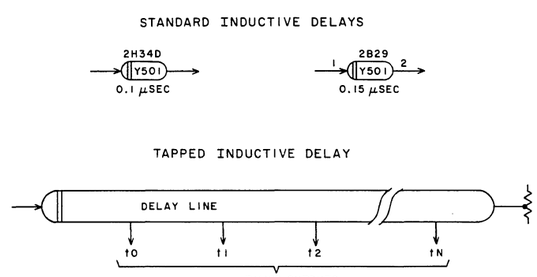


Figure 11. Inductive Delays

Line Drivers/Receivers

Voltage levels used to represent 1's and 0's on cables are different from those used for internal logic. The level shift to and from internal logic is made by line drivers and line receivers. These cards may be considered as inverting the signal electrically, but not logically. The letters commonly associated with these cards are L & M (1604) and R & T (3000 Series). A 3000 Series Receiver may also be used to perform a logical inversion by swapping the twisted pair wires. This usage is indicated by a circle on the input side of the symbol. In Figure 12, 1's and 0's have been added to clarify the logic states - they are not part of the symbol.

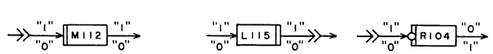


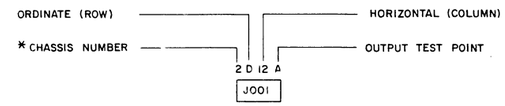
Figure 12. Typical Line Driver/Receiver Symbols

NON-LOGIC CONVENTION

The use of the double vertical bar, as in Figure 12, denotes a shift in signal voltage level from that used in internal logic. The double bar appears on the input or output side of the symbol, depending on which side connects to the non-logic-level signal. No particular voltage level is implied by the double bar; only that it is non-logic.

JACK ASSIGNMENTS

Each numbered term in the logic diagrams contains a jack assignment showing the physical location of that hardware element, and the test point (circuit section) associated with it. For some card types, the test point letter is replaced by a pin number. For these cases, a card extender must be used in order to test that section of the card. Also, some single inverters show no test point - test point A is assumed in these cases. Figure 13 illustrates the inverter J001, with 2D12A representing its jack assignment.

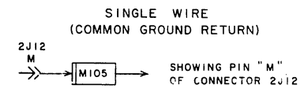


* When most or all jack assignments are located on one chassis, the chassis numbers for that chassis are omitted.

Figure 13. Jack Assignment Scheme

CABLE IDENTIFICATION

Cable connections are represented by the MIL STD-15 symbol and identified as to connector location and pins used, as shown in Figure 14.



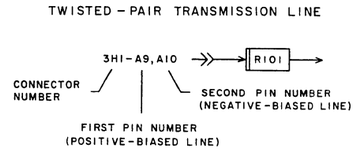
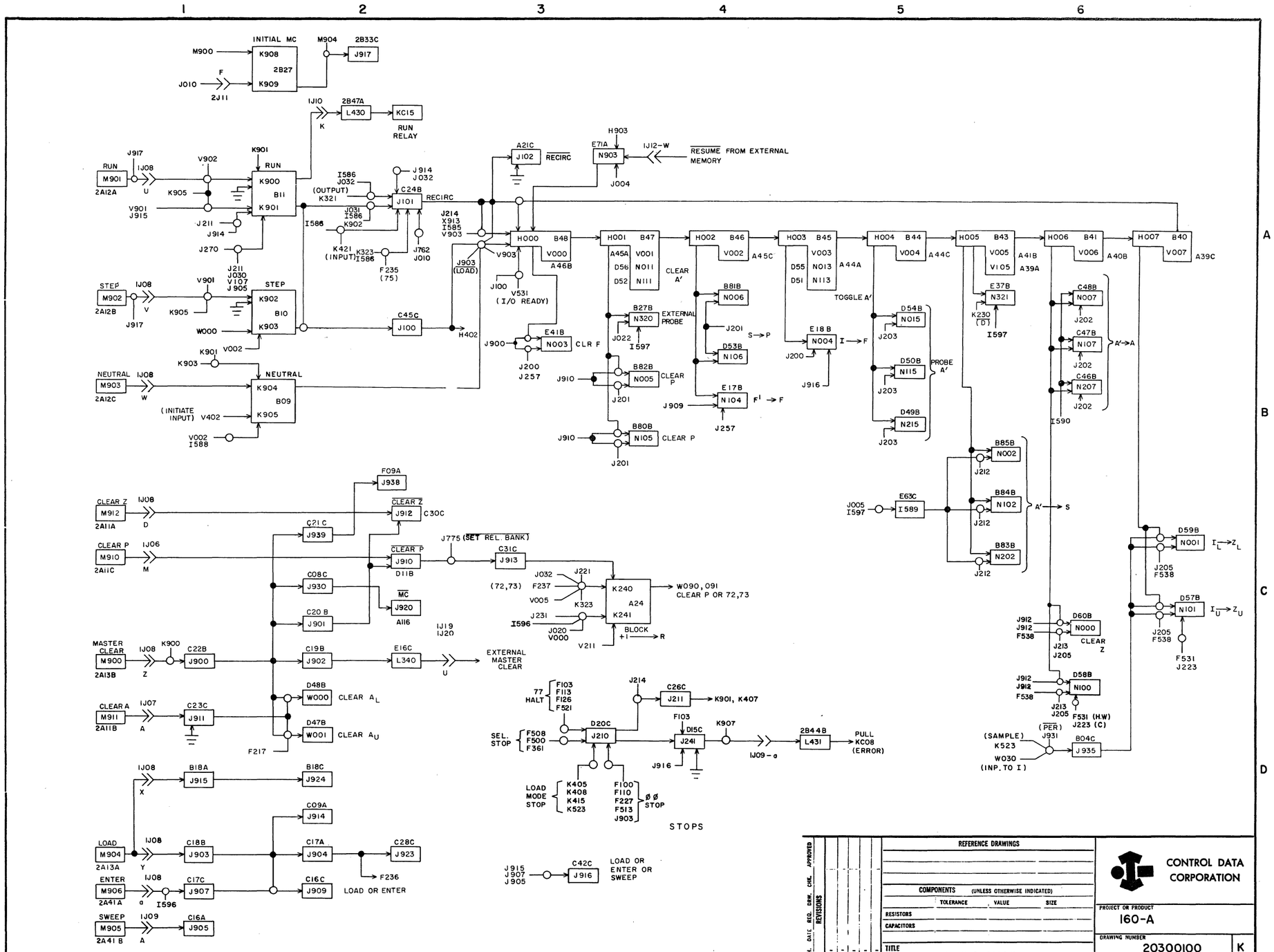


Figure 14. Cable Connections

TERM	LOCATION	PAGE	DEFINITION
F100	E34	4	XXXX00
F103	E11	4	XXXX11
F110	E30	4	XX00XX
F113	E28	4	XX11XX
F126	E23	4	11XXXX — F Reg. Translators
F217	D26C	5	$\overline{Z_L \rightarrow Q}$
F227	D16B	5	0X
F235	D12C	5	75
F237	D10A	5	72, 73
F243	A08C	5	76 — Function Translators
F361	F120C	6	Bit 6 F^1 Register
F500	F110C	6	11111X
F508	E62C	6	Selective Stop
F513	E106A	6	XX00
F521	E13A	6	XX77, XX00
F531	D03C	6	Half Write
F536	F86A	6	$\overline{7677}$
F538	D04C	6	$\overline{7677}$ 4 quarter — F^1 Translators
H903	A26	2	Resync Timing
I585	B25C	20	$\overline{\text{Storage Sequence Interrupt}}$
I586	B25A	20	$\overline{\text{Storage Sequence Interrupt}}$
I588	A21A	20	$\overline{\text{Buffer Step + Storage Sequence Int.}}$
I590	F57B	20	Buffer Cycle
I593	F59A	20	$\overline{\text{Buffer Cycle}}$
I596	B23A	20	$\overline{\text{Buffer Cycle}}$
I597	B23C	20	Buffer Cycle
J001	C39B	2	1 quarter
J005	E72A	2	$\overline{1}$ quarter
J004	E72C	2	$\overline{1}$ quarter
J010	C38A	2	E-2 quarter
J014	B01C	2	E-2 quarter
J020	C37B	2	$\overline{E\text{-}3}$ quarter
J022	B04A	2	$\overline{E\text{-}3}$ quarter
J030	C36B	2	E-4 quarter
J031	C35B	2	4 quarter
J032	C34B	2	4 quarter
J200	C31A	3	$\overline{\text{Clear F}}$ $\overline{Z \rightarrow F}$
J201	C30A	3	$\overline{CL \rightarrow P}$ $\overline{S \rightarrow P}$
J202	C32B	3	$\overline{A^1 \rightarrow A}$
J203	C29B	3	$\overline{\text{Probe } A^1}$
J205	C27A	3	$\overline{\text{Clear Z}}$ $\overline{I \rightarrow Z}$
J212	E32C	3	$\overline{A^1 \rightarrow S}$ — Timing Controls
J213	C23A	3	$\overline{\text{Clear Z}}$
J214	B19A	2	Memory Voltages Ok
J221	B08B	2	C & $\overline{\text{Buffer Cycle}}$
J223	B17A	2	C Cycle
J231	B07B	2	$\overline{D \text{ Cycle}}$
J257	E09A	3	$\overline{F^1 \rightarrow F}$
J270	E67C	19	$\overline{\text{Interrupt}}$
J762	C102A	13	Block Recirc
J775	E76C	13	$\overline{A \rightarrow P}$
J931	D06A	17	$\overline{\text{PER And Load}}$
K221	A29B	2	$\overline{C \text{ Cycle}}$
K230	A25A	2	$\overline{D \text{ Cycle}}$
K321	B29C	16	Wait Output
K323	B28C	16	Function Ready
K405	C07C	17	$\overline{\text{Load Mode Control}}$
K408	A10A	17	$\overline{\text{Sense 7th Level}}$
K415	A11C	17	Load Mode Stop
K421	B24C	16	Wait Input
K523	B22C	16	Sample
K907	E03C	2	Program Step
M006	A36A	27	Set Bit 6 "P" Register
V211	A33	2	B Cycle
V402	A12C	17	Input - PER Control
V521	C11B	16	Sample Pulsing
V531	E71C	16	Start Timing Chain
V901	C14A	2	Resync Timing ODD
V902	C13A	2	Resync Timing EVEN
V903	C10A	2	Resync Timing ODD
W000	D48	3	Clear A_L
W030	E113	3	Input $\rightarrow I^L$
X913	A42C	20	Buffer Step

FORM 510



REV.	AUTH.	DATE	REQ.	DRW.	CHK.	REVISIONS	APPROVED
							APPROVED
							CHECKED
							DRAWN
							DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
MAIN TIMING CHAIN

CONTROL DATA CORPORATION

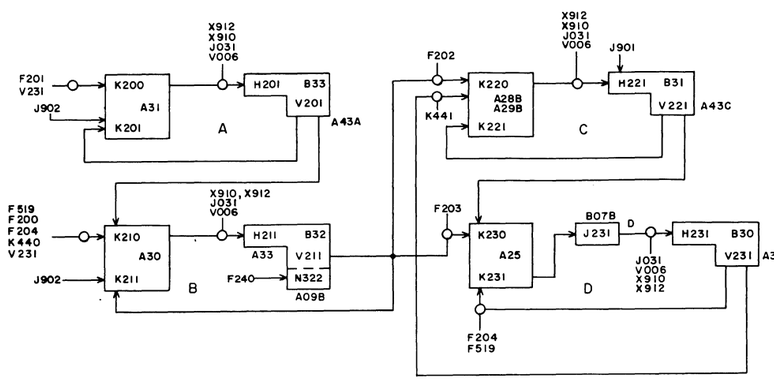
PROJECT OR PRODUCT
160-A

DRAWING NUMBER
20300100 K

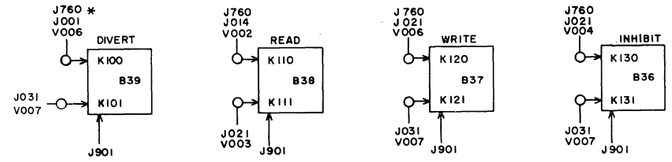
PAGE
1

TERM	LOCATION	PAGE	DEFINITION
F200	D33B	5	$\overline{\text{Indirect}}$
F201	D32A	5	Indirect
F202	D32C	5	B → C
F203	D31C	5	$\overline{\text{B → C}}$
F204	D30A	5	$\overline{\text{D → D}}$
F240	A08A	5	75
F519	E66C	6	$\overline{\text{P +2}}$ F^1 Translators
H000	B48	1	T - X0
H002	B46	1	T - X2
H004	B44	1	T - X4
I562	F104C	20	$\overline{\text{Buffer Cycle}}$
I594	F59C	20	$\overline{\text{Buffer Cycle}}$
I597	B23C	20	$\overline{\text{Buffer Cycle}}$
J760	A123A	13	Internal Module Select
J901	C20B	1	MC
J902	C19B	1	MC
K440	A07	16	$\overline{\text{I/O Sequence Control}}$
K441	A06	16	I/O Sequence Control
M916	A41C	23	$\overline{\text{Voltages in Memory Ok}}$
N001	D59B	1	$I_L \rightarrow Z_L$
N004	E40B	1	I → F
V000	A46B	1	T - X0
V002	A45C	1	R - X2
V003	A44A	1	T - X3
V004	A44C	1	T - X4
V005	A41B	1	T - X5
V006	A40B	1	T - X6
V007	A39B	1	T - X7
W000	D48	3	Cl. A_L
X910	F29A	20	$\overline{\text{Storage Sequence Interrupt}}$
X912	A42A	20	$\overline{\text{Buffer Step}}$

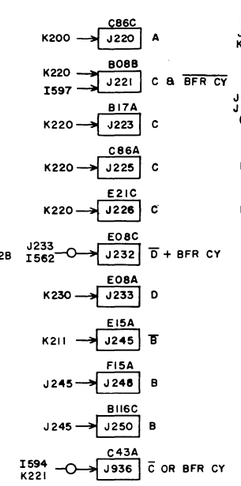
FORM 510

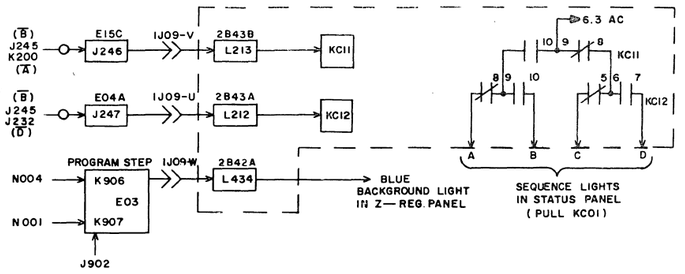


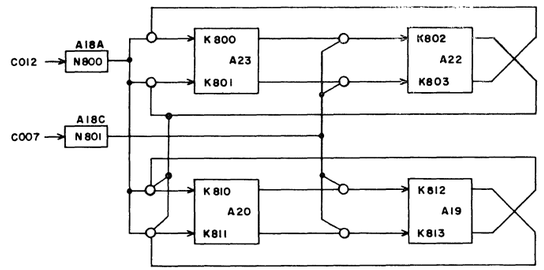
STORAGE SEQUENCE CONTROL (SSC)



STORAGE REFERENCE CONTROL (SRC)

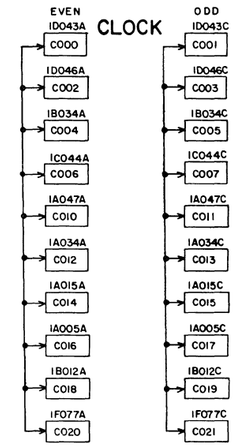


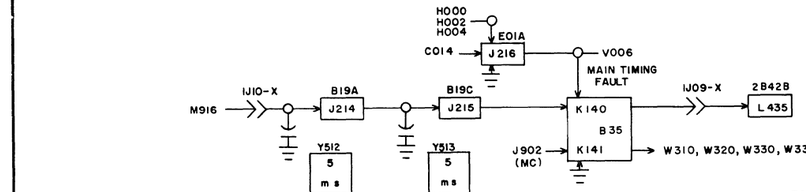


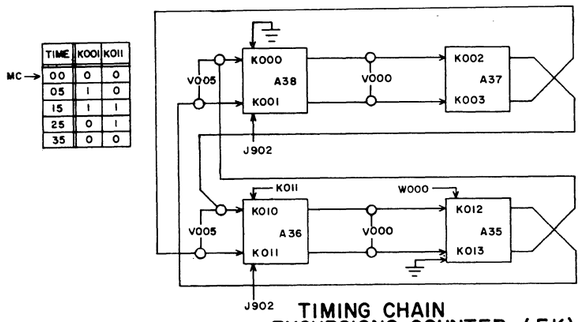


RESYNC COUNTER

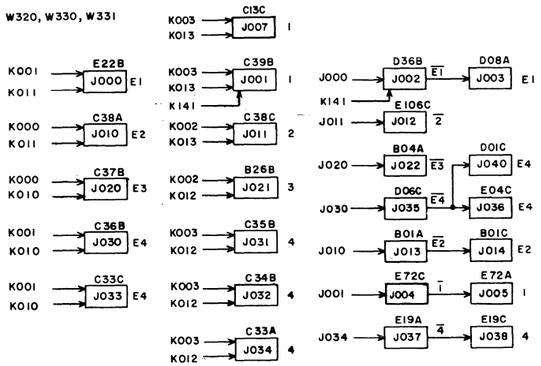
RESYNC TIMING







TIMING CHAIN EXCURSIONS COUNTER (EK)



PRIMARY TIMING CONTROL

* J760 = INTERNAL MEMORY MODULE NOT BUSY

NOTE:
FOR SYSTEMS USING THE 169, REFER TO DWG. NO. 203002B

REVISIONS					
REV.	AUTH.	DATE	REQ. DWR. CHK.	APPROVED	
-					

APPROVED 8-28-61
CHECKED -
DRAWN - R D S
DESIGNED -

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

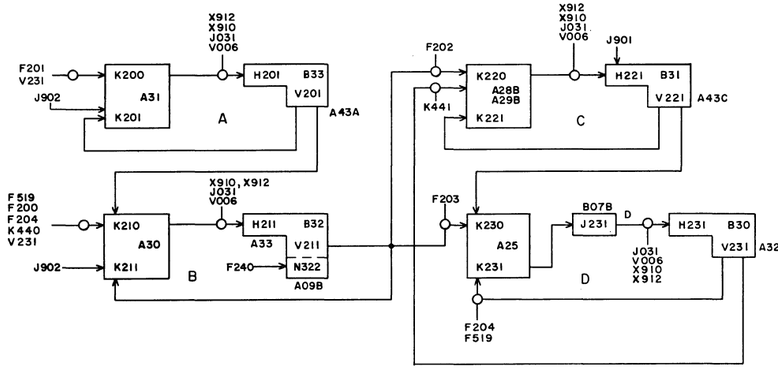
TITLE
MAIN CONTROL

CONTROL DATA CORPORATION

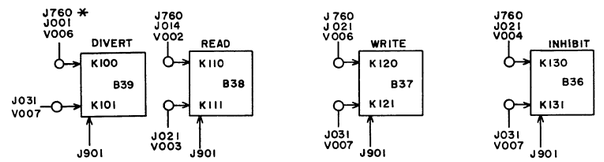
PROJECT OR PRODUCT
160-A

DRAWING NUMBER
20300200 K

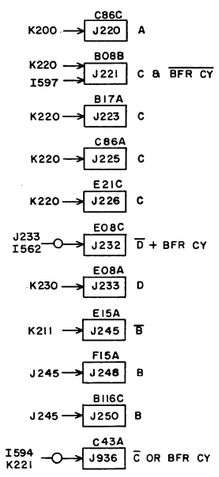
PAGE
2.0

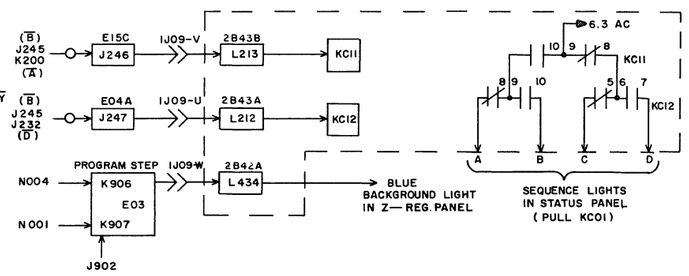


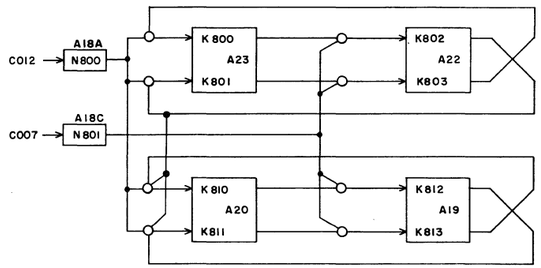
STORAGE SEQUENCE CONTROL (SSC)



STORAGE REFERENCE CONTROL (SRC)

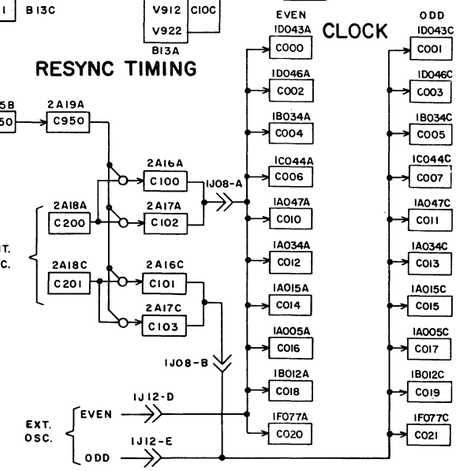




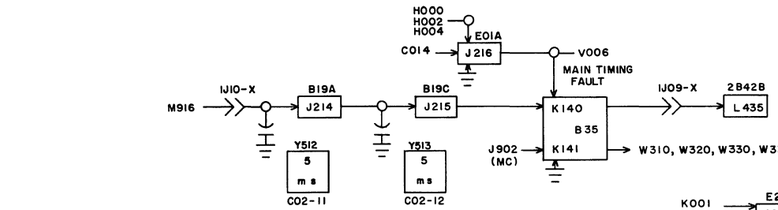


RESYNC COUNTER

RESYNC TIMING

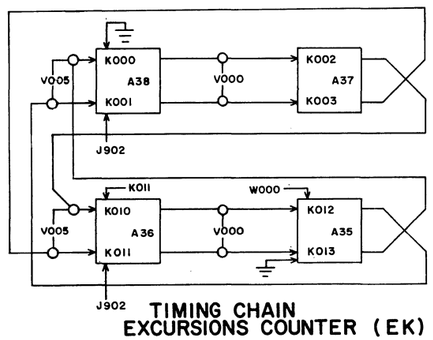


CLOCK

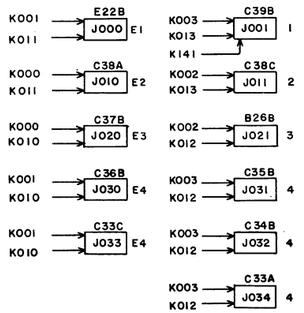


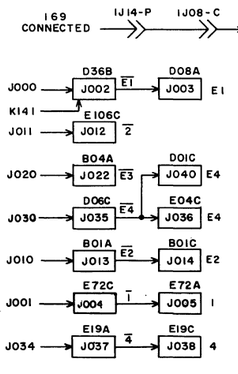
TIMING CHAIN

MC →	TIME	K001	K011
	00	0	0
	05	1	0
	15	1	1
	25	0	1
	35	0	0



EXCURSIONS COUNTER (EK)





PRIMARY TIMING CONTROL

* J760 = INTERNAL MEMORY MODULE NOT BUSY

REV.	AUTH.	DATE	REVISIONS	REQ.	DWK.	CHK.	APPROVED

APPROVED =
CHECKED = R.D.S 8-28-61
DRAWN =
DESIGNED =

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE

MAIN CONTROL

CONTROL DATA CORPORATION

PROJECT OR PRODUCT
160-A

DRAWING NUMBER
20300200 K

PAGE
2.1

TERM	LOCATION	PAGE	DEFINITION
A001	C60C	7	Bit 0
A011	C59C	7	Bit 1
A021	C58C	7	Bit 2
A031	C57C	7	Bit 3
A041	C56C	7	Bit 4
A051	C55C	7	Bit 5
A061	C54C	7	Bit 6 } A Register
A071	C53C	7	Bit 7
A081	C52C	7	Bit 8
A091	C51C	7	Bit 9
A101	C50C	7	Bit 10
A111	C49C	7	Bit 11
F001	D41C	4	Bit 6
F011	D40C	4	Bit 7
F020	D38A	4	$\overline{\text{Bit 8}}$ } F Register
F022	D39A	4	$\overline{\text{Bit 9}}$
F041	D35C	4	Bit 10
F051	D34C	4	Bit 11
F100	E34	4	XXXX00
F110	E30	4	XX00XX
F113	E28	4	XX11XX } F Translators
F120	E27	4	00XXXX
F122	E26	4	10XXXX
F126	E23	4	11XXXX
F207	D27A	5	$\overline{70}$, $\overline{71}$
F211	D25A	5	$\overline{A \rightarrow Q}$
F213	D24B	5	$\overline{73}$
F214	D08C	5	73
F215	D22A	5	$\overline{P \rightarrow Q}$
F216	D20A	5	$\overline{Z \rightarrow Q}$
F217	D26C	5	$\overline{Z_L \rightarrow Q}$
F221	C25A	5	72
F223	D18C	5	$\overline{Z \rightarrow R}$
F225	D22C	5	$\overline{-Z \rightarrow R}$
F226	D14A	5	$\overline{-Z_L \rightarrow R}$
F228	D15A	5	$\overline{+1 \rightarrow R}$
F229	C12C	5	$\overline{Z_L \rightarrow R}$, $\overline{+1 \rightarrow R_U}$
F232	D13A	5	$\overline{01}$ 3rd or 4th quarter
F236	C14C	5	$\overline{72C}$ or Load Mode
F237	D10A	5	72, 73
F238	D10C	5	72, 73
F244	D44A	5	$\overline{76}$
F245	D44C	5	76
F246	C43C	5	$\overline{72}$
F303	E111A	6	Bit 0 } F^1 Register
F322	F129A	6	$\overline{\text{Bit 3}}$
F405	A14B	6	$\overline{7100}$ C Cycle
F407	C04A	6	$\overline{7100}$
F513	E106A	6	$\overline{XX00_8}$
F523	E14C	6	$\overline{+1 \rightarrow R}$
F532	B06A	6	$\overline{\text{Indirect 00 E1 quarter A Cycle}}$
F534	C15A	6	Forced Function
F535	E02B	6	$\overline{7677}$
F537	F86C	6	$\overline{7677}$ 4 quarter
F541	A86A	6	Specific Add
F550	F113A	6	$\overline{XX02+XX03+XX12+XX13}$
F563	C123B	6	$\overline{0100}$ 4 quarter
F565	B115C	6	$\overline{0101}$ 4 quarter
F576	D21A	6	$\overline{015X}$ C Cycle + Interrupt
F577	E77C	5	01XX 3rd or 4th quarter
F578	E77A	5	$\overline{XX1X}$
F579	E76A	5	$\overline{F550}$ + XX1X

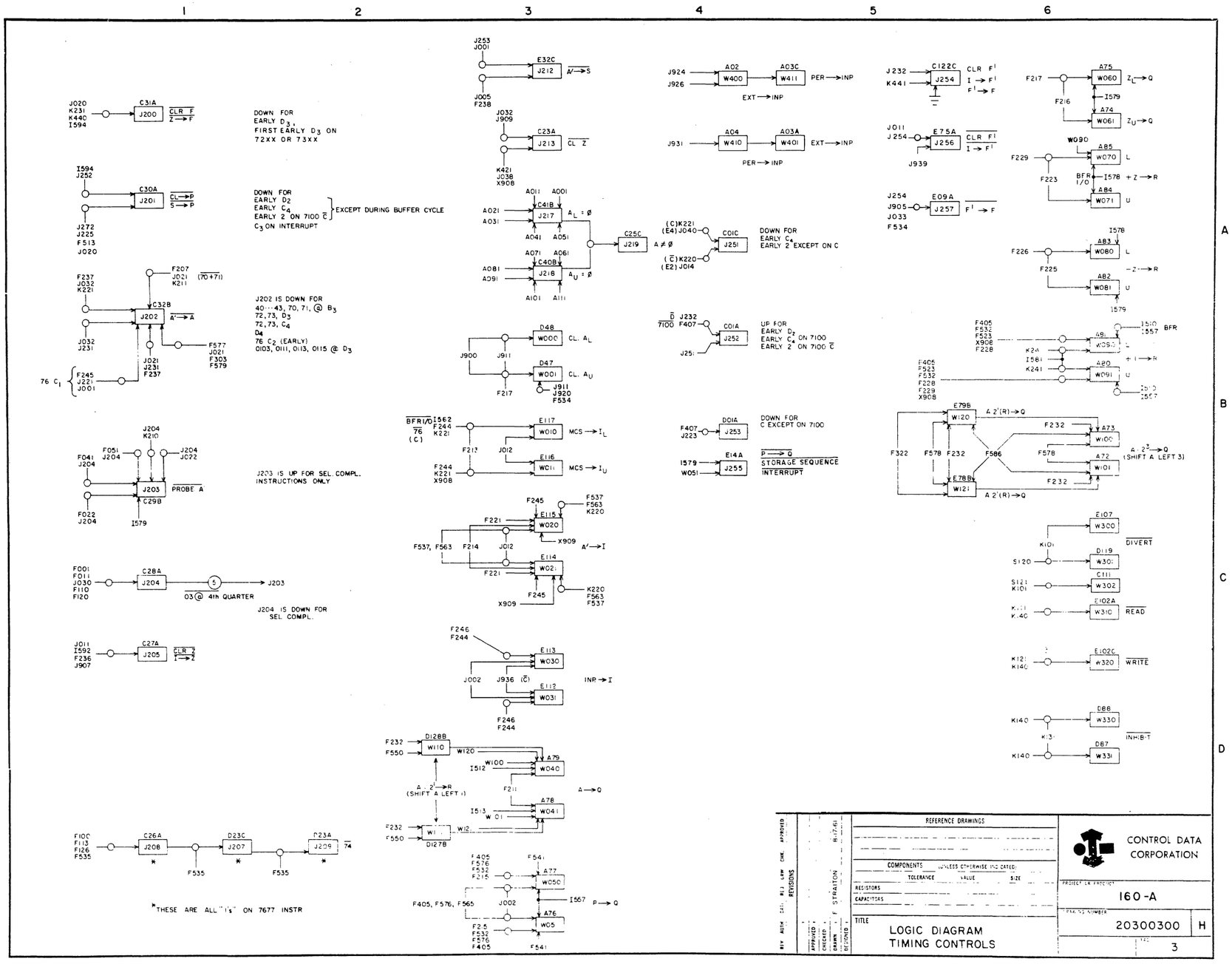
Func. Trans.

F^1 Translators

FORM 510

TERM	LOCATION	PAGE	DEFINITION
F586	A123C	6	$\overline{XXX11X}$ – F^1 Translators
I510	F76B	20	$\overline{BER \rightarrow Q}$
I512	F55C	20	BER → Q
I513	F55A	20	BER → Q
I557	F10C	20	Storage Sequence Interrupt
I562	F104C	20	$\overline{\text{Buffer Cycle}}$
I578	E104A	20	Storage Sequence Interrupt
I579	E104C	20	$\overline{\text{Storage Sequence Interrupt}}$
I581	F56C	20	$\overline{\text{Storage Sequence Interrupt}}$
I591	F58A	20	$\overline{\text{Buffer Cycle}}$
I592	F58C	20	$\overline{\text{Buffer Cycle}}$
I594	F59C	20	$\overline{\text{Buffer Cycle}}$
J001	C39B	2	1 quarter
J002	D36B	2	$\overline{E\text{-}1}$ quarter
J005	E72A	2	1 quarter
J010	C38A	2	E-2 quarter
J011	C38C	2	2 quarter
J012	E106C	2	$\overline{2}$ quarter
J014	B01C	2	E-2 quarter
J020	C37B	2	E-3 quarter
J021	B26B	2	3 quarter
J022	B04A	2	$\overline{E\text{-}3}$ quarter
J030	C36B	2	E-4 quarter
J032	C34B	2	4 quarter
J033	C33C	2	E-4 quarter
J038	E19C	2	4 quarter
J040	D01C	2	E-4 quarter
J221	B08B	2	C & $\overline{\text{Buffer Cycle}}$
J223	B17A	2	C Cycle
J225	C86A	2	C Cycle
J231	B07B	2	D Cycle
J232	E08C	2	$\overline{D}$ + Buffer Cycle
J261	E21A	19	$\overline{\text{Interrupt}}$
J272	B05C	6	F^1 Bit 3 + Int
J900	C22B	1	$\overline{MC}$
J905	C16A	1	$\overline{\text{Sweep}}$
J907	C17C	1	$\overline{\text{Enter}}$
J909	C16C	1	Load or Enter
J911	C23C	1	$\overline{\text{Clear A}}$
J920	A116	1	$\overline{MC}$
J924	B18C	1	Load
J926	B16A	17	Select PER or Load
J928	D04A	17	$\overline{\text{Select PER}}$
J931	D06A	17	$\overline{\text{PER and Load}}$
J936	C43A	2	$\overline{C}$ Or Buffer Cycle
J939	C21C	1	MC
K101	B39C	2	Divert
K111	B38C	2	Read
K121	B37C	2	Write
K131	B36C	2	Inhibit
K140	B35A	2	$\overline{\text{Main Timing Fault}}$
K210	A30A	2	$\overline{\text{B Cycle}}$
K211	A30C	2	$\overline{\text{B Cycle}}$
K220	A28B	2	$\overline{\text{C Cycle}}$
K221	A29B	2	C Cycle
K231	A25C	2	D Cycle
K241	A24C	1	Block + 1 → R
K421	B24C	16	$\overline{\text{Wait Input}}$
K440	A07	16	$\overline{\text{I/O Sequence Control}}$
K441	A06	16	I/O Seq. Control
X908	F32A	20	$\overline{\text{Buffer Cycle}}$
X909	F32C	20	Buffer Cycle
S120	C112A	13	$\overline{\text{Ext. Storage ODD/EVEN Bank Select}}$
S121	C112C	13	Ext. Storage ODD/EVEN Bank Select

FORM 510

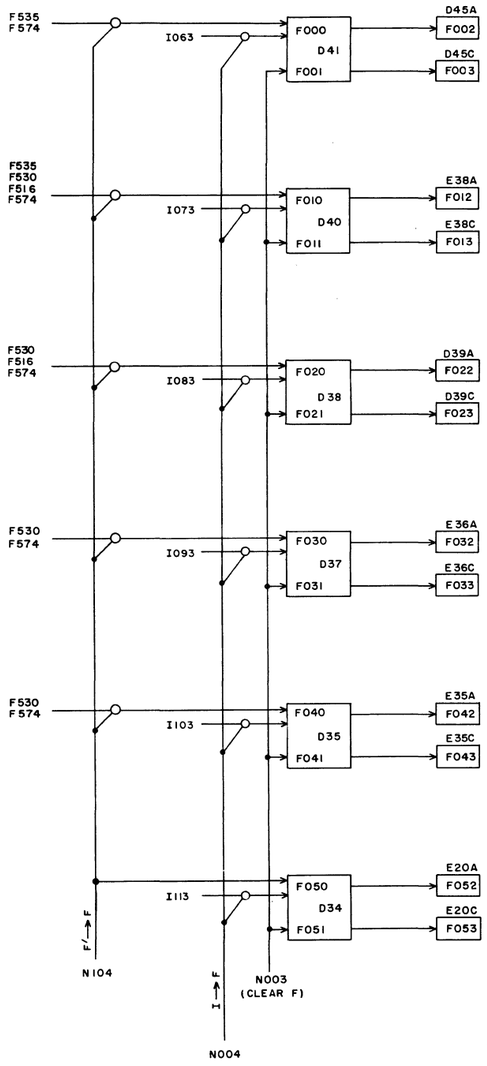

1
2
3
4
5
6
A
B
C
D
J020 K231 K440 I594
C31A J200 CLR F Z→F
DOWN FOR EARLY D3, FIRST EARLY D3 ON 72XX OR 73XX
I594 J252
C30A J201 CL→P S→P
J272 J225 F513 J020
DOWN FOR EARLY D2 EARLY C4 EARLY 2 ON 7100 C̄ } EXCEPT DURING BUFFER CYCLE
C3 ON INTERRUPT
F237 J032 K221
F207 J021 K211 (70+71)
C32B J202 A'→A
J032 J231
J021 J231 F237
F577 J021 F303 F579
76 C1 F245 J221 J001
J202 IS DOWN FOR
40···43, 70, 71, @ B3
72, 73, D3
72, 73, C4
D4
76 C2 (EARLY)
0103, 0111, 0113, 0115 @ D3
J204 K210
F041 J204
F051 J204
J204 J072
J203 C29B PROBE A
F022 J204
I579
J203 IS UP FOR SEL. COMPL. INSTRUCTIONS ONLY
F001 F011 J030 F110 F120
C28A J204 5 → J203
03 @ 4th QUARTER
J204 IS DOWN FOR SEL. COMPL.
J011 I592 F236 J907
C27A J205 CLR 2 1→2
F10C F113 F126 F535
C26A J208 * F535
D23C J207 * F535
D23A J209 * 74
*THESE ARE ALL "1's" ON 7677 INSTR
J253 J001
E32C J212 A'→S
J005 F238
J032 J909
C23A J213 CL Z
K421 J038 X908
A01 A00
C41B J217 AL = Ø
A02 A03
A04 A05
A07 A06
C40B J218 AU = Ø
A08 A09
A10 A11
C25C J219
D48 W000 CL. AL
J900 J911
D47 W001 CL. AU
J911 J920 F534
F217
BFR I/O 1562 F244 K221 X908
E117 W010 MCS → IL
E116 W011 MCS → IU
F213 J012
F245 F537 F563 K220
E115 W020
F221
X909 A'→I
F537, F563 F214 J012
E114 W021
F221
F245
K220 F563 F537
X909
F246 F244
E113 W030
J002 J936 (C̄) INP→I
E112 W031
F246 F244
D128B W110 W120 A79 W040
F232 F550
W100 I512
A-2→R (SHIFT A LEFT 1)
F211 A→Q
A78 W041
I513 W01
F232 F550 W1 W12
D127B
F405 F576 F532 F215 F541
A77 W050
F405, F576, F565 J002 I557 P→Q
A76 W05
F25 F532 F576 F405 F541
J924 J926
A02 W400 A03C W411 PER→INP
EXT→INP
J931
A04 W410 A03A W401 EXT→INP
PER→INP
(C)K221 (E4)J040
C01C J251 DOWN FOR EARLY C4 EARLY 2 EXCEPT ON C
A≠Ø
(C̄)K220 (E2) J014
J232 7100 F407
C01A J252 UP FOR EARLY D2 EARLY C4 ON 7100 EARLY 2 ON 7100 C̄
J251
F407 J223
D01A J253 DOWN FOR C EXCEPT ON 7100
1579 W051
E14A J255 P→Q STORAGE SEQUENCE INTERRUPT
J232 K441
C122C J254 CLR F1 I→F1 F1→F
J011 J254
E75A J256 CLR F1 I→F1
J939
J254 J905 J033 F534
E09A J257 F1→F
F217
A75 W060 ZL→Q
F216
I579
A74 W061 ZU→Q
W090
F229
AB5 W070 L
F223
BFR I/O I578 +Z→R
AB4 W071 U
I578
F226
AB3 W080 L
F225
−Z→R
AB2 W081 U
I579
F405 F532 F523 X908 F228
A81 W082 L
K241 I581
A80 W091 U
I580 I557 BFR
+1→R
F405 F532 F523 F228 F229 X908
I580 I557
E79B W120 A2(R)→Q
F322 F578 F232 F586
F232
A73 W100
F578
A72 W101
A-2→Q (SHIFT A LEFT 3)
E78B W121 A2(R)→Q
E107 W300 DIVERT
K101 S120
D119 W301
S121 K101
C111 W302
K141 K140
E102A W310 READ
K121 K140
E102C W320 WRITE
K140
D86 W330 INH/B-T
K13-
K140
D87 W331
REFERENCE DRAWINGS
COMPONENTS (UNLESS OTHERWISE INDICATED)
TOLERANCE VALUE SIZE
RESISTORS
CAPACITORS
REVISIONS
REV AUTH DATE
APPROVED
CHKD APPROVED
DRAWN F STRAITON 8/27/61
REVISED
CONTROL DATA CORPORATION
PROJECT OR PRODUCT
160-A
DRAWING NUMBER
20300300 H
SHEET
3
TITLE
LOGIC DIAGRAM
TIMING CONTROLS

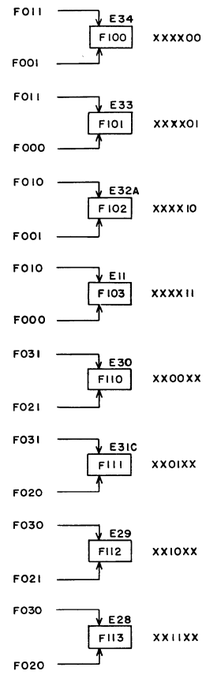
TERM	LOCATION	PAGE	DEFINITION
F514	E62A	6	Forced 71XX
F516	E13C	6	$\overline{\text{Forced 71XX}}$
F530	D03A	6	Half Write
F531	D03C	6	Half Write
F535	D02B	6	$\overline{7677}$
F536	F86A	6	7677
F574	D42B	6	$\overline{015X}$, $\overline{016X}$, $\overline{\text{Interrupt}}$
F575	D21C	6	015X, 016X, Interrupt
I063	D126B	10	Bit 6
I073	D122B	10	Bit 7
I083	D121A	10	Bit 3
I093	D121C	10	Bit 9
I103	C121C	10	Bit 10
I113	D120B	10	Bit 11
N003	E41B	1	Clear F
N004	E40B	1	I → F
N104	E17B	1	F^1 → F

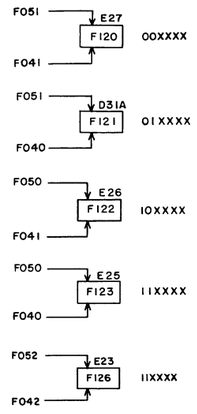
I_U Register

FORM 510

SYMBOL	REPRESENTS	F IS FORCED TO
F516	$\overline{\text{FORCED 71XX}}$	71
F530	$\overline{\text{HALF WRITE}}$	41
F535	$\overline{7677}$	74
F574	$\overline{015X}$ $\overline{016X}$ $\overline{\text{INTERRUPT}}$	40







REV.	AUTH.	DAT.	REQ.	DRW.	CHK.	APPROVED
REVISIONS						
-						
APPROVED						
CHECKED						
DRAWN			R.D.S.			8-15-61
DESIGNED						

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE: F REGISTER & TRANSLATORS

CONTROL DATA CORPORATION

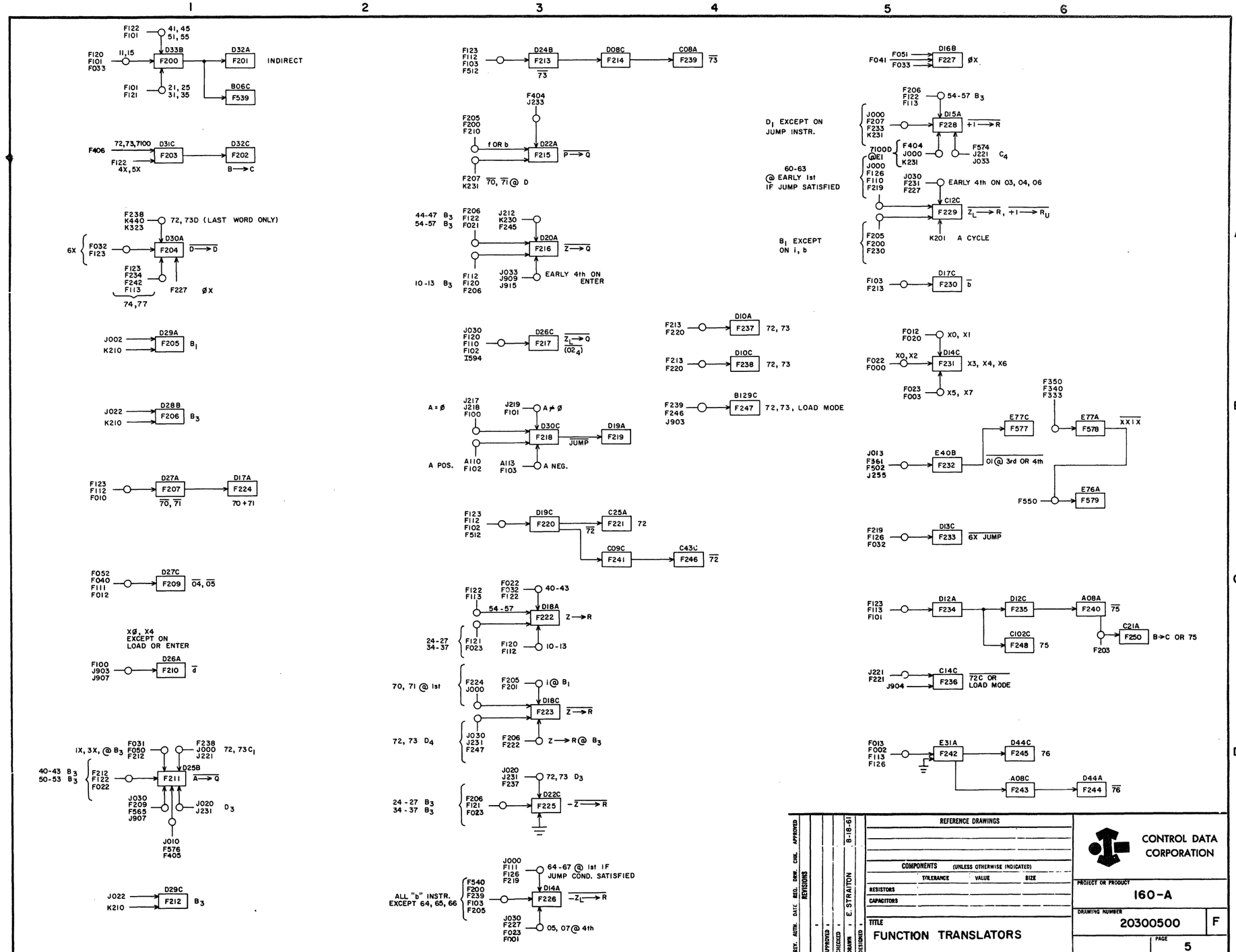
PROJECT OR PRODUCT: 160-A

DRAWING NUMBER: 20300400 A

PAGE 4

TERM	LOCATION	PAGE	DEFINITION
A110	C49A	7	Bit 11
A113	E92C	7	Bit 11 — A Register
F000	D41	4	Bit 6
F001	D41C	4	Bit 6
F002	D45A	4	Bit 6
F003	D45C	4	Bit 6
F010	D40A	4	Bit 7
F012	E38A	4	Bit 7
F013	E38C	4	Bit 7
F020	D38A	4	Bit 8
F021	D38C	4	Bit 8
F022	D39A	4	Bit 8
F023	D39C	4	Bit 8 — F Register
F031	D37C	4	Bit 9
F032	E36A	4	Bit 9
F033	E36C	4	Bit 9
F040	D35A	4	Bit 10
F041	D35C	4	Bit 10
F050	D34A	4	Bit 11
F051	D34C	4	Bit 11
F052	E20A	4	Bit 11
F100	E34	4	XXXX00
F101	E33	4	XXXX01
F102	E32A	4	XXXX10
F103	E11	4	XXXX11
F110	E30	4	XX00XX
F111	E31C	4	XX01XX
F112	E29	4	XX10XX — F Register Translators
F113	E28	4	XX11XX
F120	E27	4	00XXXX
F121	D31A	4	01XXXX
F122	E26	4	10XXXX
F123	E25	4	11XXXX
F126	E23	4	11XXXX
F333	F129C	6	Bit 3
F340	F124A	6	Bit 4
F350	F123A	6	Bit 5 — F^1 Register Translators
F361	F120C	6	Bit 6
F404	B05A	6	7100
F405	A14B	6	7100 C Cycle
F406	C04C	6	B → D
F502	F111C	6	00000X — F^1 Reg.
F512	E61C	6	$XX00_8$ — Translators
F540	D86B	6	Specific Add
F550	F113A	6	XX02, XX03, XX12, XX13
F565	B115C	6	0101 4 quarter
F574	D42B	6	015X, 016X, Interrupt
F576	D21A	6	015XC, Interrupt C Cycle
I594	F59C	20	Buffer Cycle
J000	E22B	2	E-1 quarter
J002	D36B	2	E-1 quarter
J010	C38A	2	E-2 quarter
J013	B01A	2	E-2 quarter
J020	C37B	2	E-3 quarter
J022	B04A	2	E-3 quarter
J030	C36B	2	E-4 quarter
J033	C33C	2	E-4 quarter
J212	E32C	3	$A^1 \rightarrow S$
J217	C41B	3	$A_L = \emptyset$
J218	C40B	3	$A_U = \emptyset$
J219	C25C	3	$A \neq \emptyset$
J221	B08B	2	C & Buffer Cycle
J231	B07B	2	D Cycle
J233	E08A	2	D Cycle
J255	E14A	3	P → Q, Storage Sequence Interrupt
J903	C18B	1	Load
J904	C17A	1	Load
J907	C17C	1	Enter
J909	C15B	1	Load Or Enter
J915	B18A	1	Load
K201	A31C	2	A Cycle
K210	A30A	2	B Cycle
K230	A25A	2	D Cycle
K231	A25C	2	D Cycle
K323	B28C	16	Function Ready
K440	A07	16	I/O Sequence Control

FORM 510



REV.	AUTH.	DATE	REQ.	DWR.	CHK.	APPROVED
REVISIONS						
	-					
APPROVED	-					
CHECKED	-					
DRAWN	-	E. STRAITON				8-18-61
DESIGNED	-					

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
FUNCTION TRANSLATORS

CONTROL DATA CORPORATION

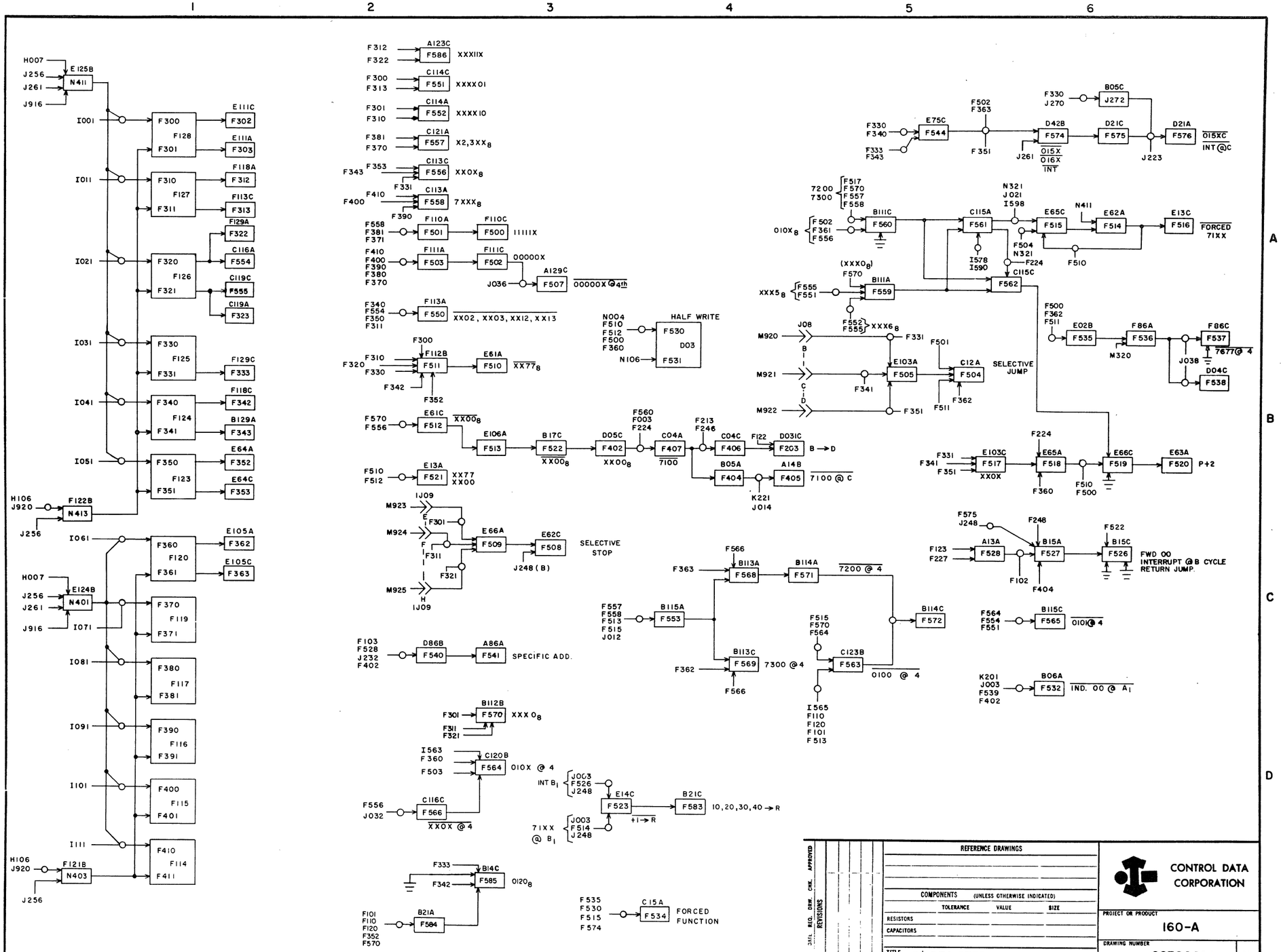
PROJECT OR PRODUCT
160-A

DRAWING NUMBER
20300500 F

PAGE
5

TERM	LOCATION	PAGE	DEFINITION
F003	D45C	4	Bit 6 F Register
F101	E33	4	XXXX01
F102	E32A	4	XXXX10
F103	E11	4	XXXX11
F110	E30	4	XX00XX
F112	E29	4	XX10XX
F120	E27	4	00XXXX
F122	E26	4	10XXXX
F123	E25	4	11XXXX (F Register Translators)
F213	D24B	5	$\overline{73}$
F224	D17A	5	70 + 71
F227	D16B	5	0X
F246	C43C	5	$\overline{72}$
F248	C102C	5	75
F539	B06C	13	Indirect + Memory
H007	B40	1	T-7
H106	F42	20	T-6
I001	E123A	10	Bit 0
I011	E123C	10	Bit 1
I021	E122A	10	Bit 2
I031	E122C	10	Bit 3
I041	E121A	10	Bit 4
I051	E121C	10	Bit 5
I061	E120A	10	Bit 6
I071	E120C	10	Bit 7
I081	E119A	10	Bit 8
I091	E119C	10	Bit 9
I101	E118A	10	Bit 10
I111	E118C	10	Bit 11 (I---Inverters)
I563	F104A	20	Buffer Cycle
I578	E104A	20	Storage Sequence Interrupt
I582	F09C	20	Buffer Busy
I590	F57B	20	Buffer Cycle
I598	F24A	20	Buffer Active
J003	D08A	2	E1 quarter
J012	E106C	2	2 quarter
J014	B01C	2	E-2 quarter
J020	C37B	2	E-3 quarter
J021	B26B	2	3 quarter
J032	C34B	2	4 quarter
J036	E04C	2	E-4 quarter
J037	E19A	2	$\overline{4}$ quarter
J038	E19C	2	4 quarter
J223	B17A	2	$\overline{C}$ Cycle
J232	E08C	2	$\overline{D}$ + Buffer Cycle
J248	F15A	2	$\overline{B}$ Cycle
J256	E75A	3	Clr. F^1 $\overline{I \rightarrow F^1}$
J261	E21A	19	Interrupt
J270	E67C	19	Interrupt
J909	C16C	1	Load Or Enter
J914	C09A	1	Load
J916	C42C	1	Load + Enter + Sweep
J920	A116	1	$\overline{MC}$
J939	C21C	1	MC
K201	A31C	2	A Cycle
K221	A29B	2	C Cycle
K441	A06	16	I/O Sequence Control
M320	F11C	16	Info. Ready
M330	A17B	16	Output Resume
M920	A40A	22	Selective Jump #1
M921	A40B	22	Selective Jump #2
M922	A40C	22	Selective Jump #3
M923	A24A	22	Selective Stop #1
M924	A24B	22	Selective Stop #2
M925	A24C	22	Selective Stop #3
N003	E41B	1	Clear F
N004	E18B	1	I → F
N100	D58B	1	Clear Z UPPER
N101	D57B	1	$I_1 \rightarrow Z_1$
N106	D53B	1	S → F
N111	D52	1	Clear A^1
N321	F37B	1	T-5 (D) = BFR Cycle
V001	A45A	1	T-X1 Timing Gate

FORM 510



REFERENCE DRAWINGS			
COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

REV. AUTH. 2611 REQ. DRW. CHG. APPROVED
REVISIONS
APPROVED
CHECKED
DRAWN
DESIGNED

CONTROL DATA CORPORATION

PROJECT OR PRODUCT: 160-A

TITLE: F' REGISTER AND TRANSLATORS

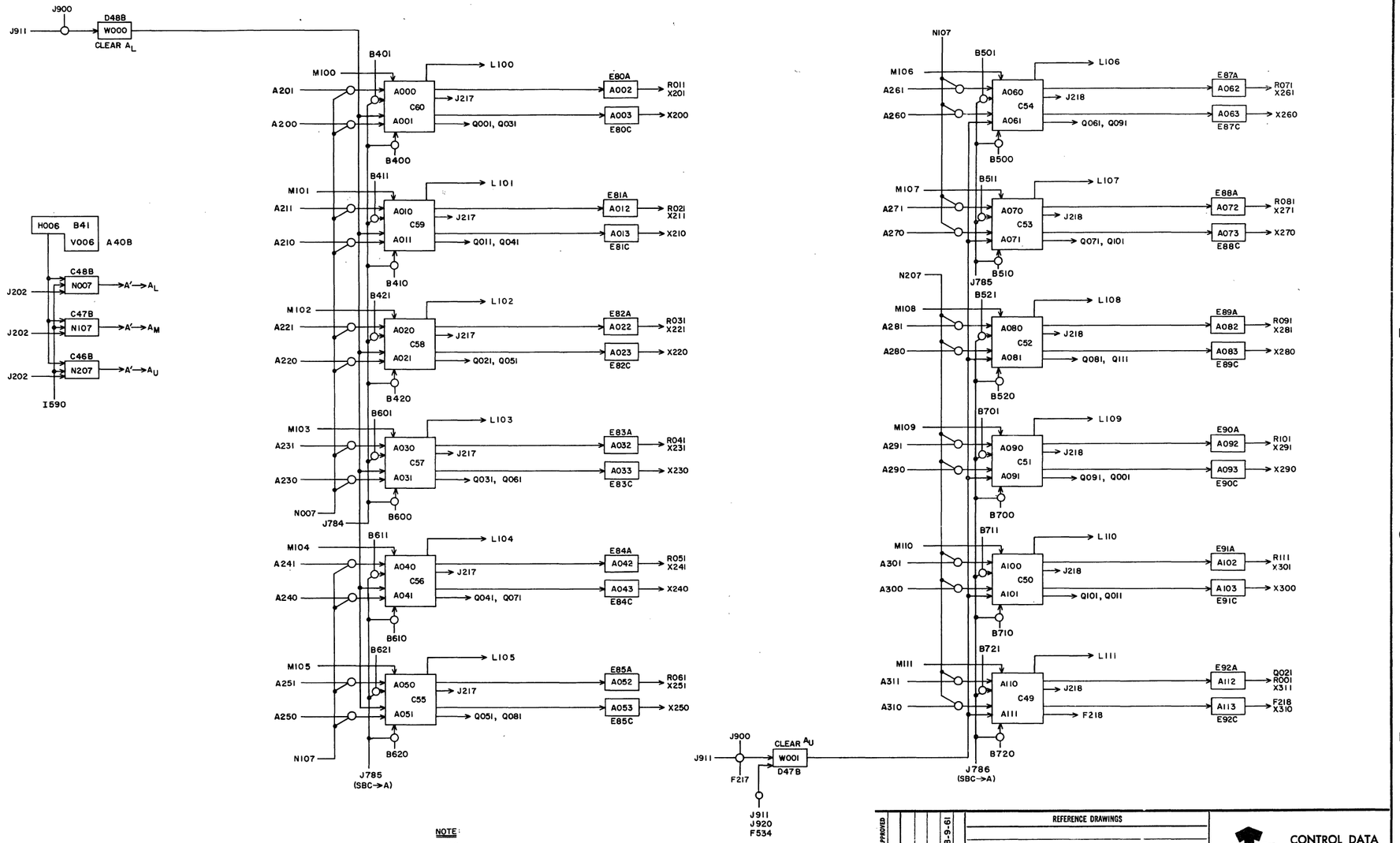
DRAWING NUMBER: 20300600 N

PAGE 6

TERM	LOCATION	PAGE	DEFINITION
A200	C73A	11	$\overline{\text{Bit 0}}$
A201	C73C	11	Bit 0
A210	C72A	11	$\overline{\text{Bit 1}}$
A211	C72C	11	Bit 1
A220	C71A	11	$\overline{\text{Bit 2}}$
A221	C71C	11	Bit 2
A230	C70A	11	$\overline{\text{Bit 3}}$
A231	C70C	11	Bit 3
A240	C69A	11	$\overline{\text{Bit 4}}$
A241	C69C	11	Bit 4
A250	C68A	11	$\overline{\text{Bit 5}}$
A251	C68C	11	Bit 5
A260	C67A	11	$\overline{\text{Bit 6}}$
A261	C67C	11	Bit 6
A270	C66A	11	$\overline{\text{Bit 7}}$
A271	C66C	11	Bit 7
A280	C65A	11	$\overline{\text{Bit 8}}$
A281	C65C	11	Bit 8
A290	C63A	11	$\overline{\text{Bit 9}}$
A291	C63C	11	Bit 9
A300	C62A	11	$\overline{\text{Bit 10}}$
A301	C62C	11	Bit 10
A310	C61A	11	$\overline{\text{Bit 11}}$
A311	C61C	11	Bit 11
B400	B128A	13	Bit 0
B401	B128C	13	Bit 0
B410	B127A	13	Bit 1
B411	B127C	13	Bit 1
B420	B126A	13	Bit 2
B421	B126C	13	Bit 2
B500	B125A	13	Bit 0
B501	B125C	13	Bit 0
B510	B124A	13	Bit 1
B511	B124C	13	Bit 1
B520	B123A	13	Bit 2
B521	B123C	13	Bit 2
B600	B122A	13	Bit 0
B601	B122C	13	Bit 0
B610	B121A	13	Bit 1
B611	B121C	13	Bit 1
B620	B120A	13	Bit 2
B621	B120C	13	Bit 2
B700	B119A	13	Bit 0
B701	B119C	13	Bit 0
B710	B118A	13	Bit 1
B711	B118C	13	Bit 1
B720	B117A	13	Bit 2
B721	B117C	13	Bit 2
F217	D26C	5	$\overline{Z_L \rightarrow Q}$
F534	C15A	6	Forced Function
I557	F10C	20	Storage Sequence Interrupt
I590	F57B	20	$\overline{\text{BFR Cycle}}$
J202	C32B	3	$A^1 \rightarrow A$
J784	B42B	13	Storage Bank Selection to A
J785	E42B	13	Storage Bank Selection to A
J786	E54B	13	Storage Bank Selection to A
J900	C22B	1	$\overline{\text{MC}}$
J911	C23C	1	$\overline{\text{Clear A}}$
J920	A116	1	$\overline{\text{MC}}$
M100	A20A	27	Set Bit 0
M101	A20B	27	Set Bit 1
M102	A20C	27	Set Bit 2
M103	A21A	27	Set Bit 3
M104	A21B	27	Set Bit 4
M105	A21C	27	Set Bit 5
M106	A22A	27	Set Bit 6
M107	A22B	27	Set Bit 7
M108	A22C	27	Set Bit 8
M109	A23A	27	Set Bit 9
M110	A23B	27	Set Bit 10
M111	A23C	27	Set Bit 11

Bit 0 – Bit 11: A^1 Register
B400 – B421: Relative Bank
B500 – B521: Direct Bank
B600 – B621: Indirect Bank
B700 – B721: Buffer Bank
M100 – M111: A Register Manual

FORM 510



NOTE:
"L" CARDS SHOWN GO TO DIGITAL DISPLAY CONTROL RELAYS, PAGE 28.
"M" CARDS ARE SHOWN ON PAGE 27.

REV.	AUTH.	DATE	REQ.	DWN.	CHK.	APPROVED
	REVISIONS					
APPROVED						
CHECKED						
DRAWN	E. STRAITON	8-9-61				
DESIGNED						

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
LOGIC DIAGRAM
REGISTER A

CONTROL DATA CORPORATION

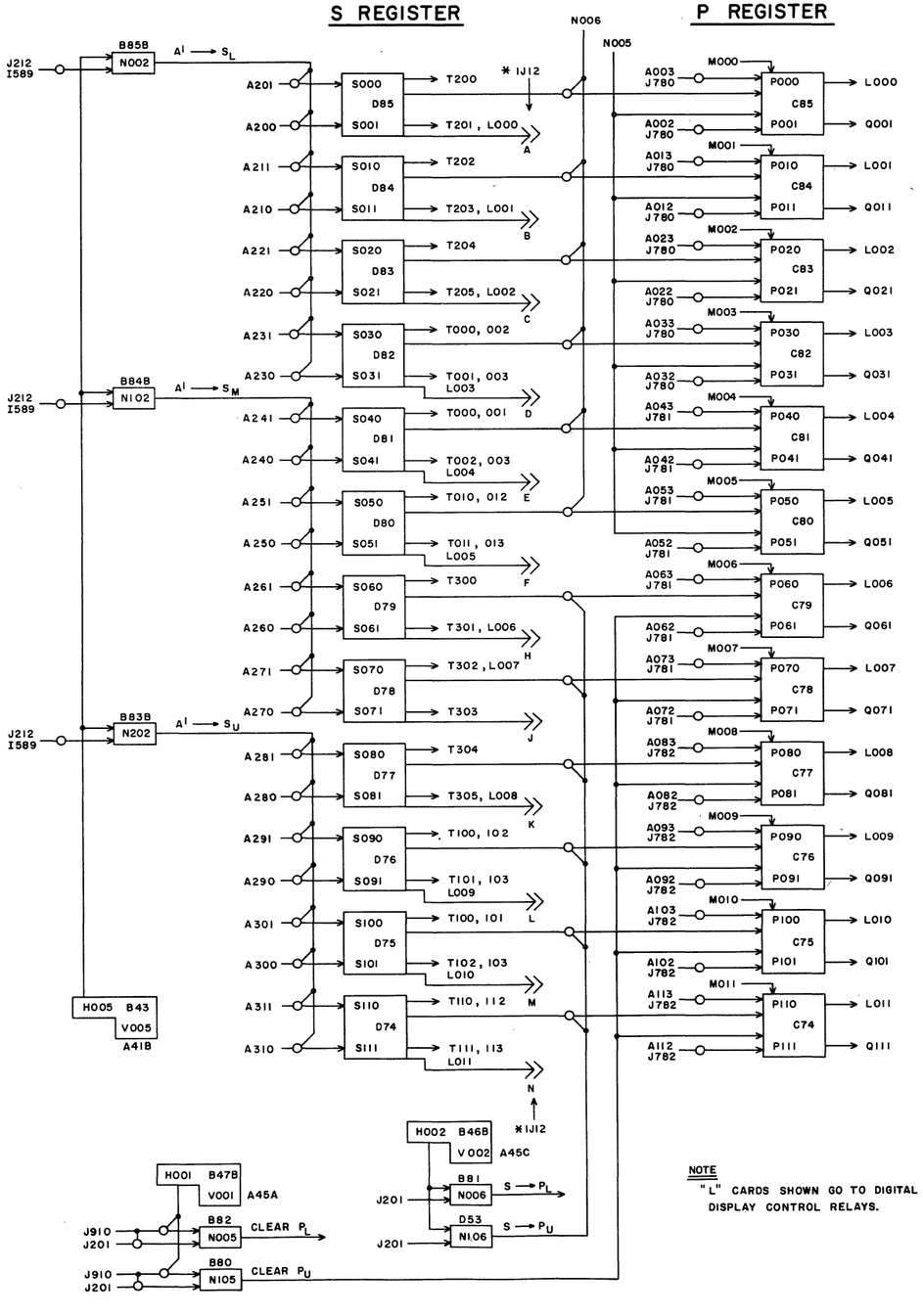
PROJECT OR PRODUCT
160-A

DRAWING NUMBER
20300700 A

PAGE 7

TERM	LOCATION	PAGE	DEFINITION
A002	E80A	7	$\overline{\text{Bit 0}}$
A003	E80C	7	Bit 0
A012	E81A	7	$\overline{\text{Bit 1}}$
A013	E81C	7	Bit 1
A022	E82A	7	$\overline{\text{Bit 2}}$
A023	E82C	7	Bit 2
A032	E83A	7	$\overline{\text{Bit 3}}$
A033	E83C	7	Bit 3
A042	E84A	7	$\overline{\text{Bit 4}}$
A043	E84C	7	Bit 4
A052	E85A	7	$\overline{\text{Bit 5}}$
A053	E85C	7	Bit 5
A062	E87A	7	$\overline{\text{Bit 6}}$
A063	E87C	7	Bit 6
A072	E88A	7	$\overline{\text{Bit 7}}$
A073	E88C	7	Bit 7
A082	E89A	7	$\overline{\text{Bit 8}}$
A083	E89C	7	Bit 8
A092	E90A	7	$\overline{\text{Bit 9}}$
A093	E90C	7	Bit 9
A102	E91A	7	$\overline{\text{Bit 10}}$
A103	E91C	7	$\overline{\text{Bit 10}}$
A112	E92A	7	$\overline{\text{Bit 11}}$
A113	E92C	7	$\overline{\text{Bit 11}}$
			} A Register
A200	C73A	11	$\overline{\text{Bit 0}}$
A201	C73C	11	Bit 0
A210	C72A	11	$\overline{\text{Bit 1}}$
A211	C72C	11	Bit 1
A220	C71A	11	$\overline{\text{Bit 2}}$
A221	C71C	11	$\overline{\text{Bit 2}}$
A230	C70A	11	$\overline{\text{Bit 3}}$
A231	C70C	11	Bit 3
A240	C69A	11	$\overline{\text{Bit 4}}$
A241	C69C	11	$\overline{\text{Bit 4}}$
A250	C68A	11	$\overline{\text{Bit 5}}$
A251	C68C	11	Bit 5
A260	C67A	11	$\overline{\text{Bit 6}}$
A261	C67C	11	Bit 6
A270	C66A	11	$\overline{\text{Bit 7}}$
A271	C66C	11	Bit 7
A280	C65A	11	$\overline{\text{Bit 8}}$
A281	C65C	11	Bit 8
A290	C63A	11	$\overline{\text{Bit 9}}$
A291	C63C	11	Bit 9
A300	C62A	11	$\overline{\text{Bit 10}}$
A301	C62C	11	$\overline{\text{Bit 10}}$
A310	C61A	11	$\overline{\text{Bit 11}}$
A311	C61C	11	Bit 11
			} A^1 Register
I589	E63C	1	$\overline{\text{Buffer Cycle \& 1st quarter}}$
J201	C30A	3	$\overline{CL \rightarrow P,\ S \rightarrow P}$
J212	E32C	3	$\overline{A^1 \rightarrow S}$
J780	D64B	13	} $A \rightarrow P$
J781	F64B	13	
J782	E86B	13	
J910	D11B	1	$\overline{\text{Clear P}}$
J920	A116	1	MC
M000	A34A	27	Manual Set Bit 0
M001	A34B	27	Manual Set Bit 1
M002	A34C	27	Manual Set Bit 2
M003	A35A	27	Manual Set Bit 3
M004	A35B	27	Manual Set Bit 4
M005	A35C	27	Manual Set Bit 5
M006	A36A	27	Manual Set Bit 6
M007	A36B	27	Manual Set Bit 7
M008	A36C	27	Manual Set Bit 8
M009	A37A	27	Manual Set Bit 9
M010	A37B	27	Manual Set Bit 10
M011	A37C	27	Manual Set Bit 11
			} P Register
M910	A11C	27	Clear P

FORM 510



* IJ12 CONNECTS TO EXTERNAL MEMORY MODULE(S) WHEN USED.

NOTE
"L" CARDS SHOWN GO TO DIGITAL DISPLAY CONTROL RELAYS.

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

REV. AUTH. DATE REQ. DRW. CHK. APPROVED
REVISIONS
APPROVED
CHECKED
DRAWN R. R. M. 10-2-61
DESIGNED

CONTROL DATA CORPORATION

PROJECT OR PRODUCT 160-A

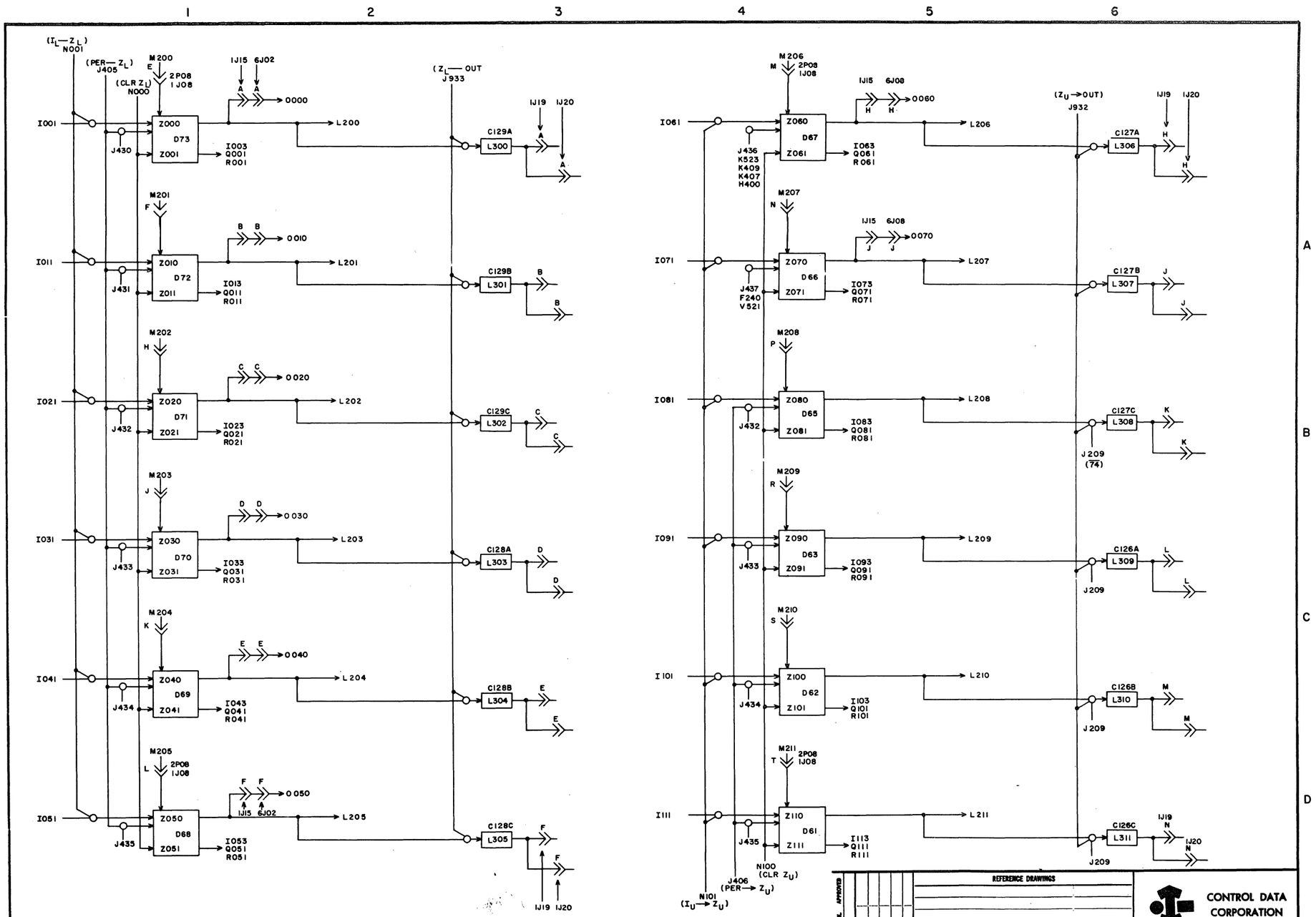
DRAWING NUMBER 20300800

PAGE 8

TITLE
LOGIC DIAGRAM
REGISTERS S AND P

TERM	LOCATION	PAGE	DEFINITION
F240	A08A	5	$\overline{75}$
H400	B03	17	Load Mode Control
I001	E123A	10	Bit 0
I011	E123C	10	Bit 1
I021	E122A	10	Bit 2
I031	E122C	10	Bit 3
I041	E121A	10	Bit 4
I051	E121C	10	Bit 5
I061	E120A	10	Bit 6
I071	E120C	10	Bit 7
I081	E119A	10	Bit 8
I091	E119C	10	Bit 9
I101	E118A	10	Bit 10
I111	E118C	10	Bit 11
			I--- Inverters
J209	D23A	3	$\overline{74}$
J405	E43	17	Enable Inputs to Z^0 - Z^5
J406	E12	17	Enable Inputs to Z^8 - Z^{11}
J430	E53A	17	Level 1
J431	E53C	17	Level 2
J432	E52A	17	Level 3
J433	E52C	17	Level 4
J434	E51A	17	Level 5
J435	E51C	17	Level 6
J436	B14A	17	Level 7
J437	A01C	17	Level 8
			Per Input
J932	C124	16	L306 - L311
J933	C125	16	L300 -- L305
			Output Cable Gates
K407	C06C	17	Clutch Control
K409	A10C	17	Sense 7th Level
K523	B22C	16	Sample
M200	A06A	27	Manual Set Bit 0
M201	A06B	27	Manual Set Bit 1
M202	A06C	27	Manual Set Bit 2
M203	A07A	27	Manual Set Bit 3
M204	A07B	27	Manual Set Bit 4
M205	A07C	27	Manual Set Bit 5
M206	A08A	27	Manual Set Bit 6
M207	A08B	27	Manual Set Bit 7
M208	A08C	27	Manual Set Bit 8
M209	A09A	27	Manual Set Bit 9
M210	A09B	27	Manual Set Bit 10
M211	A09C	27	Manual Set Bit 11
			Z Register
N000	D60B	1	Clear Z_L
N001	D59B	1	$I_L \rightarrow Z_L$
N100	D58B	1	Clear Z_U
N101	D57B	1	$I_U \rightarrow Z_U$
V521	C11B	16	Sample

FORM 510



NOTES:
1. "L2---" CARDS GO TO DIGITAL DISPLAY RELAYS.
2. "L3---" CARDS FEED THE NORMAL OUTPUT CABLE.

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

REVISIONS — REV. | AUTH. | DATE | ENG. APPR. | DRW. CHK. | APPROVED

APPROVED | CHECKED | DRAWN | DESIGNED

CONTROL DATA CORPORATION

PROJECT OR PRODUCT: 160-A

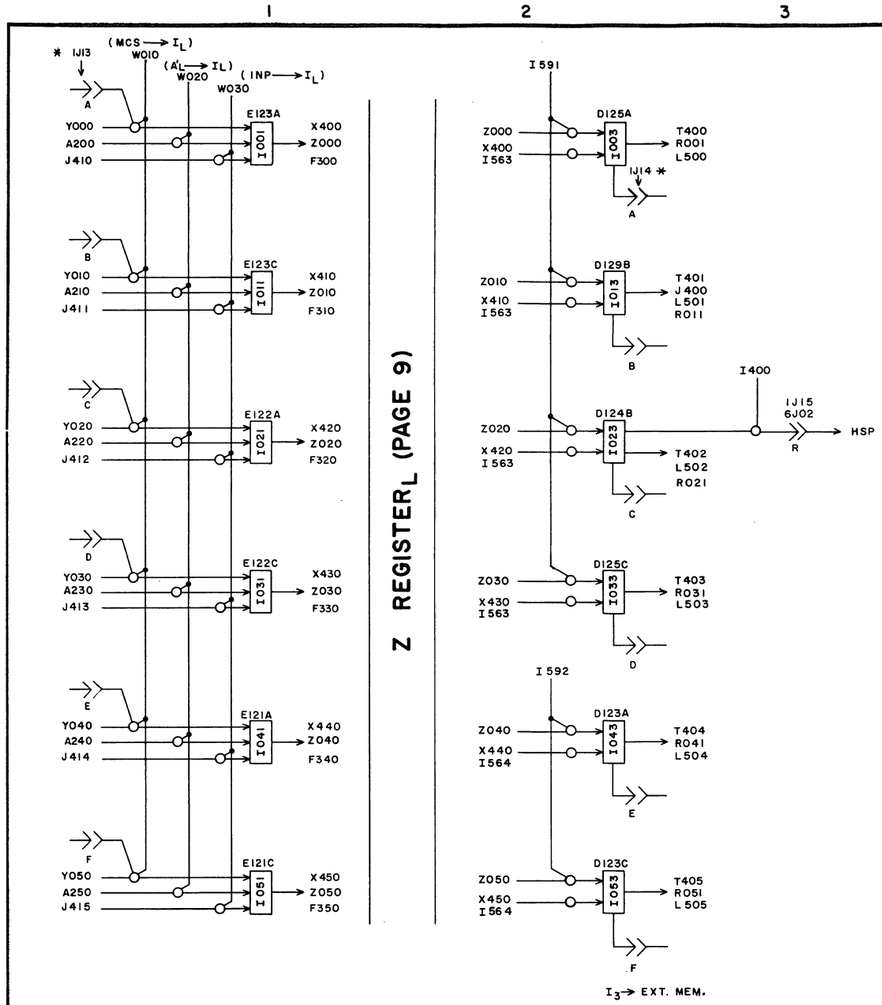
TITLE: Z REGISTER

DRAWING NUMBER: 20300900

PAGE 9

TERM	LOCATION	PAGE	DEFINITION
A200	C73A	11	$\overline{\text{Bit 0}}$
A210	C72A	11	$\overline{\text{Bit 1}}$
A220	C71A	11	$\overline{\text{Bit 2}}$
A230	C70A	11	$\overline{\text{Bit 3}}$
A240	C69A	11	$\overline{\text{Bit 4}}$
A250	C68A	11	$\overline{\text{Bit 5}}$
A260	C67A	11	$\overline{\text{Bit 6}}$
A270	C66A	11	$\overline{\text{Bit 7}}$
A280	C65A	11	$\overline{\text{Bit 8}}$
A290	C63A	11	$\overline{\text{Bit 9}}$
A300	C62A	11	$\overline{\text{Bit 10}}$
A310	C61A	11	$\overline{\text{Bit 11}}$
			} A^1 Register
I400	E39A	17	Select PER + Punch
I563	F104A	20	} BFR Cycle
I564	F105C	20	
I565	F105A	20	
I591	F58A	20	$\overline{\text{Buffer Cycle}}$
I592	F58C	20	$\overline{\text{Buffer Cycle}}$
I593	F59A	20	$\overline{\text{Buffer Cycle}}$
J410	E49A	17	$\overline{\text{Level 1}}$
J411	E49C	17	$\overline{\text{Level 2}}$
J412	E48A	17	$\overline{\text{Level 3}}$
J413	E48C	17	$\overline{\text{Level 4}}$
J414	E47A	17	$\overline{\text{Level 5}}$
J415	E47C	17	$\overline{\text{Level 6}}$
J430	E53A	17	$\overline{\text{Level 1}}$
J431	E53C	17	$\overline{\text{Level 2}}$
J432	E52A	17	$\overline{\text{Level 3}}$
J433	E52C	17	$\overline{\text{Level 4}}$
J434	E51A	17	$\overline{\text{Level 5}}$
J435	E51C	17	$\overline{\text{Level 6}}$ } PER Input
W010	E117	3	$\text{MCS} \rightarrow I_L$
W011	E116	3	$\text{MCS} \rightarrow I_U$
W020	E115	3	} $A^1 \rightarrow I$
W021	E114	3	
W030	E113	3	} $\text{INP} \rightarrow I$
W031	E112	3	
X400	F88A	21	$\overline{\text{Bit 0}}$
X410	F89A	21	$\overline{\text{Bit 1}}$
X420	F90A	21	$\overline{\text{Bit 2}}$
X430	F91A	21	$\overline{\text{Bit 3}}$
X440	F92A	21	$\overline{\text{Bit 4}}$
X450	F93A	21	$\overline{\text{Bit 5}}$
X460	F94A	21	$\overline{\text{Bit 6}}$
X470	F95A	21	$\overline{\text{Bit 7}}$
X480	F96A	21	$\overline{\text{Bit 8}}$
X490	F97A	21	$\overline{\text{Bit 9}}$
X500	F98A	21	$\overline{\text{Bit 10}}$
X510	F99A	21	$\overline{\text{Bit 11}}$ } Buffer Data Register
Y000	C98		Bit 0
Y010	C97		Bit 1
Y020	C96		Bit 2
Y030	C95		Bit 3
Y040	C94		Bit 4
Y050	C93		Bit 5
Y060	C92		Bit 6
Y070	C91		Bit 7
Y080	C90		Bit 8
Y090	C89		Bit 9
Y100	C88		Bit 10
Y110	C87		Bit 11 } Sense Amps
Z000	D73A	9	$\overline{\text{Bit 0}}$
Z010	D72A	9	$\overline{\text{Bit 1}}$
Z020	D71A	9	$\overline{\text{Bit 2}}$
Z030	D70A	9	$\overline{\text{Bit 3}}$
Z040	D69A	9	$\overline{\text{Bit 4}}$
Z050	D68A	9	$\overline{\text{Bit 5}}$
Z060	D67A	9	$\overline{\text{Bit 6}}$
Z070	D66A	9	$\overline{\text{Bit 7}}$
Z080	D65A	9	$\overline{\text{Bit 8}}$
Z090	D63A	9	$\overline{\text{Bit 9}}$
Z100	D62A	9	$\overline{\text{Bit 10}}$
Z110	D61A	9	$\overline{\text{Bit 11}}$ } Z Register

FORM 510



* IJ13 & IJ14 ARE CONNECTED TO EXTERNAL MEMORY MODULE(S) WHEN USED.

SENSE AMPLIFIERS	
SYMBOL	LOCATION
Y000	C98
Y010	C97
Y020	C96
Y030	C95
Y040	C94
Y050	C93
Y060	C92
Y070	C91
Y080	C90
Y090	C89
Y100	C88
Y110	C87

REV. | AUTH. | DATE | BGD. | DRW. | CHK. | APPROVED
REVISIONS
APPROVED
CHECKED
DRAWN
DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE I--- INVERTERS

CONTROL DATA CORPORATION

PROJECT OR PRODUCT 160-A

DRAWING NUMBER 20301000

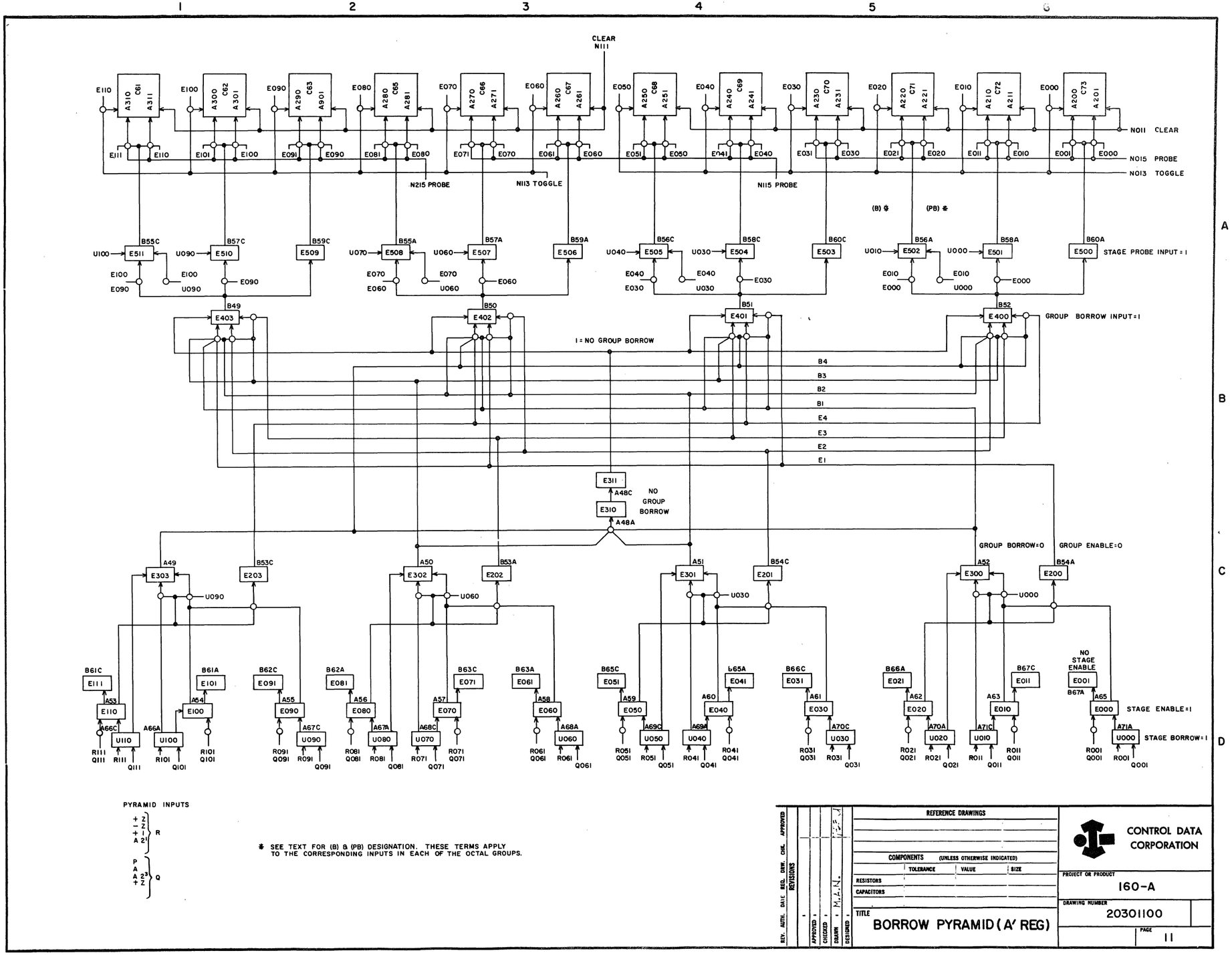
PAGE 10

TERM	LOCATION	PAGE	DEFINITION
N011	D56	1	Clear A^1
N013	D55	1	Toggle A^1
N015	D54B	1	Probe A^1
N111	D52	1	Clear A^1
N113	D51	1	Toggle A^1
N115	D50B	1	Probe A^1
N215	D49B	1	Probe A^1
Q001	B79	12	Bit 0
Q011	B78	12	Bit 1
Q021	B77	12	Bit 2
Q031	B76	12	Bit 3
Q041	B75	12	Bit 4
Q051	B74	12	Bit 5
Q061	B73	12	Bit 6
Q071	B72	12	Bit 7
Q081	B71	12	Bit 8
Q091	B70	12	Bit 9
Q101	B69	12	Bit 10
Q111	B68	12	Bit 11
R001	E60A	12	Bit 0
R011	E60C	12	Bit 1
R021	E59A	12	Bit 2
R031	E59C	12	Bit 3
R041	E58A	12	Bit 4
R051	E58C	12	Bit 5
R061	E57A	12	Bit 6
R071	E57C	12	Bit 7
R081	E56A	12	Bit 8
R091	E56C	12	Bit 9
R101	E55A	12	Bit 10
R111	E55C	12	Bit 11

Q Inverters

R Inverters

FORM 510



REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

REV. AUTH. DATE REQ. DRW. CHK. APPROVED

REVISIONS

APPROVED

CHECKED

DRAWN M.A.N.

DESIGNED

TITLE

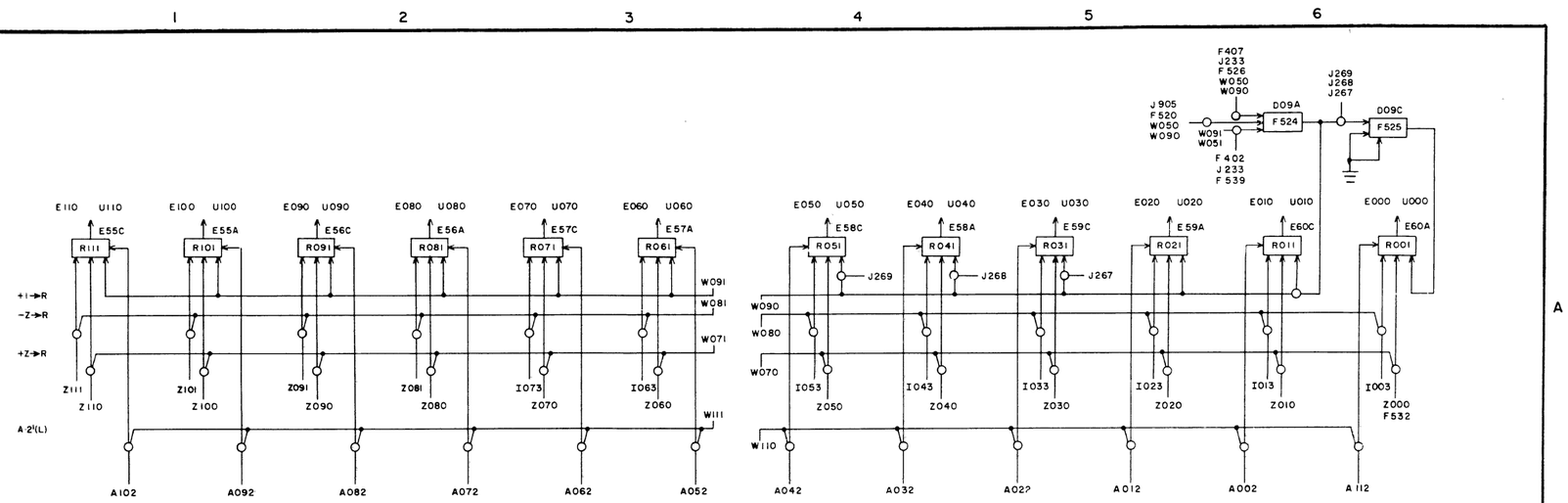
BORROW PYRAMID (A' REG)

CONTROL DATA CORPORATION

PROJECT OR PRODUCT 160-A

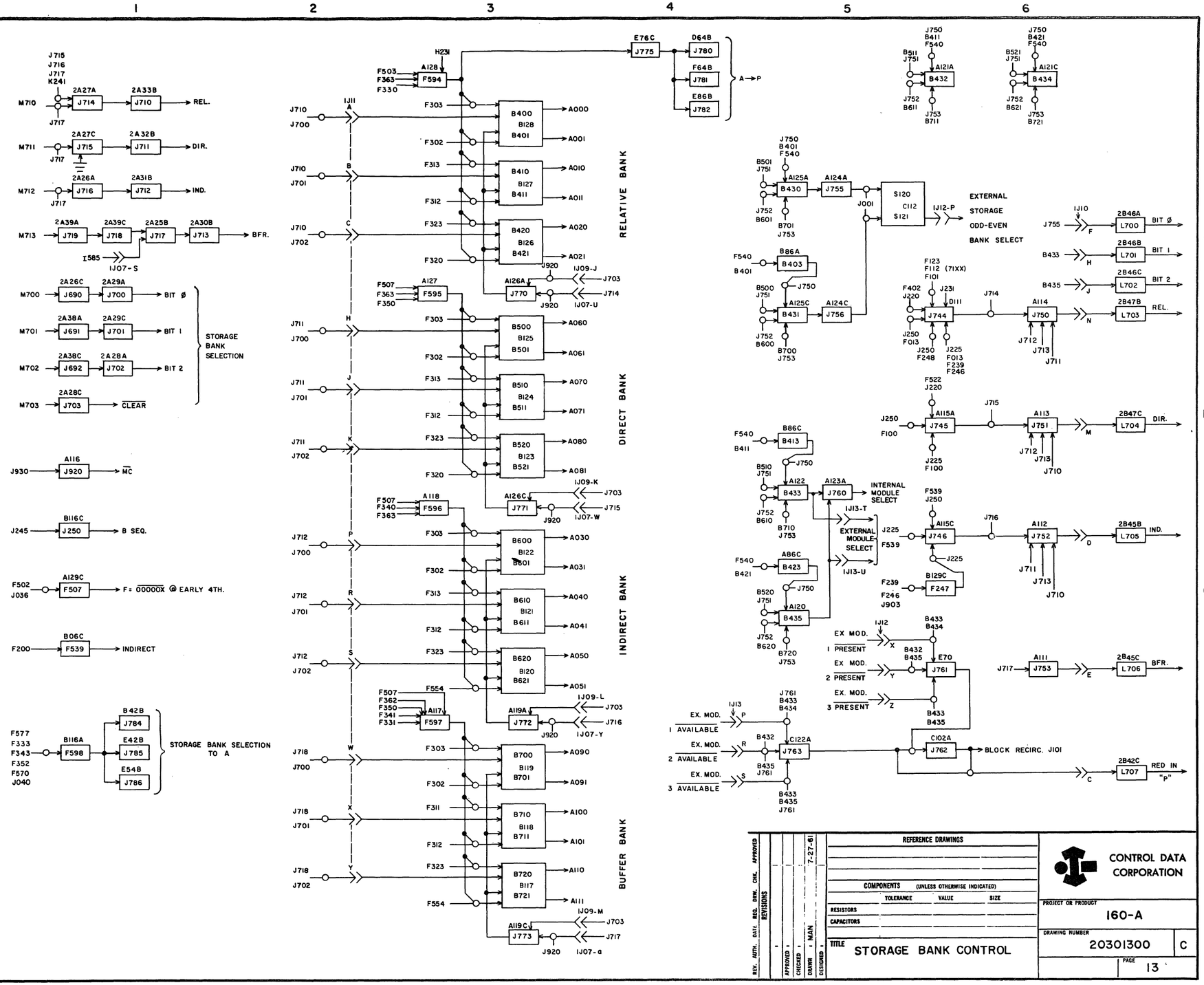
DRAWING NUMBER 20301100

PAGE 11


F407 J233 F526 W050 W090
J905 F520 W050 W090
W091 W051
F402 J233 F539
D09A F524
D09C F525
J269 J268 J267
E110 U110 E100 U100 E090 U090 E080 U080 E070 U070 E060 U060
E55C E55A E56C E56A E57C E57A
R111 R101 R091 R081 R071 R061
+I→R
-Z→R
+Z→R
A·2^I(L)
W091 W081 W071 W111
Z111 Z110 Z101 Z100 Z091 Z090 Z081 Z080 I073 Z070 I063 Z060
A102 A092 A082 A072 A062 A052
E050 U050 E040 U040 E030 U030 E020 U020 E010 U010 E000 U000
E58C E58A E59C E59A E60C E60A
R051 R041 R031 R021 R011 R001
J269 J268 J267
W090 W080 W070 W110
I053 I043 I033 I023 I013 I003
Z050 Z040 Z030 Z020 Z010 Z000 F532
A042 A032 A022 A012 A002 A112
I513 (BER→Q)
E110 U110 E100 U100 E090 U090 E080 U080 E070 U070 E060 U060
B68 B69 B70 B71 B72 B73
Q111 Q101 Q091 Q081 Q071 Q061
BER→Q
A·2^I(L)
Z→Q
P→Q
A→Q
A·2^I(R)
I512 W101 W061 W051 W041 W121
X110 X100 X090 X080 X070 X060
A080 A070 A060 A050 A040 A030
Z110 Z100 Z090 Z080 Z070 Z060
P110 P100 P090 P080 P070 P060
A110 A100 A090 A080 A070 A060
A112 A112 A102 A092 A082 A072
I511 (BER→Q)
E050 U050 E040 U040 E030 U030 E020 U020 E010 U010 E000 U000
B74 B75 B76 B77 B78 B79
Q051 Q041 Q031 Q021 Q011 Q001
I512
W100 W050 W040 W120
X050 X040 X030 X020 X010 X000
A020 A010 A000 A110 A100 A090
Z050 Z040 Z030 Z020 Z010 Z000
P050 P040 P030 P020 P010 P000
A050 A040 A030 A020 A010 A000
A062 A052 A042 A032 A022 A012
A
B
C
D
REFERENCE DRAWINGS
COMPONENTS (UNLESS OTHERWISE INDICATED)
TOLERANCE VALUE SIZE
RESISTORS
CAPACITORS
TITLE
R AND Q INVERTERS
REV. AUTH. DATE REVISIONS APPROVED CHK. DRAW. REQ. APPROVED CHECKED DRAWN DESIGNED
CONTROL DATA CORPORATION
PROJECT OR PRODUCT
160-A
DRAWING NUMBER
20301200 A
PAGE
12

TERM	LOCATION	PAGE	DEFINITION
F013	E38C	4	Bit 2 F Register
F100	E34	4	XXXX00
F101	E33	4	XXXX01
F112	E29	4	XX10XX
F123	E25	4	11XXXX
F200	D33B	5	Indirect } Function Translators
F230	C08A	5	$\overline{73}$
F246	C43C	5	$\overline{72}$
F248	C102C	5	75
F302	E111C	6	$\overline{\text{Bit 0}}$
F303	E111A	6	Bit 0
F311	F127	6	$\overline{\text{Bit 1}}$
F312	F118A	6	Bit 1
F313	F113C	6	Bit 1
F320	F126A	6	$\overline{\text{Bit 2}}$
F323	C119A	6	Bit 2
F330	F125A	6	$\overline{\text{Bit 3}}$
F331	F125C	6	Bit 3 } F^1 Register
F333	F129C	6	Bit 3
F340	F124A	6	$\overline{\text{Bit 4}}$
F341	F124C	6	Bit 4
F343	B129A	6	$\overline{\text{Bit 4}}$
F350	F123A	6	$\overline{\text{Bit 5}}$
F352	E64A	6	$\overline{\text{Bit 5}}$
F362	E105A	6	$\overline{\text{Bit 6}}$
F363	E105C	6	Bit 6
F402	D05C	6	XX00
F502	F111C	6	00000X
F503	F111A	6	$\overline{\text{00000X}}$
F507	A129C	6	$\overline{\text{00000X}}$ 4th quarter
F522	B17C	6	$\overline{XX00_8}$
F539	B06C	13	Indirect
F540	D86B	6	$\overline{\text{Specific ADD}}$
F554	C116A	6	$\overline{\text{Bit 2}}$
F570	B112B	6	$XXX0_8$
F577	E77C	5	01 3rd Or 4th quarter
H231	B30	2	D Cycle Timing
I585	B25C	20	Storage Sequence Interrupt
J001	C39B	2	1 quarter
J036	E04C	2	E-4 quarter
J040	D01C	2	E-4 quarter
J220	C86C	2	A Cycle
J225	C86A	2	C Cycle
J231	B07B	2	D Cycle
J245	E15A	2	$\overline{\text{B Cycle}}$
J250	B116C	2	B Cycle
J903	C18B	1	$\overline{\text{Load}}$
J930	C08C	1	MC
K241	A24C	1	Block +1 → R
M700	A42B	22	Bit 0
M701	A42C	22	Bit 1
M702	A43A	22	Bit 2 SBC
M703	A42A	22	SBC Clear
M710	A43B	22	Rel } Manual SB Controls
M711	A44B	22	Dir
M712	A44A	22	Ind
M713	A43C	22	BFR

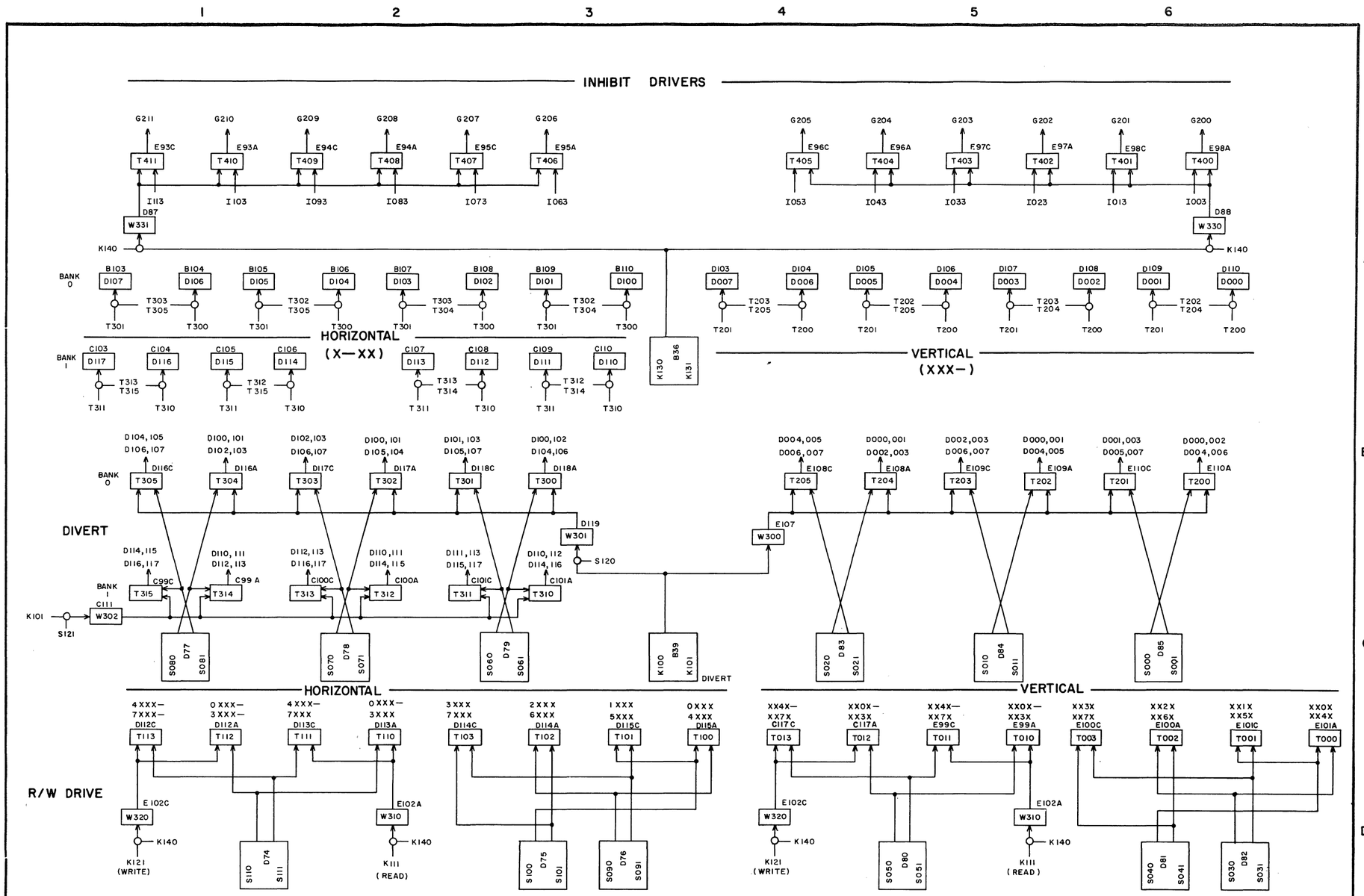
FORM 510



TERM	LOCATION	PAGE	DEFINITION
I003	D125A	10	Bit 0
I013	D129B	10	Bit 1
I023	D124B	10	Bit 2
I033	D125C	10	Bit 3
I043	D123A	10	Bit 4
I053	D123C	10	Bit 5
I063	D126B	10	Bit 6
I073	D122B	10	Bit 7
I083	D121A	10	Bit 8
I093	D121C	10	Bit 9
I103	C121C	10	Bit 10
I113	D120B	10	Bit 11
K101	B39C	2	Divert
K111	B38C	2	Read
K121	B37C	2	Write
K140	B35A	2	Main Timing Fault
S120	C112A	13	Ext. Stor. ODD-EVEN Select.
S121	C112C	13	Ext. Stor. ODD-EVEN Select.

I--- Inverters

FORM 510



NOTE:
LOW—ORDER DIGIT IN DESTINATION SYMBOL SIGNIFIES MAGNITUDE OF DIVERTER LINE SELECTED. THUS:
D104,105= X4XX OR X5XX
D106,107= X6XX OR X7XX
OUTPUT DESIGNATIONS FROM T305, AND T205 = XXX4, XXX5, XXX6, XXX7

REV.	AUTH.	DATE	REVISIONS	REQ.	DRW.	CHK.	APPROVED
							7-13-61

DESIGNED • R. SIMMONS
DRAWN •
CHECKED •
APPROVED •

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
STORAGE TRANSLATORS

CONTROL DATA CORPORATION

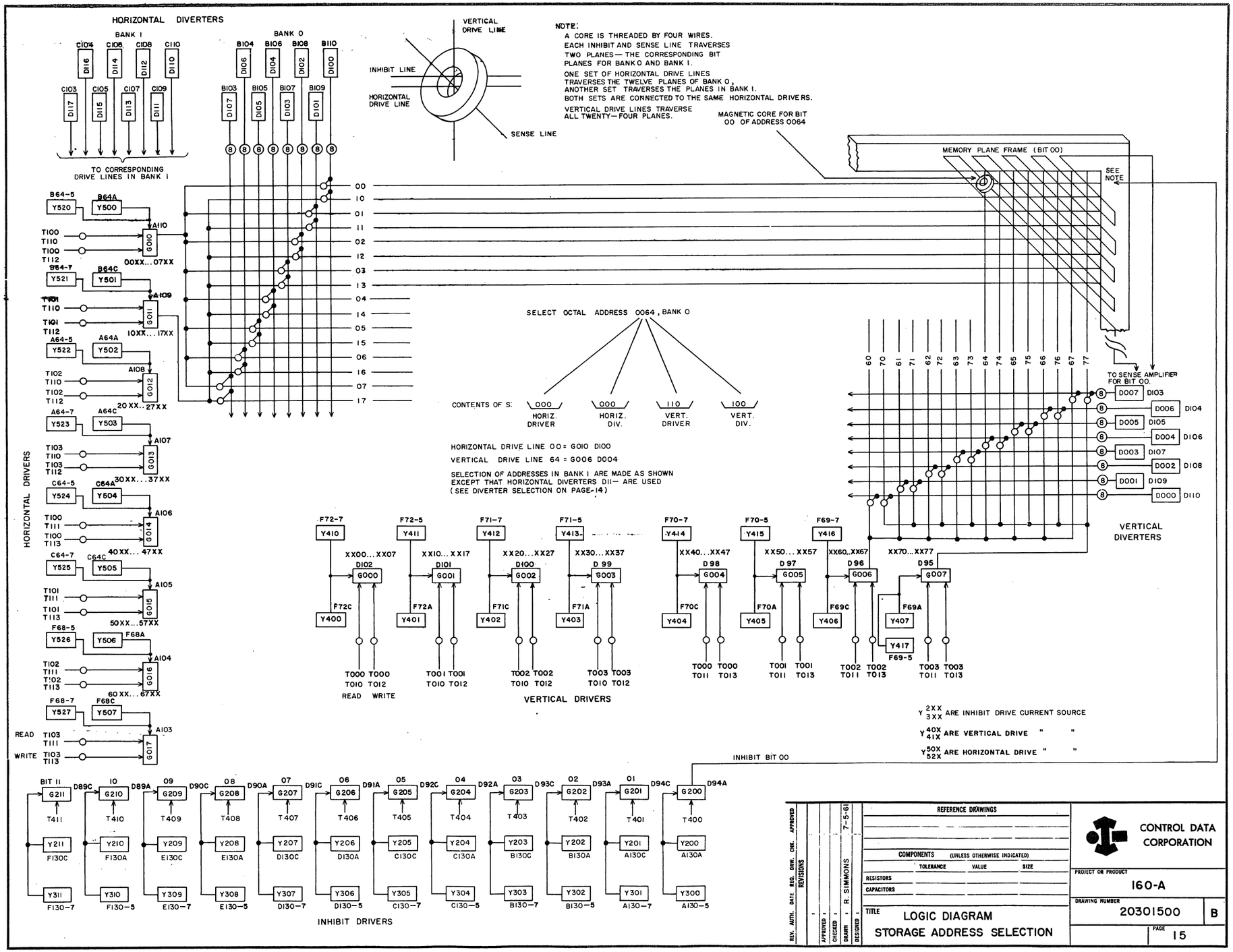
PROJECT OR PRODUCT
160-A

DRAWING NUMBER
20301400

PAGE
14

TERM	LOCATION	PAGE	DEFINITION	
T000	E101A	14	XX0X, XX4X	Vertical Translators
T001	E101C	14	XX1X, XX5X	
T002	E100A	14	XX2X, XX6X	
T003	E100C	14	XX3X, XX7X	
T010	E99A	14	XX0X-XX3X	
T011	E99C	14	XX4X-XX7X	
T012	C117A	14	XX0X-XX3X	
T013	C117C	14	XX4X-XX7X	
T100	D115A	14	0XXX, 4XXX	Horizontal Translators
T101	D115C	14	1XXX, 5XXX	
T102	D114A	14	2XXX, 6XXX	
T103	D114C	14	3XXX, 7XXX	
T110	D113A	14	0XXX-3XXX	
T111	D113C	14	4XXX-7XXX	
T112	D112A	14	0XXX-3XXX	
T113	D112C	14	4XXX-7XXX	
T400	E98A	14	Bit 0	Inhibit Drivers
T401	E98C	14	Bit 1	
T402	E97A	14	Bit 2	
T403	E97C	14	Bit 3	
T404	E96A	14	Bit 4	
T405	E96C	14	Bit 5	
T406	E95A	14	Bit 6	
T407	E95C	14	Bit 7	
T408	E94A	14	Bit 8	
T409	E94C	14	Bit 9	
T410	E93A	14	Bit 10	
T411	E93C	14	Bit 11	

FORM 510



REV.	AUTH.	DATE	REVISIONS
-			

APPROVED =
CHECKED = R. SIMMONS 7-5-61
DRAWN =
DESIGNED =

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE: LOGIC DIAGRAM STORAGE ADDRESS SELECTION

CONTROL DATA CORPORATION

PROJECT OR PRODUCT: 160-A

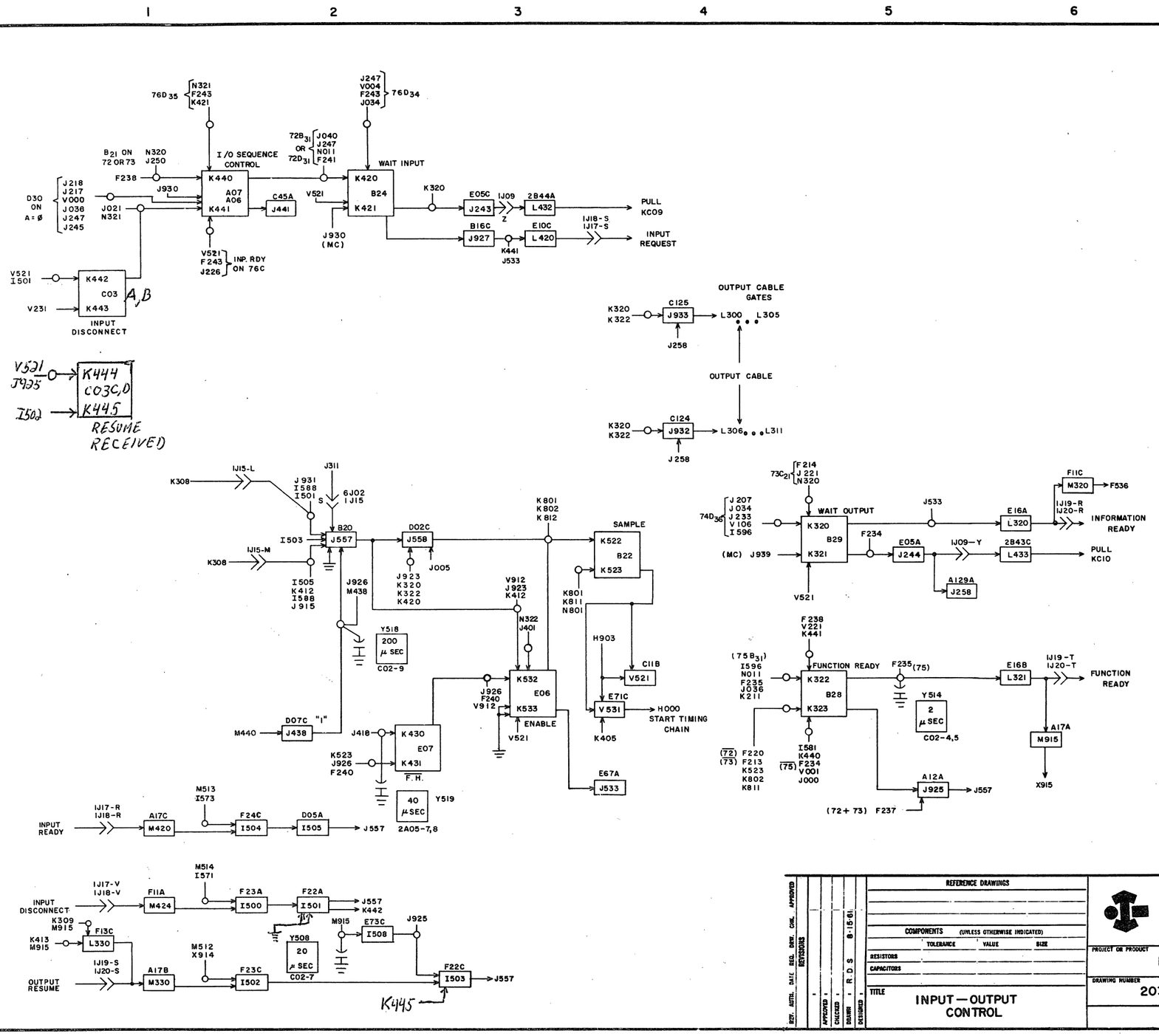
DRAWING NUMBER: 20301500 B

PAGE 15

NOTE: Terms not in complete alphanumeric order.

TERM	LOCATION	PAGE	DEFINITION
F213	D24B	5	$\overline{73}$
F214	D08C	5	73
F220	D19C	5	$\overline{72}$
F221	C25A	5	72
F234	D12A	5	$\overline{75}$
F235	D12C	5	75
F238	D10C	5	72, 73
F239	C08A	5	$\overline{73}$
F240	A08A	5	$\overline{75}$
F241	C09C	5	72
F243	A08C	5	76
F237	D10A	5	72, 73
F535	E02B	6	$\overline{7677}$
H903	A26	2	Odd Resync Timing
I571	F20A	20	Buffer Cable To Input
I573	F19A	20	Buffer Cable To Input
I581	F56C	20	Storage Sequence Interrupt
I588	A21A	20	Buffer Step
I596	B23A	20	Buffer Cycle
J000	E22B	2	E-1 quarter
J005	E72A	2	1 quarter
J021	B26B	2	3 quarter
J032	C34B	2	4 quarter
J034	C33A	2	4 quarter
J036	E04C	2	E-4 quarter
J038	E19C	2	4 quarter
J040	D01C	2	E-4 quarter
J100	C45C	1	Step Or Run
J207	D23C	3	$\overline{74}$
J208	C26A	3	74
J217	C41B	3	$A_L = 0$
J218	C40B	3	$A_U = 0$
J221	B08B	2	C & Buffer Cycle
J226	E21C	2	C Cycle
J233	E08A	2	D Cycle
J245	E15A	2	B Cycle
J246	E15C	2	A & B Cycles
J247	E04A	2	B & D Cycles
J250	B116C	2	B Cycle
J311	6A08A	18	Z → 0
J401	E39C	17	Select PER
J418	D07A	17	F. H. PER Input
J915	B18A	1	Load
J923	C28C	1	Load
J926	B16A	17	Select PER Or Load
J930	C08C	1	MC
J931	D06A	17	Per and Load
J939	C21C	1	MC
K211	A30C	2	B Cycle
K308	6C07A	18	Select HSP
K405	C07C	17	Load Mode Control
K407	C06C	17	Clutch Control
K412	C05A	17	Select PER
K801	A23C	2	Resync Counter
K802	A22A	2	Resync Counter
K811	A20C	2	Resync Counter
K812	A19A	2	Resync Counter
M438	E44C	17	Feed Hole
M440	F11B	17	Clear Load Mode Stop
M512	F14A	20	Output Resume
M513	F14B	20	Input Ready
M514	F14C	20	Input Disconnect
N011	D56	1	Clear A[1]
N320	B27B	1	External Probe
N321	E37B	1	D Cycle X5
N322	A09B	2	B Cycle 75 Instruction
N801	A18C	2	RK1 → RK2 Resync Counter
V000	A46B	1	TX0 } Timing Chain
V001	A45A	1	TX1 } Timing Chain
V004	A44C	1	TX4 } Timing Chain
V106	F21A	20	TX6 } Timing Chain
V211	A33	2	B Cycle
V221	A43C	2	C Cycle
V231	A32B	2	D Cycle
V902	C13A	2	Resync Timing X6
V912	C10C	2	Resync Timing X6
X914	F16A	20	Buffer Busy
K309	6C07C	18	Select HSP
K413	1C05C	17	Select PER

FORM 510



REFERENCE DRAWINGS			
COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

DES. AUTH. — DATE — REG. ENGR. CHG. — APPROVED
REVISIONS — - — APPROVED - — CHECKED - R. D. S 8-15-61 — DRAWN - — DESIGNED -

CONTROL DATA CORPORATION

PROJECT OR PRODUCT: 160-A

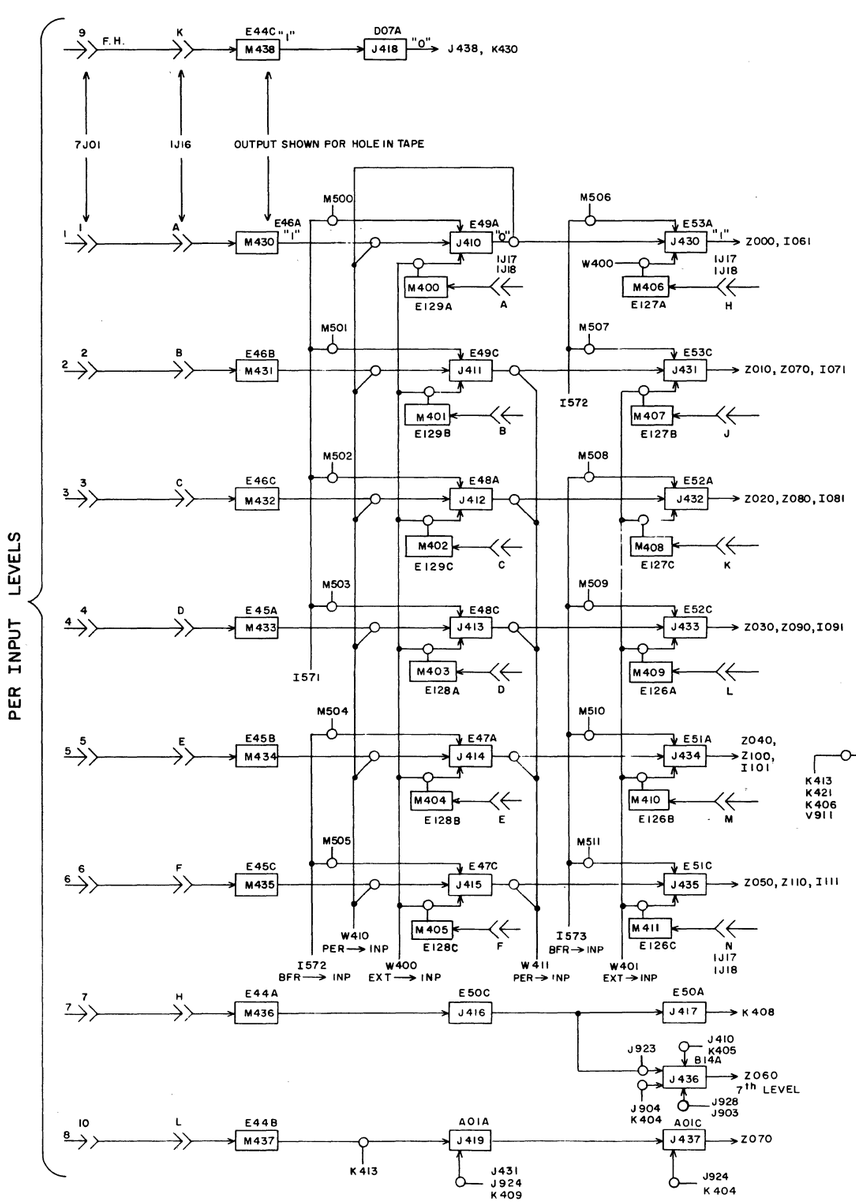
DRAWING NUMBER: 20301600 P

PAGE: 16

TITLE: INPUT—OUTPUT CONTROL

TERM	LOCATION	PAGE	DEFINITION
F100	E34	4	XXXX00
F103	E33	4	XXXX11
F110	E30	4	XX00XX — F Translators
F113	E28	4	XX11XX
F126	E23	4	11XXXX
F227	D16B	5	0X
F361	F120C	6	Bit 6 F^{1} Register
F500	F110C	6	11111X
F508	E62C	6	Selective Stop
F513	E106A	6	XX00
F521	E13A	6	XX77, XX00
I013	D129B	10	Bit 1 I^{---3} Inverters
I023	D124B	10	Bit 2
I063	D126B	10	Bit 6
I073	D122B	10	Bit 7
I083	D121A	10	Bit 8 — I^{---} Inverters
I093	D121C	10	Bit 9
I103	C121C	10	Bit 10
I113	D120B	10	Bit 11
I571	F20A	20	Buffer Cable to Input
I572	F19C	20	Buffer Cable to Input
I573	F19A	20	BFR Cable to Input
J100	C45C	1	Step Or Run
J214	B19A	2	Memory Voltages Ok
J901	C20B	1	MC
J903	C18B	1	$\overline{\text{Load}}$
J904	C17A	1	Load
J911	C23C	1	$\overline{\text{Clear A}}$
J914	C09A	1	Load
J916	C42C	1	Load + Enter + Sweep
J923	C28C	1	$\overline{\text{Load}}$
J924	B18C	1	Load
K421	B24C	16	Wait Input
K431	E07C	16	$\overline{\text{F. H.}}$
K522	B22A	16	$\overline{\text{Sample}}$
K523	B22C	16	$\overline{\text{Sample}}$
K532	E06A	16	$\overline{\text{Enable}}$
K907	E03C	2	Program Step
N320	B27B	1	External Probe
N322	A09B	2	B Cycle 75
M500	F83A	21	Bit 0
M501	F83B	21	Bit 1
M502	F83C	21	Bit 2
M503	F84A	21	Bit 3
M504	F84B	21	Bit 4
M505	F84C	21	Bit 5
M506	F102A	21	Bit 6 — Buffer Cable
M507	F102B	21	Bit 7
M508	F102C	21	Bit 8
M509	F103A	21	Bit 9
M510	F103B	21	Bit 10
M511	F103C	21	Bit 11
V521	C11B	16	Odd Resync Time Sample
V531	E71C	16	Start Timing Chain
V911	B13C	2	Resync Time X5
W400	A02	3	Ext. → INP
W401	A03A	3	Ext. → INP
W410	A04	3	PER → INP
W411	A03C	3	PER → INP

FORM 510



REV.	AUTH.	DATE	REQ.	DRW.	CHK.	APPROVED
REVISIONS						

APPROVED -
CHECKED -
DRAWN - R.D.S. 8-11-61
DESIGNED -

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
INPUT

CONTROL DATA CORPORATION

PROJECT OR PRODUCT
160-A

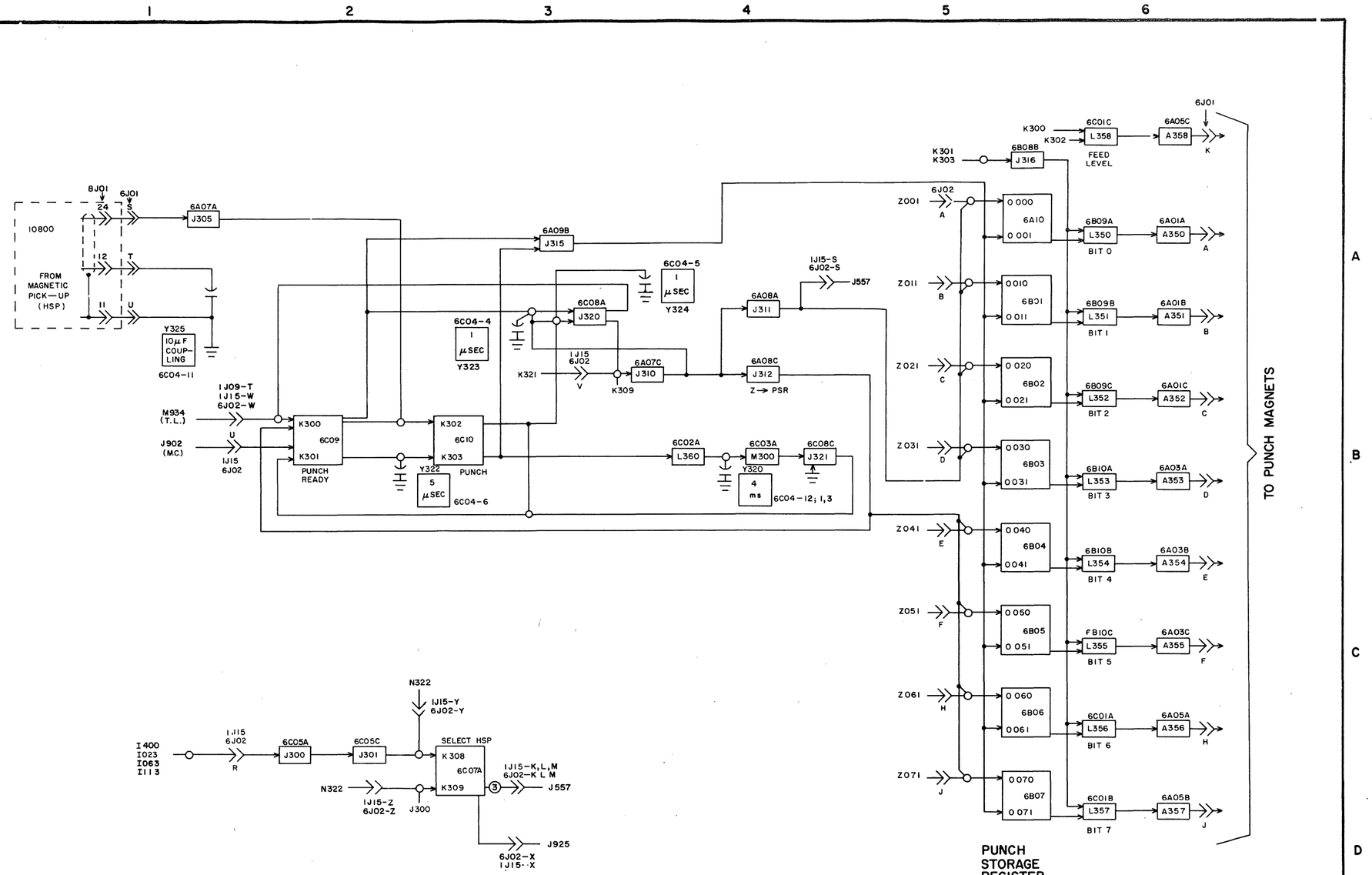
DRAWING NUMBER
20301700 F

PAGE
17

TERM	LOCATION	PAGE	DEFINITION
I023	D124B	10	Bit 3 I''' Inverters
I063	D126B	10	Bit 11 I''' Inverters
I113	D120B	10	Bit 6 I''' Inverters
I400	E73	17	HSP Select
J930	C08C	1	MC
K321	B29C	16	Wait Output
M934	A44C	22	Tape Leader
N322	A09B	2	B Cycle 75
Z001	D73C	9	Bit 0
Z011	D72C	9	Bit 1
Z021	D71C	9	Bit 2
Z031	D70C	9	Bit 3
Z041	D69C	9	Bit 4
Z051	D68C	9	Bit 5
Z061	D67C	9	Bit 6
Z071	D66C	9	Bit 7

Z Register

FORM 510



REV.	AUTH.	DATE	REQ. DRW. CHK. APPROVED REVISIONS
-			

APPROVED -
CHECKED -
DRAWN R. SIMMONS 7-11-61
DESIGNED -

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

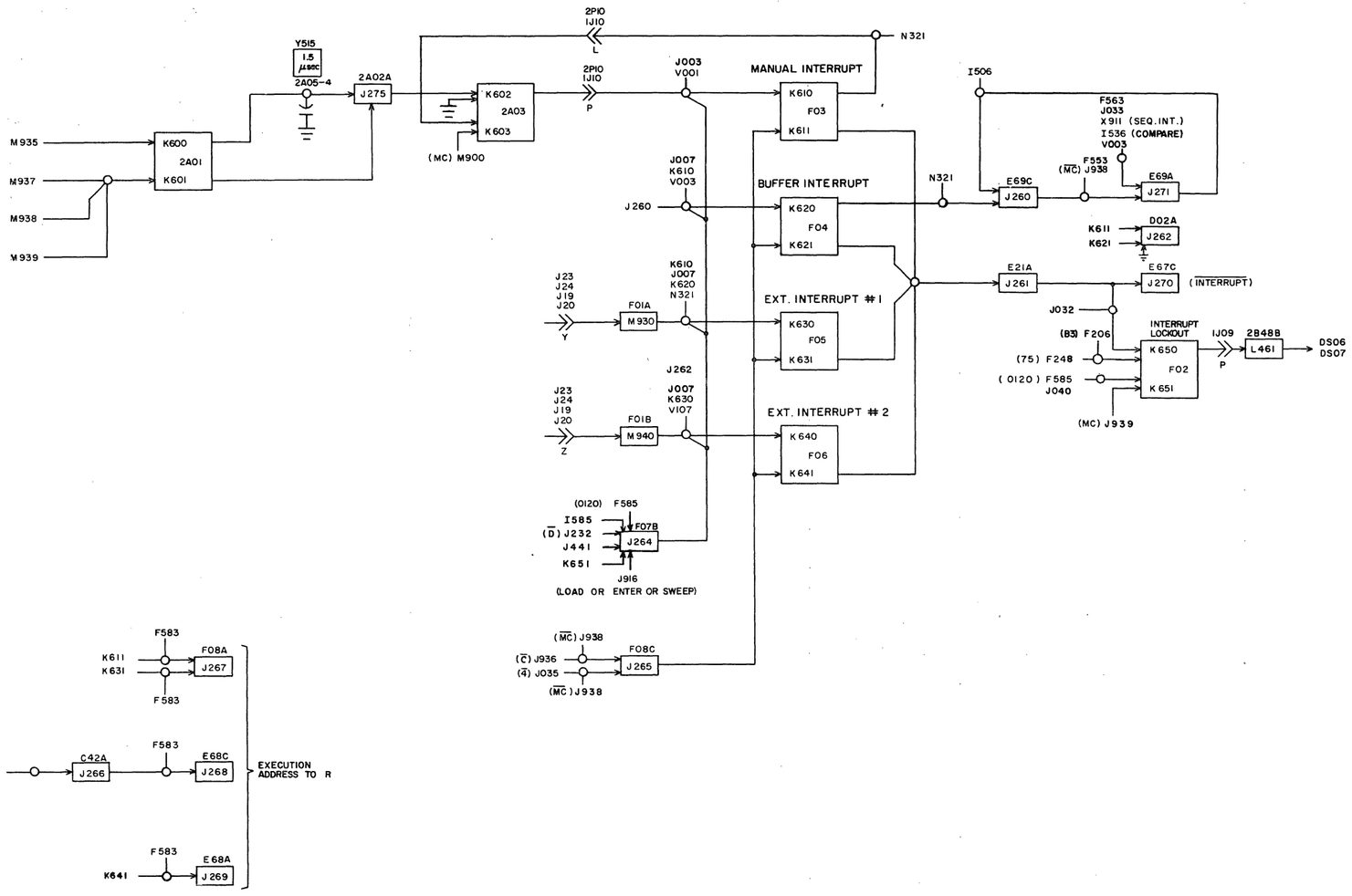
TITLE PUNCH OUTPUT

CONTROL DATA CORPORATION

PROJECT OR PRODUCT 160-A

DRAWING NUMBER 20301800 C

PAGE 18



REV.	AUTH.	DATE	BRD.	DRW.	CHK.	APPROVED
REVISIONS						
-						
APPROVED	-					
CHECKED	-					
DRAWN	-					
DESIGNED	-					

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE
INTERRUPT

CONTROL DATA CORPORATION

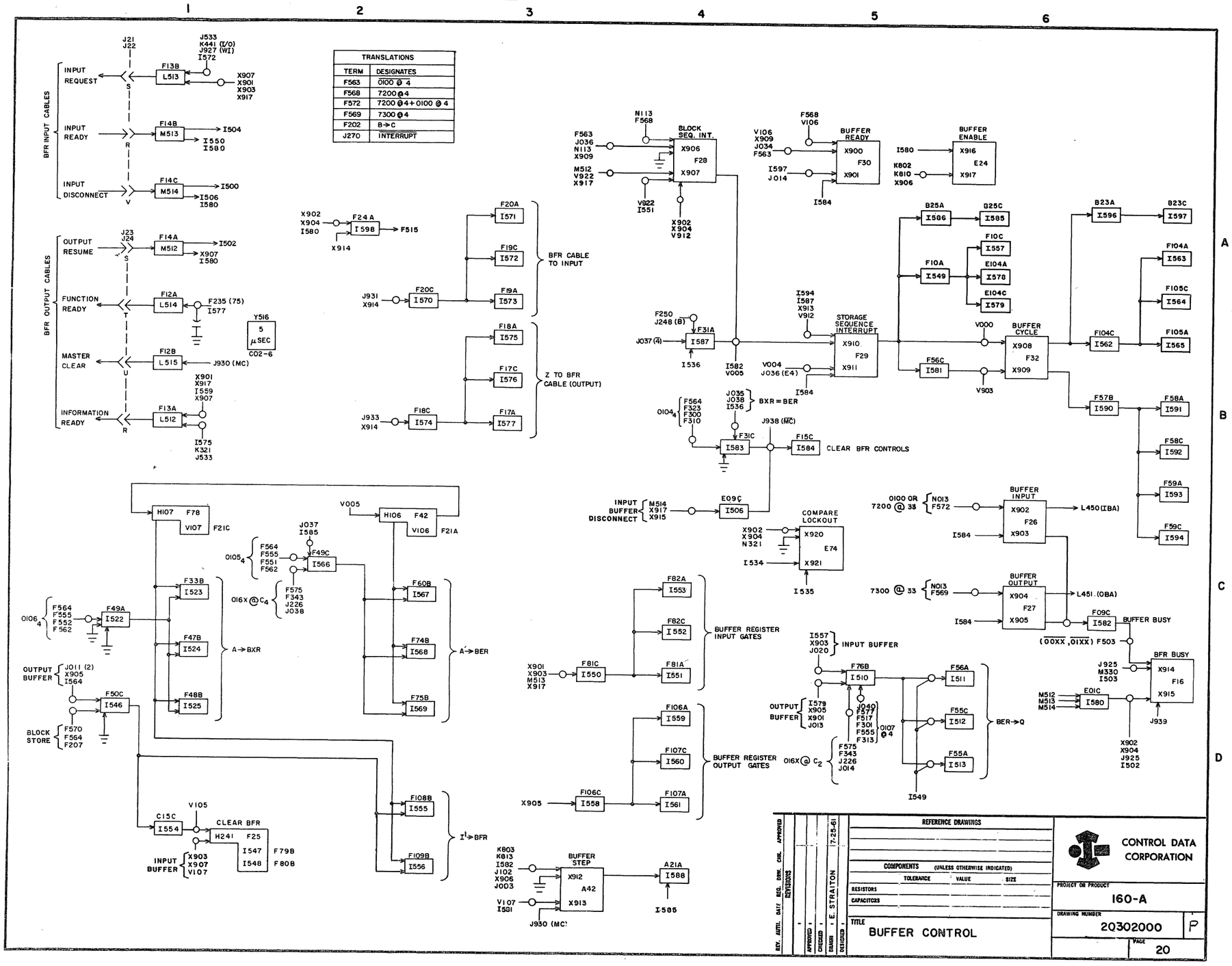
PROJECT OR PRODUCT
160-A

DRAWING NUMBER
20301900 N

PAGE
19

Note: Terms not in alpha-numeric order

TERM	LOCATION	PAGE	DEFINITION
F206	D26B	5	B_3
F248	C102C	5	75
F563	C123B	6	0100 4 quarter
F583	B21C	6	10, 20, 30, 40 → R
F585	B14C	6	0120_8
I506	E09C	20	Clear Buffer Controls
I536	F50A	21	Compare (BER = BXR)
I585	B25C	20	Storage Sequence Interrupt
J003	D08A	2	E1
J007	C13C	2	1 quarter
J032	C34B	2	4
J033	C33C	2	E-4 quarter
J035	D06C	2	E-4 quarter
J040	D01C	2	E-4 quarter
J232	E08C	2	D + Buffer Cycle
J441	C45A	16	I/O Seq. Control
J916	C42C	1	Load Or Enter Or Sweep
J936	C43A	2	C Or Buffer Cycle
J938	F09A	1	MC + RUN
J939	C21C	1	MC
M900	A13B	22	MC
M935	A13C	22	Man. Interrupt
M937	A14A	22	Selective Jump
M938	A14B	22	Selective Jump
M939	A14C	22	Selective Jump
N321	E37B		DX5 · BFR
V001	A45A	1	T-1
V003	A44A	1	T-3
V107	F21C	20	T-7
X911	F29C	20	Storage Seq. Interrupt
F553	B115A	6	7200 + 7300 + Forced 71XX



FORM 510

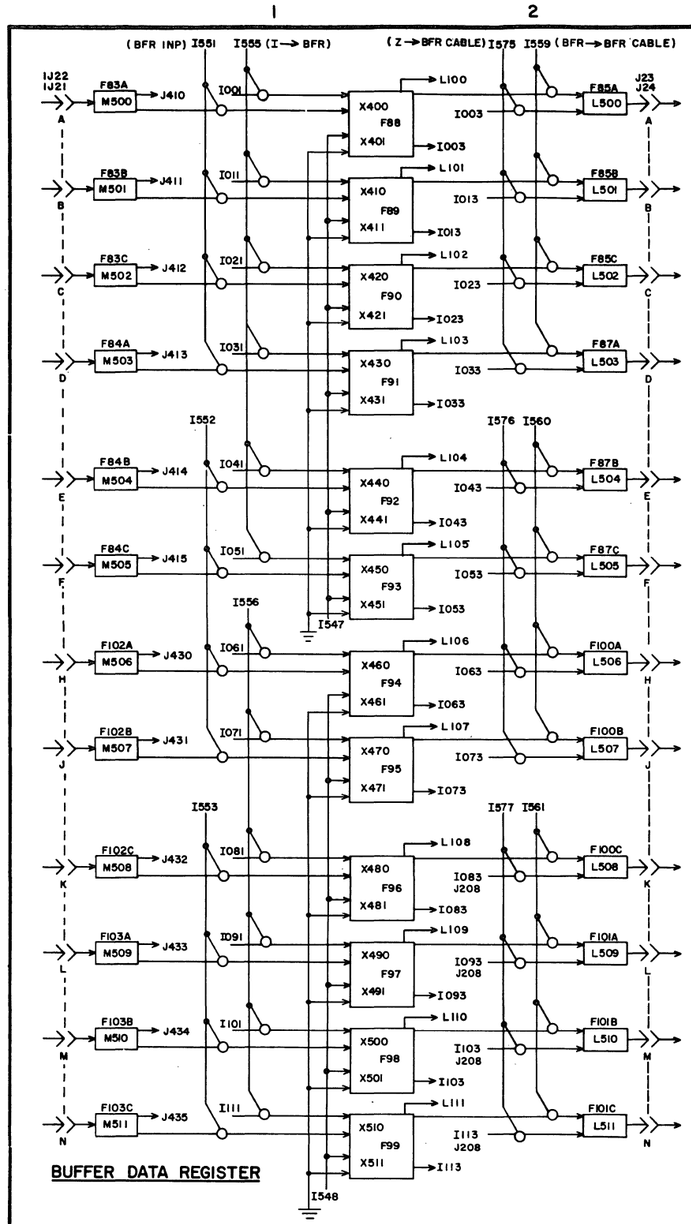
TERM	LOCATION	PAGE	DEFINITION
A002	E80A	7	Bit 0
A003	E80C	7	Bit 0
A012	E81A	7	Bit 1
A013	E81C	7	Bit 1
A022	E82A	7	Bit 2
A023	E82C	7	Bit 2
A032	E83A	7	Bit 3
A033	E83C	7	Bit 3
A042	E84A	7	Bit 4
A043	E84C	7	Bit 4
A052	E85A	7	Bit 5
A053	E85C	7	Bit 5
A062	E87A	7	Bit 6
A063	E87C	7	Bit 6
A072	E88A	7	Bit 7
A073	E88C	7	Bit 7
A082	E89A	7	Bit 8
A083	E89C	7	Bit 8
A092	E90A	7	Bit 9
A093	E90C	7	Bit 9
A102	E91A	7	Bit 10
A103	E91C	7	Bit 10
A112	E92A	7	Bit 11
A113	E92C	7	Bit 11
A200	C73A	11	Bit 0
A201	C73C	11	Bit 0
A210	C72A	11	Bit 1
A211	C72C	11	Bit 1
A220	C71A	11	Bit 2
A221	C71C	11	Bit 2
A230	C70A	11	Bit 3
A231	C70C	11	Bit 3
A240	C69A	11	Bit 4
A241	C69C	11	Bit 4
A250	C68A	11	Bit 5
A251	C68C	11	Bit 5
A260	C67A	11	Bit 6
A261	C67C	11	Bit 6
A270	C66A	11	Bit 7
A271	C66C	11	Bit 7
A280	C65A	11	Bit 8
A281	C65C	11	Bit 8
A290	C63A	11	Bit 9
A291	C63C	11	Bit 9
A300	C62A	11	Bit 10
A301	C62C	11	Bit 10
A310	C61A	11	Bit 11
A311	C61C	11	Bit 11
I001	E123A	10	Bit 0
I003	D125A	10	Bit 0
I011	E123C	10	Bit 1
I013	D129B	10	Bit 1
I021	E122A	10	Bit 2
I023	D124B	10	Bit 2
I031	E122C	10	Bit 3
I033	D125C	10	Bit 3
I041	E121A	10	Bit 4
I043	D123A	10	Bit 4
I051	E121C	10	Bit 5
I053	D123C	10	Bit 5
I061	E120A	10	Bit 6
I063	D126B	10	Bit 6
I071	E120C	10	Bit 7
I073	D122B	10	Bit 7
I081	E119A	10	Bit 8
I083	D121A	10	Bit 8
I091	E119C	10	Bit 9
I093	D121C	10	Bit 9
I101	E118A	10	Bit 10
I103	C121C	10	Bit 10
I111	E118C	10	Bit 11
I113	D120B	10	Bit 11
I523	F33B	20	A → BXR
I524	F47B	20	A → BXR
I525	F48B	20	A → BXR
I547	F79B	20	Clear Buffer
I548	F80B	20	Clear Buffer
I551	F81A	20	Buffer Input
I552	F82C	20	Buffer Input
I553	F82A	20	Buffer Input
I555	F108B	20	I → Buffer Register
I556	F109B	20	I → Buffer Register
I559	F106A	20	Buffer Register → Buffer Cable
I560	F107C	20	Buffer Register → Buffer Cable
I561	F107A	20	Buffer Register → Buffer Cable
I567	F60B	20	A^1 → BER
I568	F74B	20	A^1 → BER
I569	F75B	20	A^1 → BER
I575	F18A	20	Z → Buffer Cable
I576	F17C	20	Z → Buffer Cable
I577	F17A	20	Z → Buffer Cable
J208	C26A	3	7677
X921	E74C	20	Compare Lockout

A Register

A^1 Register

I Iverters

FORM 510



NOTES:
1. "LI--, L2--" CARDS SHOWN GO TO DIGITAL DISPLAY CONTROL RELAYS.
2. "L5--" SHOWN FEED THE BUFFER OUTPUT CABLE.

REV. APPR. | DATE | REQ. DRW. CHG. APPROVED | REVISIONS
APPROVED
CHECKED
DRAWN E. STRAITON 7-28-61
DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

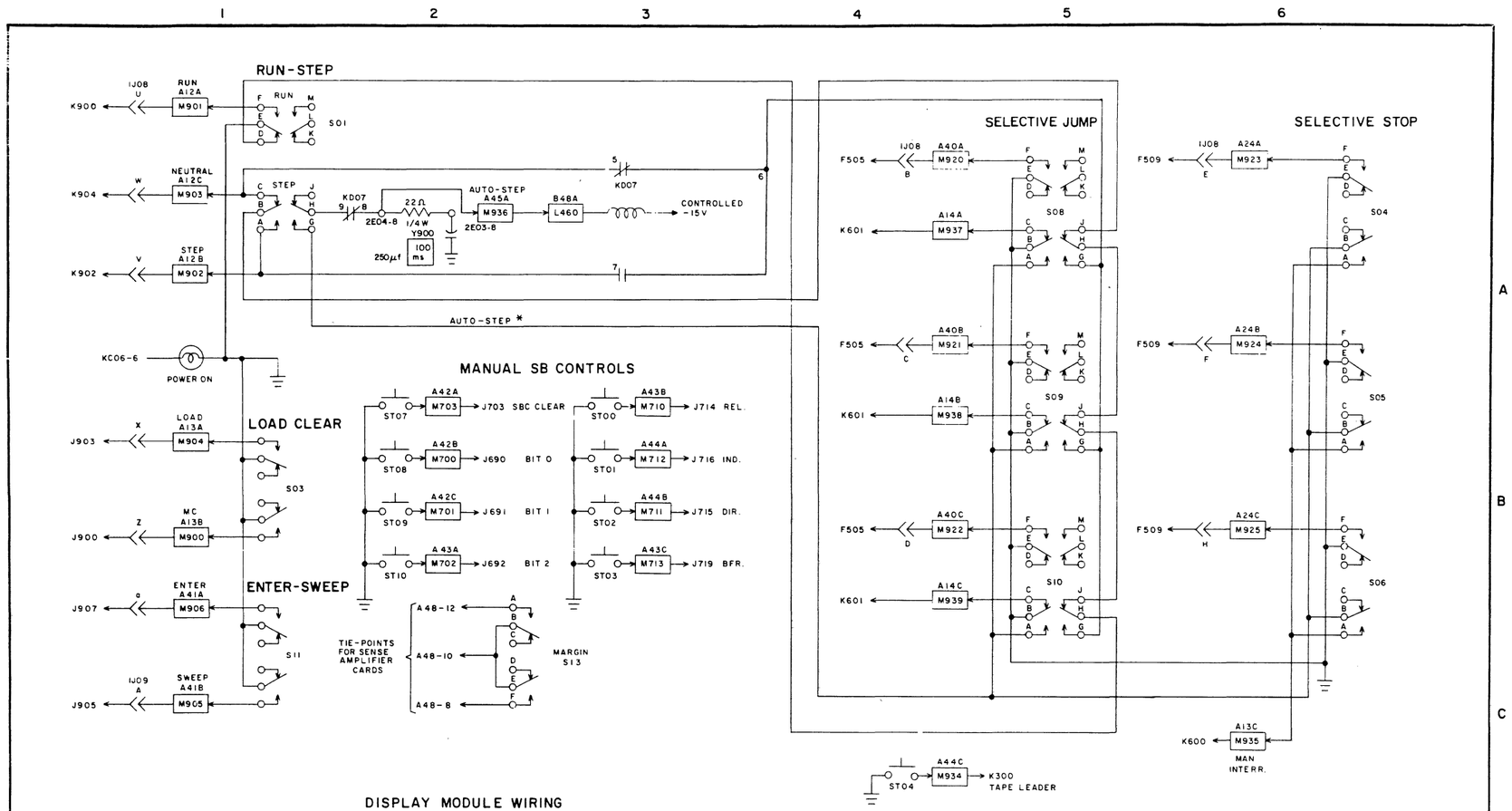
CONTROL DATA CORPORATION

PROJECT OR PRODUCT: 160-A

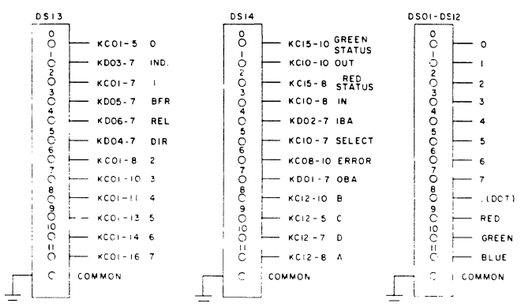
TITLE: BUFFER REGISTERS

DRAWING NUMBER: 20302100 C

PAGE 21



DISPLAY MODULE WIRING



DISPLAY UNIT	(9) RED	(10) GREEN	(11) BLUE
DS01		S02-G	KC16-7
DS02	KC04-16		DS01-11
DS03	DS02-9		KC16-10
DS04		S02-M	DS03-11
DS05	KC13-7	S07-G	
DS06	DS05-9	DS07-10	
DS07	KC13-10	KC17-7	
DS08	DS07-9	S07-M	
DS09	KC14-7	S12-G	
DS10	DS09-9		
DS11	KC14-10		
DS12	DS11-9	S12-M	

* NOTE
FOR AUTO-STEP OPERATION PLACE RUN-STEP SWITCH IN STEP AND DEPRESS ANY SELECTIVE JUMP SWITCH CARDS SHOWN ON THIS DIAGRAM ARE LOCATED ON CARD RACK (CHASSIS 10200)

REVISIONS | REV | AUTH | DATE | DES | CHK | APPROVED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED:) TOLERANCE VALUE SIZE
RESISTORS
CAPACITORS

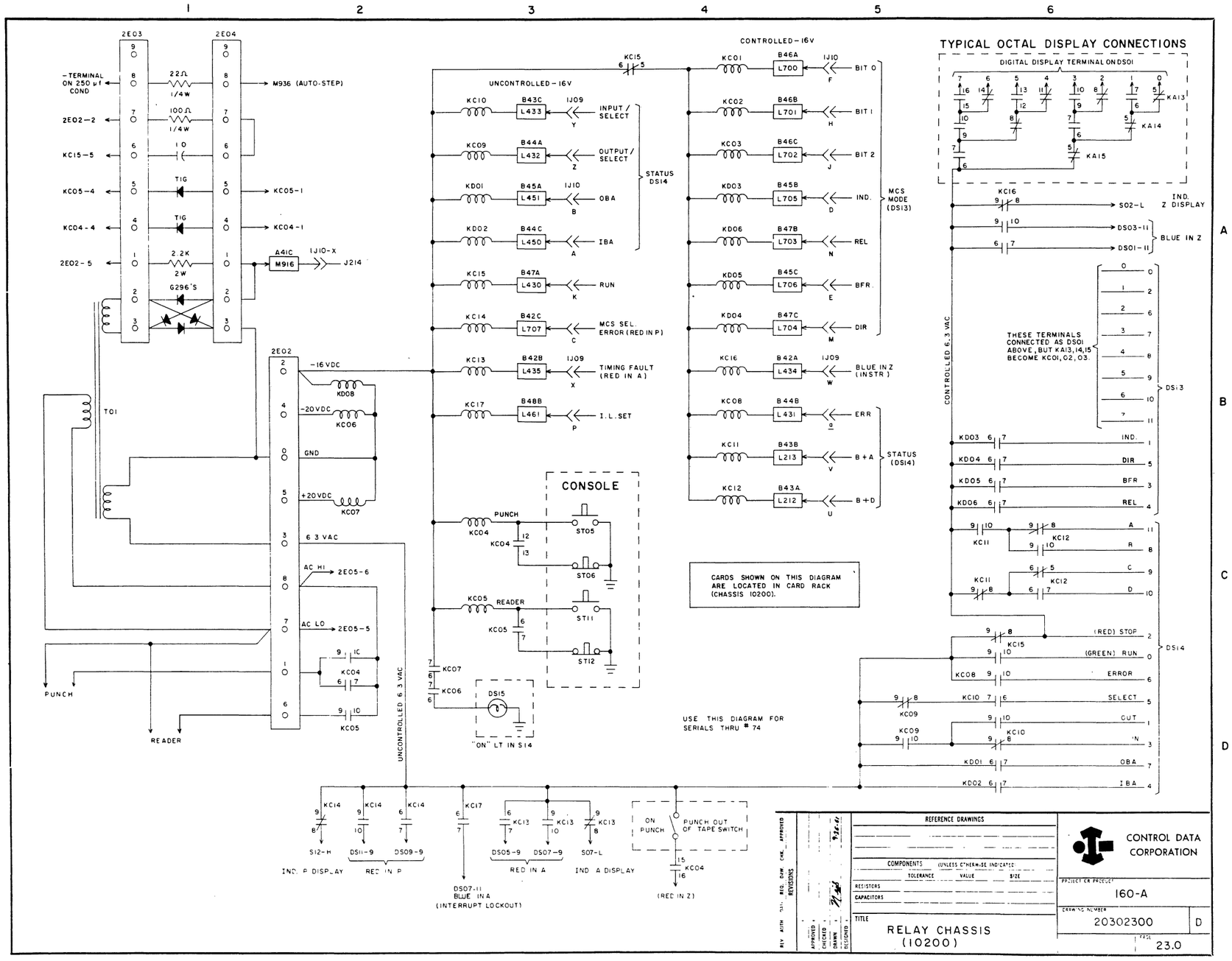
TITLE
CONSOLE (10200)

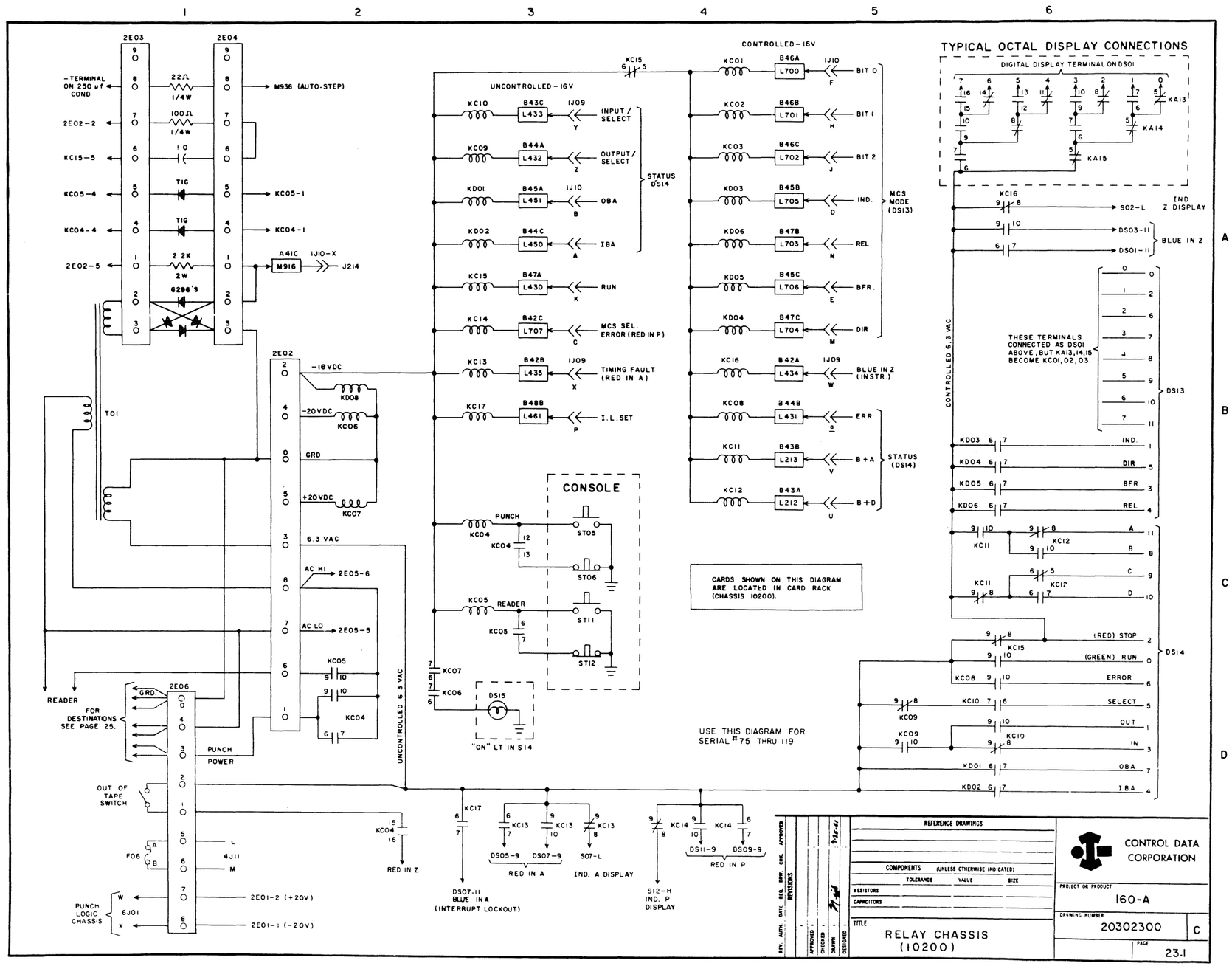
DESIGNED 2-28-64
DRAWN
CHECKED
APPROVED

CONTROL DATA CORPORATION

PROJECT OR PRODUCT
160-A

DRAWING NUMBER
20302200 A


1
2
3
4
5
6
2E03
2E04
-TERMINAL ON 250 µf COND
2E02-2
KC15-5
KC05-4
KC04-4
2E02-5
22Ω 1/4W
100Ω 1/4W
1.0
TIG
TIG
2.2K 2W
G296'S
M936 (AUTO-STEP)
KC05-1
KC04-1
A41C M916
1J10-X
J214
T01
2E02
-16VDC
KD08
-20VDC
KC06
GND
+20VDC
KC07
6.3 VAC
AC HI → 2E05-6
AC LO → 2E05-5
PUNCH
READER
UNCONTROLLED 6.3 VAC
UNCONTROLLED -16V
KC15
KC10 B43C L433 1J09 INPUT / SELECT Y
KC09 B44A L432 OUTPUT / SELECT Z
KD01 B45A L451 1J10 OBA B
KD02 B44C L450 IBA A
STATUS DS14
KC15 B47A L430 RUN K
KC14 B42C L707 MCS SEL ERROR (RED IN P) C
KC13 B42B L435 1J09 TIMING FAULT (RED IN A) X
KC17 B48B L461 I.L.SET P
CONSOLE
PUNCH KC04
KC04 12 13
ST05
ST06
KC05 READER
KC05 6 7
ST11
ST12
KC07
KC06
DS15
"ON" LT IN S14
CONTROLLED -16V
KC01 B46A L700 1J10 BIT 0 F
KC02 B46B L701 BIT 1 H
KC03 B46C L702 BIT 2 J
KD03 B45B L705 IND. D
KD06 B47B L703 REL N
KD05 B45C L706 BFR. E
KD04 B47C L704 DIR M
MCS MODE (DS13)
KC16 B42A L434 1J09 BLUE IN Z (INSTR.) W
KC08 B44B L431 ERR a
KC11 B43B L213 B+A V
KC12 B43A L212 B+D U
STATUS (DS14)
CARDS SHOWN ON THIS DIAGRAM ARE LOCATED IN CARD RACK (CHASSIS 10200).
USE THIS DIAGRAM FOR SERIALS THRU # 74
TYPICAL OCTAL DISPLAY CONNECTIONS
DIGITAL DISPLAY TERMINAL ON DS01
KA13
KA14
KA15
KC16
S02-L
IND. Z DISPLAY
DS03-11
DS01-11
BLUE IN Z
CONTROLLED 6.3 VAC
THESE TERMINALS CONNECTED AS DS01 ABOVE, BUT KA13,14,15 BECOME KC01,02,03.
DS13
KD03 6 7 IND. 1
KD04 6 7 DIR 5
KD05 6 7 BFR 3
KD06 6 7 REL 4
KC11 A 11
KC12 B 8
KC11 C 9
KC12 D 10
(RED) STOP 2
(GREEN) RUN 0
KC08 ERROR 6
KC10 7 6 SELECT 5
KC09 OUT 1
KC10 IN 3
KD01 6 7 OBA 7
KD02 6 7 IBA 4
DS14
S12-H
DS11-9
DS09-9
IND. P DISPLAY
RED IN P
DS07-11 BLUE IN A (INTERRUPT LOCKOUT)
DS05-9
DS07-9
RED IN A
S07-L
IND. A DISPLAY
ON PUNCH
PUNCH OUT OF TAPE SWITCH
KC04 15 16
(RED IN Z)
REFERENCE DRAWINGS
COMPONENTS (UNLESS OTHERWISE INDICATED)
TOLERANCE
VALUE
SIZE
RESISTORS
CAPACITORS
TITLE
RELAY CHASSIS (10200)
CONTROL DATA CORPORATION
PROJECT OR PRODUCT
160-A
DRAWING NUMBER
20302300
D
FSCM
23.0
REV
WITH
REQ. DWR
CHG. APPROVED
REVISIONS
APPROVED
CHECKED
DRAWN
DESIGNED
A
B
C
D



REV.	AUTH.	DATE	REQ. DRW. CHG. APPROVED
			REVISIONS
			APPROVED -
			CHECKED -
			DRAWN -
			DESIGNED -

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

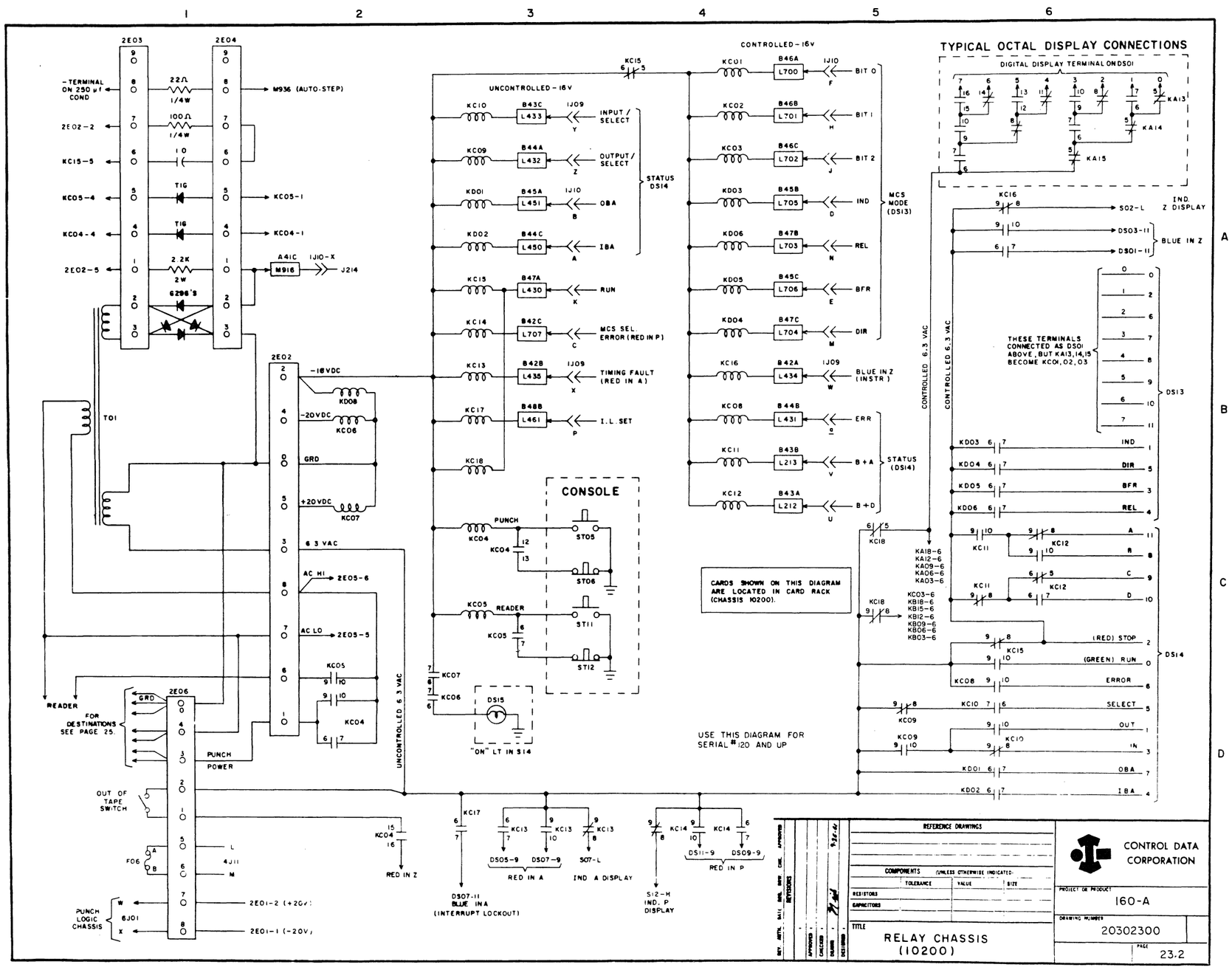
TITLE
RELAY CHASSIS (10200)

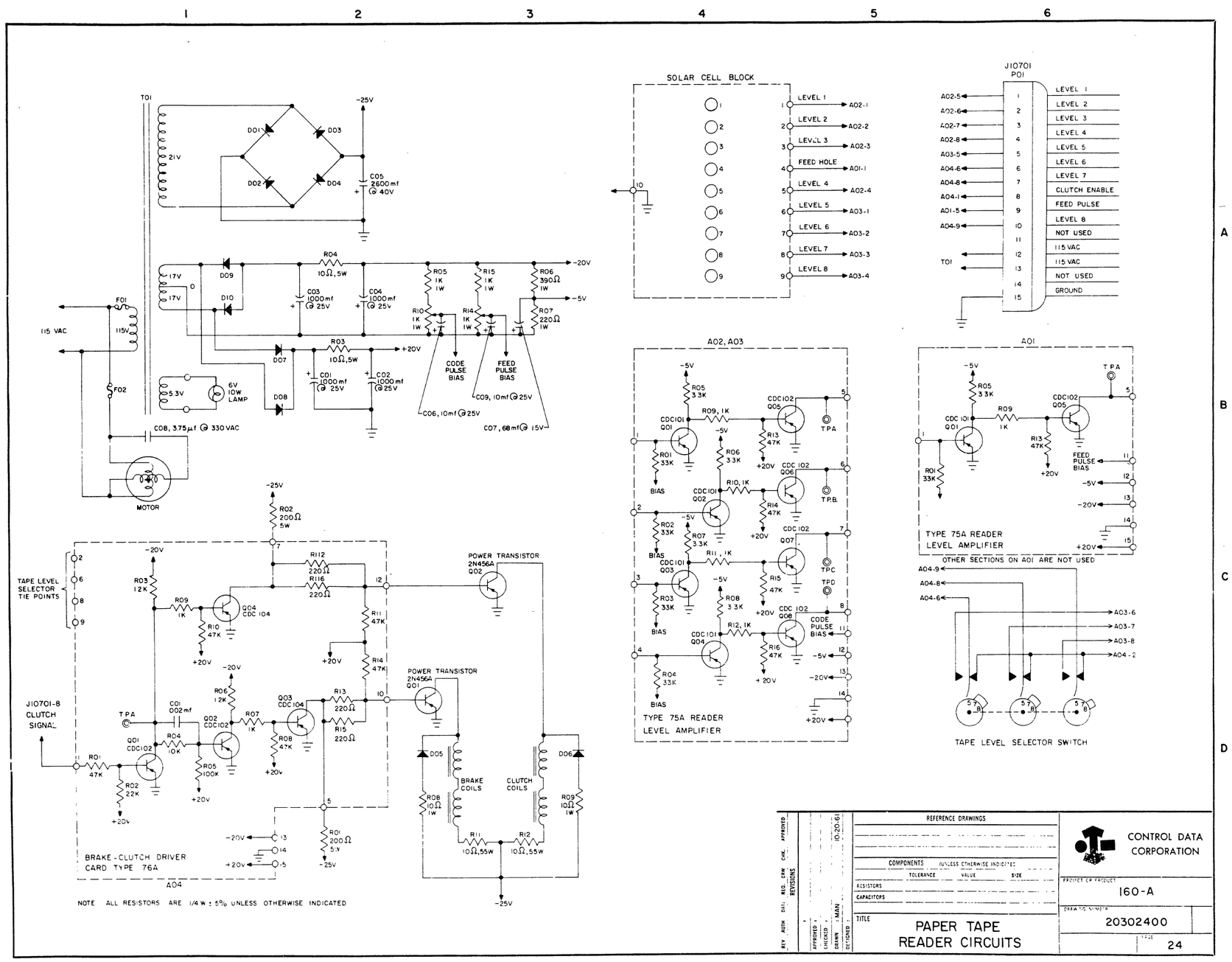
CONTROL DATA CORPORATION

PROJECT OR PRODUCT
160-A

DRAWING NUMBER
20302300 C

PAGE
23.1


1
2
3
4
5
6
A
B
C
D
2E03
2E04
-TERMINAL ON 250 µf COND
2E02-2
KC15-5
KC05-4
KC04-4
2E02-5
22Ω 1/4W
100Ω 1/4W
1.0
TIG
TIG
2.2K 2W
6296'S
M936 (AUTO-STEP)
KC05-1
KC04-1
A41C
M916
IJ10-X
J214
2E02
-18VDC
KD08
-20VDC
KC06
GRD
+20VDC
KC07
6.3 VAC
AC HI
2E05-6
AC LO
2E05-5
KC05
KC04
T01
READER
2E06
GRD
FOR DESTINATIONS SEE PAGE 25.
PUNCH POWER
OUT OF TAPE SWITCH
F06
4J11
L
M
PUNCH LOGIC CHASSIS
6J01
W
X
2E01-2 (+20V)
2E01-1 (-20V)
UNCONTROLLED 6.3 VAC
UNCONTROLLED -16V
KC10 B43C L433 IJ09 INPUT / SELECT Y
KC09 B44A L432 OUTPUT / SELECT Z
KD01 B45A L451 IJ10 OBA B
KD02 B44C L450 IBA A
STATUS DSI4
KC15 B47A L430 RUN K
KC14 B42C L707 MCS SEL ERROR (RED IN P) C
KC13 B42B L435 IJ09 TIMING FAULT (RED IN A) X
KC17 B48B L461 I.L. SET P
KC18
PUNCH KC04
KC04 12 13
KC05 READER
KC05 6 7
KC07
KC06
DS15
"ON" LT IN S14
CONSOLE
ST05
ST06
ST11
ST12
CONTROLLED -16V
KC15 6 5
KC01 B46A L700 IJ10 F BIT 0
KC02 B46B L701 H BIT 1
KC03 B46C L702 J BIT 2
KD03 B45B L705 D IND
KD06 B47B L703 N REL
KD05 B45C L706 E BFR
KD04 B47C L704 M DIR
MCS MODE (DSI3)
KC16 B42A L434 IJ09 W BLUE IN Z (INSTR)
KC08 B44B L431 a ERR
KC11 B43B L213 V B+A
KC12 B43A L212 U B+D
STATUS (DSI4)
CONTROLLED 6.3 VAC
CONTROLLED 6.3 VAC
KC18 6 5
KA18-6
KA12-6
KA09-6
KA06-6
KA03-6
KC03-6
KB18-6
KB15-6
KB12-6
KB09-6
KB06-6
KB03-6
KC18 9 8
CARDS SHOWN ON THIS DIAGRAM ARE LOCATED IN CARD RACK (CHASSIS 10200).
USE THIS DIAGRAM FOR SERIAL # 120 AND UP
TYPICAL OCTAL DISPLAY CONNECTIONS
DIGITAL DISPLAY TERMINAL ON DS01
KA13
KA14
KA15
KC16
S02-L
IND. Z DISPLAY
DS03-11
DS01-11
BLUE IN Z
THESE TERMINALS CONNECTED AS DS01 ABOVE, BUT KA13,14,15 BECOME KC01, 02, 03
DS13
KD03 6 7 IND 1
KD04 6 7 DIR 5
KD05 6 7 BFR 3
KD06 6 7 REL 4
KC11 KC12 A 11
KC11 KC12 B 8
C 9
D 10
KC15
(RED) STOP 2
(GREEN) RUN 0
KC08 ERROR 6
KC10 SELECT 5
KC10 OUT 1
KC10 IN 3
KD01 OBA 7
KD02 IBA 4
DS14
15 KC04 16
RED IN Z
KC17 6 7
DS07-11 BLUE IN A (INTERRUPT LOCKOUT)
KC13 6 7
KC13 9 10
KC13 9 8
DS05-9
DS07-9
S07-L
RED IN A
IND A DISPLAY
KC14 9 8
KC14 9 10
KC14 6 7
DS11-9
DS09-9
S12-H IND. P DISPLAY
RED IN P
REFERENCE DRAWINGS
COMPONENTS (UNLESS OTHERWISE INDICATED:
TOLERANCE
VALUE
SIZE
RESISTORS
CAPACITORS
TITLE
RELAY CHASSIS (10200)
CONTROL DATA CORPORATION
PROJECT OR PRODUCT
160-A
DRAWING NUMBER
20302300
PAGE
23.2



REV	AUTH	DATE	REVISIONS	ENG	CHK	APPROVED
						10-20-61

APPROVED –
CHECKED –
DRAWN J. MAN
DETAILED –

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE

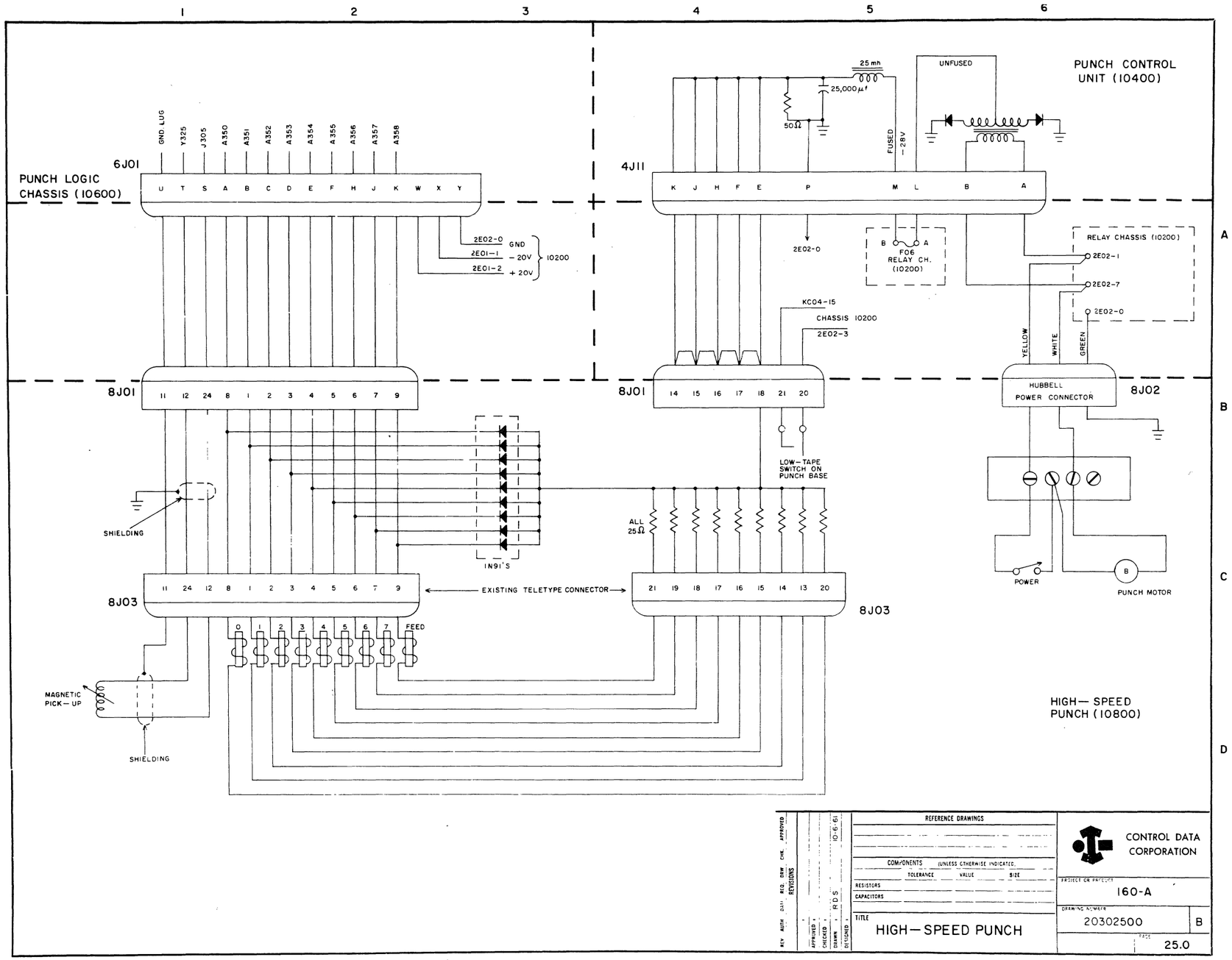
PAPER TAPE READER CIRCUITS

CONTROL DATA CORPORATION

PROJECT OR PRODUCT
160-A

DRAWING NUMBER
20302400

PAGE
24



REV	AUTH	DATE	REQ. DRW. CHK. APPROVED REVISIONS			
			APPROVED			
			CHECKED			
			DRAWN	10-6-61	R D S	
			DESIGNED			

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE

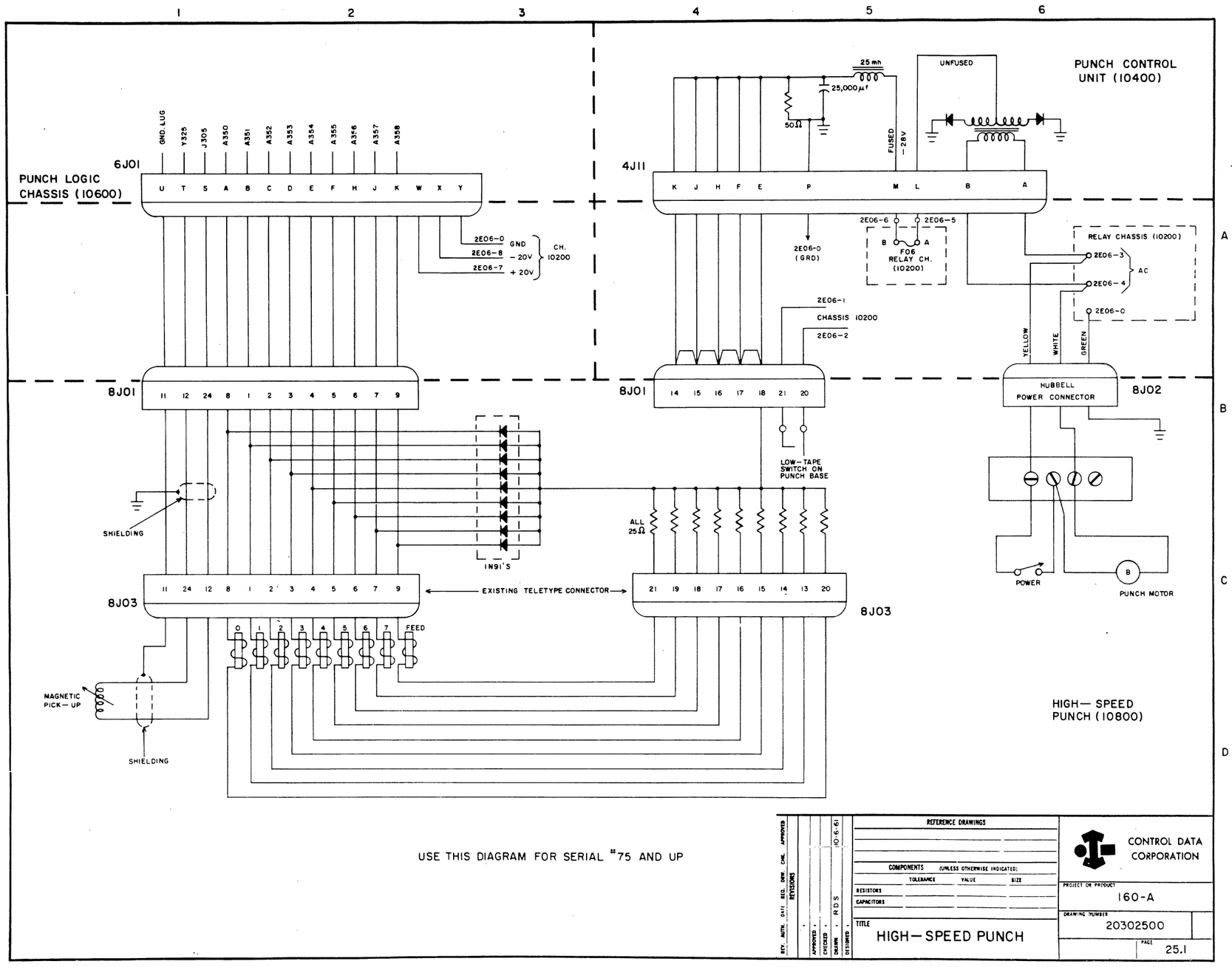
HIGH-SPEED PUNCH

CONTROL DATA CORPORATION

PROJECT OR PAYCODE: 160-A

DRAWING NUMBER: 20302500 B

PAGE: 25.0



USE THIS DIAGRAM FOR SERIAL #75 AND UP

REV.	AUTH.	DATE	REQ.	DRW.	CHK.	APPROVED
REVISIONS						

APPROVED ,
CHECKED ,
DRAWN , R D S 10-6-61
DESIGNED ,

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

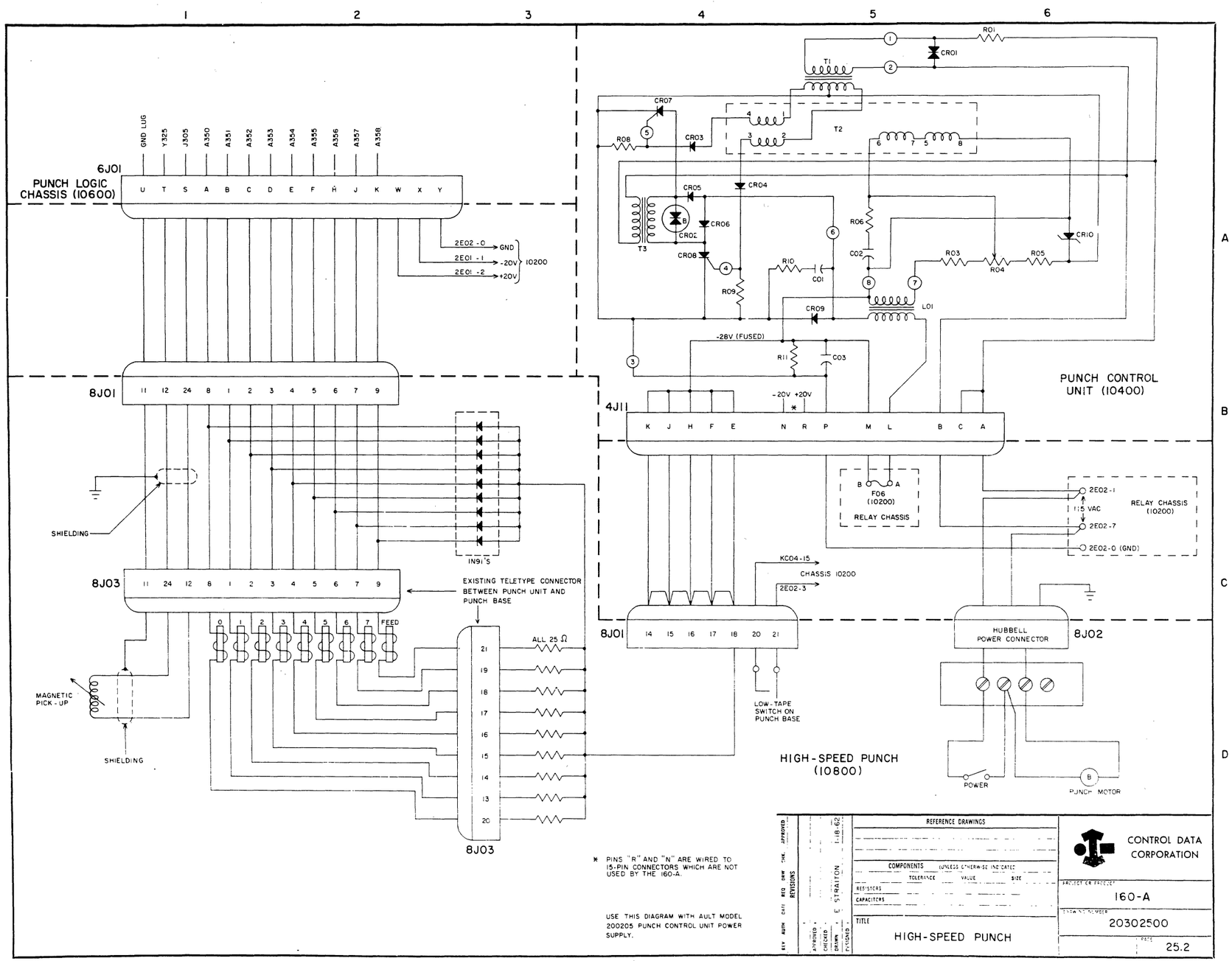
TITLE
HIGH-SPEED PUNCH

CONTROL DATA CORPORATION

PROJECT OR PRODUCT
160-A

DRAWING NUMBER
20302500

PAGE
25.1



* PINS "R" AND "N" ARE WIRED TO 15-PIN CONNECTORS WHICH ARE NOT USED BY THE 160-A.

USE THIS DIAGRAM WITH AULT MODEL 200205 PUNCH CONTROL UNIT POWER SUPPLY.

REV	AUTH	DATE	REVISIONS	REQ	DRW	CHK	APPROVED

APPROVED
CHECKED
DRAWN E. STRAITON 1-18-62
DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

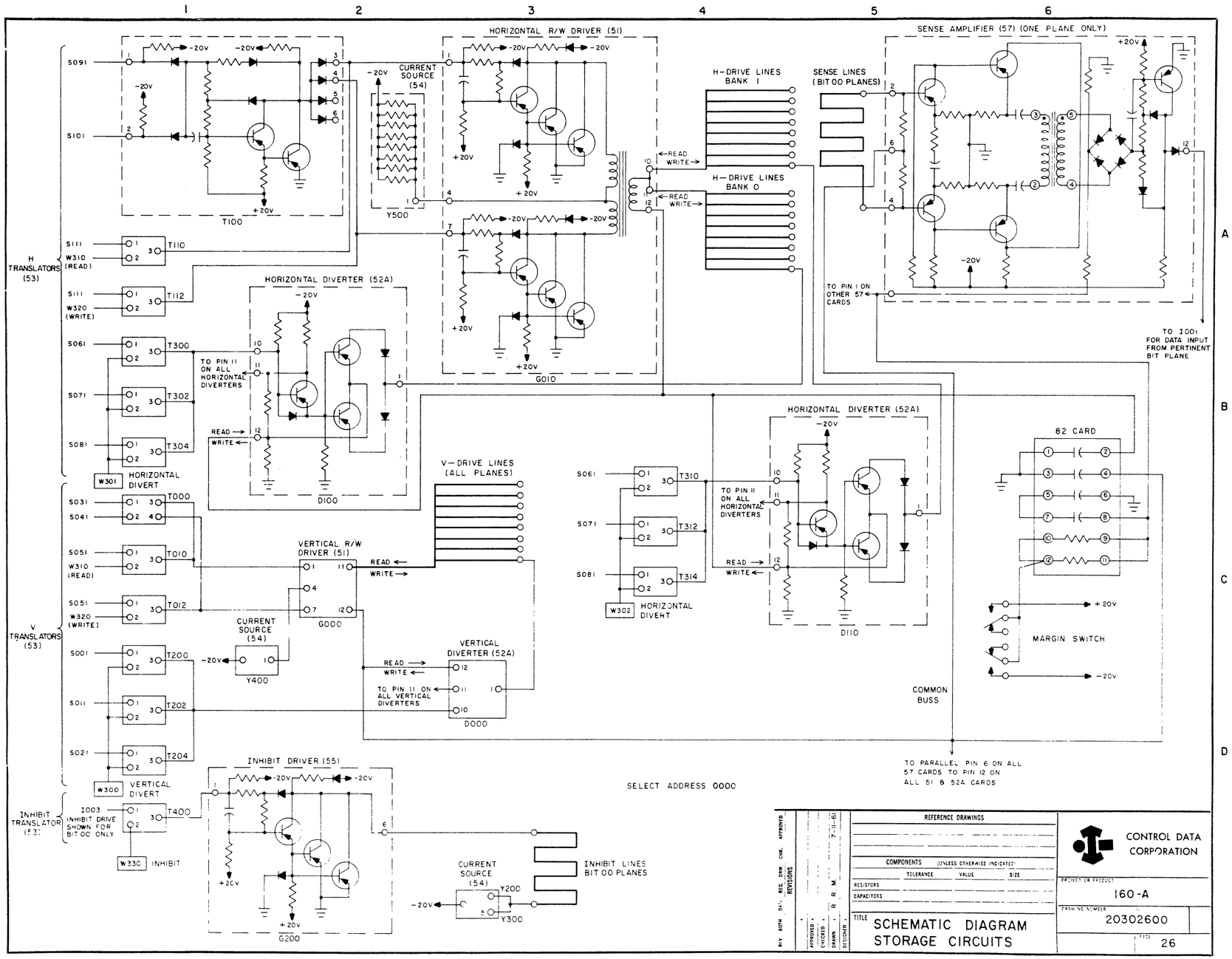
TITLE
HIGH-SPEED PUNCH

CONTROL DATA CORPORATION

PROJECT OR PROD. NO.
160-A

DRAWING NUMBER
20302500

PAGE
25.2



REVISIONS	BY	AUTH	DATE	APPROVED
				CHKD.
				DRW.
				REQ.
				ENGR.

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

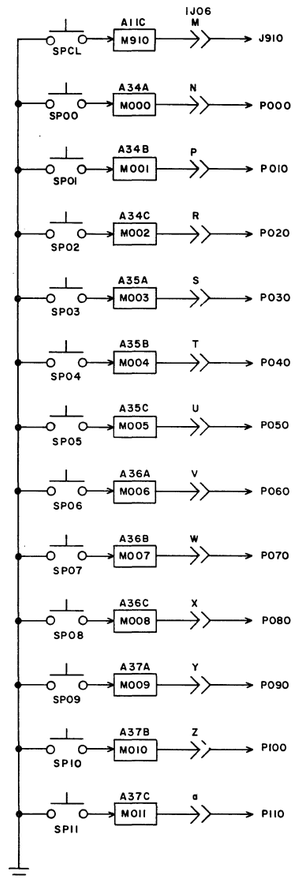
TITLE: SCHEMATIC DIAGRAM STORAGE CIRCUITS

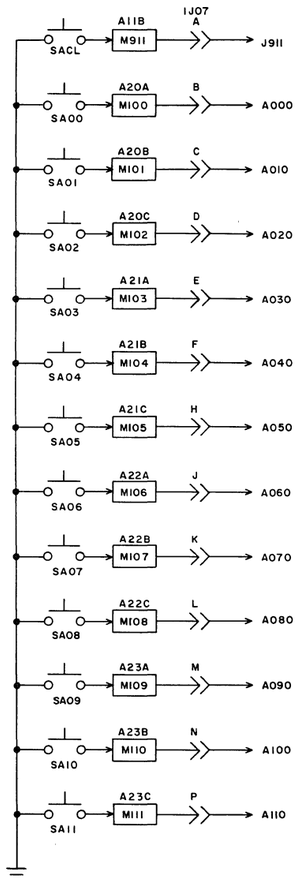
CONTROL DATA CORPORATION

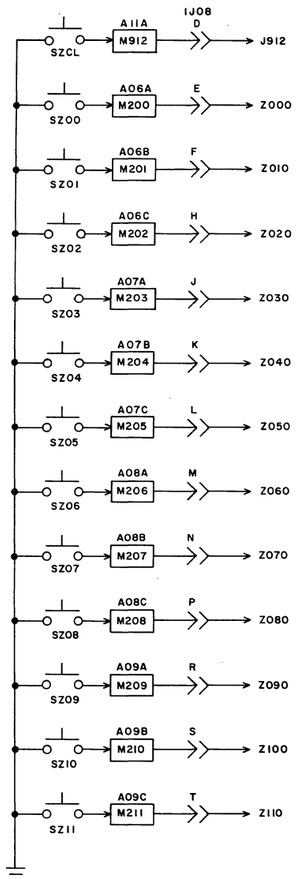
PROJECT OR PRODUCT: 160-A

DRW. NO. NUMBER: 20302600

PAGE 26







NOTE:
THESE CARDS ARE LOCATED ON CARD RACK (CHASSIS 10200).

REV.	AUTH.	DATE	REQ.	DRW.	CHK.	APPROVED
REVISIONS						

APPROVED
CHECKED
DRAWN — 12-64
DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

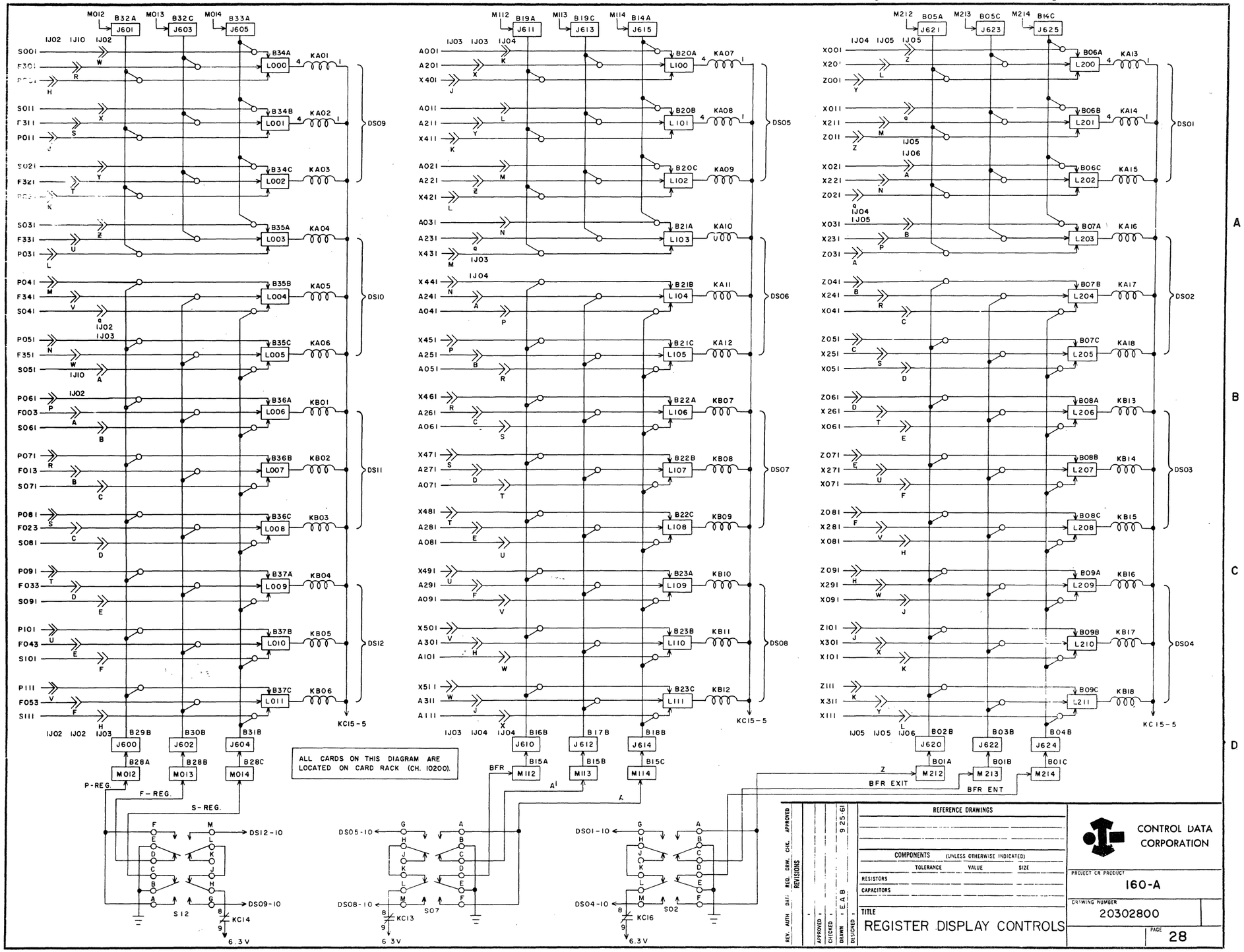
TITLE
REGISTER SET (M) CARDS

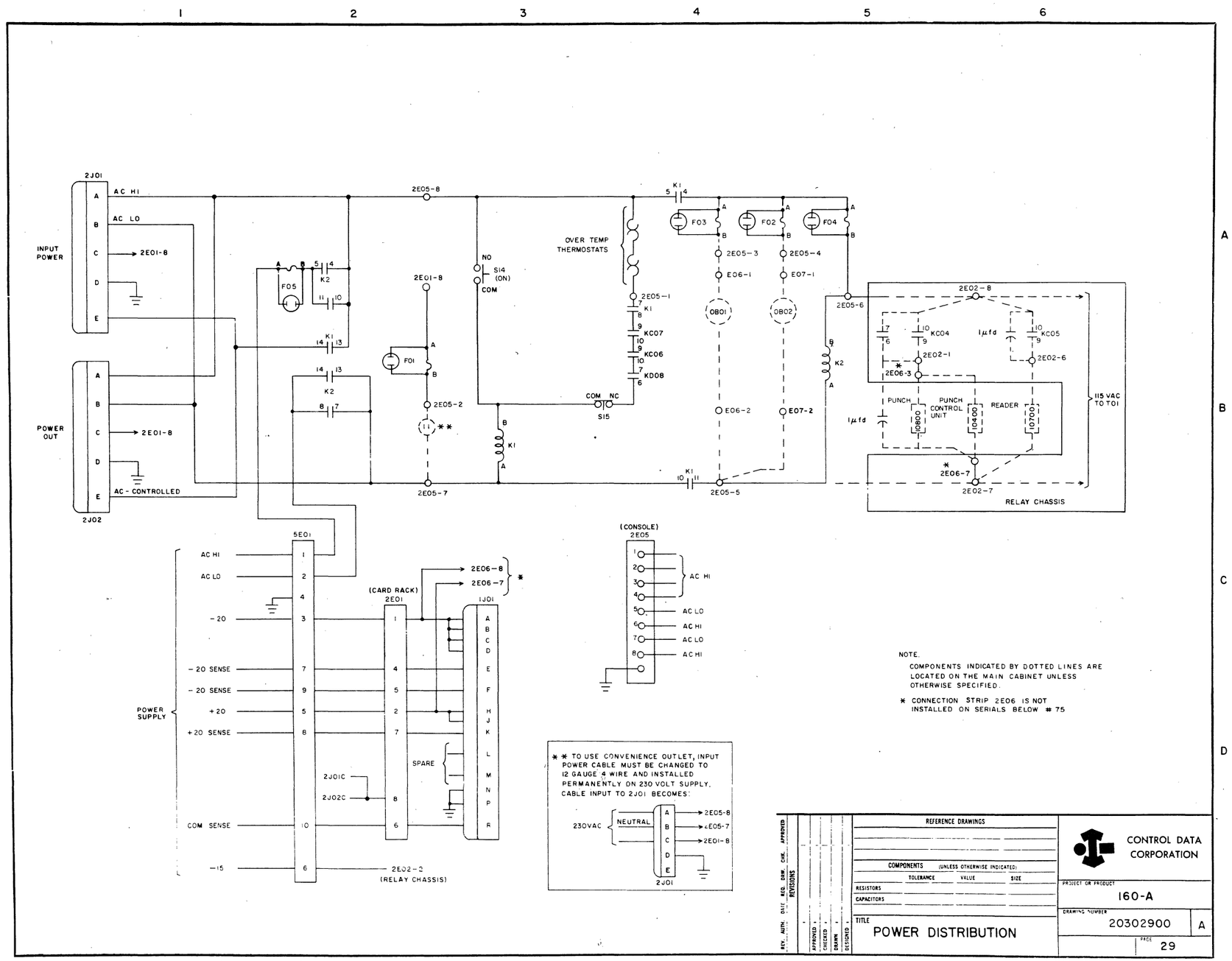
CONTROL DATA CORPORATION

PROJECT OR PRODUCT
160-A

DRAWING NUMBER
20302700

PAGE
27


1
2
3
4
5
6
A
B
C
D
M012 B32A J601
M013 B32C J603
M014 B33A J605
M112 B19A J611
M113 B19C J613
M114 B14A J615
M212 B05A J621
M213 B05C J623
M214 B14C J625
IJ02 IJ10 IJ02
IJ03 IJ03 IJ04
IJ04 IJ05 IJ05
S001 F301 P001
S011 F311 P011
S021 F321 P021
S031 F331 P031
S041 F341 P041
S051 F351 P051
S061 F003 P061
S071 F013 P071
S081 F023 P081
S091 F033 P091
S101 F043 P101
S111 F053 P111
A001 A201 X401
A011 A211 X411
A021 A221 X421
A031 A231 X431
A041 A241 X441
A051 A251 X451
A061 A261 X461
A071 A271 X471
A081 A281 X481
A091 A291 X491
A101 A301 X501
A111 A311 X511
X001 X201 Z001
X011 X211 Z011
X021 X221 Z021
X031 X231 Z031
X041 X241 Z041
X051 X251 Z051
X061 X261 Z061
X071 X271 Z071
X081 X281 Z081
X091 X291 Z091
X101 X301 Z101
X111 X311 Z111
B34A L000 KA01
B34B L001 KA02
B34C L002 KA03
B35A L003 KA04
B35B L004 KA05
B35C L005 KA06
B36A L006 KB01
B36B L007 KB02
B36C L008 KB03
B37A L009 KB04
B37B L010 KB05
B37C L011 KB06
B20A L100 KA07
B20B L101 KA08
B20C L102 KA09
B21A L103 KA10
B21B L104 KA11
B21C L105 KA12
B22A L106 KB07
B22B L107 KB08
B22C L108 KB09
B23A L109 KB10
B23B L110 KB11
B23C L111 KB12
B06A L200 KA13
B06B L201 KA14
B06C L202 KA15
B07A L203 KA16
B07B L204 KA17
B07C L205 KA18
B08A L206 KB13
B08B L207 KB14
B08C L208 KB15
B09A L209 KB16
B09B L210 KB17
B09C L211 KB18
DS09
DS10
DS11
DS12
DS05
DS06
DS07
DS08
DS01
DS02
DS03
DS04
KC15-5
IJ02 IJ02 IJ03 B29B J600
B30B J602
B31B J604
IJ03 IJ04 IJ04 B16B J610
B17B J612
B18B J614
IJ05 IJ05 IJ06 B02B J620
B03B J622
B04B J624
B28A M012
B28B M013
B28C M014
B15A M112
B15B M113
B15C M114
B01A M212
B01B M213
B01C M214
P-REG.
F-REG.
S-REG.
BFR
BFR EXIT
BFR ENT
DS12-10
DS09-10
S12
KC14
6.3V
DS05-10
DS08-10
S07
KC13
DS01-10
DS04-10
S02
KC16
ALL CARDS ON THIS DIAGRAM ARE LOCATED ON CARD RACK (CH. 10200).
REV. AUTH DAT: REQ. DRW. CHK. APPROVED
REVISIONS
APPROVED
CHECKED
DRAWN T.E.A.B 9-25-61
DESIGNED
REFERENCE DRAWINGS
COMPONENTS (UNLESS OTHERWISE INDICATED)
TOLERANCE VALUE SIZE
RESISTORS
CAPACITORS
TITLE
REGISTER DISPLAY CONTROLS
CONTROL DATA CORPORATION
PROJECT OR PRODUCT
160-A
DRAWING NUMBER
20302800
PAGE
28



NOTE.

COMPONENTS INDICATED BY DOTTED LINES ARE LOCATED ON THE MAIN CABINET UNLESS OTHERWISE SPECIFIED.

* CONNECTION STRIP 2E06 IS NOT INSTALLED ON SERIALS BELOW # 75

REV.	AUTH.	DATE	REVISIONS	REQ.	DRW.	CHK.	APPROVED

APPROVED
CHECKED
DRAWN
DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

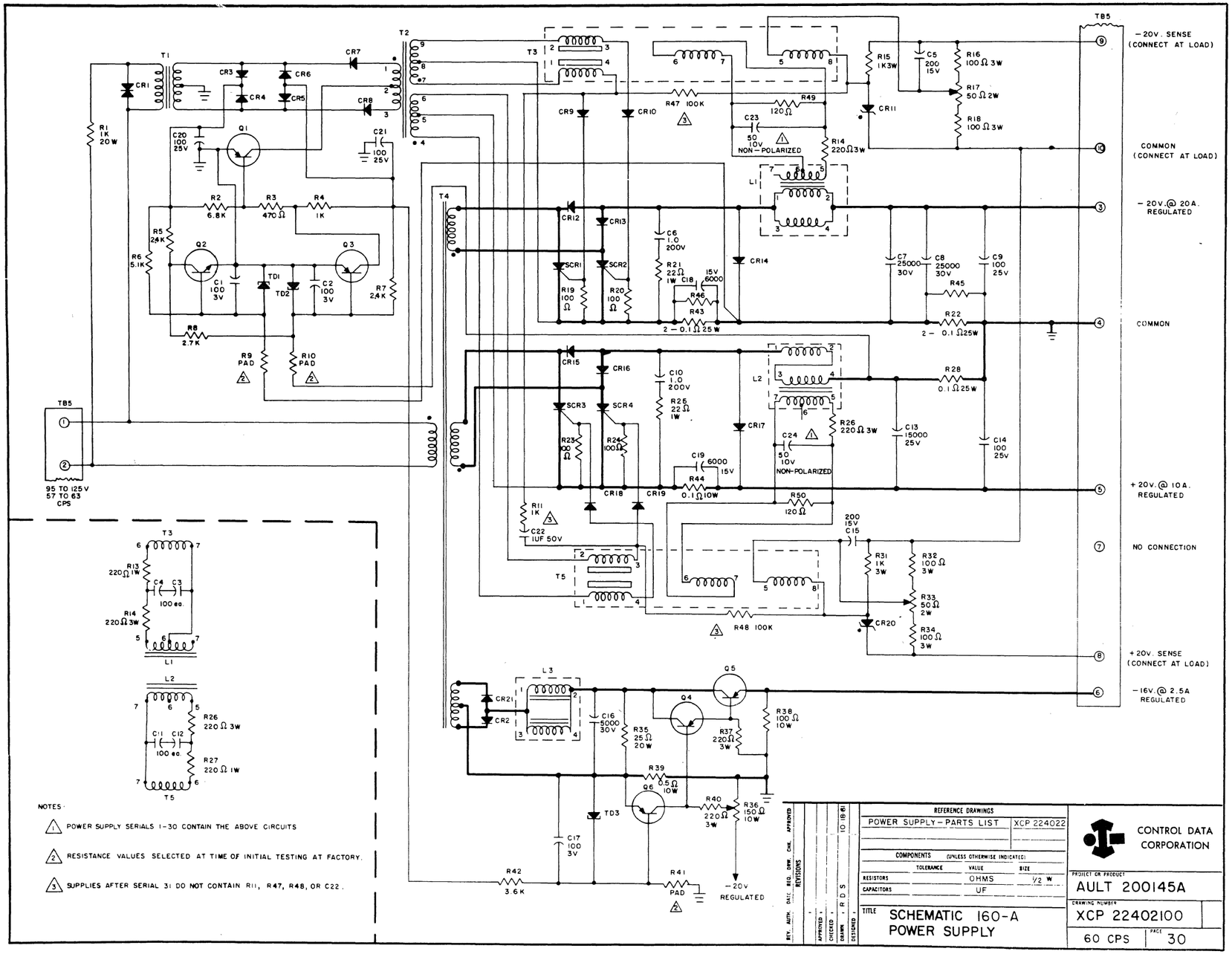
TITLE
POWER DISTRIBUTION

CONTROL DATA CORPORATION

PROJECT OR PRODUCT
160-A

DRAWING NUMBER
20302900 A

PAGE
29



NOTES:

1. POWER SUPPLY SERIALS 1-30 CONTAIN THE ABOVE CIRCUITS
2. RESISTANCE VALUES SELECTED AT TIME OF INITIAL TESTING AT FACTORY.
3. SUPPLIES AFTER SERIAL 31 DO NOT CONTAIN R11, R47, R48, OR C22.

REV.	AUTH.	DATE	REVISIONS	APPROVED	CHECKED	DRAWN	DESIGNED
	-			-	-	R D S	10-18-61

REFERENCE DRAWINGS

POWER SUPPLY - PARTS LIST	XCP 224022

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS		OHMS	1/2 W
CAPACITORS		UF	

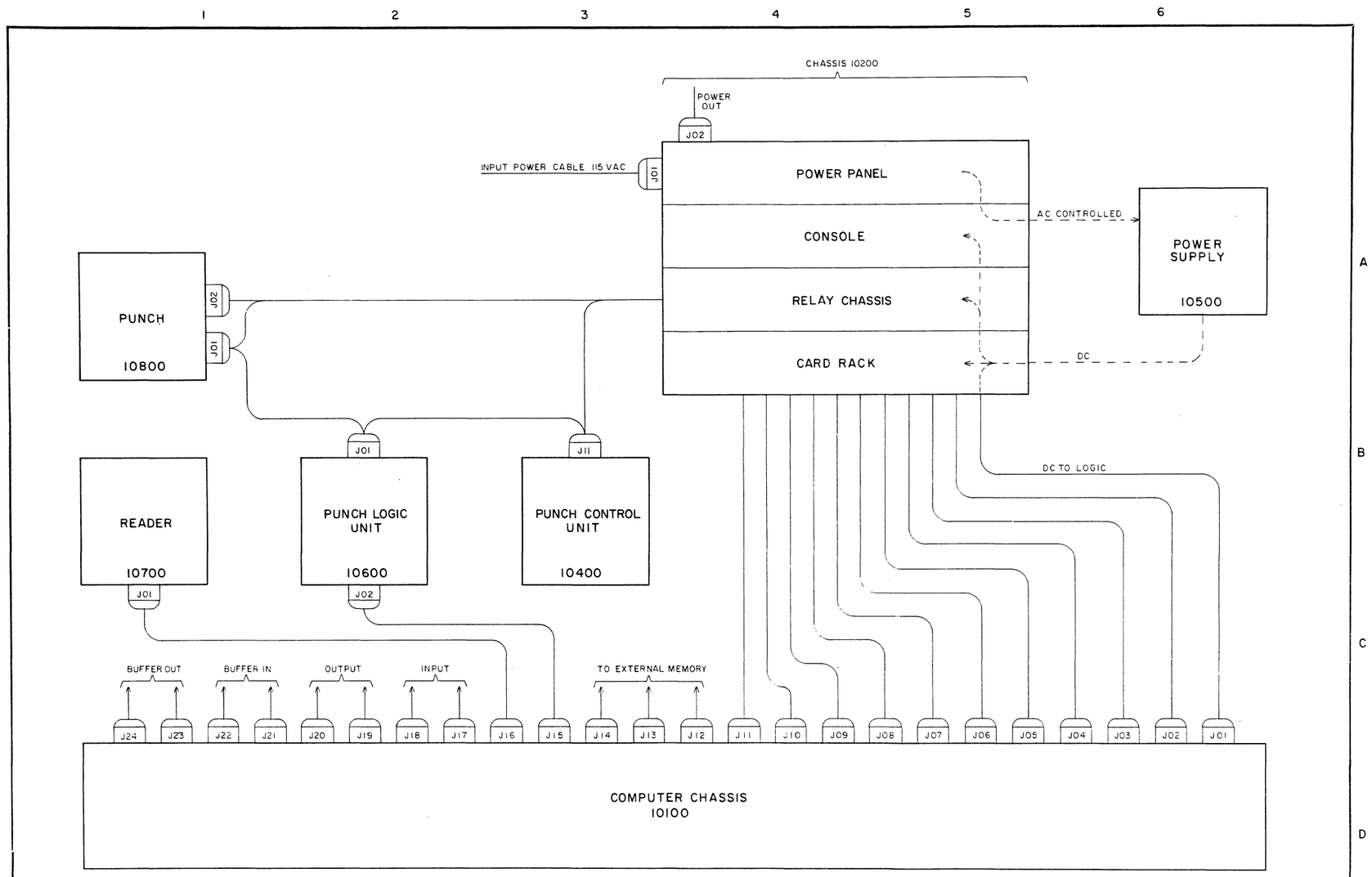
TITLE: SCHEMATIC 160-A POWER SUPPLY

CONTROL DATA CORPORATION

PROJECT OR PRODUCT: AULT 200145A

DRAWING NUMBER: XCP 22402100

60 CPS | PAGE 30



NOTE
DOTTED LINES INDICATE
PERMANENT WIRING

REV. AUTH | ECI | REQ. DRW. | FINAL | APPROVED
REVISIONS

APPROVED
CHECKED
DRAWN
DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

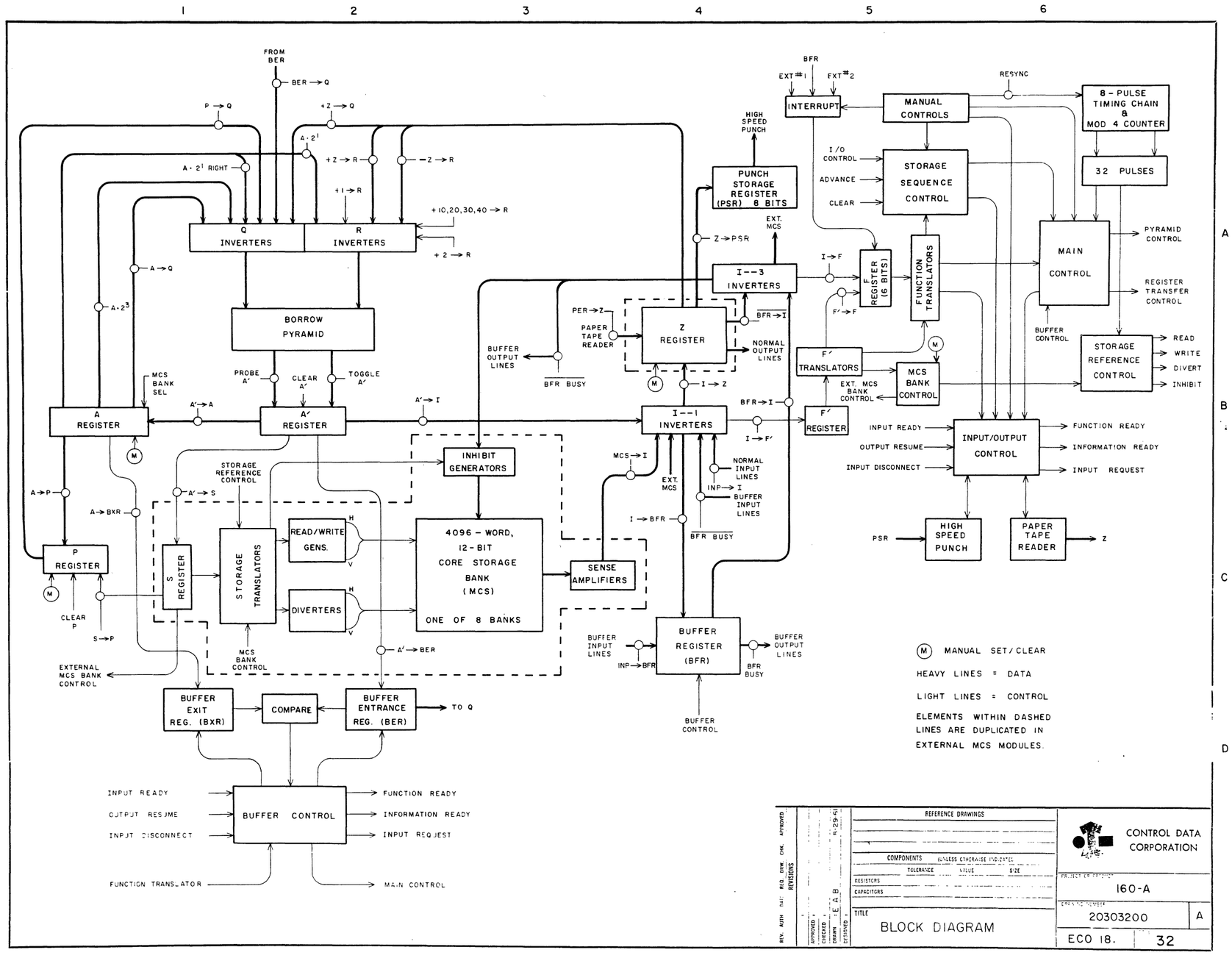
TITLE
CABLING DIAGRAM

CONTROL DATA CORPORATION

PROJECT OR PRODUCT
160-A

DRAWING NUMBER
2030100

31



REV.	AUTH	DATE	REQ.	CHK.	APPROVED
REVISIONS					

APPROVED
CHECKED
DRAWN E A B
DESIGNED

REFERENCE DRAWINGS

COMPONENTS (UNLESS OTHERWISE INDICATED)

	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			

TITLE

BLOCK DIAGRAM

CONTROL DATA CORPORATION

PROJECT OR PRODUCT

160-A

DRAWING NUMBER

20303200 | A

ECO 18. | 32

COMMENT SHEET

CONTROL DATA 160-A Computer
Customer Engineering Diagrams
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