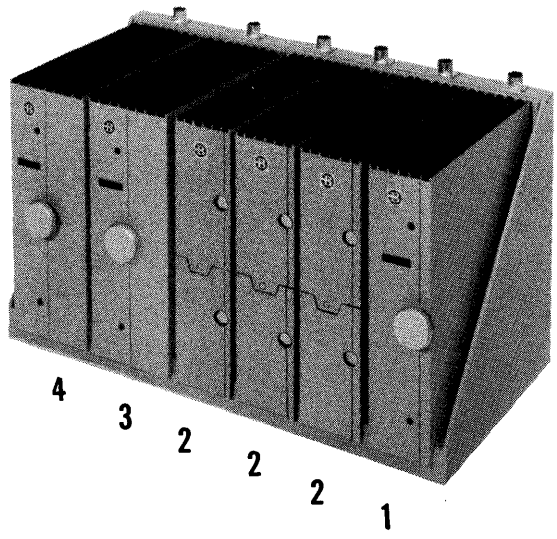
Burroughs

D84M MODULAR COMPUTER SYSTEM

TYPICAL D84M COMPUTER CONFIGURATION



1 POWER SUPPLY MODULE, SERIES D84/400
Uses discrete component solid-state circuits

2 MEMORY MODULE, SERIES D84/200
Uses monolithic integrated circuits, thin-film hybrid circuits, and/or discrete components to implement logic and drivers of DRO and NDRO memories

3 INPUT/OUTPUT MODULE, SERIES D84/500
Uses monolithic integrated circuits and discrete component solid-state circuits

4 CENTRAL DATA PROCESSOR MODULE, SERIES D84/100
Uses monolithic integrated circuits

EQUIPMENT DEFINITION

The D84M Modular Computer System is a general-purpose, solid-state, high-speed computing system that employs integrated circuits exclusively for logic implementation, resulting in a system capable of withstanding severe environmental extremes and which is compact, reliable, light weight and of low power consumption.

The D84M has been specifically designed for military field environments.

FEATURES

The D84M Modular Computer System features:

- Four basic types of functionally and physically independent modules (see figure)
- Multiplicity of possible system configurations through combining one or more of Input/Output and Memory modules.
- Flexible design that allows for system expansion and input/output flexibility without design changes
- Built-in logic and controls for interfacing with associated systems and peripheral equipment
- "Custom" input/output design features without the usually attendant high cost

APPLICATIONS

The D84M System's low power, rugged design, and built-in growth potential ideally suit it for military field applications, including centralized command and control functions, guidance and fire control, tactical control, real-time simulation, data reduction and analysis, message switching and digital communications, ground support checkout, navigation, and general-purpose data processing.

EQUIPMENT DESCRIPTION

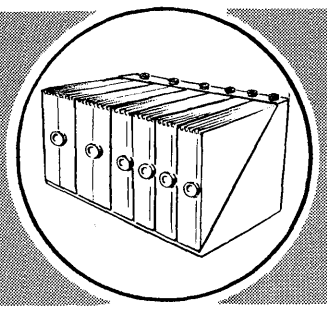
The D84 Modular Computing System comprises the following functional units, which can be combined into a multiplicity of computer system configurations:

	Series Reference No.
Central Data Processor Module	D84/100
Memory Module	D84/200
Power Supply Module	D84/400
Input/Output Module	D84/500
Peripheral Equipment	D84/600
Mounting Base Assemblies	D84/700
Control Panel Assemblies	D84/800

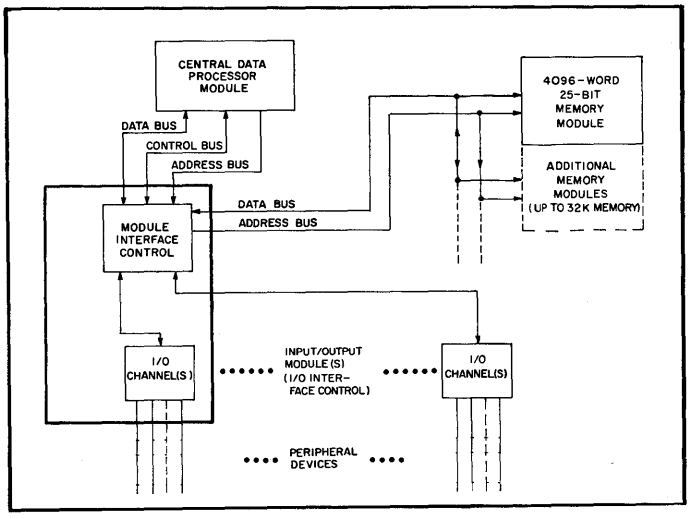
Each major series of modules is subdivided according to model (or design variation), with the last two numbers of the series reference bearing the specific module identification. A family of modules is thus available, from which the types of modules to be used can be selected according to system needs.

Input/Output Modules may be specially designed for specific needs. Since the D84M System is designed primarily for military applications, the I/O control concept permits the inclusion of special-purpose units. The D84/500 series of Input/Output Modules include several models implementing differing I/O interface control (channel) concepts.

A series of Data Sheets provides detailed information on specific models of the major series of modules and equipment of the D84M Modular Computer System. Identified by both Series and Model Numbers, these data sheets contain equipment descriptions, functional descriptions, block diagrams, and equipment characteristics.



FUNCTIONAL DESCRIPTION



Basic D84 Modular Computer System for Non-Concurrent Memory Access

A specific D84 computer system configuration may utilize one or more I/O and Memory Modules. The types of input/output modules used in a system depend on the specific system application. However, even though the I/O modules are specifically designed for the taks to be performed, the CDP interface with the I/O interface control module remains unchanged.

The basic I/O module includes the CDP-memory-I/O interface control, hereafter called the module interface control (MIC). This control group forms the connection between the I/O functions, the memory modules and the central data processor (CDP). Included in the MIC are the interrupt priority control, and the logic needed to resolve memory and CDP access conflicts.

Data transfers to and from peripheral devices are routed via independent I/O interface controls or channels. An I/O module accommodates the MIC, 1 unbuffered channel, and up to 2 buffered channels.

When access to a memory module by a buffered I/O channel is desired, the program supervises the data transfer by using the descriptor command. The descriptor assigns a memory module, or a block of locations within a module, to the I/O channel. The program may, however, interrupt the I/O memory interface to gain access to the memory for loading or unloading. It thus retains control over all memory modules.

Unbuffered channels are under direct program control, requiring an instruction per word transferred.

AVAILABLE SOFTWARE

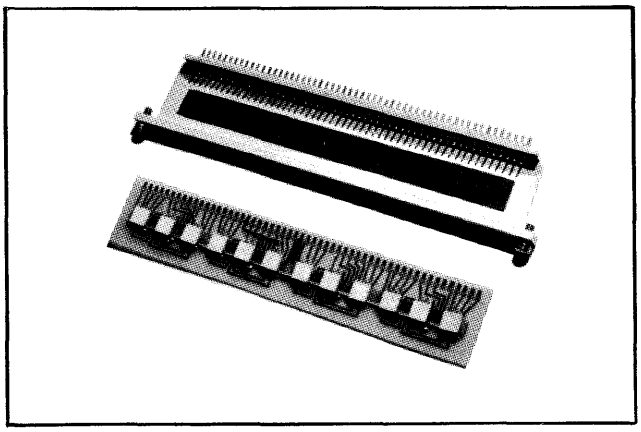
An Assembler Program written in FORTRAN IV language for use on the 7044 or 7094, and Mathematical Subroutines (trigonometric, exponential, double precision, floating point, etc.) are currently available and applicable to any D84 Computer System configuration. Simulator and Diagnostic Routines written for D84 Systems of specific configurations are also available, portions of which likewise apply to any D84 System configuration.

PACKAGING

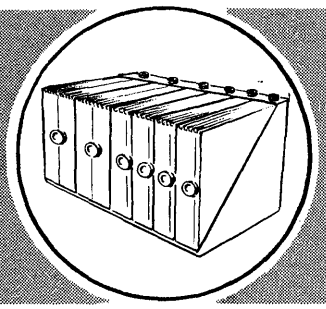
A typical D84 Modular Computer System consists of a CDP Module, an I/O module, a Power Supply Module, six Memory Modules, and a Mounting Base Assembly. The modules are separate, sealed packages that plug into the base assembly which contains interconnection wiring between modules. The entire unit is 16 inches deep and 18 inches high; width and weight vary according to module type.

All module housings are cast aluminum magnesium alloy. The base assembly uses a combination of extruded and wrought structural members. The modular concept, a split-casting "suitcase" technique, permits easy access to all internal electronics upon removal from the main frame. Each module has a manually operable rod assembly with a threaded stud on one end. The rod assembly extends through the module to engage the stud with the mounting base assembly. Each module has multi-pin male connector assemblies that plug into receptacles in the interconnecting wiring box of the mounting base assembly. Combination alignment and support pins on the base mounting assembly assure rigid mounting. Connections to external devices are via the connector assemblies on top of the interconnection wiring box. Cam latch devices lock the "suitcase" prior to insertion into the base assembly. A continuous gasket covers the facing edges of the split castings to provide a completely sealed assembly immune to environmental conditions.

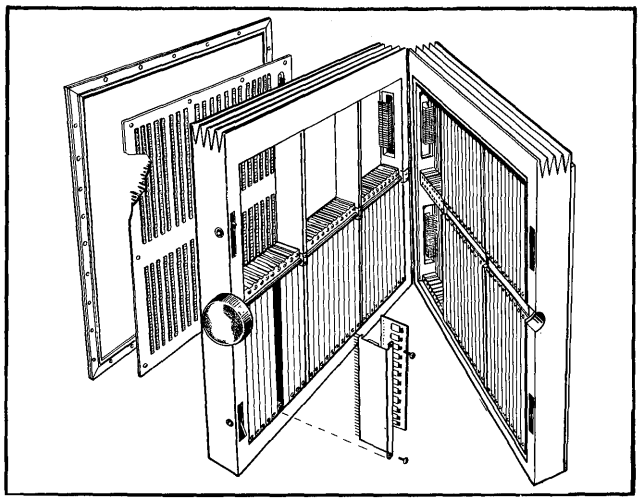
Circuits are packaged on printed circuit pluggable modules. The circuit network module is formed by joining together a carrier assembly and a glass epoxy printed circuit board containing integrated circuit flat-paks. The holder assembly contains 55 connector pins; the pins are formed as blade contacts on one end for external connections, and hooked upward on the other end to accept the plated-through holes on the printed circuit board. The printed circuit board can accommodate up to 12 flat-paks, which are dip-soldered to the



Circuit Network Module



boards. At final assembly, the printed circuit board is inserted into a grooved trough on the inside edge of the holder; the other end of the board is then fitted over the connector pins that protrude slightly above the p.c. board. The pin-to-board connection is then rigidly fixed by dip-soldering the assembly, thus ruggedizing the circuit network module. Heat is removed directly from the flat-pak source via an interface between the flat-pak and the aluminum carrier.



Typical D84 Module

CIRCUITS

Monolithic integrated circuits implement the logic throughout the system, except in the Memory Module, where special circuits are used to satisfy special high-frequency, low-level, and high-power signal requirements. Burroughs specifications for these circuits ensure worst-case operation over a temperature range of -50°C to 71°C. A life test in excess of 6×10^6 circuit-hours has resulted in zero failures – an indication of the reliability that can be expected from the proven circuits of the D84 System.

Integrated circuits make possible the small physical size and low power consumption of the D84 System. The simple construction and small number of component parts minimize cost and enable automated assembly, while maintaining environmental protection. Packaging of these circuits into circuit network modules has evolved from proven concepts implemented in earlier systems designs that used discrete components.

SYSTEM FUNCTIONAL CHARACTERISTICS

Because any particular D84 Modular Computer System is composed of a number of functional units, each of which has been selected from the many models available within its series, it is impractical to tabulate in this data sheet the characteristics of each unit that could be selected. Reference to the data sheets of the modules selected to comprise the desired system is therefore suggested. There are, however, many characteristics common to all models within a particular module series. These may be summarized as follows:

Central Data Processor - Series D84/100

Models within this series differ only in packaging approach. All models utilize the identical instruction complement. Execution times are a function of the type of memory module employed.

Memory Module - Series D84/200

Access times are maintained at 1 microsecond, but cycle times and/or write times vary among the various types.

SYSTEM FUNCTIONAL CHARACTERISTICS (Cont'd)

Input/Output Module - Series D84/500

This series is inherently the most variable, since the design must be tailored to meet the needs of a wide variety of devices. Available for inclusion in this series of models are channel designs such as:

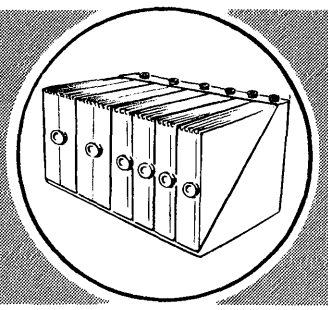
- A fully buffered channel capable of transfer rates up to 250,000 24-bit words per second when operating with a 4-μsec cycle time memory
- An unbuffered channel with transfer rates of 125,000 words per second when operating with a 4-μsec cycle time memory

Power Supply Module - Series D84/400

One model of this series serves the majority of the system configurations.

Control Panel Assemblies - Series D84/800

Models of this series generally contain identical panel indicators and controls. Major differences are in the interface logic contained in circuit network modules housed in the enclosure associated with the panel. The number of basic peripheral devices and the types employed will be the major element in the model determination.



ENVIRONMENTAL CAPABILITIES

The D84 is designed to withstand environments for vibrations, shock, and temperature imposed on military equipment. Some of the important operating and non-operating environments which the D84 can withstand are listed here.

Operating Environment	Imposed Stress Level	Applicable Specifications
Vibrations, Linear	MIL-STD-167 Type I, 0.5 to 5 cps, 5g peak, but not to exceed 6-inch peak-to-peak displacement; 5 to 200 cps, 10 g; 200 to 2000 cps, 20 g	MIL-I-983
Altitude	Pressures of 1062 to 11 millibars (1,300 feet below sea level to 100,000 feet above sea level)	MIL-M-1191 MIL-E-5400, Classes I through IV MIL-E-4158
Temperature	High: +71°C (160°F) at sea level Low: —50°C (—65°F) at sea level	MIL-I-983 MIL-E-4158 MIL-E-5400, Class II MIL-E-16400, Class I MIL-M-11991
RFI	MIL-I-26600	MIL-E-4158
Linear Shock	MIL-S-901, Type II MIL-E-5400, para. 3.2.21.6	MIL-I-983 MIL-E-16400
Humidity	100 percent from —32°C (—25°F) to +37.8°C (100°F) and as low as 5 percent at +52°C (+85°F)	MIL-I-983 MIL-E-5400 MIL-E-4158 MIL-E-16400 MIL-M-11991
Enclosure, Drip-proof	MIL-STD-108	MIL-I-983 MIL-E-16400
Blowing Sand & Dust	Air Force Specification Bulletin 106	MIL-M-11991 MIL-E-5400
Corrosive Atmosphere	Federal Test Method Standard No. 151, Method 811.1, for 48 hours	MIL-M-11991 MIL-I-983B MIL-E-5400 MIL-E-16400
Fungus	MIL-E-5272	MIL-M-11991 MIL-E-4158 MIL-E-5400

Non-operating Environment	Imposed Stress Level	Applicable Specifications
Temperature	—62°C (—80°F) to 75°C (+167°F)	MIL-I-983 MIL-E-4158 MIL-E-5400, Class II MIL-E-16400, Classes I through IV MIL-M-11991
Humidity	Absolute humidity as high as 13 grains of moisture per cubic foot of air. Relative humidity as great as 100 percent, with condensation as a result of temperature change	MIL-I-983 MIL-E-4158 MIL-E-5400 MIL-E-16400 MIL-M-11991
Transportation Shock	The D84 can withstand specified shock requirements, such as 28g shock in each of three mutually perpendicular directions. In addition, the D84 when packaged in the shipping container can withstand a 30 inch drop to concrete on all faces	As required
Mishandling Shock	The D84 assembly and each of the packages can withstand a 2-inch drop on a hardrock maple surface	As required

PHYSICAL CHARACTERISTICS

Since the D84 Modular Computer System admits of many possible combinations of modules, two different system configurations are given in the Module Complement Table in order to exemplify system capability and flexibility versus corresponding physical dimensions and power requirements.

Module Complement

	1 CDP 1 I/O 1 Power Supply (403) 1 Mounting Base (704) 1 4096-Wd Memory	1 CDP 1 I/O 1 Power Supply (403-1) 1 Mounting Base (704) 6 4096-Wd Memories
Height	18.0 inches	18.0 inches
Depth	16.5 inches	16.5 inches
Width	21.0 inches	30.0 inches
Volume	3.9 cu. ft.	5.25 cu. ft.
Weight	150 pounds	218 pounds
Power	160 watts	230 watts*

*Based on one 4096-word memory active, balance or standby

additional information

Available on request from
Defense and Space Marketing Division,
Burroughs Corporation
Paoli, Pennsylvania 19301

Burroughs Corporation

D676-21M

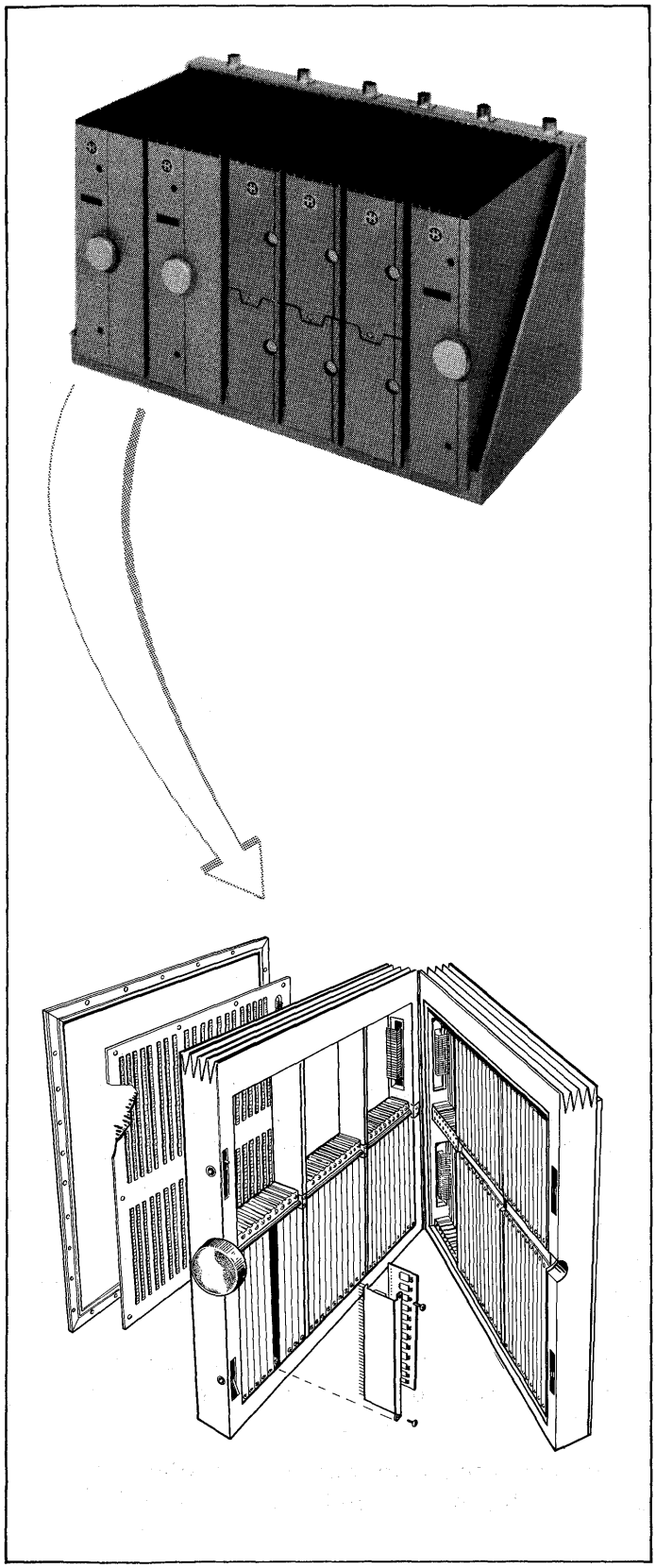
18 February 1965

Litho in U.S.A.

Burroughs

D84M Modular Computer System

CENTRAL DATA PROCESSOR MODULE (CDP) SERIES D84/100 MODEL D84/103

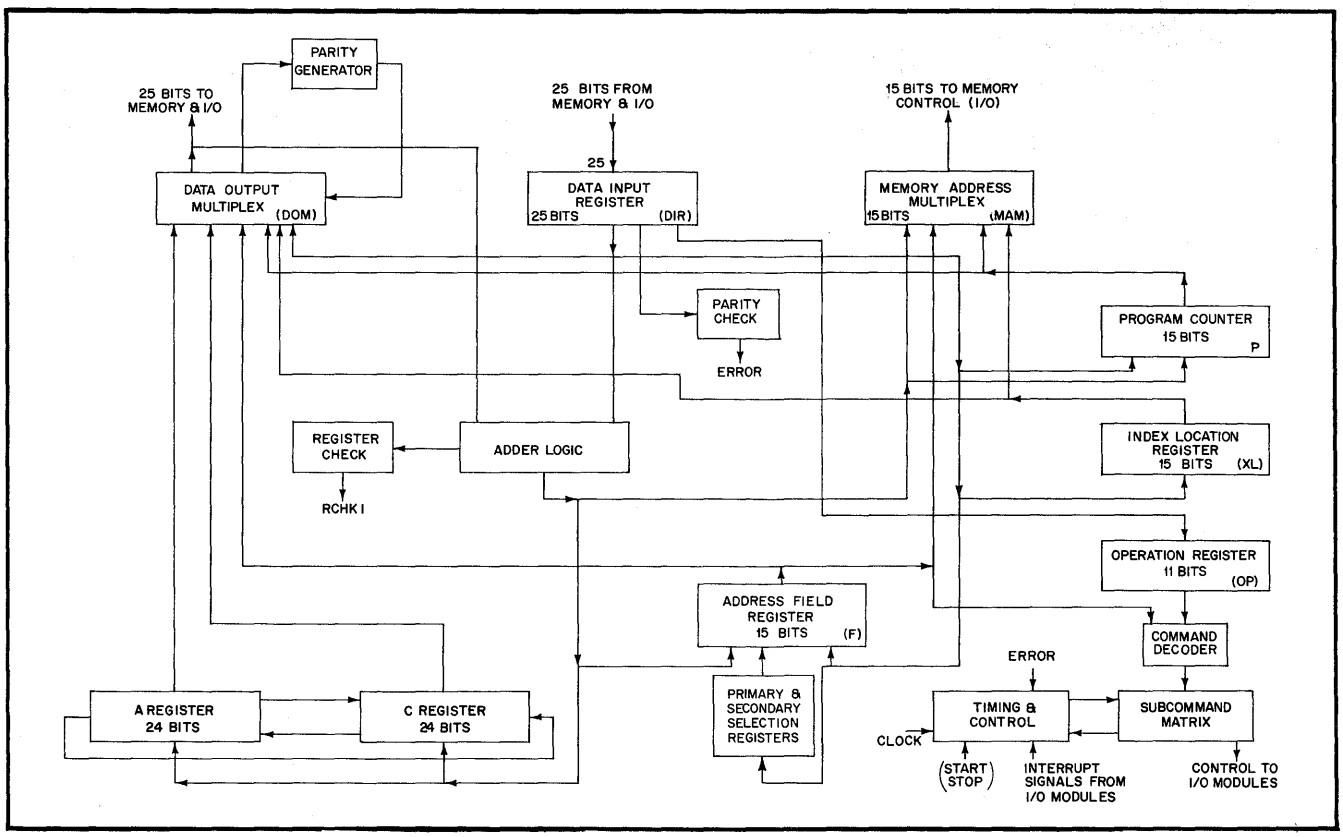


EQUIPMENT DEFINITION

The Series D84/100 Central Data Processor Module, one of the modular elements of the D84 Modular Computer System, is the arithmetic and program execution module. The CDP interfaces with and exercises control over all other modules of the D84 System.

FEATURES

- Fractional binary, fixed-point operation
- 23-bit parallel adder
- One-megacycle clock
- 47 basic commands; over 300 variations
- Multi-level indirect addressing
- Addressing capability of 32,768 words
- Index registers stored in memory
- Index registers program-determined
- Program interrupts
- Logical operations
- Memory block search
- Double precision operations
- Floating - point arithmetic programmable
- Monolithic integrated circuits
- MTBF: 11,700 hrs



Central Data Processor

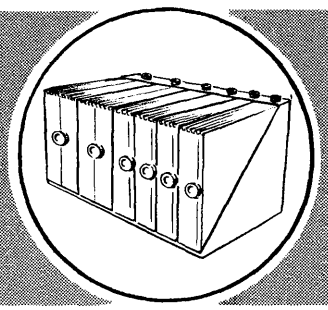
FUNCTIONAL DESCRIPTION

The D84/103 Central Data Processor Module consists of two functional areas: the arithmetic and the program execution control. As the diagram indicates, there is no complete separation between the two since they share many logic blocks in order to increase over-all system efficiency.

The arithmetic unit includes the two arithmetic registers, A and C, a 23-bit parallel adder, the data input register, and the data output multiplex. All data enters the CDP via the data input register. All data exiting the CDP is transferred out via the data output multiplex. Most arithmetic and logical operations are carried out either in the A or C registers.

The CDP program execution control comprises all the logic necessary for command decoding and subcommand generation, for fetching instructions and data from memory, and for control of data transfer between the CDP and other modules of the D84 system.

Instructions read from memory are transferred to the operation register and the address field register. If address field modification or indirect addressing is indicated, the appropriate address is transferred to the memory.



FUNCTIONAL CHARACTERISTICS

Operation

Synchronous, parallel

Word Length

24 bits plus parity check bit

Arithmetic Registers

Sign plus 23 bits magnitude

Operating Speeds

Basic clock rate: 1 mc/sec
Basic instruction execution, including memory access time: 4 μsecs
Typical execution times for a 4-μsec read/restore cycle DRO memory:

Literal:	4 μsecs
Add:	8 μsecs
Branch:	4 μsecs
Multiply:	28 μsecs

Addressing

Addressing capability up to 32,768 words.

Access time: 1 μsec
Read/restore cycle (DRO): 4 μsecs
Single address, direct, modular (4096 words/module)
On program command: multi-level indirect to any memory location within 32,768 words of memory

Index Registers

Index registers stored in memory
Number of index registers and their locations program-determined

Indexing

All instructions modifiable by content of selected index register.
Index modification of address field is modulo 32,768

Command Repertoire

47 basic commands; over 300 variations
Commands include single and double precision arithmetic, logical operation, and memory block search

Input/Output

Input and output commands for I/O data transfer between memory and I/O, or arithmetic unit and I/O
Program control over I/O by use of control descriptors
Program interrupts

AVAILABLE SOFTWARE

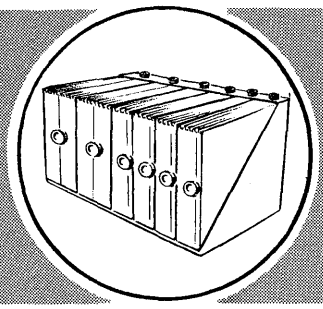
An Assembler Program, written in FORTRAN IV language, and Mathematical Subroutines (trigonometric, exponential, double precision, floating point, etc.) are currently available and applicable to any D84 Computer System configuration. Simulator and Diagnostic Routines, written for D84 Systems of specific configurations are also available; portions of which likewise apply to any D84 System configuration.

CDP ORDER CODES

Octal Code	Mnemonic Code	Description & Variations	Execution Time* (μsec)
30	ADD	Basic Addition	8
	ADA	Add to A	
	ADC	Add to C	
	ADAM	Add to A Magnitude	
	ADCM	Add to C Magnitude	
31	SUB	Basic Subtraction	8
	SBA	Subtract from A	
	SBC	Subtract from C	
	SBAM	Subtract from A Magnitude	
	SBCM	Subtract from C Magnitude	
10	ADL	Basic Add Literal	4
	ADAL	Add to A Literal	
	ADCL	Add to C Literal	
	ADALM	Add to A Literal Magnitude	
	ADCLM	Add to C Literal Magnitude	
11	SBL	Basic Sub Literal	4
	SBAL	Subtract from A Literal	
	SBCL	Subtract from C Literal	
	SBALM	Subtract from A Literal Magnitude	
	SBCLM	Subtract from C Literal Magnitude	
70	ADS	Basic Add & Store	12
	ADAS	Add to A and store	
	ADCS	Add to C and store	
	ADAMS	Add to A Magnitude and store	
	ADCMS	Add to C Magnitude and store	
71	SBS	Basic Sub & Store	12
	SBAS	Subtract from A and Store	
	SBCS	Subtract from C and Store	
	SBAMS	Subtract from A Magnitude and Store	
	SBCMS	Subtract from C Magnitude and Store	
61	BTE	Basic Block Test Equal	16+8(m-1)[1] 12+8(m-1)[2]
	BTAE	Block Test A Equal	
	BTCE	Block Test C Equal	
	BTAEM	Block Test A Equal Magnitude	
	BTCEM	Block Test C Equal Magnitude	
65	BTG	Block Test Greater Than	16+8(m-1)[1] 12+8(m-1)[2]
	BTAG	Block Test A Greater Than	
	BTCG	Block Test C Greater Than	
	BTAGM	Block Test A Greater Than Magnitude	
	BTCGM	Block Test C Greater Than Magnitude	
64	BTL	Block Test Less Than	16+8(m-1)[1] 12+8(m-1)[2]
	BTAL	Block Test A Less Than	
	BTCL	Block Test C Less Than	
	BTALM	Block Test A Less Than Magnitude	
	BTCLM	Block Test C Less Than Magnitude	
01	TLE	Test Literal Equal	4
	TAEL	Test A Equal Literal	
	TCEL	Test C Equal Literal	
	TAELM	Test A Equal Literal Magnitude	
	TCELM	Test C Equal Literal Magnitude	
05	TLG	Test Literal Greater Than	4
	TAGL	Test A Greater Than Literal	
	TCGL	Test C Greater Than Literal	
	TAGLM	Test A Greater Than Literal Magnitude	
	TCELM	Test C Greater Then Literal Magnitude	

[1]Test met.
[2]Test not met.
*Based on DRO memory, 1μsec access time, 4 μsec cycle time

Octal Code	Mnemonic Code	Description & Variations	Execution Time* (μsec)
04	TLL	Test Literal Less Than	4
	TALL	Test A Less Than Literal	
	TCLL	Test C Less Than Literal	
	TALLM	Test A Less Than Literal Magnitude	
	TCLLM	Test C Less Than Literal Magnitude	
21	TEQ	Basic Test Equal	8
	TAE	Test A Equal	
	TCE	Test C Equal	
	TAEM	Test A Equal Magnitude	
	TCEM	Test C Equal Magnitude	
25	TGT	Basic Test Greater Than	8
	TAG	Test A Greater Than	
	TCG	Test C Greater Than	
	TAGM	Test A Greater Than Magnitude	
	TCGM	Test C Greater Than Magnitude	
24	TLT	Basic Test Less Than	8
	TAL	Test A Less Than	
	TCL	Test C Less Than	
	TALM	Test A Less Than Magnitude	
	TCLM	Test C Less Than Magnitude	
35	RRB	Basic Reset Register Bits	8
	RAB	Reset A Bits	
	RCB	Reset C Bits	
	ANA	AND to A	
	ANC	AND to C	
34	SRB	Basic Set Register Bits	8
	SAB	Set A Bits	
	SCB	Set C Bits	
	XØRA	Exclusive OR to A	
	XØRC	Exclusive OR to C	
15	RRL	Reset Register Bits Literal	4
	RABL	Reset A Bits Literal	
	RELA	Reset Least Significant Half of A	
	RELC	Reset Least Significant Half of C	
	RCBL	Reset C Bits Literal	
	ANAL	AND to A Literal	
	REUA	Reset Upper Half of A	
	REUC	Reset Upper Half of C	
	ANCL	AND to C Literal	
14	SRL	Set Register Bits Literal	4
	SABL	Set A Bits Literal	
	SCBL	Set C Bits Literal	
	XØRAL	Exclusive OR to A Literal	
	XØRCL	Exclusive OR to C Literal	
75	RRS	Reset Register Bits & Store	12
	ANAS	AND to A and Store	
	ANCS	AND to C and Store	
	RABS	Reset A Bits and Store	
	RCBS	Reset C Bits and Store	
	BLOCK TEST	START ADDR = EFF ADDR Y STOP ADDR = Z (contents of XL) MATCHED ADDR(15BITS)→(PX) & IJC = 1 IF NO MATCH, IJC = 0 & PX UNCHANGED	



CDP ORDER CODES

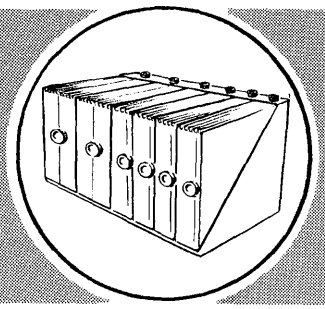
Octal Code	Mnemonic Code	Description & Variations	Execution Time* (μsec)
74	SRS	Set Register Bits & Store	12
	SABS	Set A Bits and Store	
	SCBS	Set C Bits and Store	
	XØRAS	Exclusive OR to A and Store	
	XØRCS	Exclusive OR to C and Store	
53	NMR	Basic Normalize	8+n
	NMA	Normalize A	
	NMC	Normalize C	
	NMB	Normalize Both	
	NMAG	Normalize A Logical	
	NMCG	Normalize C Logical	
	NMBG	Normalize Both Logical	
13	RSR	Reset & Shift Register	4+n
	REA	Reset A	
	REC	Reset C	
	REB	Reset Both	
	SRA	Shift Right A	
	SLA	Shift Left A	
	SRC	Shift Right C	
	SLC	Shift Left C	
	SRBAC	Shift Right Both A and C	
	SLBAC	Shift Left Both A and C	
	SRAG	Shift Right A Logical	
	SLAG	Shift Left C Logical	
	SRCG	Shift Right C Logical	
	SLCG	Shift Left C Logical	
	SRBG	Shift Right Both Logical	
	RØTA	Rotate A Left	
	RØTC	Rotate C Left	
	RØTB	Rotate Both Left	
	RSRA	Reset C and Shift Right A	
	RSLA	Reset C and Shift Left A	
	RSRC	Reset A and Shift Right C	
	RSLC	Reset A and Shift Left C	
	RASRB	Reset A and Shift Right Both	
	RCSRB	Reset C and Shift Right Both	
	RASLB	Reset A and Shift Left Both	
	RCSLB	Reset C and Shift Left Both	
	RSRAG	Reset C and Shift Right A Logical	
	RSLAG	Reset C and Shift Left A Logical	
	RSRCG	Reset A and Shift Right C Logical	
	RSLCG	Reset A and Shift Left C Logical	
	RASRBG	Reset A and Shift Right Both Logical	
	RCSRBG	Reset C and Shift Right Both Logical	
	RASLBG	Reset A and Shift Left Both Logical	
	RCSLBG	Reset C and Shift Left Both Logical	
	RRØTA	Reset C and Rotate A Left	
	RRØTC	Reset A and Rotate C Left	
	RARØTB	Reset A and Rotate Both Left	
	RCRØTB	Reset C and Rotate Both Left	
	DELAY	Program Delay Pseudo-Op	
	NOP	No Operation	
	SLBG	Shift Left Both Logical	

Octal Code	Mnemonic Code	Description & Variations	Execution Time* (μsec)
12	TTR	Test & Transfer Register	4
	TAZ	Test A all Zeros	
	TCZ	Test C all Zeros	
	TAØ	Test A all Ones	
	TCØ	Test C all Ones	
	TAMZ	Test A Magnitude all Zeros	
	TCMZ	Test C Magnitude all Zeros	
	TAMØ	Test A Magnitude all Ones	
	TCMØ	Test C Magnitude all Ones	
	TAN	Test A Negative	
	TCN	Test C Negative	
	TAP	Test A Positive	
	TCP	Test C Positive	
	TRAC	Transfer A to C	
	TRCA	Transfer C to A	
	TRCCA	Transfer Complement of C to A	
	TRCAC	Transfer Complement of A to C	
	TRMAC	Transfer Magnitude of A to C	
	TRMCA	Transfer Magnitude of C to A	
	TRCMAC	Transfer Complement of Magnitude of A to C	
	TRCMCA	Transfer Complement of Magnitude of C to A	
	TRSAC	Transfer Sign of A to C	
	TRSCA	Transfer Sign of C to A	
	TRCSAC	Transfer Complement of Sign of A to C	
	TRCSCA	Transfer Complement of Sign of C to A	
	CØMA	Complement A	
	CØMC	Complement C	
	CØMAM	Complement A Magnitude	
	CØMCM	Complement C Magnitude	
	CSA	Complement Sign of A	
	CSC	Complement Sign of C	
	SSA	Set Sign of A	
	SSC	Set Sign of C	
	RSA	Reset Sign of A	
	RSC	Reset Sign of C	
	ADØVTA	Add ØVC to A	
	ADØVTC	Add ØVA to C	
	AØVTRC	Add ØVC to A and Transfer to C	
	CØVTRA	Add ØVA to C and Transfer to A	
	TABL	Test A Bits Literal (12 - 23)	
	TCBL	Test C Bits Literal (12 - 23)	
16	TMC	Basic Test or Modify Controls	4
	S/RIJC	Set or Reset IJC	
	S/R/T/TREJC	Set, Reset, Test or Test and Reset EJC	
	S/R/T/TRRTE	Set, Reset, Test or Test and Reset RTE	
	S/R/T/TRØVA	Set, Reset, Test or Test and Reset ØVA	
	S/R/T/TRØVC	Set, Reset, Test or Test and Reset ØVC	
	S/R/T/TRDPE	Set, Reset, Test or Test and Reset DPE	
	S/R/T/TRCPE	Set, Reset, Test or Test and Reset CPE	
	S/R/T/TRIPE	Set, Reset, Test or Test and Reset IPE	
	S/R/T/TRPC	Set, Reset, Test or Test and Reset Program Control	
	SBJC	Set Both Jump Controls	
	RBJC	Reset Both Jump Controls	
	SBØV	Set Both Overflows	
	RBØV	Reset Both Overflows	
	TBØV	Test Both Overflows	
	TRBØV	Test and Reset Both Overflows	
	SCFF	Set Control Flip-Flops	
	RCFF	Reset Control Flip-Flops	
	TCFF	Test Control Flip-Flops	
	TRCFF	Test and Reset Control Flip-Flops	
		+2 Resets of IJC before Test - then reset	

CDP ORDER CODES

Octal Code	Mnemonic Code	Description & Variations	Execution Time* (μsec)
63	TMX	Test or Modify Index	12
	ADX	Add to X	
	DECX	Decrement X (Pseudo-Op)	
	TXL	Test X Less Than	
	TXG	Test X Greater Than	
	SEX	Set X	
45	STR	Basic Store Register	8
	STA	Store A	
	STC	Store C	
	STZ	Store Zeros	
40	SXL	Store XL Register	8
55	SCA	Double Precision Store	12
72	DPA	Algebraic (Basic DP Add)	12
	DPAM	Double-Precision Add Magnitude	
73	DPS	Algebraic (Basic DP Sub)	12
	DPSM	Double-Precision Subtract Magnitude	
76	LCA	Double Precision Load	12
33	MUL	Basic Multiply	28
	MULR	Multiply and Round	
	MULA	Multiply and Add A	
32	DIV	Basic Divide	51
	DVA	Divide A	
	DVB	Divide Both	
36	LDR	Load Register	8
	LDA	Load A	
	LDC	Load C	
37	LXL	Load XL Register	8
77	MDT	Memory Data Transfer	12
	STX	Store X	
	LDX	Load X	
03	BCN	Branch Conditional	4
	BIS	Branch on IJC Set	
	BIR	Branch on IJC Reset	
	BES	Branch on EJC Set	
	BPCS	Branch on Program Control Set	

Octal Code	Mnemonic Code	Description & Variations	Execution Time* (μsec)
02	BUN	Unconditional Branch	4
	LDP	Load P	
27	BCM	Branch on Condition of Memory	8
	LPM	Load Primary Selection Register	
	LSM	Load Secondary Selection Register	
	LBM	Load Both Selection Registers	
	LMAC	Load Memory Access Controls	
	APM	Assign Primary Module (Pseudo-Op)	
	ASM	Assign Secondary Module (Pseudo-Op)	
67	LSP	Load & Store P Count	12
	LPSAC	Load P and Store Access Controls	
	LACSP	Load Access Controls and Store P	
	LSMAC	Load and Store Memory Access Controls	
41	STP	Store P and Memory Access Controls	8
	SMAC	Store Memory Access Controls	
06	CDT	Control Descriptor Transfer	4
	ØCDA	Output Control Descriptor via A	
	ØCDB	Output Control Descriptor via B	
	ØCDC	Output Control Descriptor via C	
	ØCDD	Output Control Descriptor via D	
07	TRO	Transfer Register Out	4
	ØFAA/B/C/D	Output from A Register via A, B, C or D	
	ØFCA/B/C/D	Output from C Register via A, B, C or D	
22	TDO	Transfer Data Out	8
	ØFMA/B/C/D	Output from Memory via A, B, C or D	
26	TIR	Transfer Input to Register	4
	INAA/B/C/D	Input to A Register via A, B, C or D	
	INCA/B/C/D	Input to C Register via A, B, C or D	
66	TIM	Transfer Input to Memory	8
	INMA/B/C/D	Input to Memory via A, B, C or D	
		Memory Access Controls:	
		P Register	
		Primary Selection Register	
		Secondary Selection Register	



TYPICAL AVAILABLE SUBROUTINES

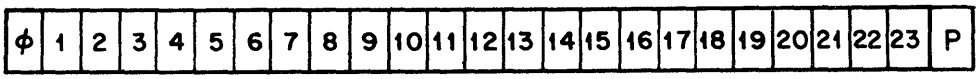
SUBROUTINE		EXECUTION TIME (μsec)*
Double precision multiplication		132
Double precision division	min	234+2n**
	max	316+2n
Square root (single precision)	min	234
	max	1060+6n
Square root (double precision)		1279+6n
Floating point multiplication		74
Floating point division	min	106+n
	max	188+n
Floating point addition/subtraction	min	28
	max	85+2n

*Based on 4 μsec memory cycle time

**n is the number of shifts executed

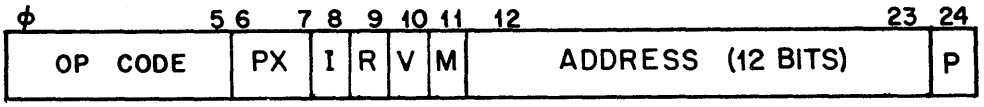
CDP WORD STRUCTURE

DATA WORD

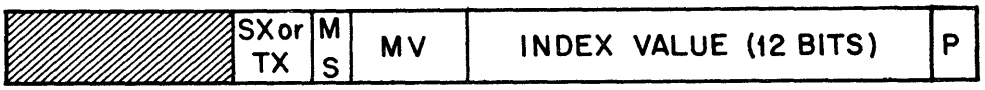


ϕ – SIGN POSITION 1-23 – MAGNITUDE BITS

INSTRUCTION



INDEX



INDIRECT ADDRESS

PX - Specifies primary index register

I - Specifies indirect address (follows indexing)

R-V - Command options

M - "0" specifies primary memory
"1" specifies secondary memory

SX - Secondary index (specifies register)

TX - Tertiary index (specifies register)

MS - Specifies that MV is to be substituted for previous module designation

MV - Designates Memory Module

OTHER CHARACTERISTICS

CDP logic is implemented by single-input resistor transistor logic (RTL) circuits in monolithic integrated circuit form. Burroughs specifications for these devices ensure worst-case operation over the full temperature range of the D84 equipment. Both medium-power and low-power devices are used.

The Central Data Processor Module is housed in a hinged cast aluminum-magnesium enclosure which is completely environmentally sealed and RF tight. Each portion of the housing is basically identical, accommodating 172 circuit network modules when both halves are filled to capacity. Back-plane wiring in each housing is readily accessible upon removal of the sealed side covers.

Height	Weight
16 inches	50 pounds
Width	Volume
6 inches	0.78 cubic foot
Depth	Power
14 1/2 inches	43 watts

ENVIRONMENTAL CHARACTERISTICS

See Data Sheet 676-21M

additional information

Available on request from
Defense and Space Marketing Division,
Burroughs Corporation
Paoli, Pennsylvania 19301

Burroughs Corporation

D676-22M

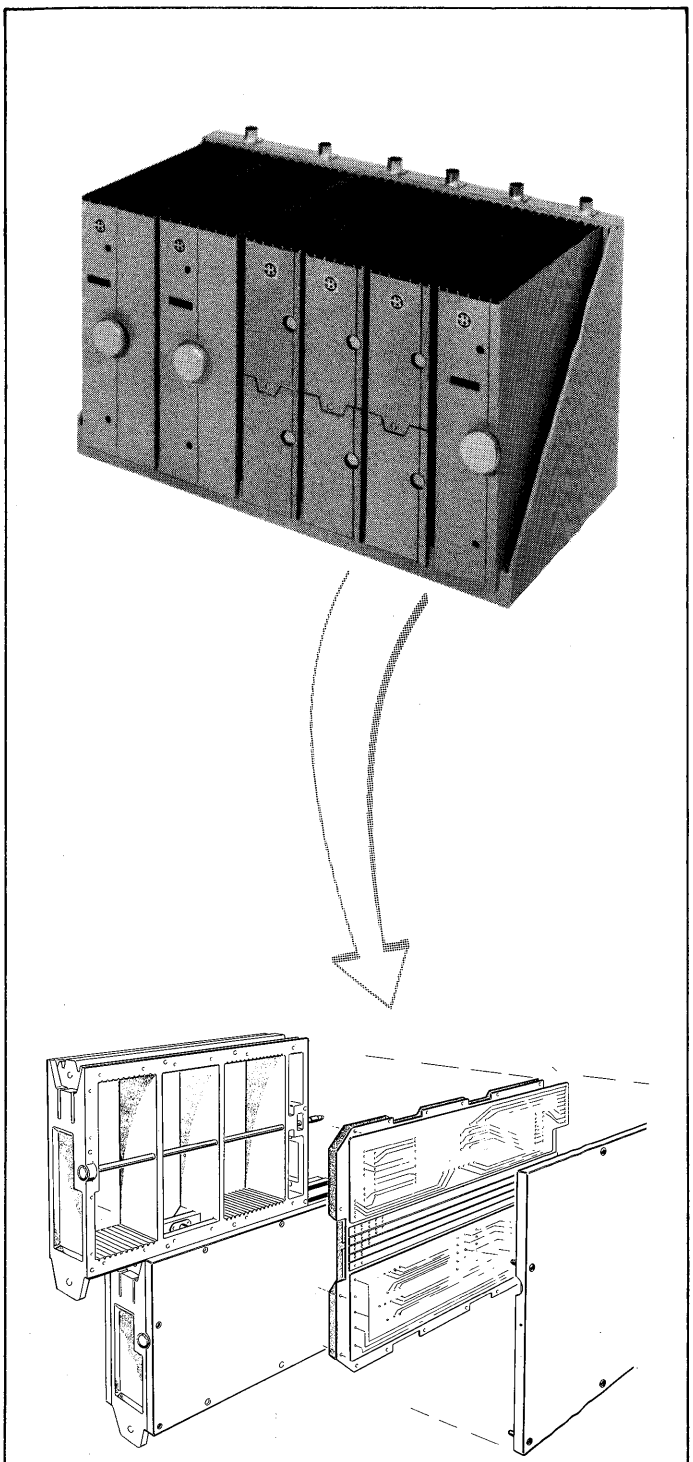
18 February 1965

Litho in U.S.A.

Burroughs

D84M Modular Computer System

MEMORY MODULE
SERIES D84/230
MODEL D84/233



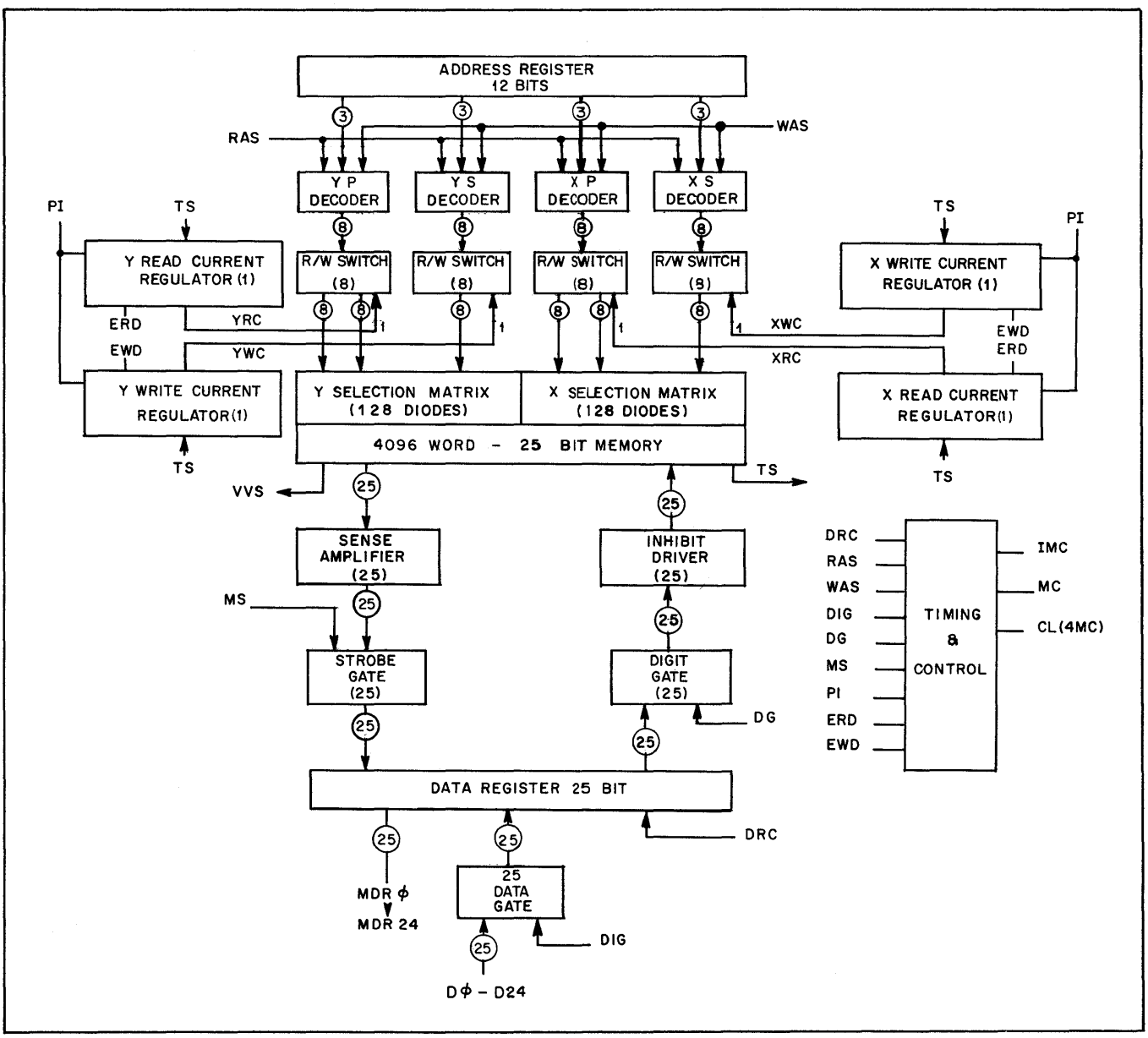
EQUIPMENT DEFINITION

The Model D84/233 Memory Module, one of the modular elements of the D84 Modular Computer System, performs the information storage function. The memory is a DRO (destructive read-out) type, using wide temperature ferrite cores operated in a coincident current mode, and configured in a 4096-word 25-bit array. Operation may be in a read-restore or clear-write mode. Access time is less than 1 microsecond; cycle time is 4 microseconds. Silicon monolithic integrated circuits implement logical gating up to the final switching stages. Highly reliable discrete components are used in the final driver-switch stages.

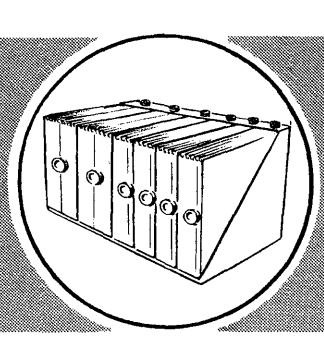
FEATURES

The Model D84/233 Memory Module features:

- Maximum use of integrated circuits
- Low input power
- Stable operation over wide temperature range
- 25-bit words: 24 data, 1 parity
- Rugged, light-weight construction
- RFI protected
- Environmentally sealed
- Pluggable circuit module cards
- Pluggable core stack assemblies
- Forced air cooling or fans not required
- Backplane wiring readily accessible
- Corrosion - resistant exterior
- Memory protected against overheat, over-flow, over/under-voltage
- MTBF: 3,500 hrs



Memory Module



FUNCTIONAL DESCRIPTION

A 12-bit address is required to provide selection of one of 4096 memory locations. The desired 12-bit address is transmitted to the selected Memory Module from an address register which is part of the Module Interface Control located in the Input-Output module. Three bits from the address register are presented to the Y prefix (YP) decoder array, while three additional bits are presented to the Y suffix (YS) decoder array. This arrangement provides for selecting one of 64 "Y" drive lines via the sixteen read-write (R/W) switches. Similarly, the remaining six bits are used to select one of 64 "X" drive lines through sixteen read-write switches.

With the address selection completed, the current regulators supplying X and Y read currents are enabled. Cores at the intersection of the selected drive lines are switched to the ZERO state, causing output signals to be introduced to the sense amplifiers at bit locations corresponding to the cores that originally had ONEs stored in them. After amplification in the sense amplifiers, the information is strobed into the 25-bit data register (DR), for use elsewhere in the system.

In the read-restore mode of operation, re-entry of information from the data register to the Memory Module cores is accomplished by energizing the X and Y write current regulators, following the application of an inhibit current to those bits which are to remain ZERO. In the clear-write mode, external information is presented to the Memory Module data register prior to application of the inhibit and write currents.

Active power dissipation of a memory block (4096 words) is less than 75 watts. Stand-by power consumption is 12 watts. The power drain at a given time is a function of the number of active and stand-by memory blocks. Input power values are based on one 4096-word system being active, and the remaining words on "stand-by". Worst-case active power considers a 4-μsec cycle with all inhibit drivers turned on.

The Model D84/233 Memory Module enclosure accommodates 4,096 words. A maximum of eight such modules may be employed in a D84 system.

FUNCTIONAL CHARACTERISTICS

Memory Access Time

Less than 1.0 μsec

Memory Cycle Time

Less than 4.0 μsecs

Memory Type

DRO (Destructive Read-Out)

Modes

Read-restore or Clear-write

Cores

Wide temperature ferrites

Memory Module Capacity

4096, 25-bit, words

ELECTRICAL CHARACTERISTICS

Circuits

Silicon monolithic, and highly reliable discrete components

RFI (Radio Frequency Interference)

See Data Sheet D676-21M

Power

75 watts active, 12 watts standby

ENVIRONMENTAL CHARACTERISTICS

See Data Sheet D676-21M

PHYSICAL CHARACTERISTICS

Module Height

8 inches

Module Width

3.9 inches

Module Depth

14 1/2 inches

Module Volume

0.26 cubic feet

Module Weight

13 pounds

Housing

Cast aluminum magnesium

Cooling

Radiation and internal conduction (no fans required)

additional information

Available on request from
Defense and Space Marketing Division,
Burroughs Corporation
Paoli, Pennsylvania 19301

Burroughs Corporation

Litho in U.S.A.

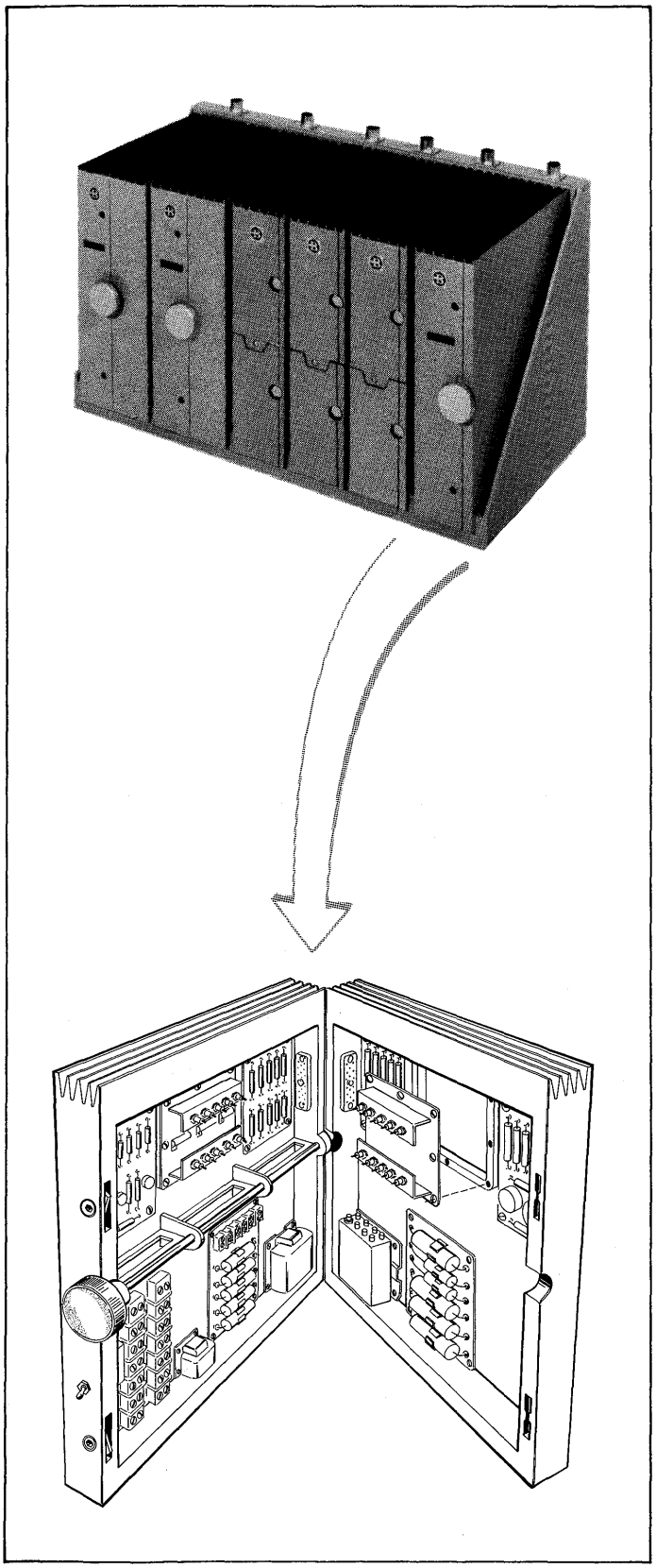
D676-26M

18 February 1965

Burroughs

D84M Modular Computer System

POWER SUPPLY MODULE
SERIES D84/400
MODEL D84/403



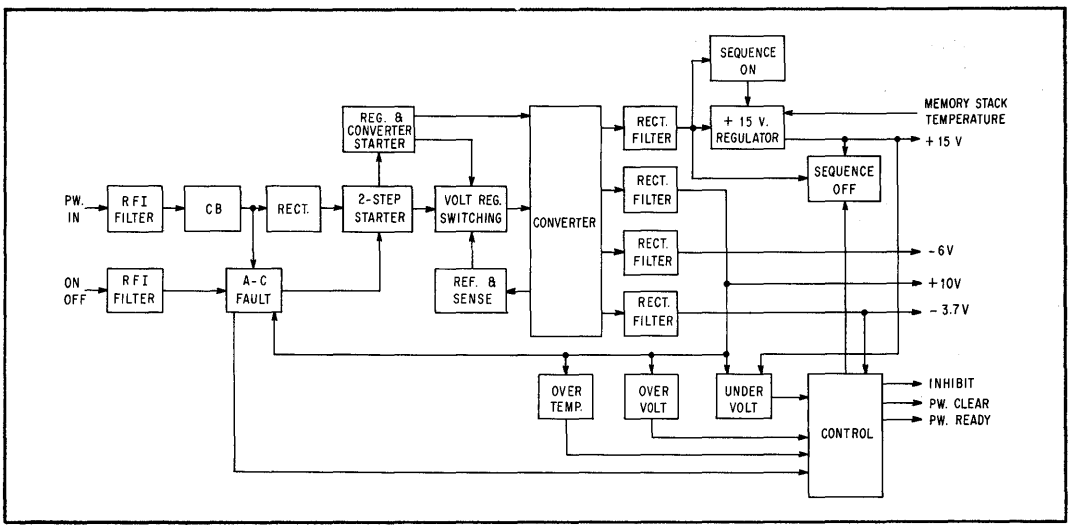
EQUIPMENT DEFINITION

The Model D84/403 Power Supply Module supplies operating voltages for D84 Modular Computer System Modules:

Central Data Processor Module, Series 100
Memory Modules, Series 230
Input/Output Modules, Series 500

FEATURES

- Efficiency approximately 80 percent
- High speed fault protection
- Converter provides all outputs
- Single voltage regulator for converter
- Memory information protection if primary power fails
- No input power transformer
- Forced cooling not required
- Quick access to internal parts
- Various sizes available to suit system size requirements
- One temperature variable output for memory
- MTBF: 29,860 hrs.



Power Supply

FUNCTIONAL DESCRIPTION

A power system efficiency of about 80 percent is achieved by using a single high-voltage switching type regulator rather than several low-voltage regulators. Compactness is achieved by eliminating the need for an input power transformer and using a high-frequency d-c to d-c converter.

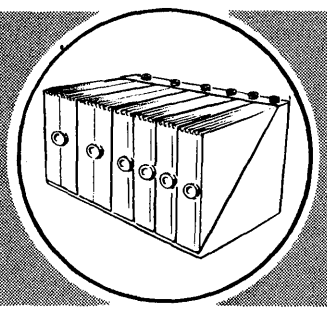
Input power, filtered and rectified, is fed to the starter and converter drive circuit. A series regulator controls the converter input voltage. The converter output is sensed to provide input control to the regulator. Rectified converter outputs provide the specified d-c outputs to the computer circuits. A temperature-controlled series regulator gives the temperature-variable 15-V supply.

Power sequencing protects information storage in memory. Logical control signals to the computer control ensure proper computer operation during power interrupts. Over- and under-voltage sensing on the output and under-voltage sensing on the input are also provided.

PHYSICAL CHARACTERISTICS

The power supply module comprises two cast aluminum-magnesium housings that are hinged together for quick access to internal parts. The enclosures thus formed is completely sealed with respect to environment. Radiation cooling and internal conduction are used; no fans or external cooling air are required within the temperature limits of the D84 specifications (see Data Sheet D676-21M). Electrical components are mounted directly in the casting or on subassembly modules that are easily removed for maintenance and repair.

	D84/403		D84/403
Height:	16 inches	Volume:	0.52 cu ft
Width	4.5 inches	Weight:	35 lb.
Depth:	14 1/2 inches	Output Capacity:	300 watts



ELECTRICAL CHARACTERISTICS

Primary Power Requirements

120/208 volts (84v to 190v per phase)
3-Phase; 400 cycles (47 cps to 1000 cps)
Power Factor - Near unity

Voltage Outputs

- 6 volts
+ 3.7 volts
+10 volts
+15 volts (output designed to vary linearly from +15 volts at 100°C to +13.5 volts at -55°C)

Voltage Regulation

+15-volt output ±3 percent (for 100 percent active load change)
Other outputs ±5 percent (includes maximum output voltage variations measured peak to peak, resulting from worst case combination of maximum variation of input voltage, input frequency, temperature, output noise, output ripple, and 50 percent load changes)

Memory Data Protection

Loss of a-c input power, and turn-on/turn-off transients will not result in loss of information stored in memory

Supply Protection

Over- and under-voltage protection and automatic shut-off
Short circuit detection and automatic shut-off
Over-temperature detection

Restart Provisions

Automatic restart following input failures
Manual restart following internal or load failure
Manual restart following output voltage fault detection of over-temperature conditions

Components

All solid-state elements except for one 3-phase circuitbreaker

Signals Generated

Clear
Power Ready
Memory Inhibit

ENVIRONMENTAL CHARACTERISTICS

See Data Sheet D676-21M

additional information

Available on request from
Defense and Space Marketing Division,
Burroughs Corporation
Paoli, Pennsylvania 19301

Burroughs Corporation

D676-31M

18 February 1965

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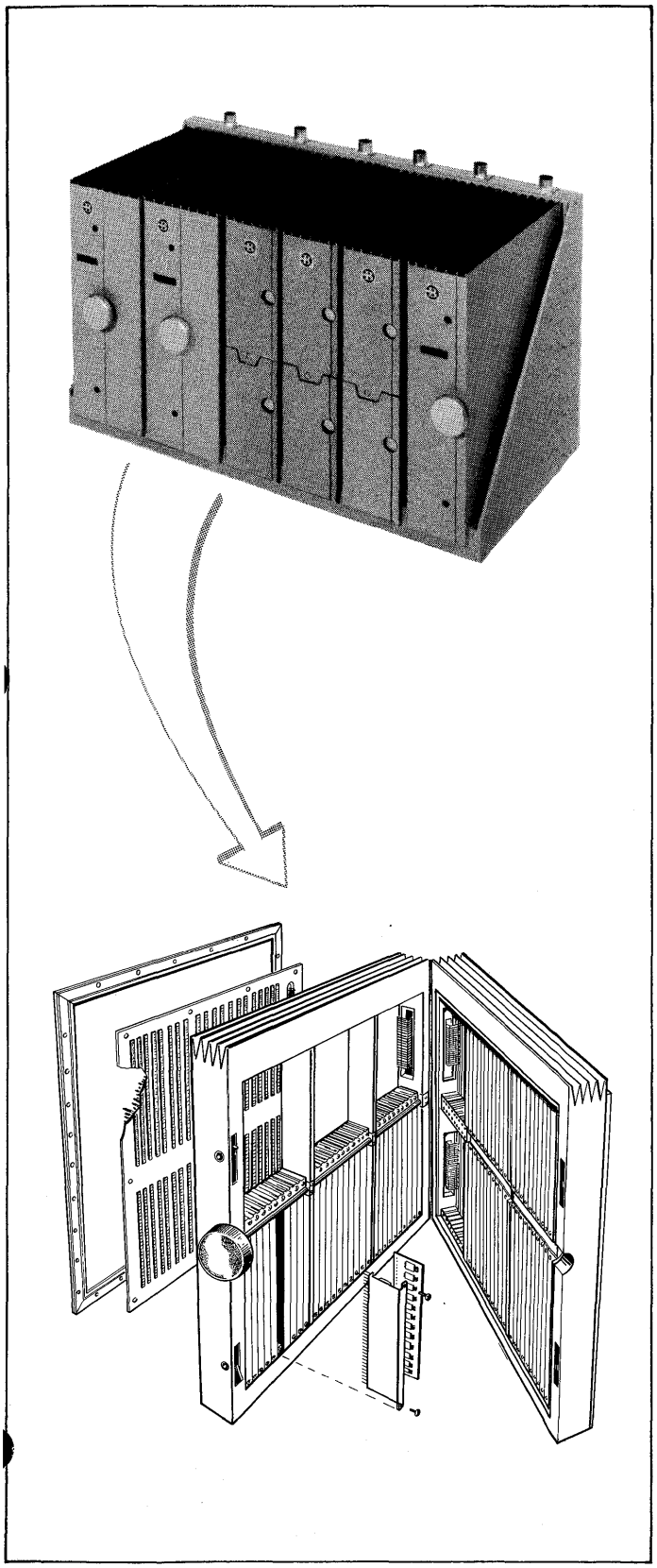
D84M Modular Computer System

INPUT-OUTPUT MODULE
SERIES D84/500
MODEL D84/504



EQUIPMENT DEFINITION

The Series D84/500 Input/Output Module, one of the modular elements of the D84 Modular Computer System, handles all inputs and outputs to the D84 System. The D84/504 I/O Module is used in systems employing low-speed peripheral devices.

FEATURES

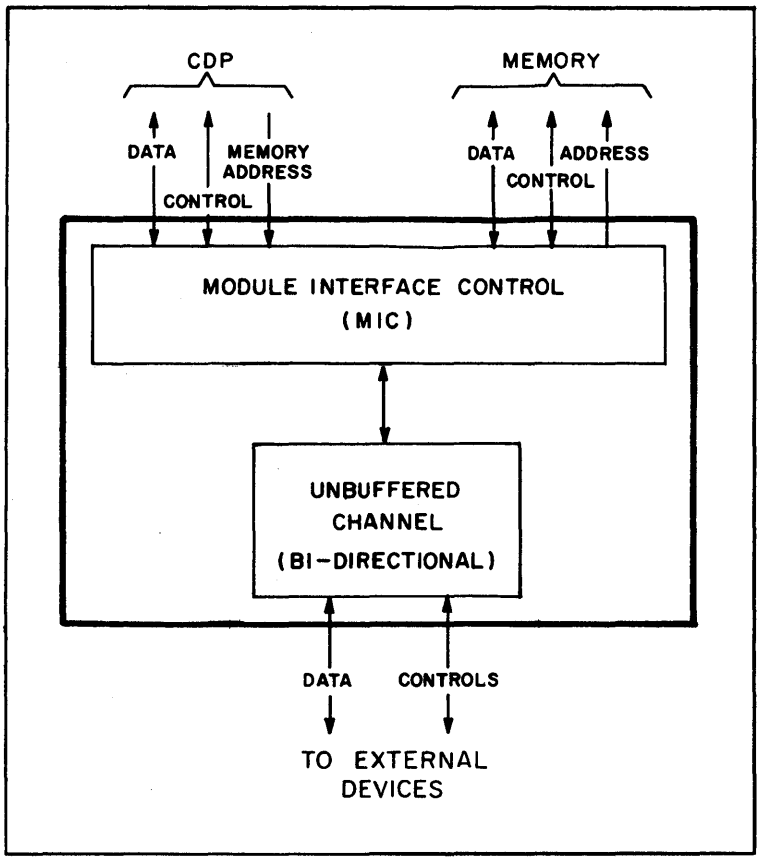
The Model D84/504 I/O Module features:

- An unbuffered channel capable of carrying on multiple programmed data transfers after a single initial descriptor set-up
- Module interface control (MIC), used for memory addressing, switching, and interrupt functions
- Addressable interval timer with programmable presets
- Compatibility logic to interface with paper tape reader and punch, and typewriter input and output.

MTBF: 12000 hrs.

FUNCTIONAL DESCRIPTION OF D84/504-1 I/O MODULE

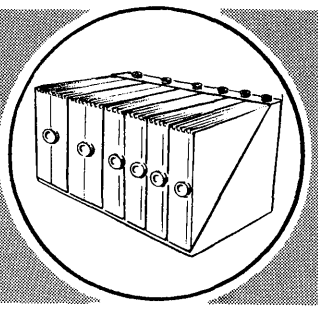
This module is divided into three functional areas: module interface control (MIC), an unbuffered channel, and the compatibility logic for paper-tape and typewriter.

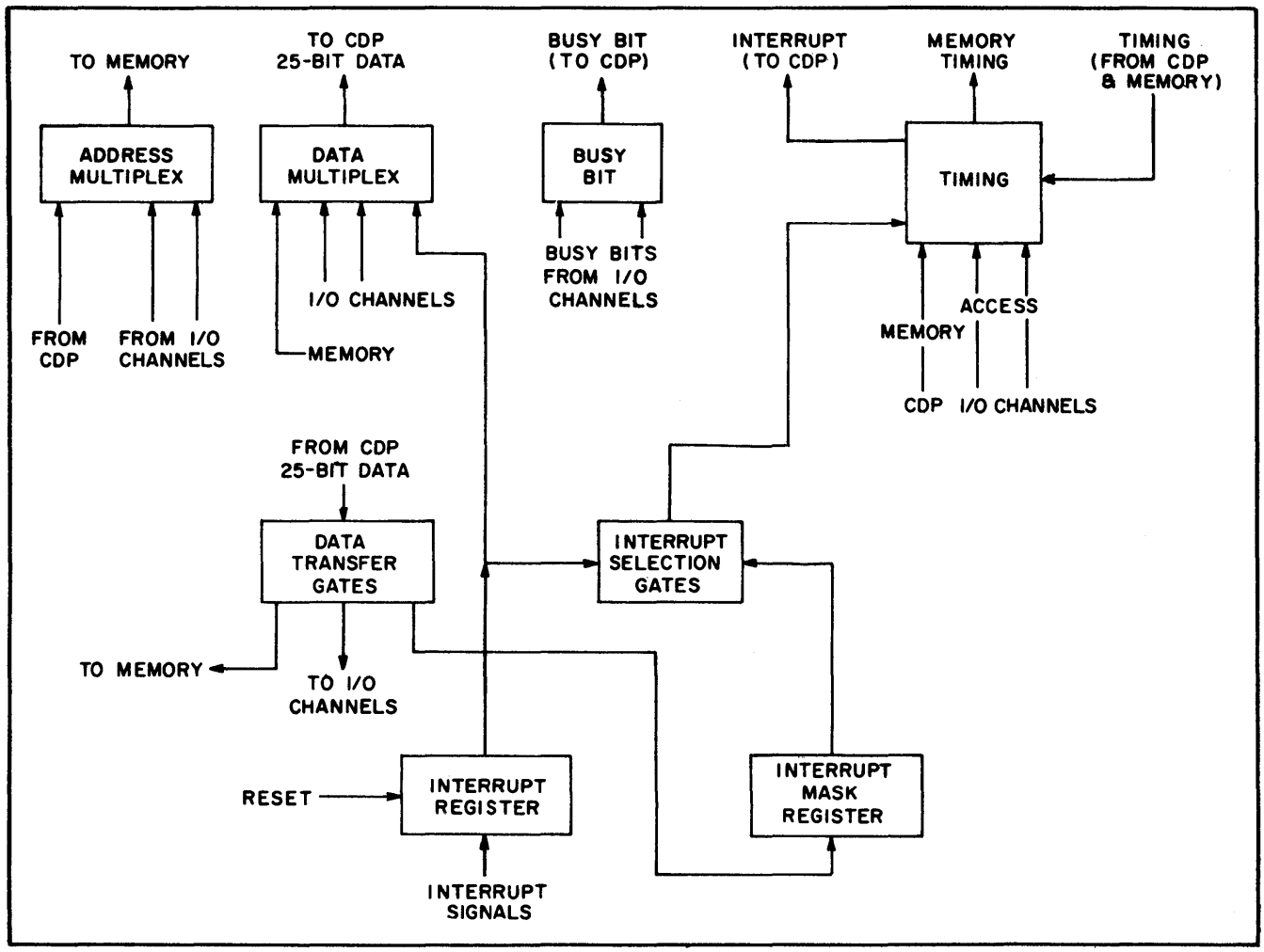


Model D84/504-1 Input/Module

Module Interface Control (MIC)

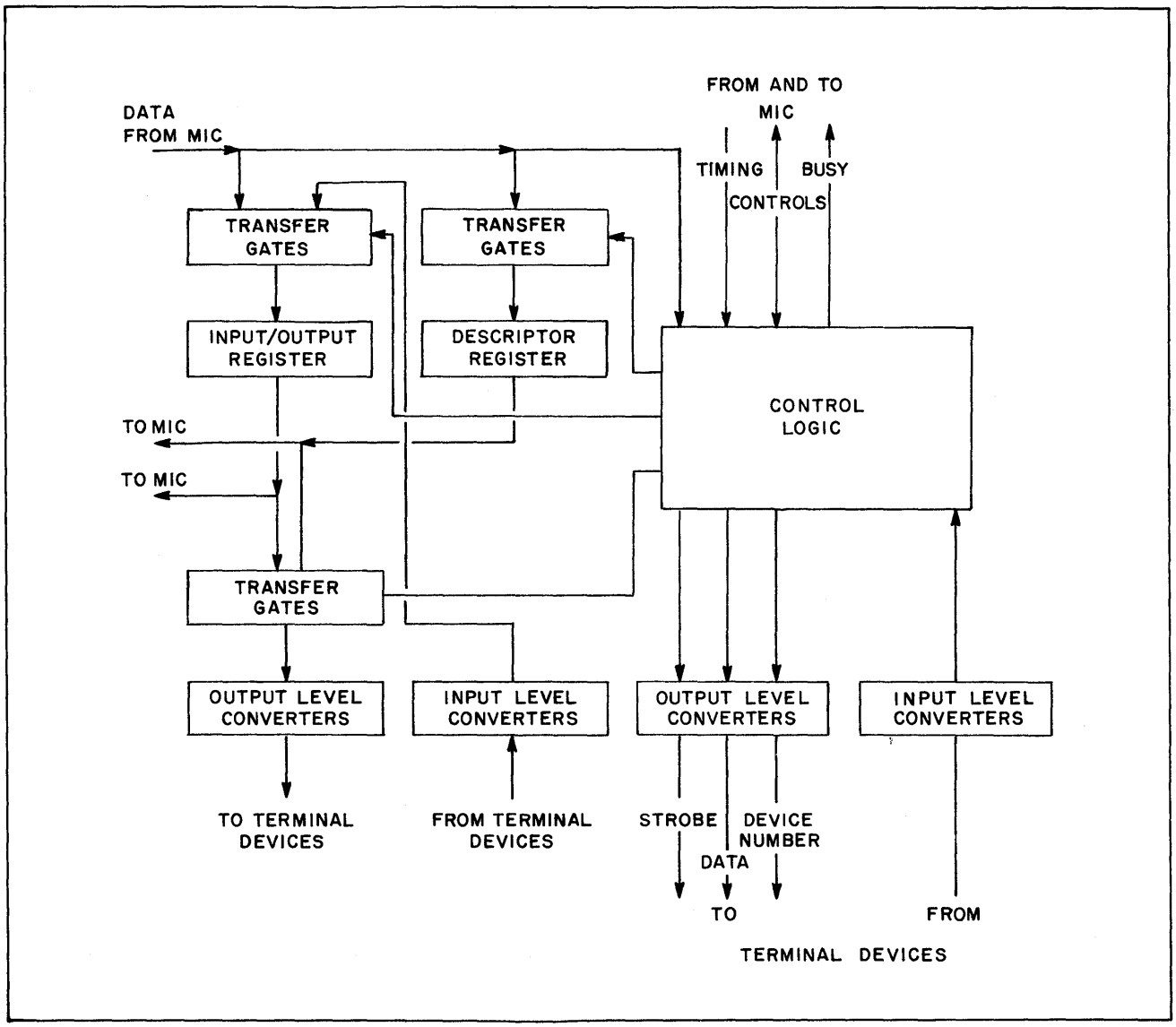
The module interface control logic controls the flow of data between the Central Data Processor (CDP), memory, and input/output; resolves memory access conflicts; and contains the program interrupt logic. The MIC services memory access requests in order of their occurrence, with an access request from the CDP having the priority. If input and output data is handled by program command, the MIC provides the logic for the data





Module Interface Control

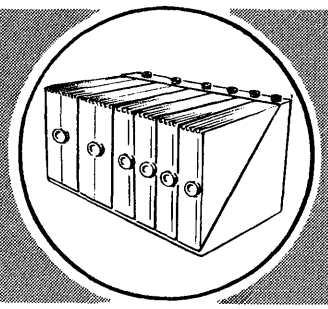
routing. The MIC also provides a fully maskable program interrupt. Provisions are made for 24 program interrupts. When an interrupt signal occurs, a bit is set in the interrupt register. However, a program interrupt is generated only if the specific interrupt has not been masked out by the interrupt mask. The interrupt mask is preset by the program. The program may also sample and/or reset the content of the interrupt register.



Unbuffered I/O Channel

Unbuffered Input/Output Channel

The unbuffered channel is capable of servicing a number of peripheral devices. It does not include any specialized input and output controls except the interval timer and the specialized logic to present attachment of paper tape and typewriter (both for input and output use). The program controls operation of the unbuffered channel, using the control descriptor command to identify a peripheral device and to determine the function to be performed



The program, finding the unbuffered channel not busy, transmits a descriptor specifying a device. A "select device strobe" is generated, indicating that a descriptor transfer is in process. The descriptor is presented on the common 24-bit output bus linking all peripheral devices. When the "select device strobe" is high, all devices examine the output bus to determine which device is being selected. The intended recipient then transmits a "received" signal on the common control line. The selected device also transmits an identification code which is compared with the descriptor, thus assuring that only the proper device has been selected. The device selection descriptor need not be retransmitted as long as the selected device remains the source or sink of data. When the device selection has been completed, data transfers may be made under program control.

Interval Timer

Functionally, the interval timer is part of the unbuffered channel. The interval timer can be preset, under program control, with a least significant bit precision of 1 millisecond.

FUNCTIONAL CHARACTERISTICS

Data Transfer Rates

Based upon use of 4 μsec cycle time DRO memory

Buffered channel: 250,000 24-bit words per second (maximum)

Unbuffered channel: 125,000 24-bit words per second (maximum)

PHYSICAL CHARACTERISTICS

Height

16 inches

Weight

40 pounds

Width

6 inches

Volume

0.78 cu ft

Depth

14 1/2 inches

ELECTRICAL CHARACTERISTICS

Silicon monolithic integrated, and discrete components

Circuit Network

Module Capacity

172

RFI Protected

See Data Sheet D676-21M

Input Power

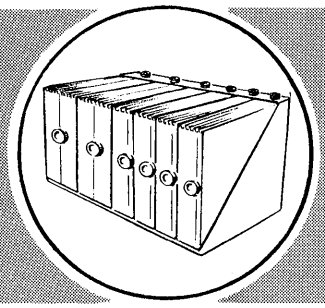
21 watts

Interface Signal Levels

0 and +3 volts

ENVIRONMENTAL CHARACTERISTICS

See Data Sheet D676-21M



additional information

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Burroughs Corporation

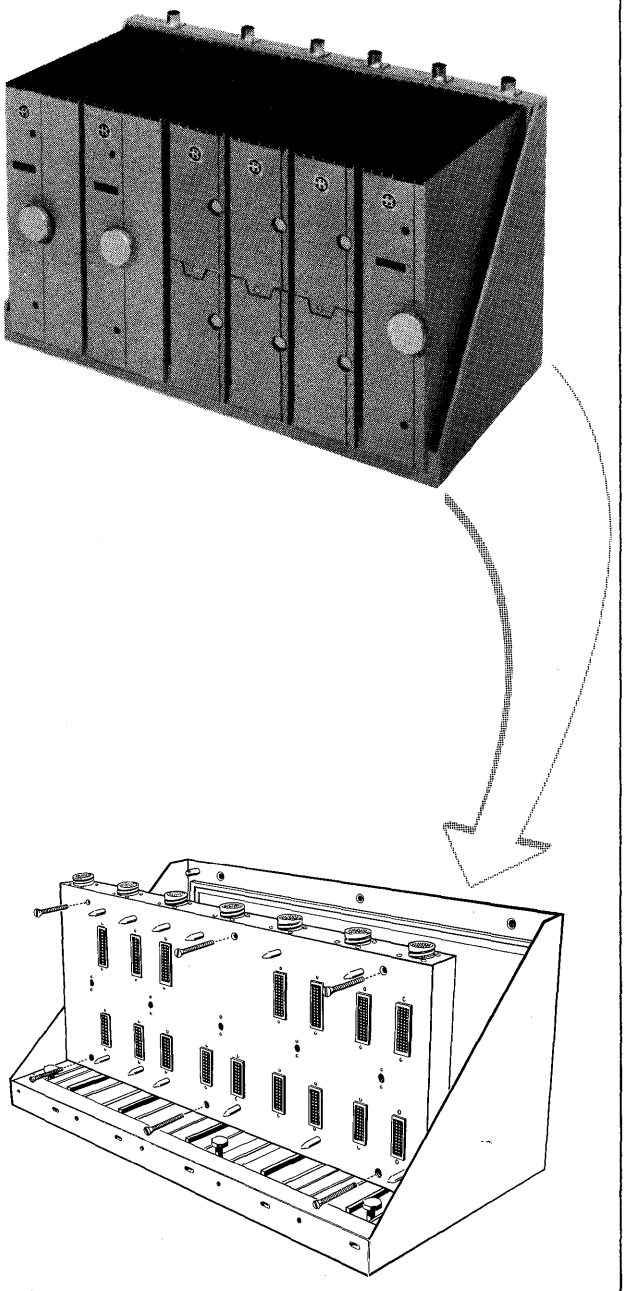
D676-36M

18 February 1965

Burroughs

D84M Modular Computer System

MOUNTING BASE ASSEMBLY SERIES D84/700 MODEL D84/704



EQUIPMENT DEFINITION

The Model D84/704 Mounting Base Assembly

Provides a common mounting for D84 Modular Computer System Modules:

Provides backplane wiring for all module interconnections

Provides for connection of peripheral equipment, primary power input, and other signal sources or destinations

FEATURES

- Available for various size system configurations
- Simple, rugged construction
- Removable backplane assembly
- Module arrangement to suit requirements
- Connector types and locations to suit customer requirements
- Rapid removal of module packages for ease of maintenance
- Expandable memory capacity without electrical or structural alterations

PHYSICAL CHARACTERISTICS

A rugged structural aluminum framework and backplane assembly, both designed to withstand or exceed the environmental specifications of the D84 system. The removable backplane assembly provides interfacing connection between each D84 module to produce an integrated computer system. Power and input/output connections to the computer system are provided for by standard MIL type connectors mounted on the top edge of the backplane assembly. Module positioning and support pins and rails are included; installation mounting bolt locations can be arranged to suit customer requirements.

Height

18 inches

Depth

16 inches

Width

determined by module complement

Weight

approximately 15 pounds

ENVIRONMENTAL CHARACTERISTICS

See Data Sheet D676-21M

additional information

Available on request from
Defense and Space Marketing Division,
Burroughs Corporation
Paoli, Pennsylvania 19301

Burroughs Corporation

D676-29M

18 February 1965

Litho in U.S.A.