MAINTENANCE TEST ROUTINE (MTR)

CARD DECK

The enclosed card deck consists of a two-card binary loader, six tape unit designation cards and a mag tape loader routine. When reading the deck in, the sequence must be as stated above with one exception. The tape unit designation card which corresponds to the tape unit on which the test tape is mounted must be the last card in the group of six. All six cards can be left in the deck between the binary loader and the tape loader.

TEST TAPE

The enclosed test tape contains the four basic tests, the General Control Routine (GCR) and all the test cases used by GCR. The test tape can be mounted on one of the tape units A thru F at high density.

INSTRUCTIONS

Load the test tape on one of the tape units A thru F. Place the appropriate tape unit identification card as the last card of the six identification cards. At the processor, inhibit IOST and turn the "Step on Operator" switch on. All other switches in normal position. Memory modules 0 and 1 must be on line and operating properly. If any of the other memory modules are in local for any reason, the modules above this module must be placed in local also. The SPO must be operative. Any of the basic I/O channels can be used. Place "Card Load Select" in "Card Load". After the tape unit and card reader are loaded and ready, hit halt/load.

OPERATION

After the card deck has read into memory, the first basic test will be read into memory. After the first has successfully passed the required number of times, the second basic test will be read in from tape and start running. This continues until all four basic tests have been read in and passed successfully. The fifth read-in from tape is the General Control Routine and after it has been read in, control is transferred to this routine. A message is printed out on the SPO indicating the number of processors and memory modules on line. GCR will call in the first group of test cases from tape and start the MTR testing procedures. Each test case is repeated twenty-five (25) times. After all test cases in this group or block have successfully passed the required number of times, the next group is called in from tape. This procedure continues until all test cases have been tested, at which time a message will be printed out on the SPO signaling the end of testing. If the

system has only one processor, the tape will rewind and the complete operation will be repeated. If two processors are on the system, after the printout is completed, change the processor designation switch and push the single pulse button on the new processor 1. This will cause the tape to be rewound and the testing operation will be repeated on the new processor 1.

The total running time for the four basic tests and the MTR portion is less than 15 minutes, provided no errors are detected.

ERROR DETECTION

Basic Tests - If an error is detected by any of the four basic tests, the only indication will be the routine stops with a 2411 in the T register. All conditional halts in these basic tests are controlled halts and will only be used if the test failed. If this condition occurs, record the contents of the C and S registers and the number of the basic test which failed. The basic test number can be determined by counting the number of tape reads before the failure. Until receipt of the manuals, call FETO, Pasadena, for further instructions.

MTR - If one of the test cases being tested by the GCR fails, a message will be printed out on the SPO and the program will halt. The message will give the test case number, example - *04621.0, the type of failure and the number of times the test failed. The type of failure can be either a "C", which signifies that the control words produced by the store for test operator in the test case did not compare with the known control words, or an I-XX, which signifies an interrupt failure, or both. If the type of failure printout is I-00, it indicates that an interrupt should have occurred but did not occur. If I equals any other number, it indicates that this interrupt should not have occurred or it is the wrong interrupt. The second line will contain ET-00XX. If XX is other than 31, the number indicates how many times the test case failed out of 25 tests of this test case. In this case, the six erroneous control words will also be typed out. Their order, starting with the first word, will be INCW, IRCW, ICW, ILCW, B reg. and A reg. and any memory output words if the test case called for them.

After the printout, there are four alternates which may be taken: 1) repeat the test case 25 more times, 2) skip this test case, 3) single pulse this test case, or 4) continuously loop on this test case for scoping.

Repeat - If it is desired to repeat the test case, just push the single pulse button. This will perform the testing of this case 25 more times and the error tally will be printed out on the SPO.

Skip - If it is desired to skip this test case, turn on A01F and push the single pulse button.

Single Pulse - If it is desired to single pulse the test case, turn on A02F and push the single pulse button. The processor will again halt with a 2411 and the P register will contain CHP, LTS, LCD, NOF. Place the single pulse switch to SINGLE and single pulse until the T register contains a 5111. Single pulse this operator until TROF goes off and then single pulse once more. The registers now contain all the information necessary for this test case and the operator being tested will be in T. At this time, check the flow of this operator at the appropriate J count and determine what is supposed to happen. Push the single pulse button and check if the expected results did occur. If a memory read was initiated, push the button until the required register is loaded and then check the results. The error should be easily spotted by this operation. After the trouble has been fixed, restart the program from the beginning by loading the card deck in the reader and reading it into memory again. The deck will automatically rewind tape.

Scope Loop - If it is desired to loop on this test case while checking with a scope, turn on A02F, turn off the "Stop on Operator" switch and push the single pulse button. This test case will be continually tested although no comparison of control words takes place. This is useful for tracking down an intermittent trouble or slow gate. (See Intermittent Troubles.)

Intermittent Troubles - If the error tally is not 31, indicating a solid failure, the problem is intermittent and possibly cannot be found by single pulsing. To cover this possibility, the following procedure is given.

Figure 3 of the enclosure gives the location of the error tank of GCR. The six control words are the words which will be printed out on the SPO. These are the control words produced by the "Store for Test" operator of the test case and one or more did not compare with the expected results. The expected results can be found in the following memory cells:

00510 - A reg.

00511 - B reg.

00512 - ILCW

00513 - ICW

00514 - INCW

00515 - INCW

Check the contents of these cells with the printout or error tank to determine where the comparison failed.

If there are any questions or if you are not able to find the trouble with these instructions, call FETO, Pasadena. Complete instructions and necessary manuals will be forwarded to you as soon as possible. Although this routine is for testing the processor only, certain portions of I/O operation, Central Control and memory are used in process of running the routine. Care should be taken that the failure is not misleading. Failure in one of the units could be causing the test case to fail rather than a processor failure. Troubles have been found in Central Control, I/O and memory by the use of this routine.

Figure 1

INPUT BUFFER STACK
(03012 thru 03771)

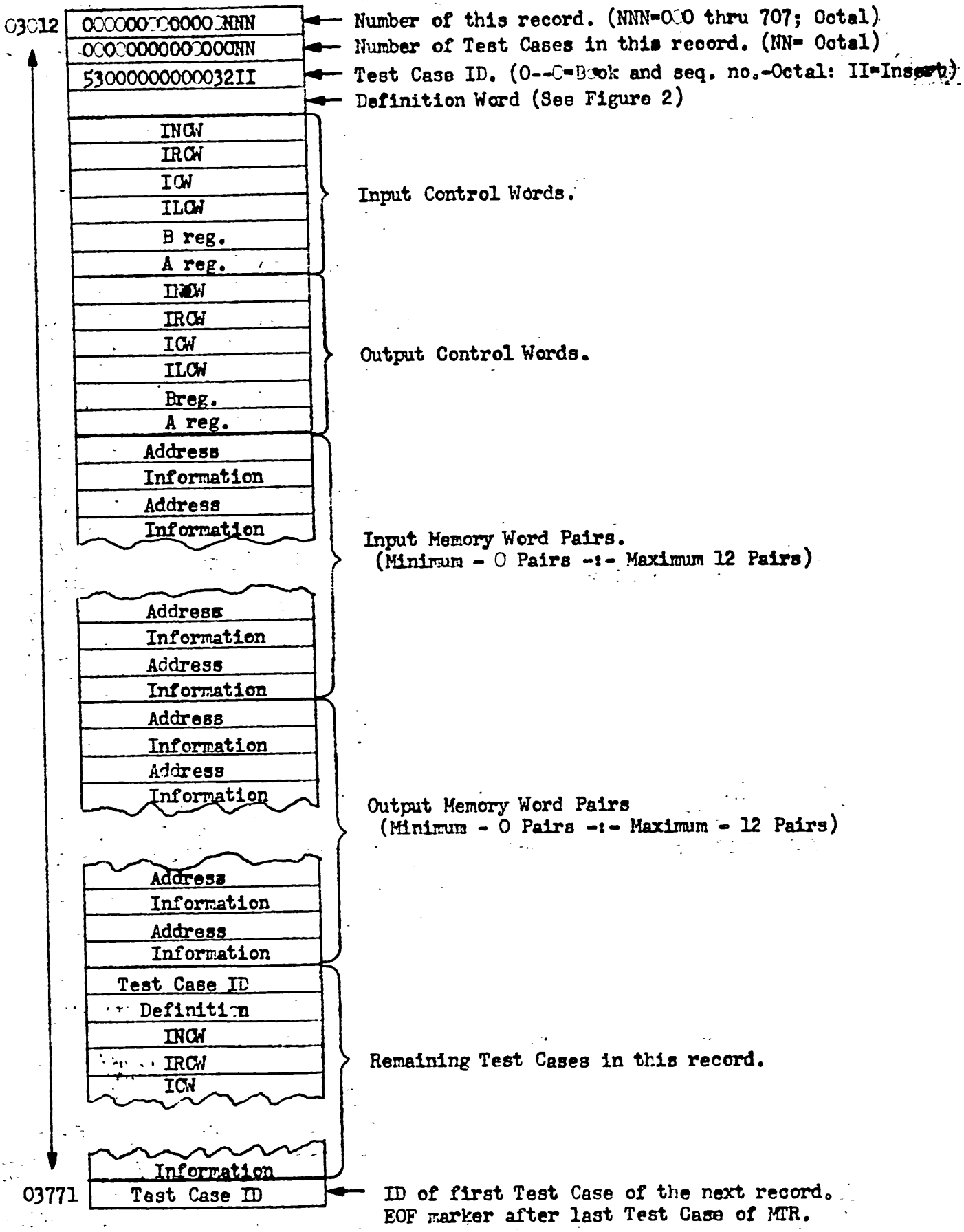
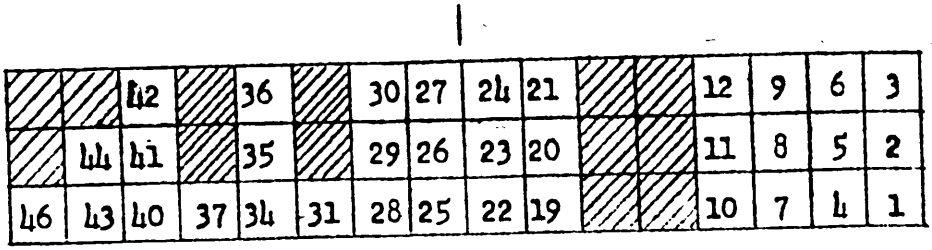


Figure 2

DEFINITION WORD



▨ ← Not Used. (Will be 0)

Bits 1 thru 12 - T reg. setting of operator being tested. (First operator if test uses more than one operator)

Bits 19 thru 24- Equal 00 (octal) - Check that no interrupt occurs. (None should occur.)
Equal 01 (octal) - Do not check for interrupt.
Not Equal 00 or 01 (octal) - Interrupt should occur. Check for interrupt specified at this address.

Bits 25 thru 27- Highest memory module required for this test case. (octal)

Bits 28 thru 31- Number of Output Word Pairs. (octal)

Bits 34 thru 37- Number of Input Word Pairs. (octal)

Bits 40 thru 42- Number of memory module which must be absent for this test case to be tried.

Bits 43 and 44 - Equal 0 - Compare "After" Control Words.
Equal 1 - Do not compare "After" Control Words.
Equal 2 - Force interrupt for test case.

Bit 46 - - - - - Equal 0 - This test case is for P1 only.
Equal 1 - This test case is for P1 and P2.

Figure 3

ERROR TANK
(00411 thru 00436)

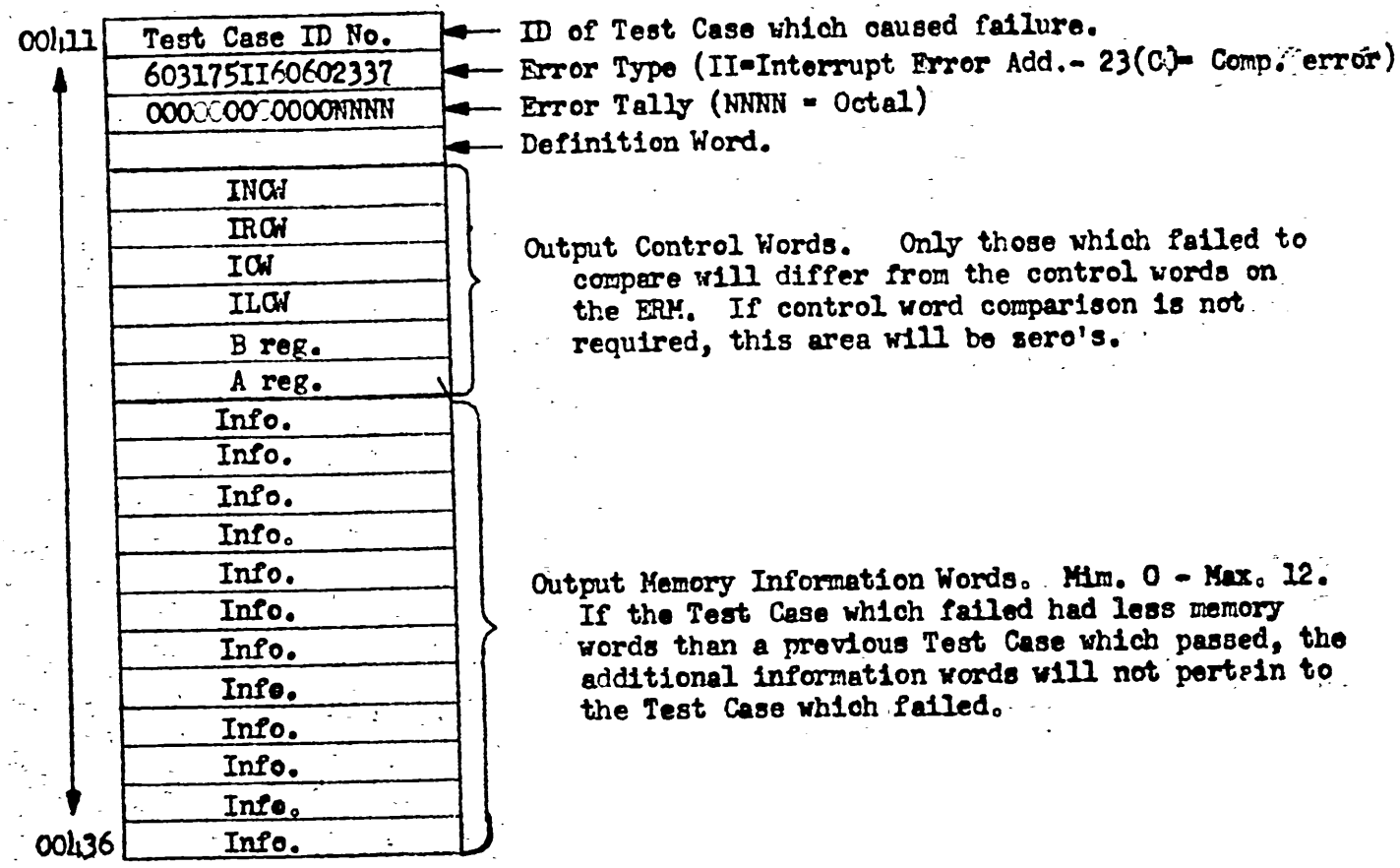


Figure 4

INITIATE CONTROL WORD
(SFT only)

48	45	42	39	36	33	30	27	24	21	18	15	12	9	6	3
47	44	41	38	35	32	29	26	23	20	17	14	11	8	5	2
46	43	40	37	34	31	28	25	22	19	16	13	10	7	4	1

Bits 1 thru 15 - S reg. , pointing to ILCW.

Bit 16 - - - - - CWMF.

Bits 17 thru 20- J reg, setting. Transfers to TM 1 thru 4.

Bit 21 - - - - - NCSF. Transfers to TM5F.

Bit 22 - - - - - CCCF. Transfers to TM6F.

Bits 23 thru 28- Z reg.

Bits 29 thru 34- Y reg.

Bits 35 thru 43- Q reg.

Bit 44 - - - - - MWOF. Transfers to TM7F.

Bit 46 - - - - - MROF. Transfers to TM8F.

Bit 45 = 0
Bit 47 = 1 ID Bits.
Bit 48 = 1