Burroughs

B 5290

DISPLAY & DISTRIBUTION

TECHNICAL MANUAL

B 5000 DATA PROCESSING SYSTEM

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B 5290.51

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1. Inspect and replace Plenum Filters, if necessary.
2. Inspect and clean fan screens, if necessary.

1.4 QUARTERLY -- There are no quarterly checks.

1.5 SEMI-ANNUALLY

EXHAUST FANS

Lubricate Rotron Muffin fans with Andersol L-326 using special oil injector.

Oil Injector.....Pt. No. 11838588
Oil.....Pt. No. 11838596

Procedure

The exhaust fans are lubricated by inserting the Oil Injector needle through a self-sealing rubber cap located in the center of the motor hub.

NOTE: On some units a Gold Seal label is mounted over the rubber plug; this series of fans is called the Gold Seal series. An earlier series of fans (034 series) have a clear decal which covers the plug.

1. Fan Grill, remove and clean as necessary.
2. Remove air from Oil Injector by holding the needle up and pressing on the plunger.
3. Place Oil Injector needle at the center of the circle marked on the Gold label (on the 034 series place needle approximately 1/8" from the edge of the rubber cap).
4. Position the needle at an angle of approximately 45 degrees to the surface of the label and point it toward the center of the rubber cap.
5. Pierce the label and the concealed self-sealing rubber cap located under the label.
6. Insert the needle approximately 1/4".
7. Depress the plunger of the Oil Injector to allow approximately 1/16" of oil to escape. Rotating the fan will relieve air pressure and allow oil to flow into the oil chamber.
8. Wipe off excess oil as needle is removed and remount fan.

SECTION 2

TROUBLESHOOTING

2.1 CC MAINTENANCE PANEL

INTRODUCTION

A line drawing of the B 5290 CC Maintenance Panel is shown in Figure 2.1-1. The Indicator switches, Switches and Indicators on this panel are described in this subsection.

INDICATOR SWITCH - LIGHTS (CROSSPOINT CONTROL)

MnMCYF (DA-56.01.08.0 thru 56.01.15.0)

MnMCYF Flip-flop being set indicates that the associated (M0 thru M7) Core Memory Module is in a T0 thru T5 memory access cycle. Memory Cycle Flip-flop being reset indicates that the associated Core Memory Module is at "T ZERO" or IDLE time.

MnPAXF (DA-56.01.08.0 thru 56.01.15.0)

MnPAXF Flip-flop being set indicates that communication, address and control lines between Processor A and the selected Core Memory Module (M0 thru M7) have been established.

MnPBXF (DA-56.01.08.0 thru 56.01.15.0)

MnPBXF Flip-flop being set indicates that communication, address and control lines between Processor B and the selected Core Memory Module (M0 thru M7) have been established.

MnI1XF thru MnI4XF (DA-56.01.08.0 thru 56.01.15.0)

One of these four flip-flops being set indicates that communication, address and control lines between the indicated I/O and the selected Core Memory Module (M0 thru M7) have been established.

INDICATOR SWITCH - LIGHTS (I/O CONTROL)

AD1F thru AD4F (DA-56.96.20.0)

These flip-flops are used to indicate an I/O-1 thru I/O-4 busy status, respectively. AD1F thru AD4F may be set by an INITIATE I/O operator or by the initiation of a LOAD operation. The I/O Finished Interrupts, CCI08F thru CCI11F, are gated by AD1F thru AD4F, respectively.

✓ Changes or addition since last issue

CL1F (DA-56.96.20.0)

CL1F serves as a single pulse control when the CLOCK MODE switch is in the SINGLE pulse position. CL1F is also set by depressing the START CLOCK switch (CC Display Panel), or one of the LOAD switches. The first clock generated pulse always resets CL1F.

CL2F (DA-56.96.20.0)

CL2F being set normally enables the clock B.O. and line driver packages. If the CLOCK MODE switch is in the DOUBLE-PULSE position, CL2F is set by the first pulse and reset with the second pulse.

INDICATOR SWITCH - LIGHTS (INTERRUPT)

IA1F thru IA6F (DA-56.01.06.0)

These flip-flops are normally set as a result of evaluating interrupts on a priority basis. This register contains the address of the first program word which has been assigned to handle this interrupt condition.

IASF (DA-56.01.06.0)

IASF when set indicates that the contents of the Interrupt Address Register are to be shifted to rC for programed control of this interrupt.

CCI03F thru CCI16F

These flip-flops are used to indicate the following interrupt conditions: (Refer to Test and Field Document C1192534, Index Number 4.07.0 for System Interrupts Address chart.)

✓TABLE 2.1-1 INDICATORS

INDICATOR SWITCH LITE	CONDITION	DA NUMBER
CCI03F	TIME INTERVAL INTERRUPT	DA 56.01.07.0
CCI04F	I/O BUSY INTERRUPT	DA 56.96.20.0
CCI05F	KEYBOARD REQUEST INTERRUPT	DA 56.96.22.0
CCI06F	PRINTER #1 FINISHED INTERRUPT	DA 56.96.22.0
CCI07F	PRINTER #2 FINISHED INTERRUPT	DA 56.96.22.0
CCI08F	I/O-1 FINISHED INTERRUPT	DA 56.96.21.0
CCI09F	I/O-2 FINISHED INTERRUPT	DA 56.96.21.0
CCI10F	I/O-3 FINISHED INTERRUPT	DA 56.96.21.0
CCI11F	I/O-4 FINISHED INTERRUPT	DA 56.96.21.0
CCI12F	PROCESSOR #2 BUSY INTERRUPT	DA 56.96.20.0
CCI13F	INQUIRY REQUEST	DA 56.96.22.0
CCI14F	SPECIAL INTERRUPT - 1	DA 56.96.22.0
CCI15F	DF READ CHECK FINISHED 1	DA 56.96.22.0
CCI16F	DF READ CHECK FINISHED 2	DA 56.96.22.0

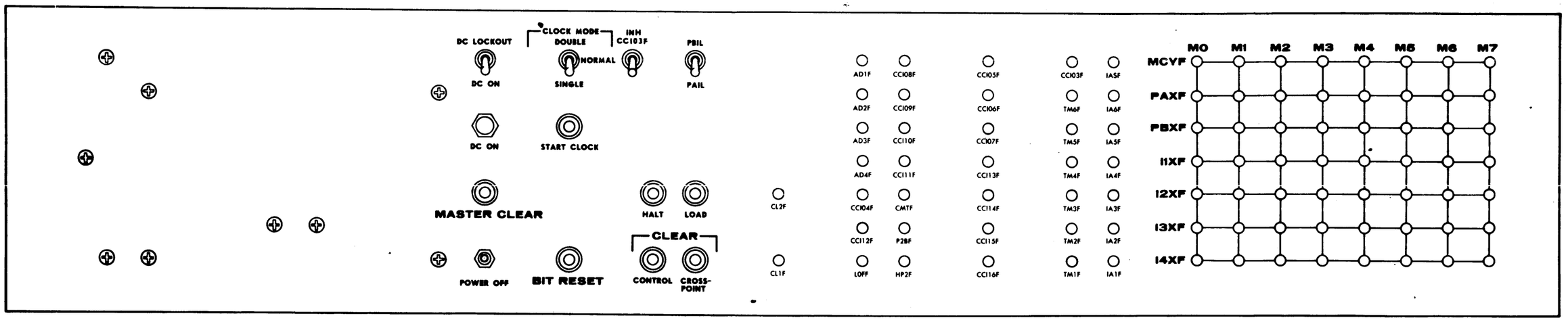


FIGURE 2.1-1 CC DISPLAY PANEL

INDICATOR SWITCH - LIGHTS (MISC. CONTROL)

CMTF (DA-56.96.21.0)

The I/O Commence Timing Flip-flop may normally be set by Processor 1 or a LOAD function in order to initiate an I/O operation.

HP2F (DA-56.96.21.0)

HP2F when set serves as one of the logical gates to halt Processor 2 at SECL time. HP2F may also be set by the execution of the HALT P2 operator.

P2BF (DA-56.96.21.0)

P2BF is normally set by Processor 1 during a LOAD operation and indicates that Processor 2 is not idle.

LOFF (DA-56.96.21.0)

The LOFF Flip-flop is used as a logical gate to enable a card or drum load operation.

TM1F thru TM6F (DA-56.01.07.0)

TM1F thru TM6F comprise a 6 bit timer register which is counted by a CLOCKED 60 cycle timing pulse. The 60 cycle is used to actuate the TM0Y synchronizer which, in conjunction with the System Clock, advances the counter. The outputs of the Timer Register are made available to Processor 1 to enable the Master Control Program to check the contents of this register under control of the READ TIMER operator. A Time Interval Interrupt is set when the Timer Register passes through its maximum count and carries to zero. The setting of the Time Interval Interrupt may be inhibited during maintenance operations by the INHIBIT CCI03F TEST switch.

SWITCHES - PUSH BUTTON

Bit Reset (DA-56.01.04.0)

If the Bit Reset PB switch is held depressed, depression of any of the indicator switch-lights on the CC Maintenance Panel resets the corresponding flip-flop and indicator.

Control Clear (DA-56.01.04.0)

PB switch is used to clear the following flip-flops.

1. AD1F thru AD4F
2. CCI03F thru CCI16F
3. TM1F thru TM6F
4. IA1F thru IA6F
5. IASF
6. P2BF
7. HP2F

Crosspoint Clear (DA-56.01.04.0)

PB switch is used to clear the 56 Core Memory corsspoint flip-flops and indicators which control all memory exchange switching necessary to interconnect any requesting unit with any High Speed Memory Module installed within the system.

Halt (DA-56.01.05.0)

PB switch performs the same function as the HALT switch-indicator located on the operator console. It is used to halt both Processor 1 and Processor 2 after the execution of the current Processor syllables. The Processors remain halted until a subsequent load operation is initiated. There is no provision for continuing operations from the console at the point in the program where the HALT occurred. However, Processor operations may be continued through the use of the SINGLE PULSE push button.

Load (DA-56.01.05.0)

PB switch performs the same function as the LOAD switch located on the Operators Console. It is used to clear the system and initiate a LOAD operation from a Card Reader or the Drum Memory Unit. It initiates a LOAD from Card Reader or Magnetic Drum as controlled and indicated by the CARD LOAD SELECT switch on the Operators Console. If either Processor is busy, depressing the LOAD switch has no effect.

Master Clear (DA-56.01.04.0)

PB switch is used to actuate the master clear relay which causes all system logical controls and indicators to be cleared.

Power Off (DA-56.01.05.0)

The PB switch performs the same function as the POWER OFF switch located on the Operators Console and Power Supply meter panel. It is used to initiate a POWER OFF

cycle which results in power being disconnected from all units of the system including fans; however, the voltage to the convenience outlets and the -24V to D & D (power sensing) and SPO are controlled by the main wall circuit breaker for the B 5000 Power Supply.

Start Clock (DA-56.01.05.0)

The PB switch initiates a clock output which is defined by the DOUBLE-NORMAL-SINGLE switch. It is paralleled by START clock switches located in each Core Memory Unit, and by the Processor Single pulse push button.

SWITCHES - TOGGLE

Double-Normal-Single (Clock Mode) (DA-56.01.05.0)

The toggle switch allows the selection of the following clock operations which are initiated by the START CLOCK switch:

1. Continuous one megacycle clock pulses.
2. A double pulse clock output.
3. A single pulse clock output.

DC Lockout (DA-56.01.05.0)

The toggle switch enables 40 ms slow pull relay K19. This switch also provides the following:

1. An inhibit Master Clock ground level ($\overline{\text{PGDL}}$) to Centrl Control.
2. Core Memory ground level to cycle down Core Memory power.

K19 being energized enables the following:

1. "INHIBIT GROUND" to the base of the +20V Control switch in the B 5370 Power Supply Unit.
2. Inhibits POWER FAIL sense.
3. Establishes Core Memory Power Down delay.

Processor 1 Designation (DA-56.01.05.0)

The toggle switch designates either PA or PB as Processor 1 (Control Processor).

Inhibit CCI03F

This switch is used to inhibit the Real Time Interrupt Flip-flop to enable the Field Engineer to step through Normal State operators.

INDICATORS

DC On (DA-56.01.05.0)

Indicates that the Power Control Relay K17 is energized, power is cycled up, and DC voltages are available to the B 5000 system. The DC ON light is controlled by both the -12V Supply and the -24V Supply.

CC Maintenance Panel

Figure 2.1-2 is a schematic of the CC Maintenance Panel.

Refer to Figure 4.1-1, Assembly and Disassembly for the physical location of components.

CONSOLE

CABLE 252 CABLE 14

AB J3 DD K6 AH R1

CABLE 42

AH P1 EA B0 A2 SNHD/ WPID/ HIND/ PALOSD/ PANOSD/ PBLOSD PBNOSD LODL LOCL HIBL/ SCLL/ LOBL/ NOT NORMAL SPCL/ PAIL PBIL NITL/

CONTROL FLIP-FLOPS

CROSSPOINTS FLIP-FLOPS

CABLES 37 — 41

AH J1 EA A0 A2 AH M1 EA A0 N2 AH K1 AA A0 A2 AH L1 AA A0 N2 AH N1 AA B0 A2

56.96.20.0
AD1F ⇒ AD4F
CL1F
CL2F

56.01.06.0
IA1F ⇒ IA6F
IA5F

56.01.07.0
TM1F ⇒ TM6F
CC103F

56.96.20.0
56.96.21.0
56.96.22.0
CCI04F ⇒ CCI16F
CM1F
HP2F
LOFF
P2BF

56.01.08.0 THRU 56.01.15.0

CC

DISPLAY PANEL

56.01.05.0
HALT
.047μf
START CLOCK
LOAD
B8 680Ω D9
C8 12KΩ C9
C6 24Ω C7
D0 12KΩ D1
D2 5Ω D3
D8 12KΩ D7
D4 5Ω D5
-12V
LOBL-C/
DOUBLE
NORMAL
SINGLE
-4.5V
E1 47Ω E0
SELECT P1
PB1L
PA1L
INCANDESCENT LIGHTS
-24B
POFL-0/
POFL-1/
POFL-2
PONL-2
POWER ON-OFF BUTTONS
POWER OFF
PONL-1
-24A
E3 620Ω E2
.004μf E4 E5
.015μf E9 E8
E6 100Ω E7
INHIBIT CCI103F

CENTRAL CONTROL

CABLE 42

AH P1 EA B0 A2 LORS

A0
B6 5.11Ω
B7 B9 0.5μf
-100VM-C
B2 B3 B1 3.3KΩ B0
A1
MERCURY RELAY
ABN8
-4.5V
56.01.04.0
MASTER CLEAR
02 01
B4 1Ω B5
A8 51KΩ A9 -12V
+100V
56.01.05.0
DC
NORMAL
LOCKOUT

SWITCH LIGHT DRIVER ASSEMBLY
7 4 -120V
2 9
8 6
C1 750Ω C0
56.01.04.0
CLEAR CROSSPOINTS
C3 750Ω C2 CLEAR CONTROL
C5 2KΩ C4 BIT RESET
A2 20K A3
F5 5.5Ω F4
F0 0.2μf F1
NEON DRIVERS

AH P1 EA B0 A2 CLEAR SENSE

PRE-STOP

60 CYCLE
F2 F8
F3 F9
F7 500Ω F6

D & D
POWER SENSE PANEL

CABLE 64
AH S1 AK A2 A2
PGDL/
MASTER CLEAR TO OTHER UNITS
DC ON
-24B
-24A
-120V
+100V
-12V
-4.5V
-100VM-C
-100V
+20V
-1.2V
LOCKOUT
POFL-0/
POFL-3
PONL-2
POFL-2
PONL-1

FIGURE 2.1-2
CC MAINTENANCE PANEL
SCHEMATIC

2.2 PROCESSOR MAINTENANCE PANEL

GENERAL

This subsection describes the Processor Maintenance Panel Indicator Switch Lights and TEST switches. A line drawing of the B 5290 Processor Maintenance Panel is shown in Figure 2.2-1.

Refer to Test and Field Document C11891298, Index Number 4.02.0 for a description of the various Processor registers and their functions.

LOGICAL CONTROL INDICATOR SWITCH LIGHTS (Q REGISTER)

Q01F thru Q09F & Q12F

These flip-flops are used as logical controls for the B 5000 word and character mode operators. Q12F also serves as the True/False Flip-flop (TFFF) and Mark Stack Flip-flop (MSFF).

MWOF

Memory Write Obtained Flip-flop is used to indicate that the information to be stored and its address are in the Memory Information and Memory Address registers respectively.

NSCF

Normal/Control State Flip-flop is used to indicate whether a Processor is operating in the Normal or Control state.

SALF

Sub Level Flip-flop is used to indicate a SUB routine program level of operation.

CWMF

Character/Word Mode Flip-flop is used to indicate character or Word Mode program operation.

MISCELLANEOUS LOGICAL CONTROL INDICATOR SWITCH LIGHTS

MRAF

Memory Read Access Flip-flop is used to indicate that the program word requested is in the Memory Information Register.

MROF

Memory Read Obtained Flip-flop is used to indicate that the information requested is in the Memory Information Register.

HLTF

The Halt Flip-flop is used as one of the logical gates to enable the STOP CLOCK driver UIMCD1. This flip-flop may be set by any one of the following:

1. A Single Pulse Memory Write (refer to US25X).
2. At SECL time with the STOP EXIT switch US16X in the TEST position.
3. At SECL time by the HALT push button.

EIHF

E Inhibit Flip-flop is used to prevent selecting a second Memory Module, while an access to one is in progress. This condition occurs when the address register in use (the one selected by the setting of E) is changed during an active memory cycle.

Example: S=07777 at start of access and is counted up one before E is cleared. Thus two Memory Modules would be accessed for one E register setting.

EIHF is used to inhibit setting of the CROSSPOINT flip-flops during the time MWOF through MROF of a Memory cycle.

AROF

"A" Register Occupied Flip-flop.

BROF

"B" Register Occupied Flip-flop.

PROF

"P" Register Occupied Flip-flop.

TROF

"T" Register Occupied Flip-flop.

TOGGLE SWITCHES

Table 2.2-1 lists the Processor Maintenance Panel toggle switches (DA-66.01.25.0 thru 66.01.38.0).

TABLE 2.2-1 TOGGLE SWITCHES

SWITCH NUMBER	ACTION
US01X	INHIBIT COUNT REPEAT FIELD (T) (BY -1, -4, -8)
US02X	INHIBIT COUNT G & H
US03X	INHIBIT COUNT M
US04X	INHIBIT COUNT K, V & N
US05X	INHIBIT COUNT S
US06X	INHIBIT COUNT C
US07X	INHIBIT COUNT L
US08X	INHIBIT RESET AROF
US09X	INHIBIT RESET BROF
US10X	INHIBIT T <-P (L)
US11X	INHIBIT STORE
US12X	INHIBIT IN/OUT
US13X	INHIBIT INTERRUPT
US14X	STOP INSTRUCTION (OPERATOR)
US15X	"STOP CLOCK" - DRIVER
US16X	STOP ON SECL
US17X	STOP ON INTERRUPT (PROCESSOR TYPE)
US18X	STOP WHEN NORMALIZED
US19X	STOP ON J COUNT
US20X - US23X	J CODE SWITCHES
US24X	SINGLE PULSE
US25X	SINGLE PULSE MEMORY WRITE
US26X	INHIBIT RESET "A" MANTISSA
US27X	INHIBIT B02ZD LEVEL
US28X	LOCK UP ON J (US20X - US23X)
US29X	MEMORY LOAD

US01X - Inhibit Count Repeat Field

In TEST position, decrementing of the REPEAT COUNT FIELD in T is inhibited. The following actions will not occur:

1. T[12 thru 7]-1
2. T[12 thru 7]-4
3. T[12 thru 7]-8

US02X - Inhibit Count G and H

This switch in TEST position inhibits incrementing or decrementing of the G and H registers.

US03X - Inhibit Count M

In TEST position this switch inhibits the incrementing or decrementing of the M register.

US04X - Inhibit Count K, V and N

This switch in TEST position inhibits the incrementing or decrementing of the K, V and N registers; however, these registers may be set or reset.

US05X - Inhibit Count S

This switch in TEST position inhibits incrementing or decrementing of the S register.

US06X - Inhibit Count C

This switch in TEST position inhibits incrementing or decrementing of the C register. This switch in TEST position prevents the fetch of a new program word from memory and the Processor will cycle on the word in P.

US07X - Inhibit Count L

In TEST position this switch inhibits incrementing or decrementing of the L register. This switch locks the Processor on a single operator syllable unless an interrupt is encountered.

US08X - Inhibit Reset of AROF

This switch in TEST position inhibits the -K- inputs to AROF.

US09X - Inhibit Reset of BROF

This switch in TEST position inhibits the -K- inputs to BROF.

US10X - INHIBIT T <— P[L]

This switch in TEST position inhibits the fetch transfer of the L syllable from P to T but will not directly inhibit the character transfer from P to T employed within the CALL REPEAT FIELD operator.

US11X - Inhibit Store

When this switch is in TEST, writing of information into memory is inhibited. The memory cycle is simulated as follows:

1. E will set normally.
2. $\overline{\text{UMAIS1}}$ will come true for all writes (E08F) which will prevent the memory access.
3. DMTOX will be simulated (E08F • US11X).

All memory reads will occur normally.

US12X - Inhibit In/Out

This switch in TEST position forces Initiate Input/Output operators to become NO OPS.

US13X - Inhibit Interrupt

In TEST position inhibits the set inputs to the UInnFF's.

US14X - Stop Operator

This switch in TEST position provides a level which in conjunction with the Conditional Halt Operator Level (CHPL-2411) and JOOL enables the STOP CLOCK driver UIMCD1. Registers may be set or cleared manually during this interval and Processor operation will resume when the clock is restarted.

When this switch is in NORMAL position and a CONDITIONAL HALT OPERATOR is encountered, the Processor executes a NO OP and proceeds with the next operator in sequence.

US15X - Stop Clock

In TEST position this switch enables the STOP CLOCK driver UIMCD1 which inhibits the clock driver in Central Control.

US16X - Stop Exit

In TEST position this switch stops the clock with the clock pulse gated by SECL by enabling the STOP CLOCK DRIVER UIMCD1.

US17X - Stop On Interrupt (Processor Type)

This switch in TEST position enables the STOP CLOCK driver UIMCD1 when any one of the UInnFF's is set.

US18X - Stop Normalized

This switch in TEST position enables the STOP CLOCK driver UIMCD1 when both operands are aligned.

US19X - Stop on J Count

This switch is used in conjunction with US20X thru US23X during TEST, and enables the STOP CLOCK driver UIMCD1 when the J count reaches a predetermined value. Should inhibit the first clock pulse in the assigned J count as designated by the J CODE switches (UP).

US20X thru US23X - "J" CODE AND LOCK UP

The J code switches are used to encode the BCD value of the J value to be used in conjunction with "STOP ON J COUNT" (US19X) or "LOCK UP ON J" (US28X).

US24X - SINGLE PULSE

When pressed, this switch causes a start pulse to be sent to Central Control. When the STOP clock switch (US15X) is in TEST position a single clock pulse results if a FETCH or a MEMORY ACCESS request is not indicated; otherwise, the required number of pulses will be generated to complete the fetch or memory request.

US25X - Single Pulse Memory Write

When pressed, this switch causes the contents of the B register to be written into memory under control of the S register. The S register is incremented by one after each store.

To use this switch the MEMORY LOAD switch (US29X) must be in TEST position and TROF must be off.

The following logic is used to cause a single memory write:

1. HLTF EEZL•$\overline{\text{TROF}}$•US25X•US29X
2. [E=11] HLTF•EEZL•$\overline{\text{TROF}}$•$\overline{\text{US25X}}$•US29X
3. [S+1] US29X•MWOF
4. ($\overline{\text{HLTF}}$) US29X•E08F

US26X - Inhibit Reset of "A" Mantissa

This switch in TEST position inhibits the clearing of the A mantissa.

US27X - Inhibit 42 Bit Add

This switch in TEST position inhibits the B02ZD level at the outputs of the adder circuit which prevents the sum of the addition from being fed into the "B" register.

US28X - LOCK UP ON J

This switch when used in conjunction with US20X thru US23X during a TEST operation inhibits further alteration of the J count when a predetermined value of J has occurred.

US29X - Memory Load

A memory load from the B register occurs when this switch is in TEST and the single pulse memory switch (US25X) is pressed.

SWITCHES - PUSH BUTTON

The register clear PB's do not interrupt the system clock or unit BO and line clock drivers. Therefore, these clear PB's should be used only when the clock mode switch is in either the single or double pulse position, or the HALT condition exists. (STOP CLOCK driver UIMCD1 is enabled).

CAUTION

It was not intended that the various clear buttons on the Processor Maintenance Panel be used during NORMAL clock mode operation of the system. Indiscriminate depression of the UNIT CLEAR button and the various register clear buttons should be avoided.

Register Clear PB's

Each Processor Register has an associated CLEAR push button which is located on the same plane and on the extreme right of the display panel.

Unit Clear

The Processor Unit clear push button causes all Processor logical toggles to be cleared.

CAUTION

If this button is depressed while the clock is running and an interrupt bit is set, memory can be flushed with zeros. The same undesirable result occurs if an interrupt bit is set after the UNIT CLEAR button is depressed.

Bit Reset

If the Bit Reset PB switch is held depressed, depressing any one of the switch indicators on the Processor Maintenance Panel clears the corresponding flip-flop and indicator.

DP MAINTENANCE PANEL SCHEMATIC

Figure 2.2-2 is a schematic of the DP Maintenance Panel.

Refer to Figure 4.2-1, Assembly and Disassembly, for the physical location of components.

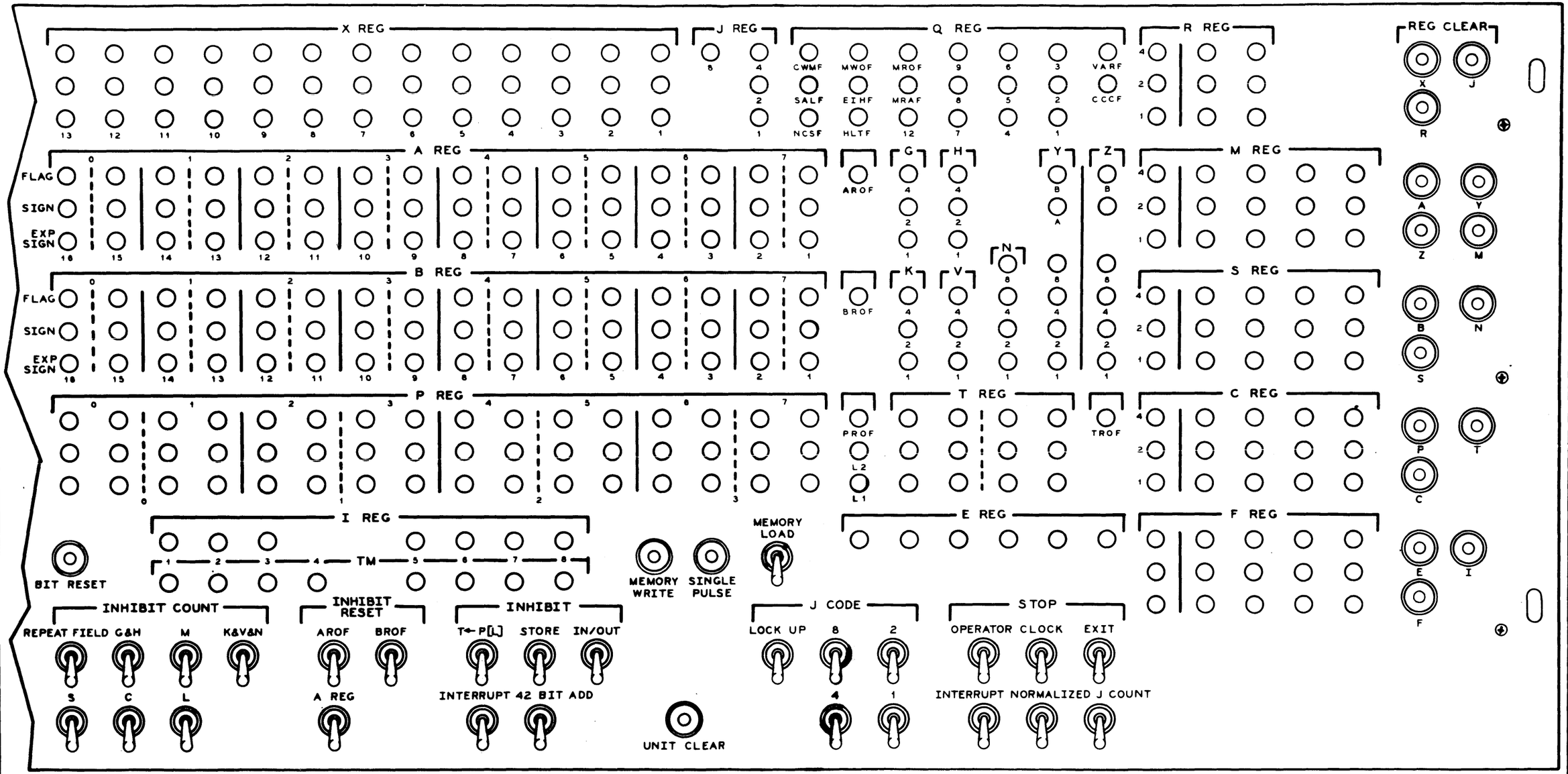


FIGURE 2.2-1
PROCESSOR DISPLAY PANEL

Revised Febr

PROCESSOR

"A" REG | "B" REG | "C" REG | "E" REG | "F" REG | "I" REG | "J" REG | "M" REG | "N" REG

FLIP-FLOPS

CABLES 62 & 63

CABLES 45 ⇒ 61

+100V

SWITCH LIGHT DRIVERS

48 | 48 | 15 | 6 | 15 | 7 | 4 | 15 | 4

-120V

A7 | B5 | C5 | C9 | D3 | D1 | A3 | C7 | B3 | B7

750Ω | 750Ω | 750Ω | 750Ω | 750Ω | 750Ω | 750Ω | 2KΩ | 750Ω | 750Ω

CLEAR "A" A6 | CLEAR "B" B4 | CLEAR "C" C4 | CLEAR "E" C8 | CLEAR "F" D2 | CLEAR "I" D0 | CLEAR "J" A2 | C6 CLEAR "M" B2 | CLEAR "N" B6

-100V

MASTER CLEAR

UNIT CLEAR

BIT RESET

E4 20K E5

TO NEON DRIVERS

+20V

-1.2V

GND

K & V & N

M

G & H

REPEAT FIELD

MEMORY WRITE

D6 47Ω D7

SINGLE PULSE

E1 27Ω E0

0.1μf E2 E3

D8 12K D9

IN/OUT

STORE

T ← P (L)

BROF

AROF

L

C

S

"J" CODE

STOP "J" COUNT

STOP NORMALIZED

STOP INTERRUPT

STOP EXIT

STOP CLOCK

OPERATOR

INHIBIT INTERRUPT

MEMORY LOAD

LOCK UP

42 BIT ADD

"A" REG

"J" CODE 8

"J" CODE 4

"J" CODE 2

CABLES 45 ⇒ 61

US24X/ US25X US25X/ US01X/ US02X/ US03X/ US04X/

US05X/ US06X/ US07X/ US08X/ US09X/ US10X/ US11X/ US12X/ US12X

US13X/ US14X US15X US16X US17X US18X US19X US20X/ US20X

US21X/ US21X US22X/ US22X US23X/ US23X US26X/ US27X/ US28X US29X/ US29X

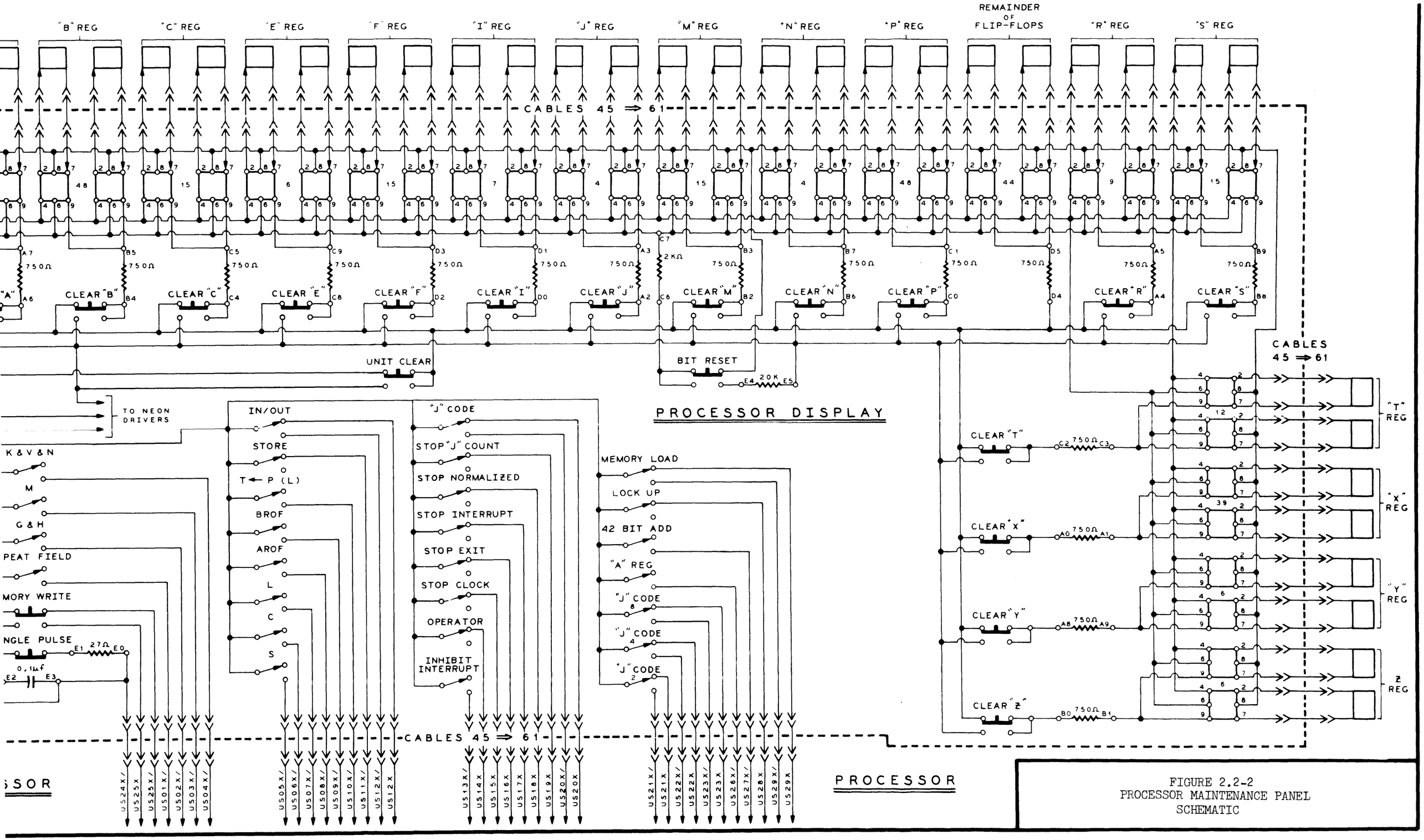
POWER SENSE PANEL (D & D)

PROCESSOR

PROCESSOR DISPLAY

PROC

PROCESSOR



PROCESSOR

FIGURE 2.2-2
PROCESSOR MAINTENANCE PANEL
SCHEMATIC

2.3 I/O MAINTENANCE PANEL

INTRODUCTION

A line drawing of the B 5290 I/O Maintenance Panel is shown in Figure 2.3-1. The indicator switches and test switches are described below.

INDICATOR SWITCH-LIGHTS

Buffers

The following I/O Buffers are used for the transfer of information between peripheral units and core memory.

1. IB

   The Input Buffer is used to receive information from the peripheral units. During Magnetic Tape operations the contents of IR are shifted to IB which consists of IB1F ⇒ IBPF.

2. IR

   The Tape Information Read Buffer is used to receive information from the Tape Transport units. It consists of IR1F ⇒ IRPF.

3. OB

   The Output Buffer consists of six flip-flops and a parity generator.

4. WB

   The Tape Write Buffer consists of 7 flip-flops and is used to reflect the state of the Output character to the TTU.

Registers W & D

Refer to B 5000 I/O Descriptor Card for rW and rD I/O Descriptor functions.

Refer to Table 2.3-1 for Result Descriptor Error and Control Field.

TABLE 2.3-1 RESULT DESCRIPTOR ERROR AND CONTROL FIELD

I/O DESCRIPTORS	STANDARD ERROR FIELD				SPECIAL ERROR FIELD		
	16	17	18 NOT READY	22 MEMORY ADDRESS	19	20	21
PRINTER	X	X	X	X	PARITY-MEM TO I/O	PRINT CHECK PREVIOUT LINE	END-OF-PAGE
DRUM WRITE	X	X	X	X	PARITY-MEM TO I/O		LOCKOUT
DRUM READ	X	X	X	X	PARITY-DRUM TO I/O		
CARD INPUT	X	X	X	X	INVALID CHARACTER	READ CHECK	END-OF-FILE
CARD OUTPUT	X	X	X	X	PARITY-MEM TO I/O	PUNCH ERROR	
MAG. TAPE READ	X	X	X	X		PARITY-TAPE TO I/O	END-OF-FILE
MAG. TAPE WRITE	X	X	X	X	PARITY-MEM TO I/O	READ-BACK PARITY	END-OF-TAPE
				*SEE D20		*WRITE LOCKOUT (D20 & D22)	
SUPV. PRINTER	X	X	X	X	PARITY-MEM TO I/O		
KEYBOARD	X	X	X	X	PARITY-MEM TO I/O	PARITY OR OPERATOR ERROR	
PAPER TAPE READ	X	X	X	X	PARITY IN READER	BEGINNING OF TAPE	END-OF-TAPE
PAPER TAPE WRITE	X	X	X	X	PARITY-MEM TO I/O		LOW TAPE

MAGNETIC TAPE FLIP-FLOPS

BKWF

The Backward Drive Flip-flop controls Backward Tape Drive.

FWDF

The Forward Drive Flip-flop controls Forward Tape Drive.

IMFF

The Information Flip-flop stores the fact that one of the Information Density Multi's (IM1M or IM2M) has been set.

IMIF

The Information Index Flip-flop in conjunction with IMFF synchronizes the indexing logic with the one megacycle clock.

PUCF

The Pile Up Control Flip-flop indicates that the Information Buffer contains a character which is to be shifted to the "W" register.

RCNF

The Record Control Flip-flop indicates that the body of a record is being read from tape.

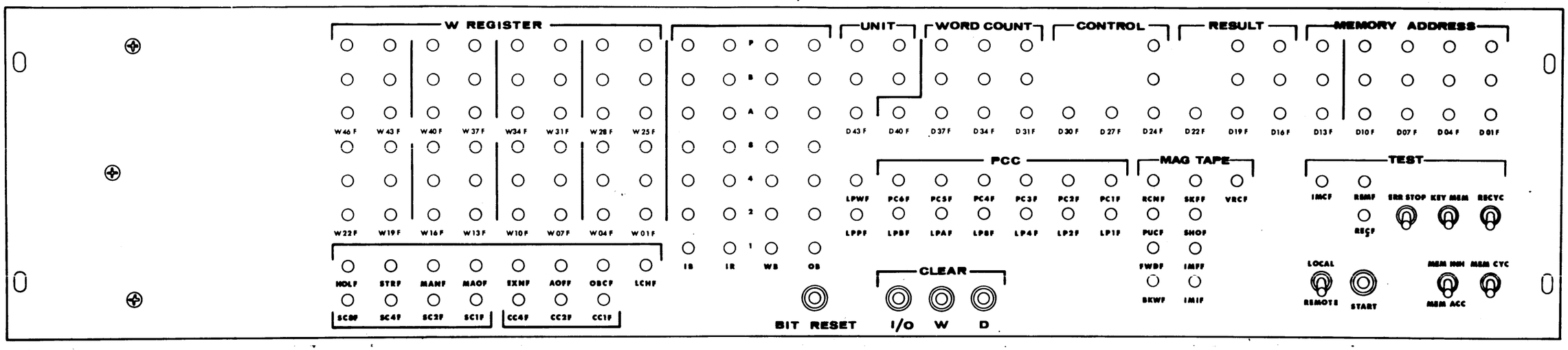


FIGURE 2.3-1 I/O DISPLAY PANEL

SHOF

The Skew Holdover Flip-flop in conjunction with SKFF synchronizes the input checking logic with the one megacycle clock.

SKFF

The Skew Flip-flop is used as a storage element to signify the setting of one of the Digit Skew Multi's.

VRCF

The Valid Record Flip-flop indicates that seven or more characters have been read from tape.

PCC

The Pulse Counter consists of PC1F thru PC6F which are used to divide down the one megacycle clock to some predetermined rate.

LPnF

The Longitudinal Parity 1 thru P Flip-flops accumulate longitudinal parity during the tape operations.

LPWF

The Longitudinal Parity Write Flip-flop in conjunction with the Last Character Flip-flop (LCHF) indicates that the last characters of a record are about to be written on tape. LCHF and LPWF on, along with CC4F on and the Pulse Counter equal to zero or one, form the gate to produce the Tape Write Reset Pulse which causes the writing of the longitudinal parity character.

LOGICAL FLIP-FLOPS

AOFF

The Address Overflow Flip-flop indicates that the D register (D01F ⇒ D15F) has reached its maximum octal addressing capability of 77777 or its minimum addressing capability of 00000.

CC1F ⇒ CC4F

The Character Counter consists of three flip-flops which are used as a counter to indicate when the Word Register is full and to control information transfer to or

from the word register. It is also used at SC-00 time to allow sequential checking of trunk availability and unit busy.

EXNF

External Control Flip-flop serves as a logical toggle to indicate when an I/O descriptor has been obtained. It also is used during the following peripheral unit operators.

1. Card Punch
2. Inquiry
3. KB
4. Printer - 650 LPM
5. Tape Write (Magnetic)

HOLF

Holdover Flip-flop is used in conjunction with STRF to allow transfer of information between units performing asynchronous operations.

LCHF

Last Character Flip-flop.

MANF

Memory Access Needed Flip-flop indicates that a memory access is requested by this I/O unit.

MAOF

Memory Access Obtained Flip-flop indicates the information and its Core Memory address are in the Memory Information Register and the Memory Address Register, respectively.

OBCF

Output Buffer Call Flip-flop indicates that new information is to be shifted to the Output Buffer register.

SC1F thru SC8F

The Sequence Counter consists of four flip-flops which can total any value from 0 ⇒ 15. It is used to control the sequence of I/O operations.

STRF

Strobe Flip-flop is used in conjunction with HOLF to allow tranfer of information between units performing asynchronous operations.

TEST FLIP-FLOPS

IMCF

Initiate Maintenance Cycle Flip-flop remembers that a maintenance cycle has been initiated.

RECF

Recycle Flip-flop allows consecutive maintenance cycles of a particular operation to occur.

REMF

Remote Flip-flop indicates a LOCAL/REMOTE I/O status to Central Control.

SWITCHES - PUSH BUTTON

Bit Reset

If the Bit Reset PB switch is held depressed, depression of any of the indicator switch-lights on the I/O Maintenance Panel clears the corresponding flip-flop and indicator.

Clear

1. I/O

   Clears all the associated I/O logical toggles.

2. D REGISTER

   Clears D register toggles.

3. W REGISTER

   Clears W register toggles.

Start

Depression of the START Switch causes IMCF (Initiate Maintenance Cycle) to set

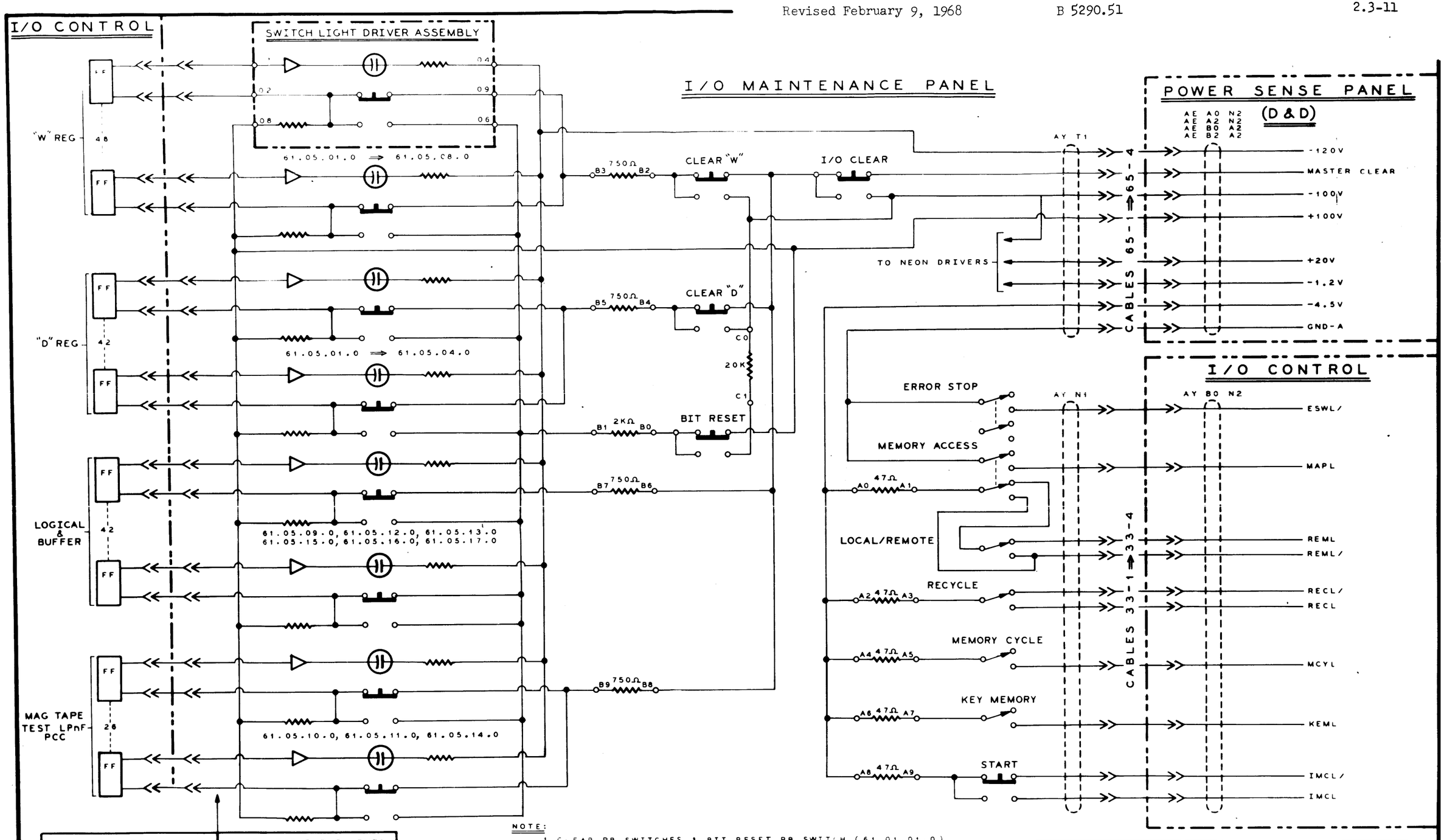
if the sequence counter is equal to zero and the Logical/Remote switch is in LOCAL.

SWITCHES - TOGGLE

Refer to I/O TM5283.51, Section 2.4, Maintenance Aids, for information relative to the use of the I/O maintenance switches.

I/O MAINTENANCE PANEL SCHEMATIC

Figure 2.3-2 is a schematic of the I/O Maintenance Panel. Refer to Figure 4.3-1, Assembly and Disassembly, for the physical location of components.



MANUAL CONTROL LINES			INDICATOR INPUT LINES		
FROM	TO	CABLE NOS	FROM	TO	CABLE NOS
AY N1	AA B0 N2	33-1 ⇒ 33-4	AA B0 A2	AY J1	29-1 ⇒ 29-4
AY P1	AE C0 N2	34-1 ⇒ 34-4	AC C0 A2	AY K1	30-1 ⇒ 30-4
AY R1	AE C0 A2	35-1 ⇒ 35-4	AE C0 N2	AY L1	31-1 ⇒ 31-4
AY S1	AE D0 A2	36-1 ⇒ 36-4	AE D0 N2	AY M1	32-1 ⇒ 32-4

NOTE:

1. CLEAR PB SWITCHES & BIT RESET PB SWITCH (61.01.01.0)
2. TEST SWITCHES (61.01.02.0) LOGICALLY SHOWN IN NON-MAINTENANCE POSITION.

FIGURE 2.3-2
I/O MAINTENANCE PANEL
SCHEMATIC

2.4 POWER FAIL AND POWER SENSE PANEL

GENERAL

A line drawing of the B 5290 Power Fail Display Panel is shown in Figure 2.4-1. Refer to TM B 5370.51, Sections 2 and 6 for troubleshooting and circuit discription.

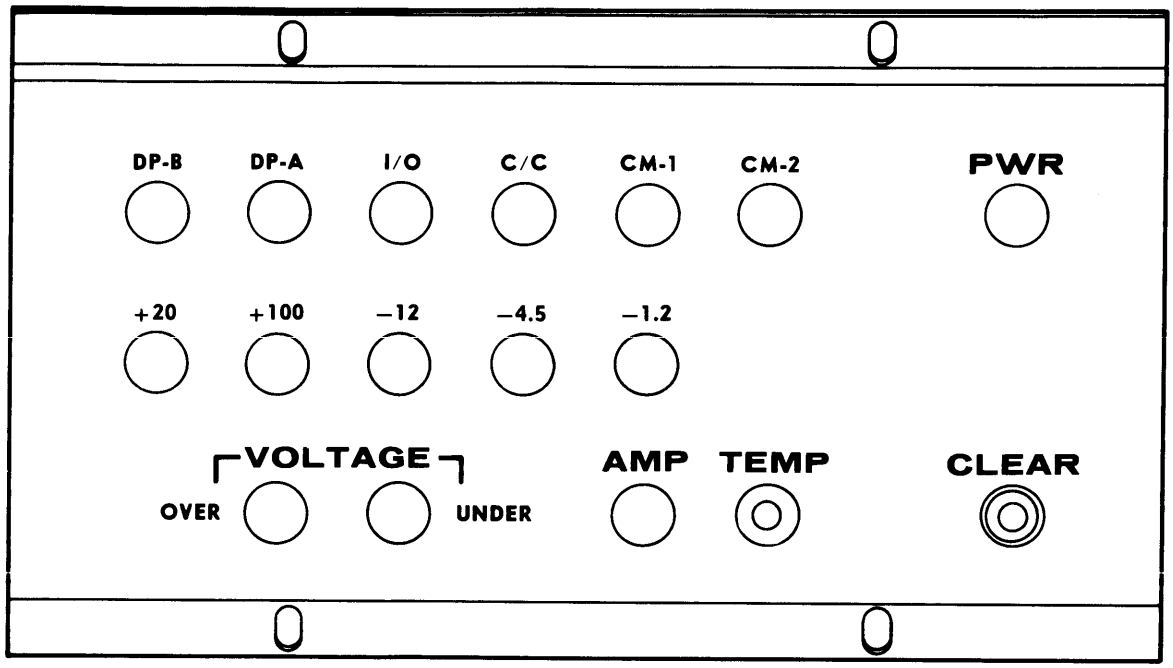


FIGURE 2.4-1 POWER FAIL DISPLAY PANEL

POWER FAIL DISPLAY PANEL

Power Fail Indicators

The Power Fail Indicators remember power failures through the actuation of latching relays supplied by -24V. Power failures are defined by the following:

CABINET - These indicators are used to localize a -12V, -4.5V, and a -1.2V failure to a particular cabinet.

VOLTAGE - These indicators are used to show a voltage failure in +20V, +100V, -12V, -4.5V, and -1.2V. The +20V and +100V indicators are used for the entire system and are not associated with the cabinet indicators.

OVER/UNDER - These indicators are used to show an over/under voltage condition in the +20V, +100V, -12V, -4.5V and -1.2V supplies.

AMP - This indicator shows an excess current condition in the -12V supply of any one of the cabinets.

TEMP - This indicator shows the sensing of an overheat condition by a cabinet thermostat.

PWR - This indicator shows the sensing of an overheat condition in the Power Supply Cabinet.

SWITCH - P.B.

Clear P.B.

The Clear Push Button is used to open the -24V circuit to the power fail latching relays.

2.5 INDICATOR SWITCH LIGHT ASSEMBLY

Refer to Figure 2.5-1 for Indicator Switch light pin numbering and connections. Refer to Section 6 for circuit description.

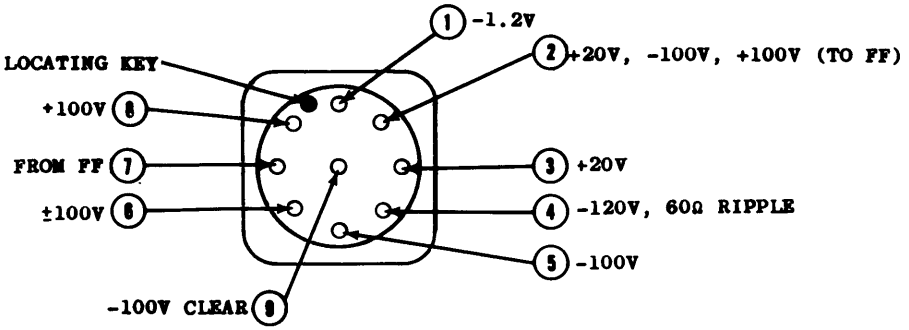


FIGURE 2.5-1 INDICATOR SWITCH LIGHT SOCKET

Refer to Figure 2.5-2 for Indicator Switch Light schematic. Refer to Figure 4.4-1 for view of Switch-Light Driver Assembly.

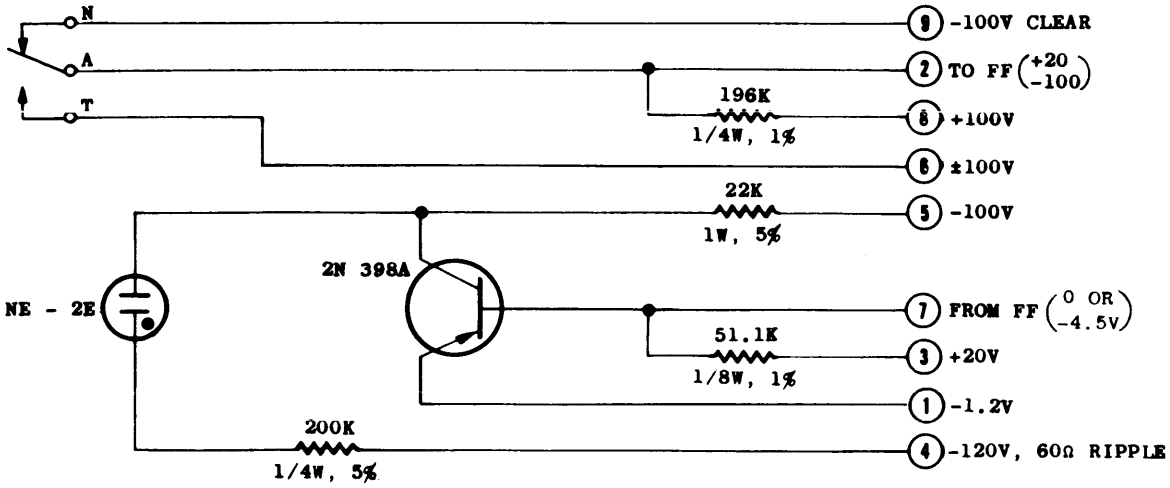
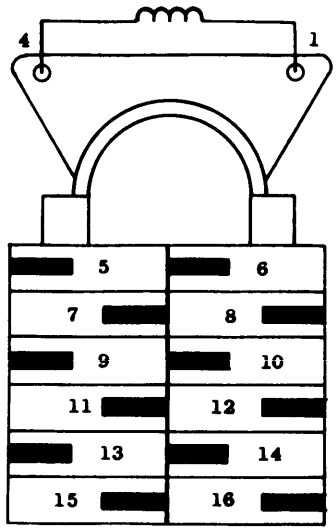


FIGURE 2.5-2 INDICATOR SWITCH LIGHT SCHEMATIC

2.6 RELAYS

POWER CONTROL

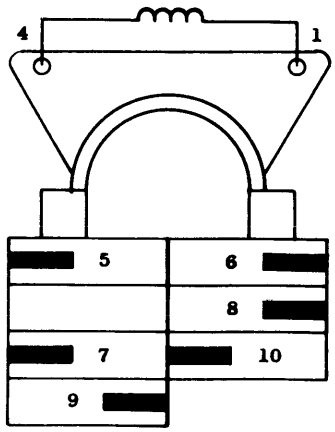
The Power Control Panel Relays are shown in the following figures.



COIL CHARACTERISTICS

COIL RESISTANCE: 300 OHMS ± 10 PERCENT @ 25° C.
OPERATING CURRENT: .080 AMPS NOMINAL.
OPERATING VOLTAGE: 12V DC.

✓FIGURE 2.6-1 K13, 18, 19, 16 (S-11036969)



COIL CHARACTERISTICS

COIL RESISTANCE: 500 OHMS ± 10 PERCENT @ 25° C.
OPERATING CURRENT: .048 AMPS NOMINAL.
OPERATING VOLTAGE: 24V DC.

FIGURE 2.6-2 K14 AND K15 (S-11895380)

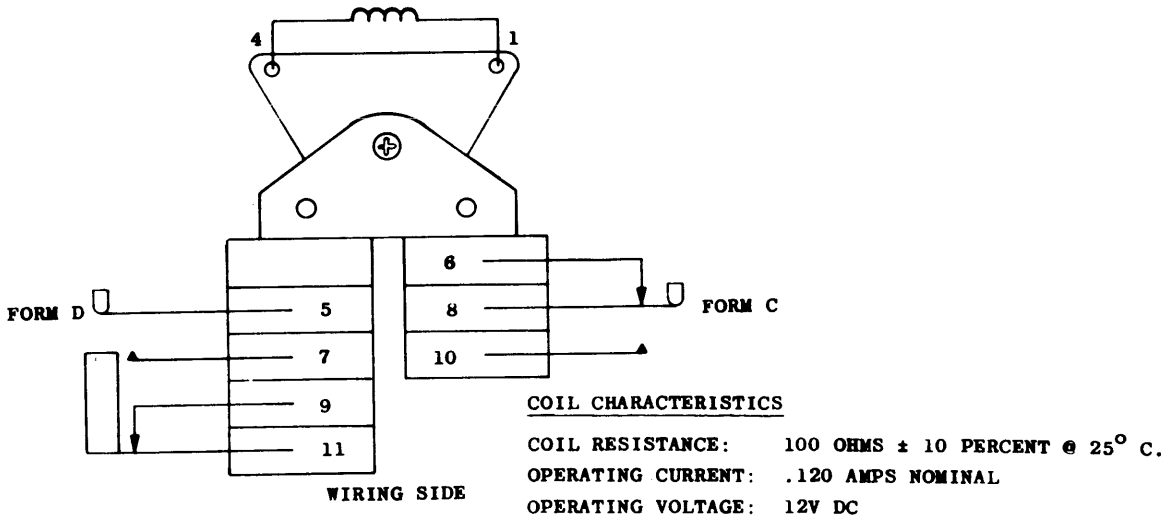


FIGURE 2.6-3 K17 (S-11895398)

Refer to Section 5, Figure 5.2-2 for physical location of the above relays.

Refer to Technical Manual B 5370.51, Sections 2 and 6 for Troubleshooting and Circuit Analysis.

FIGURE 2.6-4

✓(NO LONGER APPLICABLE)

POWER FAIL RELAYS

The Power Fail relays are mounted four to a paralled plate package. The location of these KPK relay packs is shown in Figure 5.5-2.

SYSTEM CLEAR RELAY

The System Clear Relay may be energized by the CC Master Clear switch, or by the Load switches located on the CC Maintenance Panel and Operators Console Display Panel. Refer to Figure 2.1-2 for circuit wiring. Refer to Figure 4.1-1 for physical location. Refer to Figure 2.6-5 for relay characteristics.

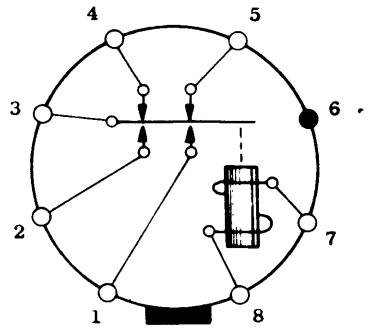


FIGURE 2.6-5 SYSTEM CLEAR RELAY

NOTE: This page replace Page 2.6-3 dated February 2,1964

2.7 SPECIAL TOOLS

In addition to the normal tools provided for system maintenance the following special tools are also provided:

1. Diode-stick cutters.
2. Wire-wrap tools.
3. Cable-connector-pin insertion and removal tools.
4. Cover-removal tool.
5. Package handles.
6. Indicator Switch Light Assembly removal tool.

DIODE STICK CUTTING TOOL (P/N 11838109)

The diode sticks provided as spares are uncut. The diode stick cutter is a plier-like device which can be used to cut the diode sticks as needed. Care must be taken when using the cutter to keep from breaking the bond between the diodes or resistors and the common bus. The diode-stick tool must not be used for any other purpose.

WIRE UNWRAP TOOL (P/N 11838058)

The hand wrapping tool (see Figure 2.7-1) is used when it is necessary to remove a wire from a pin. The tool has two ends; one end is for wires which are wrapped in a clockwise direction; the other end is for wires which are wrapped in a counter-clock-wise direction. To use this tool, proceed as follows:

1. Determine the direction of wrap and insert the appropriate end of the tool over the pin.
2. Rotate the tool until the wire is sufficiently uncoiled so that it can be removed from the pin.

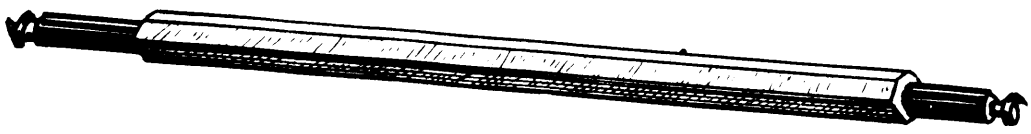


FIGURE 2.7-1 DUAL, RIGHT & LEFT HAND, UNWRAPPING TOOL

WIRE WRAP TOOL (P/N 1183804-2)

The wire-wrap tool is a hand-wrapping tool and is shown in Figure 2.7-2. The tool will wrap a standard field change wire (24 guage).

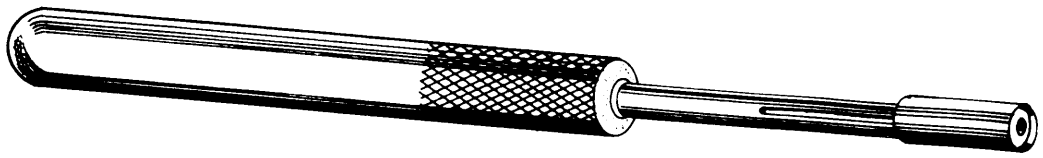


FIGURE 2.7-2 WIRE WRAP TOOL

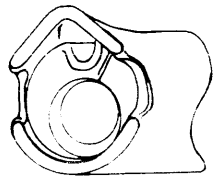
Figure 2.7-3, A through F, shows the steps used to wrap a connection. To wrap a new wire, proceed as follows:

1. Remove the insulation from the end of the wire. Approximately 1 1/4" of wire is required for a six-turn connection of 24-guage wire.

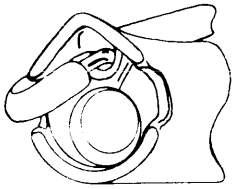
2. Place the tool over the wire as shown in Figure 2.7-3B.

3. Anchor the wire as shown in Figure 2.7-3C and insert the tool over the pin as shown in Figure 2.7-3D.

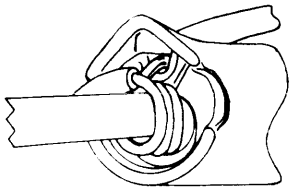
4. Rotate the tool in a clockwise direction. The wire will wrap around the pin as shown in Figure 2.7-3E and Figure 2.7-3F. Too much pressure will cause the wire to bunch.



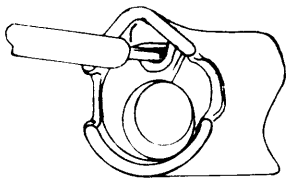
A-BIT AND SLEEVE



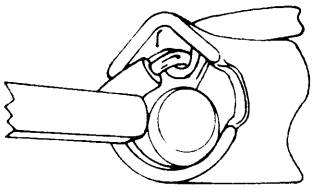
C-WIRE ANCHORING



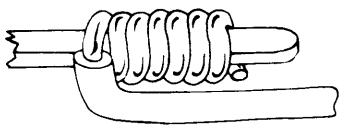
E-WRAPPING



B-WIRE INSERTION



D-TERMINAL INSERTION



F-FINISHED CONNECTION

FIGURE 2.7-3 WIRE WRAPPING

The following should be used as a guide when installing FCNs, or when making wire wrap changes in the field.

1. Number of turns - The minimum number of turns (per connection) of bare wire is FIVE, and the maximum number is SEVEN. The maximum number of turns of insulation preceding the bare wire is THREE for any connection.

2. Insufficient Insulation - Wire insulation shall be no greater than 1/32" from wire wrap connections.

3. Wire and Terminal Contact - The bare wire and terminal must make contact on all corners following the point at which the origin of the number of turns is counted.

4. Separation of Turns - Turns may have a maximum separation of 1/2 the thickness of wire being used to make the wrapped connection.

5. Excessive Tail Wire - The wire tail shall be constructed as being "That end of bare wire which follows the last wrap." That wire tail shall be paralleled to the terminal surface within 1/32".

6. Overlapping of Turns - This condition is caused when succeeding wraps overlap the ones previously made. If this condition exists, it will be necessary to make a new connection.

7. Clearance - There shall be at least 1/32" clearance between grid pattern connections, terminals, bare wire or components.

8. Height - The maximum clearance between the connector block and the first turn of the first connection shall be 1/16".

9. Height for Single Wire Wrap - The maximum height for a single wire wrap shall be 1/4".

10. Height for Two Wire Wraps - The maximum height for two wire wrap connections shall be 1/2".

11. Unwrapping - The wire wrap connection shall be capable of being unwrapped from the wire wrap terminal without breaking. The unwrapping operation shall be done with a standard unwrapping tool only, so as to insure the life of the wire wrap terminal.

12. Wire Re-use - IF A WIRE WAS PREVIOUSLY WRAPPED, THE PORTION OF THE WIRE WHICH WAS WRAPPED CANNOT BE USED AGAIN. If the old wire is not long enough to strip off enough insulation to permit another wrap, a new wire must be routed in its place. Soldering a wire wrapped connection directly at the wire wrapped terminal shall not be permitted at any time.

13. Terminal Re-use - Prior to rewrapping, the terminal shall be inspected for planting loss, corrosion or other damage. The evidence of any damage, planting loss or corrosion will in effect cause the wire connection not to maintain the high degree of quality and reliability which is required. The terminal therefore, must be replaced with a new terminal.

CABLE-CONNECTOR PIN INSERTION TOOL (P/N 11838075)

Refer to page 4.7-1 of this manual for a description of how to use this tool.

CABLE-CONNECTOR PIN REMOVAL TOOL (P/N 11838067)

Refer to page 4.7-1 of this manual for a description of how to use this tool.

COVER-REMOVAL TOOL (P/N 80551)

The cover-removal tool is a 3/8" Allen-set-screw wrench. The short end is cut off to approximately 1/2" and a plastic handle is inserted on the long portion of the wrench.

PACKAGE HANDLES (P/N 77213)

Special non-conduction handles are provided for use in removing diode sticks. These handles must be removed from the package before the gates are closed.

INDICATOR SWITCH LIGHT REMOVAL TOOL (16200016)

This tool is used for the removal of the nut which secures the Indicator Switch light driver assembly to the Maintenance Panel. Refer to Figure 2.7-4.

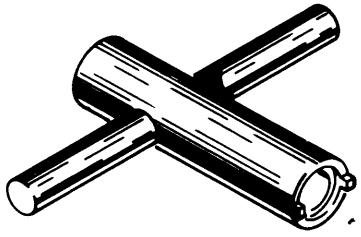


FIGURE 2.7-4 INDICATOR SWITCH LIGHT REMOVAL TOOL

2.8 PRECAUTIONS

1. Do not use a battery-buzzer for continuity checking. The buzzer current exceeds the maximum current rating for diodes and transistors.

2. Do not use the first two low scales (X1 or X10) on the Triplett ohmmeter for continuity checking. For these scales, the meter current exceeds the maximum current rating for diodes and transistors.

3. Do not remove packages or diode sticks when Power is Up.

4. Care must be taken when using Scope or Jumper Clip Leads to prevent touching adjacent pins. Use Minigator Clips with insulators or the Wire Wrap Pin Probe Tip (Part No. 1183854?).

5. Use extreme caution when working on the plug-in side of the panels. Avoid hitting packages when moving the scope.

6. Do not attempt to force a TRUE level with -12V.

7. A ground jumper may be used to force a FALSE level.

NOTE

Connect clip to the point to be grounded prior to making ground connection.

8. Do not pull Cable Plugs with POWER ON.

9. Only soldering irons that have an isolation transformer may be used.

10. Scope ground - To prevent ground loops and noise interference use only the ground clip on the scope probe. Attach it to a suitable ground as near as possible to the point being observed.

2.9 RIN INDEX

RIN INDEX FOR THE B 5290 DISPLAY & DISTRIBUTION UNIT (11858230)

RIN NO.	INSTAL. TIME IN HOURS	PRE-REQUISITE	UNITS EFFECTED	DESCRIPTION
5003	2.5		102 ⇒ 143	Install a DC Power On Time Meter and System Clear on DC Power UP sequence.
5003S1	1.5	5003	102 ⇒ 143	(same as 5003)
5009	1.5		102 ⇒ 143	Replacement of the interlock switch in order to obtain a positive, reliable operation.
5010	2.0		102 ⇒ 143	Installation of adhesive identification labels on each cable connector.
5016	1.0		102 ⇒ 143	B 5000 interim test routines revision.
5025	1.0		102 ⇒ 143	Removal of "Master Clear" line termination circuit, plus relocation of bit reset isolation resistor.
5025S1	0.5	5025	102 ⇒ 143	(same as 5025)
5026	0.5		102 ⇒ 143	Prevent Power Interlock Level from turning power down.
5029	0.5		102 ⇒ 143	Installation of cable supports to prevent pinching of cables.
5030	0.5		102 ⇒ 143	Change D&D Panel - connector "D" silkscreening.
5037	1.0		102 ⇒ 143	Install cover over power sense panel.
5039	1.0		102 ⇒ 143	Issue updated and new Test Routines and Card Decks.
5039S1	0.5	5039	102 ⇒ 143	Revise TR5222A.
5039S2	0.5	5039	102 ⇒ 143	TR5206 - Cards 011 and 027 corrections.
5058	1.0		102 ⇒ 143	Release - TR5560A, TR5559A and TR5903. Revision - TR Manual and TR5557.
5059	1.5		102 ⇒ 143	Inhibit occasional short between -100V and +100V, when depressing the BIT RESET button.

RIN NO.	INSTAL. TIME IN HOURS	PRE-REQUISITE	UNITS EFFECTED	DESCRIPTION
5069	1.0		102 ⇒ 143	Revised TR5206 and TR5230, plus revision to the Test Routine Manual.
5077	0.5		102 ⇒ 155	TR5558A revised to B revision.
5089	1.0		102 ⇒ 155	Installation of diode across coil of K19 to limit voltage spike.
5094	4.0		102 ⇒ 155	Plug-in heatsink replacement to prevent the shorting of the collectors in common heatsink.
5094S1	1.0		102 ⇒ 155	Supply transistors for installation of RIN 5094.
5101	1.0		102 ⇒ 155	TR5340 "D" to "E" revision. Improved check on punched card information.
5114	1.0	5113	102 ⇒ 155	Removes -4.5V and adds ground to the Clock Control toggle switch.
5118	2.0		102 ⇒ 155	Installation of hinges on D&D Front Skin Assembly.
5121	0.5		102 ⇒ 155	Revised program for Marginal Test Tape which includes 18 increments and history file.
5122	1.5		102 ⇒ UP	Neon interlock removal to prevent setting random bits in the Central Control Interrupt Register.
5126	0.5		102 ⇒ UP	Revised B 5000 System Special Instruction Book.
5131	0.5		102 ⇒ UP	Addition of a register to eliminate erroneous set of the Halt Flip-flop.

SECTION 3

ADJUSTMENTS

No adjustments are necessary on the Display and Distribution Unit.

SECTION 4

ASSEMBLY AND DISASSEMBLY

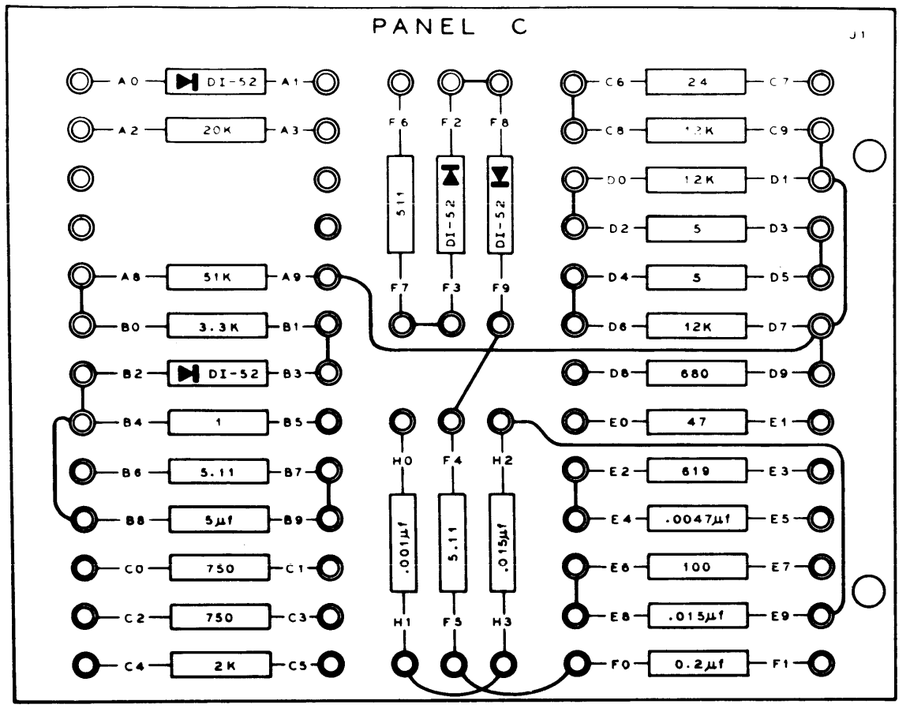
4.1 CC MAINTENANCE PANEL

COMPONENT LOCATION

Refer to Figure 4.1-1 for CC Maintenance Panel Component location.

CIRCUIT FUNCTIONS

Refer to Figure 2.1-2 for Circuit Functions.



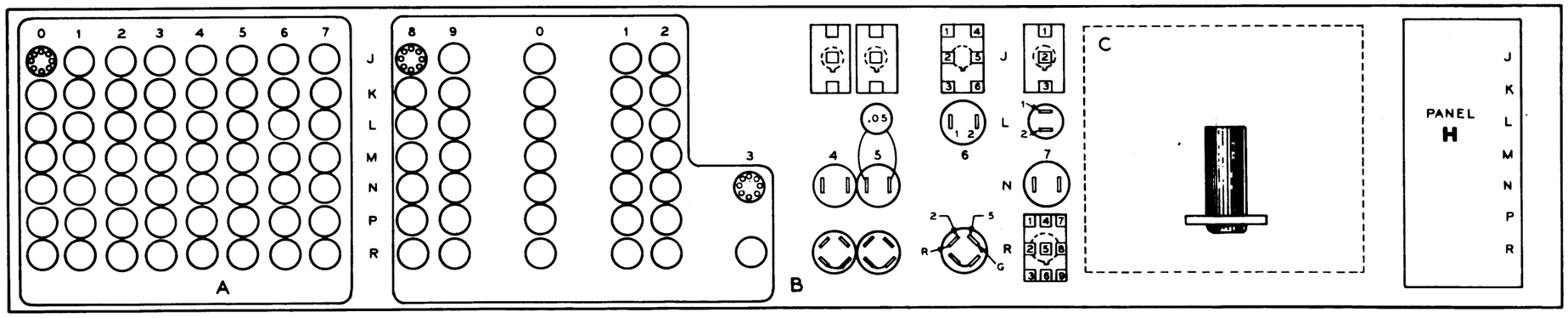


FIGURE 4.1-1
CC MAINTENANCE PANEL
REAR

4.2 PROCESSOR MAINTENANCE PANEL

COMPONENT LOCATION

Refer to Figure 4.2-1 for Processor Maintenance Panel component location.

CIRCUIT FUNCTIONS

Refer to Figure 2.2-2 for Circuit Functions.

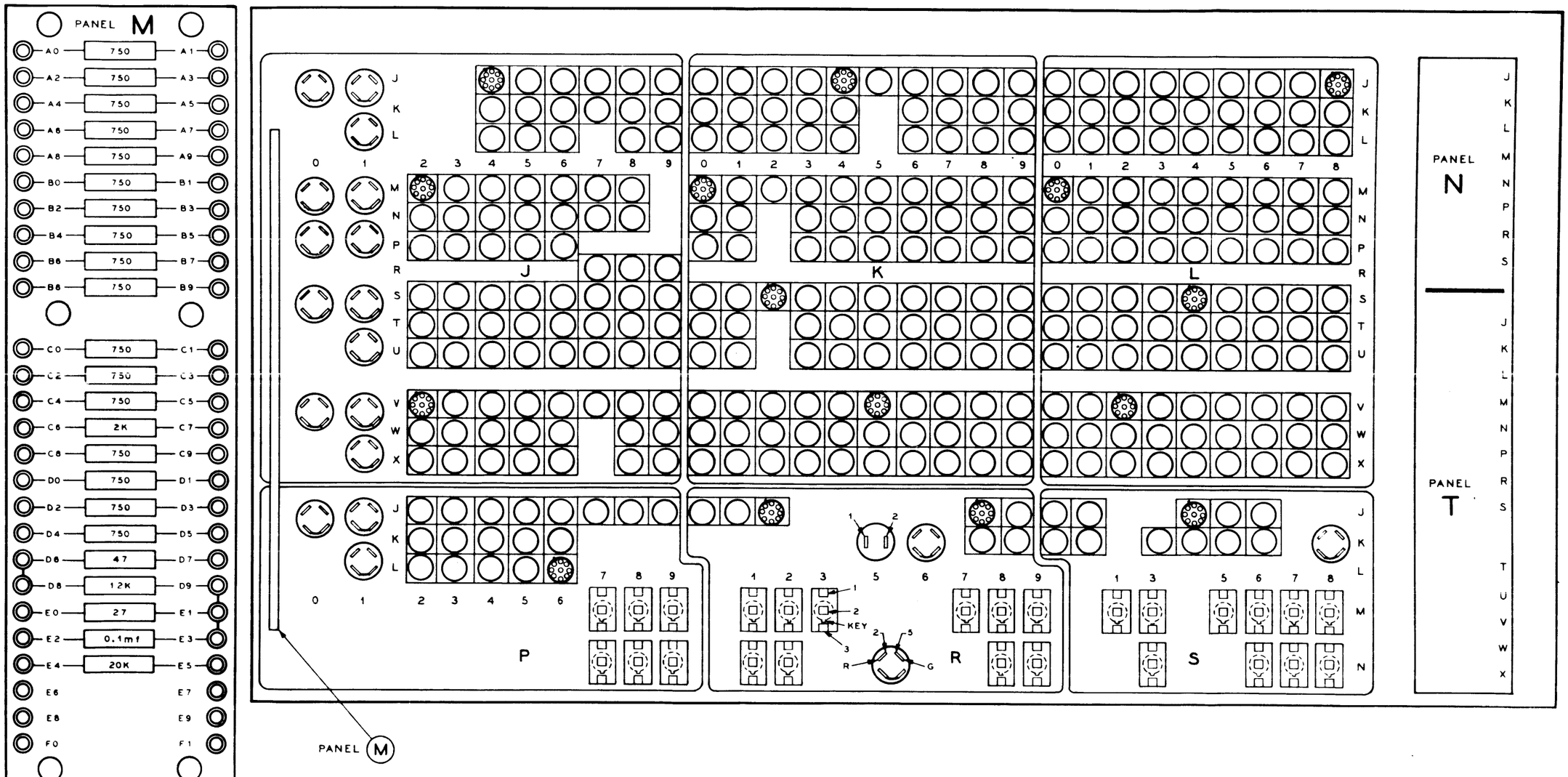


FIGURE 4.2-1
PROCESSOR MAINTENANCE PANEL
PEAR

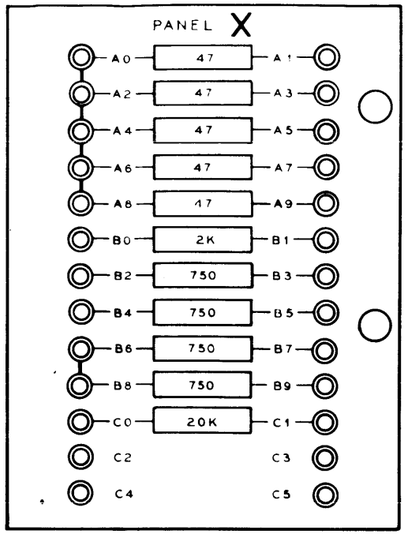
4.3 I/O MAINTENANCE PANEL

COMPONENT LOCATION

Refer to Figure 4.3-1 for I/O Maintenance Panel Component location.

CIRCUIT FUNCTIONS

Refer to Figure 2.3-2 for Circuit Functions.



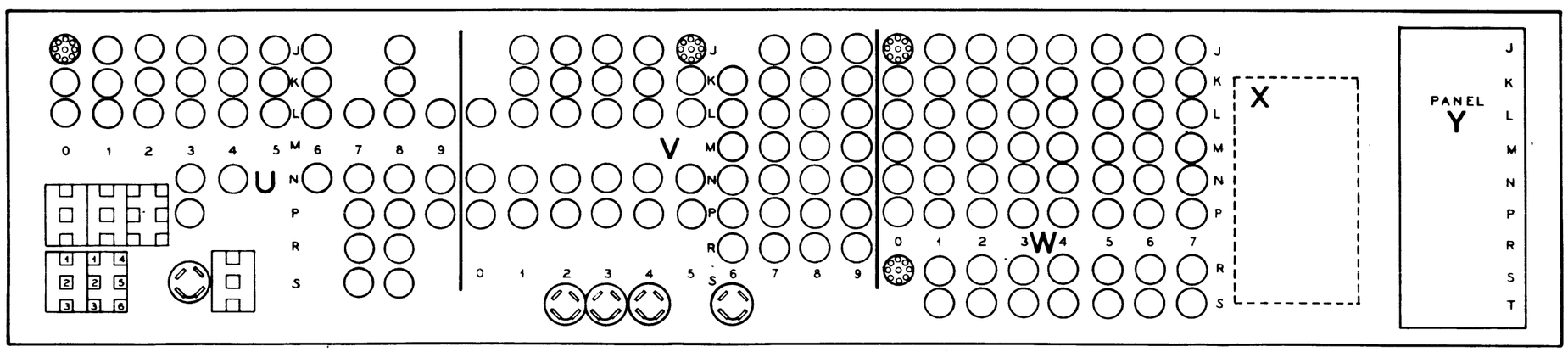


FIGURE 4.3-1
I/O MAINTENANCE PANEL
REAR

4.4 IND. SW-LIGHT DRIVER ASSEMBLY

Refer to Figure 4.4-1 for a line drawing of an Indicator Switch Light Driver Assembly. Refer to Figure 2.5-1 for socket pin numbering.

The Indicator Switch Light Removal Tool P/N 11869382 is to be used for the removal and replacement of this unit.

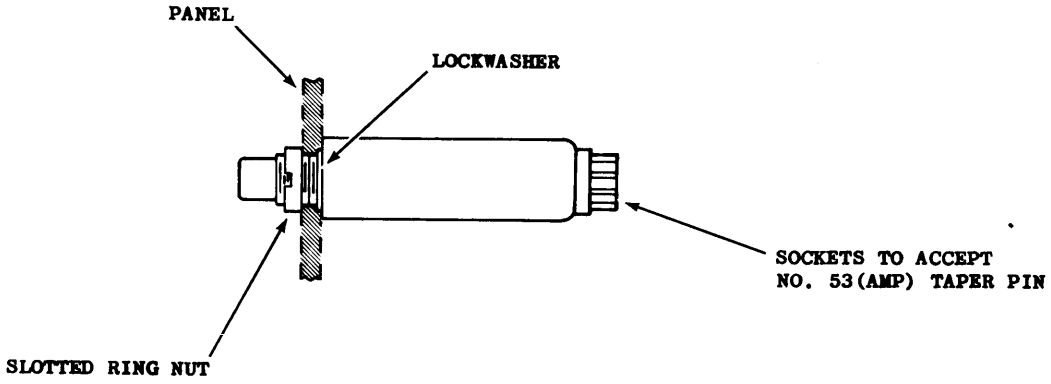


FIGURE 4.4-1 INDICATOR SWITCH LIGHT DRIVER ASSEMBLY

4.5 PACKAGES

Packages, diode sticks, and resistor sticks are removable. Handles are provided which fit into the package extensions. Do not exert any pressure during removal or insertion of a package except on the pull pins. Damage to the package may result if pressure is exerted on the phenolic mounting boards or on any element of the package.

CAUTION

The diode stick handles must be removed before the gate is closed or the package may be damaged.

WARNING

Power must be OFF before removing any element.

4.6 WIRE WRAP PINS

REMOVAL

1. Remove wires with unwrapping tool.
2. If pin is bent, straighten it with long nose pliers.
3. Push on pin from the wire side with long nose pliers. As soon as the pin clears the block (package side), grasp the pin with the pliers and pull it out.
4. If the pin is broken off flush with the pin block, use a small drift punch or another pin held with pliers to drive the pin out.

REPLACEMENT

1. Insert the pin in the block from the package side of the gate. Make sure that the pin is inserted correctly (the contact side of the pin points away from the slot on the side of the pin hole).
2. Take the long-nose pliers and pull on the pin from the wire side until the pin is even with adjacent pins. Do not pull it too far or the pin block may be damaged.

NOTE

The M row pins are U shaped and do not extend through to the package side.

4.7 PINS IN WINCHESTER PLUG

The pins in the Winchester plugs are held in place by a circular spring clip which clips on at the approximate center of the pin. When the pin is fully inserted, the spring clip expands into a groove in the block. This holds the spring in place.

REMOVAL

1. Obtain the cable-pin removal tool (P/N 11838067).

2. Slide the removal tool over the end of the pin until contact is made with the spring clip. Do not put any side strain on the removal tool since there is danger of breaking it. Applying slight pressure to the tool should cause the pin to become free.

REPLACEMENT

1. Use a crimper to connect the pin to its wire.

2. Insert the pin into the plug using the cable-pin insertion tool (P/N 11838075). Take care not to damage the spring clip.

SECTION 5

INSTALLATION

5.1 UNIT PLACEMENT

Refer to Figure 5.1-1 for the B 5290 unit placement within a maximum B 5000 system.

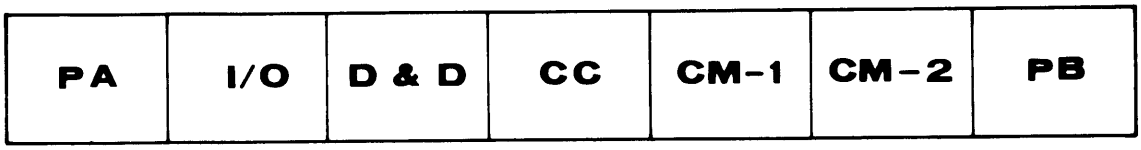


FIGURE 5.1-1 UNIT PLACEMENT

5.2 POWER

INTRODUCTION

Power distribution to the B 5000 system units is routed through rack D of the B 5290 Display and Distribution unit. Refer to Test and Field Document, B 5000 System Distribution and Sensing Index, PL11976693.

POWER CABLES

Power Supply To Display And Distribution

Power Supply cable installation procedures are outlined in the Power Supply Technical Manual, B 5370.51, Section 5. Figure 5.2-1 in this section is to be referenced in conjunction with the procedures mentioned above.

Display And Distribution To All Units

Power distribution and power control cable installation procedures are outlined in the Power Supply Technical Manual, B 5370.51, Section 5. Figures 5.2-2, 5.5-1 and 5.5-2 are to be referenced in conjunction with the procedures mentioned above.

POWER SENSE CABLES

All Units To Display And Distribution

Power sensing cable installation and checkout procedures are outlined in the Power Supply Technical Manual, B 5370.51, Section 5. Figures 5.5-1 and 5.5-2 are to be referenced in conjunction with the procedures mentioned above.

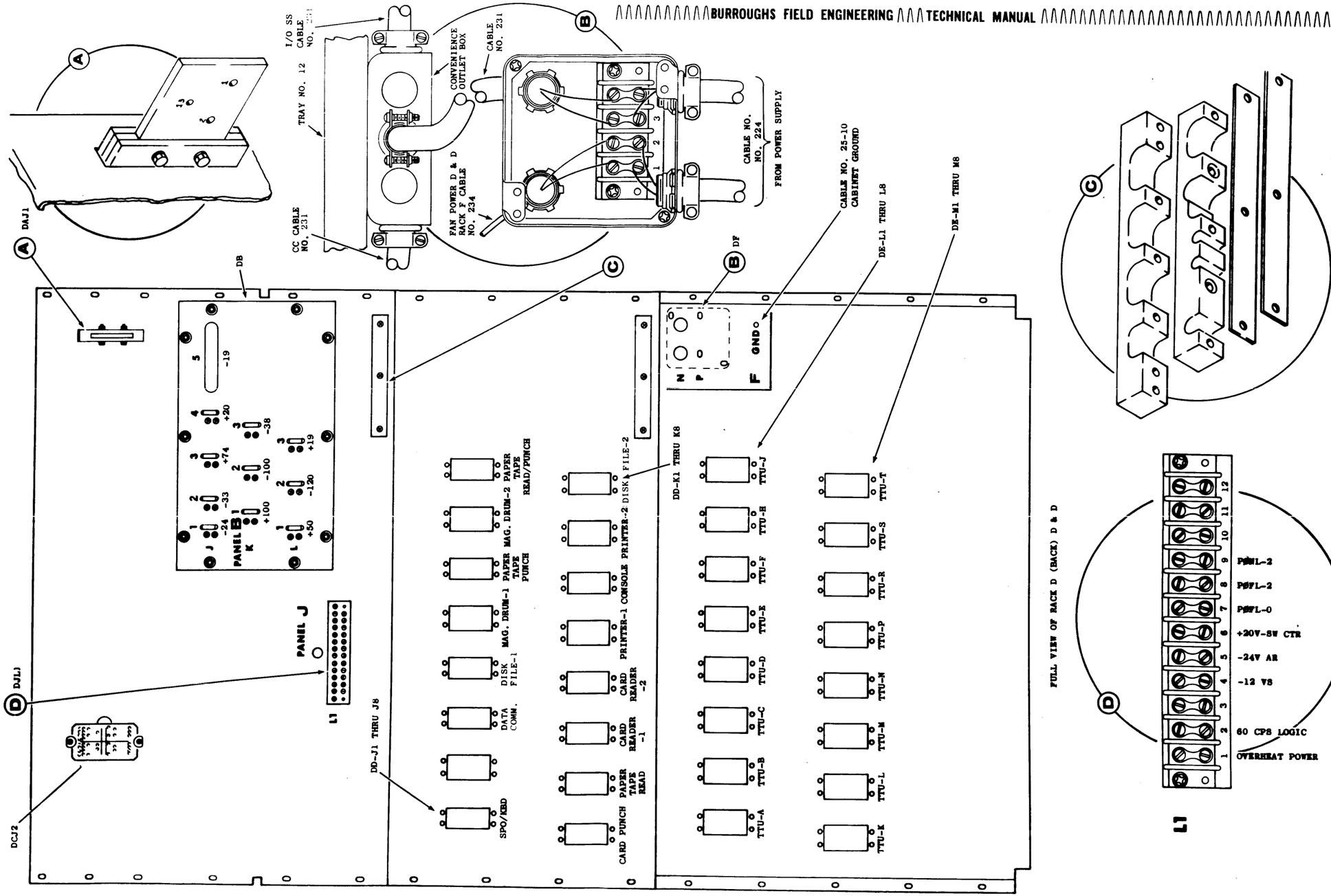
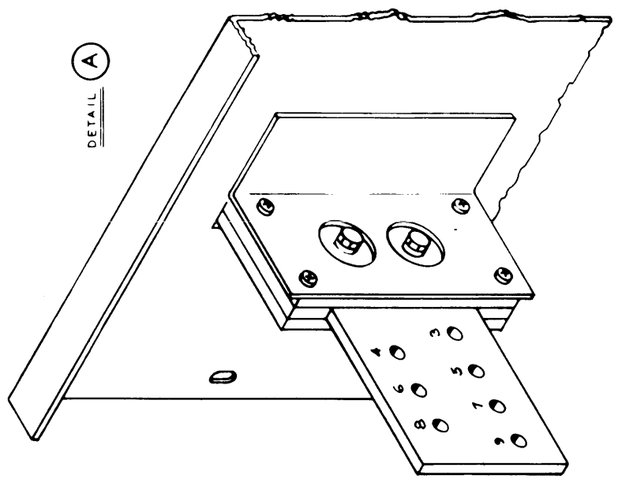
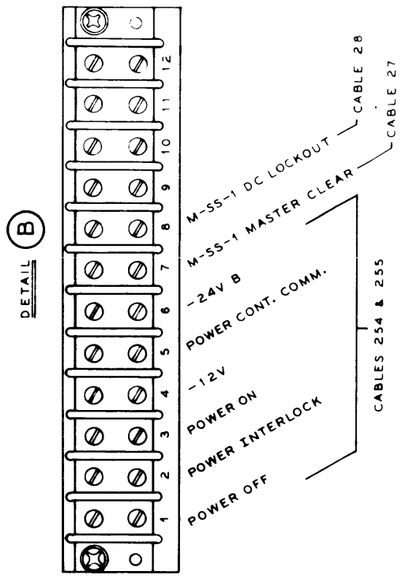
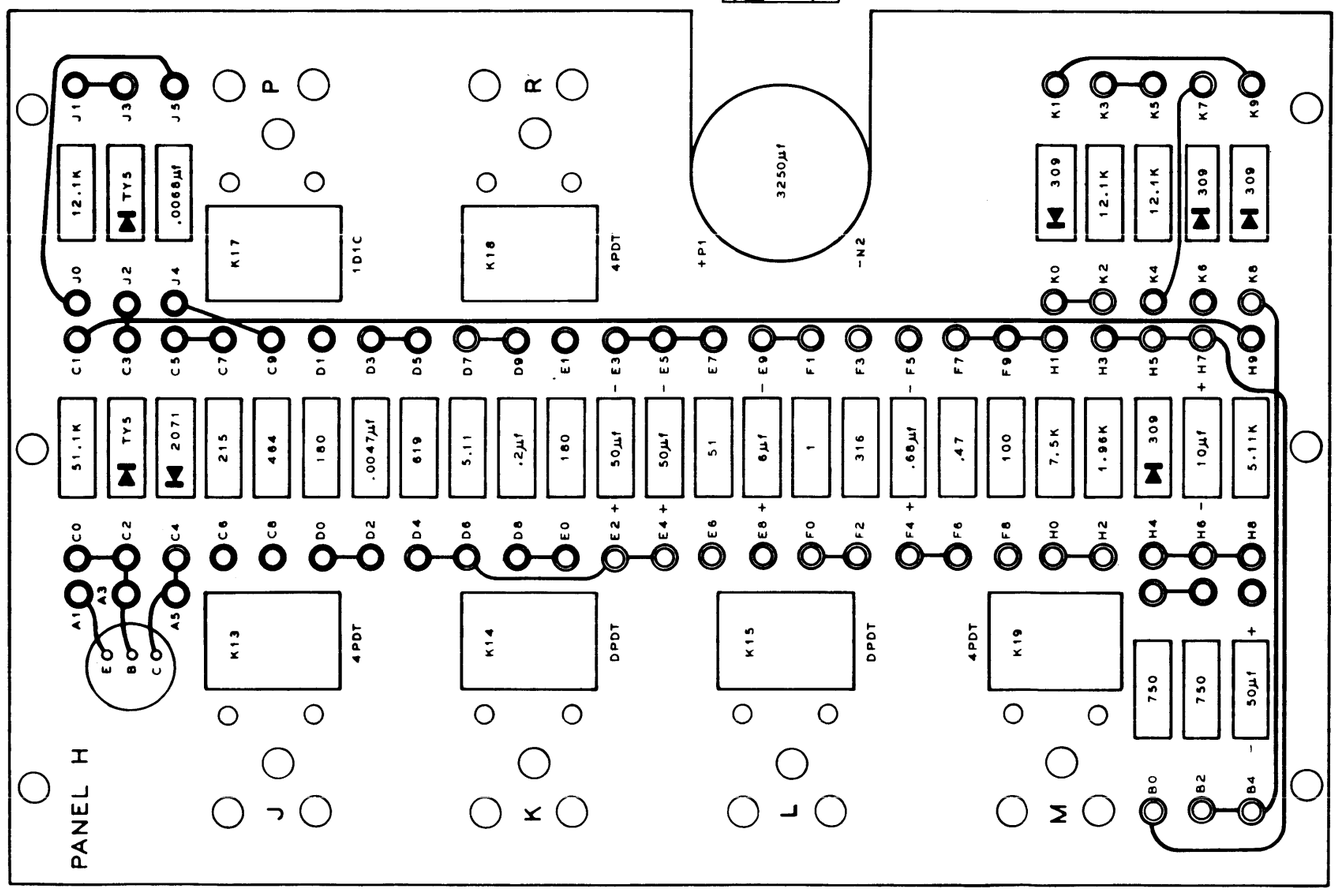
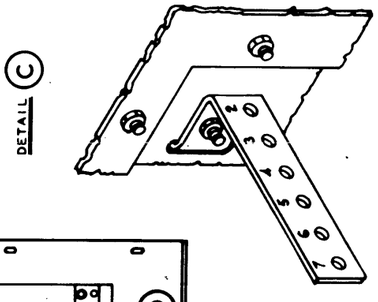


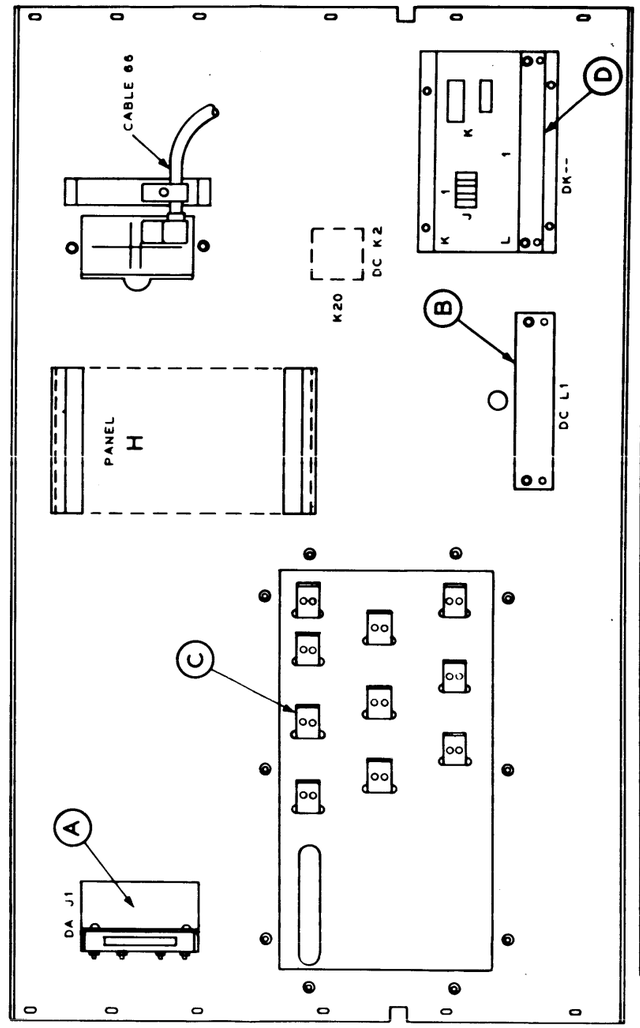
FIGURE 5.2-1 D & D POWER DISTRIBUTION - REAR











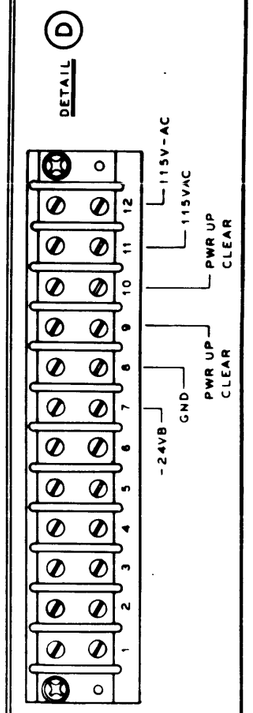


FIGURE 5.2-2
D&D POWER DISTRIBUTION
FRONT

5.3 GROUND, FAN AND CONVENIENCE CABLE DISTRIBUTION

Install cables as listed in the following tables.

TABLE 5.3-1 D & D GROUND AND FAN CABLES

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
25-10	CABINET GROUND (#4 AWG)	D & D	FRAME	D & D	DF GROUND	NT
234	115VAC FAN DISTRIBUTION (#12 AWG)	D & D	DF P1 01/02	D & D	FA K1 06/07	NT

NOTE: INTERCABINET GROUND STRAPS SHOULD BE CONNECTED WHEN THE CABINET FRAMES ARE BOLTED TOGETHER.

TABLE 5.3-2 D & D TO CC - FAN CABLE

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
225	115VAC FAN INPUT (#12 AWG)	D & D	FA K1 06/07	CC	FA K1 06/07	NT

TABLE 5.3-3 D & D TO I/O SS - FAN CABLE

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
228	115VAC FAN INPUT (#12 AWG)	D & D	FA K1 06/07	I/O-SS	FA K1 06/07	NT

TABLE 5.3-4 D & D TO ALL UNITS - CONVENIENCE OUTLETS

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
231	115VAC CONVENIENCE CIRCUIT (#12 AWG)	D & D	DF P1 03/04	ALL UNITS	HBL1/L2 01/02	NT

TABLE 5.3-5 D & D TO DRUM S/S - GROUND CABLE

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
25-15	CABINET GROUND	D & D	DF GROUND	DRUM-SS	DRUM CABINET GROUND	NT

5.4 D & D TO D & D DISPLAY PANEL CABLES

GATES A AND B

Table 5.4-1 lists the D & D to D & D Power Cables.

TABLE 5.4-1 POWER CABLES

CABLE NO.	FUNCTION	FROM		TO		VIA TRAY
		UNIT	CONNECTOR	UNIT	CONNECTOR	
14		D & D	AH R1	D & D	DD K6	3F
62	DISPLAY POWER - PA (GATE A)	D & D	AE A0 A2	D & D	AT U1	NT
63	DISPLAY POWER - PB (GATE B)	D & D	AE B0 N2	D & D	AT U1	NT
64	DISPLAY POWER - CC	D & D	AE A2 A2	D & D	AH S1	NT
65-1	DISPLAY POWER - I/O-1 (GATE A)	D & D	AE A0 N2	D & D	AY T1	NT
65-2	DISPLAY POWER - I/O-2 (GATE A)	D & D	AE A2 N2	D & D	AY T1	NT
65-3	DISPLAY POWER - I/O-3 (GATE B)	D & D	AE B0 A2	D & D	AY T1	NT
65-4	DISPLAY POWER - I/O-4 (GATE B)	D & D	AE B2 A2	D & D	AY T1	NT
66	POWER CONTROL	D & D	DC J2 N2	D & D	AE B2 N2	NT
140	POWER CONTROL	CC	CS 07	D & D	AE A0 A7	2F

Check Gates A and B (Figure 5.5-1 and Figure 5.5-2) to verify proper installation.

5.5 INTER-UNIT CABLES

GATES A AND B

Refer to Figure 5.5-1 and 5.5-2 for physical placement of D & D cables.

Refer to Section 5 of the following Technical Manuals for the installation of Inter-Unit cables to gates A and B of the B 5290 Display and Distribution unit.

1. B 5220.51 - Central Control Technical Manual
2. B 5282.51 - I/O Technical Manual
3. B 5260.51 - Core Memory Manual
4. B 5281.51 - Central Processor Manual

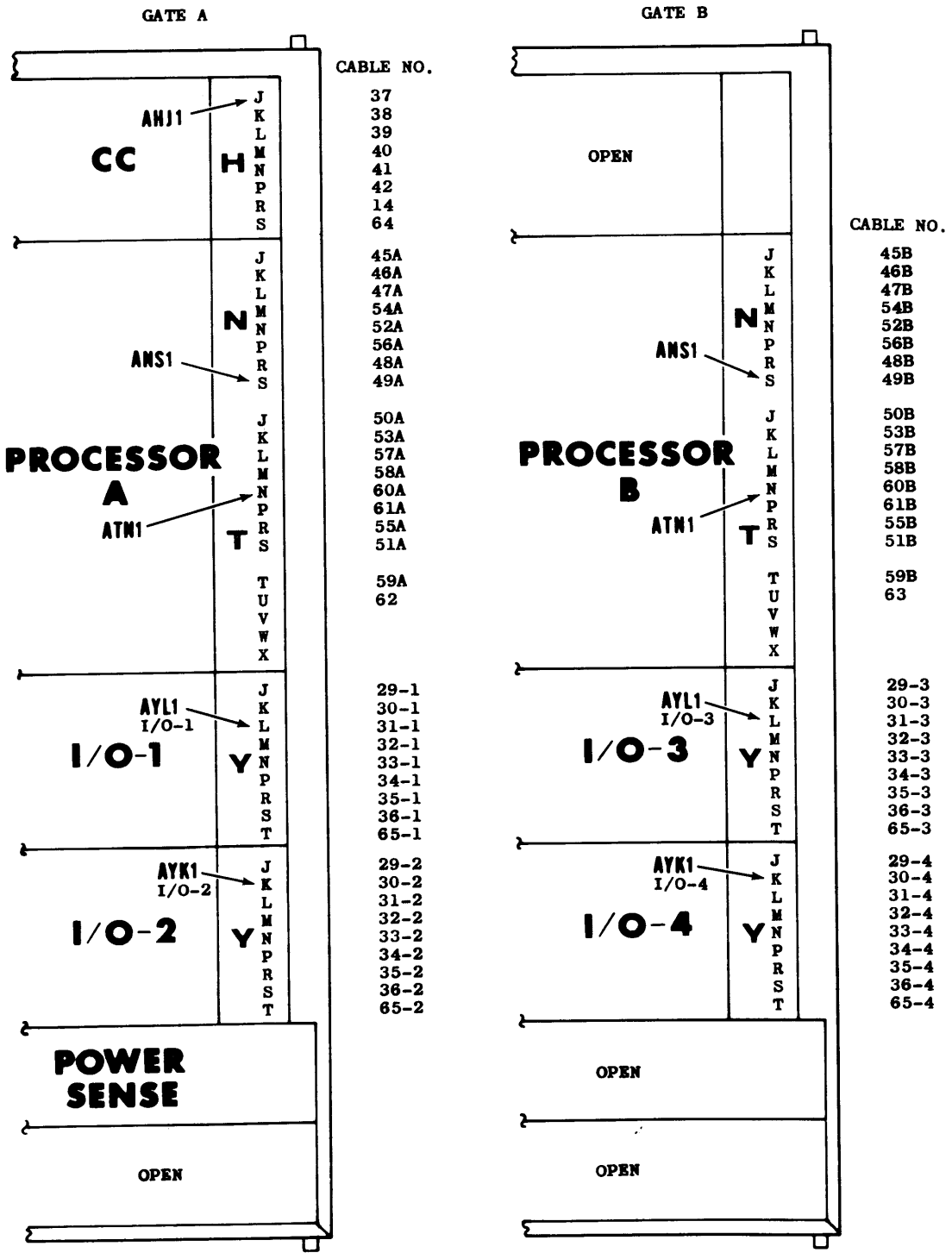


FIGURE 5.5-1 D & D GATE A & B CABLE LOCATOR

PANEL - F

PANEL -

	4	3	2	1	0	9	8	7	6	5
A						SW-L 1. PA FAIL 2. PB FAIL 3. CC FAIL 4. I/O FAIL 5. O.H. POWER SUPPLY	VSC -4.5 CC	VSC -4.5 PB	VSC -4.5 PA	VSC -1.2 CC
						SW-L 1. CM-1 FAIL 2. CM-2 FAIL 3. O.H. FAIL 4. EC CM-1 5. EC CM-2	VSC -4.5 CM-2	VSC -4.5 CM-1	VSC -4.5 I/O	VSC -1.2 I/O
B			CONNECTORS TO INDICATORS & CLEAR BUTTON	KPK CM-1 CM-2 POWER OVERHEAT	KPK PA PB CC I/O	SW-L 1. CM-1 RELAY 2. CM-2 RELAY 3. O.H. RELAY 4. POWER RELAY	SW-L 1. I/O RELAY 2. PA RELAY 3. PB RELAY 4. CC RELAY	SW-L 1. INH. LEVEL 2. EC I/O 3. EC CC 4. EC PB 5. EC PA	VSC -12 CC	VSC -12 PB	VSC -12 PA	VSC -1.2 CM-1
				KPK -12 -1.2 -4.5 +100	KPK EC UV OV +20	SW-L 1. +20 RELAY 2. -12 RELAY 3. -1.2 RELAY 4. 4.5 RELAY 5. +100 RELAY	SW-L 1. EC RELAY 2. OV RELAY 3. UV RELAY	SW-L 1. +20V OV/UV 2. -12 FAIL 3. -1.2 FAIL 4. -4.5 FAIL 5. +100V OV/UV	VSC -12 CM-2	VSC -12 CM-1	VSC -12 I/O	VSC -1.2 CM-2

L – F					PANEL – E																
2	1			0	9		8		7		6		5		4		3		2		1		0
					SW-L 1. PA FAIL 2. PB FAIL 3. CC FAIL 4. I/O FAIL 5. O.H. POWER SUPPLY			VSC -4.5 CC		VSC -4.5 PB		VSC -4.5 PA		VSC -1.2 CC		VSC -1.2 PA			C50 FROM AH-S1 ON CC DISPLAY PANEL CABLE NO. 64		C50 POWER FROM CC REGULATOR CABLE NO. 140	C50 PA SENSE & POWER CABLE NO. 62
					SW-L 1. CM-1 FAIL 2. CM-2 FAIL 3. O.H. FAIL 4. EC CM-1 5. EC CM-2			VSC -4.5 CM-2		VSC -4.5 CM-1		VSC -4.5 I/O		VSC -1.2 I/O		VSC -1.2 PB			C50 I/O 2 SENSE & POWER CABLE NO. 65-2			C50 I/O 1 SENSE & POWER CABLE NO. 65-1
KPK PA PB CC I/O	SW-L 1. CM-1 RELAY 2. CM-2 RELAY 3. O.H. RELAY 4. POWER RELAY	SW-L 1. I/O RELAY 2. PA RELAY 3. PB RELAY 4. CC RELAY			SW-L 1. INH. LEVEL 2. EC I/O 3. EC CC 4. EC PB 5. EC PA			VSC -12 CC		VSC -12 PB		VSC -12 PA		VSC -1.2 CM-1		VSC +20			C50 I/O 4 SENSE & POWER CABLE NO. 65-4			C50 I/O 3 SENSE & POWER CABLE NO. 65-3
KPK EC UV OV +20	SW-L 1. +20 RELAY 2. -12 RELAY 3. -1.2 RELAY 4. 4.5 RELAY 5. +100 RELAY		SW-L 1. EC RELAY 2. OV RELAY 3. UV RELAY		SW-L 1. +20V OV/UV 2. -12 FAIL 3. -1.2 FAIL 4. -4.5 FAIL 5. +100V OV/UV			VSC -12 CM-2		VSC -12 CM-1		VSC -12 I/O		VSC -1.2 CM-2		VSC +100		VRP	C50 SPECIAL D/D VOLTAGES NOT SENSING LEVELS CABLE NO. 66			C50 PB SENSE & POWER CABLE NO. 63

FIGURE 5.5-2 POWER SENSE PANEL - REAR

5.6 UNIT CONNECTORS

RACK D PERIPHERAL

Refer to CC Technical Manual B 5220.51, Section 5 for the installation of CC to D & D peripheral unit cables.

Refer to Figure 5.2-1 in this section for the physical location and callouts of the Winchester connector sockets.

5.7 ADDING ADDITIONAL D & D GATE

INTRODUCTION

It is Field Engineering's responsibility to install and checkout any D & D Display Panels which may be added to the system whenever a customer's needs require additional units.

This section outlines the procedure for installing and checking out these additional units.

INNER GATE INSTALLATION

Mounting Gate

Gates A and B are located as shown in Figure 5.7-1.

Figure 5.7-1 shows the location of each part used in mounting the gates.

Use Figure 5.7-1 and the following instructions to facilitate mounting the new unit. Numbers in brackets (NO.) refer to parts location shown in circles in Figure 5.7-1.

NOTE

Due to the weight of the gate complete with panels and packages it is advisable to remove at least two panels (if shipped complete) prior to installation.

1. Open the outer gate to a 90° angle with the front of the cabinet.
2. Place blocks under the gate to support it while removing the upper door hinge mounting (2).
3. Remove upper dowel pin (1).
4. Place the top inner gate bracket (11) into position and replace upper dowel pin (1) through the bracket into the outer gate.
5. Replace the upper door hinge mounting (2).
6. Remove the lower door hinge mounting (6).
7. Using a suitable lever (2 x 4, crowbar or pinch bar) lift the outer gate at the same time moving the bottom toward the center of the cabinet. Remove the lower dowel pin (3), thrust washers (4) and spacer (5).
8. Place the bottom inner gate bracket (12) on the lower dowel pin with 1 thrust washer (4a) above and below the bracket. Insert the dowel pin into the bottom of the gate.

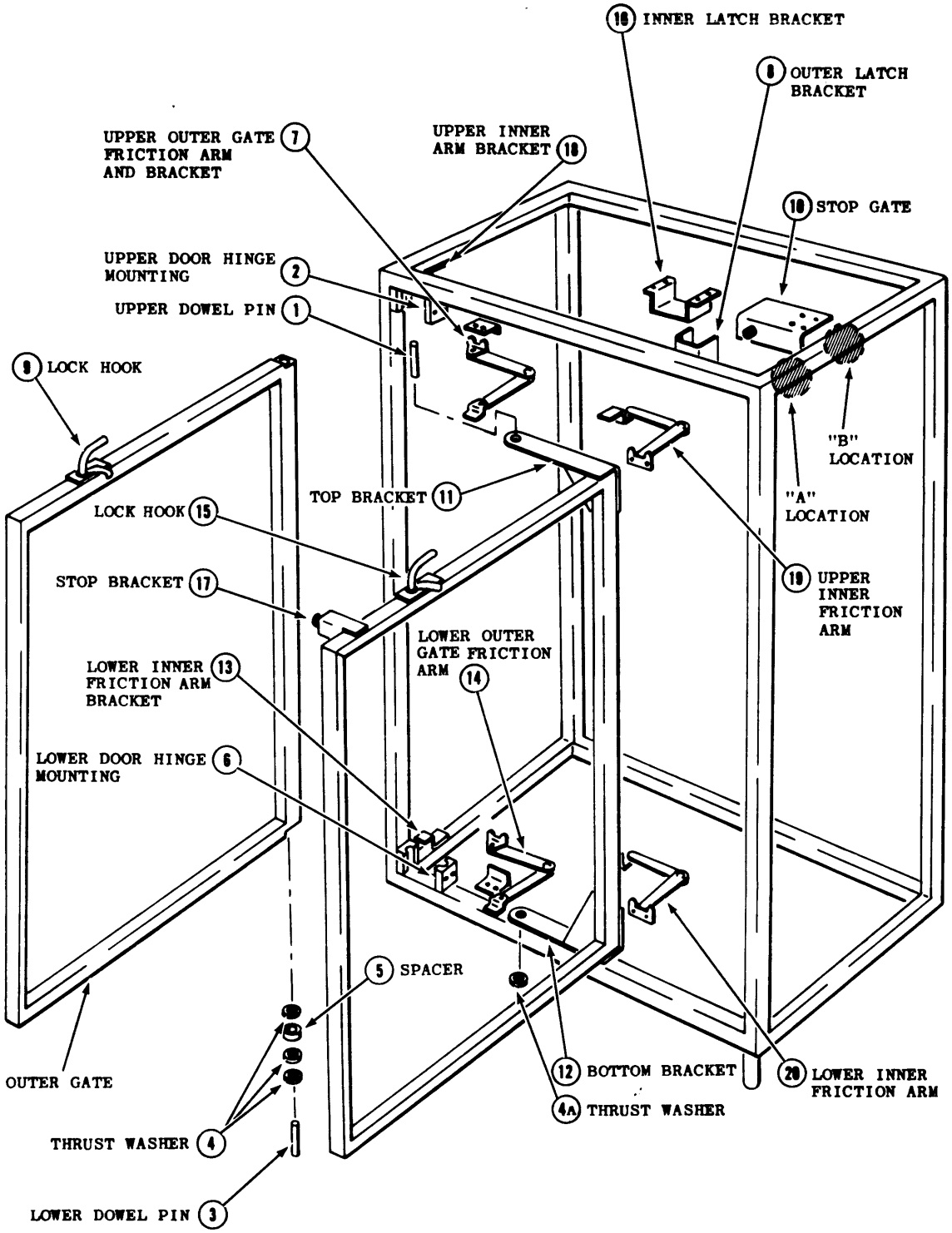


FIGURE 5.7-1 INNER AND OUTER GATE ASSEMBLIES

9. Position the lower part of the gate into position to allow replacement of the lower door hinge mounting (6).

10. Install upper and lower stop bracket (17) on the inner gate.

11. Position the top and lower inner gate brackets to a suitable angle to allow moving the new gate into position to bolt it to the brackets.

12. Move the gate into position against the brackets using blocks to support the weight after aligning the holes for the bolts. Install bolts and tighten.

13. Install the inner friction arm bracket (18), the upper inner friction arm (14), the lower inner gate friction arm bracket (18) and the inner lower friction arm (20).

14. Install the inner gate lock hook (15).

15. Install the inner gate latch bracket (16).

16. Move the stop gate (10) from location "A" to location "B".

17. The physical mounting of the new gate is now complete.

Cable Hook-Up And Power "ON" Check

Refer to Figures 5.2-1 and 5.2-2 for additional cable installations. Also refer to Section 5 of the Technical Manual associated with the unit installed for cable hook-up and POWER-ON checks. Check the set and re-set of all indicators and the operation of the maintenance switches.

SECTION 6

CIRCUIT ANALYSIS

6.1 NEON SWITCH - DRIVER INDICATOR

NEON DRIVER ASSEMBLY (FIGURES 6.1-1 AND 6.1-2)

The neon driver, neon indicator, and set switch are all included in one self-contained assembly. This method of assembly saves space and simplifies the wiring as compared to having the drivers mounted on separate cards. The neon driver furnishes power to light the neon, yet is a very small load on the FF. The neon will light when its flip-flop is in the ON state. A SPDT switch is included for setting the flip-flop on or off, and for clearing.

The neon driver (ND) consists of a single transistor (Figure 6.1-1). Pin 7 of the ND is connected to pin 22 of a flip-flop. If the flip-flop is off, pins J-0/5, W-0/5 will be false or zero volts; the base of the driver transistor will be false; therefore the transistor will be cut off. Pin 4 is -120V and goes to the neon through a 200K resistor. The other terminal of the neon is connected to the transistor, and through a 22K resistor to -100V on pin 5. With the transistor cut off, there will be a 20V difference across the neon. A NE-2E neon requires about 70V to fire, so the neon will be off.

If the flip-flop is on, pins J-0/5, W-0/5 will be true; the base of the driver transistor will be true and the driver will be conducting. Current can now flow from -120V, through the 200K resistor, the neon, and the driver transistor to -1.2V. This, in effect, puts -120V on one side of the neon circuit and -1.2V on the other, and the neon will be on.

Figure 6.1-2 is a simplified diagram of how the neon set switch is connected. As used in this system, the switch has three functions: to set, reset, or clear a flip-flop.

To set a flip-flop, the Master Set/Reset switch must be in the Set position. This will make +100V available at the N/O contact (Pin 6) of the neon switch. When the switch is closed, the positive voltage will go through pin 2 to the base of Q4 in the flip-flop. This positive voltage will turn Q4 off. When Q4 is off, the flip-flop is in the ON state.

To turn the flip-flop OFF, the Set/Reset switch must be in the reset position. This makes -100V available to the N/O contact. When the switch is closed, this negative voltage will go to the base of Q4, turning it on. When Q4 is on, the flip-flop is off, or reset.

The Master Clear switch is connected to pin 9 of all the neon indicators. When the Clear switch is closed, -100V goes through the N/C contacts of the neon switches to the base of Q4. The flip-flops will all be reset or cleared.

The high voltages used in this circuit (-100V and +100V) are necessary because of the high-impedance load. The input to the flip-flop is through a 51.1K resistor. This high impedance will help isolate the base of the flip-flop transistor from any noise picked up on the line going to the neon switch.

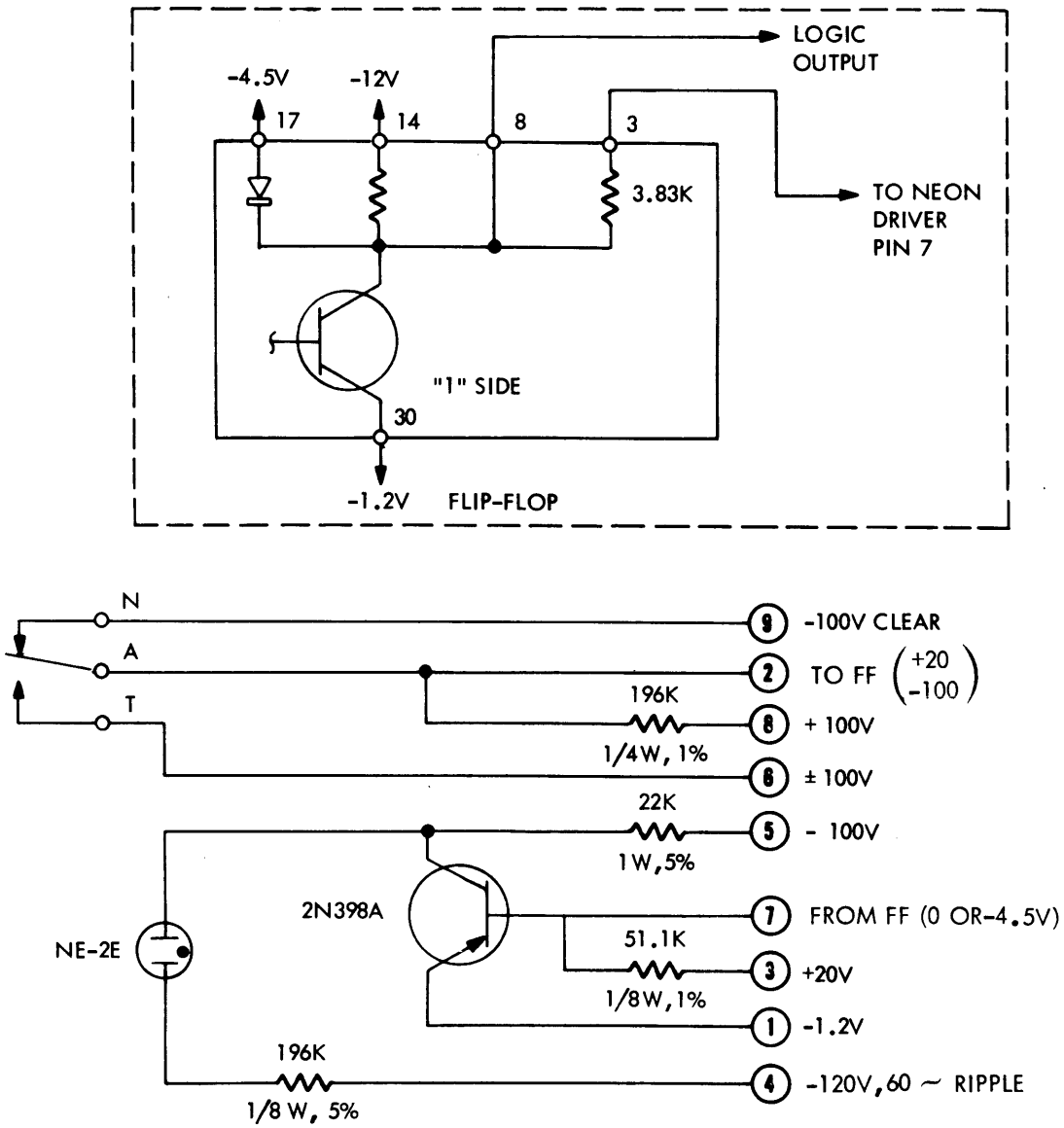


FIGURE 6.1-1 NEON DRIVER ASSEMBLY

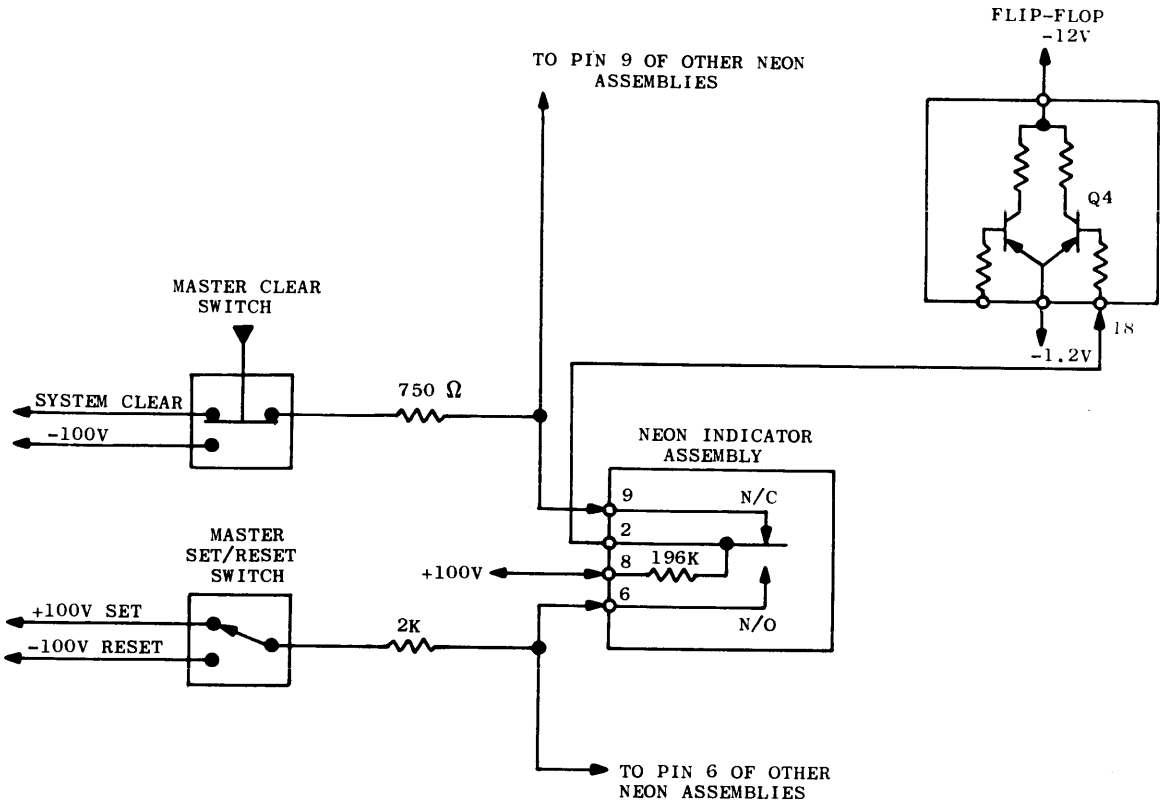


FIGURE 6.1-2 NEON DRIVER ASSEMBLY SET SWITCH

6.2 SWITCH L

INTRODUCTION

The switch is an active element in current steering diode logic circuitry. Switches are used for power gain (DC restoration) or logic inversion. Because of the circuit and logical requirements (i.e., load handling and switching speed), three types of switch circuits and parallel plate packages are required. There are five individual switch circuits in each parallel plate package, and they are all of the same type. The three types are: Low Speed, High Speed-High Current, and High Speed-Low current.

LOW SPEED (LS) - DRAWING C-77172

The circuit of Figure 6.2-1 is the first switch circuit on drawing C-77172 and is connected to representative input and output circuitry.

CR26 and CR1 are Type 5 diodes (stabistors). The stabistor is a silicon diode that maintains a forward drop of .5V to .7V for currents of 100 μa to 1 ma, respectively. The combined forward drops across CR26 and CR1 establishes 1V of cutoff bias or noise threshold when the input is false. A false input is established when QX of the driving element is conducting (in saturation). QX shunts the current through Rg away from the input terminal. The false input voltage is the forward drop across X1 plus the collector voltage of QX less the forward drop across X2. By specification, the forward drop across X1 can be no more than .3V. Likewise, the collector voltage of QX can be no more than .3V. The forward drop across X2 is .1V. Therefore, the input voltage (false) is a maximum of -.5V. Ideally, the false input voltage for this gate configuration is -.2V to -.3V.

With a -.3V to -.5V input, and an assumed ICBO of 20 μa, approximately 140 μa is flowing through X2, CR26, CR1, and R2 to the +20V Supply. This is sufficient current to maintain .5V across the stabistors. Q1 is held cutoff by the +.8V to +.5V at its base. The voltage at the collector of Q1, and the output is very close to -12V. When Q1 is cutoff, the current through R24 is due to ICBO in Q1 and the reverse currents in X3, X4 and X5. These currents are in the order of microamperes and produce a very small drop across R24. A voltage more negative than -3V is "true". Therefore, the output is true. The input is inverted.

The resistance of base-resistor R2 is selected to provide a balance between two circuit requirements.

1. Temperature stability gained by providing a minimum resistance path for ICBO.

2. Prevent shunting more than 180 μa of the available base drive when the switch is on (Q1 conducting).

A true input is produced when QX is cut off. This back biases X1 and causes the current through Rg to be steered into the switch. The input terminal tries to go to -9V, but the forward-biased base-emitter junction of Q1 clamps the input

voltage at -1.5V. The -1.5V is the result of the forward drop across CR26 and CR1 plus the base-emitter drop (.6V+ .6V+ .3V = 1.5V). Q1 conducts to saturation and the output is -.3V to -.1V (false).

When the input to the switch is true, the base current of Q1 is equal to the current through Rg (.87 ma) less the current shunted through R2 (.17 ma). Base current is .7 ma. The Type F transistor has a minimum DC beta H_{FE} of 35. Collector current is equal to base current (.7 ma) times H_{FE} (35) or 24.5 ma. The current available to the load is the collector current (24.5 ma) less the current through R24 (3.5 ma) or 21 ma. It is apparent from this discussion that the load handling ability of the switch is determined by the DC beta of the transistor, and the available base current which is determined by the input gate configuration. The Type F transistor has a minimum DC beta specification of 35. Therefore, additional load current is obtained by increasing base current. Base current is increased by paralleling Rg with one or two additional standard 12.1K resistors. The Low Speed Switch can handle loads up to 50 ma.

"ON" TO "OFF" SWITCHING TIME

Turn-off time is measured from the time QX conducts (forward biasing X1 and steering current away from the input terminal) to the time when output voltage reaches -3V. The factors which affect switching time are:

1. The discharge time of input capacity (CI).

2. The time required to neutralize the stored charge in the base of Q1.

3. The time required to charge the output capacity (CO) to -3V.

Since the input voltage swing is approximately 1V, keeping the input capacity (CI) as small as possible minimizes its effect. The Type 5 diode (CR26 and CR1) has a minimum of 600 μμ coulombs stored charge. This closely matches the stored charge in the Type F transistor base and minimizes its effect. The output capacity (CO) must charge through R24. The resistance of R24 (3.6K) is chosen to be as small as possible without causing excessive loss of load current when Q1 is conducting.

The maximum turn-off time of the Low Speed Switch is 5 μs with Rg = $\frac{12.1K}{3}$.

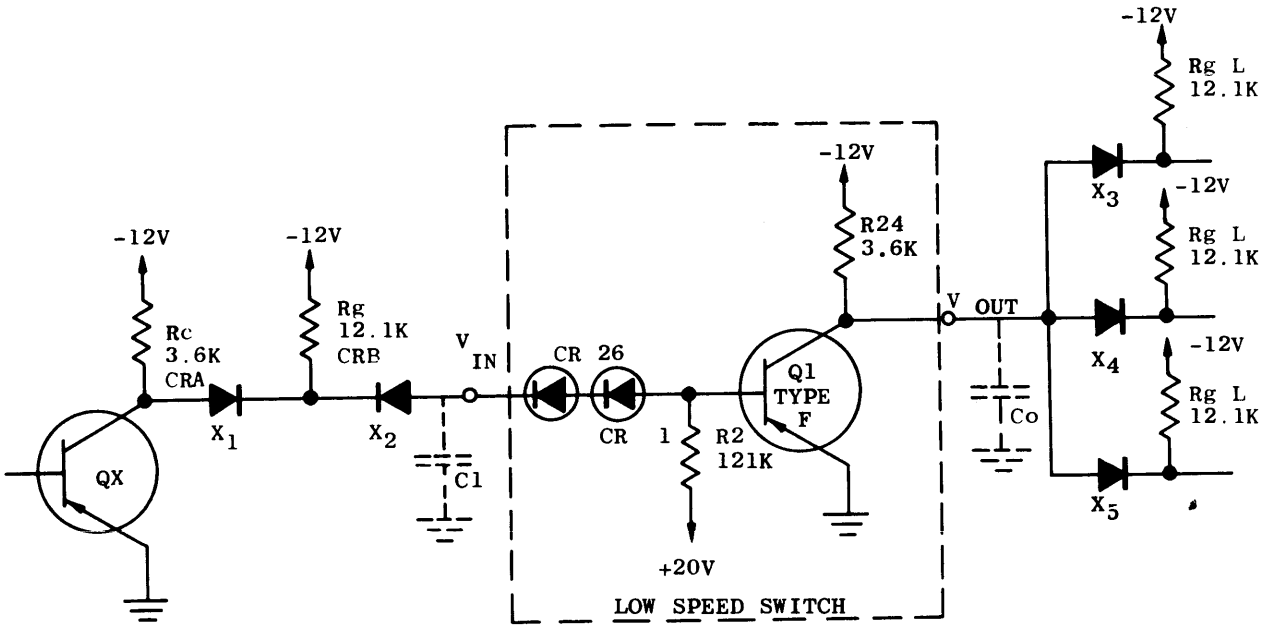


FIGURE 6.2-1 LOW SPEED SWITCH

6.3 KPK RELAY

Refer to TM B 5370.51, Section 6.19-1 for circuit analysis of package 11900453.

SECTION 7

FUNCTIONAL DESCRIPTION

7.1 GENERAL

In order to provide maintenance facilities for the field engineer and permit the programmer to have access to the various flip-flops of the system for debugging of machine routines, the neon indicators and maintenance control switches have been grouped together in the Display and Distribution Cabinet.

This cabinet contains a display panel for each of the two Processors, four Input-Output units and Central Control.

The front of the cabinet has two swinging racks. The first rack contains a panel for Central Control, Processor A, I/O-1 and I/O-2. This will provide panels for a basic system. If a larger system is used, the second rack holds the panels for Processor B, I/O-3 and I/O-4. In the rear of the cabinet is a fixed panel which is used as a terminal board in connecting the Power Supply to the system. Cable connections are also provided for peripheral equipment.

The Power Fault Panel is located on the bottom of the first gate to provide an indication of Power Supply troubles.

The cabinet has a cover which must be removed for access to the panels. An interlock switch removes the voltage from the neon indicators when the cover is installed.

Refer to Section 2 for a description of the indicators and switches associated with each maintenance panel.