SECTION D

THE SPECIAL COMMANDS

This section requires a reasonable understanding of previous sections, although back references are given to assist the reader's memory. Little description is devoted to optional auxiliary equipment which is associated with certain commands, since such equipment is a study in itself and is documented in other literature.

THE SPECIAL COMMANDS-GENERAL

D-1a The SPECIAL COMMANDS are those in which DESTINATION 31 is selected and the SOURCE number, and sometimes CHARACTERISTIC, define the operation to take place during the time of TRANSFER. Drawing 3 lists the operations.

D-1b SPECIAL COMMANDS with a SOURCE number less than 16 all initiate INPUT-OUTPUT operations and will be discussed in sec. F. In this section SPECIAL COMMANDS with SOURCE numbers equal to or greater than 16 will be discussed.

D-1c "DS": A CONTROL SWITCH (dwg. 23) signal common to all SPECIAL COMMANDS is DS ("DESTINATION SPECIAL"). DS = TR·D7·DX, hence is a special case of TRANSFER. This signal ordinarily activates all SPECIAL COMMANDS by qualifying the appropriate gates. This will become apparent as SPECIAL COMMANDS are analyzed.

SOURCE 16: HALT

D-2 DS·S4·SU resets CH causing the computer to idle indefinitely in the WRC state after TR is terminated. (ref. Dwg. 30-upper left and sec. C-20e).

SOURCE 17: RING BELL, ETC.

D-3a SOURCE 17, RING BELL: DS·S4·SV (see dwg. 23 right) is applied to the grid of a relay puller tube (V12 in the LOGIC PANEL - RELAY SECTION - dwg. 62) during the time of TRANSFER. If TRANSFER lasts 108 word times (approximately 30 milliseconds), RY1 will pull in and its points will complete the circuit to energize the bell solenoid. The command should be immediate with T = L+1. Considering the electro - mechanical requirements of the hardware associated with the bell, three drum cycles should elapse between repeat executions of this command.

D-3b SOURCE 17·CH=1, RING BELL and ⟨MAN PUNCH⟩ TO TEST: (dwg. 30-left) DS·S4·SV·① arises during TR, interrogating the ⟨MAN PUNCH⟩ signal. ① = $\overline{CX}$·CW (char. =1). ⟨MAN PUNCH⟩ is a signal which is high if the PUNCH SWITCH on the typewriter is in the ON position. If the punch switch is ON, DS·S4·SV·① · ⟨MAN PUNCH⟩ will set CQ and the next command will be read from WT =N+1. The bell will ring if TR lasts 108 word times; if TR is programmed to last only one word time the bell will not ring but the test will take place. (1 word time = approximately 270 microseconds, which is insufficient to activate the bell circuit relay or the bell).

D-3c SOURCE 17·CH=2, RING BELL AND START INPUT REGISTER: DS·S4·SV·② is coupled to a connector into which an INPUT-OUTPUT REGISTER accessory may be plugged (see dwg. 23-right). This signal, high during TR, is for the purpose of controlling the above accessory, but can be used to control other types of external accessories.

D-3d SOURCE 17·CH=3, RING BELL AND STOP INPUT REGISTER: DS·S4·SV·③ is coupled to a connector, etc. (see D-3c).

SOURCE 18: TRANSFER M20·ID to OUTPUT REGISTER

D-4 This operation supplies M20·ID to an output connector during the time of TRANSFER, providing DS·S4·SW is present. The signal to output is DS·S4·SW·M20·PJ, where PJ is ID's output flip-flop. In addition to this, WRITE PULSE is supplied to the connector, by itself and also qualified by DS·S4·SW·PJ. If the INPUT-OUTPUT REGISTER accessory is connected, the above hardware (dwg. 23-right) supplies it with LINE 20 data and WRITE PULSES under control of ONES in the ID REGISTER.

SOURCE 19: DA-1 CONTROL

D-5 Ref. Dwg. 23 - right: DS·S4·SX·④ and DS·S4·SX·① are sent to a connector into which a DA-1 (DIGITAL DIFFERENTIAL ANALYZER) may be plugged. SOURCE 19·CH=0 STARTS the DA-1; SOURCE 19·CH=1 STOPS the DA-1.

SOURCES 20 and 21: SELECT COMMAND LINE, MARK EXIT, AND RETURN EXIT

D-6a These commands frequently are programmed as a pair and serve to set up new command lines in addition to other operations.

D-6b Commands are read during the RC state from one of eight possible COMMAND LINES (00, 01, 02, 03, 04, 05, 19, and 23). The particular line which supplies the commands is a function of three flip-flops: CD1, CD2, and CD3. The three flip-flops, once set up in a particular configuration, will remain in that configuration until changed by programming or by manual control. Therefore, commands will emerge from the same line until another line is established by changing the configuration of the CD flip-flops.

D-6c The CD flip-flops are shown on Drawing 22-bottom. Above them are eight gates supplying $\overline{MC}$, the inverted command information from the false side of the selected command line. Which gate is qualified, hence which line supplies commands, is a function of the CD's.

D-6d When either SOURCE 20 (RETURN EXIT) or SOURCE 21 (MARK EXIT) is programmed, DS·S5·C8 appears during TRANSFER, setting the CD's in accordance with the contents of CX, CW, and C1, which are the CHARACTERISTIC and S/D bits in the 13 STATIC FLIP-FLOPS. Hence a new command line may be established by the CH and S/D bits as shown on Drawing 32 (lower left). Other signals originating in switch contacts can control these flip-flops (see secs. E-6, E-7, E-11d and G-2m). In addition to the command line selection function, these two commands perform other functions as follows:

D-6e SOURCE 21, MARK EXIT: (Ref. dwg. 32). This command, during the time of TRANSFER, blocks recirculation of the COMMAND REGISTER AUGEND term during pulse periods T2-T13, effectively loading this portion of CM with ZEROS. T1·DS·S5·SV sets CJ; T13·CJ·(TR+CQ) resets it. CJ·DS·S5·SV blocks CU. The reader may recall that CJ has other functions (sec. C-18k-n); this does not prohibit its use in this capacity since the different functions are isolated by a barrier of time.

D-6f If the MARK EXIT command is written as deferred, TRANSFER takes place during WT=T only, regardless of the S/D bit of the command.

(TR_r = DS·S5·SV·T29-ref. sec. C-18g and dwg. 30.) This allows the S/D bit to equal 1 or 0 (in accordance with the desired number of the new command line to be selected) without influencing the TRANSFER state.

D-6g Since CU was rendered equal to zero during TR, and TR occurred during WT = T, then CU = 0 at WT = T. T1 unconditionally sets the COMMAND REGISTER CARRY FLIP-FLOP (CC) every word time adding a ONE to the lowest order bit (T2) of this newly established AUGEND. Hence, during WT = T, the sum (CA) equals 1. During the next 107 word times 107 carries will be added to this number (CC_s=T1) and at WT=107 a CORRECTIVE 1940 will enter the ADDEND (CD) from the NUMBER TRACK (CN) yielding a total of 2048. This sum equals 2^{11} and will appear as (1) all ZEROS in the T2-T12 positions of the COMMAND REGISTER line and (2) an END CARRY at T13 time of WT = T-1 of the drum cycle following the MARK EXIT command. Furthermore, this T13·CC will exist at WT = T-1 during every drum cycle thereafter until another MARK EXIT command establishes a new "MARK".

D-6h SOURCE 20, RETURN EXIT: (ref. dwg. 30-top) When this command is read, during the time of TRANSFER it will perform its command line switching function. However, when it comes to establishing the next READ COMMAND state, an additional gate can set CJ to permit the next T29 pulse (TR_r+T29·CL·CK) to initiate RC. This new gate is qualified by T13·CC·CJ·D7·DX·S5·SU and allows the T13·CC, established by the last MARK EXIT command, to initiate RC instead of the usual T21·CC. That is, the next command will be read during WT = T of the last MARK EXIT command instead of WT = N of the RETURN EXIT command.

D-6i The above will take place provided the MARK EXIT and RETURN EXIT commands are constructed as illustrated on Drawing 32.

D-6j If the previous MARK EXIT command had been written as IMMEDIATE, the T13·CC would have occurred during WT = L of the MARK EXIT command (as a function of TR), hence the command following the RETURN EXIT would be read during WT = L+1 of the MARK EXIT command. (The T number of an IMMEDIATE MARK EXIT command can be anything; however TR will last only one word time since TR_r=T29·DS·S5·SV.)

D-6k The T13.CC will initiate RC following a RETURN EXIT only if the T21·CC does not initiate it first. Relative timing of these two CARRIES will determine the location of the next command. When N of the RETURN EXIT command = L+1, T13·CC initiating RC prior to T21·CC is inevitable.

D-6l A RETURN EXIT command should not have its BP bit =1. This will serve to prevent T21·CC from initiating the next RC state (see sec. C-20); however, it will not prevent T13·CC from doing so. If T13·CC initiates RC, the state of CZ and CH will prevent T21·CC established by the new command from initiating the RC state to follow, effectively postponing the stop by one program step. Also, if relative timing of T13·CC and T21·CC is such that T21·CC is intended to precede T13·CC and initiate RC during WT = N of the RETURN EXIT command, the state of CZ and CH will block T21·CC to initiate RC regardless of sequence. This would mean that a program could proceed in one way with the COMPUTE SWITCH on "GO" and another with the COMPUTE SWITCH

on "BP". SINGLE CYCLING (sec. E-5) will also give rise to this problem for the same reason. The solution is: 1) do not place a BP in a RETURN EXIT command and 2) do not SINGLE CYCLE a RETURN EXIT command unless fully aware of all possible results.

SOURCE 22: SIGN OF AR TO TEST

D-7 If this command is programmed, it will cause the next command to be read from WT = N+1 if a negative number exists in AR. This is accomplished by DS·S5·SW·T1·AR setting CQ (ref. dwg. 30-left and sec. C-19).

SOURCE·23 CH=0: CLEAR MQ, ID, PN and IP FLIP-FLOP

D-8 DS·S5·SX·④ blocks recirculation of the three two-word lines and resets the IP flip-flop (ref. dwg. 36). TRANSFER must last for two word times to block recirculation of the lines for a complete recirculation cycle. Exactly when these two word times take place makes no difference.

SOURCE 23·CH=3: PN·M2 to ID and PN·$\overline{M2}$ to PN

D-9a (Ref. dwg. 36) This command causes two separate concurrent "extract" operations:

1) PN·M2 to ID: This requires blocking ID recirculation and application of PN·M2 to the ID writing circuit. DS·S5·SX·③ accomplishes the former, DS·S5·SX·③·M2·PP accomplishes the latter. (PP is the READ FLIP-FLOP of the PN register).
2) PN·M2 to PN: This operation can be described as blocking recirculation of PN if M2 is high. DS·S5·SX·③·M2·PP accomplishes this.

D-9b The operations performed by the command facilitate efficient DECIMAL--BINARY conversion routines, but may be used to advantage for sorting purposes in any program.

SOURCE 24 : MULTIPLY

D-10a MULTIPLY may be considered an automatic sub-routine built into the computer hardware. The purpose of the sub-routine is to form a fractional product (in PN) from a fractional multiplicand (in ID) and a fractional multiplier (in MQ). The binary point, for this purpose, must be considered to the left of the highest order bit (T29·$\overline{CE}$) in these registers.

D-10b The sub-routine involves the addition (accumulation) of: $(ID_o \times 2^{-1}) \times 2^{-1}$ of MQ_o + $(ID_o \times 2^{-2}) \times 2^{-2}$ of MQ_o ··+ $(ID_o \times 2^{-n}) \times 2^{-n}$ of MQ_o, these values being accumulated in the PN adder to form a product. The hardware is shown on Drawing 36 and an example on Drawing 37.

D-10c In order to obtain $(ID_o \times 2^{-n})$, a means of shifting the contents of ID to the right one bit each recirculation time is provided (i.e. ID shifted right one bit = ID x 2^{-1}, two bits = ID x 2^{-2}, three bits = ID x 2^{-3}, etc.).

D-10d The means of shifting ID is shown on Drawing 36 (left). The PJ flip-flop reads the contents of ID one recirculation time after it is written

(57 +1 = 58 pulse delay) and is considered to be the "OUTPUT FF" of the line. If PJ is the writing term of ID (normal recirculation), information in the line is synchronized such that every recirculation time it is written in the same place relative to the time reference. If, however, PI is coupled as the writing term instead of PJ, information will be written one pulse-period in advance, meaning that bits will be recirculated out of phase with the time reference resulting in the information being advanced one bit each recirculation cycle.

D-10e This principle, known as PRECESSION, effectively shifts the number in ID to the right (relative to this right-to-left time axis) one bit every two word times. This particular case may be referred to as a "ONE BIT PRECESSION TO THE RIGHT".

D-10f Note that $\overline{TE}$ qualifies PI when it is the writing term. This means that during TE (sign position of double precision words), nothing but a ZERO can be "written". 57 pulse periods later ($T29 \cdot \overline{CE}$), PI will read this ZERO. In effect, this $\overline{TE}$ qualifying term inserts ZEROS into the highest order end of the word as it is shifted to right; bits at the lowest order end of the numerical portion are lost as the number shifts right. Drawing 37 illustrates this in terms of a ten-bit example.

D-10g Note in the example on Drawing 37 that even though ID_o and MQ_o contain single precision numbers, the PRODUCT acquires numerical bits below the lowest order numerical bit position of PN_{odd} (i.e. $T2 \cdot \overline{CE}$). If a subsequent single precision command transfers only PN_{odd} to memory, the PRODUCT sign bit stored in IP will be substituted for the numerical bit in $T1 \cdot \overline{CE}$ of PN in the INVERTING GATES during TRANSFER (ref. D-10p and Drawing 34).

D-10h As a result of the PRECESSION circuit mentioned above, ID times 2 to reducing powers is available to be accumulated in the PRODUCT REGISTER (PN) in accordance with the MULTIPLIER (MQ) data. A means must be provided to interrogate the bits in MQ corresponding to these powers of 2 for the purpose of controlling the additions of ID x 2^{-n} in the PN register.

D-10i The means of interrogating MQ bits, starting with the highest order bit (2^{-1}), also involves precession. Ref. Drawing 36: The contents of MQ can shift to the left by virtue of delay flip-flop PQ. During a multiplication, normal recirculation of MQ is blocked and another recirculation path including a one bit delay (provided by PQ) is substituted. The result of this is that information from the reading station is re-written after a 59 pulse delay, effectively shifting it one bit position to the left relative to the right-to-left time axis each recirculation cycle. This may be called a "ONE BIT PRECESSION TO THE LEFT".

D-10j $\overline{TE}$ qualifies the writing term when this precession path is connected. This means that at TE time a ZERO is written each recirculation cycle, effectively inserting zeros in the lowest order end of the number each time it shifts to the left one bit. Furthermore, this means that as the number shifts to the left, the highest order bit is shifted "out of the end" of the line and lost.

D-10k The PM FLIP-FLOP monitors the highest order bit of MQ (at $T29 \cdot \overline{CE}$ time) at the end of each recirculation cycle. Timewise, PM will register,

for a 2 word time duration, each MQ (multiplier) digit starting with 2^{-1}.

D-10l Whenever the highest order MQ bit is a ONE after a shift, ID x 2^{-n} will be applied to the ADDEND of PN, hence accumulated in the product (PD= PM·PI·DS·S6·C8·C7·TE). In the event of a multiplier bit equal to ZERO, no addition takes place. After the last (lowest order) MQ ONE bit has performed its ID x 2^{-n} addition function, the product is complete. If a non-ZERO number existed in PN prior to the multiplication, it would be included in the product. Sometimes this is convenient; at any rate, programming will determine the initial contents of PN.

D-10m The "T" number in a multiplication command is interpreted as being RELATIVE (sec. C-17p). If T = 114, this allows 57 MQ bits to be interrogated (114 WT's = 57 two-word recirculation cycles) hence will form a complete product in accordance with a double precision multiplier up to and including the lowest order MQ numerical bit (T2.CE). If the multiplier is a single precision number, only 28 numerical MQ bits need be interrogated and T may be equal to 56 with no loss in product precision. Furthermore if the multiplier is a constant, interrogation of MQ bits need only proceed to include the lowest order ONE bit. (e.g., if the lowest order one bit is in the 2^{-5} location, only 5 iterations are necessary and T may equal 10 with no loss in product precision - each iteration requires 2 word times, the recirculation time of a two-word line.) (T2·CE)

D-10n The MULTIPLY command must be located in an odd word time so that the first word time of TRANSFER takes place at an even word time, the beginning of a recirculation time of a two-word line. The command must be IMMEDIATE and T must be an even number to assure termination of TRANSFER at the end of a two-word line recirculation cycle (odd word time). The CH and S/D precision bits can contain anything since they do not control anything associated with multiply; normally these bits are ZEROS. (SOURCE and DESTINATION contents obviously must be 24 and 31 respectively.)

D-10o Round-off: Should the total number of significant MQ and ID bits exceed 57, the lowest order end of PN will be inaccurate in that bits from ID x 2^{-n} will be lost from the lowest order end of ID. This form of round-off is not conventional and should be recognized by the programmer.

D-10p The sign of the product is not included in PN but is held in the IP FLIP-FLOP. When the product is transferred from PN to memory with a TR or TVA characteristic, the sign in IP will be attached to the absolute value of the product (sec. C-13). A multiplication overflow is impossible since the product of two fractional numbers will always be fractional.

SOURCE 25 : DIVIDE

D-11a DIVIDE, like MULTIPLY, is an automatic sub-routine built into the computer hardware. The sub-routine obtains the ratio of two numbers and inserts it, bit-by-bit, into the MQ. The operation is: NUMERATOR (PN) ÷ DENOMINATOR (ID) → QUOTIENT (MQ). The quotient may only approach 2 in magnitude (i.e., 1.11111---1). For this reason the ratio of PN to ID must be less than 2 (i.e. PN/ID<2 or PN<2ID is a requirement of the input data).

D-11b A DIVIDE command may be written in several ways as far as TRANSFER timing is concerned depending upon the form in which the quotient is desired. These are outlined on Drawing 40 - lower right.

D-11c Cases involving T = 57 or 116 are most frequently used since the binary point exists in a conventional location. PN must be < ID to assure that the quotient (MQ) will be fractional; an integral bit (2^0) constitutes an overflow in these cases and will be detected (sec. D-11ae).

D-11d Cases involving T = 55 or 114 have their programming virtues. In these cases, if PN/ID≥2, a useless quotient will result; furthermore, no overflow indication will exist (i.e., FO FLIP-FLOP). The virtue of these cases exists in the accommodation of one integral bit (2^0).

D-11e In all cases the quotient information replaces the original contents of MQ as indicated on Drawing 40. The final sign bit (T1·CE) will = 0 and the quotient will be in terms of absolute value.

D-11f In all cases command information must include I/D = 0, CH = 1, S = 25, and D = 31 to define the command. BP and N will be programmed as in any other command. LOCATION of the command must be an ODD word time.

D-11g The S/D bit can contain anything since other terms in the STATIC PORTION of the command assure that TS = TE regardless of the S/D bit (see dwg. 15: $\overline{S6 \cdot SV \cdot DS}$, low during DIVIDE, forbids generation of TS at T1.CE time even though $\overline{C1}$ calls for it. $\overline{C1}$ means S/D bit = 0 = single precision.) If the DIVIDE command calls for only a single precision quotient, the iterations involved in its formation are nevertheless dealing with double precision registers and the timing must be controlled accordingly.

D-11h The division algorithm employed by the G-15 is essentially a standard one with certain deviations to minimize the electronic control circuitry. Drawings 38 and 39 illustrate the evolution of the system employed. Drawing 38 figure (A) illustrates "long division" in binary, using the method analagous to the decimal system taught in grade school. At the extreme left of figure (A) is the abbreviated version of the division; to the right is the same example, iteration-by-iteration. Insignificant ZEROS are shown as solid lower-case ZEROS and account for 12 binary places. Associated with this example are algebraic notations and orders of magnitude as an analysis of the proceedings.

D-11i As the notations suggest, the denominator (ID) times 2 to decreasing powers is subtracted from the numerator (PN) to achieve minimum positive remainders. Whenever ID x 2^{-n} can be subtracted from the previous remainder rendering a positive remainder, a ONE representing 2^{-n} is put in the quotient. Whenever ID x 2^{-n} cannot be subtracted from the previous remainder without yielding a negative remainder, the subtraction is by-passed (shown as subtraction of ZEROS), and a ZERO appears in the quotient corresponding to 2^{-n}.

D-11j This system depends upon an inspection to determine the relative magnitudes of ID x 2^{-n} and the remainder from which it will be subtracted in order to determine the feasibility of the subtraction to follow. This cannot be done by the computer without actually performing a subtraction to determine whether the remainder will be positive or negative.

D-11k Therefore, the algorithm in figure (B) is considered. This does not involve inspection of magnitudes followed by subtraction or no subtraction, but instead involves both additions and subtractions of ID x 2^{-n} from PN. The remainders are both positive and negative. The sign of each remainder determines the following:

+ remainder : 2^{-n} quotient bit = 1
next operation will SUBTRACT ID x 2^{-n-1}

- remainder : 2^{-n} quotient bit = 0
next operation will ADD ID x 2^{-n-1}

D-11l In this case, the same quotient is developed as in the first case (fig. A) and the positive remainders are the same. This may be confirmed by inspection of the algebraic notations.

D-11m Note that once an all ZERO remainder is established, all remainders to follow must be negative since $[- ID \times 2^{-n} + ID \times 2^{-n-1} + ID \times 2^{-n-2} - - - + ID \times 2^{-n-m}]$ can never be positive; hence all quotient bits developed following a ZERO remainder will be ZEROS.

D-11n The reader will note that in both figures (A) and (B) insignificant ZEROS account for a great many of the bit locations. Therefore a system illustrated in figure (C) will be considered. This system involves multiplying each remainder by 2 and not multiplying ID by 2 to reduced powers. Hence the denominator, unchanged, is either added to or subtracted from 2 times the preceding remainder. This keeps orders of magnitude of the factors approximately in the same range without altering the signs of the remainders. The only difference between remainders in figures (B) and (C) is a scaling factor which is compensated for by adjustment of the ID scaling factor. In this system, bit locations need not be allotted in wholesale quantities to insignificant ZEROS. This implies more efficient use of registers hence greater precision capabilities of registers of fixed length.

D-11o This last algorithm is the basis of the G-15D division system. However, the G-15D does not have a subtractor. Furthermore, a sign bit must be considered. Therefore the algorithm must be adapted to the arithmetic system in use and the circuits available.

D-11p Drawing 39, fig. (D) is a proposition for performing the algorithm illustrated on Drawing 38, fig. (C), but performing subtractions by adding COMPLEMENTS of ID. A sign bit is located to the left of the highest order (2^o) bit position. (The sign bit of the two-word registers occurs at T1.CE which follows directly the highest order numerical bit, T29·$\overline{CE}$).

D-11q An integral (2^o) position is allowed in the example on Drawing 39, figure (D) to accommodate shifted negative remainders (i.e., r x 2) which can approach 2 in absolute value (see dwg. 38, fig. (C) - orders of magnitude). Note that in the proposition on Drawing 39, fig. (D), the 2^o bit and sign bit of each unshifted remainder are always alike. It can be proved that this will always be the case (considering the fact that signs of augend and addend are opposite and the absolute value of any augend cannot exceed twice the absolute value of its associated addend).

D-11r Since the integral and sign bits in the unshifted remainders will be alike, they can occupy the same bit position as shown in Drawing 39, figure (E). In terms of the PN, where this arithmetic takes place, T29·$\overline{CE}$ is the location of the highest order fractional bit (2^{-1}) and T1·CE (= TE = TS) is the location of the "combination" sign and integral bit.

D-11s For the sake of division analysis, consider the sign bit of a number as following the number rather than preceeding it. There is no sign position at the beginning of the number associated with that number. Consider the iteration cycle displaced from a standard two-word recirculation cycle by a factor of one bit period (i.e., the iteration cycle starts at T2·CE, not T1·CE). Drawing 39, figure (G) illustrates this concept.

D-11t Note that in Drawing 39, figure (E), when the remainders are shifted left one bit (multiplication by 2), they still appear in the same form as they did prior to shifting (i.e. NORMAL or COMPLEMENT) except in the cases noted "N". These cases result when a negative remainder in complement form exceeds a fractional magnitude when shifted and an overflow exists. The shifted remainders in these cases resemble numbers in NORMAL form since their sign bits = 0; they are nevertheless COMPLEMENTS. When the addend is applied to such a number, END CARRY behavior compensates for the overflow and yields the next remainder in correct form.

D-11u This system (fig.E) would be that used in the computer except that the sign bit associated with each unshifted remainder must be reversed. This SIGN BIT decides whether an addition or subtraction will take place in the next iteration (sec. D-11k) by controlling the IS FLIP-FLOP in the INVERTING GATES. The contents of ID, being applied to the EARLY BUS, will arrive on the LATE BUS (hence the PN addend) either in COMPLEMENT or NORMAL form in accordance with the orientation of IS.

D-11v At TE (sign) time, the remainder sign (TE·PA) is applied to the EARLY BUS and consequently controls IS in accordance with the rules of the ADD characteristic (programmed in the command). This means a "1" in the sign bit of the sum (PA) will set IS, complementing ID for use as the next addend, hence performing a subtraction. This is the exact opposite of the desired results. Therefore, the sign bit of every remainder is purposely reversed. This is accomplished by applying the wrong sign bit to each addend (i.e. 1 for +, 0 for -). Drawing 39, fig. (F) illustrates this arrangement.

D-11w Fig. (G) illustrates fig. (F) in terms of the time axis. This six-bit example illustrates the activity in the 58 bit register actually used. Note that the first iteration unconditionally involves a subtraction since the EB bit at the first pulse period during TRANSFER is a ONE as a function of the starting data.

D-11x During every iteration the IS flip-flop in the INVERTING GATES will remain set or reset as a result of the sign of the previous remainder. The setting of IS controls the following items:

Positive remainder, IS is high.

1) Supply the numerical portion of ID, COMPLEMENTED, to PN as ADDEND (for subtraction)
2) Supply a "0" as sign bit to the PN ADDEND at TE time.

3) Allow a "1" to be retained by MQ as quotient bit.

Negative remainder, $\overline{IS}$ is high

1) Supply the numerical portion of ID, UNCOMPLEMENTED, to PN as ADDEND (for addition)
2) Supply a "1" as sign bit to the PN ADDEND at TE time.
3) Do not allow a "1" to be retained by MQ as quotient bit (i.e. quotient bit = 0)

D-11y Regardless of the remainder of the final iteration prior to termination of TRANSFER, a "1" is entered as the lowest order quotient bit. This is known as the PRINCETON ROUND-OFF and has its mathematical virtues.

D-11z Drawing 41 illustrates the 6-bit example used during this evolution in terms of actual signals associated with the circuits involved in a division. A block diagram of the DIVIDE circuits is shown on Drawing 40.

D-11aa ID supplies the EARLY BUS by virtue of S6·SV which is the same term that allows ID to feed EB when ID is programmed as SOURCE, and DESTINATION is not 31.

D-11ab QUOTIENT: The MQ precesses to the left during a divide operation. During every cycle a "1" is inserted in the line at T2·CE time (lowest order bit). 2 word times later at T2·CE time, the state of IS (a function of the previous remainder's sign) determines whether or not this "1" can reach the writing station at T3·CE time and be retained as a quotient bit = 1.

D-11ac Since division is terminated by the TRANSFER terminating pulse, which occurs at T29, the last "1" written at T2·CE time will not be blocked; this provides the PRINCETON ROUND-OFF.

D-11ad At the conclusion of a division the MQ will contain the absolute value of the quotient with a precision which is a function of the number of iterations, hence the T number. The sign bit, now again considered at the low end of the number will contain ZERO. The actual quotient sign is held in IP and will be applied to the number when it is transferred to memory (sec. C-13).

D-11ae OVERFLOW: If at the time of TR_r, (TR reset pulse) a "1" exists in the reading flip-flop of MQ, it represents a 2^0 quotient bit = 1 and constitutes an overflow in the cases when a fractional quotient is called for by programming T = 116 or 57. The reason that a single precision division is programmed to last 57 word times, rather than an even number, is so that the TR_r pulse will occur at T29·CE time (rather than T29·$\overline{CE}$)and will interrogate the state of the appropriate bit. In the event of an overflow, ⊗ (=DIVIDE·PR·TR_r) will set the OVERFLOW FLIP-FLOP (FO).

SOURCE 26 : SHIFT MQ LEFT AND ID RIGHT

D-12a Ref. Drawing 36: This command performs the SHIFTING operations by virtue of the same circuits employed by MULTIPLY (which also shifts MQ left and ID right). CONTROL SWITCH terms control precession of ID and MQ during the time of TRANSFER.

D-12b Also high during TRANSFER is the term $T1 \cdot \overline{CE} \cdot DS \cdot S6 \cdot C8 \cdot (4)$, which turns on the CARRY FLIP-FLOP (AC) of the ACCUMULATOR REGISTER (AR). This results in adding a ONE to the lowest order numerical bit position (T2) of AR during every ODD word time of the time of TRANSFER if characteristic is 0. The number in AR will be "incremented" once every two word times and will count the number of bit positions the contents of ID and MQ are shifted.

D-12c Assume that n is the desired number of bit positions of shift to be imposed upon ID and MQ. If this number is established in AR (prior to the shift command) as a negative number (in complement form) it will appear as $1 - n \times 2^{-28}$.

D-12d Once the TRANSFER state of the SHIFT command is initiated, at the beginning of an EVEN word time, precession will take place in ID and MQ. At the end of each recirculation cycle of the two-word lines ($T29 \cdot \overline{CE}$) the sum in the AR will have been increased by 2^{-28}. That is, after the contents of ID and MQ have shifted one bit, AR will contain $1 - n \times 2^{-28} + 2^{-28} = 1 - (n-1) \times 2^{-28}$. After 2n word times of TRANSFER, the contents of ID and MQ will have been shifted n bit positions and AR will contain $1 - (n-n)\ 2^{-28} = 1 - 0$. 1 - 0 in the AR yields all ZEROS in the numerical portion (T2-T29) and an END CARRY into T1 to change the sign bit to 0. The END CARRY set term, AC_S, occurred at $T29 \cdot \overline{CE}$ - the end of the two-word recirculation cycle which yielded n bits of ID and MQ shift.

D-12e The AC_S term can terminate TRANSFER by the [illegible] gate qualified by $AC_S \cdot T29 \cdot \overline{CE} \cdot DS \cdot S6 \cdot SW$, active during the execution of a SHIFT command (see dwg. 30). This means that the number in AR can control how many bits of shift the contents of ID and MQ will experience.

D-12f The T number of the SHIFT command can also cause termination of TRANSFER by virtue of $T29 \cdot CC$. The T number of a SHIFT command is RELATIVE hence states how many word times TRANSFER can last. If n bits of shift are desired, T should equal 2n.

D-12g The number of bits of shift can be controlled either by $T29 \cdot CC$ or AC_S. Whichever one of these signals precedes the other will control termination of TRANSFER. The order in which these signals arise is a matter of programming. In any event, AR will be incremented if CH = 0. Should the increment AR feature be unwanted a non-zero characteristic may be used.

D-12h Needless to say, the command must be located in an ODD word time and be IMMEDIATE to yield TRANSFER starting with an EVEN word time to accommodate an integral number of two-word recirculation cycles. The S/D bit can contain anything since it controls nothing associated with this command.

SOURCE 27 : NORMALIZE MQ

D-13a Ref. Drawing 36: A number in MQ is normalized when the highest order numerical bit position ($T29 \cdot \overline{CE}$) contains a ONE. (i.e. $1/2 \leqslant n < 1$). During the time of TRANSFER, a NORMALIZE command will cause MQ to precess, shifting its contents to the left one bit position every two word times. The NORMALIZE command must be written as IMMEDIATE and be located at an ODD word time. Its T number is interpreted as relative.

D-13b As in the case of the SHIFT command, AR is incremented every odd word time of TRANSFER if CH = 0; however, AR has no control over TRANSFER.

Incrementing AR serves only to record the number of bit positions of shift experienced by MQ for later program reference.

D-13c The NORMALIZE operation can be terminated by two different terms. One is the T29·CC which is a function of the T number. The other term is a function of the contents of the T29·$\overline{CE}$ position of MQ itself. If a ONE is written in MQ at T29·$\overline{CE}$ time, the PM flip-flop will be set; a ZERO written at that time will reset PM. When a number in MQ is being shifted left, PM will remain reset until a ONE is shifted up to the highest order bit position, hence written at T29·$\overline{CE}$ - setting PM. When PM is set, PM·DS·S6·SX will terminate TRANSFER, stopping the shift. As in the case of the SHIFT command, whichever terminating signal arises first will terminate TRANSFER.

D-13d Since a T29·$\overline{CE}$ pulse sets PM, and PM terminates TRANSFER, TRANSFER will not be terminated until the end of T1·CE (due to the one pulse period delay between the rise of a SET term and CLOCK). This is tolerable since during T1·CE time nothing can be written in MQ to alter its contents because $\overline{TE}$ qualifies the writing term during precession. The advantage in using PM to terminate TRANSFER rather than another suitable pulse (such as PM_S) is that if a number to be NORMALIZED already has a ONE in its T29·$\overline{CE}$ position when TRANSFER starts, TRANSFER will be terminated by PM after one pulse period preventing any shift. The only result of TRANSFER lasting one pulse period will be blocking recirculation of the sign bit which should be ZERO anyway.

SOURCES 28 AND 29: TEST COMMANDS

D-14a These commands all test certain signals. In the event the selected signal is present, CQ will be set and the next command will be read during WT = N+1 instead of WT = N. (Ref. dwg. 30 and sec. C-19). One word time of TRANSFER is all that is required, so these commands are ordinarily written IMMEDIATE with T = L+2.

D-14b SOURCE 28·CH = 0, TEST "READY": DS·S7·SU·④·READY sets CQ. READY is a signal which is high whenever the INPUT-OUTPUT system is idle and is defined as $\overline{OC1}\cdot\overline{OC2}\cdot\overline{OC3}\cdot\overline{OC4}\cdot\overline{OD}$. READY is ordinarily interrogated prior to the initiation of a new INPUT-OUTPUT operation.

D-14c SOURCE 28·CH = 1, TEST "READY IN": DS·S7·SU·①·READY IN sets CQ. READY IN is a signal which can originate in the INPUT-OUTPUT REGISTER accessory.

D-14d SOURCE 28·CH = 2, TEST "READY OUT": DS·S7·SU·②·READY OUT sets CQ. READY OUT can originate in the INPUT-OUTPUT REGISTER.

D-14e SOURCE 28·CH = 3, TEST "DA-1 OFF" DS·S7·SU·③·$\overline{GO}$ sets CQ. $\overline{GO}$ originates in the DA-1 (DIGITAL DIFFERENTIAL ANALYZER) accessory.

D-14f SOURCE 29, TEST OVERFLOW: DS·S7·SV·FO sets CQ. If the OVERFLOW FLIP-FLOP (FO) was set during some previous operation, this command will interrogate it and set CQ accordingly. Upon interrogation, FO is reset by DS·S7·SV·FO·CQ, at T2 time.

SOURCE 30: MAGNETIC TAPE WRITE FILE CODE

D-15 (See sec. F-13)

SOURCE 31·CH = 0: NEXT COMMAND FROM AR

D-16 This command allows the following command (and the following command only) to be read from AR instead of the normal command line established by the configuration in the CD flip-flops. RC timing considerations remain unchanged. One word time of TRANSFER is sufficient, hence the command is usually written IMMEDIATE with T = L+2. During TRANSFER, DS·S7·SX·④ sets CG (ref. dwg. 22). When the next command is read, CG permits $\overline{AR}$·RC to constitute the INVERTED COMMAND and simultaneously blocks $\overline{MC}$, which is the normal inverted command line information. After this next command has been read, T29·RC resets CG and normal operation resumes. (⟨OP⟩ , a signal generated during the initial computer turn-on cycle, resets CG to prevent the first command of the first program from being taken from AR as a function of CG stabilization in the TRUE state when D.C. voltage is first applied.)

SOURCE 31·CH = 1: TRANSFER NT to LINE 18

D-17 The NUMBER TRACK (CN) contains information for timing purposes; however, this information constitutes a handy source of constants especially useful for diagnostic routines. CN may be transferred to LINE 18 (M18) by the M18 writing term DS·S7·SX·①. No provision is made for blocking re-circulation of M18 by this command; therefore, a command clearing the appropriate word(s) of M18 should precede the operation unless M18 is known to be cleared.

"DO NOTHING" COMMANDS

~~D-18 SOURCE 19·CH = 2, SOURCE 19·CH = 3, SOURCE 23·CH = 1, SOURCE 18·CH = 2, SOURCE 31·CH = 2, and SOURCE 31·CH = 3 will accomplish nothing. They will, however, cause the computer to cycle through its states.~~

SECTION E

MANUAL CONTROLS

This section, although small, may constitute the handiest reference material for the reader who will actually operate and/or maintain a G-15D. Many of these controls merely duplicate the functions of commands.

MANUAL OPERATIONS - GENERAL

E-1a The G15 is equipped with several switches to perform logical functions. Most of these are located on the typewriter, though some are located inside the computer on a maintenance panel.

E-1b Drawing 42 shows the typewriter keyboard and the switch panel with indications of the functions. In general, the switches are for the purpose of setting up the computer prior to the performance of a program. They are also useful for diagnostic purposes.

E-1c Many of the controls deal with INPUT-OUTPUT functions or other material covered in sections of this manual to follow. These controls will be mentioned in this section; however, to fully understand their functions it is necessary to understand the associated circuits.

E-1d Many of the manual controls are typewriter keys. Associated with each typewriter key is a mechanical switch which will close for at least 30 milliseconds (one drum cycle) when the key is depressed. When a particular switch closes, its floating point is grounded yielding OV on its output wire; when the switch is open, its floating point is held at -20V by a PULL-DOWN resistor. For example, if the "M" key is depressed, its associated switch contact closes, rendering the output signal, ⟨M⟩, at OV (see dwg. 43 - upper right.) If the switch is not closed, a 1k PULL-DOWN resistor to -20V renders the output signal, ⟨M⟩, at -20V. In other words, ⟨M⟩ can qualify a gate if the "M" key is activated.

THE ENABLE SWITCH - ⟨SA⟩

E-2 The ENABLE SWITCH, located on a component chassis underneath the typewriter, is a toggle switch, which, when closed, will yield the signal ⟨SA⟩. ⟨SA⟩, sometimes called "SAFETY", qualifies certain gates in the computer for purposes which will become apparent as the other switches are discussed. In general, when most typewriter keys are depressed, the ENABLE switch must be ON for the computer function to be performed. This prevents accidental activation of a key from affecting the computer. If the notation ⟨M⟩⟨SA⟩ is made, this means that the "M" key is depressed with the ENABLE switch ON. In addition to its gating functions, ⟨SA⟩ can interrupt a TYPE-OUT operation (sec. F-8u.)

THE PUNCH SWITCH - ⟨MAN PUNCH⟩

E-3 This switch, if ON, yields the signal ⟨MAN PUNCH⟩. ⟨MAN PUNCH⟩ will cause the punch to operate during TYPE-OUT operations (sec. F-8ae). The state of this switch may be interrogated by a TEST command (sec. D-36).

THE COMPUTE SWITCH - ⟨$\overline{\text{GO}}$⟩, ⟨GO⟩, and ⟨BP⟩

E-4 See section C-20.

"I" KEY - SINGLE CYCLE - ⟨I⟩

E-5 Ref. Drawing 30 - upper left: If the COMPUTE SWITCH is in the ⟨$\overline{GO}$⟩ position, ⟨I⟩·⟨SA⟩ will cause one command to be performed followed by a stop. That is, if the computer is idling in the WRC state with CH·$\overline{CZ}$ preventing initiation of RC,⟨I⟩⟨SA⟩ will allow TO to set CZ, yielding CH·CZ permits initiation of RC, hence the next command will be read and executed. When this command is read, ⟨$\overline{GO}$⟩·RC resets CH, yielding $\overline{CH}$·CZ which will prevent the following command from being read, hence the computer will idle in the WRC state. When ⟨I⟩⟨SA⟩ returns to -20V, the next TO pulse resets CZ, yielding $\overline{CH}$·$\overline{CZ}$. This configuration is followed (after one pulse period) by the CH·$\overline{CZ}$ configuration since $\overline{CZ}$ sets CH. CH·$\overline{CZ}$ was the configuration at the beginning of this cycle. At this point another command may be performed by activating the "I" key again. This SINGLE CYCLE feature should be used with caution when RETURN EXIT commands exist (sec. D-61).

"C" KEY - SET COMMAND LINE = 00 - ⟨C⟩

E-6 Ref. Drawing 22 - lower right: ⟨C⟩⟨SA⟩ resets the CD flip-flops yielding the 000 configuration. $\overline{CD1}$·$\overline{CD2}$·$\overline{CD3}$ qualifies the gate permitting $\overline{MO}$ to become $\overline{MC}$, thereby rendering LINE 00 the COMMAND LINE.

"1" - "7" KEYS - SET COMMAND LINE

E-7a These are dual function keys. They are used primarily for generation of codes to supply digital data to the computer under control of the INPUT-OUTPUT SYSTEM. Their other function is that of controlling the CD flip-flops, hence the COMMAND LINE.

E-7b In the component chassis under the typewriter is an array of diode OR gates known as the TYPEWRITER OUTPUT MATRIX. This is an encoding circuit which yields '5-level' codes as a function of several data-input and input-control keys. (This will be discussed more fully in sec. F-3c-f).

E-7c For the time being, the 1-7 keys generate codes such that signals known as TYPE 1, TYPE 2, and TYPE 3 assume 7 different configurations. These signals, providing ⟨SA⟩ is high, and the INPUT-OUTPUT system is idle, can set the CD flip-flops, hence the command line as follows:

Key	Type 3	Type 2	Type 1	CD3	CD2	CD1	Comm. Line
(C				0	0	0	00)
1			1	0	0	1	01
2		1		0	1	0	02
3		1	1	0	1	1	03
4	1			1	0	0	04
5	1		1	1	0	1	05
6	1	1		1	1	0	19
7	1	1	1	1	1	1	23

E-7d The CD's must be reset prior to each set-up operation since the TYPE levels will only serve to set the CD flip-flops and will not reset them. Ordinarily, to manually set a new command line, the sequence is: ⟨C⟩⟨SA⟩, then "1"-"7" ⟨SA⟩. Drawing 22 illustrates the circuit.

"F" KEY - SET "N" = 00 - ⟨F⟩

E-8a The "N" number in the COMMAND REGISTER causes the generation of T21·CC during WT = N-1 to initiate RC. N is ordinarily a function of the previous command; however, means must be provided to establish the initial N number for the first command in a program.

E-8b The "F" key provides this feature by manipulating the COMMAND REGISTER such that on subsequent ~~revolutions~~ cycles a T21·CC will occur during WT 107, causing the first command to be read at WT 00.

E-8c Ref. Drawing 22 - left: A signal known as ["WORD 107"] (=CT+TO+T1·CN) is high during all pulse periods of WT 107. ⟨F⟩⟨SA⟩·["WORD 107"] will occur at least once when the "F" key is activated (⟨F⟩ lasts at least 30 milliseconds). $\overline{CJ}$ may be assumed high during WT 107 as long as the computer is idling in the WRC state). ⟨F⟩⟨SA⟩·["WORD 107"]·$\overline{CJ}$ supplies all ONES to the AUGEND of the COMMAND REGISTER (CU) during WT 107. As a result of the arithmetic in the COMMAND REGISTER, during WT 107 of all subsequent drum ~~revolutions~~ cycles a T21·CC will be generated.

E-8d Since, during WT 107, all bit positions of CU are loaded with ONES, T13·CC and T29·CC end carries will also exist at WT 107 of subsequent ~~revolutions~~ cycles. Thus a previously established T13·CC from a MARK EXIT command will be altered. These, however, are of no consequence in initiating RC of the first command. The first command will establish a new T29·CC.

E-8e Note that the signal "TAPE START" also "sets N = 00" by the same method. This will be covered in sections E-11d and G-2m.

"M" and "R" KEYS - MARK and RETURN - ⟨M⟩ and ⟨R⟩

E-9a These keys act as a pair. (Do not confuse their functions with the MARK EXIT and RETURN EXIT commands.) Frequently it is desirable to interrupt a problem and manually perform some functions which may serve to alter the contents of the ACCUMULATOR REGISTER (AR) and/or the COMMAND REGISTER (CM). In such cases it is desirable to store the original contents of AR and CM, perform the manipulations, then return the original contents to AR and CM. MARK stores the information, RETURN returns it.

E-9b MARK: (Ref. Dwg. 59) The signal MARK (=⟨M⟩⟨SA⟩·["WORD 107"]) causes the contents of AR to be written into word 107 of LINE 1. Simultaneously $\overline{MARK}$ blocks recirculation of LINE 1. At the same time, MARK causes the inverted contents of CM (i.e. $\overline{CM}$) to be written into word 107 of LINE 0; $\overline{MARK}$ blocks recirculation of LINE 0 at this time. This suggests that word 107 of LINES 0 and 1 should be reserved for this function and not employed in any program.

E-9c RETURN: (Ref. Dwg. 59) The signal RETURN (=⟨R⟩⟨SA⟩·["WORD 107"]) blocks recirculation of AR (AUGEND term) during word 107 inserting M1 as the ADDEND.

The writing term will be the original contents of AR prior to the MARK operation. RETURN substitutes $\overline{MO}$ for CM as the AUGEND term of the COMMAND REGISTER during word 107. The double inversion experienced by original CM information is compensatory. Since MARK and RETURN both performed their functions during word 107, the arithmetic in the COMMAND REGISTER is effectively unaltered and T29·CC, T21·CC, and T13·CC will appear during the same word times as they did prior to the MARK.

"T" KEY - "N" to AR - ⟨T⟩

E-10a The object in this operation is to transfer "N" number information to the AR where it can be viewed on an oscilloscope or typed out. This is particularly useful in "checking out" new programs to see if they follow the sequence anticipated by the programmer.

E-10b Since the "N" number is in the dynamic portion of a command, it is sent to the COMMAND REGISTER and modified every word time by the arithmetic, presenting a monitoring problem. Therefore, evidence of the "N" number, T21·CC, is used to obtain a constant representing "N". The NUMBER TRACK (CN) contents immediately following T21·CC consists of the 'WT+1' factor. Since T21·CC occurs during WT = N-1, and the contents of CN during that word time equals WT+1, the CN data = WT+1 = (N-1) +1 = N. This data, during T22-T28, is transferred from CN to AR as illustrated on Drawing 59. The T1-T21 portion of AR remains unchanged.

E-10c When N = 00, T21·CC occurs during WT 107 yielding CN information =20 rather that WT+1 (See Dwg. 6). This results in ambiguity between the indications from CN arising from N = 00 and N = 20. For this reason, whenever T21·CC occurs during word 107, TO is written into AR yielding 10010100 as the configuration in the highest order eight bits of AR.

E-10d Usually when N is transferred to AR by "T" key operation, an AR TYPE-OUT follows (initiated by the "A" key). AR is ordinarily typed out in terms of SIGN and 7 HEXADECIMAL DIGITS. The highest order two hex. digits indicate the "N" number (i.e. LOCATION of the next command). 01_{16} - $6u_{16}$ $=01_{10}$ - 106_{10} and $94_{16} \equiv 00_{10}$.

E-10e Needless to say, the original contents of AR are disturbed, therefore the MARK and RETURN keys could be used to advantage. A typical sequence in SINGLE CYCLING a new program and producing a record of command locations is: M-T-A-R-I-M-T-A-R-I-M-T-A-R-I-----.

"A", "Q", "P", "B", and "S" KEYS - INPUT/OUTPUT

E-11a These keys are for purposes of manually initiating or terminating INPUT-OUTPUT Operations. Reference is directed to the INPUT-OUTPUT section of this manual (sec. F) and to Drawing 45.

E-11b "A" KEY - TYPE AR: ⟨A⟩⟨SA⟩·Ⓝ sets the OC's to a 1000 configuration and sets the OD flip-flop, initiating a TYPE-OUT AR. ⟨SA⟩ must be released before any typing will occur.

E-11c "Q" KEY - SET TO TYPE IN: ⟨Q⟩⟨SA⟩ sets the OC's to a 1100 configuration, rendering the INPUT system receptive to typewriter input-data and input-control keys.

E-11d "P" KEY - PHOTO-TAPE READ, SET COMMAND LINE = 23 and N = 00: ⟨P⟩⟨SA⟩ sets the OC's to a 1111 configuration, starting the PHOTO-TAPE READER. Also, ⟨P⟩⟨SA⟩ generates the TAPE START signal (ref. dwg. 22). TAPE START·["WORD 107"] duplicates the function of the "F" KEY, setting N = 00. TAPE START also sets the CD's to a 111 configuration, establishing LINE 23 as the COMMAND LINE. The last two functions are a convenience for the operator.

E-11e "B" KEY - START PHOTO-TAPE REVERSE CYCLE: ⟨B⟩⟨SA⟩ sets the OC's to a 0110 configuration, initiating a PHOTO-TAPE REVERSE CYCLE (see sec. F-5)

E-11f "S" KEY - STOP INPUT-OUTPUT: ⟨S⟩·(SA +$\overline{OC1}$·$\overline{OC2}$) resets the OC flip-flops, manually terminating any INPUT-OUTPUT operation. It is not necessary to hold the ENABLE switch ON when using the "S" KEY to terminate a TYPE-IN. (Do not confuse the function of this key with that of the STOP code.)

LOGIC PUSH-BUTTON MAINTENANCE SWITCHES

E-12a A small maintenance panel is located inside the computer behind the power control panel. This panel includes many banana jacks yielding frequently needed oscilloscope signals for "SYNC." and "Y-AXIS". Also, six push-button switches exist as follows:

CLEAR	SET
M19	M19
M23	OP
NT	NT

E-12b These switches perform logical functions associated with the initial TURN-ON CYCLE and are described in the section on that subject - Section G-3.

SECTION F

THE INPUT-OUTPUT SYSTEM

This section accounts for the subdivision of the computer without which there could be no communication between the computer and the operator. Prerequisite knowledge should include the contents of Sections A, B, and C-15. The principle of PRECESSION should also be understood; examples of this are given in Sections D-10c-j.

THE INPUT-OUTPUT SYSTEM - GENERAL

F-1a The INPUT-OUTPUT SYSTEM of the G-15D may almost be considered an independent data processing system. Its logical linkage to the COMPUTER PROPER is very loose. It utilizes some of the basic timing signals and two of the programmable memory lines, M19 and M23. Another memory line, MZ (a 4 word line), is "private property" of the INPUT-OUTPUT system and facilitates certain data handling functions. An INPUT or OUTPUT operation and a program can progress concurrently as long as LINES 19 and 23 are not involved in the program.

F-1b The different INPUT-OUTPUT operations available are listed on Drawing 3 as SOURCES 00-15 and 30. The SOURCE 30 operation is a special case and does not employ the INPUT-OUTPUT SYSTEM. It will be discussed separately in sec. F-13.

F-1c Note that the sixteen INPUT-OUTPUT operations (defined by SOURCES 00-15) are divided into four categories: FAST-OUT, FAST-IN, SLOW-OUT, and SLOW-IN. These states of the INPUT-OUTPUT system define the nature of the operation in progress; further subdivision selects the particular INPUT-OUTPUT medium to be active.

F-1d A central control circuit for all INPUT-OUTPUT operations exists in the form of a 4-bit static register composed of the OC FLIP-FLOPS: OC1, OC2, OC3, and OC4. Note on Drawing 3 that each operation is represented by a binary configuration in these flip-flops. The configurations are the same as the SOURCE number (i.e., 00-15).

F-1e In general, when no INPUT-OUTPUT operation is in process the OC configuration is 0000 - representing the "READY" state. A particular INPUT-OUTPUT operation may be initiated by setting these flip-flops to the appropriate configuration. While they are set in a non-zero configuration the INPUT or OUTPUT operation takes place. Normally a signal within the INPUT-OUTPUT SYSTEM itself will call for termination of the operation and will accomplish this end by resetting the OC flip-flops to the all-ZERO configuration (READY state). The latter may also be accomplished manually ("S" Key), or by a special command (SET READY). Once the READY state is established, a new INPUT-OUTPUT operation may be initiated. (The special command, "TEST READY", permits a programmable interrogation of this state - ref. sec. D-14b.)

F-1f The contents of the OC flip-flops are decoded, yielding signals which serve to control the logic of the INPUT-OUTPUT circuits and also the activity of the various electro-mechanical INPUT-OUTPUT media. The means of controlling the OC's varies. A glance at Drawing 45 should acquaint the reader with the various OC control options and the output signals from the decoding gates. Neon indicators on the front panel monitor the state of the OC'S at all times.

OC FLIP-FLOP CONTROL

F-2a PROGRAMMED OC SET-UP: Whenever the READY state is present, an INPUT-OUTPUT operation may be initiated by a special command. Such a command

involves DESTINATION - 31 and SOURCE = 00 - 15. In these cases the contents of the SOURCE flip-flops in the CONTROL SWITCH will contain a configuration such that the 2^4 bit is equal to ZERO. The 2^4 static flip-flop is CV; therefore, during the time of TRANSFER, DS·$\overline{CV}$ will be high and is used to transfer the 2^0 - 2^3 source information to the OC'S as shown at the top of Drawing 45. Once this OC configuration is established, new commands may be read and executed independently of the INPUT-OUTPUT system, provided LINES 19 and 23 are not involved in the program.

F-2b MANUAL OC SET-UP: This has been partially covered in sec. E-11. Drawing 45 (left) illustrates the options. More will be said about these functions under the appropriate headings (e.g., the "A" key, hence ⟨A⟩⟨SA⟩, will be discussed in sec. F-8, which includes AR TYPE-OUT).

F-2c OC RESET: Drawing 45 (lower left) shows these options. As the notes suggest, the means of resetting the OC'S (other than manually) depend upon the nature of their configuration. These too will be discussed under the appropriate headings.

THE INPUT MEDIA

F-3a When the OC'S assume the configuration 11xx, a SLOW IN operation is called for. The highest order two bits (configuration OC4·OC3) set up the logic circuits with qualifying signals IN and SLOW IN. The lowest order two bits determine which input medium is to be active but do not in all cases directly control the particular medium.

F-3b Before the behavior of the INPUT LOGIC circuits can be intelligently discussed, the INPUT MEDIA themselves must be understood. The sections to follow will attempt to accomplish this end.

F-3c TYPEWRITER: Ref. dwg. 43) when the typewriter is to be used as the input medium, manual activation of certain keys supplies data-input characters (hexadecimal) and functions in terms of 5-level codes. These codes appear on five signal wires: TYPE 1, TYPE 2, TYPE 3, TYPE 4, and TYPE 5. Drawing 46 in the INPUT-ORIGIN-TYPEWRITER column indicates the active keys and the codes they generate.

F-3d Generation of these 5-level codes is accomplished in an encoding circuit known as the TYPEWRITER OUTPUT MATRIX. This is nothing more than an array of OR gates such that when any of the 20 typewriter keys which produce codes is activated, its switch contacts will raise the appropriate output level lines to 0V to represent ONES (see dwg. 43). Any level line not raised to 0V by an OR gate diode is held at -20V by a 4.7k pull-down resistor (indicated on the DETAILED PRINT - 3D282). Each one of the five output level lines except Type 4 is provided with an R-C filter to integrate the signal with a suitable time constant to reduce signal irregularities due to point bounce and transient effects. This is necessary to prevent an electronic synchronizing circuit in the computer from being illegally triggered. These output level lines contain the typewriter output signals for the INPUT system.

F-3e In addition to these level signals, "F-B" reaches the computer for synchronization purposes. This signal is required for proper operation of the INPUT-OUTPUT system when the typewriter is used as the OUTPUT medium; however, it will reach the input system and must be mentioned. The signal

will be high if the SPACE BAR, SPACE KEY or PERIOD key is activated. The line is provided with an R-C filter since this signal will be used to trigger the synchronization circuit mentioned above. This function will have no effect on the INPUT system as far as data entry is concerned.

F-3f All of the signals mentioned above may be expected to last at least 30 milliseconds (over one DRUM CYCLE). 1/10 second is the average duration.

F-3g PHOTO-TAPE READER: (Ref. dwg. 44) This device "reads" the 5-level codes punched on a paper tape. The nature and sequence of the codes are a function of how the tape to be read was punched. This is ordinarily a function of the OUTPUT system of the computer and the programming thereof. The PHOTO-TAPE READER supplies the INPUT SYSTEM with the codes on 5 level lines: PHOTO 1, PHOTO 2, PHOTO 3, PHOTO 4 and PHOTO 5. These signals are similar to those originating in the typewriter but are of much shorter duration and occur in rapid succession. The PHOTO-TAPE READER will supply, as output, any code appearing on the tape being read; however, only the codes indicated on Drawing 46, column INPUT-ORIGIN-PAPER TAPE should ever appear.

F-3h Assuming that photo-electric reading circuits exist, the problem of tape motion will now be considered. Motion of the tape can assume two directions past the reading station - FORWARD and REVERSE. The direction is a function of torque delivered by two motors which constitute the prime-movers of reels containing tape in a magazine. (Which reel is the FEEDER and which is the COLLECTOR varies with the direction of motion.)

F-3i Torque applied to the reels is a function of two relays: The FORWARD relay (RY-A) and the REVERSE relay (RY-B). Assume that the FORWARD relay is energized. Points on this relay will accomplish the following:

1) Apply 115 VAC to the upper winding of the two-phase TOP MOTOR.

2) Apply 115 VAC to the lower winding of the TOP MOTOR via the 1.2mf starting condenser C1 such that the phase relationship results in counterclockwise (from front) torque.

3) Apply reduced AC (function of R12 setting) to the upper winding of the BOTTOM MOTOR.

4) Apply reduced AC to the lower winding of the BOTTOM MOTOR via the 1.2mf starting condenser C2 such that phase relationship results in counterclockwise (from front) torque. The amount of torque is sufficient to overcome friction of the feed reel system.

5) Complete circuit to energize illuminator lamp (for photo-electric circuit).

6) Charge C3A and C3B (80 mfd each) to peak value of line voltage to prepare for "dynamic braking".

F-3j The result of the above is that the tape will move in a FORWARD (upward) direction past the reading station and will be illuminated. The linear speed of the tape is a function of the angular velocity of the motors and the radius to the point of tangency of the tape on the reels. Therefore,

no specific linear speed can be given. Linear speed is considered to average 20 inches/sec yielding an average rate of 200 characters/sec. Applying assisting torque (reduced) to the feed reel overcomes friction and improves acceleration characteristics. (Too much assisting torque could result in tape spillage. A 1k potentiometer, R12, is adjusted so that with no magazine on the reader, the feed reel drive is just on the verge of creeping.)

F-3k Had the REVERSE relay been energized instead of the FORWARD relay, the above functions would have been performed except that the torques would have been clockwise and the BOTTOM MOTOR would have yielded full torque while the TOP MOTOR would have yielded reduced (assisting) torque.

F-3l Whenever either relay is de-energized yielding the "no-go" state following a "go" state, the charged 80 mfd condensers (C3A and C3B) are connected by relay points to the windings of each motor supplying "dynamic braking". By the time the charges have been spent, the motors should be stopped and the circuit static. Various R-C and L-C circuits distributed about the schematic are for transient suppression purposes.

F-3m Relay control: Controlling the relays controls the reader. Usually the relays are energized by puller tubes caused to conduct by signals from the OC flip-flops (FORWARD = 1111, REVERSE = 0110 or 0111). The puller tubes may also be controlled by a front panel switch: FORWARD-REWIND. It turns on the appropriate puller tube but breaks the illuminator lamp circuit to prevent any reading activity.

F-3n Reading activity assumes that the tape is in motion and the illuminator lamp is lit. There are six channels to be read: LEVELS 1-5 and SPROCKET HOLE. The SPROCKET HOLE is read to provide a time-gating signal to probe for the presence or absence of LEVELS 1-5. The gating accomplishes the following: (1) it assures that the output signals on the level lines are simultaneous and of roughly the same shape, and (2) it overcomes the adjacent-hole problem, in which the signal between adjacent holes does not decay to zero signal level due to the optics. This is illustrated at the bottom of Drawing 44.

F-3o IN77B photo-diodes are used as the photo-sensitive elements for each channel. These diodes have the following characteristics: high back-resistance when dark and low back-resistance when illuminated. By placing such a photo-diode in a voltage-divider such that its back-resistance constitutes a variable resistance in the voltage-divider, a varying potential may be obtained which is a function of the light striking the cell.

F-3p The SPROCKET cell, CR 13, is connected in such an arrangement, with the negative return at -24.6V (jct. R55-R66) and the positive return at +100V. The junction of CR13 and R17 (clamped by CR7 so it cannot exceed 0V) yields an output potential which should equal 0V when the cell is dark and approach -24.6 when the cell is illuminated. Potentiometer R18 (2.5 meg) permits adjustment of the series resistance to "custom-tailor" the voltage divider parameters to the back-resistance characteristics of the particular cell.

F-3q Potentiometer R18 ("S") is available on the side of the PHOTO-READER

and is adjusted for a desirable oscilloscope indication at test point "S", which contains the output of a cathode-follower (V2A, pin 3). This follows the potential at the CR13-R17 junction. Desirable indication consists of maximum signal output (approaching -20V) with no base-line (OV) noise. If the adjustment renders the circuit too sensitive to light, translucency of tape can be a problem.

F-3r The SPROCKET level cathode-follower (V2A) supplies a gating signal to the five other channels such that only during the time of the SPROCKET signals can the other levels yield an output signal if illuminated. The five voltage dividers in the other channels resemble that of SPROCKET except that the negative returns are connected to the SPROCKET channel cathode-follower. This means that between sprocket holes, when the cathode-follower output is at OV, the level photo-diodes (cathodes) cannot yield a signal less than OV regardless of illumination. However, should a level be illuminated, during the time that the sprocket signal approaches -20V, the level photo-diode will yield a signal approaching -20V.

F-3s Such a level signal is inverted by its associated triode. The plate circuit of such a triode yields a positive-going signal clamped at OV and with a base line of approximately -20V (negative clamping is not necessary considering the nature of the circuits to follow). A degenerative circuit is connected to the cathode of each triode. This will not alter the peak-to-peak value of the output signals but will offer reduced gain to undesirable high frequency components on the leading and trailing edges. These high frequency components are further suppressed by .0018 mfd integrating condensers on the output lines. This reduces the possibility of transient-triggering of the synchronization circuit in the INPUT system of the computer.

F-3t Adjustments are available on the side of the reader to adjust the response of each channel. Associated with each adjustment is a test point. The adjustments are made in a manner similar to that of sprocket. Periodic observation of these test points is advisable.

F-3u MAGNETIC UNITS: These supply codes on five level lines in the form of square waves (with peaks of -20V and OV) which appear at a peak rate of 463 characters/sec (i.e. 1 code every 8 word times). The signals will appear whenever the tape transport mechanism is programmed to be in motion and the tape has data recorded upon it.

F-3v CARD UNIT: (IBM 026 with adapter circuits) Mechanical contacts supply level signals in a manner similar to that in the typewriter. In addition to the 5 level signals, a MINUS SIGN signal can be generated and will enter the computer INPUT system independently of the levels.

SLOW-IN LOGIC

F-4a The INPUT SYSTEM will respond to codes from the input media, e.g. the typewriter, photo-tape reader, and magnetic tape units. The codes to which the INPUT SYSTEM will respond are indicated on page 46. Note that all codes for which level 5 is a one are considered numerical hexadecimal characters. When level 5 is a zero the code indicates a control function. The SLOW-IN

logical hardware is shown on page 48. An illustrative SLOW-IN timing example is given on page 49.

F-4b Any code arriving at the input levels (ref. dwg. 48 - bottom) will cause the HC buffer-inverter to become high. This will activate a synchronizing circuit which will control the subsequent activity of the input system. Fourth input level control of HC is absent, but note that when fourth level does occur it will always be accompanied by fifth level. In this case fifth level will provide the necessary synchronizing signal. The synchronization circuit is composed of HC, OF1, OF2, and associated gates.

F-4c The signal HC, which triggers the synchronization circuit, must be reasonably free of transients to avoid multiple triggering. This was handled to some extent in the sources of the level signals. Additional high frequency suppression is accomplished by modifying the BUFFER-INVERTER package itself which includes the HC circuit (see dwg. 13). It is essential that this modified package be plugged into the appropriate jack. The package can be identified by a notation on its handle.

F-4d Note that the gates associated with the OF flip-flops in the synchronization circuit are all qualified by "IN". This arises from certain configurations of the OC'S, all of which represent INPUT operations. The OF flip-flops are used for different purposes during OUTPUT operations and are controlled by different gates. In such cases the signal "IN" is low, and the gates it qualifies are effectively out of the circuit. This principle of multiple use of tube circuits is repeated throughout the INPUT-OUTPUT system and accounts for component economy.

F-4e Activation of HC by an input code will set OF1. OF1·IN will enable the input code at the input levels to be inserted into a 5-bit static buffer register consisting of the OB flip-flops. Once the code is in the OB's the signals on the level lines can decay.

F-4f OF1 also sets OF2. HC will decay upon the decay of the input level signals, and the synchronizing circuit will perform its closing cycle yielding the signal Ⓔ, which controls the activity in the INPUT logic circuits.

F-4g Ⓔ is a gated TF pulse. TF is a basic G15D timing signal. TF=T29·$\overline{CE}$·CF, therefore occurs during WORD TIMES CONGRUENT TO 3 MODULO 4, i.e. at T29 of words 3, 7, 11...103, 107. TF is suitable for initiating or terminating activities dealing with 4-word lines at the beginning or the end of their four-word recirculation cycles (ref. sec. C-15). Ⓔ will occur at the first TF pulse after OF1 is reset which will be just after the input levels decay. The TF pulse which is gated to become a Ⓔ is also used to reset OF2, thereby freeing the synchronizing circuit to generate a new trigger from the next input code. A Ⓔ will occur during any INPUT operation after a code is inserted into the OB's. Ⓢ = Ⓔ·OC4 = Ⓔ during SLOW-IN operations only.

F-4h If prior to generation of the Ⓔ associated with one code, a new code arrives at the level lines, the OF2 term disqualifying the OF1 set gate inhibits the next synchronization cycle until Ⓔ is generated. This prevents skipping codes due to loss of Ⓔ at high input rates.

F-4i Once Ⓔ is generated by the synchronization circuit, it will start the logic circuits functioning under control of the code in the OB'S. There is a decoder yielding several signals defining the code residing in the OB'S. (Like many circuits requiring no clarification, the OB decoding gates are not shown in the simplified drawings. They may be easily located in the more detailed prints--in this case dwg. #'s 3C303 and 3D287.)

F-4j A principle employed in most INPUT-OUTPUT operations is PRECESSION. One bit precessions have been used in MULTIPLY, DIVIDE, SHIFT and NORMALIZE. The VIA AR characteristic is a one-word precession. The INPUT SYSTEM involves 1-bit precessions, 4-bit precessions, and 4-word precessions for information positioning purposes. As the reader may recall, a precession to the left involves inserting a delay in the recirculation path of a memory line.

F-4k Assume the case of a hexadecimal character arriving at the input levels (level 5 must be high). The character will be inserted into the OB's (1xxxx) and a Ⓔ will be generated. Because OB5 is high, Ⓔ will allow the contents of OB1-OB4 to be copied into OA4-OA1 respectively. The OB's will also reset at Ⓔ time freeing them to receive a subsequent code. Ⓢ (= Ⓔ·SLOW) will reset OF3 and set OG because the code in the OB's defines a digit (1xxxx). OG will be high for four word times (terminated at the next TF pulse) and the following will occur:

1) Normal recirculation of M23 will be disqualified - because $\overline{OG}$ is low.

2) OG and $\overline{OF3}$ will enable a precession path for M23 such that M23's read flip-flop will feed OA1. OA1 will feed OA2, etc., and OA4 will feed a gate enabled by OF3 which will write into M23.

3) During the first four pulse periods the code in the OA's will be written into M23 (this was the original new input hexadecimal character) and....

4) The original contents of M23 will be delayed 4 bit times (or precessed to the left) and hence will be rewritten 4 bit times late.

5) This path is enabled for four word times. At the end of the four word times normal recirculation of M23 is resumed.

6) The following changes will now be noted in M23's contents. The lowest order four bits (T1-T4 of word 00) contain the newest input code, the original M23 information has been shifted four pulse periods to the left, and the original highest order four bits of M23 are ~~now residing in the OA's (to be lost when a new hexadecimal character is inserted).~~ dumped

7) Each hexadecimal input code will have the effect of entering four bits into the lowest four bit positions of M23.

F-41 Commands or numbers may be entered into the G15D by first converting them to hexadecimal. The procedure to accomplish the conversion of commands into hexadecimal is outlined on drawing 5. The procedure for converting decimal numbers to hexadecimal may be accomplished by simple arithmetic or by consulting a conversion table (drawing 4). To enter a word into the

G15D (be it a number or command) the following sequences of codes could occur:

(SIGN) - 7 HEX. DIGITS - TAB or CARRIAGE RETURN

The total effect of the above will be to enter 29 bits of information into M23 word 00. It may be noted that the sign may be entered at any time providing it precedes the TAB or CARRIAGE RETURN code. The reason for this flexability will be explained later in this section. In practice the programmer uses a program preparation routine which allows him to communicate with the computer using binary-coded decimal leaving the drudgery of conversion to the computer.

F-4m Should a minus sign code (00001) appear at the input levels the following sequence of events will occur:

1) The sign code will be inserted into the OB's and a Ⓔ will be generated as was the case for a hex. code in section F-4k.

2) With $[SIGN]_{OB,}$ 0x001, at Ⓔ time OS is set.

3) Should it have been desired to enter a plus sign no code entry would have been necessary as OS would have been reset already by a previous TAB or CARRIAGE RETURN code or the READY signal.

4) Note entry of the minus sign code has only succeeded in setting the OS flip-flop and not actually entering this information into G15D memory. Further processing of the sign will be accomplished upon receipt of a TAB or CARRIAGE RETURN at the input levels. OS will remember the sign until then.

F-4n Entry of the hexadecimal portion of the word procedes character by character as described in section F-4k. Normally 7 hex. characters will be entered thus these bits will be located in T1-T28 of word 00 of M23.

F-4o The sign bit, presently residing in the OS flip-flop, represents the final bit of data to be entered into M23. Its position should be T1 of word 00. A TAB code (00011) or CARRIAGE RETURN code (00010) entry will give rise to the following sequence of events:

1) The TAB or CARRIAGE RETURN code will be inserted into the OB's and a Ⓔ will be generated as in the case for the hex. character in section F-4k.

2) With $[TAB + CARRIAGE\ RETURN]_{OB,}$ 0x01x, at Ⓔ time the contents of the OS flip-flop will be transferred to OA1, at the same time OS will be reset (hence the sign will be assumed positive for the next word, thus eliminating necessity for ever having a + code).

3) With $[TAB + CARRIAGE\ RETURN]_{OB,}$ Ⓢ will set OF3 and OG. OG being high for four word times will block M23's normal recirculation path, while OF3 and OG establish a one bit precession path for four word times from M23's read flip-flop to OA1 to a M23 write gate.

4) During the first pulse period the contents of OA1 (the previous contents of OS) will be written into the T1 position of word 00 and all the original contents of M23 will be written one pulse period late.

5) Precession will last four word times. At the end of this time M23's normal recirculation is resumed.

6) The following changes will now be noted in M23's contents. The T1 bit position of word 00 contains the sign information, and the original contents of M23 has been shifted to the left one bit. The highest order bit of M23 (T29 of word 03) has been lost.

7) If previous to this operation 7 hex. characters had been entered then they are all sitting in M23 in word 00 in the desired bit positions.

8) In effect it is the TAB or CARRIAGE RETURN which enters the sign information into the G15D memory.

F-4p Should the above procedure of entering (SIGN), 7 HEX. DIGITS, TAB or CARRIAGE RETURN be repeated, then the first word entered into word 00 would be shifted into word 01 and the most recent entry would now reside in word 00. A maximum of four words may be entered into M23 in this manner. Additional entry would result in the loss of the original word occupying word 03 as it would be shifted out the high end of M23. Therefore a means is provided to store M23 in a long line, M19. The RELOAD code will initiate this function.

F-4q When RELOAD, 00101, arrives in the OB's, the following sequence of activity occurs:

1) Ⓢ will set OD and OY. This will block normal recirculation of a four word line, MZ. OY will stay high four word times causing M23 to be copied into MZ. This frees LINE 23 for reception of new data.

2) At the first TO after OD was set, OE will set. OE will remain high for one drum cycle. With OD and OE high normal recirculation of MZ and LINE M19 is interrupted, but a four word precession path is established for 108 word times involving MZ and M19. The path is such that beginning at word 00, MZ's contents are written into M19, and M19's contents are written into MZ. M19's original contents reappear at MZ's read flip-flop delayed four word times and are rewritten into M19. After 108 word times normal recirculation of MZ and M19 is resumed.

3) As a result of the precession the original contents of MZ (which came from M23) reside in words 0-3 of line M19. The original contents of M19 are shifted to the left four words. The original highest order four words (104-107) of M19 reside in MZ where they will be lost upon receipt of the next RELOAD code.

F-4r If 27 four-word groups are entered in this manner, LINE 19 will be "filled", with the first word entered residing in word 107. At this time the INPUT operation should be terminated. If the typewriter is the input medium, the "S" key should be activated following the final RELOAD code. This resets the OC flip-flops terminating the INPUT operation. The ENABLE switch need not be ON for this operation since $\langle S \rangle \cdot \overline{OC1} \cdot \overline{OC2}$ resets the OC's.

F-4s If any other input medium is used it should substitute a STOP code for the final RELOAD code. A STOP code performs not only the OC reset function but also the RELOAD function. When a STOP code resets the OC'S it does so approximately one drum cycle prior to the time that the LINE 19 - MZ precession is completed. This is for the purpose of stopping the PHOTO-READER at the earliest possible time. For this reason the precession gates must be qualified by "FAST OUT" as well as "IN" ("FAST OUT" includes the 0000 configuration). Also $\overline{OD}$ must qualify the gate which forms the READY signal so the INPUT-OUTPUT system will not appear to be idle while it is still occupied in this final precession.

F-4t Remaining aspects of the INPUT system should be evident considering the material on Drawings 48 and 49. Miscellaneous elusive facts are as follows:

1) OB5 qualifies the $OA1_r$ gate ($\textcircled{E} \cdot \overline{OB4} \cdot OB5$) to prevent the fourth-level ZERO in a TAB or CARRIAGE RETURN code from resetting OA1 at the same time a ONE in OS calls for setting OA1.

2) When a MINUS SIGN is to be stored in OS, the MINUS SIGN code is entered; entry of a PLUS SIGN involves merely the failure to enter a MINUS SIGN since OS is reset every time a TAB or CARRIAGE RETURN is entered. CA-1 CARD EQUIPMENT can set OS without the formality of HC, etc.

3) A buffer-inverter is used to set OG and prevent the possibility of simultaneous reset. This is to permit a high data entry rate involving consecutive TF pulses becoming $\textcircled{E}$'s.

4) $\overline{TF}$ qualifies $\textcircled{O}$, which permits the contents of the OA's to shift during precessions. Preventing OA shift at TF time has no effect on the desired precession results in LINE 23; however, it does permit a new character to be transferred from OB's to OA's without conflict in the event of consecutive TF pulses becoming $\textcircled{E}$'s.

5) The purpose in resetting the OC's approximately one drum cycle prior to the completion of the STOP code operation is to stop the input medium with minimum delay. (Once a STOP code reaches the OB's it will remain there until the OC's are reset rendering the INPUT system insensitive to any incoming level codes which may follow.)

6) The SPACE and PERIOD keys on the typewriter generate no codes but do raise HC. This is for the benefit of the typewriter when used as an output medium. A PERIOD code coming from tape will raise HC and be inserted in the OB's; however, no circuit beyond the OB's will respond to it. An incoming SPACE code is no code at all. SPACE is an output function.

7) A WAIT code performs the same data entry function as HEXADECIMAL ZERO. WAIT is an editing feature.

F-4u The codes may arrive at the input at any rate less than 926 characters/sec. (i.e., 1 character/4 WT), except in the case of the RELOAD code which cannot exceed a rate of 17.2/sec. (i.e., 1 character/2 drum cycles). Considering the normal sequence of codes involved in data entry, the RELOAD rate is the limiting factor. In practice, the maximum input rate delivered by any of the media is 463 characters/sec. and 15 RELOADS/sec.

F- 4v It is suggested that the reader study the example on Drawing ~~50~~ 49 confirming the activity on Drawing ~~50~~ 48 This combines the time axis with the logical hardware-- both of which should be fully understood. (Drawing of colored vertical lines joining key TF dots at the top and bottom of the timing diagram is advisable.)

PHOTO-TAPE SEARCH (FAST-IN)

F-5a FAST-IN involves searching for certain codes either on PAPER or MAGNETIC TAPE with the purpose of positioning tape but not obtaining data. This discussion will be devoted to PHOTO-TAPE search operations only. MAGNETIC TAPE search operations will be discussed in sec. F-14.

F-5b Data ordinarily is punched on tape in the form of 108 word blocks (27 four-word groups) terminated by a STOP code. A few inches of blank tape should be provided between adjacent blocks to allow for tape acceleration and deceleration. When a tape in the PHOTO-READER is read for data entry purposes (i.e., SLOW-IN), it should be started from a blank tape area. The PHOTO-READER will read tape until a STOP code is read; the STOP code causes the OC's to be reset stopping the mechanism.

F-5c Assume now that a block of tape has been read and the tape is stationary in a blank tape area. The programmer wants to back the tape up one block so that the same block can be re-read. The PHOTO-TAPE reverse cycle will accomplish this. (Two PHOTO-TAPE REVERSE CYCLES would back the tape up two blocks.)

F-5d (Ref. dwg. 45) The cycle can be initiated by setting the OC's in the 0110 configuration, representing PHOTO-TAPE REVERSE-PHASE 1. This can be accomplished manually ("B" key) or by a special command (S = 6, D = 31). The configuration yields the signals "IN" and "PHOTO TAPE REVERSE".

F-5e "PHOTO-TAPE REVERSE" energizes the REVERSE relay in the PHOTO-READER, lighting the illuminator lamp and moving the tape in a REVERSE direction. "IN" qualifies the "front end" of the INPUT system (dwg. 48 - bottom) allowing it to register all incoming codes in the OB's and to generate Ⓔ's; however, none of the data goes into any memory lines since "SLOW-IN" is not present.

F-5f (Ref. dwg. 45 - upper left) When the first STOP code is registered in the OB's, the signal PHOTO-TAPE REVERSE·$[\text{STOP}]_{OB}$·Ⓔ sets OC1 (gate 1), producing the 0111 configuration in the OC's, representing PHOTO-TAPE REVERSE-PHASE 2. The tape continues reading in REVERSE until it encounters the next STOP code; then PHOTO-TAPE REVERSE·OC1·$[\text{STOP}]_{OB}$·Ⓔ (gates 1 and 2) sets OC4, yielding the 1111 configuration in the OC's, starting a regular FORWARD PHOTO-TAPE READ operation. This reverses tape motion.

F-5g The FORWARD operation reads tape until the first STOP code is reached. This resets the OC's, stopping the tape (according to normal procedure in SLOW-IN). The complete operation succeeds in backing the tape up one block as illustrated on Drawing 45 (upper left).

F-5h Miscellaneous facts: (1) Among the terms which form Ⓚ (dwg. 48) to reset the OB's is Ⓔ · $[STOP]_{OB}$ · PHOTO-TAPE REVERSE. This permits the OB's to be cleared after the STOP codes have been interrogated during the REVERSE search, permitting normal operation of the OFl_S gate on subsequent codes. (2) During the final part of the cycle, the FORWARD reading will affect LINES 19 and 23 since codes will be read during a SLOW-IN situation. Therefore it is advisable that the contents of these lines be insignificant when the cycle is initiated. (3) Programming a PHOTO-TAPE REVERSE-PHASE 2 may appear worthless, but it can serve the purpose of "homing in" on a particular STOP code when necessary.

SLOW-OUT - GENERAL

F-6a The SLOW-OUT system may almost be considered an independent computer. It is independently programmable to provide maximum flexibility in editing computer output. The destination of information extracted from the selected output memory line (M19 or AR) is a 5-bit buffer register consisting of the OB flip-flops. (The reader may recall that the OB's served as a 5-bit buffer register for incoming codes during INPUT operations.)

F-6b The means of loading the OB's with information is a function of the FORMAT, which is actually a program consisting of a series of instructions known as FORMAT CHARACTERS. The FORMAT CHARACTERS are 3-bit commands and are interrogated and obeyed in a fixed sequence.

F-6c Assuming that the desired output codes appear in the OB's, one of the output media will respond to them. Which output medium will respond to the codes is a function of the particular SLOW-OUT operation selected. As Drawing 3 indicates, the TYPEWRITER, the paper tape PUNCH, and the CA-1 CARD EQUIPMENT are the different options. The OC flip-flops determine which medium will receive an "execute" pulse and respond to the code in the OB's. The PUNCH switch on the front of the TYPEWRITER enables the PUNCH to operate whenever the TYPEWRITER is operated as an output medium.

THE SLOW OUTPUT MEDIA

F-7a TYPEWRITER: The TYPEWRITER has already been mentioned as an INPUT device. In this case activation of the keys was manual. When the TYPEWRITER serves as an OUTPUT medium, the keys are electrically activated by means of solenoids.

F-7b Drawing 43 illustrates the 21 solenoids which can be energized by computer control. These include data and control functions. Which one of the 21 solenoids will be energized by the computer is a function of the contents of the OB flip-flops.

F-7c All solenoids are returned to +160V. Relays RY1-RY5 follow the contents of the OB's. The relay points, in accordance with the configuration of the relays, will complete a path from the points of RY6 either to one or none of the solenoids. If and when RY6 is energized by an "execute" pulse, its points will apply ground to the input of the path just described and energize one solenoid or none at all depending upon the contents of the OB's. Obviously, a code in the OB's representing a given function will result in the activation of the corresponding key (i.e., $10011_{OB} = 3$, therefore the "3" key is pulsed).

F-7d The same codes that appear at INPUT can be delivered to OUTPUT. There is no purpose in the typewriter responding to three of these codes, therefore no accommodations are made for activation of any solenoids in these cases. The codes are: WAIT, RELOAD, and STOP. (Ref. dwg. 46)

F-7e Whenever any key is operated, the associated switch contacts close. This raises the HC signal mentioned in SLOW-IN. The HC signal is used as feedback to indicate to the SLOW-OUT circuits whether the typewriter is ready for a new code. All keys which are subject to solenoid activation except SPACE and PERIOD yield LEVEL signals from the TYPEWRITER OUTPUT MATRIX. SPACE and PERIOD raise HC independently of the levels to provide the necessary feedback signal (see sec. F-3e).

F-7e' The switch contacts associated with each key remain closed for the duration of the operation of the typing mechanism, hence supply an ideal feed-back signal. In the cases of TAB and CARRIAGE RETURN, different methods of providing switch contact are provided to render contact for the entire duration of the operation. In the case of TAB, two switches in parallel are required such that one or the other or both will be in contact for the duration of the operation.

F-7f A SPACE KEY, as opposed to the SPACE BAR, is used to shift the carriage one space. This key activates a typing lever as any other character key but no character is typed; the carriage merely shifts. The reason for avoiding use of the SPACE BAR is that it is designed to cause multiple spacing if held down more than a short time.

F-7g The SLOW-OUT system is designed to operate the typewriter at an average rate of approximately 8 characters/second (i.e., 1 character/4 drum cycles). The OB's and the "execute" pulse energize the associated TYPEWRITER relays by means of puller tubes located in the LOGIC CHASSIS (dwg. 62.)

F-7h THE PUNCH: The PAPER TAPE PUNCH is a standard FLEXOWRITER punch unit. Reference is directed to FLEXOWRITER literature for a detailed description. In brief, the unit perforates tapes conditionally in 5 levels and unconditionally in the sprocket level whenever it is pulsed. The punching in 5 levels is a direct function of the contents of the OB flip-flops (which contain the output code). Whenever a frame is punched, the tape is advanced 1/10 inch by a sprocket wheel.

F-7i The punching is under the control of six 2D21 thyratrons located behind the PUNCH unit. Ref. Drawing 47: Five of these thyratrons control the LEVEL SOLENOIDS; the sixth (V6) controls the CLUTCH SOLENOID. Whenever the GRID #1 common becomes high (1 millisecond approx.), the CLUTCH SOLENOID thyratron is unconditionally fired and the other thyratrons fire as a function of the OB's.

F-7j When the CLUTCH SOLENOID is energized a mechanical cycle proceeds, punching the appropriate levels and sprocket and also advancing the tape. During this cycle a cam-controlled switch opens, removing B+ from the thyratron plate circuits extinguishing them at the appropriate time. An INTERLOCK switch can also remove B+ to prevent thyratron firing in the event that the tape supply reel is empty.

F-7k The CLUTCH SOLENOID may be energized continuously by means of a manually-controlled switch on the PHOTO-TAPE READER front panel. This causes the PUNCH to punch blank tape in an un-interrupted manner.

F-71 PUNCH PULSES (1 millisecond) are delivered to the PUNCH thyratrons by the OUTPUT SYSTEM at a rate of one every two drum cycles (i.e., 17/sec.) provided the OC configuration or the PUNCH switch (on the TYPEWRITER) calls for them. The PUNCH requires no synchronization. It will respond properly to each PUNCH PULSE provided the pulses do not exceed the maximum permissible rate. 17/sec is safely below that rate.

F-7m A detailed schematic of the punch driver circuit may be found on Drawing 51. SW1, both sections of which are shown on this drawing, permits the operator to turn the PUNCH MOTOR and B+ supply off. This switch may be turned off to avoid running the PUNCH MOTOR when programs being run do not call for any PUNCH OUT operations. The switch is located on the PUNCH CHASSIS itself.

F-7n CARD EQUIPMENT: The CA-1 CARD EQUIPMENT consists of an IBM 026 unit with adapting circuits. The adapting circuits are fed by the contents of the OB's by means of relay puller tubes located in the LOGIC CHASSIS (dwg. 62). Control signals also arise in the OUTPUT system as a function of the OC's and also energize relays by means of puller tubes. Since the CARD EQUIPMENT is optional accessory equipment and is a study in itself, no more details of the equipment itself will be given in this particular manual. Study of the G-15D circuits will reveal that characters are delivered to the CARD PUNCH at the rate of 1 character/3 drum cycles ---- (i.e., approx. 12 char./sec.).

SLOW-OUT LOGIC

F-8a In order to permit maximum flexibility in controlling the sequence and nature of codes to be supplied to the OB's, 8 different operations may be called for by means of the individual FORMAT CHARACTERS (instructions) in the FORMAT (sequence of instructions). Since both LINE 19 and AR can supply the output data, independent FORMATS may be established for each. The formats are stored in words 0-3 of LINE 2 (for LINE 19) and LINE 3 (for AR); the OC configuration will decide which FORMAT will be followed.

F-8b The 8 FORMAT CHARACTERS (instructions) are listed on Drawing 50. Below is an outline of activity resulting from each character. Assume that at the beginning of each code-to-OUTPUT cycle a FORMAT character will reside in a 3-bit static register, consisting of the OF flip-flops, and will be decoded and interrogated.

ACTION RESULTING FROM FORMAT CHARACTERS (Ref. Dwg. 52)

F-8c $[\text{DIGIT}]_{OF}$: The output line (M19 or AR) will be precessed through the four OA flip-flops for a recirculation cycle. This results in: (1) the highest order 4 bits (hex. character) residing in the OA's, (2) the original contents of the line shifting to the left 4 bit positions, and (3) all ZEROS in the lowest order 4 bit positions of the line. (The latter is accomplished by resetting the OA's prior to the precession.) After the highest order 4 bits are obtained in the OA's, (M) transfers them to the lowest order four OB's, (OB1-OB4), simultaneously resetting the OA's. OB5 will be set to ONE

at this time (if it is not already set) provided the OA data was non-ZERO or if the OC configuration or PUNCH switch called for a PUNCH TAPE or PUNCH CARD.

F-8d These conditions pertaining to OB5 control facilitate suppression of insignificant ZEROS. That is, if an all-ZERO code from the OA's is placed in OB1-OB4, and OB5 is not set, the resulting code (00000) will cause the typewriter to SPACE rather than TYPE "0". Whenever the PUNCH or CA-1 CARD EQUIPMENT is involved, the zero suppression circuit is disabled (by OC2+⟨MAN PUNCH⟩), and OB5 will be high for any hex. character. A ZERO will appear as 10000 in the OB's, hence "0" will be typed out whether significant or not. More will be mentioned on the subject of zero suppression as the other FORMAT CHARACTERS are discussed.

F-8e $[\text{SIGN}]_{OF}$: During SLOW-OUT operations the OS flip-flop monitors the sign bit position of the word being sent to output. In the case where AR constitutes the output line, the T1 position of AR is periodically monitored; when LINE 19 is the output line, the T1 position of word 107 of LINE 19 is monitored. This is under the control of the OC's and appropriate timing signals.

F-8f When the FORMAT CHARACTER calls for SIGN, if the OS flip-flop has been set, OB1 will be set at Ⓜ time; the remaining OB's will all remain reset. This will yield a 00001 configuration which is the MINUS SIGN code. Had the OS flip-flop been in the reset state at this time (representing +), the OB's would have assumed a 00000 configuration, representing a SPACE.

F-8g No AR or LINE 19 precession takes place during this operation. When a SIGN-to-OUTPUT is called for, the word involved should be in its initial state (i.e., not shifted) to assure that the sign position actually contains sign information rather than some other bit which appeared there as the result of previous shifting operations. The OS flip-flop merely monitors whatever bit happens to be in the sign position whether or not it actually represents a sign.

F-8h $[\text{CR+TAB}]_{OF}$: When either a TAB or CARRIAGE RETURN constitutes the FORMAT CHARACTER, the same SLOW-OUT activity takes place, the only difference being in the exact code sent to the OB's for control of the output medium. A CR or TAB is ordinarily called for at the end of every word transmitted to the OB's. At this time, normally a total of 28 bit positions of shift have been experienced by the line (M19 or AR) supplying the output information. An additional bit of shift is appropriate for positioning purposes only.

F-8i The operation calls for a 1-bit precession of the appropriate output line through OA1 only, and lasting for one recirculation time of the line in question (M19 or AR); also, at Ⓕ time, the FORMAT CHARACTER itself is copied from the OF's to OB1-OB3. OB4 and OB5 will be reset. As a result, a 00011 configuration will appear in the OB's as a result of a TAB or 00010 in the case of CARRIAGE RETURN.

F-8j $[\text{STOP}]_{OF}$: The last character of a FORMAT should be STOP (sometimes called END). In the case of AR feeding OUTPUT, the STOP code in the OF's is copied into the OB's yielding the 00100 configuration in the OB's -- the STOP

code. Also the OC flip-flops will be reset, terminating the OUTPUT operation.

F-8k If LINE 19 feeds the output, as soon as the STOP code appears in the OF's, LINE 19 is interrogated. If during the course of one drum cycle any ONES are detected in LINE 19, OF1 is set, converting the STOP code to a RELOAD code. As LINE 19 is precessed and its contents sent to output, ZEROS are inserted in its lowest order end. This is accomplished every time a precession takes place by resetting the OA's prior to each precession. When the contents have been "emptied into output" and there is no more information left, this is an appropriate time to terminate the OUTPUT operation. If LINE 19 is "empty", the STOP code will remain in the OF's, be copied into the OB's, and the OC's will be reset (as in the case of AR to OUTPUT).

F-81 In the event that upon interrogation of LINE 19, a "1" converted the STOP code to a RELOAD code, the procedure will follow that outlined below.

F-8m $[\text{RELOAD}]_{OF}$: When a RELOAD code appears in the OF's, at the time of interrogation (i.e., after the conversion process above), the code itself is sent to the OB's yielding a 00101 configuration. Also the OD flip-flop is set, which causes a repetition of the entire FORMAT (i.e., after the RELOAD operation is performed, the FORMAT CHARACTERS will be interrogated again, starting with the first character.

F-8n RELOAD codes in the OF's normally arise only as the result of a converted STOP code. RELOADS placed in a FORMAT by the programmer would result in an OUTPUT operation which could not terminate itself. RELOADS can be used in conjunction with a "SET READY" command for certain special purposes, but a thorough understanding of the conditions and timing involved in SLOW-OUT is a pre-requisite.

F-8o $[\text{PERIOD}]_{OF}$: This calls for copying the OF's into OB1-OB3, yielding the 00110 configuration in the OB's. This is for the purpose of editing typed copy. As a byproduct of the operation, OB5 is set when OB1-OB4 are cleared (after the response to the PERIOD code by the output medium). This stops zero suppression so that any "0" code following the period will be typed as "0".

F-8p $[\text{WAIT}]_{OF}$: This is strictly an editing function to cause the typewriter to ignore (skip) a hex. character in the output line. WAIT calls for a 4-bit precession just as a $[\text{DIGIT}]_{OF}$ does; however, the character obtained in the OA's is ignored. Instead of sending the character in the OA's to the OB's, the WAIT code in the OF's is copied into the OB's, yielding the 00111 configuration. The TYPEWRITER will not respond, but the PUNCH will punch 00111. (Should the tape be used for INPUT, the WAIT code will compensate in INPUT for the 4-bit precession in OUTPUT by inserting a hex. ZERO in LINE 23.)

F-8q SUMMARY OF FORMAT CHARACTER ACTION: A brief outline of the activity mentioned above is provided on Drawing 53. Drawing 46 illustrates the response of the PUNCH and TYPEWRITER to the codes in the OB's assuming that an "execute" pulse is delivered to the medium. A space punched on PAPER TAPE is insignificant since it represents only a frame of blank tape.

F-8r Standard FORMATS are illustrated on Drawing 50. The FORMAT used for LINE 19 output yields a tape, the sequence of characters upon which renders it compatible with the INPUT SYSTEM. Any FORMAT sequence may be written by the programmer and is limited only by his imagination and/or computer

restrictions.

F-8s (note that FORMAT CHARACTERS listed on dwg. 50 appear in reverse as to order of digits when appearing in the OF's or the lowest order three OB's (dwg. 53). This is a function of the circuit wiring and is a minor technicality resulting in no logical discontinuity--the placement of bits is only arbitrary anyway.)

SLOW-OUT TIMING

F-8t (Ref. dwg. 52 - bottom) Primary timing signals are provided by flip-flops OZ, OY, OE, and OG. Configurations of these flip-flops qualify gates which provide other timing signals. Activity of these circuits is illustrated on the timing diagrams shown on Drawings 54 and 55.

F-8u A basic character output cycle involves two drum cycles beginning with the OY·$\overline{OE}$ configuration and concluding with the OY·OE configuration. In the event that the TYPEWRITER or CARD PUNCH is involved in the OUPPUT operation, time is "killed" between character cycles in the $\overline{OY}$·$\overline{OE}$ configuration to the extent of an integral number of drum cycles as a function of OC and feedback control as follows:

PUNCH: no delay; OY is always high.

CARD PUNCH: one drum cycle delay. This is introduced by "TYPE" signal (present if OC's = 1011) which causes OY to be reset at the conclusion of each basic cycle yielding $\overline{OY}$·$\overline{OE}$. One drum cycle later OY is set ($\overline{HC}$ is high) establishing OY·$\overline{OE}$ which begins a new cycle.

TYPEWRITER: two or more drum cycles delay. "TYPE" (present with OC's = 1000 or 1001) causes OY to be reset, yielding $\overline{OY}$·$\overline{OE}$. When the TYPEWRITER is executing a mechanical cycle, HC will be high until it is concluded. Until HC drops and $\overline{HC}$ becomes high, OY cannot be set. If DIGIT, SIGN, CR, or TAB is the FORMAT CHARACTER being processed, $\overline{OF3}$ (function of the FORMAT CHARACTER) will prevent OY from being set after one drum cycle delay (regardless of TYPEWRITER feedback) by holding HC high. After one drum cycle delay, TYPE·$\overline{OY}$·$\overline{OE}$·TO sets OF3, dropping HC, provided TYPEWRITER switches do not hold it high. Once HC drops, OY can be set, starting a new cycle. HC may be kept high indefinitely by ⟨SA⟩, hence the ENABLE switch provides a means of interrupting a TYPE OUT or CARD PUNCH.

F-8v At the beginning of each cycle (OY·$\overline{OE}$), OG controls the circuit which obtains the new FORMAT CHARACTER in the OF's. The character is interrogated and its process is executed. The OB's do not receive the output code until the conclusion of the 2 drum cycle period, and the "execute" pulse is not delivered to the medium to cause response until the beginning of the following

character cycle. Therefore while the output medium is responding to one code, the SLOW-OUT circuits are obtaining the next.

OBTAINING FORMAT CHARACTERS

F-8w The FORMATS are stored in words 0-3 of LINES 2 and 3. The OC's determine the line from which FORMAT should be taken. When the SLOW-OUT operation is initiated, OD is set. The first OG output will cause the appropriate line (M2 or M3) to be read via the three OF flip-flops into the four-word line, MZ, during word times 0-3. (OD, in conjuction with the OC's, sets up the path; OG determines the time.) As a result of this, the highest order 3 bits of word 3 (of LINE 2 or 3) will reside in the OF's and the remaining information (originally in words 0-3 of LINE 2 or 3) will reside in MZ, displaced 3 bits to the left. The lowest order end of MZ, containing information to the right of the STOP code, is logically unimportant. The operation does not disturb the contents of the selected format line (M2 or M3).

F-8x This first FORMAT CHARACTER in the OF's will be interrogated and the process for which it calls will be executed. When the next FORMAT CHARACTER is called for (when OG rises), OD will be in the reset state (unless the first format character was a RELOAD--which is ridiculous). $OG \cdot \overline{OD}$ will cause MZ to precess through the OF's obtaining the next 3-bit character in the OF's and shifting MZ to the left 3 more bit positions.

F-8y This activity repeats until a RELOAD code appears in the OF's. A RELOAD sets OD causing the initial process to be repeated.

F-8z (Note that OG is set by a T1 pulse of word time 0 and reset by $TF \cdot OG$. This means OG will be high during word times 0-3 except for the T1 period of word time 0. This is one pulse period short of the desired four word times; however, this will only affect MZ to the extent that the T1 position of word 0 will always contain whatever was originally in that bit location of MZ. It will not affect the FORMAT CHARACTERS and their positioning in any respect.)

F-8aa At this point the reader should be able to trace through any SLOW-OUT activity by referring to Drawings 52 - 55. In Drawings 54 and 55 the key signals are shown in reference to the time axis - an important factor in understanding the activity. The reader is advised to draw colored lines between corresponding TO dots at the top and bottom of each drawing. The signals are labelled at the left in abbreviated form. (For instance, the signal $\textcircled{M} = \textcircled{N} \cdot \overline{OE} \cdot$ SLOW-OUT, where $\textcircled{N} = T1 \cdot OZ$. The label on dwg. 55 defines $\textcircled{M} = \overline{OE} \cdot OZ \cdot T1$, which is incomplete. SLOW-OUT also qualifies $\textcircled{M}$; however, the reader is expected to take such a term for granted since the operation is a SLOW-OUT. When in doubt, consult the more detailed drawings.)

MISCELLANEOUS (SLOW-OUT):

F-8ab (1) $\langle A \rangle \langle SA \rangle \cdot \textcircled{N}$ sets OD in addition to setting the OC's. This is the manual method of initiating TYPE OUT AR. OD must be set by the above signal since $S2 \cdot DS$ will not be present to do so as in the case of program-initiated SLOW-OUT operations. Also, until the ENABLE switch is turned off, no type-out will occur since HC will be held high by $\langle SA \rangle$.

F-8ac (2) When the PUNCH is the output medium, one frame of blank tape will be punched prior to the first data element in the OB's. Suppression of this initial insignificant PUNCH "execute" pulse would have involved extra cost to conserve absurdly small amounts of paper tape. OD inhibits the corresponding TYPEWRITER "execute" pulse to prevent a SPACE, but in so doing inhibits the "execute" pulse when RELOAD is the code in the OB's. This is tolerable in the case of the TYPEWRITER since it does not respond to RELOAD anyway; in the PUNCH case it would be intolerable since RELOADS must be punched to render the output tape compatible with the INPUT SYSTEM.

F-8ad (3) After a STOP code has been obeyed as the final FORMAT CHARACTER, the three bits that follow it in the format line will appear in the OF's. $[\overline{STOP}]_{OB}$ is applied to the Ⓑ, Ⓘ, and Ⓟ terms to prevent simultaneous set and reset terms from being applied to the OB's at OC_r time. This could result in malfunction of a subsequent PUNCH operation. The most fool-proof method of writing formats is to follow the STOP code with a SIGN code.

F-8ae (4) In any of the cases in which the OC configuration calls for a TYPE-OUT, an "execute" pulse may also be delivered to the PUNCH if the PUNCH SWITCH on the typewriter is in the ON position - raising <MAN PUNCH> to OV. In such a case, the output speed is a function of the typewriter and the ZERO-suppression is disabled.

FAST-OUT - GENERAL

F-9a The active FAST OUT operations only involve optional auxiliary equipment--MAGNETIC TAPE and the HIGH SPEED PUNCH.

F-9b READY: A passive FAST OUT "operation" is the READY STATE. Programming SET READY merely resets the OC's and establishes the READY STATE by qualifying the READY gate ($\overline{OC1}\cdot\overline{OC2}\cdot\overline{OC3}\cdot\overline{OC4}\cdot\overline{OD}$). The signal "READY" lights a front panel neon "R" in an unusual way. Most neon exciting signals in the G-15D involve approximately a 60V difference between ON and OFF. The READY signal involves a difference of 20V since it is the output of a conventional AND gate. This signal (OV or -20V) is used to turn a neon exciter triode on or off. This triode is located in the LOGIC CHASSIS (dwg. 62).

MAGNETIC TAPE WRITE (FAST-OUT)

F-10a This FAST-OUT operation delivers data to the magnetic tape unit(s) at the peak rate of 463 characters/second. There is no flexibility in output format as there is in the SLOW-OUT system. The sequence in which data is sent from LINE 19 to the MAGNETIC TAPE equipment is:

> 29 HEX. CHARACTERS followed by either a RELOAD or a STOP depending upon whether or not LINE 19 is empty.

F-10b The flexibility in SLOW-OUT was available since the individual output code cycles were of long duration (minimum of 2 drum cycles). However, there is no need for flexibility in the FAST-OUT sequence since the fixed format which is followed supplies a code sequence to MAGNETIC TAPE which is compatible with the INPUT SYSTEM. The purpose of the MAGNETIC TAPE equipment is primarily storage. That is, if a 108 WORD BLOCK is written on the tape

from LINE 19, it may be restored to LINE 19 later by an INPUT operation. The fixed format fulfills this requirement.

F-10c In general, the sequence calls for "unloading" LINE 19, in 4-word groups, onto MAGNETIC TAPE. The manipulation of the 4-word groups is almost a SLOW-IN operation in reverse.

F-10d Ref. dwg. 61: To facilitate the sequence above, LINE 19 is precessed through MZ for 108 word times (starting with word time 0). This results in: (1) the original contents of words 104-107 of LINE 19 residing in MZ, (2) the original contents of LINE 19 being shifted left 4 words, and (3) the lowest order 4 words of LINE 19 being filled with ZEROS (original contents of MZ - rendered all ZEROS by proper programming of the initiating command).

F-10e Once MZ has extracted the highest order 4 words from LINE 19, MZ is copied into LINE 23, freeing MZ to obtain the next highest order 4 words of LINE 19 (synchronized on the next TO pulse).

F-10f With the original highest order 4 words now in LINE 23, precessions of LINE 23 through the OA's proceed on alternate 4-word recirculation cycles. During the 4-word recirculation cycles between precessions, the OA's will contain 4-bit configurations starting with the highest order hex. character and progressing sequentially to the lowest order hex. character. During the time that these hex. characters are static in the OA's, an "execute" pulse permits AND gates to send them to the writing circuits in the MAGNETIC TAPE equipment (see dwg. 60 - top). These "execute" pulses last 4 word times or approximately one millisecond. This takes care of LEVELS 1-4. LEVEL 5 is written any time the information written on tape is a hex. character.

F-10g A means is provided to determine when 29 hex. characters (i.e., the entire contents of LINE 23) have been written on tape. This involves turning OA2 on (by Ⓩ) prior to the precession which obtains the first hex. character in a 29 character group. This is known as the MARKER BIT. As a result of this, after the first precession, the 0100 configuration will have been written in the lowest order 4 bit positions of LINE 23. Prior to any other precession the OA's are reset to 0000.

F-10h During the course of the first 29 precessions, the MARKER BIT established in OA2 (by Ⓩ) will be transmitted to the writing station of M23. Only after the 29th precession (i.e., during the 30th) will the MARKER BIT fail to reach M23w. OF1 monitors OA4 during each precession. During the first 29 precessions OF1 is set, and remains set between precessions causing 5th LEVEL to be written. After the 30th precession, OF1 remains down, failing to write 5th LEVEL. The configuration in the OA's at this time is 0100. Since 5th LEVEL is not written, the tentative configuration of the LEVELS to be written on tape is 00100; however, $OB3 \cdot \overline{OF1}$ can qualify the LEVEL 1 gate which could result in a 00101 configuration.

F-10i For a period of more than one drum cycle prior to establishment of the above code, an $OB3_s$ gate searched LINE 19 for ONES. If LINE 19 contained any ONES, OB3 would be set; if it contained no ONES, OB3 would remain reset. Since OB3 controls writing of LEVEL 1 at this time, and LINE 19 controls OB3, an "empty" LINE 19 will cause a 00100 configuration (STOP code) to be written; otherwise 00101 (RELOAD code) will be written. This resembles

the activity in the SLOW-OUT system when $[STOP]_{OF}$ is the FORMAT CHARACTER; the means, however, differ considerably.

F-10j Had the RELOAD code been written, the next 4-word group residing in MZ (resulting from the second M19 - MZ precession) would be copied into LINE 23 and the 29 HEX. CHARACTER - STOP/RELOAD cycle would repeat.

F-10k These 4-word cycles will repeat until LINE 19 is exhausted of information. Normally 108 words of LINE 19 will contain data, hence 27 4-word cycles will occur. If the tape-recorded data from LINE 19 is, at some future time, to be read back into LINE 19 in the same relative word positions, at least one ONE should exist in the original lowest order 4-word group of LINE 19. Simple programming can assure this. The operation is concluded after the STOP code is written and the OC's are reset, establishing READY.

F-10l Drawing 60 is the FAST-OUT block diagram covering the MAGNETIC TAPE WRITE case. Drawing 61 provides an example of a writing operation in which only the highest order 8 words of LINE 19 contain data. Beyond this, little can be said about the data handling logic.

F-10m MAGNETIC TAPE motion control as applied to MAGNETIC TAPE WRITE is a simple matter as far as the G-15D circuits are concerned. Ref. Drawing 60 - top: DS·SO·SV (high during the time of TRANSFER associated with the initiating command) will fire the FORWARD thyratron in the electro-mechanical tape transport system. The tape will be accelerated to its normal speed of 7.5 in/sec in approximately 5 milliseconds. How soon data will appear to be written on the tape is a function of the word time during which the initiating command is in the TRANSFER state; this should be WORD 0 to assure maximum leader.

F-10n The tape transport mechanism is stopped by the READY signal which fires the STOP thyratron.

F-10o The MAGNETIC TAPE recording mode is similar to that employed by the drum in that only ONES are written and ZEROS are erased magnetic surface. Any section of tape which is selected for recording must be erased. This is accomplished by bulk erasure.

MAGNETIC TAPE READ CONTROL (SLOW-IN)

F-11 MAGNETIC TAPE has already been mentioned as a source of INPUT data; however, its control was not mentioned at that time. Ref. Drawing 47 - lower right: Control of the mechanism is similar to the MAGNETIC TAPE WRITE case. DS·S3·SV (high during the TRANSFER state of the initiating command) fires the FORWARD thyratron. The tape will move past the READ-WRITE head resulting in codes being read into the INPUT system. Finally, when a STOP code reaches the OB's, $\textcircled{S} \cdot [STOP]_{OB}$ will fire the STOP thyratron; this minimizes tape travel after the STOP code is detected. (The READY signal, which normally stops the tape, will not appear until 1 - 2 drum cycles after the STOP code is received since this much time must be allowed for the MZ - M19 precession associated with a STOP code.) There are no restrictions on TRANSFER timing. Once the tape is in motion (7.5 in/sec.), data previously recorded on it will appear in terms of LEVEL signals at the same character rate that was established in the writing operation.

MULTIPLE MAGNETIC UNITS

F-12a CHARACTERISTIC qualification: Up to four MAGNETIC UNITS may be attached to one G-15D. The one selected to be active during a MAGNETIC INPUT-OUTPUT operation is a function of the CHARACTERISTIC bits of the initiating command. The CHARACTERISTIC to which a unit will respond is selected by a 4-position switch on the unit itself as shown on Drawing 47.

F-12b When more than one MAGNETIC UNIT is attached to a G-15D, the units are "chain-wired". Input and output wires are connected to two connectors on each MAGNETIC TAPE UNIT. In this way, the G-15D itself only requires one connector for MAGNETIC equipment.

F-12c The LEVEL output stages of each unit are cathode-followers. Connecting the outputs of each unit in parallel constructs cathode-follower OR gates, hence no additional mixing circuits are required. Only one unit should be operated as a reader at any one time; however, more than one can be simultaneously writing in the event that duplication is desired.

MAGNETIC TAPE WRITE FILE CODE

F-13 The 6th LEVEL on MAGNETIC TAPE is available for FILE CODES, which may be used to locate information blocks or groups of blocks. Just where these FILE CODES are written is a function of the controlling program in the G-15D. Once written, a FILE CODE may be used as the object of a SEARCH operation (for tape positioning purposes). Writing a FILE CODE does not involve tape motion. $DS \cdot S7 \cdot SW$, which arises during the TRANSFER state of the WRITE FILE CODE command, qualifies the 6th LEVEL writing circuit in the magnetic unit selected by the CHARACTERISTIC code. TRANSFER must last for 4 word times to yield a 1 millisecond writing pulse; there are no restrictions as to when these word times can occur during a drum cycle.

MAGNETIC TAPE SEARCH

F-14a TAPE SPEED: 0100 or 0101 in the OC's yields the signal "FAST". This turns on a pair of relay puller triodes in the tape unit energizing the FAST relay (see dwg. 47). This relay reconnects the windings of the multi-pole capstan drive motor in the tape transport mechanism such that its angular velocity is increased by a factor of 6:1. This means that the tape, when in motion, will be driven at a rate of 45 inches/sec (i.e., 6 x 7.5 in/sec).

F-14b FORWARD or REVERSE: Regardless of direction, when the tape reaches a FILE CODE, a 6th LEVEL output will arise. If the TRANSFER state of the initiating command is not still high, the 6th LEVEL output signal will set OF3 which will reset the OC's. This yields READY, which fires the STOP thyratron.

F-14c The $\overline{DS \cdot S1}$ term, which qualifies the $OF3_S$ gate, permits the system to ignore FILE CODES existing close to the point on the tape from which the search starts. By programming the duration of TRANSFER the programmer can render the search selective to different degrees.

F-14d FORWARD SEARCH: $DS \cdot S1 \cdot SV$ (if qualified by CHARACTERISTIC) fires the FORWARD Thyratron; READY fires the STOP thyratron.

F-14e REVERSE SEARCH: DS·S1·SU (if qualified by CHARACTERISTIC) fires the REVERSE thyratron; READY fires the STOP thyratron.

TIME ALLOWANCES - MAGNETIC

F-15a A MAGNETIC TAPE READ or WRITE should not directly follow a SEARCH. The capstan drive motor requires time to decelerate from FAST to SLOW. A few drum cycles should be allowed in accordance with programming rules. This holds true even if different MAGNETIC TAPE UNITS are involved since all capstan motors are subject to FAST control regardless of CHARACTERISTIC code.

F-15b A MAGNETIC TAPE READ should not follow a MAGNETIC TAPE WRITE by less than a few drum cycles in accordance with programming rules. A writing operation saturates the reading amplifiers in the MAGNETIC TAPE UNIT and recovery time must be allowed. As a matter of fact no INPUT operation should immediately follow a MAGNETIC TAPE WRITE since the MAGNETIC TAPE reading circuits, until stabilized, will disturb the INPUT LEVELS and HC.

FAST PUNCH LINE 19 (FAST-OUT)

F-16 Provisions are built into the G-15D to handle a high speed (60 character/sec) TELETYPE punch and adapting circuits. The data handling circuits are the same FAST-OUT circuits employed by MAGNETIC TAPE except for a synchronization circuit which slows down the character output rate. Details of this system are available in literature dealing with the accessory itself.

FAST PUNCH LEADER (FAST-OUT)

F-17 This is identical to the FAST PUNCH LINE 19 operation except that the "execute" pulse is not generated. The PUNCH nevertheless will feed frames of blank tape at 60 frames/sec (i.e., 6 in/sec) as long as the OC's are set in the 0010 or 0011 configuration. How long this operation will last, hence how much blank tape is fed, is a function of the LINE 19 data. Other literature elaborates on this feature.

SECTION G

POWER SUPPLIES AND TURN-ON CYCLE

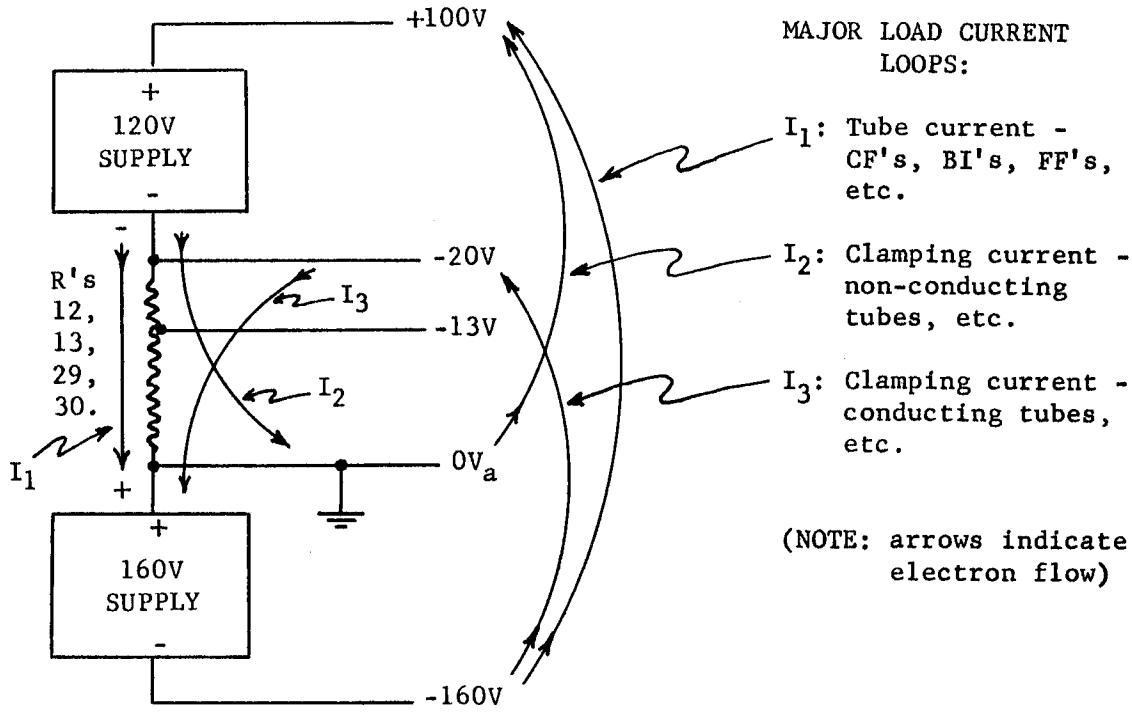
The circuits described in this section introduce no new logical concepts, but do require a reasonable knowledge of some circuits previously described.

POWER SUPPLIES

G-1a Four D.C. power supplies supply all of the necessary D. C. potentials to operate the computer. These supplies will yield their outputs, provided their primary circuits are connected to A.C., by a relay (K3) associated with the TURN-ON system. The four supplies are all conventional full-wave bridge rectifiers terminated with choke input filters and yield outputs as follows:

+ 250V	for writing pentodes and the CLOCK CHASSIS
+ 160V	for relays and solenoids
+ 120V - 160V	for +100V, OV, -13V, -20V, and -160V to supply the logic circuits (The -25V and -75V supplies for READ CLOCK are parasites on the +100V and -160V supplies - ref. B-3h-j.)

G-1b The +120V and -160V supplies are interconnected in terms of load current loops and form the circuit shown below:



G-1c This hookup yields four stable output voltages by means of only two supplies. Drawing 58 shows the details of the arrangement.

G-1d The ground returns for +250V, +160V, and [+120V and -160V] are OV_c, OV_b and OV_a respectively. They are all at OV as far as D.C. is concerned but not necessarily in terms of RF (i.e. transients). By using separate ground returns, the transient problem is reduced.

G-1e The average load presented by the logic circuits is steady since, on the average, whenever one tube cuts off, another turns on. Deviations from this average may be expected to be of very short duration. At any rate, generous amounts of filter capacitance shunt every supply, rendering them tolerant of changing load requirements and relatively immune to line voltage transients unless they are of unreasonable proportions.

G-1f Since these supplies are unregulated, their output levels are a function of line voltage. Line voltage is adjustable by means of a variable transformer (front panel control), the output of which supplies a boost to the line by means of T4 (dwg. 56 - left). The adjusted (boosted) AC feeds the primary circuits of the power supply transformers and the filament transformer. The motors employ AC directly from the line since they are not critical. The variable transformer is adjusted for a 6.3V indication on the filament voltmeter.

G-1g Gradual drifts in line voltage may be compensated for by manually adjusting the variable transformer; however, should this become a problem, a line voltage regulator is recommended. Should the line voltage be subject to unreasonable dips and/or interruptions, rotary machinary (M-G set) is recommended. The G-15D is tolerant of sizable deviations in line voltage, but it has its limits. The limits are a function of how effective the scheduled maintenance activities are. Ordinarily a G-15D should be expected to tolerate at least 10% line voltage deviations.

G-1h To facilitate scheduled maintenance (marginal checking) activities all supplies are variable by means of front panel controls. Varying the supplies individually can upset circuit constants to the extent that a deteriorating component may be detected and replaced before it fails in normal service. Varying the line voltage transformer reduces all supplies in proportion and also the filament voltage, providing another means of marginal checking.

G-1i A per-cent reading meter is available to monitor all potentials. A switch is provided to connect the supply to be measured in the correct polarity and with the proper amount of multiplier resistance.

G-1j Varying of supplies is accomplished as follows:

+250V: Control C (variac), continuously variable.

+160V: Control B (switch - SW3), 10% drop.

+100V: Control A (switch - SW2), 10% drop.

-13V: Control D (potentiometer - R12), continuously variable.

-20V: Control E (potentiometer - R13), continuously variable - affects - 13V in proportion

-160V: Control F (switch - SW1), 10% drop.

G-1k Controls A and F, when inserting resistance in series with the loads of their associated supplies (to create 10% drop), also adjust the load on the supply

by compensatory resistance to keep power supply current constant. This is necessary since the currents of the +120V and -160V supplies determine the level of the -20V and -13V potentials.

THE TURN-ON CYCLE

POWER

G-2a Drawing 56 illustrates the TURN-ON CYCLE activity and the hardware involved. When power is first applied to the computer, TIMING-MOTOR #1 (TM1) runs, driving a built-in gear train. The output shaft drives a rotary 2-wafer switch which controls relays K1 and K2 as shown on Drawing 56 (upper right). TM1 stops when the K1·K2 configuration is achieved. K1 and K2 control the amount of series resistance in the filament transformer primary circuit, incrementing the filament voltage as shown on Drawing 56 (upper left).

G-2b The system is relaxed when TM1 stops, but is ready to proceed if the D.C. RESET button is pushed. D.C. RESET starts the second phase of the TURN-ON-CYCLE by starting TM2. TM2 with its gear train also drives a rotary switch. This switch has 4 wafers. Shortly after TM2 starts, K3 pulls in, energizing all D.C. power supplies. When this happens, the D.C. RESET button can be released.

G-2c Safety circuits can open K3 and turn off D.C. K5, K6, K7, and K8 provide overload safety features. Also pairs of jumpered points located in each DIODE CLAMP package (points L and M) are chain-wired such that removal of any DIODE CLAMP package will break the chain, opening K3 and turning off D.C. (Naturally, D.C. should have been turned off - by the D.C. OFF button - prior to removal of such a package).

TURN-ON LOGIC (Ref. dwgs. 56, 57)

G-2d As soon as D. C. appears, the ⟨CLEAR⟩ signal rises to make sure the OC's are reset immediately in order to prevent random activation of an INPUT-OUTPUT device. ⟨CLEAR⟩ also resets CQ to assure the first command to be read will be read at word N, rather than N+1 (dwg. 30).

G-2e Then ⟨$\overline{\text{CLEAR}}$⟩ drops to -20V, blocking recirculation of the NUMBER TRACK (CN) to clear it of any ONES.

G-2f Then the signal ⟨$\overline{\text{OP}}$⟩ drops to -20V and ⟨OP⟩ becomes high, resetting the CY flip-flop in the ORIGIN PULSE (i.e. TO) generating circuit to be found on Drawing 57. CY resets at the first clock pulse to detect ⟨OP⟩, and after many drum cycles it will be set when the first clock pulse detects ⟨$\overline{\text{OP}}$⟩.

G-2g While CY was set it caused CE to be set. With CY reset, CE remains set since nothing can reset it - yet. This $\overline{\text{CY}}$·CE configuration permits gate A to write ONES in every T29 position of CN, provided a ZERO is read at the READING FLIP-FLOP ($\overline{\text{CN}}$). When the 109th T29 pulse prepares to write a ONE, the very first ONE which was written appears at the READING FLIP-FLOP (CN) dropping the $\overline{\text{CN}}$ signal and preventing the writing by gate A.

G-2h CN, now present, causes CE to be reset, qualifying recirculation gate B. The information now recirculating consists of ONES in all but one of the

T29 positions. That particular T29 position containing a ZERO may be defined as "TO" (= T29·$\overline{CN}$), the ORIGIN PULSE. Gate B will continue to provide recirculation until ⟨$\overline{OP}$⟩ sets CY; then gate C takes over and the activity of gate B is of no consequence.

G-2i As soon as CY was set, rendering gate C the recirculation path, CE assumed its normal function of being high during EVEN word times and low during ODD. Note that CE cannot be reset at T29·$\overline{CN}$ (i.e. TO) time therefore it will inevitably be high during WORD 0; this is the "locking-in" system assuring CE's proper orientation.

G-2j From this point on, the basic timing signals required to operate the SLOW-IN system are established (i.e. TO and TF).

G-2k ⟨OP⟩ also resets CG, assuring that the first command to be read will not come from AR (dwg. 22).

G-21 The next operation of the TURN-ON CYCLE is the generation of the ⟨AUTO TAPE START⟩ signal. When this signal arises, it sets the OC's to 1111, initiating a PHOTO TAPE READ operation, resulting in LINE 19 obtaining the first block of information from the tape. This should be the desired contents of the NUMBER TRACK.

G-2m The next signal to arise from the motor-driven switch is ⟨NT⟩, which qualifies gate D (dwg. 57). Gate D copies the contents of LINE 19 into the NUMBER TRACK. It is not necessary to block recirculation of the NUMBER TRACK during this operation since it was cleared by dropping ⟨$\overline{CLEAR}$⟩, and the T29 information just established in it is the same as the new information to be copied from LINE 19.

G-2n The next operation in the TURN-ON CYCLE is another automatic PHOTO TAPE READ. This loads the next block of tape information into LINE 19 (and LINE 23), simultaneously making sure the COMMAND LINE is set to 23 and N = 00 (see dwg. 22). This last block of information can be a "LOADING ROUTINE".

G-2o After this operation is concluded K4 pulls in, stopping TM2 and lighting the READY light (green).

G-2p An interlock is provided to stop TM2 if its associated rotary switch needs stopping (to prevent premature signals) while the PHOTO TAPE READER is still operating. The condition of the FORWARD relay in the PHOTO TAPE READER provides this feature.

G-2q From the time the READY lamp lights, the computer is ready for operation. (Do not confuse this READY light with the READY ("R") neon on the neon panel.)

MAINTENANCE SWITCHES

G-3a These switches were mentioned in sec. E-12. Half of them duplicate the functions which are ordinarily provided automatically by the switch sections driven by TM-2. The switches are as follows:

CLEAR NT: duplicates the function of ⟨$\overline{CLEAR}$⟩. That is, it blocks recirculation of the NUMBER TRACK, clearing it of any ONES.

It does so by shorting the true output of CN to -20V; unusual, but effective.

SET OP: duplicates the functions of ⟨OP⟩ and ⟨$\overline{\text{OP}}$⟩ in controlling CY, thereby establishing ORIGIN PULSE (TO) in the NUMBER TRACK.

SET NT: duplicates the function of ⟨NT⟩, applying the LINE 19 reading flip-flop (M19) to the writing station of the NUMBER TRACK.

CLEAR M23: when depressed, drops ⟨$\overline{\text{M23 CLEAR}}$⟩ to -20V, thereby blocking recirculation of LINE 23 - clearing it of any ONES. (dwg. 3D290)

CLEAR M19: when depressed, raises ⟨M19 CLEAR⟩ to 0V, thereby blocking recirculation of LINE 19 - clearing it of any ONES (dwg. 3D290)

SET M19: when depressed, raises ⟨M19 SET⟩ to 0V, thereby qualifying the M19 writing gate ⟨M19 SET⟩·CN, copying the NUMBER TRACK into LINE 19. This does not block M19 recirculation, therefore "CLEAR M19" should be depressed first (dwg. 3D290)

G-3b (The D.C. LOCKOUT toggle switch is a safety switch which renders application of D.C. voltage impossible - ref. dwg. 56. It is particularly useful in preventing complete machine "turn-on" while maintenance procedures are being undertaken.)

SECTION H

APPENDIX

H-1 FUNDAMENTAL OPERATIONS - BOOLEAN ALGEBRA

The system of notation employed for describing the operation of the computer is variously called BOOLEAN ALGEBRA, the PROPOSITIONAL CALCULUS, or LOGICAL ALGEBRA. The basic symbols are letters that, in this case, are interpreted as signals which may have two values, HIGH and LOW. The basic connectives are "+", ".", and " $\bar{}$ ",which approximate the usage of "or", "and", and "not" respectively, in ordinary language. The following tables, called TRUTH TABLES, explain the meaning attached to the connectives, where "1" indicates a high signal and "0" a low signal.

		"OR"	"AND"	"NOT"
A	B	A+B	A·B	$\bar{A}$
1	1	1	1	0
1	0	1	0	0
0	1	1	0	1
0	0	0	0	1

In writing expressions, the following convention may be adopted to reduce the use of parenthesis: "·" binds two symbols more strongly than "+". This, it will be seen, is the same convention adopted in the normal numerical algebra if "·" is treated as "x" (times) and "+" is treated as "+" (plus). For example, the algebraic expression (a x b) + (c x d) is written as a x b + c x d; similarly, the logical expression (A · B) + (C · D) is written as A · B + C · D. Again, $[a + (b \times c)] \times d$ is written (a + b x c) x d and $[A + (B \cdot C)] \cdot D$ is written (A + B · C) · D.

Using the TRUTH TABLE given above, conditions under which a given combination of signals is high may be derived. For example, given the combination of signals

$$D = A \cdot B + (A+C) \cdot (A+\bar{B}),$$

the following table lists the steps employed in deriving the conditions of A, B, and C under which D is high. Note that the first step is to write all possible combinations of the given terms, and that the number of these combinations is 2^n, where n is the number of different letters in the expression.

A B C	A·B	A+C	$A+\overline{B}$	$(A+C)\cdot(A+\overline{B})$	$A\cdot B+(A+C)\cdot(A+\overline{B})$
1 1 1	1	1	1	1	1
1 1 0	1	1	1	1	1
1 0 1	0	1	1	1	1
1 0 0	0	1	1	1	1
0 1 1	0	1	0	0	0
0 1 0	0	0	0	0	0
0 0 1	0	1	1	1	1
0 0 0	0	0	1	0	0

In addition, to determine the conditions under which a given combination of signals is high, it is also desirable that the expression representing a given configuration of signals be in its simplest form. "Simplest" in this case is difficult to define in abstract generality; however, in any given instance the relative simplicity of two forms of a given expression is not difficult to determine. In order to manipulate logical expressions, the following rules are employed:

Associativity	$(A \cdot B)\cdot C = A\cdot(B\cdot C) = A\cdot B\cdot C$	(a)	I
Distributivity	$A\cdot(B+C) = A\cdot B + A\cdot C$	(b)	I
Commutivity	$A\cdot B = B\cdot A$	(a)	II
	$A+B = B+A$	(b)	II
DeMorgan's Law	$\overline{A+B} = \overline{A}\cdot\overline{B}$	(a)	III
	$\overline{A\cdot B} = \overline{A}+\overline{B}$	(b)	III

$$B \cdot (A + \bar{A}) = B \qquad \text{(a)}$$

$$B + A \cdot \bar{A} = B \qquad \text{(b)} \qquad \text{IV}$$

$$A + \bar{A} \cdot B = A + B \qquad \text{(a)}$$

$$A + A \cdot B = A \qquad \text{(b)} \qquad \text{V}$$

$$A \cdot A = A \qquad \text{(a)}$$

$$A + A = A \qquad \text{(b)} \qquad \text{VI}$$

$$\bar{\bar{A}} = A \qquad \text{VII}$$

Consider now the expression: $C \cdot \bar{B} \cdot \bar{A} + C \cdot \bar{B} \cdot A + \overline{\bar{C} \cdot B \cdot A + \bar{C} \cdot B \cdot \bar{A}}$

Applying rules

IIIa $\quad C \cdot \bar{B} \cdot \bar{A} + C \cdot \bar{B} \cdot A + \overline{\bar{C} \cdot B \cdot A} \cdot \overline{\bar{C} \cdot B \cdot \bar{A}}$

IIIb $\quad C \cdot \bar{B} \cdot \bar{A} + C \cdot \bar{B} \cdot A + (\bar{\bar{C}} + \bar{B} + \bar{A}) \cdot (\bar{\bar{C}} + \bar{B} + \bar{\bar{A}})$

VII $\quad C \cdot \bar{B} \cdot \bar{A} + C \cdot \bar{B} \cdot A + (C + \bar{B} + \bar{A}) \cdot (C + \bar{B} + A)$

Ib $\quad C \cdot \bar{B} \cdot \bar{A} + C \cdot \bar{B} \cdot A + C \cdot C + C \cdot \bar{B} + C \cdot A + \bar{B} \cdot C + \bar{B} \cdot \bar{B} + \bar{B} \cdot A + \bar{A} \cdot C + \bar{A} \cdot \bar{B} + \bar{A} \cdot A$

VIa,b $\quad C \cdot \bar{B} \cdot \bar{A} + C \cdot \bar{B} \cdot A + C + C \cdot \bar{B} + C \cdot A + \bar{B} + \bar{B} \cdot A + C \cdot \bar{A} + \bar{B} \cdot \bar{A} + \bar{A} \cdot A$

IVb $\quad C \cdot \bar{B} \cdot \bar{A} + C \cdot \bar{B} \cdot A + C + C \cdot \bar{B} + C \cdot A + \bar{B} + \bar{B} \cdot A + C \cdot \bar{A} + \bar{B} \cdot \bar{A}$

II $\quad C \cdot \bar{B} \cdot \bar{A} + C \cdot \bar{B} \cdot A + C + C \cdot \bar{B} + \bar{B} \cdot \bar{A} + \bar{B} \cdot A + C \cdot A + C \cdot \bar{A} + \bar{B}$

Ib $\quad C \cdot \bar{B} \cdot (\bar{A} + A) + C + C \cdot \bar{B} + \bar{B} \cdot (\bar{A} + A) + C \cdot (A + \bar{A}) + \bar{B}$

IVa $\quad C \cdot \bar{B} + C + C \cdot \bar{B} + \bar{B} + C + \bar{B}$

VIb $\quad C \cdot \bar{B} + C + \bar{B}$

V $\quad C + \bar{B}$

therefore $C \cdot \bar{B} \cdot \bar{A} + C \cdot \bar{B} \cdot A + \overline{\bar{C} \cdot B \cdot A + \bar{C} \cdot B \cdot \bar{A}} = C + \bar{B}$

H-2 FUNDAMENTAL OPERATIONS - BINARY ARITHMETIC

EXAMPLE OF BINARY NOTATION

$118\frac{9}{16}$ is a quantity expressed in decimal notation. It may also be expressed in terms of the following:

$$118\frac{9}{16} = 64 + 32 + 16 + 4 + 2 + 1/2 + 1/16$$
$$= 2^6 + 2^5 + 2^4 + 2^2 + 2^1 + 2^{-1} + 2^{-4}$$

The presence or absence of 2^i in the quantity above may be expressed in terms of "0" and "1" multipliers as shown below. The BINARY POINT indicates the location of 2^0. (This is a binary number.)

$2^n \cdots 2^8 + 2^7 + 2^6 + 2^5 + 2^4 + 2^3 + 2^2 + 2^1 + 2^0 + 2^{-1} + 2^{-2} + 2^{-3} + 2^{-4} + 2^{-5} + 2^{-6} \cdots 2^{-n}$

o $\cdots$ o 0 1 1 1 0 1 1 0 ▲ 1 0 0 1 0 o $\cdots$ o

This may also be expressed in terms of an integral number:

(0 1 1 1 0 1 1 0 1 0 0 1 ▲) x 2^{-4}

- or a fractional number:

(▲ 0 1 1 1 0 1 1 0 1 0 0 1) x 2^8

- or in terms of groups of four binary digits:

(0111.) x 2^4 (0110.) x 2^0 (1001.) x 2^{-4}

- which may be represented by hexadecimal digits (0 - z):

7 x 16^1 6 x 16^0 9 x 16^{-1}

- abbreviated: 76.9_{16}

- conclusion: decimal $118\frac{9}{16}$ = binary 1110110.1001 = hexadecimal 76.9

CONVERSION OF A BINARY NUMBER TO DECIMAL

$$1110110.1001 = 2^6 + 2^5 + 2^4 + 2^2 + 2^1 + 2^{-1} + 2^{-4}$$
$$= 64 + 32 + 16 + 4 + 2 + 1/2 + 1/16 = 118\frac{9}{16}$$

CONVERSION OF A DECIMAL NUMBER TO BINARY

$118\frac{9}{16}$ = ?

118 9/16	
-64	2^6
54 9/16	
-32	2^5
22 9/16	
-16	2^4
6 9/16	
- 4	2^2
2 9/16	
- 2	2^1
9/16	
- 8/16	2^{-1}
1/16	
- 1/16	2^{-4}

2^6 2^5 2^4 2^2 2^1 2^{-1} 2^{-4}

= 1 1 1 0 1 1 0 . 1 0 0 1

▲

ADDITION IN BINARY

AUGEND U	ADDEND D	INPUT CARRY C	OUTPUT CARRY C_s	SUM A
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

EXAMPLE:

CAR.	1		1	1				
AUG.		1	0	1	1	0.	=	22
ADD.		1	0	1	1	1.	=	23
SUM.	1	0	1	1	0	1.	=	45

G-15D NUMBERS (28 binary digits and /sign):

EXAMPLE is decimal $118\frac{9}{16}$ =

.01110110100100000000000000000/0 x 2^8 =(.7690000$_{16}$) x 2^8

or

.11101101001000000000000000000/0 x 2^7 =(.yx20000$_{16}$) x 2^7 (NORMALIZED)

or

.00000000000000000011101101001/0.x 2^{24}=(.0000769$_{16}$) x 2^{24} (lowest order bit = 1/16)

or

.11111111111111111100010010111/1 x 2^{24}=(.zzzz897$_{16}$) x 2^{24} (COMPLEMENTED)

H-3 INDEX OF FREQUENTLY-REFERRED-TO SIGNALS

SIGNAL	ORIGIN	DESCRIPTION AND (REFERENCE DRAWING)
①	G	CHAR. = 1 (23)
②	G	CHAR. = 2 (23)
③	G	CHAR. = 3 (23)
④	G	CHAR. = 0 (23)
AC	FF	ACCUMULATOR REG. CARRY FF (27)
AR	FF	ACCUMULATOR REG. READ FF; also abbrev. for reg. (27)
BP		abbrev. for BREAK POINT (5, 30)
*C1	FF	S/D STATIC FF
*C2-C6	FF's	DESTINATION STATIC FF's
*C7-CV	FF's	SOURCE STATIC FF's (30)
*CX,CW	FF's	CHARACTERISTIC STATIC FF's
CC	FF	COMMAND REG. CARRY FF (22, 27)
*CD's	FF's	COMMAND LINE designators (22)
CE	FF	High during EVEN word times
$\overline{CE}$	FF	High during ODD word times (15)
*CG	FF	"NEXT COMMAND FROM AR" control FF (22)
*CH	FF	START-STOP control FF's (30)
CZ	FF	
CI	BI	COMMAND info. (not inverted) (22)
CM	FF	COMMAND REG. READ FF; also abbrev. for reg. (22, 27)
CN	FF	NUMBER TRACK READ FF; also abbrev. for track (15, 57)
*CQ	FF	TEST FF; when set, next comm. is read from WT=N+1 (30)
CS	BI	"VIA AR" CHARACTERISTIC (26)
D0-D7	G's	DESTINATION designators (23)
DU-DX	G's	
(DA-1		DIGITAL DIFFERENTIAL ANALYZER attachment)
DS	G	TRANSFER when DEST. is 31 (=TR·D7·DX) (23)

* (neon indicator)

Ⓔ	G	selected TF pulse initiating INPUT CODE process (48)
EB	G	abbrev. for EARLY BUS (26, 28)
*FO	FF	OVERFLOW FF (27)
HC	G	sync. signal from INPUT/OUTPUT media (47, 48, 52)
IB	G	abbrev. for INTERMEDIATE BUS (26)
IC	FF	"when to invert" FF in INVERTING GATES (26)
ID		abbrev. for MULTIPLICAND-DENOMINATOR REG. (PJ is READ FF) (34, 36, 40)
*IP	FF	SIGN FF in INV. GATES (for two-word lines) (26, 34, 40)
(IR		abbrev. for INPUT-OUTPUT REG. attachment output)
IS	FF	"whether to complement" FF in INV. GATES (26)
"L"		word-time LOCATION of a COMMAND (5, 20)
LB	G	abbrev. for LATE BUS (26)
MO-M23	FF's	READING FF's of LINES 00-23 (also used as abbrev. for lines) (21)
MQ		abbrev. for MULTIPLIER-QUOTIENT REG. (PR is READ FF) (34, 36, 40)
MZ	FF	LINE Z READ FF; also abbrev. for line (48, 52, 60)
"N"		COMMAND info.: location of NEXT COMMAND (5, 20)
OA's	FF's	4-bit reg. used in INPUT/OUTPUT precession activities (48, 52, 60)
OB's	FF's	5 FF's in INPUT/OUTPUT system - sometimes used as 5-bit reg. (48, 52, 60)
*OC's	FF's	4-bit static reg. used to designate INPUT/OUTPUT operation (45)
OF's	FF's	FF's used for INPUT/OUTPUT control - sometimes as 3-bit reg. (48, 52, 60)
OD,OE,OG,OY		FF's used for INPUT/OUTPUT timing and control (48, 52, 60)
OS	FF	sign handling FF in INPUT/OUTPUT system (48, 52)
OZ	FF	FF high during WORD 00 (52)
PM	FF	monitors T29·CE (2-1) bit at MQ's writing ckt (36)
PN		abbrev. for PRODUCT-NUMERATOR REG. (PP is READ FF) (34, 36, 40)

*READY	G	idle state of INPUT/OUTPUT system (=$\overline{OC1}\cdot\overline{OC2}\cdot\overline{OC3}\cdot\overline{OC4}\cdot\overline{OD}$) (45)
RC	G	abbrev. for READ COMMAND (state or signal) (30)
(S)	G	(E) during SLOW-IN operation (48)
S0-S7 SU-SX	G's G's	SOURCE designators (23)
⟨SA⟩	SW	signal high when ENABLE SWITCH is ON (43)
"T"		COMMAND info.: TIMING NUMBER (5, 19, 20)
T1	FF	sign position of SINGLE PRECISION numbers (15)
TE	FF	sign position of DOUBLE PRECISION numbers (T1·CE) (15)
TF	G	T29 of word times congruent to 3 mod. 4 (15)
TS	FF	sign position - occurs at T1 or TE depending on C1 (S/D bit) (15)
TO	G	T29 of word 107 (ORIGIN PULSE) (15, 57)
TM	FF	TIMING TRACK READ FF; also abbrev. for track (15)
TR	G	abbrev. for TRANSFER (state or signal) (30)